STABILITY CONTROL AND PROTECTION OF POWER SYSTEMS WITH VSC HVDC AND VSC FACTS

by

RUI GUAN

A thesis submitted to
The University of Birmingham
for the degree of
DOCTOR OF PHILOSOPHY

Department of Electronic,
Electrical and Systems Engineering
The University of Birmingham
March 2018

To my parents

ACKNOWLEDGEMENTS

Foremost, I would like to express my deepest gratitude to my supervisor, Prof. Xiao-Ping Zhang. It is his invaluable guidance and devoted support that encourages my pursuit of research achievements. His pioneering foresight and cognition of energy internet has formed the foundation of my research goal. His patient guidance and advanced resources has provided me with the platform to carry out my study. There would be no chance that I can manage to complete this thesis and related academic achievements, without his professionalism and dedication. I am truly privileged to study in his research group.

This Ph.D. study was partly sponsored by Department of Electronic, Electrical and Systems Engineering, School of Engineering, University of Birmingham. I would like to acknowledge my gratitude for the financial support.

I would also like to thank my colleagues Dr. Dechao Kong, Dr. Suyang Zhou, Dr. Jingchao Deng, Dr. Jianing Li, Dr. Puyu Wang, Dr. Na Deng, Dr. Jing Li, Dr. Ying Xue, Dr. Zhi Wu, Dr. Can Li, Dr. Mingyu Xie, Dr. Hao Fu, Dr. Conghuan Yang, Mr. Zuanhong Yan, Mr. Mao Li, Miss Xianxian Zhao, Mr. Jiajie Luo, and Mr. Min Zhao from the Electrical Power and Control Systems Group for their kind advices and inspiring discussions. It has been a beneficial experience to work with them over the past three years.

Last but not least, I would like to thank my beloved parents, Mr Jun Guan and Mrs. Cuili Shang and all of my family members. I am deeply grateful for their devotion and support through my whole research period. They have made me who I am.

ABSTRACT

The recent progress of high-voltage high-power fully controlled semiconductor technology laid the foundation of voltage source converter (VSC) technology, which continues to advance the developments of high voltage direct current (HVDC) technology and flexible alternating current transmission systems (FACTS). Nowadays, due to the ever increasing amount of the integration of renewable energy sources into power systems and the demand of long-distance bulk power transmission with enhanced power system controllability and increased power transfer capability, VSC converter based technology (in particular, VSC HVDC and VSC FACTS) has been applied as a crucial solution to these big challenges. However, the high penetration of these VSC based systems may introduce certain risks to existing power systems in two primary aspects: dynamic stability and protection. This thesis investigates the impacts of VSC HVDC and VSC FACTS on system dynamic stability and protection.

VSC based HVDC system is the preferred solution for grid connection of large-scale offshore wind farms, as it is a feasible option for long distance submarine interconnection of passive and weak systems. With increasing installations of VSC HVDC systems in power grids, the investigation of controllability and stability of VSC-based multi-terminal direct current (MTDC) systems becomes important as it benefits the existing AC systems with a means of increased energy transfer between interconnected system operators. However, for VSC-based MTDC systems, the current flow control of DC grid has become a challenge, with more installed and planned applications of multi-terminal HVDC transmission systems. The DC current flow controller (CFC) is a DC-DC converter based power flow control solution which can provide multi-line flexible current flow control in a simple meshed DC network. Small-signal stability analysis has been widely used for the study of system dynamics and design of controllers for VSC converters. However, the most of the published research papers on small-signal stability of VSC MTDC systems have mainly been focused on the dynamics of the VSC while there is a lack of considerations of the potential impacts of DC power-flow controller on existing MTDC systems in terms of system stability and dynamic performance under disturbances. And there is a real need to fill in the gap of the study of interactions between DC networks with CFC and VSC converters (even more broadly, the detailed representation of connected AC networks). In this thesis, an integrated small-signal stability

model for the study of interactions between CFC and VSC is established. Modal analysis results are verified by simulation results from real time digital simulations (RTDS) under both small and large AC/DC disturbances. The impacts of control parameters of CFC on the integrated AC/DC system and the interactions between VSC and CFC are investigated using both modal analysis and time-domain simulations.

The emerging VSC FACTS devices are commonly regarded as an effective solution for fast-response voltage/reactive power support during normal and fault conditions. However, the implementation of VSC FACTS (for instance, STATCOM) and VSC HVDC in high voltage transmission systems may introduce certain potential risks or impacts to the existing protection and control systems. Unexpected changes of the impedance measurements due to the integration of VSC-FACTS and VSC HVDC may trigger mal-operation of feeder distance protection of AC systems, since the performance of feeder distance protection is heavily dependent on the impedance measurements. The mathematical representation of the apparent impedance measurement of distance relay is derived considering the infeed current from VSC HVDC and VSC FACTS at different locations. The apparent impedance measurements analysis and dynamic simulation study are performed to investigate the impacts of VSC HVDC and VSC FACTS on distance protection. A RTDS-based hardware-in-loop testing platform is established using practical distance relays and detailed model of VSC HVDC and multiple VSC FACTS. The impacts of VSC HVDC and VSC FACTS on feeder distance protection are investigated, based on different types of internal/external fault test simulation occurred at various locations.

In this thesis, a small-signal stability model of the integrated AC/DC systems with VSC and CFC is presented to characterize modes and investigate various control parameters of CFC on the eigenvalue trajectories of system modes. Small-signal stability analysis is performed to investigate the interactions between CFC and VSC. The mathematical representation of the apparent impedance measurements of feeder distance relays against various fault scenarios is derived considering the infeed current from VSC HVDC and VSC FACTS at different locations.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

CB	Circuit Breaker
CFC	Current Flow Controller
CT	Current Transformer
DPFC	Distributed Power Flow Controller
EHV	Extra High Voltage
FACTS	Flexible Alternating Current Transmission Systems
HIL	Hardware in Loop
HV	High Voltage
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LCC	Line Commutated Converter
MMC	Modular Multilevel Converter
MSC	Mechanically Switched Capacitor
MTDC	Multi-Terminal HVDC
PCC	Point of Common Coupling
PLL	Phase Locked Loop
PSS	Power System Stabilizer
PWM	Pulse Width Modulation
RTDS	Real-Time Digital Simulator
SLD	Single Line Diagram

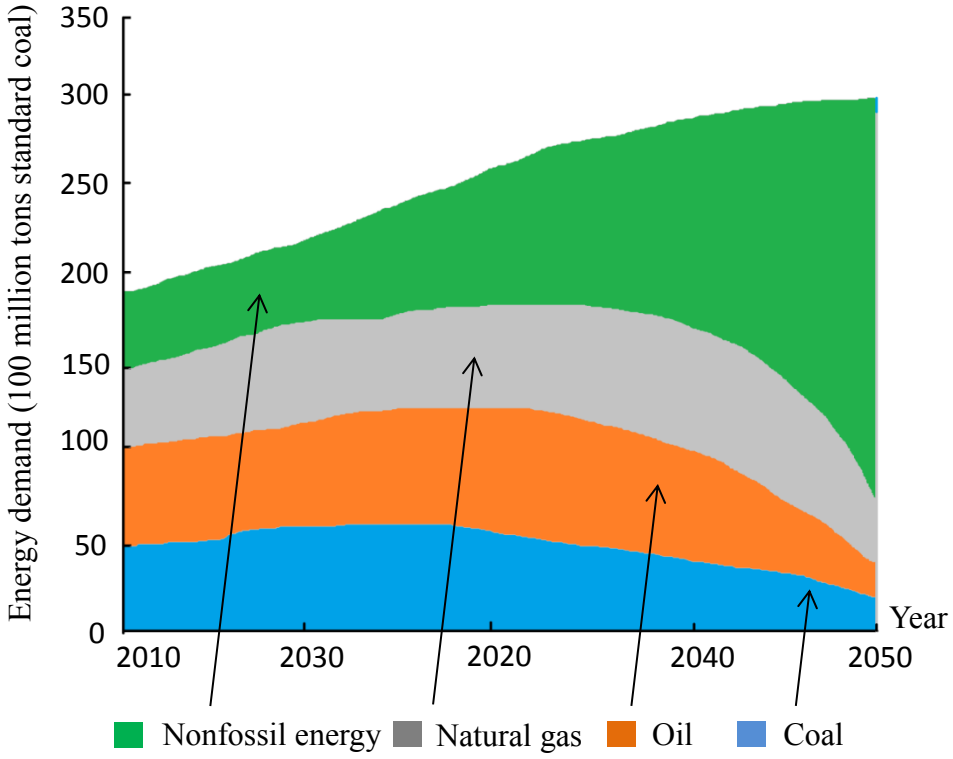
SLG	Single Line to Ground
SM	Sub-Module
SSSC	Static Synchronous Series Compensator
STATCOM	Static Synchronous Compensator
SVC	Static VAR Compensator
TCR	Thyristor Controlled Reactor
TCSC	Thyristor Controlled Series Compensator
TSC	Thristor Switched Capacitor
UPFC	Unified Power Flow Controller
VSC	Voltage Source Converter
VT	Voltage Transformer

CHAPTER 1 INTRODUCTION

1.1 Research Background

1.1.1 VSC HVDC

The debates on most preferred technology for major electricity transmission via AC or DC have been on since later 19th century. Three-phase AC has been widely used for that it can be easier transformed to high voltages than DC and can produce rotating fields for rotating machines[1-2]. However, due to the ever increasing amount of the integration of renewable energy sources into power systems and the demand of long-distance bulk power transmission, high voltage direct current (HVDC) technology has been applied as a solution to these big challenges [3-4].



Global demand for different forms of primary energy, 2010 - 2050

Figure 1- 1 Global demand for different forms of primary energy (2010 – 2050) [5].

The widespread use of HVDC transmission is in the following areas [6]:

1. Underground and underwater cable transmission. The installed cable costs and cost of losses using HVDC transmission is considerably less than using AC cable transmission. This is due to long-distance (longer than 30 km) AC cables are capacitive and require intermediate compensation. On the contrary, DC cables do not need reactive power compensation. Hence there is no physical restriction that limits the distance or power level for HVDC underground or underwater cable transmission.
2. Long-distance bulk power transmission. HVDC transmission systems provide a competitive and economical alternative to AC transmission for large amounts of power over long distances (longer than 600 km) by overhead line from remote resources. Unlike long-distance AC overhead line transmission, HVDC transmission does not requires additional reactive power compensation devices caused by line inductances. The cost of transmission line of DC transmission is also less than AC transmission. Although the cost of converter station is higher than AC substations, the per km distance cost of HVDC transmission is lower. The typical break-even distance of application of HVDC transmission is about 600 km.
3. Asynchronous interconnection between AC systems. By use of HVDC transmission, interconnections between asynchronous AC systems can be achieved where AC ties are not feasible due to system stability problems or different frequencies.

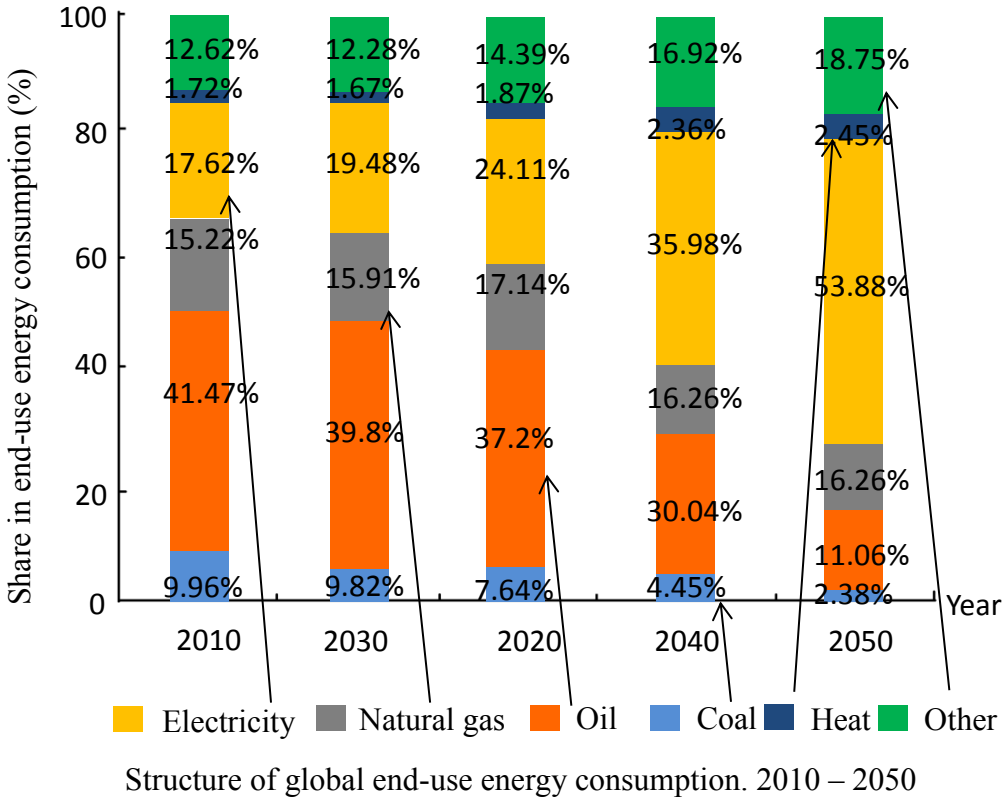


Figure 1- 2 Structure of global end-use energy consumption (2010 – 2050) [5].

The recent progress of high-voltage high-power fully controlled semiconductor technology continues to advance the developments of HVDC technology [7-9]. The emerging fully controlled semiconductor devices, for instance Insulated-Gate Bipolar Transistor (IGBT), are used by Voltage Source Converter (VSC) HVDC systems [10-11]. The IGBT is self-commuted via gate pulse, which can be turned on and turned off without relying on line voltage. On the contrary to thyristor valves used by conventional line commutated converter (LCC) HVDC technology [12], the self-commutated characteristic of IGBT valves makes it possible for VSC HVDC technology to control active and reactive power independently [13-18]. Since VSC HVDC technology requires no reactive power compensation and fewer AC filters, it is a more economical alternative to conventional HVDC technology when connecting to weak or passive AC network [19-24]. And VSC HVDC uses smaller footprint because of reduced reactive power compensation and filter requirements [25-29].

In attempt to achieve environment protection goal, the European Community has announced the focus on an increase in installed wind power capacity up to the level of 300 GW by 2030 among Europe [30-31]. The application of wind energy and especially offshore wind energy in the North Sea is going to make up the major planned installations of 150 GW [32-35]. As a

more attractive alternative to AC link and LCC HVDC transmission, VSC HVDC transmission has advantages over AC link and LCC HVDC transmission in following aspects [36-38]:

1. VSC HVDC requires no external voltage source for commutation and less auxiliary AC filters, which makes VSC HVDC uses smaller footprint for offshore installation.
2. The reactive power control is independent of active power control at each terminal using VSC HVDC, which enables voltage regulation and connection to weak or passive AC network.
3. Power flow reversal can be achieved by reverse of direction of DC current.
4. The DC transmission line costs and cable power losses are lower than AC cable transmission.

Table 1- 1 Typical power ratings of three power electronic components

Power Electronic Components	Thyristor	GTO	IGBT/IGCT
Switching Frequency	50/60 Hz	<500 Hz	>1000 Hz
Losses	1-2%		2-4%

It should also be pointed out that the switching losses of VSC HVDC caused by high switching frequency of semiconductors are higher than that of LCC HVDC [39]. Another challenging issue of VSC HVDC is the lower power rating of converter caused by the fact that the power rating of IGBT is less than that of thyristor [40]. This results in high cost of converters. As the typical parameters of thristor, GTO and IGBT/IGCT shown in Table 1- 1, the switching frequency of IGBT is higher than that of thyristor and the losses of IGBT are higher than that of thyristor.

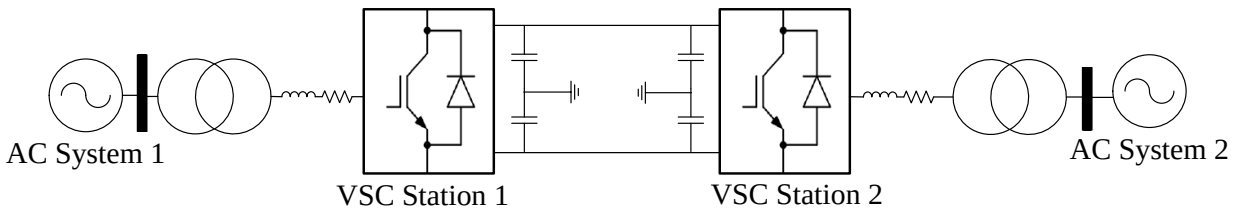


Figure 1- 3 Configuration of VSC HVDC.

As shown in Figure 1- 3, the basic configuration of VSC HVDC system comprises of two VSC converter stations (VSC Station 1 and VSC Station 2). Figure 1- 4 shows the topology of a basic two-level three-phase bridge inside of VSC stations. The IGBT with antiparallel diode is used to form a valve. The DC bus capacitors store energy and filter DC harmonics. Other topologies of VSC with different level of voltage are also used. Figure 1- 5 shows the topology of a three-level VSC, which is a commonly used topology of multilevel VSC [41]. The converter output voltage is created by pulse width modulation (PWM) technique. Figure 1- 6 shows the basic waveforms associated with PWM and line-to-neutral voltage waveform of a two-level converter. The VSC converter is connected via a reactor to the AC system at the point of common coupling (PCC). AC filters are used on the AC side to reduce harmonics content.

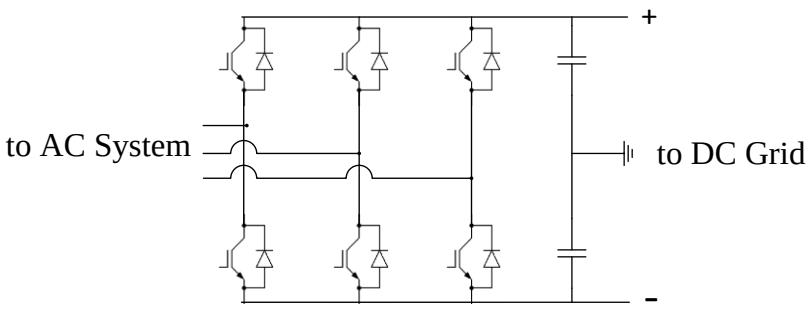


Figure 1- 4 Topology of a two-level three-phase bridge inside VSC.

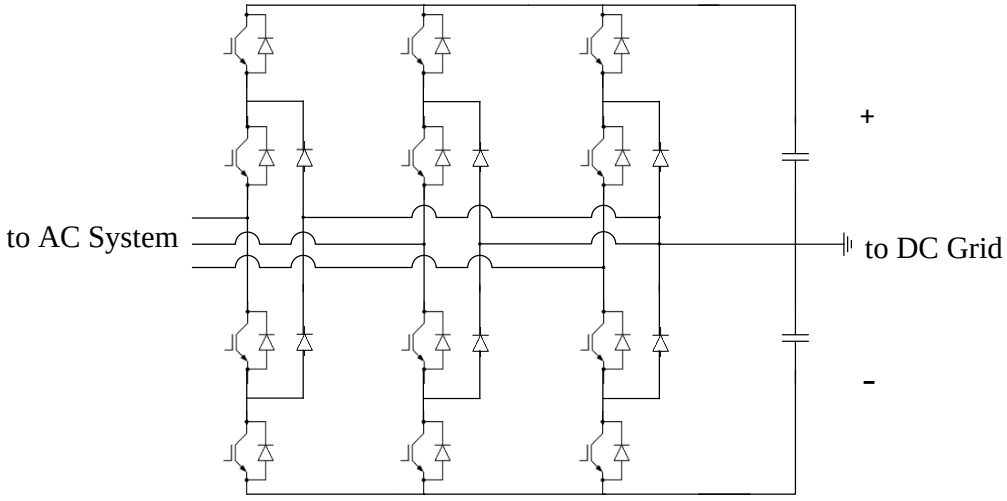


Figure 1- 5 Topology of a three-level VSC.

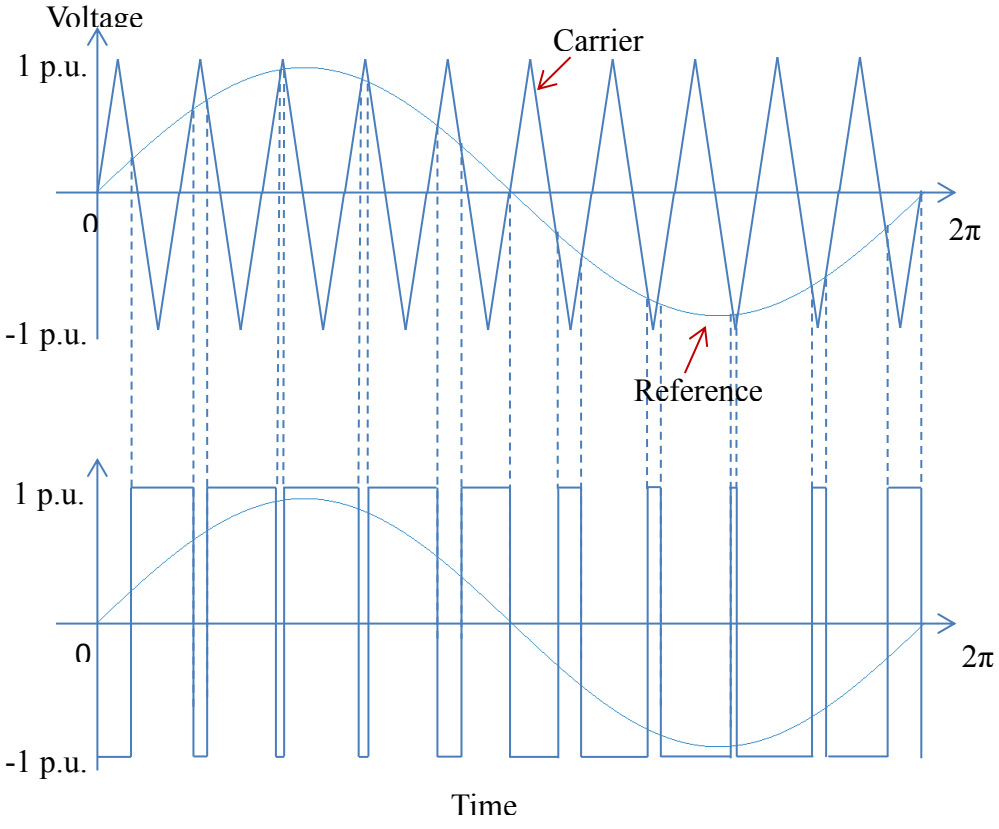


Figure 1- 6 Waveforms associated with PWM and voltage of a two-level converter.

The modular multilevel converter (MMC) has been recognized as an attractive multilevel converter topology for medium/ high power applications [42-49]. As shown in Figure 1- 7, the whole converter consists of a selected number of identical submodules (SM_1 to SM_n) in each arm. As a typical configuration of half-bridge SM (SM_k) shown in Figure 1- 8, each SM

comprise of two IGBTs with antiparallel diodes (S_1 and S_2) and a DC storage capacitor, which can operate in switched-on(unit DC storage capacitor voltage V_c) or switched-off/bypassed(zero voltage) state. There are two arms in each phase-leg of MMC, where each arm comprises of a selected number of series SMs. The SMs in each arm are controlled to generate required AC voltage. The different principles that reflects how converter voltage is created of two-level VSC, three-level VSC and MMC [47-50] are presented in Figure 1- 9.

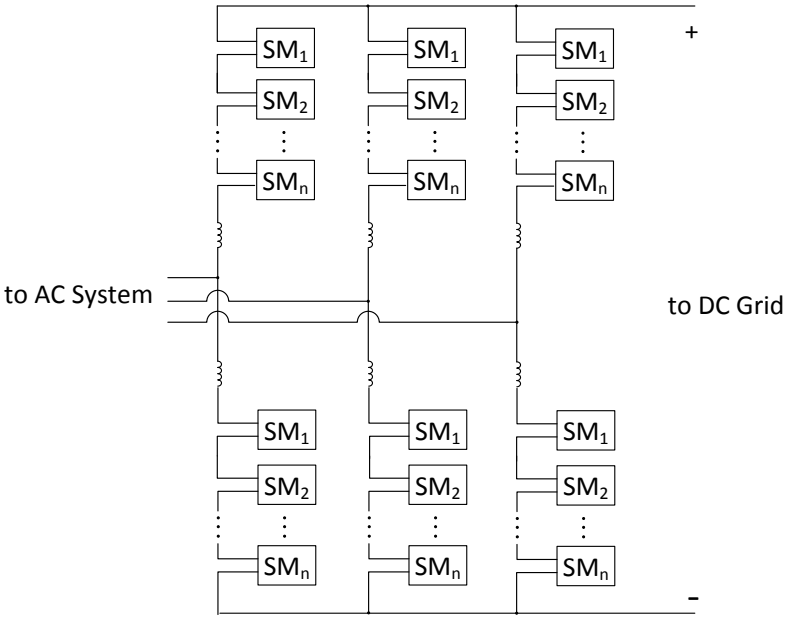


Figure 1- 7 Topology of a MMC.

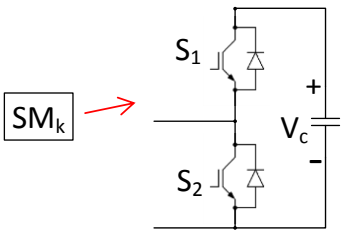


Figure 1- 8 Configuration of a half-bridge SM.

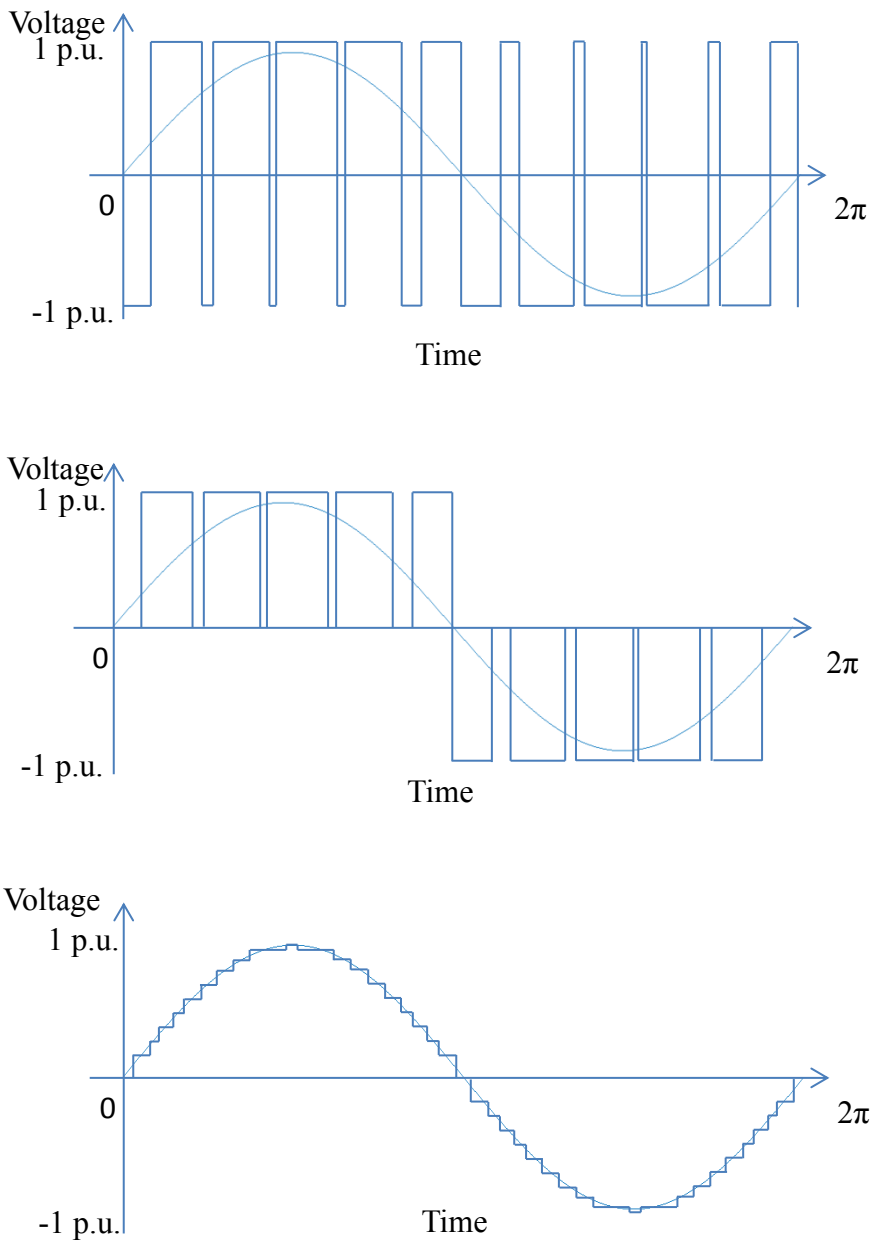


Figure 1- 9 Converter voltage creation of two-level VSC, three-level VSC and MMC.

In comparison with two-level, three-level and other multilevel converter topologies, the MMC has following advantages [51-55]:

1. The voltage generation is modular and scalar that can meets different voltage level requirements.
2. The efficiency of MMC is higher than that of the other VSC topologies for high-power applications due to the low stitching frequency of submodules.
3. The harmonics of MMC are greatly reduced in high-voltage applications due to the stack of a large number of SMs with low-voltage rating.
4. The use of DC side capacitor is avoided.

It should also be pointed out that there are inevitable drawbacks of the applications of MMC as follows:

1. More complex topology of converter and extra controller submodule voltage balance control are required.
2. Unsuppressed circulating current due to voltage variation of submodules on each phase can cause increased device losses.

Table 1- 2 shows the major applications of VSC HVDC systems.

Table 1- 2 Major applications of VSC HVDC systems [2]

Project	Country	Year	Topology	Power	DC Voltage
Hallsjon	Sweden	1997	2-level	3 MW	± 10 kV
Gotland	Sweden	1999	2-level	50 MW	± 80 kV
Eagle Pass	USA	2000	3-level	36 MW	± 16 kV
Terranora	Australia	2000	2-level	180 MW	± 80 kV
Cross Sound	USA	2002	3-level	330 MW	± 150 kV
Estlink	Finland	2006	2-level	350 MW	± 150 kV
Trans Bay Cable	USA	2010	MMC	400 MW	± 200 kV
Zhoushan	China	2014	MMC	1 GW	± 200 kV
DolWin3	Germany	2017	MMC	900 MW	± 320 kV

1.1.2 VSC FACTS

Along with the developments of VSC HVDC, VSC flexible alternating current system (FACTS) also continue to advance in recent decades as a power electronic based system to enhance power system controllability and increase power transfer capability [56-59]. On the contrary to the conventional thyristor based reactive power compensator (such as SVC, TCSC, and TCSR), VSC FACTS (such as STATCOM, SSSC and UPFC) are built upon self-commutating controllable switches (such as GTO and IGBT) [60-63]. The FACTS systems are applied to power systems for reactive power compensation, bus voltage regulation, power flow control, power quality improvement, and system stability enhancement [64-66]. The classification of major FACTS devices are shown in Table 1- 3.

Table 1- 3 Classifications of major FACTS devices

	Thyristor-valve based	VSC based
Series	TCSR, and TCSC	SSSC
Shunt	SVC (TCR, TSC and MSC)	STATCOM
Series-shunt	DPFC	UPFC

Static synchronous compensator (STATCOM) is a promising shunt connected FACTS, which generates three-phase balanced output voltage at fundamental frequency with rapidly controllable amplitude and phase angle [67-69]. STATCOM is used as a typical example of shunt VSC FACTS to study stability, control and protection of VSC FACTS in this thesis. A STATCOM can provide the connected power system with reactive power control or bus voltage regulation support at PCC. The major advantages of STACOM compared to thyristor based FACTS are quick response time, optimum voltage waveform, smaller footprint requirement, and higher operational flexibility [60,70-71]. Figure 1- 10 shows a basic configuration of a two-level star-connection STATCOM.

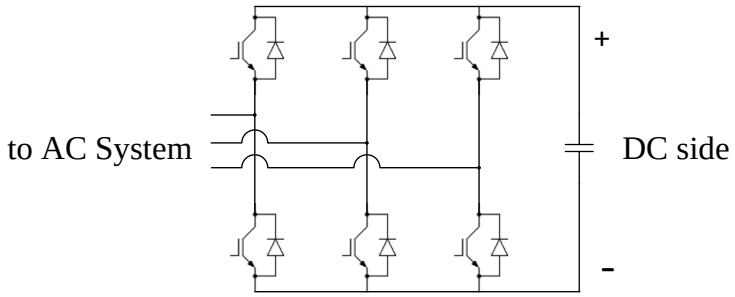


Figure 1- 10 Configuration of a two-level star-connection STATCOM.

1.1.3 CFC in MTDC

The major established applications of HVDC interconnections are using two-terminal point-to-point or back-to-back configuration [2]. However, with more and more installed and planned applications of multi-terminal HVDC transmission systems, the current flow control of DC grid has become a challenge [72-75].

In DC grids with no DC power flow control, the DC currents are flowing from one node to another through the path of least resistance. This may result in the situation where one or more DC branches are overloaded. In a multi-terminal VSC based DC grid, the DC voltage level is usually regulated by one VSC converter station, whilst other converter stations control active power of connected DC branch [76-80]. In this way, the DC power flow can be controlled by VSC converter stations in a DC grid with a simple radial topology. However, for a DC grid with more complex meshed topology, additional meshed DC transmission lines

or DC cables may be used. In consequence, such DC power flow control by use of only converter stations is not feasible because the number of DC branch exceeds the number of converter station. New DC power flow control methods or devices are required.

There are three approaches for controlling DC power flow as follows:

1. Variable Series Resistor.
2. Series Voltage Source.
3. DC-DC Converter.

The principle of controlling DC power flow by use of variable series resistor is to insert a number of additional resistors in series with a DC transmission line. Each resistor is controlled by mechanical or electronic based switch to be embedded into DC line in series or to be bypassed. In this way, the total amount of additional resistance can be controlled by switching on or switching off these switches. The impedance of DC network is changed by insertion of variable series resistors and the DC power flow is changed in consequence.

The disadvantage of this approach is that the standing power losses due to the additional resistance is significant compared with the overall cable losses [72-73,81-83]. And the cost of additional cooling equipment is required for power electronic based switching devices.

The principle of controlling DC power flow by use of series voltage source is to insert controlled voltage source in series with a DC line to vary the voltage in the embedded branch. The DC power flow of series voltage source integrated can be controlled by controlling the magnitude and polarity of inserted voltage source. The voltage source can be regarded as a power sink (when it absorb power to the DC branch) or a power source (when it provide power to the DC branch), depending on the polarity. The practical implementation of the series voltage source is achieved by thyristor, or IGBT based AC/DC converter.

The disadvantage of this approach is the cost of these additional AC/DC converters and their power losses [72-73,82]. And the power rating of the voltage source is relatively small compared to the DC network.

As for controlling DC power flow by use of DC-DC converters, DC current flow controller (CFC) is a DC-DC converter based device which can provide multi-line flexible current flow control in a simple meshed DC network. Figure 1- 11 shows the topology of a two-line CFC. By control of DC-DC converter, CFC is capable of controlling current flow of the connected

DC branches. The power can be transferred from one connected DC branch to another (for instance, power can be transferred from DC branch 12 to DC branch 13).

The advantage of CFC is that it uses smaller footprint and has lower cost since the power is transferred between DC branches rather than dissipated or flew out of DC network [84-86]. However, the major disadvantage of the application of CFC is the cost of additional DC-DC converters.

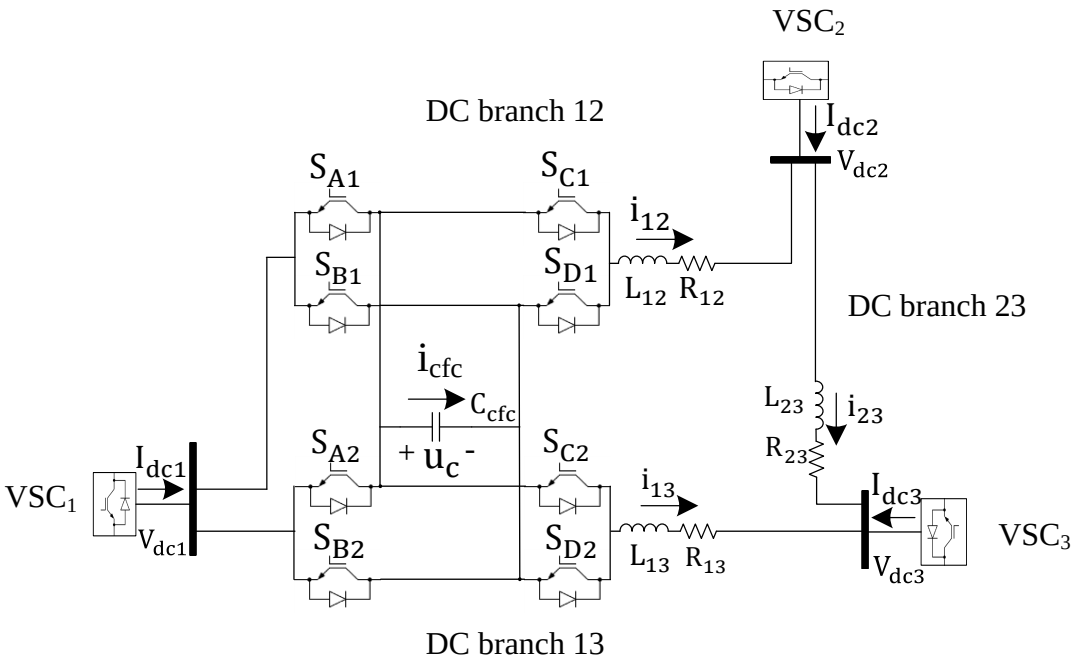


Figure 1- 11 Topology of a two-line CFC.

1.1.4 Distance Protection

Distance protection is a typical non-unit system of protection, in order to protect designated areas, which are also known as protection zones [87-90]. The performance of distance protection is heavily dependent on the impedance measurements, which results in potential risks of mal-operation of distance relays, due to unexpected changes of impedance measurement caused by the implementation of VSC FACTS (for instance, STATCOM) and VSC HVDC. Figure 1- 12 shows the single-line diagram of distance protection. Distance relays use measurements of line voltage and line current from protected area to calculate the apparent impedance. The impedance of high voltage and extra high voltage transmission lines is usually proportional to the line length. In consequence, it is possible to determine if a fault

occurs in the protection zone or out of protection zone by comparing the calculated impedance to the protected line impedance [91-96].

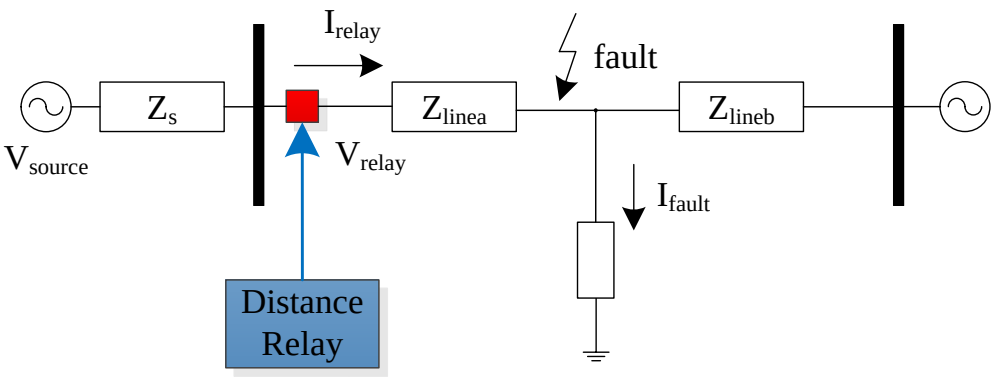


Figure 1- 12 Single-line diagram of distance protection.

Distance protection is considered to be simple to apply and fast in operation for faults located along most of a protected circuit. It is suitable for application with high-speed auto-reclosing [97-99]. The measured apparent impedance by distance relay is independent of the source impedance.

Distance relays are designed to operate only when faults occurred are within the protection zone, which is the protection range between the relay location and the selected reach point. The calculated apparent impedance is compared with the reach point impedance. If the calculated apparent impedance is less than the reach point impedance, it is assumed that a fault occurred on the line between the relay and the reach point. The distance relay operates and sends signals to related circuit breakers (CB) and circuit breakers trip. If the calculated apparent impedance is greater than the reach point impedance, it is assumed that no fault occurred on the line between the relay and the reach point. Once the settings of a distance relay are determined, the protection is relatively unaffected by changes in the power systems [100-101].

The reach point of a distance relay is a certain point along the line impedance locus which indicates the boundary of protection. The reach point can be plotted on an R/X diagram since it is dependent on the ratio of voltage and current and phase angle between them.

The major advantages of distance protection are as follows [87,92-93]:

1. High-speed of operation.
2. Ability to protect independent of communication services.

And the major disadvantages of distance protection are considered to be as follows [92-93,95]:

1. Need of both CTs (current transformer) and VTs (voltage transformer).
2. Limited resistive fault coverage.

1.2 Literature Review

1.2.1 Modelling and Control of VSC HVDC and VSC FACTS

dq decoupled control, which is also known as vector control, is the most commonly used control strategy of VSC converters, compared to the conventional "voltage margin method" presented in [7] and the other control methods of output voltage magnitude and phase angle used in [8,9,13,41]. VSC HVDC systems use *dq* decoupled control to achieve independent control of active power and reactive power [102-103]. As *dq* decoupled control presented in [10-11,17], active power or DC voltage is controlled in *d* axis, while reactive power or AC voltage is controlled in *q* axis. Figure 1- 13 shows the architecture of a typical *dq* decoupled control system. The advantage of using *dq* decoupled control is that the independent control of active power or DC voltage in *d* axis and reactive power AC voltage can be achieved while the conventional control of converter output voltage magnitude and phase angle can not. *dq* decoupled control is also widely used for VSC HVDC system connections of offshore wind farms and VSC FACTS compensation, as deeper penetration of distributed resources into modern power systems [23,28,35]. Novel control strategies of VSC converters are also emerged as alternatives to meet various control purposes such as power synchronization control in [14-16,18] for avoidance of instability caused by a standard phase-locked loop in a weak AC-system connection , and impedance based resonance control in [14] by use of resonance stability analysis.

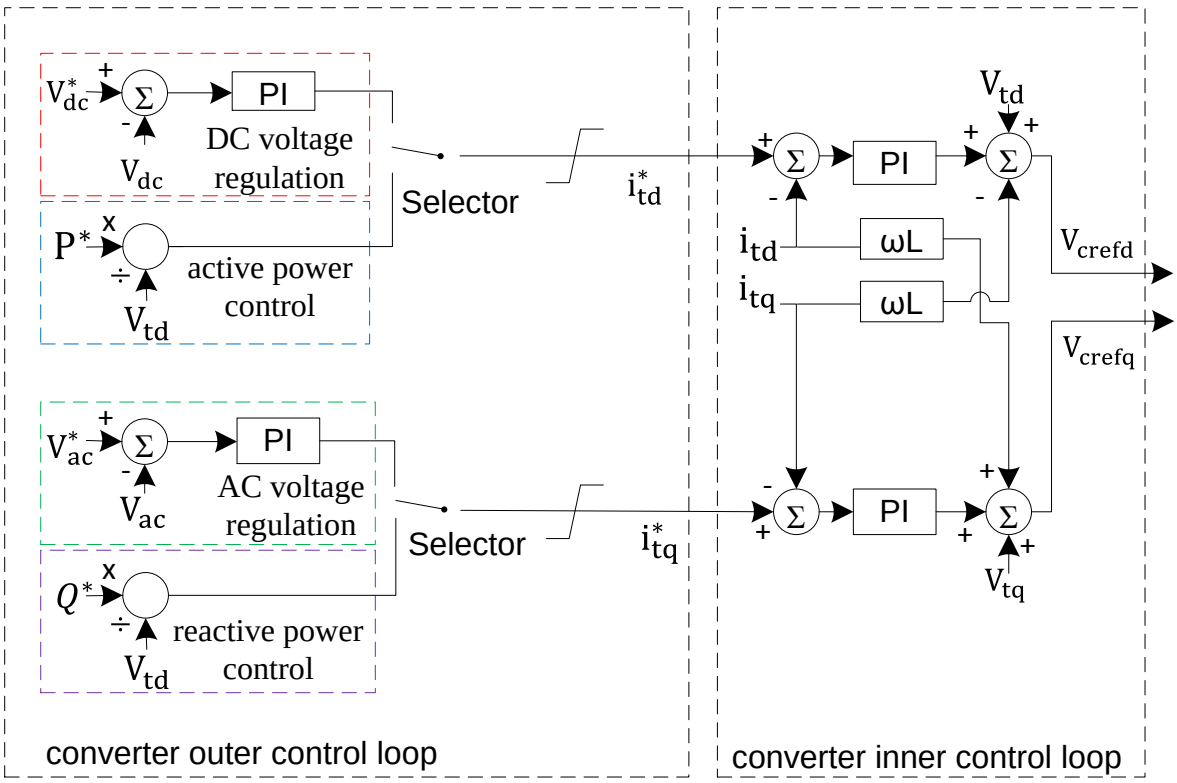


Figure 1- 13 Architecture of dq decoupled control.

For MMC based VSC HVDC systems, the major control strategies mentioned above can be extended to application of MMC, since MMC is essentially a new topology of VSC. As two-terminal back-to-back MMC HVDC system presented in [46] and two terminal point-to-point MMC HVDC system presented in [49], *dq* decoupled control is applied. The general control strategy of two-terminal VSC HVDC system (including MMC HVDC system) using *dq* decoupled control is that one VSC terminal regulates DC voltage level and AC voltage at its PCC while the other VSC terminal control active power transfer through the HVDC link and AC voltage at its PCC [44]. The major difference of control systems between MMC and VSC is that the control block of modulation of submodules is necessary for MMC.

For VSC MTDC systems, master-slave control [104] and voltage droop control [34,105-106] are two major control strategies of VSC converters. For the master-slave control, one VSC terminal operates as "master" to regulate DC voltage level of DC network, while the other VSC terminals act as "slave" to control their active power transfer through VSC terminals. For droop control, the control of DC voltage or active power are shared amount all VSC terminals. The advantage of the master-slave control of VSC converters in VSC based MTDC system as presented in [104,107-109], is relatively simple control design since additional droop control loop is not used. However, the drawback of the master-slave control is that the

collapse of DC voltage level may occur, resulting from a severe fault occurred at the master VSC terminal.

The master-slave control is used in this thesis for control of VSC based MTDC system. The mathematical modelling of single VSC converter using *dq* decoupled control is presented in [10-11,17,28], which considers the dynamic characteristic of control system of VSC, and power transfer between AC system and DC network through VSC converter. The mathematical modelling of VSC based MTDC system is presented in [24,26,35], which considers the dynamic characteristic of VSC and DC network.

Static synchronous compensator (STATCOM), or static synchronous condenser (STATCON), is a power electronics VSC based regulating device integrated to AC power transmission system [58,61-62]. As the same with VSC HVDC system, there a number of various topologies of STATCOM in different voltage levels, since the converter of STATCOM is VSC based. These topologies vary in different voltage levels, depending on different application scenarios: two-level converter, three-level converter, or multilevel modular converter [110-112]. As for the connection topologies for converter legs, unlike VSC HVDC system, there are two connections for converter legs of STATCOM, star-connection and delta-connection. The topology of two-level star-connection STATCOM is shown in Figure 1- 10 while the topology of a MMC based delta-connection STATCOM is shown in Figure 1-14.

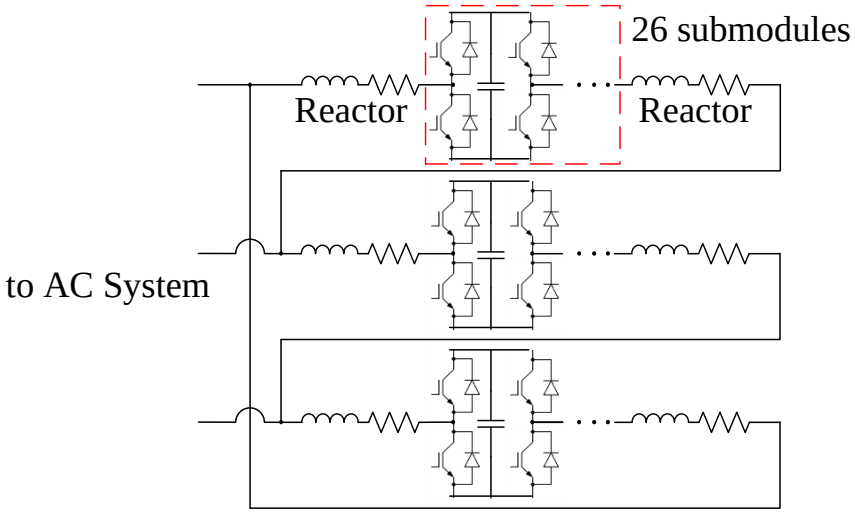


Figure 1- 14 Configuration of a MMC-based delta-connection STATCOM.

The major control strategies of VSC converter can be extended to STATCOM, since STATCOM is based on VSC converter technology. *dq* decoupled control is the most commonly used control strategy of STATCOM, compared to conventional control strategies based on $\alpha\beta$ control (which uses currents in $\alpha\beta 0$ frame instead of $dq0$ frame as controlled variables to generate converter output voltage) presented in [58,63,113]. As *dq* decoupled control of STATCOM presented in [60,64-65,67-71,116-117], AC side voltage at PCC or the reactive power compensated by STATCOM is controlled by use of *q* axis current. And as presented in [60,64-65,67-71,116-117], during normal steady state operation with the active power loss of converter ignored, the generated voltage of STATCOM is in phase with voltage at PCC of connected power system. This means there is no active power flow between STATCOM and connected power system. Only reactive power is transferred. When Q is positive, the STATCOM supplies reactive power to the external ac network. When Q is negative, the STATCOM absorbs reactive power from the external ac network. The amount of reactive power transfer during steady state can be expressed as follows:

$$Q = \frac{V_{c,abc} - V_{t,abc}}{X_c} V_{t,abc} \tag{1. 1}$$

The advantage of using *dq* decoupled control is that the independent control of DC voltage in *d* axis and reactive power/AC voltage in *q* axis can be achieved while the conventional control of converter output voltage can not. This applies to the star-connection VSC based STATCOM. For MMC based delta-connection STATCOM, normally only *q* axis current is used to control reactive power or AC voltage, since there is no DC side energy storage

capacitor of STATCOM [69,115]. As *dq* decoupled control of delta-connection STATCOM presented in [115] and other independent three-phase voltage control presented in [59,119-120], the advantages of using delta-connection STATCOM are lower rated current of switching devices and negative sequence current compensation in unbalanced circuit. MMC converter has also been extended to the application of STATCOM due to its advantages of increased voltage levels of output waveform and reduced switching losses caused by switching frequency [69,121-125]. Control block of modulation of submodules should be added into *dq* decoupled control of MMC based STATCOM [69].

dq decoupled control is used in this study for the control of delta-connection STATCOM. The mathematical modelling of VSC converters using *dq* decoupled control is presented in [60, 64-65,67-71,116-117], which considers the dynamic characteristic of control system of STATCOM, DC voltage across DC energy storage capacitor, and reactive power transfer between AC system and STATCOM.

1.2.2 Small-Signal Stability Analysis of VSC MTDC

With the increasing installations of VSC HVDC systems in power grids, the investigation of controllability and stability of MTDC systems becomes important for it benefits the existing AC systems with a means of increased energy trading between interconnected system operators [126-127]. The generalized dynamic model of VSC MTDC is derived in a number of papers, for instance [11-12,35,77-78,128-143], to investigate dynamic stability of VSC MTDC in different scenarios. Various control strategies of MTDC system including the master-slave DC voltage control, voltage and power droop control, and power synchronization control are presented in [76-80,137,143-145]. Advanced control extensions with distributed DC voltage control were developed in [137], and a supplementary decentralized control structure to damp interarea oscillations was proposed in [76]. Frequency support function for the surrounding interconnected AC systems and adaptive droop control for effective power sharing through MTDC system were presented and analysed in depth in [77,141]. Electromechanical transient modelling of MMC MTDC was studied in [146] to provide the theoretical foundation for future MMC MTDC applications.

Small-signal stability analysis has been widely used for the study of system dynamics and design of controllers for VSC [6,26,147-150]. For VSC-based MTDC system, small-signal stability analysis is used to study if the MTDC system is capable of maintaining synchronism

(in broaden sense) when it is subjected to small disturbances [6,147]. Small-signal stability analysis has been applied in [11,77-78,130-133,135-137,139-142,151-152] to study the impacts of different control strategies, system parameters, and power system devices on system dynamic stability. In [140] the small-signal stability analysis has been carried out for a symmetric bipolar MTDC grid where different modes and interaction between AC systems and VSC following various disturbances were characterized. In [139] small-signal stability analysis was carried out to define the ranges for the gains of VSC controllers that ensure the dynamic stability of MTDC system. Wind farm generators were considered and a method to calculate converter controller gains was provided in [137]. In [141], an adaptive frequency droop control was proposed by investigating the sensitivity of eigenvalues with respect to different droop coefficients, control parameters and changes in operating conditions. In [77], small-signal stability analysis was used for the design of an adaptive droop control scheme. In [132], a method was introduced for systematically identifying interactions of modes in a VSC MTDC system by analysing the participation pattern from different system elements.

Modal analysis is a commonly used approach in small-signal stability analysis to reflect dynamic characteristic of studied systems. It can provide enlightening insights of the essential dynamic behaviour of state variables by use of mathematical analysis of eigenvalue results. Modal analysis is used as the approach to study dynamic response of VSC based MTDC systems against small perturbation in [77,132-133,135, 139-142,151-153]. Eigenvalues of state matrix can be calculated based on dynamic equations of MTDC system in state- space representation, which consists of state variables and inputs. By analysing of the values of eigenvalue results, the time dependent characteristics of modes can be determined, including oscillation type, frequency of oscillation, and damping ratio [11,77,132-133,135, 139-142,151-153].

Eigenvalue trajectory study is a means of modal analysis to reveal impacts of certain parameter of power systems, or control system on eigenvalues [6,11,77,132-133,140,151-153]. The trajectory of varying pole placements of eigenvalues is plotted on a complex plane in response to the changing of certain studied parameter. Eigenvalue trajectory analysis is used in [11,77,132-133,141,151-153] to investigate the impacts of control parameter, system strength, short-circuit ratio, and phase locked loop (PLL) parameters on root locus of test system for the purpose of control system design [11,77,141,153], interactions studies between power system components[132-133,151], and coordination optimization of multi VSC converters [141,152].

Previous publications on small-signal stability analysis of VSC MTDC have been focused on the dynamics of VSC converters while there is a lack of consideration of DC networks with CFC. Hence there is also a lack of analysis on the potential impacts of DC power flow controller on existing MTDC system in terms of network stability and dynamic performance under disturbances. There is a real need to fill in the gap of the interactions between DC networks with CFC and VSC (even more broadly, the detailed representation of connected AC networks).

1.2.3 Impacts of VSC HVDC and VSC FACTS on Distance Protection

The emerging shunt VSC FACTS (for instance, STATCOM) and VSC HVDC technology are commonly regarded as effective solutions for fast-response voltage/reactive power support during normal and faulty conditions [64,67]. In recent years, there has been an increase of STATCOM applications and VSC HVDC integrations in the high voltage (HV) transmission systems around the world [121].

However, the implementations of VSC FACTS and VSC HVDC in the HV transmission systems may introduce certain risks to the existing protection and control (P&C) systems [89,154]. For example, if one or more VSC FACTS (in particular, STATCOM as an example studied in this thesis) or VSC converters are put into service for fast voltage/reactive power control, it may cause unexpected transient changes of impedance [155]. As the performance of feeder distance protection is heavily dependent on the impedance measurements, these unexpected changes of impedance may trigger mal-operation of feeder distance protection. As a result, such risk should be carefully investigated when introducing the VSC FACTS and VSC HVDC into HV transmission system.

In [155], comparative investigation of the performance of various distance protection schemes is presented for transmission lines compensated by shunt connected FACTS devices. In [156], the impacts of VSC based multiline FACTS controllers on distance relays are evaluated. An adaptive distance protection scheme in the presence of STATCOM is presented in [157]. An adaptive distance protection scheme is proposed in [158] to improve the performance of the conventional distance protection scheme for compensated lines with high resistance faults. In [159], a methodology of calculation of fundamental frequency-based per phase digital impedance pilot relaying scheme for STATCOM compensated transmission lines is presented using two end synchronised measurements.

The study of the impacts of HVDC interconnectors on distance protection are mainly focused on the measurement accuracy at the boundary of protection zones [160-161]. A fast full-line tripping distance protection method for HVDC transmission line is proposed in [160] to achieve accurate measurement near protection zone boundary to distinguish internal faults from external faults. The representation of HVDC transmission line is in distributed parameter model to design tripping distance protection method. In [161], the application of distance protection for HVDC transmission lines is considered in frequency-dependent parameter model to enhance the calculation accuracy of fault distance. However, these studies are on distance protection design for DC cable of conventional LCC HVDC link. The impacts of VSC HVDC systems on distance protection are yet to be investigated.

The methodologies of the study of STATCOM's impacts on feeder distance protection can be extended to the study of impacts of VSC HVDC systems on distance protection, since STATCOM and VSC HVDC are both VSC converter based, and the commonly used control strategies of them are same *dq* decoupled control. In [162], a robust distance protection approach is proposed to consider these impacts based on μ synthesis analysis. The apparent impedance measurements of distance relays affected by infeed current from VSC HVDC connected bus are studied in [163-165]. An apparent impedance calculation method considering impacts of VSC HVDC is presented in [164] to identify the possible mal-operations of distance relays in aspects of Zone 2 protection. It should also be noted that the potential interactions between VSC HVDC and STATCOM are analysed in [166-167] to provide some insights of approaches to investigate their interactions.

The major research gaps can be concluded as follows:

1. The previous research on small-signal stability analysis of VSC MTDC have been focused on the dynamics of VSC converters while there is a lack of consideration of DC networks.
2. There is also a lack of studies on the potential impacts of DC power flow controllers on existing MTDC systems in terms of network stability and dynamic performance under disturbances.
3. The previous research on distance protection considering the effects of VSC FACTS are mainly on impacts of SVC or STATCOM only while there has no studies on the combined impacts of VSC FACTS and VSC HVDC under various fault scenarios.

1.3 Research Focuses and Contributions

1.3.1 Research Focuses

The main research focuses of this thesis are:

1. To implement detailed mathematical models of integrated AC/DC system consisting multiple AC synchronous generators, VSC, and CFC.
2. To use modal analysis to characterize modes, via participation factor matrix, of the integrated AC/DC systems without/with CFC and hence investigate the impacts of CFC on the integrated AC/DC system.
3. To validate the small-signal stability analysis results in RTDS by simulating small and large disturbances.
4. To investigate the effects of the control parameters of CFC controller on system stability and interactions between CFC and VSC.
5. To derive the mathematical representations of the apparent impedance measurements of feeder distance relays considering the current infeed from VSC HVDC and VSC FACTS at difference locations.
6. To study the impacts of VSC HVDC and VSC FACTS on distance protections, and validate the results by dynamic simulations in hardware in the loop (HIL) RTDS platform against various fault scenarios.

1.3.2 Scientific Contributions of the Thesis

The main contributions of the work presented in this thesis to fill aforementioned research gaps are summarized as follows:

1. A small-signal stability model of integrated AC/DC systems with VSC and CFC to characterize modes via participation factor matrix and investigate various control parameters on the eigenvalue trajectories of system modes.
2. The investigation of the interactions between CFC and VSC including impacts of control parameters of CFC on VSC and impacts of control parameters of VSC on CFC.
3. The mathematical representations of the apparent impedance measurements of feeder distance relays against various fault scenarios considering the current infeed from VSC HVDC and VSC FACTS at difference locations.

1.4 Outline of the Thesis

The thesis is presented based on both theoretical analysis and time domain simulations in RTDS. The thesis is organized as follows:

Chapter 2: The multi-model system in state-space representation is derived, including synchronous generators with excitation system and power system stabiliser (PSS), network power flow equations, VSC with its control system, and DC network without CFC. The small-signal stability analysis of VSC based MTDC system without CFC is implemented and validated in time domain simulations in RTDS.

Chapter 3: The modelling of DC network with CFC in state-space representation is derived, linearized, and merged into the VSC based MTDC system without CFC presented in Chapter 2 to formulate multi-model system with CFC. The small-signal stability analysis of VSC based MTDC system with CFC is implemented and validated in time domain simulations in RTDS to investigate interactions between CFC and VSC. The interactions between VSC and CFC are investigated by use of eigenvalue trajectory studies.

Chapter 4: The mathematical representation of the apparent impedance measurements of distance relays is derived considering the infeed current from VSC HVDC. Relevant analysis of the apparent impedance measurement representation and dynamic simulation study is performed to investigate the impacts of VSC HVDC systems on distance protection.

Chapter 5: The modelling of MMC based delta-connection STATCOM is presented, including configuration and control system. The mathematical representation of the apparent impedance measurements of distance relays is derived considering the infeed current from VSC FACTS connected busbar. Relevant analysis of the apparent impedance measurement representation and dynamic simulation study is performed to investigate the impacts of VSC FACTS on distance protection.

Chapter 6: The mathematical representation of the apparent impedance measurements of distance relays is derived considering the infeed currents from both VSC HVDC and shunt VSC FACTS at different locations. Relevant analysis of the apparent impedance measurement representation and dynamic simulation study is performed to investigate the impacts of VSC HVDC and VSC FACTS on distance protection.

Chapter 7: This chapter concludes the thesis and list possible promising future works that could be done.

The thesis can be divided into four parts as follows, to illustrate the overall structure:

1. Part 1, i.e. Chapter 1, presents the research background, literature review, research contributions, and outline of the thesis
2. Part 2 consists of Chapter 2 and Chapter 3, which study small-signal stability of VSC MTDC system. The small-signal stability analysis of VSC MTDC system without CFC is conducted in Chapter 2. Based on achievements in Chapter 2, Chapter 3 incorporates CFC into the VSC MTDC system established in Chapter 2 and investigates the interactions between VSC and CFC by use of modal analysis in Chapter 3.
3. Part 3 consists of Chapter 4, Chapter 5, and Chapter 6, which study the impacts of VSC HVDC and VSC FACTS on existing distance protection. Chapter 4 investigates the impacts of VSC HVDC on distance protection. Chapter 5 investigates the impacts of VSC FACTS on distance protection. Chapter 6 considers VSC HVDC and multiple VSC FACTS integrated to system simultaneously and their corporate impacts on distance protection under different fault scenarios.
4. Part 4, i.e. Chapter 7, presents the conclusions and future work of the thesis.

Part 2 and Part 3 present the major technical contributions of the thesis, which present the impacts of the integration of VSC HVDC and VSC FACTS on dynamic stability and protection issues of connected systems.

CHAPTER 2 SMALL-SIGNAL STABILITY ANALYSIS OF VSC BASED MTDC SYSTEM WITHOUT DC CFC

2.1 Introduction

This chapter presents the dynamic modelling of the integrated MTDC/AC system without integration of CFC to study the small-signal stability of VSC-based MTDC system. In 2.2, the modelling of AC power system is presented in dynamic equations, including synchronous generator with excitation system and PSS. The network power flow equations are also presented to reflect mathematical relationships between busbars of AC network in algebraic equations. In 2.3, the modelling of MTDC system without CFC is presented in dynamic equations, including VSC with its control system and generalized DC network without CFC. Multiple VSC converters are applied to link meshed DC network and AC systems. Aggregated parameter model of R-L based DC transmission lines is considered for the representation of DC network. In 2.4, AC power system and MTDC system without CFC are linearized around equilibrium point to derive their small-signal state-space model of subsystems. Then the state-space models of subsystems of AC power system and MTDC system are formulated by substitution of the network power flow algebraic equations. In 2.5, a test system that consists of multiple synchronous generators with excitation system and PSS, multiple VSC converters, and DC network without CFC, is established to study its small-signal stability. Small-signal model of test system is derived based on sub-models from 2.2-2.4 and the eigenvalues of state-space representation of the test system are calculated. Modal analysis of the eigenvalues results is performed to study small-signal stability of VSC based MTDC system without CFC. In 2.6, simulations results of established AC/DC system against small disturbances and large disturbances (including AC system faults, and DC cable faults) in RTDS/RSCAD are analysed to validate modal analysis results.

2.2 Modelling of AC Power System

VSC HVDC systems and VSC-based MTDC systems are applied to power systems for bulk power transmission. The AC power system dynamics are modelled in aspects of two major parts: synchronous generators (including excitation system and PSS) and the power network.

2.2.1 Synchronous Generator with Excitation System and PSS

Synchronous generators are still the majority source of commercial electrical energy [6]. They are commonly used in power generation to convert mechanical power into electrical power for the grid. There has been a significant number of literature on synchronous machines in a variety of complexity levels from second-order classic swing model to a detailed model in the order of up to eight [6, 148-150]. A 6th-order generator model is selected in this thesis so that the modelling of the synchronous generator is considered to be sufficient to reflect the transient and sub-transient dynamic characteristic of synchronous machines [149]. The state variables $\boldsymbol{x_i}$ of the 6th-order generator model are as follows:

$$\mathrm{x_i} = \left[\delta_\mathrm{i}, \omega_\mathrm{i}, \mathrm{E'_{qi}}, \mathrm{E'_{di}}, \varphi_{1\mathrm{di}}, \varphi_{2\mathrm{qi}}\right]^\mathrm{T} \tag{2. 1}$$

for $i = 1, 2, \ldots, m$, where

i : index number of synchronous generator

m : total number of synchronous generators

δ_i : rotor angle of synchronous generator

ω_i : rotor angular velocity of synchronous generator

E'_{qi} : transient electromagnetic force caused by field flux linkage in q-axis

E'_{di} : transient electromagnetic force caused by field flux linkage in d-axis

φ_{1di} : subtransient electromagnetic force caused by field flux linkage in d-axis

φ_{2qi} : subtransient electromagnetic force caused by field flux linkage in q-axis

Then the differential equations representing the subtransient dynamic behaviour of the synchronous generators i is given by:

$$\dot{\delta}_\mathrm{i} = \omega_\mathrm{i} - \omega_\mathrm{s} \tag{2. 2}$$

$$\dot{\omega}_i = \frac{1}{M_i}\left[T_{Mi} - D_i(\omega_i - \omega_s) + (X''_{di} - X''_{qi})I_{di}I_{qi} - \frac{(X''_{di} - X_{Li})}{(X'_{di} - X_{Li})}I_{qi}E'_{qi} - \frac{(X'_{di} - X''_{di})}{(X'_{di} - X_{Li})}I_{qi}\varphi_{1di}\right.$$

$$-\frac{\left(X''_{qi}-X_{Li}\right)}{\left(X'_{qi}-X_{Li}\right)}I_{di}E'_{di}+\frac{(X'_{qi}-X''_{qi})}{\left(X'_{qi}-X_{Li}\right)}I_{di}\varphi_{2qi}\ ] \quad (2.\ 3)$$

$$\dot{E}'_{qi}=\frac{1}{T'_{doi}}[-E'_{qi}+(X_{di}-X'_{di})(I_{di}-\frac{(X'_{di}-X''_{di})}{(X'_{di}-X_{Li})^2}[\varphi_{1di}+(X'_{di}-X_{Li})I_{di}-E'_{qi}]+E_{fdi})] \quad (2.\ 4)$$

$$\dot{E}'_{di}=\frac{1}{T'_{qoi}}[-E'_{di}+(X_{qi}-X'_{qi})(I_{qi}-\frac{\left(X'_{qi}-X''_{qi}\right)}{\left(X'_{qi}-X_{Li}\right)^2}[\varphi_{2qi}+\left(X'_{qi}-X_{Li}\right)I_{qi}+E'_{di}])] \quad (2.\ 5)$$

$$\dot{\varphi}_{1di}=\frac{1}{T''_{doi}}[-\varphi_{1di}+E'_{qi}-(X'_{di}-X_{Li})I_{di}] \quad (2.\ 6)$$

$$\dot{\varphi}_{2qi}=\frac{1}{T''_{qoi}}[-\varphi_{2qi}-E'_{di}-\left(X'_{qi}-X_{Li}\right)I_{qi}] \quad (2.\ 7)$$

for i = 1, 2, …, m, where

ω_s : rated rotor angular velocity of synchronous generator

M_i : shaft inertial constant of synchronous generator

D_i : synchronous mechanical damping constant of synchronous generator

T_{Mi} : mechanical torque input

T'_{doi}, T''_{doi} : open circuit transient and subtransient time constant in d-axis, respectively

T'_{qoi}, T''_{qoi} : open circuit transient and subtransient time constant in q-axis, respectively

X_{Li} : armature leakage reactance

$X_{di}, X'_{di}, X''_{di}$: synchronous, transient and subtransient reactance in d-axis, respectively

$X_{qi}, X'_{qi}, X''_{qi}$: synchronous, transient and subtransient reactance in q-axis, respectively

E_{fdi} : field voltage

I_{di} : stator current in d-axis

I_{qi} : stator current in q-axis

For stability studies, the dynamics of synchronous generator terminal voltage is much slower, compared to the dynamics of stator. Hence, the representation of synchronous generator

terminal voltage is given in algebraic equations rather than state equations. The algebraic equations of generator terminal voltage are as follows:

$$V_i \sin(\delta_i - \theta_i) - \frac{(X''_{qi} - X_{Li})}{(X'_{qi} - X_{Li})} E'_{di} + \frac{(X'_{qi} - X''_{qi})}{(X'_{qi} - X_{Li})} \varphi_{2qi} + R_{si} I_{di} - X''_{qi} I_{qi} = 0 \qquad (2.8)$$

$$V_i \cos(\delta_i - \theta_i) - \frac{(X''_{di} - X_{Li})}{(X'_{di} - X_{Li})} E'_{qi} + \frac{(X'_{di} - X''_{di})}{(X'_{di} - X_{Li})} \varphi_{1di} + R_{si} I_{qi} + X''_{di} I_{di} = 0 \qquad (2.9)$$

for $i = 1, 2, \ldots, m$, where

V_i : magnitude of synchronous generator terminal voltage

θ_i : phase angle of synchronous generator terminal voltage

R_{si} : armature resistance

It should be noted that the synchronous generator terminal voltage ($V_i \angle \theta_i$ for $i = 1, 2, \ldots, m$,) is the internal bus voltages of the generator connected buses. The same notations for the bus voltages of non-generator buses are used as the generator buses, with $i = m+1, m+2, \ldots, n$, where n is the total number of buses of power network.

Then the dynamics of excitation system is considered and included as extension of the modelling of synchronous generator. Static AC excitation system is used for synchronous generators. The dynamics of excitation system is presented in differential equation as follows:

$$\dot{E}_{fdi} = -\frac{1}{T_{Ai}} E_{fdi} + \frac{K_{Ai}}{T_{Ai}} (V_{refi} - V_i) \qquad (2.10)$$

for $i = 1, 2, \ldots, m$, where

V_{refi} : voltage reference of the excitation system

T_{Ai} : time constant of the voltage regulator

K_{Ai} : transient gain of the voltage regulator

Power system stabiliser (PSS) is commonly used with synchronous generator to add damping to generator rotor oscillations by use of auxiliary stabilizing signals to control excitation

system. The purpose of PSS is producing an additional damping torque logical signal to rotor angular velocity ω_i so that the excitation system is controlled. A third-order PSS [149] is used and dynamics of PSS are presented in differential equations as follows:

$$\dot{V}_{pss1i} = \frac{K_{pssi}}{M_i}\Bigg[T_{Mi} - D_i(\omega_i - \omega_s) + \left(X''_{di} - X''_{qi}\right)I_{di}I_{qi} - \frac{\left(X''_{di} - X_{Li}\right)}{\left(X'_{di} - X_{Li}\right)}I_{qi}E'_{qi} - \frac{\left(X'_{di} - X''_{di}\right)}{\left(X'_{di} - X_{Li}\right)}I_{qi}\varphi_{1di} - \frac{\left(X''_{qi} - X_{Li}\right)}{\left(X'_{qi} - X_{Li}\right)}I_{di}E'_{di} + \frac{\left(X'_{qi} - X''_{qi}\right)}{\left(X'_{qi} - X_{Li}\right)}I_{di}\varphi_{2qi}\Bigg] - \frac{1}{T_{Wi}}V_{pss1i} \quad (2.\ 11)$$

$$\dot{V}_{pss2i} = \frac{T_{1i}}{T_{2i}}\frac{K_{pssi}}{M_i}\Bigg[T_{Mi} - D_i(\omega_i - \omega_s) + \left(X''_{di} - X''_{qi}\right)I_{di}I_{qi} - \frac{\left(X''_{di} - X_{Li}\right)}{\left(X'_{di} - X_{Li}\right)}I_{qi}E'_{qi} - \frac{\left(X'_{di} - X''_{di}\right)}{\left(X'_{di} - X_{Li}\right)}I_{qi}\varphi_{1di} - \frac{\left(X''_{qi} - X_{Li}\right)}{\left(X'_{qi} - X_{Li}\right)}I_{di}E'_{di} + \frac{\left(X'_{qi} - X''_{qi}\right)}{\left(X'_{qi} - X_{Li}\right)}I_{di}\varphi_{2qi}\Bigg] + \left(-\frac{T_{1i}}{T_{2i}}\frac{1}{T_{Wi}} + \frac{1}{T_{2i}}\right)V_{pss1i} - \frac{1}{T_{2i}}V_{pss2i} \quad (2.\ 12)$$

$$\dot{V}_{psssi} = \frac{T_{3i}}{T_{4i}}\frac{T_{1i}}{T_{2i}}\frac{K_{pssi}}{M_i}\Bigg[T_{Mi} - D_i(\omega_i - \omega_s) + \left(X''_{di} - X''_{qi}\right)I_{di}I_{qi} - \frac{\left(X''_{di} - X_{Li}\right)}{\left(X'_{di} - X_{Li}\right)}I_{qi}E'_{qi} - \frac{\left(X'_{di} - X''_{di}\right)}{\left(X'_{di} - X_{Li}\right)}I_{qi}\varphi_{1di} - \frac{\left(X''_{qi} - X_{Li}\right)}{\left(X'_{qi} - X_{Li}\right)}I_{di}E'_{di} + \frac{\left(X'_{qi} - X''_{qi}\right)}{\left(X'_{qi} - X_{Li}\right)}I_{di}\varphi_{2qi}\Bigg] + \left(-\frac{T_{1i}}{T_{2i}}\frac{T_{3i}}{T_{4i}}\frac{1}{T_{Wi}} + \frac{T_{3i}}{T_{4i}}\frac{1}{T_{2i}}\right)V_{pss1i} + \left(-\frac{T_{1i}}{T_{2i}}\frac{T_{3i}}{T_{4i}} + \frac{1}{T_{4i}}\right)V_{pss2i} - \frac{1}{T_{4i}}V_{psssi} \quad (2.\ 13)$$

for i = 1, 2, …, m, where

$V_{pss1i}, V_{pss2i}, V_{psssi}$: damping torque logical signals inside of PSS

K_{pssi}: stabiliser gain of PSS

T_{Wi} : washout time constant of PSS

T_{1i} , T_{2i} , T_{3i}, T_{4i}: lead/lag time constant of PSS

2.2.2 Network Power Flow

The power-balance form of network power flow equations is used in this study. The network power flow equations of active and reactive power flow for generator buses (*PV* buses) are in algebraic equations as follows:

$$V_i\left(I_{qi}\cos(\delta_i-\theta_i)+I_{di}\sin(\delta_i-\theta_i)\right)+P_{Li}$$
$$=\sum_{k=1}^{n}V_iV_k(G_{ik}\cos(\theta_i-\theta_k)+B_{ik}\sin(\theta_i-\theta_k)) \quad (2.\ 14)$$

$$V_i\left(I_{di}\cos(\delta_i-\theta_i)-I_{qi}\sin(\delta_i-\theta_i)\right)+Q_{Li}$$
$$=\sum_{k=1}^{n}V_iV_k(G_{ik}\sin(\theta_i-\theta_k)+B_{ik}\cos(\theta_i-\theta_k)) \quad (2.\ 15)$$

for $i = 1, 2, \ldots, m$, where

m : total number of generator buses

n : total number of buses of power network

G_{ik} : conductance between bus i and bus k from admittance matrix

B_{ik} : susceptance between bus i and bus k from admittance matrix

P_{Li} : active power of loads on bus i

Q_{Li} : reactive power of loads on bus i

The network power flow equations of active and reactive power flow for non-generator buses (*PQ* buses) are in algebraic equations as follows:

$$P_{Li}=\sum_{k=1}^{n}V_iV_k(G_{ik}\cos(\theta_i-\theta_k)+B_{ik}\sin(\theta_i-\theta_k)) \quad (2.\ 16)$$

$$Q_{Li}=\sum_{k=1}^{n}V_iV_k(G_{ik}\sin(\theta_i-\theta_k)+B_{ik}\cos(\theta_i-\theta_k)) \quad (2.\ 17)$$

for $i = m+1, m+2, \ldots, n$

2.3 Modelling of MTDC System without CFC

The MTDC system consists of multiple VSC converters and DC network. The topology, control system and modelling of VSC are presented in 2.3.1. The DC network is formed of DC transmission lines which are modelled by series resistors and inductors in 2.3.2. The DC CFC is not included in this chapter but is to be studied in Chapter 3.

2.3.1 VSC with Its Control System

VSC is a fully controlled semiconductor based power converter. It uses self-commuted semiconductor (for instance, IGBT) which can be turned on and turned off without relying on line voltage. VSC is able to control active and reactive power independently.

There are a variety of topologies of VSC in different voltage levels, depending on different application scenarios: two-level converter, three-level converter, or multilevel modular converter. The typical topology of a two-level three-phase VSC is shown in Figure 2- 1. The IGBT with antiparallel diode is used to form a valve. The DC bus capacitors C store energy and filter DC harmonics. L_C indicates the inductance of series AC reactor and coupling transformer. R_C indicates the equivalent resistance of reactor and power losses of converter. The control system of VSC is realised by the control of turned on or turned off state of all six valves. There is one valve in every arm of all six arms. There are two arms in each phase of converter. There is always one valve turned on while the other one valve in the same phase turned off. Hence the voltage at AC side of converter equals to either the positive or the negative voltage of DC bus capacitor. The VSC converter applied in this study is two-level converter.

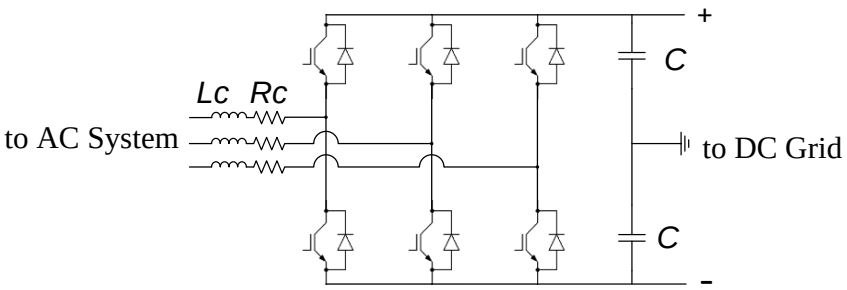


Figure 2- 1 Topology of a two-level three-phase VSC.

The single-line diagram (SLD) of a two-level VSC and its control system is shown in Figure 2- 2. *dq* decoupling control is used to regulate voltage at DC side V_{dc} or active power transfer P in d frame and voltage at AC side $V_{C,abc}$ or reactive power transfer in q frame.

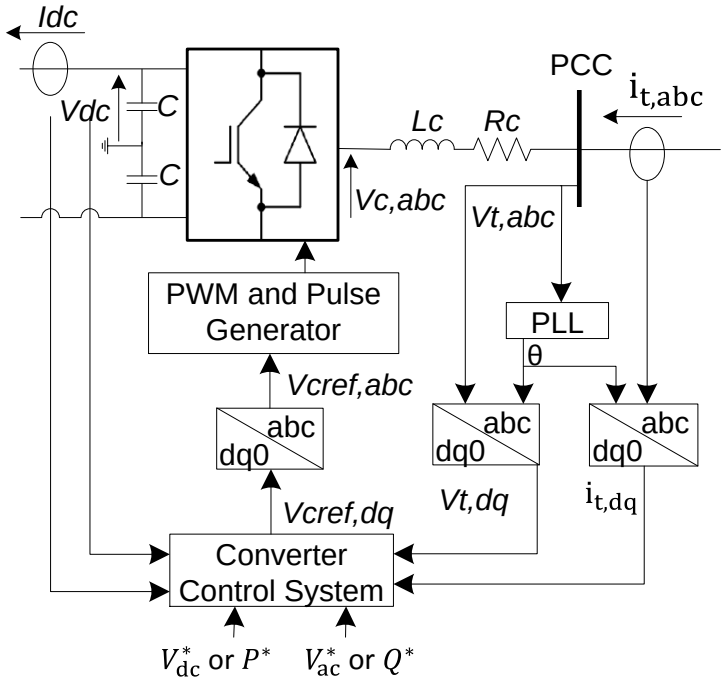


Figure 2- 2 Single-line diagram of a two-level VSC and its control system.

The *dq*0 transformation (which is also known as the Park transformation) is usually used in *dq* decoupling control for VSC. This method was firstly used in the modelling of synchronous machines to reduce considerable complexity in solving synchronous machine and power system problems and then spread to control strategy of VSC. It is an effective approach to derive a simpler and clearer representation of the dynamics of VSC. The transformation from the state variables in *abc* phase to *dq0* variables is presented in the following matrix form [6]:

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \qquad (2.\ 18)$$

where

i_d , i_q , and i_0 : state variables of currents in *dq0* frame

i_a , i_b , and i_c : state variables of currents in *abc* phase

θ : initial phase angle of *d* frame

The inverse transformation is presented as follows:

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta & 1 \\ \cos\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ \cos\left(\theta + \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \quad (2.\ 19)$$

The peak value of i_d equals to the peak value of i_a. Under balanced condition $i_0 = i_a + i_b + i_c = 0$.

As the single-line diagram of the control system of VSC shown in Figure 2- 2, the line-to-line voltages $v_{t,abc}$ and currents $i_{t,abc}$ at PCC (the primary side of the coupling transformer of VSC) in *abc* phase, and DC current through one DC transmission line I_{dc} and DC voltage across one DC energy storage capacitor V_{dc} at DC side of VSC are acquired. The line-to-line voltages at PCC $v_{t,abc}$ is inputted into PLL block to compute its frequency *f* and phase angle *θ*. Then the computed phase angle *θ*, along with line-to-line voltages $v_{t,abc}$ and currents $i_{t,abc}$ at PCC are input into two *abc*-to-*dq0* transformation blocks to compute line-to-line voltages $v_{t,dq}$ and currents $i_{t,dq}$ in *dq0* frame. The computed line-to-line voltages $v_{t,dq}$ and currents $i_{t,dq}$ in *dq0* frame, along with acquired DC current I_{dc} , DC voltage V_{dc} , reference of DC voltage V_{dc}^* or reference of active power transfer P^*, and reference of AC voltage at the AC terminal of VSC V_{ac}^* or reference of reactive power transfer Q^* (these four references are set by user) are inputted into the converter control system (which includes converter outer control loop and converter inner control loop). Through converter control system block, the output signal is computed, which is the reference of AC voltage at the AC terminal of VSC $v_{cref,dq}$in *dq* frame. Then the computed reference of AC voltage at the AC terminal of VSC $v_{cref,dq}$ is inputted *dq0*-to-*abc* transformation block. Through *dq0*-to-*abc* transformation block, the output signal is the computed reference of AC voltage at the AC terminal of VSC $v_{cref,abc}$ in *abc* phase. The computed reference of AC voltage at the AC terminal of VSC $v_{cref,abc}$ is inputted into PWM and pulse generator block to compute PWM signal and generate corresponding gate pulses to control valves of VSC. The output of PWM and pulse generator block is gate pulse signals which are inputted into VSC to control every valves of VSC to either turn on or turn off.

By use of the state variables in *dq* frame, the dynamic equation of the VSC connected to AC system by series reactor at PCC can be represented as follows:

$$v_{cd} - v_{td} = -R_c i_{td} - L_c \frac{di_{td}}{dt} + L_c \omega i_{tq} \quad (2.20)$$

$$v_{cq} - v_{tq} = -R_c i_{tq} - L_c \frac{di_{tq}}{dt} - L_c \omega i_{td} \quad (2.21)$$

The dynamic equation for DC side capacitor of VSC can be represented as follows:

$$V_{dc}\left(I_{dc} + C\frac{dV_{dc}}{dt}\right) = \frac{3}{2}\left(v_{cd} i_{td} + v_{cq} i_{tq}\right) \quad (2.22)$$

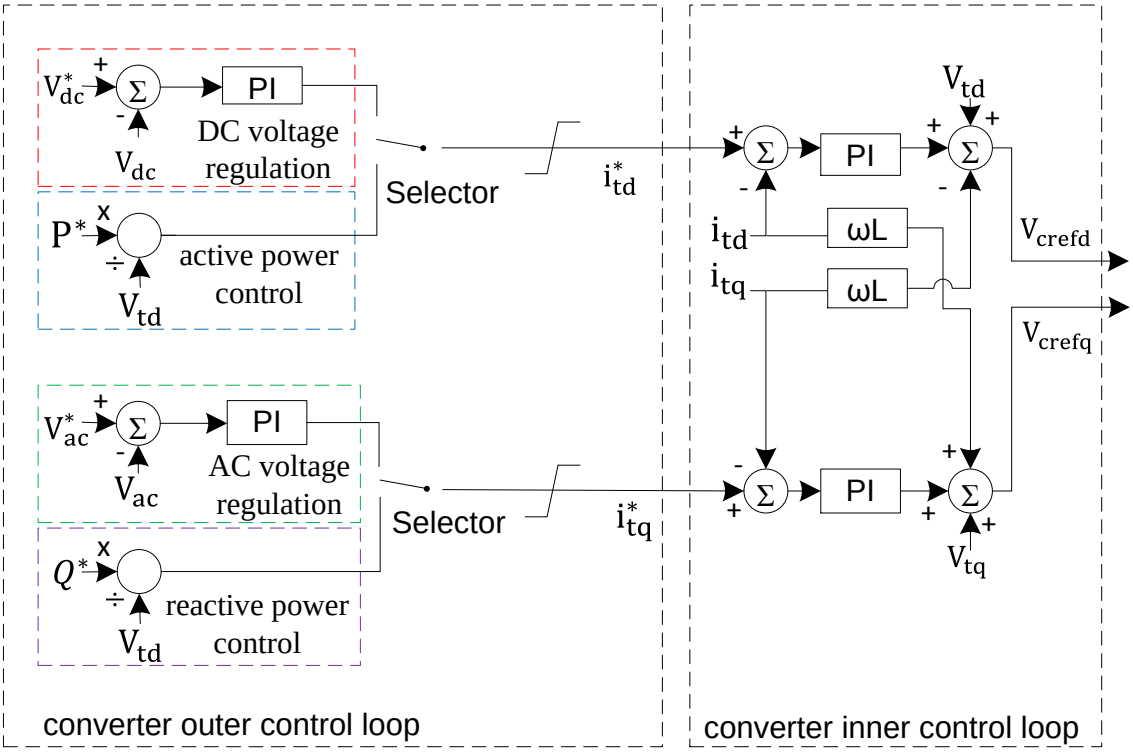


Figure 2- 3 Converter control system block.

The converter control system block of the whole control system of VSC is shown in Figure 2-3. The converter control system block consists of converter outer control loop and converter inner control loop. Reference of DC voltage V_{dc}^*, reference of active power transfer P^*, reference of AC voltage at the AC terminal of VSC V_{ac}^*, reference of reactive power transfer Q^*, V_{dc}, V_{ac}, and v_{td} are inputted into converter outer control loop. For DC voltage regulation block, the difference of V_{dc}^* and V_{dc} is inputted into a PI control loop to compute the output signal. For active power control block, the division of P^* divided by v_{td} formulates the output. For AC voltage regulation block, the difference of V_{ac}^* and V_{ac} is

inputted into a PI control loop to compute the output signal. For reactive power control block, the division of Q^*divided by v_{td} formulates the output. A selector is controlled by user to assign the control system of VSC to operate either in DC voltage regulation or active power control mode in *d* frame. Another selector is controlled by user to assign the control system of VSC to operate either in AC voltage regulation or reactive power control mode in *q* frame. The outputs of two selector blocks are then inputted to two limitation block to compute the final output signals of converter outer control loop i_{td}^* and i_{tq}^*, which are the reference of line-to-line current at PCC in *dq* frame.

When converter outer control loop operates in DC voltage regulation mode in *d* frame, the current reference i_{td}^* can be obtained from the converter outer control loop by:

$$i_{td}^* = k_{pdc}(V_{dc}^* - V_{dc}) + k_{idc}\int (V_{dc}^* - V_{dc})dt$$

$$= k_{pdc}(V_{dc}^* - V_{dc}) + k_{idc}x_1 \quad (2.23)$$

where

k_{pdc} : proportional gain of the PI control loop of converter outer control loop in *d* frame

k_{idc} : integral gain of PI control loop of converter outer control loop in *d* frame

x_1 : auxiliary state variable to represent the integral terms of the PI control loop of converter outer control loop in *d* frame

When converter outer control loop operates in active power control mode in *d* frame, the current reference i_{td}^* can be obtained from the converter outer control loop by:

$$i_{td}^* = \frac{P^*}{v_{td}} \quad (2.24)$$

When converter outer control loop operates in AC voltage regulation mode in *q* frame, the current reference in i_{tq}^* can be obtained from the converter outer control loop by:

$$i_{tq}^* = k_{pac}(V_{ac}^* - V_{ac}) + k_{iac}\int (V_{ac}^* - V_{ac})dt$$

$$= k_{pdc}(V_{ac}^* - V_{ac}) + k_{iac}x_2 \quad (2.25)$$

where

k_{pac} : proportional gain of the PI control loop of converter outer control loop in q frame

k_{iac} : integral gain of PI control loop of converter outer control loop in q frame

x_2 : auxiliary state variable to represent the integral terms of the PI control loop of converter outer control loop in q frame

And the AC voltage at point of common coupling V_{ac1} can be represented as:

$$V_{ac} = \sqrt{{v_{td}}^2 + {v_{tq}}^2} \tag{2.26}$$

When converter outer control loop operates in reactive power control mode in q frame, the current reference in i_{tq}^* can be obtained from the converter outer control loop by:

$$i_{tq}^* = \frac{Q^*}{v_{td}} \tag{2.27}$$

The reference of line-to-line current at PCC in dq frame i_{td}^* and i_{tq}^*, along with acquired value of line-to-line current at PCC in dq frame i_{td} and i_{tq}, are inputted into converter inner control loop. The difference of i_{td}^* and i_{td}, is inputted into PI controller loop and then added by v_{td} subtracted by $\omega L i_{tq}$ to compute output signal of v_{crefd}. The difference of i_{tq}^* and i_{tq}, is inputted into PI controller loop and then added by v_{td} and $\omega L i_{td}$ to compute output signal of v_{crefq}.

The reference of voltage at the AC terminal of VSC $v_{cref,dq}$ can be obtained from the converter inner control loop as:

$$\begin{aligned} v_{crefd} &= k_{pvd}(i_{td}^* - i_{td}) + k_{ivd}\int (i_{td}^* - i_{td})dt - \omega L_C i_{tq} + v_{td} \\ &= k_{pvd}(i_{td}^* - i_{td}) + k_{ivd}x_3 - \omega L_C i_{tq} + v_{td} \end{aligned} \tag{2.28}$$

$$\begin{aligned} v_{crefq} &= k_{pvq}\left(i_{tq}^* - i_{tq}\right) + k_{ivq}\int \left(i_{tq}^* - i_{tq}\right)dt + \omega L_C i_{td} + v_{tq} \\ &= k_{pvq}\left(i_{tq}^* - i_{tq}\right) + k_{ivq}x_4 + \omega L_C i_{td} + v_{tq} \end{aligned} \tag{2.29}$$

where

k_{pvd}, and k_{ivd} : proportional and integral gain of the PI control loop of converter inner control loop in *d* frame

k_{pvq}, and k_{ivq} : proportional and integral gain of the PI control loop of converter inner control loop in *q* frame

x_3 : auxiliary state variable to represent the integral terms of the PI control loop of converter outer control loop in *d* frame

x_4 : auxiliary state variable to represent the integral terms of the PI control loop of converter outer control loop in *q* frame

The dynamics of PWM and gate pulse generator are not considered in this study.

2.3.2 DC Network without CFC

As the topology of DC network without CFC shown in Figure 2- 4, the DC network consists of a number of DC transmission lines which connect a number of VSC converters (from VSC_1 to VSC_n where *n* indicates the total number of VSC). Figure 2- 4 shows a typical topology of simple meshed DC network. With no DC power flow control (no CFC) in the DC network, the DC currents flow from one node to another through the path of least resistance. The DC transmission line is modelled by series resistance and inductance (R_{1i} + L_{1i} for the impedance of DC cable that connects VSC_1 and VSC_i).

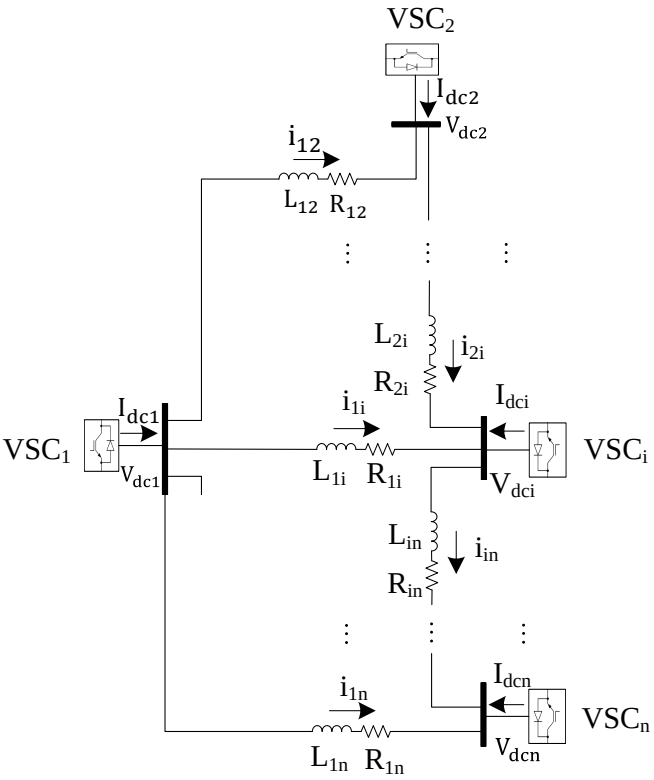


Figure 2- 4 Topology of DC network without CFC.

The dynamics of DC network without CFC can be represented by dynamic equations of all DC transmission lines as follows:

$$L_{12}\frac{di_{12}}{dt} + R_{12}i_{12} = V_{dc1} - V_{dc2} \tag{2.30}$$

$$\vdots$$

$$L_{1i}\frac{di_{1i}}{dt} + R_{1i}i_{1i} = V_{dc1} - V_{dci} \tag{2.31}$$

$$\vdots$$

$$L_{1n}\frac{di_{1n}}{dt} + R_{1n}i_{1n} = V_{dc1} - V_{dcn} \tag{2.32}$$

$$L_{2i}\frac{di_{2i}}{dt} + R_{2i}i_{2i} = V_{dc2} - V_{dci} \tag{2.33}$$

$$\vdots$$

$$L_{in}\frac{di_{in}}{dt} + R_{in}i_{in} = V_{dci} - V_{dcn} \tag{2.34}$$

⋮

$$L_{(n-1),n}\frac{di_{(n-1)n}}{dt} + R_{(n-1),n}i_{(n-1),n} = V_{dc,(n-1)} - V_{dcn} \quad (2.35)$$

for i = 1, 2, …, n, where

i : index number of VSC converter

n : total number of VSC converters

i_{12} , i_{1i} , i_{1n} , i_{2i} , i_{in} , and $i_{(n-1),n}$ i_{in} : the currents for DC branch 12, 1i, 1n, 2i, in and (n-1)n

V_{dc1}, V_{dc2}, V_{dci}, $V_{dc,(n-1)}$, and V_{dcn} : the DC voltages of one DC energy storage capacitor at DC side of VSC_1, VSC_2, VSC_2, VSC_{n-1} and VSC_n

R_{12} , R_{1i} , R_{1n} , R_{2i} , $R_{i,(n-1)}$, and R_{in} : the resistance of DC cable for branch 12, 1i, 1n, 2i, in and (n-1),n

L_{12} , L_{1i} , L_{1n} , L_{2i} , $L_{i,(n-1)}$, and L_{in} : the reactance of DC cable for branch 12, 1i, 1n, 2i, in and (n-1),n

2.4 Linearization and Formulation of Multi-Model System

The models of AC power system and MTDC system without CFC are linearized and presented in state-space representation in this section, in order to study the small-signal stability of the multi-model system. The independent models of AC power system and MTDC system without CFC presented in 2.4.3 are linearized with respect to the equilibrium point and then reformed into a number of sets of differential-algebraic equations (DAE) in state-space form [6]. Finally, the independent linearized state-space representations are formulated as whole in a form as follows:

$$\Delta\dot{x} = \boldsymbol{A}\Delta x + \boldsymbol{B}\Delta u \quad (2.36)$$

where

Δx : incremental change of the state variable vector

Δu : incremental change of the input vector

$\boldsymbol{A}$: state matrix

$\boldsymbol{B}$: input matrix.

2.4.1 Linearization of AC Power System

The linearization of the synchronous generator dynamics (2.2)-(2.7) can be expressed as follows:

$$\Delta\dot{x}_{SGi} = \boldsymbol{A_{SGi}}\Delta x_{SGi} + \boldsymbol{B_{SG1i}}\Delta I_{gi} + \boldsymbol{B_{SG2i}}\Delta V_{gi} + \boldsymbol{E_{SG1i}}\Delta u_{gi} \quad (2.37)$$

where

$$\Delta x_{SGi} = \left[\Delta\delta_i, \Delta\omega_i, \Delta E'_{qi}, \Delta E'_{di}, \Delta\varphi_{1di}, \Delta\varphi_{2qi}\right]^T \quad (2.38)$$

$$\Delta I_{gi} = \left[\Delta I_{di}, \Delta I_{qi}\right]^T \quad (2.39)$$

$$\Delta V_{gi} = [\Delta\theta_i, \Delta V_i]^T \quad (2.40)$$

$$\Delta u_{gi} = \left[\Delta T_{Mi}, \Delta V_{refi}\right]^T \quad (2.41)$$

The linearization of the excitation system dynamics (2.10) can be expressed as follows:

$$\Delta\dot{x}_{EXCi} = \boldsymbol{A_{EXCi}}\Delta x_{EXCi} + \boldsymbol{B_{EXC1i}}\Delta I_{gi} + \boldsymbol{B_{EXC2i}}\Delta V_{gi} + \boldsymbol{E_{EXC1i}}\Delta u_{gi} \quad (2.42)$$

where

$$\Delta x_{EXCi} = \left[\Delta E_{fdi}\right]^T \quad (2.43)$$

The linearization of the PSS of synchronous generator dynamics (2.11)-(2.13) can be expressed as follows:

$$\Delta\dot{x}_{PSSi} = \boldsymbol{A_{PSSi}}\Delta x_{PSSi} + \boldsymbol{B_{PSS1i}}\Delta I_{gi} + \boldsymbol{B_{PSS2i}}\Delta V_{gi} + \boldsymbol{E_{PSS1i}}\Delta u_{gi} \quad (2.44)$$

where

$$\Delta x_{PSSi} = \left[\Delta V_{pss1i}, \Delta V_{pss2i}, \Delta V_{psssi}\right]^T \quad (2.45)$$

The formulation form of linearized model of synchronous generator with its excitation system and PSS can be obtained by adding all independent linearized models of synchronous generator, excitation system, and PSS as follows:

$$\Delta\dot{x}_{SGAi} = \boldsymbol{A_{SGAi}}\Delta x_{SGAi} + \boldsymbol{B_{SGA1i}}\Delta I_{gi} + \boldsymbol{B_{SGA2i}}\Delta V_{gi} + \boldsymbol{E_{SGA1i}}\Delta u_{gi} \qquad (2.46)$$

where

$$\Delta x_{SGAi} = \left[\Delta {x_{SGi}}^T, \Delta {x_{EXCi}}^T, \Delta {x_{PSSi}}^T\right]^T \qquad (2.47)$$

$$\boldsymbol{A_{SGAi}} = \begin{bmatrix} \boldsymbol{A_{SGi}} & & \\ & \boldsymbol{A_{EXCi}} & \\ & & \boldsymbol{A_{PSSi}} \end{bmatrix} \qquad (2.48)$$

$$\boldsymbol{B_{SGA1i}} = \begin{bmatrix} \boldsymbol{B_{SG1i}} & & \\ & \boldsymbol{B_{EXC1i}} & \\ & & \boldsymbol{B_{PSS1i}} \end{bmatrix} \qquad (2.49)$$

$$\boldsymbol{B_{SGA2i}} = \begin{bmatrix} \boldsymbol{B_{SG2i}} & & \\ & \boldsymbol{B_{EXC2i}} & \\ & & \boldsymbol{B_{PSS2i}} \end{bmatrix} \qquad (2.50)$$

$$\boldsymbol{E_{SGA1i}} = \begin{bmatrix} \boldsymbol{E_{SG1i}} & & \\ & \boldsymbol{E_{EXC1i}} & \\ & & \boldsymbol{E_{PSS1i}} \end{bmatrix} \qquad (2.51)$$

The dynamic equations of all synchronous generators can be expressed by adding all dynamic equations of synchronous generators in a compact matrix form as follows:

$$\Delta\dot{x}_{SGA} = \boldsymbol{A_{SGA}}\Delta x_{SGA} + \boldsymbol{B_{SGA1}}\Delta I_g + \boldsymbol{B_{SGA2}}\Delta V_g + \boldsymbol{E_{SGA1}}\Delta u_g \qquad (2.52)$$

where

$$\Delta x_{SGA} = [\Delta {x_{SGA1}}^T, \dots, \Delta {x_{SGAi}}^T, \dots, \Delta {x_{SGAm}}^T]^T \qquad (2.53)$$

$$\Delta V_g = [\Delta {V_{g1}}^T, \dots, \Delta {V_{gi}}^T, \dots, \Delta {V_{gm}}^T]^T \qquad (2.54)$$

$$\Delta I_g = [\Delta {I_{g1}}^T, \dots, \Delta {I_{gi}}^T, \dots, \Delta {I_{gm}}^T]^T \qquad (2.55)$$

$$\Delta u_g = [\Delta {u_{g1}}^T, \dots, \Delta {u_{gi}}^T, \dots, \Delta {u_{gm}}^T]^T \qquad (2.56)$$

$$\boldsymbol{A_{SGA}} = \begin{bmatrix} \boldsymbol{A_{SGA1}} & & & \\ & \ddots & & \\ & & \boldsymbol{A_{SGAi}} & \\ & & & \ddots \\ & & & & \boldsymbol{A_{SGAm}} \end{bmatrix} \tag{2.57}$$

$$\boldsymbol{B_{SGA1}} = \begin{bmatrix} \boldsymbol{B_{SGA11}} & & & \\ & \ddots & & \\ & & \boldsymbol{B_{SGA1i}} & \\ & & & \ddots \\ & & & & \boldsymbol{B_{SGA1m}} \end{bmatrix} \tag{2.58}$$

$$\boldsymbol{B_{SGA2}} = \begin{bmatrix} \boldsymbol{B_{SGA21}} & & & \\ & \ddots & & \\ & & \boldsymbol{B_{SGA2i}} & \\ & & & \ddots \\ & & & & \boldsymbol{B_{SGA2m}} \end{bmatrix} \tag{2.59}$$

$$\boldsymbol{E_{SGA1}} = \begin{bmatrix} \boldsymbol{E_{SGA11}} & & & \\ & \ddots & & \\ & & \boldsymbol{E_{SGA1i}} & \\ & & & \ddots \\ & & & & \boldsymbol{E_{SGA1m}} \end{bmatrix} \tag{2.60}$$

The linearized form of the algebraic equations of generator terminal voltage (2.8)-(2.9) can be represented as follows:

$$0 = \boldsymbol{C_{SGAi}}\Delta x_{SGAi} + \boldsymbol{D_{SGA1i}}\Delta I_{gi} + \boldsymbol{D_{SGA2i}}\Delta V_{gi} \tag{2.61}$$

In same way as the dynamic equations of synchronous generator, the linearized form of the algebraic equations of all generator terminal voltages can be expressed by adding all of the linearized algebraic equations of generator terminal voltages in a compact matrix form as follows:

$$0 = \boldsymbol{C_{SGA}}\Delta x_{SGA} + \boldsymbol{D_{SGA1}}\Delta I_g + \boldsymbol{D_{SGA2}}\Delta V_g \tag{2.62}$$

The linearized form of the network power flow balancing equations of generator buses (*PV* buses) (2.14)-(2.15) can be represented as follows:

$$0 = \boldsymbol{C_2}\Delta x_{SGA} + \boldsymbol{D_3}\Delta I_g + \boldsymbol{D_4}\Delta V_g + \boldsymbol{D_5}\Delta V_l \tag{2.63}$$

where

$$\Delta V_l = [\Delta V_{l,(m+1)}{}^T, \dots, \Delta V_{li}{}^T, \dots, \Delta V_{ln}{}^T]^T \quad (2.64)$$

for $i = m+1, m+2, \dots, n$ where

$$\Delta V_{li} = [\Delta\theta_i, \Delta V_i]^T \quad (2.65)$$

Similarly, the linearized form of the network power flow balancing equations of non-generator buses (*PQ* buses) (2.16)-(2.17) can be represented as follows:

$$0 = \boldsymbol{D_6}\Delta V_g + \boldsymbol{D_7}\Delta V_l \quad (2.66)$$

The whole linearized model of AC power system can be represented by (2.52,)(2.62)-(2.66).

2.4.2 Linearization of MTDC System without CFC

The linearized form of the dynamic equations of DC network without CFC (2.30)-(2.35) can be expressed as follows:

$$\Delta\dot{x}_{DC} = \boldsymbol{A_{DC1}}\Delta x_{DC} + \boldsymbol{A_{DC2}}\Delta x_{Vdc} \quad (2.67)$$

where

$$\Delta x_{DC} = [\Delta i_{12}, \dots, \Delta i_{1i}, \dots, \Delta i_{1n}, \Delta i_{2i}, \dots, \Delta i_{in}, \dots, \Delta i_{(n-1),n}]^T \quad (2.68)$$

$$\Delta x_{Vdc} = [\Delta V_{dc1}, \dots, \Delta V_{dci}, \dots, \Delta V_{dcn}]^T \quad (2.69)$$

for $i = 1, 2, \dots, n$, where

i : index number of VSC converter

n : total number of VSC converters

In order to obtain the linearized form of the dynamic equations of VSC, (2.23)-(2.29) are substituted into (2.20)-(2.22). In this way, the linearized form of the dynamic equations of VSC can be expressed as follows:

$$\Delta \dot{x}_{VSC} = \boldsymbol{A_{VSC}} \Delta x_{VSC} + \boldsymbol{B_{VSC1}} \Delta I_{dc} + \boldsymbol{B_{VSC2}} \Delta I_t + \boldsymbol{B_{VSC3}} \Delta V_t + \boldsymbol{E_{VSC}} \Delta u_{VSC} \quad (2.70)$$

where

$$\Delta x_{VSC} = \left[{\Delta x_{VSC1}}^T, \dots, {\Delta x_{VSCi}}^T, \dots, {\Delta x_{VSCn}}^T \right]^T \quad (2.71)$$

$$\Delta x_{VSCi} = [\Delta V_{dci}, \Delta x_{1i}, \Delta x_{2i}, \Delta x_{3i}, \Delta x_{4i}]^T \quad (2.72)$$

$$\Delta I_{dc} = [\Delta I_{dc1}, \dots, \Delta I_{dci}, \dots, \Delta I_{dcn}]^T \quad (2.73)$$

$$\Delta I_t = \left[{\Delta I_{t1}}^T, \dots, {\Delta I_{ti}}^T, \dots, {\Delta I_{tn}}^T \right]^T \quad (2.74)$$

$$\Delta I_{ti} = \left[\Delta i_{tdi}, \Delta i_{tqi} \right]^T \quad (2.75)$$

$$\Delta V_t = \left[{\Delta V_{t1}}^T, \dots, {\Delta V_{ti}}^T, \dots, {\Delta V_{tn}}^T \right]^T \quad (2.76)$$

$$\Delta V_{ti} = \left[\Delta v_{tdi}, \Delta v_{tqi} \right]^T \quad (2.77)$$

$$\Delta u_{VSC} = \left[{\Delta u_{VSC1}}^T, \dots, {\Delta u_{VSCi}}^T, \dots \Delta {u_{VSCn}}^T \right]^T \quad (2.78)$$

$$\Delta u_{VSCi} = [\Delta V_{dci}^*, \Delta P_i^*, \Delta V_{aci}^*, \Delta Q_i^*,]^T \quad (2.79)$$

for $i = 1, 2, \dots, n$, where

i : i is introduced as the index number of VSC converter

n : total number of VSC converters

For MTDC system with arbitrary topology of DC network, the relationship between output DC current from VSC and branch current of DC cables can be determined by algebraic equation as follows:

$$\Delta I_{dc} = \boldsymbol{F} \Delta x_{DC} \quad (2.80)$$

where

$\boldsymbol{F}$: DC network matrix that can be determined by topology of DC network

By merging (2.67) and (2.70) using (2.80), the linearized form of the dynamic equations of MTDC system without CFC can be expressed as follows:

$$\Delta\dot{x}_{MTDC} = \boldsymbol{A_{MTDC}}\Delta x_{MTDC} + \boldsymbol{B_{VSC2}}\Delta I_t + \boldsymbol{B_{VSC3}}\Delta V_t + \boldsymbol{E_{VSC}}\Delta u_{VSC} \qquad (2.81)$$

where

$$\Delta x_{MTDC} = \left[\Delta {x_{VSC}}^T, \Delta {x_{DC}}^T\right]^T \qquad (2.82)$$

2.4.3 Formulation of Multi-Model System

The independent linearized models of AC power system and MTDC system without CFC studied in 2.4.1 and 2.4.2 are formulated into a whole multi-model system, in order to investigate the small-signal stability of VSC based MTDC system without CFC.

When MTDC system is integrated to AC power system via VSC converters connected at non-generator buses, the relationship between voltage and current at PCC of VSC and voltage and current of network power flow balancing equations can be expressed as follows:

$$V_k e^{j\theta_k} = v_{tdi} + jv_{tqi} \qquad (2.83)$$

$$\left(i_{tdi} + ji_{tqi}\right)(R_{Ci} + j\omega L_{Ci}) = \left(v_{tdi} + jv_{tqi}\right) - \left(v_{cdi} + jv_{cqi}\right) \qquad (2.84)$$

for $i = 1, 2, \ldots, n$, where

i : index number of VSC converter

k : index number of bus where VSC_i is connected

n : total number of VSC converters

By substituting (2.83)-(2.84) into (2.81), the linearized form of the dynamic equations of MTDC system without CFC can be simplified as follows:

$$\Delta\dot{x}_{MTDC} = \boldsymbol{A_{MTDCP}}\Delta x_{MTDC} + \boldsymbol{B_{MTDCP}}\Delta V_l + \boldsymbol{E_{MTDCP}}\Delta u_{VSC} \qquad (2.85)$$

where

$$\Delta x_{MTDC} = \left[\Delta {x_{VSC}}^T, \Delta {x_{DC}}^T\right]^T \qquad (2.86)$$

When MTDC system is integrated to AC power system via VSC converters connected at non-generator buses, the power injection at non-generator bus *i* can concluded as follows:

$$P_{VSCi} + jQ_{VSCi} = V_k e^{j\theta_k}(i_{tdi} + ji_{tqi})^* \tag{2.87}$$

(2.87) is linearized and simplified as power injection equations as follows:

$$\begin{bmatrix}\Delta P_{VSCi} \\ \Delta Q_{VSCi}\end{bmatrix} = \boldsymbol{BL_{ci}}\Delta x_{MTDCi} + \boldsymbol{BL_{ui}}\Delta u_{VSCi} + \boldsymbol{DL_i}\Delta V_{li} \tag{2.88}$$

By substituting (2.88) into (2.66), the updated network power flow equations of non-generator buses (*PQ* buses) are in algebraic equations as follows:

$$0 = \boldsymbol{D_6}\Delta V_g + \boldsymbol{D_7}\Delta V_l + \boldsymbol{BL_c}\Delta x_{MTDC} + \boldsymbol{BL_u}\Delta u_{VSC} + \boldsymbol{DL}\Delta V_l \tag{2.89}$$

$$0 = \boldsymbol{D_6}\Delta V_g + \boldsymbol{D_7'}\Delta V_l + \boldsymbol{BL_{ST}}\Delta x_{MTDC} + \boldsymbol{D_{ST}}\Delta u_{VSC} \tag{2.90}$$

Finally, linearized dynamic equations of all synchronous generators (2.52) and linearized dynamic equations of MTDC system without CFC (2.81) are merged, via substituting all network power flow equations of generator buses (2.63) and non-generator buses (2.90) as follows:

$$\Delta\dot{X} = \boldsymbol{A_{ACDC}}\Delta X + \boldsymbol{B_{ACDC}}\Delta U \tag{2.91}$$

where

$$\Delta X = \left[\Delta x_{SGA}{}^T, \Delta x_{MTDC}{}^T\right]^T \tag{2.92}$$

$$\Delta U = \left[\Delta u_g{}^T, \Delta u_{VSC}{}^T\right]^T \tag{2.93}$$

2.5 Small-Signal Stability Analysis

Small-signal stability analysis is to study if a power system is capable of maintaining synchronism when it is subjected to small disturbances [147]. A disturbance is considered to be small if the equations that describe the response of the power system against disturbance can be linearized with respect to the equilibrium point [147]. A test system that consists of

AC power system with multiple synchronous generators and MTDC system with multiple VSC converters is established in 2.5.1. Modal analysis of the established AC/DC system is implemented to investigate its small signal stability in 2.5.2.

2.5.1 Test System

As shown in Figure 2- 5, the topology of the studied AC/DC system consists of AC power system with multiple synchronous generators and MTDC system with multiple VSC converters. The studied system is based on Kundur's 4-generator 2-area system proposed in [6] where all parameters of AC system can be found. There are two areas connected by a week tie (220 km double-circuit transmission line) and VSC converters integrated three-terminal DC network. The AC system consists of 4 synchronous generators with excitation system and PSS as described in 2.2.1. The DC network consists of three VSC converters connected by meshed DC cables as described in 2.2.2. The pole-to-pole voltage of all VSC converters is 120 kV. The master-slave control is used for VSC MTDC system. VSC_2 is operating in V_{dc} - V_{ac} control, controlling the DC voltage level of DC network and AC voltage at the PCC of VSC_2 to AC system. VSC_1 and VSC_3 are operating in P-V_{ac} control, controlling active power transferred through VSC converters and AC voltage at their PCC to AC system. The generator parameters, Excitation system parameters and PSS parameters are listed in Appendix A.1, A.2, and A.3. The Transmission line parameters are listed in Appendix A.4. The generation data, and load data are listed in Appendix A.5 and A.6. The parameters of VSC converters and DC network are shown in Appendix A.7 and A.8.

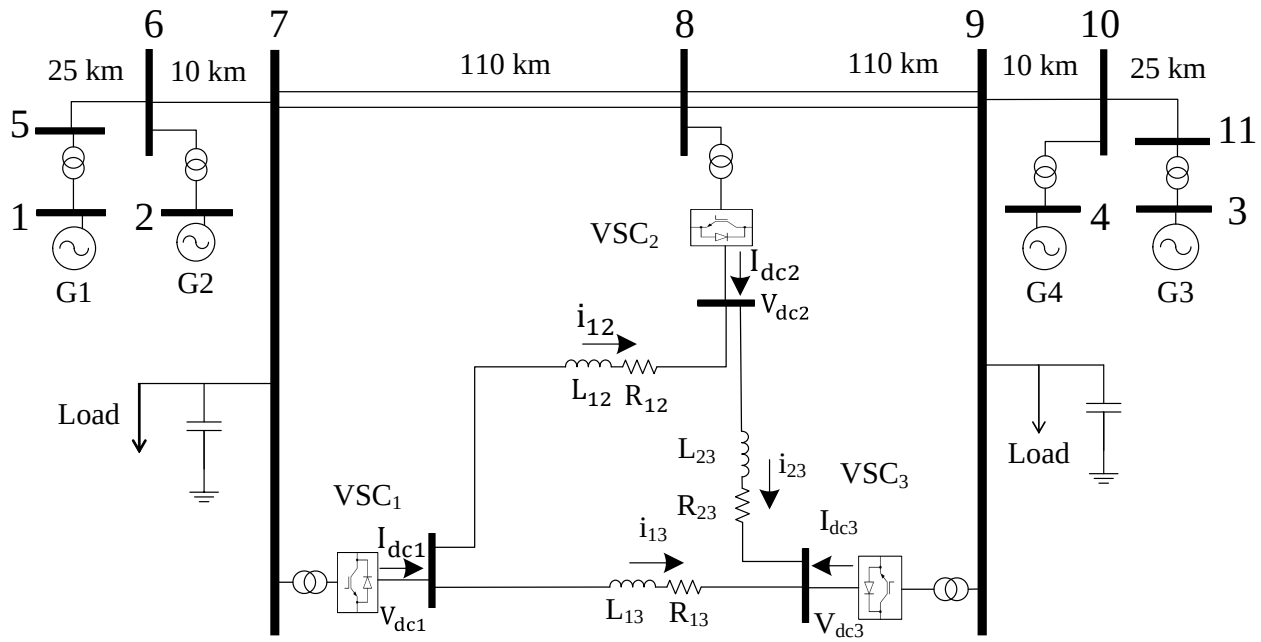


Figure 2- 5 Topology of the studied AC/DC system.

2.5.2 Modal Analysis

The small-signal stability analysis of the integrated AC/DC system established in 2.5.1 is presented in this section. The eigenvalues of the state matrix $\boldsymbol{A_{ACDC}}$ of the studied system are defined as the values of the scalar parameter $\boldsymbol{\lambda_{ACDC}}$ for which there exist non-trivial solutions (other than $\Phi = 0$) to the equation:

$$\boldsymbol{A_{ACDC}\Phi = \lambda_{ACDC}\Phi} \tag{2.94}$$

where

n : the order of $\boldsymbol{A_{ACDC}}$

$\boldsymbol{\Phi}$: an $n \times 1$ vector

Generally, (2.95) is used to compute the eigenvalues as follows:

$$(\boldsymbol{A_{ACDC} - \lambda_{ACDC}I})\boldsymbol{\Phi} = 0 \tag{2.95}$$

For a non-trivial solution

$$(\boldsymbol{A_{ACDC} - \lambda_{ACDC}I}) = 0 \tag{2.96}$$

The n solutions of $\boldsymbol{\lambda_{ACDC}} = \lambda_{ACDC1}, \lambda_{ACDC2}, \dots, \lambda_{ACDCn}$ are the eigenvalues of $\boldsymbol{A_{ACDC}}$.

The right eigenvector Φ_i of $\boldsymbol{A_{ACDC}}$ is defined as that for any eigenvalue λ_{ACDCi}, the n-column vector Φ_i which satisfies (2.93) is called the right eigenvector of $\boldsymbol{A_{ACDC}}$ associated with the eigenvalue λ_{ACDCi} [6].

$$\boldsymbol{A_{ACDC}}\Phi_i = \lambda_{ACDCi}\Phi_i \tag{2.97}$$

for $i = 1,2,\dots, n$

And the right eigenvector Φ_i is with the form of

$$\boldsymbol{\Phi}_i = \begin{bmatrix} \Phi_{1i} \\ \Phi_{2i} \\ \vdots \\ \Phi_{ni} \end{bmatrix} \tag{2.98}$$

Similarly, the left eigenvector Ψ_i of $\boldsymbol{A_{ACDC}}$ is defined as the n-column vector Ψ_i which satisfies (2.99) is called the left eigenvector of $\boldsymbol{A_{ACDC}}$ associated with the eigenvalue λ_{ACDCi}.

$$\Psi_i\boldsymbol{A_{ACDC}} = \lambda_{ACDCi}\Psi_i \tag{2.99}$$

for $i = 1,2,\dots, n$

Since the eigenvectors are determined only to within a scalar multiplier, generally the left and right vectors should be normalized to satisfy the (2.96) as follows:

$$\Phi_i\Psi_i = 1 \tag{2.100}$$

for $i = 1,2,\dots, n$

Participation matrix $\boldsymbol{P}$ that combines the right and the left eigenvectors, is usually used as a measure of association between state variable and the modes as follows:

$$\boldsymbol{P} = [\boldsymbol{P_1}, \boldsymbol{P_2}, \dots, \boldsymbol{P_i}, \dots \boldsymbol{P_n}] \tag{2.101}$$

$$\boldsymbol{P_i} = \begin{bmatrix} p_{1i} \\ p_{2i} \\ \vdots \\ p_{ni} \end{bmatrix} = \begin{bmatrix} \Phi_{1i}\Psi_{i1} \\ \Phi_{2i}\Psi_{i2} \\ \vdots \\ \Phi_{ni}\Psi_{in} \end{bmatrix} \tag{2.102}$$

where

Φ_{ki} : the k-th entry of the right eigenvector Φ_i

Ψ_{ik} : the *k*-th entry of the left eigenvector Ψ_i

The term $p_{ki} = \Phi_{ki}\Psi_{ik}$ is defined as participation factor, as a measure of the relative participation of the *k*-th state variable in the *i*-th mode. From Participation matrix, the dominant state is defined as the state variable which has the largest participation factor of corresponding mode.

The complete state-space matrix $\boldsymbol{A_{ACDC}}$ has a dimension of 52×52, which consists of sub state-space matrix of two synchronous with excitation system ($2 \times (7 \times 7) = 2 \times (6 + 1) \times (6 + 1)$), sub state-space matrix of two synchronous with excitation system and PSS ($2 \times (10 \times 10) = 2 \times (6 + 1 + 3) \times (6 + 1 + 3)$), sub state-space matrix of three VSC converters ($3 \times (5 \times 5)$) and sub state-space matrix of DC network (3×3).

By use of the approach to compute eigenvalues presented in (2.96), the calculated eigenvalues $\boldsymbol{\lambda_{ACDC}}$ of $\boldsymbol{A_{ACDC}}$ are shown in Table 2- 1. The frequency of oscillation, damping ratio and dominant state of all conjugate pairs of complex eigenvalues are also provided in Table 2- 1.

Table 2- 1 Eigenvalue results of the test system

No.	*Eigenvalue		*Frequency	*Damping Ratio	*Dominant State
1	-989.996909		\	\	ΔE_{fd4}
2	-992.295150		\	\	ΔE_{fd1}
3	-995.595105		\	\	ΔE_{fd1}
4	-995.707401		\	\	ΔE_{fd4}
5	-50.413426		\	\	ΔV_{pss23}
6	-50.366195		\	\	ΔV_{pss21}
7	-21.427299	+15.161188 *j	2.413	0.816	$\Delta\varphi_{1d4}$
8	-21.427299	-15.161188 *j	2.413	0.816	$\Delta\varphi_{1d4}$
9	-40.882330		\	\	ΔV_{dc2}
10	-37.917394		\	\	ΔV_{dc3}
11	-36.146715	+0.024978 *j	0.004	1.000	$\Delta\varphi_{2q4}$
12	-36.146715	-0.024978 *j	0.004	1.000	$\Delta\varphi_{2q4}$
13	-36.288964		\	\	ΔV_{dc1}
14	-32.194002		\	\	$\Delta\varphi_{1d2}$
15	-30.737547	+0.158066 *j	0.025	1.000	$\Delta\varphi_{2q2}$
16	-30.737547	-0.158066 *j	0.025	1.000	$\Delta\varphi_{2q2}$
17	-31.405309		\	\	$\Delta\varphi_{1d4}$
18	-20.867438	+9.467676 *j	1.507	0.911	ΔE_{q1}
19	-20.867438	-9.467676 *j	1.507	0.911	ΔE_{q1}
20	-1.324679	+7.721609 *j	1.229	0.169	$\Delta\delta_2 \setminus \Delta\omega_2$
21	-1.324679	-7.721609 *j	1.229	0.169	$\Delta\delta_2 \setminus \Delta\omega_2$
22	-1.353152	+7.949151 *j	1.265	0.168	$\Delta\delta_3 \setminus \Delta\omega_3$
23	-1.353152	-7.949151 *j	1.265	0.168	$\Delta\delta_3 \setminus \Delta\omega_3$
24	-10.373650		\	\	ΔE_{q1}
25	-10.232562		\	\	ΔE_{q4}
26	-0.218620	+4.107588 *j	0.654	0.053	$\Delta\delta_1 \setminus \Delta\omega_1$
27	-0.218620	-4.107588 *j	0.654	0.053	$\Delta\delta_1 \setminus \Delta\omega_1$

28	-3.018354		\	\	ΔE_{q3}
29	-3.006456		\	\	ΔE_{d1}
30	-2.845598		\	\	Δi_{12}
31	-3.463600	+0.021567 *j	0.003	1.000	ΔE_{d2}
32	-3.463600	-0.021567 *j	0.003	1.000	ΔE_{d2}
33	-3.455578		\	\	Δi_{13}
34	-0.228905		\	\	Δi_{23}
35	-0.203891		\	\	ΔV_{pss31}
36	-0.180524		\	\	ΔV_{pss33}
37	-0.133536		\		Δx_{32}
38	-0.102150		\	\	ΔV_{pss13}
39	-0.051441		\	\	ΔV_{pss11}
40	-0.034907		\	\	Δx_{42}
41	-0.016020		\	\	Δx_{41}
42	-0.003969		\	\	Δx_{43}
43	-0.011648		\	\	Δx_{32}
44	-0.011527		\	\	Δx_{31}
45	-0.000000	+0.000000 *j	0.000	0.000	$\Delta\delta_4 \setminus \Delta\omega_4$
46	-0.000000	-0.000000 *j	0.000	0.000	$\Delta\delta_4 \setminus \Delta\omega_4$
47	-3.333333		\	\	Δx_{21}
48	-3.333333		\	\	Δx_{12}
49	-3.333333		\	\	Δx_{13}
50	-3.333333		\	\	Δx_{23}
51	-3.333333		\	\	Δx_{22}
52	-3.333333		\	\	Δx_{23}

It can be seen from Table 2- 1 that all 52 eigenvalues have non-positive real part. This indicates a stable operating condition at the equilibrium point. There are two zero eigenvalues $\lambda_{ACDC45,46}$, as there is no infinite busbar in the testing network. One of the zero eigenvalues arises from a redundancy in synchronous generator angle. The second zero eigenvalue results from that the generator torque is independent of machine speed deviations, and this is because mechanical damping is neglected and governor action is not represented. This can also be proved by the fact that the dominant states of the two zero eigenvalues are rotor angle and rotor angular velocity of synchronous generator G_4. If the rotor angle and angular velocity of one synchronous generator are regarded as references, and the governor action of mechanical damping is considered, the two zero eigenvalues will be reduced [148-149].

All the conjugate pairs of complex eigenvalues $\lambda_{ACDC7,8}$, $\lambda_{ACDC11,12}$, $\lambda_{ACDC15,16}$, $\lambda_{ACDC18,19}$, $\lambda_{ACDC20,21}$, $\lambda_{ACDC22,23}$, $\lambda_{ACDC26,27}$, and $\lambda_{ACDC31,32}$ are related to the dominant state variables of synchronous generators according to their participation factors. The damping of these modes is mainly affected by synchronous generator setting, associated exciter setting, and corresponding power system stabilizer parameters. The eigenvalues that significantly affects the dynamic response of the system are $\lambda_{ACDC26,27}$ (with frequency of oscillation of 0.654 Hz, and damping ratio of 0.053). According to participation matrix, the state variables of

synchronous generator G_1 have a dominant effect on the conjugate pair of $\lambda_{ACDC26,27}$. In consequence, these states should be considered primarily in attempt to improve network damping characteristic.

The conjugate pairs of complex eigenvalues $\lambda_{ACDC20,21}$(with frequency of oscillation of 1.229 Hz, and damping ratio of 0.169), $\lambda_{ACDC22,23}$(with frequency of oscillation of 1.265 Hz, and damping ratio of 0.168), and $\lambda_{ACDC26,27}$(with frequency of oscillation of 0.654 Hz, and damping ratio of 0.053) are related to the rotor angle and rotor angular velocity of synchronous generator G_2, G_3, and G_1 respectively, if the rotor angle and rotor angular velocity of synchronous generator G_4 are regarded as reference. These oscillation characteristic reflected by modal analysis can be further validated by simulation results in section 2.6. The conjugate pairs of complex eigenvalues $\lambda_{ACDC18,19}$ are associated to the transient electromagnetic force caused by field flux linkage in *q*-axis of synchronous generator G_1. The remaining conjugate pairs of complex eigenvalues $\lambda_{ACDC7,8}$, and $\lambda_{ACDC11,12}$ are associated to the states of synchronous generator G_4 and conjugate pairs $\lambda_{ACDC15,16}$, and $\lambda_{ACDC31,32}$ are associated to the states of synchronous generator G_2. The incorporation of additional PSS can contribute to the damping of these modes since the existing PSS are installed to synchronous generator G_1, and G_3 only.

2.6 Simulation Validation

The AC/DC test system as shown in Figure 2- 5 has been established in RSCAD to validate the results of modal analysis. The power flow data, AC voltages, and impedance values are based on 4-generator 2-area benchmark system model in [6] where same parameters are used in 2.5.2.

The purpose of using RTDS-based simulation and testing platform is due to the fact that it can provide an effective solution for such a development with the following benefits:

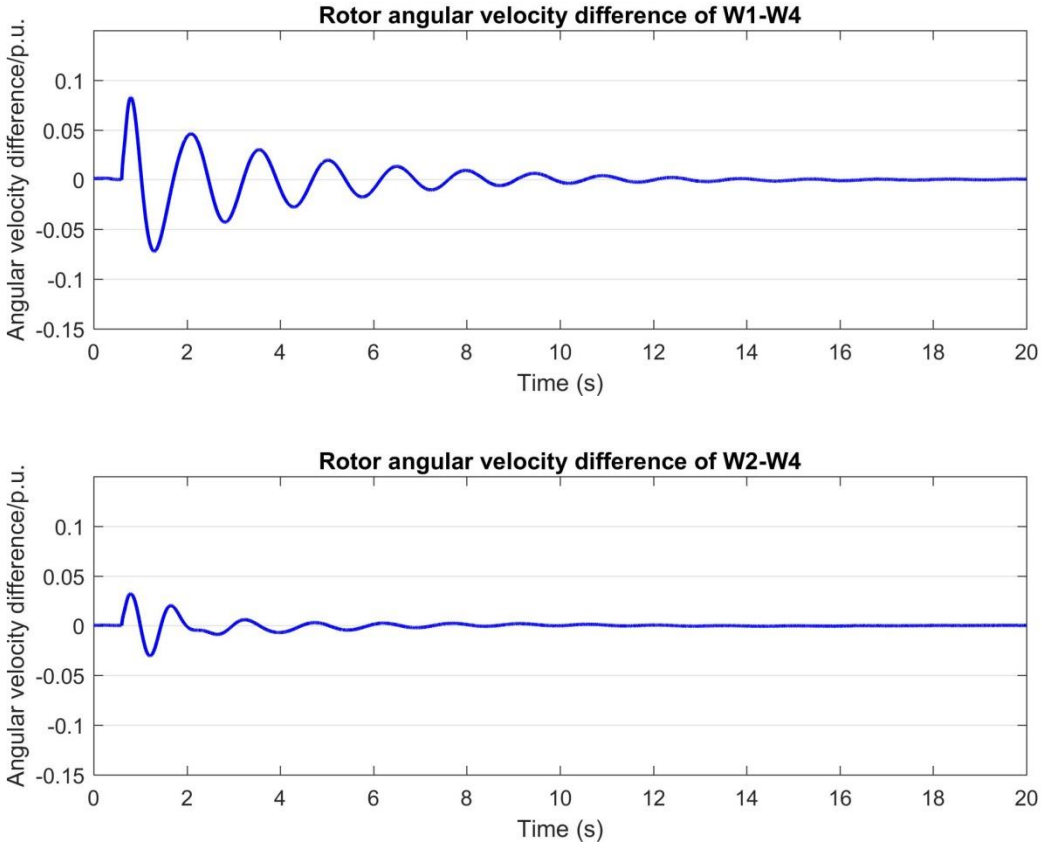
1. In the RSCAD environment (RSCAD is the specifically-designed software platform for power system modelling and interfacing to RTDS hardware), the power electronic devices can be represented using detailed models in close to practical devices. In this way, it can reflect the steady-state and dynamic characteristics of power electronic devices (including VSC FACTS and VSC HVDC devices);

2. With specifically-designed multiple processing units for digital simulation, the computational capability of RTDS hardware can be powerful enough to achieve real-time simulation. In doing so, the simulation efficiency of RTDS can satisfy the requirements for multi-scenario detailed analysis of power electronic devices;
3. RTDS can provide the function of hardware-in-the-loop to realise the interactions between the simulated virtual power networks in RSCAD and those physical protective relays and hardware-based controllers.

2.6.1 Small Disturbances

Small disturbances (changes of reference) are applied to AC/DC test system to validate the result of modal analysis to investigate small signal stability of the test system. A step reference change is applied to VSC_2, with V_{dc2ref} changes from 2.0 (p.u.) to 2.1 (p.u.) at 0.6s.

The dynamic response of rotor angular velocity difference of synchronous generators 1-4 in response to the small disturbance are shown in Figure 2- 6. The damping frequency and damping ratio of difference of synchronous generators seen from the figure are in line with modal analysis results.



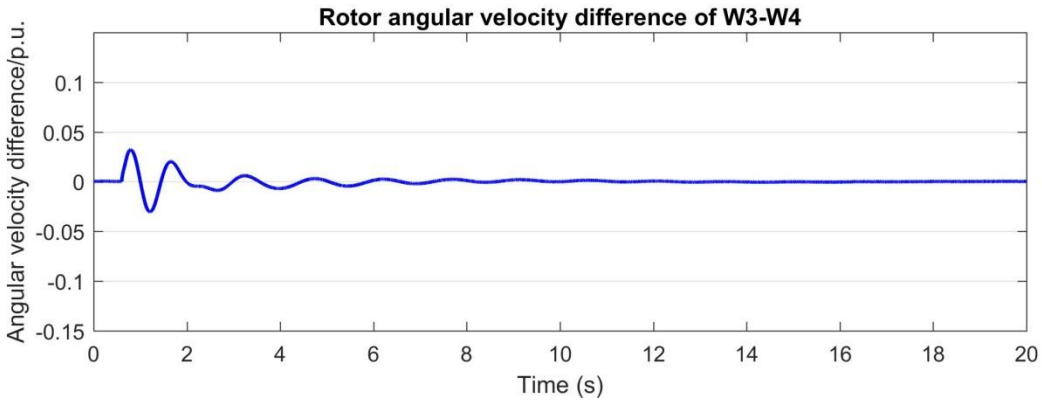
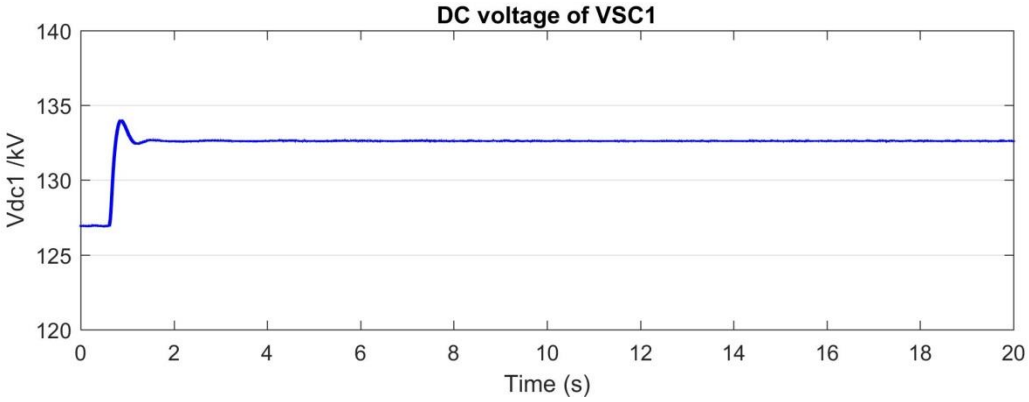
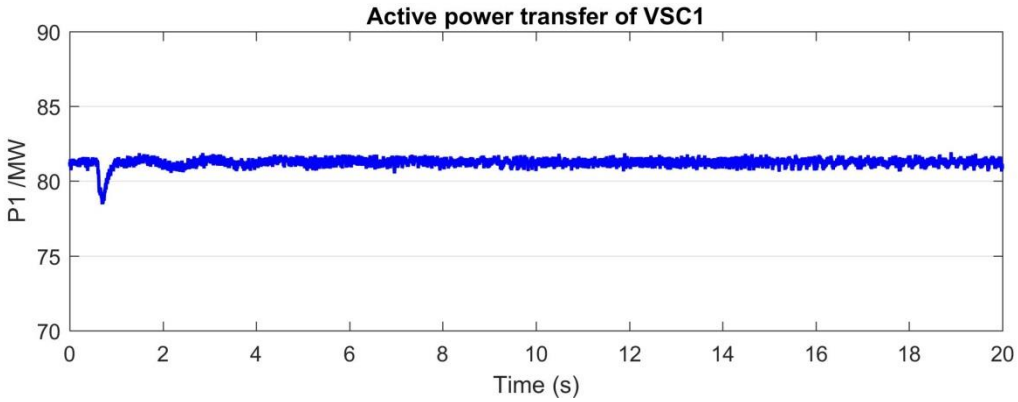


Figure 2- 6 Rotor angular velocity differences of synchronous generators 1-4.

The dynamic response of VSC related data of VSC_1, VSC_2, and VSC_3, including DC voltage, active power transfer, and AC voltage are shown in Figure 2- 7 to Figure 2- 9. It can be seen from the figures that the DC voltages of all VSC reached a new steady state after a short period of time while active power transfer and AC voltage recovers to their former value after the disturbance. This is due to the control system of all VSC are set to AC voltage regulation in *q* axis. The VSC_2 is set to DC voltage regulation, while VSC_1 and VSC_3 are set to active power transfer control.





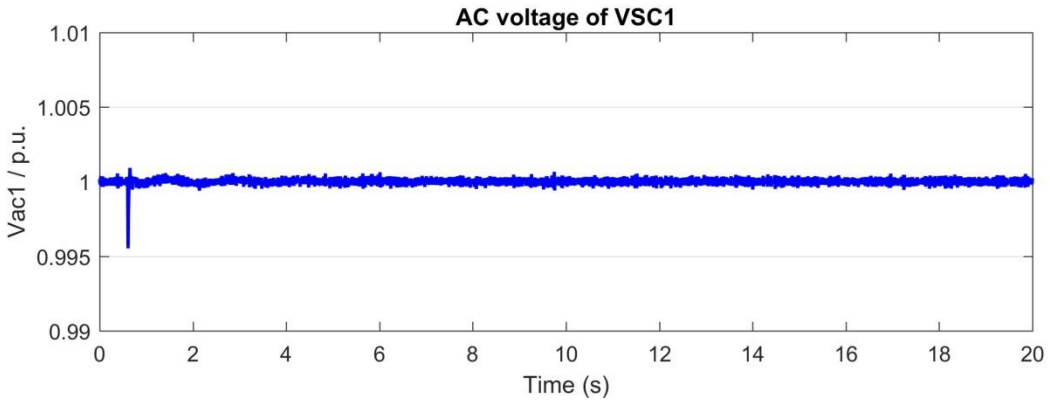
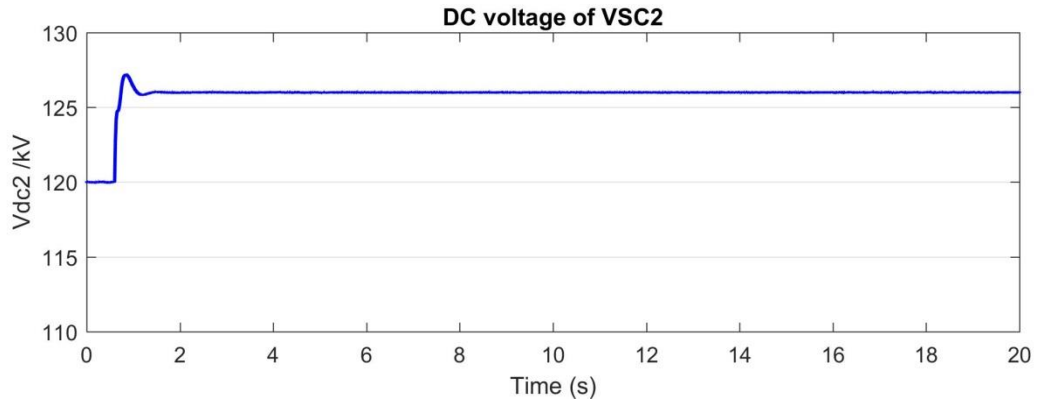
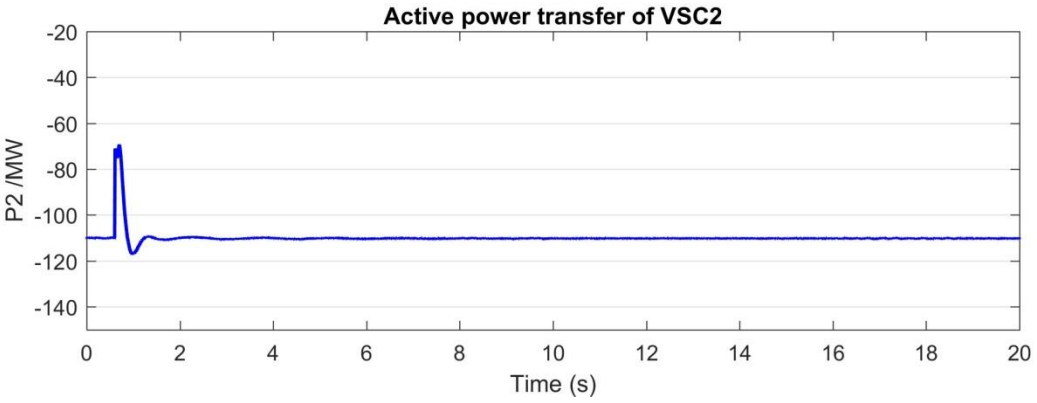


Figure 2- 7 Dynamic response of VSC1 against small disturbance.





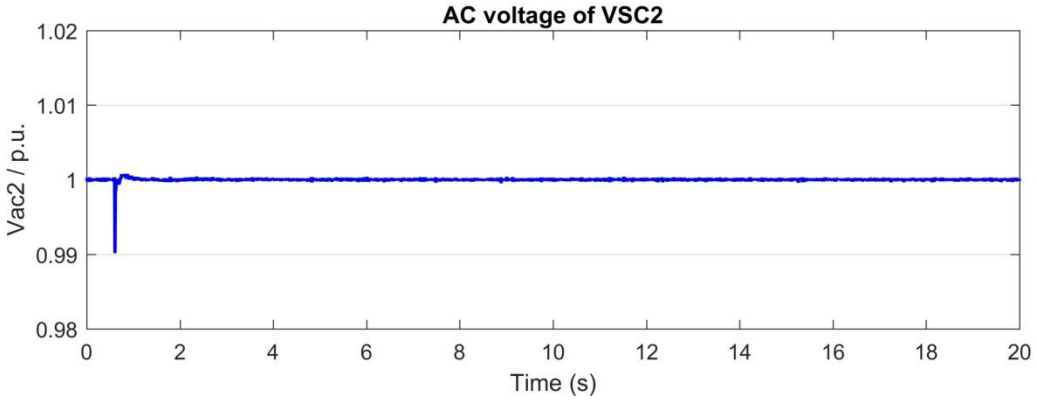


Figure 2- 8 Dynamic response of VSC2 against small disturbance.

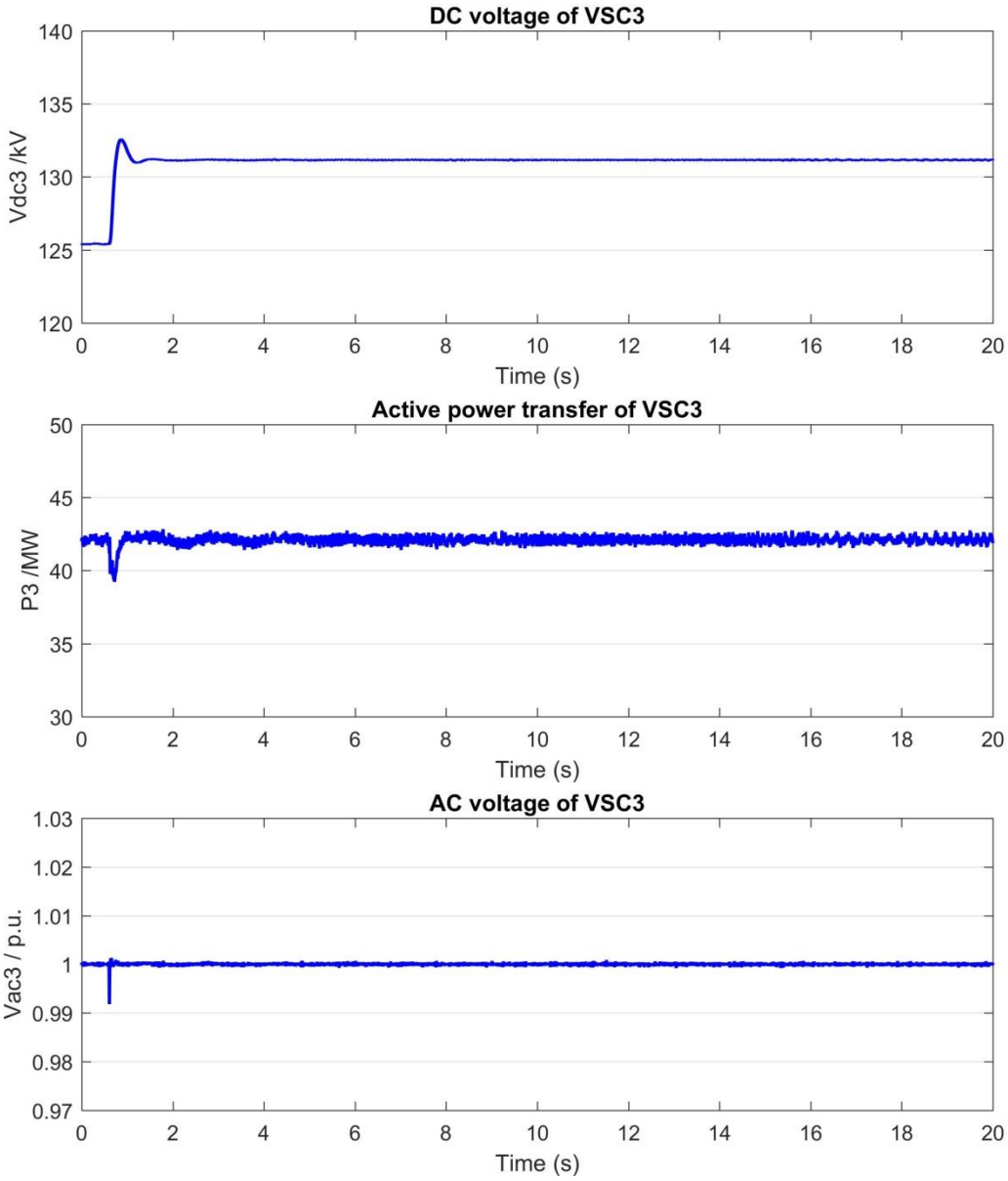


Figure 2- 9 Dynamic response of VSC3 against small disturbance.

The dynamic response of DC network, including current of DC branch 12, 13 and 23 are shown in Figure 2- 10. It can be seen from the figures that the currents of all DC braches reach to a new steady states after a short period of time. And small oscillations of DC branch 13 are seen since no DC current flow controller is applied to DC network and active power through branch 13 is not controlled. Stable dynamic performance against small disturbance can be seen from the simulation results, which is in line with the modal analysis results.

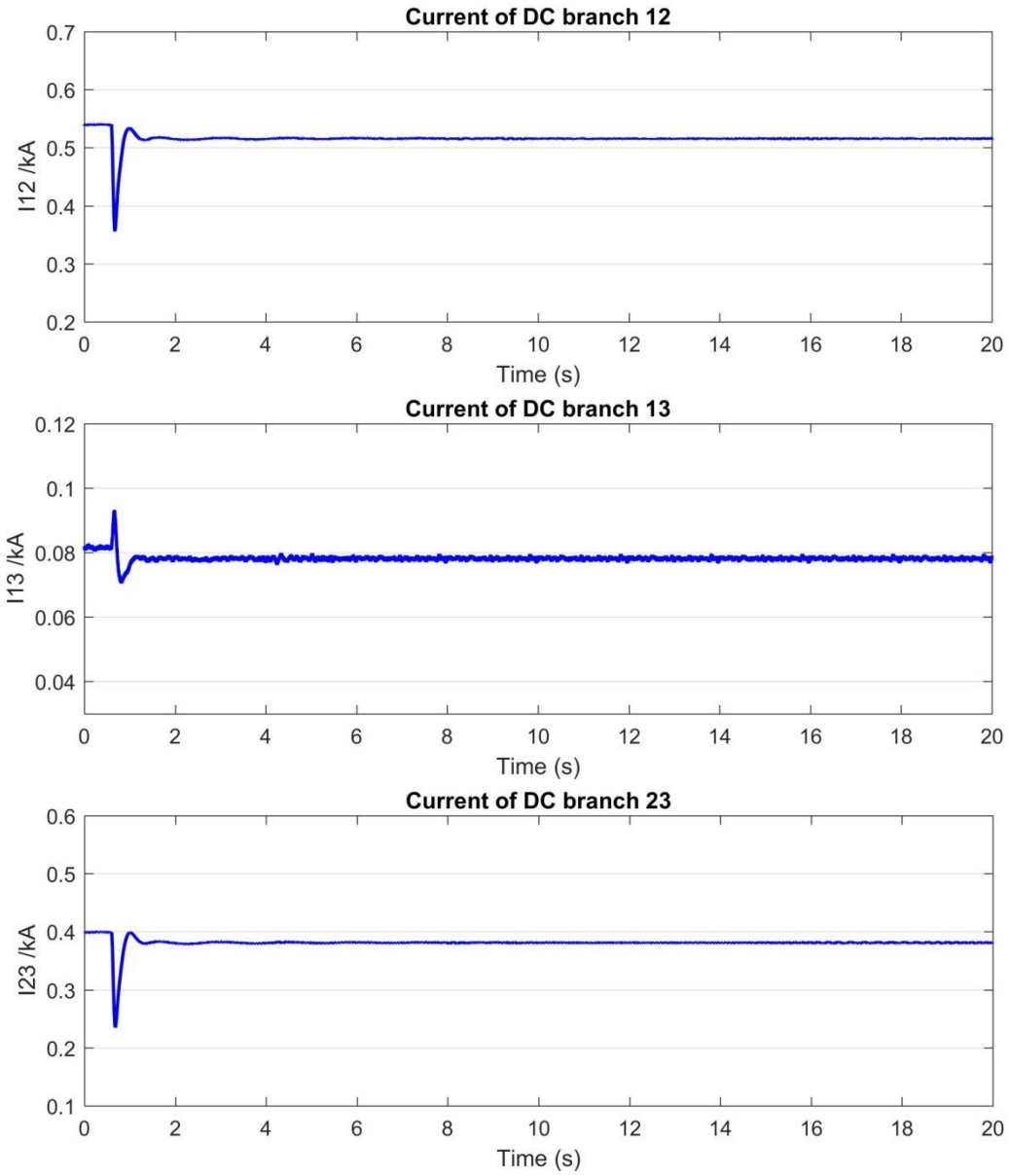


Figure 2- 10 Dynamic response of DC network.

2.6.2 Large Disturbances

AC-System fault

A large disturbance is applied to test the stability of the system under large disturbances. A 10Ω single-line-to-ground (SLG) fault is simulated at PCC of VSC terminal 3 (primary side of coupling transformer) at 0.15s lasting for 7 cycles (116 ms).

The dynamic response of VSC related data of VSC_1, VSC_2, and VSC_3, including DC voltage, active power transfer, and AC voltage are shown in Figure 2- 11 to Figure 2- 13. It can be

seen from the figures that the DC voltages, active power transfer, and AC voltage of all VSC recovers to their former values after the disturbance.

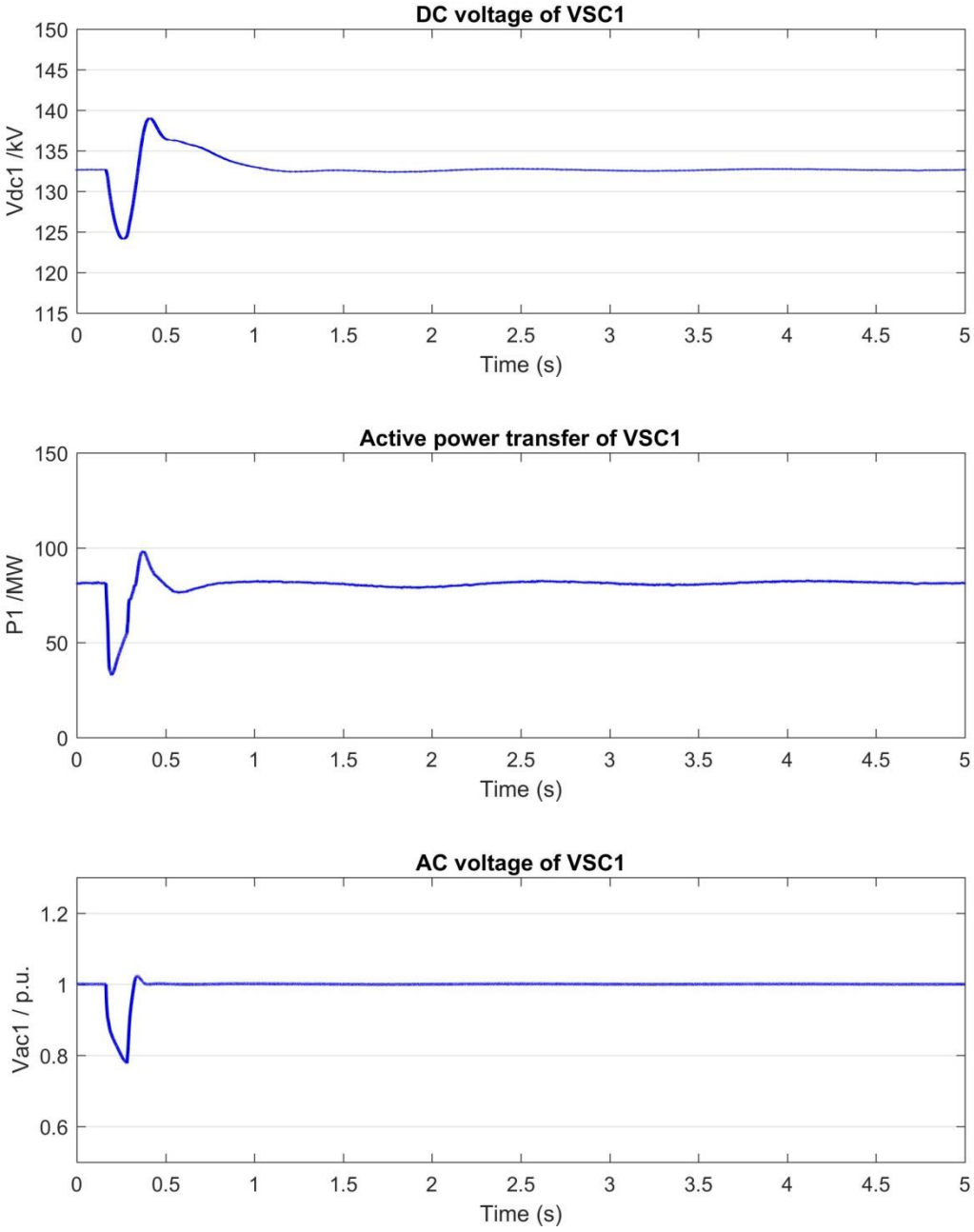


Figure 2- 11 Dynamic response of VSC1 against AC system fault.

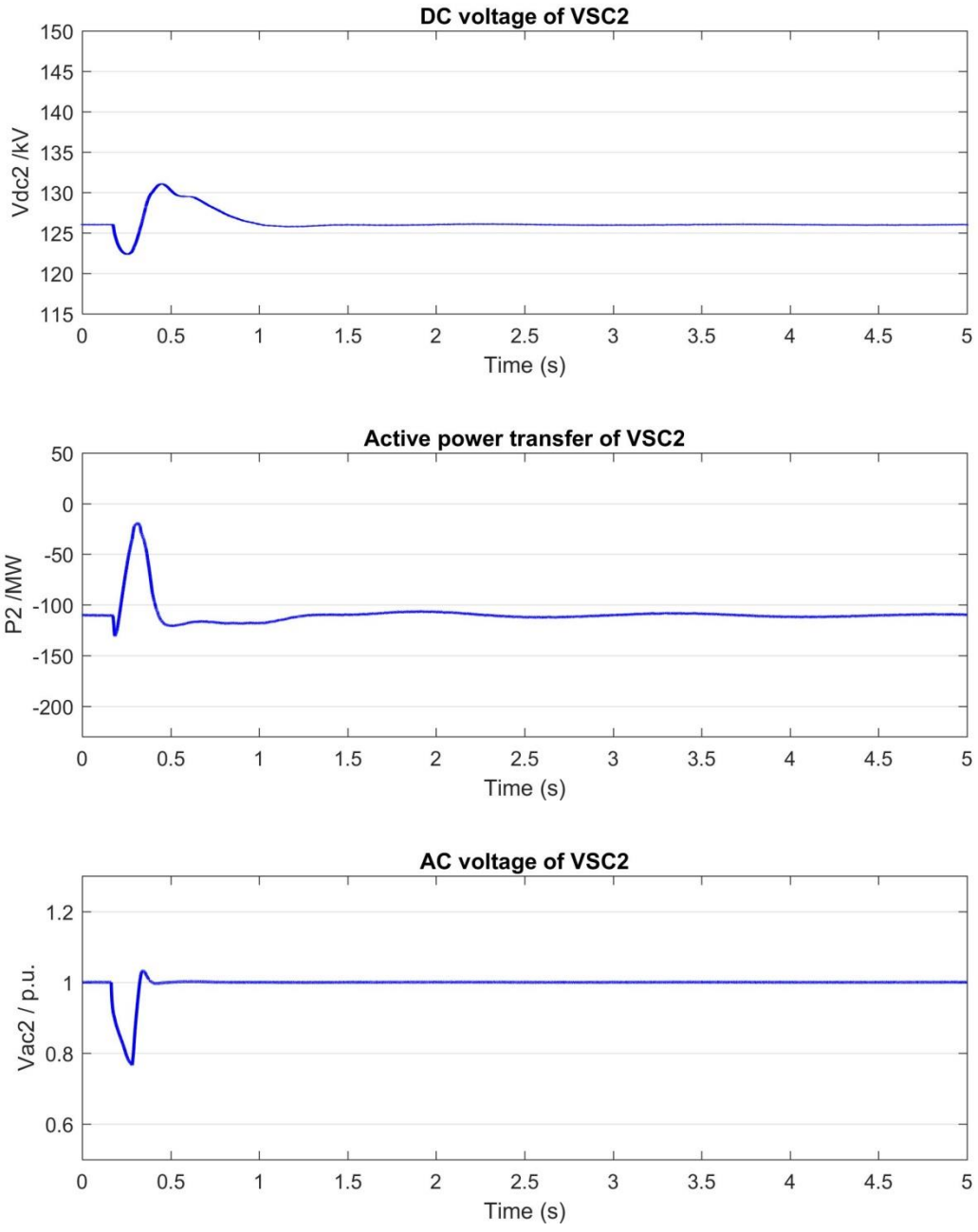
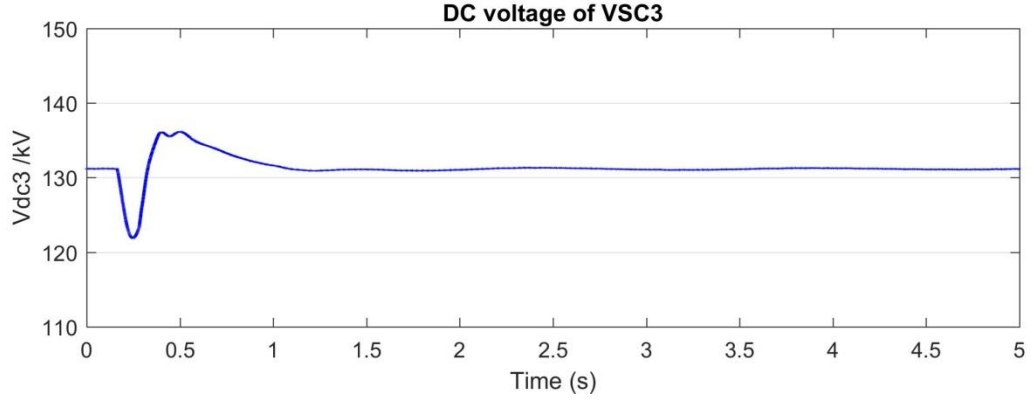


Figure 2- 12 Dynamic response of VSC2 against AC system fault.



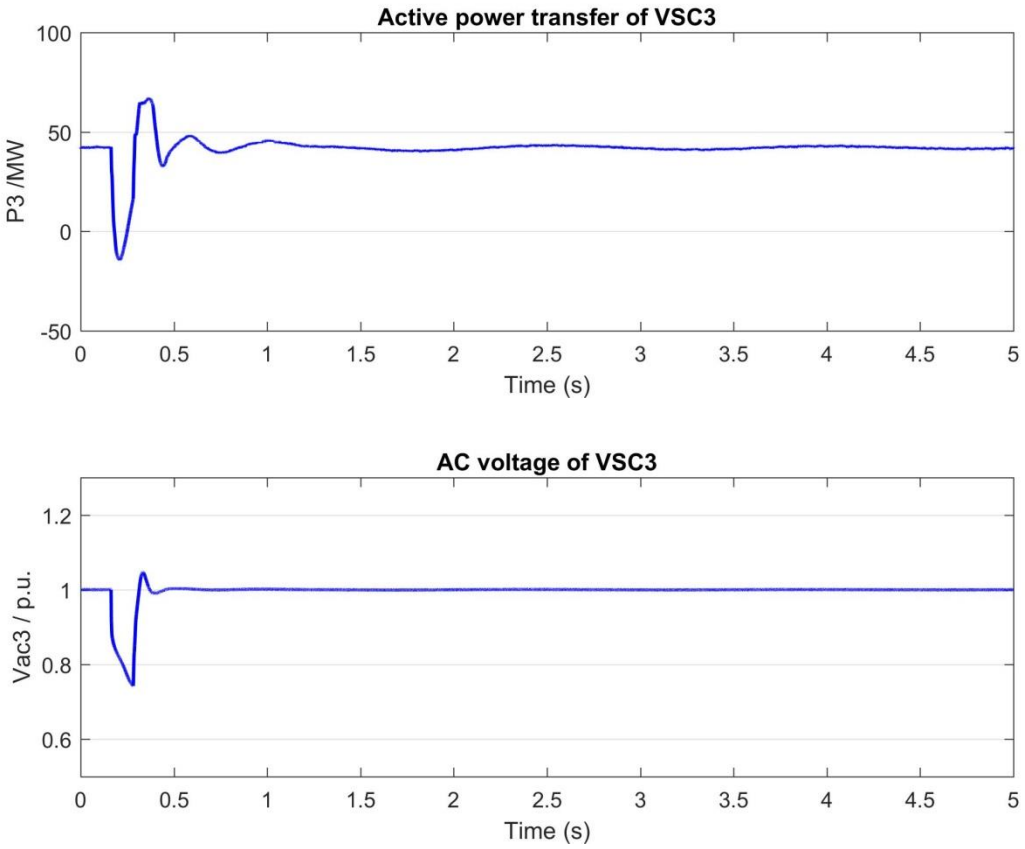
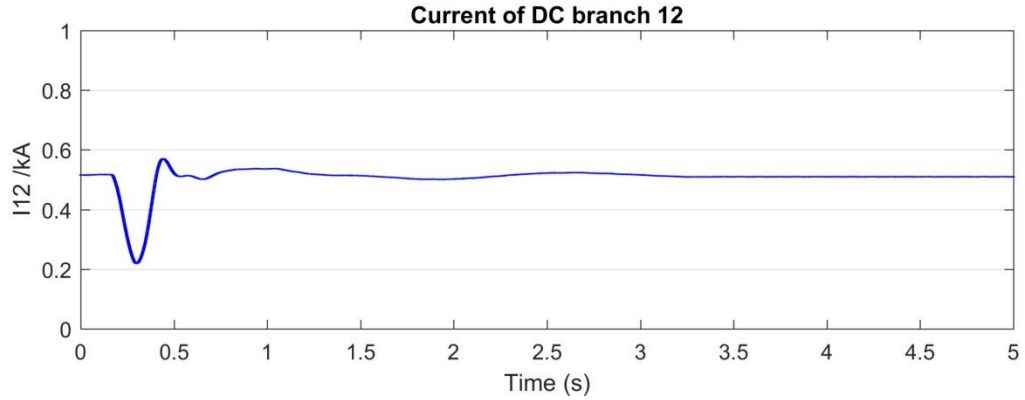


Figure 2- 13 Dynamic response of VSC3 against AC system fault.

The dynamic response of DC network, including currents of DC branch 12, 13 and 23 are shown in Figure 2- 14. It can be seen from the figures that the currents of all DC braches recover to its former values after the fault. The simulation results against large AC system fault demonstrate that the system can endure large AC disturbance.



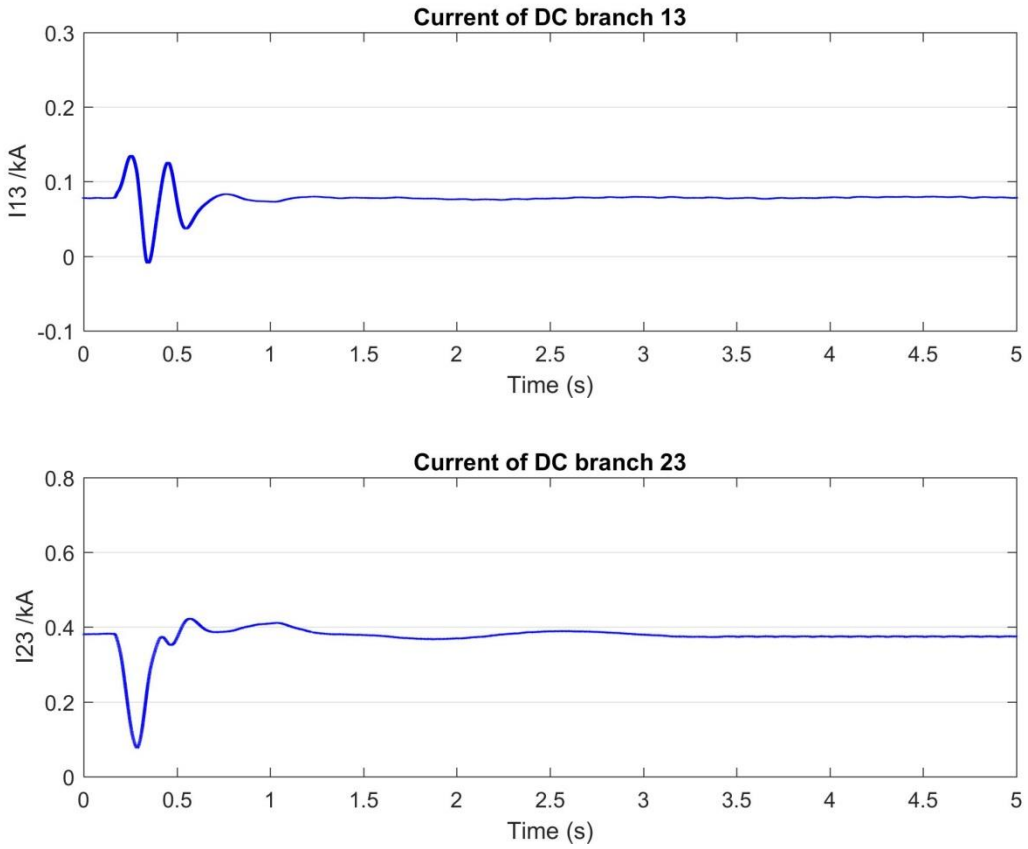
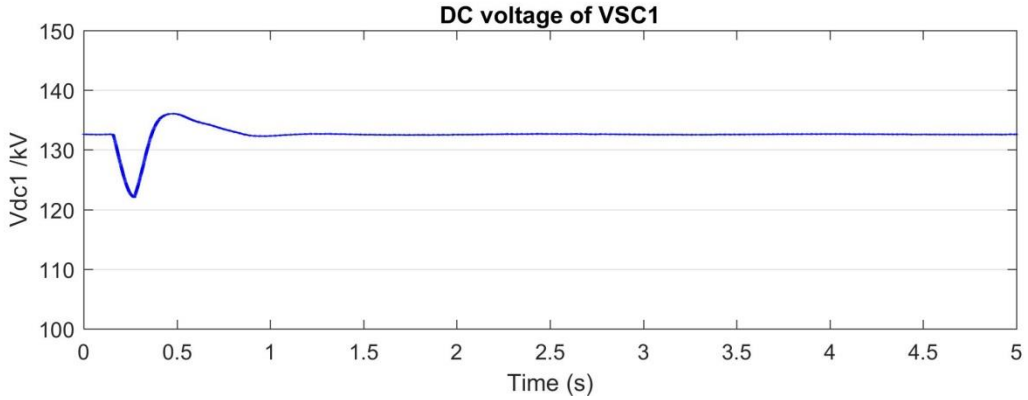


Figure 2- 14 Dynamic response of DC network against AC system fault.

DC Cable fault

For the testing of large disturbance at DC side, a 25 Ω line-to-ground DC-cable fault is simulated at DC-side of VSC3 at 0.15s lasting for 7 cycles (116 ms).

The dynamic response of VSC related data of VSC_1, VSC_2, and VSC_3, including DC voltage, active power transfer, and AC voltage are shown in Figure 2- 15 to Figure 2- 17. It can be seen from the figures that the DC voltages, active power transfer, and AC voltage of all VSC recovers to their former values after the DC cable fault.



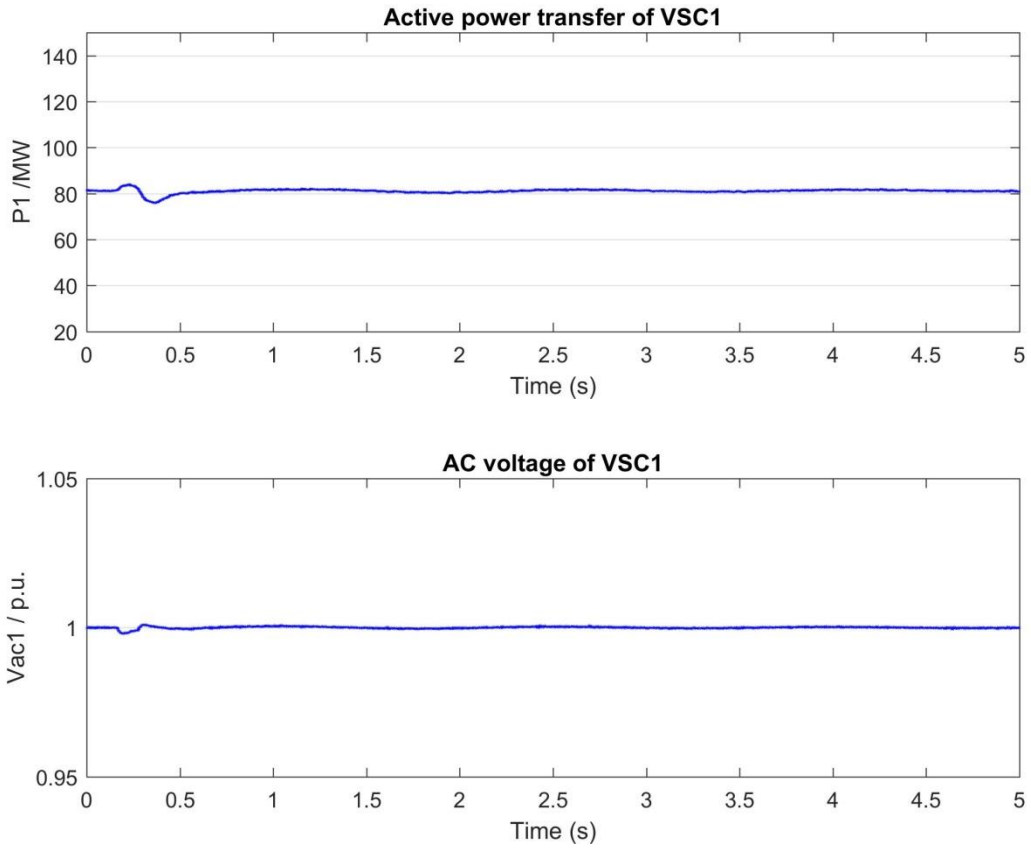
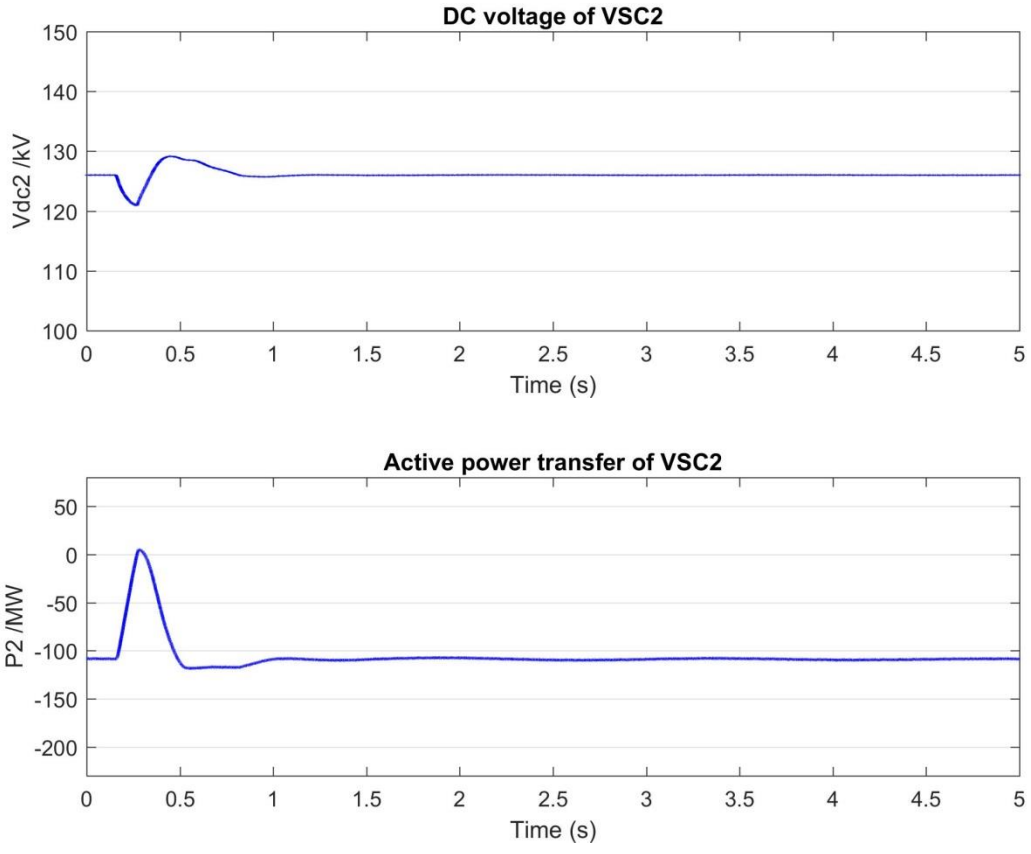


Figure 2- 15 Dynamic response of VSC1 against DC cable fault.



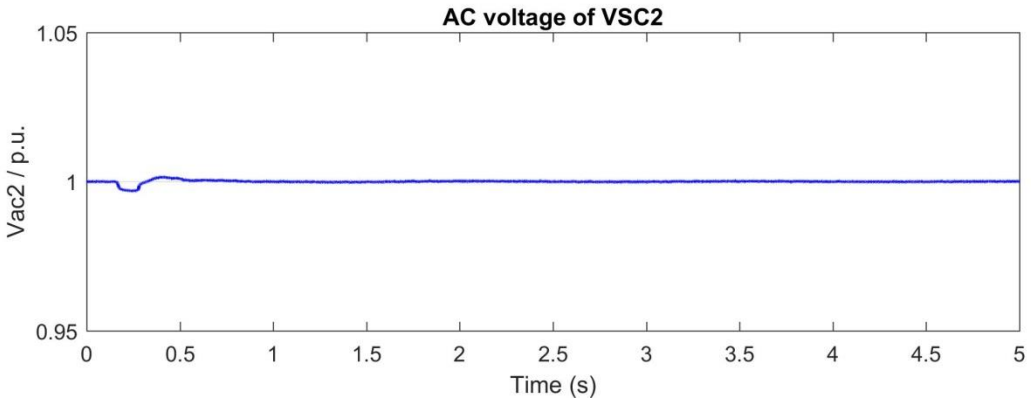
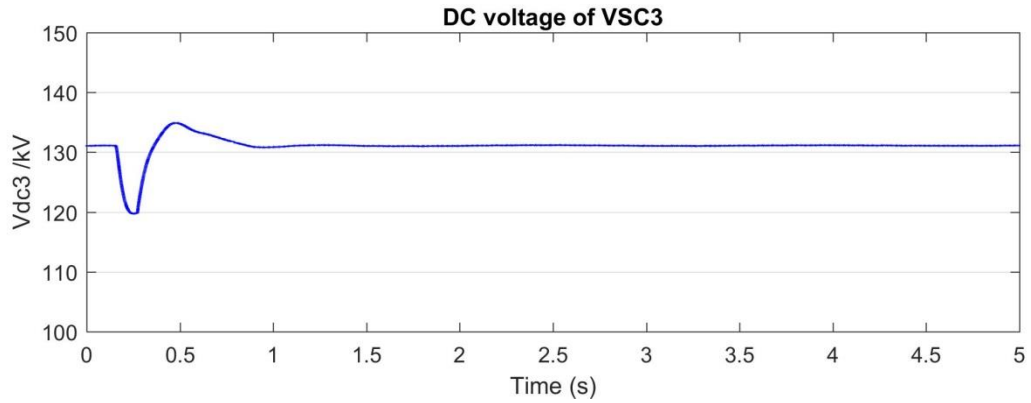
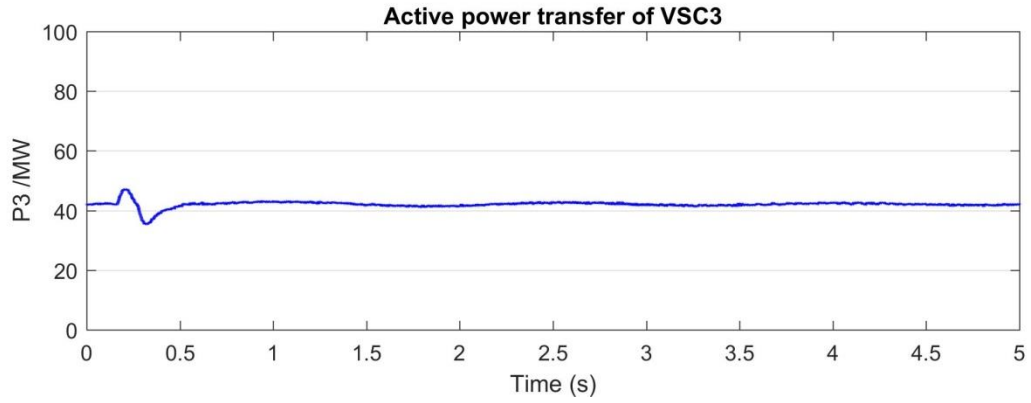


Figure 2- 16 Dynamic response of VSC2 against DC cable fault.





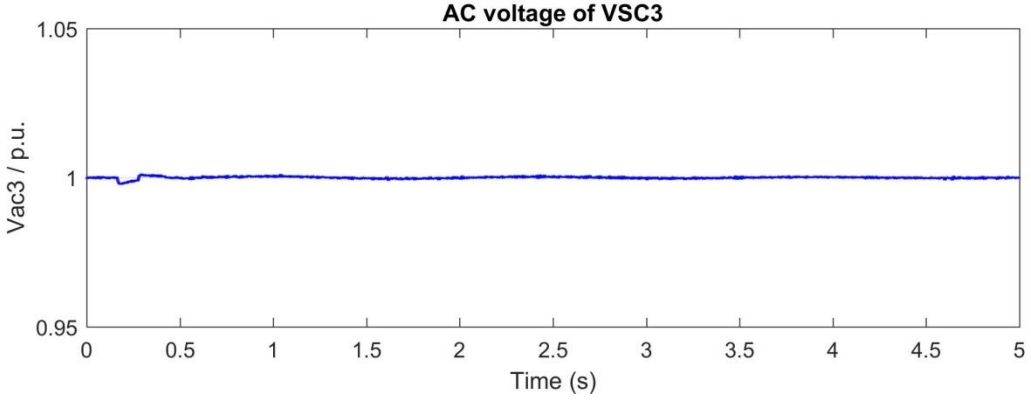


Figure 2- 17 Dynamic response of VSC3 against DC cable fault.

The dynamic response of DC network, including current of DC branch 12, 13 and 23 are shown in Figure 2- 18. It can be seen from the figures that the currents of all DC braches recover to its former values after the fault. The simulation results against DC cable fault demonstrate that the system can endure large DC disturbance.

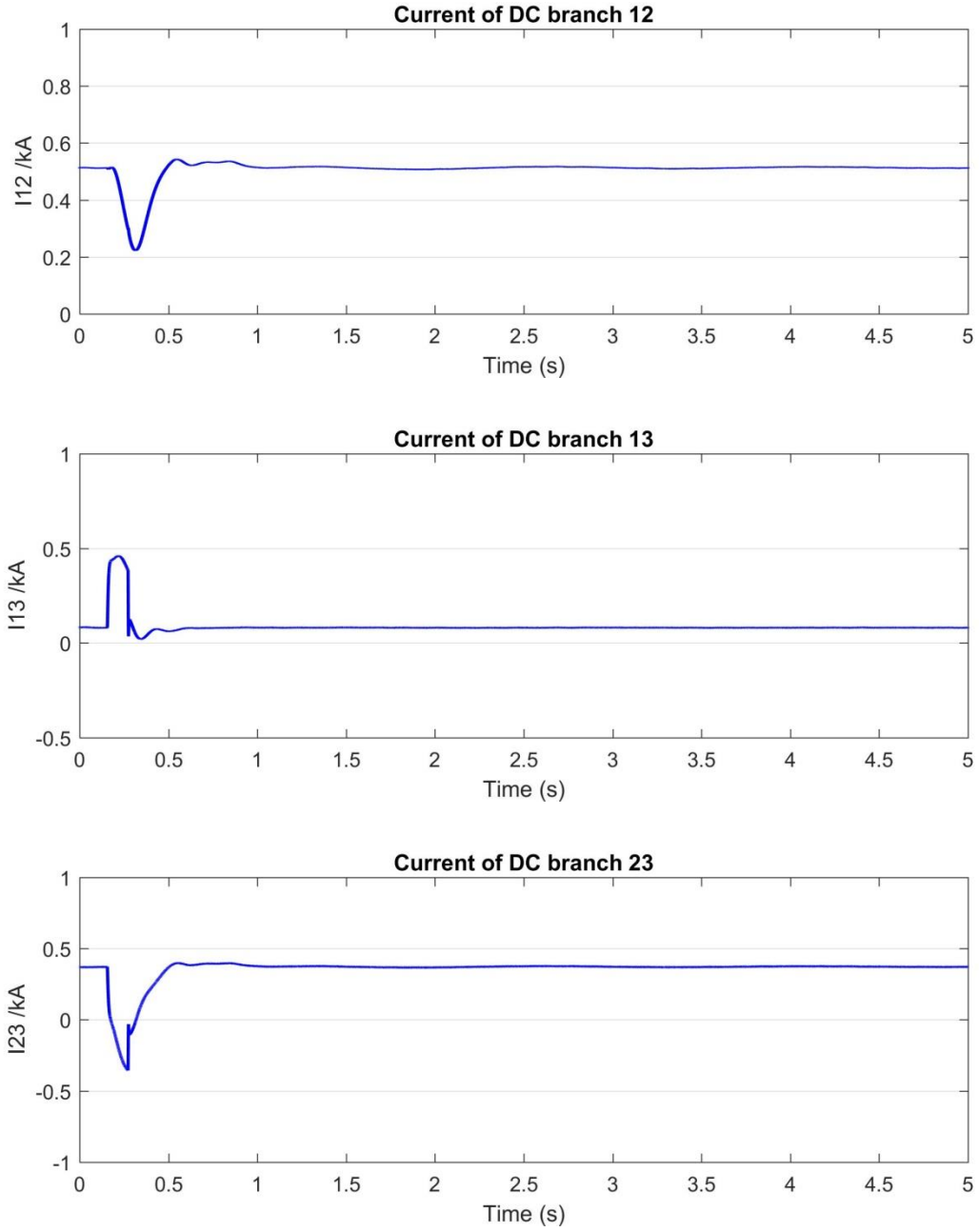


Figure 2- 18 Dynamic response of DC network against DC cable fault.

2.7 Summary

In this chapter, AC power system including synchronous generator with excitation system and PSS, and network power flow has been modelled in dynamic and algebraic equations. MTDC system without CFC, including VSC with its control system and generalized DC network without CFC has been modelled in dynamic equations. Dynamic model of these two subsystems have been linearized and formulated to form state-space representation of multi-model system for small-signal stability analysis. An integrated AC/DC system that consists of multiple synchronous generators with excitation system and PSS, multiple VSC converters, and DC network without CFC, has been established. Small-signal model of test system has been derived based on approaches in 2.2-2.4 and the eigenvalues of state-space representation of test system have been calculated. Modal analysis of the eigenvalues results has been performed to study small-signal stability of VSC-based MTDC system without CFC.

It can be found from eigenvalue results that all 52 eigenvalues have non-positive real part. This indicates a stable operating condition at the considered operating point. There are two zero eigenvalues, as there is no infinite bus bar in the testing network. One of the eigenvalue arises from a redundancy in synchronous generator angle. The second zero eigenvalue results from that the generator torque is independent of machine speed deviations, and this is because mechanical damping is neglected and governor action is not represented. If the rotor angle and angular velocity of one synchronous machine are regarded as references, and the governor action of mechanical damping is considered, the two zero eigenvalues will be reduced. All the conjugate pairs of complex eigenvalues are related to the dominant state variables of synchronous generators according to their participation factors. The damping of these modes is mainly affected by synchronous generator setting, associated exciter setting, and corresponding power system stabilizer parameters.

Simulations results of established AC/DC system against small disturbances in aspects of damping frequency and damping ratio of difference of synchronous generators are in line with modal analysis results. A stable operating condition around operating point is seen from simulation results in RTDS/RSCAD against both small disturbance of change of reference and large disturbances (including AC system faults, and DC cable faults), which is in line with modal analysis results.

CHAPTER 3 SMALL-SIGNAL STABILITY ANALYSIS OF VSC BASED MTDC SYSTEM WITH DC CFC

3.1 Introduction

This chapter presents the dynamic modelling of the integrated MTDC/AC system with integration of CFC to study the small-signal stability of VSC-based MTDC system with CFC and the potential interactions between CFC and VSC. In 3.2, the modelling of DC network with CFC and its control system is presented in dynamic equations. The small-signal state-space model of DC network with CFC is linearized around equilibrium point. Then the linearized state-space model of the subsystem of DC network with CFC is merged into VSC-based MTDC system without CFC presented in Chapter 2 to formulate multi-model system with CFC. In 3.3, a test system that consists of multiple synchronous generators with excitation system and PSS, multiple VSC converters, and DC network with CFC, is established. Small-signal model of test system is derived based on approaches presented in Chapter 2 and the eigenvalues of state-space representation of the test system are calculated. Modal analysis of calculated eigenvalues in comparison between integrated AC/DC system without/with CFC is implemented to study the impacts of the incorporation of CFC, and its control parameters on small-signal stability of the integrated AC/DC system. Simulations results of established AC/DC system against small disturbances and large disturbances (including AC system faults, and DC cable faults) in RTDS/RSCAD are analysed to validate modal analysis results. Eigenvalue trajectories are used to study the potential interactions between CFC and VSC, including impacts of control parameters of CFC on VSC, and impacts of control parameters of VSC on CFC.

3.2 Modelling, Linearization and Formulation of VSC Based MTDC System with CFC

3.2.1 Modelling of DC Network with CFC

The meshed MTDC networks are currently facing an operational challenge, which is that the DC branch currents cannot be fully controlled. Existing DC current flow control approaches are only capable of regulating a certain branch current. Recently, CFC emerges as a DC-DC converter based device which can provide multi-line flexible current flow control in a simple meshed DC network.

Figure 3- 1 shows the single-line diagram of the topology of a two-line CFC that is integrated to a VSC based three-terminal DC network [84,86]. The CFC model consists of two identical full-bridge DC-DC converter modules sharing a common capacitor, which is used as a channel for the power exchange between two bridge converter modules. These two DC-DC converter modules can be controlled independently. The branch currents of the CFC installed meshed DC network can be fully controlled, by use of designed switching patterns of the DC-DC converter modules of CFC.

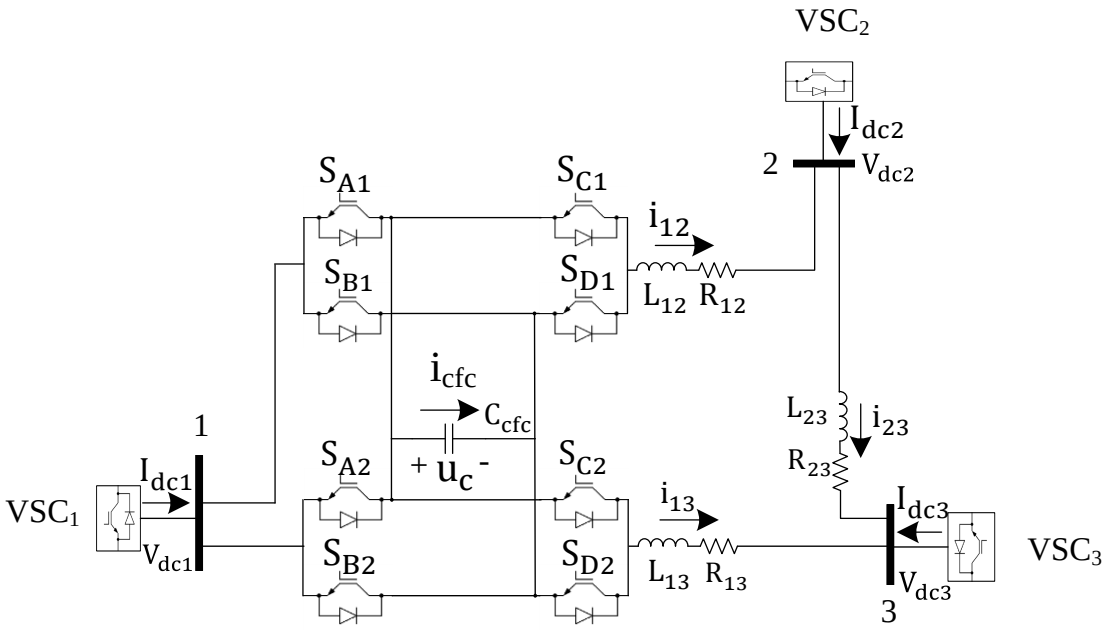


Figure 3- 1 Single-line diagram of the topology of a two-line CFC.

As shown in Figure 3- 1, one DC-DC converter consists of two legs, with two switches (which consist of IGBT with anti-parallel diode) on each leg. S_{Ai} and S_{Bi} (i = 1,2) are on same leg, whilst S_{Ci} and S_{Di} (i = 1,2) are on the other leg. Two switches on the same leg are switched complementarily. This switching manner ensures the energy storage capacitor works in two operational modes (charging or discharging) as shown in Table 3- 1. The

capacitor is charging when both S_A and S_D are on, while the capacitor is discharging when both S_B and S_C are on.

Table 3- 1 DC-DC converter operational modes

DC-DC CONVERTER OPERATIONAL MODES

Mode	Capacitor State	S_A	S_B	S_C	S_D
1	Charging	ON	OFF	OFF	ON
2	Discharging	OFF	ON	ON	OFF

The target of the CFC control system is to maintain the voltage across the capacitor and to control DC current of a certain DC transmission line branch, for example i_{12} in this case.

The duty cycles of switch-on state of all the switches in two full-bridge module are shown in Table 3- 2.

Table 3- 2 Switch duty cycles

SWITCH DUTY CYCLES

Switches	S_{A1}, S_{A2}	S_{B1}, S_{B2}	S_{C1}	S_{D1}	S_{C2}	S_{D2}
Duty Cycles	d_a	$1 - d_a$	d_{c1}	$1 - d_{c1}$	d_{c2}	$1 - d_{c2}$

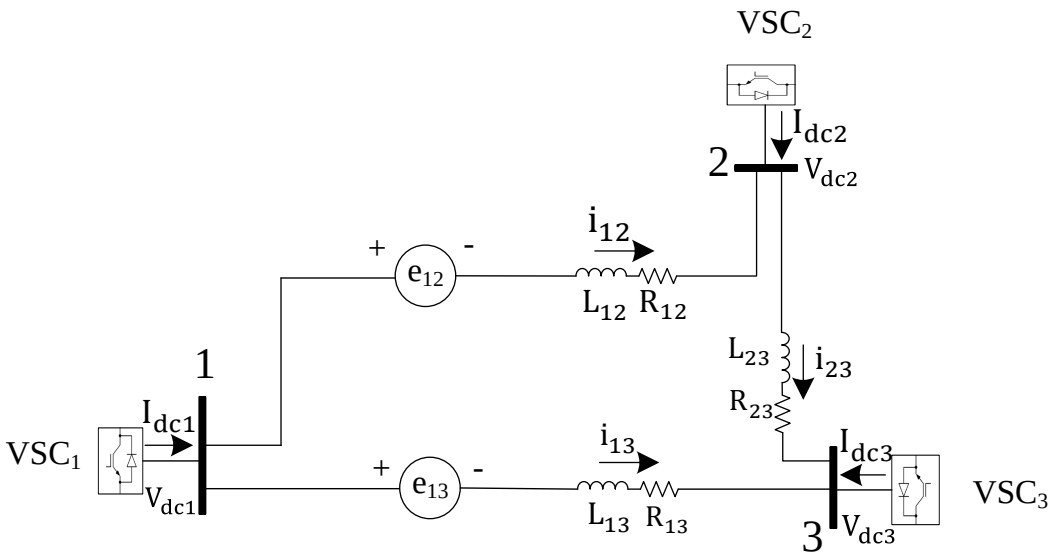


Figure 3- 2 Equivalent circuit of two-line CFC.

By this operation manner, the voltages across DC-DC converter in two DC branch, e_{12} and e_{13} can be regarded as two voltage sources as shown in Figure 3- 2, and current through CFC i_{cfc} , can be summarized as in Table 3- 3.

Table 3- 3 Switching modes of CFC.

SWITCHING MODES OF CFC

Switching Mode	Switches On	Duty Cycle	e_{12}	i_{cfc}
1	S_{A1}, S_{C1}	a_1	0	0
2	S_{A1}, S_{D1}	a_2	u_c	i_{12}
3	S_{B1}, S_{C1}	a_3	$-u_c$	$-i_{12}$
4	S_{B1}, S_{D1}	a_4	0	0
Switching Mode	Switches On	Duty Cycle	e_{13}	i_{cfc}
5	S_{A2}, S_{C2}	b_1	0	0
6	S_{A2}, S_{D2}	b_2	u_c	i_{13}
7	S_{B2}, S_{C2}	b_3	$-u_c$	$-i_{13}$
8	S_{B2}, S_{D2}	b_4	0	0

The duty cycles in Table 3- 3 can be derived as follows:

$$a_1 = min\{d_{c1}, d_a\} \quad (3.1)$$

$$a_2 = max\{d_a - d_{c1}, 0\} \quad (3.2)$$

$$a_3 = min\{d_{c1} - d_a, 0\} \quad (3.3)$$

$$a_4 = 1 - max\{d_a, d_{c1}\} \quad (3.4)$$

$$b_1 = min\{d_{c2}, d_a\} \quad (3.5)$$

$$b_2 = max\{d_a - d_{c2}, 0\} \quad (3.6)$$

$$b_3 = min\{d_{c2} - d_a, 0\} \quad (3.7)$$

$$b_4 = 1 - max\{d_a, d_{c2}\} \quad (3.8)$$

Hence the voltages across DC-DC converter in two coupling DC branch e_{12}, and e_{13} can be expressed with corresponding duty cycles as:

$$e_{12} = (a_2 - a_3)u_c = (d_a - d_{c1})u_c \quad (3.\ 9)$$

$$e_{13} = (b_2 - b_3)u_c = (d_a - d_{c2})u_c \quad (3.\ 10)$$

And by considering the charging and discharging states of the capacitor within a switching cycle, the dynamic of capacitor can be obtained as:

$$C\frac{du_c}{dt} = (a_2 - a_3)i_{12} + (b_2 - b_3)i_{13} = (d_a - d_{c1})i_{12} + (d_a - d_{c2})i_{13} \quad (3.\ 11)$$

The target of control system of the two-line CFC is to regulate the duty cycle ratio of the switches so that the voltage across the capacitor is maintained and the current of DC branch (i_{12} in this study) is controlled.

Figure 3- 3 shows the architecture of CFC control system to output duty cycle ratio of the switches. The DC branch current i_{12}, reference of DC branch current i_{12}^*, capacitor voltage u_c, and reference of capacitor voltage u_c^* are inputs of the control system. The difference of i_{12}^* and i_{12} is inputted into a PI control loop and the first limitation block. Then the output of the first limitation block (which yields $d_a - d_{c1}$), is subtracted from d_a and inputted into the second limitation block. The output signal of the second limitation block is d_{c1}. Similarly, the difference of u_c^* and u_c is inputted into a PI control loop and the first limitation block. Then the output of the first limitation block (which yields $d_a - d_{c2}$), is subtracted from d_a and inputted into the second limitation block. The output signal of the second limitation block is d_{c2}. And by use of same kind of gate signal generator that is commonly used in VSC, the gate signals G_{SC1}, and G_{SC2} to control the switches are generated.

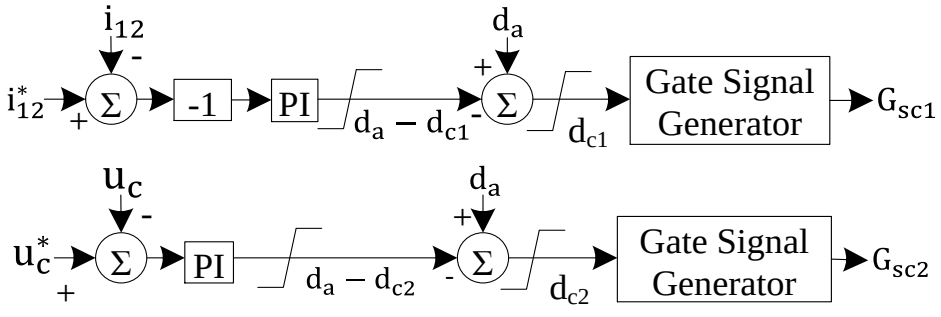


Figure 3- 3 Architecture of CFC control system.

In this way, the duty cycle reference d_{c1}, and d_{c2} can be obtained as:

$$d_{c1} = d_a - k_{pc1}(-i_{12}^* + i_{12}) - k_{ic1}\int(-i_{12}^* + i_{12})dt$$

$$= d_a - k_{pc1}(-i_{12}^* + i_{12}) - k_{ic1}y_1 \quad (3.12)$$

$$d_{c2} = d_a - k_{pc2}(u_c^* - u_c) - k_{ic2}\int (u_c^* - u_c)dt$$

$$= d_a - k_{pc2}(u_c^* - u_c) - k_{ic2}y_2 \quad (3.13)$$

where

k_{pc1}, k_{ic1}, k_{pc2}, and k_{ic2} : the proportional and integral gains of the PI control loops of CFC control system

y_1 and y_2 : auxiliary state variables to represent integral parts of the PI control loops

Applying Kirchhoff's voltage law, the dynamic equations of all DC braches of the three-terminal DC network with CFC can be derived as:

$$L_{12}\frac{di_{12}}{dt} + R_{12}i_{12} = V_{dc1} - V_{dc2} - e_{12} \quad (3.14)$$

$$L_{13}\frac{di_{13}}{dt} + R_{13}i_{13} = V_{dc1} - V_{dc3} - e_{13} \quad (3.15)$$

$$L_{23}\frac{di_{23}}{dt} + R_{23}i_{23} = V_{dc2} - V_{dc3} \quad (3.16)$$

The final mathematical dynamic equations of DC network with CFC can be obtained by substitute (3.9)-(3.10), (3.12), and (3.13), into (3.11), and (3.14)-(3.16), with auxiliary state variable dynamics as follows:

$$\frac{dy_1}{dt} = -i_{12}^* + i_{12} \quad (3.17)$$

$$\frac{dy_2}{dt} = u_c^* - u_c \quad (3.18)$$

3.2.2 Linearization of DC Network with CFC

The linearization of the dynamic equations of DC network with CFC (3.11), (3.14)-(3.18) can be expressed as follows:

$$\Delta\dot{x}_{CFC} = \boldsymbol{A_{CFC}}\Delta x_{CFC} + \boldsymbol{A_{CFC2}}\Delta x_{Vdc} + \boldsymbol{E_{CFC}}\Delta u_{CFC} \quad (3.19)$$

where

$$\Delta x_{CFC} = [\Delta i_{12}, \Delta i_{13}, \Delta i_{23}, \Delta u_c, \Delta y_1, \Delta y_2,]^T \quad (3.20)$$

$$\Delta x_{Vdc} = [\Delta V_{dc1}, \Delta V_{dc2}, \Delta V_{dc3}]^T \quad (3.21)$$

$$\Delta u_{CFC} = [\Delta i_{12}^*, \Delta u_c^*]^T \quad (3.22)$$

3.2.3 Formulation of Multi-Model System

The independent linearized models of AC power system, MTDC system without CFC, and DC network with CFC studied in 2.4.1, 2.4.2, and 3.2.2 respectively, are formulated into a whole multi-model system, in order to investigate the small-signal stability of VSC–based MTDC system with CFC.

The DC network with CFC is integrated into MTDC system without CFC via VSC converters connected at VSC terminal of DC network, when CFC is installed into DC network. The state-space representation of DC network with CFC obtained in 3.2.2 is merged with the state-space representation of VSC obtained in 2.4.2 as follows:

$$\Delta\dot{x}_{MTDCCFC} = \boldsymbol{A_{MTDCCFC}}\Delta x_{MTDCCFC} + \boldsymbol{B_{MTDCCFC}}\Delta V_l + \boldsymbol{E_{MTDCCFC}}\Delta u_{MTDCCFC} \quad (3.23)$$

where

$$\Delta x_{MTDCCFC} = \left[\Delta {x_{VSC}}^T, \Delta {x_{CFC}}^T\right]^T \quad (3.24)$$

$$\Delta u_{MTDCCFC} = \left[\Delta {x_{VSC}}^T, \Delta {u_{CFC}}^T\right]^T \quad (3.25)$$

Finally, the linearized dynamic equations of MTDC system with CFC (3.23) can be merged with the linearized dynamic equations of all synchronous generators (2.52) using the same approach that presented in 2.4.3 as follows:

$$\Delta\dot{X}_{ACDCCFC} = \boldsymbol{A_{ACDCCFC}}\Delta X_{ACDCCFC} + \boldsymbol{B_{ACDCCFC}}\Delta U_{ACDCCFC} \quad (3.26)$$

where

$$\Delta X_{ACDCCFC} = \left[\Delta {x_{SGA}}^T, \Delta {x_{MTDCCFC}}^T\right]^T \quad (3.27)$$

$$\Delta U_{ACDCCFC} = \left[\Delta {u_g}^T, \Delta {u_{MTDCCFC}}^T\right]^T \quad (3.28)$$

3.3 Impacts of CFC on Small-Signal Stability of the Integrated AC/DC System

As CFC is integrated into MTDC system, the small-signal stability of the integrated AC/DC system is studied in this section to investigate the potential impacts of CFC that might be brought in. The modified test system is described in 3.3.1 with CFC installed into DC network. The modal analysis for the modified integrated AC/DC system is studied to investigate the small-signal stability in 3.3.2. The dynamic simulations in case of small disturbances and large disturbances are performed in 3.3.3 to validate modal analysis results. Finally, the impacts of the incorporation of CFC on existing MTDC system is studied in 3.3.4.

3.3.1 Test System

The single-line diagram of the topology of CFC integrated AC/DC system is shown in Figure 3- 4. The modified system is based on the MTDC system established in 2.5.1 which is added with a two-line CFC. As shown in Figure 3- 4, the CFC is located at the DC side of VSC_1 to control the current flow of DC branch i_{12} and i_{13}. The parameters of CFC are listed in Appendix A.9 while other parameters of existing MTDC system are the same with the test system in Chapter 2.

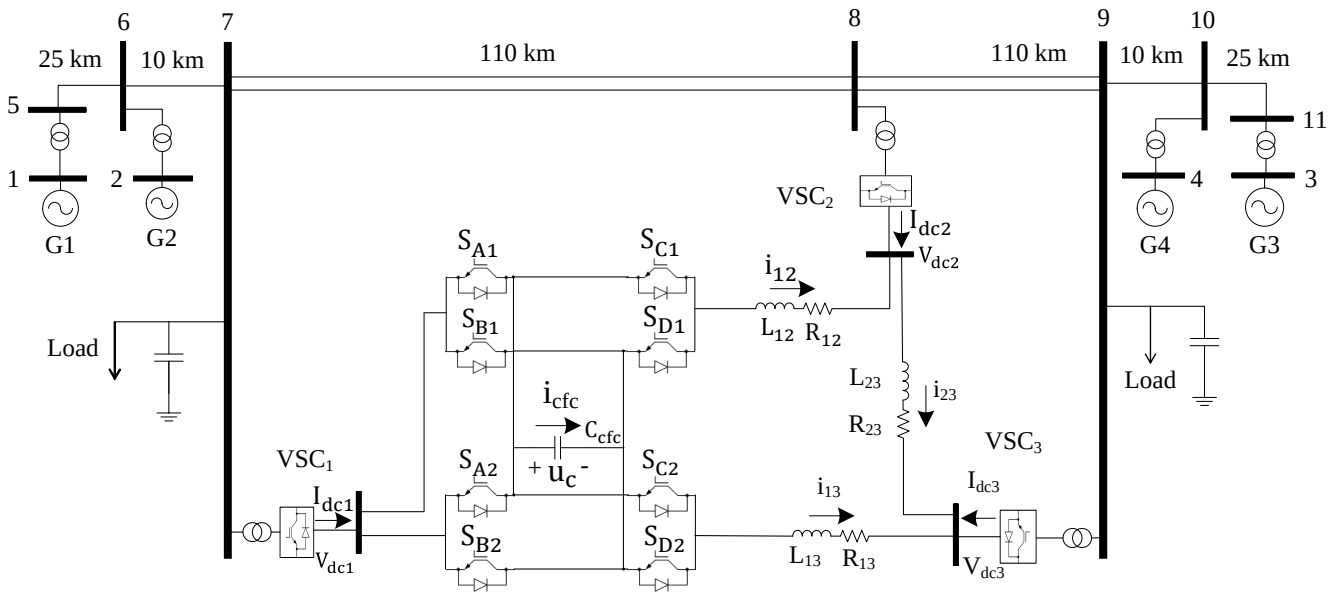


Figure 3- 4 Single-line diagram of the topology of CFC integrated AC/DC system.

3.3.2 Modal Analysis

In order to illustrate the impacts of the incorporation of CFC on small-signal stability of the integrated AC/DC system, eigenvalue analysis is implemented for the system with CFC.

The complete state-space matrix $\boldsymbol{A_{ACDCCFC}}$ has a dimension of 55×55, which consists of sub state-space matrix of two synchronous generators with excitation system ($2 \times (7 \times 7) = 2 \times (6+1) \times (6+1)$), sub state-space matrix of two synchronous generators with excitation system and PSS ($2 \times (10 \times 10) = 2 \times (6+1+3) \times (6+1+3)$), sub state-space matrix of three VSC converters ($3 \times (5 \times 5)$), sub state-space matrix of DC network (3×3)(the state variables are $\Delta i_{12}, \Delta i_{13}, \Delta i_{23}$), and sub state-space matrix of CFC (3×3)(the state variables are $\Delta u_c, \Delta y_1, \Delta y_2$). There are 52 eigenvalues for the system without CFC as presented in 2.5.2, and 55 eigenvalues of the system with CFC. The additional three states result from the CFC capacitor and 2 integral controllers of CFC ($\Delta u_c, \Delta y_1, \Delta y_2$).

By use of the approach to compute eigenvalues presented in 2.5.2, the calculated eigenvalues $\boldsymbol{\lambda_{ACDCCFC}}$ of $\boldsymbol{A_{ACDCCFC}}$ are shown in Table 3- 4. The frequency of oscillation, damping ratio and dominant state of all conjugate pairs of complex eigenvalues are also provided in Table 3- 4.

Table 3- 4 Eigenvalue results of CFC integrated AC/DC system

No.	*Eigenvalue	*Frequency	*Damping Ratio	*Dominant State
1	-989.996909	\	\	ΔE_{fd4}
2	-992.295149	\	\	ΔE_{fd1}
3	-995.595105	\	\	ΔE_{fd1}
4	-995.707401	\	\	ΔE_{fd4}
5	-29.207818 +79.733757 *j	12.690	0.344	Δi_{13}
6	-29.207818 -79.733757 *j	12.690	0.344	Δi_{13}
7	-36.172771 +74.960903 *j	11.930	0.435	Δi_{12}
8	-36.172771 -74.960903 *j	11.930	0.435	Δi_{12}
9	-50.413402	\	\	ΔV_{pss23}
10	-50.366193	\	\	ΔV_{pss21}
11	-21.427289 +15.161162 *j	2.413	0.816	$\Delta \varphi_{1d4}$
12	-21.427289 -15.161162 *j	2.413	0.816	$\Delta \varphi_{1d4}$
13	-40.284553	\	\	ΔV_{dc3}
14	-36.147588 +0.024697 *j	0.004	1.000	$\Delta \varphi_{2q4}$
15	-36.147588 -0.024697 *j	0.004	1.000	$\Delta \varphi_{2q4}$
16	-32.194893	\	\	$\Delta \varphi_{1d2}$
17	-31.405286	\	\	$\Delta \varphi_{1d4}$
18	-30.737465 +0.158230 *j	0.025	1.000	$\Delta \varphi_{2q2}$
19	-30.737465 -0.158230 *j	0.025	1.000	$\Delta \varphi_{2q2}$
20	-20.867725 +9.466367 *j	1.507	0.911	ΔE_{q1}
21	-20.867725 -9.466367 *j	1.507	0.911	ΔE_{q1}
22	-1.324673 +7.721606 *j	1.229	0.169	$\Delta \delta_2 \setminus \Delta \omega_2$
23	-1.324673 -7.721606 *j	1.229	0.169	$\Delta \delta_2 \setminus \Delta \omega_2$
24	-1.353150 +7.949151 *j	1.265	0.168	$\Delta \delta_3 \setminus \Delta \omega_3$
25	-1.353150 -7.949151 *j	1.265	0.168	$\Delta \delta_3 \setminus \Delta \omega_3$
26	-13.782411	\	\	Δi_{23}
27	-10.373649	\	\	ΔE_{q1}
28	-10.232547	\	\	ΔE_{q4}
29	-0.218588 +4.107533 *j	0.654	0.053	$\Delta \delta_1 \setminus \Delta \omega_1$
30	-0.218588 -4.107533 *j	0.654	0.053	$\Delta \delta_1 \setminus \Delta \omega_1$
31	-0.554283 +0.930014 *j	0.148	0.512	Δy_2
32	-0.554283 -0.930014 *j	0.148	0.512	Δy_2
33	-3.018345	\	\	ΔE_{d3}
34	-3.006447	\	\	ΔE_{d1}
35	-3.462913 +0.020338 *j	0.003	1.000	ΔE_{d2}
36	-3.462913 -0.020338 *j	0.003	1.000	ΔE_{d2}
37	-0.204027	\	\	ΔV_{pss31}
38	-0.180561	\	\	ΔV_{pss33}
39	-0.092289 +0.087653 *j	0.014	0.725	Δx_{32}
40	-0.092289 -0.087653 *j	0.014	0.725	Δx_{32}
41	-0.133912	\	\	Δx_{31}
42	-0.102123	\	\	ΔV_{pss13}
43	-0.051550	\	\	ΔV_{pss11}
44	-0.034554	\	\	Δx_{42}
45	-0.016087	\	\	Δx_{41}
46	-0.011626	\	\	Δx_{31}
47	-0.003970	\	\	Δx_{43}
48	0.000000 +0.000000 *j	0.000	-0.000	$\Delta \delta_4 \setminus \Delta \omega_4$
49	0.000000 -0.000000 *j	0.000	-0.000	$\Delta \delta_4 \setminus \Delta \omega_4$
50	-3.333333	\	\	Δx_{21}
51	-3.333333	\	\	Δx_{13}
52	-3.333333	\	\	Δx_{22}
53	-3.333333	\	\	Δx_{12}
54	-3.333333	\	\	Δx_{11}
55	-3.333333	\	\	Δx_{23}

CFC related

VSC related

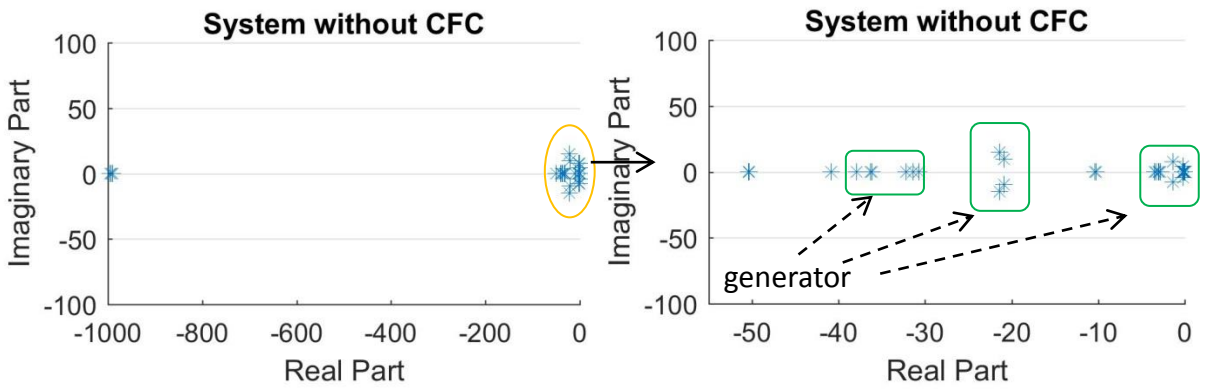
Generator related

It can be seen from Table 3- 4 that all 55 eigenvalues have non-positive real part. This indicates a stable operating condition around the equilibrium point. There are two zero eigenvalues $\lambda_{ACDC48,49}$, as there is no infinite busbar in the testing network. These two zero eigenvalues are caused by same reasons of AC/DC system without CFC presented in Chapter 2. One of the zero eigenvalues arises from a redundancy in synchronous generator angle. The second zero eigenvalue results from that the generator torque is independent of machine speed deviations, and this is because mechanical damping is neglected and governor action is not represented. This can also be proved by the fact that the dominant states of the two zero eigenvalues are rotor angle and rotor angular velocity of synchronous generator G_4. If the rotor angle and angular velocity of one synchronous generator are regarded as reference, and the governor action of mechanical damping is considered, the two zero eigenvalues will be reduced [148-149].

The conjugate pairs of complex eigenvalues $\lambda_{ACDC11,12}$, $\lambda_{ACDC14,15}$, $\lambda_{ACDC18,19}$ to $\lambda_{ACDC24,25}$, $\lambda_{ACDC29,30}$, and $\lambda_{ACDC35,36}$ are related to the dominant state variables of synchronous generators according to their participation factors. The damping of these modes is mainly affected by synchronous generator settings, associated exciter settings, and corresponding PSS parameters. The eigenvalues that significantly affects the dynamic response of the system are $\lambda_{ACDC29,30}$ (with frequency of oscillation of 0.654 Hz, and damping ratio of 0.053). According to participation matrix, the state variables of synchronous generator G_1 have a dominant effect on the conjugate pair of $\lambda_{ACDC29,30}$. In consequence, these states should be considered primarily in attempt to improve network damping characteristic. Compared to eigenvalue results of AC/DC system without CFC presented in Table 2- 1, there is no significant changes of values of these synchronous generator related conjugate pairs due to the incorporation of CFC. This presents that the corporation of CFC has no significant impacts on dynamic stability of multi synchronous generators.

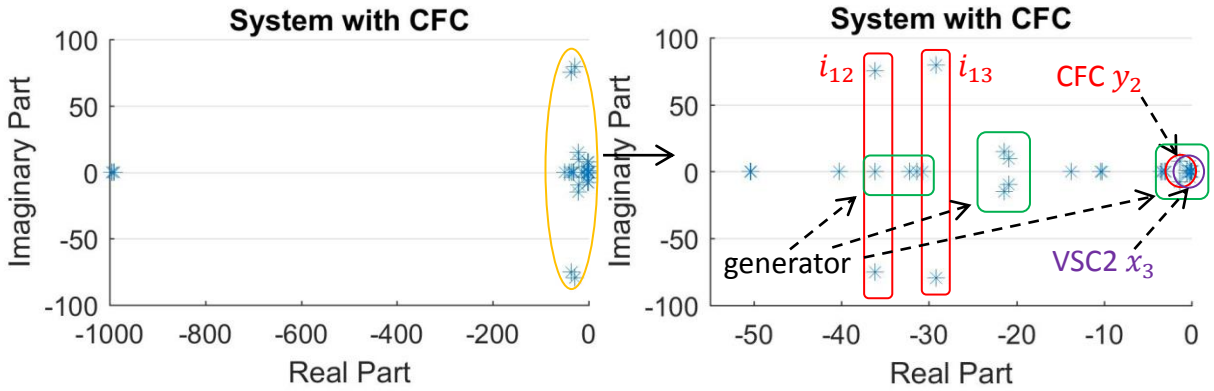
The conjugate pairs of complex eigenvalues $\lambda_{ACDC5,6}$, $\lambda_{ACDC7,8}$, and $\lambda_{ACDC31,32}$ are related to the dominant state variables of DC networks with CFC according to their participation factors. The dominant state of $\lambda_{ACDC7,8}$ is i_{12} which is controlled by CFC. The dominant state of $\lambda_{ACDC31,32}$ is CFC y_2 which represents the state variable of CFC integral controller. Based on these results, the incorporation of CFC results in the emergence of CFC related eigenvalues which means the oscillations of relevant DC network states are expected.

It should be noted that the dominant state of $\lambda_{ACDC39,40}$ is VSC_2 Δx_{32} which represents the state variable of the integral controller of VSC_2. This interesting phenomenon indicates that the incorporation of CFC can even cause the emergence of VSC related conjugate pairs. And the emergence of new oscillations of relevant VSC states is expected. The dynamic stability of VSC is affected by the integration of CFC into DC network.



(a) Clustering of eigenvalues (b) Highlighted eigenvalues

Figure 3- 5 Eigenvalues of the integrated AC/DC system without CFC.



(a) Clustering of eigenvalues (b) Highlighted eigenvalues

Figure 3- 6 Eigenvalues of the integrated AC/DC system with CFC.

Figure 3- 5 shows a plot of eigenvalues of system without CFC while Figure 3- 6 shows a plot of eigenvalues of system with CFC. The dominant states and the associated pairs of eigenvalues are highlighted in Figure 3- 5 (b) for the system without CFC and in Figure 3- 6 (b) for the system with CFC. Compared to system without CFC as shown in Figure 3- 5 (b), it can be seen that the system with CFC (as shown in Figure 3- 6 (b)) has 3 additional conjugate pairs of eigenvalues, which are dominated by state variables of DC branch currents i_{12}, i_{13}, and CFC integral controller auxiliary state y_2. Also, the integration of CFC has small impacts on the synchronous generator related eigenvalues as there are no significant changes in the placements of these eigenvalues. However, the integration of CFC leads to the

changing of VSC controller related eigenvalues from the pure negative real values to the conjugate pair of eigenvalues with negative real part, as highlighted by VSC2 x_3 in Figure 3-6 (b). This change indicates VSC controller related system oscillations for the system with CFC. The reason of this change can be the potential interactions between CFC and adjacent VSC.

From Figure 3- 6, the critical modes which have major impacts on small signal performance of the system are associated with CFC auxiliary statey_2, VSC2 auxiliary state x_3, and the angle and rotating speed of Synchronous Generator 1.

3.3.3 Impacts of Control Parameters of CFC

It has been found from modal analysis presented in 3.3.2 that the integration of CFC can affect dynamic stability of the integrated AC/DC system, especially on those VSC state variable related modes. In this section the potential effects of the control parameters of CFC (different values of the gains of CFC controller including k_{pc1}, k_{ic1}, k_{pc2}, and k_{ic2}) on small-signal stability of integrated AC/DC systems are studied.

The stable/unstable setting ranges of k_{pc1}, k_{ic1}, k_{pc2}, and k_{ic2} are obtained by procedures shown in Figure 3- 7. As shown in Table 3- 5 to Table 3- 7, the stable/unstable setting ranges of k_{ic1}, k_{pc2}, and k_{ic2} derived following these procedures are listed. For the given test system described in 3.3.1, the system is stable for $0.001 \leq k_{pc1} \leq 1000$ by use of the procedures shown in Figure 3- 7.

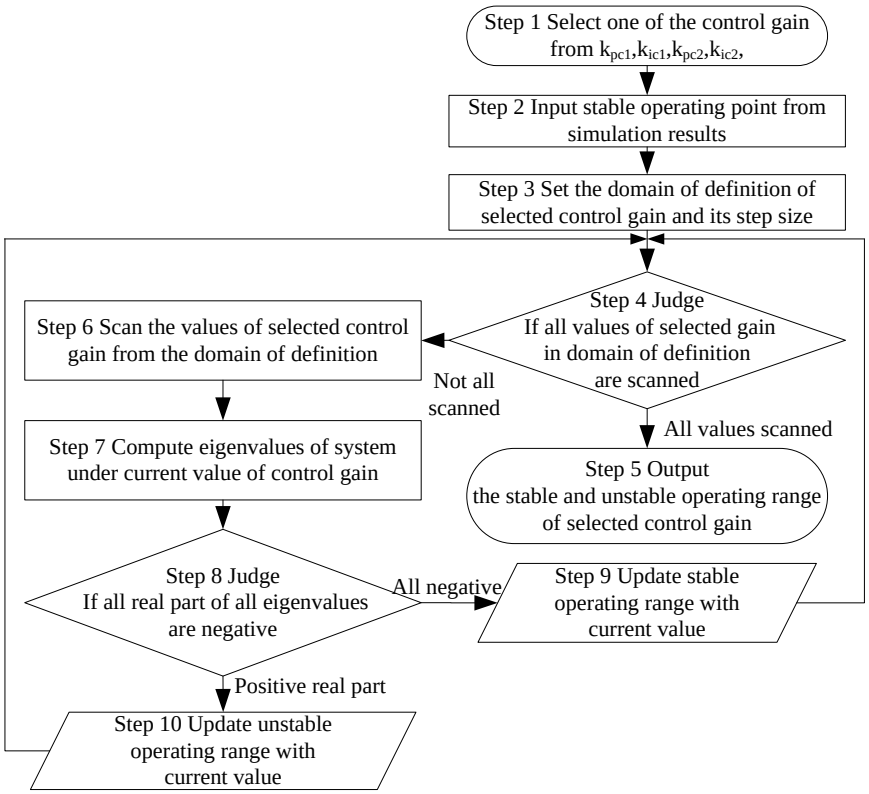


Figure 3- 7 Flowchart to obtain stable/unstable operating range of control gains.

Table 3- 5 Setting ranges of Kic1 on the integrated MTDC/AC system dynamics

SETTING RANGES OF K_{ic1} ON THE INTEGRATED MTDC/AC SYSTEM DYNAMICS

Value	Stability
$k_{ic1} \leq 2.25$	Stable
$k_{ic1} \geq 2.25$	unstable, 2 positive eigenvalues are seen

Table 3- 6 Setting ranges of Kpc2 on the integrated MTDC/AC system dynamics

SETTING RANGES OF K_{pc2} ON THE INTEGRATED MTDC/AC SYSTEM DYNAMICS

Value	Stability
$k_{pc2} \leq 0.231$	unstable, 1 positive pair of eigenvalues
$k_{pc2} \geq 0.231$	Stable

Table 3- 7 Setting ranges of Kic2 on the integrated MTDC/AC system dynamics

SETTING RANGES OF K_{ic2} ON THE INTEGRATED MTDC/AC SYSTEM DYNAMICS

Value	Stability
$k_{ic2} \leq 0.73$	unstable, 1 positive pair of eigenvalues

$k_{ic2} \geq 0.73$	stable

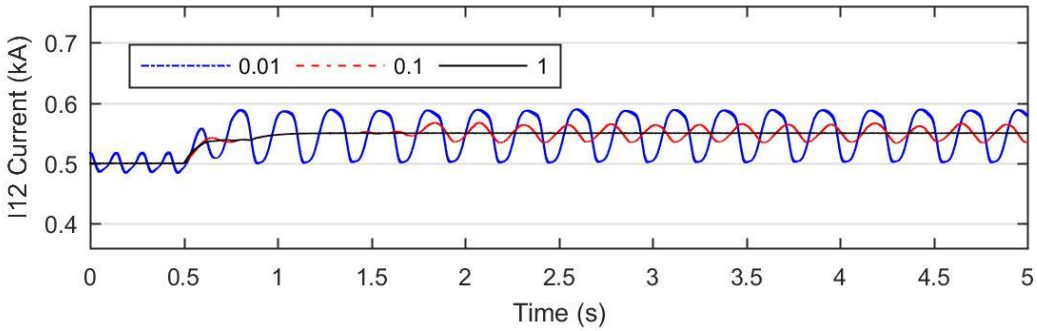
For the sake of illustration, proportional gain k_{pc2} is selected as an example to investigate system dynamic stability when CFC controller gains are changed. Table 3- 8 lists three different values of k_{pc2} ($k_{pc2} = 0.01, 0.1,$ and 1) and relevant modes. The corresponding values of $\lambda_{31,32}$ are 0.16 ± j1.07, 0.09 ± j1.08, and -0.55±j0.93. The system is stable only when $k_{pc2} \geq 1$ ($\lambda_{31,32} = -0.55 \pm j0.93$).

Table 3- 8 Impacts of Kpc2 on the integrated MTDC/AC system dynamics

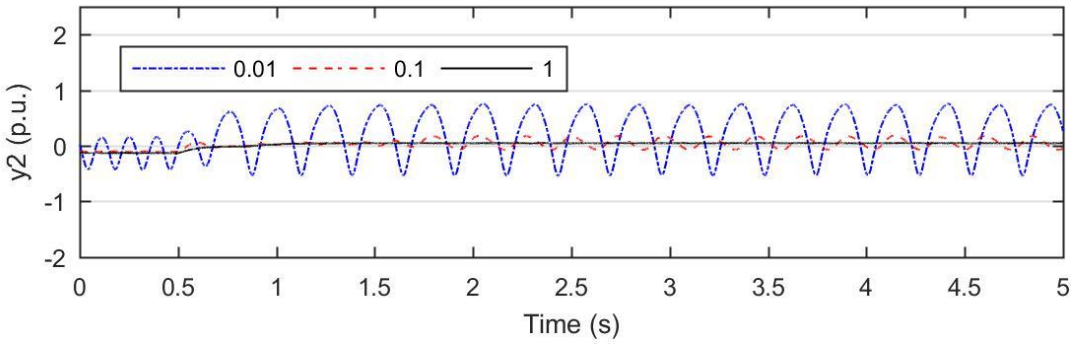
IMPACT OF K_{pc2} ON THE INTEGRATED MTDC/AC SYSTEM DYNAMICS

Value	$\lambda_{31,32}$	Stability
$k_{pc2} = 0.01$	$0.16 \pm j1.07$	unstable, 1 positive pair of eigenvalues
$k_{pc2} = 0.1$	$0.09 \pm j1.08$	unstable, 1 positive pair of eigenvalues
$k_{pc2} = 1$	$-0.55 \pm j0.93$	stable

The time-domain simulations in Figure 3- 8 are in line with the results shown in Table 3- 8 when a small change of the reference is applied (i_{12ref} changes from 0.55 kA to 0.50 kA at 0.5 s). Stable system dynamics can be achieved only when $k_{pc2} = 1$. Unstable oscillations are observed for $k_{pc2} = 0.1$ and $k_{pc2} = 0.01$. It can also be seen that large k_{pc2} decreases the oscillation frequency and the settling time. The value of k_{pc2} has significant effects on state variables i_{12}, and y_2. These results demonstrate that the control parameters of CFC may cause instability of the system if they are not carefully-tuned.



(a) Current of DC branch 12.



(b) Auxiliary variable y_2.

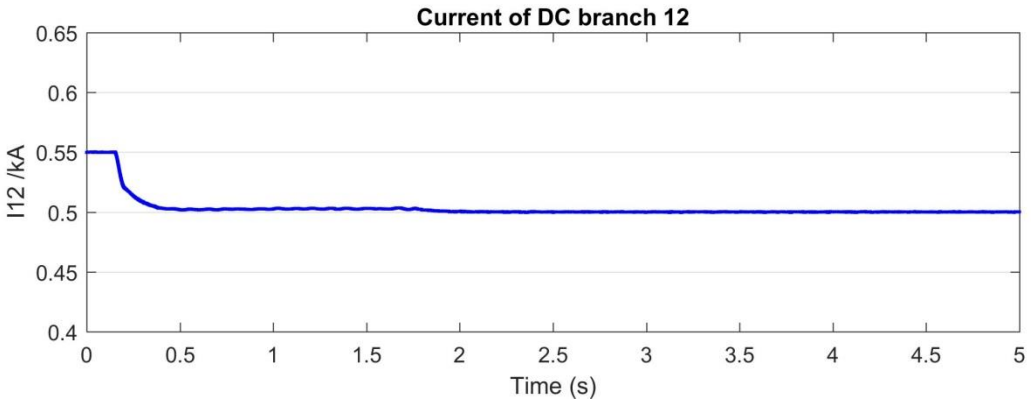
Figure 3- 8 Dynamics of DC network under different DC CFC control parameters.

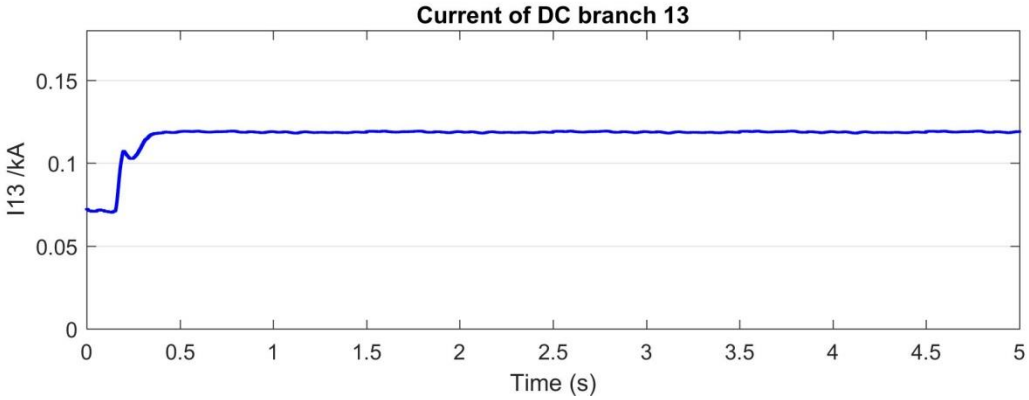
3.3.4 Dynamic Simulation Validation

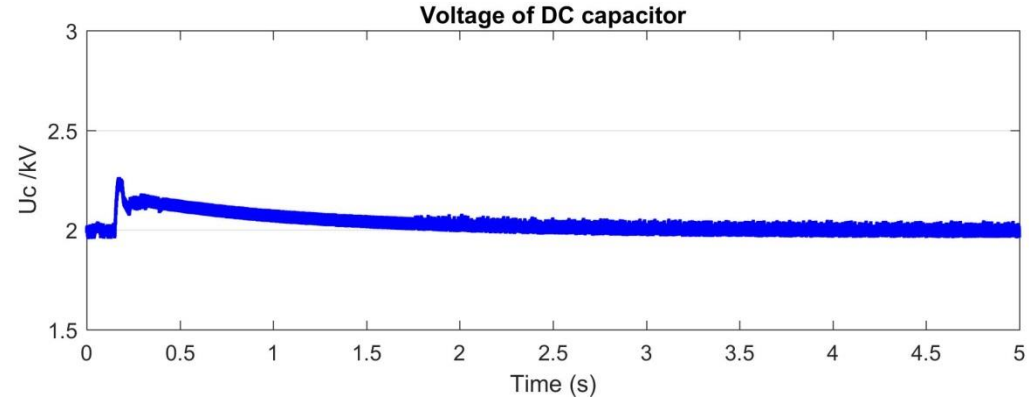
The AC/DC test system as shown in Figure 3- 4 has been established in RSCAD to validate the results of modal analysis. The power flow data, AC voltages, and impedance values are based on 4-generator 2-area benchmark system model in [6] while parameters of the DC network and CFC are shown in Appendix A.9.

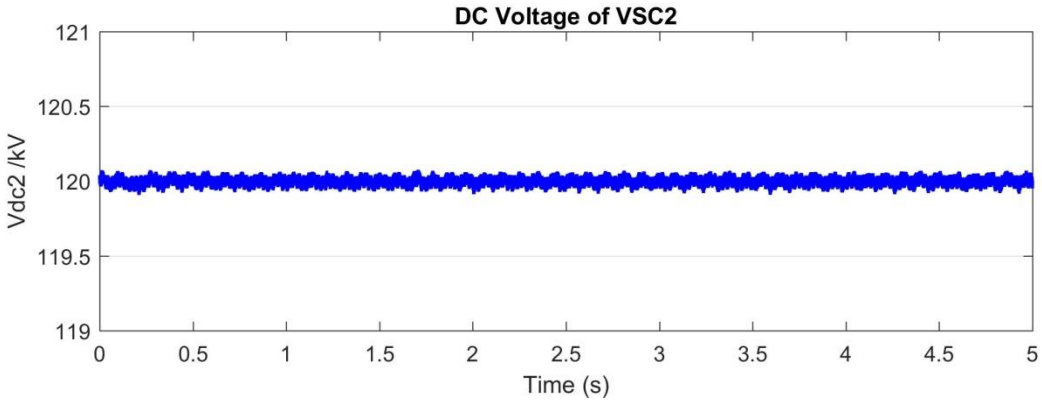
Small disturbances

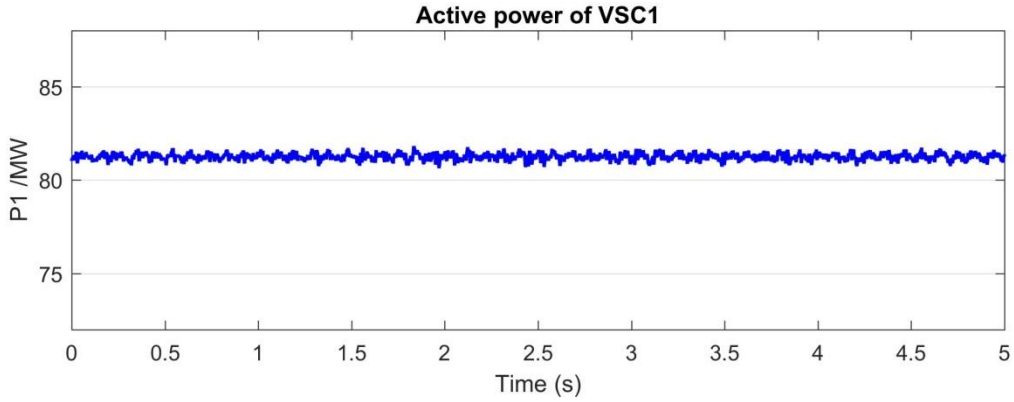
Figure 3- 9 shows the dynamic behaviour of the system in response to a step reference change applied to CFC (i_{12ref} changes from 0.55 kA to 0.50 kA at 0.15 s). It can be seen from Figure 3- 9 that the controlled current of DC branch 12 decreases by 0.05 kA and the current of DC branch 13 increases by 0.05 kA. The total DC current through VSC_1 remains unchanged. The voltage of DC capacitor returns to its reference value after the small disturbance. There are no significant changes in VSC related variables (DC voltage of VSC_2, active power of VSC_1 and VSC_3). Stable dynamic performance can be seen from the simulation results, which is in line with the modal analysis results.




Current of DC branch 13
I13 /kA
0.15
0.1
0.05
0
0 0.5 1 1.5 2 2.5 3 3.5 4 4.5 5
Time (s)


Voltage of DC capacitor
Uc /kV
3
2.5
2
1.5
0 0.5 1 1.5 2 2.5 3 3.5 4 4.5 5
Time (s)


DC Voltage of VSC2
Vdc2 /kV
121
120.5
120
119.5
119
0 0.5 1 1.5 2 2.5 3 3.5 4 4.5 5
Time (s)


Active power of VSC1
P1 /MW
85
80
75
0 0.5 1 1.5 2 2.5 3 3.5 4 4.5 5
Time (s)

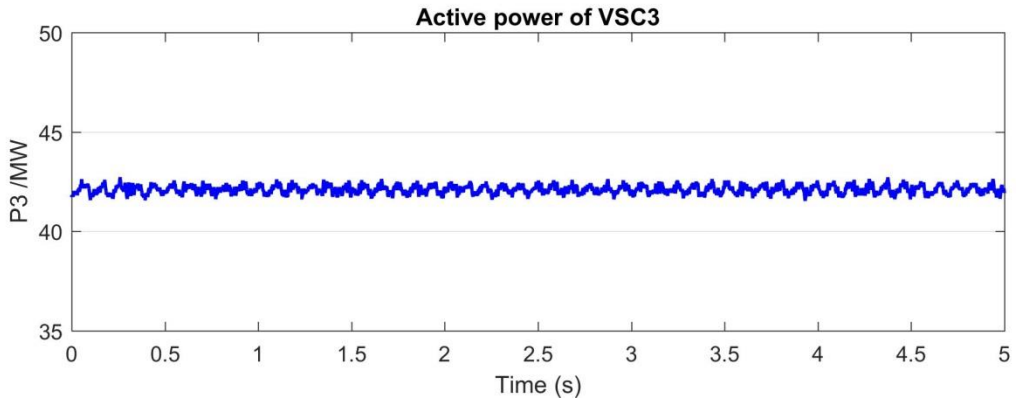
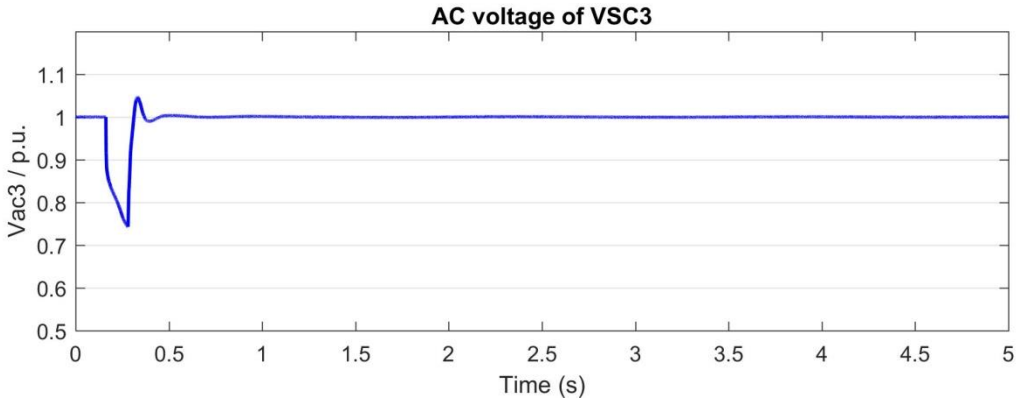


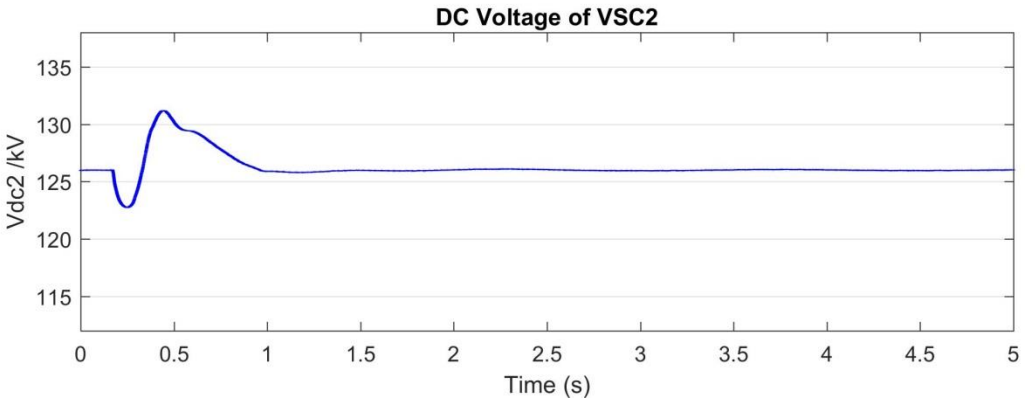
Figure 3- 9 Dynamics of DC network during small disturbance.

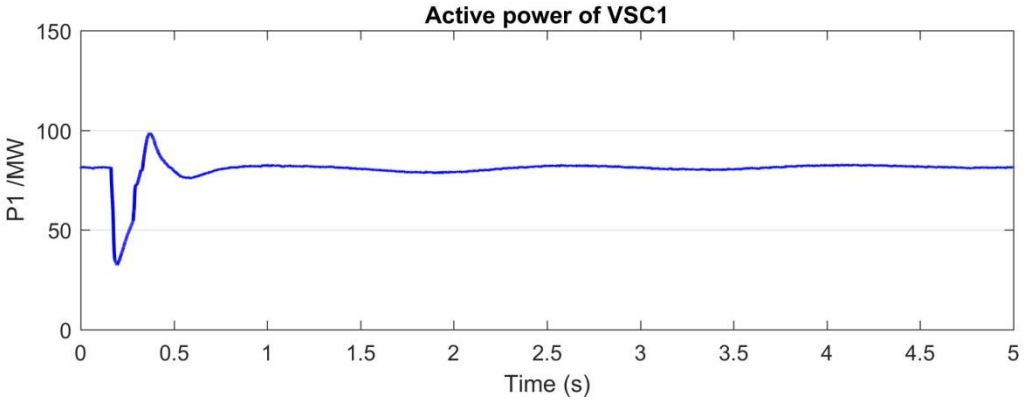
Large disturbances (AC-System Fault)

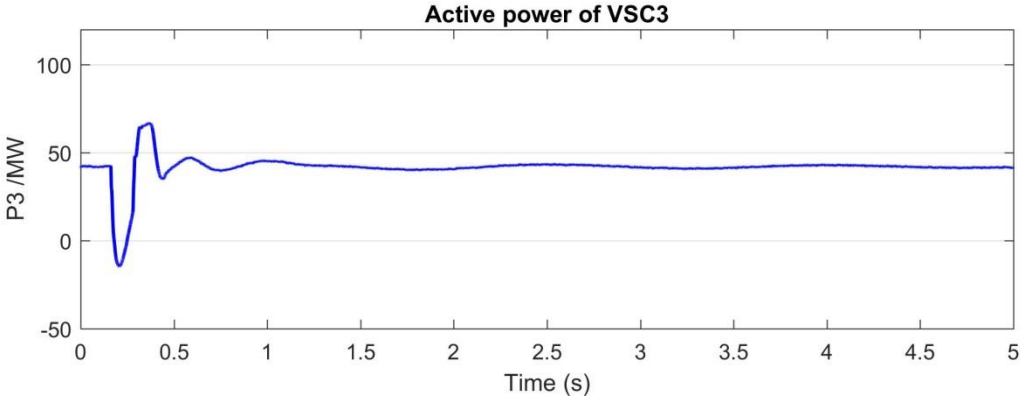
A large disturbance is applied to test the stability of the system under large disturbances. A 10 Ω single-line-to-ground fault is simulated at the PCC of VSC terminal 3 (primary side of coupling transformer) at 0.15 s lasting for 7 cycles (116 ms).

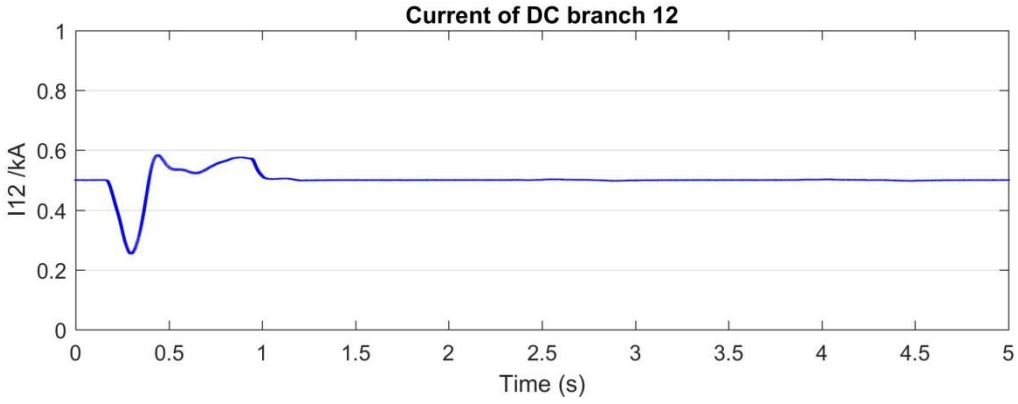
Figure 3- 10 shows system dynamics of MTDC system, including AC voltage of VSC_3, active power transfer of VSC_1 and VSC_3 (these two converters are in P-V_{ac} control), regulated DC voltage of VSC_2 (VSC_2 is in V_{dc} - V_{ac} control), currents of DC branch 12, 13 and voltage of DC capacitor. The system recovers to steady-state in a short period of time after the fault is cleared. It demonstrates that the system can endure large AC disturbance and recover quickly.




DC Voltage of VSC2
Vdc2 /kV
135
130
125
120
115
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Time (s)


Active power of VSC1
P1 /MW
150
100
50
0
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Time (s)


Active power of VSC3
P3 /MW
100
50
0
-50
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Time (s)


Current of DC branch 12
I12 /kA
1
0.8
0.6
0.4
0.2
0
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Time (s)

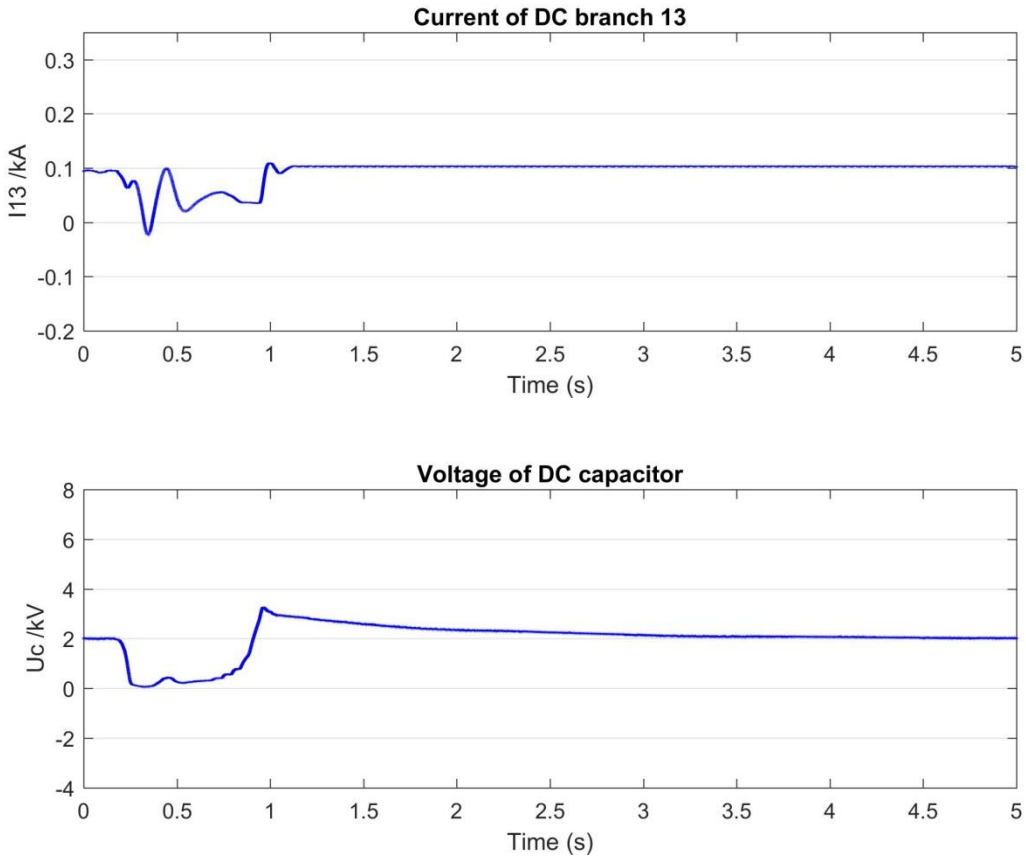
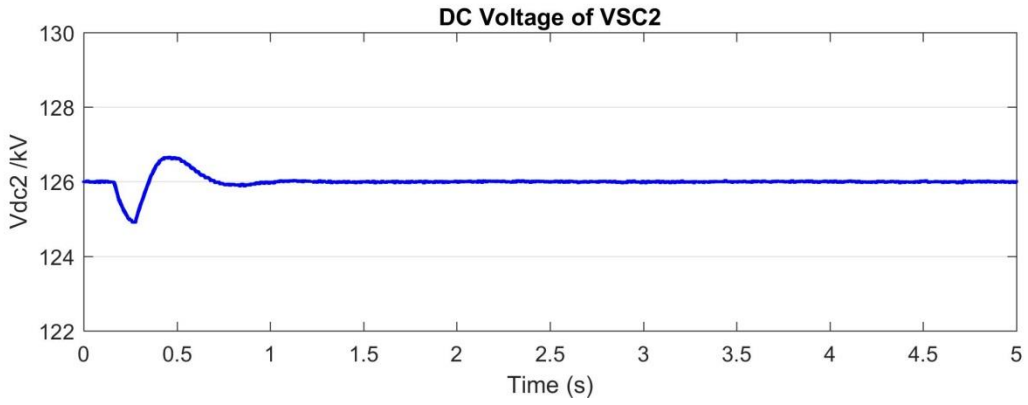


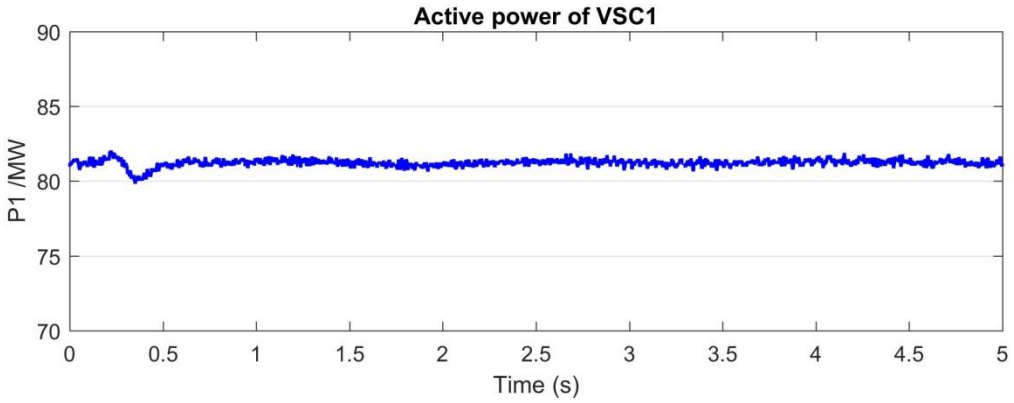
Figure 3- 10 System dynamic during AC system fault.

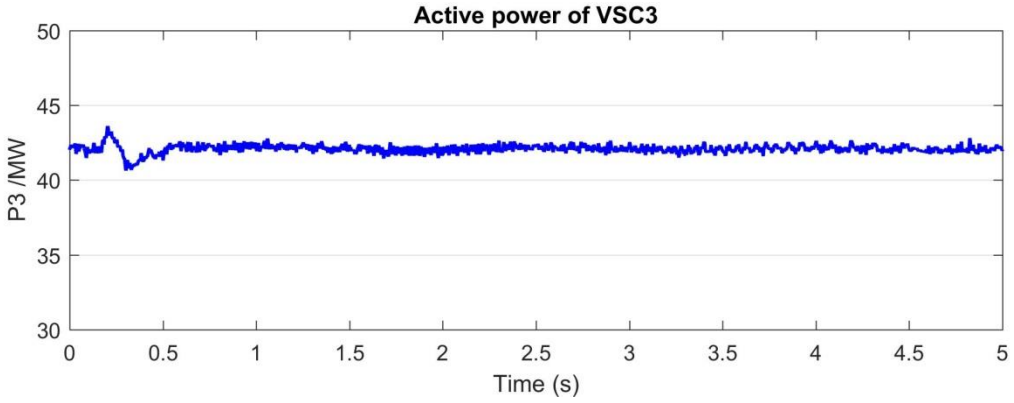
Large disturbances (DC-Cable Fault)

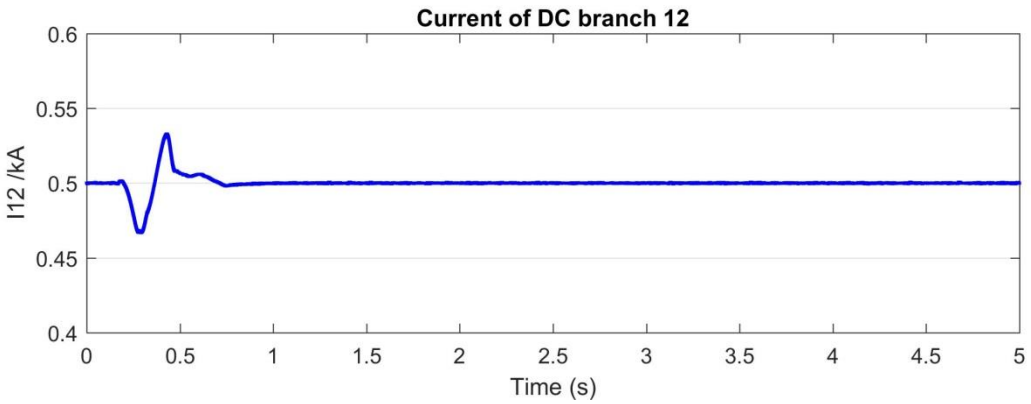
For the testing of large disturbance at DC side, a 25Ω line-to-ground DC-cable fault is simulated at the DC-side of VSC_3 at 0.15 s lasting for 7 cycles (116 ms).

Figure 3- 11 shows the system dynamic response results of DC voltage of VSC_2, active power of VSC_1 and VSC_3, controlled DC branch current i_{12}, i_{13} and voltage across CFC bridge capacitor U_{cfc}. When the fault is cleared the system recovers to its former state. The values of MTDC system related variables recover to its former level after the fault is clear. The simulation results show that the system can endure large disturbances at DC side.


DC Voltage of VSC2
Vdc2 /kV
130
128
126
124
122
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Time (s)


Active power of VSC1
P1 /MW
90
85
80
75
70
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Time (s)


Active power of VSC3
P3 /MW
50
45
40
35
30
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Time (s)


Current of DC branch 12
I12 /kA
0.6
0.55
0.5
0.45
0.4
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
Time (s)

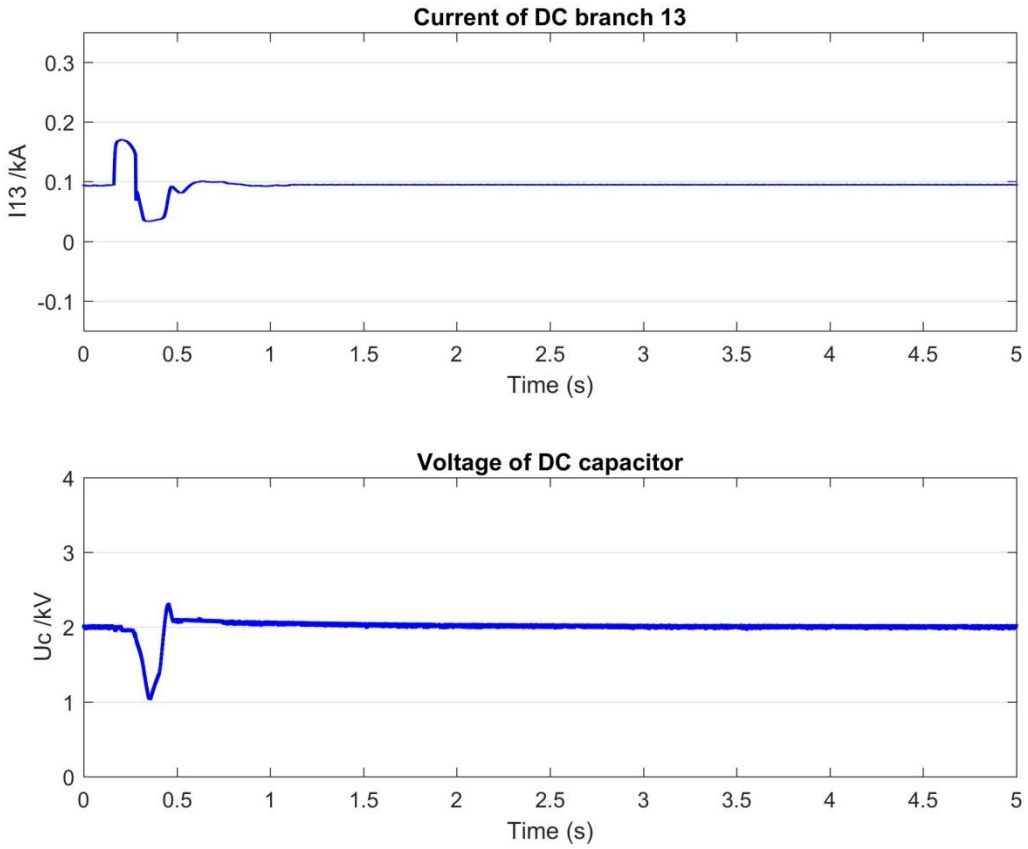


Figure 3- 11 System dynamic during DC cable fault.

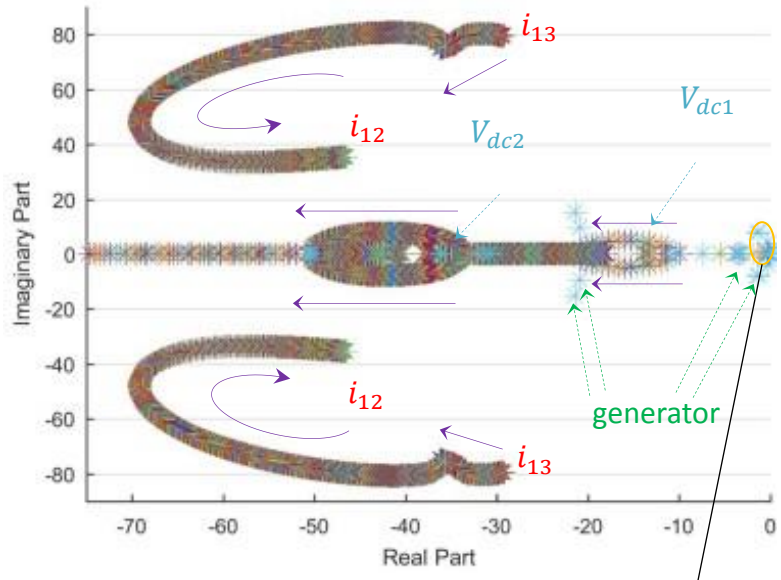
3.4 Interactions between CFC and VSC

Based on the interesting phenomenon discovered from modal analysis presented in 3.3.2, further research in potential interactions between CFC and VSC in aspects of system dynamic stability is implemented in this section. In 3.4.1, the investigation of impacts of control parameters of CFC control system on VSC is studied. In 3.4.2, the investigation of impacts of control parameters of VSC control system on CFC is studied

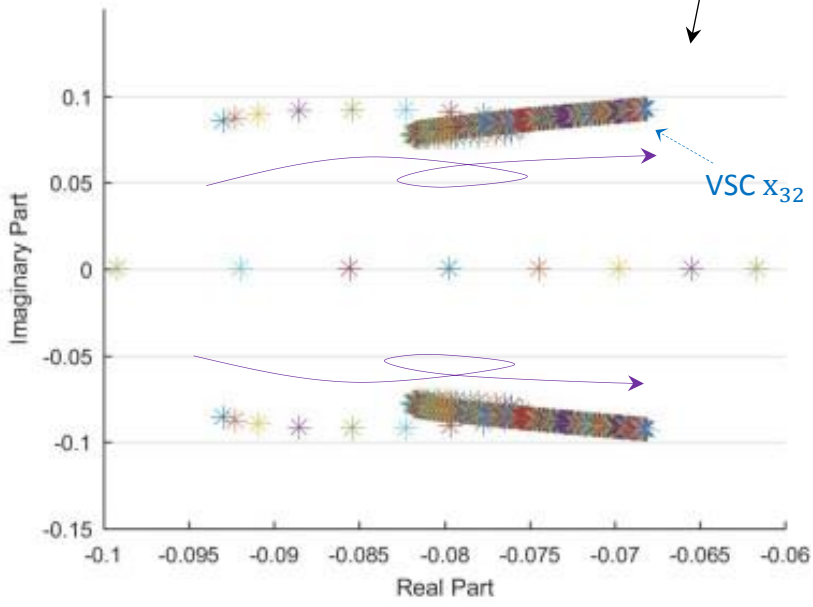
3.4.1 Impacts of Control Parameters of CFC on VSC

As shown in Figure 3- 12, eigenvalue trajectory study is used to plot the movements of critical conjugate pairs so that the impacts of changing control parameters of CFC on VSC related modes are presented. In Figure 3- 12, the control gain k_{pc2} varies from 0 (p.u.) to 1000 (p.u.) while the values of other control gains of CFC remain the same. The purple arrows indicate the movement of conjugate pairs resulting from this variation of k_{pc2}. As shown in Figure 3- 12 (a). The imaginary parts of CFC related conjugate pairs (i_{12} and i_{13}) decrease

as k_{pc2} increases, which indicate greater damping ratios of CFC related states. As shown in Figure 3- 12 (a), two new VSC related conjugate pairs $V_{dc2}$and V_{dc1} (highlighted in blue) emerge as k_{pc2} increases. The movements of VSC related pairs (V_{dc2}, V_{dc1}, and VSC x_{32}) as shown in Figure 3- 12 (a)-(b) clearly present the impacts of CFC on VSC. The two conjugate pairs of $V_{dc2}$and V_{dc1} move towards left half of s-plane which indicates greater damping ratios of VSC related states $V_{dc2}$and V_{dc1}. The conjugate pairs of VSC x_{32} move towards right hand side indicating less damping ratios of VSC x_{32}. As shown in Figure 3- 12 (a)-(b), there are no significant movements of generator related poles, which indicates CFC has no significant impacts on synchronous generator related states.



(a)



(b)

Figure 3- 12 Eigenvalue trajectories of various CFC control parameter kpc2.

Based on eigenvalue trajectory studies of CFC control gains, it can be summarised that the variation of CFC controller can affect dynamic stability of CFC and VSC related modes. These impacts of CFC on VSC can result in different damping characteristic of VSC related states, as CFC controller changes.

As listed in Table 3- 9, three cases of different CFC control parameters are designed based on eigenvalue trajectory studies of various CFC control gains, to investigate their effects on the VSC controller related modes.

Case 1: the control system of CFC is disabled as the base case to represent system without CFC control system.

Case 2: the gains of CFC control system are set the same as those in [84] ($k_{pc1} = 1, k_{ic1} = 1, k_{pc2} = 1, k_{ic2} = 1$), to represent normal settings. The oscillations of VSC2 controller related modes are seen from Table 3- 9. The AC/DC system is stable for the first two cases.

Case 3: the gains of CFC control system are changed ($k_{pc1} = 0.01, k_{ic1} = 1000, k_{pc2} = 1, k_{ic2} = 1000$), to represent extreme or possible fault condition of CFC control system. One conjugate pair of eigenvalues with positive real part is seen, which indicates small-signal instability.

Table 3- 9 Impacts of control parameters of CFC on VSC_2 related modes.

IMPACT OF CONTROL PARAMETERS OF DC CFC ON VSC2 RELATED MODES

	Related Eigenvalues	Stability
Case 1	$-0.13, -0.017(\lambda_{39,43})$	Stable
Case 2	$-0.09 \pm j0.09(\lambda_{39,40})$	Stable
Case 3	$0.02 \pm j0.10(\lambda_{38,39})$	unstable, 1 positive pair of eigenvalues

Figure 3- 13 shows time-domain simulation results for the three cases. As shown in Figure 3-13, a small perturbation (DC branch current control reference i_{12}^* changes from 0.55 kA to 0.5 kA) is applied to CFC at 0.15s. For Case 1, no significant change of VSC2 auxiliary state variable x_3 is observed because the CFC control system is disabled. For Case 2, a small increase of x_3 at 0.2s can be seen. Then the value of x_3 recovers to the pre-disturbance level after a period time of oscillations. For Case 3, large unstable oscillations are seen.

Simulation results are in line with modal analysis results in Table 3- 9, and illustrate that the CFC control system can affect dynamic performance of VSC converter controller. This effect

can be severe and cause instability to the AC/DC system, for extreme CFC operating conditions.

The possible reason of this interaction between CFC control system and VSC converter controller can be the dynamical changing of the interfacing variables that relate CFC controlled variable and adjacent VSC controlled variable. For instance, CFC controls DC branch current i_{12}, and VSC converter 2 controls DC voltage of VSC_2 V_{dc2}. And the relation between these two controlled state variables is given in (3.14).

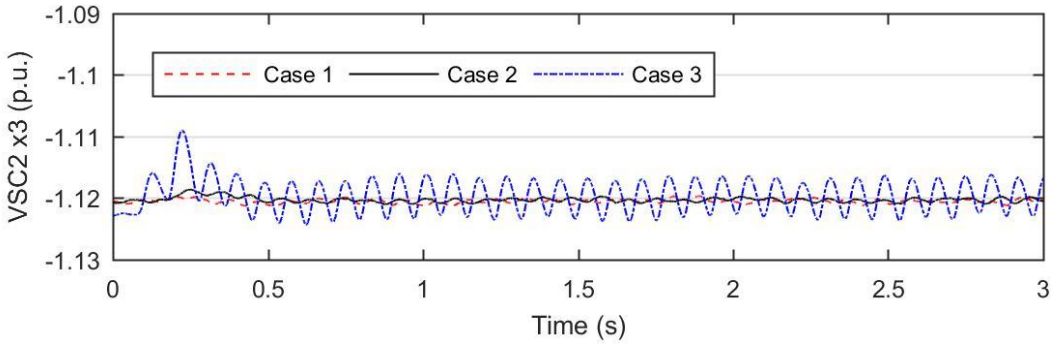


Figure 3- 13 Effects of CFC control parameters on dynamics of VSC 2.

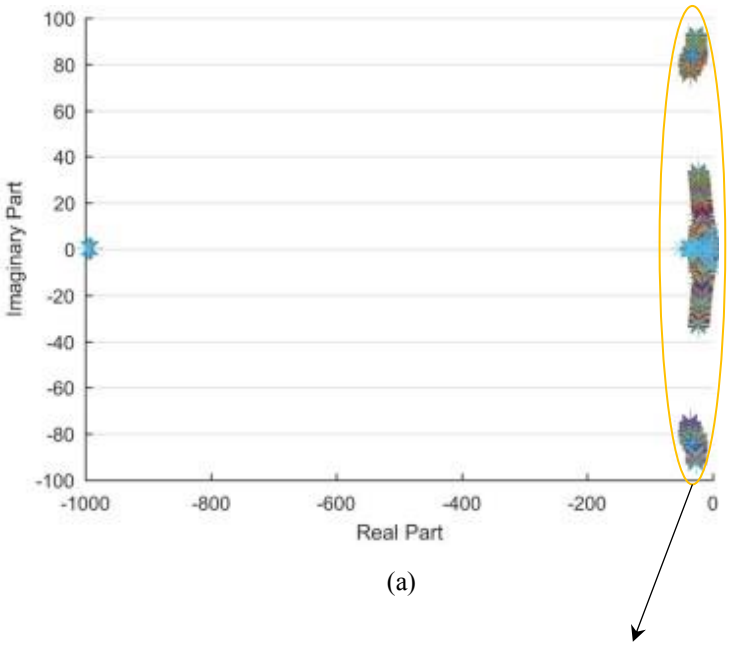
3.4.2 Impacts of Control parameters of VSC on CFC

The effects of the control parameters of VSC on CFC are studied in this section. Eigenvalue trajectory study is implemented to investigate potential impacts of different values of the control gains of VSC controller (k_{pdc}, k_{idc}, k_{pid}, k_{iid}, k_{pac}, k_{iac}, k_{piq} and k_{iiq}) on system dynamic stability of the integrated AC/DC system, especially on CFC state variable related critical modes. The stable setting ranges of the control parameters of VSC controller are based on approaches presented in [139].

As eigenvalue trajectories shown in Figure 3- 14, the movements of critical conjugate pairs presents the impacts of changing control parameters of VSC on CFC related modes. In Figure 3- 14, the control gain k_{idc} varies from 0 (p.u.) to 1000 (p.u.) while the values of other gains of VSC remain same. The purple arrows indicate the movement of conjugate pairs resulting from this variation of k_{idc}. As shown in Figure 3- 14(c), three new generator related conjugate pairs (highlighted in green arrow and purple arrow) emerge as k_{idc} increases. As shown in Figure 3- 14(b)-(d), the imaginary parts of major generator related conjugate pairs increase as k_{idc} increases. This indicates greater damping ratios of corresponding generator related states. The movements of generator related pairs are less than those of CFC related

and VSC related pairs as shown in Figure 3- 14(b) and (d). A new VSC x_{32} related conjugate pairs emerge as k_{idc} increases as shown in Figure 3- 14(d). The VSC related conjugate pairs move towards left half of s-plane as k_{idc} increases, which indicates greater damping ratios of VSC related states. It should be noted that positive eigenvalues are seen in Figure 3- 14(d). This is due to the variation range of k_{idc} covers all stable and some points of unstable operating range. As shown in Figure 3- 14(b) and (d), the movement of CFC related pairs (i_{12}, i_{13}, and CFC y_2) clearly presents the impacts of VSC on CFC. The two conjugate pairs of i_{12} and i_{13} move towards right half of s-plane which indicates reduced damping ratios of CFC related states i_{12} and i_{13}. The conjugate pairs of CFC y_2 move towards left hand side indicating increased damping ratios of CFC y_2.

Based on eigenvalue trajectory studies of VSC control gains, it can be summarised that the variation of VSC controller can affect dynamic stability of synchronous generator, VSC, and CFC related modes. These impacts of VSC on CFC can result in different damping characteristic of CFC related states, as VSC controller changes.



(a)

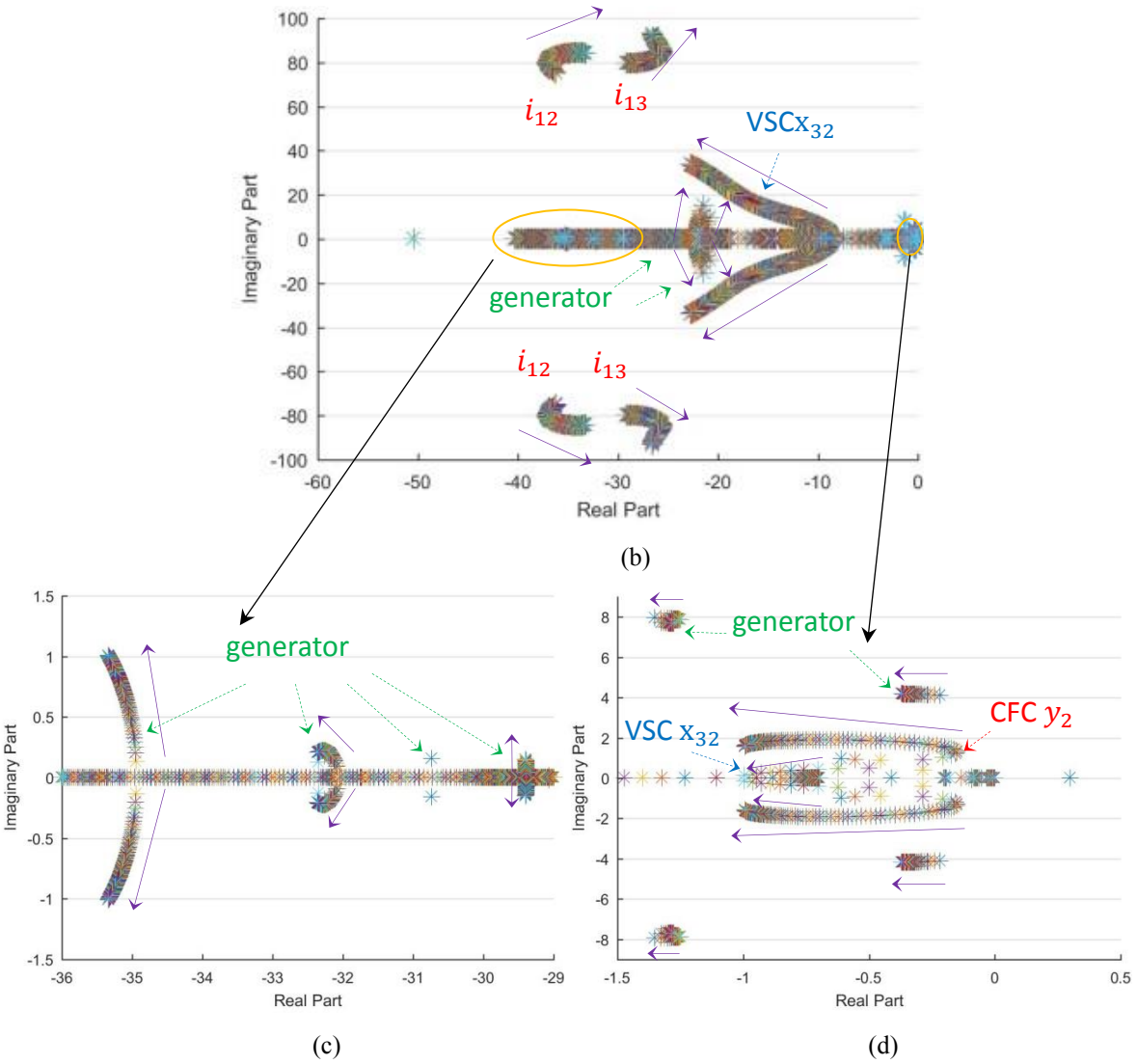


Figure 3- 14 Eigenvalue trajectories of various VSC control parameter kidc.

As listed in Table 3- 10, two cases of different control parameters of VSC converter are designed based on eigenvalue trajectories of various VSC control gains, to investigate their effect on the CFC related system stability modes.

Case 4: control parameters (value of the gains of proportional and integral controllers) of VSC_2 are set to normal operating values ($k_{pdc} = 7.52, k_{pac} = -10, k_{pid} = 0.3, k_{piq} = 0.3,\ k_{idc} = 1,\ k_{iac} = -1,\ k_{iid} = 1,$ and $k_{iiq} = 1$) [139]. The system is stable.

Case 5: controller of VSC 2 is set to abnormal operating values ($k_{pdc} = 7.52, k_{pac} = -10, k_{pid} = 0.3, k_{piq} = 0.3,\ k_{idc} = 10, k_{iac} = -1000\ k_{iid} = 1, and\ k_{iiq} = 1$) which represents extreme or possible fault VSC operating condition. One conjugate pair of eigenvalues with positive real part can be seen which indicates small signal instability.

Table 3- 10 Impacts of control parameters of VSC_2 on CFC related modes

IMPACT OF CONTROL PARAMETERS OF VSC 2 ON DC CFC RELATED MODES

	Related Eigenvalues	Stability
Case 4	$-0.09 \pm j0.09(\lambda_{39,40})$	stable
Case 5	$0.52 \pm j1.65(\lambda_{33,34})$	unstable, 1 positive pair of eigenvalues

Figure 3- 15 shows time-domain simulation results for the effects of control parameters of VSC_2 on dynamic performance of CFC. As shown in Figure 3- 15, a small perturbation (DC branch current control reference i_{12} changes from 0.5 kA to 0.55 kA) is applied to CFC at 0.3s. For Case 4, i_{12} quickly increases to 0.55 kA in response to the change of reference. For Case 5, large oscillations can be observed which indicates instability of CFC integrated DC network.

Simulation results demonstrate that the VSC controller can affect the dynamic performance of CFC. And this effect can be severe and cause instability of the CFC integrated DC network, for extreme VSC operating conditions.

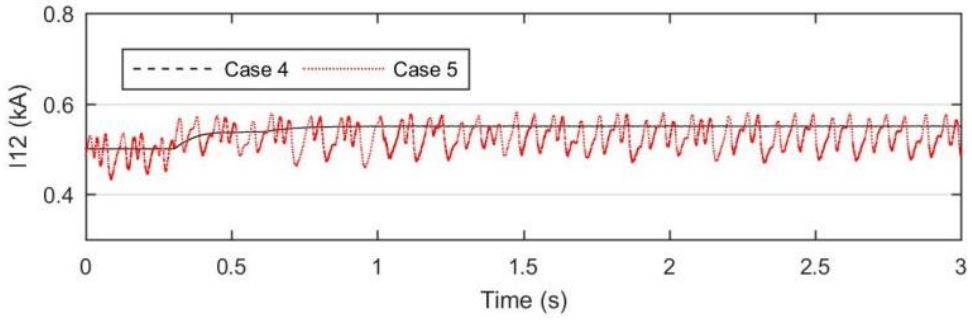


Figure 3- 15 Effect of control parameters of VSC converter 2 on DC CFC.

It should be pointed out here that the coordinated design of CFC control system and control system of VSC can be carried out as future work in order to avoid possible negative interactions between them.

3.5 Summary

In this chapter, DC network with CFC, including CFC and its control system has been modelled in dynamic equations. The dynamic model of DC network with CFC has been linearized and merged into VSC-based MTDC system without CFC presented in Chapter 2 to formulate the state-space representation of multi-model system with CFC for small-signal stability analysis. An integrated AC/DC system that consists of multiple synchronous

generators with excitation system and PSS, multiple VSC converters, and DC network with CFC, has been established. Small-signal model of the test system has been derived based on approaches presented in Chapter 2 and the eigenvalues of state-space representation of the test system have been calculated. Modal analysis of calculated eigenvalues in comparison between the integrated AC/DC system without/with CFC has been implemented to study the impacts of incorporation of CFC, and its control parameters on small-signal stability of the integrated AC/DC system.

It can be found from eigenvalue results that all 55 eigenvalues have non-positive real part. This indicates a stable operating condition at the considered operating point. There are two zero eigenvalues, as there is no infinite busbar in the testing network. One of the eigenvalue arises from a redundancy in synchronous generator angle. The second zero eigenvalue results from that the generator torque is independent of machine speed deviations, and this is because mechanical damping is neglected and governor action is not represented. If the rotor angle and angular velocity of one synchronous machine are regarded as references, and the governor action of mechanical damping is considered, the two zero eigenvalues will be reduced. Compared to eigenvalue results of AC/DC system without CFC, there is no significant changes of values of synchronous generator related conjugate pairs caused by the incorporation of CFC. This indicates that the corporation of CFC has no significant impacts on dynamic stability of multi synchronous generators.

The conjugate pairs which are related to the dominant state variables of DC networks with CFC are seen, according to their participation factors. The dominant states of these conjugate pairs are CFC controlled state variables. These results indicate that the incorporation of CFC causes the emergence of CFC related eigenvalues, hence the oscillations of relevant DC network states are expected. It should be noted that the VSC related conjugate pairs is seen, which indicates that the incorporation of CFC can even results in the emergence of VSC related eigenvalues. The dynamic stability of VSC is affected by the integration of CFC. An approach of determining stable/unstable setting ranges of control parameters of CFC is presented and validated by simulation results in RTDS/RSCAD. The simulation results demonstrate that the control parameters of CFC may cause instability of the system if they are not carefully-tuned.

Simulations results of established AC/DC system against disturbances are in line with the modal analysis results, since stable operating condition around operating point is seen from

simulation results in RTDS/RSCAD against both small disturbance of change of reference and large disturbances (including AC system faults, and DC cable faults).

Based on eigenvalue trajectory studies of CFC control gains, it can be summarised that the variation of CFC controller can affect dynamic stability of CFC and VSC related modes. These impacts of CFC on VSC can result in different damping characteristics of VSC related states, as CFC controller changes. This effect can be severe and cause instability to the AC/DC system, for extreme CFC operating conditions. And it can also be found that the variation of VSC controller can affect dynamic stability of synchronous generators, VSC, and CFC related modes, based on eigenvalue trajectory studies of VSC control gains. These impacts can result in different damping characteristics of CFC related states, as VSC controller changes. And this effect can be negative and cause instability of the CFC integrated DC network, for extreme VSC operating conditions. It should be pointed out here that the coordinated design of CFC control system and control system of VSCs can be carried out as future work in order to avoid possible negative interactions between them.

CHAPTER 4 IMPACTS OF VSC HVDC SYSTEM ON DISTANCE PROTECTION

4.1 Introduction

This chapter investigates the impacts of the integration of VSC HVDC system on HV feeder distance protection. The mathematical representation of the apparent impedance measurements of distance relays is presented considering the infeed current from VSC HVDC system connected busbar. Relevant analysis of the apparent impedance measurement representation and dynamic simulation study is conducted to investigate the impacts of VSC HVDC system on distance protection. In 4.2, a typical feeder distance protection of two-ended overhead transmission lines is reviewed, including basic principles of distance protection, zones of protection, distance relay characteristics, and under-reach and overreach effect of distance relay application. In 4.3, mathematical representation of the apparent impedance measurement of distance relay for zone 2 protection is derived considering infeed current from VSC HVDC connected busbar. A RTDS-based hardware in the loop (HIL) testing platform is established to perform dynamic simulation studies of test system with VSC HVDC. The dynamic simulation results are analysed in comparison between the test system without/with VSC HVDC.

4.2 Distance Protection of Two-Ended Overhead Transmission Lines

Normal application of distance protection of two-ended overhead transmission lines is presented in this section, including basic principles, zones of protection, residual compensation, and under-reach and overreach effect.

4.2.1 Basic Principles of Distance Protection

Distance protection is a kind of economic and fast-reacted non-unit system of protection. Distance relays use measurements of line voltages and line currents from protected area to calculate apparent impedance. The impedance of HV and extra high voltage (EHV) transmission lines is usually proportional to the line length. In consequence, it is possible to

determine if a fault occurs in the protection zone or out of protection zone by comparing the calculated impedance to the protected line impedance [93].

Distance protection is considered to be simple to apply and fast in operation for faults located along most of a protected circuit. It is suitable for application with high-speed auto-reclosing. As single-line diagram of distance protection shown in Figure 4- 1, the measured apparent impedance by distance relay is independent of the source impedance which can be derived as follows:

$$I_{fault} = \frac{V_{source}}{Z_{source}+Z_{linea}} \quad (4.\ 1)$$

$$I_{relay} = I_{fault} \quad (4.\ 2)$$

$$V_{relay} = I_{fault} \times Z_{linea} \quad (4.\ 3)$$

$$Z_{relay} = \frac{V_{relay}}{I_{relay}} = Z_{linea} \quad (4.\ 4)$$

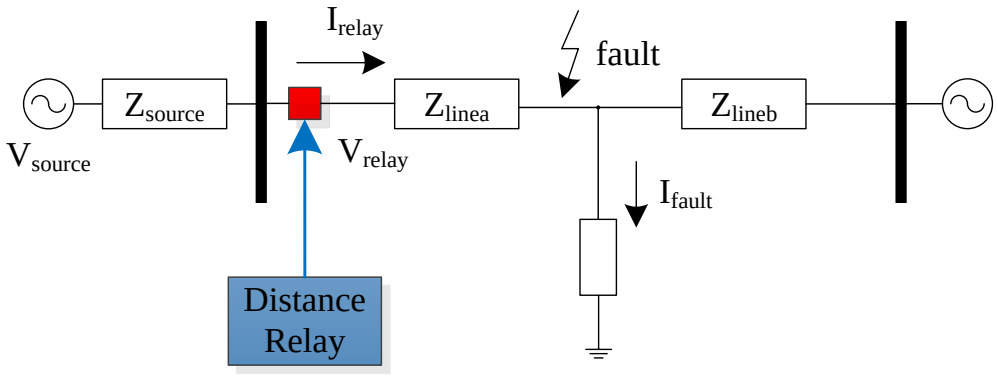


Figure 4- 1 Single-line diagram of distance protection.

Distance relays are designed to operate only when faults occurred are within the protection zone, which is the protection range between the relay location and the selected reach point. The calculated apparent impedance is compared with the reach point impedance. If the calculated apparent impedance is less than the reach point impedance, it is assumed that a fault occurs on the line between the relay and the reach point. The distance relay operates and sends signals to related circuit breakers and circuit breakers trip. If the calculated apparent impedance is greater than the reach point impedance, it is assumed that no fault occurs on the line between the relay and the reach point. Once the settings of distance relay are determined the protection is relatively unaffected by changes in the power system.

The reach point of a distance relay is a certain point along the line impedance locus which indicates the boundary of protection. The reach point can be plotted on an R/X diagram since it is dependent on the ratio of voltage and current and phase angle between them.

The major advantages of distance protection are as follows [93]:

1. High-speed of operation.
2. Ability to protect independent of communication services.

And the major disadvantages of distance protection are considered to be as follows [93]:

1. Need of both CTs and VTs.
2. Limited resistive fault coverage.

4.2.2 Zones of Protection

The reach settings and tripping times for various zones of protection should be carefully selected so that correct coordination between multiple distances relays on power system are achieved. Basic distance protection consists of instantaneous Zone 1 protection and one or more time-delayed zones. The protection zones studied in this thesis are Zone 1 protection and Zone 2 protection.

Conventional electromechanical/ static relays usually use a reach setting of up to 80% of the protected line impedance for instantaneous Zone 1 protection. Digital/numerical distance relays may use settings of up to 85% to be safe. The 15%-20% safety margin ensures no risk of over-reaching effect in Zone 1 protection, due to errors in the current and voltage measurement of coupling transformers, inaccuracies in line impedance data and errors of relay settings. The relay setting for Zone 1 protection in this study is 75% of the line impedance, which is in line with the Grid Code of UK.

The reach settings of the Zone 2 protection is usually at least 120% of the protected line impedance to ensure that full length of line is covered with allowance for the sources of error as listed for Zone 1 protection. The relay settings for Zone 2 protection in this study is 150% of the line impedance, which is in line with the Grid Code of UK so that the full protection range of Zone 1 and Zone 2 protection of a distance relay overlaps the protection range of Zone 1 protection of the remote end distance relay located at adjacent transmission line.

The tripping of Zone 2 protection should be time-delayed so that the Zone 1 protection of remote relay can operates first. Thus complete length of a transmission line is covered with fast clearance of faults in the first 80-85% of the line and slower clearance of faults in the remaining section of the line. Other protection zones for additional protection proposes are not considered in this study.

4.2.3 Distance Relay Characteristics

Plain impedance characteristic of distance relay which takes no account of the phase angle between the current and voltage applied to it is considered in this study. The calculated impedance is a circle with its centre at the origin of the coordinates and radius equal to its setting in ohms when plotted on an R/X diagram. The distance relay operates if the calculated impedance is less than setting value, that is, for all points within in the circle in R/X diagram. This relay characteristic is non-directional.

As for distance relay located near bus *A* (the distance between distance relay and bus *A* can be neglected) protecting line *AB* shown in Figure 4- 2, the plain impedance relay characteristic is shown is Figure 4- 3. The segment *AB* in R/X diagram represents the complete line impedance of transmission line *AB*. The parameters of transmission line *AC* and *AB* can be considered same as an example. Hence, the segment *AC* represents the complete line impedance of transmission line *AC*. The green circle in R/X diagram represents the impedance locus of fault occurred in protection Zone 1, which is 75% of the complete length of line *AB*. The radius of circle Zone 1 is 75% of segment *AB*. Similarly, the blue circle in R/X diagram represents the impedance locus of fault occurred in protection Zone 2, which is 150% of the complete length of line *AB*. The radius of circle Zone 2 is 150% of segment *AB*. For any fault with impedance locus within the circle of Zone 1 and Zone 2, the distance relay operates and sends trip signals to related circuit breakers. For any fault with impedance locus without the circle Zone 2, the distance relay restraints. This protection range covers the whole length of line *AB* and even adjacent transmission lines (for example *AC* in this case).

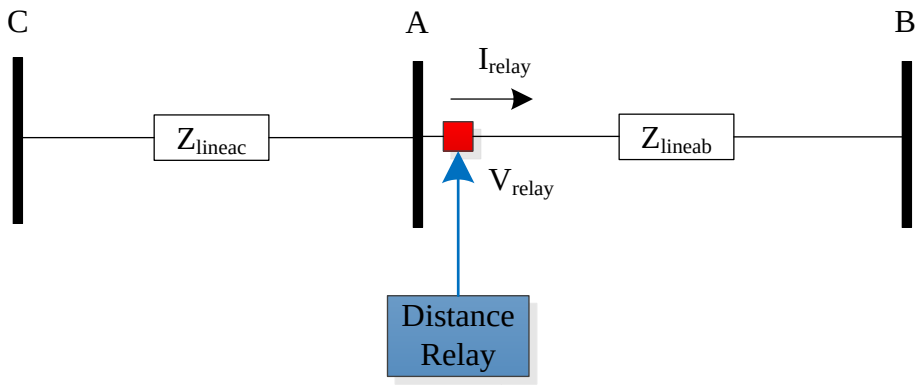


Figure 4- 2 Single-line diagram of distance protection located at two adjacent lines.

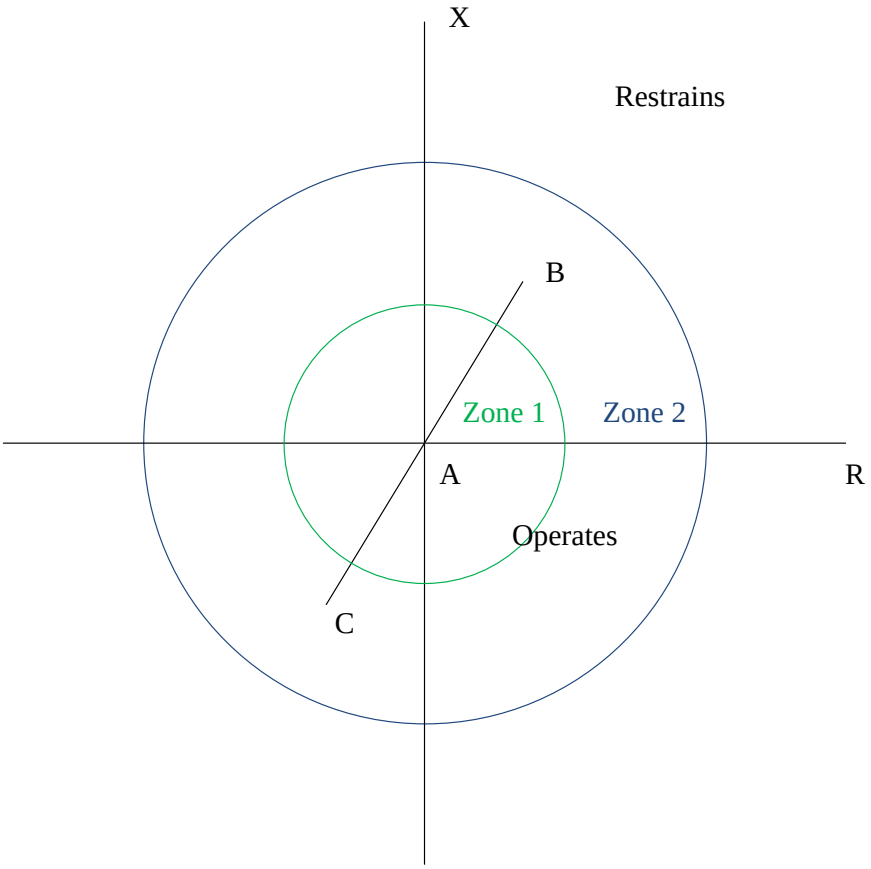


Figure 4- 3 Plain impedance relay characteristic.

It should also be noted that the plain impedance relay characteristic has disadvantages. It is non-directional which means it reacts to faults both in front of and behind the relaying point.

For unbalanced and line to ground faults, the voltage and current measurements of a particular phase should be compensated to ensure correct measured quantities are used. Distance relays compare positive sequence apparent impedance from measurements to those from line data. But for unbalanced and earth faults, the measurements of line voltage and

current are not in positive sequence and should be compensated with residual compensation factor. Considering phase A to ground fault as an example to study, the voltage drop to the fault and current in the fault loop can be expressed as follows:

$$V_a = I_1 Z_{L1} + I_2 Z_{L2} + I_0 Z_{L0} \quad (4.5)$$

$$I_a = I_1 + I_2 + I_0 \quad (4.6)$$

where

V_a and I_a : voltage and current of phase *a* measured by distance relay

I_1, I_2, and I_0 : positive, negative and zero sequence current through transmission line

Z_{L1}, Z_{L2}, and Z_{L0}: positive, negative and zero sequence impedance from fault point

The line positive and negative sequence impedances are assumed equal (Z_{L1}=Z_{L2}). And the zero sequence current can be expressed as follows:

$$I_a + I_b + I_c = 3I_0 \quad (4.7)$$

where

I_b and I_c : phase current of phase *b* and *c* at relaying point

(4.5) can be simplified by substituting (4.6) and (4.7) as follows:

$$V_a = Z_{L1}(I_a + I_0 \frac{Z_{L0} - Z_{L1}}{Z_{L1}}) \quad (4.8)$$

The residual compensation factor K_{Z0} is defined as follows:

$$K_{Z0} = \frac{Z_{L0} - Z_{L1}}{3Z_{L1}} \quad (4.9)$$

(4.8) can be simplified as follows by substituting (4.9):

$$V_a = Z_{L1}(I_a + 3I_0 K_{Z0}) \quad (4.10)$$

$$Z_{L1} = \frac{V_a}{I_a + 3I_0 K_{Z0}} \quad (4.11)$$

In this case, the relationship between I_a and I_0 can be expressed as follows:

$$I_a = 3I_0 \quad (4.12)$$

(4.11) can be simplified as follows by substituting (4.12):

$$Z_{L1} = \frac{V_a}{I_a(1+K_{Z0})} \quad (4.\ 13)$$

In this way, the correct positive sequence apparent impedance from fault location can be calculated by use of phase voltage and current measurement compensated with residual compensated factor.

4.2.4 Under-reach and Over-reach Effect of Distance Relay Application

A number of various problems might be encountered in application of distance relays. The major problems that are likely to happen are under-reach and over-reach effect. These unwanted effects of distance relays should be made aware of to avoid consequent mal-operations.

The under-reach is defined as that the measured apparent impedance by distance relay is greater than the real impedance to the fault [93]. And the percentage under-reach is defined as follows:

$$\frac{Z_R - Z_M}{Z_R} \times 100\% \quad (4.\ 14)$$

where

Z_R : intended relay reach (relay reach setting)

Z_M : measured reach

The main cause of under-reach is the fault current infeed at remote busbars which is shown in Figure 4- 4. For fault occurred at point *C*, the measured apparent impedance is not $Z_a + Z_c$ due to the infeed current I_b. The measured apparent impedance is calculated by distance relay as follows:

$$Z_M = Z_a + Z_c \frac{I_a + I_b}{I_a} \quad (4.\ 15)$$

where

Z_a and Z_c : line impedance of line *AB* and line *BC*

I_a and I_b : line current of line *AB* and line *BD*

The percentage under-reach is:

$$\frac{Z_R - Z_M}{Z_R} \times 100\%$$

$$= -\frac{Z_c}{Z_a+Z_c}\frac{I_b}{I_a} \times 100\% \quad (4.16)$$

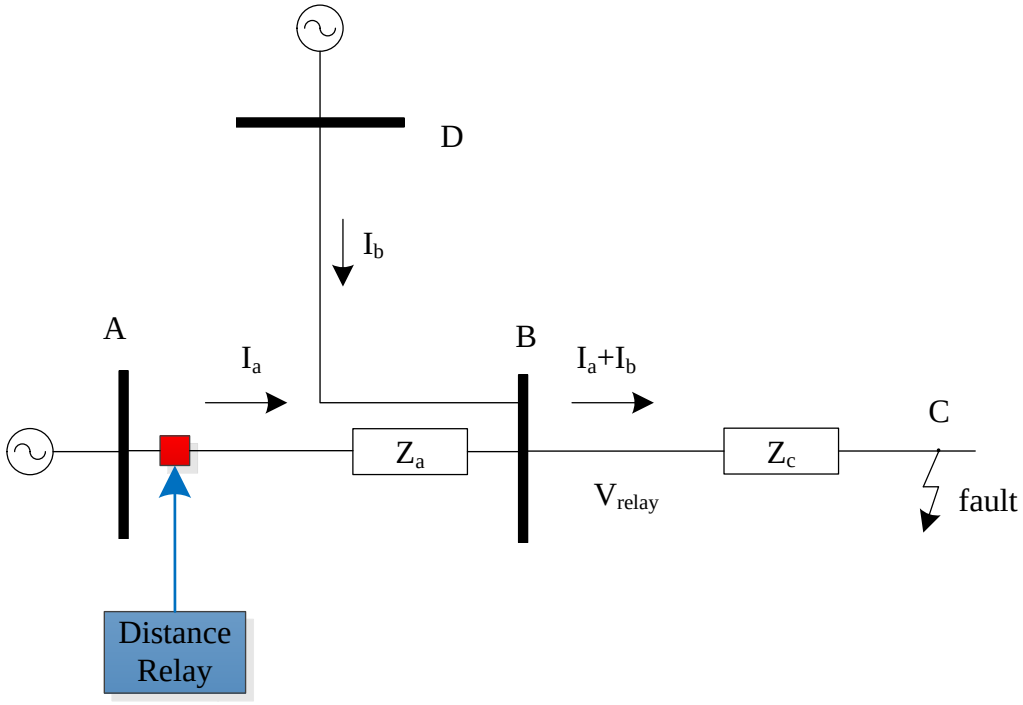


Figure 4- 4 Under-reach due to fault current infeed at remote busbars.

Another problem that is likely to happen is over-reach effect. The over-reach is defined as that the measured apparent impedance by distance relay is less than the real impedance to the fault. And the percentage over-reach is defined as follows:

$$\frac{Z_M - Z_R}{Z_R} \times 100\% \quad (4.17)$$

4.3 Impacts of VSC HVDC System on Distance Protection

The mathematical analysis of the impacts of VSC HVDC system on the apparent impedances measured by feeder distance protection relays is presented in this section.

Figure 4- 5 shows the simplified single line diagram of a faulted network for the analysis of impacts of VSC HVDC system. Two AC systems (represented by ideal voltage source with internal impedance) are connected via double-circuit transmission lines TL1 and TL2. The line parameters for the double circuits of same transmission line are same. A VSC converter is connected near *B2* (the distance between VSC converter and *B2* can be neglected) to provide voltage support and active power transmission. Two distance relays (Distance relay 1 and Distance relay 2) are located at the both ends of one single-circuit of TL1. These distance relays collect voltage and current measurements from voltage transformer (VT) and current transformer (CT) and send trip signals to circuit breakers (CB1 and CB2). An external single-phase-to-ground (SLG) fault or three-phase fault on TL2 occurs at *p*% of the full length of TL2 from *B2*.

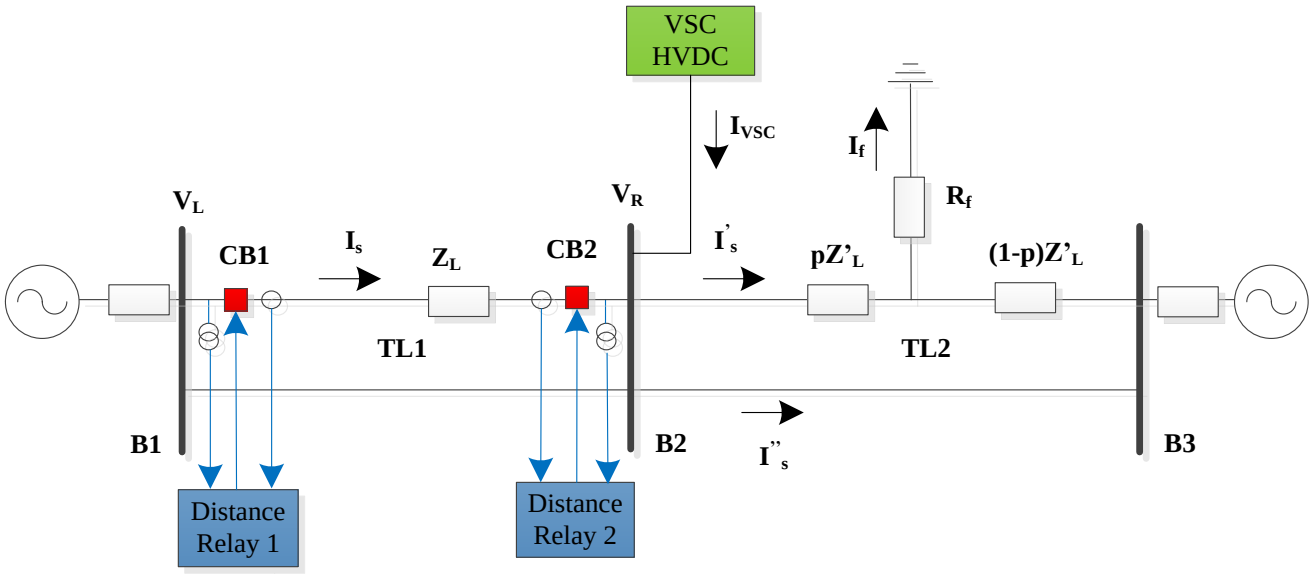


Figure 4- 5 Simplified SLD of a faulted network for the analysis of impacts of VSC system.

The distance protection used on TL1 applies the normal protection scheme that is presented in 4.2. Two distance relays, Distance relay 1 and Distance relay 2 are set to use Zone 1 and Zone 2 protection. The relay settings for Zone 1 protection is 75% of the line impedance. The relay settings for Zone 2 protection is 150% of the line impedance so that the full protection range of Zone 1 and Zone 2 protection of a distance relay covers the full length of transmission line. Plain impedance characteristic of distance relay is considered in this study.

The VSC converter connected at *B2* is modelled as that presented in Chapter 2. The control mode of VSC control system can be set to DC voltage regulation or active power transfer control for *d* axis, and AC voltage regulation or reactive power control for *q* axis.

Considering the fact that VSC HVDC is normally connected to busbars, the impacts of VSC HVDC system are mainly on Zone 2 protection. This is because the current infeed from VSC HVDC is without the protection range of Zone 1 protection but it is within the protection range of Zone 2 protection. Hence the distance protection against internal fault of TL1 is not affected by the incorporation of VSC, but the external fault located at TL2 is affected by the incorporation of VSC HVDC.

The apparent impedance of VSC-connected transmission line measured by distance relay is derived for SLG faults and three-phase faults to investigate the impacts of VSC HVDC system on distance protection.

For SLG faults, the voltages seen by VT at *B1* can be expressed as follows:

$$V_{Lx} = Z_{Lx}I_{sx} + pZ'_{Lx}I'_{sx} + I_{fx}R_f \qquad (4.18)$$

for $x = 1,2, or\ 0$ as a suffix denote of the sequence components, where

V_{Lx} : sequence voltages seen by VT at *B1*

I_{sx} : sequence currents seen by CT at *B1*

I'_{sx} : sequence phase current through faulted single-circuit of *TL2* from *B2* to *B3*

I_{fx} : sequence current through fault resistance

R_f : fault resistance

$Z_{Lx}$and Z'_{Lx} : sequence components of the line impedance of *TL1* and *TL2*.

p : fault location from *B2* to *B3* in per unit of the total line length

The line positive and negative sequence impedances are assumed equal.

$$Z_{L1} = Z_{L2}, Z'_{L1} = Z'_{L2} \qquad (4.19)$$

By adding all three sequence components of left-hand side of (4.18) and substitute (4.19) into (4.18), the voltages seen by VT can be expressed after simplification as follows:

$$V_L = Z_{L1}(I_s + kI_{s0}) + pZ'_{Lx}(I'_s + k'I'_{s0}) + I_f R_f \qquad (4.20)$$

where

$V_L$and I_s : phase voltage and current of faulted phase through *TL1*

I'_s : phase current of faulted phase through faulted single-circuit of *TL2* from *B2* to *B3*

I_f : fault current through fault resistance

k : zero sequence current compensation factors of *TL1*

k' : zero sequence current compensation factors of *TL2*

$$k = \frac{Z_{L0} - Z_{L1}}{Z_{L1}} \tag{4.21}$$

$$k' = \frac{Z'_{L0} - Z'_{L1}}{Z'_{L1}} \tag{4.22}$$

For transient response study of double-circuit transmission line, the fault currents through the double circuits of *TL1* can be assumed to be equal due to the line parameters of double circuits are same. Hence, by use of KCL law to *B2*, the relationship of inflow currents and outflow currents can be expressed as follows:

$$2I_s + I_{VSC} = I'_S + I''_S \tag{4.23}$$

where

I_{VSC} : phase current infeed from VSC HVDC

I''_S : phase current of faulted phase through unfaulted single-circuit of *TL2* from *B2* to *B3*

By substitute (4.23) into (4.20), the voltages seen by VT can be expressed as follows:

$$V_L = Z_{L1}(I_s + kI_{s0}) + pZ'_{Lx}[2I_s + I_{VSC} - I''_S + k'(2I_{s0} + I_{VSC0} - I''_{S0})] + I_f R_f \tag{4.24}$$

By use of delta connection at one side of the coupling transformer of VSC converter, the zero-sequence current injection can be eliminated [155]. Hence the zero-sequence current of VSC is eliminated.

$$I_{VSC0} = 0 \tag{4.25}$$

By substitute (4.25) into (4.24), the voltages seen by VT can be expressed as follows:

$$V_L = Z_{L1}(I_s + kI_{s0}) + pZ'_{Lx}[2I_s + I_{VSC} - I''_S + k'(2I_{s0} - I''_{S0})] + I_f R_f \quad (4.26)$$

By use of phase voltage measurements at *B1* (V_L) and phase current measurement compensated by zero sequence current (I_L), the apparent impedance seen by the Distance relay 1 are given as:

$$Z_{relay1} = \frac{V_L}{I_L} = Z_{L1} + pZ'_{L1}\frac{2I_s + I_{VSC} - I''_S + k'(2I_{s0} - I''_{S0})}{I_s + kI_{s0}} + \frac{I_f}{I_L}R_f$$

$$= Z_{L1} + pZ'_{L1}\frac{2I_s - I''_S + k'(2I_{s0} - I''_{S0})}{I_s + kI_{s0}} + pZ'_{L1}\frac{I_{VSC}}{I_s + kI_{s0}} + \frac{I_f}{I_L}R_f \quad (4.27)$$

$$I_L = I_s + kI_{s0} \quad (4.28)$$

where

Z_{relay1} : apparent impedance measured Distance relay 1

I_L : compensated phase current of faulted phase measure by Distance relay 1

For three-phase faults, the phase current seen by distance relay is as follows:

$$I_L = I_s + kI_{s0} = I_s \quad (4.29)$$

$$I_{s2} = I_{s0} = 0 \quad (4.30)$$

$$I'_{s2} = I'_{s0} = 0 \quad (4.31)$$

Similarly, the apparent impedance seen by the distance relay is given as follows:

$$Z_{relay1} = \frac{V_L}{I_L} = Z_{L1} + pZ'_{L1}\frac{2I_s + I_{VSC} - I''_S}{I_s} + \frac{I_f}{I_L}R_f$$

$$= Z_{L1} + pZ'_{L1}\frac{2I_s - I''_S}{I_s} + pZ'_{L1}\frac{I_{VSC}}{I_s} + \frac{I_f}{I_L}R_f \quad (4.32)$$

By carefully looking into (4.27) and (4.32), the VSC's impacts on the apparent impedance measured by Distance relay 1 in case of external fault can be summarised as:

1. The first and second terms ($Z_{L1} + pZ'_{L1}\frac{2I_s - I''_S + k'(2I_{s0} - I''_{S0})}{I_s + kI_{s0}}$ and $Z_{L1} + pZ'_{L1}\frac{2I_s - I''_S}{I_s}$) of (4.27) and (4.32) represent the actual line impedance of *TL1* and proportional line impedance of

TL2 to the fault location. The fourth term ($\frac{I_f}{I_L}R_f$) represents the contribution of fault resistance. These terms (the first, second and fourth) are not affected by the integration of VSC HVDC.

2. The third terms ($pZ'_{L1}\frac{I_{VSC}}{I_L}$) of (4.27) and (4.32) indicates that the VSC HVDC's impacts on the apparent impedance measured by Distance relay 1 against external fault lead to greater apparent impedance measurement. The under-reach effect is introduced as the impacts of VSC HVDC. Since during external fault, the VSC is injecting reactive power and current to support bus voltage, the apparent impedance is greater than test system with no VSC HVDC. For steady state, while VSC HVDC is absorbing reactive power and current from bus bar, the third term could be negative. This negative value indicates less apparent impedance of connected *TL1*, which results in overreach effect as the impacts of VSC HVDC. This error in apparent impedance measurements caused by VSC HVDC is proportional to the current ratio of VSC HVDC and relay, and fault location.

4.4 Dynamic Simulation Study

4.4.1 Establishment of RTDS-based Hardware-in-Loop Testing Platform

A RTDS-based HIL testing platform for protective relay studies proposed in [168] is established as shown in Figure 4- 6. Digital signals are generated from RTDS, and converted into analogue signals via Giga-Transceiver Analogue Output (GTAO) card. The output analogue signals are amplified by power amplifier for practical distance protective relays. The trip signals are sent back from the protective relays to RTDS via the front panel to control the operations of circuit breakers. Identical network topology described in 4.3 is used for external fault test. The transmission line parameters and equivalent voltage source parameters are listed in Appendix B.1 and B.2.

As listed in Appendix B.2, the voltage level of equivalent voltage source is set based on transmission data from the Electricity Ten Year Statement (ETYS) published annually by National Grid UK. The internal impedance parameters at each end of transmission lines are set based on fault level data from the ETYS. As listed in Appendix B.1, the transmission line parameters are set based on transmission line data from the ETYS.

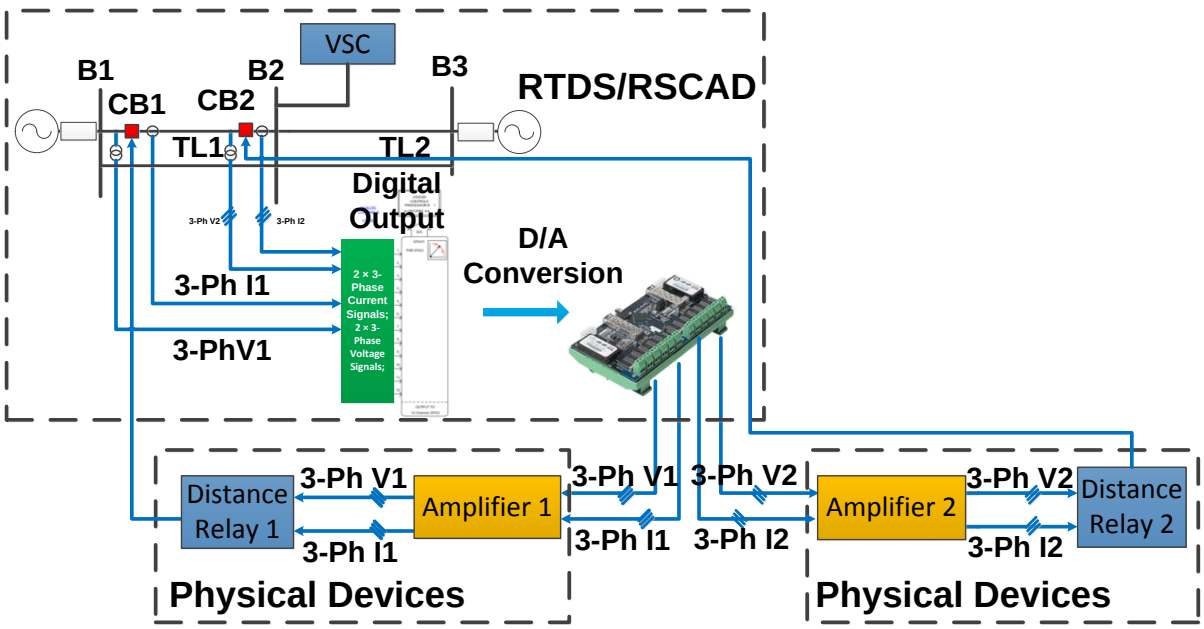


Figure 4- 6 RTDS-base HIL testing platform for VSC HVDC studies.

4.4.2 Test System with VSC HVDC and Protection Relay Settings

The schematic diagram of the trial network is illustrated in Figure 4- 6. There is one GE MiCOM P40 Agile P443 distance relay located at each end of two-ended transmission lines from *B1* to *B2*, measuring the local current and voltage signals. In this thesis, communications between relays are not considered.

Figure 4- 6 shows the arrangements of VT, CT and CB for one of the aforementioned series compensated lines between B1 and B2. Distance protection using GE MiCOM P40 Agile P443 distance protection relays is used. Two VTs and two CTs at both ends of the transmission line provide voltage and current measurements. The transmission line parameters and equivalent voltage source parameters are listed in Appendix B.1 and B.2.

The following considerations are taken into account for the settings of the 2-ended distance protections:

1. Zone 1 is set to 75% of the complete circuit positive sequence impedance. The tripping delay is set to 0ms.
2. Zone 2 is set to reach 150% of the complete circuit positive sequence impedance. The tripping delay is set to 500ms.

4.4.3 Dynamic Simulation Result of Test System without/with VSC HVDC

External faults occur at one single-circuit of TL2 from B2 to B3 under such fault conditions:

1. 600ms fault occurred at 105% and 135% of the equivalent whole length of TL1.
2. Fault resistance is 0.01Ω, and 1 Ω.
3. SLG, and three-phase to ground faults are considered.

Table 4- 1 shows the simulation results of external fault. The tripped zone is noted as "I", "II", or "X" for Zone 1, Zone 2 or no relay operation is seen, respectively. Fault type is noted as "RYB-G", or "R-G" for three-phase to ground, or SLG faults, respectively.

Table 4- 1 Simulation results for test system without/with VSC HVDC against external fault

Case	Fault Location	Fault Impedance	Fault Type	Fault Duration	Distance relay 1	
					No VSC	VSC
1	105%	0.01Ω	RYB-G	600ms	**II 105.6%**	**II 107.6%**
2	105%	0.01Ω	R-G	600ms	**II 106.1%**	**II 108.2%**
3	105%	1Ω	RYB-G	600ms	**II 106.0%**	**II 108.3%**
4	105%	1Ω	R-G	600ms	**II 106.6%**	**II 108.8%**
5	135%	0.01Ω	RYB-G	600ms	**II 136.4%**	**II 143.1%**
6	135%	0.01Ω	R-G	600ms	×	×
7	135%	1Ω	RYB-G	600ms	×	×
8	135%	1Ω	R-G	600ms	×	×

Figure 4- 7 shows digital signals from RSCAD for a typical external fault Case 1 of Table 4- 1 with no VSC HVDC integration, and Figure 4- 7 shows the trajectory of impedance measurements by distance relay during fault. Figure 4- 8 shows digital signals from RSCAD for a typical external fault Case 1 of Table 4- 1 with VSC HVDC, and Figure 4- 8 shows the corresponding trajectory of impedance measurements by distance relay.

As shown in Figure 4- 8, VT and CT send voltage and current measurements (noted as VA/VB/VC and IA/IB/IC) to distance relay. By use of the received measurements and impedance calculation algorithm presented in 4.3, the apparent impedance is calculated (noted as ZIM vs ZRE in Figure 4- 8). The trip signals (noted as TripA/TripB/TripC in Figure 4- 8) are sent to corresponding CBs, by judgement if calculated apparent impedance is within protection zones. The CBs are turn off or turn on (noted as CBA/CBB/CBC in Figure 4- 8), controlled by received trip signals.

By comparison of the apparent impedances measured by distance relay, the apparent impedance with VSC is greater than impedance with no VSC HVDC integration. The under-reach effect of distance relay is seen due to the incorporation of VSC HVDC.

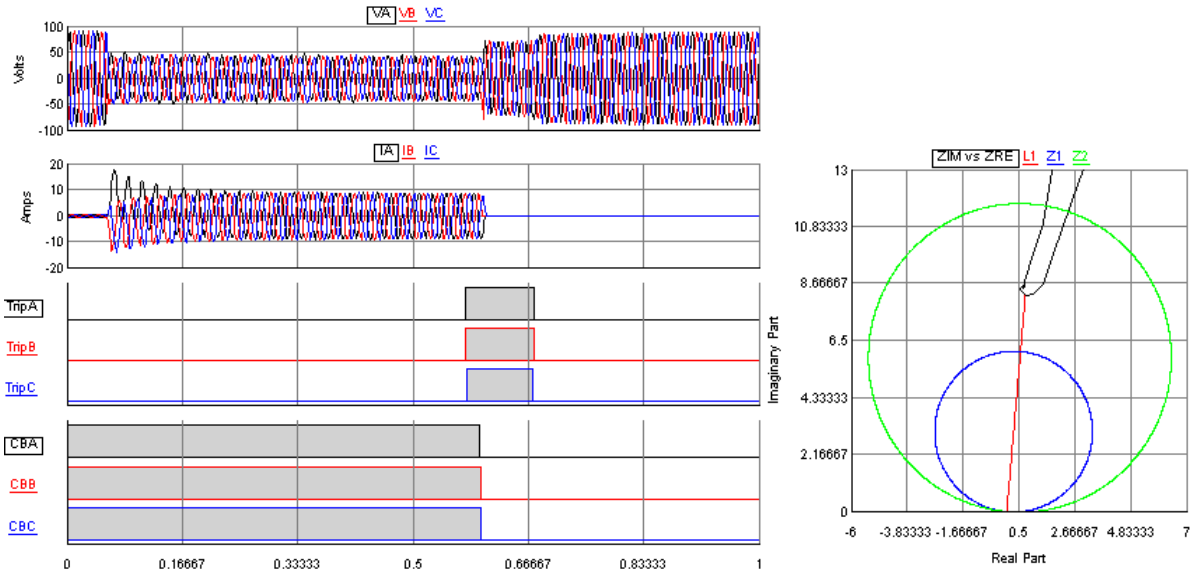


Figure 4- 7 Digital signals from RSCAD for test system without VSC HVDC in Case 1.

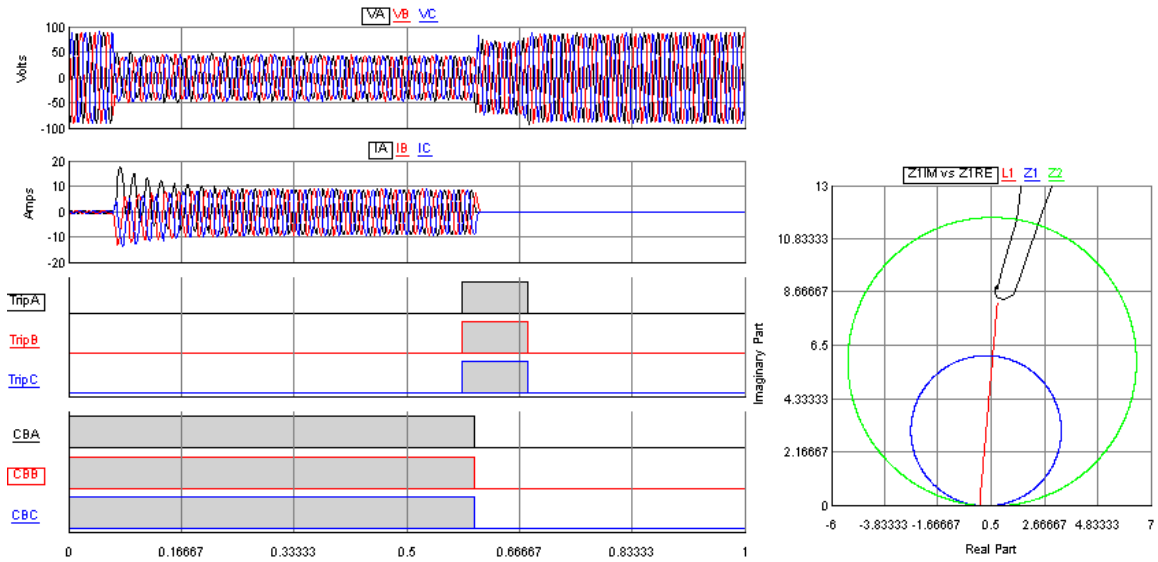


Figure 4- 8 Digital signals from RSCAD for test system with VSC HVDC in Case 1.

Figure 4- 9 shows digital signals from RSCAD for a SLG external fault Case 2 of Table 4- 1 with VSC HVDC.

As voltage and current measurement of VT and CT (noted as VA/VB/VC and IA/IB/IC) shown in Figure 4- 9, SLG fault occurred. The three-phase trip signals (noted as TripA/TripB/TripC) are sent to corresponding CBs. This is due to the fact that distance relay settings require relays trip all three phases for Zone 2 protection.

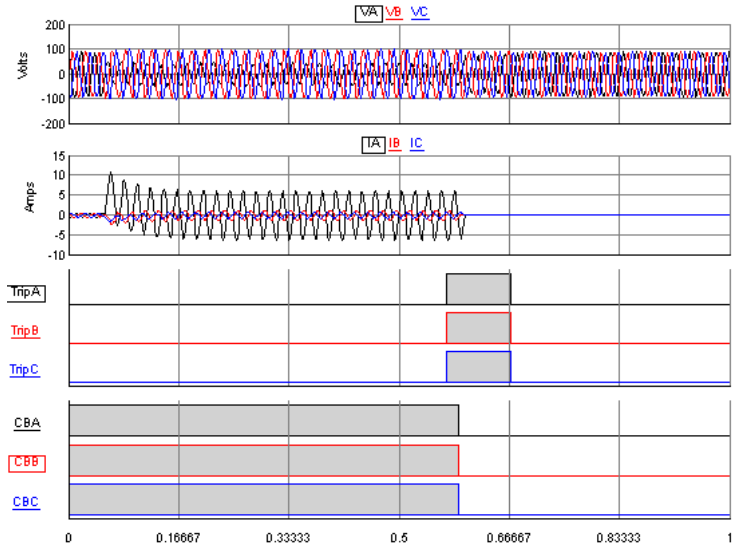


Figure 4- 9 Digital signals from RSCAD for test system with VSC HVDC in Case 2.

Figure 4- 10 shows digital signals from RSCAD for a 1 Ω external fault Case 3 of Table 4- 1 with VSC HVDC integration, and Figure 4- 10 shows the trajectory of impedance measurement by distance relay. By comparison of the apparent impedances measured by distance relay, the apparent impedance against 1 Ω fault is greater than impedance against

0.01 Ω. These results are in line with the conclusion in 4.3 that the error of measured impedance is positively related to fault resistance.

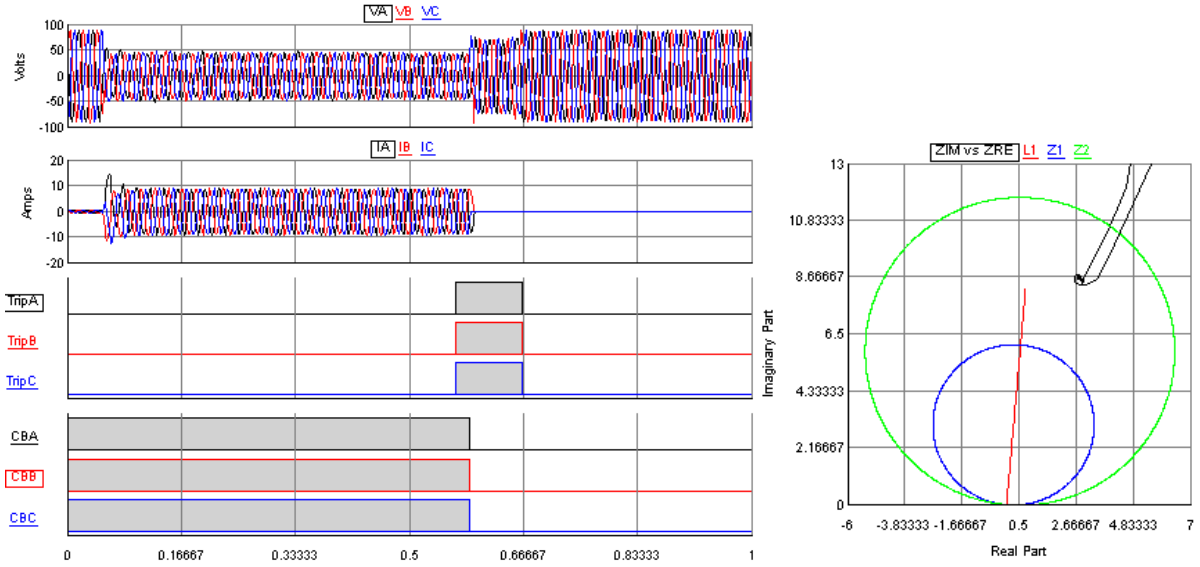


Figure 4- 10 Digital signals from RSCAD for a 1 Ω external fault Case 3.

Figure 4- 11 shows digital signals from RSCAD for a 135% external fault Case 7 of Table 4-1 with VSC HVDC integration, and Figure 4- 11 shows the trajectory of impedance measurement by distance relay. It can be seen from Figure 4- 11 that the distance relay is not tripped if the fault distance is too far. By comparison of the apparent impedances measured by distance relay, the apparent impedance against 135% fault is greater than impedance against 105% fault. These results are in line with the conclusion in 4.3 that the error of measured impedance is positively related to fault distance.

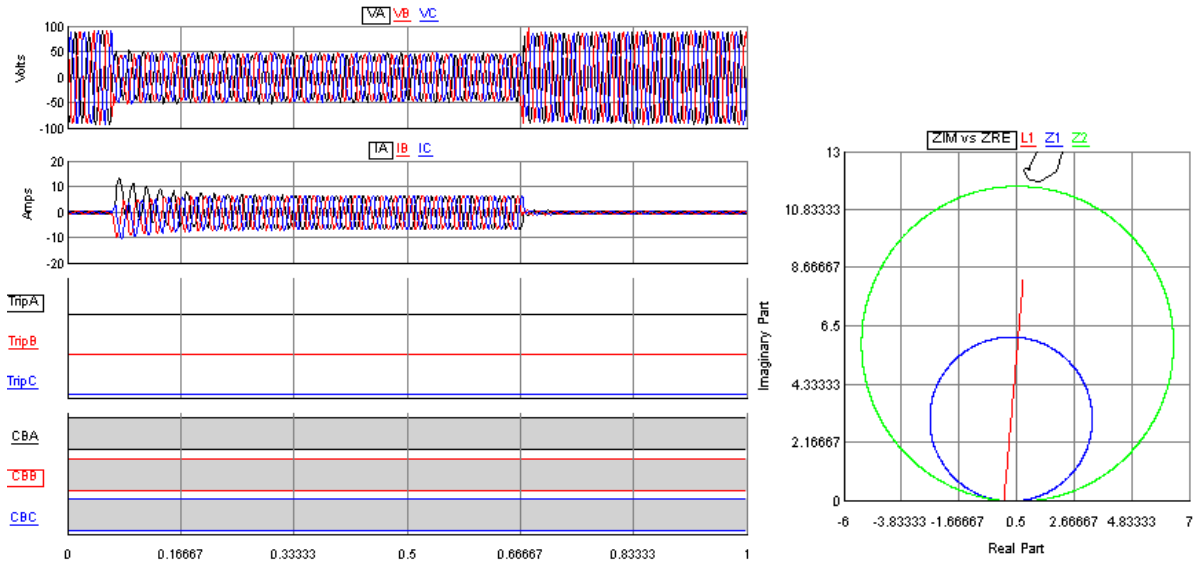


Figure 4- 11 Digital signals from RSCAD for a 135% external fault Case 7.

4.5 Summary

In this chapter typical feeder distance protection of two-ended overhead transmission lines has been reviewed, including basic principles of distance protection, zones of protection, distance relay characteristics, and under-reach and over reach effect of distance relay application. Mathematical representation of the apparent impedance measurements of distance relay for Zone 2 protection has been derived considering infeed current from VSC HVDC connected busbar. For derived mathematical representation of apparent impedance measurement of distance relay for Zone 2 protection against external faults, some part (the first, second and fourth terms) is not affected by the integration of VSC HVDC while the other part (the third term) indicates that the VSC HVDC's impacts on apparent impedance measured by distance relay against external fault lead to a greater apparent impedance measurement. The under-reach effect is introduced as the impacts of VSC HVDC. Since during external fault, the VSC is injecting reactive power and current to support bus voltage, the apparent impedance is greater than test system with no VSC HVDC. For steady state, while VSC is absorbing reactive power and current from bus bar, the third term could be negative. This negative value indicates less apparent impedance of connected TL1, which results in overreach effect as impact of VSC HVDC. This error in apparent impedance measurements caused by VSC HVDC is proportional to the current ratio of VSC HVDC and relay, and fault location.

As shown in dynamic simulation results in RTDS/RSCAD, the apparent impedance with VSC HVDC is greater than impedance with no VSC HVDC integration, by comparison of the apparent impedances measured by distance relay. The under-reach effect of distance relay is seen due to the incorporation of VSC HVDC. The dynamic simulation results are in line with mathematical analysis presented in 4.3, considering the results that the error of measured impedance is positively related to fault resistance, and fault distance.

CHAPTER 5 IMPACTS OF VSC FACTS ON DISTANCE PROTECTION

5.1 Introduction

This chapter presents the mathematical representation of the apparent impedance measurements of distance relay considering the infeed current from shunt VSC FACTS (in particular, STATCOM as a typical example) connected busbar. Relevant analysis of the apparent impedance measurement representation and dynamic simulation study is implemented to investigate the impacts of VSC FACTS on distance protection. In 5.2, dynamic representation of STATCOM is modelled considering its configuration and control system. In 5.3, mathematical representations of the apparent impedance measurements of neighbouring and remote distance relays against internal and external faults are derived considering infeed current from STATCOM connected at different busbars. A RTDS-based HIL testing platform is established to perform dynamic simulation studies of test system with STATCOM. The dynamic simulation results are analysed in comparison between test system without/with STATCOM at different locations against internal and external faults.

5.2 Modelling of STATCOM

The modelling of detailed delta-connected MMC based STATCOM is presented in this section, comprising of configuration, and control system.

5.2.1 Configuration of STATCOM

A static synchronous compensator (STATCOM), or static synchronous condenser (STATCON), is a VSC-based power electronics regulating system integrated to AC power transmission system. It is used to regulate AC voltage or provide reactive AC power to the connected power network. It is a commonly used shunt device of FACTS family and a typical example of shunt VSC FACTS to study in this thesis.

As the same with VSC HVDC, there a number of various topologies of STATCOM in different voltage levels, since the converter of STATCOM is VSC based. These topologies vary in different voltage levels, depending on different application scenarios: two-level

converter, three-level converter, or multilevel modular converter. As for the connection topologies for converter legs, unlike VSC HVDC, there are two connections for converter legs for STATCOM, star-connection and delta-connection. Figure 5- 1 shows the topology of a star-connected STATCOM which shares the same VSC converter topology of VSC-HVDC system as reviewed in 2.2, only except that the DC side of STATCOM is a DC storage capacitor rather than DC link to DC network.

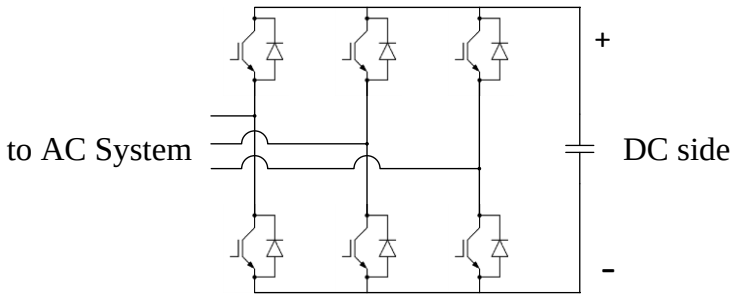


Figure 5- 1 Topology of a star-connected STATCOM.

The three-phase circuit configuration of the delta-connection MMC-based STATCOM is shown in Figure 5- 2. As shown in Figure 5- 2, the detailed model of delta-connected STATCOM consists of three MMC-based legs. There are 26 full-bridge submodules and two identical series phase reactors in each leg. Full-bridge IGBT-based valve is applied for all submodules. All the full-bridge submodules are identical, and all the switches and diodes have the same ratings.

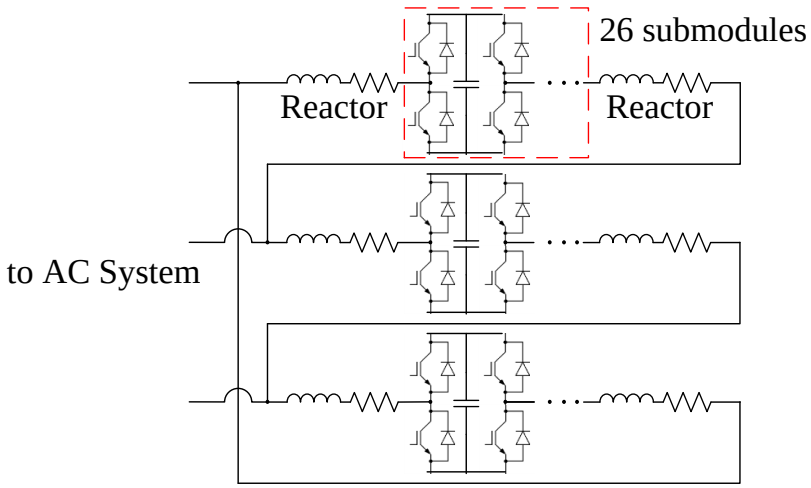


Figure 5- 2 Three-phase circuit configuration of the MMC-based STATCOM.

The purposes of using delta-connection of STATCOM are as follows [59,115,119-120]:

1. By use of delta topology, the zero sequence fundamental current is circulated through the arm converters to keep active power of each phase is zero, when it is connected to unbalanced circuit.

2. The rated current of switching devices is lower compared to star-connection.

5.2.2 Control System of STATCOM

The single-line diagram of the STATCOM and its control system is shown in Figure 5- 3. *dq* decoupling control is used. AC side voltage at common coupling point or the reactive power compensated by STATCOM is controlled. The active power and reactive power exchange between the STATCOM and the connected AC network are given by:

$$P = \frac{V_{c,abc}V_{t,abc}}{X_c}\sin\delta \quad (5.\ 1)$$

$$Q = \frac{V_{c,abc}\cos\delta - V_{t,abc}}{X_c}V_{t,abc} \quad (5.\ 2)$$

where

$V_{c,abc}$ and $V_{t,abc}$: magnitudes of converter output voltage of STATCOM and the connected AC network voltage at PCC, respectively

X_c : equivalent reactance between STATCOM and the connected AC network

δ : angle difference between the converter output voltage of STATCOM and the connected AC network voltage at PCC

During normal steady state operation with the active power losses of converter ignored, the generated voltage of STATCOM is in phase with voltage at PCC of connected power system. This means there is no active power flow between STATCOM and connected power system. Only reactive power is transferred. When Q is positive, the STATCOM supplies reactive power to the external ac network. When Q is negative, the STATCOM absorbs reactive power from the external ac network. The amount of reactive power transfer during steady state can be expressed as follows:

$$Q = \frac{V_{c,abc} - V_{t,abc}}{X_c}V_{t,abc} \quad (5.\ 3)$$

Hence the direction of reactive power flow can be determined by comparing the magnitudes of converter output voltage of STATCOM ($V_{c,abc}$) and external AC network voltage at common coupling point ($V_{t,abc}$). If $V_{c,abc}$ is greater than $V_{t,abc}$, reactive power is flowing from STATCOM to the power system. If $V_{c,abc}$ is less than $V_{t,abc}$, reactive power is flowing from the power system to STATCOM. In this way, the reactive power control or AC voltage regulation can be achieved, by control of converter output voltage of STATCOM.

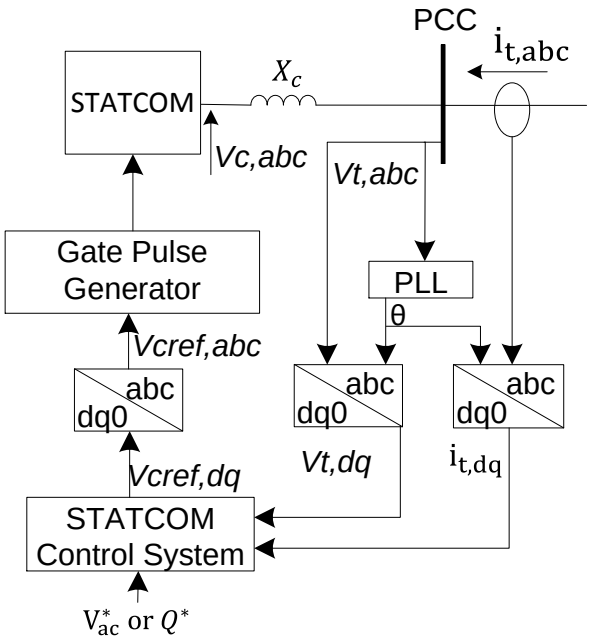


Figure 5- 3 Single-line diagram of the STATCOM and its control system.

As the single-line diagram of the control system of STATCOM shown in Figure 5- 3, the line-to-line voltages $v_{t,abc}$ and currents $i_{t,abc}$ at PCC (the primary side of the coupling transformer of VSC) in *abc* phase are acquired. The line-to-line voltages at PCC $v_{t,abc}$ are inputted into PLL block to compute its frequency f and phase angle θ. Then the computed phase angle θ, along with line-to-line voltages $v_{t,abc}$ and currents $i_{t,abc}$ at PCC are input into two *abc*-to-*dq0* transformation blocks (which are the same as those of VSC converter presented in 2.2) to compute line-to-line voltages $v_{t,dq}$ and currents $i_{t,dq}$ in *dq0* frame. The computed line-to-line voltages $v_{t,dq}$ and currents $i_{t,dq}$ in *dq0* frame, along with reference of AC voltage at the AC terminal of VSC V_{ac}^* or reference of reactive power transfer Q^* (these two references are set by user) are inputted into the STATCOM control system (which includes converter outer control loop and converter inner control loop). Through STATCOM control system block, the output signal is the computed reference of AC voltage at the AC terminal of STATCOM $v_{cref,dq}$in dq frame. Then the computed reference of AC voltage at

the AC terminal of STATCOM $v_{cref,dq}$ is inputted *dq0*-to-*abc* transformation block. Through *dq0*-to-*abc* transformation block, the output signal is the computed reference of AC voltage at the AC terminal of STATCOM $v_{cref,abc}$ in *abc* phase. The computed reference of AC voltage at the AC terminal of STATCOM $v_{cref,abc}$ is inputted into gate pulse generator block to compute and generate corresponding gate pulses to control valves of submodules. The output of gate pulse generator block is gate pulse signals which are inputted into STATCOM converter to control every valve of submodules to either turn on or turn off.

By use of the state variables in *dq* frame, the dynamic equations of the STATCOM connected to AC system by series reactor at PCC can be represented as follows:

$$v_{cd} - v_{td} = -L_c \frac{di_{td}}{dt} + L_c \omega i_{tq} \tag{5.4}$$

$$v_{cq} - v_{tq} = -L_c \frac{di_{tq}}{dt} - L_c \omega i_{td} \tag{5.5}$$

where

ω : angular velocity derived of AC voltage at PCC

L_c : equivalent inductance of reactor

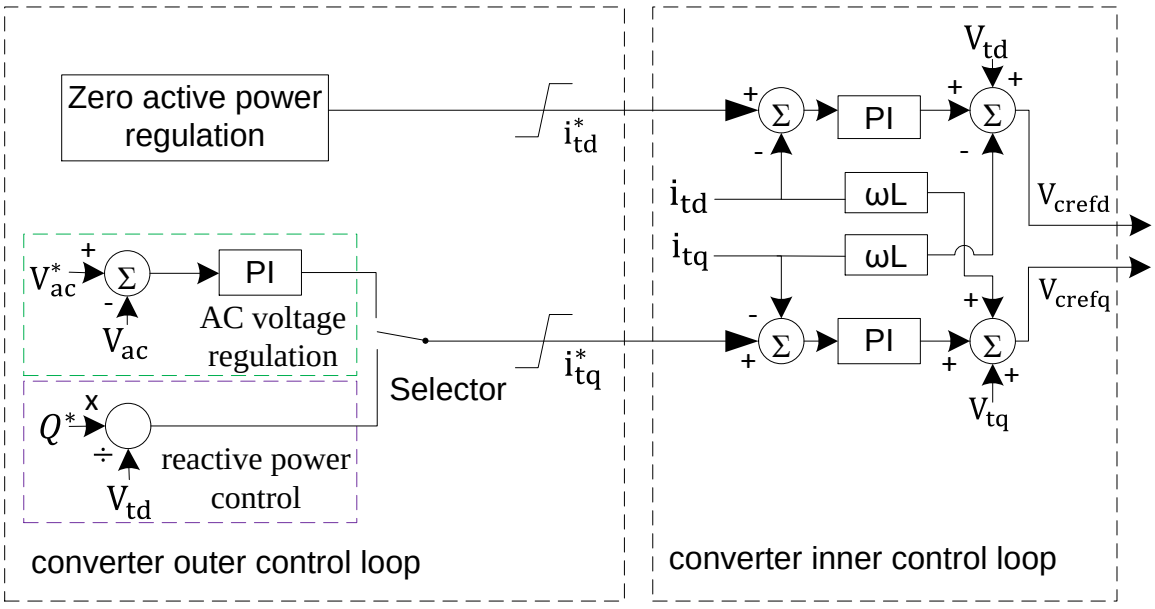


Figure 5- 4 Architecture of the STATCOM control system block.

The architecture of the STATCOM control system block of the whole control system of STATCOM is shown in Figure 5- 4. The STATCOM can operate in either AC voltage regulation mode or reactive power control mode. The STATCOM control system block consists of converter outer control loop and converter inner control loop. Reference of AC voltage at the AC terminal of converter V_{ac}^{*} , reference of reactive power transfer Q^{*}, V_{ac} , and v_{td} are inputted into converter outer control loop. The zero active power regulation block is used to compute reference of line-to-line current at PCC in d-axis i_{td}^{*}. The details of zero active power block is not included since this block is not a necessity and could be replaced by other control block, such as voltage balance control block. This is due to i_{td}^{*} is usually set to zero for normal STATCOM operation. For AC voltage regulation block, the difference of V_{ac}^{*} and V_{ac} is inputted into a PI control loop to compute the output signal. For reactive power control block, the division of Q^{*}divided by v_{td} formulates the output. A selector is controlled by user to assign the control system of STATCOM to operate either in AC voltage regulation or reactive power control mode in q frame. The output of selector is then inputted to limitation block to compute the final output signals of converter outer control loop i_{tq}^{*}, which is the reference of line-to-line current at PCC in q frame.

When converter outer control loop operates in AC voltage regulation mode in q frame, the current reference in i_{tq}^{*} can be obtained from the converter outer control loop by:

$$i_{tq}^{*} = k_{pac}(V_{ac}^{*} - V_{ac}) + k_{iac}\int (V_{ac}^{*} - V_{ac})dt$$

$$= k_{pdc}(V_{ac}^{*} - V_{ac}) + k_{iac}x_1 \qquad (5.6)$$

where

k_{pac} : proportional gain of the PI control loop of converter outer control loop in q frame

k_{iac} : integral gain of PI control loop of converter outer control loop in q frame

x_1 : auxiliary state variable to represent the integral terms of the PI control loop of converter outer control loop in q frame

And the AC voltage at point of common coupling V_{ac1} can be represented as:

$$V_{ac} = \sqrt{{v_{td}}^2 + {v_{tq}}^2} \qquad (5.7)$$

When converter outer control loop operates in reactive power control mode in q frame, the current reference in i_{tq}^* can be obtained from the converter outer control loop by:

$$i_{tq}^* = \frac{Q^*}{v_{td}} \tag{5. 8}$$

The reference of line-to-line current at PCC in dq frame i_{td}^* and i_{tq}^*, along with acquired value of line-to-line current at PCC in dq frame i_{td} and i_{tq}, are inputted into converter inner control loop. The difference of i_{td}^* and i_{td}, is inputted into PI controller loop and then added by v_{td} subtracted by $\omega L i_{tq}$ to compute output signal of v_{crefd}. The difference of i_{tq}^* and i_{tq}, is inputted into PI controller loop and then added by v_{td} and $\omega L i_{td}$ to compute output signal of v_{crefq}.

The reference of voltage at the AC terminal of STATCOM $v_{cref,dq}$ can be obtained from the converter inner control loop as:

$$\begin{aligned} v_{crefd} &= k_{pvd}(i_{td}^* - i_{td}) + k_{ivd}\int (i_{td}^* - i_{td})dt - \omega L_C i_{tq} + v_{td} \\ &= k_{pvd}(i_{td}^* - i_{td}) + k_{ivd}x_3 - \omega L_C i_{tq} + v_{td} \end{aligned} \tag{5. 9}$$

$$\begin{aligned} v_{crefq} &= k_{pvq}\left(i_{tq}^* - i_{tq}\right) + k_{ivq}\int \left(i_{tq}^* - i_{tq}\right)dt + \omega L_C i_{td} + v_{tq} \\ &= k_{pvq}\left(i_{tq}^* - i_{tq}\right) + k_{ivq}x_4 + \omega L_C i_{td} + v_{tq} \end{aligned} \tag{5. 10}$$

where

k_{pvd}, and k_{ivd} : proportional and integral gain of the PI control loop of converter inner control loop in *d* frame

k_{pvq}, and k_{ivq} : proportional and integral gain of the PI control loop of converter inner control loop in *q* frame

x_3 : auxiliary state variable to represent the integral terms of the PI control loop of converter inner control loop in *d* frame

x_4 : auxiliary state variable to represent the integral terms of the PI control loop of converter inner control loop in *q* frame

The dynamics of modulation of submodules and gate pulse generator are not considered in this study.

5.3 Impacts of STATCOM on Distance Protection

The mathematical analysis of the impacts of STATCOM on the apparent impedance measured by feeder distance protection relay is presented in this section. The impacts of STATCOM are studied in aspects of internal faults and external faults. Zone 1 and Zone 2 protection as presented in Chapter 4 are applied for distance protection.

5.3.1 Analysis of Internal Faults

Figure 5- 5 shows the simplified single line diagram of a faulted network for the analysis of internal faults. Same topology of power network is studied as the investigation of VSC HVDC's impacts on distance protection presented in Chapter 4, except that the STATCOM is integrated into power network instead of VSC HVDC. Two AC systems (represented by ideal voltage source with internal impedance) are connected via double-circuit transmission lines *TL1* and *TL2*. A STATCOM is connected near *B1* (the distance between STATCOM and *B1* can be neglected) to provide voltage support. Two distance relays (Distance relay 1 and Distance relay 2) are located at the both ends of the faulted single-circuit of *TL1*. These distance relays collect voltage and current measurements from VT and CT and send trip signals to circuit breakers (CB1 and CB2). An internal SLG fault or three-phase fault on *TL1* is occurred at *p*% of the full length of *TL1* from *B1*.

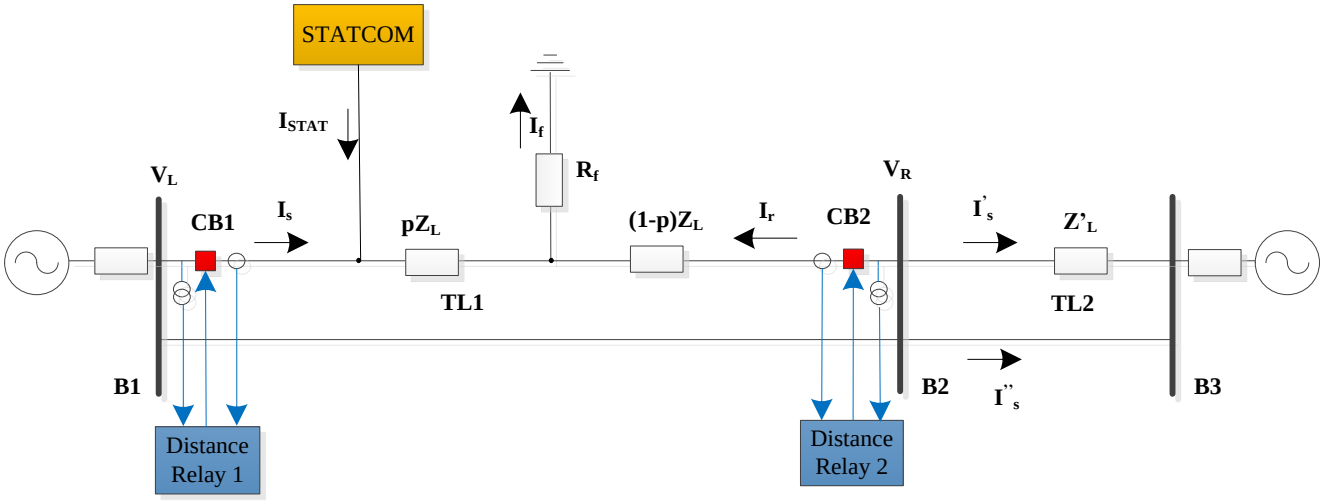


Figure 5- 5 Simplified SLD of test network for internal fault.

The distance protection used on *TL1* applies the normal protection scheme that is presented in 4.2. Same relay settings are applied as those of investigation of VSC HVDC's impacts on distance protection in Chapter 4. Two distance relays, Distance relay 1 and Distance relay 2 are set to use Zone 1 and Zone 2 protection. The relay settings for Zone 1 protection is 75% of the line impedance. The relay settings for Zone 2 protection is 150% of the line impedance so that the full protection range of Zone 1 and Zone 2 protection of a distance relay covers the full length of transmission line. Plain impedance characteristic of distance relay is considered in this study.

The STATCOM connected at *B1* is modelled as that presented in 5.2. The control mode of STATCOM control system can be set to AC voltage regulation or reactive power control. On the contrary to the investigation of VSC HVDC's impacts on distance protection, the location of STATCOM is within the protection reach of Zone 1 protection and Zone 2 protection. This is due to the fact that shunt FACTS devices can be installed on transmission lines (for instance, mid-point shunt compensation [89,155]), and at busbars (busbar voltage regulation or reactive power source). Hence the impacts of STATCOM on distance protection against internal faults of *TL1*, and external faults located at *TL2* are both considered.

The apparent impedance of STATCOM-compensated transmission line measured by distance relays are derived for SLG faults and three-phase faults.

For SLG faults, the voltages seen by VTs at both ends of *TL1* can be expressed as:

$$V_{Lx} = pZ_{Lx}(I_{STATx} + I_{sx}) + I_{fx}R_f \quad (5.\ 11)$$

$$V_{Rx} = (1 - p)Z_{Lx}I_{rx} + I_{fx}R_f \quad (5.\ 12)$$

for $x = 1,2, or\ 0$ as a suffix denote of the sequence components, where

V_{Lx} and V_{Rx} : sequence voltages seen by VTs at both ends of *TL1*

I_{sx} and I_{rx} : sequence currents seen by CTs at both ends of *TL1*

I_{STATx} : sequence currents infeed from STATCOM

I_{fx} : sequence current through fault resistance

R_f : fault resistance

Z_{Lx} : sequence components of the line impedance of *TL1*

p : fault location from *B1* to *B2* in per unit of the total line length

The line positive and negative sequence impedances are assumed equal.

$$Z_{L1} = Z_{L2} \quad (5.\ 13)$$

By adding all three sequence components of left-hand side of (5.11)-(5.12) and substitute (5.13) into (5.11)-(5.12), the voltages seen by VTs can be expressed after simplification as follows:

$$V_L = pZ_{L1}(I_s + kI_{s0}) + pZ_{L1}(I_{STAT} + kI_{STAT0}) + I_f R_f \quad (5.\ 14)$$

$$V_R = (1 - p)Z_{L1}(I_r + kI_{r0}) + I_f R_f \quad (5.\ 15)$$

where

$V_L$and V_R : phase voltage of faulted phase at both ends of *TL1*

$I_s$and I_r : phase current of faulted phase through *TL1* at both ends

I_f : fault current through fault resistance

k : zero sequence current compensation factors of *TL1*

$$k = \frac{Z_{L0} - Z_{L1}}{Z_{L1}} \quad (5.\ 16)$$

By use of phase voltage measurements at both ends of transmission lines (V_L and V_R) and phase current compensated by zero sequence current (I_L andI_R), the apparent impedances seen by the distance relays are given as:

$$Z_{relay1} = \frac{V_L}{I_L} = pZ_{L1} + \frac{pZ_{L1}(I_{STAT} + kI_{STAT0})}{I_L} + \frac{I_f}{I_r}R_f \quad (5.\ 17)$$

$$Z_{relay2} = \frac{V_R}{I_R} = (1-p)Z_{L1} + \frac{I_f}{I_s}R_f \quad (5.\ 18)$$

$$I_L = I_s + kI_{s0} \quad (5.\ 19)$$

$$I_R = I_r + kI_{r0} \quad (5.\ 20)$$

$$I_f = I_s + I_{STAT} + I_r \quad (5.\ 21)$$

where

Z_{relay1} and Z_{relay2} : apparent impedances measured by Distance relay 1 and Distance relay 2

I_L and I_R: compensated phase current of faulted phase measure by Distance relay 1 and Distance relay 2

By use of delta connection at one side of the coupling transformer of STATCOM, the zero-sequence current injection can be eliminated. Hence the zero-sequence current of STATCOM is eliminated.

$$I_{STAT0} = 0 \quad (5.\ 22)$$

Then (5.17) can be further simplified as:

$$Z_{relay1} = pZ_{L1} + pZ_{L1}\frac{I_{STAT}}{I_L} + \frac{I_f}{I_r}R_f \quad (5.\ 23)$$

For three-phase faults, the phase currents seen by distance relay are:

$$I_L = I_s + kI_{s0} = I_s \quad (5.\ 24)$$

$$I_R = I_r + kI_{r0} = I_r \quad (5.\ 25)$$

$$I_{s2} = I_{s0} = 0 \tag{5. 26}$$

$$I_{r2} = I_{r0} = 0 \tag{5. 27}$$

Similarly, the apparent impedances seen by the distance relays are given as:

$$Z_{relay1} = \frac{V_L}{I_L} = pZ_{L1} + pZ_{L1}\frac{I_{STAT}}{I_s} + \frac{I_f}{I_r}R_f \tag{5. 28}$$

$$Z_{relay2} = \frac{V_R}{I_R} = (1-p)Z_{L1} + \frac{I_f}{I_r}R_f \tag{5. 29}$$

By carefully looking at (5.23) and (5.28), the STATCOM's impacts on the apparent impedance measured by neighbouring distance relay (Distance relay 1) against internal faults can be summarised as:

1. The first term (pZ_{L1}) of (5.23) and (5.28) represents the actual proportional line impedance to the fault location. This term is not affected by the compensation of STATCOM.
2. The second term ($pZ_{L1}\frac{I_{STAT}}{I_L}$) of (5.23) and (5.28) indicates that the STATCOM's impacts on the apparent impedance measured by neighbouring distance relay against internal faults lead to larger apparent impedance. The under-reach effect is introduced as the impact from STATCOM. Since during internal fault, the STATCOM is injecting reactive power and current to support bus voltage, the apparent impedance is greater than no STATCOM compensated transmission lines. For steady state, while STATCOM is absorbing reactive power and current from bus bar, the second term could be negative. This negative value indicates smaller apparent impedance measured by distance relays which results in overreach effect. This error in apparent impedance measurement caused by STATCOM is proportional to the fault location from *B1* to *B2* and the current ratio of STATCOM and relay.
3. The third term of (5.23) and (5.28) also indicates greater apparent impedance measured by neighbouring distance relay as STATCOM's impact, since$I_f = I_s + I_{STAT} + I_r$. A larger amount of current injection infeed from STATCOM would lead to a larger apparent impedance error and cause more significant under-reach effect.

Similarly, by carefully looking into (5.18) and (5.29), the STATCOM's impact on the apparent impedance measured by remote distance relay (Distance relay 2) against internal faults can be summarised as:

1. The first term ($(1-p)Z_{L1}$) of (5.18) and (5.29) represents the actual proportional line impedance to the fault location. This term is not affected by the compensation of STATCOM.
2. The second term ($\frac{I_f}{I_r}R_f$) of (5.18) and (5.29) indicates greater apparent impedance measured by remote distance relay as STATCOM's impact, since$I_f = I_s + I_{STAT} + I_r$. On the contrary to the neighbouring relay (Distance relay 1), the remote relay is only affected by the amount of current injection of STATCOM which can be seen from second term of (5.18) and (5.29). The location of fault has no effects on the error in measured impedance by remote relay. This issue can be explained by the fact that the STATCOM is located beyond the fault location seen from the remote relay. A greater amount of current injection of STATCOM would lead to a greater apparent impedance error and cause more significant under-reach effect.

5.3.2 Analysis of External Faults

Figure 5- 6 shows the simplified single line diagram of a faulted network for the analysis of external fault. Identical network topology described in 5.3.1 is used except that the fault location is located at one single-circuit of *TL2*. Same relay and STATCOM settings are applied as those of investigation of STATCOM's impacts on distance protection against internal faults in 5.3.1.

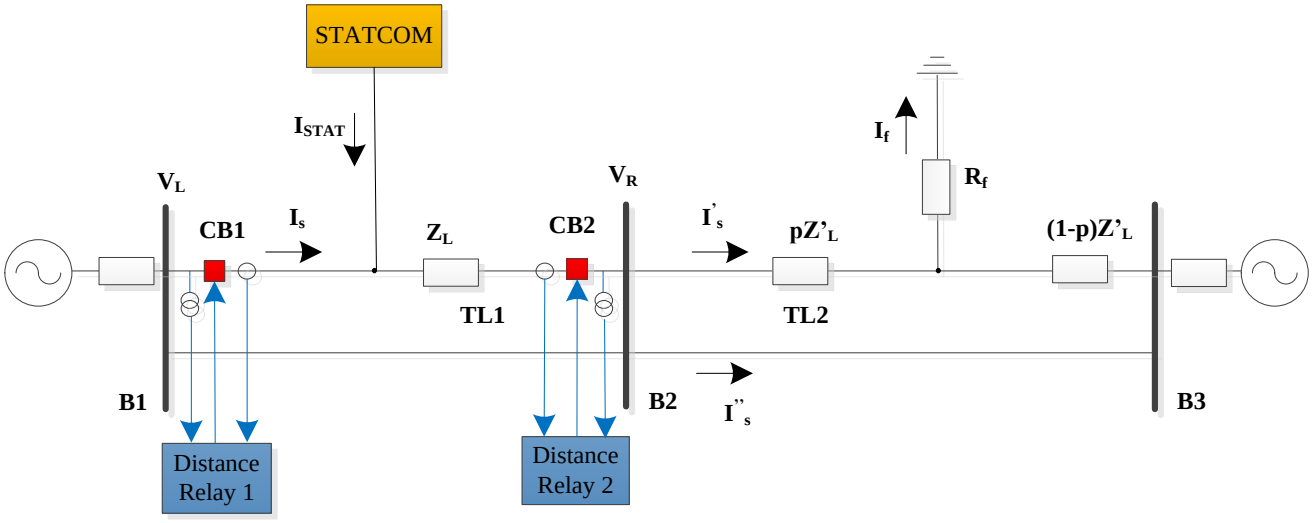


Figure 5- 6 Simplified network for external fault.

The apparent impedance of STATCOM-compensated transmission line measured by Distance relay 1 is derived for SLG fault and three-phase fault. The apparent impedance of Distance relay 2 is not considered in this subsection since the fault location is located without of the protection zones.

The voltage seen by VT at *B1* can be expressed as:

$$V_{Lx} = Z_{Lx}(I_{STATx} + I_{sx}) + pZ'_{Lx}I'_{sx} + I_{fx}R_f \qquad (5.\ 30)$$

for $x = 1,2, or\ 0$ as a suffix denote of the sequence components, where

I'_{sx} : sequence phase current through faulted single-circuit of TL2 from *B2* to *B3*

Z'_{Lx} : sequence components of the line impedance of *TL2*

p : fault location from *B2* to *B3* in per unit of the total line length

The line positive and negative sequence impedances are assumed equal.

$$Z'_{L1} = Z'_{L2} \qquad (5.\ 31)$$

By adding all three sequence components of left-hand side of (5.30) and substituting with (5.31), the voltages seen by VT can be expressed after simplification as:

$$V_L = Z_{L1}(I_s + kI_{s0}) + Z_{L1}(I_{STAT} + kI_{STAT0})$$

$$+pZ'_{Lx}(I'_s + k'I'_{s0}) + I_f R_f \quad (5.\ 32)$$

where

I'_s : phase current of faulted phase through faulted single-circuit of *TL2* from *B2* to *B3*

k' : zero sequence current compensation factors of *TL2*

$$k' = \frac{Z'_{L0} - Z'_{L1}}{Z'_{L1}} \quad (5.\ 33)$$

For transient response study of double-circuit transmission line, the fault currents through the double circuits of *TL1* can be assumed to be equal due to the line parameters of double circuits are same. Hence, by use of KCL law to *B2*, the relationship of inflow currents and outflow currents can be expressed as follows:

$$2I_s + I_{STAT} = I'_S + I''_S \quad (5.\ 34)$$

where

I''_S : phase current of faulted phase through unfaulted single-circuit of *TL2* from *B2* to *B3*

By substitute (5.34) into (5.32), the voltages seen by VT can be expressed as follows:

$$V_L = Z_{L1}(I_s + kI_{s0}) + Z_{L1}(I_{STAT} + kI_{STAT0})$$
$$+pZ'_{Lx}[2I_s + I_{STAT} - I''_S + k'(2I_{s0} + I_{STAT0} - I''_{S0})] + I_f R_f \quad (5.\ 35)$$

By use of delta connection at one side of the coupling transformer of STATCOM, the zero-sequence current injection can be eliminated. Hence the zero-sequence current of STATCOM is eliminated.

$$I_{STAT0} = 0 \quad (5.\ 36)$$

By substitute (5.36) into (5.35), the voltages seen by VT can be expressed as follows:

$$V_L = Z_{L1}(I_s + kI_{s0}) + Z_{L1}I_{STAT}$$

$$+pZ'_{Lx}[2I_s + I_{STAT} - I''_S + k'(2I_{s0} - I''_{S0})] + I_f R_f \quad (5.37)$$

By use of phase voltage measurements at *B1* (V_L) and phase current measurement compensated by zero sequence current (I_L), the apparent impedance seen by Distance relay 1 is given as:

$$Z_{relay1} = \frac{V_L}{I_L}$$

$$= Z_{L1} + Z_{L1}\frac{I_{STAT}}{I_L} + pZ'_{L1}\frac{2I_s - I''_S + k'(2I_{s0} - I''_{S0})}{I_L} + pZ'_{L1}\frac{I_{STAT}}{I_s + kI_{s0}} + \frac{I_f}{I_L}R_f \quad (5.38)$$

$$I_L = I_s + kI_{s0} \quad (5.39)$$

For three-phase faults, the phase current seen by distance relay is as follows:

$$I_L = I_s + kI_{s0} = I_s \quad (5.40)$$

$$I_{s2} = I_{s0} = 0 \quad (5.41)$$

$$I'_{s2} = I'_{s0} = 0 \quad (5.42)$$

Similarly, the apparent impedance seen by the distance relay is given as follows:

$$Z_{relay1} = \frac{V_L}{I_L} = Z_{L1} + Z_{L1}\frac{I_{STAT}}{I_s} + pZ'_{L1}\frac{2I_s - I''_S}{I_s} + pZ'_{L1}\frac{I_{STAT}}{I_s} + \frac{I_f}{I_s}R_f \quad (5.43)$$

By carefully looking into (5.38) and (5.43), the STATCOM's impacts on the apparent impedance measured by distance relay against external fault can be summarised as:

1. The first and third terms ($Z_{L1} + pZ'_{L1}\frac{2I_s - I''_S + k'(2I_{s0} - I''_{S0})}{I_L}$and $Z_{L1} + pZ'_{L1}\frac{2I_s - I''_S}{I_s}$) of (5.38) and (5.43) represent the actual line impedance of *TL1* and proportional line impedance of *TL2* to the fault location. The fifth term ($\frac{I_f}{I_L}R_f$) represents the contribution of fault resistance. These terms (the first, third and fifth) are not affected by compensation of STATCOM.
2. The second and fourth terms ($Z_{L1}\frac{I_{STAT}}{I_L} + pZ'_{L1}\frac{I_{STAT}}{I_s + kI_{s0}}$ and $Z_{L1}\frac{I_{STAT}}{I_s} + pZ'_{L1}\frac{I_{STAT}}{I_s}$) of (5.38) and (5.43) indicates that the STATCOM's impacts on the apparent impedance measured

by Distance relay 1 against external faults lead to greater apparent impedance measurement. The under-reach effect is introduced as the impacts of STATCOM. Since during external fault, the STATCOM is injecting reactive power and current to support bus voltage, the apparent impedance is greater than no STATCOM compensation. For steady state, while STATCOM is absorbing reactive power and current from bus bar, the second and fourth term could be negative. This negative value indicates less apparent impedance of connected *TL1*, which results in overreach effect as impacts of the compensation of STATCOM. This error in apparent impedance measurement caused by STATCOM is related to the current ratio between STATCOM and relay, and fault location.

Another study scenario of investigation of STATCOM's impacts on distance protection against external faults located at *TL2* is also considered, where STATCOM is connected at *B2* instead of *B1* end of *TL1*.

Figure 5- 7 shows the simplified SLD of a faulted network for the analysis of external faults with STATCOM connected at *B2*. Same topology of power network is studied except that the STATCOM is connected at *B2* end of *TL1* instead of *B1*. Same relay and STATCOM settings are applied.

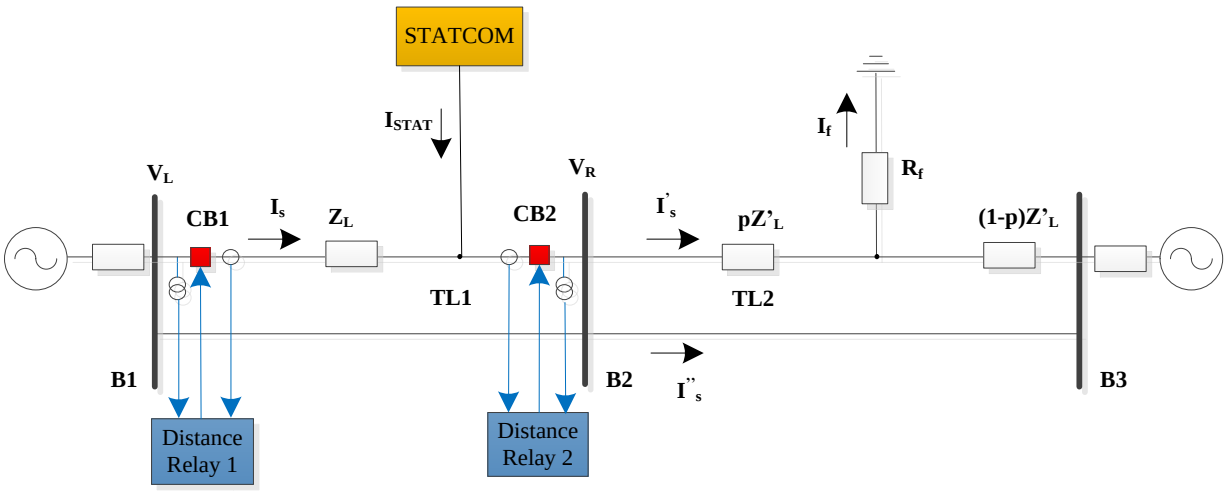


Figure 5- 7 Simplified SLD of test network for external fault.

Similarly, the apparent impedance seen by the Distance relay 1 against SLG faults can be calculated as follows:

$$Z_{relay1} = \frac{V_L}{I_L}$$

$$= Z_{L1} + pZ'_{L1}\frac{2I_s - I''_S + k'(2I_{s0} - I''_{S0})}{I_L} + pZ'_{L1}\frac{I_{STAT}}{I_s + kI_{s0}} + \frac{I_f}{I_L}R_f \quad (5.44)$$

$$I_L = I_s + kI_{s0} \quad (5.45)$$

And the apparent impedance seen by the distance relay against three-phase faults can be calculated as follows:

$$Z_{relay1} = \frac{V_L}{I_L} = Z_{L1} + pZ'_{L1}\frac{2I_s - I''_S}{I_s} + pZ'_{L1}\frac{I_{STAT}}{I_s} + \frac{I_f}{I_s}R_f \quad (5.46)$$

By carefully looking into (5.44) and (5.46), the STATCOM's impacts on apparent impedance measured by Distance relay 1 in case of external fault can be summarised as:

1. The first and second terms ($Z_{L1} + pZ'_{L1}\frac{2I_s - I''_S + k'(2I_{s0} - I''_{S0})}{I_L}$ and $Z_{L1} + pZ'_{L1}\frac{2I_s - I''_S}{I_s}$) of (5.44) and (5.46) represent the actual line impedance of *TL1* and proportional line impedance of *TL2* to the fault location. The fourth term ($\frac{I_f}{I_s}R_f$) represents the contribution of fault resistance. These terms (the first, second and fourth) are not affected by compensation of STATCOM.
2. The third terms ($pZ'_{L1}\frac{I_{STAT}}{I_s + kI_{s0}}$ and $pZ'_{L1}\frac{I_{STAT}}{I_s}$) of (5.44) and (5.46) indicates that the STATCOM's impacts on the apparent impedance measured by Distance relay 1 against external fault lead to greater apparent impedance measurement of distance relay. The under-reach effect is introduced as the impacts of STATCOM. Since during external fault, the STATCOM is injecting reactive power and current to support bus voltage, the apparent impedance is greater than no STATCOM compensation. For steady state, while STATCOM is absorbing reactive power and current from busbar, the third term could be negative. This negative value indicates less apparent impedance, which results in overreach effect as impacts of the compensation of STATCOM. This error in apparent impedance measurement caused by STATCOM is related to the current ratio between STATCOM and relay, and fault location. On the contrary to the STATCOM connected at *B1*, the error in apparent impedance measurement caused by STATCOM connected at *B2* is related to Z'_{L1} rather than Z'_{L1} and Z_{L1}. And the error due to STATCOM connected at *B2* is less than error due to STATCOM connected at *B1*.

5.4 Dynamic Simulation Study

5.4.1 Test System with VSC FACTS and Protection Relay Settings

The schematic diagram of the trial network is illustrated in Figure 5- 8. There is one GE MiCOM P40 Agile P443 distance relay located at each end of two-ended transmission lines from B1 to B2. In this thesis, communications between relays are not considered. Same transmission line parameters and equivalent voltage source parameters are used as those in 4.4 which are listed in Appendix B.1 and B.2. A MMC delta connection STATCOM modelled in 5.2 is connected to *B1* or *B2* to investigate its impacts on distance protection at different locations.

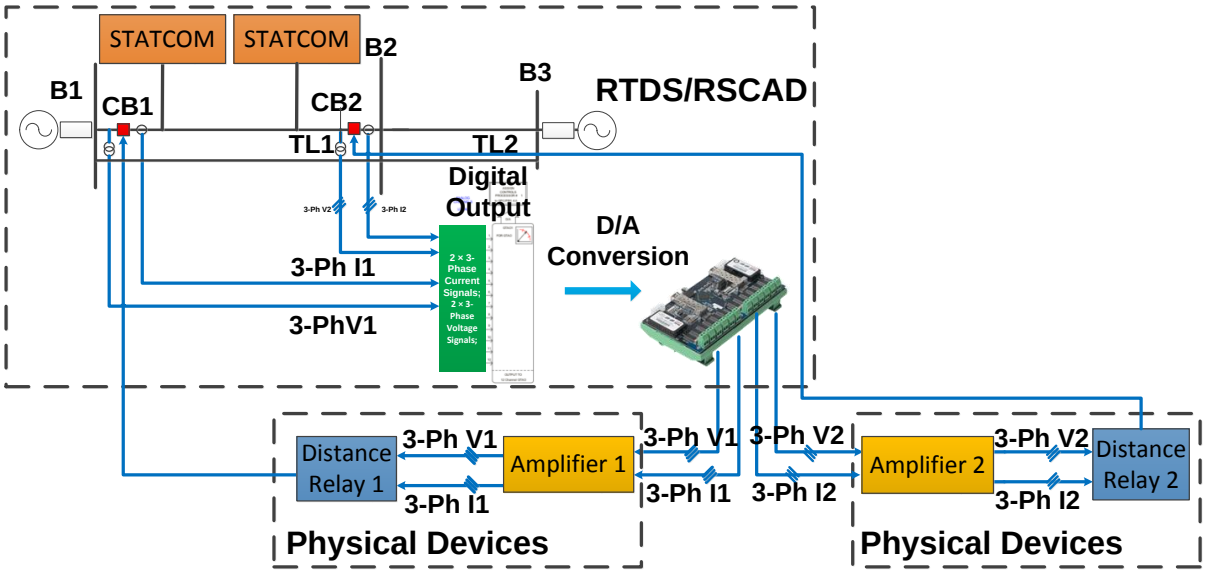


Figure 5- 8 RTDS-base HIL testing platform for STATCOM studies.

Figure 5- 8 shows the same arrangements as applied in Chapter 4 of VTs, CTs and CBs for one of the aforementioned series compensated lines between *B1* and *B2*. Same Distance protection as applied in Chapter 4 using GE MiCOM P40 Agile P443 distance protection relays is used. Two VTs and two CTs at both ends of the transmission line provide voltage and current measurements.

The following considerations are taken into account for the setting of the 2-ended distance protections:

3. Zone 1 is set to 75% of the complete circuit positive sequence impedance. The tripping delay is set to 0ms.

4. Zone 2 is set to reach 150% of the complete circuit positive sequence impedance. The tripping delay is set to 500ms.

5.4.2 Dynamic Simulation Results of Test System against Internal Faults

Internal faults occur at one single-circuit of TL1 from B1 to B2 under such fault conditions:

1. Fault durations are 140ms (7 cycles), or 600ms.
2. Fault locations are 5%, 50% and 85% of the whole length.
3. Fault resistances are 0.01Ω, 1 Ω and 2.5 Ω.
4. SLG, and three-phase to ground faults are considered.

Table 5- 1 shows the simulation results of internal fault. The tripped zone is noted as "I", "II", or "X" for Zone 1, Zone 2 or no relay operation is seen, respectively. Fault type is noted as "RYB-G", or "R-G" for three-phase to ground, or SLG faults, respectively.

Table 5- 1 Simulation results of internal fault

Case	Fault Location	Fault Impedance	Fault Type	Fault Duration	Distance relay 1		Distance relay 2	
					No STAT	STAT	No STAT	STAT
1	15%	0.01Ω	RYB-G	600ms	**I 15.1%**	**I 15.4%**	**II 85.2%**	**II 85.1%**
2	15%	0.01Ω	R-G	600ms	**I 15.3%**	**I 15.8%**	**II 85.4%**	**II 85.4%**
3	15%	1Ω	RYB-G	600ms	**I 15.3%**	**I 15.9%**	**II 85.6%**	**II 85.7%**
4	15%	1Ω	R-G	600ms	**I 15.7%**	**I 16.1%**	**II 85.9%**	**II 85.8%**
5	50%	0.01Ω	RYB-G	140ms	**I 50.1%**	**I 51.1%**	**I 50.1%**	**I 50.1%**
6	50%	0.01Ω	R-G	140ms	**I 50.4%**	**I 51.7%**	**I 50.4%**	**I 50.5%**
7	50%	2.5Ω	RYB-G	140ms	×	×	×	×
8	50%	2.5Ω	R-G	140ms	×	×	×	×
9	85%	0.01Ω	RYB-G	600ms	**II 85.2%**	**II 87.4%**	**I 15.1%**	**I 15.1%**
10	85%	0.01Ω	R-G	600ms	**II 85.5%**	**II 87.9%**	**I 15.3%**	**I 15.3%**

11	85%	1Ω	RYB-G	140ms	×	×	×	×
12	85%	1Ω	R-G	140ms	×	×	×	×

Figure 5- 9 and Figure 5- 10 show digital signals from RSCAD and the trajectory of impedance measurement by Distance relay 1 and Distance relay 2 respectively against a typical internal fault Case 1 of Table 5- 1 with no STATCOM. Figure 5- 11 and Figure 5- 12 show digital signals from RSCAD and the trajectory of impedance measurement by Distance relay 1 and Distance relay 2 respectively against a typical internal fault Case 1 of Table 5- 1 with STATCOM.

As shown in Figure 5- 11, VT and CT send voltage and current measurements (noted as V1A/V1B/V1C and I1A/I1B/I1C) to Distance relay 1. By use of the received measurements and impedance calculation algorithm presented in 5.3, the apparent impedance is calculated (noted as ZIM1 vs ZRE1). The trip signals (noted as Trip1A/Trip1B/Trip1C) are sent to corresponding CBs with no delay time, by judgement if calculated apparent impedance is within the protection zones. The CBs are turn off or turn on (noted as CB1A/CB1B/CB1C in Figure 5- 11), controlled by received trip signals. As for Distance relay 2 as shown in Figure 5- 12, the trip signals (noted as Trip2A/Trip2B/Trip2C) are sent to corresponding CBs with a delay time of 500ms to meet distance relay settings for Zone 2 protection.

By comparison of the apparent impedances measured by Distance relay 1, the apparent impedance with STATCOM is greater than impedance with no STATCOM. The under-reach effect is seen due to the incorporation of STATCOM. For impedance measurements of Distance relay 2, there is no significant difference of impedance measurement with/without STATCOM. These results are in line with conclusions in 5.3.1.

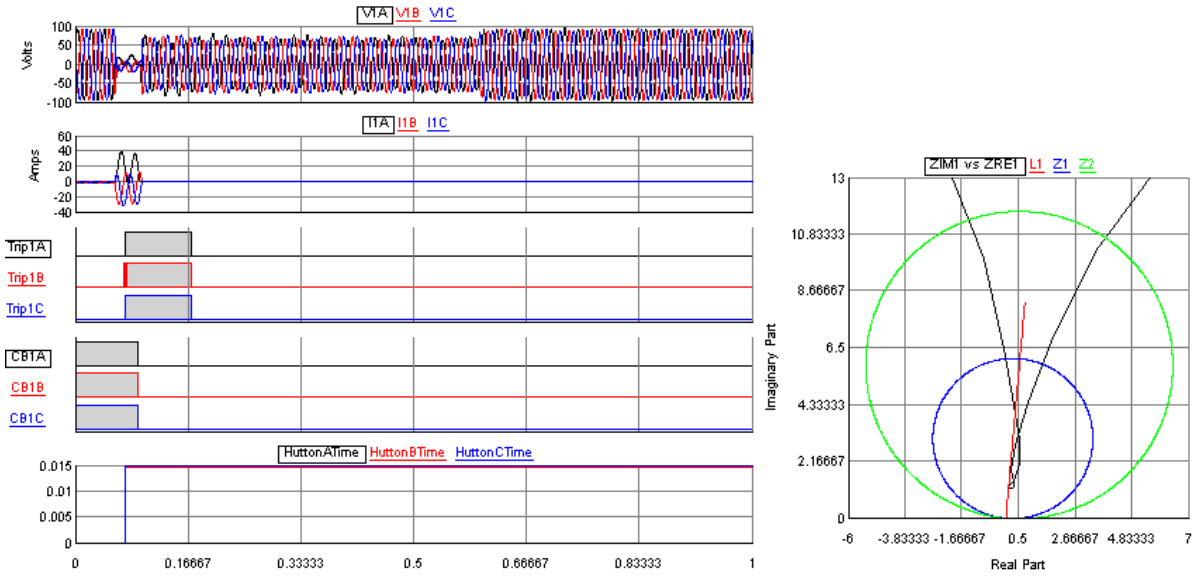


Figure 5- 9 Digital signals from RSCAD and trajectory of impedance measurement by Distance relay 1 against internal fault Case 1 without STATCOM.

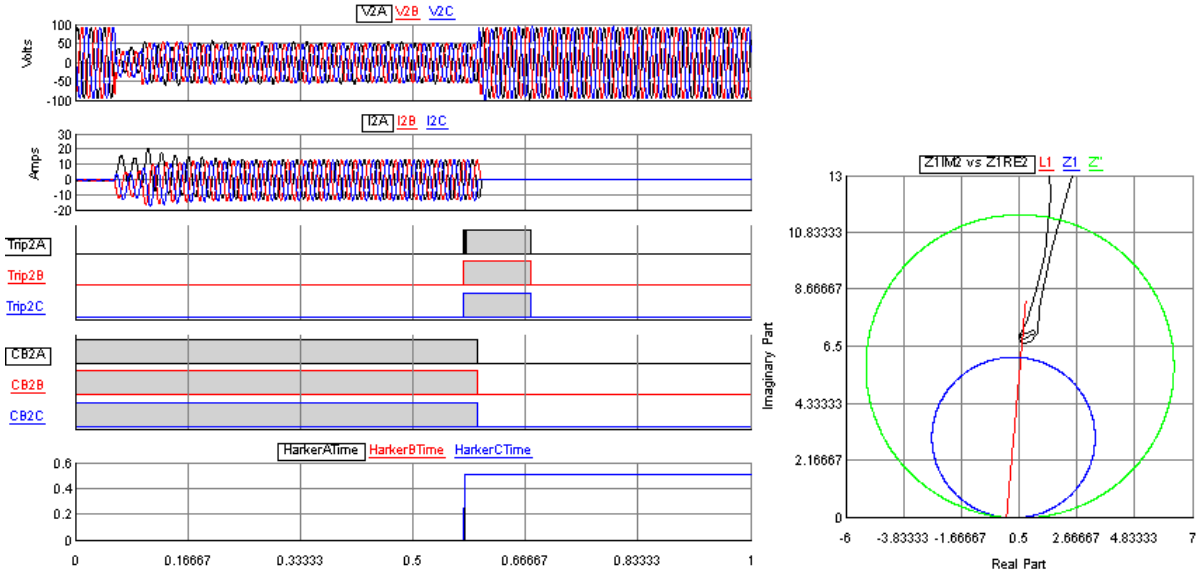


Figure 5- 10 Digital signals from RSCAD and trajectory of impedance measurement by Distance relay 2 against internal fault Case 1 without STATCOM.

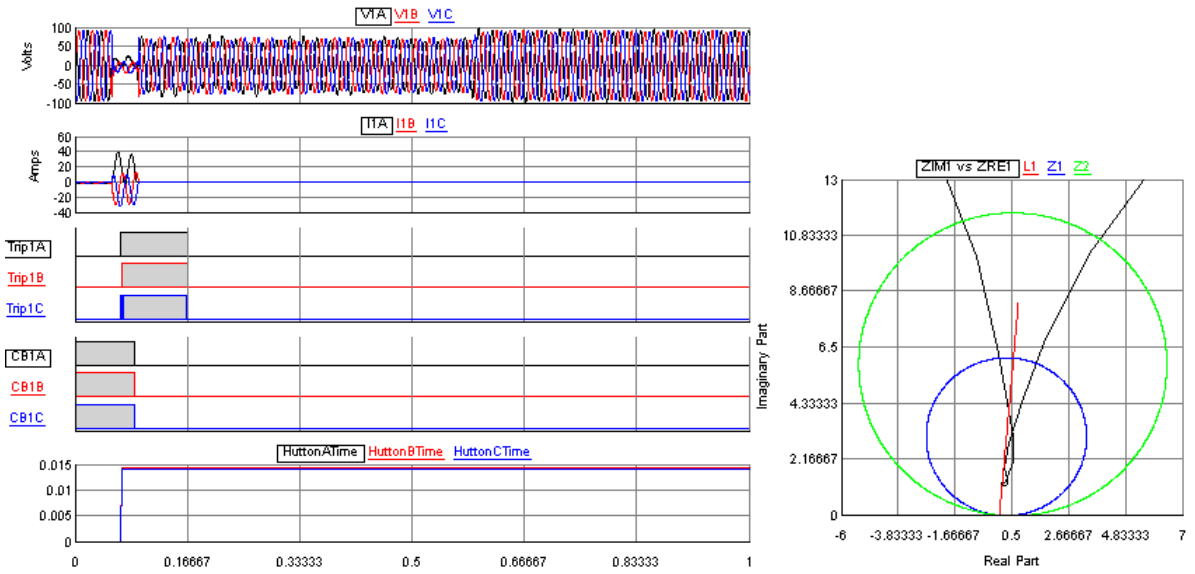


Figure 5- 11 Digital signals from RSCAD and trajectory of impedance measurement by Distance relay 1 against internal fault Case 1 with STATCOM.

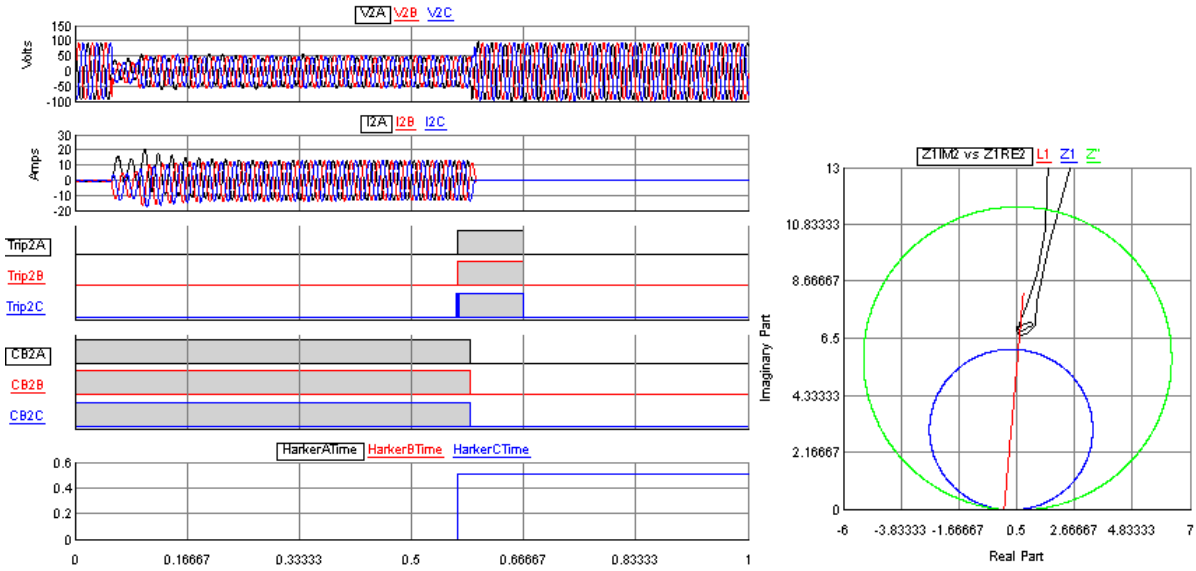


Figure 5- 12 Digital signals from RSCAD and trajectory of impedance measurement by Distance relay 2 against internal fault Case 1 with STATCOM.

Figure 5- 13 and Figure 5- 14 show digital signals from RSCAD of Distance relay 1 and Distance relay 2 respectively against a SLG external fault Case 2 of Table 5- 1 with STATCOM. As voltage and current measurements of VT and CT (noted as V1A/V1B/V1C and I1A/I1B/I1C) shown in Figure 5- 13, SLG fault occurred. The trip signal of faulted phase A (noted as Trip1A) is sent from Distance relay 1 to corresponding CB. The three-phase trip signals (noted as Trip2A/Trip2B/Trip2C in Figure 5- 14) are sent from Distance relay 2 to corresponding CBs. This is due to the fact that distance relay settings require relay trips all three phase for Zone 2 protection.

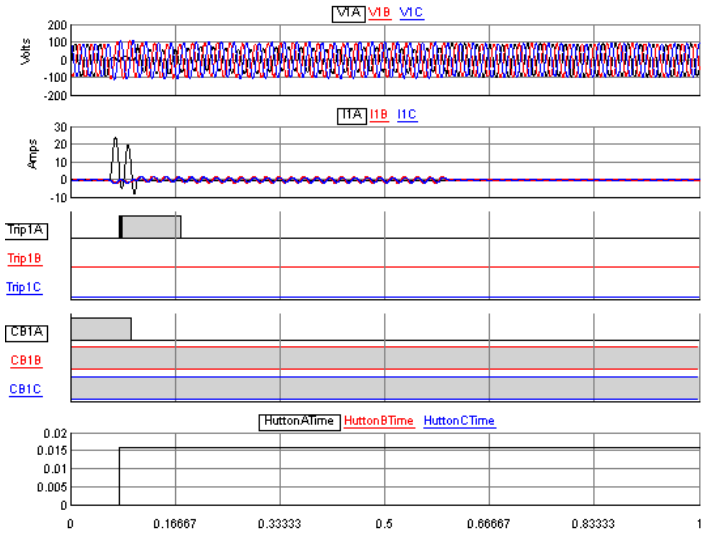


Figure 5- 13 Digital signals from RSCAD by Distance relay 1 against internal fault Case 2 with STATCOM.

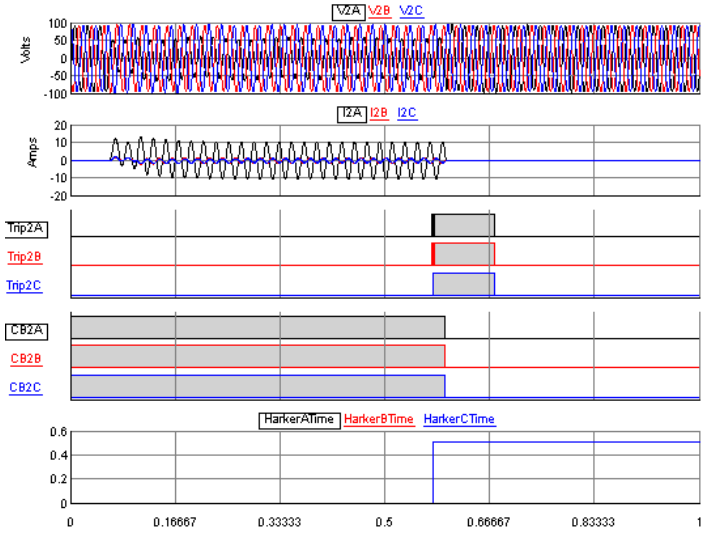


Figure 5- 14 Digital signals from RSCAD by Distance relay 2 against internal fault Case 2 with STATCOM.

Figure 5- 15 and Figure 5- 16 show digital signals from RSCAD and the trajectory of impedance measurement by Distance relay 1 and Distance relay 2 respectively against a 50%, 140ms internal fault Case 5 of Table 5- 1 with STATCOM. By comparison of the apparent impedances measured by distance relay, the apparent impedance against 50% fault is greater than impedance against 15% fault. These results are in line with the conclusion in 5.3 that the error of measured impedance is positively related to fault distance.

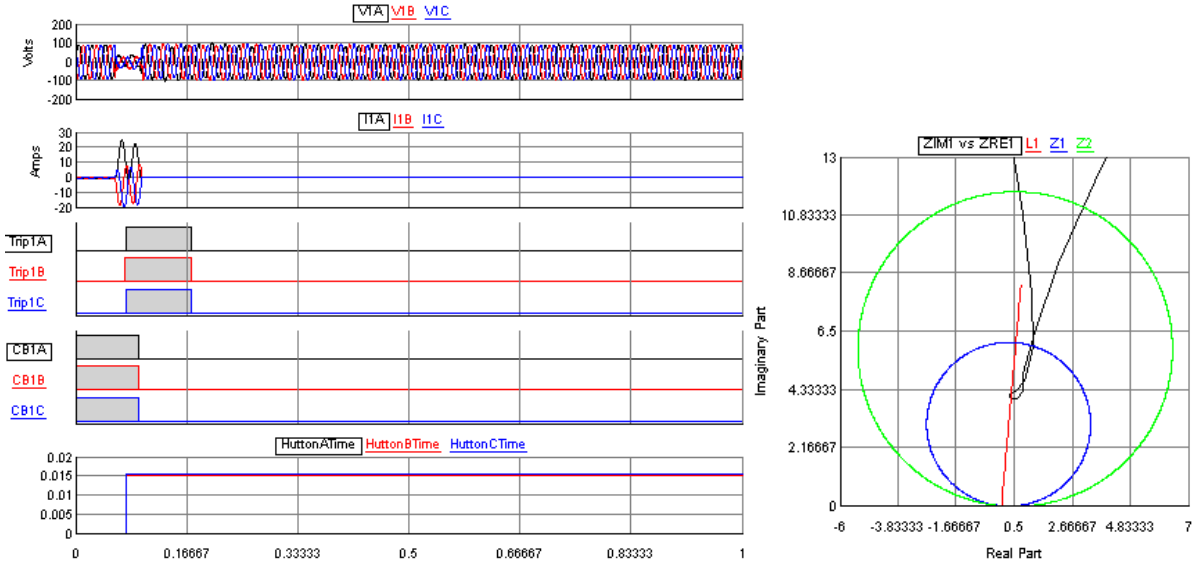


Figure 5- 15 Digital signals from RSCAD and trajectory of impedance measurement by Distance relay 1 against internal fault Case 5 with STATCOM.

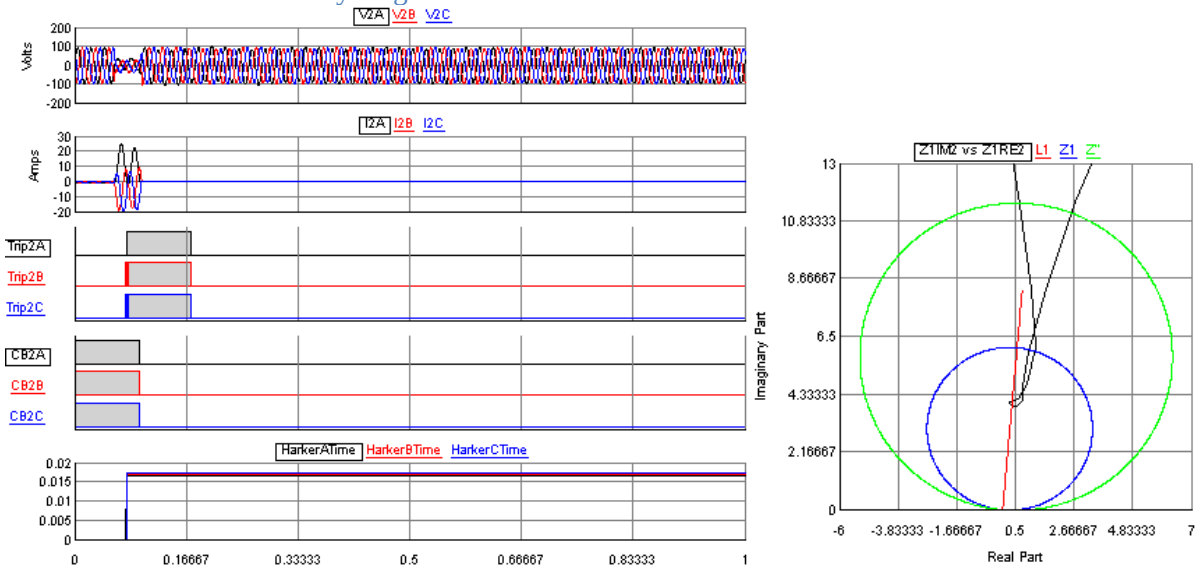


Figure 5- 16 Digital signals from RSCAD and trajectory of impedance measurement by Distance relay 2 against internal fault Case 5 with STATCOM.

Figure 5- 17 and Figure 5- 18 show digital signals from RSCAD and the trajectory of impedance measurement by Distance relay 1 and Distance relay 2 respectively against a 2.5 Ω internal fault Case 7 of Table 5- 1 with STATCOM. It can be seen from Figure 5- 17 that the distance relay is not tripped if the fault distance is without reach of Zone 1 (and the fault duration is shorter than trip delay of Zone 2 protection, hence Zone 2 protection also restraints). By comparison of the apparent impedances measured by distance relay, the apparent impedance against 2.5 Ω fault is greater than impedance against 0.01 Ω. These

results are in line with the conclusion in 5.3 that the error of measured impedance is positively related to fault resistance.

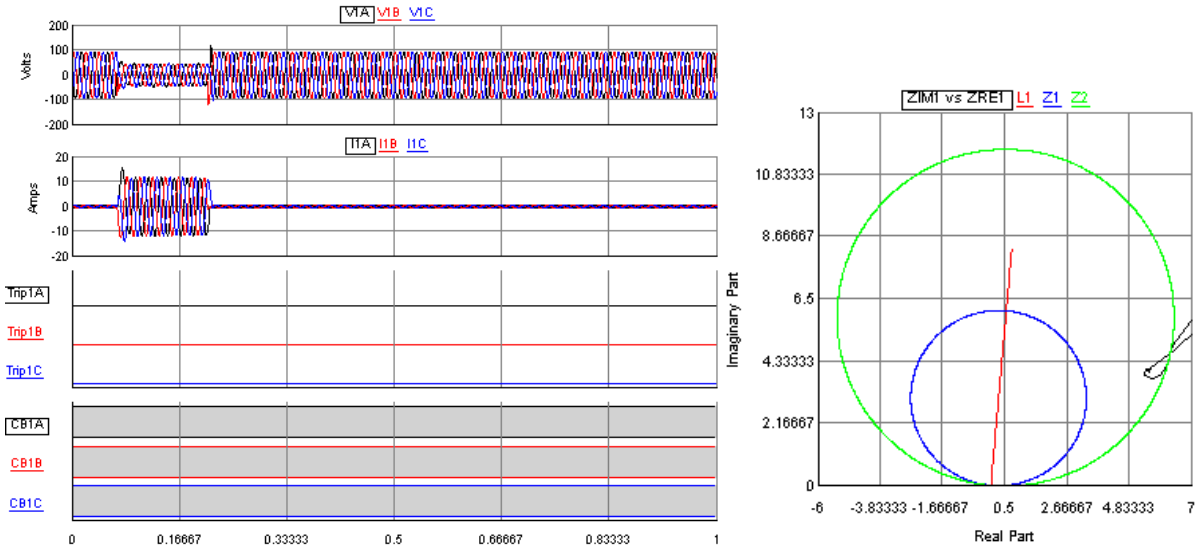


Figure 5- 17 Digital signals from RSCAD and trajectory of impedance measurement by Distance relay 1 against internal fault Case 7 with STATCOM.

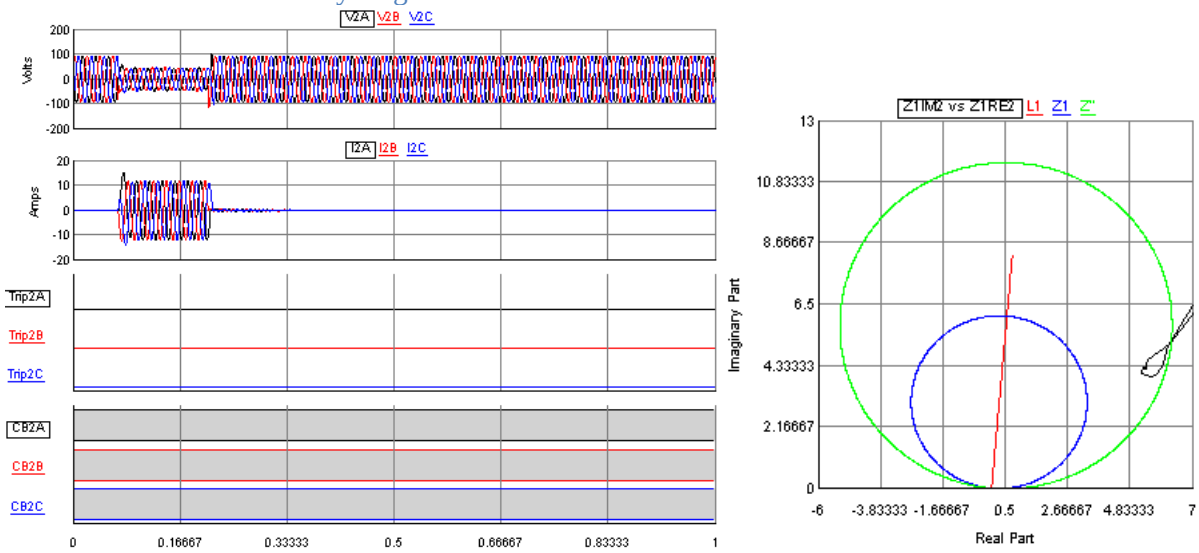


Figure 5- 18 Digital signals from RSCAD and trajectory of impedance measurement by Distance relay 2 against internal fault Case 7 with STATCOM.

5.4.3 Dynamic Simulation Results of Test System against External Faults

External faults occur at one single-circuit of *TL2* from *B2* to *B3* under such fault conditions:

1. 600ms fault occurred at 105% and 135% of the equivalent whole length of TL1.
2. Fault resistance is 0.01Ω, and 1 Ω.
3. SLG and three-phase to ground faults are considered.

Table 5- 2 shows the simulation results of external fault. The tripped zone is noted as “I”, “II”, or “X” for Zone 1, Zone 2 or no relay operation is seen, respectively. Fault type is noted as “RYB-G”, or “R-G” for three-phase to ground, or SLG faults, respectively. Different locations of STATCOM are noted as “STATB1” or “STATB2” for connection to *B1* or *B2*.

Table 5- 2 Simulation results of external fault

Case	Fault Location	Fault Impedance	Fault Type	Fault Duration	Distance relay 1		
					No STAT	STATB1	STATB2
1	105%	0.01Ω	RYB-G	600ms	**II 105.5 %**	**II 106.7%**	**II 106.3%**
2	105%	0.01Ω	R-G	600ms	**II 106.0 %**	**II 107.3%**	**II 106.9%**
3	105%	1Ω	RYB-G	600ms	**II 106.1 %**	**II 107.4%**	**II 106.9%**
4	105%	1Ω	R-G	600ms	**II 106.6 %**	**II 107.9%**	**II 107.4%**
5	135%	0.01Ω	RYB-G	600ms	**II 136.4 %**	**II 139.7%**	**II 138.3%**
6	135%	0.01Ω	R-G	600ms	×	×	×
7	135%	1Ω	RYB-G	600ms	×	×	×
8	135%	1Ω	R-G	600ms	×	×	×

Figure 5- 19 shows digital signals from RSCAD against a typical external fault Case 1 of Table 5- 2 with no STATCOM, and the trajectory of impedance measurement by distance relay. Figure 5- 20 shows digital signals from RSCAD against same external fault with STATCOM connected to *B1*, and the corresponding trajectory of impedance measurement by distance relay. Figure 5- 21 shows digital signals from RSCAD against same external fault with STATCOM connected to *B2*, and the corresponding trajectory of impedance measurement by distance relay.

As shown in Figure 5- 20, VT and CT send voltage and current measurements (noted as VA/VB/VC and IA/IB/IC) to distance relay. By use of the received measurements and impedance calculation algorithm presented in 5.3, the apparent impedance is calculated (noted as ZIM vs ZRE). The trip signals (noted as TripA/TripB/TripC) are sent to corresponding CBs, by judgement if calculated apparent impedance is within protection zones. The CBs are turn off or turn on (noted as CBA/CBB/CBC), controlled by received trip signals.

By comparison of the apparent impedances measured by distance relay, the apparent impedance with STATCOM is greater than impedance with no STATCOM. The under-reach effect of distance relay is seen due to the incorporation of STATCOM. The relationship of the measured impedances of different location of STATCOM can be expressed as follows:

$$Z_{noSTAT} < Z_{STATB2} < Z_{STATB1} \tag{5. 47}$$

where

Z_{noSTAT}, Z_{STATB1}, and Z_{STATB2}: measured impedance by distance relay with no STATCOM, STATCOM connected to *B1*, and STATCOM connected to *B2*

The relationship of measured impedances of different location of STATCOM is in line with the conclusions in 5.3.2.

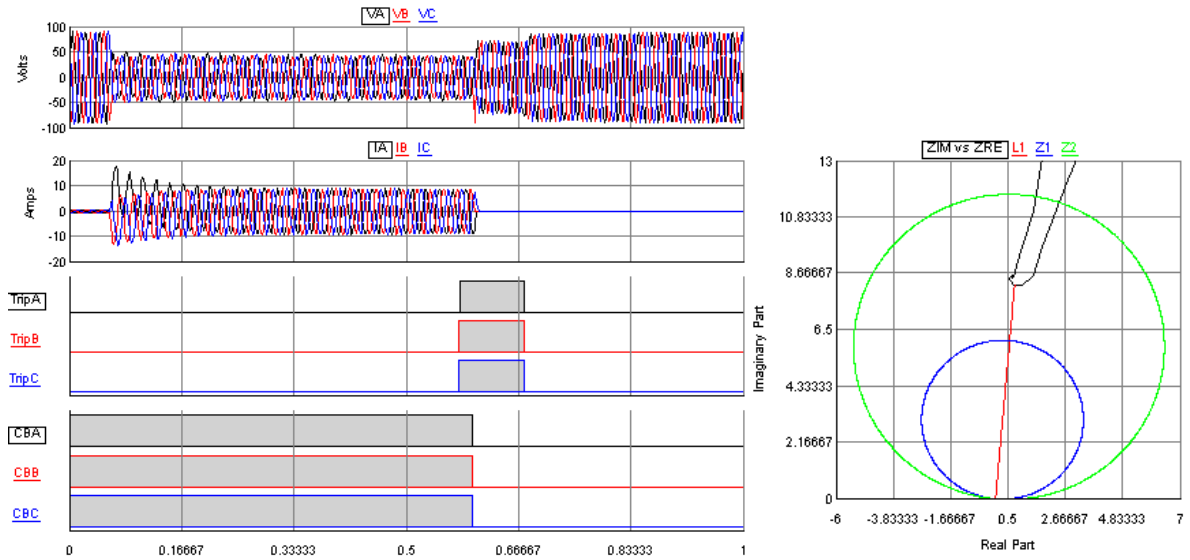


Figure 5- 19 Digital signals from RSCAD against external fault Case 1 with no STATCOM.

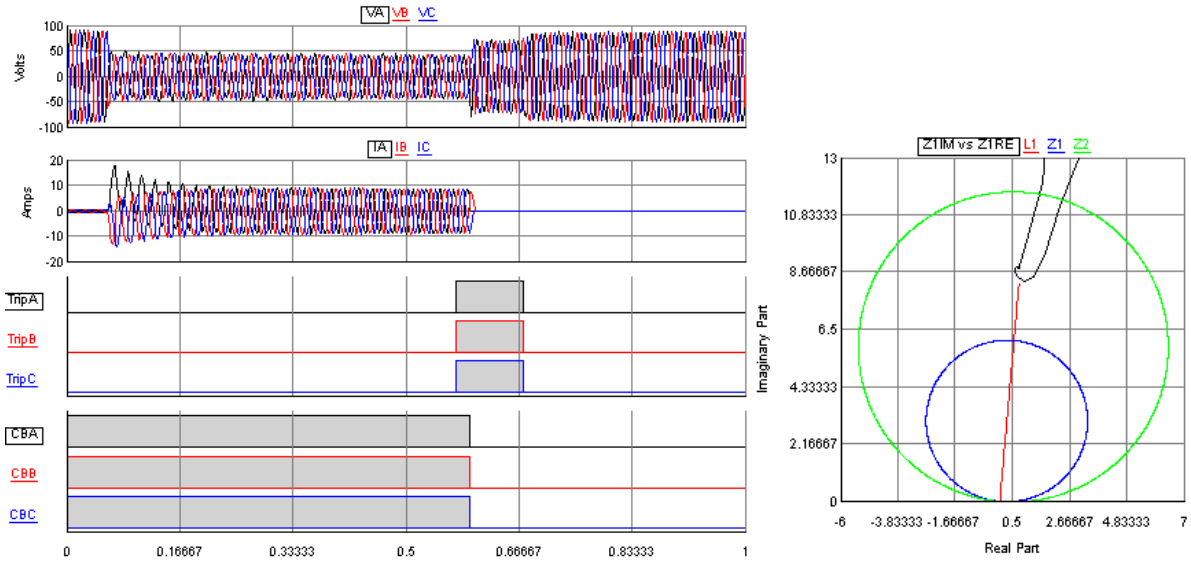


Figure 5- 20 Digital signals from RSCAD against external fault Case 1 with STATCOM at B1.

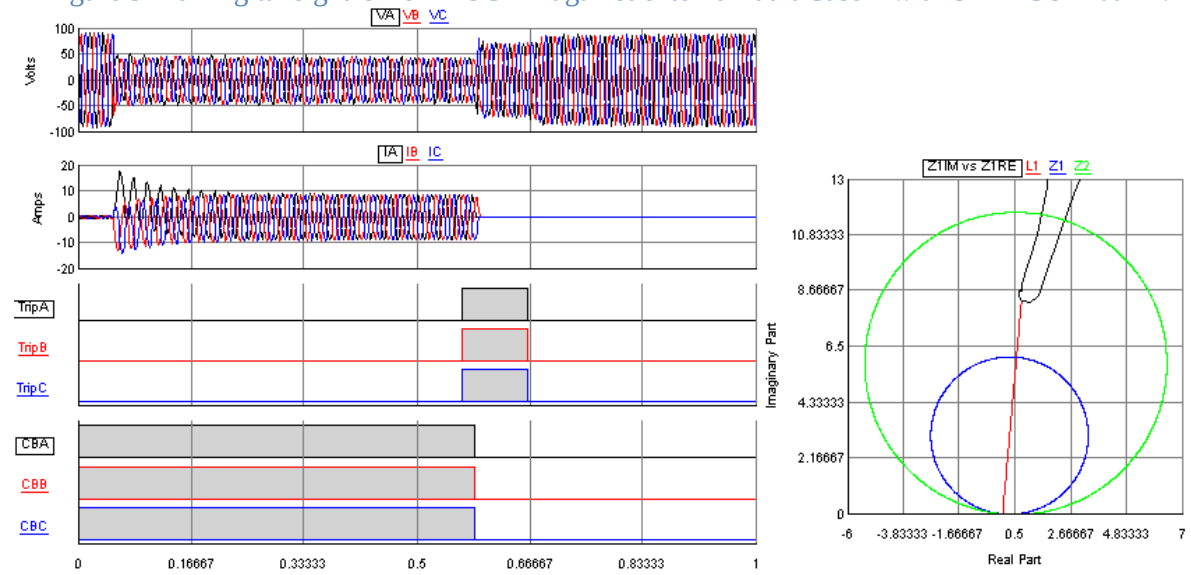


Figure 5- 21 Digital signals from RSCAD against external fault Case 1 with STATCOM at B2.

Figure 5- 22 shows the digital signals from RSCAD against a SLG external fault Case 2 of Table 5- 2 with STATCOM connected to *B1*. As voltage and current measurements of VT and CT (noted as VA/VB/VC and IA/IB/IC) shown in Figure 5- 22, SLG fault occurred. The three-phase trip signals (noted as TripA/TripB/TripC) are sent to corresponding CBs. This is due to the fact that distance relay settings require relays trip all three phase for Zone 2 protection.

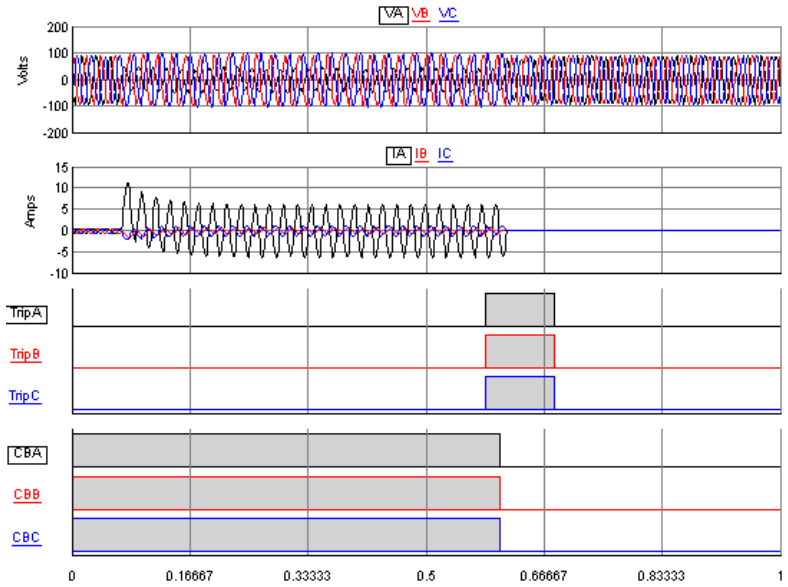


Figure 5- 22 Digital signals from RSCAD against external fault Case 2 with STATCOM at B1.

Figure 5- 23 shows digital signals from RSCAD against a 1 Ω external fault Case 3 of Table 5- 2 with STATCOM at *B1*, and the trajectory of impedance measurement by distance relay. By comparison of the apparent impedances measured by distance relay, the apparent impedance against 1 Ω fault is greater than impedance against 0.01 Ω. These results are in line with the conclusion in 5.3 that the error of measured impedance is positively related to fault resistance.

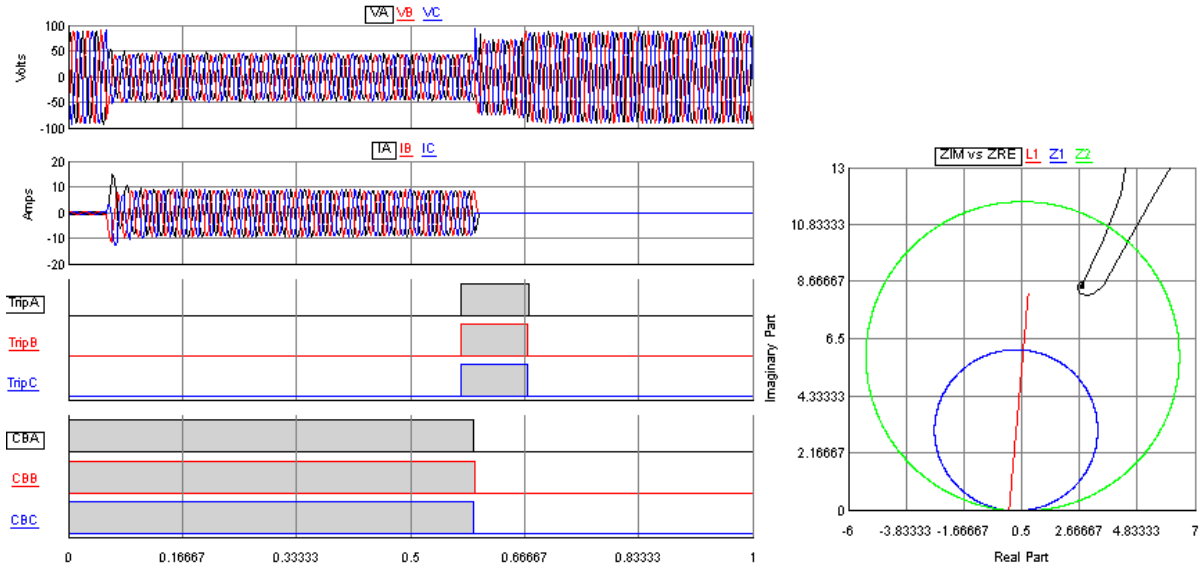


Figure 5- 23 Digital signals from RSCAD for a 1 Ω external fault Case 3 of Table 5- 2 with STATCOM at B1.

Figure 5- 24 shows the digital signals from RSCAD against a 135% external fault Case 7 of Table 5- 2 with STATCOM at *B1*, and the trajectory of impedance measurement by distance relay. It can be seen from Figure 5- 24 that the distance relay is not tripped if the fault distance is too far. By comparison of the apparent impedances measured by distance relay, the apparent impedance against 135% fault is greater than impedance against 105% fault. These results are in line with the conclusion in 5.3 that the error of measured impedance is positively related to fault distance.

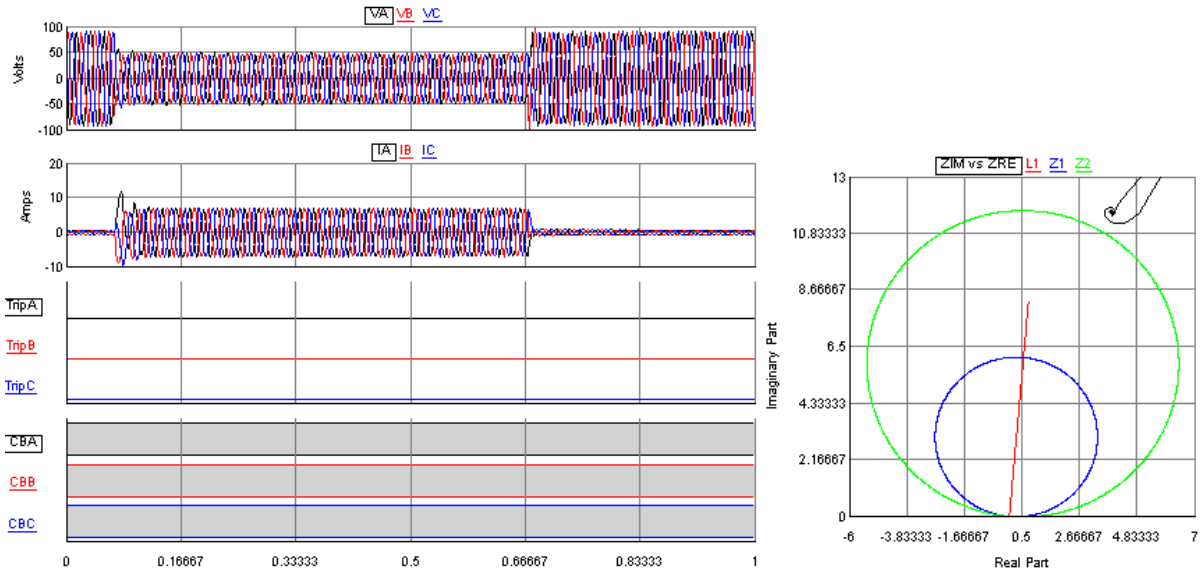


Figure 5- 24 Digital signals from RSCAD for a 135% external fault Case 7 of Table 5- 2 with STATCOM at B1.

5.5 Summary

In this chapter, dynamic representation of STATCOM has been modelled considering configuration and control system. Mathematical representations of the apparent impedance measurements of neighbouring and remote distance relays against internal and external faults have been derived considering infeed currents from STATCOM connected to different busbars. For derived mathematical representation of apparent impedance measurement of neighbouring distance relay against internal faults, some part (the first term) is not affected by the compensation of STATCOM while the other part (the second term and third) indicates that the STATCOM's impacts on the apparent impedance measured by neighbouring distance relay against internal faults lead to greater apparent impedance measurement. The under-reach effect is introduced as the impacts of STATCOM. Since during internal fault, the STATCOM is injecting reactive power and current to support bus voltage, the apparent

impedance with STATCOM is greater than that without STATCOM. For steady state, while STATCOM is absorbing reactive power and current from bus bar, the second term could be negative. This negative value indicates smaller apparent impedance measured by distance relays which results in overreach effect. This error in apparent impedance measurements caused by STATCOM is proportional to the fault location and the current ratio between STATCOM and relay.

As for the derived mathematical representation of the apparent impedance measurements of remote distance relay against internal faults, some part (the first term) is not affected by the compensation of STATCOM while the other part (the second term) indicates greater apparent impedance measured by remote distance relay as STATCOM's impacts. On the contrary to the neighbouring relay, the remote relay is only affected by the amount of current injection of STATCOM. The location of fault has no effects on the error in measured impedance by remote relay. This issue can be explained by the fact that the STATCOM is located beyond the fault location seen from the remote relay. A greater amount of current injection of STATCOM would lead to a greater apparent impedance error and cause more significant under-reach effect.

As for the derived mathematical representation of the apparent impedance measurement of distance relay against external faults with STATCOM located at *B1*, some part (the first and third terms) are not affected by the compensation of STATCOM while the other part (second and fourth terms) indicates that the STATCOM's impacts on the apparent impedance measured by distance relay against external faults lead to greater apparent impedance measurement. The under-reach effect is introduced as the impact of STATCOM. This error in the apparent impedance measurement caused by STATCOM is related to the current ratio between STATCOM and relay, and fault location.

As for the derived mathematical representation of the apparent impedance measurement of distance relay against external faults with STATCOM located at *B2*, some part (the first, second and fourth terms) are not affected by the compensation of STATCOM while the other part (the third term) indicates that the STATCOM's impacts on apparent impedance measured by Distance relay 1 against external fault lead to greater apparent impedance measurement. The under-reach effect is introduced as the impacts of STATCOM. On the contrary to the STATCOM connected at B1, the error in apparent impedance measurement

caused by STATCOM connected at *B2* is related to Z'_{L1} rather than $Z'_{L1}$and Z_{L1}. And the error due to STATCOM connected at *B2* is less than error due to STATCOM connected at *B1*.

As shown in dynamic simulation results in RTDS/RSCAD, the apparent impedance against internal faults with STATCOM is greater than impedance with no STATCOM, by comparison of the apparent impedances measured by distance relay. The under-reach effect of distance relay is seen due to the incorporation of STATCOM. For impedance measurements of remote distance relay, there is no significant difference of impedance measurement with/without STATCOM. The dynamic simulation results are in line with the mathematical analysis presented in 5.3, considering that results that the error of measured impedance is positively related to fault resistance, and fault distance.

For dynamic simulation results against external faults, the apparent impedance with STATCOM is greater than impedance with no STATCOM, by comparison of the apparent impedances measured by distance relay. The under-reach effect of distance relay is seen due to the incorporation of STATCOM. The relationship of measured impedances of different locations of STATCOM can be expressed as follows:

$$Z_{noSTAT} < Z_{STATB2} < Z_{STATB1}$$

The dynamic simulation results are in line with the mathematical analysis presented in 5.3, considering the results that the error of measured impedance is positively related to fault resistance, and fault distance.

CHAPTER 6 COMBINED IMPACTS OF VSC HVDC AND VSC FACTS ON DISTANCE PROTECTION

6.1 Introduction

This chapter presents the mathematical representation of the apparent impedance measurement of distance relay considering the infeed current from VSC HVDC and shunt VSC FACTS at different locations. Relevant analysis of the apparent impedance measurement representation and dynamic simulation study is performed to investigate the impacts of VSC HVDC and VSC FACTS (in particular, STATCOM as a typical example) on distance protection. In 6.2, mathematical representations of the apparent impedance measurement of distance relay against external faults are derived considering infeed currents from VSC HVDC and STATCOM connected to different buses, VSC HVDC and STATCOM connected to same bus, and VSC HVDC and multiple STATCOM. A RTDS-based HIL testing platform is established to perform dynamic simulation studies of test system with VSC HVDC and VSC FATCTS. The dynamic simulation results are analysed in comparison between test system with VSC HVDC and STATCOM at different locations against external faults.

6.2 Impacts of VSC HVDC and VSC FACTS on Distance Protection

The VSC HVDC and VSC FACTS are integrated simultaneously to a regional power system network. The impacts of the incorporation of these VSC converter based systems on distance protection are studied for two-ended double-circuit transmission lines. In this section, the mathematical analysis of the impacts of VSC HVDC and VSC FACTS on the apparent impedance measured by feeder distance protection relay is presented in aspects of VSC HVDC and VSC FACTS connected to same bus, different buses, and VSC HVDC and multiple VSC FACTS installed.

6.2.1 VSC HVDC and VSC FACTS Connected to Different Buses

Figure 6- 1 shows the simplified single line diagram of a faulted network for the analysis of impacts of VSC HVDC and VSC FACTS connected simultaneously to different buses on

distance protection of two-ended double-circuit transmission lines. With same topology of transmission system studied as presented in 4.3, two AC systems (represented by ideal voltage source with internal impedance) are connected via double-circuit transmission lines *TL1* and *TL2*. The line parameters for the double circuits of same transmission line are same. A VSC converter of VSC HVDC system is connected near *B2* (the distance between VSC converter and *B2* can be neglected) to provide voltage support and active power transmission. One STATCOM is connected near *B1* (the distance between STATCOM and *B1* can be neglected) to provide voltage regulation support or reactive power compensation. Two distance relays (Distance relay 1 and Distance relay 2) are located at the both ends of one single-circuit of *TL1*. These distance relays collect voltage and current measurements from VT/CT and send trip signals to circuit breakers (CB1 and CB2). An external SLG fault or three-phase fault on *TL2* is occurs at *p*% of the full length of *TL2* from *B2*.

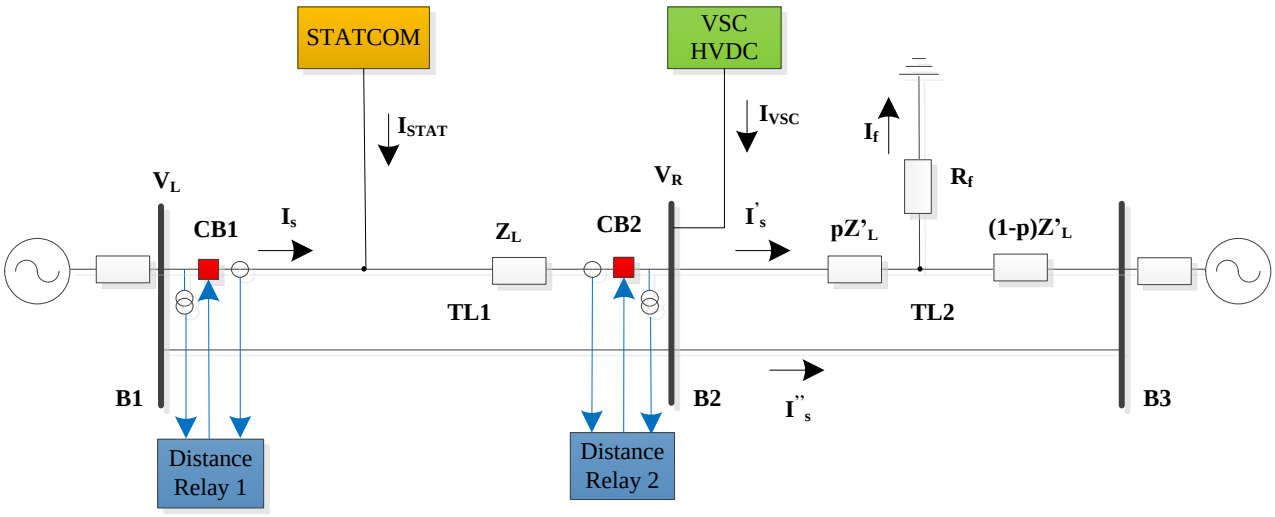


Figure 6- 1 Simplified single line diagram of a faulted network for the analysis of impact of VSC HVDC and VSC FACTS connected to different buses.

The distance protection used on *TL1* applies the normal protection scheme that is presented in 4.2. Two distance relays, distance relay 1 and distance relay 2 are set to use Zone 1 and Zone 2 protection. The relay setting for Zone 1 protection is 75% of the line impedance. The relay setting for Zone 2 protection is 150% of the line impedance so that the full protection range of Zone 1 and Zone 2 protection of a distance relay covers the full length of transmission line. Plain impedance characteristic of distance relay is considered in this study.

The VSC converter connected at *B2* is modelled as that presented in Chapter 2. The control mode of VSC HVDC control system can be set to DC voltage regulation or active power

transfer control for *d* axis, and AC voltage regulation or reactive power control for q axis. The impacts of VSC HVDC are studied mainly on Zone 2 protection, due to the same reason of protection range that has been described in 4.3.

The STATCOM connected at *B1* is modelled as that presented in Chapter 5. The control mode of STATCOM control system can be set to AC voltage regulation or reactive power control. The impacts of VSC FACTS on distance protection are on both Zone 1 protection and Zone 2 protection as presented in Chapter 5. The impacts of VSC HVDC and VSC FACTS connected simultaneously to different buses on Zone 1 protection are the same with the impacts of VSC FACTS alone that has been studied in Chapter 5, since VSC HVDC has no significant impacts on Zone 1 protection as studied in Chapter 4. The impacts of VSC HVDC and VSC FACTS connected to different buses on Zone 2 protection are studied since they both have significant impacts on Zone 2 protection. Hence the distance protection against external fault located at *TL2* is selected as research scenario to investigate the impacts of the incorporation of VSC HVDC and VSC FACTS.

The apparent impedance of VSC HVDC and VSC FACTS connected transmission line measured by distance relays are derived for SLG faults and three-phase faults to investigate their impacts.

For SLG faults, the voltages seen by VT at *B1* can be expressed as follows:

$$V_{Lx} = Z_{Lx}(I_{sx} + I_{STATx}) + pZ'_{Lx}I'_{sx} + I_{fx}R_f \qquad (6.\ 1)$$

for $x = 1,2, or\ 0$ as a suffix denote of the sequence components, where

V_{Lx} : sequence phase voltages seen by VT at *B1*

I_{sx} : sequence phase currents seen by CT at *B1*

I'_{sx} : sequence phase current through faulted single-circuit of *TL2* from *B2* to *B3*

I_{STATx}: sequence phase currents infeed from STATCOM

I_{fx} : sequence current through fault resistance

R_f : fault resistance

$Z_{Lx}$and Z'_{Lx} : sequence components of the line impedance of *TL1* and *TL2*

p : fault location from *B2* to *B3* in per unit of the total line length

The line positive and negative sequence impedances are assumed equal.

$$Z_{L1} = Z_{L2}, Z'_{L1} = Z'_{L2} \tag{6. 2}$$

By adding all three sequence components of left-hand side of (6.1) and substitute (6.2) into (6.1), the voltage seen by VT can be expressed after simplification as follows:

$$V_L = Z_{L1}(I_s + kI_{s0}) + Z_{L1}(I_{STAT} + kI_{STAT0}) + pZ'_{Lx}(I'_s + k'I'_{s0}) + I_f R_f \tag{6. 3}$$

where

$V_L$and I_s : phase voltage and current of faulted phase through *TL1*

I_{STAT}: phase current of faulted phase infeed from STATCOM

I'_s : phase current of faulted phase through faulted single-circuit of *TL2* from *B2* to *B3*

I_f : fault current through fault resistance

k : zero sequence current compensation factors of *TL1*

k' : zero sequence current compensation factors of *TL2*

$$k = \frac{Z_{L0} - Z_{L1}}{Z_{L1}} \tag{6. 4}$$

$$k' = \frac{Z'_{L0} - Z'_{L1}}{Z'_{L1}} \tag{6. 5}$$

For transient response study of double-circuit transmission line, the fault currents through the double circuits of *TL1* can be assumed to be equal due to the line parameters of double circuits are same. Hence, by use of KCL law to *B2*, the relationship of inflow currents and outflow currents can be expressed as follows:

$$2I_s + I_{VSC} + I_{STAT} = I'_S + I''_S \tag{6. 6}$$

where

I_{VSC} : phase current infeed from VSC HVDC

I''_S : phase current of faulted phase through unfaulted single-circuit of *TL2* from *B2* to *B3*

By substitute (6.6) into (6.3), the voltage seen by VT can be expressed as follows:

$$V_L = Z_{L1}(I_s + kI_{s0}) + Z_{L1}(I_{STAT} + kI_{STAT0}) + pZ'_{Lx}[2I_s + I_{VSC} + I_{STAT} - I''_S + k'(2I_{s0} + I_{VSC0} + I_{STAT0} - I''_{S0})](I'_s + k'I'_{s0}) + I_f R_f \quad (6.7)$$

By use of delta connection at one side of the coupling transformer of VSC HVDC and STATCOM, the zero-sequence current injection can be eliminated. Hence the zero-sequence currents are eliminated.

$$I_{VSC0} = 0 \quad (6.8)$$

$$I_{STAT0} = 0 \quad (6.9)$$

By substitute (6.8) and (6.9) into (6.7), the voltage seen by VT can be expressed as follows:

$$V_L = Z_{L1}(I_s + I_{STAT} + kI_{s0}) + pZ'_{Lx}[2I_s + I_{VSC} + I_{STAT} - I''_S + k'(2I_{s0} - I''_{S0})] + I_f R_f \quad (6.10)$$

By use of phase voltage measurements at *B1* (V_L) and phase current measurement compensated by zero sequence current (I_L), the apparent impedance seen by the distance relay 1 are given as:

$$Z_{relay1} = \frac{V_L}{I_L} = Z_{L1}\left(1 + \frac{I_{STAT}}{I_s + kI_{s0}}\right) + pZ'_{L1}\frac{2I_s + I_{VSC} + I_{STAT} - I''_S + k'(2I_{s0} - I''_{S0})}{I_s + kI_{s0}} + \frac{I_f}{I_L}R_f$$

$$= Z_{L1} + Z_{L1}\frac{I_{STAT}}{I_s + kI_{s0}} + pZ'_{L1}\frac{2I_s - I''_S + k'(2I_{s0} - I''_{S0})}{I_s + kI_{s0}} + pZ'_{L1}\frac{I_{VSC} + I_{STAT}}{I_s + kI_{s0}} + \frac{I_f}{I_L}R_f \quad (6.11)$$

$$I_L = I_s + kI_{s0} \quad (6.12)$$

where

Z_{relay1} : apparent impedance measured distance relay 1

I_L : compensated phase current of faulted phase measure by distance relay 1

For three-phase faults, the phase current seen by distance relay is as follows:

$$I_L = I_s + kI_{s0} = I_s \quad (6.13)$$

$$I_{s2} = I_{s0} = 0 \quad (6.14)$$

$$I'_{s2} = I'_{s0} = 0 \tag{6. 15}$$

Similarly, the apparent impedance seen by the distance relay is given as follows:

$$Z_{relay1} = \frac{V_L}{I_L} = Z_{L1}\left(1 + \frac{I_{STAT}}{I_s}\right) + pZ'_{L1}\frac{2I_s + I_{VSC} + I_{STAT} - I''_S}{I_s} + \frac{I_f}{I_L}R_f$$

$$= Z_{L1} + Z_{L1}\frac{I_{STAT}}{I_s} + pZ'_{L1}\frac{2I_s - I''_S}{I_s} + pZ'_{L1}\frac{I_{VSC}+I_{STAT}}{I_s} + \frac{I_f}{I_L}R_f \tag{6. 16}$$

By carefully looking into (6.11) and (6.16), the impacts of VSC HVDC and VSC FACTS connected to different buses on apparent impedance measured by distance relay against external faults can be summarised as:

1. The first and third terms ($Z_{L1} + pZ'_{L1}\frac{2I_s - I''_S + k'(2I_{s0} - I''_{S0})}{I_s + kI_{s0}}$ and $Z_{L1} + pZ'_{L1}\frac{2I_s - I''_S}{I_s}$) of (6.11) and (6.16) represent the actual line impedance of *TL1* and proportional line impedance of *TL2* to the fault location. The fifth term ($\frac{I_f}{I_s}R_f$) represents the contribution of fault resistance. These terms (the first, third and fifth) are not affected by VSC HVDC and VSC FACTS.
2. The second and fourth terms ($Z_{L1}\frac{I_{STAT}}{I_s + kI_{s0}} + pZ'_{L1}\frac{I_{VSC}+I_{STAT}}{I_s + kI_{s0}}$and $Z_{L1}\frac{I_{STAT}}{I_s} + pZ'_{L1}\frac{I_{VSC}+I_{STAT}}{I_s}$) of (6.11) and (6.16) indicates the impacts of VSC HVDC and VSC FACTS connected to different buses on distance relay against external faults lead to greater apparent impedance measurements. The under-reach effect is introduced as their impacts. Since during external fault, the VSC HVDC and STATCOM are injecting reactive power and current to support bus voltage, the apparent impedance is greater than no VSC HVDC or STATCOM. For steady state, while they are absorbing reactive power and current from busbars, the second and fourth terms could be negative. This negative value indicates less apparent impedance, which results in overreach effect. This error in apparent impedance measurement is related to fault location, and the current ratio of VSC HVDC/VSC FACTS and relay. For VSC HVDC and VSC FACTS connected to different buses, their impacts on distance protection are generally combination of their separate impacts.

6.2.2 VSC HVDC and VSC FACTS Connected to Same Bus

Figure 6- 2 shows the simplified single line diagram of a faulted network for the analysis of impacts of VSC HVDC and VSC FACTS connected simultaneously to same bus on distance protection of two-ended double-circuit transmission lines. Same topology of transmission system is studied as presented in 6.2.1, while the STATCOM is connected to *B2* the same bus with VSC HVDC. Same parameters and settings of transmission lines, power system, distance relays, STATCOM, and VSC HVDC are used as those studied in 6.2.1.

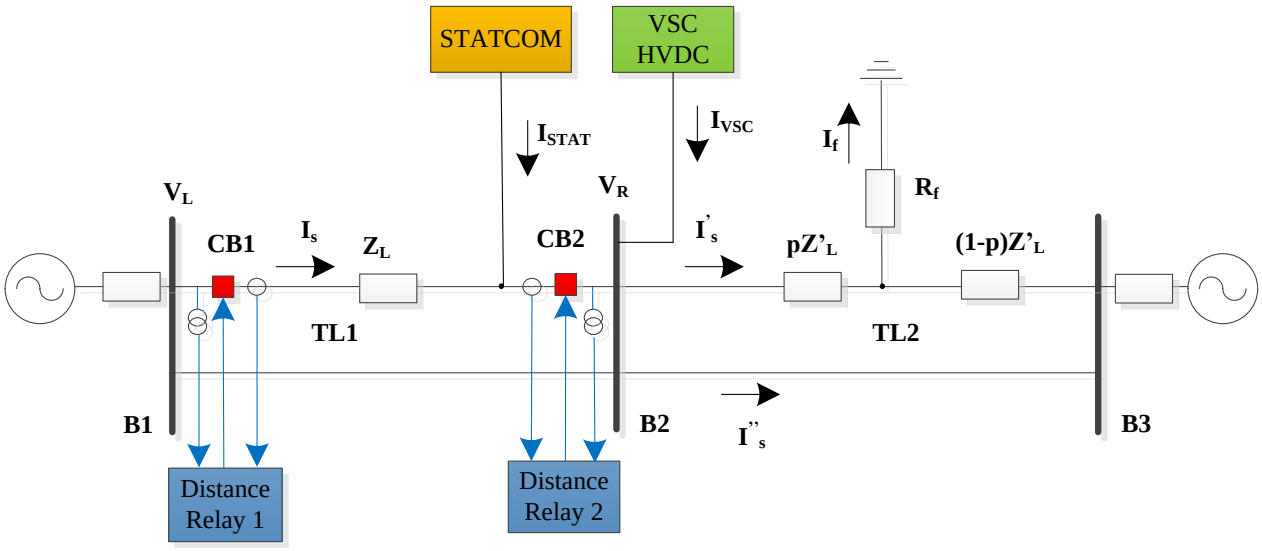


Figure 6- 2 Simplified single line diagram of a faulted network for the analysis of impact of VSC HVDC and VSC FACTS connected to same bus.

The impacts of VSC HVDC and VSC FACTS connected to the same bus on Zone 1 protection are the same with the impacts of VSC FACTS alone that has been studied in Chapter 5, since VSC HVDC has no significant impacts on Zone 1 protection as studied in Chapter 4. The impacts of VSC HVDC and VSC FACTS connected to the same bus on Zone 2 protection are studied since they both have significant impacts on Zone 2 protection.

The apparent impedance of VSC HVDC and VSC FACTS connected transmission line measured by distance relays are derived for SLG faults and three-phase faults to investigate their impacts.

For SLG faults, the voltages seen by VT at *B1* can be expressed as follows:

$$V_{Lx} = Z_{Lx} I_{sx} + pZ'_{Lx} I'_{sx} + I_{fx} R_f \quad (6.\ 17)$$

for $x = 1,2, or\ 0$ as a suffix denote of the sequence components, where

V_{Lx} : sequence phase voltages seen by VT at *B1*

I_{sx} : sequence phase currents seen by CT at *B1*

I'_{sx} : sequence phase current through faulted single-circuit of *TL2* from *B2* to *B3*

I_{fx} : sequence current through fault resistance

R_f : fault resistance

$Z_{Lx}$and Z'_{Lx} : sequence components of the line impedance of *TL1* and *TL2*

p : fault location from *B2* to *B3* in per unit of the total line length

The line positive and negative sequence impedances are assumed equal.

$$Z_{L1} = Z_{L2}, Z'_{L1} = Z'_{L2} \tag{6. 18}$$

By adding all three sequence components of left-hand side of (6.17) and substitute (6.18) into (6.17), the voltage seen by VT can be expressed after simplification as follows:

$$V_L = Z_{L1}(I_s + kI_{s0}) + pZ'_{Lx}(I'_s + k'I'_{s0}) + I_f R_f \tag{6. 19}$$

where

$V_L$and I_s : phase voltage and current of faulted phase through *TL1*

I'_s : phase current of faulted phase through faulted single-circuit of *TL2* from *B2* to *B3*

I_f : fault current through fault resistance

k : zero sequence current compensation factors of *TL1*

k' : zero sequence current compensation factors of *TL2*

$$k = \frac{Z_{L0} - Z_{L1}}{Z_{L1}} \tag{6. 20}$$

$$k' = \frac{Z'_{L0} - Z'_{L1}}{Z'_{L1}} \tag{6. 21}$$

For transient response study of double-circuit transmission line, the fault currents through the double circuits of *TL1* can be assumed to be equal due to the line parameters of double

circuits are same. Hence, by use of KCL law to *B2*, the relationship of inflow currents and outflow currents can be expressed as follows:

$$2I_s + I_{VSC} + I_{STAT} = I'_S + I''_S \quad (6.\ 22)$$

where

I_{VSC} : phase current infeed from VSC HVDC

I_{STAT}: phase current of faulted phase infeed from STATCOM

I''_S : phase current of faulted phase through unfaulted single-circuit of *TL2* from *B2* to *B3*

By substitute (6.22) into (6.19), the voltage seen by VT can be expressed as follows:

$$V_L = Z_{L1}(I_s + kI_{s0})$$

$$+pZ'_{Lx}[2I_s + I_{VSC} + I_{STAT} - I''_S + k'(2I_{s0} + I_{VSC0} + I_{STAT0} - I''_{S0})](I'_s + k'I'_{s0}) + I_f R_f \quad (6.\ 23)$$

By use of delta connection at one side of the coupling transformer of VSC HVDC and STATCOM, the zero-sequence current injection can be eliminated. Hence the zero-sequence currents are eliminated.

$$I_{VSC0} = 0 \quad (6.\ 24)$$

$$I_{STAT0} = 0 \quad (6.\ 25)$$

By substitute (6.24) and (6.25) into (6.23), the voltage seen by VT can be expressed as follows:

$$V_L = Z_{L1}(I_s + kI_{s0}) + pZ'_{Lx}[2I_s + I_{VSC} + I_{STAT} - I''_S + k'(2I_{s0} - I''_{S0})] + I_f R_f \quad (6.\ 26)$$

By use of phase voltage measurements at *B1* (V_L) and phase current measurement compensated by zero sequence current (I_L), the apparent impedance seen by Distance relay 1 is given as:

$$Z_{relay1} = \frac{V_L}{I_L} = Z_{L1} + pZ'_{L1}\frac{2I_s + I_{VSC} + I_{STAT} - I''_S + k'(2I_{s0} - I''_{S0})}{I_s + kI_{s0}} + \frac{I_f}{I_L}R_f$$

$$= Z_{L1} + pZ'_{L1}\frac{2I_s - I''_S + k'(2I_{s0} - I''_{S0})}{I_s + kI_{s0}} + pZ'_{L1}\frac{I_{VSC} + I_{STAT}}{I_s + kI_{s0}} + \frac{I_f}{I_L}R_f \quad (6.\ 27)$$

$$I_L = I_s + kI_{s0} \tag{6. 28}$$

where

Z_{relay1} : apparent impedance measured by distance relay

I_L : compensated phase current of faulted phase measure by distance relay

For three-phase faults, the phase current seen by distance relay is as follows:

$$I_L = I_s + kI_{s0} = I_s \tag{6. 29}$$

$$I_{s2} = I_{s0} = 0 \tag{6. 30}$$

$$I'_{s2} = I'_{s0} = 0 \tag{6. 31}$$

Similarly, the apparent impedance seen by the distance relay is given as follows:

$$Z_{relay1} = \frac{V_L}{I_L} = Z_{L1} + pZ'_{L1}\frac{2I_s + I_{VSC} + I_{STAT} - I''_S}{I_s} + \frac{I_f}{I_L}R_f$$

$$= Z_{L1} + pZ'_{L1}\frac{2I_s - I''_S}{I_s} + pZ'_{L1}\frac{I_{VSC} + I_{STAT}}{I_s} + \frac{I_f}{I_L}R_f \tag{6. 32}$$

For VSC HVDC and STATCOM connected to same bus, the potential interactions between these two VSC based power system devices should be considered.

For VSC HVDC and STATCOM operated with same control reference, positive interactions are expected [166-167]. In this situation, the VSC HVDC and STATCOM connected bus can be regarded as multiple shunt VSC-STATCOM connected bus with same control reference in aspect of bus voltage regulation. The bus voltage recovery in transient response is faster as more shunt STATCOM installed.

The infeed current from VSC HVDC and STATCOM can be expressed as follows:

$$I_{VSC} = \sqrt{{I_{VSCd}}^2 + {I_{VSCq}}^2} \tag{6. 33}$$

$$I_{STAT} = \sqrt{{I_{STATd}}^2 + {I_{STATq}}^2} \tag{6. 34}$$

where

I_{VSCd} and I_{VSCq}: phase currents infeed from VSC HVDC in *dq0* frame

I_{STATd} and I_{STATq} : phase currents infeed from STATCOM in *dq0* frame

For VSC HVDC and STATCOM modelled in this study and operated with same control reference, the power rating of VSC is normally higher than that of STATCOM in practical situation. Then the relationship of infeed currents in *q*-axis from VSC HVDC and STATCOM modelled in this study with same control reference can be expressed as follows:

$$I_{VSCq} > I_{STATq} \tag{6. 35}$$

For STATCOM with delta connection presented in Chapter 5, the relationship of infeed currents in *d*-axis from VSC and STATCOM can be expressed as follows:

$$I_{VSCd} > I_{STATd} \approx 0 \tag{6. 36}$$

Hence the relationship of infeed current from VSC HVDC and STATCOM can be expressed as follows:

$$I_{VSC} = \sqrt{{I_{VSCd}}^2 + {I_{VSCq}}^2} > I_{STAT} = \sqrt{{I_{STATd}}^2 + {I_{STATq}}^2} \tag{6. 37}$$

By look into the third term of (6.27) and (6.32), the relationship of error in measured apparent impedance due to VSC HVDC (ΔZ_{VSC}) and error in measured apparent impedance due to STATCOM (ΔZ_{STAT}) can be expressed as follows:

$$\Delta Z_{VSC} = pZ'_{L1}\frac{I_{VSC}}{I_L} > \Delta Z_{STAT} = pZ'_{L1}\frac{I_{STAT}}{I_L} \tag{6. 38}$$

For VSC HVDC and STATCOM operated with different control reference, negative interactions are expected [166-167]. In this situation, the bus voltage recovery in transient response is slower.

By carefully looking into (6.27) and (6.32), the impacts of VSC HVDC and VSC FACTS connected to same bus on apparent impedance measured by distance relay against external faults can be summarised as follows:

1. The first and second terms ($Z_{L1} + pZ'_{L1}\frac{2I_s - I''_S + k'(2I_{s0} - I''_{S0})}{I_s + kI_{s0}}$ and $Z_{L1} + pZ'_{L1}\frac{2I_s - I''_S}{I_s}$) of (6.27) and (6.32) represent the actual line impedance of TL1 and proportional line impedance of TL2 to the fault location. The fourth term ($\frac{I_f}{I_s}R_f$) represents the contribution of fault resistance. These terms (the first, second and fourth) are not affected by compensation of VSC HVDC and VSC FACTS connected to same bus.
2. The third terms ($pZ'_{L1}\frac{I_{VSC} + I_{STAT}}{I_s + kI_{s0}}$ and $pZ'_{L1}\frac{I_{VSC} + I_{STAT}}{I_s}$) of (6.27) and (6.32) indicates that the impacts of VSC HVDC and VSC FACTS connected to same bus on the apparent impedance measured by distance relay against external fault lead to greater apparent impedance measurements. The under-reach effect is introduced as their impacts. Since during external fault, the VSC HVDC and STATCOM are injecting reactive power and current to support bus voltage, the apparent impedance is greater than test system without VSC HVDC and VSC FACTS. For steady state, while they are absorbing reactive power and current from busbar, the third term could be negative. This negative value indicates less apparent impedance, which results in overreach effect. This error in apparent impedance measurement caused by VSC HVDC and VSC FACTS is related to the current ratio, and fault location.
3. For VSC and STATCOM modelled in this study and operated with same control reference, the error in measured apparent impedance due to VSC HVDC is generally higher than error due to STATCOM.

6.2.3 VSC HVDC and Multiple VSC FACTS

Figure 6- 3 shows the simplified single line diagram of a faulted network for the analysis of impacts of VSC HVDC and multiple VSC FACTS on distance protection of two-ended double-circuit transmission lines. Same topology of transmission system is studied as presented in 6.2.1, while two STATCOMs are connected to *B1* and *B2*. Same parameters and settings of transmission lines, power system, distance relays, STATCOM, and VSC HVDC are used as those studied in 6.2.1.

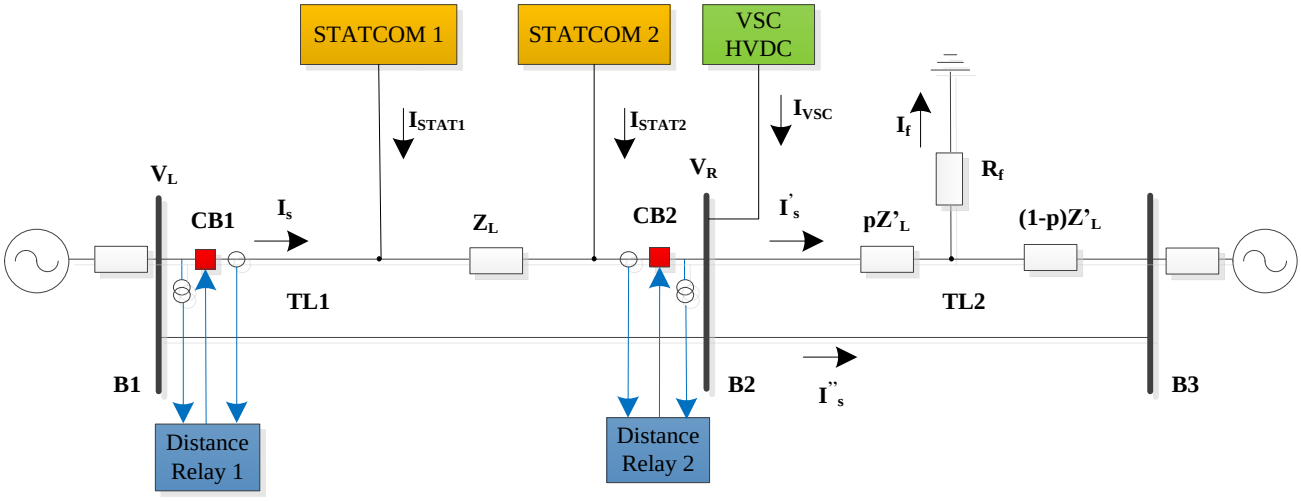


Figure 6- 3 Simplified single line diagram of a faulted network for the analysis of impacts of VSC HVDC and multiple VSC FACTS.

The impacts of VSC HVDC and multiple VSC FACTS on Zone 1 protection are the same with the impacts of VSC FACTS alone that has been studied in Chapter 5, since VSC HVDC system has no significant impacts on Zone 1 protection as studied in Chapter 4. The impacts of VSC HVDC and multiple VSC FACTS on Zone 2 protection against external faults are studied since they both have significant impacts on Zone 2 protection.

The apparent impedance of VSC HVDC and multiple VSC FACTS connected transmission line measured by Distance relay 1 is derived for SLG faults and three-phase faults to investigate their impacts.

By use of approaches presented in 6.2.1 and 6.2.2, the voltage seen by VT at *B1* against SLG faults can be calculated as follows:

$$Z_{relay1} = \frac{V_L}{I_L} = Z_{L1} + Z_{L1}\frac{I_{STAT1}}{I_s + kI_{s0}} + pZ'_{L1}\frac{2I_s - I''_S + k'(2I_{s0} - I''_{S0})}{I_s + kI_{s0}}$$

$$+pZ'_{L1}\frac{I_{VSC}+I_{STAT1}+I_{STAT2}}{I_s+kI_{s0}} + \frac{I_f}{I_L}R_f \qquad (6.\ 39)$$

$$I_L = I_s + kI_{s0} \qquad (6.\ 40)$$

$$2I_s + I_{VSC} + I_{STAT1} + I_{STAT2} = I'_S + I''_S \qquad (6.\ 41)$$

where

$V_L$and I_s : phase voltage and current of faulted phase through *TL1*

I_L : compensated phase current of faulted phase measure by Distance relay 1

I_{s0} : zero sequence phase currents seen by CT at *B1*

$I_{STAT1}$and I_{STAT2} : phase current of faulted phase infeed from STATCOM 1 and STATCOM 2

I_{VSC} : phase current of faulted phase infeed from VSC HVDC

I'_s and I''_S: phase currents of faulted phase through faulted and unfaulted single-circuit of *TL2* from *B2* to *B3*

I_f : fault current through fault resistance

R_f : fault resistance

Z_{relay1} : apparent impedance measured by Distance relay 1

$Z_{L1}$and Z'_{L1} : positive sequence components of the line impedance of *TL1* and *TL2*

p : fault location from *B2* to *B3* in per unit of the total line length

k : zero sequence current compensation factors of *TL1*

k' : zero sequence current compensation factors of *TL2*

$$k = \frac{Z_{L0} - Z_{L1}}{Z_{L1}} \tag{6. 42}$$

$$k' = \frac{Z'_{L0} - Z'_{L1}}{Z'_{L1}} \tag{6. 43}$$

Similarly, the apparent impedance seen by the Distance relay 1 against three-phase faults can be calculated as follows:

$$Z_{relay1} = \frac{V_L}{I_L} = Z_{L1} + Z_{L1}\frac{I_{STAT1}}{I_s} + pZ'_{L1}\frac{2I_s - I''_S}{I_s} + pZ'_{L1}\frac{I_{VSC} + I_{STAT1} + I_{STAT2}}{I_s} + \frac{I_f}{I_L}R_f \tag{6. 44}$$

By carefully looking into (6.39) and (6.44), the impacts of VSC HVDC and multiple VSC FACTS on apparent impedance measured by distance relay against external faults can be summarised as follows:

1. The first and third terms ($Z_{L1} + pZ'_{L1}\frac{2I_s - I''_S + k'(2I_{s0} - I''_{S0})}{I_s + kI_{s0}}$ and $Z_{L1} + pZ'_{L1}\frac{2I_s - I''_S}{I_s}$) of (6.39) and (6.44) represent the actual line impedance of *TL1* and proportional line impedance of *TL2* to the fault location. The fifth term ($\frac{I_f}{I_L}R_f$) represents the contribution of fault resistance. These terms (the first, third and fifth) are not affected by VSC HVDC and multiple VSC FACTS.
2. The second and fourth terms ($Z_{L1}\frac{I_{STAT1}}{I_s + kI_{s0}} + pZ'_{L1}\frac{I_{VSC} + I_{STAT1} + I_{STAT2}}{I_s + kI_{s0}}$ and $Z_{L1}\frac{I_{STAT1}}{I_s} + pZ'_{L1}\frac{I_{VSC} + I_{STAT1} + I_{STAT2}}{I_s}$) of (6.39) and (6.44) indicate that the impacts of VSC HVDC and multiple VSC FACTS on the apparent impedance measured by distance relay against external faults lead to greater apparent impedance measurements. The under-reach effect is introduced as their impacts. Since during external faults, the VSC HVDC and multiple VSC FACTS are injecting reactive power and current to support bus voltage, the apparent impedance is greater than test system without them. For steady state, while they are absorbing reactive power and current from busbar, the second and fourth terms could be negative. This negative value indicates less apparent impedance, which results in overreach effect. This error in apparent impedance measurement caused by VSC HVDC and multiple VSC FACTS is related to the current ratio, and fault location
3. For VSC HVDC and multiple STATCOM, their impacts on distance protection are generally combination of separate impacts of VSC HVDC and STATCOM connected to same bus and separate impacts of the other isolated STATCOM.

6.3 Dynamic Simulation Study

6.3.1 Test System with VSC HVDC and VSC FACTS and Protection Relay Settings

The schematic diagram of the trial network is illustrated in Figure 6- 4. There is one GE MiCOM P40 Agile P443 distance relay located at each end of two-ended transmission lines from *B1* to *B2*. In this thesis, communications between relays are not considered. Same transmission line parameters and equivalent voltage source parameters are used as those in 4.4 which are listed in Appendix B.1 and B.2. A VSC HVDC system is connected to *B2*. A MMC delta connection STATCOM modelled in 5.2 is connected to *B1*or *B2*.

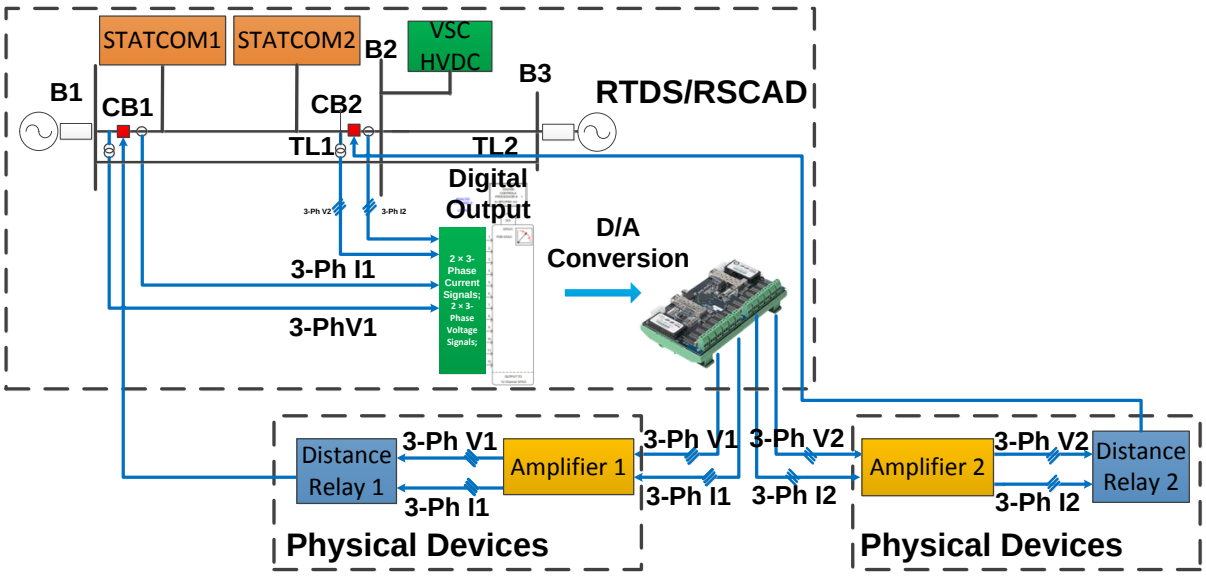


Figure 6- 4 RTDS based HIL test platform for VSC and STATCOM studies.

Figure 6- 4 shows the same arrangements of VTs, CTs and CBs for one of the aforementioned series compensated lines between *B1* and *B2* as applied in Chapter 4. Same distance protection as applied in Chapter 4 using GE MiCOM P40 Agile P443 distance protection relays is used. Two VTs and two CTs at both ends of the transmission line provide voltage and current measurements.

The following considerations are taken into account for the setting of the 2-ended distance protections:

1. Zone 1 is set to 75% of the complete circuit positive sequence impedance. The tripping delay is set to 0ms.
2. Zone 2 is set to reach 150% of the complete circuit positive sequence impedance. The tripping delay is set to 500ms.

6.3.2 Dynamic Simulation Results of Test System with VSC HVDC and VSC FACTS at Different Locations

External faults occur at one single-circuit of *TL2* from *B2* to *B3* under such fault conditions:

1. 600ms fault occurred at 5% and 35% of the equivalent whole length of *TL1*.
2. Fault resistance is 0.01Ω, and 1 Ω.
3. SLG and three-phase to ground faults are considered.

Table 6- 1 shows the simulation results of external fault. The tripped zone is noted as "I", "II", or "X" for Zone 1, Zone 2 or no relay operation is seen, respectively. Fault type is noted as "RYB-G", or "R-G" for three-phase to ground, or SLG faults, respectively. Different locations of STATCOM are noted as "VSC+STATB1", "VSC+STATB2", or "VSC+STATB1+STATB2" for connection to *B1*, *B2*, or both *B1*and *B2*.

Table 6- 1 Simulation results of external fault

Case	Fault Location	Fault Impedance	Fault Type	Fault Duration	Distance relay 1			
					No VSC No STAT	VSC+ STATB1	VSC+ STATB2	VSC+STATB1 +STATB2
1	105%	0.01Ω	RYB-G	600ms	**II 105.5%**	**II 108.2%**	**II 107.6%**	**II 109.5%**
2	105%	0.01Ω	R-G	600ms	**II 105.9%**	**II 108.9%**	**II 108.3%**	**II 110.5%**
3	105%	1Ω	RYB-G	600ms	**II 106.1%**	**II 108.9%**	**II 108.1%**	**II 110.1%**
4	105%	1Ω	R-G	600ms	**II 106.5%**	**II 109.6%**	**II 108.8%**	**II 111.0%**
5	135%	0.01Ω	RYB-G	600ms	**II 136.5%**	**II 147.0%**	**II 145.3%**	**II 149.1%**
6	135%	0.01Ω	R-G	600ms	×	×	×	×
7	135%	1Ω	RYB-G	600ms	×	×	×	×
8	135%	1Ω	R-G	600ms	×	×	×	×

Figure 6- 5 shows digital signals from RSCAD against a typical external fault Case 1 of Table 6- 1 with no VSC HVDC or STATCOM, and the trajectory of impedance measurement by distance relay. Figure 6- 6 shows digital signals from RSCAD against same external fault with VSC HVDC and STATCOM connected to *B1*, and the corresponding trajectory of impedance measurement. Figure 6- 7 shows digital signals from RSCAD against same external fault with VSC HVDC and STATCOM connected to *B2*, and the corresponding trajectory of impedance measurement. Figure 6- 8 shows digital signals from RSCAD against same external fault with VSC HVDC and STATCOM connected to *B1* and *B2*, and the corresponding trajectory of impedance measurement.

As shown in Figure 6- 7, VT and CT send voltage and current measurements (noted as VA/VB/VC and IA/IB/IC) to distance relay. By use of the received measurements and impedance calculation algorithm presented in 6.2, the apparent impedance is calculated (noted as ZIM vs ZRE). The trip signals (noted as TripA/TripB/TripC) are sent to corresponding CBs, by judgement if calculated apparent impedance is within protection zones. The CBs are turn off or turn on (noted as CBA/CBB/CBC), controlled by received trip signals.

By comparison of the apparent impedances measured by distance relay in Table 4- 1, Table 5- 2, and Table 6- 1, the apparent impedance with VSC HVDC and STATCOM is greater than impedance without them. The under-reach effect of distance relay is seen due to the incorporation of VSC HVDC and STATCOM. The relationship of measured impedances of VSC HVDC and different location of STATCOM can be expressed as follows:

$$Z_{noSTAT} < Z_{STATB2} < Z_{STATB1} < Z_{VSC+STATB2} < Z_{VSC+STATB1} < Z_{VSC+STATB1+STAT2} \quad (6.\ 45)$$

where

Z_{noSTAT}: measured impedance with no STATCOM or VSC HVDC

Z_{STATB1}: measured impedance with STATCOM connected to *B1*

Z_{STATB2}: measured impedance with STATCOM connected to *B2*

$Z_{VSC+STATB1}$: measured impedance with VSC HVDC and STATCOM connected to *B1* (different buses)

$Z_{VSC+STATB2}$: measured impedance with VSC HVDC and STATCOM connected to *B2* (same bus)

$Z_{VSC+STATB1+STAT2}$: measured impedance with VSC HVDC and STATCOM connected to *B1* and *B2*

This relationship of measured impedances of VSC HVDC with different locations of STATCOM is in line with the conclusions in 6. 2.

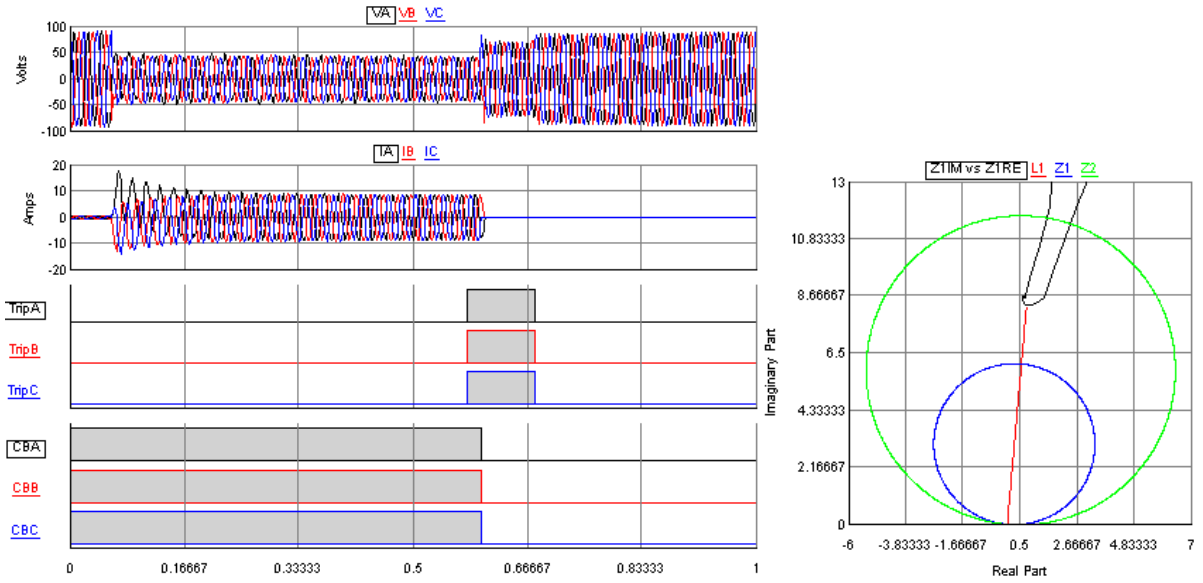


Figure 6- 5 Digital signals from RSCAD against external fault Case 1 of Table 6- 1 with no VSC HVDC or STATCOM.

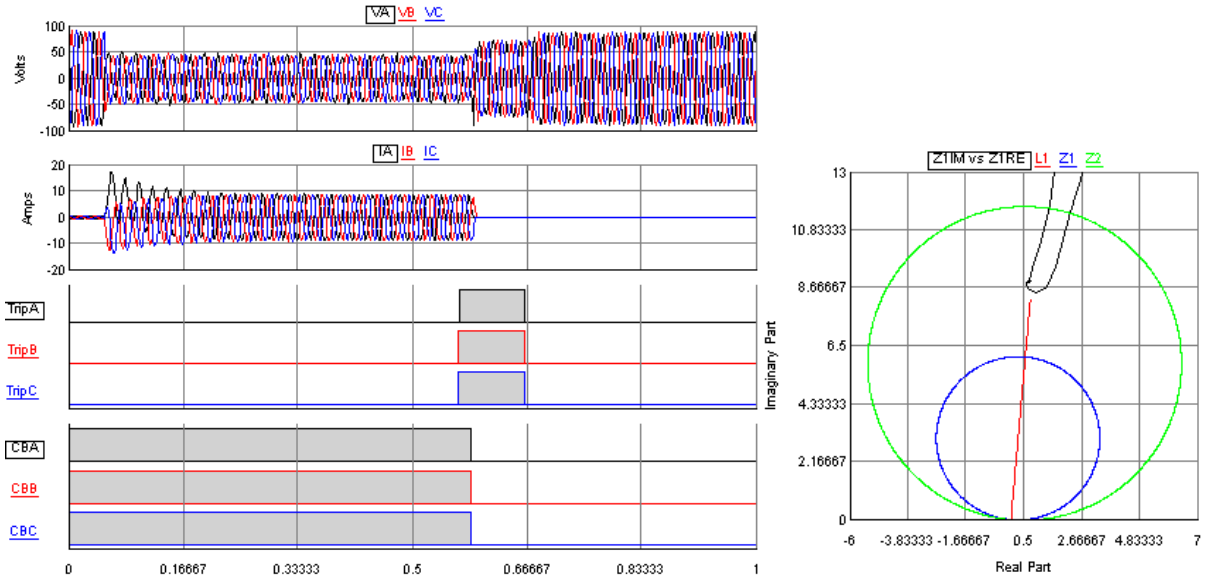


Figure 6- 6 Digital signals from RSCAD against same external fault with VSC HVDC and STATCOM connected to B1.

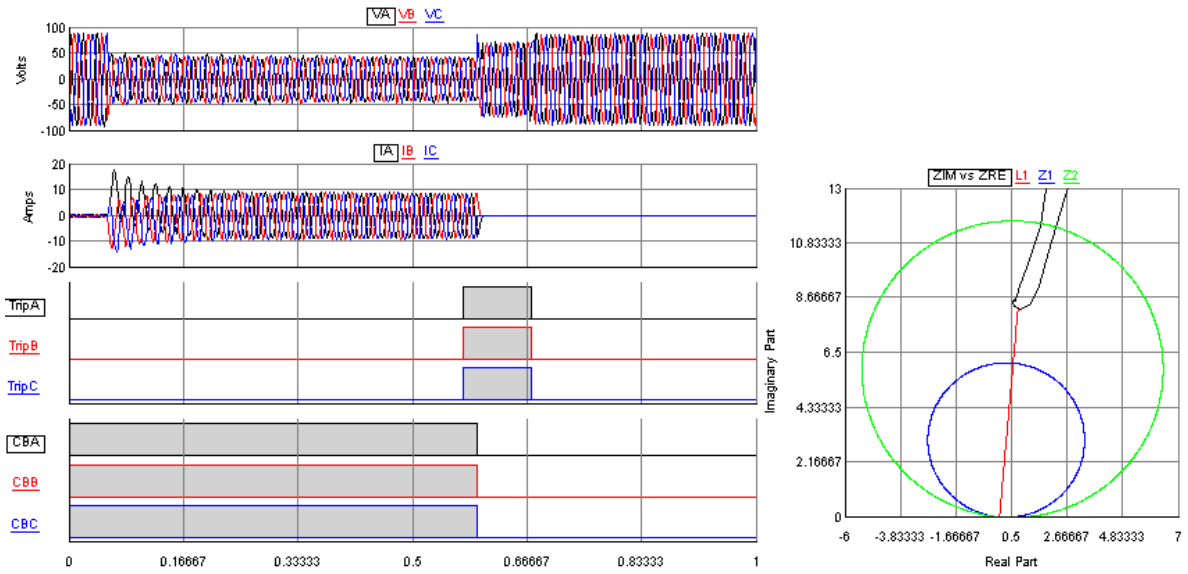


Figure 6- 7 Digital signals from RSCAD against same external fault with VSC HVDC and STATCOM connected to B2.

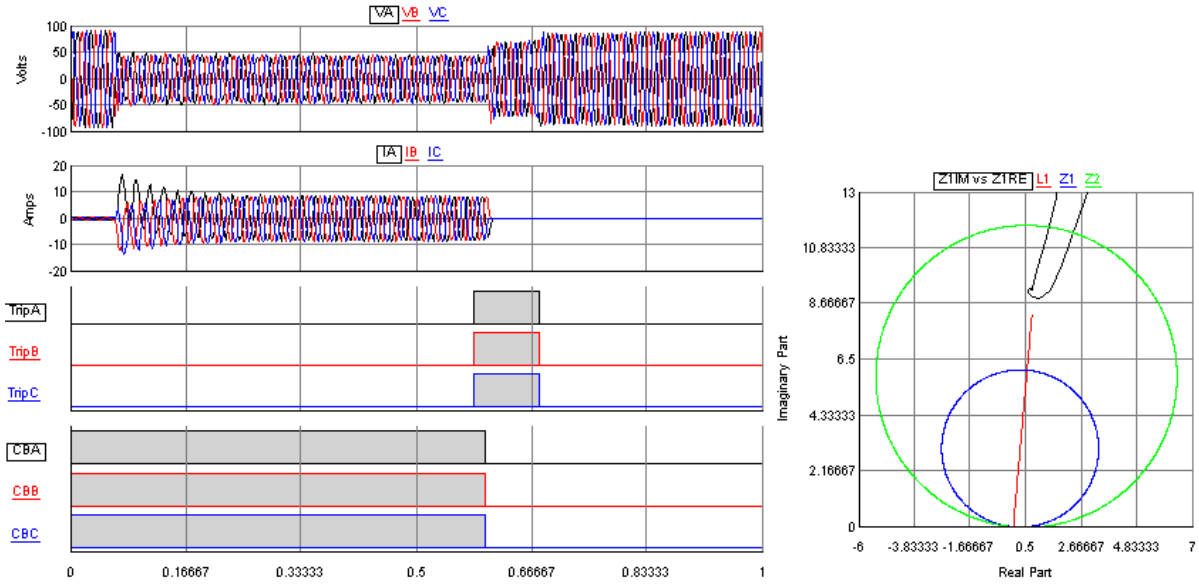


Figure 6- 8 Digital signals from RSCAD against same external fault with VSC HVDC and STATCOM connected to B1 and B2.

Figure 6- 9 shows the digital signals from RSCAD for a SLG external fault Case 2 of Table 6- 1 with VSC HVDC and STATCOM connected to *B2*. As voltage and current measurement of VT and CT (noted as VA/VB/VC and IA/IB/IC) shown in Figure 6- 9, SLG fault occurred. The three-phase trip signals (noted as TripA/TripB/TripC) are sent to corresponding CBs. This is due to the fact that distance relay settings require relays trip all three phase for Zone 2 protection.

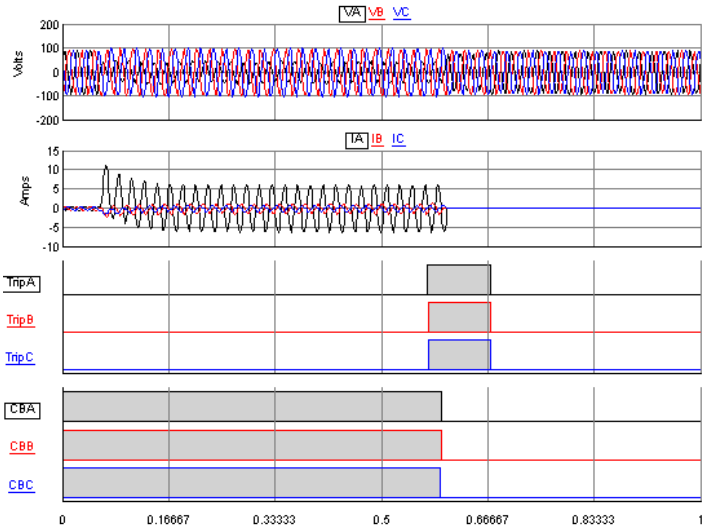


Figure 6- 9 Digital signals from RSCAD for a SLG external fault Case 2 with VSC HVDC and STATCOM connected to B2.

Figure 6- 10 shows digital signals from RSCAD against a 1 Ω external fault Case 3 of Table 6- 1 with VSC HVDC and STATCOM at *B2*, and the trajectory of impedance measurement. By comparison of the apparent impedances measured by distance relay, the apparent impedance against 1 Ω fault is greater than impedance against 0.01 Ω. These results are in line with the conclusion in 6.2 that the error of measured impedance is positively related to fault resistance.

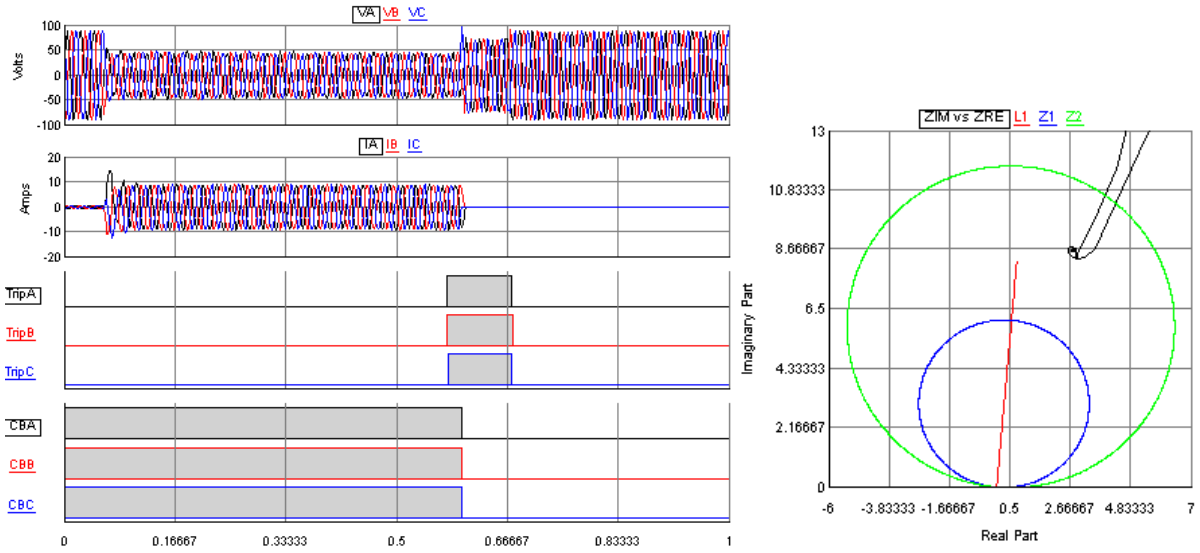


Figure 6- 10 Digital signals from RSCAD for a 1 Ω external fault Case 3 with VSC HVDC and STATCOM at B2.

Figure 6- 11 shows digital signals from RSCAD against a 135% external fault Case 7 of Table 6- 1 with VSC HVDC and STATCOM at *B2*, and the trajectory of impedance measurement by distance relay. It can be seen from Figure 6- 11 that the distance relay is not tripped if the fault distance is too far. By comparison of the apparent impedances measured

by distance relay, the apparent impedance against 135% fault is greater than impedance against 105% fault. These results are in line with the conclusions in 6.2 that the error of measured impedance is positively related to fault distance.

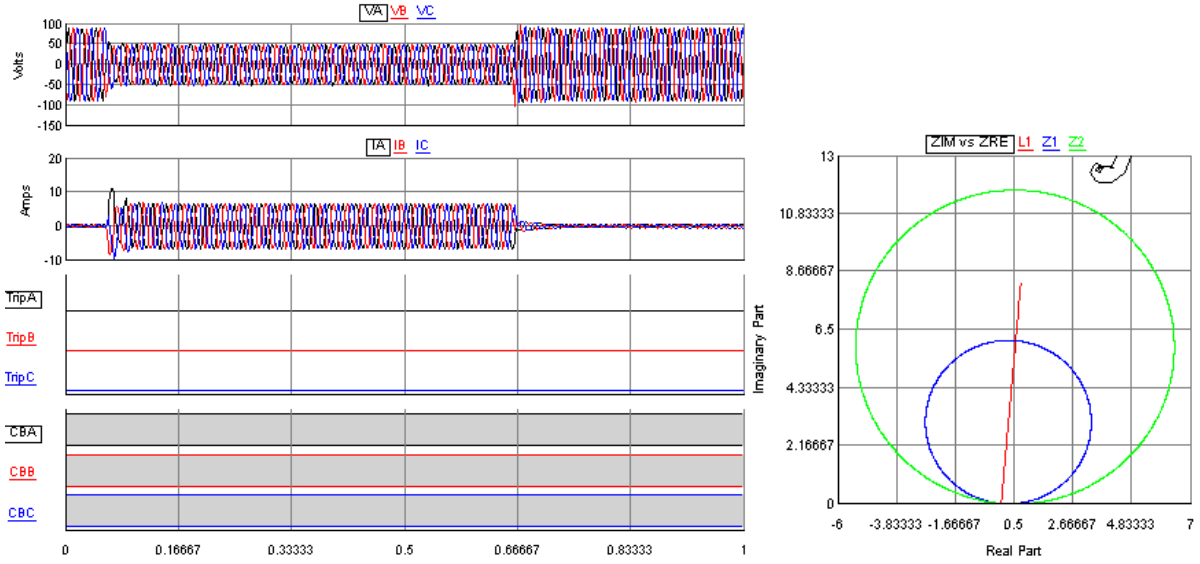


Figure 6- 11 Digital signals from RSCAD for a 135% external fault Case 7 with VSC HVDC and STATCOM at B2.

6.4 Summary

In this chapter, the mathematical representations of the apparent impedance measurement of distance relay against external faults have been derived considering the infeed current from VSC HVDC and shunt VSC FACTS connected simultaneously to different buses, VSC HVDC and shunt VSC FACTS connected simultaneously to same bus, and VSC HVDC and multiple shunt VSC FACTS. For the derived mathematical representation of the apparent impedance measurement of distance relay with VSC HVDC and STATCOM connected to different buses, some part (the first, third and fifth terms) is not affected by them while the other part (the second and fourth terms) indicates that the impacts of VSC HVDC and VSC FACTS connected to different buses on distance relay against external faults lead to greater apparent impedance measurement. The under-reach effect is introduced as their impacts. Since during the external fault, the VSC HVDC and STATCOM are injecting reactive power and current to support bus voltage, the apparent impedance is greater than no VSC HVDC and VSC FACTS. For steady state, while they are absorbing reactive power and current from busbars, the second and fourth terms could be negative. This negative value indicates less apparent impedance, which results in overreach effect. This error in apparent impedance

measurement caused by VSC HVDC and VSC FACTS is related to the current ratio, and fault location. For VSC HVDC and VSC FACTS connected to different buses, their impacts on distance protection are generally combination of their separate impacts.

For VSC HVDC and STATCOM connected to same bus, the potential interactions between these two VSC based power system devices have be considered. The relationship of error in measured apparent impedance due to VSC HVDC and error in measured apparent impedance due to STATCOM can be expressed as follows:

$$\Delta Z_{VSC} = pZ'_{L1}\frac{I_{VSC}}{I_L} > \Delta Z_{STAT} = pZ'_{L1}\frac{I_{STAT}}{I_L}$$

Hence for the derived mathematical representation of the apparent impedance measurement of distance relay against external faults with VSC HVDC and STATCOM connected to same bus, some part (the first, second and fourth terms) is not affected by them while the other part (the third term) indicates greater apparent impedance measurements. The under-reach effect is introduced as their impacts. The error in apparent impedance measurement caused by VSC HVDC and VSC FACTS is related to the current ratio, and fault location. For VSC HVDC and STATCOM modelled in this study and operated with same control reference, the error in measured apparent impedance due to VSC HVDC is generally higher than error due to STATCOM.

As for the derived mathematical representation of apparent impedance measurement of distance relay against external faults with VSC HVDC and multiple STATCOM, some part (the first, third and fifth terms) are not affected by compensation of VSC HVDC and multiple STATCOM while the other part (second and fourth terms) indicates that the impacts of VSC HVDC and multiple VSC FACTS on apparent impedance distance relay against external faults lead to greater apparent impedance measurement. This error in apparent impedance measurement caused by VSC HVDC and multiple VSC FACTS is related to the current ratio, and fault location. For VSC HVDC and multiple STATCOM, their impacts on distance protection are generally combination of separate impacts of VSC HVDC and STATCOM connected to same bus and separate impacts of the other isolated STATCOM.

As shown in dynamic simulation results in RTDS/RSCAD, the apparent impedance with VSC HVDC and STATCOM is greater than impedance without them, by comparison of the

apparent impedances measured by distance relay. The under-reach effect of distance relay is seen due to the incorporation of VSC HVDC and STATCOM.

In general, to conclude the summaries of Chapter 4, Chapter 5, and Chapter 6, the combined impacts of VSC HVDC and VSC FACTS connected at different busbars are combination of the separate impacts of VSC HVDC and VSC FACTS. However, when VSC HVDC and VSC FACTS are connected at same busbar, the control strategy and control reference matters. Negative interactions between VSC HVDC and VSC FACTS and unstable oscillations would show, if different voltage references are set. While under same control reference settings, the relationship of measured impedances of VSC HVDC with different location of STATCOM can be expressed as follows:

$$Z_{noSTAT} < Z_{STATB2} < Z_{STATB1} < Z_{VSC+STATB2} < Z_{VSC+STATB1} < Z_{VSC+STATB1+STAT2}$$

The error of the measured impedance is positively related to fault resistance, and fault distance.

CHAPTER 7 CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

The recent progress of high-voltage high-power fully controlled semiconductor technology laid the foundation of VSC, which continues to advance the developments of HVDC technology and FACTS. Nowadays, due to the ever increasing amount of the integrations of renewable energy sources into power systems and the demand of long-distance bulk power transmission with enhanced power system controllability and increased power transfer capability, VSC converter based technology (in particular, VSC HVDC and VSC FACTS) has been applied as a crucial solution to these big challenges. However, the high penetration of these VSC based systems may introduce certain risks to the existing power systems in two primary aspects: dynamic stability and protection.

This thesis has conducted comprehensive investigations on system dynamic stability and protection due to the integration of VSC HVDC and VSC FACTS. The main conclusions of the thesis on system dynamic stability studies of VSC HVDC based MTDC system can be summarised as follows:

1. In this thesis, an integrated small-signal stability model for the study of interactions between CFC and VSC has been established, which consists of multiple synchronous generators with excitation system and PSS, multiple VSC converters, and DC network with CFC. Modal analysis of small-signal stability model of multi-model system has been conducted and the modal analysis results have been verified by the simulation results from RTDS under both small and large AC/DC disturbances.
2. Based on the eigenvalue analysis and dynamic simulations, the incorporation of CFC has been shown to affect dynamic stability of the existing MTDC/AC system especially the adjacent VSC converters. Compared to eigenvalue results of AC/DC system without CFC, there is no significant changes of values of synchronous generator related conjugate pairs caused by the incorporation of CFC. This indicates that the corporation of CFC has no significant impacts on dynamic stability of multi synchronous generators.
3. An approach of determining stable/unstable setting ranges of control parameters of CFC has been presented and validated by simulation results in RTDS/RSCAD. The simulation

results have demonstrated that the control parameters of CFC could cause instability of the system if they are not carefully-tuned.

4. Based on eigenvalue trajectory studies of CFC control gains, the variation of CFC controller has shown to affect dynamic stability of CFC and VSC related modes. These impacts of CFC on VSC have resulted in different damping characteristics of VSC related states, as CFC controller changes. This effect can be severe and cause instability to the AC/DC system, for extreme CFC operating conditions.
5. The variation of VSC controller has shown to affect dynamic stability of synchronous generators, VSC, and CFC related modes, based on eigenvalue trajectory studies of VSC control gains. These impacts have resulted in different damping characteristics of CFC related states, as VSC controller changes. And this effect can be negative and cause instability of the CFC integrated DC network, for extreme VSC operating conditions. It has been found that the interactions between CFC and VSC could be severe and may cause instability to the integrated MTDC/AC system. The proposed modelling approach and methodology of analysis in this thesis has provided a useful foundation that can be expanded for potential research of coordinated design of CFC control system and control system of VSC to avoid possible negative interactions between them.

The main conclusions of the thesis on the impacts of VSC HVDC and VSC FACTS (in particular, STATCOM as an example to study) on existing feeder distance protection can be summarised as follows:

1. For test system without/with VSC HVDC, the apparent impedance of test system with VSC is greater than impedance with no VSC HVDC integration. A RTDS-based HIL testing platform has been established using realistic transmission data, practical distance relays, VSC HVDC and multiple detailed STATCOM. The VSC HVDC's impact on feeder distance protection has been investigated, by conducting different types of internal/external fault tests occurred at various distances. The under-reach effect of distance relay has been found due to the incorporation of VSC. The error of measured impedance has shown to be positively related to fault resistance, and fault distance.
2. The detailed representation of delta-connected MMC STATCOM has been modelled in this thesis and its impact on feeder distance protection has been studied.
    - For test system without/with STATCOM against internal faults, the apparent impedance of neighbouring distance relay with STATCOM is greater than impedance

with no STATCOM. The under-reach effect of neighbouring distance relay has been found due to the incorporation of STATCOM. The error of the measured impedance has shown to be positively related to fault resistance, and fault distance. For impedance measurements of remote distance relay, there is no significant difference of impedance measurement with/without STATCOM.

- For test system without/with STATCOM against external faults, the apparent impedance with STATCOM is greater than impedance with no STATCOM. The under-reach effect of distance relay is seen. The error of measured impedance is positively related to fault resistance, and fault distance.

3. For test system with VSC HVDC and STATCOM integrated simultaneously at different locations, the apparent impedance with VSC HVDC and STATCOM is greater than impedance without them. The under-reach effect of distance relay has been found due to the incorporation of VSC HVDC and STATCOM. The relationship of error in the measured apparent impedances due to VSC HVDC and that due to STATCOM can be expressed as follows:

$$\Delta Z_{VSC} = pZ'_{L1}\frac{I_{VSC}}{I_L} > \Delta Z_{STAT} = pZ'_{L1}\frac{I_{STAT}}{I_L}$$

And the relationship of measured impedances of VSC HVDC with different locations of STATCOM can be expressed as follows:

$$Z_{noSTAT} < Z_{STATB2} < Z_{STATB1} < Z_{VSC+STATB2} < Z_{VSC+STATB1} < Z_{VSC+STATB1+STAT2}$$

The impacts of the main contributions of this thesis on the industry and commerce can be concluded as follows:

1. The dynamic analysis of the impacts of CFC on existing MTDC systems and the interactions between CFC and VSC converters can be used as a viable methodology to design and improve DC current flow controllers and their control systems so that they can be installed into DC grid in practise.
2. The studies of the impacts of VSC HVDC and VSC FACTS on distance protection can be applied for improvements of the existing distance protection schemes and design of new distance protection schemes that considers the impacts of VSC systems.

7.2 Future Work

Built upon the achievements of this PhD work, the possible future works are suggested as follows:

1. The dynamic characteristics of modulation technique of VSC converters can be considered to reflect more accurate dynamic stability of VSC converters. The dynamic characteristics of modulation algorithm of submodules of MMC can be considered and the MMC converters can be applied as AC/DC converters for MTDC system.
2. Other control strategies of MTDC system can be considered, for instance voltage and active power droop control, and power synchronization control. The study of small-signal stability analysis of various control strategies can meet the needs of investigation of system dynamic stability under different control targets.
3. The coordinated design of CFC control system and control system of VSC can be carried out in order to avoid possible negative interactions between them.
4. Investigation of potential interactions between VSC HVDC and VSC FACTS can be conducted in depth, and the mathematical analysis of these interactions can be performed for coordinated controlled design of these two VSC based systems.

APPEDNDIX A

A.1 Generator Parameters

Table A- 1 Generator parameters

	G1	G2	G3	G4
Rated MVA	900	900	900	900
X_L	0.2	0.2	0.2	0.2
R_s	0	0	0	0
X_d	1.8	1.8	1.8	1.8
X'_d	0.3	0.3	0.3	0.3
X''_d	0.25	0.25	0.25	0.25
T'_{do}	8	8	8	8
T''_{do}	0.03	0.03	0.03	0.03
X_q	1.7	1.7	1.7	1.7
X'_q	0.55	0.55	0.55	0.55
X''_q	0.25	0.25	0.25	0.25
T'_{qo}	0.4	0.4	0.4	0.4
T''_{qo}	0.05	0.05	0.05	0.05
H	6.5	6.5	6.175	6.175

A.2 Excitation System Parameters

Table A- 2 Excitation system parameters

	G1	G2	G3	G4
K_A	200	200	200	200
T_A	0.05	0.05	0.05	0.05

A.3 PSS Parameters

Table A- 3 PSS parameters

	G1	G3
K_{pss}	10	10
T_w	10	10
T_a	0.05	0.05
T_b	0.02	0.02
T_c	0.08	0.08

T_d	0.015	0.015

A.4 Transmission Line Parameters

Table A- 4 Transmission line parameters

End 1 bus index	End 2 bus index	Resistance (p.u.)	Reactance (p.u.)	Line charging (p.u.)
1	5	0	0.0167	0
2	6	0	0.0167	0
3	11	0	0.0167	0
4	10	0	0.0167	0
5	6	0.0025	0.025	0.0437
10	11	0.0025	0.025	0.0437
6	7	0.001	0.01	0.0175
9	10	0.001	0.01	0.0175
7	8	0.0022	0.22	0.385
8	9	0.0022	0.22	0.385

A.5 Generation Data

Table A- 5 Generation data

	Active power (MW)	Reactive power (Mvar)
G1	700	185
G2	700	235
G3	700	176
G4	700	202

A.6 Load Data

Table A- 6 Load data

Bus index	Active power (MW)	Reactive power (Mvar)	Reactive compensation (Mvar)
7	967	100	200
9	1767	100	350

A.7 VSC Parameters

Table A- 7 VSC parameters

	VSC1	VSC2	VSC3
$R_c(\Omega)$	0.01	0.01	0.01
$L_c(mH)$	7.18	7.18	7.18
$C_{dc}(\ mF)$	5	5	5

A.8 DC Network Parameters

Table A- 8 DC network parameters

End 1 VSC index	End 2 VSC index	Resistance (Ω)	Reactance (H)
1	2	1	0.07
1	3	1	0.09
2	3	1	0.1

A.9 CFC Parameters

Table A- 9 CFC parameters

	CFC
$C_{cfc}(mF)$	1
d_{a1}	0.5
d_{c1}	0.5
d_{a2}	0.5
d_{a2}	0.5

APPENDIX B

B.1 Transmission Line Parameters

Table B- 1 Transmission line parameters

	TL1	TL2
Length (km)	25.4	26.7
Z_1 (Ω/km)	0.32∠84.8°	0.31∠85.4°
Z_0 (Ω/km)	0.85∠80.7°	Z0=0.84∠80.3°

B.2 Equivalent Voltage Sources and Internal Impedance Parameters

Table B- 2 Equivalent voltage sources and internal impedance parameters

	Voltage Source 1	Voltage Source 2
Voltage level (kV)	400	400
Z_1 (Ω)	1.37∠86.5°	1.37∠86.5°
Z_0 (Ω)	3.82∠86.5°	3.82∠86.5°

LIST OF PUBLICATIONS & OUTCOMES

Papers published

1. Rui Guan, Ying Xue, and Xiao-Ping Zhang, "Advanced RTDS-based Studies of the Impact of STATCOM on Feeder Distance Protection," *14th International Conference on Development in Power System Protection 2018 (DPSP)*, Belfast, 2018, pp. 1-6.
2. Ying Xue, Dechao Kong, Rui Guan, Can Li, Andrew Taylor, Ray Zhang, Xiao-Ping Zhang, Dilan Jayaweera, "System performance studies in RTDS for a complex power network with multiple FACTS devices," *13th IET International Conference on AC and DC Power Transmission (ACDC 2017)*, Manchester, 2017, pp. 1-6.
3. Can Li, Dechao Kong, Ying Xue, Rui Guan, Andrew Taylor, Ray Zhang, Xiao-Ping Zhang, Dilan Jayaweera, "Enhancement of power system small-signal stability by coordinated damping control of multiple FACTS devices," *13th IET International Conference on AC and DC Power Transmission (ACDC 2017)*, Manchester, 2017, pp. 1-6.

Papers under review/preparation

4. Rui Guan, Na Deng, Ying Xue and Xiao-Ping Zhang, "Small-Signal Stability Analysis of the Interactions between Voltage Sourced Converters and DC Current Flow Controllers," *IEEE Access*, 2018. *(submitted)*
5. Rui Guan, Ying Xue, and Xiao-Ping Zhang, "Impact of STATCOM on Distance Protection for VSC and LCC HVDC Systems Connected Transmission Lines," *IEEE Power and Energy Technology Systems Journal*, 2018. *(under preparation)*

Contribution to report:

6. "A New Independent Methodology for Protection & Control Coordination Studies Using Real Time Digital Simulation (RTDS)," Project Report for National Grid, Mar. 2017.

REFERENCES

[1] S. Cole and R. Belmans, "Transmission of bulk power," *IEEE Industrial Electronics Magazine*, vol. 3, no. 3, pp. 19-24, Sept. 2009.

[2] N. Flourentzou, V. G. Agelidis and G. D. Demetriades, "VSC-Based HVDC Power Transmission Systems: An Overview," *IEEE Transactions on Power Electronics*, vol. 24, no. 3, pp. 592-602, March 2009.

[3] M. P. Bahrman and B. K. Johnson, "The ABCs of HVDC transmission technologies," *IEEE Power and Energy Magazine*, vol. 5, no. 2, pp. 32-44, April 2007.

[4] B. Gemmell, J. Dorn, D. Retzmann and D. Soerangr, "Prospects of multilevel VSC technologies for power transmission," *2008 IEEE/PES Transmission and Distribution Conference and Exposition*, Chicago, IL, 2008, pp. 1-16.

[5] Global Energy Interconnection Development and Cooperation Organization, "Two replacements of strategic vision of GEIDCO," [Online]. Available: http://www.geidco.org/html/qqnycoen/col2015100766/column_2015100766_1.html. Accessed on: Feb.12,2018

[6] P. Kundur, *Power System Stability and Control*. New York: McGraw Hill, 1994.

[7] T. Nakajima and S. Irokawa, "A control system for HVDC transmission by voltage sourced converters," *1999 IEEE Power Engineering Society Summer Meeting. Conference Proceedings (Cat. No.99CH36364)*, Edmonton, Alta., 1999, pp. 1113-1119 vol.2.

[8] S. Lefebvre, W. K. Wong, J. Reeve, J. M. Gagnon and B. K. Johnson, "Experience with modeling MTDC systems in transient stability programs," *IEEE Transactions on Power Delivery*, vol. 6, no. 1, pp. 405-413, Jan 1991.

[9] F. Schettler, H. Huang and N. Christl, "HVDC transmission systems using voltage sourced converters design and applications," *2000 Power Engineering Society Summer Meeting (Cat. No.00CH37134)*, Seattle, WA, 2000, pp. 715-720 vol. 2.

[10] G. P. Adam, K. H. Ahmed, S. J. Finney, K. Bell and B. W. Williams, "New Breed of Network Fault-Tolerant Voltage-Source-Converter HVDC Transmission System," *IEEE Transactions on Power Systems*, vol. 28, no. 1, pp. 335-346, Feb. 2013.

[11] G. Pinares and M. Bongiorno, "Modeling and Analysis of VSC-Based HVDC Systems for DC Network Stability Studies," *IEEE Transactions on Power Delivery*, vol. 31, no. 2, pp. 848-856, April 2016.

[12] C. Osauskas and A. Wood, "Small-signal dynamic modeling of HVDC systems," *IEEE Transactions on Power Delivery*, vol. 18, no. 1, pp. 220-225, Jan 2003.

[13] Z. Chao, Z. Xiaoxin and L. Ruomei, "Dynamic Modeling and Transient Simulation for VSC based HVDC in Multi-Machine System," *2006 International Conference on Power System Technology*, Chongqing, 2006, pp. 1-7.

[14] H. Liu and J. Sun, "Impedance-based stability analysis of VSC-based HVDC systems," *2013 IEEE 14th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Salt Lake City, UT, 2013, pp. 1-8.

[15] L. Zhang, L. Harnefors and H. P. Nee, "Interconnection of Two Very Weak AC Systems by VSC-HVDC Links Using Power-Synchronization Control," *IEEE Transactions on Power Systems*, vol. 26, no. 1, pp. 344-355, Feb. 2011.

[16] L. Zhang, L. Harnefors and H. P. Nee, "Modeling and Control of VSC-HVDC Links Connected to Island Systems," *IEEE Transactions on Power Systems*, vol. 26, no. 2, pp. 783-793, May 2011.

[17] Y. Huang, X. Yuan, J. Hu and P. Zhou, "Modeling of VSC Connected to Weak Grid for Stability Analysis of DC-Link Voltage Control," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 4, pp. 1193-1204, Dec. 2015.

[18] L. Zhang, L. Harnefors and H. P. Nee, "Power-Synchronization Control of Grid-Connected Voltage-Source Converters," *IEEE Transactions on Power Systems*, vol. 25, no. 2, pp. 809-820, May 2010.

[19] T. Lüth, M. M. C. Merlin, T. C. Green, F. Hassan and C. D. Barker, "High-Frequency Operation of a DC/AC/DC System for HVDC Applications," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4107-4115, Aug. 2014.

[20] L. Tang and B. T. Ooi, "Locating and Isolating DC Faults in Multi-Terminal DC Systems," *IEEE Transactions on Power Delivery*, vol. 22, no. 3, pp. 1877-1884, July 2007.

[21] J. Cao, W. Du, H. F. Wang and S. Q. Bu, "Minimization of Transmission Loss in Meshed AC/DC Grids With VSC-MTDC Networks," *IEEE Transactions on Power Systems*, vol. 28, no. 3, pp. 3047-3055, Aug. 2013.

[22] J. Yang, J. E. Fletcher and J. O'Reilly, "Short-Circuit and Ground Fault Analyses and Location in VSC-Based DC Network Cables," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 10, pp. 3827-3837, Oct. 2012.

[23] C. Meyer, M. Hoing, A. Peterson and R. W. De Doncker, "Control and Design of DC Grids for Offshore Wind Farms," *IEEE Transactions on Industry Applications*, vol. 43, no. 6, pp. 1475-1482, Nov.-dec. 2007.

[24] L. Xu, L. Yao and M. Bazargan, "DC grid management of a multi-terminal HVDC transmission system for large offshore wind farms," *2009 International Conference on Sustainable Power Generation and Supply*, Nanjing, 2009, pp. 1-7.

[25] P. F. Ribeiro, B. K. Johnson, M. L. Crow, A. Arsoy and Y. Liu, "Energy storage systems for advanced power applications," *Proceedings of the IEEE*, vol. 89, no. 12, pp. 1744-1756, Dec 2001.

[26] L. Xu and L. Yao, "DC voltage control and power dispatch of a multi-terminal HVDC system for integrating large offshore wind farms," *IET Renewable Power Generation*, vol. 5, no. 3, pp. 223-233, May 2011.

[27] C. Feltes, H. Wrede, F. W. Koch and I. Erlich, "Enhanced Fault Ride-Through Method for Wind Farms Connected to the Grid Through VSC-Based HVDC Transmission," *IEEE Transactions on Power Systems*, vol. 24, no. 3, pp. 1537-1546, Aug. 2009.

[28] L. Xu, L. Yao and C. Sasse, "Grid Integration of Large DFIG-Based Wind Farms Using VSC Transmission," *IEEE Transactions on Power Systems*, vol. 22, no. 3, pp. 976-984, Aug. 2007.

[29] P. Bresesti, W. L. Kling, R. L. Hendriks and R. Vailati, "HVDC Connection of Offshore Wind Farms to the Transmission System," *IEEE Transactions on Energy Conversion*, vol. 22, no. 1, pp. 37-43, March 2007.

[30] D. Van Hertem, M. Ghandhari and M. Delimar, "Technical limitations towards a SuperGrid — A European prospective," *2010 IEEE International Energy Conference*, Manama, 2010, pp. 302-309.

[31] T. K. Vrana, R. E. Torres-Olguin, B. Liu and T. M. Haileselassie, "The North Sea Super Grid - a technical perspective," *9th IET International Conference on AC and DC Power Transmission (ACDC 2010)*, London, 2010, pp. 1-5.

[32] K. Rudion, A. Orths, P. B. Eriksen and Z. A. Styczynski, "Toward a Benchmark test system for the offshore grid in the North Sea," *IEEE PES General Meeting*, Minneapolis, MN, 2010, pp. 1-8.

[33] X. Chen *et al*., "Integrating Wind Farm to the Grid Using Hybrid Multiterminal HVDC Technology," *IEEE Transactions on Industry Applications*, vol. 47, no. 2, pp. 965-972, March-April 2011.

[34] E. Prieto-Araujo, F. Bianchi, A. Junyent-Ferre and O. Gomis-Bellmunt, "Methodology for droop control dynamic analysis of multiterminal VSC-HVDC grids for offshore wind farms," *2014 IEEE PES General Meeting | Conference & Exposition*, National Harbor, MD, 2014, pp. 1-1.

[35] L. Xu, B. W. Williams and L. Yao, "Multi-terminal DC transmission systems for connecting large offshore wind farms," *2008 IEEE Power and Energy Society General Meeting - Conversion and Delivery of Electrical Energy in the 21st Century*, Pittsburgh, PA, 2008, pp. 1-7.

[36] J. Yang, J. E. Fletcher and J. O'Reilly, "Multiterminal DC Wind Farm Collection Grid Internal Fault Analysis and Protection Design," *IEEE Transactions on Power Delivery*, vol. 25, no. 4, pp. 2308-2318, Oct. 2010.

[37] S. M. Muyeen, R. Takahashi and J. Tamura, "Operation and Control of HVDC-Connected Offshore Wind Farm," *IEEE Transactions on Sustainable Energy*, vol. 1, no. 1, pp. 30-37, April 2010.

[38] Weixing Lu and Boon-Teck Ooi, "Optimal acquisition and aggregation of offshore wind power by multiterminal voltage-source HVDC," *IEEE Transactions on Power Delivery*, vol. 18, no. 1, pp. 201-206, Jan 2003.

[39] J. Arrillaga, Liu Yonghe, C. S. Crimp and M. Villablanca, "Harmonic Reduction In Group-Connected Generators-HVDC Convertor," *ICHPS V International Conference on Harmonics in Power Systems.*, 1992, pp. 202-207.

[40] C. Karawita and U. D. Annakkage, "Multi-Infeed HVDC Interaction Studies Using Small-Signal Stability Assessment," *IEEE Transactions on Power Delivery*, vol. 24, no. 2, pp. 910-918, April 2009.

[41] B. R. Andersen, L. Xu and K. T. G. Wong, "Topologies for VSC transmission," *Seventh International Conference on AC-DC Power Transmission*, 2001, pp. 298-304.

[42] Q. Song, W. Liu, X. Li, H. Rao, S. Xu and L. Li, "A Steady-State Analysis Method for a Modular Multilevel Converter," *IEEE Transactions on Power Electronics*, vol. 28, no. 8, pp. 3702-3713, Aug. 2013.

[43] G. T. Son *et al*., "Design and Control of a Modular Multilevel HVDC Converter With Redundant Power Modules for Noninterruptible Energy Transfer," *IEEE Transactions on Power Delivery*, vol. 27, no. 3, pp. 1611-1619, July 2012.

[44] J. Peralta, H. Saad, S. Dennetiere, J. Mahseredjian and S. Nguefeu, "Detailed and averaged models for a 401-level MMC-HVDC system," *2013 IEEE Power & Energy Society General Meeting*, Vancouver, BC, 2013, pp. 1-1.

[45] H. Saad *et al*., "Dynamic Averaged and Simplified Models for MMC-Based HVDC Transmission Systems," *IEEE Transactions on Power Delivery*, vol. 28, no. 3, pp. 1723-1730, July 2013.

[46] M. Saeedifard and R. Iravani, "Dynamic Performance of a Modular Multilevel Back-to-Back HVDC System," *IEEE Transactions on Power Delivery*, vol. 25, no. 4, pp. 2903-2912, Oct. 2010.

[47] U. N. Gnanarathna, A. M. Gole and R. P. Jayasinghe, "Efficient Modeling of Modular Multilevel HVDC Converters (MMC) on Electromagnetic Transient Simulation Programs," *IEEE Transactions on Power Delivery*, vol. 26, no. 1, pp. 316-324, Jan. 2011.

[48] R. Marquardt, "Modular Multilevel Converter: An universal concept for HVDC-Networks and extended DC-Bus-applications," *The 2010 International Power Electronics Conference - ECCE ASIA -*, Sapporo, 2010, pp. 502-507.

[49] M. Guan and Z. Xu, "Modeling and Control of a Modular Multilevel Converter-Based HVDC System Under Unbalanced Grid Conditions," *IEEE Transactions on Power Electronics*, vol. 27, no. 12, pp. 4858-4867, Dec. 2012.

[50] K. Friedrich, "Modern HVDC PLUS application of VSC in Modular Multilevel Converter topology," *2010 IEEE International Symposium on Industrial Electronics*, Bari, 2010, pp. 3807-3810.

[51] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt and S. Kouro, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 2930-2945, Dec. 2007.

[52] Xiao-Ping Zhang, "Multiterminal voltage-sourced converter-based HVDC models for power flow analysis," *IEEE Transactions on Power Systems*, vol. 19, no. 4, pp. 1877-1884, Nov. 2004.

[53] S. Allebrod, R. Hamerski and R. Marquardt, "New transformerless, scalable Modular Multilevel Converters for HVDC-transmission," *2008 IEEE Power Electronics Specialists Conference*, Rhodes, 2008, pp. 174-179.

[54] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard and P. Barbosa, "Operation, Control, and Applications of the Modular Multilevel Converter: A Review," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 37-53, Jan. 2015.

[55] S. Kouro *et al*., "Recent Advances and Industrial Applications of Multilevel Converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553-2580, Aug. 2010.

[56] Y. Cheng, C. Qian, M. L. Crow, S. Pekarek and S. Atcitty, "A Comparison of Diode-Clamped and Cascaded Multilevel Converters for a STATCOM With Energy Storage," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1512-1521, Oct. 2006.

[57] D. Soto and T. C. Green, "A comparison of high-power converter topologies for the implementation of FACTS controllers," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, pp. 1072-1080, Oct 2002.

[58] A. M. Gole and V. K. Sood, "A static compensator model for use with electromagnetic transients simulation programs," *IEEE Transactions on Power Delivery*, vol. 5, no. 3, pp. 1398-1407, Jul 1990.

[59] F. Z. Peng and Jin Wang, "A universal STATCOM with delta-connected cascade multilevel inverter," *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*, 2004, pp. 3529-3533 Vol.5.

[60] P. S. Sensarma, K. R. Padiyar and V. Ramanarayanan, "Analysis and performance evaluation of a distribution STATCOM for compensating voltage fluctuations," *IEEE Transactions on Power Delivery*, vol. 16, no. 2, pp. 259-264, Apr 2001.

[61] N. Mithulananthan, C. A. Canizares, J. Reeve and G. J. Rogers, "Comparison of PSS, SVC, and STATCOM controllers for damping power system oscillations," *IEEE Transactions on Power Systems*, vol. 18, no. 2, pp. 786-792, May 2003.

[62] A. Edris, "FACTS technology development: an update," *IEEE Power Engineering Review*, vol. 20, no. 3, pp. 4-9, Mar 2000.

[63] Q. Song and W. Liu, "Control of a Cascade STATCOM With Star Configuration Under Unbalanced Conditions," *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 45-58, Jan. 2009.

[64] P. Rao, M. L. Crow and Z. Yang, "STATCOM control for power system voltage control applications," *IEEE Transactions on Power Delivery*, vol. 15, no. 4, pp. 1311-1317, Oct 2000.

[65] C. Hochgraf and R. H. Lasseter, "Statcom controls for operation with unbalanced voltages," *IEEE Transactions on Power Delivery*, vol. 13, no. 2, pp. 538-544, Apr 1998.

[66] B. Singh, R. Saha, A. Chandra and K. Al-Haddad, "Static synchronous compensators (STATCOM): a review," *IET Power Electronics*, vol. 2, no. 4, pp. 297-324, July 2009.

[67] Yiqiao Liang and C. O. Nwankpa, "A new type of STATCOM based on cascading voltage source inverters with phase-shifted unipolar SPWM," *Conference Record of 1998 IEEE Industry Applications Conference. Thirty-Third IAS Annual Meeting (Cat. No.98CH36242)*, St. Louis, MO, USA, 1998, pp. 1447-1453 vol.2.

[68] Z. Liu, B. Liu, S. Duan and Y. Kang, "A Novel DC Capacitor Voltage Balance Control Method for Cascade Multilevel STATCOM," *IEEE Transactions on Power Electronics*, vol. 27, no. 1, pp. 14-27, Jan. 2012.

[69] S. Du, J. Liu, J. Lin and Y. He, "A Novel DC Voltage Control Method for STATCOM Based on Hybrid Multilevel H-Bridge Converter," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 101-111, Jan. 2013.

[70] H. Akagi, S. Inoue and T. Yoshii, "Control and Performance of a Transformerless Cascade PWM STATCOM With Star Configuration," *IEEE Transactions on Industry Applications*, vol. 43, no. 4, pp. 1041-1049, July-aug. 2007.

[71] K. R. Padiyar and N. Prabhu, "Design and performance evaluation of subsynchronous damping controller with STATCOM," *IEEE Transactions on Power Delivery*, vol. 21, no. 3, pp. 1398-1405, July 2006.

[72] C. D. Barker and R. S. Whitehouse, "A current flow controller for use in HVDC grids," *10th IET International Conference on AC and DC Power Transmission (ACDC 2012)*, Birmingham, 2012, pp. 1-5.

[73] H. Diab, S. Tennakoon, C. Gould and M. Marei, "An investigation of power flow control methods in multi terminal high voltage DC grids," *2015 50th International Universities Power Engineering Conference (UPEC)*, Stoke on Trent, 2015, pp. 1-5.

[74] K. Rouzbehi, A. Miranian, A. Luna and P. Rodriguez, "DC Voltage Control and Power Sharing in Multiterminal DC Grids Based on Optimal DC Power Flow and Voltage-Droop Strategy," *IEEE Journal of Emerging and Selected Topics in Power*

[75] D. Jovcic and B. T. Ooi, "Developing DC Transmission Networks Using DC Transformers," *IEEE Transactions on Power Delivery*, vol. 25, no. 4, pp. 2535-2543, Oct. 2010.

[76] R. Eriksson, "A New Control Structure for Multiterminal DC Grids to Damp Interarea Oscillations," *IEEE Transactions on Power Delivery*, vol. 31, no. 3, pp. 990-998, June 2016.

[77] N. R. Chaudhuri and B. Chaudhuri, "Adaptive droop control for effective power sharing in multi-terminal DC (MTDC) grids," *2013 IEEE Power & Energy Society General Meeting*, Vancouver, BC, 2013, pp. 1-1.

[78] L. Zhang, H. P. Nee and L. Harnefors, "Analysis of Stability Limitations of a VSC-HVDC Link Using Power-Synchronization Control," *IEEE Transactions on Power Systems*, vol. 26, no. 3, pp. 1326-1337, Aug. 2011.

[79] C. D. Barker and R. Whitehouse, "Autonomous converter control in a multi-terminal HVDC system," *9th IET International Conference on AC and DC Power Transmission (ACDC 2010)*, London, 2010, pp. 1-5.

[80] J. Sun, "Autonomous Local Control and Stability Analysis of Multiterminal DC Systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 4, pp. 1078-1089, Dec. 2015.

[81] K. Rouzbehi, J. I. Candela, A. Luna, G. B. Gharehpetian and P. Rodriguez, "Flexible Control of Power Flow in Multiterminal DC Grids Using DC–DC Converter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 1135-1144, Sept. 2016.

[82] Q. Mu, J. Liang, Y. Li and X. Zhou, "Power flow control devices in DC grids," *2012 IEEE Power and Energy Society General Meeting*, San Diego, CA, 2012, pp. 1-7.

[83] D. Jovcic, M. Hajian, H. Zhang and G. Asplund, "Power flow control in DC transmission grids using mechanical and semiconductor based DC/DC devices," *10th IET International Conference on AC and DC Power Transmission (ACDC 2012)*, Birmingham, 2012, pp. 1-6.

[84] N. Deng, P. Wang, X. P. Zhang, G. Tang and J. Cao, "A DC current flow controller for meshed modular multilevel converter multiterminal HVDC grids," *CSEE Journal of Power and Energy Systems*, vol. 1, no. 1, pp. 43-51, March 2015.

[85] W. Chen, X. Zhu, L. Yao, X. Ruan, Z. Wang and Y. Cao, "An Interline DC Power-Flow Controller (IDCPFC) for Multiterminal HVDC System," *IEEE Transactions on Power Delivery*, vol. 30, no. 4, pp. 2027-2036, Aug. 2015.

[86] N. Deng, P. Wang, and X.-P. Zhang, "Small-signal Stability Analysis and Control System Design of a Meshed Multi-terminal High-Voltage Direct Current Grid with a Current Flow Controller", *Electric Power Components and Systems*, vol. 44, no.10, 1126–1137, 2016.

[87] W. A. Lewis and L. S. Tippett, "Fundamental Basis for Distance Relaying on 3-Phase Systems," *Transactions of the American Institute of Electrical Engineers*, vol. 66, no. 1, pp. 694-709, Jan. 1947.

[88] P. J. Moore, R. K. Aggarwal, H. Jiang and A. T. Johns, "New approach to distance protection for resistive double-phase to earth faults using adaptive techniques," *IEE Proceedings - Generation, Transmission and Distribution*, vol. 141, no. 4, pp. 369-376, Jul 1994.

[89] T. S. Sidhu, R. K. Varma, P. K. Gangadharan, F. A. Albasri and G. R. Ortiz, "Performance of distance relays on shunt-FACTS compensated transmission lines," *IEEE Transactions on Power Delivery*, vol. 20, no. 3, pp. 1837-1845, July 2005.

[90] A. H. Osman and O. P. Malik, "Transmission line distance protection based on wavelet transform," *IEEE Transactions on Power Delivery*, vol. 19, no. 2, pp. 515-523, April 2004.

[91] P. K. Dash, A. K. Pradhan, G. Panda and A. C. Liew, "Adaptive relay setting for flexible AC transmission systems (FACTS)," *2000 IEEE Power Engineering Society Winter Meeting. Conference Proceedings (Cat. No.00CH37077)*, Singapore, 2000, pp. 1855 vol.3-.

[92] Y. Q. Xia, K. K. Li and A. K. David, "Adaptive relay setting for stand-alone digital distance protection," *IEEE Transactions on Power Delivery*, vol. 9, no. 1, pp. 480-491, Jan 1994.

[93] Alstom Grid, Network Protection & Automation Guide Protective Relays, Measurement & Control. Alstom, 2011.

[94] Zhang Zhizhe and Chen Deshu, "An Adaptive Approach in Digital Distance Protection," *IEEE Power Engineering Review*, vol. 11, no. 1, pp. 44-, January 1991.

[95] P. A. Crossley and P. G. McLaren, "Distance Protection Based on Travelling Waves," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-102, no. 9, pp. 2971-2983, Sept. 1983.

[96] C. Pang and M. Kezunovic, "Fast Distance Relay Scheme for Detecting Symmetrical Fault During Power Swing," *IEEE Transactions on Power Delivery*, vol. 25, no. 4, pp. 2205-2212, Oct. 2010.

[97] K. Seethalekshmi, S. N. Singh and S. C. Srivastava, "A Classification Approach Using Support Vector Machines to Prevent Distance Relay Maloperation Under Power Swing and Voltage Instability," *IEEE Transactions on Power Delivery*, vol. 27, no. 3, pp. 1124-1133, July 2012.

[98] Z. Y. Xu *et al.*, "A Distance Protection Relay for a 1000-kV UHV Transmission Line," *IEEE Transactions on Power Delivery*, vol. 23, no. 4, pp. 1795-1804, Oct. 2008.

[99] S. Jamali, "A fast adaptive digital distance protection," *2001 Seventh International Conference on Developments in Power System Protection (IEE)*, Amsterdam, 2001, pp. 149-152.

[100] M. M. Eissa and M. Masoud, "A novel digital distance relaying technique for transmission line protection," *IEEE Transactions on Power Delivery*, vol. 16, no. 3, pp. 380-384, Jul 2001.

[101] A. G. Jongepier and L. van der Sluis, "Adaptive distance protection of a double-circuit line," *IEEE Transactions on Power Delivery*, vol. 9, no. 3, pp. 1289-1297, Jul 1994.

[102] C. Schauder and H. Mehta, "Vector analysis and control of advanced static VAr compensators," *IEE Proc. C Gen. Trans. Distrib.*, vol. 140, pp. 299–306, Jul. 1993.

[103] I. Papic, P. Zunko, D. Povh, and M. Weinhold, "Basic control of unified power flow controller," *IEEE Trans. Power Syst., vol. 12*, pp. 1734–1739, Nov. 1997.

[104] T. M. Haileselassie, "Control, dynamics and operation of multi-terminal VSC-HVDC transmission systems," *Ph.D. dissertation, Norwegian University of Science and Technology*, Trondheim, Norway, 2012.

[105] T. M. Haileselassie and K. Uhlen, "Power system security in a meshed north sea HVDC grid," *Proc. IEEE*, vol. 101, no. 4, pp. 978–990, Feb. 2013.

[106] C. Dierckxsens, K. Srivastava, M. Reza, S. Cole, J. Beerten, and R. Belmans, "A distributed DC voltage *control method for VSC MTDC systems," Elect. Power Syst. Res.*, vol. 82, no. 1, pp. 54–58, Jan. 2012.

[107] *K. Ou, H. Rao, Z. Cai, H. Guo, X. Lin, L. Guan, T. Maguire, B. Warkentin, and Y. Chen, "MMC-HVDC simulation and testing based on real-time digital simulator and physical control system," IEEE J. Emerging and Selected Topics in Power Electron.,* vol. 2, no. 4, pp. 1109–1116, Dec. 2014.

[108] *J. Cao, W. Du, H. F. Wang, and S. Q. Bu, "Minimization of transmission loss in meshed AC/DC grids with VSC-MTDC networks," IEEE Trans. Power Syst.,* vol. 28, no. 3, pp. 3047–3055, Aug. 2013.

[109] *N. Yousefpoor, S. Kim, and S. Bhattacharya, "Multi-terminal DC grid control under loss of terminal* station," *IEEE Energy Conv. Cong. Exposition (ECCE*), Sept. 2014, pp. 744–749.

[110] C. K. Lee, J. S. K. Leung, S. Y. R. Hui and H. S. H. Chung, "Circuit-level comparison of STATCOM technologies," *IEEE Transactions on Power Electronics*, vol. 18, no. 4, pp. 1084-1092, July 2003.

[111] D. Basic, M. Geske, J. Janning and S. Schröder, "Injection capability of delta connected STATCOM in imbalanced situations," *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Karlsruhe, 2016, pp. 1-10.

[112] A. H. Norouzi and A. M. Sharaf, "Two control schemes to enhance the dynamic performance of the STATCOM and SSSC," *IEEE Transactions on Power Delivery*, vol. 20, no. 1, pp. 435-442, Jan. 2005.

[113] M. S. El-Moursi, B. Bak-Jensen and M. H. Abdel-Rahman, "Novel STATCOM Controller for Mitigating SSR and Damping Power System Oscillations in a Series Compensated Wind Park," *IEEE Transactions on Power Electronics*, vol. 25, no. 2, pp. 429-441, Feb. 2010.

[114] M. Hagiwara, R. Maeda and H. Akagi, "Negative-Sequence Reactive-Power Control by a PWM STATCOM Based on a Modular Multilevel Cascade Converter (MMCC-SDBC)," *IEEE Transactions on Industry Applications*, vol. 48, no. 2, pp. 720-729, March-April 2012.

[115] Z. He *et al.*, "Reactive Power Strategy of Cascaded Delta-Connected STATCOM Under Asymmetrical Voltage Conditions," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 2, pp. 784-795, June 2017.

[116] C. Han *et al*., "STATCOM Impact Study on the Integration of a Large Wind Farm into a Weak Loop Power System," *IEEE Transactions on Energy Conversion*, vol. 23, no. 1, pp. 226-233, March 2008.

[117] B. Singh, S. S. Murthy and S. Gupta, "STATCOM-Based Voltage Regulator for Self-Excited Induction Generator Feeding Nonlinear Loads," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1437-1452, Oct. 2006.

[118] A. Jain, K. Joshi, A. Behal and N. Mohan, "Voltage regulation with STATCOMs: modeling, control and results," *IEEE Transactions on Power Delivery*, vol. 21, no. 2, pp. 726-735, April 2006.

[119] G. Kish, R. Shi and P. Lehn, "The delta configured modular multilevel converter," *2016 IEEE Power and Energy Society General Meeting (PESGM)*, Boston, MA, 2016, pp. 1-1.

[120] P. Sochor and H. Akagi, "Theoretical Comparison in Energy-Balancing Capability Between Star- and Delta-Configured Modular Multilevel Cascade Inverters for Utility-Scale Photovoltaic Systems," *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 1980-1992, March 2016.

[121] H. M. P. and M. T. Bina, "A Transformerless Medium-Voltage STATCOM Topology Based on Extended Modular Multilevel Converters," *IEEE Transactions on Power Electronics*, vol. 26, no. 5, pp. 1534-1545, May 2011.

[122] B. Gultekin and M. Ermis, "Cascaded Multilevel Converter-Based Transmission STATCOM: System Design Methodology and Development of a 12 kV ±12 MVAr Power Stage," *IEEE Transactions on Power Electronics*, vol. 28, no. 11, pp. 4930-4950, Nov. 2013.

[123] W. Song and A. Q. Huang, "Fault-Tolerant Design and Control Strategy for Cascaded H-Bridge Multilevel Converter-Based STATCOM," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2700-2708, Aug. 2010.

[124] J. A. Barrena, L. Marroyo, M. Á. Rodriguez Vidal and J. R. Torrealday Apraiz, "Individual Voltage Balancing Strategy for PWM Cascaded H-Bridge Converter-Based STATCOM," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 1, pp. 21-29, Jan. 2008.

[125] Yiqiang Chen, B. Mwinyiwiwa, Z. Wolanski and Boon-Teck Ooi, "Regulating and equalizing DC capacitance voltages in multilevel STATCOM," *IEEE Transactions on Power Delivery*, vol. 12, no. 2, pp. 901-907, Apr 1997.

[126] Xiao-Ping Zhang, "Multiterminal voltage-sourced converter-based HVDC models for power flow analysis," *IEEE Transactions on Power Systems*, vol. 19, no. 4, pp. 1877-1884, Nov. 2004.

[127] R. Preece and J. V. Milanović, "Tuning of a Damping Controller for Multiterminal VSC-HVDC Grids Using the Probabilistic Collocation Method," *IEEE Trans. Power Del*., vol. 29, no. 1, pp. 318-326, Feb. 2014.

[128] R. Teixeira Pinto, P. Bauer, S. F. Rodrigues, E. J. Wiggelinkhuizen, J. Pierik and B. Ferreira, "A Novel Distributed Direct-Voltage Control Strategy for Grid Integration of Offshore Wind Energy Systems Through MTDC Network," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 6, pp. 2429-2441, June 2013.

[129] J. Beerten, S. Cole and R. Belmans, "A sequential AC/DC power flow algorithm for networks containing Multi-terminal VSC HVDC systems," *IEEE PES General Meeting*, Minneapolis, MN, 2010, pp. 1-7.

[130] S. Cole, J. Beerten and R. Belmans, "Generalized Dynamic VSC MTDC Model for Power System Stability Studies," *IEEE Transactions on Power Systems*, vol. 25, no. 3, pp. 1655-1662, Aug. 2010.

[131] J. Beerten, S. Cole and R. Belmans, "Generalized steady-state VSC MTDC model for sequential AC/DC power flow algorithms," *2013 IEEE Power & Energy Society General Meeting*, Vancouver, BC, 2013, pp. 1-1.

[132] J. Beerten, S. D'Arco and J. A. Suul, "Identification and small-signal analysis of interaction modes in VSC MTDC systems," *2016 IEEE Power and Energy Society General Meeting (PESGM)*, Boston, MA, 2016, pp. 1-1.

[133] J. Z. Zhou, H. Ding, S. Fan, Y. Zhang and A. M. Gole, "Impact of Short-Circuit Ratio and Phase-Locked-Loop Parameters on the Small-Signal Behavior of a VSC-HVDC Converter," *IEEE Transactions on Power Delivery*, vol. 29, no. 5, pp. 2287-2296, Oct. 2014.

[134] P. Rault, F. Colas, X. Guillaud and S. Nguefeu, "Method for small signal stability analysis of VSC-MTDC grids," *2012 IEEE Power and Energy Society General Meeting*, San Diego, CA, 2012, pp. 1-7.

[135] N. R. Chaudhuri, R. Majumder, B. Chaudhuri, J. Pan and R. Nuqui, "Modeling and stability analysis of MTDC grids for offshore wind farms: A case study on the North Sea benchmark system," *2011 IEEE Power and Energy Society General Meeting*, San Diego, CA, 2011, pp. 1-7.

[136] H. Yuan, X. Yuan and J. Hu, "Modeling of Grid-Connected VSCs for Power System Small-Signal Stability Analysis in DC-Link Voltage Control Timescale," *IEEE Transactions on Power Systems*, vol. 32, no. 5, pp. 3981-3991, Sept. 2017.

[137] J. Beerten, S. Cole and R. Belmans, "Modeling of Multi-Terminal VSC HVDC Systems With Distributed DC Voltage Control," *IEEE Transactions on Power Systems*, vol. 29, no. 1, pp. 34-42, Jan. 2014.

[138] Xiao-Ping Zhang, "Multiterminal voltage-sourced converter-based HVDC models for power flow analysis," *IEEE Transactions on Power Systems*, vol. 19, no. 4, pp. 1877-1884, Nov. 2004.

[139] G. O. Kalcon, G. P. Adam, O. Anaya-Lara, S. Lo and K. Uhlen, "Small-Signal Stability Analysis of Multi-Terminal VSC-Based DC Transmission Systems," *IEEE Transactions on Power Systems*, vol. 27, no. 4, pp. 1818-1830, Nov. 2012.

[140] N. R. Chaudhuri, R. Majumder and B. Chaudhuri, "Stability analysis of VSC MTDC grids connected to multimachine ac systems," *2012 IEEE Power and Energy Society General Meeting*, San Diego, CA, 2012, pp. 1-1.

[141] N. R. Chaudhuri, R. Majumder and B. Chaudhuri, "System frequency support through multi-terminal DC (MTDC) grids," *2013 IEEE Power & Energy Society General Meeting*, Vancouver, BC, 2013, pp. 1-1.

[142] J. Beerten, G. B. Diaz, S. D'Arco and J. A. Suul, "Comparison of small-signal dynamics in MMC and two-level VSC HVDC transmission schemes," *2016 IEEE International Energy Conference (ENERGYCON)*, Leuven, 2016, pp. 1-6.

[143] M. Sultan, J. Reeve and R. Adapa, "Combined transient and dynamic analysis of HVDC and FACTS systems," *IEEE Transactions on Power Delivery*, vol. 13, no. 4, pp. 1271-1277, Oct 1998.

[144] L. Wang and K. H. Wang, "Dynamic Stability Analysis of a DFIG-Based Offshore Wind Farm Connected to a Power Grid Through an HVDC Link," *IEEE Transactions on Power Systems*, vol. 26, no. 3, pp. 1501-1510, Aug. 2011.

[145] T. M. Haileselassie and K. Uhlen, "Impact of DC Line Voltage Drops on Power Flow of MTDC Using Droop Control," *IEEE Transactions on Power Systems*, vol. 27, no. 3, pp. 1441-1449, Aug. 2012.

[146] S. Liu, Z. Xu, W. Hua, G. Tang and Y. Xue, "Electromechanical Transient Modeling of Modular Multilevel Converter Based Multi-Terminal HVDC Systems," *IEEE Transactions on Power Systems*, vol. 29, no. 1, pp. 72-83, Jan. 2014.

[147] P. Kundur *et al*., "Definition and classification of power system stability IEEE/CIGRE joint task force on stability terms and definitions," *IEEE Transactions on Power Systems*, vol. 19, no. 3, pp. 1387-1401, Aug. 2004.

[148] B. Pal and B. Chaudhuri, Robust Control in Power Systems. New York, NY, USA: Springer-Verlag, 2005.

[149] P. W. Sauer and M. A. Pai, Power System Dynamics and Stability.Englewood Cliffs, NJ: Prentice–Hall, 1998.

[150] J. Arrillaga, High Voltage Direct Current Transmission. London, U.K.: Inst. Electr. Eng., 1998.

[151] S. D'Arco, J. Beerten and J. A. Suul, "Classification and analysis of impact on small-signal dynamics and stability from expansion of VSC-HVDC systems to multi-terminal HVDC grids," *13th IET International Conference on AC and DC Power Transmission (ACDC 2017)*, Manchester, 2017, pp. 1-8.

[152] Y. Huang, D. Wang, L. Shang, G. Zhu, H. Tang and Y. Li, "Modeling and Stability Analysis of DC-Link Voltage Control in Multi-VSCs With Integrated to Weak Grid," *IEEE Transactions on Energy Conversion*, vol. 32, no. 3, pp. 1127-1138, Sept. 2017.

[153] P. Rault, F. Colas, X. Guillaud and S. Nguefeu, "Method for small signal stability analysis of VSC-MTDC grids," *2012 IEEE Power and Energy Society General Meeting*, San Diego, CA, 2012, pp. 1-7.

[154] A. Salemnia, M. Khederzadeh and A. Ghorbani, "Impact of static synchronous compensator (STATCOM) on performance of distance relay," *2009 IEEE Bucharest PowerTech*, Bucharest, 2009, pp. 1-8.

[155] F. A. Albasri, T. S. Sidhu and R. K. Varma, "Performance Comparison of Distance Protection Schemes for Shunt-FACTS Compensated Transmission Lines," *IEEE Transactions on Power Delivery*, vol. 22, no. 4, pp. 2116-2125, Oct. 2007.

[156] M. Khederzadeh and A. Ghorbani, "Impact of VSC-Based Multiline FACTS Controllers on Distance Protection of Transmission Lines," *IEEE Transactions on Power Delivery*, vol. 27, no. 1, pp. 32-39, Jan. 2012

[157] A. Kazemi, S. Jamali and H. Shateri, "Adaptive distance protection in presence of STATCOM on a transmission line," *IEEE PES T&D 2010*, New Orleans, LA, USA, 2010, pp. 1-6.

[158] R. Dubey, S. R. Samantaray and B. K. Panigrahi, "Adaptive distance protection scheme for shunt-FACTS compensated line connecting wind farm," *IET Generation, Transmission & Distribution*, vol. 10, no. 1, pp. 247-256, 1 7 2016.

[159] A. R. Singh, N. R. Patne, V. S. Kale and P. Khadke, "Digital impedance pilot relaying scheme for STATCOM compensated TL for fault phase classification with fault location," *IET Generation, Transmission & Distribution*, vol. 11, no. 10, pp. 2586-2598, 7 13 2017.

[160] J. Zhang, J. Suonan, Z. Jiao, G. Song and X. Su, "A Fast Full-Line Tripping Distance Protection Method for HVDC Transmission Line," *2012 Asia-Pacific Power and Energy Engineering Conference*, Shanghai, 2012, pp. 1-5.

[161] J. Suonan, J. Zhang, Z. Jiao, L. Yang and G. Song, "Distance Protection for HVDC Transmission Lines Considering Frequency-Dependent Parameters," *IEEE Transactions on Power Delivery*, vol. 28, no. 2, pp. 723-732, April 2013.

[162] M. Zolfaghari, R. M. Chabanlo, M. Abedi and M. Shahidehpour, "A Robust Distance Protection Approach for Bulk AC Power System Considering the Effects of HVDC Interfaced Offshore Wind Units," *IEEE Systems Journal*, vol. PP, no. 99, pp. 1-10.

[163] P. Tünnerhoff, C. Petino, M. Battiato and A. Schnettler, "Distance protection for HVDC transmission lines based on MMC modulation strategy," *2016 Electric Power Quality and Supply Reliability (PQ)*, Tallinn, 2016, pp. 283-288.

[164] L. He, C. C. Liu, A. Pitto and D. Cirio, "Distance Protection of AC Grid With HVDC-Connected Offshore Wind Generators," *IEEE Transactions on Power Delivery*, vol. 29, no. 2, pp. 493-501, April 2014.

[165] C. C. Teixeira and H. Leite, "The influence of a VSC based HVDC link on distance protection relay assessed by CAPE software," *2017 IEEE Manchester PowerTech*, Manchester, 2017, pp. 1-4.

[166] L. Shen, M. Barnes and J. V. Milanović, "Interactions between STATCOM and VSC HVDC in dynamic GB system," *7th IET International Conference on Power Electronics, Machines and Drives (PEMD 2014)*, Manchester, 2014, pp. 1-6.

[167] L. Shen, M. Barnes, J. V. Milanovic, K. R. W. Bell and M. Belivanis, "Potential interactions between VSC HVDC and STATCOM," *2014 Power Systems Computation Conference*, Wroclaw, 2014, pp. 1-7.

[168] D. Kong, A. Taylor, Y. Xue and X. P. Zhang, "A new independent methodology for protection and control coordination studies using real time digital simulation," *13th International Conference on Development in Power System Protection 2016 (DPSP)*,