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PHD

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Partridge, James G.

Award date:
2000

Awarding institution:
University of Bath

[Link to publication](#)
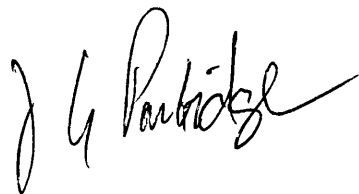
A MEMS APPROACH TO SUBMILLIMETRE-WAVE FREQUENCY MULTIPLIER DESIGN.

Submitted by James G. Partridge

for the degree of PhD

of the University of Bath

2000

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UMI Number: U601746

UMI U601746

Abstract

This thesis describes an investigation into micromachined integrated submillimetre wave components. The main focus of the work has been on the development of a micromachined frequency tripler (output frequency 810GHz) based on a Schottky varactor diode with a novel integrated device contact. The associated design and fabrication methods are described. Due to the lack of availability of a suitable pump source, RF measurements were not possible within the duration of the project. A micromachined frequency doubler operating with lower fundamental input frequency will undergo RF testing in the near future. Passive components including tuning stubs and rectangular waveguide bandpass filters have been fabricated using Epon SU8 epoxy resist. Transmission tests were performed on micromachined D-band waveguides and iris-coupled waveguide filters with pass-band centre frequencies of 135GHz.

Contents

1. Introduction

The first pages of this introductory chapter aim to describe existing and proposed applications of terahertz frequency systems. The techniques used to machine these components are described in section 1.2 and typical components are illustrated. An overview of MEMS (Micro-Electro-Mechanical-Structures) then follows, since this technology has provided the necessary methods for forming many of the structures featured in this thesis. Finally, a summary of the contents of the remaining chapters is provided.

1.1 Application of terahertz frequency techniques

Radioastronomy

The developing fields of submillimetre and terahertz astronomy depend upon sensitive receivers, large accurate telescopes and good ground-based or space-borne observing platforms. This part of the spectrum is important for studies of the early stages of star formation in interstellar molecular clouds and nearby galaxies, and for observations of the cosmic background radiation [1].

For astronomical and remote sensing applications, the lowest noise and highest sensitivity is usually required, often necessitating the use of cooled detectors. For molecular line astronomy, high spectral resolution ($f/\Delta f \sim 10^6$) is also needed. Submillimetre-wave spectroscopy can be used to study spectral lines occurring due to rotational transitions of simple molecules, such as ^{12}CO, ^{13}CO, HCO^+, CN and many others found in the interstellar medium. Such molecules are normally found in trace ($< 10^{-4}$) quantities, embedded in interstellar clouds of molecular hydrogen. Detailed analysis of the spectral line shapes can be used to determine, for example, temperatures, densities and motions of the material making up the molecular cloud. Physical and chemical models representing conditions within the cloud can be built up through observations of differing molecular species and of different transitions of the same molecular species. Different molecular species will tend to have different degrees of opacity (optical depth) to the electromagnetic radiation; observations made of different species can often be used to trace out gas distribution in different parts of

the cloud. Observations of different transitions of the same molecular species can be used to determine the state of excitation of that species within the cloud. Simple rotational spectra of linear molecules are characterised by a series of harmonically related frequencies, given by $f = Jh / 4 \pi^2 I$, where J is an integer, h is Planck's constant and I is the molecular moment of inertia. Thus, observations of higher transition lines at higher frequencies can be used to probe regions of high excitation.

Diffuse molecular clouds collapse under their self-gravitational attraction. Gravitational instability can lead to the formation of clumps of material within the cloud, out of which protostars are formed. The ionization by ultra-violet radiation and cosmic rays of atoms and molecules within these regions leads to a complex chemistry. Of key importance in understanding this chemistry is the study of carbon, both in atomic form (e.g. as neutral carbon CI) and in molecular form (e.g. as CO).

Recently, much attention has been given to the study of neutral carbon in molecular clouds. Observations of the $^3P_1 \rightarrow {}^3P_0$ transition of CI at 492GHz have shown that its distribution is widespread in interstellar molecular clouds [2] and external galaxies [3]. At 492GHz, CI has been readily detected in cold clouds, intermediate and high-mass clouds, bipolar outflows, carbon stars, shocked regions near supernovae and in external galaxies. The state of excitation is not established by observation of a single spectral line. CI in cool / tenuous regions congregates in the $^3P_0$ ground state, producing high optical depth in the $^3P_1 \rightarrow {}^3P_0$ transition. When studying rotational spectra of molecules such as CO, it is customary to observe the optically thin lines of the weaker isomer ^{13}C. At 492GHz, the ^{13}C isotopic $^3P_1 \rightarrow {}^3P_0$ fine structure line lies only 1.6MHz away from the ^{12}C line and cannot be resolved; the ^{13}C 809GHz line has components up to 220MHz away. Complementary observations of the $^3P_2 \rightarrow {}^3P_1$ transition of CI at 809GHz would permit its state of excitation to be established and would also probe deeper into cool cloud cores.

The development of instrumentation for millimetre-wave astronomy is now fairly mature. It is important that technologies suitable for terahertz astronomy are similarly developed.

A number of ground based submillimetre telescopes are either in operation e.g. the James Clerk Maxwell Telescope (JCMT) and the Caltech Submillimeter Observatory, or under construction e.g. the SubMillimeter Array (SMA) of the Smithsonian Astrophysical Observatory. There are several space-borne missions planned by both ESA and NASA to carry submillimetre heterodyne receivers both for astronomy, e.g. FIRST (500-2000GHz), SMIM (400-1200GHz), LDR (300-3000GHz), and for remote sensing e.g. SOPRANO (500-1000GHz) and EOS-MLS (to 2.5THz).

Completed in 1987, the 15m diameter James Clerk Maxwell Telescope (JCMT) is still the world's largest facility designed specifically to operate in the sub-mm region of the spectrum. It is situated close to the summit of Mauna Kea, Hawaii, at an altitude of 4092m. At this height the telescope is above 97% of the water held in the atmosphere.

The JCMT operates facility heterodyne instruments [4] in four bands, A (215-275 GHz) [5], B (318-373GHz), C (430-510GHz) and D (630-710GHz). Major objects of study include stars in their earliest stages of formation, where they are surrounded by gas and dust disks that have not yet coallessed to form planets. Also taking up large amounts of telescope time are observations of extra-galactic objects. These studies are looking at overall star formation rates in different types of galaxies ranging from nearby to objects exhibiting high red-shift.

The space-borne Far InfraRed and Submillimetre Telescope (FIRST) is planned for launch in 2007 and carries the Heterodyne Instrument for *FIRST* (*HIFI*). This will cover at least the frequency range 492GHz to 1113GHz and will provide sensitive observations with resolving powers ranging from less than 5×10^5 to 1.2×10^7. The instrument is optimised for the measurement of weak, broad spectral lines of distant galaxies and for performing fast line surveys of galactic objects [6].

SOFIA, the Stratospheric Observatory For Infrared Astronomy is a NASA operated Boeing 747 mounted high altitude telescope [7]. CASIMIR (CAltech Submillimeter and far-Infrared MIxing Receiver) is the submillimeter and far-infrared heterodyne receiver for SOFIA. This instrument will be used to study a wide range of astrophysical problems ranging from the evolution of galaxies to the birth and death

of stars. The goal is to cover the 500-2100GHz frequency range in seven bands: SIS mixers in four bands up to 1200GHz, and HEB mixers in three bands covering 1200-2100GHz.

Atmospheric remote sensing

Absorption or emission lines corresponding to certain molecules in the Earth's atmosphere can be used to measure the density of these molecules or related parameters including temperature and pressure [8, 9]. Two methods are employed for attaining this data

1)   Looking vertically through the atmosphere from ground based receivers.

2)   Looking tangentially through the upper atmosphere with varying inclination, using satellite based receivers.

The latter method (known as limb-sounding), is a proven choice for observations investigating chemical and physical processes involved in ozone depletion and other reactions caused by air pollution. Many spectral lines that are observable at high altitude are not visible to ground based telescopes. The altitude range over which these measurements are made is typically 15-85km. In NASA's Upper Atmosphere Research Satellite (UARS) a multichannel instrument (63, 183 and 205GHz) is designed to measure ClO (25-45km), O_3 (15-80km) and H_2O (15-85km) combined with pressure calculated from O_2 emission [10]. The European Submillimetre wave Atmospheric Sounder (SUMAS) has been operated on board a research aircraft at 10km. This instrument is equipped to measure, amongst others, the ClO molecular emission line at 649GHz [11].

Chemical and biological warfare agent detection

Terahertz technology is still waiting for a mass-market application. A possible first step in this direction comes from the defence market. In a paper by Woolard [12], terahertz spectroscopy is discussed with defensive military applications in mind.

The recent proliferation of chemical and biological agents as instruments of warfare and terrorism has lead the US Department of Defence to show considerable interest in the development of early warning systems for these agents. Very recent spectroscopic studies at millimetre- and submillimetre-wave have indicated that DNA (and possibly other cellular material) possesses large numbers of unique resonances due to localised

phonon modes. Data is presented in [12] showing that in the 300-750GHz frequency range, unique contributions are visible from these localised phonons, arising from DNA base-pair interactions. These contributions are absent from far infrared data.

Technological challenges must be met before terahertz early warning systems are viable but considerable advancement of the terahertz field would almost certainly result from military backing.

Secure communications

The internet and mobile communications have become increasingly important as communications media in the modern world. There will continue to be an increasing demand for more services, faster access, combined with mobility and flexibility. The potential for submillimetre-wave wireless communication networks is very real. Certain applications can make use of the strong atmospheric absorption that occurs in parts of the millimetre and submillimetre spectrum. The high absorption and narrow beamwidths make these wavelengths well suited to applications such as covert, intra-building, high-speed, wireless communication links

Plasma diagnostics

By measuring the phase shift, absorption and scattering of millimetre wave radiation propagated through a plasma, it is possible to deduce the electron density and temperature of the plasma [13]. There is a region of extinction below a certain critical frequency (f_p) which is dependant on the electron density (ρ_e) such that

$$(f_p) = 8.974 \ \sqrt{\rho_e} \ \text{Hz}. \tag{1.1}$$

When electron densities reach 10^{15} electrons/cm^3, the critical frequency falls into the submillimetre wave range. An example application is within a Tokamak fusion reactor, where the plasma has a critical frequency within the submillimetre range and therefore requires a diagnostic system with an operating frequency exceeding this minimum [14].

Suzuki et al. [15] describe a fabrication process for submillimeter-wave detecting and mixing diodes with plasma diagnostics as a primary application. The devices are designed to exhibit low noise particularly in the image frequency (IF) range of plasma diagnostic systems (below 10MHz).

Mass market potential

Applications further down the frequency range (~100GHz) include vehicle avoidance systems and imaging systems to identify plastic guns and explosives in non-invasive security installations. In communications systems, higher frequencies offer greater bandwidth and speed (100s of megabits per second), higher antenna gain for a given antenna size, narrower antenna beam widths and smaller system size. If these applications are to be fully exploited inexpensive and reliable components and systems are necessary.

1.2   Available technology

The terahertz frequency region, usually defined as ranging from 100GHz-10THz, has not yet been opened up for commercial exploitation. One reason for this is the lack of availability of small solid-state power sources that operate at these frequencies. In addition, the technology required to form passive circuit components is expensive and time consuming. Addressing the source availability problem first, the following section describes current limits on devices that may have potential for future application in the submillimetre region.

1.2.1   Solid state sources

Above 10THz the 'optical' region begins and is supported with developed devices such as near infra-red lasers and LEDs. Below this frequency point and above 250GHz, there is a region where useable solid-state sources do not exist [16]. A 712GHz RTD source [17] has been tested but the output power at that frequency was less than $1\mu W$. This falls short of the few hundred microwatts required for the most sensitive mixers operating at that frequency.

Gunn diodes

Gunn diodes are the standard choice for many millimetre-wave local oscillator applications and when allied to frequency multipliers can supply sufficient power for mixers operating at terahertz frequencies.

Fundamental to the operation of Gunn diode oscillators is the Negative Differential Region (NDR) in their IV characteristic. Tuning of the external circuit can change the resonant frequency of these transit-time devices and various modes of operation are

possible. DC to RF conversion efficiencies in the region of 1.2% have been reported for devices with operating frequencies exceeding 100GHz [18, 19].

State of the art performance of Gunn diodes has been achieved using n+/n/n+ structures with graded doping profiles. Attention paid to effective heat sinking has also proved valuable in optimising operating characteristics. Employing harmonic frequency generation has extended the upper frequency limit of these devices and output powers in the region of 1mW have been demonstrated at about 200GHz [20].

Field Effect Transistors (FETs)

This range of devices includes MESFETS (Metal Semiconductor FETs), HEMTS (High Electron MobilityTransistors) and pHEMTS (pseudomorphic High Electron Mobility Transistors). Recent developments in HEMT type structures indicate that they have the potential to operate in the terahertz region. Integrated circuits based on pHEMTS have been demonstrated at 140GHz and maximum operating frequencies of 800GHz are predicted [21]. As these devices are decreased in size in order to function at higher frequencies the demands on their fabrication processes become the limiting factor. Advances are continually being made in this area but these devices are subject to a $1/f^2$ power scaling (common to all transit-time devices) that probably means signal processing will be a target application rather than power generation.

Heterojunction Bipolar Transistors (HBTs)

The cut-off frequencies for HBTs have not reached those of FET devices. Minimising the base width in these devices causes a reduction in surface recombination and increases the maximum operating frequency. With a base width of 5nm, the limit is now around 170GHz. It is unlikely then that the HBT will be considered over field effect devices for terahertz applications.

The vertical structure of the HBT does mean that multiple finger configurations can be implemented to increase device area and improve power handling. With this in mind the device is being considered for driving frequency multipliers.

Resonant Tunnelling Diodes (RTDs)

The resonant tunneling diode is a promising device for generating signals in the millimeter and submillimeter wave regions. However, the RTD has two problems. The first of these is its low output power. The second difficulty is that undesirable low frequency spurious oscillations often result from the RTD's inherently broadband negative differential resistance (NDR). To get more power, one solution is coherent power combining of multi-RTD's using a quasi-optical resonator.

A Fabry-Perot resonator with a grating has been reported for coherent power combining of a RTD array in the millimetre wave region [22]. Coherent power combining with two RTD's in the resonator was successfully observed at 75GHz. The authors have demonstrated a series configuration as a means to eliminate unwanted low frequency spurious oscillations and present some preliminary results.

1.2.2 The requirement for frequency multipliers

Whilst continual improvement is being made in the fabrication technologies and maximum operating frequencies of the devices described in the previous section, there still exists a gap between 300GHz and 10THz where frequency multiplication is the only means of providing appreciable signal power. Frequency multipliers have been demonstrated up to and beyond 1THz [23, 24] and as such represent a vital means to bridge the terahertz gap. Section 1.3 provides an overview of heterodyne detection. The mechanical aspects of a frequency multiplier are reviewed in section 1.5.

1.3   Basic receiver systems

Figure 1.1 illustrates a simple heterodyne receiver system in block diagram form. The input signal is collected by the antenna and fed to the input of the mixer. A local oscillator (LO) signal is also fed to the input of the mixer and through non-linear mixing, difference and product frequencies are generated. The solid-state device chosen to perform the role of local oscillator is usually a Gunn diode, in which case the LO frequency will be limited to a maximum 160-200GHz and more typically around 100GHz. Receivers operating above 100GHz will normally feature diode frequency multipliers in the LO section.
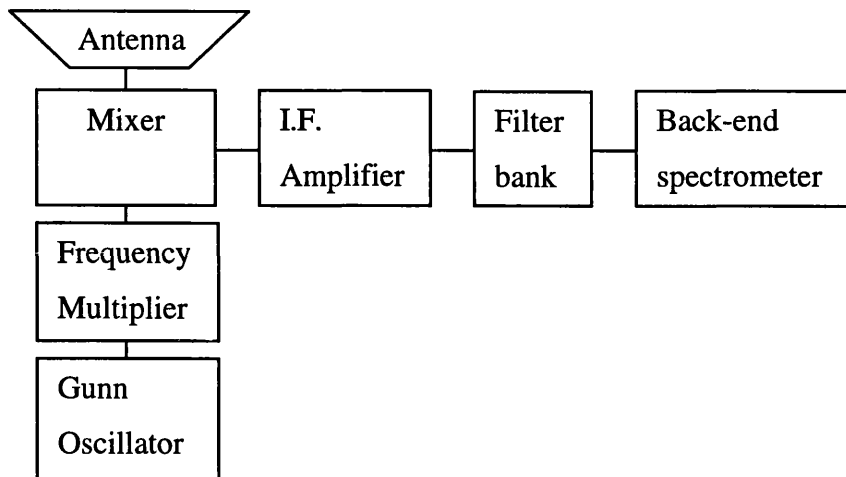
Figure 1.1. Simple Heterodyne Receiver.

Assuming sufficient power is available from the LO chain, power at the mixer Intermediate Frequency (IF) is amplified and detected at the back-end spectrometer. At terahertz frequencies two distinct mixer types are available and these are described in the next sections. A brief description of the operation of a varactor as a frequency-multiplying device is given in section 1.3.3 with a more detailed analysis to be found in chapter two.

1.3.1 Schottky barrier diode mixer receivers

Here, the incoming signal is mixed with the local oscillator using the non-linear I-V relation of a small-area GaAs Schottky barrier diode. At lower frequencies (< 500 GHz) the devices are normally waveguide mounted. Sliding tuners are conventionally used to optimise the embedding impedance seen by the diode. At higher frequencies, devices have traditionally been mounted in open-structure mounts, such as corner-cube reflectors, although the upper frequency limit on waveguide mount technology is being extended. Waveguide mounts permit the use of high quality corrugated feedhorns to couple radiation into the mixer. An extremely symmetric and well-defined beam pattern is critical in astronomy and remote sensing applications.

At higher frequencies (> 1 THz), GaAs Schottky diodes are the only currently viable mixer devices proven to operate satisfactorily. Diode mixers offer a well-established technology. The main limitations to the performance of these devices are their large

parasitic losses, compromising high frequency response and their large LO power requirements. Schottky diode mixers can be operated at room temperature but if they are cooled, typical operating temperatures are 77K and 20K (readily achieved using mechanical refrigerators). As a consequence of relaxed temperature requirements, Schottky diode mixer receivers are usually selected for space applications.

1.3.2 Superconducting mixer receivers

The most sensitive heterodyne receivers for millimetre and submillimetre wavelengths use superconductor-insulator-superconductor (SIS) tunnel junctions as the mixing element. These devices consist of two superconducting electrodes separated by a thin (~ 2nm) insulating film. Typical double-sideband SIS receiver noise temperatures are $T_R \approx$ 70K at 250GHz [25], 150K at 350GHz [26], 220K at 500GHz [27] and < 400K at 700GHz [28]. At frequencies where the photon energy exceeds the energy gap of the superconductor (> 700GHz for niobium) however, the performance of an SIS mixer falls off rapidly. DSB receiver noise temperature of 840K at 1040GHz has been reported using a Nb SIS mixer [29]. Operation at significantly higher frequencies will require the use of materials with higher superconducting transition temperatures.

An alternative type of superconducting detector has been proposed [30] that offers great potential as a mixer for terahertz frequencies. The device, a superconducting transition-edge microbolometer, consists of a short (< 0.50 μm), narrow (~ 0.15 μm), thin (~ 10nm) superconducting microbridge contacted by thick normal metal (gold) films that connect to the RF coupling structure (e.g. waveguide mount; integrated antenna). These devices rely upon electron heating effects and are not limited by the superconducting energy gap. The devices must be small to generate sufficient IF bandwidth to be useful for astronomy and remote sensing applications. A DSB receiver noise temperature of T_R ~ 650K at 533GHz at an IF of 1.4GHz has been reported [31].

SIS mixers are the first choice for low-noise operation, but need cooling to around 4K, as do transition-edge microbolometers.

1.3.3   Schottky varactor diodes for frequency multiplication

Chapter two describes the surrounding theory behind these devices but for the present it is sufficient to say that they provide harmonic multiplication above a fundamental RF input signal through the non-linear charge/voltage characteristic of a reverse biased Schottky barrier. This frequency conversion can in theory be 100% efficient due to the purely reactive nature of the reverse biased junction. This ideal is never achieved due to the substrate resistance associated with these devices and the stringent harmonic matching requirements that are imposed by the inherently narrow-band varactor. As with mixer (varistor) diodes, varactor diodes function at room temperature, although benefits in noise reduction can be gained if cooling is possible.

1.4   Frequency multiplier construction
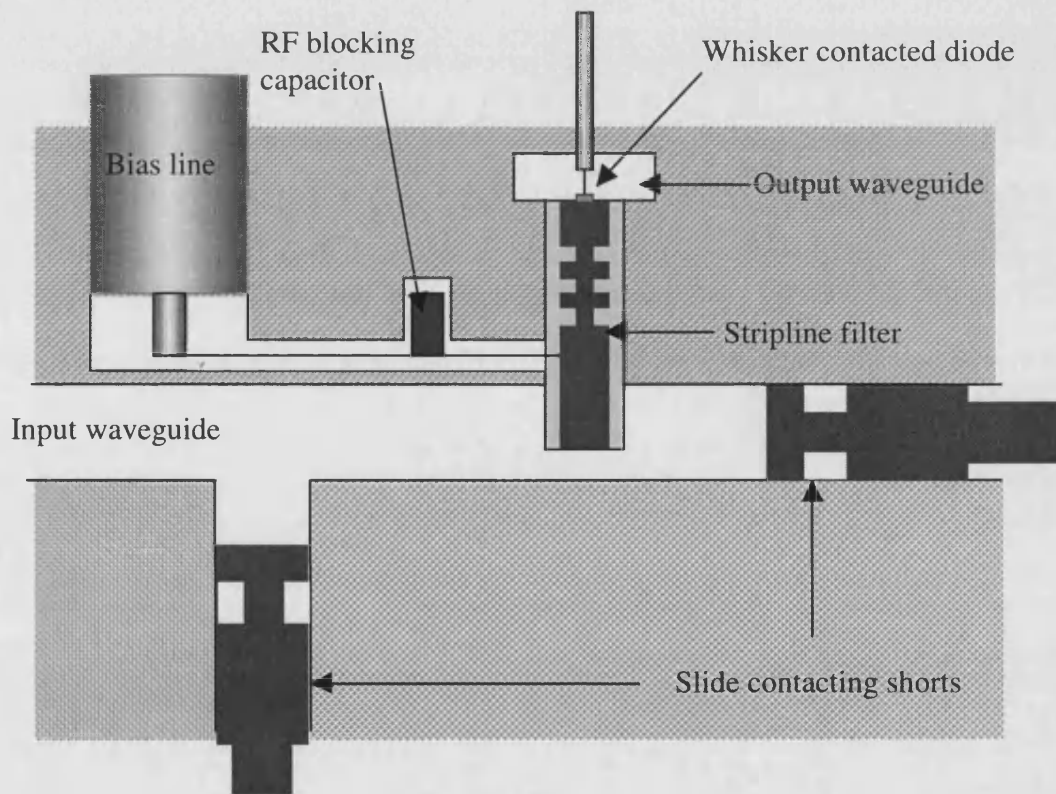
Figure 1.2. Schematic diagram illustrating a crossed waveguide multiplier with stripline coupling between the input and output guides.

Fig. 1.2 shows a typical crossed waveguide multiplier block design. This design was first employed by Takada et al. [32] and has been popularised by Archer [33]. It is now a proven performer for submillimetre multipliers. The design features sliding

tuners on the input waveguide that allow optimum tuning at the plane of the waveguide/stripline transition. The diode chip (featuring an array of similar devices) is housed in the output waveguide and is contacted by a whisker wire with a spark-eroded or chemically etched tip. An ohmic contact on the reverse side of the diode chip contacts to the stripline filter which is designed to transmit fundamental power, whilst reflecting the desired harmonic output frequency. Bias is provided via the whisker post and a contact to the stripline filter. RF rejection is performed by a coaxial cavity filter around the whisker post and a capacitor that transforms to a RF open circuit at the coaxial-line/stripline junction.

Erickson [34] has employed a similar multiplier configuration. This design is again based on crossed waveguides but a coaxial rather than stripline filter provides the frequency dependent connection.

The crossed waveguide mount has a proven record and has been a standard choice in many millimetre and submillimetre wave LO circuits. However different approaches have been sought in order to alleviate some of the problems experienced when forming crossed waveguide multiplier blocks.

Archer and Erickson designs are normally fabricated in 'split-block' form. The block is initially electroformed around a gold-coated mandrel of rectangular cross-section. This has the dimensions of the output waveguide and is usually etched out, leaving the gold coating inside the block. The block is then machined down to a regular shape and sliced perpendicularly to the output waveguide. The input waveguide, bias cavity and additional tuning cavities are then machined into the two halves of the block.

Edrich and Sanborn [35] presented an alternative layout for a frequency doubler (45-90GHz) utilising the properties of rectangular waveguide to provide the necessary input circuit harmonic rejection. The input waveguide featured a single sided E-plane taper ending in a cavity designed for rejection of the doubled output frequency (>16dB achieved) followed by the diode mounting area. The output waveguide extended from the diode region in line with the input waveguide and again featured a single sided taper to reach full height at the output port. The waveguide tapers

facilitated improved impedance matching of the embedding circuit to the combined parallel diode pair used for harmonic multiplication.

Raisanen et al. [36] presented a novel approach to mixer and multiplier design based on a split-block. The design consisted of mirror image halves that were capable of being machined using either an endmill or a slitting saw, with no electroforming necessary. The input and output circuits of the doubler (110-220GHz) consisted of waveguide T-junctions. On the input side, tuners were mounted on two branches of the T with the feeding waveguide and a stripline probe located between them. The output circuit followed this arrangement with tuners situated around a planar diode chip and the output guide. A wide tuning range was obtained using this layout and waveguide lengths were minimal thereby reducing ohmic loss.

Newman and Erickson presented a design in 1999 [37] for a planar multiplier based around an antiseries diode configuration. Separate blocks based on the same configuration were produced for doublers with output frequencies of 160GHz and 320GHz. The input waveguide features multiple E-plane waveguide bends in order to reduce the overall size of the block. A dual stepped E-plane impedance transformer matches the input and diode circuit impedances. The diode chip is located in a cavity between the input waveguide and the quartz stripline filter feeding the output waveguide. A dual step E-plane waveguide transformer is again implemented for improved matching on the output waveguide. The stripline filter extends through a cavity and provides a path for the DC bias.

The designs reviewed above all feature waveguide input and output circuits machined or electroformed in metal. The Edrich design dispenses with coaxial/stripline harmonic filtering, instead achieving this design requirement via waveguide cavities. This approach could prove useful at terahertz frequencies due to its inherently lower loss. The in-line arrangement of the input and output circuits is also a departure from the crossed guides which feature in standard split-blocks. Edrich relied upon rigorous optimisation pre-production, rather than including multiple tuning circuits. Nowadays Finite Element Method (FEM) electromagnetic simulators allow designs to be optimised prior to fabrication, so in principle it is possible to design efficient fixed-tuned multipliers before any machining takes place. At terahertz frequencies, tuning

elements are difficult to make and incur appreciable loss. If designs are not totally fixed-tuned, alternative approaches to circuit tuning may be necessary.

Multipliers designed for harmonic output above the second (triplers, quadruplers and quintuplers) have circuits that are further complicated by a requirement to provide current flow at certain intermediate harmonic frequencies. This requirement is discussed in terms of the varactor diode characteristic in section 2.3 and in terms of the external circuit in section 3.3.

1.5 Split-block versus MEMS

The technology behind split-block multipliers is now mature and the designs described in the preceding section illustrate innovative features that afford a wide tuning range and simplified machining requirements. However, the fact remains that as frequencies extend into the terahertz region, engineering tolerances become more stringent and forming waveguide circuit elements becomes increasingly difficult. In addition, once the block has been constructed mounting the diode chip can prove extremely difficult. The exact location of the diode can affect the circuit tuning capability and is therefore an important design parameter. Whisker contacted devices can fail due to mechanical shock and/or corrosion whilst multipliers based on planar devices (section 2.6) often require delicate soldering operations which can result in damage to the device/circuit.

Advantages of the split block approach include compatibility with other components and strength (particularly at low-temperature). For the purposes of testing, millimetre- and submillimetre-wave MEMS components should attach readily to measurement systems with conventionally machined flanges. This requirement is met during the normal machining process adopted for split-block components. Temperature stability is naturally afforded by components formed from brass or copper. By contrast MEMS components based on epoxy/semiconductor materials tend to be subject to differing rates of contraction as the ambient temperature falls. This can lead to build up of stress within the epoxy layers and ultimately, fracture.

Despite the difficulties mentioned above MEMS techniques offer enormous advantages over conventional machining in terms of the tolerances that can be achieved and the speed of manufacture. Many prototype ideas can be included on a single mask plate and reach the finished component stage without laborious machining. Eventually it is envisaged that integration will reach a level where interconnected source, multiplier, mixer and filter modules will be replaced by a single micro-fabricated waveguide circuit. Rectangular waveguide components possible at microwave frequencies but unrealisable at terahertz frequencies, including inductive irises and stepped transformers, become trivial to form using surface micromachining techniques (section 4.4).

Planar integrated circuit technology offers practical advantages for terahertz systems, but planar components are subject to detrimental substrate modes and other loss mechanisms. These severely limit performance with increasing frequency of operation. Rectangular waveguide is a proven low-loss transmission medium in the submillimetre-wave frequency band and can be fabricated via surface or bulk micromachining.

1.6 MEMS (Micro-Electromechanical-Machined-Systems)

In the 1960s, fabrication of integrated circuits began. Physically small components capable of high-speed operation and/or vast information storage are now commonplace in affordable consumer products. In order to make this possible, high accuracy patterning techniques have been developed to form the many semiconductor devices and interconnecting tracks that constitute an integrated circuit chip. MEMS, first proposed by Feynman [38], utilises similar techniques to produce very small mechanical and electromechanical structures.

The necessary differences between MEMs and conventional processing arise due to the three-dimensional possibilities offered by MEMs structures. IC processing is planar and generally relies on stacking thin layers (typically of the order of 1 micron) with conducting, semiconducting or passivating properties. Micromachined structures often feature components exceeding $100\mu m$ in thickness and therefore require very different forming techniques. Broadly speaking, the methods involved in MEMs can

be divided into two categories, bulk micromachining and surface micromachining [39].

1.6.1 Bulk micromachining

This technique is relatively mature and was originally developed in the late 1950s in order to fabricate pressure sensors in silicon. It entails creating component features via selective etching of a bulk substrate material. By judiciously combining highly directional (anisotropic) etchants, with nondirectional (isotropic) etchants and using the wafer's crystallographic orientation, features with varying depths and sidewall inclines can be produced. This technique has found application in sub-mm wave component design in the guise of novel micromachined feedhorns [40] and air-bridged device contacts [41]. By creating regions with increased levels of impurity doping the etch-rate can be slowed down and in the case of a pn junction, etching can be completely halted. Deep cavities suitable for, amongst others, sensor diaphragms and microwave resonators can be fabricated by employing these methods.

Despite its maturity, bulk micromachining has traditionally suffered from a lower attainable aspect ratio and less directional flexibility when compared with other MEMs techniques, which fall into the surface micromachining category. The outlook for bulk machining is positive though, due to advances in dry etching [42] with directional etch rates in silicon of up to 4μm/minute reported.

1.6.2 Surface micromachining

Surface micromachining represents a logical progression from standard IC lithography. A material is deposited as a film on to a substrate and subsequently patterned. As in the IC industry this film can be metallic (evaporated, sputtered or plated) or dielectric (evaporated, sputtered or spin-on polymer). Following patterning, the remaining areas of the layer can be used as an integral part of the component (structural material) or removed (sacrificial material) after acting as a mould, or to release other micromachined parts.

Typical structural materials employed in MEMs are metals including copper and aluminium, polycrystalline and single crystal silicon, silicon dioxide and nitride materials. Recently, spin-on photoresists have been developed which allow ultra

thick layer formation (>1000μm) and offer excellent aspect ratios coupled with high resistance to acid and alkali attack (relevant when employed in process schemes involving etching and plating). Conventional photoresists, developed for planar processing can also be applied in MEMs fabrication sequences, example applications being release layers and formers for electroplated components.

Surface micromachining has evolved into an accurate and low-cost method with new applications and materials emerging as interest from a variety of subject groups increases. Producing static and moving components, it readily lends itself to submillimetre wave component fabrication. The fabrication chapter of this thesis describes in detail the surface processing methods available for use within the Terahertz Technology Group at the University of Bath. In the structures shown in later chapters, conventional and MEMs photoresists have been employed in conjunction with electroplated and vacuum deposited metals to form millimetre and submillimetre passive and active components. The following diagrams (figs. 1.3 and 1.4) offer an introduction and illustrate two applications that will be discussed at greater length in chapter 4.
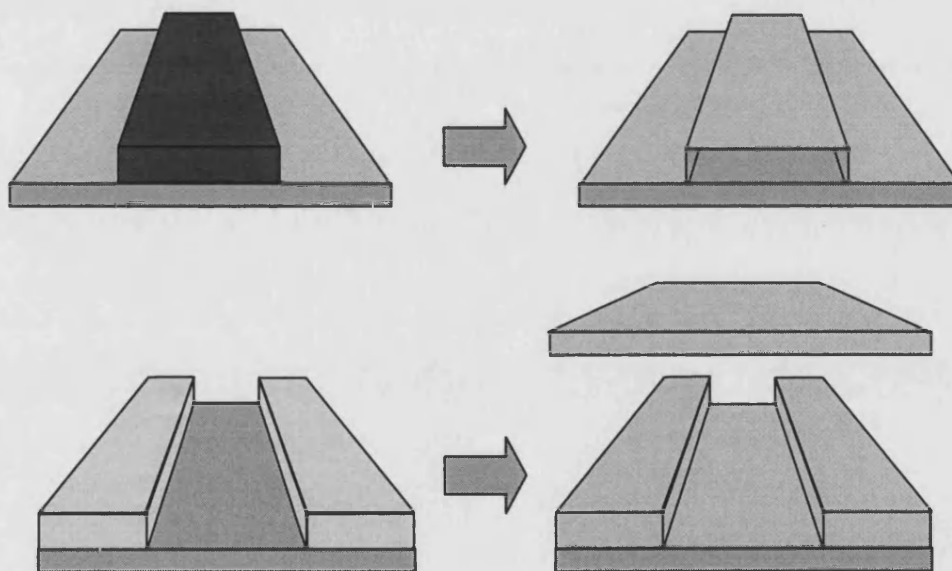
Figure 1.3. Positive resist waveguide former (top) and
negative SU8 epoxy resist trench (bottom).
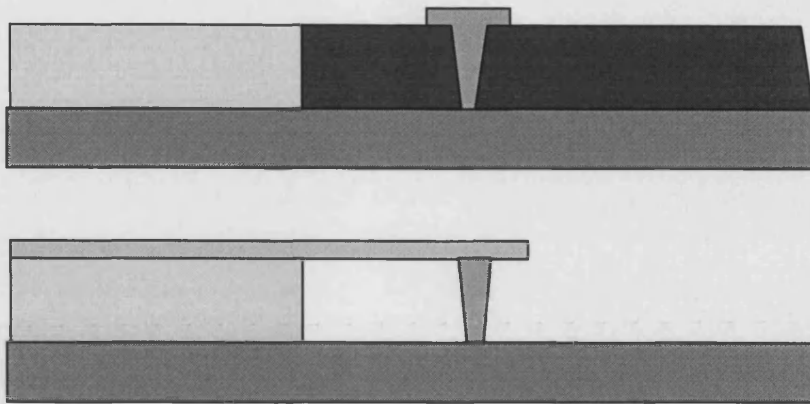
Figure 1.4. Electroformed device contact post in conventional photoresist
with dielectric support and evaporated metal strip contact.

Figure 1.3 illustrates the fundamental difference between processing with conventional and negative epoxy resists (more detail in chapter 4). The approach adopted prior to the acquisition of epoxy based negative resist was to produce a waveguide former from conventional positive resist and wash this away after seeding and plating the former. Negative epoxy resist is a permanent feature once exposed and thus required a modified approach. Trenches were lithographically formed in the dielectric sheet, seeded, plated and finally capped with a metallic lid to form rectangular waveguides/filter-cavities etc.

Having introduced the basic concepts behind bulk and surface micromachining, the next section reviews some of the work carried out to date on terahertz micromachined components.

1.7 Micromachining for terahertz applications

The application of micromachining technology to terahertz circuits was explored as early as 1979 [43] with the fabrication of a 2.5THz 40µm wide by 400µm long (3.5λ) tapered-dielectric-rod antenna micromachined from a silicon substrate.

In terms of bulk micromachining, the ability to form waveguide cavities in silicon via anisotropic etching is proven [44, 45]. This technique is normally based on a wet potassium hydroxide (KOH) etch through a pattern formed in Silicon Nitride [46]. Alignment is made to the 110 planes in order to produce smooth internal waveguide

surfaces. In [44] electroless nickel plating was used as a seed layer, followed by gold to produce a low resistance internal coating. Half width waveguides were formed in two substrates, then the two halves were mated together to form WR8 and WR4 waveguides. Reported loss was less than 1dB/wavelength for the WR4 waveguides.

An example of combined bulk and surface micromachining is described in [40]. Here anisotropic etching of a silicon substrate is combined with patterning of a negative epoxy based photoresist (SU8) to form an antenna and broadband transition into rectangular waveguide suitable for operation at 585GHz.

Dichroic plates have been batch processed on sacrificial substrates using the same photosensitive resin as used in [40]. The patterned resin is released and plated and designs have been demonstrated that pass 640GHz whilst rejecting 240GHz [47].

In addition to the photolithographic techniques described thus far, alternative methods have been sought for the scaling down of conventional microwave components. Laser micromachining is a technique that involves computer controlled laser milling of silicon. Amongst other components, it has been successfully employed to produce 810GHz and 2.0THz corrugated feedhorn antennas. The technique has also been used to produce master components from which multiple replica horns can be fabricated [48].

Aiming for methods suitable for mass production and further cost reduction has led to research into casting or moulding of terahertz components [49]. Inexpensive high precision copies of conventionally fabricated terahertz structures have been produced through the casting of polyurethane structures using a silicone-based mould formed from a master. The silicone mould is formed on a conventionally machined master and then filled with polyurethane, which is subsequently cured and removed. Measurements have shown that a 690GHz mixer-block produced using this method and subsequently gold-plated performs as well as a metal block with the same dimensions.

Lubecke and Rebeiz [50] presented a detailed review of micromachining for terahertz applications, published at the end of 1998. This paper includes descriptions of the

aforementioned techniques and describes the development of micromachined planar transmission line technology for operation in the submillimetre-wave region.

1.8   Thesis overview

In following chapters, the design and fabrication of a number of micromachined sub-mm wave components is presented. This introductory chapter has highlighted existing and potential terahertz applications and introduced the circuit topologies of typical sub-millimetre frequency mutlipliers. The following chapter contains fundamental theory relating to the Schottky devices conventionally used within sub-millimetre wave multiplier circuits. It also contains a review of fabrication techniques developed by various research groups in order to produce devices with optimal operating characteristics.

The third chapter introduces constituent elements of the fabricated components and outlines the design procedure adopted for the frequency multipliers that have provided the primary focus of the project. Critical design aspects are highlighted and solutions that are compatible with a MEMs approach are described. Modelling using commercially available finite-element-method and non-linear circuit simulator software is presented.

Processing schemes are presented in chapter four accompanied with full details of all novel processing methods. The scope and constraints of developed techniques are clarified and supported with detailed guidelines for processes suitable for the creation of micromachined waveguiding structures.

Chapter five contains results from DC device testing and RF testing of completed waveguiding structures. These results are discussed and performance-critical aspects of component fabrication are emphasised.

Suggested improvements and concluding remarks form the basis of chapter six. The drive to apply micromachining techniques to microwave, mm-wave and terahertz systems has gathered pace rapidly but many possibilities remain unexplored. Ideas forming the basis for continuing work are introduced.

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2. Device Theory and Design

2.1 Frequency multipliers

Before looking at the constituent elements of a frequency multiplier in detail, it is helpful to consider what requirements are placed on a working frequency multiplier. The most fundamental requirement is that an incoming signal with a frequency f_0 will produce a multiplied frequency f_{out} at the output. It is desirable that this multiplication is as efficient as possible in order that suitable signal power is available for LO operation in a mixer. Bandwidth must be considered, and maximised if the multiplier is intended for use with varying input frequencies. The system must exhibit low noise, as any noise present in the multiplier output will appear as LO noise in the mixer [1, 2].

Harmonic multiplication requires a device with non-linear behaviour. To date, millimetre and submillimetre wave multipliers have normally used the non-linear CV or IV characteristics of a reverse or forward biased diode to provide harmonic multiplication. The most widely used device for this purpose is the Schottky diode and this may be operated in varistor or varactor mode depending on whether its IV or CV non-linearity is utilised. From the outset, it should be stated that whilst forward biased diodes have broad bandwidth and stable operating characteristics, varactor diodes can offer higher efficiency and low noise [1, 3]. For this reason submillimetre multipliers normally feature diodes operating predominantly in varactor mode.

2.2 The Schottky barrier

The Schottky-barrier diode is a two-terminal semiconductor device that utilises the non-linear properties (CV&IV) of a metal-semiconductor junction (fig. 2.1). Unequal work functions in the metal and semiconductor give rise to an electrostatic barrier at their interface. This barrier leads to rectifying properties and conduction that is controlled primarily by thermionic emission of majority carriers over the barrier. As a majority carrier device, the Schottky diode has increased high-frequency capability over devices such as pn diodes that exhibit minority carrier effects.

In microwave and sub-mm wave applications it is necessary to minimise device series resistance and junction capacitance and thus maximise cut-off frequency. A semiconducting material with high carrier mobility and saturation velocity is required to meet these criteria. Gallium arsenide has higher carrier mobility and saturation velocity than silicon and is the primary choice for high-speed mixer, detector and multiplier diodes. Silicon, being less expensive than gallium arsenide, still has a place for lower frequency applications. Platinum, gold and aluminium are commonly used to form the Schottky barrier.

A schematic view of the Schottky diode layer structure is presented in fig. 2.1. Varactor and varistor structures are shown with typical layer properties for submillimetre wave operation and illustrate the differences between these devices in epilayer thickness and doping. Both varactor and varistor diodes are based on a metal/n/n+ layer scheme. The diode is formed as a metal/n-type interface and the heavily doped n+ layer serves to reduce substrate impedance. The varactor diode has a thicker n-type layer in order to accommodate the increased depletion region under conditions of high reverse bias. If the epilayer thickness t_e is smaller than the maximum width of the barrier w_{br}, then the epilayer is punched through before the reverse breakdown voltage is reached. If the epilayer thickness is chosen such that $t_e > w_{br}$, then the junction will adhere to the device capacitance/voltage relationship up to the breakdown voltage.
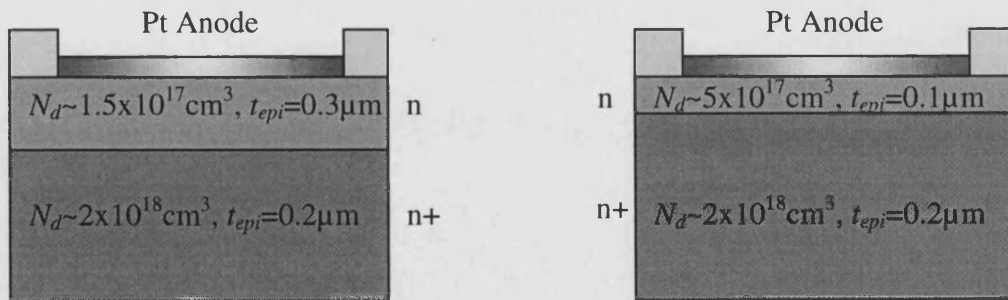
Figure 2.1 Submillimetre wave Schottky barrier (a) varactor and (b) varistor diodes.

2.2.1   Formation of the barrier

Band structures are presented in fig. 2.2 for the individual metal and semiconductor and the combined Schottky junction. Electrons in the semiconductor have on average a higher energy than electrons in the metal. These electrons of higher energy move into the metal and collect on its surface. Ionised donor locations are left in the semiconductor, adjacent to the interface and an electric field is established due to the separation of positive charges in the semiconductor and negative charges on the surface of the metal. This field inhibits further flow of electrons into the semiconductor when the Fermi levels of both materials are equalised. The valence and conduction bands are thus forced to bend.
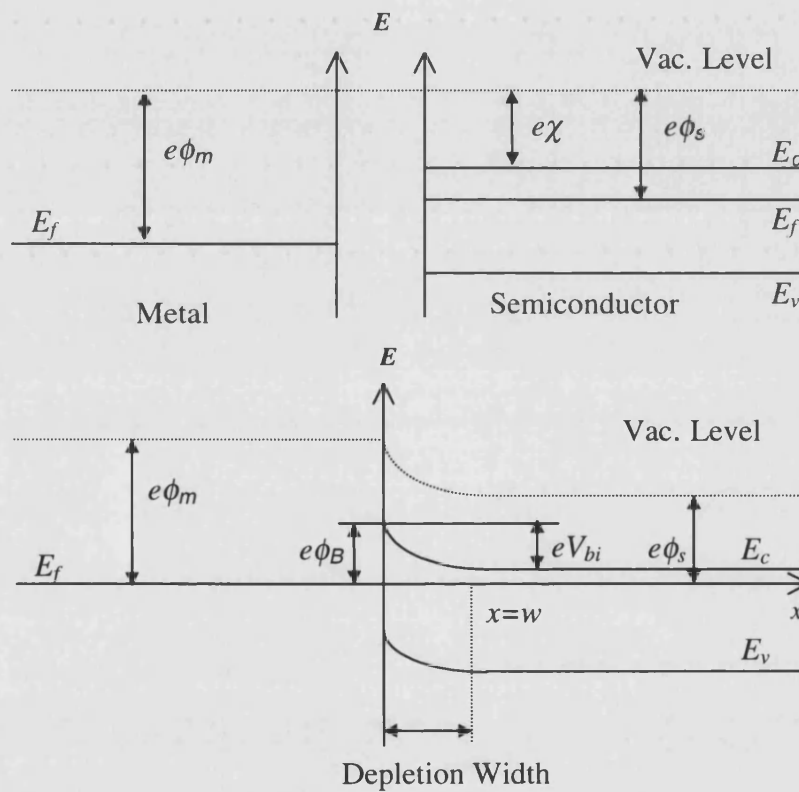
Figure 2.2 Metal/Semiconductor band diagram before and after contact.

In fig. 2.2, e is electron charge, ϕ_s is the semiconductor work function, ϕ_m is the metal work function and ϕ_B is the difference between them. χ is the electron affinity, describing the energy difference between an electron on the vacuum level and an

electron on the lower edge of the conduction band. E_c, E_v, and E_f are the conduction, valence and Fermi energies respectively. The barrier width is w.

In the *depletion approximation* it is assumed that in the region of the semiconductor where the bands are bent upwards, the space charge is due entirely to the ionised donors. In the depletion region, uniform distribution of these donors is assumed and therefore a uniform space charge. The electric field will increase linearly from $-E_{max}$ ($x=0$) to 0 ($x=w$) and the magnitude of the electrostatic potential will decrease quadratically, resulting in a potential barrier parabolic in shape. The width of the depletion region is given by [1]

$$ w = \left[\frac{2\varepsilon_s}{qN_d} (V_{bi} - V_b - V_T) \right]^{1/2}, \tag{2.1} $$

where N_d is the donor density, ε_s is the total permittivity of the semiconductor, V_{bi} is the built-in potential, V_b is a voltage applied externally to the barrier, k is Boltzman's constant and T is the temperature. The term $V_T = kT/q$ (~26 mV at room temperature) arises from the presence of the transition region (at $x=w$) where the electron concentration falls from a value equal to N_d to a value negligible compared with N_d.

The space charge due to the ionised donors contained in the depletion region per unit area is then

$$ Q_{sc} = \varepsilon_s |E_{max}| = qN_d w = [2q\varepsilon_s N_d (V_{bi} - V_b - V_T)]^{1/2}. \tag{2.2} $$

As there is no minority carrier storage in a Schottky diode, there is no diffusion capacitance. The capacitance of the device is therefore due only to the charge in the depletion layer. Hence for microwave diodes (see section 2.4 for sub-mm equivalent)

$$ c_b = \left| \frac{\partial Q_{sc}}{\partial V_a} \right| = \left[\frac{q\varepsilon_s N_d}{2(V_{bi} - V_b - V_T)} \right]^{1/2} = \frac{\varepsilon_s}{w}. \tag{2.3} $$

The idealised situation used to derive the equations above is in reality never achieved. The barrier height will depend not only on the materials and the applied bias, but also on the thickness of a thin oxide layer that (during fabrication) inevitably appears at the

metal/semiconductor interface. Deviations from the ideal case will be discussed in the following sections.

2.2.2 Current-transport mechanisms

In most practical Schottky diodes the dominant carrier transport mechanism is by emission of the electrons from the semiconductor over the barrier and into the metal. Quantum-mechanical tunnelling provides a second transport mechanism with electrons tunnelling through the potential barrier and appearing in the semiconductor.

2.2.3 Emission over the barrier

Motion of electrons through the semiconductor depletion region is governed by the mechanisms of diffusion and drift in the electric field of the barrier. When they arrive at the interface, their emission into the metal is determined by the rate of transfer of electrons across the semiconductor/metal interface. These two processes are essentially in series and the process that imposes a lower limit on the flow of electrons essentially sets the current.

Diffusion theory assumes that the diffusion and drift of electrons in the depletion region limit the current flow, and that the conduction electrons in the semiconductor immediately adjacent to the semiconductor are in thermal equilibrium with those in the metal. The thermionic-emission theory assumes that the effects of drift and diffussion are negligible and the transfer of electrons across the interface dictates the current flow. A synthesis of the two theories [4] considers the two mechanisms to be in series. Assuming that the thermionic-emission current must equal the drift-diffusion current, the theory predicts (except for high bias) that the current density at the junction is

$$J_b = \left[A^{**} T^2 \exp\left(\frac{-q\phi_b}{kT} \right) \right] \left[\exp\left(\frac{qV_b}{kT} \right) - 1 \right] = J_s \left[\exp\left(\frac{qV_b}{kT} \right) - 1 \right]. \qquad (2.4)$$

At room temperature for high-mobility semiconductors doped to 10^{16} to $10^{17} cm^{-3}$ and in the electric field strength range 10^4 to $2 \times 10^5 \ Vcm^{-1}$ (normal operating conditions) the Richardson constant A^{**}, remains essentially at a constant value. Reported values for A^{**} vary between 8.2 $Acm^2 K^{-2}$ [5] and 8.6 $Acm^{-2} K^{-2}$ [6] for GaAs.

2.2.4 Tunnelling through the barrier

Schottky barriers formed on heavily doped semiconductors and/or operating at low temperature will have a junction current that is influenced by quantum mechanical tunnelling of electrons through the barrier. Field emission describes the condition where the temperature is low enough and the doping sufficiently high so as to allow electrons with energies close to the Fermi energy in the semiconductor to easily tunnel through the barrier. An increase in temperature causes the electrons to see a thinner and lower barrier. Thermionic field emission occurs when the quantum tunnelling current stabilises at a certain temperature dependent value. If the temperature is increased further, a point eventually arises where thermionic emission over the barrier is the dominant influence on the junction current.

The forward tunnelling current-voltage relationship is given (except at very low V_b) by

$$J_b = J_s \exp\left(\frac{V_b}{E_0}\right), \tag{2.5}$$

where

$$E_0 = E_{00} \coth\left(\frac{qE_{00}}{kT}\right) \tag{2.6}$$

and

$$E_{00} = \frac{h}{4\pi}\left(\frac{N_d}{m^* \varepsilon_s}\right)^{\frac{1}{2}}. \tag{2.7}$$

In these formulae, m^* is the effective mass of electrons in the n-type semiconductor, ε_s is its permittivity and h is Planck's constant.

Experiments have been performed to determine the temperature ranges at which emission mechanisms dominate the device behaviour [5]. For Schottky diodes made on n-type GaAs with $N_d \approx 2 \times 10^{17}\text{cm}^{-3}$ the tunnelling of electrons may be neglected above 100K where pure thermionic emission dominates.

2.2.5 Generalised IV relationship

A generalised I-V relationship may be used to describe the Schottky junction at any temperature and for various dopant levels. This expression follows from the formal

similarity of the thermionic and tunnelling current definitions. The ideality factor η is introduced and described so $\eta = 1$ for pure thermionic emission. An increase in η is due to deviation from this ideal model.

$$\eta = \frac{q}{kT}\frac{\partial V_b}{\partial(\ln J_b)}.$$ (2.8)

Using this definition, the I/V characteristic of the junction in which current flows due to pure thermionic emission ($I_b \gg I_s$) can be expressed in the form

$$I_b = SA^{**}T^2 \exp\left(\frac{-q\phi_b}{\eta kT}\right)\exp\left(\frac{-qV_b}{\eta kT}\right) = SA^{**}T^2 \exp\left(\frac{V_b - \phi_b}{V_0}\right),$$ (2.9)

where S is the area of the junction and

$$V_0 = \frac{k}{q}\eta T = 8.617\times10^{-5}\eta T \quad [V]$$ (2.10)

is the slope parameter of the I/V characteristic.

Diode ideality can be measured by determining the slope of the I/V curve in millivolts per decade of current. From equation (2.4) the change in voltage, ΔV, giving a decade change in current is

$$\Delta V = \frac{\eta kT}{q\log(e)},$$ (2.11)

where e is the base of the natural logarithms. Thus for a known change in voltage over a decade of current, the ideality may be derived. The saturation current $I_s = SJ_s$, can then be determined from (2.4).

The DC resistance of the diode is calculated by using the deviation (caused by the series resistance) from exponential I/V behaviour at higher device currents. For a current of 1mA and a typical series resistance of 10Ω, 10mV will be dropped across the series resistance. In general R_s is calculated from

$$R_s = \frac{\Delta V}{I},$$ (2.11)

where ΔV is the deviation from the extrapolated low current characteristic and I is in the range 100-1000μA.

2.2.6 Reverse characteristics

The conventional layered Schottky structure shown in fig 2.1 allows the substrate resistance to be minimised via the highly doped n++ layer, whilst junction performance is optimised using the doping and thickness of the n layer. The width of the depletion region increases with increasing reverse bias until it punches through the n layer. Beyond this bias point the device capacitance will decrease only marginally due to low penetration of the depletion region into the n++ layer.

At sufficiently high reverse bias, avalanche breakdown occurs. The point at which this takes place is dependent on the electric field strength, temperature and crystal orientation. The breakdown voltage V_{br} under the condition of punch-through is nearly independent of the donor concentration, as the applied voltage and epitaxial layer thickness predominantly determine the field strength.

From [7], the punch through voltage and avalanche breakdown voltage can be calculated from

$$V_{pt} = \frac{qN_d l^2}{2\varepsilon}$$

(2.12)

and

$$V_{abr} = \frac{\varepsilon E_{max}^2}{2qN_d},$$

(2.13)

where l is the epilayer thickness and E_{max} is the maximum electric field obtainable in the diode. Lipsey and Jones [7] offer the following empirical relation for E_{max}

$$E_{max} = 1.3 \times 10^{-12} (Vcm^2).N_d(cm^{-3}) + 4 \times 10^5 (Vcm^{-1}).$$

(2.14)

2.3 Multiplication using nonlinear charge/voltage operation

Fig. 2.3 illustrates the way in which nonlinear capacitance can be used to convert a harmonic input signal into a periodic output signal containing components at the multiples of the input frequency.
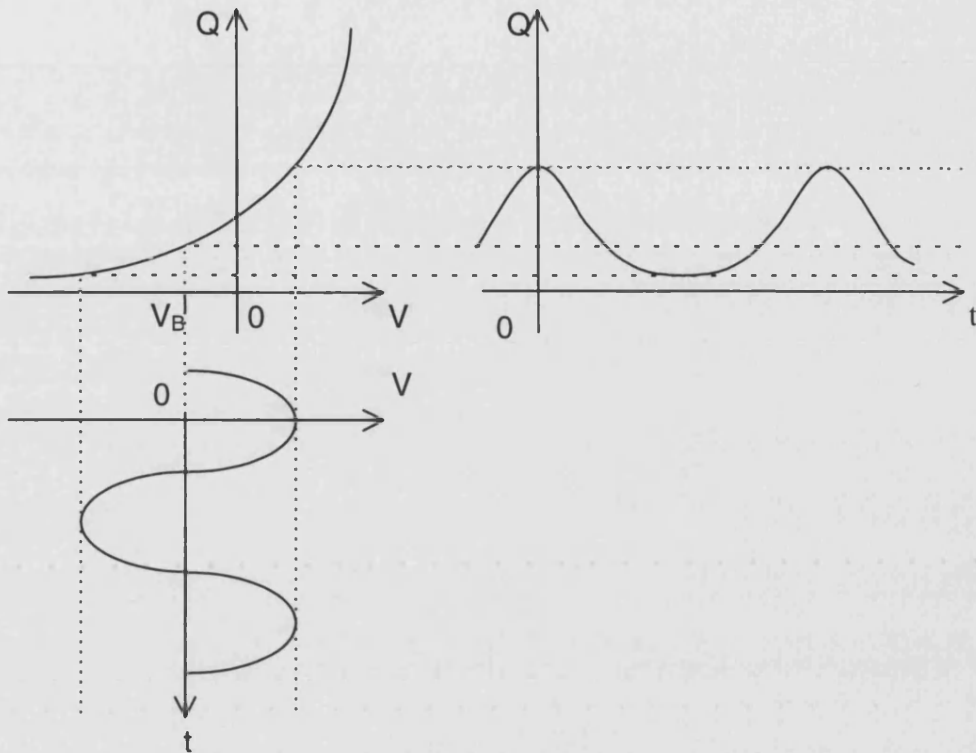
Figure 2.3. Principle of multiplication for a reverse biased Schottky junction.

The nonlinear charge-voltage characteristic may be expanded into power series about the operating point fixed by the bias voltage V_b.

$$Q(V_b + \Delta V) = b_b + b_1 \Delta V + b_2 \Delta V^2 + b_3 \Delta V^3 + ... \qquad (2.15)$$

The input voltage applied to the device may be expressed as

$$\Delta V = V_d \cos(\omega_g t) \qquad (2.16)$$

Using expression (2.5) in (2.4) leads to the charge waveform

$$Q(t) = Q_0 + Q_1 \cos(\omega_g t) + Q_2 \cos(2\omega_g t) + Q_3 \cos(3\omega_g t) + ... \qquad (2.17)$$

Thus, a nonlinear device provides power at harmonic frequencies above the fundamental. In a multiplier, filters are employed in order to select the required output frequency and separate the source from the generated harmonics. Matching circuits are also necessary to provide optimum embedding impedance for the device and efficient frequency conversion.

From the preceding analysis, it appears that a square law device is only capable of producing second harmonic power from the fundamental input. This is not the case however, as the non-linear mixing properties of the device can be utilised to allow generation of power at higher order harmonics.

A conventional Schottky varactor tripler is designed so that current at the second harmonic is allowed to flow through the diode. Mixer products from the first and second harmonics are generated at the third and fourth harmonics. Filtering is employed to select the third harmonic as the output. This method can be expanded for use in higher order multipliers [3].

Frequencies existing in a multiplier which produce the required output via mixing in a non-linear device are known as idler frequencies. The circuits designed to allow idler currents to flow are called idler circuits. A doubler requires no intermediate idlers but it is wise to short circuit the third harmonic. The most practical configuration for a tripler includes an idler circuit that resonates with the junction capacitance and provides a short circuit at the second harmonic. Penfield and Rafuse [3] give idler configurations for tripler and higher order multipliers.

2.3.1 Diode noise

Thorough treatments of noise sources within metal-semiconductor junctions are presented in [1] and [5]. In varistor diodes device generated noise is a significant concern, with contributions from shot noise, thermal noise, hot electron noise (due to heating of the electron energy distribution under high forward current conditions) and trap noise (due to electron traps at the interface causing a fluctuation in the number of electrons flowing across the barrier). Therefore in the literature, noise treatment of Schottky diodes tends to focus on diodes operated in forward bias as mixer devices [8, 9 and 10]. Varactor diodes offer low noise operation, due to the lack of current flow across the depletion region. Thermal noise generated in the diode series resistance is normally the dominant noise source in varactor diodes. If the varactor series resistance and the resistance associated with the surrounding multiplier circuit are minimised, a submillimeter multiplier can operate with extremely low noise levels [1].

Varactor multipliers do however behave as phase multipliers, so phase deviations in the fundamental oscillator signal will be amplified and the carrier to noise ratio will be degraded by a minimum factor of

$$\Delta CNR = 20\log_{10}(n) \qquad (2.18)$$

where n is the multiplication factor. Thus a frequency doubler will exhibit a CNR which has degraded by at least 6dB from the input signal.

2.3.2 Varactor performance

If a varactor diode is going to enable efficient harmonic multiplication, its structure and behaviour must be optimised for the intended operating frequencies and input power. The capacitance modulation range should be such that it is efficiently exploited without breakdown, punch-through or conduction. Series resistance must be kept to a minimum for high cut-off frequencies and the anode diameter must be selected with capacitance and power handling in mind. Section 2.4 describes how the epitaxial structure of the diode can be optimally engineered whilst taking account of a variety of high-frequency effects.

Within the multiplier circuit, the DC bias point should be chosen to provide maximum capacitance change from the RF input signal. The embedding network must provide optimum embedding impedances at the input, output and idler frequencies and must have low resistive loss. These design points are discussed in chapter 3.

2.4   Layer structure and junction diameter

From the characteristic equations describing a Schottky varactor diode it is evident that the doping and thickness of the epitaxial layer and the anode diameter are key aspects in dictating device performance. Doping concentration and epilayer thickness influence the reverse and avalanche breakdown voltages, zero bias capacitance and capacitance modulation ratio. Reducing the anode area is a simple means of decreasing the zero bias capacitance and thereby increasing the dynamic cut-off of the device.

Louhi and Räisänen [11, 12, 13, 14] have performed extensive modelling of varactor behaviour as a function of anode size and epilayer parameters. In their varactor

model [11], behavioural aspects including spreading of the depletion layer at the perimeter of the anode [12, 13], electron velocity saturation and electron velocity overshoot [14] are accounted for.

For devices which have an anode diameter that is not large compared to the thickness of the epilayer, the transition front between the depleted and undepleted sections of the n-layer is found to be larger than the lithographically defined device area. The potential of the epilayer and the transition front itself are curved near the periphery of the circular metal anode (fig. 2.4). Edge effects caused by the small size of the anode are accounted for in [12] and correction factors are introduced to reflect the increased area of the transition front between the depleted and undepleted regions of the n-GaAs epilayer.
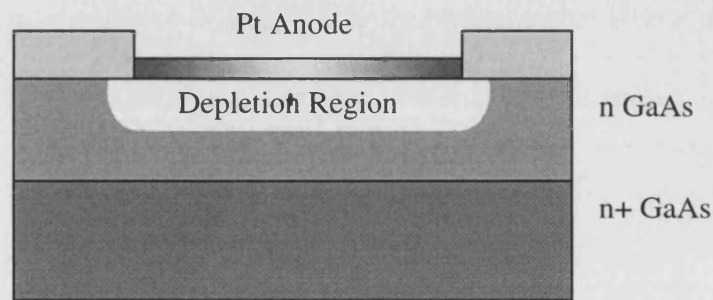
Figure 2.4. Schematic view of curved depletion region.

The capacitance of the circular Schottky junction can be found by calculating the net charge of the depletion layer from the numerically solved potential of the epilayer [13]. A correction term is usually added for millimeter wave varactors and for submillimeter devices this is accompanied by a second correction term so that

$$C_j = \frac{\varepsilon A}{W}\left(1 + \frac{b_1 W}{R_0} + \frac{b_2 W^2}{R_0^2}\right) = \frac{\varepsilon A}{W}\gamma_c, \qquad (2.19)$$

where A is the metal anode area, W is the depletion layer width and R_0 is the radius of the metal anode. The numerical constants b_1 and b_2 are 1.5 and 0.3 and γ_c is the net correction factor when compared with the simple parallel plate formula.

Electron velocity saturation is accounted for in [14] by limiting the velocity of the transition front to a value less than the maximum velocity of the electron.

$$\left|\frac{\partial W}{\partial t}\right| < v_{max} \tag{2.20}$$

For a current required to pump the junction capacitance

$$I_d = C_j \frac{\partial V_j}{\partial t} = C_j \frac{\partial V_j}{\partial W} \frac{\partial W}{\partial t} \tag{2.21}$$

The maximum current of the diode is predicted in [14] as

$$I_{max} = A q N_D v_{max} \gamma_c \tag{2.22}$$

This is a higher value than previously predicted by East et al. [15] and can lead to significant differences in the predicted performance of a varactor multiplier.

The modelling method employed by Louhi in [14] also accounts for electron velocity overshoot. This is the effect witnessed when GaAs varactor junctions experience fast transients and the electron velocity in the semiconductor can overshoot the steady-state value [16] by a significant factor. In [14] a constant low-field saturation velocity and a second constant high-field saturation velocity are used to simulate electron velocity overshoot.

The model presented in [14] was verified via comparison with experimental results from a two-diode 160GHz, balanced doubler from Erickson [17]. Agreement surpassed that provided by [15] and this was attributed to the correction factor for the device area including edge-effects.

In addition, a proposed multiplier chain for 160-320-960GHz (doubler then tripler) was analysed and interesting conclusions were drawn regarding the epilayer thickness and the DC bias point. Focusing on the second stage of the analysis involving the tripler, the model predicted that the UVA 2T2 diode (a proven varactor in this application) would perform best as a tripler with zero applied DC bias. The authors found that the maximum ratio of depletion width modulation (0.15μm) could be attained from a zero bias point with no appreciable loss through forward conduction.

Moreover, at this zero bias point the non-linear charge/voltage characteristic was at its most pronounced, therefore the 2T2 diode would provide lower harmonic conversion efficiency if a DC reverse bias was applied. This was particularly significant since it meant that most of the epitaxial layer (thickness 0.6μm) remained undepleted during varactor operation, thereby serving only to add to the combined series impedance of the device.

Based on the work presented in [11], optimised layer structures and anode diameters for sub-mm wave varactors were suggested by the authors. Table 2.1 shows the optimised diode parameters for varactor operation at 800GHz. For comparison, the structures of various fabricated sub-mm wave multiplier diodes are shown with the operating frequencies of the multipliers they were employed in.

Based on the proposed layer structure it is possible to obtain the expected avalanche (2.12) and punch-through voltages (2.13, 2.14) and the expected zero-bias depletion width (2.1) and capacitance (2.19). These are V_{abr}= 8.5V, V_{pt}= 9.4V, W=0.098μm and C_{j0}=6.1fF.

Reference	Output frequency/ Application	Doping (cm^{-3})	Epilayer thickness (µm)	Series resistance (Ω)	Zero bias Capacitance (fF)
[18]	750GHz Tripler	9x10^{16}	0.49µm	20 Ohms	1.6-3.4
'Optimised' [18]	750GHz Tripler	1.5-3.5x10^{16}	0.25-0.35	10	1.6-3.4
[19]	THz freq's (Proposed)	1.6x10^{17}	0.3	12	5.0 (d=2.4µm)
UVA 6P2/6P4 [20]	Quadrupler & Sextupler 450-750GHz	3x10^{16} (6P4 data)	1.1 (6P4 data)	10 (6P4 data)	20 (d=6µm) (6P4 data)
UVA 2T2 [21]	Quadrupler 750GHz	1.0x10^{17}	0.59	11.5	5.5 (d=2.5µm)
UVA 1E4 Mixer type [22]	Octupler (Varistor mode)	-	-	6.4	3.5
UVA 2T2 [23]	499GHz Chain-Tripler	1.0x10^{17}	0.59	11.5	5.5 (d=2.5µm)
'Diode C – Farran' [24]	800GHz 4x200, 2x400	2.0x10^{17}	0.25	11.5	5.1 (d=2.0µm)
[11]	800GHz (proposed)	1.5x10^{17}	0.2-0.25	-	2.4µm = Opt. diameter.
[25]	450 & 600GHz	2.5x10^{17}	0.3	9.8	C_{min}=1.1 (d=3.0µm)
Bath Univ.	800GHz	1.5x10^{17}	0.3	10 (aimed)	Expected 6.1fF (d=2.5µm)

Table 2.1. Terahertz varactor characteristics from proposed and fabricated diodes.

2.5   Practical aspects of Schottky contact fabrication

In the preceding sub-sections the importance of certain device parameters to high frequency varactor operation has been discussed. In Schottky diode fabrication schemes, practical ways to achieve the required junction area and interface quality must be found. In addition, mechanical and thermal considerations come into the choice of metallisation employed. The following pages contain a review of reported processing procedures that have been adopted in the fabrication of sub-mm mixer and multiplier diodes.

The University of Virginia has an established reputation in the area of diode fabrication and many references for processing have originated there. In [26] Bishop and Li describe a processing sequence suitable for plated platinum diodes. These diodes are of the planar type (discussed in section 2.6). Both planar diodes and arrayed diodes suitable for whisker contacting require surface treatment before metallisation, as well as carefully controlled plating conditions. Methods developed for preparation and plating are transferable to either type of diode configuration.

The processing carried out by Bishop begins with patterning of the SiO_2 passivation layer so that ohmic contacts can be evaporated in a lift-off process. Established recipes exist for the purpose of ohmic contact formation [27, 28]; most involve gold/germanium and a capping layer to seal the outer contact layer and direct the diffusion of the germanium into the GaAs substrate during alloying. Electroplating gold onto the alloyed ohmic pad helps in producing low contact resistance when the device pad is bonded to the external circuitry.

The SiO_2 layer is subsequently patterned to form circular via holes through which the anode plating will occur. Optical lithography is employed to pattern an approximately $1 \mu m$ thick layer of photoresist (a photosensitive polymer – see section 4.1.1) with the desired anode layout. The insulating dielectric layer is selectively etched through the via holes developed away in the photoresist. In [26], the etching process began with reactive ion etching (RIE), a process that allows etching of a specified material via a reactive species generated from a plasma [29]. This method is anisotropic and provides via holes with vertical sidewalls, but is thought to introduce

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surface damage to the substrate if the etch is continued all the way through the SiO_2 layer. Typically the RIE stage is continued until around 50nm of the passivation layer remains. Buffered HF is then used to remove the final trace layer of SiO_2.

The native oxide layer that forms on GaAs must be removed if an intimate contact is to be formed between metal and semiconductor. Bishop initially employed a wet-etchant composed so as to oxidise the GaAs (using H_2O_2), then etch the resulting oxide layer (using NaOH). This etchant, for given component concentrations H_2O_2/NaOH/H_2O (1:1:10), etches GaAs at a rate of 0.38µm/min [29].

Surface oxides and/or the presence of contaminants at the device interface layer can severely inhibit the operation of a Schottky diode, so much emphasis has been placed on developing techniques to produce interfaces which are clean and oxide free. The technique of anodic etching is described in section 2.5.1 and was employed by Bishop and Li in their processing scheme, prior to electroplating the anodes. This step is necessary in order to remove the film of oxide that will grow in the intervening time between the native oxide etch and the electroplating stage.

The diodes were then plated. The paper does not describe the platinum plating solution used, but based on the application of the pulse-etch method [30, 31], 'Low-Stress' Platanex [section 5.1] was the probable choice. A typical apparatus set-up for electroplating diodes is shown in fig. 2.5. Platanex is most effective at elevated temperatures (50-80°C) so a means of heating the solution is essential. Agitation (usually via a stirrer) is employed to aid regeneration of the electrolyte around the anode vias. After a continuous layer of platinum is deposited, each anode is capped with gold (via electroplating) to improve contact reliability.

Following the method detailed in [26] and above, Bishop achieved diode characteristics that, at first, showed creep (movement of the forward voltage knee following application of reverse bias) and low reverse breakdown. Counter measures employed to prevent these negative aspects of the diode characteristics involved removing H_2O_2 from the oxide etch (for improved V_{br}) and opening large sacrificial plating areas near the ohmic pads. The latter step was adopted to prevent galvanic

corrosion of the anode areas. Results reported following these revisions were much improved.
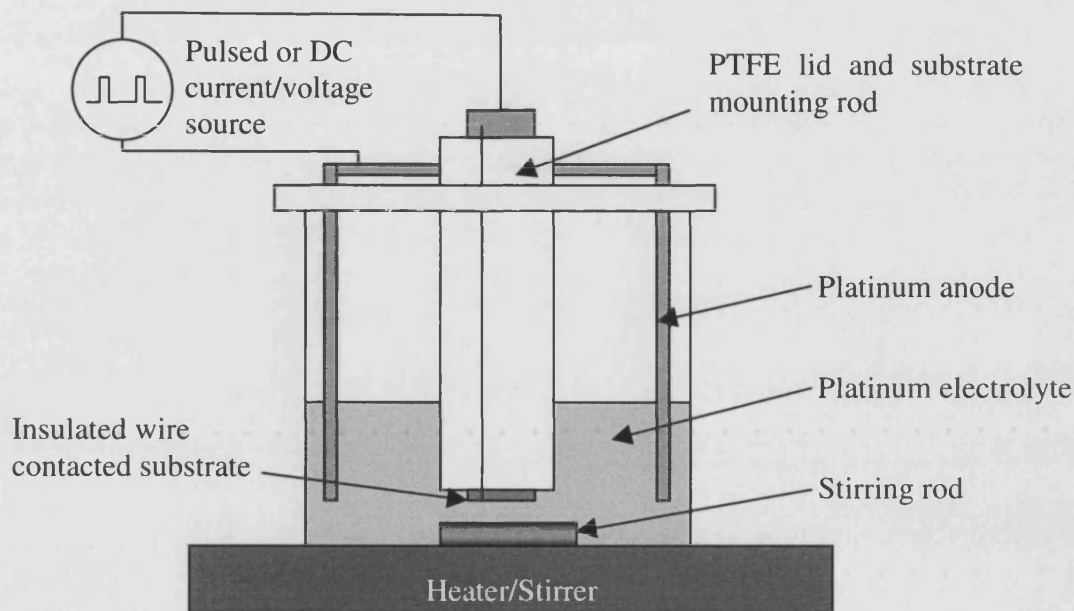

Figure 2.5. Typical apparatus for electroplating of platinum diodes

2.5.1 Anodic etching of GaAs anode interfaces

As mentioned in the previous section, elimination of surface oxide from the interface of a diode is a desirable fabrication goal that cannot be achieved with complete success using a pre-plating wet-etch. A novel technique has been developed that allows removal of native oxide from the GaAs via the platinum plating solution required for electroforming the anodes [30, 31]. In this way and by simply switching the polarity of the applied voltage, plating can begin immediately after the anode surface etching is completed.

The procedure is based on the fact that the Electrolyte/GaAs junction behaves like a Schottky junction. Application of a large reverse voltage drives the junction into avalanche breakdown. During the impact ionisation in the space charge region, electron-hole pairs are generated. The holes drift to the GaAs/electrolyte interface where they assist in anodic dissolution of the GaAs. In [30], 25V pulses of duration

0.3μs were applied to arrayed 0.8μm diameter GaAs vias at intervals of 4ms. The etch rate for the n GaAs epilayer was found to be 4nm/pulse. The reverse voltage is pulsed in order to permit regeneration of the platinum plating solution and prevent saturation effects.

This method provides a simple means of producing nearly oxide free Schottky junctions. Excellent control and reproducibility have been reported and the etch-profile is shown to be anisotropic, thereby proving the technique suitable for very small diameter anode formation. Idealities ranging from 1.04 to 1.18 are reported for doping concentrations ranging from $2 \times 10^{16} cm^{-3}$ to $2 \times 10^{17} cm^{-3}$.

2.5.2 Comparison of evaporated and electroplated platinum diodes

In a paper by Marsh and Pavlidis [32], evaporation was compared with electroplating as a means of forming Schottky contacts on InGaAs. Evaporation was carried out using an electron beam evaporator.

The plating solution adopted for the electroformed anodes was Enthone Platanex III a platinum plating solution based on sulfamic acid with a pH of 1.5 at 80°C. The solution etches InGaAs and GaAs rapidly and the authors found it necessary to apply a plating voltage across the anode and sample before immersion. This measure immediately sealed the open GaAs with platinum and prevented excessive anodic etching. Reverse voltage pulsed anodic etching was not attempted due to the high etch rate of the unbiased plating solution. A pulse plating technique [33] was used to plate the anodes. This technique uses a switched capacitor circuit to provide periodic voltage pulses. For a diode chip measuring 1.5 x 3.0cm, the plating conditions were applied voltage 8.5V, peak current 4A and duty cycle 1μs on, 1ms off. The duration of the plating was 17s. The authors aimed to exceed 50nm to prevent diffusion of the gold through the platinum layer. An upper limit of 150nm was set based on evidence suggesting that thicker films tended to have high in-built stress. This caused larger diodes to pull away from the substrate causing fracture within the InGaAs substrate.

After mechanical and electrical tests were performed on the evaporated and plated diodes, the authors found the plated variety to be a more reliable choice. The plated diodes had higher yield (80% successful junction formation) and idealities were

consistently in the region of 1.2. By contrast, the e-beam-evaporated diodes had yields as low as 5% and idealities in the range 1.4-1.66. Plated platinum anodes had noise temperature ~220K compared with ~360K for evaporated anodes. The plated diodes also exhibited higher mechanical strength. Fracture tests resulted in 92% of the plated diodes causing fracture within the InGaAs whilst 69% of the evaporated diodes broke at the interface.

The authors also make comparison with plated and evaporated anodes on GaAs. A titanium diode formed by evaporation achieved an ideality of 1.19 compared with 1.14 for a plated platinum diode on the same material.

A wide spread in the evaporated diode characteristics was attributed to confinement of the diode current to areas smaller than the plated area, due to inhomogeneous contact of the evaporated metal to the GaAs. It was believed that the significant differences in the measured IV curves indicated varying effective device areas.

2.5.3 Schottky fabrication using sputtered metal

Work has been conducted at the National Microelectronics Research Centre (NMRC) [34, 35] on Schottky diodes formed using sputtering rather than electroplating. A processing route is described in [34] using sputtered tungsten and reports increased thermal stability when these are compared with platinum diodes.

The processing running up to the formation of these anodes is essentially identical to that described in [26] and section 2.5. RIE is used to remove SiO_2 through via holes formed in photoresist. Due to the high temperatures incurred during sputtering it was deemed necessary to deep UV expose the resist layer, thereby preventing thermal flow in the layer up to 210°C [36]. Once again the final 70nm of SiO_2 was removed using a dilute buffered HF solution to minimise damage at the GaAs surface. This wet etch, being isotropic, caused fractional under-cut of the SiO_2, a useful characteristic for the subsequent lift-off process which leaves the anodes isolated in the passivation layer.

This method yielded ideality factors of around 1.18 for micron and sub-micron sized junctions. Deviations from the ideal were attributed in the main to damage caused by the sputtering process.

In order to simulate thermal ageing, the samples at NMRC were subjected to annealing temperatures of 500°C for a period of 20 minutes (in a forming gas atmosphere $H_2:N_2 - 5\%$ H_2). These tests resulted in an improvement in the ideality factor from 1.18 to 1.14. Increasing the temperature of the annealing step caused the metal to peel from the substrate.

A follow-up paper [35] was published in 1991 and listed more characteristics taken from annealed diodes. The aim of the work presented in this paper was to assess the thermal annealing process in terms of its ability to reduce noise in fabricated devices. At device current 1mA the thermally annealed device exhibited a noise temperature of 280K compared with 360K for the device undergoing no annealing stage. The relative stability of the ideality factors at high temperatures indicates that the W/GaAs interface is resistant to interdiffusion. W acts as a diffusion barrier to the gold cap layer, which is deposited to minimise the resistance when the device is whisker contacted. Platinum/gold metal layer structures on GaAs are reported to be subject to interdiffusion effects at temperatures as low as 150°C.

A rapid thermal annealer was purpose built for the experiments detailed in [35]. Ramping from room temperature up to 700°C was achievable in 30s at a pressure of 200 mT. The finalised ramp characteristic consisted of a ceiling temperature 600°C (held for 2mins) ramped from room temperature in 30s.

2.5.4 Temperature effects for various metallisation schemes

Keen [37] reviewed results from various studies into Schottky diode performance. In this paper it is stated that based on reliability tests [38], Ti/Pd/Au and Ti/Pt/Au diodes seemed the best choice for low noise mixer diodes. The comment is made that in view of the fact that platinum readily diffuses into GaAs at temperatures above 150°C, it is not entirely clear whether good device characteristics always mean simple junctions.

Sinha and Poate [39] carried out an investigation into thermal ageing effects on platinum, tungsten and gold diodes. Tungsten was shown to provide the greatest thermal stability as in [34] but improvements in the diode ideality factor were witnessed for platinum diodes undergoing a 350°C annealing stage. The tungsten and platinum diodes used in this work were formed via sputtering whilst the gold was thermally evaporated.

I/V data is presented that shows the ideality of a 250μm-diameter platinum Schottky anode as prepared and after annealing at 350°C and 500°C. The ideality as prepared was 1.29 compared to 1.15 following annealing for two hours (under vacuum) at the lower temperature. Following similar annealing at 500°C, the ideality was found to be 1.19, an increase attributed to significant out-diffusion of Ga into the platinum and formation of $PtAs_2$ near the Schottky interface.

In a later paper by Sinha et al. [40], n-GaAs Schottky diodes metallised with Ti and Pt/Ti layers were subjected to thermal ageing processes. Ti/n-GaAs diodes showed near ideal forward characteristics (n=1.03) with no measurable inter-diffusion taking place at 350°C. At 500°C TiAs formed but no significant change in the barrier height or ideality was observed. Platinum diodes were formed using RF sputtering, whilst titanium diodes were e-beam evaporated and Ti/Pt diodes were produced using sequential e-beam evaporation.

The I/V results presented for the Pt/Ti/GaAs junction showed an ideality that improved from 1.22 to 1.05, following a 2-hour anneal at 350°C. This layer structure essentially behaved as a Pt junction following annealing at 500°C, with the Ti layer failing to prevent interdiffusion of the Pt and GaAs. As a result, the diode ideality changed from 1.05 to 1.13.

2.6 Planar diode construction

Boccon-Gibod and Harrop presented an alternative diode contacting mechanism [41] in 1978 and this device has since evolved into a genuine rival to the whisker contacted variety. The diode is positioned close to an ohmic pad and contacted by a finger that extends from a gold contact pad. The substrate between the ohmic and gold contact pads initially supports the finger, but is subsequently etched away to leave the finger

as an air-bridged contact to the device. In this manner, the parasitic capacitance of the planar diode is greatly reduced. Fig. 2.6 shows a typical planar Schottky device layout.

This technology, whilst not quite matching the high end cut-off frequency of whisker contacted diodes, affords greater flexibility in the mounting of devices and allows cascading of devices to form parallel and series connection of diodes within a waveguiding structure [42]. Since the diode is contacted using an electroplated feature, its mechanical strength exceeds that of conventional whisker contacted assemblies. In addition, planar diodes are well suited to contact via stripline, thus enabling effective incorporation into bias and IF strip-type circuits in mixers and multipliers.
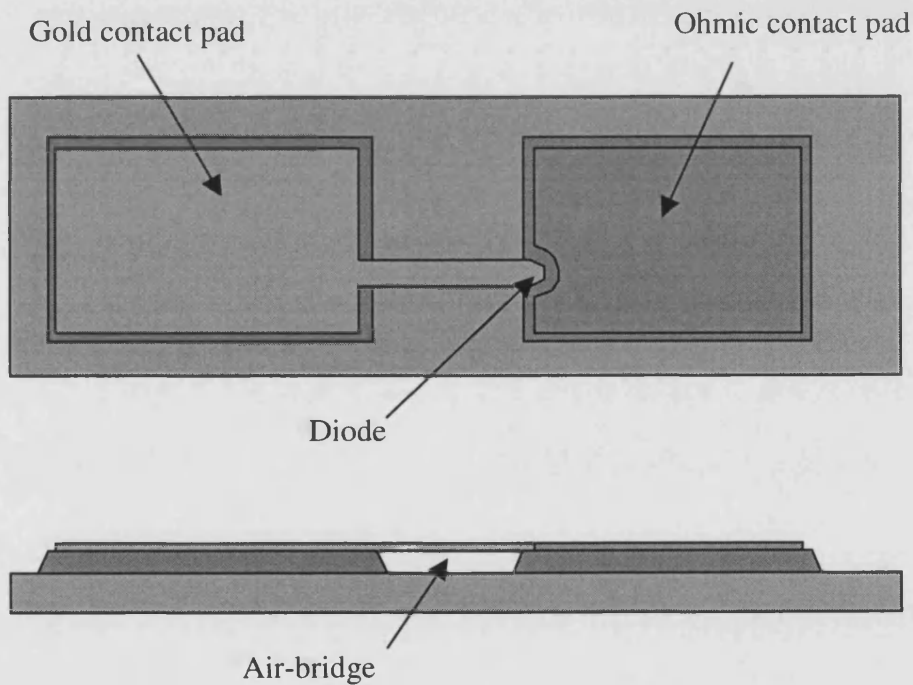
Figure 2.6. Schematic aerial and side views of a typical single planar diode.

In [41] the Schottky diode was fabricated using an evaporated aluminium layer. An ideality of 1.07 and a series resistance of 1.5Ω were recorded. This device had considerably higher contact area than would be required for a sub-mm wave varactor. The total capacitance measured at 1MHz was 90fF, corresponding to a figure of merit

cut-off frequency (RC) of 1.2THz. Other geometries were fabricated with a maximum calculated cut-off frequency of 2THz.

Since this paper was published, numerous groups have fabricated planar diodes and developed methods for reducing the parasitic capacitance of these devices [43, 44]. One method employed to achieve low parasitic shunt capacitance involves complete removal of the substrate connecting the two contact pads. A wet-etch is performed down to an etch-stop layer, after the diode is flip-mounted on a quartz substrate carrying the stripline filter.

Reported idealities are as good as those obtained for arrayed diodes. However, for applications involving signal frequencies above around 600GHz, whisker contacted diodes still offer lower associated parasitics than planar diodes.

2.7 Heterostructure varactor diodes

Single barrier varactors were developed from quantum well diodes. It was realised that in QWD multipliers, the non-linear device capacitance provided the majority of the harmonic power whilst the resistive effect of the device degraded the performance. Thus, the non-linear current through the device was suppressed by using a barrier of increased width.

The layer structure for a single barrier varactor based on GaAs is shown in fig. 2.7. Jones et al. [45] provide typical details on layer thickness and doping concentration for a dual stacked varactor. An AlGaAs barrier is at the centre of the device and this blocks current flow. In [45] this barrier is 20nm thick. On either side of this barrier are undoped GaAs spacers (thickness 3.5nm). The GaAs depletion regions (N_d=8 x 10^{16}cm^{-3}) are 250nm in thickness. After MESA etching, the n+ top layer and n+ substrate layer are contacted using metallised ohmic pads.

When a voltage is applied to the device, a depletion layer forms on one side of the barrier. The length of this depletion region increases with an increase in the applied voltage. The other side of the barrier is accumulated and the total capacitance is the series combination of the barrier, depletion and accumulation region capacitances. Most of the capacitance change occurs on one side of the barrier, due to the

modulated depletion region. When the voltage across the device is reversed, the device symmetry leads to a swapping of roles for the two n-GaAs regions. Hence the single barrier varactor has a symmetric C/V characteristic with a maximum value at zero bias.

As a device with a symmetrical nonlinear capacitance/voltage characteristic, single barrier varactors offer some significant advantages over Schottky junction varactors. A particular benefit is that only odd order harmonics are generated, thereby easing idler circuit requirements. Single barrier varactor frequency triplers only require current flow at the fundamental, whilst quintuplers can be realised with a single idler circuit, resonant at the third harmonic. A further advantage, that again simplifies circuit design, is the zero bias operating point. Thus, a DC path is not necessary for a multiplier based on this device.
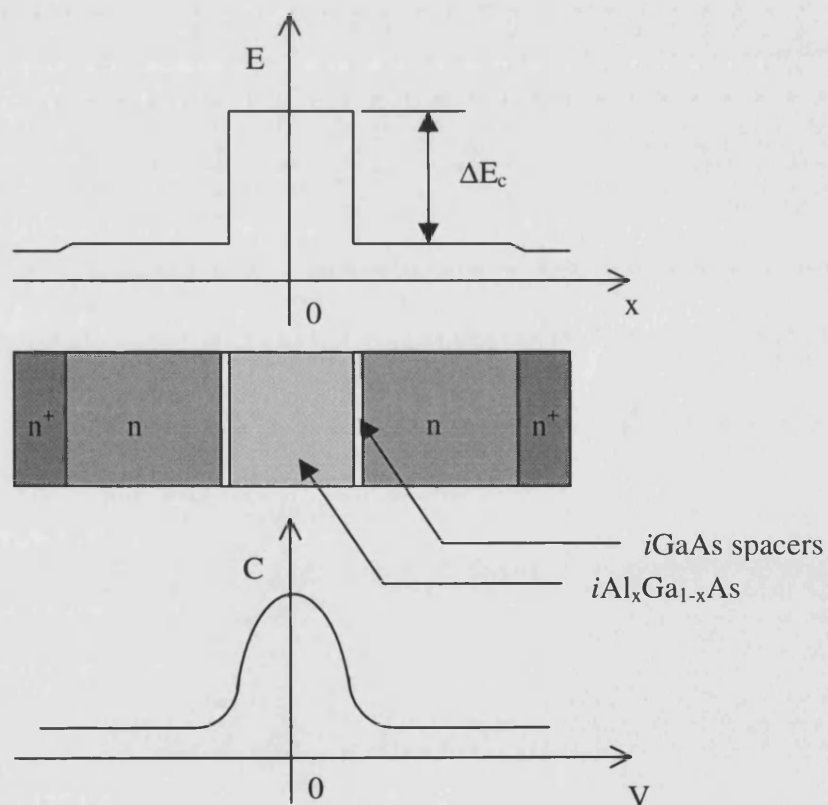
Figure 2.7. Layer structure, electric field and capacitance voltage
characteristic for a single barrier varactor.

Additional benefits can be reaped if multiple barriers are stacked to form heterostructure barrier varactors. Most importantly, this technique allows device power handling to exceed that achievable with Schottky devices. In early HBV devices, current leakage through the barrier caused low performance but using modern layer deposition systems and techniques, this problem has been overcome and high efficiencies have been reported. In 1997 Jones et al. [45] reported an efficiency of 2.5% for an 80-240GHz tripler incorporating two, four-barrier HBV devices. Mélique et al. [46] reported 5% efficiency and 5mW output power at 216GHz for an InP based HBV tripler in 1998 and in 1999 12% efficiency was achieved for a 250GHz tripler once again using multiple InP based HBVs [47].

Unfortunately, single barrier and heterostructure barrier varactor material is still difficult to fabricate and due to its complexity, is more expensive than simple Schottky varactor material. In addition, the mesa structures necessary to define the area of the HBV are more difficult to contact using the etched whisker method. Heterostructure barrier varactors are nevertheless an extremely attractive alternative to conventional Schottky varactors and when combined with the planar technology described in section 2.6, offer high efficiency, power handling and circuit matching capabilities [45, 46, 47].

2.8   Chapter summary

This chapter has described the basic principles of Schottky diode formation and varactor operation. Schottky varactor modelling techniques have been reviewed and the key attributes of several previously used submillimetre multiplier diodes have been presented (table 2.1). Based on the design methods of Louhi and Räisänen [11, 12, 13, 14] and using equations from Lipsey and Jones [7], a layer structure for the intended 810GHz tripler has been derived.

After selection of the doping and thickness properties of the n-epilayer, the quality of the diode rests with surface preparation and metal deposition. Various metallisation schemes were discussed in this chapter and of these, platinum, titanium/platinum, titanium/palladium and tungsten seem to offer the most reliable combination of thermal, mechanical and electrical properties. With the apparatus available for this project electroplated platinum is possible, as is evaporated titanium and palladium.

The fabrication of devices employing these layers will be detailed in chapter 4. In his evaluation of various metallisation schemes, Keen [37] states that at the heart of devices with high ideality complex junctions may exist that do not fit the pure metal/semiconductor interface model. Evidence from annealing studies seems to support this view. It is clear however, that techniques such as the reverse anodic etching described in [30] are extremely valuable in preserving a high quality junction directly prior to electroplating. The validity of the reverse pulse etching method of anode preparation has been established [31] by comparison with devices whose interfaces were momentarily exposed to atmosphere prior to plating.

When reviewing the literature it is apparent that excellent idealities are often reported for larger diodes, but near-ideal diodes become increasingly difficult to produce as the diameter of the oxide via decreases. Grüb et al. [48] offer reasons for this effect including reduced Pt mobility in the electrolyte and varying crystallinity in the polycrystalline platinum film constituting the anode. For anodes with diameters comparable to a micron, perimeter field effects are thought to affect the growth centres for the Platinum within the anode via. Pulsed plating was proposed as a possible means to reduce this effect and allow the electrolyte to replenish itself around the anode region. Burrus [33] had already described this technique as a means to plate substrates with low conductivity and very small areas open to the electrolyte. Constant current pulse plating was employed for electroplating the diode arrays described in chapters 4 and 5.

It was anticipated that HBV devices would be fabricated for use with the tripler featured in this project, thereby reducing the complexity of the microfabricated waveguide circuit. Unfortunately, HBV material proved difficult to source and the devices used for both the doubler and tripler were single Schottky diodes, selected from an array of identical devices (in a similar manner to conventional whisker contacted devices).

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3. Design and Modelling

3.1   Design of micromachined sub-mm wave components

In order to begin designing a frequency multiplier that may be fabricated as a micromachined structure, it is necessary to understand the constraints imposed by the available micromachining methods. The following sub-section briefly describes how micromachining considerations have acted alongside circuit requirements in defining the tripler, doubler and detector processing schemes featured in chapter 4. For greater detail on processing, basic semiconductor lithography is covered in more depth in section 4.1. Sections 4.2 and 4.4 describe the thick photoresist techniques that were developed for use in multiplier and passive component fabrication sequences.

3.1.1   Advantages and limitations

Accurate patterning of a semiconductor substrate is a fundamental requirement of any semiconductor processing. One method of achieving this is with optical photoresist, a photosensitive polymer that can be developed after selective exposure to ultraviolet light. The desired pattern is translated into a resist layer using a mask aligner and a chrome-on-glass mask plate. The mask is brought into firm contact with the resist layer and accurate substrate/mask alignment is achieved with a microscope and micro-adjustable X-Y stage. The mask itself is produced using electron beam writing techniques, and is designed using commercial software. An ultraviolet bulb (with lens assembly) provides UV exposure.

Since micromachining can be achieved with photosensitive resists, accurate location and dimensioning of components is an inherent feature. This accuracy is afforded in the two dimensions parallel to the substrate/mask. Dictating the perpendicular height above the substrate (often a waveguide height) is more difficult to achieve but methods that allow reasonable control of this dimension have been investigated as part of this project (section 4.3). The thickness of a single layer of resist on a flat substrate can be accurately controlled, so the simplest useful structures that can be produced have no vertical steps or tapers and are formed from a resist layer imaged via a single exposure and development.

SU8 is a relatively new epoxy based resist that became available mid-way through this project. An application of this resist that was immediately apparent was in the fabrication of tuning components. The mechanical properties of the epoxy based substance and its resilience in the presence of plating and etching chemicals allowed solid movable tuning stubs to be produced. Additionally, SU8 layers up to 800μm thick could be exposed and developed successfully, allowing standard height tuners and waveguides with cut-off frequencies below 100GHz to be fabricated.

Varactor multipliers are notoriously difficult to optimise so the flexibility afforded by tuning circuits is often essential. However, the simplest micromachined structures to fabricate are fixed-tuned and therefore fixed structures were selected as a primary goal for the project. Initially, doubler and tripler structures were demonstrated in fixed-tuned form and features allowing variable circuit tuning were added later.

3.1.2 Prototype multiplier circuits

Before embarking on the modelling phase of this project, prototype multiplier circuits were designed, with boundaries imposed by the processing methods available in-house. These structures formed the basis for the subsequent finite element and equivalent circuit modelling detailed later in this chapter.

As a first measure, it was decided that multiplier structures with no E-plane height changes would be adopted. This decision was made at a time when conventional AZ resist was the primary tool for forming waveguides. Modern negative resists enable multi-layer/multi-height processing, but it was decided to maintain simplicity in the E-plane for the first multiplier schemes.

It has been noted that height changes can be difficult to achieve using thick photoresist processing whilst patterning in the H-plane can be controlled to within a few microns. For this reason a filter design based on H-plane irises was used to provide harmonic rejection within the frequency doubler input circuit. Similarly, transformers with steps or tapers in the broad wall dimension were possible and again, these were utilised in the frequency doubler.

Stripline low-pass filters occur in many conventional split-block multipliers and provide an effective means of separating input and output circuits. SU8 processing made it possible to create dielectric layers with surface areas accurately controlled via optical lithography. Hence, a design was pursued that would incorporate a stripline filter with a dielectric SU8 layer formed directly on the GaAs substrate.

With all the above considerations in mind, two distinct fabrication schemes were selected. The first would produce a frequency doubler and the second would be used in order to produce a tripler. Common features of both were a pre-formed dot matrix array of varactor devices coupled to an integrated electroplated device contact.

The contact post on the doubler was full-height and based on a stacked arrangement featuring the novel electroplated whisker contact described in section 4.5, allied to a larger, lithographically formed, electroplated post. The tripler featured the same smaller whisker contact but connected directly to the stripline filter. This stripline filter would provide harmonic rejection on the tripler input circuit, whilst the doubler would feature the aforementioned H-plane iris filter to perform the same task.

The remainder of this chapter includes modelling methods employed to derive optimum embedding impedances for an ideal multiplier, then describes finite element and equivalent circuit modelling as applied to the prototype multiplier designs. Finally, the chapter provides surrounding theory on the passive components that act as constituent parts of the proposed multiplier designs.

3.2   Modelling methods

Figure 3.1 shows the general circuit for a varactor frequency multiplier. It consists of input and output matching circuits, a varactor and a number of idler resonators. Designing the multiplier requires selecting a device with suitable characteristics based on intended operating power and frequency, then finding the optimum embedding impedances for this device at the fundamental, idler and output frequencies.

One of the first recognised methods for designing varactor frequency multipliers came from Penfield and Rafuse [1]. Their analysis was based on the assumption that a nominally driven abrupt-junction diode was employed. The analysis procedure

applies to multipliers from doubler to a general multiplier with output frequency nf. This approach saw some refinements [2] before Burckhardt published an analysis that still provides a useful starting point for submillimetre-wave varactor multiplier design [3]. The Burckhardt method is reviewed and employed to derive embedding impedance and efficiency data (for a doubler and tripler) in section 3.3. Comparison is made with results obtained from a downloadable doubler design tool from the University of Virginia [4]. Section 3.4 describes the modelling procedure adopted for optimisation of the MEMS multiplier circuits. The chapter then contains detail on constituent elements of the final multiplier circuits, including waveguide filters, tuning elements and transformers.
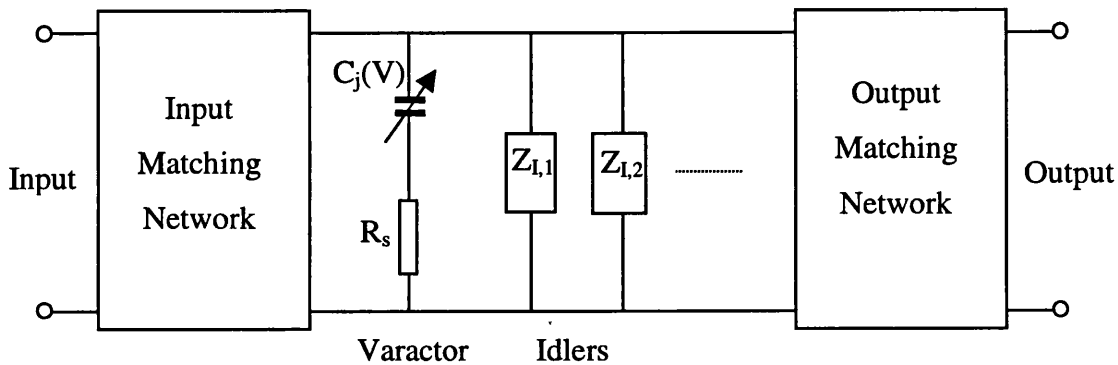
Figure 3.1. Circuit diagram for a varactor frequency multiplier.

3.3 The Burckhardt method

In this analysis, results were generated by a computer program and presented in normalised tabulated form. The paper considers varactor multipliers with any integer multiple ratio of output to input frequency. Loss in the device is included and all idler configurations and various voltage/charge relationships are encompassed.

The assumptions made by Burckhardt are:

1.   Idlers are short-circuit series resonators.

2.   Only input, output and idler currents are considered in the diode.

3.   The idler, input and output circuits series resonate with the average diode elastance.

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4.   The diode junction is driven between the reverse breakdown voltage and ϕ (although the overdriven case is also described).

5.   The varactor's dynamic Q at the output frequency is greater than 50.

6.   Constant diode series resistance is assumed for the tabulated values. Correction factors that apply to the calculated efficiency are included for varying series resistance. All other calculated parameters are reported to lie within 10% of their respective values for the fixed resistance case.

7.   Circuit loss is not included, hence the calculated efficiency and power are the highest achievable values.

This design method differs from those proposed by Penfield and Rafuse [1] and Morrison [2]. As stated previously, Penfield and Rafuse restricted their analysis to nominally driven abrupt junction varactors whilst Morrison considered a lossless diode and concentrated on maximising input power for prescribed breakdown and drive. The Burckhardt method is considered as an extension and generalisation of these earlier works.

3.3.1   Tripler and doubler designs

Using the normalised Burckhardt values, optimum source, idler and load impedances were derived for a doubler (no idlers) and a 1-2-3 tripler (second harmonic idler). As with all design methods for varactor frequency multipliers, the first requirement is to determine the device parameters that will lead to efficient multiplication above the fundamental input frequency. Once the device parameters are known, the required harmonic embedding impedances are calculated and the idler and input/output circuits are designed accordingly. For the following designs, parameters from fabricated devices were input alongside those from optimised [5] diodes. Results from the analysis using fabricated and state-of-the-art devices were compared in order to illustrate any problems that would arise in circuit realisation given device characteristics that were not optimal.

3.3.2   1-2-3 tripler

Optimum diode: Required device parameters for the Burckhardt analysis are zero bias capacitance, breakdown voltage, built-in voltage, series resistance and capacitance variation. For a state-of-the-art Schottky device, suitable for harmonic

power generation at 800GHz [5], these are $C_{j0} = 5.0\text{fF}$, $V_b = -8.0\text{V}$, $V_{bi} = 0.7\text{V}$, $R_s = 8\Omega$ and $\gamma = 0.5$. The maximum junction voltage achievable without forward conduction (V_j) is also needed in the analysis and this is estimated to be 0.6V. The fundamental frequency was selected as 270GHz.

Drive	α	β	$R_{in}\omega_1/S_{max}$	$R_L\omega_1/S_{max}$	$S_{0,1}/S_{max}$	$S_{0,2}/S_{max}$	$S_{0,3}/S_{max}$	$V_{dc,n}$
1.0	11.6	0.0241	0.137	0.0613	0.50	0.50	0.50	0.32

Table 3.1. Design parameters for frequency tripler [3,6].

Table 3.1 shows all necessary parameters for carrying out the Burckhardt analysis given the characteristics of the varactor. α and β are scaling parameters for the calculated efficiency and power. The Drive parameter is unity if the diode is driven from reverse breakdown to the point at which forward conduction occurs. Table 3.1 includes the normalised source and load resistances R_{in} and R_L and the average junction elastances at the source ($S_{0,1}$), second-harmonic idler ($S_{0,2}$) and output ($S_{0,3}$) frequencies. These elastances should be resonated by the source, idler and load networks. Finally, the normalised bias voltage, $V_{dc,n}$ is included.

The diode will not be driven into forward conduction so the drive level will actually be slightly less than 1.0. This is a necessary but trusted approximation (tabulated parameters for drive less than 1.0 are not provided).

The first step in the calculation is to find the maximum and minimum elastances (S_{max} and S_{min}) achievable within the drive range. The capacitance voltage relation is,

$$C(V) = \frac{C_{j0}}{(1 - \frac{V_b}{V_{bi}})^{\frac{1}{2}}}, \qquad (3.1)$$

where C_{j0} is the zero bias capacitance, V_b is the bias voltage and V_{bi} is the built-in potential. At reverse breakdown this relation yields 1.4fF as the capacitance, whilst at the bias point just before forward conduction, the capacitance is 13fF. Hence the elastances S_{max} and S_{min} are $7.1 \times 10^{14}\text{F}^{-1}$ and $7.6 \times 10^{13}\text{F}^{-1}$ respectively. The dynamic Q is defined as,

$$Q_\delta = \frac{S_{max}}{2\pi f_c R_s},$$ (3.2)

where R_s is the diode series resistance and the dynamic cut-off frequency f_c is defined as,

$$f_c = \frac{S_{max} - S_{min}}{2\pi R_s}.$$ (3.3)

For the given maximum and minimum elastances, the dynamic cut-off frequency is 13THz and the dynamic Q evaluated at the third harmonic frequency is 17. Thus the dynamic Q falls well below the value stipulated by Burckhardt. However, Maas [6] performs a similar analysis based on a frequency doubler and achieves results that closely agree with harmonic balance simulation despite a dynamic Q of 19. Hence it is believed that inaccuracy due to this shortfall will not greatly affect the predicted output values.

The real components of the input and load impedances are calculated using the expressions

$$R_{in} = \frac{\alpha S_{max}}{2\pi f_1}$$ (3.4)

and

$$R_L = \frac{\beta S_{max}}{2\pi f_1}.$$ (3.5)

The complex parts are found from the relation (table 3.1) giving the harmonic elastances in terms of the maximum achievable elastance,

$$\frac{1}{S_{0,1}} = \frac{1}{S_{0,2}} = \frac{1}{S_{0,3}} = \frac{1}{0.50(S_{max})}.$$ (3.6)

Hence, the required harmonic capacitance is 1.57fF and the source, idler and load impedances are according to Burckhardt's analysis, $Z_{in} = 57 + 210j\Omega$, $Z_{2nd} = 0 + 100j\Omega$, $Z_{load} = 25 + 69j\Omega$.

The bias voltage and predicted efficiency are given by,

$$V_{bias} = V_{bi} - V_{dc,n}(V_{bi} - V_b)$$ (3.7)

and

$$E_c = \exp\left[\frac{-\alpha}{Q_\delta}\right].$$ (3.8)

The output power is given by

$$P_L = \frac{\beta\omega_1}{S_{max}}(V_{bi} - V_b)^2.$$ (3.9)

Given the calculated load, source and idler impedances the tripler will then have 4.4mW of available output power and 51% efficiency, assuming a lossless circuit. The DC bias point should be –2.1V.

Fabricated diode: The diode fabricated at Bath for use in the tripler had C_{j0} = 5.0fF, V_b = -6.0V, V_{bi} = 0.7V, R_s = 12Ω and γ = 0.5. The maximum junction voltage achievable without forward conduction (V_j) was estimated at 0.5V. Using the same analysis method as in the preceding section yielded the following results for the harmonic embedding impedances and bias: Z_{in} = 28 + 100jΩ, Z_{2nd} = 0 + 51jΩ, Z_{load} = 12 + 34jΩ, bias = +0.03V. Theoretical available load power and efficiency were 0.5mW and 13%.

These figures are very different from those given for the optimised diode. The reason for the discrepancy is attributable to the material used for the diode fabricated at Bath. The material provided for this project was essentially designed for mixer diodes. Consequently, a low reverse voltage (approximately 2 volts) would cause the depletion region to extend beyond the epilayer (section 2.2.6) and the capacitance variation would be minimal for reverse voltages above the punch-through value. In order to account for this in the Burckhardt analysis, a breakdown voltage with the same value as the predicted punch-through voltage was chosen. This effectively limited the extent of epilayer modulation range to between the punch-through and forward conduction points.

3.3.3 Doubler

Optimum diode: For a state-of-the-art device capable of producing output power in the 500-600GHz frequency band, C_{j0} = 6.0fF, V_b = -8.0V, V_{bi} = 0.7V, R_s = 8Ω and γ = 0.5 [5]. The maximum junction voltage achievable without forward conduction

(V_j) is needed and this is estimated to be 0.6V. Once again the fundamental input frequency is 270GHz.

Drive	α	β	$R_{in}\omega_1/S_{max}$	$R_L\omega_1/S_{max}$	$S_{0,1}/S_{max}$	$S_{0,2}/S_{max}$	$V_{dc,n}$
1.0	9.95	0.0277	0.080	0.1355	0.50	0.50	0.35

Table 3.2. Design parameters for frequency doubler.

Table 3.2 contains parameters as defined in the previous section. As the doubler requires no intermediate idler circuit, only normalised source and load elastances are included. The Burckhardt analysis yields the following results for the embedding impedances and bias: Z_{in} = 28 + 170jΩ, Z_{load} = 47 + 87jΩ and bias = -2.3V. Theoretical available load power and efficiency were 6.1mW and 63%.

Fabricated diode: The diode fabricated at Bath for the doubler had C_{j0} = 5.0fF, V_b = -6.0V, V_{bi} = 0.7V, R_s = 12Ω and γ = 0.5 (the same specification as the tripler diode). For a doubler circuit based on this diode the embedding impedances and bias were: Z_{in} = 16 + 100jΩ, Z_{load} = 27 + 51jΩ, bias = -0.04V. Theoretical available load power and efficiency were 0.6mW and 31%. As for the aforementioned tripler, these results differ significantly from the optimised submillimetre-wave diode with an epilayer tailored for reverse-bias varactor characteristics.

The harmonic-balance method for nonlinear microwave circuit analysis has provided a higher level of accuracy in varactor multiplier design than was possible with the closed form expressions given by Burckhardt. Lipsey, Jones et al. have produced a downloadable tool for varactor multiplier design [4], using coefficients obtained from a harmonic-balance program incorporating Monte Carlo device analysis [7]. Given user-defined fundamental frequency, resistance, device area and epilayer thickness/doping, the efficiency and embedding impedances (fundamental and second harmonic) are calculated. For the doubler diode fabricated at Bath, the results returned from this program (with 10mW input power) for embedding impedances and bias were Z_{in} = 14 + 100jΩ, Z_{load} = 31 + 56jΩ and bias = +0.21V. The predicted efficiency was 5%.

The embedding impedances correspond well with those given by the Burckhardt method, whilst the recommended bias from both analyses is essentially zero. A lack of bias requirement would to some extent be advantageous in a microfabricated multiplier, leading to simplified processing. However, these diodes have a very limited capacitance modulation range and according to the harmonic-balance program, a fundamental input power above 20mW would drive the diode into forward conduction. This would lead to power dissipation in the junction and a drop in efficiency.

3.4   HFSS and APLAC modelling

Having calculated the ideal embedding conditions required for efficient harmonic generation, a circuit must be designed to provide these impedances at the diode plane. In the early design stages of this project, scale models (x160) were used in conjunction with a Vector Network Analyser (VNA) to test waveguide filter designs whilst equivalent circuit modelling was employed to look at other passive circuit elements, including waveguide steps and transformers. This is a traditional method in microwave engineering, but the process of constructing the model and the restrictions inherent in a fixed mechanical structure have led to the development of a variety of Finite Element Method (FEM) passive structure CAD packages.

The first FEM modelling carried out for this project was performed with an early version of Hewlett Packard's HFSS package. This was run across a network and proved reliable only for simple components including iris filters and transformers. On upgrading to Ansoft's HFSS version 7.0, full modelling of simple passive multiplier circuits became possible. This passive circuit modelling was then augmented with APLAC, a software package developed at the University of Helsinki. This package allowed S-parameter data from HFSS to be imported and represented in an equivalent circuit as an N-port block. User-defined models for the Schottky varactor diode could then be included in the circuit and using an in-built harmonic balance analysis, circuit efficiencies predicted. APLAC has many optimisation facilities that make it a valuable tool for circuit tuning.

The following pages describe how doubler and tripler structures were developed using HFSS and APLAC. Both structures were developed with dimensional limits (eg.

achievable waveguide height) set by fabrication processes (see sections 3.1.2, 4.2 and 4.4), with APLAC and HFSS studies performed to assess the achievable efficiencies. At the outset of this project the target fundamental frequency for the tripler was 270GHz. On the basis that no harmonic idler was required, it was also decided to develop a fabrication scheme for a frequency doubler, again operating with a fundamental input frequency of 270GHz.

Figure 3.2 shows the HFSS representation of a tuner-less waveguiding structure designed as the passive circuit for the frequency doubler. An iterative approach was adopted for optimising the passive side of the doubler circuit. S-parameter data (first, second and third harmonic) was taken from the multiplier without tuners and imported into an APLAC circuit representation including shunt transmission line tuning stubs (fig. 3.3). In the doubler configuration shown in fig. 3.3 the dual offset tuning stubs are situated on the input side of the iris coupled band-pass filter (seen in fig. 3.2). This filter provided greater than 10dB rejection of the second harmonic power and consequently the tuning stubs acted predominantly as a device matching circuit for the incoming fundamental power. Hence, the lengths of the transmission line tuners were optimised based on the fundamental guide wavelength and effects due to higher harmonic interaction with these tuners could reasonably be ignored.
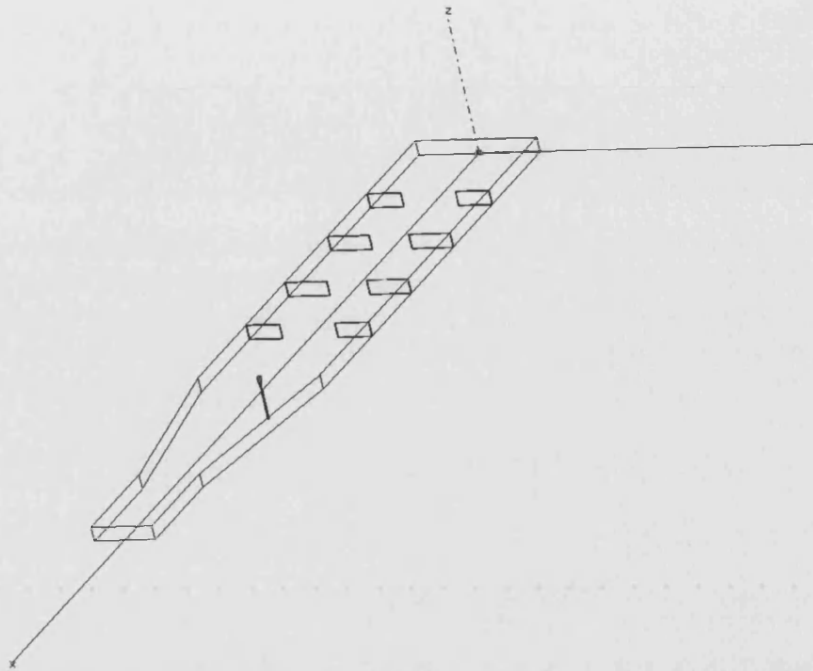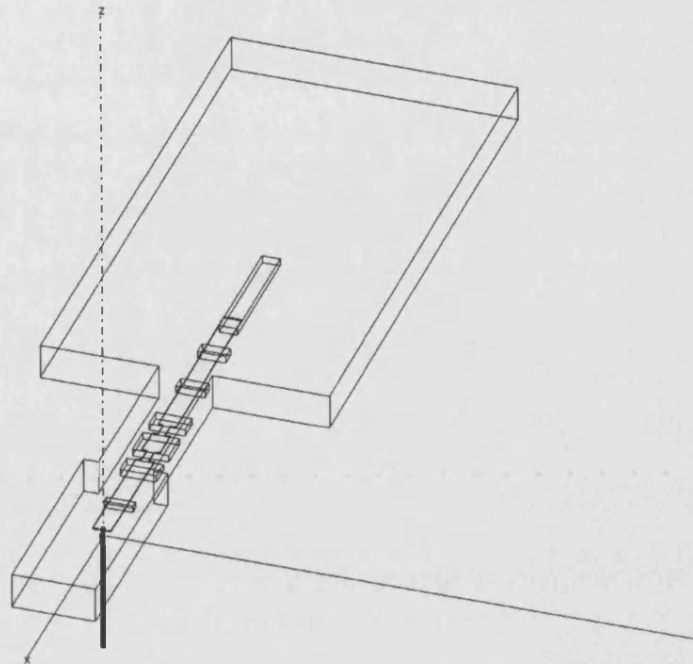
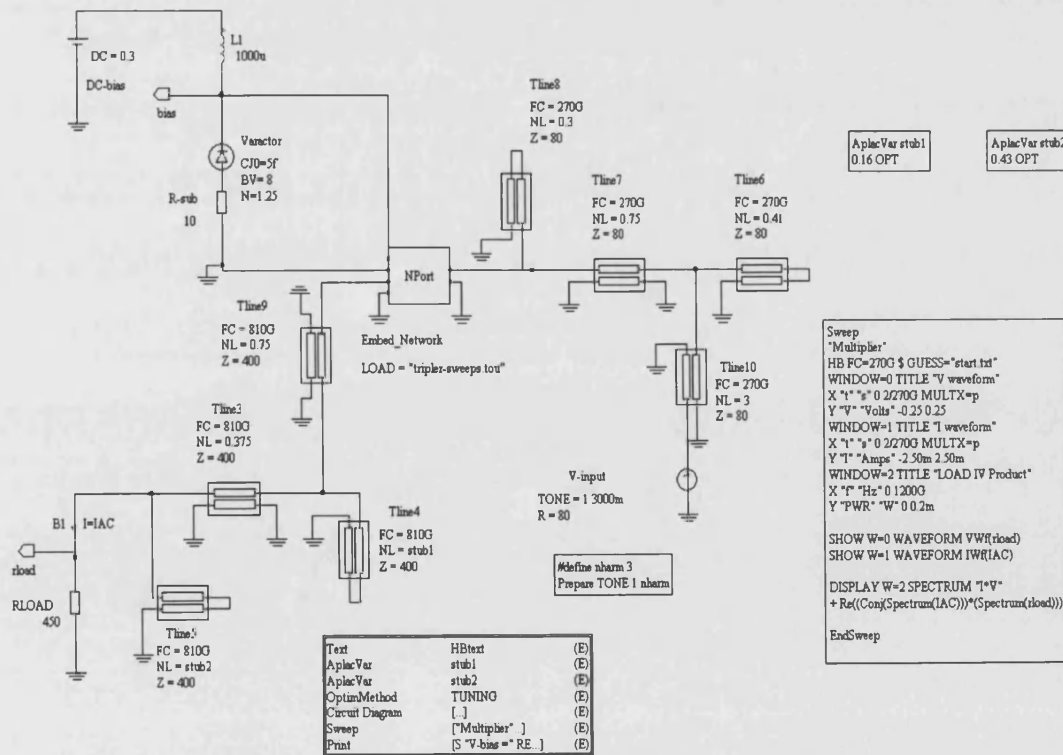Figure 3.2. HFSS 3-port representation of the frequency doubler embedding circuit.
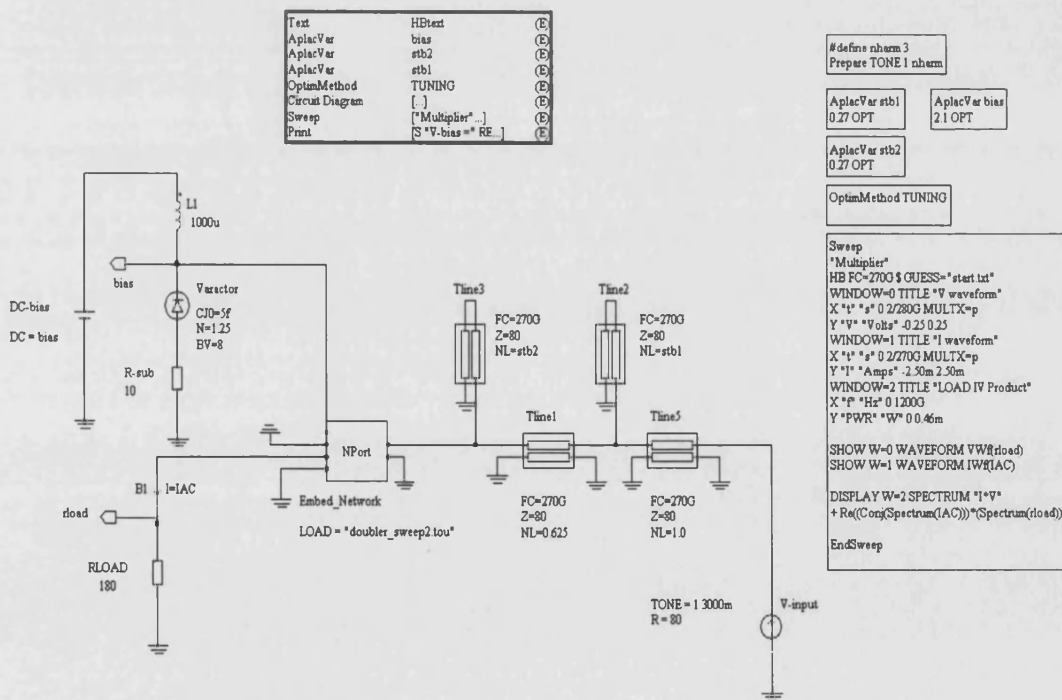
Figure 3.3. APLAC doubler circuit featuring 3-port S-parameter data from HFSS and tuning from transmission line stubs.
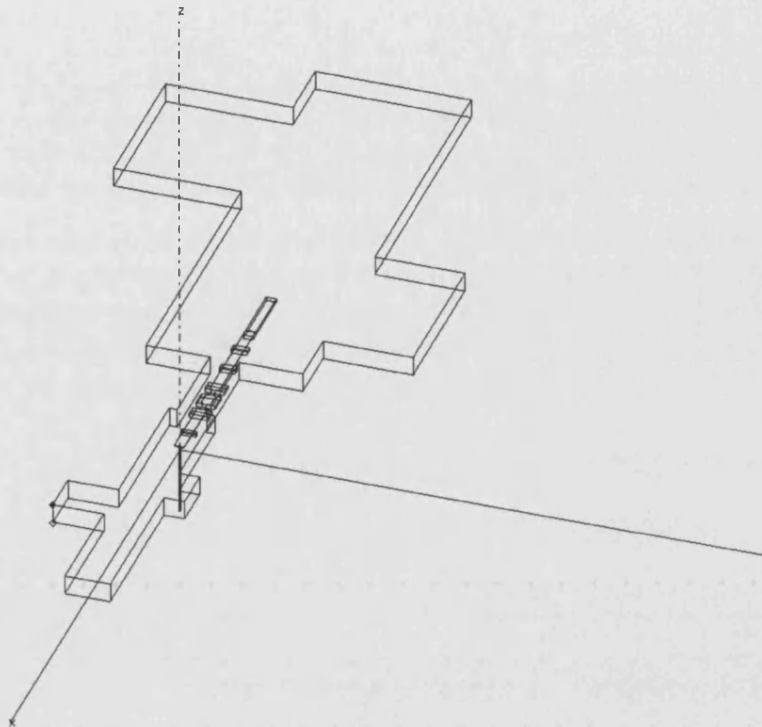
A second representation of the doubler circuit, with waveguide tuners having lengths taken from the APLAC transmission line tuners was then drawn and simulated (fig. 3.4). Once again, S-parameter data was taken from this HFSS model and incorporated into an APLAC circuit (fig. 3.5). With all transmission line tuners removed from the APLAC model, the harmonic balance analysis was repeated and the output compared with that from the doubler tuned with transmission line stubs. The harmonic output power attained from a 30mW input signal is shown in fig. 3.6 for the APLAC tuned model and fig. 3.7 for the HFSS tuned version. The corresponding efficiencies are 1.1% for the APLAC tuned model and 0.73% for the HFSS waveguide-stub tuned model.

Whilst there is clearly a difference in the second harmonic output, the simple tuning method possible in APLAC provides a fast means for circuit refinement together with tuner lengths that are close to optimal. The predicted harmonic power achieved from the structure before any tuning was down at 20µW (from 30mW input power) and the final HFSS tuned version achieved ten times this.

In order to improve on these results, one could perform multiple HFSS simulations with a range of fixed waveguide stub dimensions centred on those predicted as optimal from the APLAC transmission line models. Provided sufficient computational time was available, fine-tuning of the waveguide stub lengths would result in further improvement of the predicted output power. Accurate transferral of tuner dimensions into the actual micromachined circuit may be implemented in several ways (section 3.7.2).
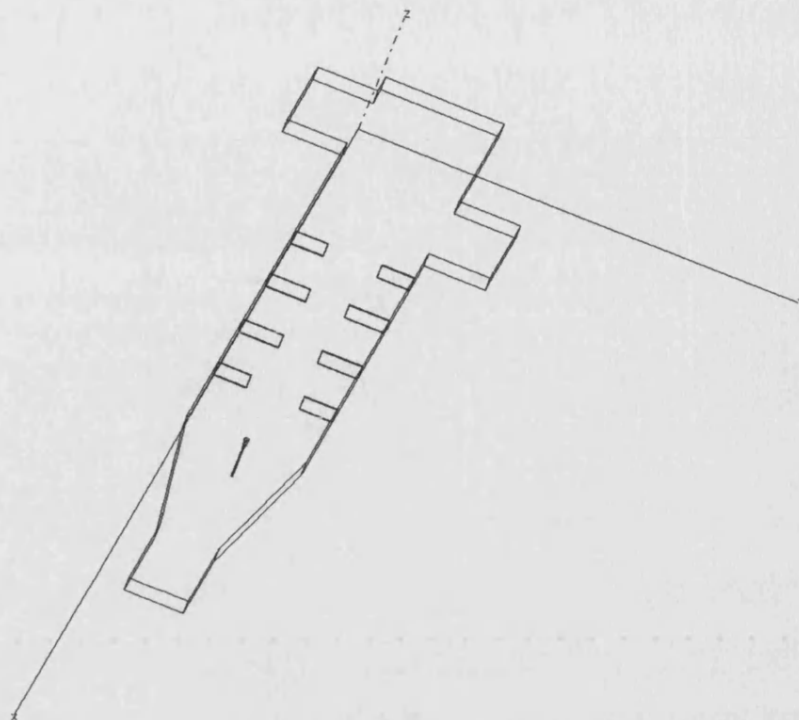
Figure 3.4. HFSS 3-port representation of the tuned doubler embedding circuit.
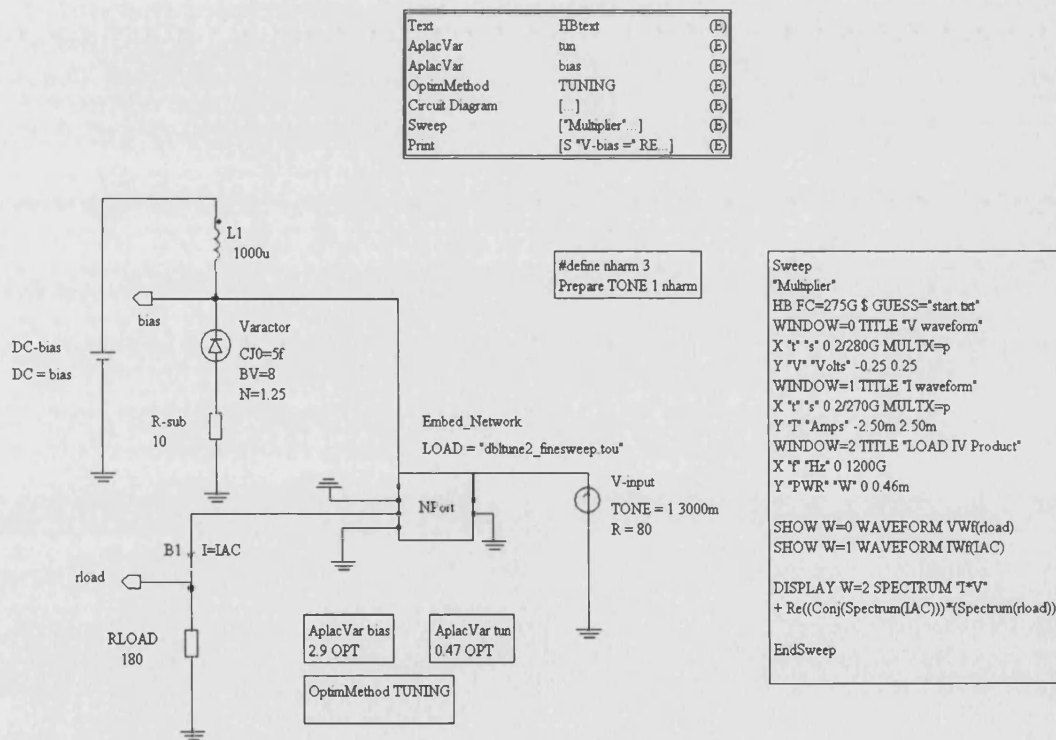
Figure 3.5. APLAC doubler circuit featuring 3-port S-parameter data from HFSS.

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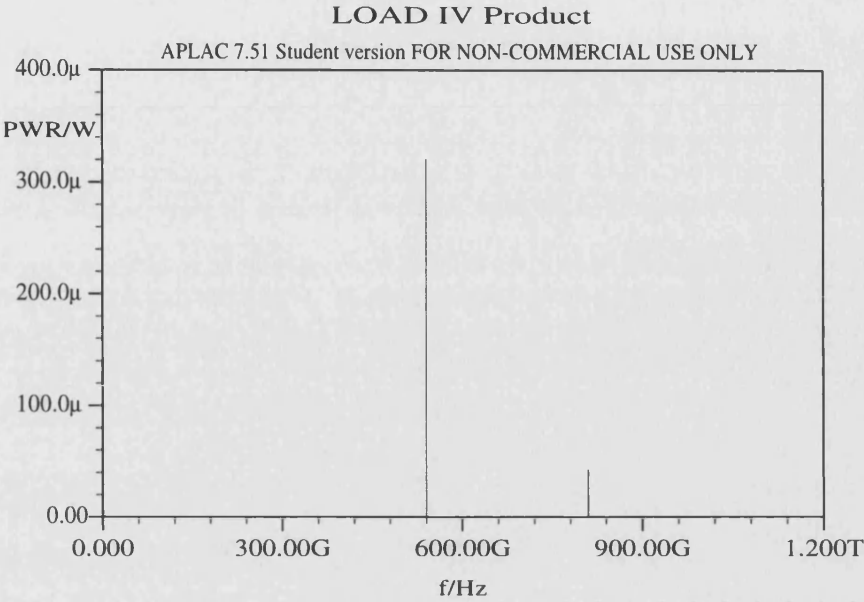
Figure 3.6. Output from APLAC doubler with transmission line tuners.
(Higher harmonic rejection was not attempted in the doubler output circuit and third
harmonic power is present in the predicted output).

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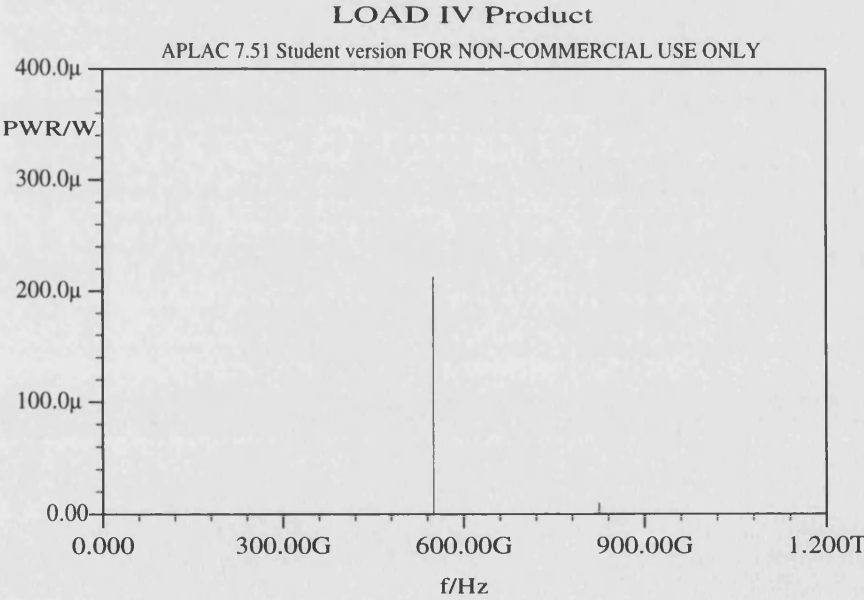
Figure 3.7. Output from APLAC doubler with HFSS waveguide stub tuners.

The process outlined above was repeated for the 270-810GHz frequency tripler shown without tuners in fig. 3.8. It should be stated at this point that this circuit was developed at a time when it was believed that a heterostructure barrier varactor (section 2.7) rather than a Schottky varactor diode would be employed as the multiplying device. For this reason the structure has no second harmonic idler cavity and consequently the idler termination is non-ideal. The output circuit, by virtue of the waveguide cut-off condition, prevents second harmonic power from appearing at the output port.

As before, the analysis began with performing harmonic balance on a circuit tuned in APLAC with transmission line stubs. The tuner lengths were then transferred to waveguide stubs implemented within HFSS. A second harmonic balance calculation was performed with all tuning removed from the APLAC model. The tuned APLAC circuit is shown in fig. 3.9 and the HFSS model, incorporating tuners, is illustrated in fig. 3.10. Input and output tuners were found to be necessary in this circuit, which is in fact very similar to the conventional split-block Archer design [8], albeit in a planar orientation.

The final APLAC treatment of the 270-810GHz tripler tuned in HFSS is shown in fig. 3.11. This analysis did not prove as successful as the doubler example. When the stub arrangement was transferred to the HFSS model and the harmonic balance re-ran, the third harmonic output was severely lowered (fig. 3.12 and fig. 3.13). It was clear from the APLAC analysis and the optimisation of the transmission line tuner lengths that this circuit was very narrow-band in operation. It is possible that slight adjustments made to the HFSS stub lengths would yield a predicted output comparable to that achieved in APLAC. Computing time was the limiting factor in this analysis, with HFSS structure simulation at the third harmonic taking 2-3 days to converge and complete.

The results from this analysis support the case for micromachined sliding shorts that are continuously tunable whilst the circuit is under test. With micrometer driven tuners, as opposed to fixed-backshort stubs, it would be possible to tailor each stub length (with the APLAC model for reference) whilst observing the output power.

Variable tuners would also allow flexibility should device characteristics vary slightly (eg. higher zero bias capacitance due to larger anode area).

Figure 3.8. HFSS 3-port representation of the frequency tripler embedding circuit.

Figure 3.9. APLAC tripler circuit featuring 3-port S-parameter data from HFSS and tuning from transmission line stubs.

Figure 3.10. HFSS 3-port representation of the tuned tripler embedding circuit.
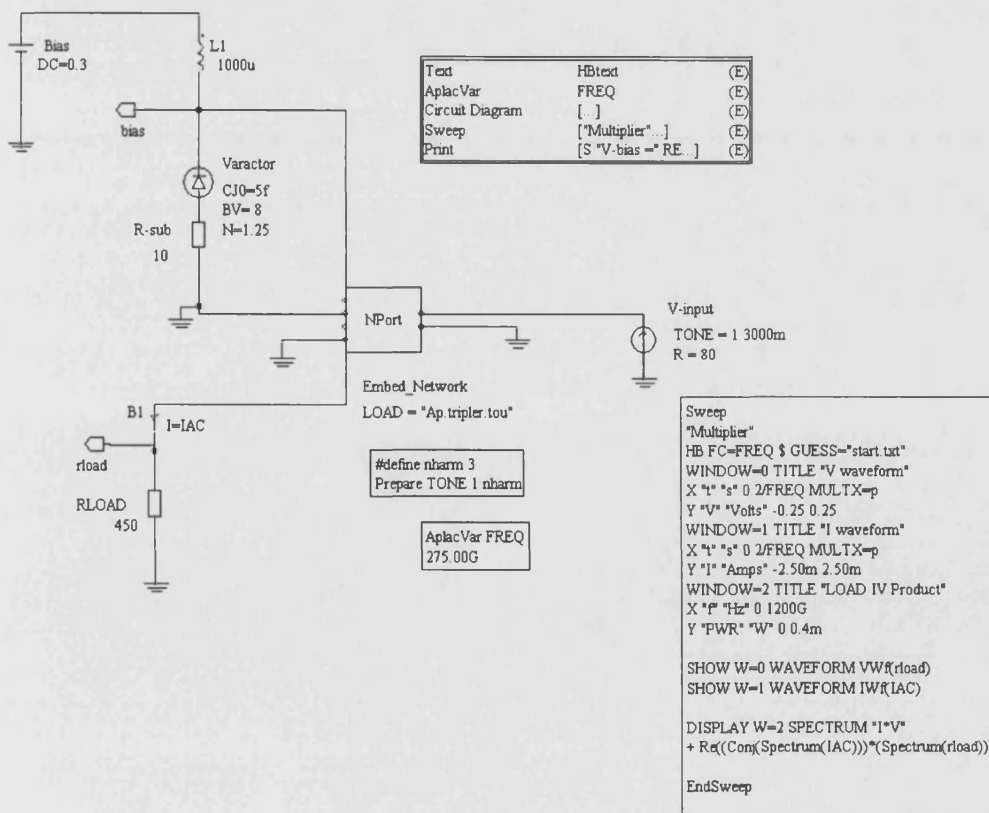
Figure 3.11. APLAC tripler circuit featuring 3-port S-parameter data from HFSS.

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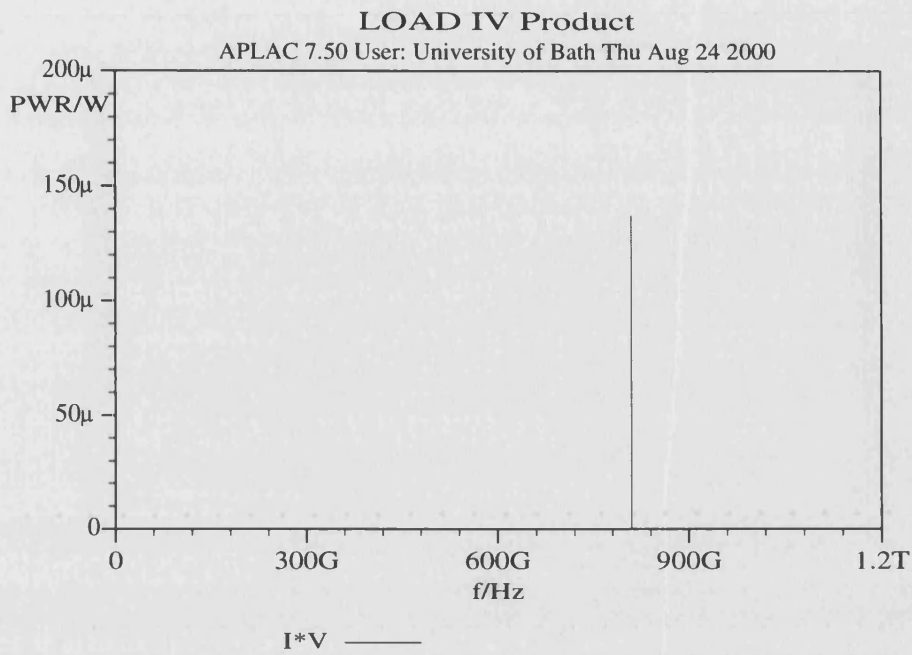
Figure 3.12. Output from APLAC tripler with transmission line tuners.

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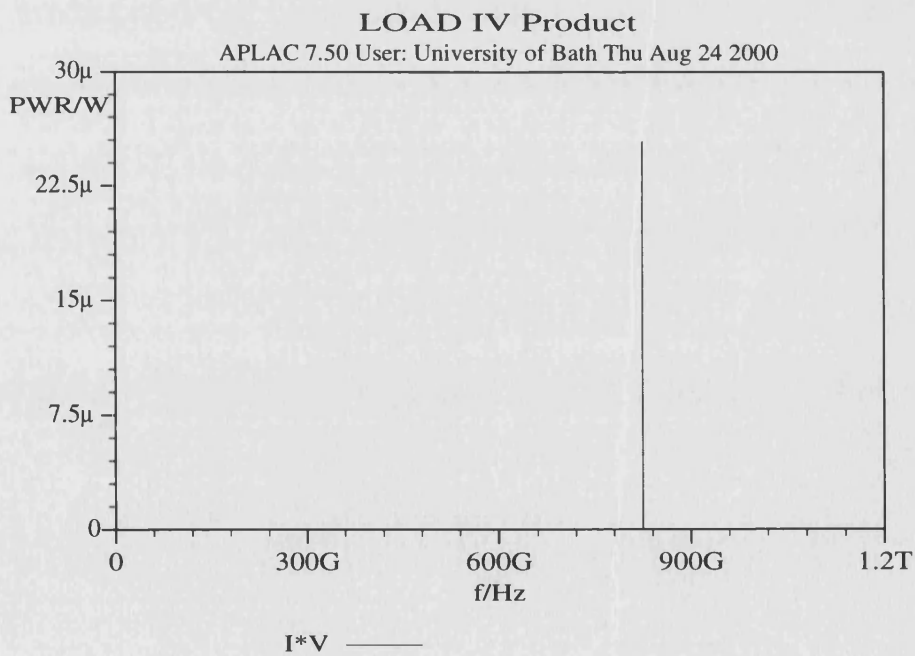
Figure 3.13. Output from APLAC tripler with HFSS waveguide stub tuners.

Alternative analysis methods exist based on a FEM/circuit simulator approach. Using our existing software a method was attempted whereby the multiplier structure was represented as an HFSS model with ports at the input and output, diode embedding point and the point where a tuner would be added. Further HFSS simulations were performed on stubs with lengths varying from zero to one half guide-wavelength in sixteenth of a guide-wavelength steps. The four-port and 1-port data created by these runs was combined in an APLAC equivalent circuit, thereby eliminating the requirement for approximate transmission line representation of the tuning element. This approach showed promise but again computational resources proved to be the limiting factor. The passive structure included filter elements, a diode post transition and a tapered transformer all of which when coupled with the requirement for four-port analysis, led to failure due to exhausted system memory. It was possible to perform this analysis if the harmonic frequencies were restricted to just the fundamental and the doubled output frequency. Results obtained clearly showed the tuning action of the added stub but the method was not pursued due to the excessive duration of the simulations.

Optimetrics is a commercially available addition to Ansoft HFSS that would allow tuners to be electronically moved in order to provide stipulated S-parameter data at a port. For a port situated at the diode embedding point, S-parameters based on the Burckhardt [3] and/or UVA [4] analysis could be entered and the appropriate tuning configuration found.

3.5 Summary

In the remainder of this chapter the multiplier circuit is broken into constituent circuit elements, which are then described in more detail. Prior to this analysis, comparison should be made with the embedding impedances predicted by the Burckhardt method. The harmonic embedding impedances seen within the tuned tripler are $Z_{01} = 70 - j8$ Ω, $Z_{02} = 14 + j6$ Ω and $Z_{03} = 16 - j21$ Ω. For the tuned doubler the embedding impedances are $Z_{01} = 150 - j60$ Ω and $Z_{02} = 75 - j23$ Ω.

Referring back to section 3.4 it is clear that the tuning positions resulting in maximised efficiency from the doubler and tripler do not produce embedding

impedances that correspond to those predicted by the Burckhardt method (section 3.3).

If certain processing constraints were lifted, the embedding conditions created within the tuned multipliers may have agreed more closely with those given by Burckhardt's analysis. Design aspects that were limited by processing considerations include the diode contact post and the stripline-to-ridge waveguide transition in the frequency tripler.

Addressing the contact post first, this is necessarily height limited to approximately 30µm due to the requirement to bake the AZ resist layer (see sections 4.6 and 4.10) on a heated microscope stage. In this process it was also necessary to avoid meniscus effects (occurring as the AZ4562 resist layer approached 50µm in thickness) around the phosphor-bronze tip (leading to cracking in the resist layer and stray electroplating). If it were possible to increase the height of this post, more efficient coupling of the harmonic power to the output circuit would be possible and constraints on the output circuit tuning would be relaxed. Similarly the stripline to ridge waveguide transition was height limited, again by the requirement that the stripline filter should meet the electroplated whisker at its output end.

It was stated in section 3.1.1 that the doubler and tripler would be designed as single height structures. This decision was made to simplify the fabrication process. Many conventionally machined frequency multipliers feature varying input and/or output waveguide heights. A common strategy is to house the varactor in a reduced height waveguide cavity in order to assist matching to the real part of the device impedance. In a single height scheme tapered height guides were not realisable and some flexibility in circuit tuning was sacrificed.

The frequency tripler was first designed around a heterostructure barrier varactor (HBV) rather than a Schottly varactor. These devices (described in section 2.7) produce only odd-order harmonics and therefore require no second harmonic idler circuitry. Full provision for a resonant second harmonic idler was not provided and this was reflected in the difference between the Burckhardt and HFSS modelled idler impedance values.

Despite the limitations described above, the modelling exercise performed indicated that both the doubler and tripler designs are capable of delivering appreciable power at the desired output frequencies using devices comparable with those already produced at Bath.

In summary, the predicted efficiencies (from the HFSS tuned versions) of the doubler and tripler are 0.73% and 0.1% respectively. This performance is not exceptional and many split-block multipliers have achieved higher efficiencies (Rydberg [9] achieved 0.8% efficiency at 803GHz from a tripler), however the designs presented here have evolved first and foremost within constraints set by the associated fabrication methods. Both the doubler and tripler schemes were designed so that all processing could be completed with equipment and materials available in-house. Limits imposed by this restriction included the height of positive photoresist waveguide formers (doubler) and the length of the electroplated contact post (doubler and tripler). Positive photoresists that would ease these restrictions and allow greater flexibility in the design process have recently become available.

The issue of circuit tuning is a vital one for varactor multipliers. It is possible to design a circuit that meets the embedding requirements given by analytical and harmonic balance style analyses but this assumes that the circuit will be built around an extremely well characterised device. In reality, parasitic reactances introduced by the diode contact mechanism require additional tuning and the vast majority of millimetre- and submillimetre-wave multipliers require variable backshorts to achieve maximum efficiency. MEMS is well suited to producing these components and incorporation of these components into the multiplier schemes was a primary goal of the project.

Finally, due to difficulties in finding a suitable source of 270GHz radiation a scaled version of the frequency doubler has been adopted as the primary test vehicle. This will operate with a fundamental of around 165GHz (G-Band) and will be mated to a standard UG387/U waveguide flange for the purposes of testing.

3.6   Microwave and sub-mm wave filters.

3.6.1   Low frequency filter implementation

Before examining methods employed to realise microwave and sub-mm wave filters, this section introduces lumped-element filter design and the insertion loss method. Frequency transformation is used to derive a band-pass design from a low-pass prototype and the principle of impedance inversion is briefly discussed. Whilst filter structures implemented for high frequency applications rely on distributed elements, the lumped element topologies reviewed in this section serve as a basis for designing at higher frequency.

The insertion loss method is implemented using established low-pass filter prototypes - Butterworth, Chebyshev, Bessel and others. These filters are LC ladder networks using series inductors and shunt capacitors. An n-section filter has n components (capacitors plus inductors). Loss is restricted to parasitic resistance in the inductors and capacitors and the filtering action occurs due to reactive reflection. An ideal low-pass filter provides a perfect match between source and load within the passband. Multi-section filters approach this ideal and wide band matching is possible when source and load impedances are non-reactive.

A filter designed with Butterworth coefficients has no pass-band ripple and is often referred to as maximally flat. It is designed so that the first n-1 derivatives with respect to frequency of the power transfer function are zero. For a half power cut-off frequency f_0, the Butterworth filter response is,

$$\frac{|V_{out}|}{|V_{in}|} = \frac{1}{1+\left(\dfrac{f}{f_0}\right)^{2n}}.$$ (3.10)

Chebyshev filters provide greater rejection away from the pass-band but also have pass-band ripple. The response is given below and is such that these ripples are of equal depth. V_r^{-1} is the depth of the ripple in volts.

$$\frac{|V_{out}|}{|V_{in}|} = \frac{1}{1+(V_r^{-2}-1)\cosh^2(n\cosh^{-1}(f/f_0))}.$$ (3.11)

Mattheai et al. [10], provide a set of tables for realising Butterworth and Chebyshev filters. The prototype values are normalised for frequency, source and load impedance.

3.6.2 A lumped element low-pass filter

An $n=3$ 0.5dB ripple Chebyshev low-pass filter has coefficients $g_0 = 1.000$, $g_1 = 1.5963$, $g_2 = 1.0967$, $g_3 = 1.5963$ and $g_4 = 1.000$. These are normalised to an angular cut-off frequency of 1rads^{-1} and load/source impedance of 1ohm. If the source/load impedance is 100ohms and the pass-band is to extend to 10GHz, then the inductance and capacitance coefficients must to be scaled. The series inductor values (g_1 and g_3) are multiplied by the characteristic impedance then divided by the angular cut-off frequency. The parallel capacitor value (g_2) is divided by the product of the characteristic impedance and the angular cut-off frequency. A circuit with the resulting component values for the scaled filter is illustrated below.
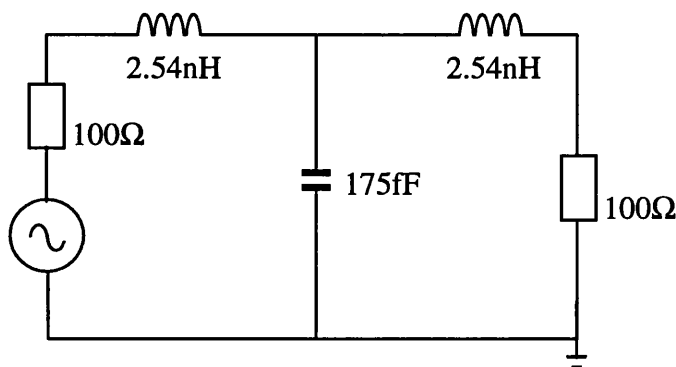
Figure 3.14 Low pass filter normalised to 100Ω and
f_c=10GHz, using lumped elements

In the circuit above the inductor/capacitor values cannot be realised using lumped components. Distributed elements however, allow the required high frequency circuit reactance values to be achieved and these may be modelled as equivalent lumped elements with the values of fig. 3.14.

3.6.3 Low-pass transformation to band-pass

In order to convert a low-pass filter into a band-pass design, series inductors and shunt capacitors are replaced with series resonant LC combinations and parallel resonant LC combinations respectively. The series resonant combinations are designed to have zero impedance at the centre frequency and the parallel resonant LC pairs have zero susceptance at the centre frequency.

Series resonant LC pairs acquire reactance outside the pass-band at twice the rate of similarly placed series inductors. Therefore the series inductor values selected for a band-pass filter are half of those for the low-pass prototype. Similarly, shunt capacitor values in the band-pass filter are halved and provide a susceptance change with frequency equivalent to the low-pass design. The bandwidth above the centre frequency is thus preserved after frequency translation. The mirror image pass-band below the centre frequency causes the total bandwidth of the frequency scaled filter to be twice that of the low-pass prototype.

The circuit of fig. 3.14 is transformed to a band-pass design with centre frequency 270GHz. The resulting circuit and response (plotted using PSPICE) are shown in fig. 3.15 and 3.16. Once again the component values are not practically achievable, but the result is effectively a lumped-element equivalent circuit for the waveguide filter developed later in this section.
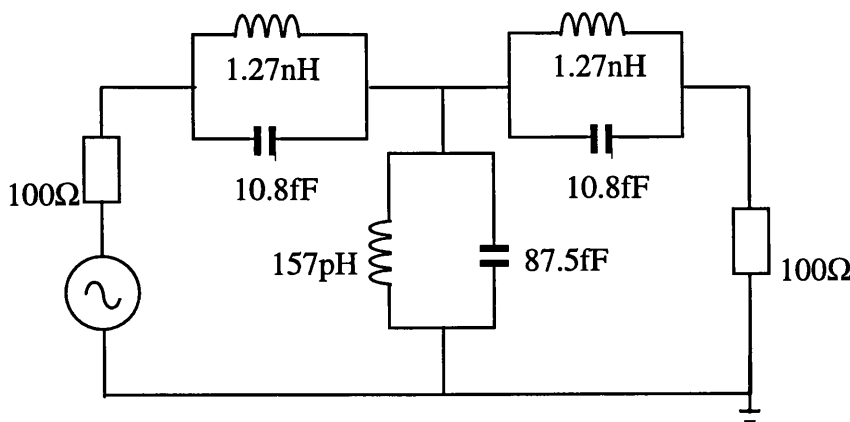
Figure 3.15. 270GHz lumped element
band-pass filter with 20GHz bandwidth.
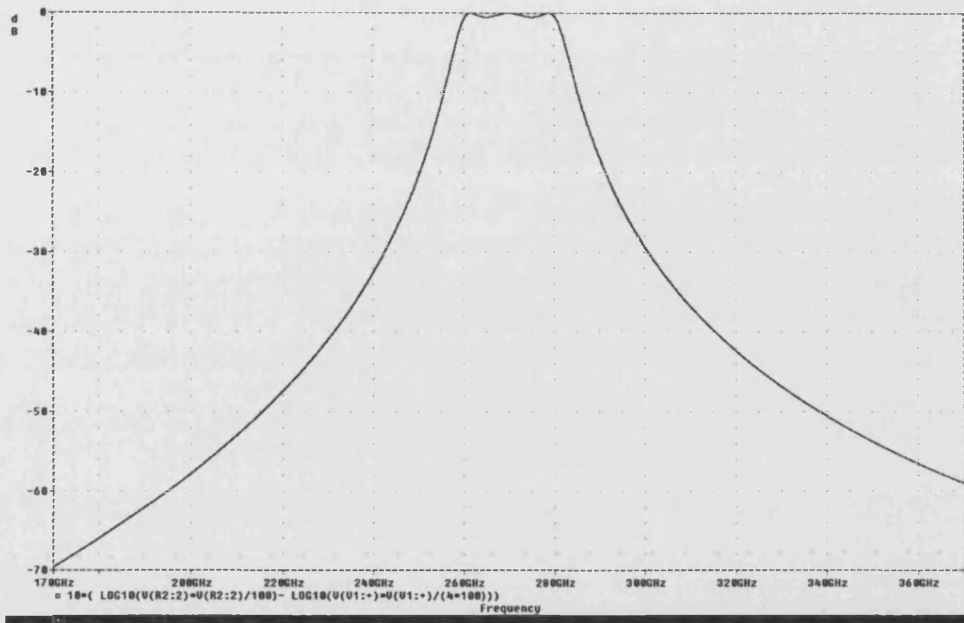
Figure 3.16. PSPICE predicted response of the lumped element band-pass filter of fig. 3.15.

3.6.4 Impedance inversion

The circuit of fig. 3.15 has alternating series and shunt resonant circuits. When this circuit configuration is applied to RF band-pass filtering, unrealistic component values may be prescribed.

(a)   (b)
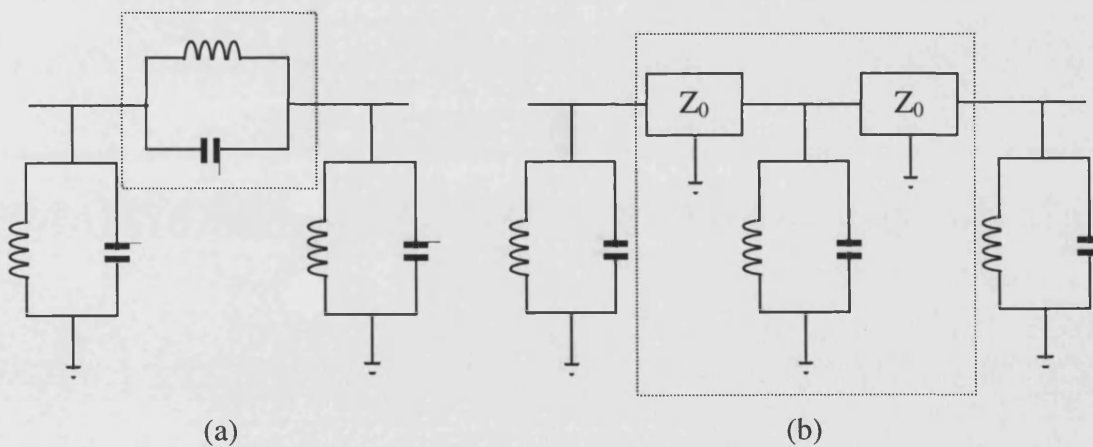
Figure 3.17. (a) A series resonator and (b) the equivalent impedance inverted shunt resonator.

This problem may be overcome by using impedance inverters and transforming the circuit into a coupled-resonator configuration [11]. In microwave circuits, it is often preferable to rely on a cascade of similar circuit elements to perform filtering, rather than alternating series and shunt components. Impedance inversion makes this possible. Fig. 3.17 illustrates how an inverter pair is used to transform a series resonator into a shunt resonator. Theory and further applications of this method can be found in [10, 11, 12].

3.7 Coupled resonator waveguide filters

Rectangular waveguide forms the input and output circuits for the tripler and doubler featured in this project, so integral coupled resonator filters were investigated as a convenient means of providing harmonic rejection. Using both conventional resist and SU8, the simplest components to fabricate within the waveguide were inductive irises. These are full height plates that protrude into the waveguide, effectively constricting the broad wall dimension (fig. 3.18 (a)). Inductive iris coupled filters are regularly employed at microwave frequencies but in the sub-mm range are prohibitively difficult to produce using conventional machining methods. Micromachining provides an inexpensive means to produce sub-mm wave iris coupled filters with very high accuracy.

(a)   (b)
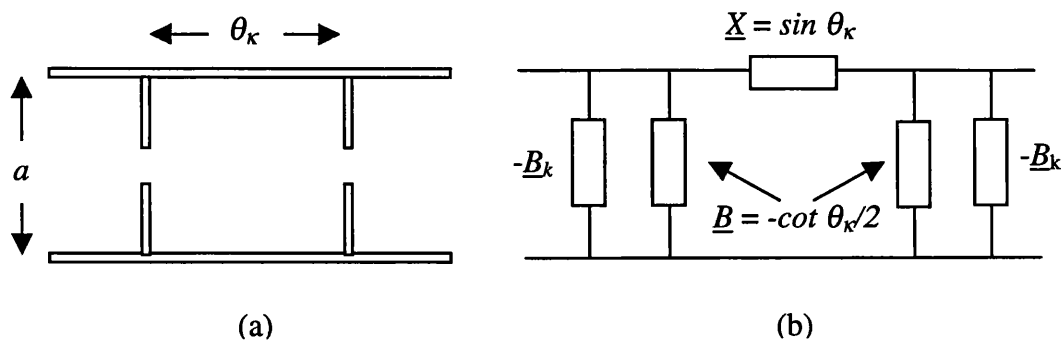
Figure 3.18. (a) A waveguide cavity former by two inductive
iris pairs and (b) its equivalent circuit

The design selected for investigation was a direct coupled cavity resonator filter. Quarter-wave coupled filters [12, 13, 14] are also possible but are less compact and offer reduced bandwidth. Cohn [15] developed a design method for direct-coupled inductive iris filters with bandwidths of up to 20%. This procedure is also described

and demonstrated by way of example in [10]. For the purposes of this project, 270GHz and 135GHz band-pass filters were adopted as optical mask patterns and translated into SU8 and conventional photoresist. The 270GHz band-pass filter also featured in the input guide (fundamental frequency 270GHz) of a frequency doubler mask pattern.

3.7.1 Overview of direct-coupled resonator filter design

Figure 3.18(b) illustrates an equivalent π network for the waveguide cavity in (a). The two shunt susceptances $\underline{B} = $ -cot $\theta_K/2$ may be neglected compared with $\underline{B}_k$ since $\underline{B}_k$ will be large and since θ_K is nearly equal to π, $\underline{B}$ is small compared with unity. The series arm $\underline{X}$ is thus used as the series resonant circuit in the prototype filter.

The Cohn design uses shunt inductive reactance and two short negative lengths of waveguide as impedance inverters (fig. 3.19). The required inverting properties are provided if

$$\theta_{1k} = -\frac{1}{2}\tan^{-1}\frac{2}{\underline{B}_k}$$
(3.12)

and

$$\underline{B}_k = \frac{1 - K^2}{K},$$
(3.13)

where K is the characteristic impedance of the quarter wave impedance inverter. With θ_{1k} and $\underline{B}_k$ determined at the pass-band angular frequency, it is found that the inverter operates effectively over a 20% bandwidth.
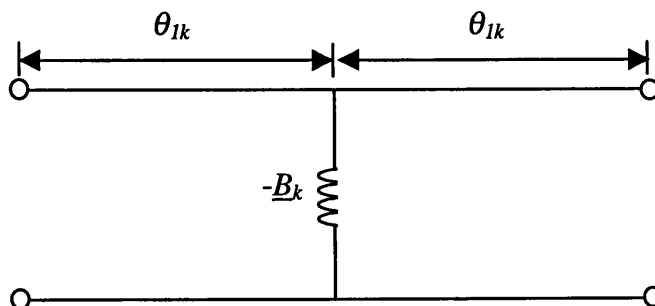
Figure 3.19. Impedance inverter used in direct iris-coupled-resonator filter.

The frequency behaviour of a lumped element series resonant circuit around the centre frequency ω_0 is

$$X = \left(\frac{L}{C}\right)^{\frac{1}{2}}\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right) \approx 2\left(\frac{L}{C}\right)^{\frac{1}{2}}\left(\frac{\omega - \omega_0}{\omega_0}\right). \qquad (3.14)$$

For the resonant cavity with $\theta_k = \pi$, the frequency behaviour around ω_0 is

$$X = \sin\theta_k \approx -\frac{\pi}{2}\left(\frac{\beta}{\beta_0} - \frac{\beta_0}{\beta}\right) \qquad (3.15)$$

where $\beta_0 l = \pi$. Thus the frequency behaviour is similar if ω/ω_0 is replaced by the frequency variable β/β_0.

When the negative line lengths of the impedance inverter are absorbed into the cavity, the physical length of the kth cavity is

$$l_k = \frac{\lambda_{g0}}{2} + \frac{\lambda_{g0}}{2\pi}(\theta_{1k} + \theta_{1k+1}). \qquad (3.16)$$

The impedance inverter properties are selected so that

$$\left(\frac{L_{0k}}{C_{0k}}\right)^{\frac{1}{2}} = \frac{\pi}{2} \quad \text{and} \quad L_{0k}C_{0k} = (\beta_0 c)^{-2}. \qquad (3.17)$$

The impedance inverter parameters may then be stated in terms of the prototype filter coefficients. The iris susceptance relations are given below

$$\underline{B}_1 = \frac{1 - \dfrac{w}{g_1}}{\sqrt{\dfrac{w}{g_1}}} \qquad (3.18)$$

$$\underline{B}_k = \frac{1}{w}\left(1 - \frac{w^2}{g_k g_{k-1}}\right)\sqrt{g_1 g_2} \qquad (3.19)$$

$$\underline{B}_N = \left(\frac{1 - \dfrac{wR}{g_N}}{\sqrt{\dfrac{wR}{g_N}}}\right) \qquad R=1 \text{ for } N \text{ odd} \qquad (3.20)$$

where

$$w = \frac{\pi}{2}\frac{\beta_2 - \beta_1}{\beta_0} \qquad (3.21)$$

$R=1$ for N odd and also for N even in the case of the maximally flat design. [10] provides tabulated values of R for N even Chebyshev filters.

Once the electrical lengths of the cavities and the susceptance values of the irises are calculated, standard formulae [16] are employed to derive the iris widths. These widths are calculated and scaled based on the dimensions of the waveguide chosen to contain the filter. Dimensions for a 270GHz band-pass coupled-resonator filter are given in fig. 3.20. The bandwidth for this $n = 3$, 0.5dB Chebyshev filter is 20GHz (7.4%). HFSS S_{21} plots are shown in fig. 3.21 and fig. 3.22 for iris plates of thickness 10μm and 60μm respectively. A MATLAB program was written to design direct-coupled iris bandpass filters based on the analysis described above [Appendix 1].
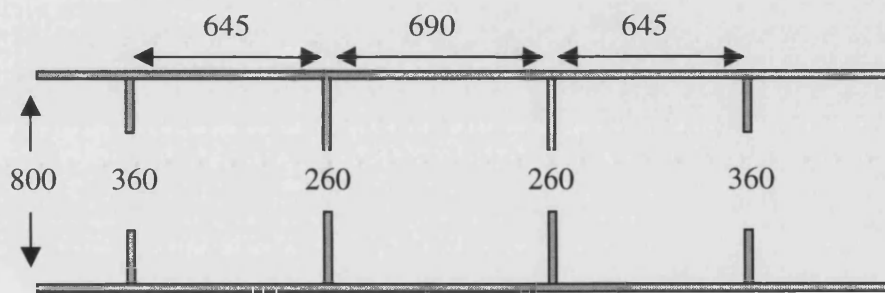
Figure 3.20. 270GHz band-pass filter implemented in rectangular waveguide.
(Iris widths are 220, 270, 270, 220 L-R, all dimensions in μm)
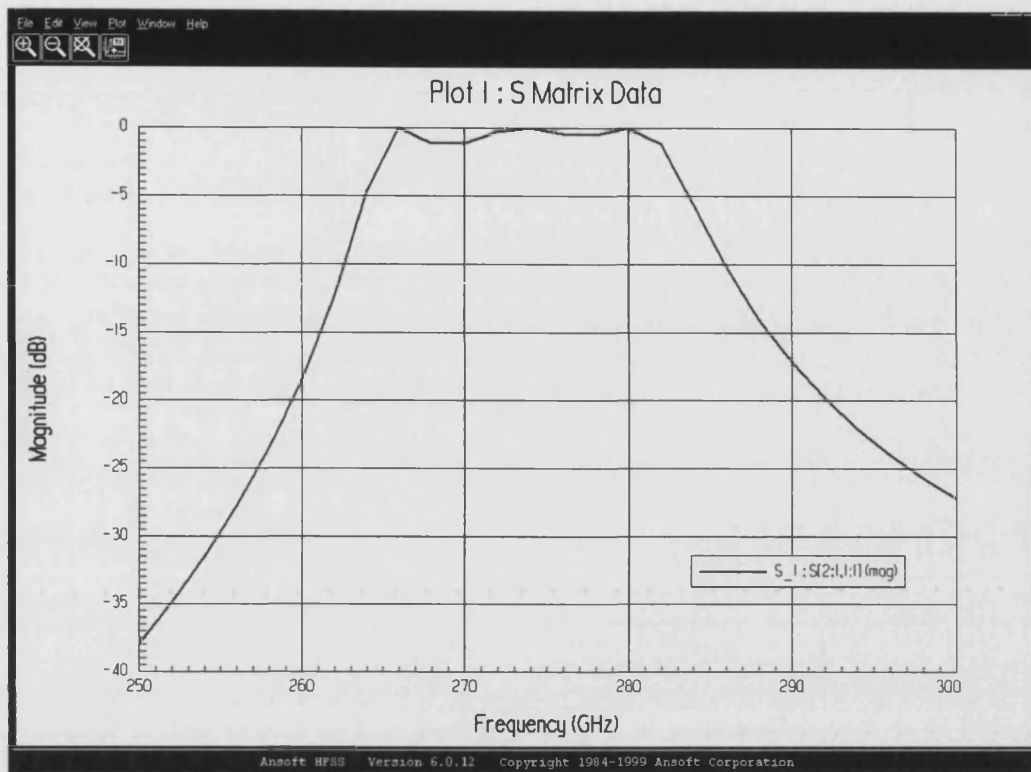
Figure 3.21. S_{21} for direct-iris-coupled resonant cavity filter with 10µm irises.
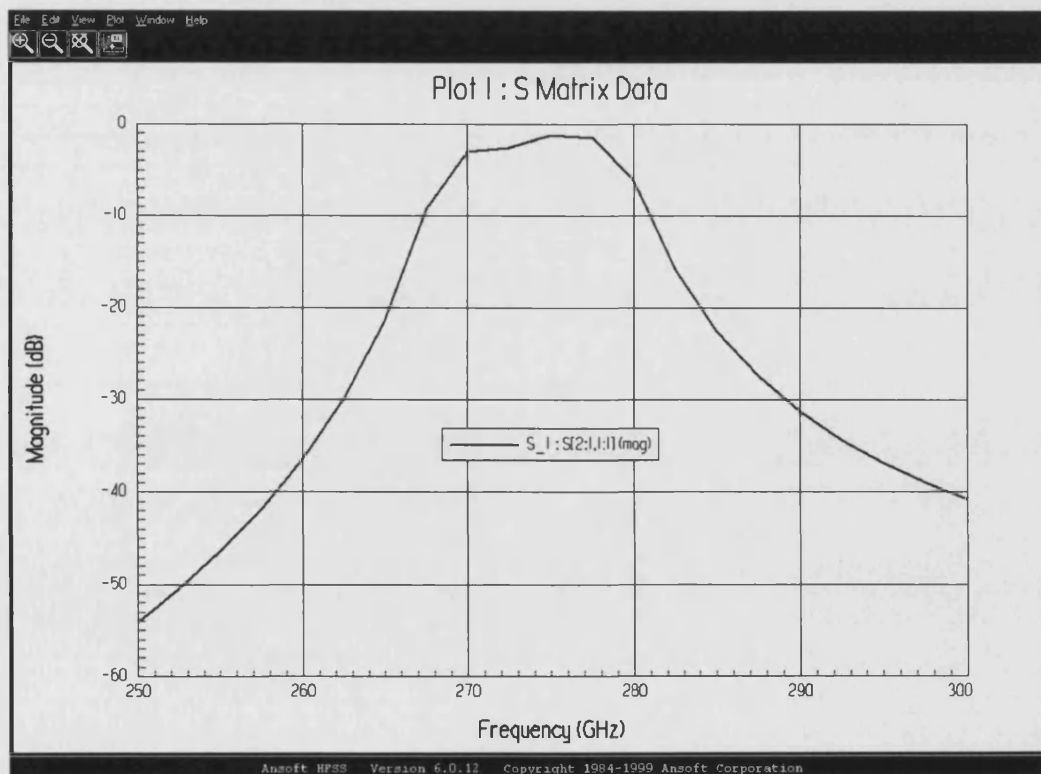
Figure 3.22. S_{21} for direct-iris-coupled resonant cavity filter with 60µm irises.

3.8   Stripline filters

References [17, 18 and 19] describe the different types of strip type transmission line available and the principles involved in their associated filter design. The possibility of incorporating a stripline filter/probe within the integrated tripler (section 4.11) was investigated following the arrival of SU8 and a suitably modified mask aligner (section 4.4). With SU8 a permanent supporting dielectric could be spun and imaged on a substrate prior to forming the strip conductor. The dual substrate 'flip-chip' layout, adopted for the tripler, was also made possible by SU8. This aspect of the design was particularly important with regard to the fabricated stripline, meaning that processing on the base substrate ended with the stripline filter. No additional stress was placed on the stripline or diode post following the successful patterning of the filter and probes.

The procedure outlined for the design of the high-pass stripline filter [19] results in a simple short-line filter topology. More sophisticated designs are available [20] but were avoided in a bid to keep fabrication difficulties to a minimum. The filter relies on the principle that relative to the input and output lines, narrower sections of stripline behave inductively and wider sections behave capacitively. A cascaded filter is therefore possible using alternating short sections of narrow (high impedance) and wide (low impedance) stripline sections. Table 3.3 includes dimensions and impedances for the SU8 (dielectric thickness, $h = 30\mu m$) supported stripline. The predicted response of this filter is shown in fig. 3.23 with the associated HFSS model.

Section	1	2	3	4	5	In/Out
Width(μm)	100	10	100	10	100	50
Length(μm)	28	46	90	46	28	700/460
$Z_0(\Omega)$	31	150	31	150	31	52

Table 3.3. Dimensions for low-pass filter design with SU8 dielectric.
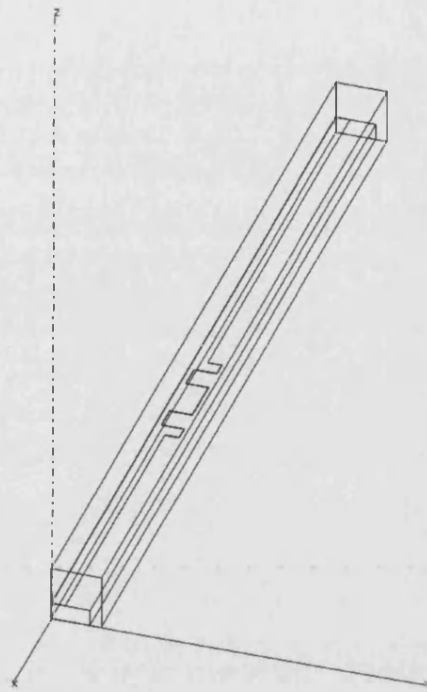
(a)
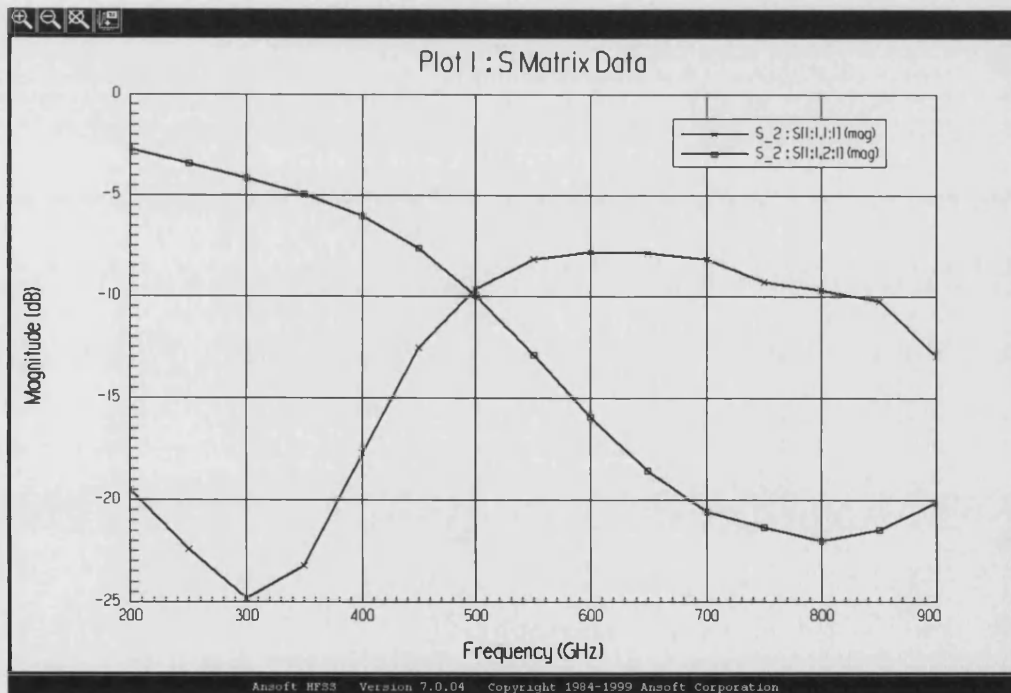
(b)

Figure 3.23. (a) HFSS model of SU8 based low-pass stripline filter and (b) associated S-parameter plot (cross marker - S_{11}, square marker - S_{21}).

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3.8.1   Air-bridged stripline filter using SU8 support blocks

As seen in fig. 3.23, SU8 exhibits high dielectric loss ($tan\delta = 0.063$ [21]). This is an unwanted characteristic in any sub-mm wave component and particularly in frequency multipliers where maximum output power is a primary goal. An alternative stripline with a low-loss substrate material was clearly needed. Designs were developed that replaced the continuous SU-8 substrate with thin, periodically placed, SU8 blocks. As a starting point, the filter was redesigned based on enclosed stripline with a dielectric constant of air. The dimensions of this filter are shown in table 3.4.
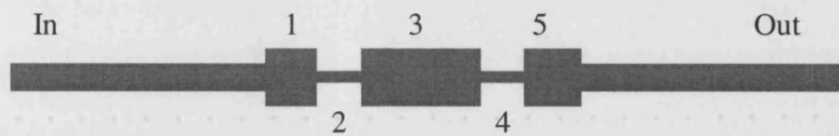
Section	1	2	3	4	5	In/Out
Width	100	20	100	20	100	50
Length	77	55	115	55	77	450/230
$Z_0(\Omega)$	65	150	65	150	65	99

Table 3.4. Low-pass filter design with SU8 'struts' and air dielectric.

The response for this filter is shown in fig. 3.24(a). The low-pass filter based on SU8 shows severe loss at the designed rejection frequency (810GHz). A reduction in this loss is seen as expected, for the stripline-in-air scheme. For the stripline filter to be realisable within the integrated multiplier it would require support, provided by the discrete SU8 blocks (height = 30µm). The development of the final design is summarised in fig. 3.24, which illustrates the HFSS modelled structures and their associated S-parameter output. Conductivity for the strip and waveguide walls was assumed to be that of gold (4.1 x $10^7\Omega^{-1}$) and the dielectric constant and loss tangent for SU8 were 2.9 and 0.063 respectively.
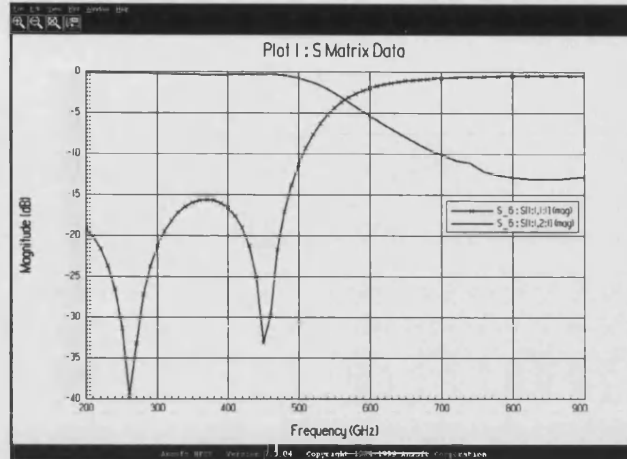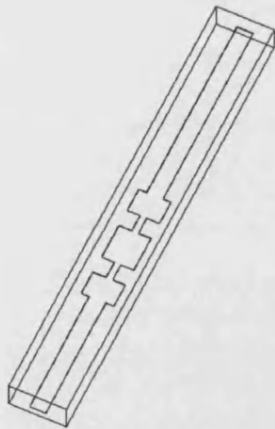
(a) Stripline filter in air filled rectangular waveguide cavity.
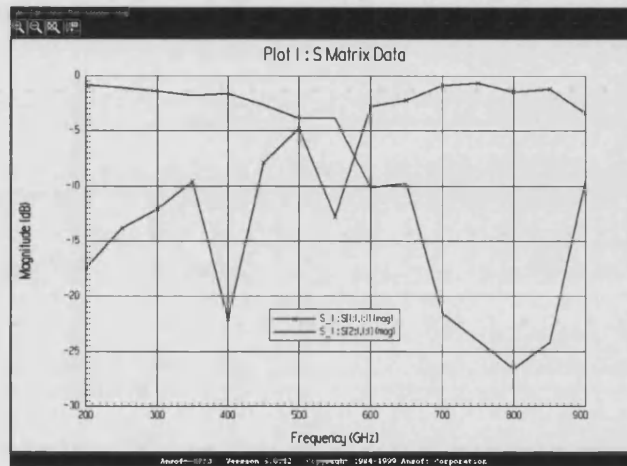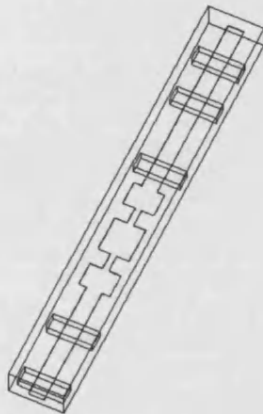
(b) Stripline filter with SU8 support blocks added to input and output lines.
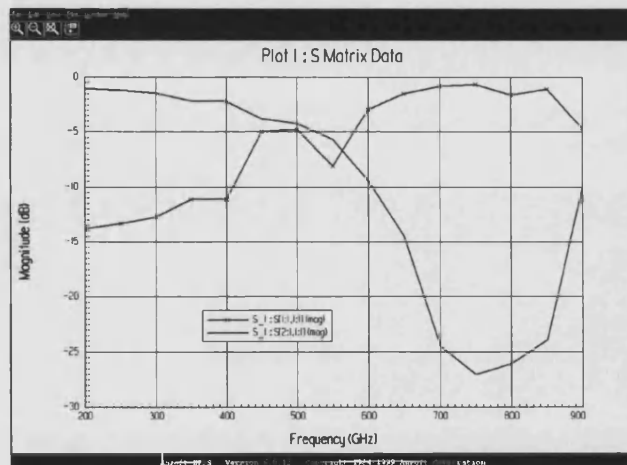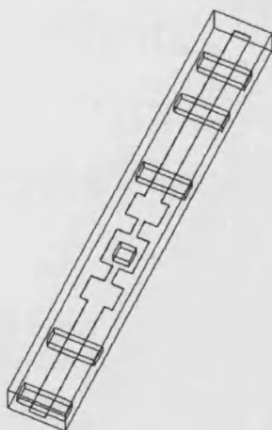
(c) Stripline filter with additional support block in central low-impedance section.

Figure 3.24. Evolution of air-bridged stripline structure suitable for use with SU8.
On S-parameter plots, cross marker indicates S_{11}, plain line indicates S_{21}.

Plot I : S Matrix Data
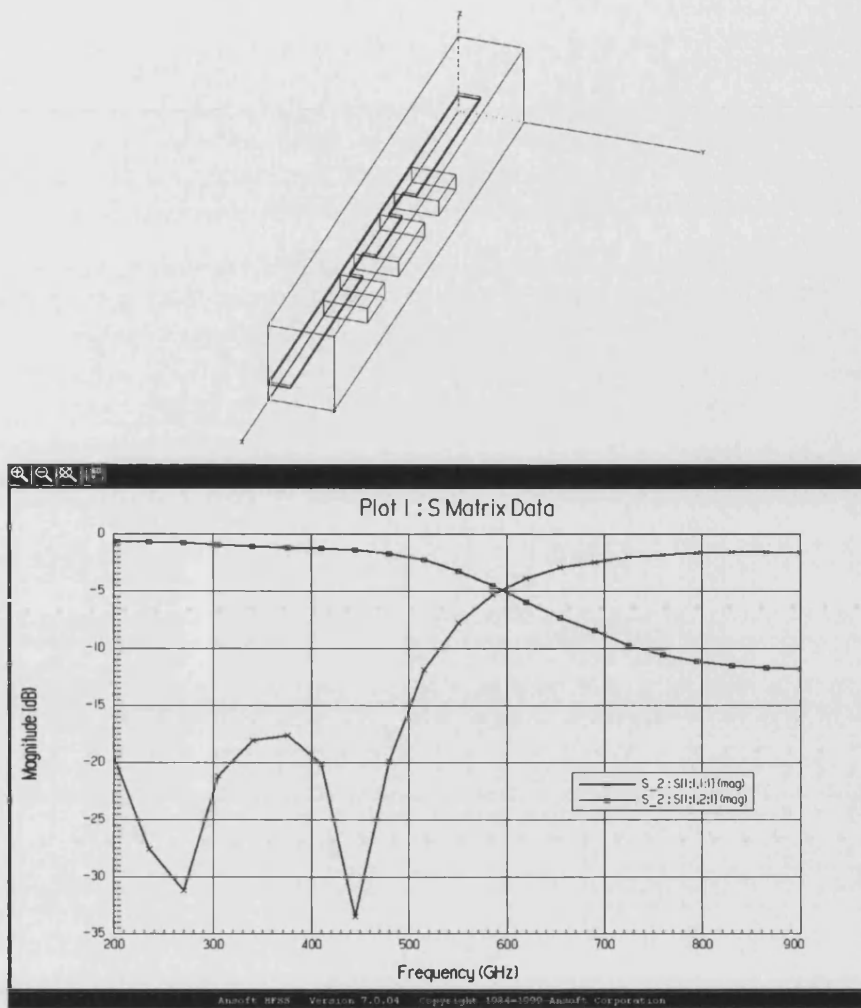
Figure 3.24 continued. (d) Model and S-parameter plot for the final stripline design.
SU8 supports provide low impedance sections for the low-pass filter.
On S-parameter plot: cross marker indicates S_{11}, square marker indicates S_{21}.
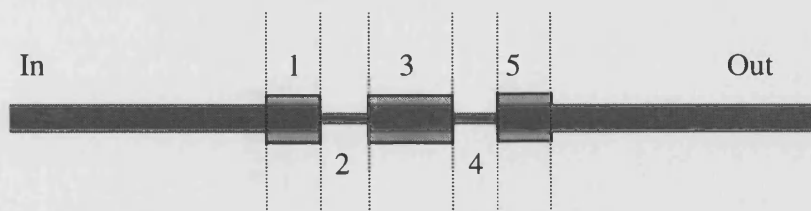
Section	1	2	3	4	5	In/Out
Width (μm)	50	20	50	20	50	50/50
Length (μm)	59	48	88	48	59	500/280
$Z_0(\Omega)$	48	126	48	126	48	82/82

Table 3.5. Dimensions and impedances for stripline filter of fig. 3.24(d).

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3.7 Waveguide tuners

The sliding short circuit shown in fig. 3.25 is a popular choice in microwave circuits for providing variable reactance for tuning [22]. The spacing between the tuning stub face and a reference plane can be altered and for the lossless case, any reactance $X = Z_0 tan(\beta L)$ can be created at this plane. At higher frequencies these tuners become harder to fabricate and alternative designs have been demonstrated [23, 24, 25].
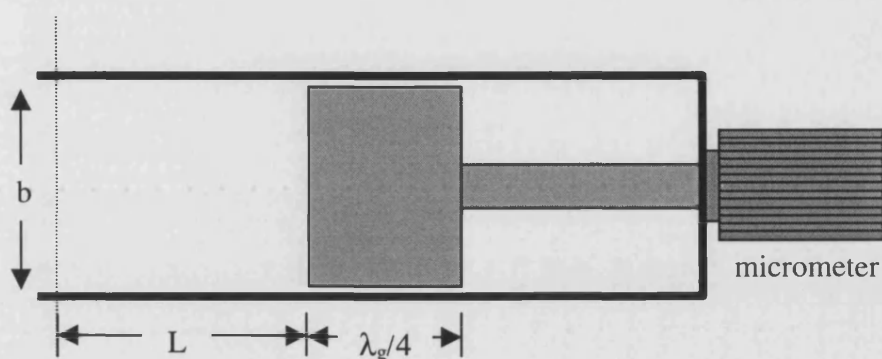
Figure 3.25. Sliding short circuit stub loaded into rectangular waveguide

In order to allow movement, the tuning stub must be fractionally smaller than the waveguide that it is housed in. The discontinuities caused by the inevitable gaps lead to higher order propagation modes at the face of the tuning stub and these add reactance. For the purposes of modelling, a simple offset can be added to the length L to accommodate this additional reactance.

Leakage around the tuning stub also causes an additional reactive contribution. Power reflected from the back wall of the waveguide, re-enters the waveguide with varying phase relative to the signal reflected directly from the stub face. The signal path is twice the distance between the stub face and the back-wall of the waveguide and hence changes with the tuner position. It resembles a low impedance section past the stub, followed by a high impedance cavity section. If the stub is made $\lambda_g/4$ thick, then the high impedance of the cavity is transformed into a short circuit at the stub face and signal leakage is greatly reduced.

3.7.1 Tuning stubs fabricated in SU8

Figures 3.26 and 3.27 show SU8 tuning stubs that were incorporated into tripler and doubler configurations. The HFSS modelled power leakage is seen to be -20dB (maximum) from 750-880GHz for the tripler stub, whilst for the doubler stub power leakage is –20dB (maximum) in the 260-295GHz and 510-595GHz ranges. These frequency regions lie respectively around the third harmonic for the tripler and the fundamental and second harmonic for the doubler. Dual shunt tuning stubs were allied to the output guide of the tripler and the input guide of the doubler.

In order to minimise processing complexity, the height of the tuning stubs was constant and impedance variation was achieved via cavities or steps in the H-plane. The design adopted for the frequency doubler features a cavity that is series resonant at the second harmonic frequency (540GHz). The low impedance path past the stub face is $\lambda_g/4$ in length (also at 540GHz) and transforms the cavity resonance into a shunt resonant circuit at the plane of the stub face. The tripler stub has alternate sections with widths 200, 120, 200μm. The first two sections back from the face are $\lambda_g/4$ in length (at the third harmonic frequency of 810GHz).

Aside from considerations involving signal loss, the micromachined tuners had to be designed with aspects of fabrication in mind. The doubler featured stubs on its input waveguide that were significantly larger than the stubs used on the output guide of the tripler. The cavity design selected for the doubler stubs was also chosen to allow the wet etchant greater access to the sacrificial release layer.

The stub design adopted for the tripler was chosen with strength as the primary consideration. In thin layers of released SU8, curling often occurs. The removal of a large section of SU8 to form a cavity in a 100μm thick stub would therefore increase the likelihood of deformation in the patterned layer. HFSS was used to validate the design presented in fig. 3.26 after trial versions were fabricated using a photo-reduced mask plate.
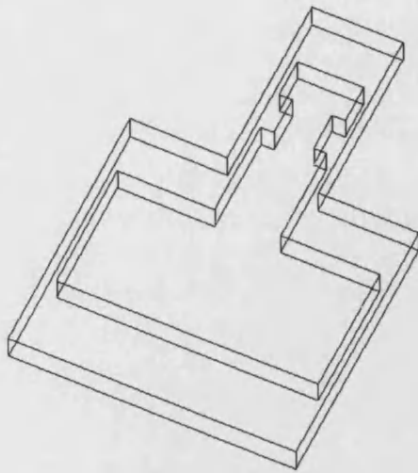
HFSS Model
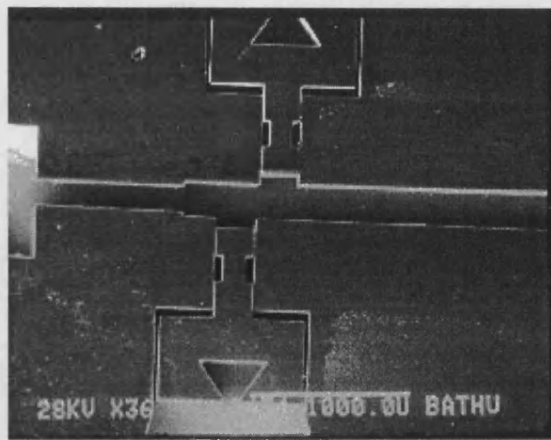
Tuners fabricated in SU8
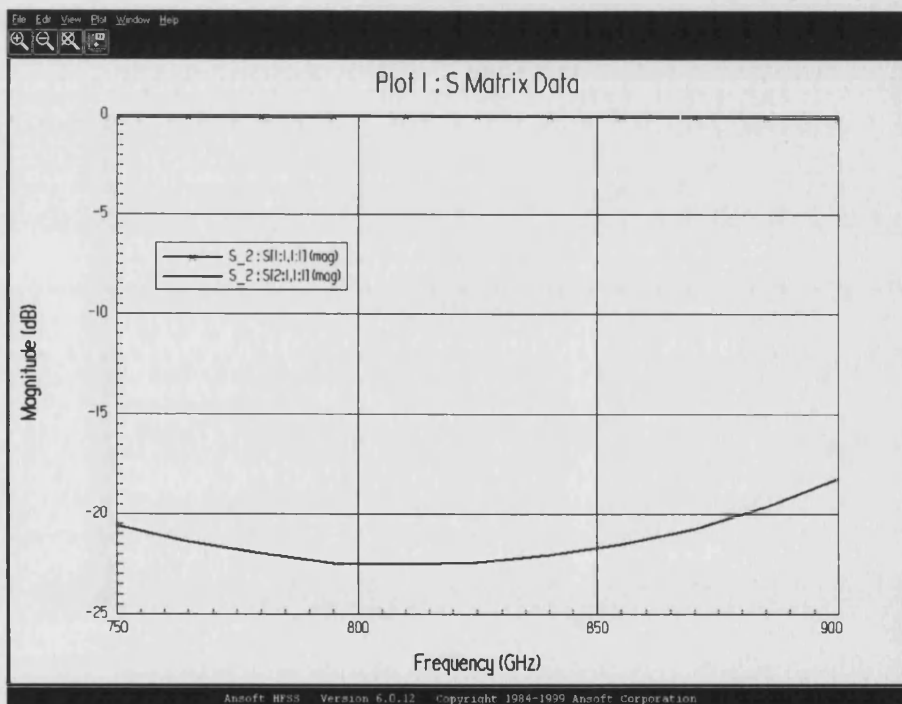
Figure 3.26. HFSS predicted S_{21} (plain line) and S_{11} (cross marker) for the tuning stubs employed in the frequency tripler (output guide – 3rd harmonic matching).
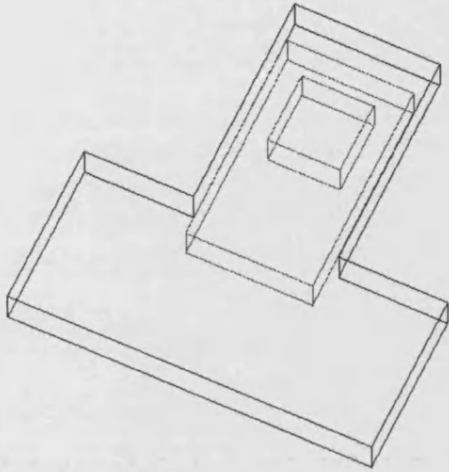
HFSS Model   Tuners fabricated in SU8
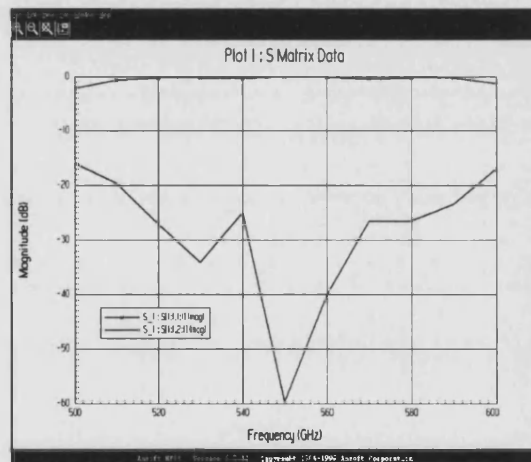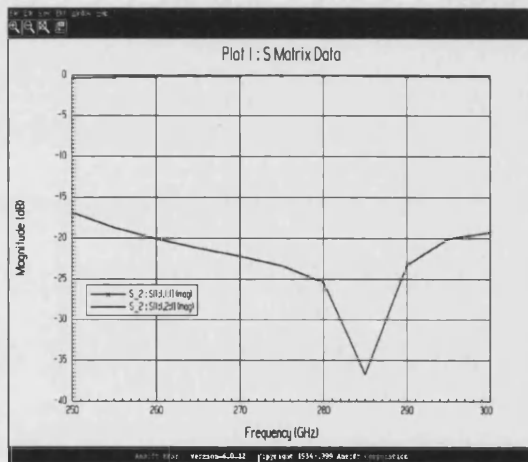
Figure 3.27. HFSS predicted S_{21} (plain line) and S_{11} (cross marker) for the tuning stubs employed in the frequency doubler (input guide – fundamental matching).

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3.7.2   Fixed versus tuneable stubs for multiplier application

Proven techniques exist that allow the production of tuning structures from SU8. Multiplier structures intended for use with Schottky devices can rarely be made as fixed tuned designs due to the highly reactive nature of reverse biased varactor diodes. It therefore follows that a low loss mechanism for tuning an integrated multiplier structure would be beneficial. Three methods were available that offered at least some degree of tuning flexibility beyond the fixed designs created using a single stage patterned SU8 approach. Of these methods one provides continuous tuning whilst the remaining approaches offer the ability to adjust fixed tuning cavities after device characterisation and prior to assembly of the 'flip-chip' multiplier.

Method 1

Step 1: Fabricate diode and stripline on base GaAs substrate.

Step 2: Measure C/V and I/V characteristics and derive values for C_{j0}, R_s, V_{br} and the turn-on voltage.

Step 3: From APLAC/HFSS analysis, derive optimum tuner positions for measured device.

Step 4: Fabricate multiplier top section on separate substrate and release tuning structures. Use micromanipulators to position stubs then secure them using either exposed SU8 or a commercial adhesive such as Loctite.

Method 2

Steps 1-3: As method 1.

Step 4: Selectively expose SU8 to form fixed tuned cavities. This procedure requires dual exposure of a single SU8 layer. The layer is first exposed with the tripler cavity pattern and tuning channels. These channels may be selectively exposed again to create terminations and the required shunt reactance values.

Method 3

Steps 1-3: As method 1.

Step 4: Construct a mount with micrometer drives that locate into the tuning stubs and thus produce a continuously tuneable structure.

A further refinement applied at microwave frequencies is a laminated or grooved stub face. The grooves run parallel to the side-wall across the face and impede the higher order modes having current flow parallel to the broad-wall. This technique could easily be translated into tuning stubs fabricated in SU8 with narrow slits created via simple cutouts in the optical mask pattern.

3.8 Waveguide transformer design

3.8.1 Multisection transmission line transformers

An in-line waveguide scheme has been adopted for the micromachined frequency doubler and impedance matching is required to efficiently couple power at the third harmonic from the input circuit to the output circuit. Impedance transformers can be implemented using stub tuning as well as in-line arrangements [10, 12, 26]. Initially, a two-stage waveguide transformer was designed, based on the layout shown in figure 3.28. SU8 was not available at that time and the adopted design for the frequency tripler was an in-line scheme based on conventional resist processing. The binomial transformer was investigated with this application in mind.
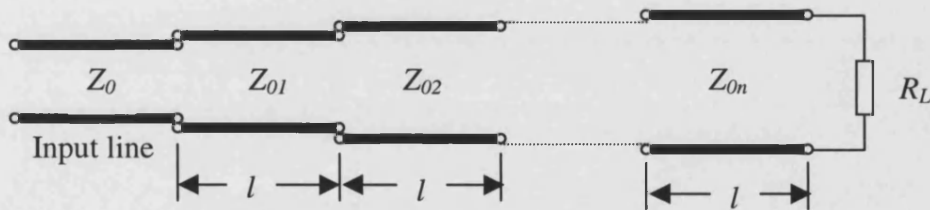
Figure 3.28. A general multi-section quarter-wave
transformer with $l=\lambda/4$ at the centre frequency

Figure 3.28 illustrates an n-section quarter-wave transformer for matching a resistive load R_L to an input line of characteristic impedance Z_0. The lengths of the line sections are identical if the wavelength is constant in all sections. For a maximally flat response the line sections are selected so that $|\Gamma_{in}|$ and its first (n-1) derivatives with respect to frequency are zero at the design frequency. This ensures the flattest possible $|\Gamma_{in}|$ versus ω characteristic at that frequency. Increasing the number of sections reduces the variation of input VSWR with frequency. The theory of maximally flat filters is given in [12]. An approximation that is widely used for this

kind of transformer is based on binomial coefficients [26]. This method was used for the following two-stage transformer, designed to match a quarter-height input waveguide (Z_0 = 76Ω at fundamental, a=800μm) to an approximately full-height output waveguide (Z_0= 434Ω at 3rd harmonic, a = 230μm). The following relation gives the required impedance for the kth section.

$$Z_{0k} = Z_0 \left(\frac{R_L}{Z_0} \right)^{\frac{M_k}{2^n}} \qquad k = 1,2,...n \qquad (3.22)$$

Where M_k is related to the coefficients of the binomial expansion given by,

$$M_k = C_1 + C_2 + ... + C_k \qquad k = 1,2,...n \qquad (3.23)$$

$$C_k = \frac{n!}{(n-k+1)!(k-1)!} \qquad k = 2,3,...n \qquad (3.24)$$

For the two-stage transformer mentioned previously,

$$Z_{in} = 76\Omega, \quad Z_{01} = 117\Omega, \quad Z_{02} = 282\Omega, \quad Z_{out} = 434\Omega \qquad (3.25)$$

Designed early in the project, it was intended that this transformer would be fabricated using conventional resist. With this in mind, the structure had to be of single height resulting in a guide wavelength that was not constant throughout the transformer. The lengths of the transformer sections were thus designed as $\lambda_{g01}/4$ and $\lambda_{g02}/4$ where λ_{g01} and λ_{g02} were the 1st and 2nd section guide wavelengths. The guide widths required to achieve the desired impedance at the 810GHz design frequency were a_1 = 540μm and a_2 = 280μm (b_{in}=b_1= b_2= b_{out}=100μm). The structure and S-parameter plots, as modelled in HFSS, are shown in fig. 3.29.
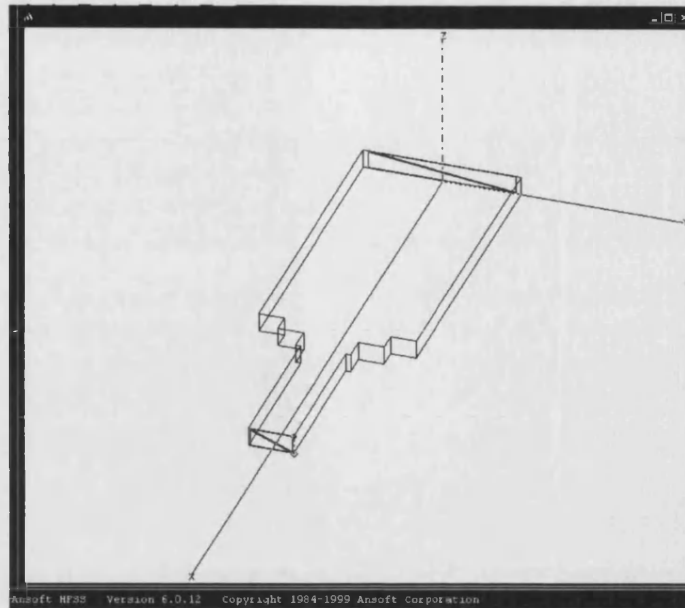
(a)
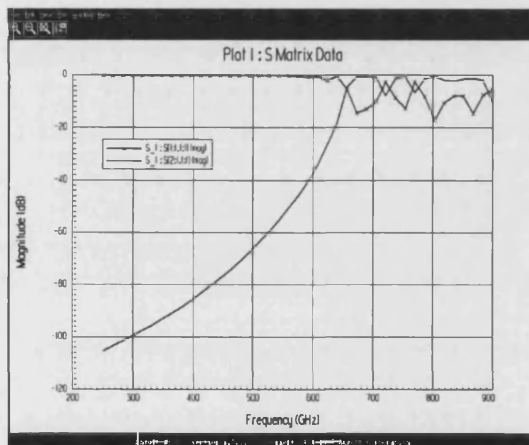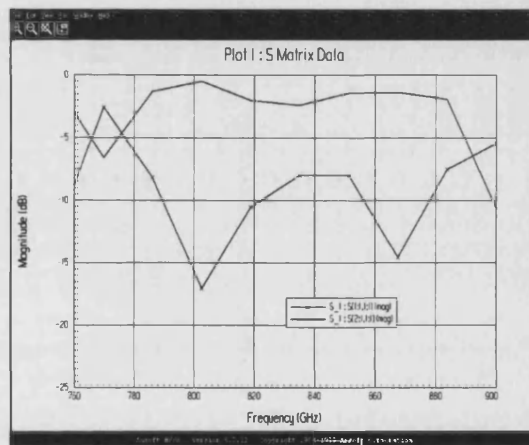
(a)   (b)

Figure 3.29. Waveguide transformer design based on binomial method.
(a) HFSS model, (b) and (c) HFSS predicted S_{11} (cross marker) and S_{21} (plain line).

3.8.2   Tapered-line transformers

An alternative to the multi-section transformer is a tapered-line transformer. A full
analysis for this type of matching network is presented in [12]. A tapered transformer
presents minimal mismatch when the length of the tapered section exceeds the guide
wavelength. The tapered transformer therefore has a high-pass characteristic as
opposed to the band-pass response of a stepped multi-section transformer. These

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transformers can be designed with different pass-band characteristics according to the nature of their taper (linear and exponential are two examples).

Smooth transitions within waveguides designed for sub-mm wave applications are difficult to machine using conventional methods, however no such limitations exist with the micromachined variety. For the purposes of the doubler a linear tapered transformer was selected and modelled using HFSS (fig. 3.30). This component could be implemented with either AZ or SU8 thick resist processing.
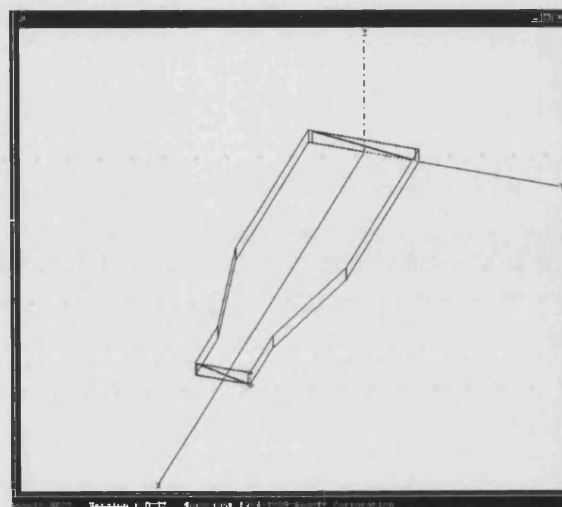
(a)
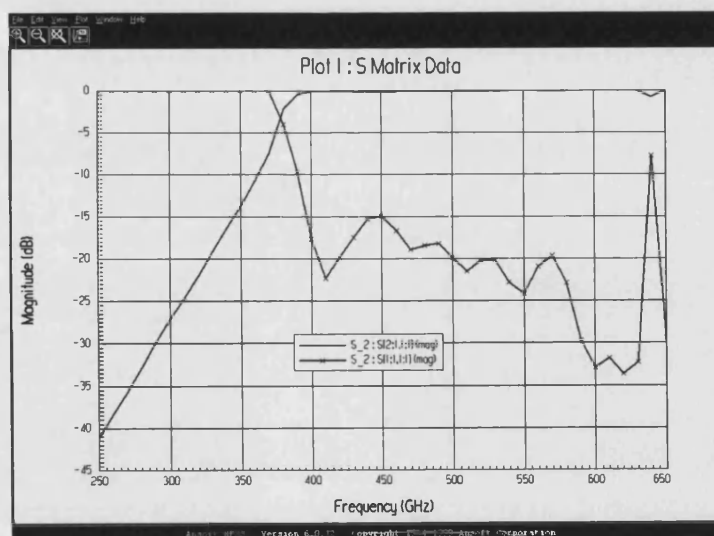
(b)

Figure 3.30. Linearly tapered waveguide transformer.
(a) HFSS model and (b) HFSS predicted S_{21} (plain line) and S_{11} (cross marker).

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4. Fabrication

4.1 Photolithography: an overview

Much of the work contained in this thesis is based on conventional resist processing. In order to produce useful structures with application in the sub-mm wave region, the techniques employed for standard planar processing have to be altered in order to cater for much thicker photoresist layers. Although transformed from an essentially planar approach to a three-dimensional one, MEMs thick resist processing abides by the same principles that govern conventional resist processing. Sample preparation, resist coating/baking and selective UV exposure and development are all cornerstones of the work presented in this chapter. The following section reviews the basic principles behind conventional lithography and briefly describes the tools that were necessary for the fabrication work presented later in this chapter.

4.1.1 Conventional photoresist

Photoresist is a liquid that is designed with a prescribed solid content to give a uniform film of specified thickness when spin coated onto a substrate. The resist contains a photosensitive polymer. Under UV illumination, polymer chains fracture in positive resists, whilst cross-linking occurs in the polymer chains of negative resists. Following development, areas of positive resist subjected to UV dissolve whilst areas of negative resist exposed to UV remain. Coupling selective exposure to deposition and etching techniques allows a substrate to be patterned in a wide variety of ways.

For the positive photoresist processing described in this chapter, Shipley and Hoechst resists were employed. For high-resolution applications including anode via hole etching and plating, Shipley S1813 was spun to produce films approximately $1\mu m$ in thickness. Hoechst AZ4533 resist was employed for the ultra-thick layers (around $100\mu m$) required for forming electroplated waveguides. Hoechst AZ4562 was found to be the optimal resist for the novel electroplated device contact post, described in section 4.5.

AZ4533 and AZ4562 resists are designed to give nominal films of thickness 3.3 and 6.2μm respectively across a 4inch wafer when spun at 4500rpm for 30s. Hoechst AZ400K was the chosen developer for the AZ resists, normally used in 3.5(DI water):1(developer) concentration. Microposit 351 developer was used in conjunction with S1813 and mixed 3.5:1 in DI water.

4.1.2   Equipment

The techniques developed for this project and the group projects preceding it, were all carried out using the equipment available in-house at the University of Bath. Therefore, the work carried out in this project would be repeatable in most small cleanrooms. Using techniques developed for thick layer processing of AZ resists and with the arrival of SU8, low cost, high quality surface micromachining for sub-mm wave component fabrication is viable and inexpensive. SU8 in particular offers a far less expensive alternative to LIGA style processing routes, previously obligatory for high aspect ratio surface micromachining [1].

Fabrication work was divided between the Department of Physics cleanroom and the Terahertz Technology Group laboratory. Resist coating, baking and development were performed in the cleanroom, as were all stages of processing preceding Schottky anode formation. A second DPI (Dage Precima International) mask aligner became available midway through this project and this was installed in the laboratory and modified to improve the profile of imaged SU8. The primary modification involved elevating the lamp housing by approximately one metre and inserting a black tube with periodic baffles into the gap between the UV outlet and the mask holder. This measure ensured a highly collimated beam at the substrate level. Increasing the duration of each exposure compensated for the UV power loss associated with greater bulb/sample separation. In addition, the optical components fitted to provide sample alignment were replaced with a bracket that accepted a Leica GZ-6 microscope head.

An Edwards 306 thermal evaporator housed in the cleanroom allowed ohmic and Schottky contact deposition in addition to simple gold layers required during formation of waveguides, ground planes and stripline contacts. A Nordica SiO_2 sputtering system, also contained in the cleanroom, allowed dielectric passivation layers to be deposited. Electroplating, using a Keithley 220 constant current source

and Keithley 617 electrometer, took place in the lab. For fabrication of the novel electroplated whisker, a stereo microscope was modified to accept a substrate heater and micromanipulators and this microscope was located on a vibration damped bench. In the remainder of this chapter, processing schemes for doubler, tripler and detector structures are presented. Detailed descriptions and diagrams of all processing stages are provided and accompanied with SEM and optical photographs of the completed structures.

4.2   Thick resist processing using standard positive resists

Before the specialist MEMS resist SU8 became available, micromachined waveguide structures at Bath were exclusively formed using conventional resist. Hoechst resists AZ4562 and AZ4533 have been successfully employed to form waveguides with operating frequencies ranging from 200-1600GHz [2,3]. Treen, Brown and Cronin [4] developed a ramped baking procedure for the thick resist films necessary in the fabrication of waveguides in this frequency band. The profile of this bake is shown in fig. 4.1. The authors also demonstrated that micromachined waveguide structures with internal contacting posts were realisable. Wootton et al. and Kazemi et al. advanced the technique and produced 600GHz and 1.6THz integrated detector structures [5,3].
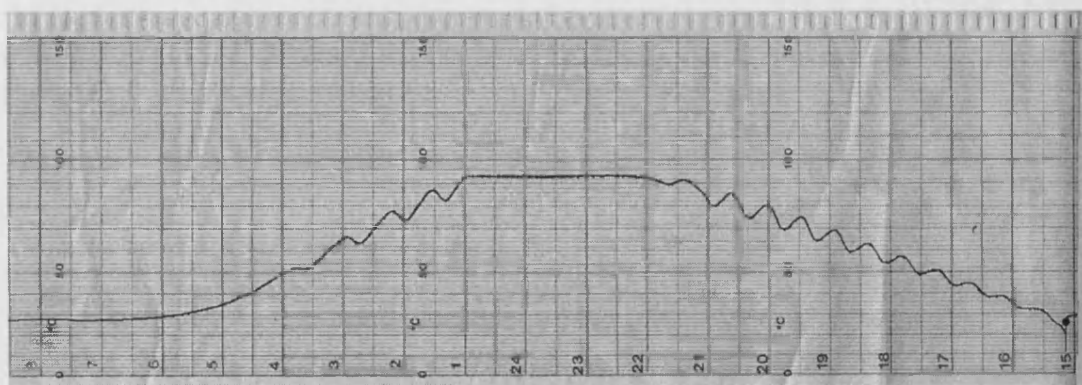
Figure 4.1. Ramp bake temperature plot

(time reads right to left, marked in one hour time divisions)

4.2.1   Application and baking

Application of thick resist layers had traditionally been performed at Bath using short duration spins (typically less than three seconds). The resist films produced using this method were perfectly suitable for fabricating waveguides, but lacked reproducibility

in the spun layer thickness. As waveguide height and therefore characteristic impedance is directly determined by the resist layer thickness, an accurate and predictable means of producing resist layers was sought.

Trials with low-speed spinning were successful (figs. 4.2 and 4.3), but at that time required an additional spinner to be installed in the cleanroom. In order to prevent disruption and minimise space consumption, a zero spin approach was adopted. Using a micropipette, measured volumes of resist were applied to substrates with constant area and the resulting baked resist layers were measured optically using a Leica microscope fitted with a 100x objective lens. AZ4533 and Shipley S1813 resists were successfully dispensed, baked and patterned and calibration graphs are shown in figs. 4.4 and 4.5.

The micropipette (Gilson Pipetteman P20) was supplied with standard tips (impervious to resist/acetone) that were shortened by 5mm when used with AZ4533. This reduction in length increased the bore diameter of the tip (from approximately 1mm to 2mm in diameter) ensuring that the prescribed volume of AZ4533 was consistently loaded. For the less viscous S1813 resist, the tips were left as standard. The high viscosity of AZ4562 prevented reliable operation of the pipette and the thickest films (up to 200μm) were produced using AZ4533. A plot showing the uniformity of a baked resist layer on a 10x10mm substrate is shown in figure 4.6. During development unexposed resist suffered some degradation in surface quality, visible as a slightly matt appearance. The degree to which the film thickness of this resist was affected was of the order of a micron and therefore negligible.

The ramp bake developed by Treen and Brown was eventually replaced by a faster ramp with no reduction in the quality of the finished formers. This bake began from room temperature and ramped to 85°C in 10°C/hour steps, the ceiling temperature was held for 3 hours and the ramp down was 15°C/hour. A constant six hour 90°C oven bake has also been used and 100μm thick formers successfully exposed and developed in this layer (fig. 4.7). Clearly some flexibility is afforded in baking the thick resist. For resist layers spun around existing structures, including contacting posts, ramp baking was adopted and found to reduce fractures and improve the sample yield.
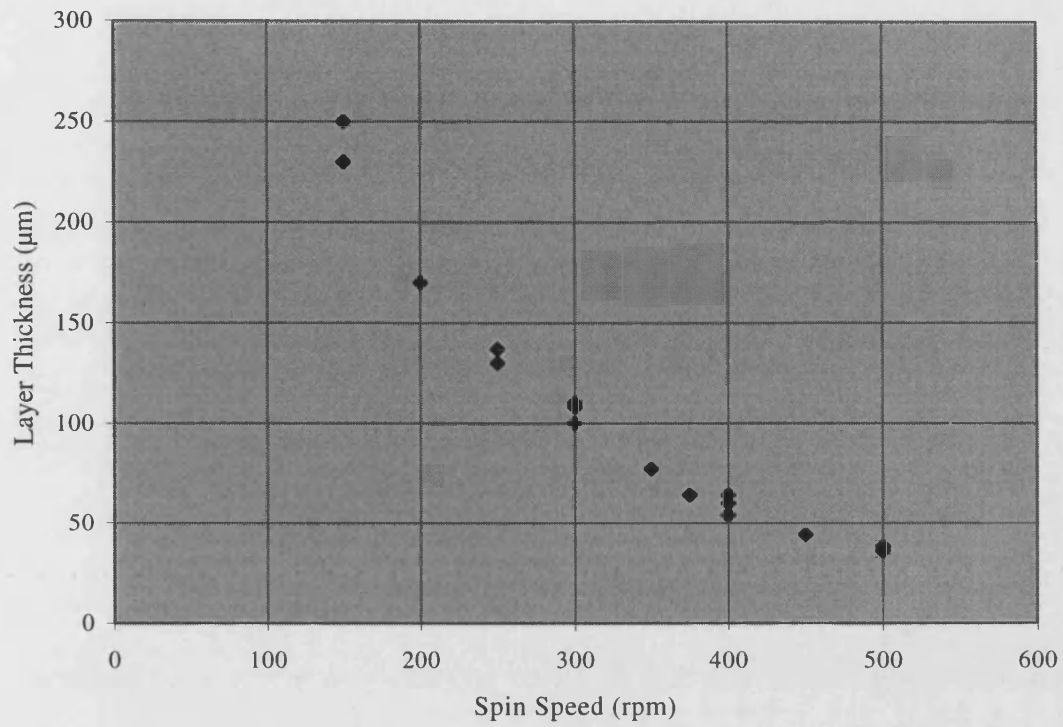
Figure 4.2. Spin calibrations of AZ4533 resist using 1inch-diameter substrates.
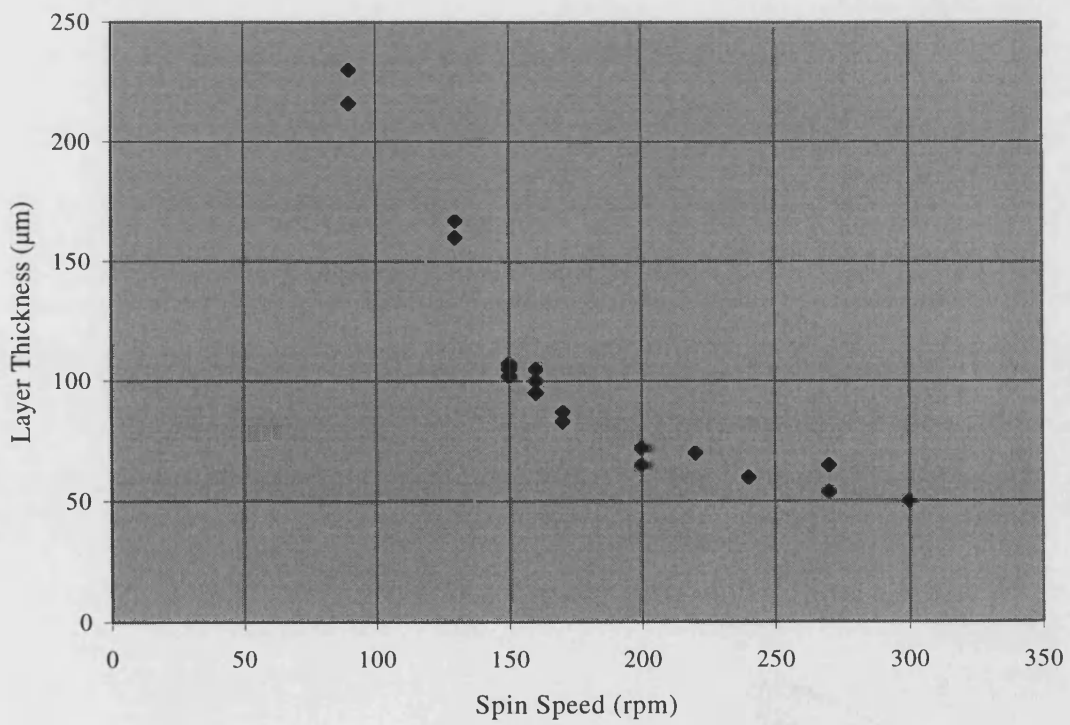
Figure 4.3. Spin calibrations of AZ4533 resist using 1.5inch-diameter substrates.

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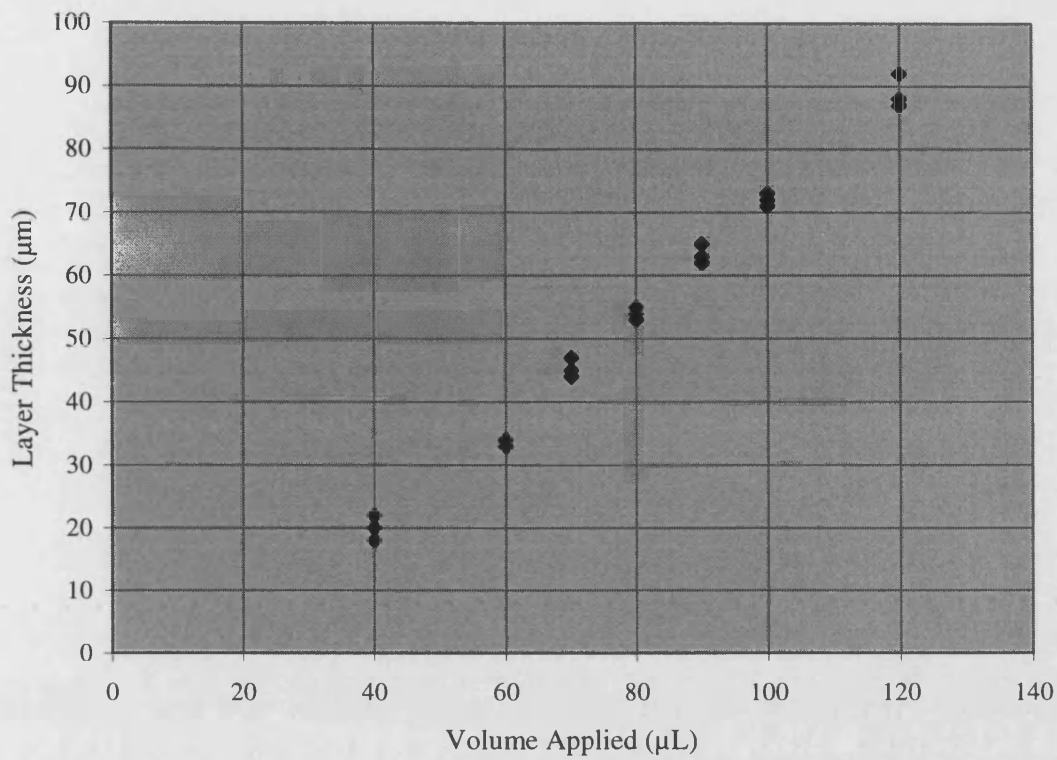
Figure 4.4. Layer thickness against applied volume of
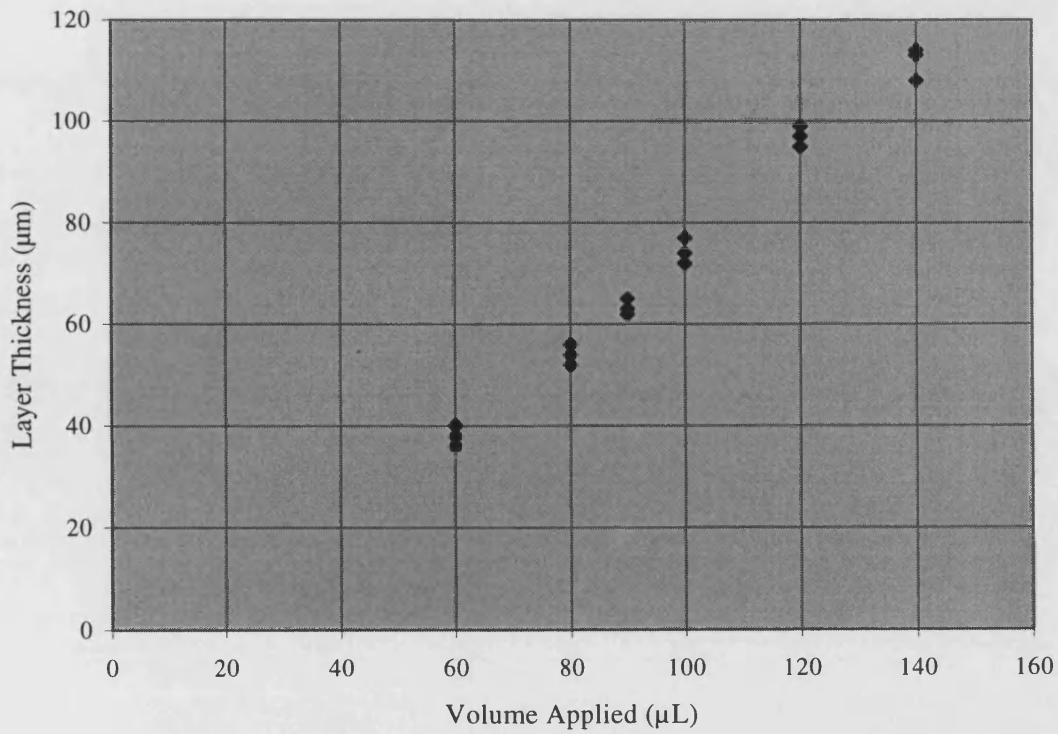S1813 photoresist (1.5-inch substrate).

Figure 4.5. Layer thickness against applied volume of
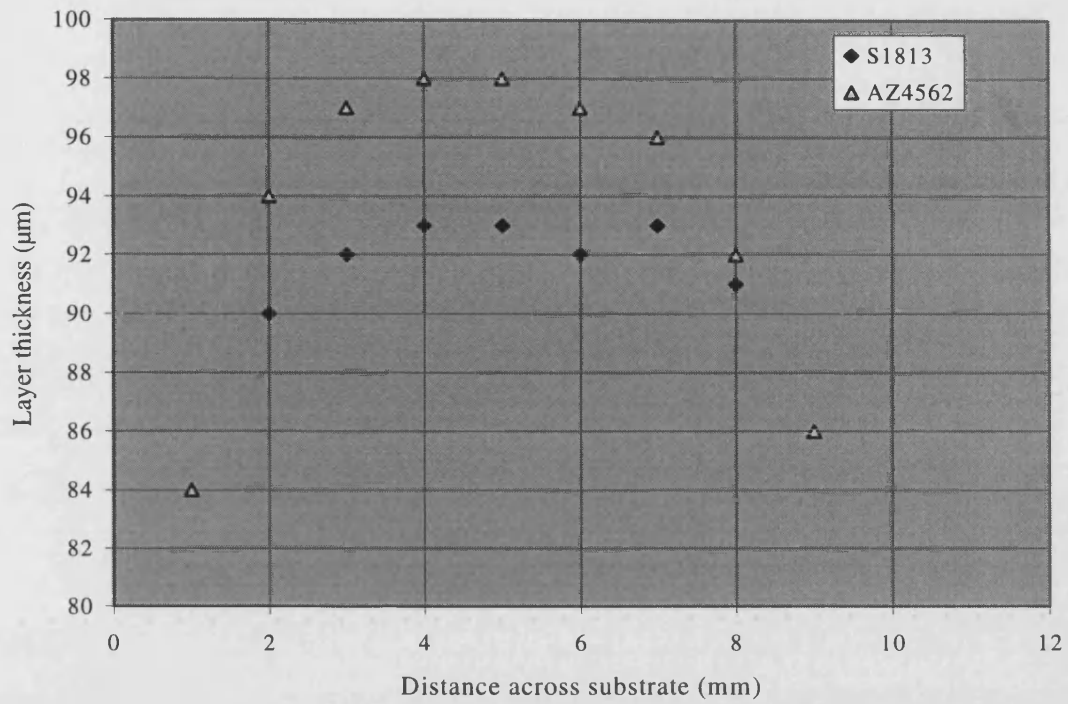AZ4533 photoresist (1-inch substrate).

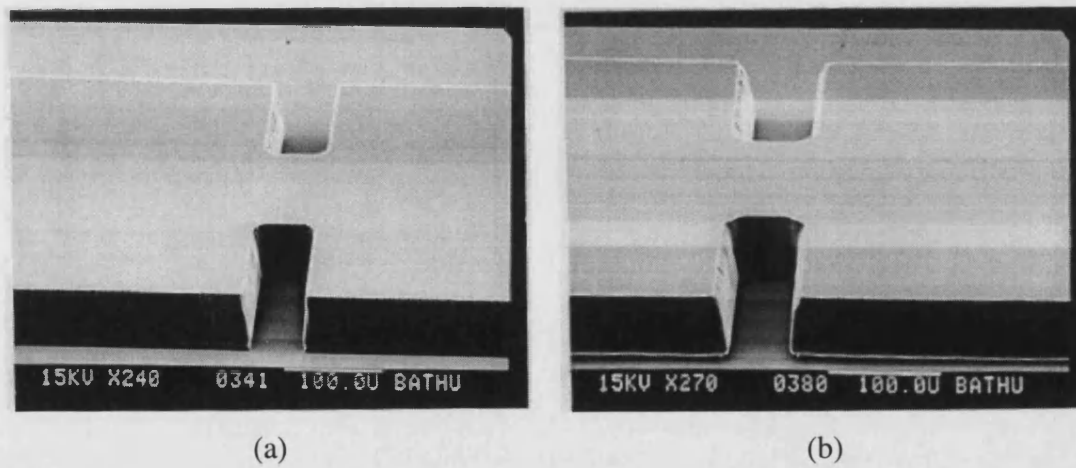Figure 4.6. Thickness measurements from micropippette deposited AZ4533 and S1813 (1.0 x 1.0cm substrates).

(a)   (b)

Figure 4.7. Waveguide formers realised in conventional resist using
(a) the ramped oven bake above and (b) a six hour 90°C oven bake.

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4.2.2 Exposure and development

Due to the lack of transparency of thick positive resist, exposures were performed on a Karl Suss MJB3 mask aligner. This aligner provides a higher dose than is possible with the DPI model, owned by the Terahertz Technology group. The MJB3 offers reduced UV beam collimation when compared to the group aligner and as a result its use was restricted to thick opaque resist layers and standard planar resist processing. A dose of $10mW/cm^2$ was quoted for the MJB3, although this changed with the age of the bulb. Typical duration of exposure for a $100\mu m$ thick resist layer was 40 minutes, but test exposures were always performed as a means of establishing dose strength at any given time.

Development was performed in 4:1 DI water:AZ400K. As unexposed conventional resist eventually dissolves in developer, exposure times were increased to a maximum (but reduced to a point where detrimental heating effects did not occur) and development times were minimised.

For resist films above $100\mu m$ in thickness, multiple exposures were attempted using an evaporated gold layer subsequently patterned and etched to replicate the original mask shape. These trials proved partially successful however resist undercut often caused the mask pattern to lift away from the former, rendering further exposures impossible. A faster method involved a simple dual exposure, using the conventional optical mask plate to image the resist a second time after 5 minutes of development. Aligning to the partially developed pattern was critical in order to prevent distorted side-walls, but this proved readily achievable with the standard optical alignment available on the MJB3.

Chlorobenzene treatment is an established planar processing technique that hardens the top surface of a resist layer, promotes undercut during development and thereby improves lift-off. It was hoped that unexposed resist subjected to long developments and/or extended contact to platinum plating solution could be protected using Chlorobenzene treatment. Soaks of up to 3 minutes had no noticeable effect, whilst longer soaks tended to cause imperfections in the resist layer. Providing exposure doses were sufficient, formers in $100\mu m$ thick resist layers could be completely

developed with no need for additional treatments and no significant marring of the resist surface. Engelhard platinum plating solution (used for the drop plating method, section 4.6) did cause some damage to thick resist surfaces, but this could be minimised to a level deemed acceptable (maximum pit depth approximately 3μm) by reducing the plating temperature from 45°C to 25°C.

4.3 Greyscale and controlled exposure techniques

The modified application, baking and exposure/development parameters detailed in the preceding section enable 3-D wave guiding structures to be formed using conventional resists for application in the millimetre and sub-millimetre wave region. The ability to align a sequence of processing steps with micron scale accuracy is an obvious benefit of this integrated approach. A particular aim of this project was to develop ways in which to control not only the dimensions parallel to the substrate but also the perpendicular height of waveguide and antenna formers.

4.3.1 Greyscale technique

Greyscale patterning of resist was reported [6,7] for application in optical micro-lens fabrication and this technique was investigated with the intention of forming waveguides and antennas with varying heights. A micromachining technique offering accurate control of both E and H-plane dimensions in conventional resist would allow fabrication of components including E plane stepped impedance transformers and tapered antenna horns.

It was necessary to simplify the greyscale technique detailed in [6] due to equipment constraints. Pattern size reduction was achieved using a procedure based on conventional black and white film negatives. Grey scale patterns were drawn using Micrografix Designer 7.0 and printed onto standard A4 paper using an inkjet printer. The dimensions of the waveguide patterns were scaled up 20:1 and the printed sheet was attached to a purpose built camera stand. A Nikon FM-2 camera fitted with a 50mm lens was used to produce negative versions of the patterns on the A4 sheet. Distance from the lens to the printed sheet was set in order to give a reduction factor of 20. Following development and fixing, the negatives were mounted on a glass sheet suitable for use as a mask plate on the MJB3. UV exposure tests were

performed and as stated in section 4.2.2, a 100μm resist layer required approximately 40 minutes exposure for satisfactory development.

A single exposure through the greyscale mask was sufficient to transfer the pattern to the resist, however a dual exposure using a conventional mask and exposure followed by the greyscale exposure proved more reliable. This approach provided complete removal of unwanted resist surrounding the waveguide component prior to the greyscale exposure and development. The duration of the development was then selected to give the desired minimum thickness of resist, and therefore minimum height of the three dimensional structure.

Figure 4.9. Plated resist former with height steps 20-36-48-64-80μm implemented with photo-reduced greyscale mask.

4.3.2 Controlled exposure method

The basic principle for this method is shown in fig. 4.10. The sample is brought into close proximity with a standard mask plate (on the Karl Suss MJB3) and using the X or Y micrometer drives, selected areas of the photoresist layer can be exposed with differing doses. For the trial pattern shown in fig. 4.11, a simple dark field/light field mask plate was used to produce a stepped horn. As with the greyscale mask method,

best results were achieved using a primary exposure and development stage to produce the former, with a follow-up exposure/development cycle creating steps or tapers. The test pattern was produced using a 40-minute exposure to produce the former, then successive exposures of 10, 7, 5, 3, 2, 1.5, 1.0 and 0.5 minutes to produce the steps. The test pattern has height variation 50-52-55-58-63-68-75-82-90μm. 90μm thickness was achieved with no exposure.
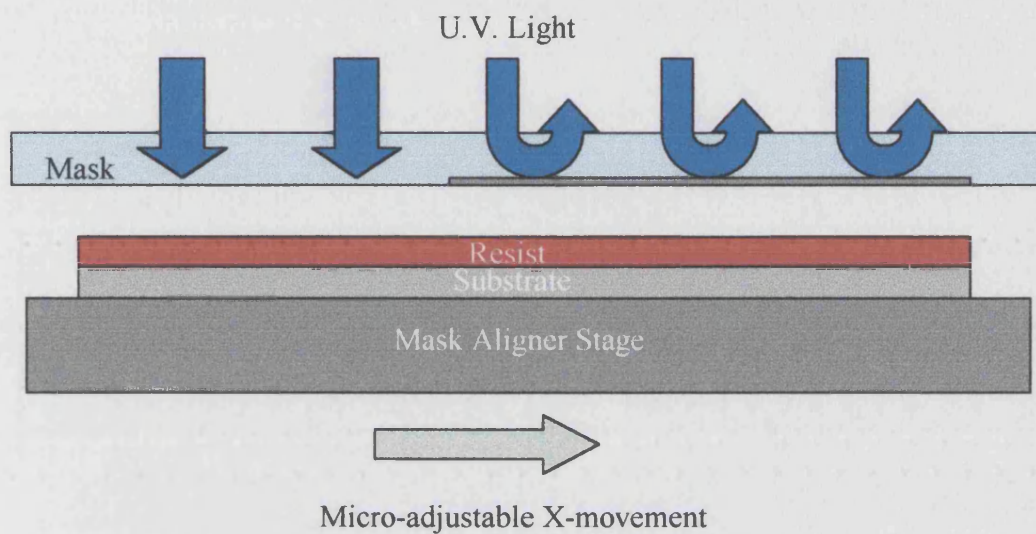
Figure 4.10. Principle of controlled exposure dose for variable resist thickness.
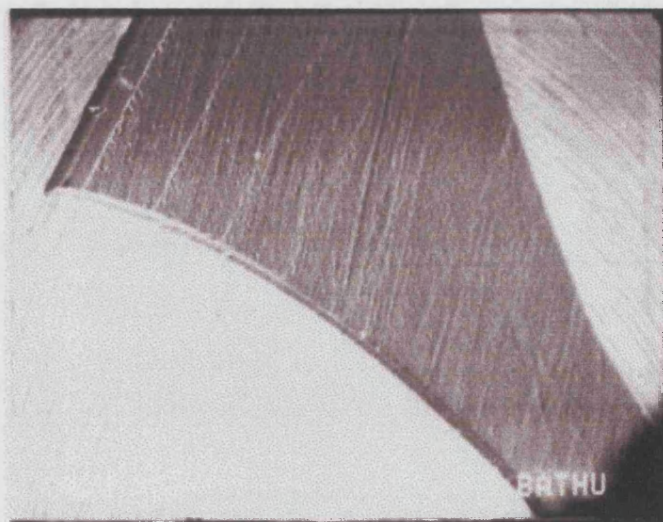
Figure 4.11. Stepped former fabricated using the controlled exposure method.

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4.3.3 Conclusion on greyscale and controlled exposure methods

As demonstrated here and in [6,7], conventional resist can be processed to form stepped and graded height layers. This is achievable using a single layer of AZ4533 for heights up to 100μm and height differences of up to around 50μm. Unfortunately, a limit was found when trying to create large height differences. When developing partially exposed AZ resist, the surface rapidly becomes pitted and uneven (evident in fig. 4.11). If desired total step heights exceed 40-50μm, the resist areas experiencing the highest UV doses become unusable due to severe surface deformation. This deformation in resist formers is translated into the components electroplated around them, resulting in poor internal surface quality. As a result, the greyscale and variable exposure techniques have limited application in fabricating useful sub-mm wave components.

4.3.4 Fabrication sequence for tapered feed horn

The following processing scheme (fig. 4.12) has been included to illustrate how a tapered feedhorn might be fabricated using greyscale/variable exposure techniques. With the achievable height difference limited by the surface quality of the partially exposed resist, this scheme is only applicable to horns with heights of 100μm or less over the waveguide height. A reasonable upper limit for the waveguide height being 100μm.
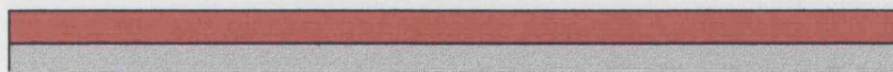
1.   Resist is applied by volume according to the calibration graph (fig. 4.5) and the desired maximum layer thickness.
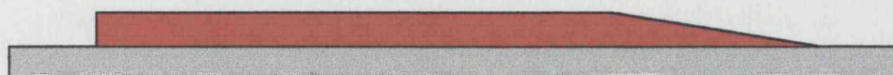
2.   A variable exposure is applied to the resist that will lie beneath the horn section of the former. Development leaves a tapered profile.

3. A gold seed layer is sputtered and followed by a nickel-plated layer. The plating is thick enough to support itself should the existing resist be removed. Gold is sputtered again to provide a tarnish free ground plane.
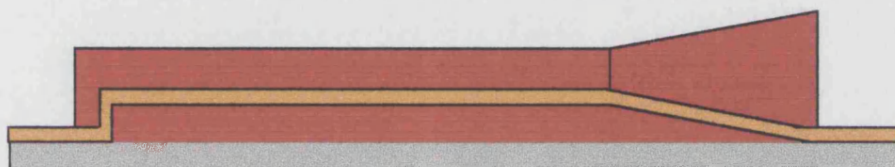
4. Another thick resist stage follows, once again with controlled volume giving the prescribed maximum thickness (fig. 4.5). Variable exposure reduces the waveguide height and produces a gradual rise in thickness for the upper half of the horn.
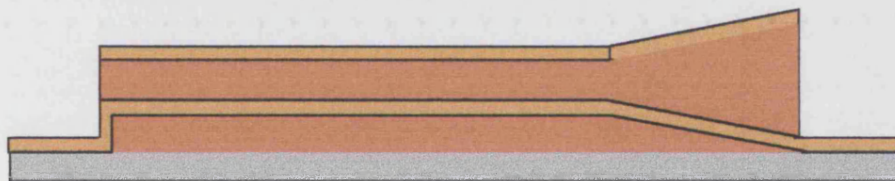
5. Gold is evaporated onto the second resist layer and again reinforced with a layer of plated nickel. The resist is washed out with acetone.

Figure 4.12. Processing scheme for tapered feedhorn fabricated from conventional photoresist using greyscale/variable exposure techniques.

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4.4 SU8 negative resist for MEMS applications

SU8 is a negative resist designed for high aspect ratio processing and resistance to harsh plating solutions. Achievable film thickness is up to 1000μm and beyond, and providing the bake and exposure are sufficient the near transparent SU8 allows successful imaging through these ultra-thick layers. The resist is based on epoxy resin technology, which possesses intrinsic adhesion characteristics superior to conventional thick resists. This is particularly beneficial on substrate coatings that may cause adhesion problems with normal resists, such as gold. SU8 has sensitivity in the near-UV, deep UV and E-beam regions and low optical absorption allows near vertical sidewall profiles and reported aspect ratios exceeding 18:1.

Once exposed, imaged SU8 must undergo a post exposure bake in order to fully cross-link the polymer chains in the exposed regions. Development takes place in EC solvent and immersion times can exceed one-hour with negligible loss or damage to the exposed SU8 [1].

In addition to its intended use as a material for electroplating formers, SU8 possesses mechanical properties that allow it to be used for moving parts. Applications in MEMs include sensors and cogs, whilst in the microwave and sub-mm wave field, passive structures including waveguide filters and tuning elements are possible.

As mentioned in the previous section, the ability to produce multi-height structures is particularly advantageous in the context of millimetre- and submillimetre-wave micromachined components. A simple example of how SU8 allows this could involve multiple spun and imaged layers that are aligned to form steps on a substrate. Stepped SU8 profiles have also been achieved using the variable exposure technique detailed in section 4.3. Due to the importance of the post exposure bake with regard to the SU8 surface quality (dictating the speed at which the partially exposed SU8 is developed), this method is less favourable than multi-layer approaches (shown in sections 4.14, 4.15).

The following processing scheme for SU8 was developed experimentally using trial patterns including waveguide irises (width 60μm), release trenches (depth 400μm,

width 50μm) and sacrificially etched tuning structures. Steps involving high temperature baking and associated thermal stress were avoided. This move towards lower temperature processing was driven by the requirement to process SU8 on substrates coated with an existing layer of conventional resist and/or featuring existing fragile microstructures.

4.4.1 SU8 processing

Substrate preparation: The substrate was immersed and ultrasonically agitated in Acetone and Isopropanol before undergoing a one hour 90°C dehydration bake.

Dispensing: The volume of SU8 dispensed affects the thickness of the final spun layer. The degree to which this occurs is far less pronounced for thinner SU8 varieties and greater applied volumes. Calibration plots have been produced for spun SU8-50 and SU8-5 (fig.s 4.13-4.16) where the volumes of applied SU8 were high and controlled only approximately. For thick films, the most economical method was performed on a hot plate mounted substrate (80°C) with no spin and approximate visually controlled volume application. SU8-500 was applied from a glass rod onto the heated substrate and spread manually to form a continuous layer. This layer tended to form with a domed profile thereby preventing intimate contact being achieved for mechanically assembled parts. It was decided to include a lapping stage that would ensure a planar layer profile. 2000 grade wet and dry silicon carbide paper was used to lap the SU8 layer down to the required thickness and polishing was achieved using a commercial fine abrasive fluid. This latter method also produced higher yield than methods involving spinning, due to lack of spin induced bubbling in the thick SU8.

Spinning: For those substrates that were spun, the results are shown for SU8-50 in figs. 4.13 and 4.14. Applications requiring films with 2-30μm thickness were eventually catered for with SU8-5 (figs. 4.15, 4.16). This thinner variant of SU8 allowed high speed spinning, without break-up or pin-holing in layers during the soft bake (previously a problem when spinning SU8-50 at high speed to form thin layers).

Softbake: Samples were normally baked on a hot plate at 110°C. The duration of the bake varied with thickness. The following minimum bake times were adopted (table 4.1), although it was found that these could be exceeded significantly with no detrimental effect to the subsequent processing. For certain thin film applications a long low temperature bake was adopted. This allowed successful imaging of SU8,

without damaging or hard baking any underlying conventional resist and/or fabricated microstructures.
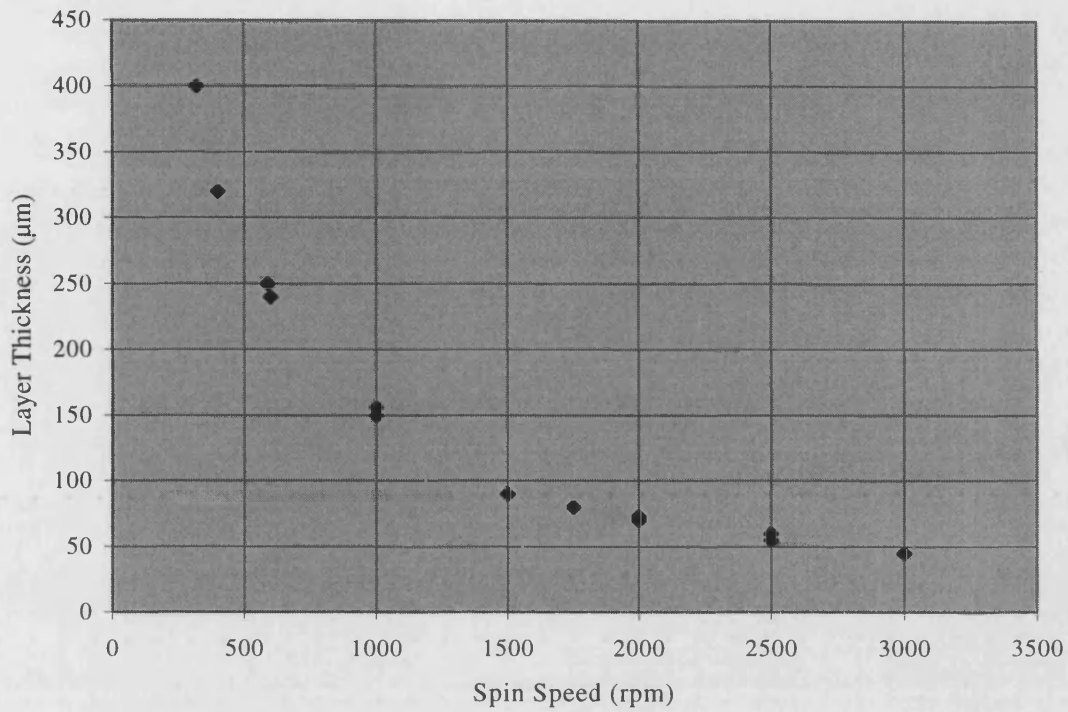

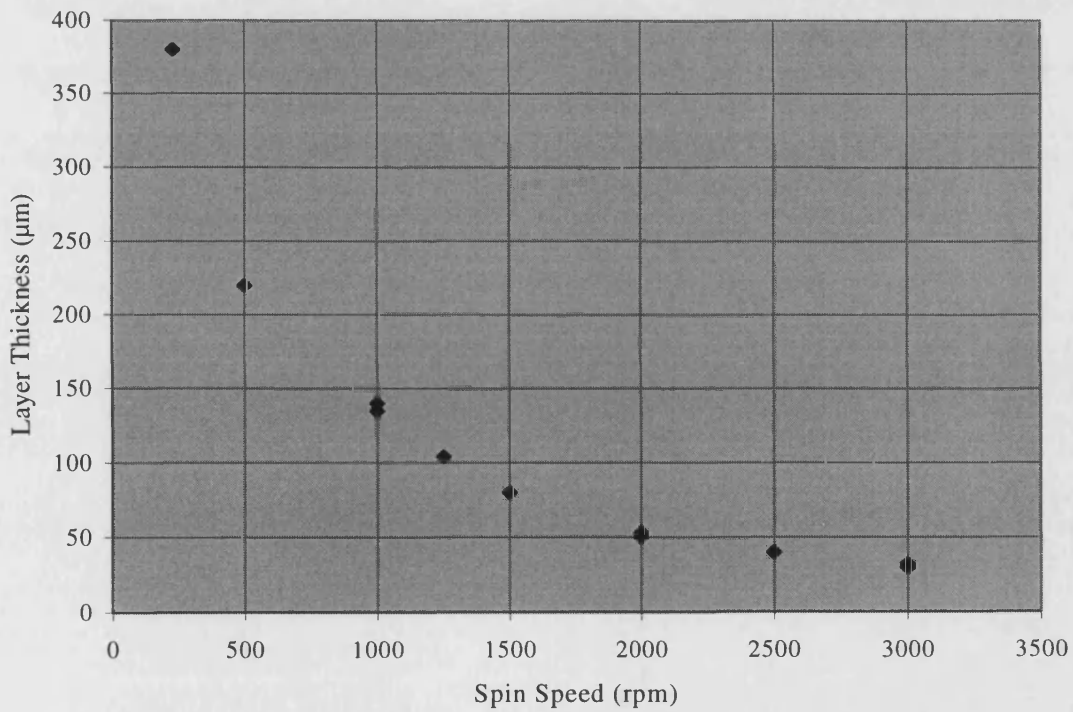Figure 4.13. SU8-50 layer thickness against spin speed (1-inch diameter substrate).

Figure 4.14. SU8-50 layer thickness against spin speed (1.5-inch diameter substrate).
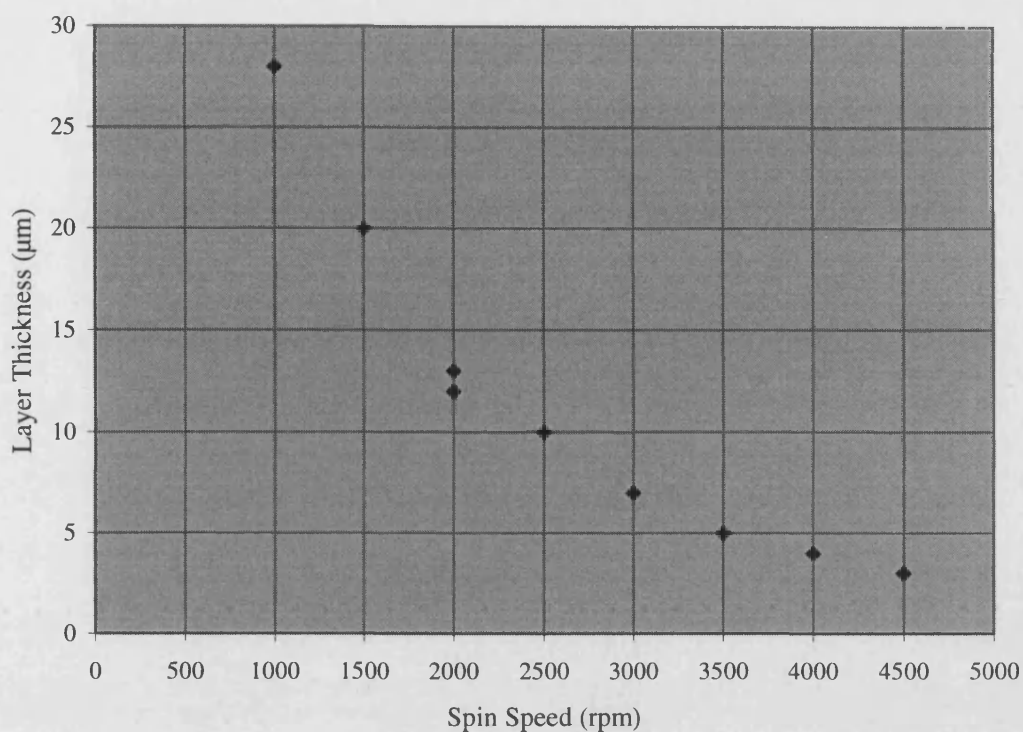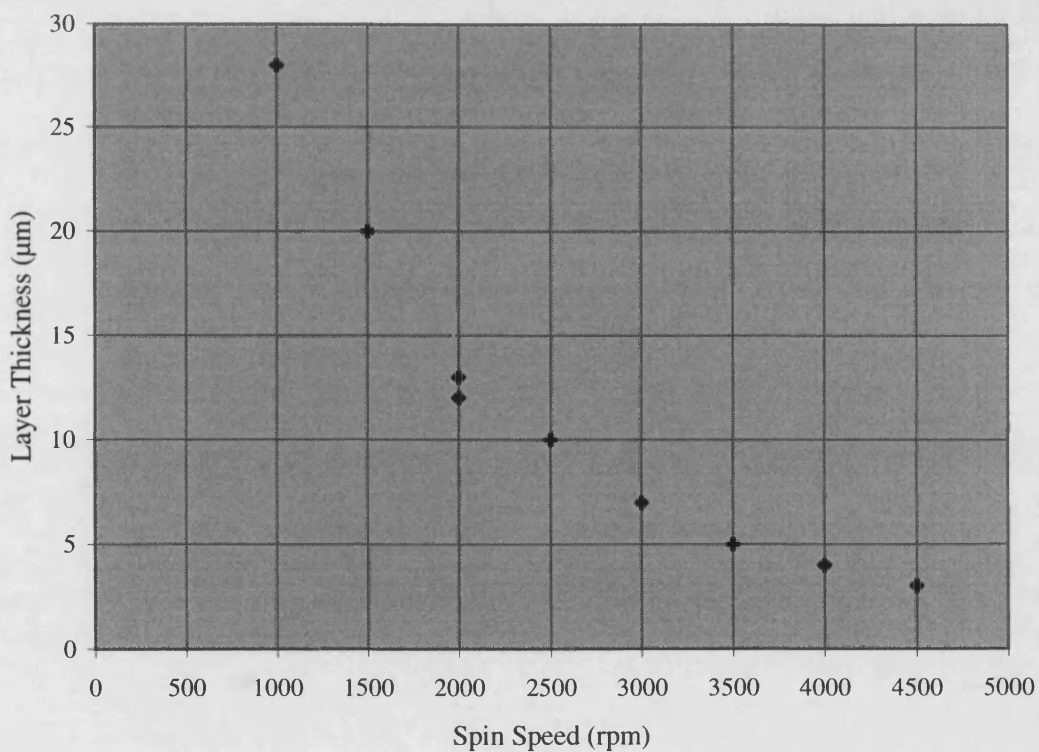
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Figure 4.15. SU8-5 layer thickness against spin speed (1.0-inch diameter substrate)

Figure 4.16. SU8-5 layer thickness against spin speed (10 x 0.5mm substrate)

Layer Thickness (μm)	Duration of hotplate bake (min)
10-20(SU8-5)	120 (50°C slow bake)
10-20 (SU8-5)	3
50 (SU8-50)	10
100 (SU8-50)	25
150 (SU8-50)	45
200 (SU8-50)	75
300(SU8-500)	140
500 (SU8-500)	Oven bake (25-110°C in 1 hour, 3 hours at 110°C, ramp down at 30°C/hour)
1200 (SU8-500)	Oven bake (25-110°C in 1 hour, 9 hours at 110°C, ramp down at 30°C/hour)

Table 4.1. Required bake times for specified SU8 layers.

Exposure: The recommended UV dose is approximately 100mJ/cm^2 per 10μm thickness of resist. For thick layer applications, particularly those requiring near-vertical side-walls and/or narrow trenches, exposures were performed on the modified mask aligner described in section 4.12. As with the softbake, considerable flexibility is afforded in the exposure of SU8 and the following may be regarded as minimum times.

Layer Thickness (μm)	Exposure time (mins)/Est. Dose (mJ/cm^2)
50	5/600
100	10/1200
150	15/1800
200	20/2400
300	40/4800
500	70/8400
800	100/12000

Table 4.2. Required dose for full exposure of specified SU8 layers.

Post Exposure Bake (PEB): The manufacturer recommends a 100°C hotplate bake for 5-30mins. In an effort to eradicate cracking and alleviate stress at the SU8/substrate interface, an extended duration, lower temperature bake was successfully employed. The SU8 waveguide (layer thickness > 100µm) structures featured in this thesis were all subjected to long (3-12 hours), low temperature (45-70°C) PEBs. Adhesion problems and unwanted lifting during development were significant on some samples undergoing higher temperature PEBs; this was not encountered with samples experiencing low temperature PEBs.

Development: Using the aforementioned processing, exposed SU8 could survive 3 hours in EC Solvent (PGMEA) with no noticeable deterioration of surface quality or rigidity. For layers much thicker than 100µm, immersion times exceeding 20 minutes were normally necessary but did not prove problematic. Agitation using a stirrer reduced development time but was not critical to successful development.

(a)   (b)
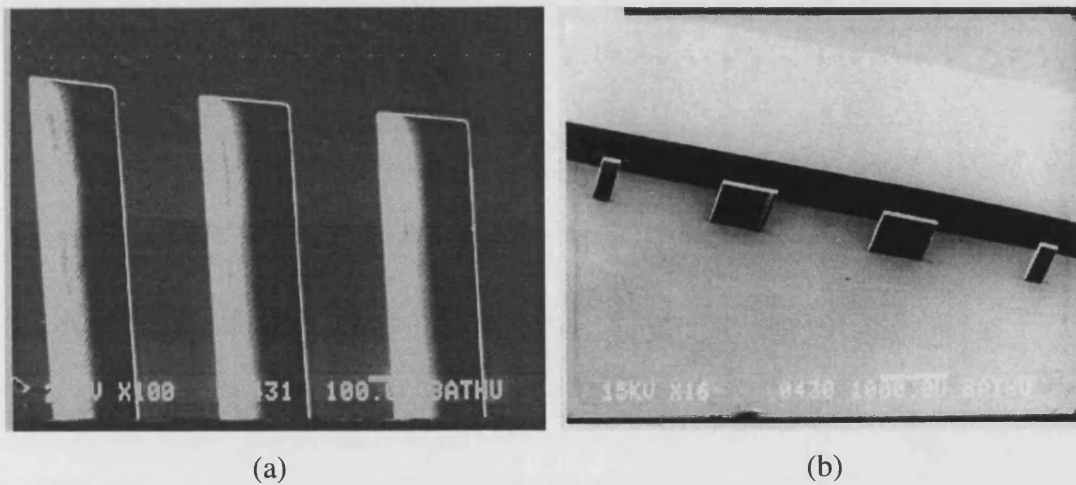
Figure 4.17. (a) 400µm deep trenches formed in SU8-500 and (b) 60µm wide septa formed in SU8-500 (layer thickness 800µm).

4.5   The electroplated whisker method

A method has been devised for electroplating low capacitance platinum contacting posts and is described in [3]. This method has been revised for the work contained in this thesis allowing increased alignment accuracy and enabling contact to pre-formed Schottky anodes. A summary of the new procedure is provided in this section. Fig. 4.18 is a schematic view illustrating the apparatus used.

Stereo Microscope

Cathode Contact   Phosphor-Bronze Whisker

Sub-Micron Etched Tip

AZ4562 Layer

Substrate Heater
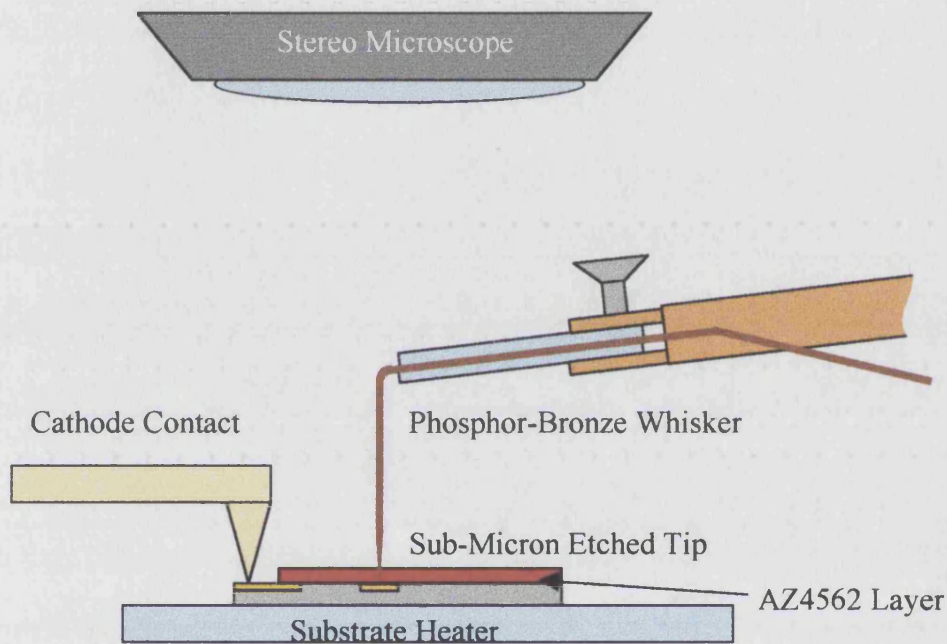
Figure 4.18. Apparatus for Aligned Whisker Method.

Electroplating of the whisker takes place following formation of a Schottky anode array electroplated through vias formed in a sputtered SiO_2 layer. This array is formed within an ohmic ring in order to minimise the series resistance of the finished device. For both the frequency tripler and doubler, AZ4562 was spun at 2500rpm for 7 seconds on a substrate measuring 0.5 x 1.0cm, producing a layer thickness of 15-17μm. Whilst this resist was still wet the etched wire was brought into contact with a single device within the array, using a purpose made probe assembly and micromanipulator. Alignment of the whisker within the ohmic ring (fig. 4.19) was achieved with the aid of a stereo microscope (max. magnification x100). A substrate heater was set at 45°C and the resist was allowed to dry for 2.5 hours. Fig. 4.20 shows an electron micrograph of an etched 50μm diameter phosphor bronze wire.

Etching was performed using 10: 1 DI Water: NaOH and a constant current of 1.0mA. The etched tip is of the order of a micron when using 50µm diameter wire and this can be reduced by using 25µm diameter wire [3].
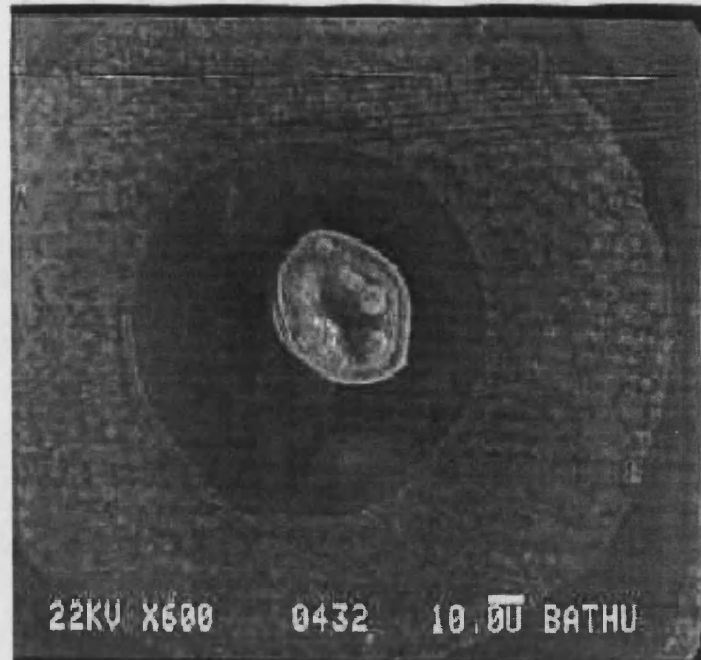
Figure 4.19. Electroplated platinum whisker located within 100µm diameter ohmic ring

Figure 4.20. 50µm diameter phosphor bronze wire with electrochemically etched tip.

4.6 The drop-plating method

Allied to the whisker method, the drop plating method was developed in order to electroplate platinum microstructures and has since found application in the fabrication of Schottky arrays. The technique allows comparatively easy fabrication of contacting posts and anodes with little chance of stray plating elsewhere on the substrate.

The drop plating method follows the whisker method and begins by applying a small drop of platinum plating solution to the substrate (when resist is dry) such that the drop surrounds the phosphor-bronze whisker. The whisker is then retracted using the Z movement on the micromanipulator. A temporary vacuum results in the recess left by the whisker tip and this causes the platinum solution to flow to the pre-formed anode. A platinum probe is then substituted for the whisker and plating can begin. If a contact hole to a pre-formed device has been formed, then plating can usually begin with a current of 10nA and this can be increased to 30nA after 30mins. Schottky diodes produced for application in the doubler and tripler were contacted using both 25μm and 50μm phosphor bronze whiskers and the aforementioned current values were suitable in the majority of cases. Occasionally initial plating at 10nA caused the measured anode-cathode voltage to be unstable and in this instance pulse plating (see section 4.8.3) was adopted. Sub-micron whisker contacts directly to GaAs required lower current values and relied initially on pulse plating [3].

4.7 Processing sequence for Schottky anode formation

4.7.1 Passivation and ohmic contacts

The GaAs wafer was scribed and cleaved to provide substrates with the required dimensions (normally 10.0 x 5.0mm). Before depositing the silicon dioxide layer, the substrates are cleaned with Trichloroethane, Acetone and Isopropanol and baked at 90°C for at least one hour. Silicon dioxide is sputtered onto the substrate to a thickness of approximately 0.2μm using a Nordica RF sputterer. This layer thickness was verified using a tallystep and visually, using the known colour/thickness relationship.

Following SiO_2 deposition, the substrates were spun with AZ4533 (4500rpm, 30s) baked and patterned to form windows for the ohmic features. Etching in buffered HF (duration 70s, 20°C) removed the SiO_2 from the areas opened in the resist. The ohmic recipe selected for the contacts was Germanium(20nm)/Gold(50nm)/Titanium(20nm) /Gold(200nm) [8]. An Edwards 306 evaporator was used for the deposition. Following lift-off and cleaning, the substrates were loaded into an alloying rig. After introducing forming gas to the alloying chamber, the temperature was raised to 400°C for 2 minutes, then allowed to fall back to room temperature.

4.7.2 Anode via-hole etching

As with the ohmic contact areas, the anode vias were formed using a wet-etch through patterned photoresist. S1813 resist was used (4500rpm, 30s) to translate the anode array pattern onto the substrate. Owing to the small dimensions of these patterns additional steps had to be taken in the lithography to allow accurate formation of the etched via holes. Adhesion promoter was spun onto the substrates (4500rpm, 30s) before applying the S1813 to prevent the HF wet-etch from creeping along the SiO_2/resist interface. The S1813 was baked following spinning at 80°C for 120s. Exposure duration on the Karl Suss MJB3 was 8s (adjustments were made for older bulbs) and complete development in 3.5:1 H_2O:Microposit 351 took 12s. A post development oven bake (90°C, 1 hour) was then employed and this significantly reduced undercut during the HF etching stage.

The via holes were etched in buffered HF for between 80 and 100s. Whilst the first stages of etching could be monitored by observing colour changes in the SiO_2 layer, as etching neared completion, it became impossible to visually verify complete removal of the SiO_2 from vias with 2-3µm diameters. In order to ensure a surface devoid of SiO_2, the holes were over-etched and a small degree of undercut was sought. The substrates were submerged in buffered HF for 60s and then inspected. Repeat cycles of 10s submersion followed by inspection were carried out, until undercut was just visible around the perimeter of each anode via. Before employing this method and actively aiming for undercut, electroplating anodes proved inconsistent and some evaporated anodes measured open circuit.

Before electroplating or evaporating to form Schottky diodes in the via holes, an etch in 1:1 HCL:H_2O was required in order to remove the surface oxide. The substrate was submerged in the oxide etch for 1-minute at room temperature.

4.7.3 Electroplating platinum anodes

The three solutions that were available for use in this project were Engelhard GP-4g/L, Engelhard GP-10g/L and Platanex low stress plating solution. Most of the developmental work was performed using the Engelhard GP-4g/L solution, as this was the only solution available at the start of the project. This solution has 4g/Litre platinum content, the optimum DC plating current density is 0.65A/dm^2 and the optimum plating temperature is 45°C. The manufacturer provides these figures with large-scale applications in mind, such as plating jewellery, nevertheless they have proved to be a useful benchmark. The diode arrays featured in this project have a total area that, according to the manufacturer's recommendation, would require an electroplating current of 300nA. Arrays were plated in this way and devices with idealities 1.4-1.5 were routinely produced. In order to improve on this, an alternative to DC plating was adopted.

Pulse electroplating methods have been reported [9, 10, 11] with high quality Schottky anodes resulting. The Keithley 220 constant current source used for plating offered constant pulse operation and this method was adopted following observations on larger anode/contact post plating experiments. In these trials, constant current was supplied to a small area with no external agitation (conditions consistent with the drop plating method). Using an electrometer the voltage between the anode and cathode was observed to steadily rise under the constant current conditions. Visible bubbling would often occur and an open circuit was a typical result when plating contacting posts through thick resist.

Pulse plating allows higher current densities for electroplating anodes and contact posts. The latter is particularly evident when fabricating whisker posts with very small base areas [3] where the recommended DC current is comparable with the expected noise pick-up on the source/measurement cables. Using pulse plating, platinum whiskers were successfully plated with current values increased by a factor of 100 over the manufacturer's recommendation. A discussion relating device

characteristics to plating current density is included in section 5.1. Chapter five also contains measured results from diodes formed using evaporated and electroplated metal. Electroplated diodes were formed using three different plating solutions with a variety of pre- and post-plating treatments, details of which may be found in section 5.1. Optical photographs of arrayed electroplated diodes (diameter 3μm) are shown in figs. 4.21 and 4.22.

4.7.4 Evaporated anodes

As an alternative to electroplating, anodes were also formed using thermal evaporation. It was not possible to evaporate platinum, so palladium was selected and anodes were evaporated with a Ti/Pd./Au structure [12].

An inherent problem with evaporation involves oxide formation on the exposed GaAs. Immersion in 1:1 HCL:H_2O was employed before electroplating diodes to remove surface oxide from the open GaAs and was similarly employed prior to all evaporations. However, when loading the samples into an evaporator, significant time elapses during which the GaAs Schottky interface areas are exposed to air. This leads to formation of a thin oxide layer and hence affects device performance. Despite this known problem, evaporated anodes were produced and measured. The time taken to load the substrates after the oxide etch and rinsing/drying stages was minimised in an effort to reduce oxide growth on the interface areas. Results from these experiments are discussed in section 5.1.
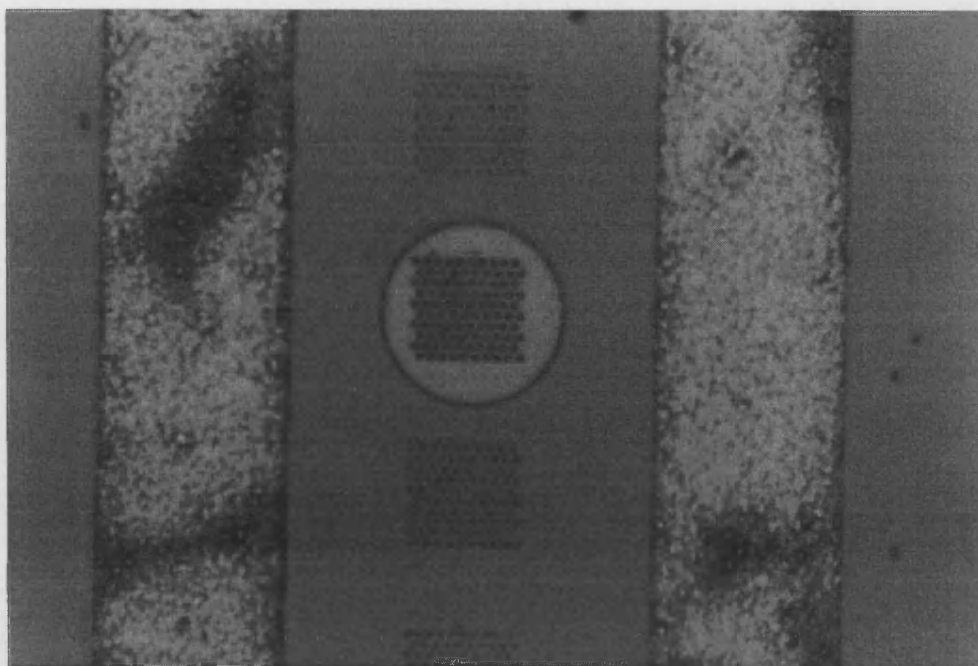
Figure 4.21. Electroplated Pt Schottky anodes, ohmic ring and SU8 isolation layer.
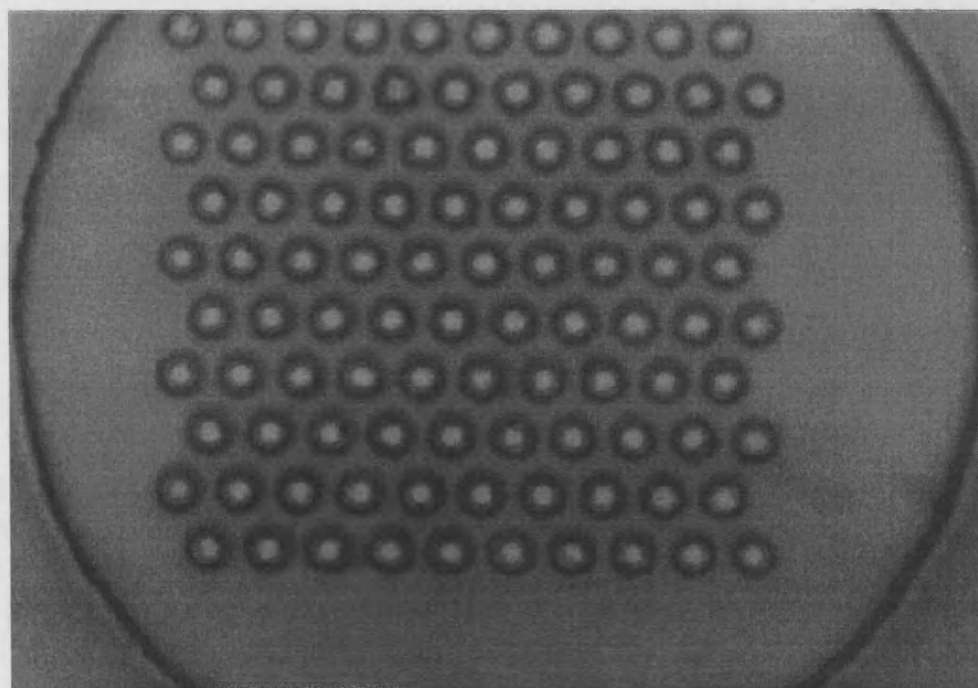
Figure 4.22. Surrounding SU8 layer and array of 3µm diameter electroplated Pt anodes.

4.8   Electron beam lithography

In house electron beam lithography was achieved using a Jeol JSM-35C scanning electron microscope running with NPGS software. Using this apparatus allowed the anode spacing and diameter to be modified and optimised for latter processing, without committing the patterns to a mask. The writing parameters, developed for use with PMMA electron beam resist, are summarised below. Arrays of 2μm and 3μm dots were successfully written using the settings below (figs. 4.23, 4.24).

PMMA layer: The substrate is cleaned and baked prior to application of the PMMA resist. A 30s, 2500rpm spin was used to produce a 0.5μm film of PMMA. The sample was then baked for 30mins in an oven at 165°C.

Writing procedure: To optimise the electron beam prior to writing, a feature near the intended writing area was viewed at high magnification (at least 8000x) and focus and astigmatism were corrected. Before writing, slow scan mode was selected and the brightness control was reduced to zero. Magnification was selected to correspond to the 'max-mag.' reported by the NPGS software and the scan switched from SEM to NPGS. The contrast control was used to indicate the beam strength. If a spot was just visible on the screen at a contrast setting of 6:00, it was found that the beam strength allowed reliable writing. Table 4.6 lists the key input parameter values required by the NPGS software.

Dose	Measured beam current	Line spacing	Centre-centre spacing	Magnification	Coarse beam current
70μC/cm^2	4.0pA	305Å	305Å	1000-1300	6.0pA

Table 4.6. Electron beam writing parameters in NPGS.

Development: Developer was 3:1 IPA:MiBK. Development typically took 1-1.5 minutes. In practice, samples were inspected under a microscope at 10-second intervals after the first 40 seconds of development. Unexposed PMMA showed high

resistance to developer and 10-second accuracy was more than sufficient to avoid damage to unexposed areas.
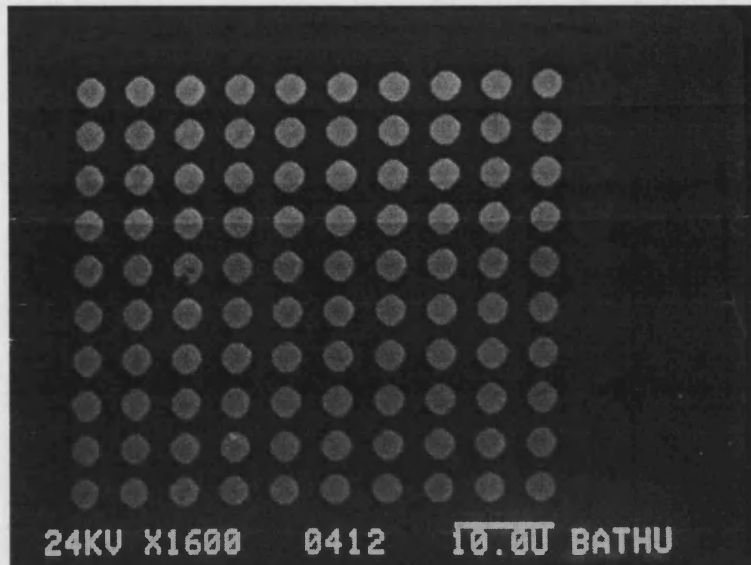
Figure 4.23. Evaporated Ti/Pd/Au Schottky anode array
Formed using electron beam lithography.
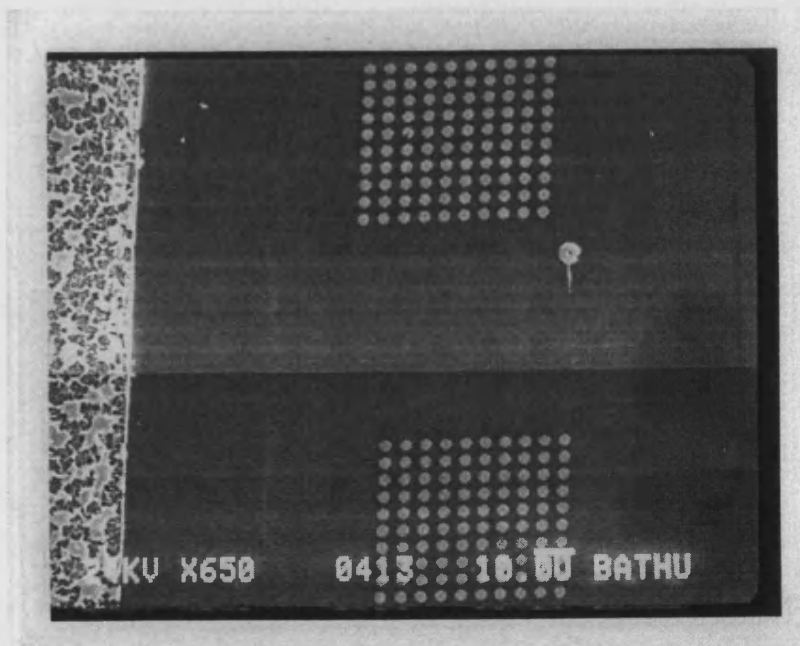
Figure 4.24. Electron beam written anode arrays and ohmic contact.

4.8.1 Conclusions drawn from electron beam lithography

Electron beam lithography was utilised in developing the tripler processing scheme and combining the whisker method with pre-formed anodes. The ability to rapidly change anode spacing and assess the likelihood of successful whisker contact was valuable to the progress of the project.

Patterning the anodes using E-beam written PMMA was eventually aborted in favour of conventional lithography. This was partly due to the time taken to process each substrate when E-beam writing, but was also prompted by difficulties experienced when etching the anode vias. Problems with undercut had been encountered when etching SiO_2 through conventional resist, but these were solved with adhesion promoter and a post development bake (section 4.8.2). A reliable solution was not found for samples with holes opened in PMMA. Buffered HF repeatedly acted along the $PMMA/SiO_2$ interface and produced undercut that was often too severe to allow satisfactory processing of the vias (fig. 4.25). In a bid to avoid HF etching, a scheme was devised that used the spun and patterned PMMA alone as a passivating layer for the whisker/anode processing. This ultimately failed as PMMA lacked sufficient resistance to the Engelhard plating solutions.

An application requiring sub-micron anodes would require E-beam writing and in this case an alternative plating solution such as Platanex may offer a solution. This was not a requirement for this project and 2-3μm features were readily achievable in S1813 using an optical mask plate.
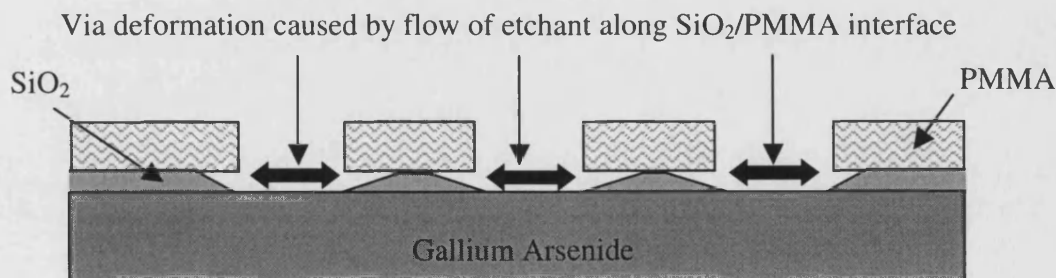
Figure 4.25. Profile of silicon dioxide vias following wet-etching (using buffered hydrofluoric acid) through patterned PMMA.

4.9   Introduction to fabrication schemes

The remainder of this chapter is devoted to the fabrication schemes that were developed for the active and passive sub-millimetre wave components featured in this thesis. The schemes are mainly presented as side cross-sectional views. This convention was chosen in order to show the successive layers required in forming the component, from the substrate level upwards. Where clarification may be required, additional views have been included.

Concise notes describing the steps performed in reaching the sequence of illustrated stages accompany each processing diagram. For planar stages including anode formation, complete processing details can be found in the preceding sections of this chapter. Similarly, for full details on the MEMS thick resist techniques used in all of the following fabrication schemes, the reader should refer to sections within this chapter concerning conventional resist and SU8 processing. Notes provided with each fabrication sequence outline the required techniques with minimal repetition of the detail provided thus far.

Fabrication sequences for an integrated tripler, doubler and detector are presented first and these share similar planar processing steps for anode and ground plane formation. The main differences encountered in these schemes are due to the topology of the circuit. The tripler utilises SU8 for the waveguide circuit whilst the detector and doubler structures have waveguides formed using conventional Hoechst AZ series resist. The tripler and doubler schemes have anode arrays that are fabricated prior to formation of the contact post, whilst the detector is based on a sub-micron contact formed at the interface of the contact post and the GaAs substrate.

Passive component designs follow those based around Schottky devices. Processing schemes are included for tuning structures, inductive iris filters and E-plane septa filters. These schemes are generally simpler, with no requirement for planar device arrays or electroplated diode contact structures. Difficulties faced with these designs usually arose due to the thick resist layers involved. The importance of a highly collimated UV beam has already been discussed (section 4.1.2) and care had to be taken to minimise abrupt temperature changes when processing ultra-thick SU8

layers. All component fabrication schemes are accompanied with supporting photographs. A discussion of the merits and difficulties associated with the formation of each component is included in chapter five.

4.10 Processing scheme for integrated frequency tripler

1. After definition and formation of ohmic regions, a silicon dioxide layer (0.2μm thick) was sputtered onto the substrate.

2. S1813 resist was spun and exposed to leave an array of holes over the SiO_2 and within the ohmic ring. Wet-etching in buffered HF transferred the array into the SiO_2 and revealed the underlying GaAs. The anodes were then electroplated.

3. The S1813 layer was dissolved in acetone and SU8-5 was spun to form a 2μm thick insulating layer. This was exposed and developed to leave the anode region clear.

4. The substrate was then spun with resist, before an evaporation/lift-off stage was used to produce a gold ground plane.

5. A thin layer of AZ4562 was used to mask the diode array region. Nickel was then electroplated until a level surface was formed with the SU8 struts. For clarity in this and the following diagrams, the anode array and passivation layers are not shown.
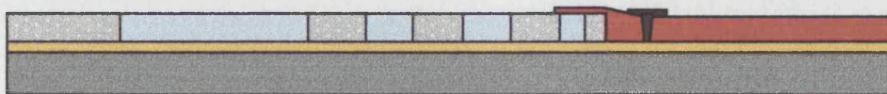
6. AZ4562 was spun at 1200rpm and the electroplated whisker process was performed.

7. AZ4562 was exposed and developed away from the SU8/nickel surface and gold was evaporated (thickness 500nm). SU8-5 was spun and baked to form a 3μm thick layer.
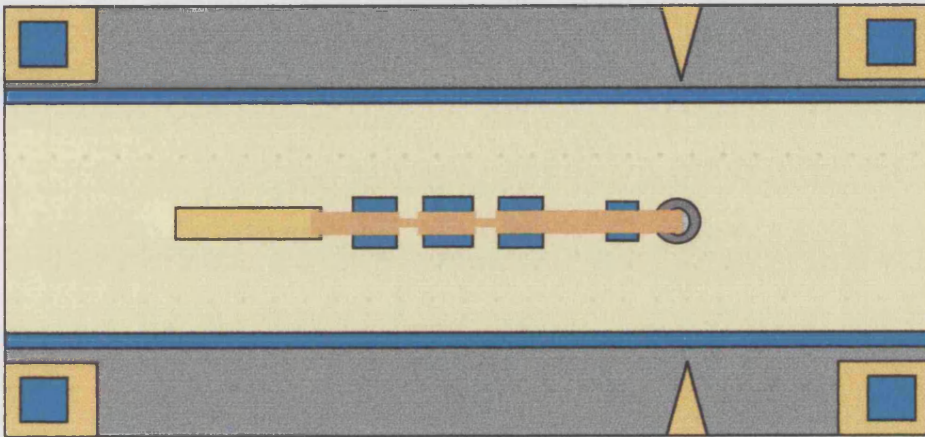
8. The SU8-5 layer was patterned to form the low-pass stripline and this shape is translated into the gold layer via wet etching. The nickel layer can then be etched away and the AZ4562 dissolved in acetone. A final evaporation is used to form the ridge/stripline transition.
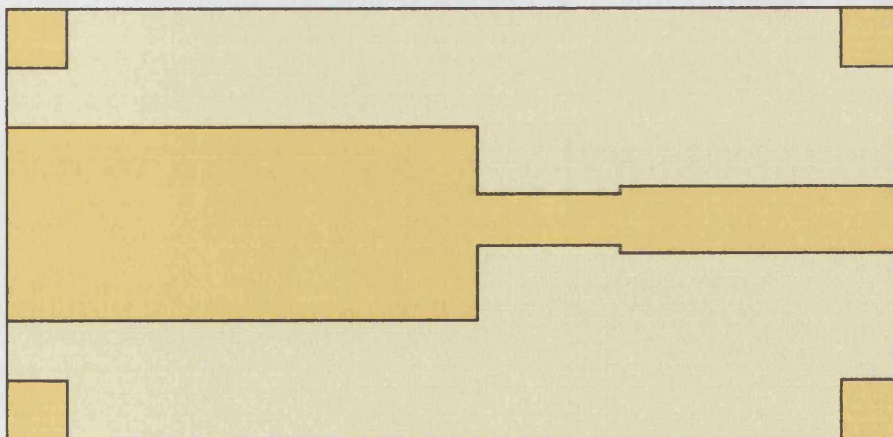
9. A separate silicon substrate was spun with SU8-50 and lapped to form a 100μm thick SU8 layer. This was then patterned and evaporated with gold from multiple angles to form the waveguide lid.
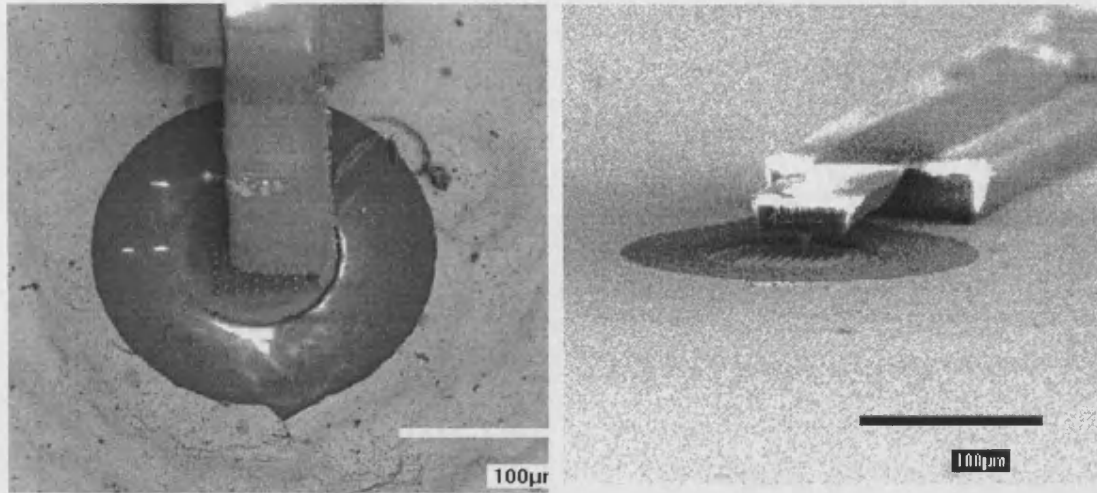
Figure 4.26. Stripline to diode array via electroplated post (figure shows solid dielectric layer rather than air-bridged structure, see section 5.1 for discussion).
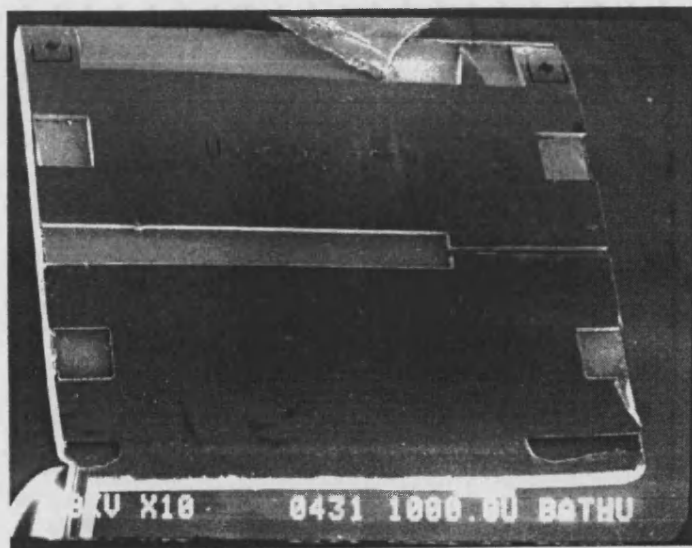
Figure 4.27. Tripler cavity formed in SU8.

4.11 Processing scheme for integrated frequency doubler

1-3. Processing for the first three stages of the integrated doubler followed the same scheme as used for the tripler (section 4.10).

4. A 25µm thick layer of AZ4562 was spun onto the substrate.

5. The whisker method was performed (section 4.5).

6. A second positive resist layer (AZ4533) was added by pipette to form a total layer thickness of 100µm. This layer was ramp baked (section 4.2) and a hole was exposed and developed in the resist above the plated pin.
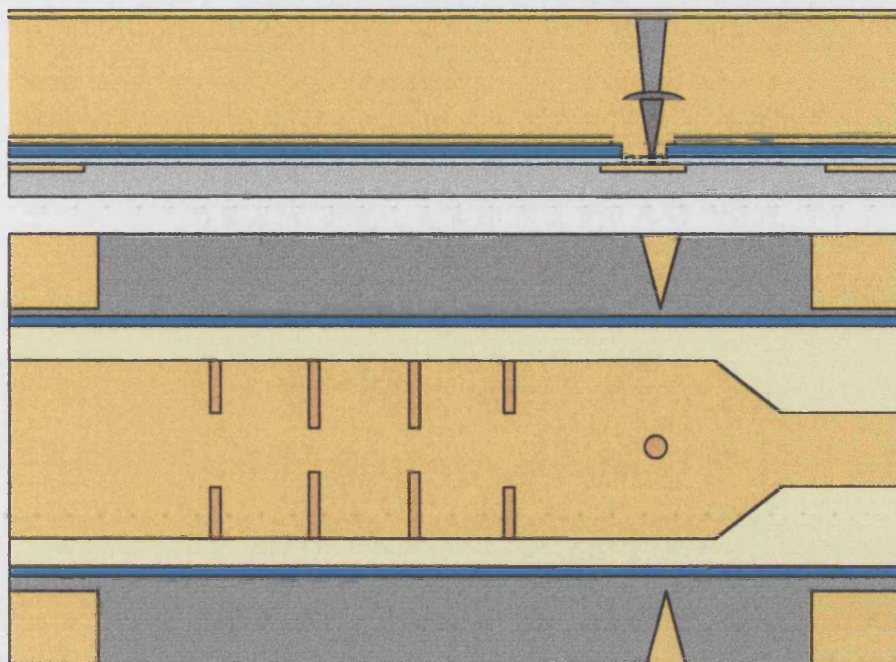
7. A second electroplated pin was formed and the resist layer was imaged with the desired former pattern. After development, gold was sputtered to form a seed layer and the waveguide was plated. Finally, the combined AZ4533 and AZ4562 layers were dissolved in acetone.
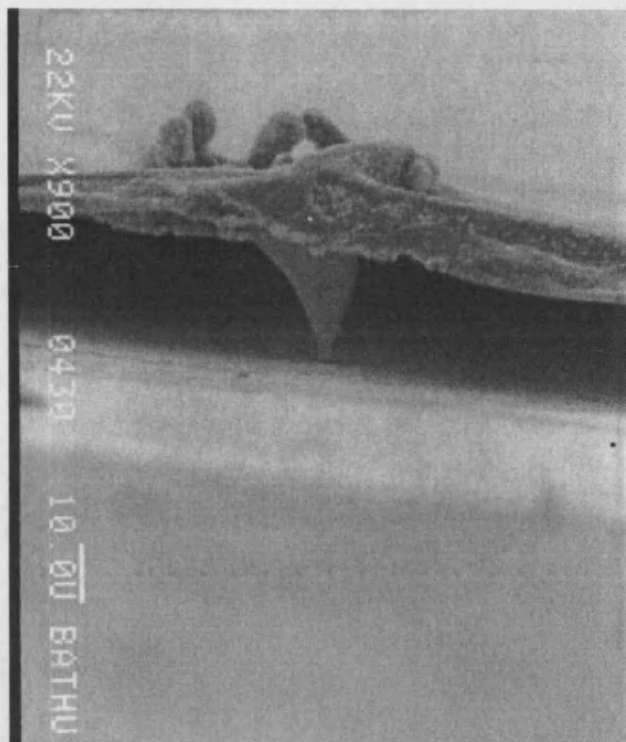
Figure 4.28. Electroplated whisker supported by a cut-away electroplated waveguide.

Figure 4.29. AZ4533 photoresist former (thickness 200μm) for frequency doubler with activation layer (sputtered gold) for electroless plating (see Appendix 3).

4.12   Detector fabrication
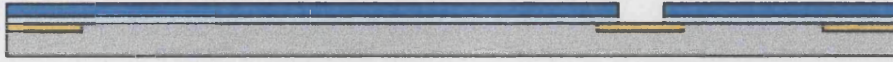
1.   For sub-micron contacts, the SiO$_2$ layer was etched to form a window 50µm in diameter onto the GaAs. SU8-5 was spun and imaged to form the secondary passivation layer. Once more, processing is similar to that used for the tripler base (section 4.11)

2.   The whisker method was performed using 25µm wire etched to form a sub-micron tip (section 4.5). Following plating, the sample underwent an overnight bake at 50°C.

3.   Gold was evaporated through a shadow mask to form a gold covered waveguide and horn.
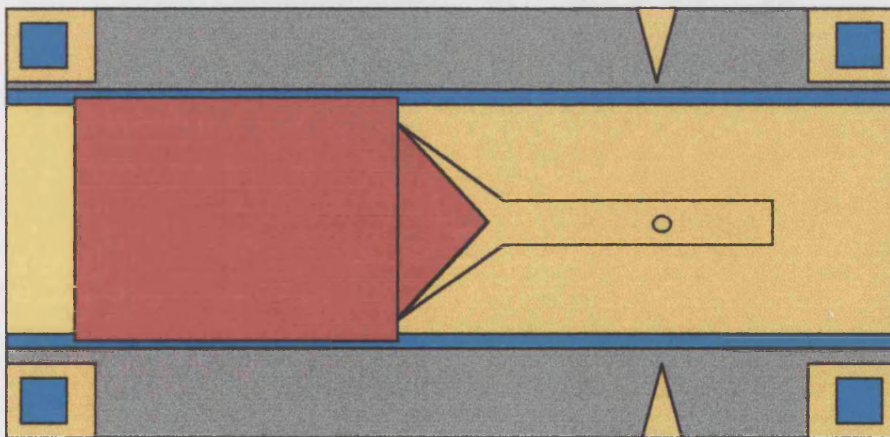
4.   AZ4533 was spun (4500rpm, 30s) and allowed to dry for 3hours in a 50°C oven. This resist was patterned to prevent plating occurring in the cut-away of the horn.

5.   Following gold plating, the resist was removed and replaced with a second layer of AZ4533 which was exposed and developed to leave a window over the cut-away section. A gold wet-etch then removed the evaporated seed layer and the remaining photoresist was removed in acetone.
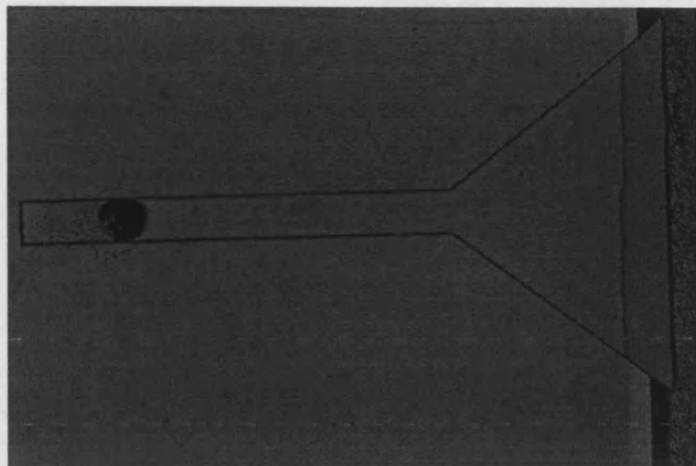
Figure 4.30. Optical photograph showing evaporated gold layer on former. (The photoresist around the whisker forms a slight mound causing a dark area in the photograph).
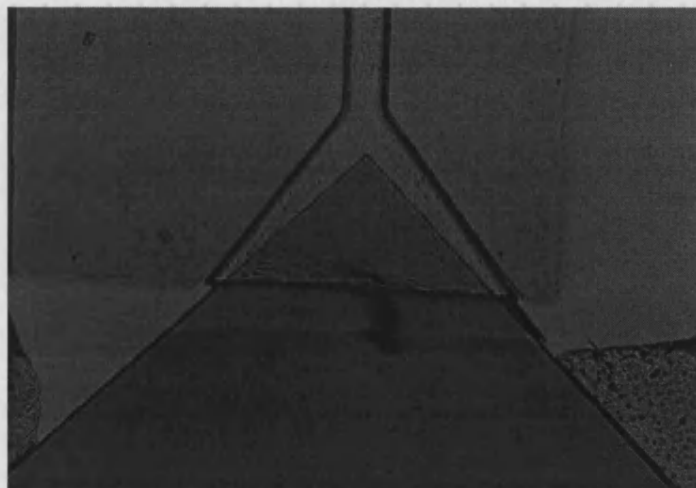
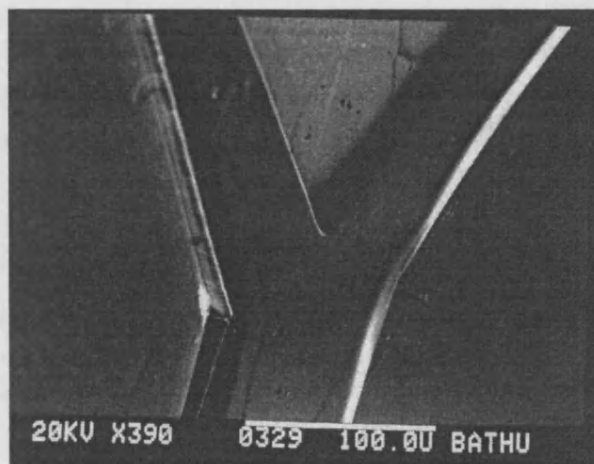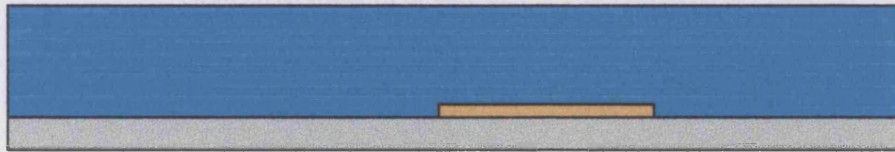Figure 4.31. Resist patterned in order to form cut-away, prior to plating.

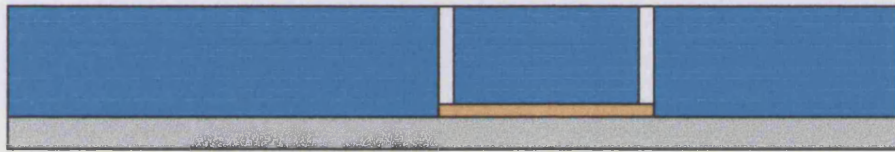Figure 4.32. SEM micrograph illustrating cut-away horn.

4.13   Processing scheme for tuning stubs

1.   A seed layer was evaporated then plated (copper or nickel) and resist was spun and patterned to form the required etch pads.

2.   A wet-etch was performed and the resist dissolved.   SU8 was then applied, baked and lapped to form a flat layer of the desired thickness.

3.   The SU8 was exposed and developed to leave the tuning component isolated and attached only via the release layer.
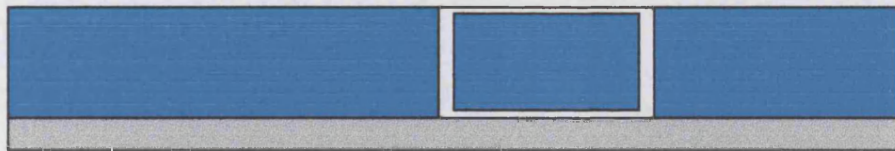
4.   The release layer was then etched away leaving the SU8 component free to move.
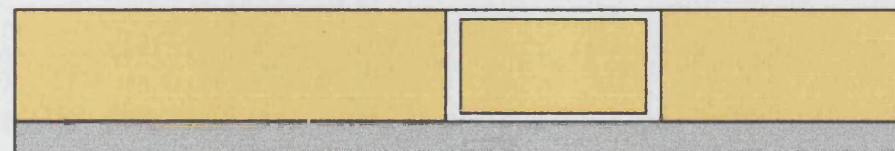
5.   The completed structure was then metallised (see Appendix 3).   Released components were removed and coated separately.
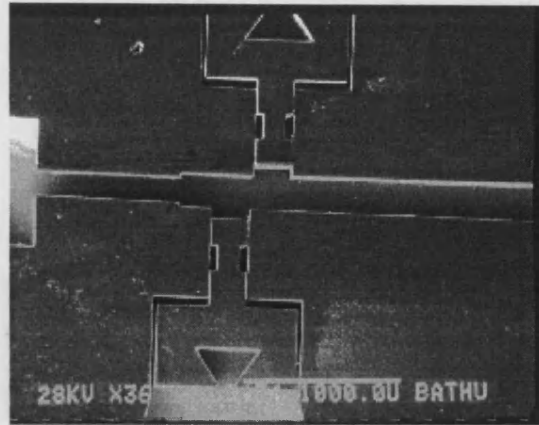
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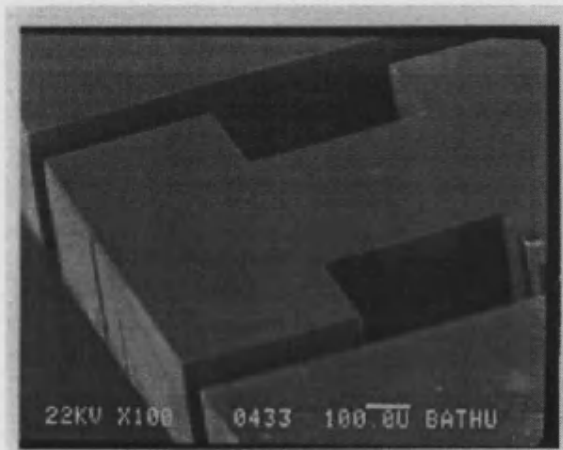Figure 4.33. Tuners on output waveguide of SU8 tripler lid.

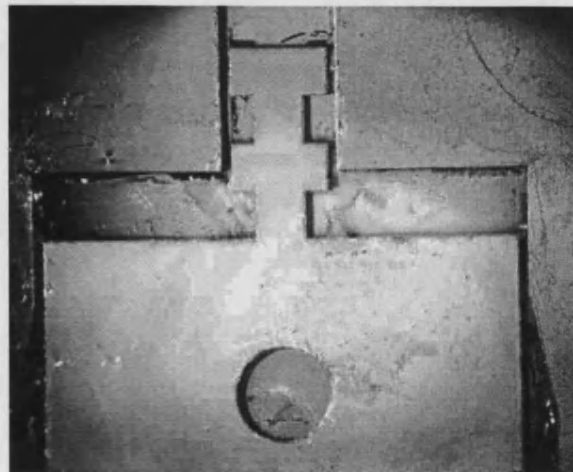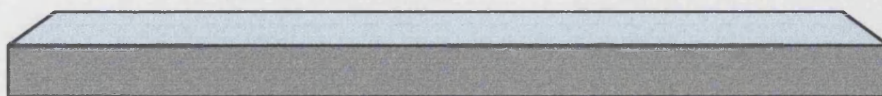Figure 4.34. SU8 tuning stub, height 400µm, guide width 800µm.
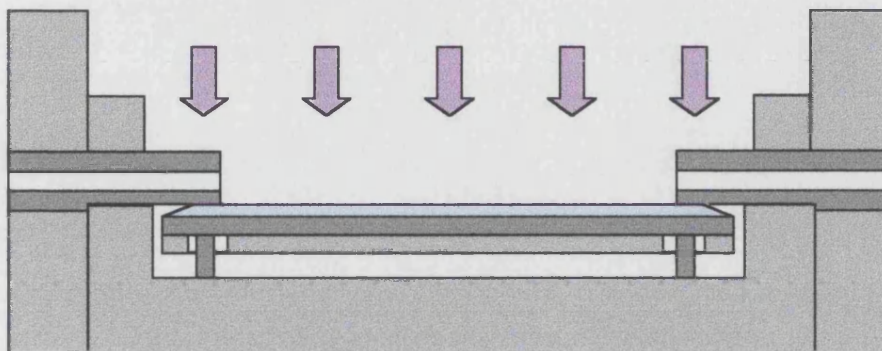

Figure 4.35. Moving SU8 tuning stub after release etch (optical photograph).

4.14   135GHz inductive iris coupled bandpass filter

1.   SU8-500 was applied, baked and lapped to a thickness of 400µm. The substrates used were ceramic and 15 x 12 x 1mm in size.


2.   The substrate was placed into the RF test mount (Appendix 2) and the SU8 layer was UV exposed under the mask aligner.

3.   Following a post-exposure bake (PEB), the SU8 layer was developed and sputter coated with a 500nm thick layer of gold.
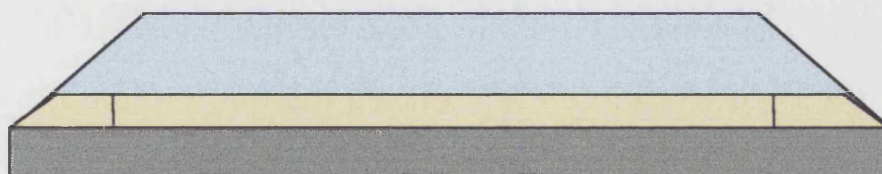
4.   A second layer of SU8-500 was applied and ramp baked (room temperature to 105°C in one hour, 110°C held for eight hours, ramp down at 30°C/hour). The target thickness was 800µm after lapping.
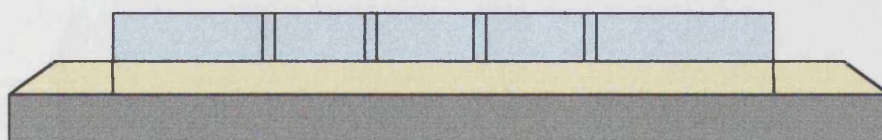
5.   Lapping produced a layer of the required thickness and eradicated the domed profile naturally adopted by the baked SU8. Exposure under a conventional mask translated the desired pattern into the SU8.
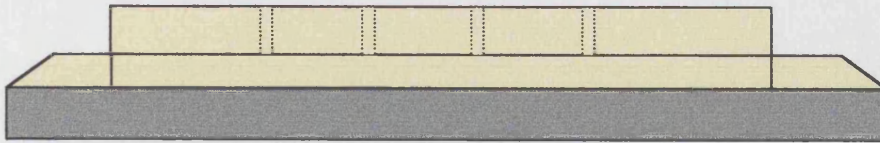
6.   The waveguide trench and inductive irises were metallised either by multi-angle sputtering or by the electrodag/metallisa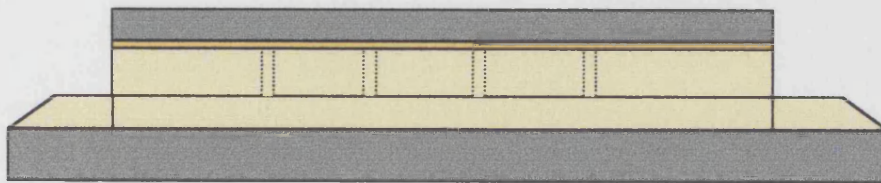tion procedure described in Appendix 3. The trench was then filled with a water-soluble paste, lapped so as to be level with the top surface of the waveguide trench.

7.   Evaporated gold formed the waveguide roof. The roof was strengthened using a bonded lid and the paste inside the waveguide was dissolved in warm water (60°C, approximately 12-hours).
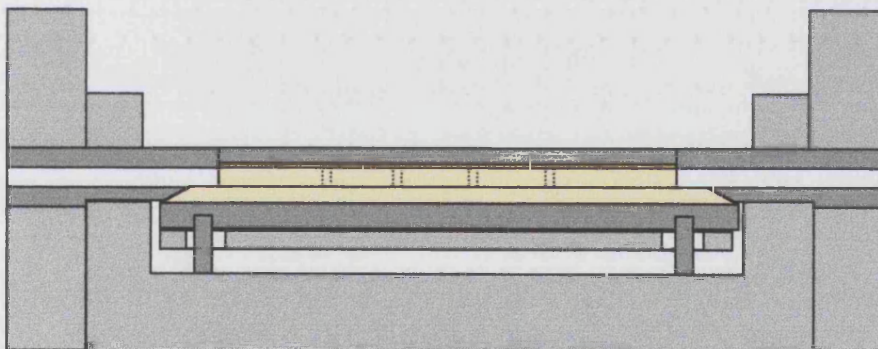
8.   The completed filter was then located within the RF test mount and eventually coupled to sources/power heads using the conventional waveguide flanges attached to the mount.

Figure 4.36. 135GHz bandpass filter (lid off) coated in nickel (multiple evaporations)
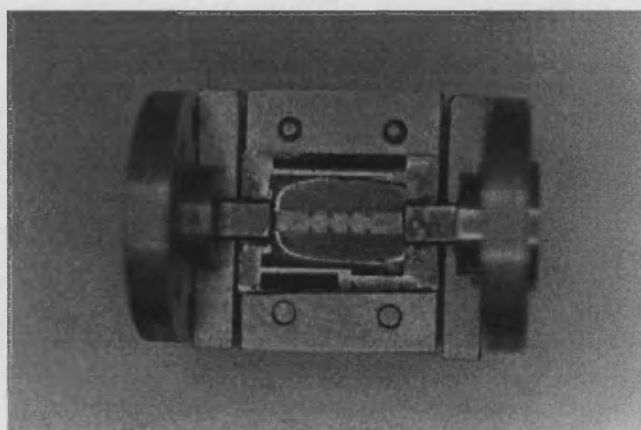
Figure 4.37. 135GHz filter electroplated with nickel and located in test mount.
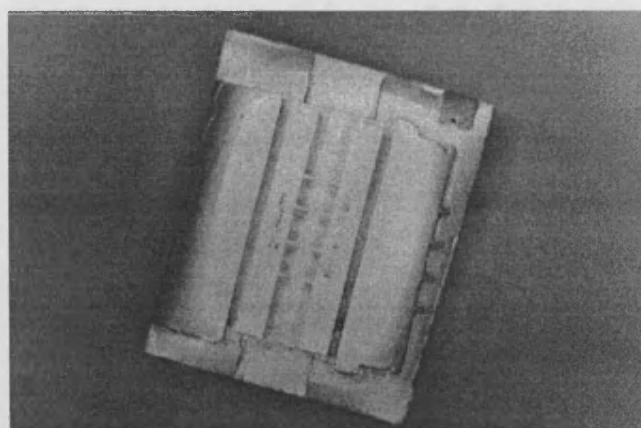
Figure 4.38. 135GHz filter with seed layer for electroless plating provided by airbrushed Electrodag 1415.

4.15   Fabrication sequence for E-plane septa components
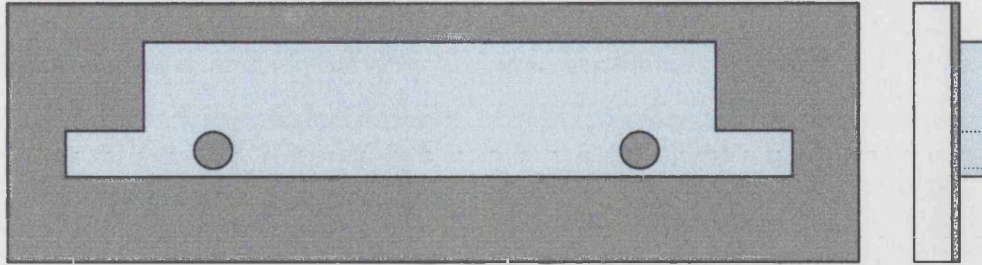
1.   SU8-100 was applied to a sacrificial substrate and lapped to a thickness of 600µm. This layer was patterned to form a single side-wall of the waveguide/block.
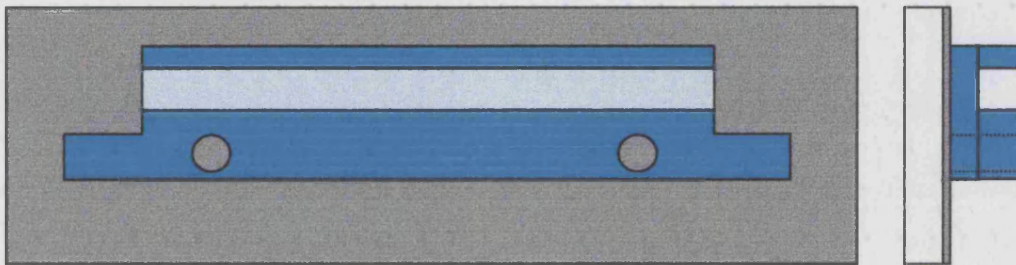
2.   SU8-100 was once again applied and lapped, this time to a thickness of 1400µm (600 + 800µm). The SU8 was patterned to form a cavity with a depth equal to half the width of the final waveguide.
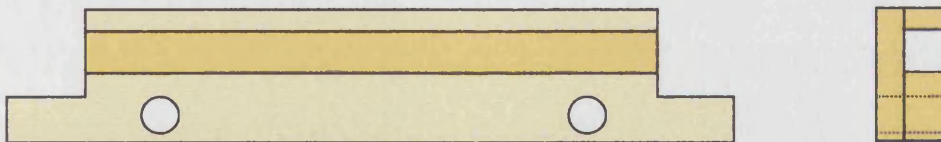
3.   After the SU8 component was released via ferric chloride etching of the nickel-plated substrate, Electrodag was airbrushed as a seed layer and electroless plating was performed (Appendix 3).
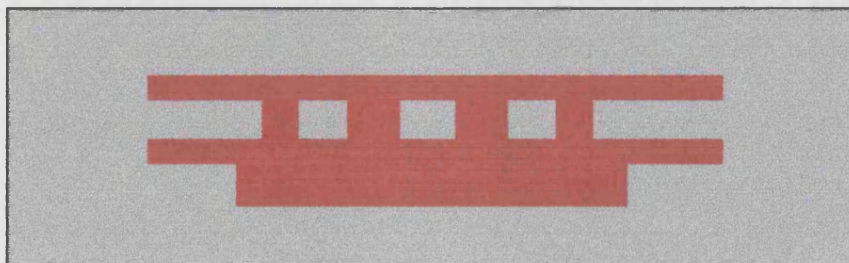
4.   Separately, foil was flattened and bonded onto a sacrificial substrate using SU8-5. AZ4533 was then spun onto the foil and imaged to form the septa pattern.

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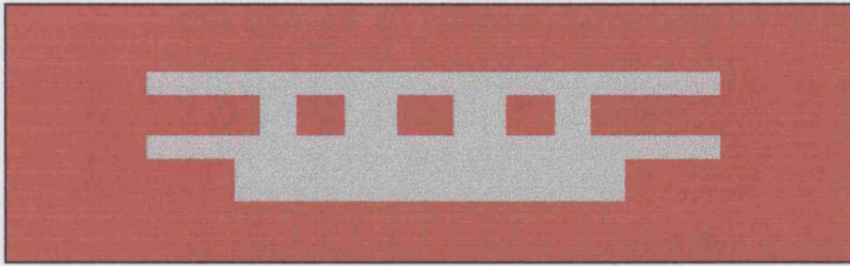
5. Using 4:1 H$_2$O:HCL, the aluminium was etched to leave the patterned foil on the sacrificial substrate. The SU8-5 was then dissolved in EC solvent to release the septa component.
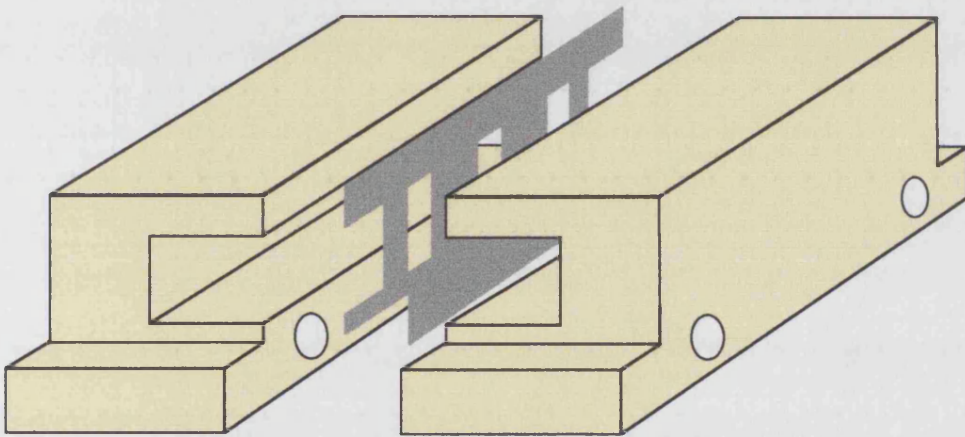
6. The first three steps of the scheme were repeated to produce a second waveguide half-section. Aligning pins (1.5mm diameter) used in conjunction with location holes in the waveguide cavity sections, provided accurate registration of the three components. The external seam was permanently joined using epoxy.

Figure 4.39. All SU8, half waveguide block with M1.6 tapped assembly holes.

Figure 4.40. Septa foil prior to release from AZ4533 spun onto glass cover slip.
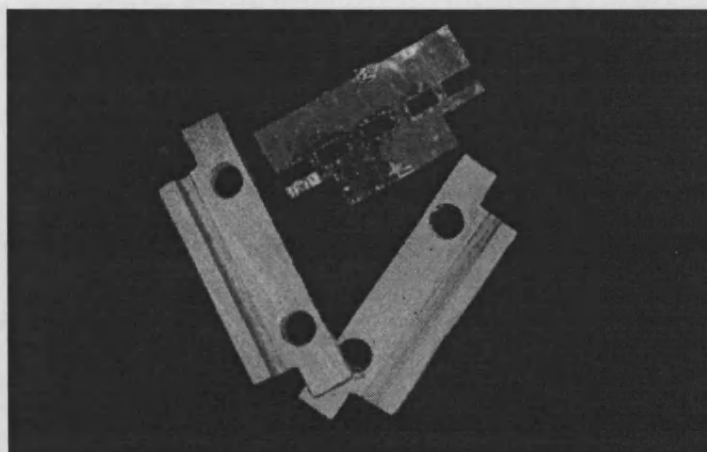
Figure 4.41. Gold plated E-plane septa filter block.

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[11]   M. Lopez-Coronado, M. Aguilar, M. T. Martinez, E. Calleja, and E. Munoz, "Electroplated Au-GaAs$_{1-x}$P$_x$ and Au-Ga$_{1-x}$Al$_x$As Schottky barriers", Electronics Letters, vol.19, no.17, pp.666-8, August 1983.

[12]   N. J. Keen, "Low-noise millimetre-wave mixer diodes: results and evaluation of a test program", Proceedings of IEE, Vol. 127, Pt. 1, No. 4, pp. 188-198, August 1980.

5. Results

This chapter contains results from DC tests carried out on electroplated and thermally evaporated Schottky diodes. RF results (D-band transmission measurements) are included for resonator filters and straight waveguide sections fabricated in SU8. Comparison is made with transmission achieved for a conventional copper waveguide section inserted into the purpose-built test mount [Appendix 2]. Details of the measurement apparatus are provided and limitations and sources of inaccuracy are discussed.

In addition to numerical results, this chapter includes information gathered visually and via mechanical tests. SU8 component quality is discussed both in terms of the imaged film and the metal coating required in order for these components to function as waveguiding structures. Finally, a discussion concerning the fabrication of the stripline filter (see sections 3.8 and 4.10) and its application to the frequency tripler design is included.

5.1 Diode processing and characteristics

For arrayed diodes, the fabrication process followed that described in section 2.5 and reference [1]. The anodes were formed using optical lithography and due to the absence of a Reactive Ion Etching (RIE) system the passivation layer (SiO_2) was etched all the way through to the underlying GaAs using buffered Hydrofluoric acid. 2-3µm diameter anodes were routinely formed with no significant difficulties encountered.

Efficient multiplier circuits rely on devices with near-unity ideality factors, low series resistance and high reverse breakdown voltages. With this in mind, an investigation into the optimum conditions for electroplated and thermally evaporated diodes was undertaken. The critical process parameters and results from this practical study are shown in tables 5.1, 5.2 and 5.3.

The data created from the electroplated diode runs can be split according to the platinum plating solution employed for each batch. For historical reasons, Engelhard

GP (4g/L platinum) was employed first. As with all the other solutions used, the first trial was designed to follow the procedure recommended by the manufacturer. The results for diode A1 show the quality achieved using the current density, temperature and agitation conditions stipulated in the data sheet accompanying the solution.

Drop electroplating was employed during this project (section 4.6) and data for this procedure using Engelhard GP 4g/L solution is labelled 'B1'. Pulse plating methods similar to those reported by Burrus [2] were used to create diode batches A2 (tank electroplated) and B2 (drop electroplated). The current densities listed for these diodes were arrived upon experimentally and for the sake of brevity, characteristics from all preceding pulse plated batches have not been included. Burrus stated that the optimum current density for pulse plating methods was far higher than that for DC plating. This was certainly corroborated for both the Engelhard and Platanex plating solutions.

Following the work described in papers by Pham et al. [3, 4] and Sinha et al. [5, 6], high temperature annealing was performed on diode batches formed with all plating solutions. In table 5.2 'E1' (DC, drop-plated) and 'E2' (pulsed, drop-plated) show the change in characteristics caused to batch B1 and B2 following annealing at 300°C for 10-minutes in forming gas (10% hydrogen, 90% nitrogen). The temperature and duration were extended for 'H1' and 'H2', which show the B1/B2 diodes following a further 10-minute anneal stage at 400°C.

The routine described above was repeated using standard Platanex IBD platinum solution. Diode batches C1 (DC plated) and C2 (pulse plated) were formed and subjected to anneal stages of temperature 300°C (duration 10-minutes) then 400°C (duration 10-minutes). Drop electroplating was not practical with this solution due to its temperature requirements and fast evaporation/crystallisation rate. An important consideration with this solution is its fast GaAs etch rate. It was found necessary to immerse the sample with the electroplating potential already applied in order to avoid removing an excessive amount of the n-epilayer.

'Low-stress' Platanex (Appendix 3) is a widely used alternative to the conventional mix. This is composed of R-unit and Sulphamic acid only (no B-unit) and provides

lower stress in the electroplated platinum deposit. Results from runs based on this solution are shown in table 5.2 with titles D2, G2 and K2. DC plating produced poor quality anodes with this solution and the results are not reproduced here. Pulse plating proved much more successful and the mechanical behaviour of the anodes after annealing supported the claimed low-stress characteristic.

Diode	Description
A1	1:1 HCL:H_2O pre-treatment, tank electroplated (moderate agitation), Engelhard 4g/L, 0.65A/dm^2 (DC), 50°C, duration 15minutes.
A2	1:1 HCL:H_2O pre-treatment, tank electroplated (moderate agitation), Engelhard 4g/L, pulse plated at 5.0A/dm^2 (duty cycle 10mS ON, 20mS OFF), 50°C, duration 15minutes.
B1	Drop electroplated platinum (no agitation), otherwise as A1.
B2	Drop electroplated platinum (no agitation), otherwise as A2.
C1	1:1 HCL:H_2O pre-treatment, tank electroplated (moderate agitation), Platanex IBD solution used at 80°C (2.0A/dm^2 DC, duration 10minutes).
C2	As C1, but pulse plated at 20.0A/dm^2 (duty cycle 10mS ON, 20mS OFF).
D2	Low-stress Platanex used at 60°C. Current density 20.0A/dm^2 (duty cycle 10mS ON, 20mS OFF). Pre-treatment, agitation and duration as C1.
E1/E2	B1/B2 annealed at 300°C in 90% nitrogen/10% hydrogen for 10 minutes.
F1/F2	C1/C2 annealed at 300°C in 90% nitrogen/10% hydrogen for 10 minutes.
G2	D2 annealed at 300°C in 90% nitrogen/10% hydrogen for 10 minutes.
H1/H2	E1/E2 annealed at 400°C in 90% nitrogen/10% hydrogen for 10 minutes.
J1/J2	F1/F2 annealed at 400°C in 90% nitrogen/10% hydrogen for 10 minutes.
K2	G2 annealed at 400°C in 90% nitrogen/10% hydrogen for 10 minutes.
L	1:1 HCL:H_2O pre-treatment, Ti/Pd/Au evaporated – 7nm Ti/ 18nm Pd/ 200nm Au.
M	1:1 HCL:H_2O pre-treatment, Ti/Pd/Au evaporated – 10nm Ti/ 20nm Pd/ 200nm Au.
N	L annealed at 300°C in 90% nitrogen/10% hydrogen for 10 minutes.
O	M annealed at 300°C in 90% nitrogen/10% hydrogen for 10 minutes.

Table 5.1. Diode fabrication conditions for devices listed in Table 5.2.

Finally, evaporated diodes were formed using a Titanium/Palladium/Gold layer structure reported by Keen [7] and annealing stages were performed on these diodes. The data for these diodes is included in Table 5.2 as L, M, N and O.

Diode	Diameter (μm)	Material	Ideality factor	Zero bias capacitance (fF)	Series resistance* (Ω)	Reverse breakdown voltage (V)
A1	5	NU1541	1.73	15	21.3	-10.3
A2	5	NU1541	1.25	16	23.6	-10.0
B1	5	NU1541	1.59	16	24.7	-9.98
B2	5	NU1541	1.41	15	11.2	-9.83
C1	5	NU1541	1.56	14	24.7	-8.94
C2	5	NU1541	1.18	17	84.2	-9.77
D2	5	NU1541	1.20	15	53.9	-9.10
E1	5	NU1541	1.13	14	43.8	-9.65
E2	5	NU1541	1.08	16	24.7	-6.71
F1	5	NU1541	1.18	16	57.2	-9.68
F2	5	NU1541	1.15	13	35.9	-9.86
G2	5	NU1541	1.07	17	92.0	-9.60
H1	5	NU1541	1.11	17	46.0	-9.67
H2	5	NU1541	1.07	16	28.1	-7.20
J1	5	NU1541	1.20	13	42.6	-9.70
J2	5	NU1541	1.14	17	19.1	-9.85
K2	5	NU1541	1.07	16	26.9	-7.40
L	5	NU1541	1.23	14	58.4	-5.90
M	5	NU1541	1.22	14	37.0	-6.83
N	5	NU1541	1.41	15	19.1	-5.16
O	5	NU1541	1.39	16	21.3	-5.52

* The series resistance value includes contribution from whisker probe contact.

Table 5.2. Measured diode characteristics for devices fabricated according to the conditions listed in Table 5.1.

Diode Batch	Diameter (μm)	Material	Ideality factor	Zero bias capacitance (fF)	Series resistance (Ω)	Reverse breakdown voltage (V)
E2	3	NU1541	1.10	6	24.0	-9.92
E2	5	NU1541	1.08	16	24.7	-6.71
E2	10	NU1541	1.09	75	17.2	-9.65
E2	25	NU1541	1.13	360	13.2	-9.67
E2	50	NU1541	1.10	1500	15.3	-9.83

Table 5.3. Diode characteristics for differing anode diameters given the plating conditions of batch A2 (details given in table 5.1)

The diodes were measured using a rudimentary two-probe method. A Keithley 220 current source and Keithley 617 electrometer were employed to gain DC IV measurements. The diodes were contacted using 50μm phosphor-bronze wire with a chemically etched tip (approximate diameter 2μm) whilst the ohmic pad was contacted with a standard probe tip. Diode idealities and series resistances were calculated as described in [8] and section 2.2.5.

High quality anodes ($\eta \leq 1.10$) were achieved with the Engelhard GP 4g/L solution and the low-stress Platanex solution. Annealing proved to be a key stage in the production of these anodes. Reverse breakdown and idealities were improved following the 300°C bake in forming gas. The widely reported problem of creep [1] was evident in some of the diodes tested immediately after electroplating but was absent from all of the diodes that underwent annealing. The evaporated anodes failed to compete with the best electroplated devices. Lowered reverse breakdown voltages, seen after the annealing stages, indicate that the constituent palladium and titanium layers were not thick enough to prevent diffusion of gold (from the anode capping layer) across the junction. Further investigation of this device structure was not undertaken due to limits on the available substrate material. It was also believed that the oxide layer inevitably present at the Ti/GaAs interface would prove significant and lead to inferior device performance when compared with electroplated platinum diodes.

The diode providing the IV data in figure 5.1 was operated continuously for 48-hours with a DC current of 100µA. After this time there were still no signs of creep and the turn-on voltage and ideality were unchanged.

Diode test data

V (mV)	I (uA)
-6820	-1000
-6770	-500
-6740	-200
-6730	-100
-6710	-50
0	0
693	1
712	2
735	5
757	10
775	20
801	50
823	100
845	200
879	500
909	1000

Eta = 1.08
Rs = 24.7 Ohms

< 5µm diameter dot
Engelhard 4g/L drop (Pulse) plated, 1:1 HCL/DI water etch
5µA for 9700µm^2 - Duty Cycle: 10mS ON / 20mS OFF

Duration 10 minutes, stage temp. 50°C
Soap solution prior to drop application prevented vias from trapping air - >90% plated fully.

High series resistance probably down to whisker probe contact
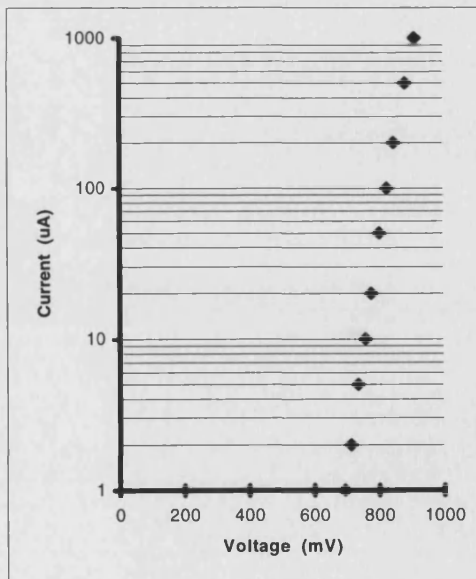
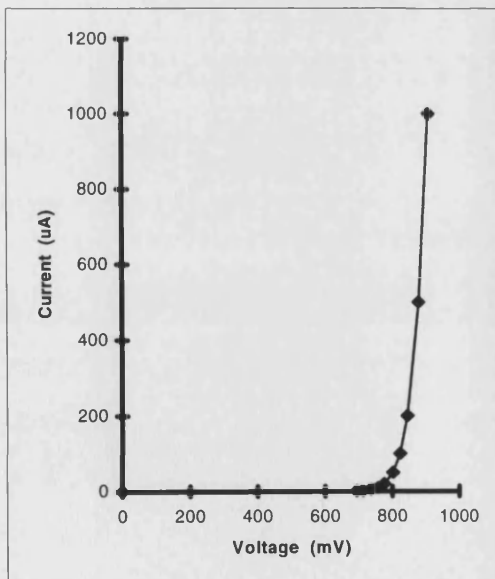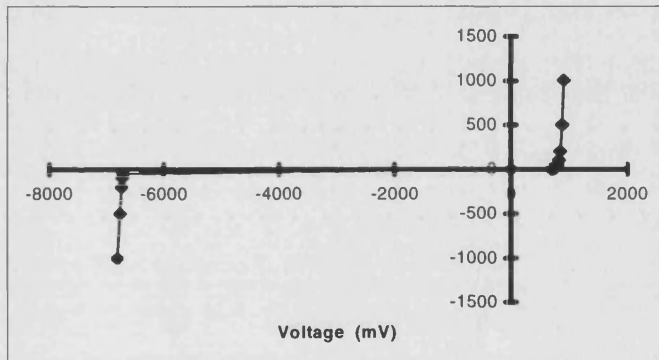Alloyed 10 mins @ 300°C - ideality change 1.20 to 1.08

Figure 5.1. IV results and graphs from 5µm-diameter Schottky diode electroplated with Engelhard 4g/L platinum solution and annealed.
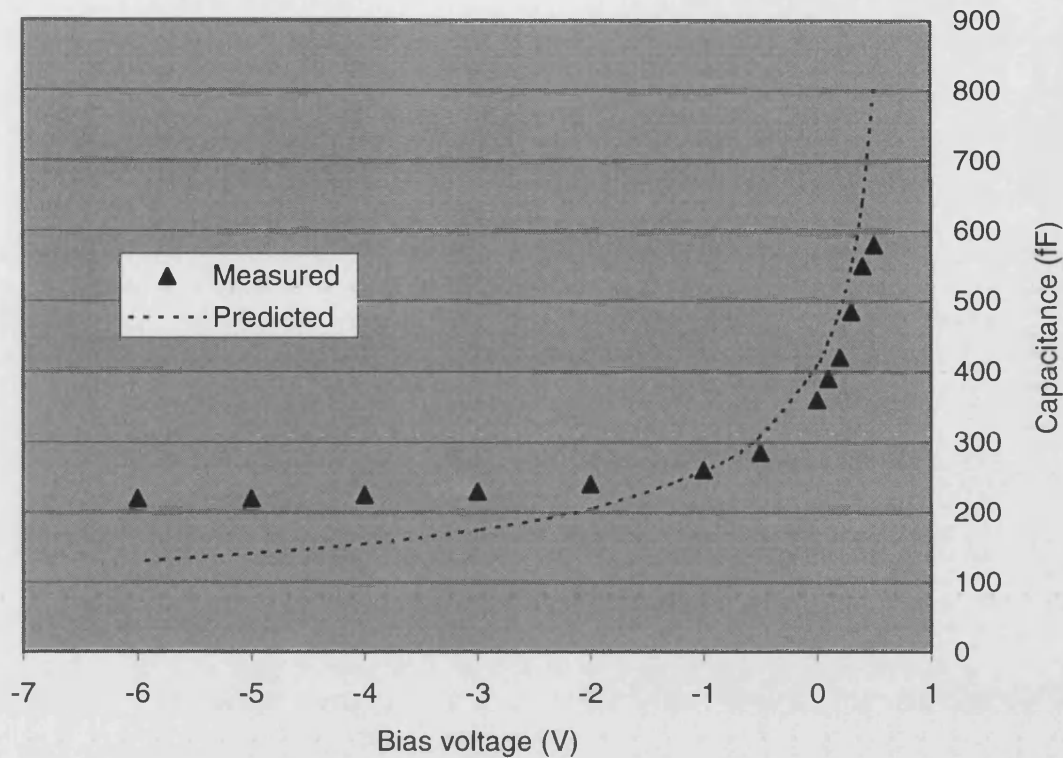
158

Figure 5.2. C/V characteristics from a 25µm diode electroplated using Engelhard GP solution (4g/L).

With no dedicated C/V meter available a Hewlett Packard 4192A LF impedance analyser was used to find the zero-bias capacitance of the diodes. Attempts were made to record the junction C/V behaviour but smaller diodes were repeatedly blown using the in-built bias supply from the impedance analyser. Data for a 25µm diameter device is shown in figure 5.2. Extrapolating the data from the 25µm-diameter anode and assuming identical behaviour for smaller junctions gives predicted maximum and minimum capacitance values of 8.4fF and 3.2fF for a 3µm-diameter device. This degree of variation is respectable for a sub-millimetre wave varactor. However, due to the problems experienced with device burn-out, it was not possible to ascertain whether the C/V behaviour of the larger devices was indicative of anodes in the 3-20µm diameter range. Finally, it is worth noting that the material used for these tests was intended for forward biased mixer diodes and not for reverse bias operation, therefore the measured capacitance variation was limited by a low (~2V) reverse punch through voltage (section 2.2.6).

5.2   Waveguide components

Successful exposure and development of SU8 waveguides and filters with heights of up to 800µm was achieved and excellent wall verticality and smoothness were inherent features. The UV bulb strength was monitored using test exposures and it was found that the operating life span reported by the manufacturer corresponded well to the useable period found by practical use. In general, processing with SU8 proved effective and repeatable. Prolonged exposure to the EC solvent developer caused no significant damage to the exposed SU8 with only slight loss of adhesion to the substrate (around edges) noticeable for extended over-development.

Unfortunately, relatively small ambient temperature changes (as low as 60-25°C over 1 minute) led to fracturing of some SU8 films and carrier substrates (fig. 5.3), a problem that became difficult to avoid in the coating stage of component fabrication. Imaging the SU8 so as to minimise the remaining areas on the carrier substrate helped minimise the possibility of fracture but depending on the component design this was not always possible. The metal coating procedures that were employed are discussed in detail in the following paragraphs. A large part of the selection process for these methods rested on minimising thermal stress in the SU8 film.

Figure 5.3. Silicon substrate (thickness 400µm) fractured beneath SU8 following copper sputter-coating (SU8 exhibited fine fracture lines over most of its surface).

It was clear from the beginning that effective metallisation of the SU8 component features would be a critical factor in RF performance. Early trials involved heavy copper sputtering onto the SU8 components. Film thickness measurements carried out using the sputtering system owned by the group indicated that coverage on vertical faces was a very small fraction of that attained on horizontal faces. Heat build-up caused fracturing of the SU8 layers before sufficient amounts of copper had been deposited onto the waveguide sidewalls and iris fins.

An angled stage was constructed and multiple sputter runs were performed with the sample inclined at 45° and rotated through 90° steps prior to each run. A total of five depositions were performed for each batch of samples, with the final sputtered coating applied to samples held horizontally. The sputterer was allowed to deposit 500nm per run following a pre-sputter to remove oxides from the sputter target. This method clearly afforded better coverage, but blistering of the copper films persisted, as did fracturing of the SU8 layers during post sputter cooling.

Attention then turned to multiple angled evaporations and electroplating. The evaporated-film approach was adopted using gold and results were much improved for films of 400-600µm in thickness. These evaporation-coated samples were the first to be taken for RF tests. Whilst loss was still higher than expected, pass-bands were evident and occurred at the desired centre frequency (see section 5.3.3).

For mechanical strength and the ability to produce conducting films many skin-depths in thickness, electroplating initially seemed the logical choice [9,10]. Appendix 3 contains details on the make-up of the electrolytes used. Whilst straight waveguides were produced with reasonable characteristics using electroplated metal coatings, poor passband throughputs were achieved for filters with gold, copper and nickel electroplated layers.

Poor performance from the plated filters was found, through optical inspection, to be due to the varying degree of coverage offered by the electroplating baths and solutions [11]. Plated layers on all samples were enormously non-uniform; large elevated areas receiving thick coatings, whilst thin, discontinuous plating occurred along the broad-wall/side-wall seams. This problem was exacerbated when

attempting to electroplate iris and septa style waveguide filters. Effort was made to remedy this problem using shielding and drop plating methods but coverage always appeared erratic. Ultimately, all SU8 waveguide filters taken for RF tests with electroplated layers showed high absorption.

Evaporated layers exceeding 1μm in thickness were not practical using our in-house systems and electroplating only proved satisfactory for straight waveguide sections. Attention then turned to electroless methods [12, 13]. Electroless plating solutions are renowned for their ability to provide uniform coverage in high aspect ratio applications including plating of integrated circuit board through-holes. The solutions adopted for testing were 230 and 850 electroless gold from Engelhard and electroless nickel from Caswell (Appendix 3).

Experimentation with electroless plating is still underway at the time of writing but in terms of adhesion, uniformity of coverage and grain size, both the Engelhard 230 and 850 processes provide superior results when compared with the previously tried electroplating methods. However, for designs such as the inductive iris and E-plane septa filters, activation of the SU8 still represents a processing challenge. The method involving airbrushed Electrodag detailed in Appendix 3 provided a suitable activation layer for the Engelhard 230 electroless solution. However, due to running in the sprayed undercoat, this method often resulted in enlargement and rounding of the plates within the inductive iris filter.

Thermally evaporated seed layers were used to provide activation and this proved partially successful for simple filters and straight waveguide sections. Limitations in this method became apparent following trials with a side-wall branch connected directional-coupler. Thermal evaporation failed to provide sufficiently uniform coverage for complete activation of the closely spaced blocks and trenches that are constituent elements of this coupler design (fig. 5.4). A primary aim of this work was to find a metallic coating method for SU8 that would be applicable to as many component designs as possible. Clearly, seed layers formed by evaporation would have limited application. In addition, the adhesion afforded by evaporated layers was often insufficient to support the (relatively high-stress) layers deposited by the

Caswell electroless nickel and Engelhard 850 gold processes. With these points in mind, trials with electroless plating solutions and activation methods are continuing.
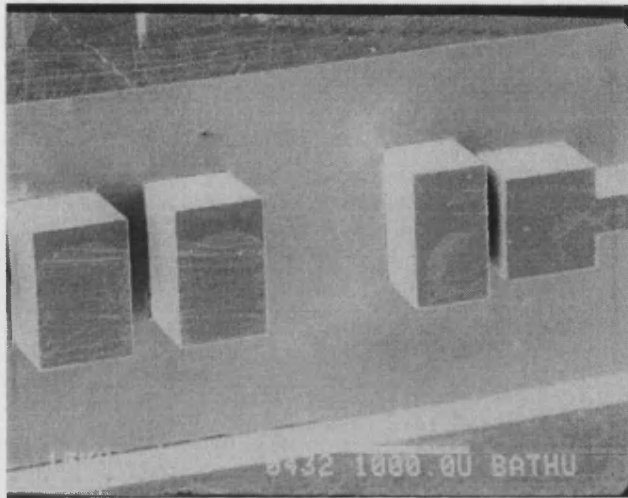

Figure 5.4. SEM micrograph of a directional coupler featuring closely spaced blocks fabricated in SU8.

5.3 RF results

Aspects of fabrication relating to SU8 waveguide components were discussed in the preceding section. This section describes the test apparatus employed to evaluate the RF performance of these structures and illustrates the results obtained. Plots showing the throughput for straight waveguides and waveguide bandpass filters (centre frequency 135GHz) are included and compared with data from a section of conventional waveguide operating in D-band.

5.3.1 RF test apparatus

Fig. 5.5 illustrates the system employed to perform measurements on the waveguides and waveguide filters developed in this thesis. The backward-wave oscillator (BWO) was an ELVA-1 G4-142cM model with continuous sweep capability from 110GHz to 180GHz. All filters produced for testing were designed to have pass-bands at 135GHz. Ideally an isolator would have featured in this set-up, however none were available and standing wave interference between the source and external circuit would have been present during measurement. The branch, coupling power 10dB

down on the input signal, was connected to an Anritsu MP81B4 power head, which was connected to an Anritsu ML83A power meter.
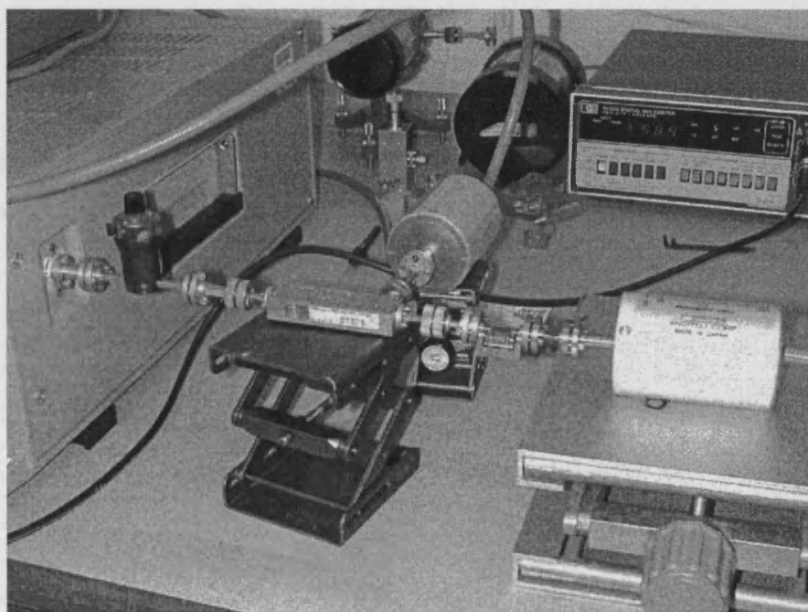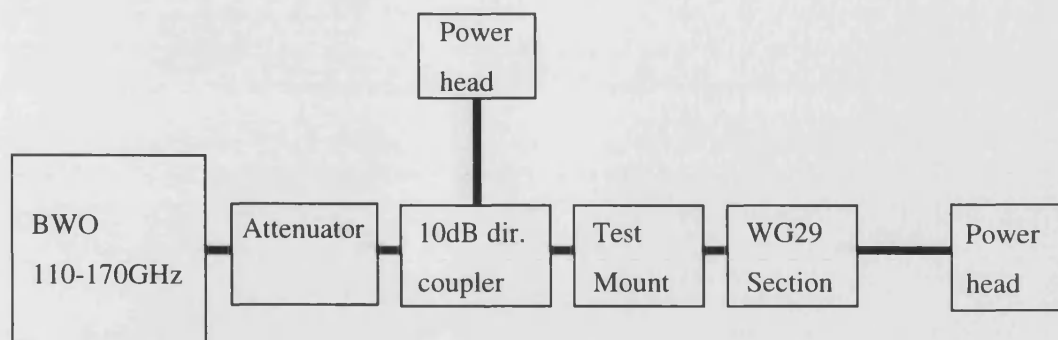

Figure 5.5. Test system employed for MEMS waveguide and filter measurements.

For measurements carried out on straight waveguide (MEMS and conventional), branch power was measured against a 1mW reference power held constant at the output power head across the full measured frequency band. The test-mount (see Appendix 2 for dimensions and layout) was then connected to the output line of the coupler and onto the output power head (Anritsu MP82B4) via a section of conventional WG29 waveguide in UG387/U flanges. This length was introduced in order to increase the distance between the test-mount (WG29) and the mismatched power head (WG28) [14]. An Anritsu ML4803A power meter registered output power. The BWO oscillator was calibrated for frequency using a wavemeter.

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Agreement within 2GHz was achieved against the manufacturer supplied calibration graphs.

5.3.2   Coated SU8 waveguides

Measurements showing throughput against frequency for the test system (fig. 5.5) prior to insertion of the test mount are shown in figure 5.6.
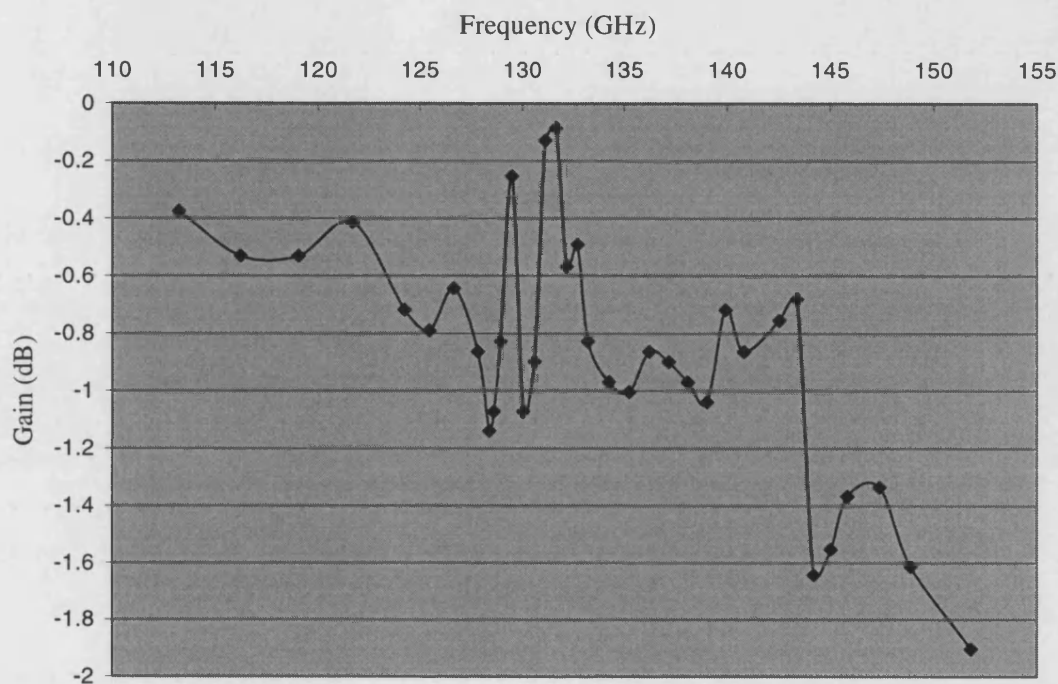
Figure 5.6. Throughput seen before insertion of the test-mount.

Figure 5.7 shows throughput achieved for SU8 WG29 waveguide trenches coated with copper and nickel and capped with aluminium lids. These aluminium lids were coated with gold via thermal evaporation, then bonded (using silver loaded epoxy) onto the substrates featuring the trench waveguides.

Figure 5.8 shows results achieved for electroplated (Electrodag seed layer) SU8 waveguides with thermally evaporated gold lids subsequently reinforced with bonded aluminium plates. A section of conventional copper WG29 waveguide was inserted into the test mount and measurements for this sample are also included.
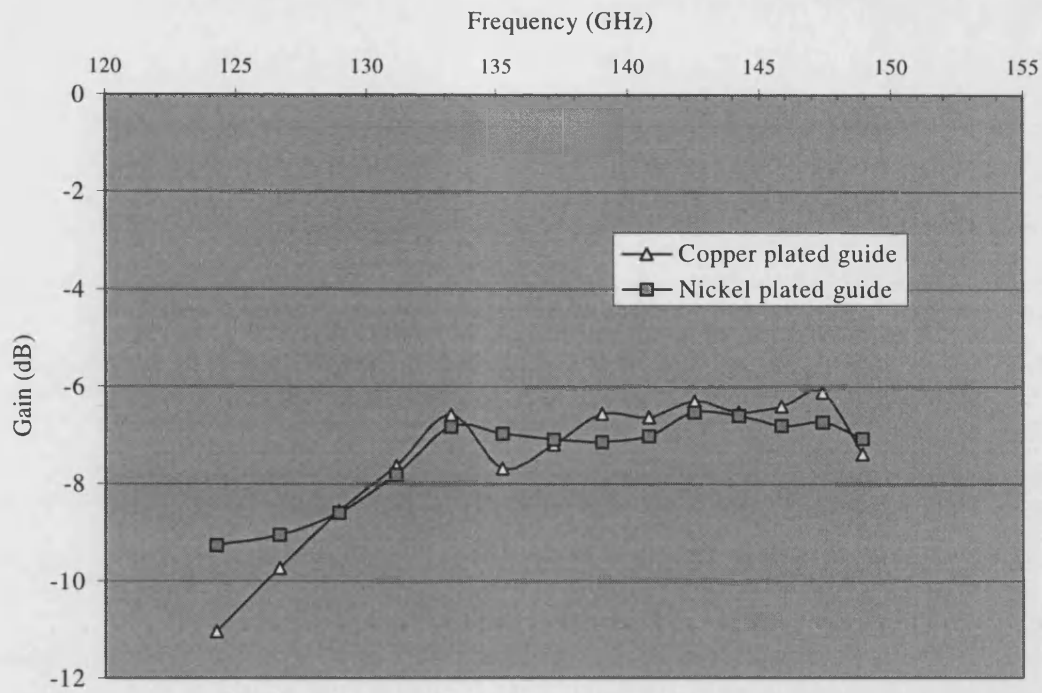
Figure 5.7. Copper and nickel electroplated SU8 WG29 waveguides with gold-coated lids bonded using silver epoxy.
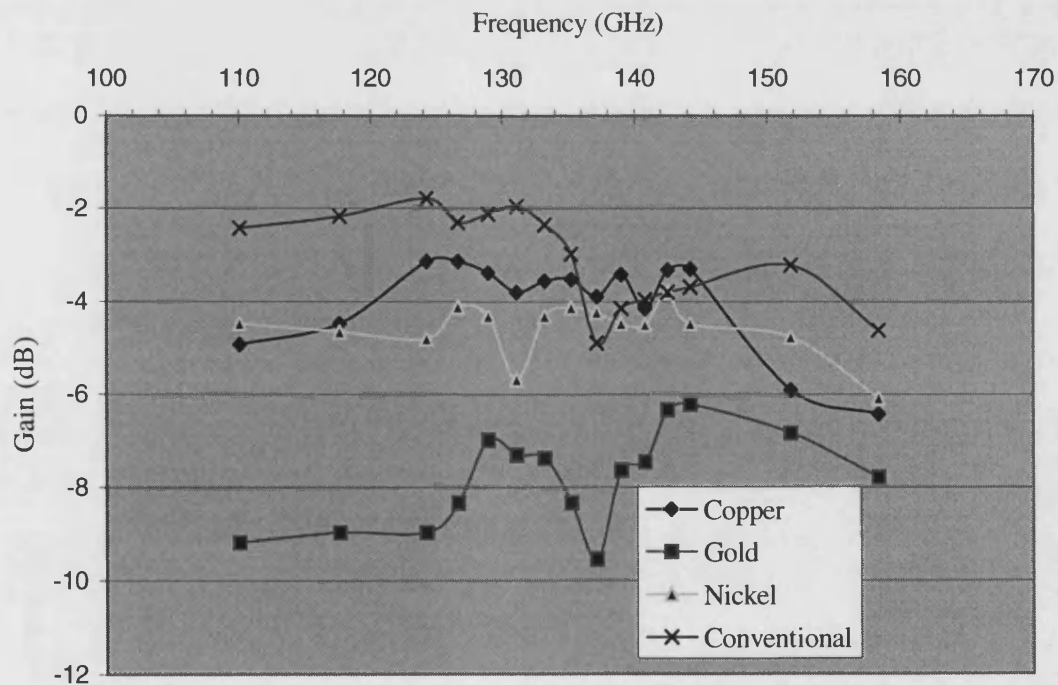

Figure 5.8. Measured throughput for conventional WG29 waveguide and WG29 waveguides formed in SU8 and coated with electroplated copper, gold and nickel.

The results achieved for straight waveguide sections fabricated in SU8 proved informative. As discussed in section 5.2, inherent limitations in the electroplating process led to difficulties in coating the waveguide cavity uniformly. Flaws were far more severe when attempting to electroplate the iris filters, but non-uniform plating was still evident on the SU8 waveguides used to produce the plots in figures 5.7 and 5.8. These samples were electroplated until the minimum thickness within the cavity (normally occurring at the seams between the waveguide floor and side-walls) was judged to be several skin depths in thickness. This inevitably resulted in over-plating in other areas, including the central regions of the broad- and side-walls. In practice, the deformation caused to the rectangular cross-section of the waveguide was minor (variation in broad-wall coating thickness was less than 20μm) and both the copper and nickel coated SU8 test guides featured in figure 5.8 enabled transmission comparable with the sample of conventional waveguide.

The second issue raised by tests on straight SU8 waveguides concerned the operation necessary to transform the SU8 cavity into a full waveguide. Initially trials were performed with lids clamped mechanically onto the substrate carrying the metallised SU8 trench. These tests showed that the guides had high transmission loss (typically 8-10dB down on the input signal). Improvements were seen using MEMs waveguide samples with bonded lids (fig. 5.7) but transmission through these samples was still significantly lower than transmission through the conventionally machined copper waveguide.

The results shown in figure 5.8 clearly indicate that the combination of thick plated coatings and evaporated lids gave the best performance. As described in section 4.14, the SU8 trenches were filled with water-soluble paste, which was then lapped down to the level of the side-walls. Thermally evaporated gold then formed a lid that intimately contacted the broad area alongside the waveguide side-walls. The final fabrication stage involved washing the paste out of the trench to form a hollow rectangular waveguide. These samples exhibited the lowest loss but were still slightly inferior to the conventional waveguide section. The additional loss was attributed to the surface quality of the evaporated waveguide lid (reflecting the surface finish of the lapped paste filling the waveguide trench).

5.3.3 Coated SU8 iris resonator filters

The points made in the previous section are substantiated by the work presented in this one. In section 5.2 much emphasis was placed on the difficulties encountered when attempting to electroplate waveguide iris filters. Results from an iris filter electroplated with gold (evaporated gold seed layer) are presented in figure 5.9 and show a high level of loss caused by inconsistent coating of the SU8 iris fins. Visual inspection of this sample revealed breaks in the metal coverage around the fins particularly at the points where the fin joined the waveguide side-wall.

Figure 5.9. Throughput for a 135GHz inductive iris bandpass filter fabricated in SU8 and coated with an evaporated gold seed layer followed by electroplated gold.

In a bid to increase the uniformity of coverage, filters were produced and coated with metal thermally evaporated from multiple angles. An example of the performance attained using this method is shown in figure 5.10. Improvement is seen over the electroplated filter of figure 5.9, however loss in the pass-band is still much higher than experienced for the straight waveguides fabricated in SU8.

Figure 5.10. Throughput for a 135GHz inductive iris bandpass filter fabricated in SU8 and coated with gold thermally evaporated from multiple angles.

Finally, results are presented in figure 5.11 for inductive iris filters coated using the same multi-angle evaporation procedure as described above but with evaporated gold lids rather than bonded lids. A further improvement is seen in these results, lending support to the arguments put forward concerning evaporated lids on straight SU8 waveguides. Samples with mechanically clamped or bonded lids consistently demonstrated low throughput. Suggested reasons for this poor performance were inconsistent contact and/or the inherent resistance of the silver epoxy or electrodag used in bonding the lids.
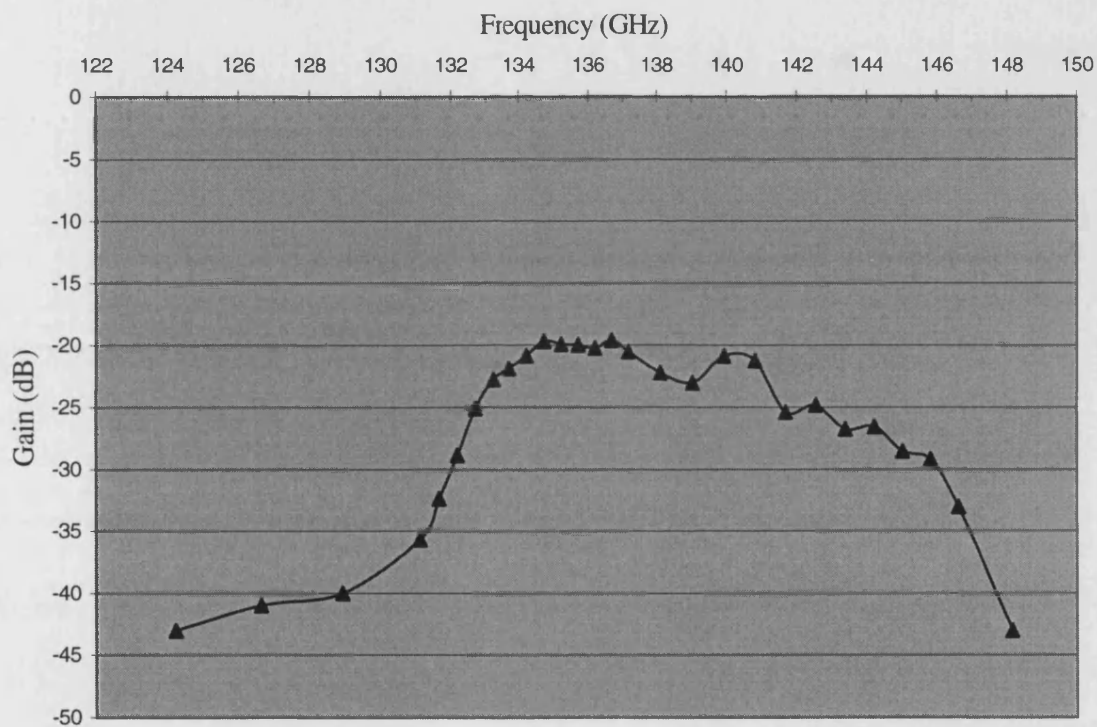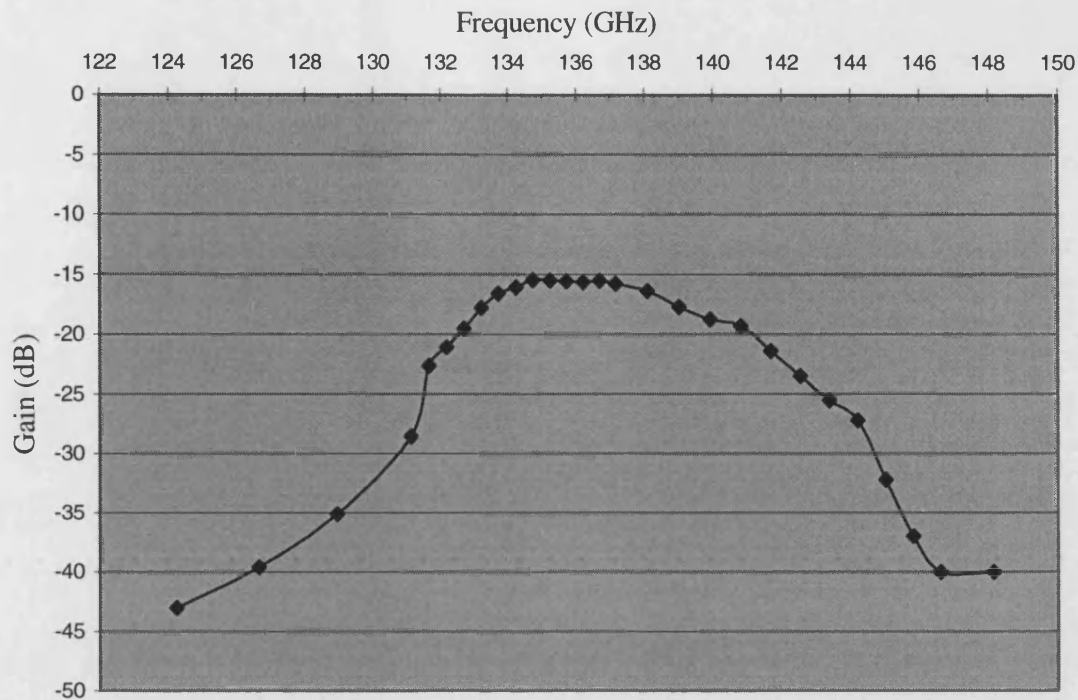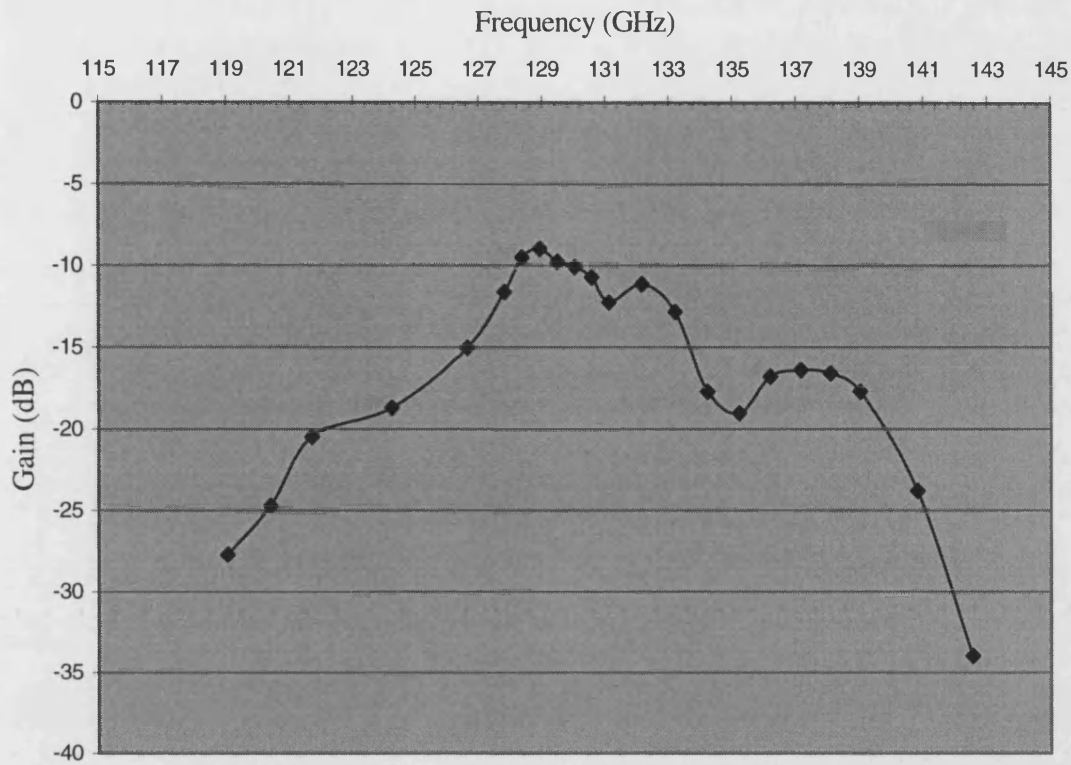
Figure 5.11. Throughput for a 135GHz inductive iris bandpass filter fabricated in SU8 and coated with an evaporated gold seed layer followed by electroplated gold.

Further improvements in the characteristics of these filters would almost certainly result from finding a means of producing evaporated lids with mirror smooth internal surfaces. Aside from concerns over surface quality, it was also unclear when using the lapped paste, whether full contact was made between the evaporated lids and the top surface of the iris fins. Filling the waveguide trenches with one of a number of alternative materials available may help in satisfying these design requirements. Proposed strategies for improving the finish and RF performance of the components described in this section are put forward in the future work section of the concluding chapter.
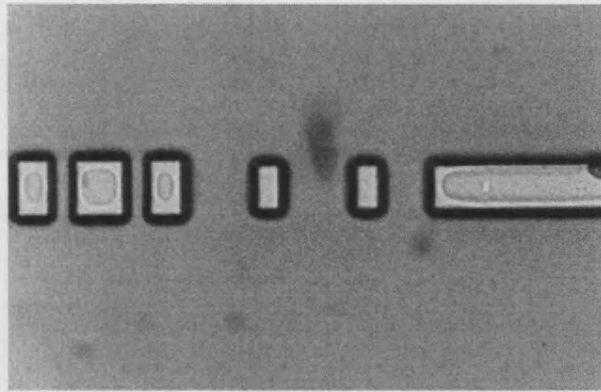
5.4 Air-bridge stripline

Section 3.8 described the development of a stripline low-pass filter suitable for application within a micromachined frequency tripler. SU8 was selected as a photo-imageable dielectric material that could support the stripline. A design based on a solid SU8 dielectric layer was shelved when the loss tangent of SU8 was found to be too high for efficient operation of the filter at the harmonic output frequency. Designs that featured large air-bridges between supporting SU8 struts were then developed.

This section illustrates the work that was carried out in an effort to make the final design a real structure. The fabrication scheme in section 4.10 illustrates the intended processing for this component. The imaged SU8 struts were surrounded with a layer of thick conventional photoresist onto which a gold film of multiple skin depths was evaporated. A second, thinner layer of SU8 was patterned with the filter shape and via a simple wet etch, this pattern was translated into the underlying gold layer.

In practice, it proved impossible to produce a planar surface with the combined AZ series resist layer and the SU8 struts. Figure 5.12 illustrates SU8 struts surrounded by an AZ4533 resist layer. Part (a) of this figure illustrates the struts after partial clearing of the AZ resist from their top surfaces and (b) shows the struts after all resist is cleared from the top of the SU8. The exposure and development required to perform this step proved repeatable with alignment achieved fairly easily. However, it was found that if the AZ resist was spun to the same thickness as the SU8, discontinuities in the gold layer arose due to the build-up of resist near the edges of the struts. Dropping the thickness of the AZ resist layer led to excessive draping of the gold film between the struts. This would have resulted in distorted and unpredictable filter characteristics.

A solution was proposed based on sacrificial etching methods. Following patterning of the SU8 struts, the anode region was masked with photoresist and the gold ground plane was electroplated with copper (using the solution listed in Appendix 3). This copper plating procedure continued until the electroplated copper layer formed a planar surface with the SU8 struts. Figure 5.13 illustrates this stage. A gold evaporation was then performed and followed by the application of a spun SU8 layer

(3μm in thickness) which was patterned with the stripline low-pass filter shape. A wet-etch then translated this pattern in SU8 into the layer of gold below. Finally, after forming the stripline filter in gold (reinforced by the SU8 top layer), a selective wet-etch was used to remove the copper.

(a)
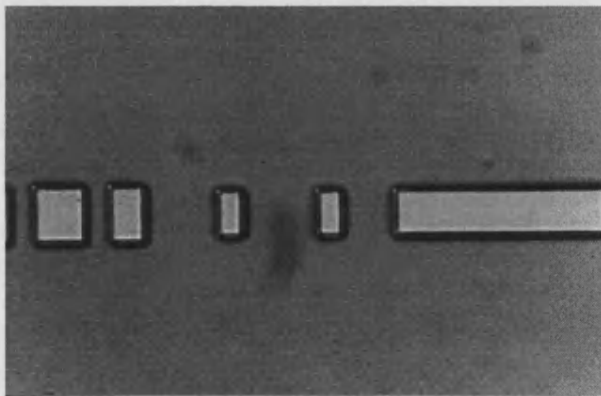
(b)

Figure 5.12. SU8 struts for air-bridged stripline filter (a) partially cleared of resist and (b) completely cleared.
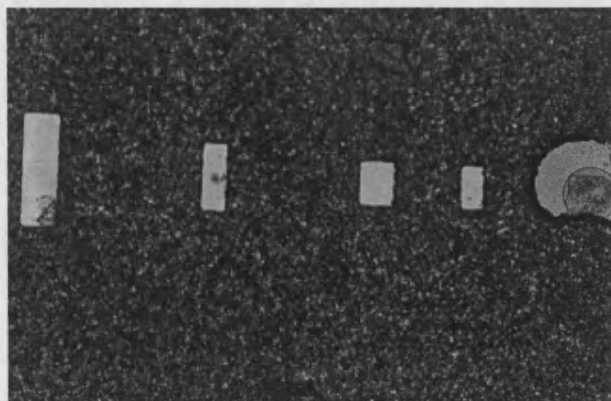
Figure 5.13. Sacrificial layer formed with electroplated copper on gold ground plane.

The sacrificial copper method showed promise initially, but the grain size of the electroplated deposit was too high for the evaporated gold to form the continuous layer necessary for the stripline filter. It is believed that this method could prove workable by employing a second planarisation stage and possibly an alternative plating solution with a finer grain size. A resist layer spun onto the electroplated copper could seal the small gaps between grains and create a smooth surface for the evaporated gold layer.

An alternative and preferable approach is to revert back to a stripline design based on a solid dielectric and find a means to pattern a low loss dielectric material. Spin-on glasses and photo-imageable dielectrics exist that fulfil the low loss requirement and would provide a more stable support for the stripline than the air-bridged scheme.

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[6]   A. K. Sinha, T. E. Smith, M. H. Read and J. M. Poate, "n-GaAs Schottky diodes metallized with Ti and Pt", Solid State Electronics, Vol. 19, No. 6, pp. 489-492, June 1976.

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6. Conclusion

The aim of this chapter is to provide a summary conclusion based on the results presented in chapter 5 and obtained from fabrication runs, DC device testing and RF testing of micromachined structures. The chapter attempts to address the difficulties and negative aspects of the processing demonstrated in this project and aims to re-emphasise beneficial steps relating to device performance and the mechanical and RF quality of the fabricated MEMS components.

Towards the latter stages of this project it became apparent that the process of metal coating was crucial to the successful operation of components based on SU8. For this reason, section 6.2 reiterates some of the observational points from chapter five. Within this section, the merits and pitfalls of three seeding methods for subsequent electroless plating are also described.

Before summarising the findings on SU8 component fabrication, the following section contains concluding remarks on the device processing aspects of this project

6.1   Schottky diode and contact post formation

It was clear from the anode plating trials described in section 5.1, that pulse plating produced diodes with better ideality and higher reverse breakdown voltages than DC plating. Pulsed electroplating also increased the yield of successfully plated devices within the test arrays (typically >90%).

The pulsed plating methods employed produced shiny, uniform plating with both the Platanex and Engelhard solutions. The grainy texture often seen with DC plating was more pronounced when electroplating with Platanex solutions. It is probable that this grainy plating led to inconsistent contact at semiconductor/platinum interface and consequently variable effective device area. Measurements of zero bias capacitance carried out across arrays of DC plated diodes showed greater fluctuations than their pulse-plated counter-parts.

The annealing stage proved to be effective in producing sub 1.10 ideality diodes. Long-term tests need to be performed in order to assess the operational stability of diodes fabricated with and without the annealing step. As a first step a 5μm diameter device was operated with a forward current of 100μA for 72-hours with no change in ideality, reverse bias or series resistance witnessed. Peeling (reported by Pham et al. [1,2]) during annealing only occurred on some samples electroplated with the standard Platanex IBD solution.

The thermally evaporated Ti/Pd/Au diodes failed to match the quality of the best electroplated devices. In the time taken to load the evaporator with substrates prepared for diode formation, a thin oxide layer would have formed on opened anode surfaces which may have contributed to the inferior idealities achieved. Limits on the available substrate material and the excellent results achieved with electroplated platinum anodes halted further investigation with evaporated metal Schottky diodes.

In short, both Engelhard GP (4g/L) and Low-Stress Platanex solutions were used to produce high quality anodes. The appropriate operating conditions are shown in figure 5.1. Annealing as a tool for diode improvement needs further qualification but initial results show great promise.

The novel diode-to-stripline transition was successfully fabricated using a solid dielectric layer to support the stripline. If a material with a suitably low loss tangent were used to form a solid dielectric layer this process should be reproducible. By contrast the air-bridged stripline proved impractical. Difficulties experienced were due to unevenness across the SU8/AZ resist surface and, when adopting a sacrificial etch method, high grain size in the electroplated layer.

Due to the absence of an in-house dicing saw, an alternative approach for realising the stripline filter has not yet been explored but may prove viable in future. In this scheme, a quartz stripline substrate is bonded onto a GaAs wafer containing the pre-formed anode array. The quartz is diced to the required dimensions and slid into place using SU8 alignment blocks on the GaAs substrate. The electroplated whisker and stripline fabrication processes could then be performed as described in section 4.10. A low-loss dielectric based stripline would result.

Through refinements in the fabrication sequences (and possibly using new MEMS positive photoresists), improvements could be made to the electroplated contact post mechanisms adopted for the doubler and tripler described in this thesis. However, it is the author's belief that although the electroplated whisker contact method described in section 4.5 may find application in the fabrication of devices operating at frequencies above 1THz, planar devices offer many advantages at lower frequencies. The possibilities for further device integration are numerous and if this project were to be repeated, a planar device scheme would be the preferred choice.

6.2 RF results

The RF results obtained for the inductive iris coupled filters were disappointing, with low throughput and poorly defined pass-bands (see section 5.3.3). The imaged SU8 filter components were relatively easy to produce and exhibited few imperfections whilst the metal coatings produced by evaporation, sputtering and plating were far from ideal on these structures. Electroplating was successfully utilised to produce straight waveguide sections with non-uniform, but complete, coverage. An attenuation of approximately 1.0dB/wavelength was achieved (fig. 5.11) which compared well with the figure reported for micromachined silicon waveguides (0.8dB/wavelength) [3]. At the time of writing the best performance attained from an SU8 filter saw the throughput in the pass-band at 3.0dB/wavelength. Electroless plating appears to be the optimum method for coating SU8 waveguides in-house. In order to activate the SU8 epoxy and allow electroless plating to begin, three methods are currently in use; air-brush application of electrodag, immersion application of electrodag and thermal evaporation of a metallic seed layer. Of these methods, thermal evaporation and airbrushed electrodag are limited in the types of component that can be successfully coated. Immersion application of electrodag (dilute) offers the best means to coat components with closely spaced features without running (airbrush) or shadowing (evaporation) effects.

Evaporated metal lids proved vital in reducing the loss in filter and straight waveguide sections. The method chosen to alleviate this problem was not ideal (due to irregularities in the lapped filling material) and a further reduction in attenuation from waveguides and waveguide filters is expected if a method can be found which produces thicker (>1μm) and smoother waveguide lids. Experimentation with

alternatively oriented waveguide splits is also underway (see section 4.15 for example with central broad-wall split).

6.3 Concluding remarks

This project has shown the potential of micromachining techniques for Terahertz applications. Taking the iris filter and tuning components as examples, it was readily apparent that precision and surface quality is achieved in MEMS that cannot be matched by conventional machining techniques. An additional benefit with the MEMS approach is that, with a dedicated mask, several iris filters or tuners can be patterned in SU8 in a few hours. Assuming similar components could be fabricated using conventional precision machining, the process would be far more labour-intensive.

The problems that led to the micromachined filters exhibiting high loss have been discussed. It will be necessary to find a method for coating SU8 components with uniform, high adhesion, high conductivity metal layers. Electroless plating should fulfil this requirement, provided a suitable means for activating the SU8 is found.

In order to permit RF testing, a scaled version of the doubler circuit will need to be fabricated and this process is underway. Many of the restrictions that led to the design evolving as it did have now been removed. These range from differences in the way the structure can be modelled in HFSS (increased computing capabilities remove component symmetry requirements) to substrate size limitations. A mount similar to the proven RF test mount (Appendix 2) adopted for the filter and waveguide measurements has been designed and will carry the multiplier during the RF tests. This mount will incorporate at least one micrometer drive for circuit tuning. Based on the modelling work carried out during this project, circuit tuning appears essential for any single varactor multiplier circuit. Certainly, the processing involved in forming SU8 tuners has been proven. The sacrificial layer technique standard in MEMS proved reliable in releasing the tuners and in other applications including E-plane septa blocks. As soon as the problems involved in coating SU8 are completely resolved, the multiplier will be assembled and RF testing will begin.

6.4   Future work

The MEMS field is expanding with new materials becoming available to support an increasing number of applications in medicine, optics, radio frequency electronics, defence and many other areas. Many more MEMS specific photoresists now exist than were available at the outset of this project. In particular, positive resists are now available that offer higher transparency and greater achievable patterned film thickness.

As an example of further component possibilities, fig. 6.1 illustrates a branch-line directional coupler fabricated in SU8 (G-band waveguide). The linking channel widths are critical to the predicted performance of this component and would represent a massive challenge to conventional machining methods. As with the waveguide iris filter shown in chapter four, the dimensions of this microfabricated component are adhered to with deviations in the sub-10µm range. Issues over temperature stability may be resolved with new materials or by allied electroforming techniques. It is clear that SU8 has allowed terahertz MEMS to advance considerably.
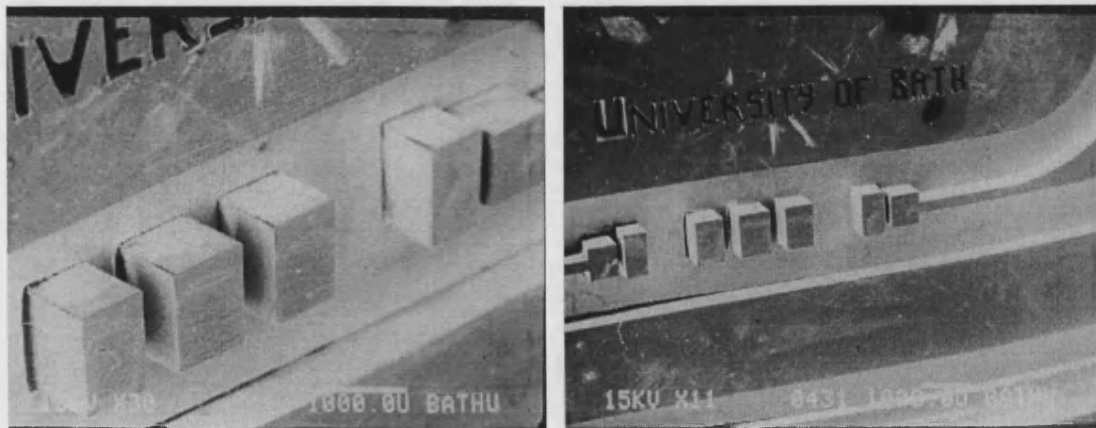

Figure 6.1. Branch-line 10dB directional coupler formed in SU8.

Moving away from passive circuit MEMS and focusing on device fabrication, this project has demonstrated a processing scheme for submillimetre-wave diodes that is integrated with the formation of the surrounding circuit. The electroplated whisker

arises from a low-throughput process but it allows precise positioning of a robust low-parasitic contact post onto pre-formed, characterised devices.

Improvements made in planar device technology have extended cut-off frequencies and this technology looks likely to substantially replace whisker diodes in terahertz mixers and multipliers. A logical progression for planar devices suggests that they be fabricated simultaneously with the supporting bias and RF circuitry on a single semiconductor substrate. Anisotropic etching techniques could allow this substrate to be patterned in such a way as to form a low-loss device embedding circuit when located inside a microformed waveguide assembly [4]. E-plane suspended components were demonstrated in this thesis in the form of passive foil septa (section 4.15). An advancement of this technique could see split SU8 blocks accepting lapped semiconductor substrates featuring planar transitions, bias lines and planar active devices. Time consuming and risky device bonding and soldering could be completely eradicated in this way.

High quality devices are critical in terahertz circuits. Techniques including pulse electroplating and annealing have been reported and refined to produce excellent results for micron scale anodes. The study found in chapter five highlights the benefits of these methods. With the arrival of a Reactive Ion Etching (RIE) system at Bath, it is hoped that high quality sub-micron anodes can be fabricated alongside the larger anodes that have been produced there to date.

When micromachined circuit elements such as multipliers, mixers and detectors have been demonstrated with high operating efficiencies, a logical progression would be towards further integration. Approaches such as those employed to produce the septa foil filter could be employed with GaAs substrates, to produce circuits mounted in waveguide that include LO, multiplier and mixer elements. This method could be expanded still further to allow the same GaAs substrate to carry IF circuitry.

The advantages offered by MEMS techniques in the field of sub-millimetre wave technology are quite clear. High precision components can be rapidly developed and fabricated with potentially very low-cost. If a mass-market application is found for terahertz frequencies, MEMS seems the logical choice for system fabrication.

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Acknowledgements

There were points during this PhD when, without intervention and assistance from numerous people, I might have packed it all in and headed West to plough fields. This section is a token of my appreciation to these people.

Work

Within the Physics department I'd like to thank Wendy Lambson, Bob Draper, Mike Harriman, Peter Ford, Barry Chapman and Miklos Tatar for assistance in ordering, photography and good-humoured banter. Dr. Alain Nogaret provided much needed advice relating to the Jeol electron-beam writer. Dr. Hooman Kazemi and Dr. Simon Wootton provided valuable conversation (technical and hysterical) and helped me retain my sanity when times were hard. Dr. Steve Davies, my supervisor, has always been available to discuss fabrication ideas and assisted in all RF measurements. His help with this thesis was greatly appreciated.

At the Rutherford Appleton Laboratory, I'd like to express thanks to Chris Mann and Dave Matheson for help with waveguide filter measurements. At Engelhard-Clal, thanks must go to Mike Wild who performed plating trials and provided sample solutions. I'd also like to thank the suppliers of Caswell plating solutions, Speed-Demon for an excellent service. For scale models, test fixtures and other well executed machining jobs, I'd like to thank Paul, Steve and Les in the central workshop.

On the outside

The support I've received from my parents throughout my undergraduate and postgraduate studies has been amazing. They have provided every means of support possible. I would never have got this far without them.

For a week of Portuguese sun, sand and Superbock just when it was most needed, I'd like to say thanks to John 'Saxby' Breland, Rich Channell, Neil 'Wilkie' Elkins and Mark Davies.

Appendix One – Filter design code.

The following MATLAB code was written as a design tool for inductive iris, coupled-resonator waveguide filters with user-stipulated Tchebyscheff or maximally-flat response. The design process is based on that of [A1.1] via lumped element models for the inductive irises obtained from [A1.2]. The normalised source and load impedances are unity for odd-order filters. Even-order Tchebyscheff filters have unity source impedance and load impedances calculated from the appropriate coefficients.

```
% Jim Partridge, Terahertz Technology Group, University of Bath.

clear

a=input('Enter width of waveguide in microns > ');
a=a*1E-6;

fc=input('Enter centre frequency of bandpass filter in GHz > ');
fc=fc*1E9;

bw=input('Enter desired bandwidth in % - max.=10% > ');

type=input('Tchebyscheff (1) or Maximally Flat (2) > ');

if type==1
  ripple=input('Enter desired passband ripple in dB - 0.1-3dB > ');
end

note = ['Attenuation as a function of filter order n is presented for w/wa=1.5.'
        'wa is the angular frequency point on the low-pass prototype roll-off '
        'corresponding to the ripple level (tcheb.) or 3dB point (max. flat). ']

note = ['Attenuation as a function of order n = 1 to 10']

% Present attenuation data for n=1 to 10
apoint = 1.5;
clear attn
if type==1
  for n=1:1:10 % Tchebyscheff attenuation as a function of order
    Ef = (10^(ripple/10)) - 1;
    attn(n) = 10 * LOG10( 1 + Ef*((cosh(n*acosh(apoint)))^2));
  end
elseif type==2
  for n=1:1:10 % Maximally flat attenuation as a function of order
    attn(n) = 10 * LOG10( 1 + apoint^(2*n));
  end
end
attn
```

185

```
order=input('Enter desired filter order - n=3 requires 4 iris pairs > ');
inum=order+1;

% Calculate guide wavelengths for centre and band edge frequencies

cwavl=2.998E+8/fc;
cgwavl=cwavl/((1-(cwavl*cwavl/(4*a*a)))^0.5);

fa=fc-((bw/200)*fc);
awavl=2.998E+8/fa;
agwavl=awavl/((1-(awavl*awavl/(4*a*a)))^0.5);

fb=fc+((bw/200)*fc);
bwavl=2.998E+8/fb;
bgwavl=bwavl/((1-(bwavl*bwavl/(4*a*a)))^0.5);

wbw=(agwavl-bgwavl)/cgwavl;

if type==1
  % Derive Tchebyscheff g coefficients
  w1=1;
  beta=log(coth(ripple/17.37));
  gamma=sinh(beta/(2*order));
  n=order;
  g0=1;

  for k=1:1:order
    a1(k)=sin(pi*((2*k)-1)/(2*order));
    b(k)=gamma^2 + (sin(k*pi/order))^2;
  end

  for k=2:1:order+1
    g(1)=2*a1(1)/gamma;
    if k > 1 & k < order+1
      g(k)=4*a1(k-1)*a1(k)/(b(k-1)*g(k-1));
    end

    if rem(order,2)==0 % For even order Tcheb. terminating impedance
      g(order+1)=(coth(beta/4))^2;
    else
      g(order+1)=1;
    end
  end

elseif type==2
  % Derive Maximally Flat g coefficients

  w1=1;
  n=order;
  g0=1;
  g(order+1)=1;
  for k=1:1:order
    g(k)=2*sin(((2*k - 1)*pi)/(2*n));
  end
end
```

```
% Find impedance inverter values
% Subscript convention - X subscript[10] is stored in Xnorm(1)
for m=0:1:order

  if m==0
    knorm(m+1) = ((pi/2)*(wbw/(g(1)*g0*w1)))^0.5;
  elseif m==order
    knorm(m+1) = ((pi/2)*(wbw/(g(order)*g(order+1)*w1)))^0.5;
  else
    knorm(m+1) = (0.5*pi*wbw/w1)*((g(m)*g(m+1))^-0.5);
  end

  Xnorm(m+1) = knorm(m+1)/(1-(knorm(m+1)^2));

% Loop finds fin size

  index=1;
  store(1)=1;
  React=Xnorm(m+1);
  clear width;

  for width=2E-6:2E-6:a/2
    index=index+1;
    store(index) = (React-...
((a/cgwavl)*((cot(pi*width/(a)))^2)*(1+(((pi*width/cwavl)^2)*0.667))))^2;
    if store(index) < store(index-1)
      irisw(m+1) = width;
    end
  end
end

% Spacing
spacing(1)=0;
distance(1)=0;
for n=1:1:order
  theta(n) = pi - 0.5*(atan(2*Xnorm(n)) + atan(2*Xnorm(n+1)));
  spacing(n+1) = theta(n)*cgwavl/(2*pi);
  distance(n+1) = distance(n) + spacing(n+1);
end

start=input('Enter start frequency for sweep in GHz > ');
finish=input('Enter finish frequency for sweep in GHz > ');
step=input('Enter step frequency for sweep in GHz > ');

freq_div=0;

for n=start:step:finish % Frequency sweep
  freq_div = freq_div + 1;
  wavl=2.998E+8/(n*1E+9);
  gwavl=wavl/((1-(wavl*wavl/(4*a*a)))^0.5);
  clear reactance j

  yload = g(order+1);
  for istep = inum:-1:1 % Calculating normalised admittance at each iris plane
    reactance(istep)=Xnorm(istep)*j;
    yr = yload + 1/reactance(istep);
    if istep > 1
```

```
      kl = 2*pi*spacing(istep)/gwavl;
      yload = (yr + ((tan(kl))*j))/(1 + (yr*(tan(kl))*j));
    elseif istep==1
      yload = yr;
      reflection(freq_div) = abs((1-yload)/(1+yload)); % Magnitude of reflection
    end
  end
end

irisw
spacing
irispairs = ['Inductive Iris Waveguide Filter (S21-solid, S11 dashed) - No. of iris pairs = 'int2str(inum)];

x=linspace(start,finish,freq_div);
y1=10*LOG10(reflection);
y2=10*LOG10(1-reflection);
plot(x,y1,'k:',x,y2), title(irispairs)
xlabel('Frequency - GHz')
ylabel('Gain - dB')
```

Figure A1.1. MATLAB design code for iris-coupled-resonator filters in rectangular waveguide.

```
EDU» IrisFilter
Enter width of waveguide in microns > 800
Enter centre frequency of bandpass filter in GHz > 270
Enter desired bandwidth in % - max.=10% > 7
Tchebyscheff (1) or Maximally Flat (2) > 2

note =
Attenuation as a function of filter order n is presented for w/wa=1.5.
wa is the angular frequency point on the low-pass prototype roll-off
corresponding to the ripple level (tcheb.) or 3dB point (max. flat).

note =
Attenuation as a function of order n = 1 to 10

attn =
  Columns 1 through 7

   5.1188   7.8265   10.9309   14.2535   17.6838   21.1643   24.6676

  Columns 8 through 10

   28.1812   31.6994   35.2196

Enter desired filter order - n=3 requires 4 iris pairs > 3
Enter start frequency for sweep in GHz > 200
Enter finish frequency for sweep in GHz > 340
Enter step frequency for sweep in GHz > 1
```

Figure A1.2. MATLAB waveguide filter design program input for a maximally flat filter with centre frequency 270GHz, n=3 and 7% bandwidth.

Figure A1.3. MATLAB waveguide filter design program output for
a maximally flat filter with centre frequency 270GHz, n=3 and 7% bandwidth.
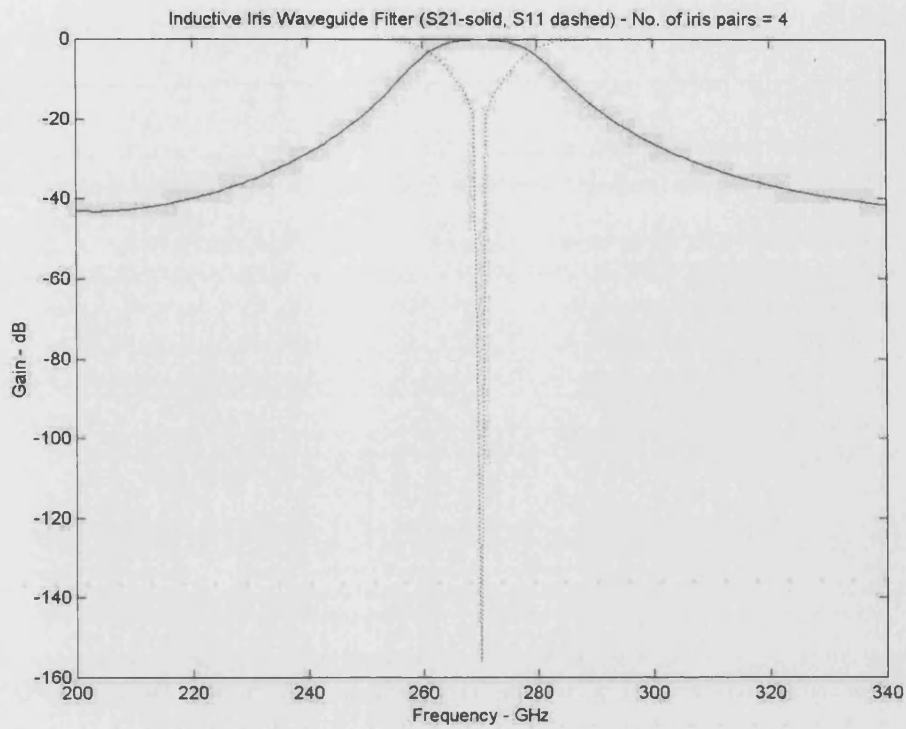
irisw =

 1.0e-003 *

  0.2040   0.2920   0.2920   0.2040

spacing =

 1.0e-003 *

   0   0.6280   0.6974   0.6280

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Networks and Coupling Structures, McGraw-Hill, 1964, pp. 450-459.

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Appendix Two – RF test fixture.

Part A:
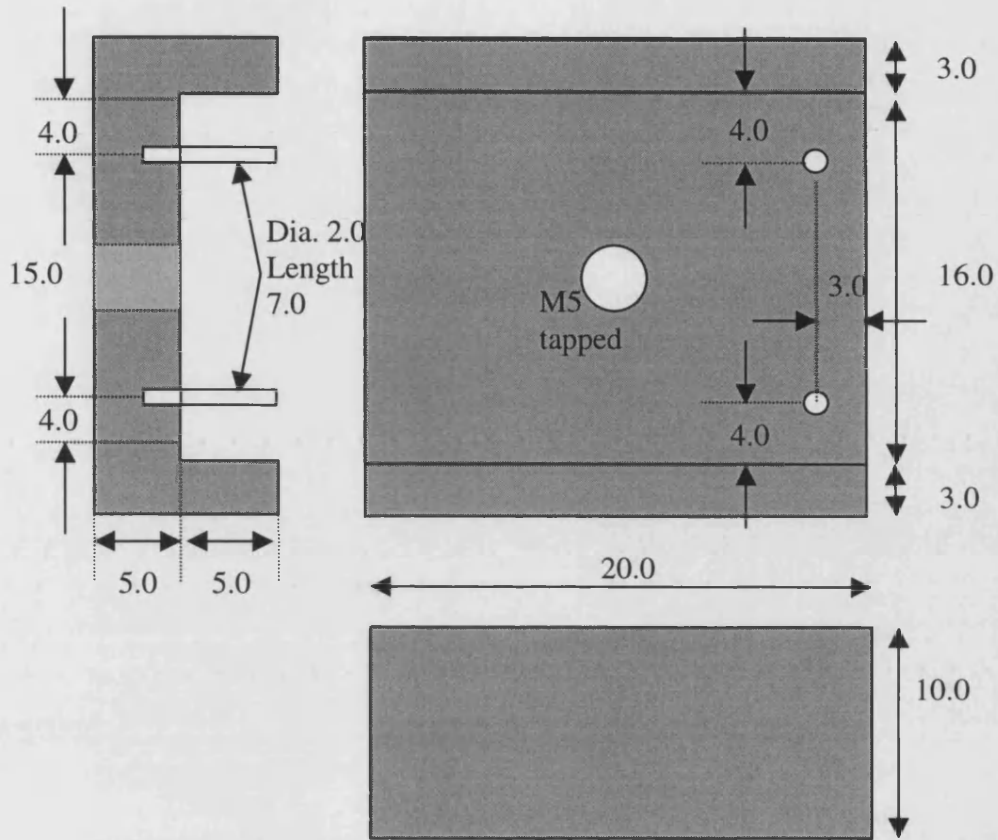
Part B:

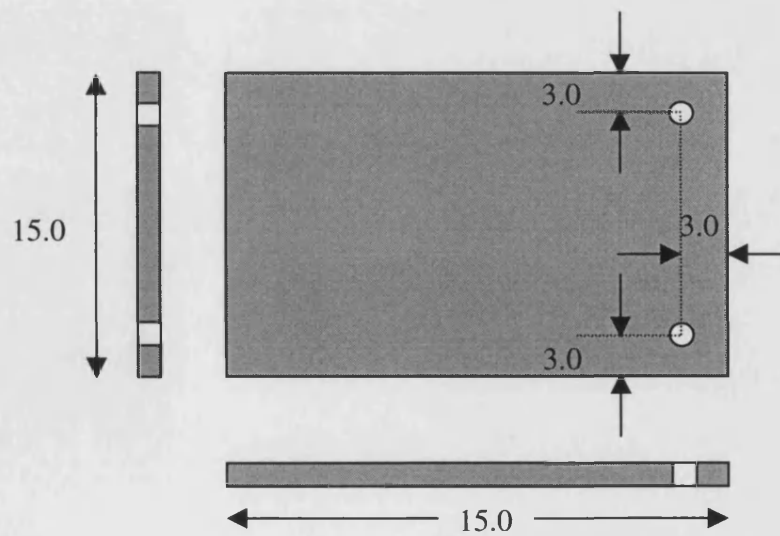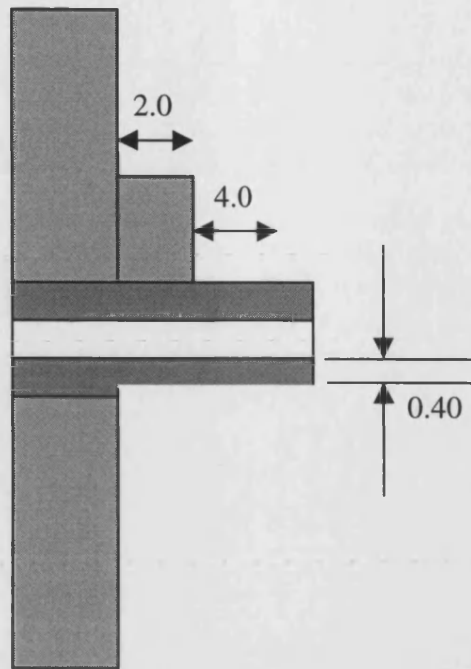Figure A2.1. Construction drawings for machined brass test fixture.

WG29 Flange (UG387/U) – Two required.

Assembled RF test fixture (side view)

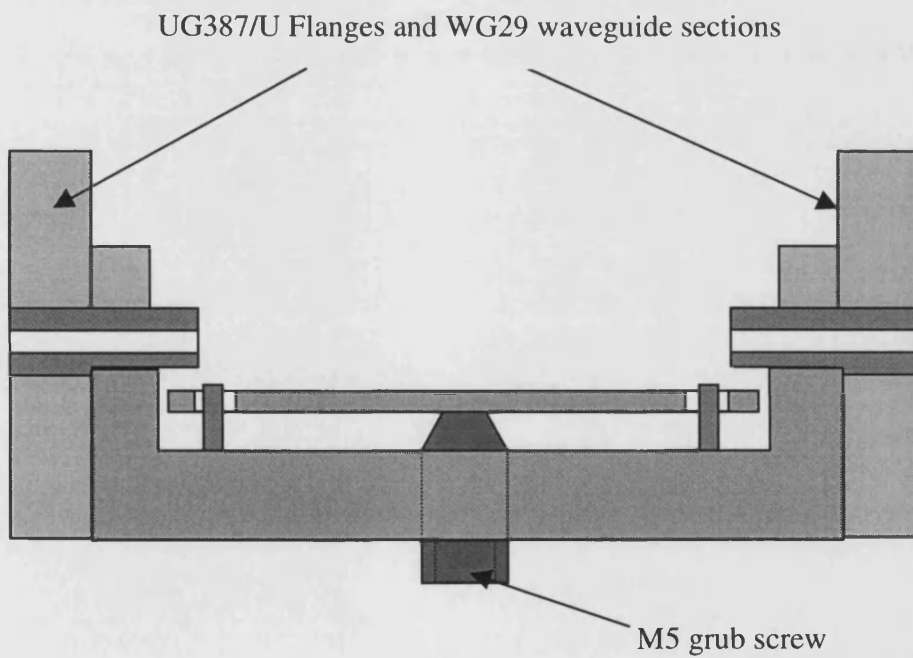UG387/U Flanges and WG29 waveguide sections

M5 grub screw

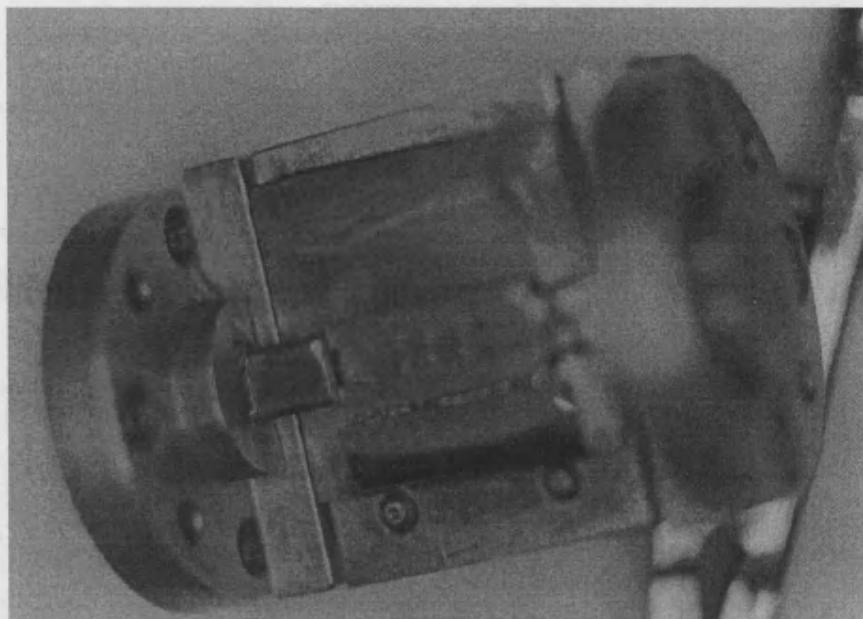Figure A2.1 continued. Construction drawings for machined brass test fixture.

Figure A2.2. Test mount and coupled resonator filter (minus lid) angled to show alignment between conventional and SU8 waveguides.

Appendix Three – Plating Solutions.

A3.1 Copper and nickel electroplating

Copper Sulphate solution

This solution offers fine grain plating and a low-stress deposit. Primary application was in electroplating the AZ4562 photoresist former for the doubler structure found in section 4.11. This solution was also adopted for much of the work conducted on sacrificial etching [sections 4.13, 5.4].

Composition

Copper sulphate	200g
Sulphuric Acid	50g
De-ionised water	1.0L

Operating conditions

Current density $20mA/cm^2$, solution temperature 50-60°C, strong agitation, anode area greater than ten times cathode area.

Nickel Sulphamate solution

Plated Nickel using this electrolyte has a smoother, brighter finish than obtained from nickel sulphate solutions. In-built stress is similar for nickel deposits from sulphate and sulphamate based plating. Detector formers [section 4.12] and SU8 straight waveguides [5.3] were finished using the following solution.

Composition

Nickel Sulphamate	320g
Boric Acid	27g
De-ionised water	1.0L

Operating conditions

Current density $5mA/cm^2$, solution temperature 40-50°C, strong agitation, anode area greater than ten times cathode area.

A3.2   Platinum plating solutions

As applied to diode plating [sections 4.6 and 5.1]

Engelhard GP platinum solution EC3749, (4g/L)

Composition as supplied.

Operating conditions:

Current density 65 pA/ μm^2 (DC plating), 0.5 nA/ μm^2 (10mS-on / 20mS-off pulsed plating), solution temperature 45-50°C, strong agitation, anode area greater than 100 times cathode area.

Engelhard GP platinum solution EC3741, (10g/L)

Composition as supplied.

Operating conditions:

Current density 130 pA/ μm^2 (DC plating), 1 nA/ μm^2 (10mS-on / 20mS-off pulsed plating), solution temperature 45-50°C, strong agitation, anode area greater 100 times cathode area.

Platanex platinum plating solution (10g/L)

Composition (for 250mL):

B unit	175mL
R unit	50mL
De-ionised water	25mL

Operating conditions:

Current density 200 pA/μm^2 (DC plating), 2.0 nA/ μm^2 (10mS-on / 20mS-off pulsed plating), solution temperature 80°C, strong agitation, anode area greater than 100 times cathode area.

Platanex low-stress solution

Composition (for 250mL)

R unit	50mL
Sulphamic acid	25g
De-ionised water	200mL

Operating conditions.

Current density 2 nA/μm^2 (10mS-on / 20mS-off pulsed plating), solution temperature 60°C, strong agitation, anode area greater than 100 times cathode area.

A3.3 Electroless plating

Macor (supplied by RS) ceramic substrates were used to avoid contamination. Pyrex glass vessels were employed and heated from a hot-plate with agitation supplied from an in-built stirrer.

Engelhard Metex 230 electroless gold plating solution.

Composition as supplied.

Operating conditions:

Solution temperature - 75°C, moderate agitation, volume 50ml (sample area 2cm^2).

Seed layers: Acheson Electrodag 1415M (airbrushed), Caswell electroless nickel plating.

Engelhard Metex 850 electroless gold plating solution.

Composition:

> 50% A : 50% B (manufacturer's recommendation).

Operating conditions:

Solution temperature - 75°C, moderate agitation, volume 100ml (sample area 2cm^2).

Seed layers: Metex 230, Caswell electroless nickel plating.

Caswell electroless nickel solution.

Composition:

> 5% A: 15% B: 80% DI water (as stipulated in accompanying literature).

Operating conditions:

Solution temperature - 85°C, moderate agitation, volume 100ml (sample area 2cm^2).

Seed layer: Acheson Electrodag 1415M (airbrushed), evaporated Palladium.