An investigation of the microwave properties of resonant tunnelling devices

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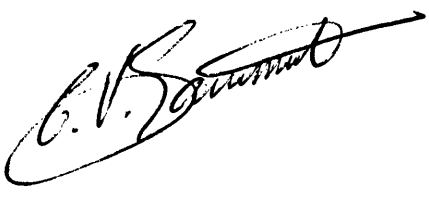

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To my wife

Mary Rose

and sons

Neil and **Keith.**

They have endured so much for the sake of Science!

ABSTRACT

This thesis presents a study of the microwave properties of resonant tunnelling devices.

Low frequency stability is considered as this affects device applicability potential. It is shown that bias circuit instabilities can be simulated assuming a simplified model and that the simulated effects can account for observed features in the dc current-voltage characteristics.

Small-signal reflection measurements between 45 MHz and 13 GHz were performed. The experimental results, the most accurate published to date, fitted to within less than 5% difference from those simulated using a tunnel diode equivalent circuit model with frequency-independent parameters and voltage-dependent conductance and capacitance. These measurements allowed the device capacitance to be determined over a wide voltage range. This was made possible by the use of a hitherto un-characterised microwave package and accurate de-embedding techniques based on the derivation of a lumped-element equivalent circuit for the package inside a novel 3.5 mm coaxial mount which was designed and constructed for the purpose.

Large-signal impedance measurements were also performed. The results fitted the tunnel diode model with frequency-independent parameters over narrow frequency bands.

The large-signal behaviour of resonant tunnelling devices was investigated numerically using a computer program modified to employ the experimental small-signal model as a starting point. A simple multiplier circuit was used to compare experimental results with calculations. The comparison shows that accurate large-signal analysis is possible with this technique.

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CHAPTER 1

RESONANT TUNNELLING DEVICES

1.1 Introduction

The first report of negative differential resistance (NDR) from a tunnelling structure was due to Esaki in 1958 [1]. In a tunnelling structure, NDR occurs when the total number of tunnelling electrons transmitted across a barrier structure per second decreases, rather than increases, with an increase in applied voltage. The negative resistance regions in the I-V characteristics themselves are not only important in solid-state electronics because of possible signal amplification, but also shed light on some fundamental aspects of tunnelling [2].

Since then, much has been achieved in the field of solid-state tunnelling structures, but the intention here is to focus on a particular class of semiconductor tunnelling structures which have become known as **resonant tunnelling devices** (RTD's). In 1969, Duke [3] predicted a new phenomenon due to quantum confinement of charge carriers. In 1973, Tsu and Esaki [4] predicted NDR in a finite superlattice as a consequence of resonant tunnelling. The first experimental results were obtained by Chang et al. [5] who demonstrated the existence of NDR regions in the I-V characteristic of a double barrier quantum well (DBQW), AlGaAs-GaAs-AlGaAs heterostructure grown by molecular beam epitaxy (MBE). Similar observations were subsequently reported [6] with an MBE-grown AlGaAs-GaAs multi-barrier quantum well (MBQW) superlattice. This epitaxial growth process was then still in its infancy. The quality of the samples grown immediately

after the pioneering work of Chang and Esaki [5,6] did not result in much improved non-linearity regions in the I/V characteristics. Indeed these works found effects only at low temperatures and even here, these were much less pronounced than expected from theory. This implicitly suggested the idea that resonant tunnelling was too critically dependent on experimental parameters to be really controllable and reproducible, let alone exploited, in actual samples with defect concentrations, surface cleanliness, actual dimensions, etc., different from the clear-cut pictures of theoretical models. As a result, interest in these structures dwindled for almost a decade.

Since then, however, the quality of epitaxial layers grown by MBE had improved considerably and in 1983, Sollner et al. reported a peak-to-valley current ratio (PVR) of 6 at low temperatures and claimed to have carried out successful detecting and mixing experiments at 2.5THz [7,8]. Almost a year later, the same group announced the observation of 18GHz oscillations from a DBRTD at temperatures of about 200K [9]. Shewchuk et al. [10] were the first to report room temperature NDR regions in the I-V characteristics of a DBRT heterostructure based on the $Al_xGa_{1-x}As$-GaAs system with a PVR of 1.5 (8) at 300K (77K).

By this time, interest in resonant tunnelling structures had rekindled, as evidenced from the vast amount of relevant literature published. Immediately after the announcement by Shewchuk et al. [10] the first observation of NDR in AlAs/GaAs DBRT heterostructures grown by metalorganic chemical vapour deposition (MOCVD) was reported [11]. Published room-temperature results on GaAs-AlGaAs MOCVD-grown resonant tunnelling structures are rare and significantly inferior to those of similar MBE structures (e.g. PVR < 1.5 and $J_p < 1 kA cm^{-2}$ [56]). For structures in the InAlAs-InGaAs material system [57] typical PVR's are about 9 times lower than for similar MBE structures. The char-

acteristics for GaAs-AlGaAs MOCVD-grown structures have been marginally improved to $J_p \approx 2 kA cm^{-2}$ and PVR's greater than 2 [58] (see chapter 2).

Until about 1985, most of the structures grown and tested had n^+-type emitters and collectors; i.e., resonant tunnelling had only been demonstrated for electrons. Mendez et al. [12] were the first to report resonant tunnelling due to holes in an AlAs-GaAs-AlAs DBQW sandwiched between p^+-GaAs regions.

By 1986, the PVR in the dc characteristics of AlAs-GaAs DBRT devices had risen to 3.5 at room temperature [13]. Huang et al. reported 3.9 at room temperature the following year for an $Al_{0.42}Ga_{0.58}As$-GaAs DBRT heterostructure [14]. There then seemed to be a consensus that the non-linearities obtainable from the AlAs-GaAs or AlGaAs-GaAs systems could not be further improved. However, the extent of NDR and peak current densities had been improved sufficiently to enable such devices to give rise to microwave oscillation at frequencies of 56GHz (60μW - fundamental) and 87GHz (18μW - second harmonic) [15,16,17] when placed in microwave cavities.

Interest was by no means confined to DB structures. NDR has been reported in a single barrier - QW device [18] in which electrons tunnel through the AlAs barrier into the GaAs QW and subsequently drift to a lateral contact. Two peaks in the I-V curve at low-temperature for a triple barrier diode were observed by Nakagawa et al. [19], while Reed et al. [20] reported resonant tunnelling in a DB structure in which the barriers had been replaced by thin short period binary superlattices of AlAs and GaAs. However, the most promising results have come from structures involving In in ternary or binary alloy systems inside or outside the QW.

The first such structure was due to Inata et al. [21]. It consisted of an InGaAs QW sandwiched between two InAlAs barriers grown by MBE on an epitaxial layer of InGaAs lattice-matched to an InP substrate. This device gave a PVR of 2.3 at room temperature and 11.7 at 77K. The first pseudomorphic structure was reported in 1987 [22]. Its structure was similar to the former but had AlAs instead of InAlAs in the barriers. The improvement was dramatic. The PVR reported for this device was 14 at 300K and 35 at 77K. However, there was yet to be a further significant improvement the following year. This was due to Broekaert et al. [23] and was another pseudomorphic heterostructure, grown by MBE, having strained AlAs barriers and a QW consisting of 3 monolayers of InGaAs cladding 6 monolayers of InAs on either side. These layers were sandwiched between InGaAs undoped spacer layers and grown on epitaxial InGaAs lattice-matched to InP as the substrate. This structure gave the best PVR to date; 30 at room temperature and 63 at 77K with a peak current density of $6kAcm^{-2}$.

The realisation that the negative resistance region in RTD characteristics is capable of providing the gain necessary for high frequency oscillations led to a series of reports of oscillations exceeding in frequency the previously reported 56GHz [15,16,17]; 200Ghz [24] and 420GHz, with a predicted maximum oscillation frequency of 1THz [25]. Various material parameters in the GaAs-AlGaAs and GaAs-AlAs material systems preclude operation at higher frequencies [25]. In this respect, the InGaAs-AlAs and similar material systems [23] were investigated in order to circumvent these problems. Other systems have been investigated, such as InAs-AlSb [59,60,61,62,63] and InSb-AlInSb [64] grown on GaAs substrates since these are more suitable for fabrication of monolithic integrated circuits. The InAs-AlSb system has proved most promising with the recent reports of 712 GHz oscillations at $0.3\mu W$ [65] from a $1.8\mu m$-diameter device.

Three-terminal devices using resonant tunnelling in various ways have also been proposed [26] and the future of such devices seems promising, even though the relative lack of literature in this area may suggest otherwise.

Considerable effort has been made towards a better understanding of the equivalent circuit of the device [27,28,29,30,31,32] and underlying processes for the frequency response [33]. It is here that this work attempts to contribute by examining the behaviour of some resonant tunnelling devices at low and microwave frequencies. The interaction of the RTD with the bias circuit is investigated in chapter 2, which analyses in detail the nature and origin of low-frequency bias circuit oscillations. Subsequent chapters tackle small- and large-signal device behaviour at microwave frequencies. In particular, chapter 5 applies numerical self-consistent methods to investigate the behaviour of RTD's as harmonic multipliers using an experimentally-based small-signal equivalent circuit model obtained as described in chapter 4.

1.2 The basic physics of resonant tunnelling

1.2.1 The tunnelling current

Let us consider a GaAs-$Al_xGa_{1-x}As$ single crystal with an abrupt interface between the two regions. The alloy $Al_xGa_{1-x}As$ has a wider bandgap than GaAs with some of this difference appearing in the conduction band. It thus acts as a barrier with height, relative to the GaAs conduction band edge, of [34]

$$\Delta E_c = 0.65(1.247x) \qquad \textbf{(1.1)}$$

where $1.247x$ is the band gap difference [35] and 0.65 is the fraction appearing in the conduction band [36] (figure 1.1).

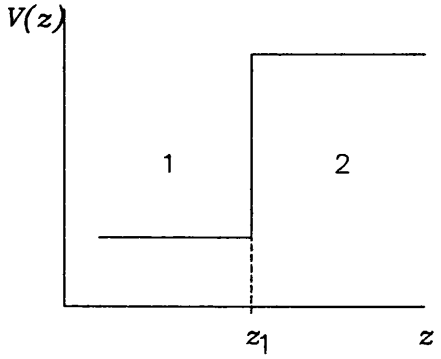

Figure 1.1. Electronic potential energy at an interface between two materials of different band gaps. The motion of an electron in material 1 is restricted along the z-direction because of a potential barrier at the junction.

The electrons on both sides of the interface move in a screened potential due to the ion cores, while interacting with each other via the Coulomb potential. The Hamiltonian of the system is complicated and is thus frequently simplified by using one electron states that take into account the periodic component of the electron-ion potential [37,38].

Since there is no electrostatic potential parallel to the interface, only a one-dimensional Schrödinger equation need be considered. Thus, in the free-electron approximation, solutions are sought to an equation of the form

$$\left[-\frac{\hbar^2}{2m}\frac{d^2}{dz^2}+V(z)-E\right]\psi_E(z) = 0 \qquad (1.2)$$

V(z) is the potential near the interface and ψ_E is an envelope function which is subject to the following conditions imposed by conservation of particle flux at any interface

$$\psi_E(z_1^-) = \psi_E(z_1^+) \qquad (1.3)$$

$$\left.\frac{1}{m_1}\frac{d\psi_E}{dz}\right|_{z_1^-} = \left.\frac{1}{m_2}\frac{d\psi_E}{dz}\right|_{z_1^+} \qquad (1.4)$$

where z_1^- and z_1^+ refer to positions to the left and to the right of z_1 respectively, and m_1 and m_2 are the electron effective masses in regions 1 and 2.

Let us now consider a potential barrier of finite width. The velocity of an incident electron associated with a state of wave number k_z is $\frac{1}{\hbar}\partial E/\partial k_z$ in a one-particle approximation. Thus, for zero external electric field, the current per unit area J can be written as

$$J = \frac{2e}{(2\pi)^3\hbar}\int\int\int dk_x dk_y dk_z f(E)\tau(E_z)\left(\frac{\partial E}{\partial k_z}\right) \qquad (1.5)$$

where $f(E)$ is the Fermi-Dirac distribution and $\tau(E_z)$ is the tunnelling probability, defined as the ratio between the incident and transmitted currents. The factor $2/(2\pi)^3$ arises from the fact that the volume of a state occupied by two electrons of opposite spin is $(2\pi)^3$ in wave vector space for a crystal of unit volume.

If an external bias V is applied across the barrier, J will have two contributions; J_{lr} and J_{rl}, the currents from left to right and from right to left, respectively, across the barrier. The energy of the transmitted electron will now be $E+eV$ such that

$$J_{lr} = \frac{e}{4\pi^3\hbar}\int\int\int dk_x dk_y dE_z f(E)[1-f(E+eV)]\tau(E_z) \qquad (1.6)$$

$$J_{rl} = \frac{e}{4\pi^3\hbar}\int\int\int dk_x dk_y dE_z f(E+eV)[1-f(E)]\tau(E_z) \qquad (1.7)$$

The net current is thus the difference between **(1.6)** and **(1.7)**;

$$J = \frac{e}{4\pi^3\hbar}\int\int\int dk_x dk_y dE_z[f(E)-f(E+eV)]\tau(E_z) \qquad (1.8)$$

The zero-temperature limit for the free-electron approximation gives [39]

$$dk_x dk_y = \frac{2\pi m}{\hbar^2} dE_{\parallel} \qquad (1.9)$$

where $E_{\parallel}$ is the electron energy component parallel to the interface. Hence, the tunnelling current can be written as [39]

$$J = \frac{em}{2\pi^2\hbar^3}\left[eV\int_0^{E_F-eV} dE_z\tau(E_z)+\int_{E_F-eV}^{E_F} dE_z(E_F-E_z)\tau(E_z)\right] \quad \text{for } eV \le E_F \qquad (1.10)$$

$$J = \frac{em}{2\pi^2\hbar^3}\int_0^{E_F} dE_z(E_F-E_z)\tau(E_z) \quad \text{for } eV \ge E_F \qquad (1.11)$$

Equations **(1.10)** and **(1.11)** can be evaluated provided that $\tau(E_z)$ is known.

1.2.2 The tunnelling probability

The tunnelling probability is determined by solving Schrödinger's equation. Analytical solutions can only be obtained for a few barrier profiles such as the one in figure 1.2 (a). This profile can serve as a first approximation to the situation of a thin, undoped, semiconductor sandwiched between two thick layers of degenerately doped semiconductors of lower energy gap (e.g. GaAs-AlGaAs-GaAs heterostructure).

If an external voltage V_A is applied across the doped regions, the barrier shifts as shown qualitatively in figure 1.2 (b) and will become essentially triangular when the applied voltage V_B is such that $eV_B > \Delta E_c$ (figure 1.2 (c)).

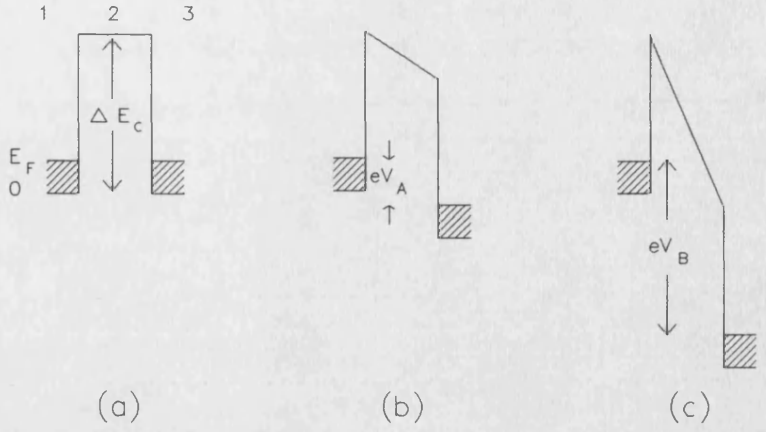

Figure 1.2. Rectangular potential model representing two regions of degenerately doped semiconductor with an interposed region of undoped material of higher band gap, (a) with no externally applied voltage, (b) and (c) with an external applied voltage V_A and V_B, respectively.

In the case of the rectangular barrier, the solution of **(1.2)** is expressed in terms of plane waves in regions 1 and 3 (figure 1.2 (a)). In region 2, ψ_E can be written as a linear combination of the Airy functions $Ai(z)$ and $Bi(z)$ [34,39,40]. By matching the wave functions and their derivatives divided by the respective effective masses in the three regions (i.e., applying the boundary conditions **(1.3)** and **(1.4)**), the relative amplitudes of the incident and transmitted waves are determined, from which τ may be calculated.

1.2.2.1 The transfer-matrix method

If, for simplicity, we assume the potential V(z) to be constant in a given region, the general solution of **(1.2)** has the form of a linear combination of waves propagating normal to the interface;

$$\psi_E = A\exp(jkz)+B\exp(-jkz) \qquad \textbf{(1.12)}$$

with

$$E - V = \frac{\hbar^2 k^2}{2m} \qquad \textbf{(1.13)}$$

When $E-V>0$, k is real and the wave functions are plane waves. When $E-V<0$, k is imaginary and the wave functions are exponentially growing and decaying waves. Thus the overall wave function for the potential step in figure 1.1 has a plane-wave form for $z<z_1$ (for electron energies such that $E-V>0$) and an exponentially decaying wave form for $z>z_1$ ($E-V<0$). The coefficients A and B in **(1.12)** are determined from the boundary conditions **(1.3)** and **(1.4)** for $z = z_1$:

$$A_1\exp(jk_1z_1)+B_1\exp(-jk_1z_1) = A_2\exp(jk_2z_1)+B_2\exp(-jk_2z_1) \qquad \textbf{(1.14)}$$

$$\frac{k_1}{m_1}\{A_1\exp(jk_1z_1)-B_1\exp(-jk_1z_1)\} = \frac{k_2}{m_2}\{A_2\exp(jk_2z_1)-B_2\exp(-jk_2z_1)\} \qquad \textbf{(1.15)}$$

A_1 and B_1 can be related to A_2 and B_2 by means of a matrix M such that

$$\begin{pmatrix} A_1 \\ B_1 \end{pmatrix} = \mathbf{M}\cdot\begin{pmatrix} A_2 \\ B_2 \end{pmatrix} \qquad \textbf{(1.16)}$$

where M is given by

$$\mathbf{M} = \frac{1}{2k_1m_2}\begin{pmatrix} (k_1m_2+k_2m_1)\exp[j(k_2-k_1)z_1] & (k_1m_2-k_2m_1)\exp[-j(k_2+k_1)z_1] \\ (k_1m_2-k_2m_1)\exp[j(k_2+k_1)z_1] & (k_1m_2+k_2m_1)\exp[-j(k_2-k_1)z_1] \end{pmatrix} \qquad \textbf{(1.17)}$$

Now, for the general case of n regions (figure 1.3) with corresponding potentials V_i and effective masses m_i (i = 1, 2, ..., n), separated by $n-1$ interfaces at positions z_i (i = 1, 2, ..., n), the wave functions at the extreme left hand region 1 and the extreme right hand region n are linked by [41]

$$\begin{pmatrix} A_1 \\ B_1 \end{pmatrix} = \prod_1^{n-1}\{\mathbf{M}_i\}\cdot\begin{pmatrix} A_n \\ B_n \end{pmatrix} \qquad \textbf{(1.18)}$$

The elements of M are, from **(1.17)**,

$$M_i|_{11} = \left(\frac{k_i m_{i+1} + k_{i+1} m_i}{2k_i m_{i+1}}\right)\exp[j(k_{i+1} - k_i)z_i] \qquad \textbf{(1.19)}$$

$$M_i|_{12} = \left(\frac{k_i m_{i+1} - k_{i+1} m_i}{2k_i m_{i+1}}\right)\exp[-j(k_{i+1} + k_i)z_i] \qquad \textbf{(1.20)}$$

$$M_i|_{21} = \left(\frac{k_i m_{i+1} - k_{i+1} m_i}{2k_i m_{i+1}}\right)\exp[j(k_{i+1} + k_i)z_i] \qquad \textbf{(1.21)}$$

$$M_i|_{22} = \left(\frac{k_i m_{i+1} + k_{i+1} m_i}{2k_i m_{i+1}}\right)\exp[-j(k_{i+1} - k_i)z_i] \qquad \textbf{(1.22)}$$

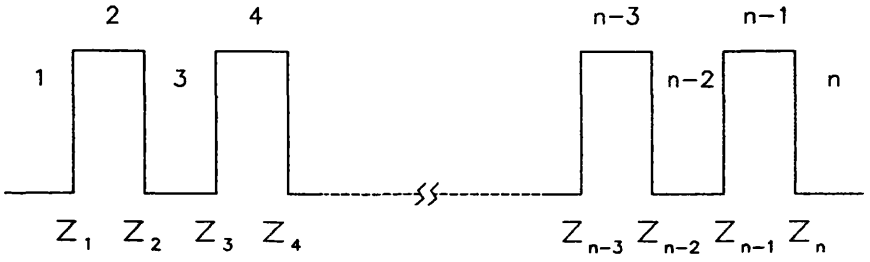

Figure 1.3. Potential energy profile for a heterostructure consisting of n rectangular regions separated by n-1 interfaces at z_i (i = 1, 2, ..., n). The electron effective masses in the respective regions are m_i (i = 1, 2, ..., n) and the potentials are V_i (i = 1, 2, ..., n).

Now, if an electron is incident on interface 1 from region 1, then B_n=0 since there will be no reflected wave in this region, and the transmission probability will be given by [39]

$$\tau = \frac{k_1 m_n |A_n|^2}{k_n m_1 |A_n|^2} \qquad \textbf{(1.23)}$$

An analytical expression for $\tau(E_z)$ may be obtained by this method [41] for the case of rectangular-barrier potential energy profiles. A typical result is shown in figure 1.4 for a symmetrical double-barrier of height 0.3 eV. The

barrier widths are 5 nm while the QW width is 6 nm. The electron effective mass was assumed to be $0.1m_0$ in the barrier regions and $0.067m_0$ in the QW [39]. At certain energies below the barrier height (E_0 and E_1), electrons incident on the left barrier can appear on the right without attenuation. This situation corresponds to constructive interference between the two plane waves coexisting in the QW. These energies are the eigen-energies of the QW (since the solutions of Schrödinger's equation in this region are standing waves). This phenomenon is called **resonant tunnelling**.

It also appears from figure 1.4 that for electron energies above the barrier, the transmission probability also reaches unity for certain values where the interference is again constructive. Such levels are often referred to as **virtual states** and the $\tau(E_z)$ peaks corresponding to these are much broader than those corresponding to **quasi-bound states** below the barrier height.

In practice, the transmission probability does not reach unity. This is mainly because the barriers are not identical. Indeed, even if they were, application of an electric field across the structure distorts the potential profile and hence destroys symmetry [42]. However, it is possible to apply the transfer-matrix technique to arbitrarily-shaped profiles by approximating them by rectangular steps of arbitrarily small width. The exact tunnelling probability may then be approached as closely as desired by chosing the appropriate step width [39].

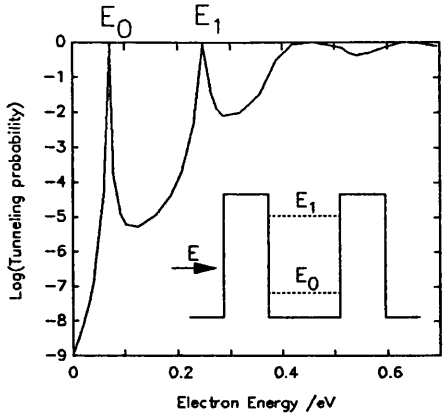

Figure 1.4. Tunnelling probability as a function of energy for a double rectangular barrier with 50Å barriers and a 60Å QW (Ref. [39]). Barrier heights are 0.3eV. The electron effective mass in the barrier regions is taken as $0.1m_o$, and $0.067m_o$ in the QW region. The sharp peaks below 0.3eV are due to resonant tunnelling via the quasi-bound states of the QW corresponding to energies E_o and E_1. The broader transmission maxima above the barrier height are due to tunnelling via virtual states above the QW.

1.3 Resonant tunnelling versus sequential tunnelling

Let us consider a typical model of an $Al_xGa_{1-x}As$-GaAs-$Al_xGa_{1-x}As$ heterostructure with individual layers 30Å - 80Å thick, clad between two thick layers of n^+-GaAs. The potential energy profile of such a structure is represented schematically in figure 1.5. The degenerately-doped GaAs cladding layers act as reservoirs of electrons while the AlGaAs regions serve as barriers to the motion of electrons from one reservoir to the other.

At a small voltage bias applied across the barriers, the tunnelling probability is small and thus also the current between the electrodes. When the bias V_b is such that the energy E_0 of the ground state is in the range of energies available from the left electrode, resonant tunnelling occurs

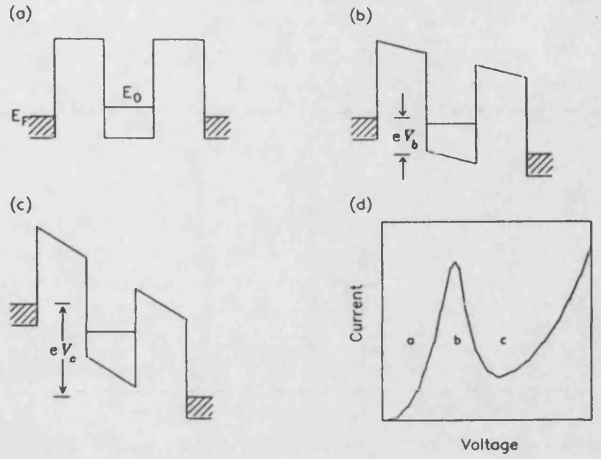

Figure 1.5. Rectangular double barrier potential energy profile for an $Al_xGa_{1-x}As$-GaAs-$Al_xGa_{1-x}As$ heterostructure between two layers of degenerately-doped GaAs with (a) zero voltage bias, (b) V_b, and (c) V_c, applied across the structure. When the applied bias is such that the energy of the quasi-bound state in the QW is within the Fermi energy of the left electrode, resonant tunnelling occurs and the I-V characteristic (d) shows a peak. As the quasi-bound state energy crosses the conduction band minimum of the left electrode the current drops drastically because conservation of momentum parallel to the interfaces is no longer possible.

and the current increases to a relatively high value. As the bias is increased to V_c, E_0 falls below the conduction band minimum at the left electrode. Here, resonant tunnelling is no longer possible because further tunnelling would violate conservation of momentum parallel to the interfaces (the electrons tunnel from a three-dimensional to a two dimensional system of electronic states). Thus the current through the structure drops drastically. At even higher bias the second barrier effectively becomes triangular and eventually disappears. The current increases at first by Fowler-Nordheim tunnelling through the right-hand triangular barrier. As this barrier is progressively lowered by the increasing voltage bias, the current increases even further

as now the electrons have only to tunnel through the first barrier to find an increased availability of unoccupied states on the other side with no reduced dimensionality.

The number of negative resistance features on the I-V characteristic depends only on the width of the QW; for narrow wells (up to about 50Å) only the ground state is quasi-bound and this gives rise to a single NDR feature.

The resonant tunnelling process assumes phase coherence across the barrier structure for the wave functions that represent the electrons in these adjacent regions. This, as has been mentioned previously, leads to physically observable negative resistance effects. In actual resonant tunnelling heterostructures, scattering effects are unavoidable. This is seen as the main reason why the peak-to-valley ratio in the NDR region decreases drastically as the device temperature approaches 300K.

One of the effects of inelastic scattering on tunnelling resonances is the decrease in the peak transmission probability [43]. If phase coherence is completely lost because of this underlying process, then it is no longer justifiable to refer to any residual NDR as due to resonant tunnelling. Luryi [44,45] demonstrated that for negative resistance to occur, the necessary and sufficient element is a QW and therefore the second barrier can be infinitely wide [18]. In such extreme situations, the proper term to describe the physical processes leading to negative resistance effects is **sequential**, **non-resonant**, or **incoherent** tunnelling [44,45].

Since the barriers considered here are of finite width, the states in the QW region are **quasi-bound**, since a particle localised in the well at a time $t = 0$ can tunnel out of it. The lifetime associated with such states is related to the tunnelling probability near resonance, and, by the uncertainty principle, to the width of the resonant state. The

resonant tunnelling process may be visualised as starting with a wavepacket incident on the left of a barrier structure similar to the one in figure 1.5. If the energy distribution of the packet is peaked at one of the eigen-energies of the QW, the waves are trapped in the well which now acts as an electronic equivalent to a Fabri-Pérot resonator with the waves reflecting back and forth between the barriers with such a phase as to continually reinforce themselves and leaking out slowly. Hence, resonant tunnelling is a 'slow' process. The average time τ_{trans} taken by an electron to leak out of the QW is related to the tunnelling probability and to the average number of times it strikes the barrier per second. It may be shown that τ_{trans} is related to the width of the resonant state ΔE by [39]

$$\tau_{trans}\Delta E \approx 2\pi\hbar \qquad \textbf{(1.24)}$$

in accordance with the uncertainty principle.

Since the resonant tunnelling process requires the build-up of the wave function in the QW region, the process leads to the accumulation of electric charge in the well (this will, in turn, modify the potential energy profile and further complicate calculations of the tunnelling probability; a realisation which has prompted self-consistent calculations of $\tau(E_z)$ [46,47]).

Because of the exponential nature of the tunnelling probability off resonance, a small increase of the barrier width drastically increases the transit time τ_{trans} (similar effects are observed by increasing barrier heights or electron effective masses). Now, the material parameter that determines whether resonant or sequential tunnelling dominates is the barrier width. If this is small then the transit time τ_{trans} is bound to be smaller than the scattering time τ_s and resonant tunnelling may be the dominant mechanism leading to negative resistance. In the other extreme of thick barriers, $\tau_{trans} \gg \tau_s$, and sequential tunnelling takes

over [48]. However, the techniques of section 1.2 are equally applicable to both mechanisms [49]. The basic difference is that the tunnelling probability near 'resonance' will be of order unity in the resonant tunnelling limit and of the order of the tunnelling probability through a single barrier [50] in the other (sequential tunnelling).

1.4 Equivalent circuit models

Estimates of the frequency limit of resonant tunnelling devices for potential application as detectors, oscillators and high frequency switching devices centres on the synthesis of equivalent circuit models of the RTD. The early models were based on the equivalent circuit of a tunnel diode [51] (figure 2.16) with $-G_d$ representing the NDC, C_d the device capacitance and R_s the device series resistance.

Luryi [44] considered the charge buildup inside the quantum well as being due to tunnelling through a single barrier. He proceeded to obtain an expression for the tunnel resistance per unit area by assuming a WKB approximation for the tunnelling current and subsequently obtained an RC time constant of 40ps, which implied a frequency limit of about 4GHz. This was in sharp contrast to more recent work [17] that dismisses the WKB approximation as inappropriate for estimation of tunnelling times.

Coleman et al. [27] noted that experimental studies [7,8,9] suggested that the equivalent circuit of a DBRTD has a different configuration to the Esaki tunnel diode. They proposed the circuit of figure 1.6 with R_s ($<\sim 1\Omega$) accounting for metal contact resistance plus the loss in the n-GaAs cladding layers, $-G(V)$ represented the NDC associated with

the double-barrier-QW, C the 'quantum capacitor' (similar in essence to Luryi's [44]), and R being a resistance which avoids shunting $-G$ through C at high frequencies[1].

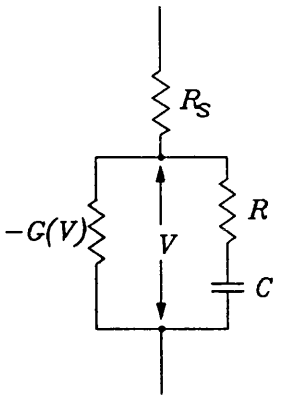

Figure 1.6. Equivalent circuit proposed by Coleman et al. [27]. The NDC is represented by $-G(V)$, while R_s and C are respectively the series resistance and device capacitance. R was introduced empirically to explain high-frequency detection experiments.

Jogai and Wang [52] suggested an alternative explanation for the high oscillation and detection frequencies, and proposed an equivalent circuit (figure 1.7) from which the oscillation frequency was estimated on the basis of the magnitude of the NDR. They showed that the measured maximum amplification frequency may be much lower than that expected from the electron transit time. In their model, Jogai and Wang assumed R to represent the ideal NDR, which need not be due to coherent tunnelling, C the total capacitance of barrier and well regions, R_s the series resistance, and introduced a new resistive element, R_p, representing the excess currents caused by leakage processes. The effect of these excess currents is to lower the oscillation frequency by smearing out the NDR. They explained Sollner et al.'s

1 This was necessary in order to explain Sollner's [7] detector experiments, i.e. to allow the nonlinear properties of $-G$ to persist up to THz frequencies.

detection at 2.5THz as being due to the frequency-independence of the second derivative of the terminal current as long as R_s was small and providing the NDR is not degraded at high frequencies.

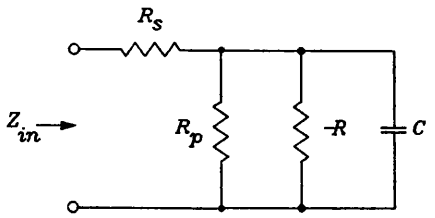

Figure 1.7. RTD equivalent circuit due to Jogai and Wang (Ref. [52]). R is a non-linear resistance representing the resonant tunnelling current, R_p represents the leakage currents, R_s is the substrate and contact resistance and C is the capacitance of the well and barrier regions.

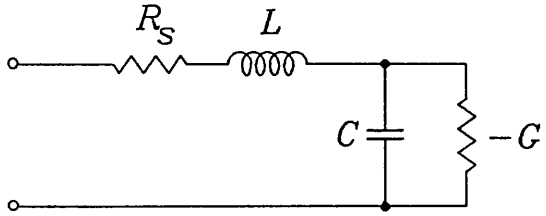

Figure 1.8. Equivalent circuit due to Gering et al. [28,53]. The circuit elements G, C and R_s have the usual reference, while L (=0.89nH [53]) is a series inductance found necessary to explain a series resonance identified at about 3GHz in their microwave impedance measurements.

Microwave impedance measurements on a DBRTD by Gering et al. [28] revealed a series resonance at approximately 3GHz. This prompted the group to postulate the presence of an inductive element L in the equivalent circuit as shown in figure 1.8. The most probable source of the inductive effect was seen to be a phase shift in the ac current associated with the storage time of electrons in the QW before tunnelling out. This effect could not, however, be explained quantitatively on the basis of theory and they were only able to suggest an empirical form for L. They noted that L should not affect the resistive cutoff frequency of the device but merely the reactive loading required to enable oscillation.

Frensley [29] had predicted that the imaginary part of the admittance is negative and proportional to frequency at lower frequencies and that, therefore, this resembled an inductance. However his inductance is several orders of magnitude smaller than the series inductance of Gering et al.. His calculations also revealed that NDC should persist to 5THz, although parasitic circuit elements limit the maximum oscillation frequency to a lower value. Similar inductive behaviour was predicted from an independent-electron solution to the time-dependent Schrödinger equation [53].

In subsequent work [54], Gering et al. gathered more experimental evidence in support of their series inductive element from studies of a RTD used as a microwave detector. They showed that the detector rectified current can be accurately predicted on the basis of their small-signal equivalent circuit. They also concluded that a RTD biased at its resonant peak would be an inherently better detector than a conventional Schottky barrier diode since the former implements full-wave rectification of an incident signal as opposed to the latter's half-wave rectification.

Recently, Brown et al. [55] have attempted to incorporate the physical effect of a finite quasi-bound state lifetime into an equivalent circuit model by analysing the response of a DBRT structure to a time-varying potential of the form of an abrupt voltage step ΔV. A finite time interval elapses before the wave function reaches its final steady-state form at a bias of $V_B+\Delta V$. The associated current through the device was assumed to be governed by this time interval τ_N (being the lifetime of the Nth quasi-bound state) acting as an exponential time constant. The small-signal admittance $y(\omega)$ of the active region was obtained as

$$y(\omega) = \frac{g}{1+j\omega\tau_N} \qquad (1.25)$$

where g is the differential small-signal conductance. From **(1.25)**, the small-signal impedance $z(\omega)$ is $1/g + j\omega\tau_N/g$, and therefore a tunnelling inductance may be defined as $l = \tau_N/g$.

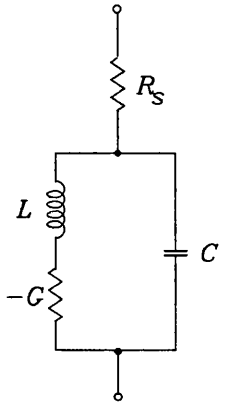

Figure 1.9. Lumped-element equivalent circuit model of a RTD due to Brown et al. [55]. G is the differential conductance, L is the inductance introduced to describe the effects of a finite quasi-bound state lifetime τ_N such that $L = \tau_N/G$, C is the device capacitance and R_s is the series resistance.

The equivalent circuit of Brown et al. was completed by assuming the usual series resistance R_s due to ohmic losses outside of the barrier regions and a capacitance $c = \epsilon A/w$ (**A**=device area, **w**=thickness of the device), which represents the physical effect of the displacement current induced across the structure by the time-varying current. c, g and l were then scaled appropriately to include the additional potential drop outside of the double-brarrier region to obtain C, G and L respectively, as shown in figure 1.9. From this circuit the maximum oscillation frequency is given by

$$f_{max} = \frac{1}{2\pi}\left\{\left[\frac{1}{LC}\left(1-\frac{C}{2LG^2}\right)\right]\left[1-\left(1-\frac{(GR_s+1)/GR_s}{(C/2LG^2-1)^2}\right)^{1/2}\right]\right\}^{1/2} \qquad \textbf{(1.26)}$$

In the limit as $L \to 0$ (or equivalently $\tau_N \to 0$), the equivalent circuit reverts to the earlier form of a single pole RC-model (figure 2.16), where f_{max} is given by equation **(2.3)** of chapter 2.

The oscillator power output was calculated on the basis of an assumption of a sinusoidal voltage waveform $v_0(t) = A\sin(\omega_0 t)$ across the device active region. This enabled expression of the large-signal conductance as

$$G_A = \frac{2}{AT}\int_0^T i_0(t)\sin(\omega_0 t)dt \qquad \textbf{(1.27)}$$

where A and T are the signal amplitude and period respectively and i_0 is the device current. R_s and C were assumed to remain unchanged under large-signal conditions whilst the inductance becomes $L_A = \tau_N / G_A$.

The power delivered to a load under steady-state conditions was then calculated as

$$P_L = -\frac{1}{2}\frac{A^2 \Re(Z_D)}{|R_s - Z_D|^2} \qquad \textbf{(1.28)}$$

where Z_D is the device large-signal impedance. Equation **(1.28)** was used to obtain estimates of the maximum oscillation power for an AlGaAs-GaAs-AlGaAs DBRTD and compare these with experimental results. The agreement was qualitatively quite good and showed a marked improvement in the prediction accuracy of the cutoff frequency over the previous RC-model, at least up to about 50GHz. Indeed, in a more recent work [25] improved accuracy in the prediction of f_{max} has been shown to be obtainable up to higher frequencies of ~450GHz and possibly above by taking into account the frequency-dependence of R_s via the skin effect and using an improved estimate of C which includes the effects of the accumulation and depletion regions outside the QW and charge accumulation within the QW at resonance. It now seems that the oscillation

frequency limit is primarily determined by the series resistance while the magnitude of the NDC determines the maximum output power, although the two effects are not independent.

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CHAPTER 2

DC CHARACTERISATION AND BIAS CIRCUIT INSTABILITY

2.1 Introduction

For a negative conductance device the potential capabilities as an active element in a microwave oscillator circuit may be tentatively assessed by considering two parameters; the maximum frequency of operation and the maximum radio frequency (rf) power output. However, the biasing circuit may effect both.

Using a simple equivalent circuit model for a resonant tunnelling device it is possible to analyse the circuit behaviour when the device is biased in different regions of its dc current-voltage (I-V) characteristic. Dc characterisation is therefore important as the results give clear indications of the suitability or otherwise of these negative conductance devices as potential active microwave circuit elements and the problems such applications are likely to encounter. Moreover, the experimental data thus obtained can be used to construct empirical equivalent circuit models for RTD's which form the basis of small- and large-signal analysis, as will be described here and in chapters 4 and 5.

This chapter starts by describing some of the double barrier resonant tunnelling structures (DBRTD's) tested and their subsequent dc characteristics. The experimental I-V curves shown here were determined using the dc characterisation station described in Appendix I.

The rest of the chapter is concerned with dc instability inherent with most of the tested devices. The recent controversy about the nature of hysteresis and bistability in the dc I-V characteristics of DBRTD's is discussed. Time-domain numerical simulations reported here will show that it is possible to explain this phenomenon on the basis of device-circuit interaction.

The necessary criteria for low frequency stability are derived and experimental observations of bias circuit oscillation are explained in detail and compared with the numerical simulations.

The final section discusses the influence of dc stabilisation on the rf power generation capabilities of RTD's.

2.2 The tested devices

This section is concerned with describing the structures of the devices tested and some results obtained from their dc characterisation.

Section 2.2.1 describes structures and dc characterisation results obtained from some MBE-grown heterostructures while section 2.2.2 is concerned with the evaluation of some structures grown by MOCVD.

2.2.1 The MBE devices

Three of the MBE structures tested were grown at Philips Research Laboratories (PRL), Redhill, Surrey. The fourth was provided by DRA (formerly RSRE), Malvern. The devices were code named as follows:

PRL devices	**G294**
	MV1484
	M269

DRA devices GWS160

All the wafer samples had Ni/Ge/Au top and bottom ohmic contacts. Devices were defined as mesas by wet chemical etching. The latest batch of M269 devices were, however, plasma-etched.

Growth schedules for the G294 wafer are not available, thus the exact details of the structure are not known. The $Al_xGa_{1-x}As$ barriers have $x = 0.67$, and they, along with the GaAs quantum well (QW) were not intentionally doped. It is not known whether undoped spacer layers have been incorporated into this structure.

Figure 2.1 shows some typical I-V characteristics of a G294 $200 \times 200 \mu m^2$ device at different temperatures. No room temperature NDC was observed with these devices. As can be expected, the peak-to-valley current ratio (PVR) decreases with increasing temperature. The valley voltage shifts to lower values with increasing temperature, as does the peak voltage. The peak current was also observed to increase significantly with temperature, an effect which was not seen in the characteristics of other devices. The low peak current density of this device ($\sim 3 A cm^{-2}$) as well as the low peak voltage of $\sim(\pm)0.2V$ seem to suggest wide (in excess of about 50 Å) barriers and QW region. The strong temperature dependence of the valley current is the cause of the lack of NDR features at room temperature. This is probably due to scattering from interface roughness, impurities present during growth, and/or Si migration into the nominally undoped regions.

The discontinuities at 0.10V are due to changes in the source resistance as the range of the voltage calibrator changes. This effect was identified and eliminated in subsequent measurements by constraining the voltage calibrator to operate on the range with the lowest resistance.

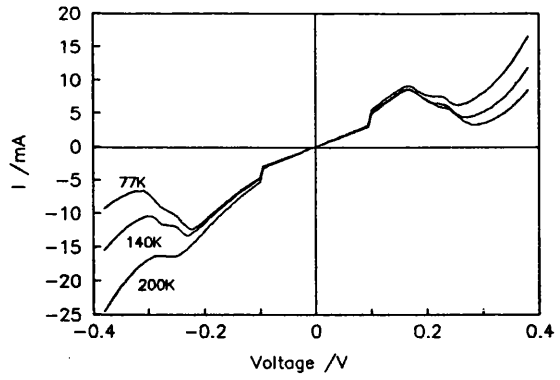


Figure 2.1. I-V characteristics at different temperatures for a device from wafer G294. The discontinuities at 0.10V are due to changes in source resistance associated with a change of range.

The MV1484 wafer structure is shown in figure 2.2. This is a strained layer structure with 5nm $Al_{0.67}Ga_{0.33}As$ barriers and a 5nm $In_{0.15}Ga_{0.85}As$ QW. The motivation for this structure stems from the work of Broekaert et al. [1] who reported a PVR of 30 at room temperature for an $In_{0.53}Ga_{0.47}As$/AlAs/InAs RTD. It was expected that the incorporation of In in the QW of the MV1484 would depress the conduction band edge within the well and thus effectively increase the barrier heights. This was expected to reduce the valley current. A corresponding reduction of the peak current brought about by the increased barrier heights suppressing more of the thermionic component was expected to be somewhat smaller. Hence, the PVR was expected to improve. However these devices did not exhibit evidence of NDR, even at 77K. Indeed their I-V characteristics were almost monotonic over the entire voltage range tested (-2.0 to 2.0V).

It is worth noting here that this structure was grown on an n^+ GaAs substrate as opposed to Broekaert et al.'s more complicated structures [1] which were lattice-matched to an n^+ or semi-insulating InP substrate and contained spacer layers on either side of the tunnel region. These spacer

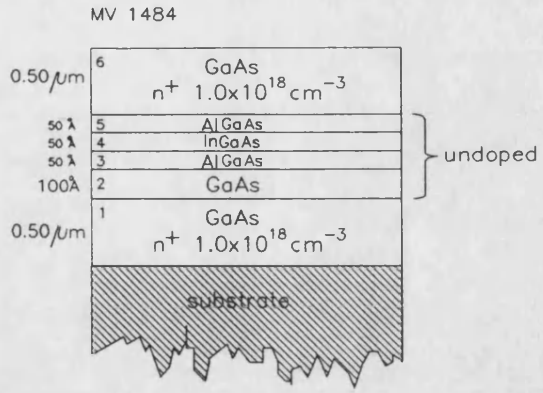


Figure 2.2. Schematic representation of the MV1484 strained layer heterostructure.

layers had graded doping between $2\times10^{18}cm^{-3}$ away from the tunnel region and nominally undoped in contact with the AlAs barriers. The lack of a top undoped spacer layer in the MV1484 structures has probably enabled dopant migration into the barrier/QW region giving rise to a high degree of scattering.

Dark field TEM studies carried out by A Wright [2] on these MV1484 SL structures have revealed good quality dislocation-free interfaces. However a high defect density was observed at the surface of the epilayer to within a depth of about $0.1\mu m$. The reason for this is not known.

The most recently fabricated PRL devices were those from wafer M269. Figure 2.3 shows the structure of this wafer. Motivation for this structure came from the work of Huang et al. [3], where it was reported that the AlGaAs-GaAs structure reproduced in figure 2.4 produced a PVR of 3.9 at 300K.

Two batches of M269 devices were characterised; the first being defined by wet chemical etching and the second by plasma-etching. All devices came from the same wafer. The wet-etched devices showed no room temperature NDC regions. However most of those which were plasma-etched showed

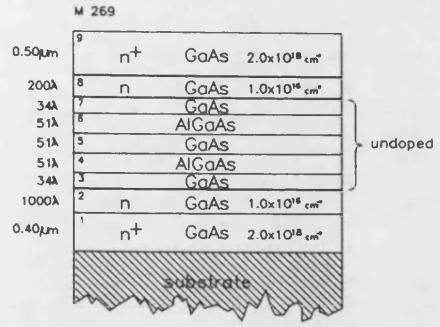


Figure 2.3. Schematic representation of the structure of the M269 wafer. The Al mole fraction in the AlGaAs barriers was 0.33.

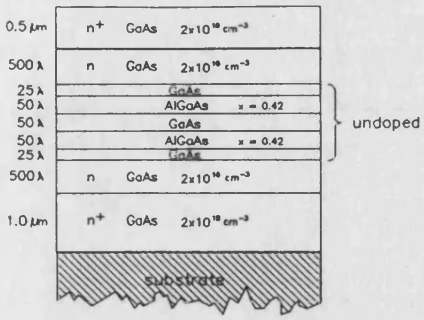


Figure 2.4. The resonant tunnelling structure due to Huang et al. (after Ref. [3])

slightly improved characteristics over the test temperature range (77 to 300K). Some of the observations are listed in table 2.1 and a few characteristics are shown in figure 2.5.

Shifts in peak and valley voltages and currents as well as changes in PVR are observed to be similar to previous observations. All devices investigated had unsymmetrical I-V characteristics and seemed to be slightly rectifying. At high reverse bias NDC regions were identified at room temperature (figure 2.6). Peak current densities in reverse bias were very small (~10A cm^{-2}) and those in forward bias even smaller (2A cm^{-2}). This was probably brought about by the thick (1000 Å) spacer layer used on the substrate side.

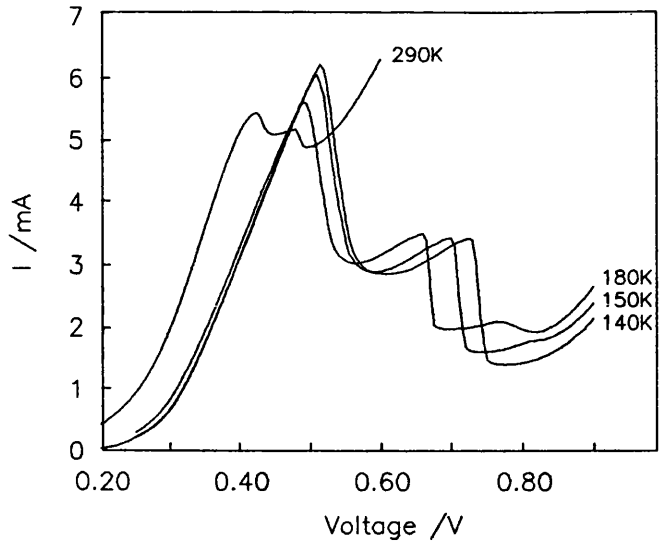


Figure 2.5. I-V characteristics in forward bias for a device from wafer M269 at different temperatures.

Table 2.1: Peak and Valley Voltages and Currents and P-V Ratios for some M269 devices.

Dia.(μm)	Temp(K)	$V_p(V)$	I_p(mA)	$V_v(V)$	I_v(mA)	J_p/J_v
*280	140	0.515	6.240	0.775	1.410	4.43
*280	150	0.510	6.074	0.740	1.611	3.77
*280	180	0.490	5.624	0.815	1.928	2.92
*280	290	0.425	5.455	0.495	4.900	1.11
*280	290	-2.040	-40.07	-2.255	-31.12	1.29
*160	290	0.380	1.867	0.445	1.719	1.09
*160	290	-1.755	-13.43	-2.010	-10.27	1.31
#280	209	0.460	5.350	0.600	3.017	1.77
#280	218	0.440	5.094	0.580	3.194	1.59
#280	224	0.440	5.092	0.580	3.272	1.56

* Plasma-etched devices
\# Wet-etched devices

Another observation which is worth noting here is the asymmetry in the I-V curves for the M269 devices. Whilst V_p in forward bias occurs at about 0.45V at room temperature, the current peak in reverse bias occurs at approximately

-2V. The NDC region in reverse bias was almost twice as wide as in forward bias and the room temperature PVR was about 1.3 when compared with 1.1 in forward bias[1]. The asymmetric forward and reverse bias regions were probably caused by the unequal spacer layer thicknesses (the epilayer spacer was 200 Å compared with 1000 Å for the other).

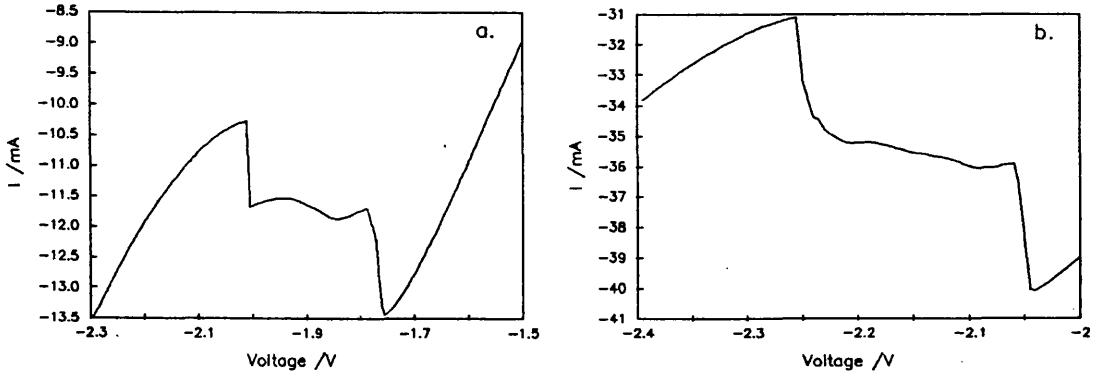


Figure 2.6. Reverse bias I-V characteristics for two resonant tunnelling devices from wafer M269 at room temperature; (a) 160μm, and (b) 280μm diameter.

In contrast, the I-V characteristics for GWS160 device (figure 2.7 (b)) show good antisymmetry and a relatively high peak current density (~2.0kA cm^{-2}). This structure, therefore, shows some potential for microwave applications even though the PVR is quite low. Figure 2.7 (a) also shows the structure of this wafer. The initial 0.5μm of the buffer layer had graded doping starting from $1.5\times10^{18}cm^{-3}$ at the substrate side to $2\times10^{17}cm^{-3}$ in contact with 0.25μm doped to $2\times10^{17}cm^{-3}$ subsequently grown after an interruption[2]. The spacer layers were each 36 monolayers thick (~100Å) and were undoped. Another important difference is the use of AlAs, rather than AlGaAs, for the barriers. This has the effect of (a) raising the barrier height, and, (b) reducing

1 Electron injection from the epilayer side.

2 Growth interruptions have been reported to be beneficial in that they tend to suppress dopant migration.

the alloy scattering inherent in ternary alloy structures. To increase the tunnel current, the barrier thickness was reduced to 11 monolayers (~31 Å). The QW region was also reduced to 15 monolayers (~42 Å). This has the effect of increasing the quasi-bound state energy relative to the emitter conduction band edge and is mainly the reason for the increased V_p (~1.4V).

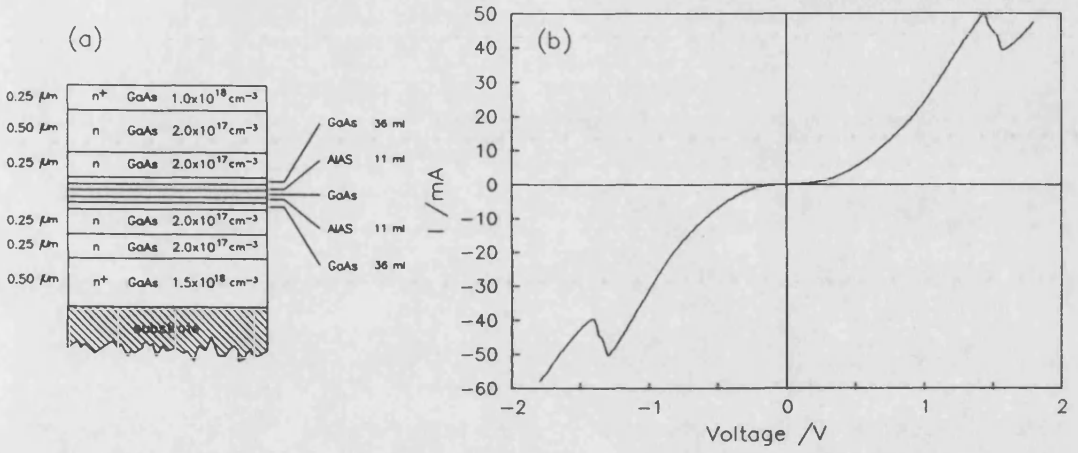


Figure 2.7. (a) the structure of the GWS160 resonant tunnelling heterostructure, and (b) room temperature characteristic of a 50×50μm device.

2.2.2 The MOCVD devices

The MOCVD wafers were grown at Siemens Research Laboratories [4] and they were kindly provided by Dr. S. J. Bending.

The structure labelled #421 was grown on n-doped ($1\times10^{18}cm^{-3}$) GaAs **(100)** substrates and has a 1μm thick GaAs buffer epilayer Si-doped to $2\times10^{18}cm^{-3}$. Undoped spacer layers of thickness 300 Å were grown cladding the double-barrier-quantum-well region, which consists of 50Å undoped $Al_{0.4}Ga_{0.6}As$ barriers and a 50Å undoped GaAs well. This undoped region is sandwiched between two 1000Å-thick n-doped

regions (Si - $1\times10^{17}cm^{-3}$). A heavily n-doped (Si - $6\times10^{18}cm^{-3}$) 2000Å-thick GaAs layer for top ohmic contact formation completes the structure (figure 2.8).

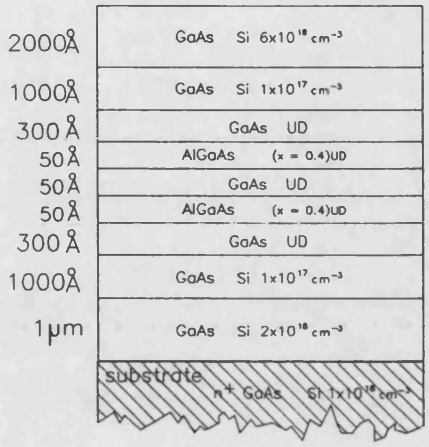


Figure 2.8. Schematic representation of the MOCVD double barrier heterostructures. The specified layer widths are for the #421. The #523 and #524 structures have 41 Å barriers and the latter has an $In_{0.07}Ga_{0.93}As$ quantum well.

The other MOCVD resonant tunnelling structures labelled #523 and #524, were similar to the #421 but both had 41Å barriers and the #524 was a pseudomorphic structure with an $In_{0.07}Ga_{0.93}As$, instead of a GaAs, QW.

Following Willer et al. [5], Ge/Au/Cr/Au ohmic contacts were evaporated on both faces and individual devices defined on the epilayer surface by lift-off. The devices were mesa-isolated by wet chemical etching using the metallisation as mask and the wafers subsequently alloyed at 400°C for 12 minutes.

Figures 2.9 and 2.10 show some typical I-V characteristics at different temperatures obtained for the MOCVD devices from wafer #421. The shift in V_p between 170 and 210K is negligible, however a shift is observed beyond this temperature which is qualitatively similar to the one observed in the M269 characteristics. In fact, in most studies

published so far reporting [6] results of I-V characterisation of DBRTD's at different temperatures V_p has been observed to shift to higher voltages at low temperatures. This effect has been attributed to a change in the space charge profile at different temperatures [7], which results in higher bias levels required to align the Fermi level on the emitter side with the quasi-bound levels in the QW. The effect can be modelled by a series resistance which increases with temperature.

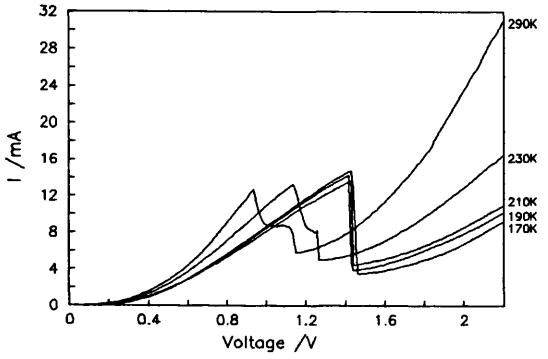


Figure 2.9. I-V characteristics of a resonant tunnelling device grown by MOCVD (wafer #421) at different temperatures. The device area is $70\times70\mu m^2$

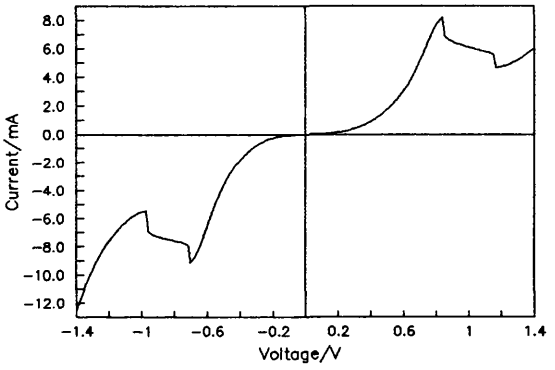


Figure 2.10. Room temperature I-V characteristic of a $50\times50\mu m^2$ device from the #421 wafer.

Figures 2.11 and 2.12 show, respectively, the room-temperature characteristics of two $50\times50\mu m^2$ devices from the #523 and #524 wafers. The #523 shows a peak current density of $1.4kAcm^{-2}$ and a PVR of 2.2, which is a marked improvement over the #421 ($0.32kAcm^{-2}$, PVR 1.9). However, V_p for the #523 is about 1.0V when compared with 0.8V for the #421. The #524 shows a slightly reduced PVR (1.5), a V_p of about 0.9V and a peak current density of about $0.36kAcm^{-2}$. The higher V_p's of the #523 and #524 are due to their narrower QW regions, which result in higher quasi-bound state levels. V_p for the #524 is lower than for the #523 probably because of the lower CB edge in the InGaAs QW. Various

devices were tested at different areas of the #523 wafer and in all cases V_p was found to be within 1.0±0.1V, thus it is unlikely that local variations in the structure are the cause of this higher peak voltage.

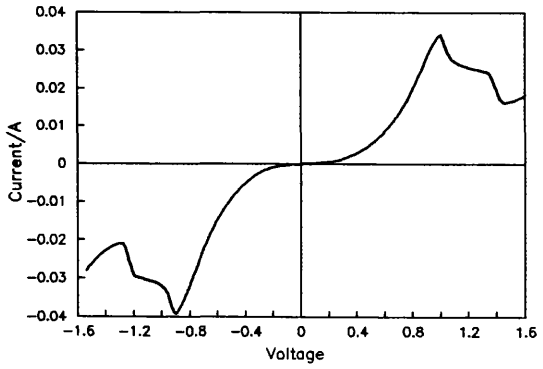


Figure 2.11. I-V characteristic of a device from the Siemens #523 DBRTD heterostructure. The device area is $50\times50\mu m^2$.

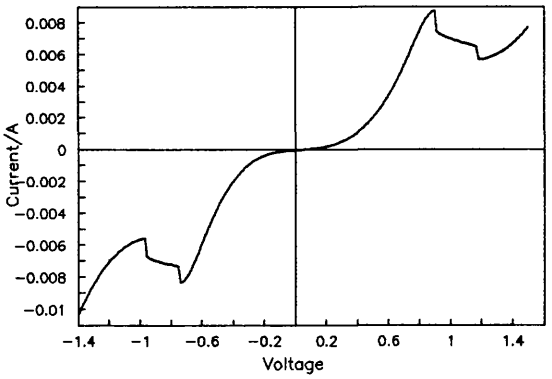


Figure 2.12. I-V characteristic of a device from the Siemens #524 DBRTD heterostructure. The device area is $50\times50\mu m^2$.

2.3 Bistability and Hysteresis in the I-V characteristic

The abrupt step-like change in current in the low temperature I-V characteristics for the #421 in figure 2.9 near the NDR region seems to suggest hysteresis. In fact, this proved to be the case as can be observed from figure 2.13 which shows the I-V curve of the same device taken at 170 K by scanning the voltage both up and down.

It has been postulated that this bistability is an intrinsic device property [8] and has been attributed to the effect on the potential profile of dynamically stored charge in the quantum well at and near resonance. That is, the band bending that occurs when the system is biased has two or even three [9] different solutions under one bias. Several authors [10,11,12,13] have reported detailed theoretical discussions and presented experimental observations on the

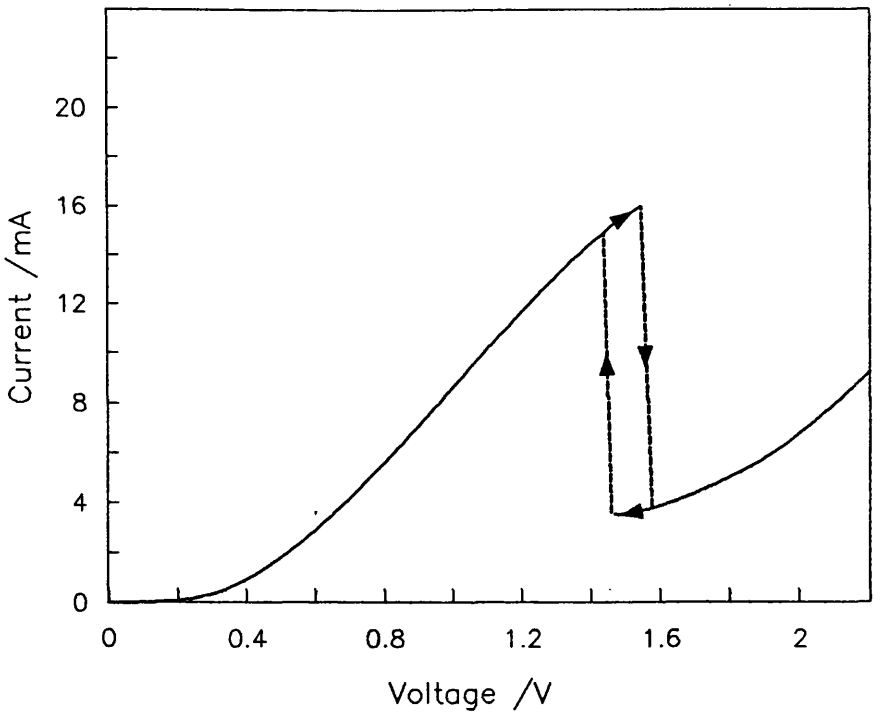


Figure 2.13. I-V characteristic of a $70\times70\mu m^2$ #421 RTD at 170 K. The hysteresis appears when the voltage is scanned first up and then down. The dotted lines represent the current jumps (bistability) and are not perfectly vertical because of the finite voltage step used in the characterisation.

hysteresis effects of DBRTD's with different barrier thicknesses and heights. However, the interpretation of the experimental results has been challenged by others [14,15,16,17,18] and the origin of the bistability shown to be equally well explained an the basis of extrinsic device-circuit interaction, as will be shown further on.

Despite the controversy over the observation of intrinsic bistability, its existence is well founded theoretically. Various authors [8,19,20] have used different theoretical approaches to the problem and their self-consistent numerical calculations led to essentially the same conclusions about the origins of intrinsic bistability. The experimental

observations have been explained as follows. Consider figure 2.14 which represents the conduction band (CB) under bias near the resonance peak with the emitter barrier to the left of the QW. Superimposed on the CB are the calculated [20] electron concentrations corresponding to the high (a) and low (b) current states across the structure. Since in figure 2.14a the solution is near the peak current point, there is an appreciable resonant buildup of electrons in the first quasi-bound state of the well. The solution represented in figure 2.14b suggests a much reduced dynamically-stored charge in the well and a corresponding buildup in the accumulation region on the emitter contact side. Thus, in figure 2.14b a greater voltage drop exists across the left-hand accumulation region than in figure 2.14a. This causes the voltage drop across the double-barrier region to decrease and hence lower the electron potential. The resonant energy level in the well therefore shifts down from the emitter CB edge taking the structure off resonance and thus reducing the charge buildup. Once this redistribution of charge between the emitter accumulation region and the QW is initiated, a regenerative action causes the device to switch between the two states.

At this point, a digression is worthwhile in order to establish the distinction between dc bistability, which involves no oscillation of the device circuit and another form of instability caused by oscillations of the current in the circuit containing the DBRTD when biased in the NDR region [14]. This latter effect is characterised by a double-stepped decrease in the current around the NDR region and will be discussed in more detail in section 2.3.2. Both effects are observable at different temperatures from the I-V curves of the #421 in figures 2.9 and 2.13.

The origin of the dc bistability can be understood on the basis of a load-line argument [21] as follows. Consider the bias circuit represented schematically in figure 2.15a,

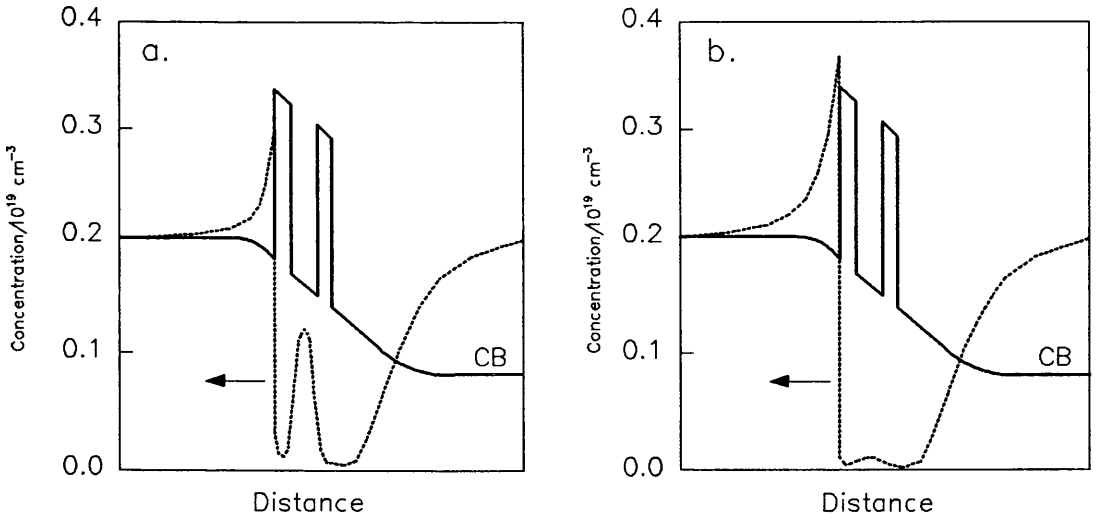


Figure 2.14. The conduction band of a DBRTD biased at resonance; the dotted line represents the electron concentration across the structure (a) in the high current state, and (b) in the low current state. (After Ref. [20])

where $R_d(V_d)$ represents the RTD in the dc circuit as a voltage-dependent resistance (which can take on negative values) and R_s, the series resistance, which here represents the sum of both the substrate and contact resistance of the RTD as well as the bias circuit resistance. V is the applied bias and I is the measured current. Assume that the I-V characteristic of the RTD has the typical shape of figure 2.15b. The device voltage V_d is related to V by

$$V = IR_s + V_d \qquad (2.1)$$

which enables the load line shown in figure 2.15b to be constructed in order to find the stable operating point of the device. The slope of the line is $-R_s$ and in this model is assumed independent of V_d. As the applied voltage V increases, the load line moves such that it intersects the I-V curve at higher voltages. The point of intersection defines the operating point (V_d, I) of the device. Now, if $\mathbf{R_s < |R_d^{min}|}$, the magnitude of the minimum value of the NDR, the intersection occurs at only one point and the whole of

the NDR region can be tracked (in principle). However, if $R_s > |R_d^{min}|$, then the load line will intersect the curve at more than one point and bistability occurs as the current jumps to the lower level. If, after having crossed the NDR region, the bias voltage is reduced, the same happens, but this time the current jumps to the higher level. The sequence of events depicted in figure 2.15b and c illustrates the origin of the hysteresis in the measured I-V characteristic.

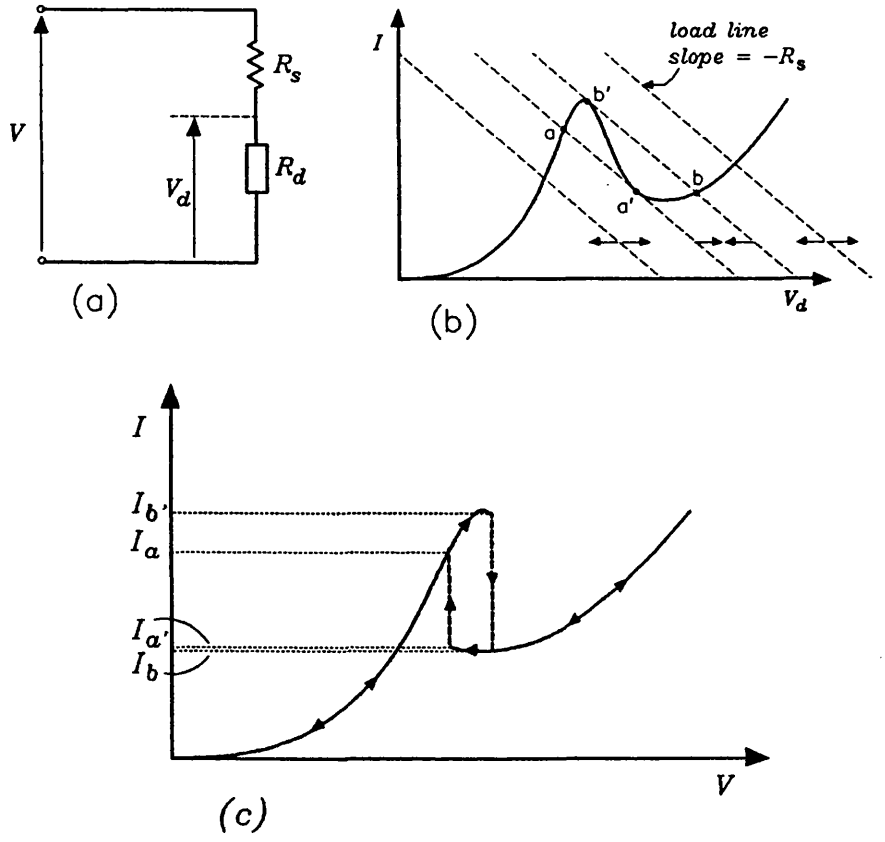


Figure 2.15. (a) bias circuit used to measure the dc I-V characteristic of a RTD, which is here represented as a voltage-dependent resistance; (b) a typical characteristic of a RTD, the x-axis represents the voltage across the intrinsic device, V_d; (c) the measured I-V curve using the circuit of (a) showing the hysteresis due to the comparatively large series resistance.

As V is increased (decreased) towards the bistable point, the current suddenly decreases (increases) from $I_{b'}$ ($I_{a'}$) to I_b (I_a). Since V is fixed by the voltage source, the drop (increase) in I has to be compensated for by an increase (drop) in V_d such that equation **(2.1)** still holds. Thus, the measured I-V curve exhibits hysteresis.

In the case of current-oscillation induced bistability, it has been proposed [14,22] that the measured dc current may be a time-averaged ac signal when the whole measurement circuit oscillates. This oscillation has been reported to be suppressed by a capacitor connected in parallel and close to the device [10]. The persistence in this case of the bistability at low temperatures, in the absence of oscillations, was interpreted as supporting the claim for its intrinsic nature. However, as the PVR increases greatly at low temperatures through the depression of the valley current, the NDR decreases correspondingly. Hence, series resistance in the measurement circuit, including contributions from the ohmic contacts and the bulk resistance of the doping region, can still introduce hysteresis [22]. Studies performed with DBRTD's of different areas [22,23] have revealed that the bistability and hysteresis cease to exist as the device area is reduced providing that oscillations in the circuit are adequately suppressed and the (total) series resistance in the circuit is less than $|R_d^{min}|$[1]. Now, if the bistability were intrinsic, it would also be manifest in the dc characteristics of the smaller devices. However, the structures of Ref. [22] and [23] were specially designed for high NDR by using thick (72 Å) AlGaAs barriers and a wide (100 Å) GaAs QW. Thus, it is still possible that

1 The argument for reducing device area is that the NDR is increased roughly in proportion to the area reduction, while the intrinsic component of the series resistance, including both the alloyed ohmic contacts and bulk semiconductor away from the DB region, does not decrease proportionally to the reducing area since the whole substrate is heavily doped [14].

intrinsic bistability exists in structures other than these and the task still remains to distinguish experimentally between the intrinsic and extrinsic mechanisms. For electrical measurements the device is inevitably connected to external elements, whereas for optical means such as photoluminescence the signal comes from both electrons and holes [24]. In the case of magnetotunnelling experiments [10,25,26] only the density of states, rather than the density of two-dimensional electrons in the quantum well, can be obtained.

2.3.1 Stability criteria

In most theoretical predictions of power from resonant tunnelling devices [27] the device is assumed to be biased at a stable point in the NDR region. In the presence of low frequency oscillations this is not possible. Since the negative resistance of the RTD extends from dc to high frequencies it is very difficult to suppress bias circuit oscillations and as a result, most of the published characteristics, as in the case of the present study, show evidence of bias-circuit related instability. Low frequency (LF) stability is a necessary criterion for most practical applications. In mixer and detector applications, the LF oscillations can occur near the IF or video frequencies, introducing additional noise. In high-frequency oscillator operation LF bias circuit instabilities may introduce undesirable up-converted signals that modulate the carrier and noise from chaotic-like oscillation bursts [28], resulting in a signal which is unacceptable for most applications.

The following describes established stability analysis and examines the nature and origin of bias circuit oscillations as well as their effect on measured current-voltage characteristics.

Consider figure 2.16 which represents schematically a simplified dc bias circuit for characterising a RTD. The intrinsic device is represented by the well known equivalent circuit of a tunnel diode, where R_s is the series resistance (including ohmic contact and bulk semiconductor resistance lumped together with the extrinsic resistance), C_d is the device capacitance and $-G_d$ ($=-1/R_d$) is the negative differential conductance of the device. L_s is the series inductance of the test leads and voltage source.

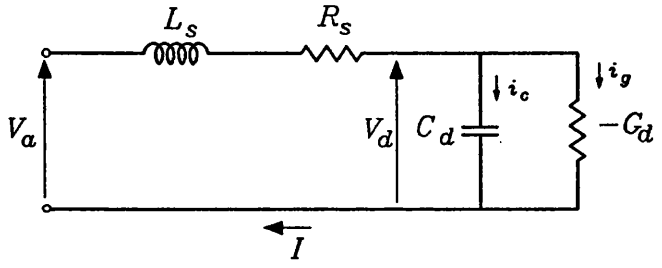


Figure 2.16. Simple equivalent circuit representing the biasing circuit of a RTD. The RTD is represented by a tunnel diode equivalent circuit model. L_s represents the circuit inductance.

The terminal impedance Z_d is given by

$$Z_d = R_s + j\omega L_s + \frac{1}{j\omega C_d - G_d}$$

$$= R_s - \frac{G_d}{G_d^2 + \omega^2 C_d^2} + j\omega\left(L_s - \frac{C_d}{G_d^2 + \omega^2 C_d^2}\right) \qquad \textbf{(2.2)}$$

At low frequencies the real part of Z_d is negative and increases monotonically with ω. The characteristic resistive cutoff frequency, f_{max}, is defined by

$$\omega_r = 2\pi f_{max} = \frac{G_d}{C_d}\sqrt{\frac{1}{R_s G_d} - 1} \qquad \textbf{(2.3)}$$

Above this frequency, the device loses its function as an active device and thus its capacity for generating power. If R_s does not include the external circuit resistance, then f_{max} would increase correspondingly to f_{rl}, the intrinsic negative resistance cutoff frequency [21], which can be used as a figure of merit for device comparison. Inspection of the imaginary term on the right-hand side of equation **(2.2)** leads to the definition of f_x, the internal resonance frequency of the device [21], which is obtained by setting the imaginary part of Z_d to zero:

$$\omega_x = 2\pi f_x = \sqrt{\frac{1}{L_s C_d} - \frac{G_d^2}{C_d^2}} \qquad \textbf{(2.4)}$$

The subsequent analysis will show the importance of the parameter f_x, which should be larger than f_{max} to prevent oscillations [29].

The dc stability criterion has been established in the previous section using the load-line concept. The basic requirement for a RTD biased at the minimum NDR point is therefore

$$R_s G_d < 1 \qquad \textbf{(2.5)}$$

Let us now assume that the RTD is biased at this point, where the voltage across $-G_d$ is V_d, and that over a small voltage range about V_d the I-V curve is linear. Then, the differential equation representing the circuit of figure 2.16 is

$$V = L_s C_d \frac{d^2 V_d}{dt^2} + (R_s C_d - L_s G_d)\frac{dV_d}{dt} + V_d(1 - R_s G_d) \qquad \textbf{(2.6)}$$

For small signals, equation **(2.6)** is linear since both G_d and C_d have been assumed independent of small changes in V_d. In this case, the general solution of **(2.6)** has the form

$$V_d = A_1 e^{m_1 t} + A_2 e^{m_2 t} + \frac{V}{1 - R_s G_d} \qquad \textbf{(2.7)}$$

where A_1 and A_2 are constants depending on the initial conditions, the third term is the dc bias voltage and m_1 and m_2 are the characteristic roots given by

$$m_{1,2} = \frac{1}{2}\left(\frac{G_d}{C_d} - \frac{R_s}{L_s}\right) \pm \sqrt{\frac{1}{4}\left(\frac{R_s}{L_s} - \frac{G_d}{C_d}\right)^2 - \frac{1 - R_s G_d}{L_s C_d}} \qquad \textbf{(2.8)}$$

These can be real or complex leading to different solutions. If m_1 and m_2 are real, an initial disturbance will either grow or decay exponentially, and if they are complex, the transient will be growing or decaying sinusoids. Equation **(2.8)** involves four equivalent circuit parameters and is thus unwieldy. It can, however, be reduced to a two-parameter function by the substitutions [30]

$$\omega_0 = \frac{1}{\sqrt{L_s C_d}} \qquad \textbf{(2.9)}$$

$$Q_0 = \frac{\omega_0 C_d}{G_d} \qquad \textbf{(2.10)}$$

Hence, **(2.8)** reduces to

$$m_{1,2} = \frac{1}{2}(1/Q_0 - R_s G_d Q_0) \pm \sqrt{\frac{1}{4}(R_s G_d Q_0 - 1/Q_0)^2 - (1 - R_s G_d)} \qquad \textbf{(2.11)}$$

For $R_s G_d > 1$, equation **(2.11)** is real and positive, representing the transient of a bistable case as discussed in the previous section. For $0 < R_s G_d < 1$, the roots m_1 and m_2 may become complex with either positive or negative real parts. Figure 2.17 shows a stability diagram proposed by Anderson [30] for a circuit similar to that of figure 2.16. The choice of substitutions **(2.9)** and **(2.10)** into **(2.8)** allow curves (a) and (b) to be calculated following the relations [30]

$$\text{a:} \qquad R_s G_d = \frac{2}{Q_0} - \frac{1}{Q_0^2}$$

$$\text{b:} \qquad R_s G_d = \frac{1}{Q_0^2} \qquad \textbf{(2.12)}$$

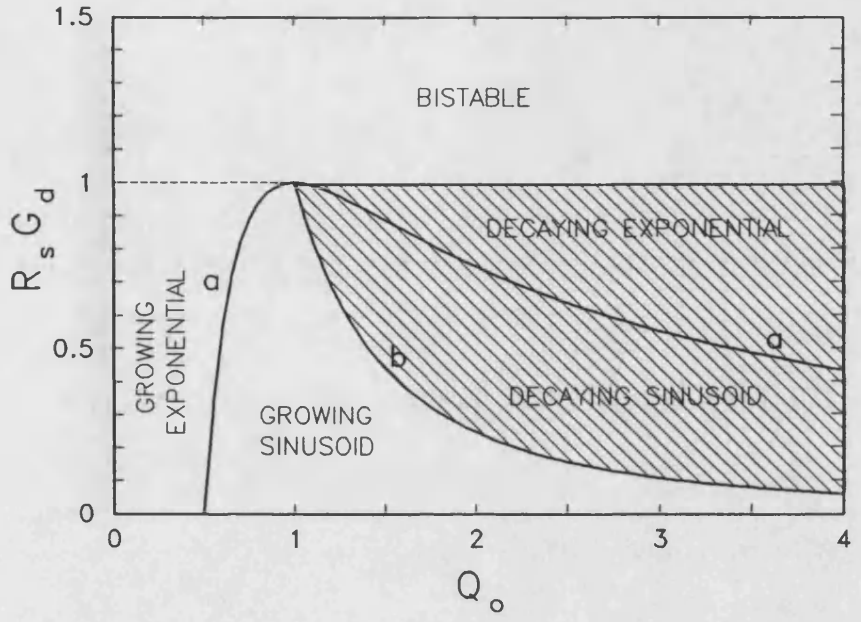


Figure 2.17. Stability chart for the circuit of figure 2.16 showing the allowed parameter ranges for particular types of transient behaviour.

These curves, along with the line $R_s G_d = 1$, subdivide parameter-space into regions where different solutions are obtained for equation **(2.6)**. The area above $R_s G_d = 1$ represents the bistable case. The area to the left of curve (a) below the dashed line represents a growing exponential function and is the region where the circuit generates relaxation oscillations [21]. These will be discussed further on. The region between (a) and (b) represents the growing sinusoidal solution. In practice, the total circuit resistance will be negative only for a small region about the bias point and so the voltage swing is constrained. There will be harmonics generated if the voltage swing moves

significantly out of the linear region. Hence, steady sinusoidal oscillations can only be obtained if R_s is close to (but less than) $1/G_d$.

The hatched area between (b) and (a) represents the decaying sinusoidal solutions and the remaining part above (a) represents the decaying exponential region. With circuit parameter values within these areas, the device is stable and it would thus be theoretically possible to measure the stable I-V characteristic.

From **(2.11)** and **(2.12)** we can quantify the circuit conditions which lead to the various regions of figure 2.17. For growing exponential solutions **(2.11)** must be real and m_1 and/or m_2 must be positive. Thus, **(2.11)** and **(2.12)** give the conditions

$$R_s G_d > \frac{2}{Q_0} - \frac{1}{Q_0^2} = 2G_d\sqrt{\frac{L_s}{C_d}} - \frac{G_d^2 L_s}{C_d} \qquad \textbf{(2.13a)}$$

$$R_s G_d < \frac{1}{Q_0^2} = \frac{G_d^2 L_s}{C_d} \qquad \textbf{(2.13b)}$$

For decaying exponentials, **(2.13a)** still holds but both m_1 and m_2 must be negative and hence,

$$R_s G_d > \frac{G_d^2 L_s}{C_d} \qquad \textbf{(2.14)}$$

Growing sinusoidal solutions require **(2.11)** to be complex with a positive real part. Thus **(2.11)** and **(2.12)** give

$$R_s G_d < \frac{2}{Q_0} - \frac{1}{Q_0^2} = 2G_d\sqrt{\frac{L_s}{C_d}} - \frac{G_d^2 L_s}{C_d} \qquad \textbf{(2.15a)}$$

$$R_s G_d < \frac{1}{Q_0^2} = \frac{G_d^2 L_s}{C_d} \qquad \textbf{(2.15b)}$$

And for decaying sinusoids, **(2.15a)** holds but **(2.11)** must have a negative real part, so that

$$R_s G_d > \frac{G_d^2 L_s}{C_d} \qquad \textbf{(2.16)}$$

Thus the stable regions of figure 2.17 (hatched areas) can be characterised by considering **(2.14)** and **(2.16)** together with **(2.5)** to give the stability criteria for the circuit of figure 2.16 as

$$\frac{G_d^2 L_s}{C_d} < R_s G_d < 1 \qquad \textbf{(2.17)}$$

From the inequality **(2.17)** and the expressions for ω_r and ω_x of **(2.3)** and **(2.4)**, it may be shown that for stability $\omega_r < \omega_x$ [21,29].

Now, for a given device, G_d and C_d are intrinsic properties, as is the part of R_s (in figure 2.16) which combines the ohmic contact and bulk semiconductor resistance. Thus, the stability criterion **(2.17)** reduces to

$$L_s < \frac{C_d}{G_d^2} \qquad \textbf{(2.18)}$$

The foregoing analysis applies for other voltage-controlled negative conductance devices which exhibit NDC from dc to high frequencies, such as tunnel diodes and Gunn devices. For tunnel diodes, minimising lead inductance is a problem. However, it is relatively simpler to stabilise a tunnel diode than a RTD because the former has a larger capacitance. Gunn devices, on the other hand, have a much smaller negative conductance at the operating point which makes stabilisation easier to achieve.

With the DBRTD's studied in chapters 4 and 5, typical values of G_d and C_d are of the order of millisiemens and picofarads respectively. This constrains L_s to nanohenries and even smaller. Thus, conventional microwave packaging may just be sufficient to introduce dc instability. Smaller devices,

with correspondingly lower G_d values, could be potentially stable providing the equivalent bias circuit inductance and capacitance are adjusted to satisfy **(2.18)**. Devices with considerably higher peak current densities and PVR's, suitable for high frequency applications, would have reduced areas. However lower values of C_d and relatively higher G_d place even more severe restrictions on L_s, which would preclude the use of conventional microwave packaging. Whisker contacting techniques could reduce L_s significantly, although in some cases not enough. Another possible method would be to mount the device between the plates of a capacitor, as is effectively the case with resonant cap circuits [31,32] which have been used successfully for millimetre-wave IMPATT oscillators. In this case, however, added capacitance inside the microwave circuit will lower the effective cutoff frequency and output power [29] especially since RTD's have a relatively low impedance.

2.3.2 Observation and Simulation of bias circuit oscillations and extrinsic bistability

The purpose of the numerical simulations to be described here is to study the effect on the I-V characteristics of external elements in the biasing circuit and to obtain a physical picture of the interaction of the RTD with the latter. Several studies [15,16,17,18] have reported numerical simulations of extrinsic instability effects on the I-V characteristics of DBRTD's which are similar to experimentally observed curves, employing methods initially applied for tunnel diodes [33]. A similar approach will be adopted here.

For the purpose of the calculation, the circuit of figure 2.16 is modified to that of figure 2.18, where the intrinsic device is now simply a nonlinear (voltage-controlled) conductance, $G_d(V)$. The resistance R represents the total

circuit resistance, L the inductance and C the capacitance. The real situation will be more complex, since the device has its own voltage-dependent capacitance and some of the extrinsic circuit elements will have a distributed nature at high frequencies.

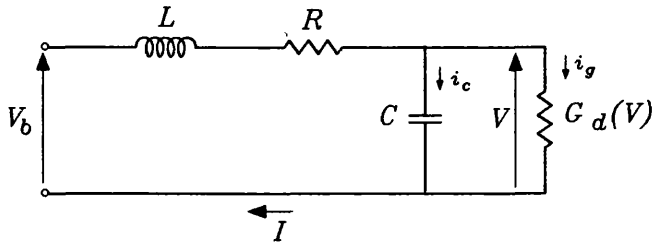


Figure 2.18 Bias circuit model representing the RTD by a nonlinear conductance $G_d(V)$. R, L and C represent the total circuit resistance, inductance and capacitance, respectively.

The differential equation representing the behaviour of the circuit of figure 2.18 will be similar to **(2.6)** but will be nonlinear [17]:

$$\frac{V_b}{LC} = \frac{d^2V}{dt^2} + \left(\frac{G_d}{C} + \frac{R}{L}\right)\frac{dV}{dt} + \left(\frac{R + R_{dc}}{LCR_{dc}}\right)V \qquad \textbf{(2.19)}$$

where $R_{dc} = V/i_g$. The initial conditions are obtained by applying dc analysis (open C and short L);

$$V(0) = \frac{V_d R_{dc}}{R_{dc} + R}$$

$$\left.\frac{dV}{dt}\right|_{t=0} = 0 \qquad \textbf{(2.20)}$$

Equation **(2.19)** can be integrated numerically providing $i(V)$ and $G_d(V)$ are known.

For the purpose of simulation a fourth-order Runge-Kutta algorithm with an adaptive step size [34] was employed, using actual dc I-V characteristics of a RTD. The device

chosen was a MOCVD $65\times65\mu m^2$ DBRTD form wafer #421. The I-V characteristic for this device was not stable and exhibited a chair-like structure similar to that of figure 2.10. A smaller $20\times20\mu m^2$ device from the same heterostructure proved to be stable when characterised through a bias network (HP11612A) with the rf input port terminated by a 50Ω load[1]. The stable NDR region obtained for the smaller device was then used to model the corresponding region of the larger RTD. This effectively simulates the stable I-V curve with reasonable accuracy. Figure 2.19 shows the final result of the 'stable' characteristic of the $65\times65\mu m^2$ device, which, like the smaller device, was assembled in a LEW Techniques E3 package (similar to the S4) as described in chapter 3 and Appendix III. The I-V data of figure 2.19 was then used to generate $G_d(V)$ by cubic spline fitting and numerical differentiation after adjusting the voltage coordinates assuming a 5Ω (intrinsic) series resistance [35]. $G_d(V)$ is also shown in figure 2.19. This data is then used by the simulation programme (see Appendix II) to obtain instantaneous values of $i_g(t)$ and $G_d(t)$, during the execution of the integration algorithm, by spline interpolation. The sampling period was chosen such that it is about 20-30 times the period of the subsequent oscillations. The integration range was chosen long enough to allow $V(t)$ and $i_g(t)$ to reach steady state values and include about 10-20 cycles of the latter.

---

1 The maximum $G_d(V)$ for the $20\times20\mu m^2$ device was about 3 mS. Now, neglecting package and mount parasitics which are swamped by the bias network dc arm elements of L = 2μH and C = 1000 pF (Hewlett Packard Operating and Service Manual: HP11612A Bias Network, 1989, p. 4), applying the stability criterion **(2.18)** reveals that the small device should be stable since $C_d/G_d^2 \approx 100\mu H \gg L$. For the $65\times65\mu m^2$ device, $G_d(V) \approx$ 35 mS giving $C_d/G_d^2 \approx 0.8\mu H < L$.

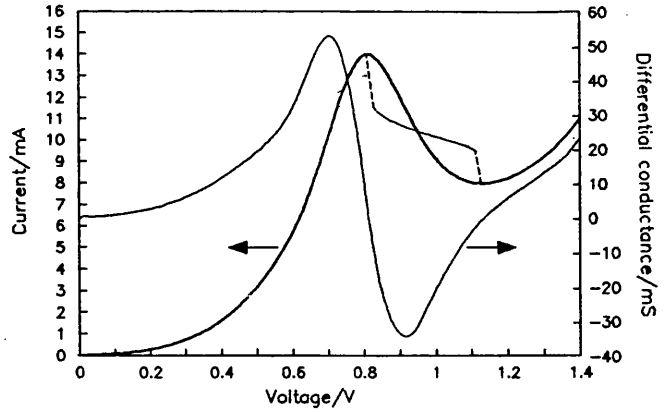


Figure 2.19. Artificially-stable I-V characteristic of the $65\times65\mu m^2$ DBRTD from wafer #421 (solid line). The dashed line represents the measured unstable characteristic. Also shown is the differential conductance as a function of voltage. The characteristics shown have been adjusted assuming a 5Ω device series resistance.

In order to simulate the unstable I-V curve, the time-averaged values of $V(t)$ and dV/dt, $\overline{V}_i$ and $\langle dV/dt \rangle_i$, are computed at the end of the i^{th} integration cycle and the initial conditions for the $(i+1)^{th}$ cycle are set according to

$$V_{i+1}(0) = \overline{V}_i + \Delta V$$

$$\left.\frac{dV}{dt}\right|_{t=0}^{i+1} = \left\langle \frac{dV}{dt} \right\rangle_i$$

where ΔV is the voltage increment.

2.3.2.1 Time-domain behaviour

Figure 2.20 represents schematically the simple experimental setup used to observe the bias circuit oscillations. The packaged $65\times65\mu m^2$ device was mounted in an N-type mount (see chapter 3) connected to an sma Tee as shown. The bias was applied through about 60 cm of 50 Ω coaxial cable from a Time Electronics™ 9814 voltage source. Circuit oscillations were monitored through a similar cable on a Tektronix

2467, 350 MHz bandwidth, oscilloscope. It was found that a 3 dB attenuator in the oscilloscope line improved the triggering and thus provided a more stable trace. This probably occurred because of attenuation of multiply-reflected signals. The equivalent inductance (L) and capacitance (C) of the arrangement are estimated to be about 0.1 μH and 2 nF respectively.

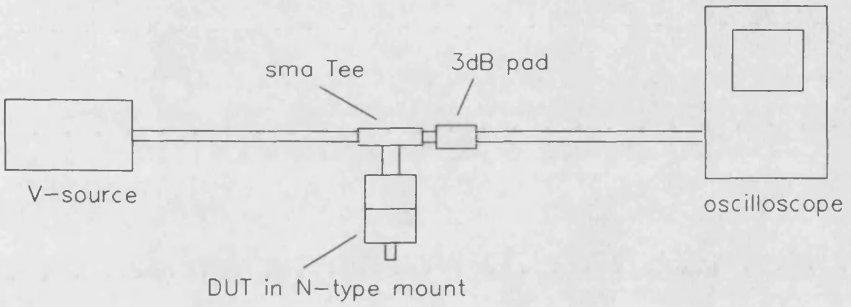
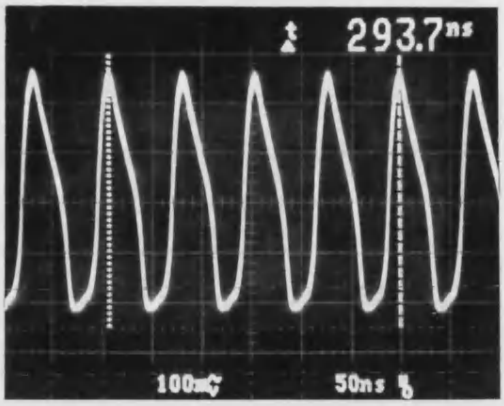


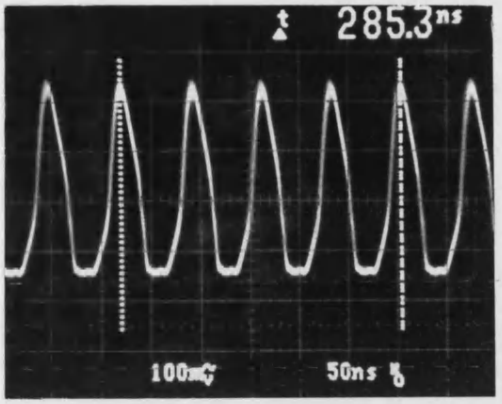
Figure 2.20 Schematic representation of the experimental circuit used to observe bias circuit oscillations.

The oscilloscope photographs of figure 2.21a-c show relaxation oscillations taking place at bias voltages of 0.92, 1.00 and 1.1V, respectively, while figures 2.22a and b are the result of simulations using the program discussed in the previous section. The calculations were performed assuming $R = 6\Omega$ (5Ω for intrinsic series resistance and about 1Ω for the extrinsic component), $L = 0.5\mu H$ and $C = 2nF$. Smaller values of L in the region of about $0.1\mu H$ resulted in similarly shaped waveforms but at frequencies about twice those measured. This is probably because the circuit inductance and capacitance estimates were not accurate enough. The calculated voltage swings of about 0.7V peak-to-peak correspond approximately to the measured values when allowing for the 3 dB attenuator in the oscilloscope line. The agreement between the observed and calculated waveforms is reasonably good when considering the over-simplified equivalent circuit used for the simulations. The model thus

represents the actual situation fairly well and should therefore allow useful qualitative (if not quantitative) information about circuit behaviour to be extracted.

Figures 2.23-2.26 give the results of simulations carried out with circuit parameters and bias voltages listed in table 2.2. In the case of figure 2.22 the initial circuit conditions are such that **(2.15a)** and **(2.15b)** are satisfied such that the transient is a growing sinusoid.





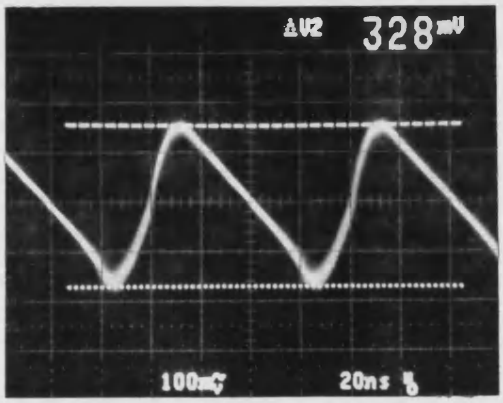


Figure 2.21. Oscilloscope photographs of bias circuit voltage oscillations: top left (a) at 0.92V, top right (b) at 1.0V, left (c) at 1.1V.

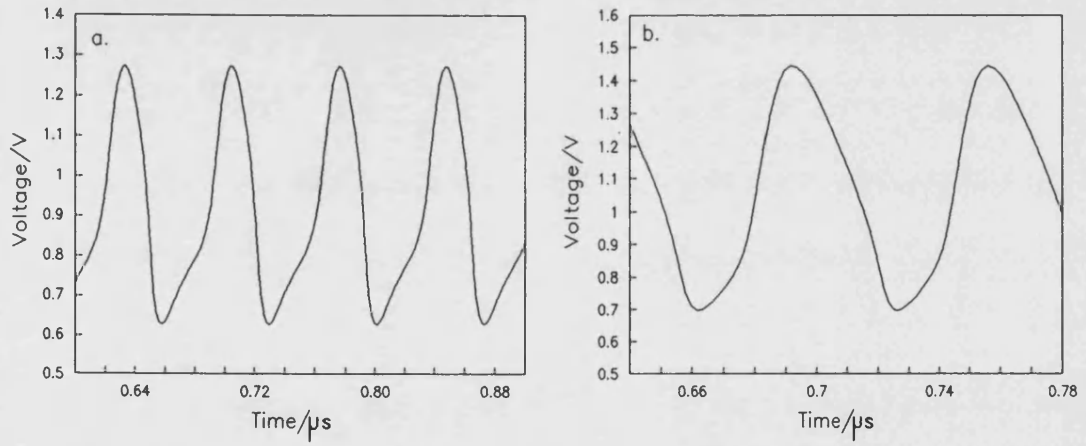


Figure 2.22. Simulated bias circuit oscillations with $L = 0.5\mu H$, $C = 0.18nF$, and $R = 6\Omega$ at bias voltages of 0.92V (a) and 1.1V (b). The frequencies are 13.8 and 15.5 MHz for (a) and (b) respectively.

The conditions leading to figure 2.24 satisfy **(2.15a)** and **(2.16)** so that the resulting transient is a decaying sinusoid. In the case of figure 2.23, however, the voltage swing moves

Table 2.2: Circuit and device conditions leading to figures 2.23-2.26

Figure	L/μH	C/nF	R/Ω	$\mathbf{v}^*$/V	$G_d(V)^*$ /mS
2.23	0.15	0.6	1.0	1.0	24.1
2.24	0.15	0.6	5.0	1.06	9.43
2.25[1]	20	0.1	10	0.89	32.6
2.25[2]	20	0.1	10	1.12	1.17
2.26[1]	1.5	0.1	50	1.03	14.5
2.26[2]	1.5	0.1	50	1.08	6.36

* Initial values
1 Corresponding to solid line
2 Corresponding to dashed line

into regions of positive differential conductance which thus limit the growth of the oscillation. Closer inspection of the final steady state waveform reveals that it is in fact almost similar to that of figure 2.22b. Now, the total circuit resistance chosen (1 Ω) is not realistic since the actual device series resistance is estimated to be close to 5 Ω. This low value of R is such that conditions **(2.15a)** and **(2.15b)** prevail almost throughout the whole of the voltage swing except at the extremes, where the conditions for decaying sinusoids and exponentials are more easily satisfied due to a smaller G_d near the peak and valley voltages.

In the case of figure 2.26, the initial conditions giving rise to the dashed line demand a growing sinusoid. However, as the voltage increases, $G_d \rightarrow 0$ and the transient changes behaviour, first to a decaying sinusoid and then a decaying exponential to eventually settle down near V_v. Similarly

for the solid line, the voltage rises initially and then falls to eventually settle near V_p. The part of the NDC region where $RG_d > 1$ is inaccessible as a final steady state.

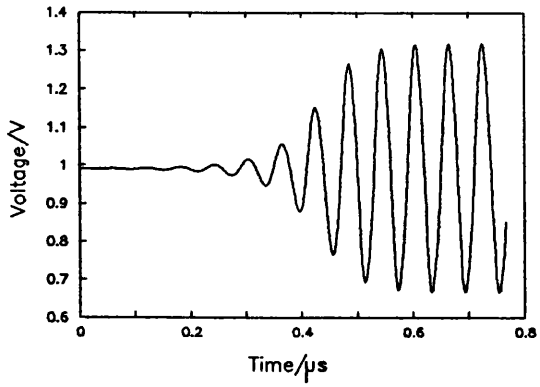


Figure 2.23. Growing sinusoid.

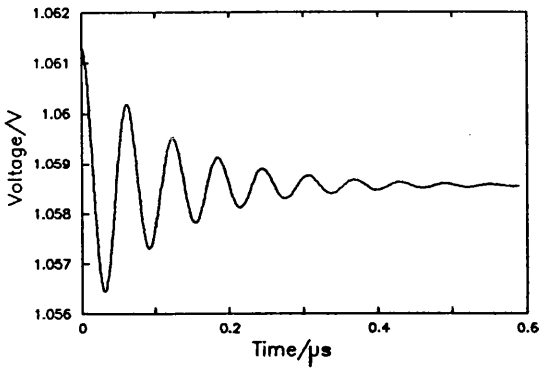


Figure 2.24. Decaying sinusoid.

The case of the relaxation oscillations of figure 2.25 merits closer inspection. It has been shown [36] that this type of electrical oscillation reaches its steady-state waveform after one cycle. The mechanism of the relaxation oscillations can be described qualitatively as follows. Consider figure 2.27, which represents a limit cycle with the calculated total circuit current plotted as a function of the calculated voltage V across G_d and C over one complete period of the oscillation. Also shown is the I-V characteristic.

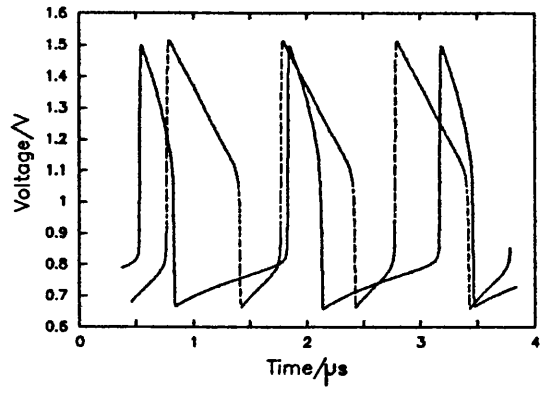


Figure 2.25. Relaxation oscillations.

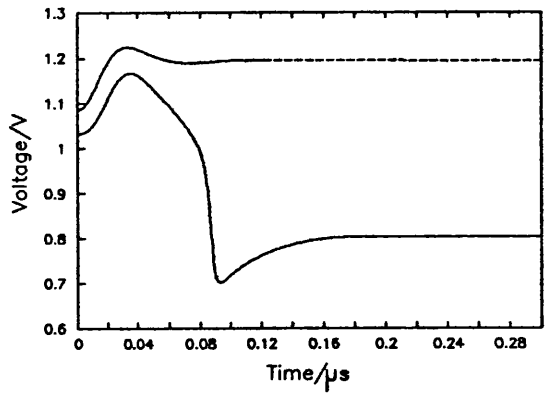


Figure 2.26. Bistability.

Let us now assume that the initial bias voltage is just below V_p such that the RTD is in its positive differential conductance (PDC) region. When the voltage is stepped so that it lies within the NDC region, the current increases. However this cannot happen rapidly because of the large circuit inductance. Thus, current is drawn from the circuit capacitance. After passing the peak point the NDC demands less current with increasing voltage across G_d. However, since the current through the inductance cannot decrease suddenly, the balance is used to charge the circuit capacitance.

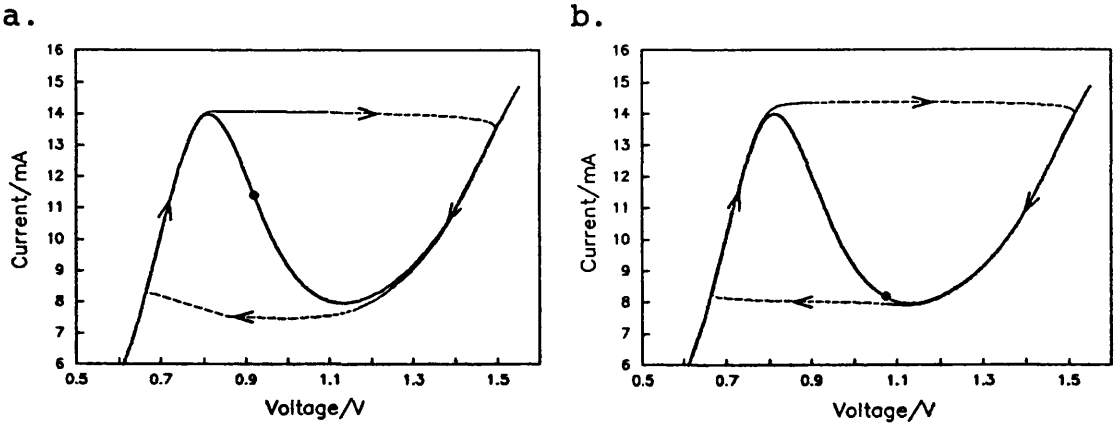


Figure 2.27. Total circuit current as a function of voltage across G_d corresponding to solid (a) and dashed (b) lines of figure 2.25. The respective (nominal) bias voltages are indicated by the solid circles.

This sequence of events is represented in figure 2.28, which shows the calculated voltage across G_d and C as functions of time for the initial 2.2μs. Since there is a large current available, the voltage across G_d increases rapidly. It overshoots the valley point and reaches a point in the high-voltage PDC region (figure 2.27). Since the source voltage is not high enough to support this point and the device is in its PDC region, the energy of the inductance is dissipated in the positive resistance of the circuit and the voltage and current decrease. When the device voltage

becomes less than V_v, it encounters the NDC region once more which demands increasing current with decreasing voltage. This excess current comes from discharging C.

When the voltage drops below V_p the device conductance is again positive and the energy stored in the capacitance is dissipated in the circuit resistance. By the time the voltage reaches its minimum value, the applied bias still demands a higher device current and voltage and so the cycle repeats indefinitely.

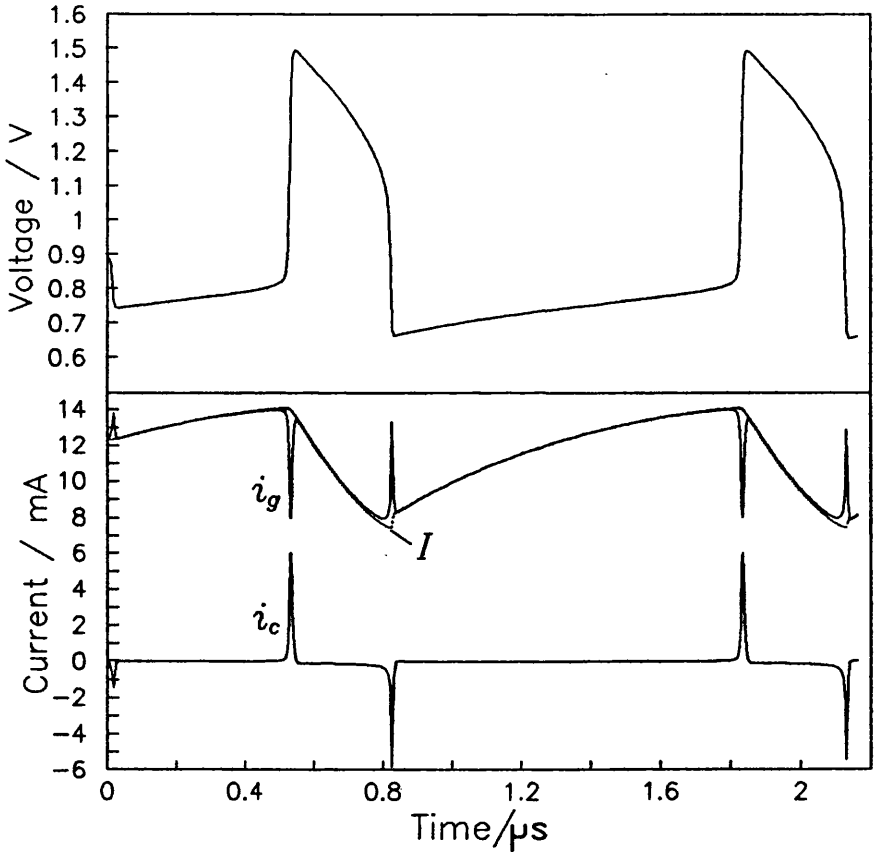


Figure 2.28. Voltage, total circuit current, I, current through the capacitance, i_c, and current through G_d, i_g, as functions of time for the first 2.2μs of the relaxation oscillations of figure 2.25 (solid line) and figure 2.27a.

In practice, the total circuit current I is the measurable quantity. When this is observed in the time-domain (figures 2.27 and 2.28) and compared with the voltage, I is seen to remain practically constant at about I_p while the voltage increases rapidly. Conversely, when the voltage is on the negative edge of the cycle, I remains practically constant at about I_v. These effects have been observed experimentally (see figure 3 of Ref. [15]) and similar results obtained by numerical simulation have been reported (see figure 4 of Ref. [17]).

2.3.2.2 Simulation of unstable I-V characteristics

As described in section 2.3.2, the program of Appendix II can be modified to allow the numerical simulation of a 'measured' I-V characteristic when the RTD is unstable. In this way, the effects of circuit parameters on the resulting shape may be investigated.

Figure 2.29 shows results of simulated characteristics for the $65\times65\mu m^2$ MOCVD DBRTD from wafer #421 using different values of L and C = 0.1 nF. The solid lines represent the dc circuit current calculated as a function of increasing bias while the dotted lines represent the results of decreasing bias. The simulations were performed between 0.7 and 1.4V, but only the unstable regions are shown since beyond the hysteresis regions all lines coincide with the dashed line representing the stable I-V curve. This has been adjusted so as to represent the actual stable characteristic that would be measured with a circuit resistance $R = 10\Omega$, as assumed in the calculations.

The extrinsic circuit-induced instabilities result in the typical chair-like structure observed experimentally towards the middle of the NDC region. In the case of $L = 0.5\mu H$ there is clearly a region of PDC approximately in the middle of

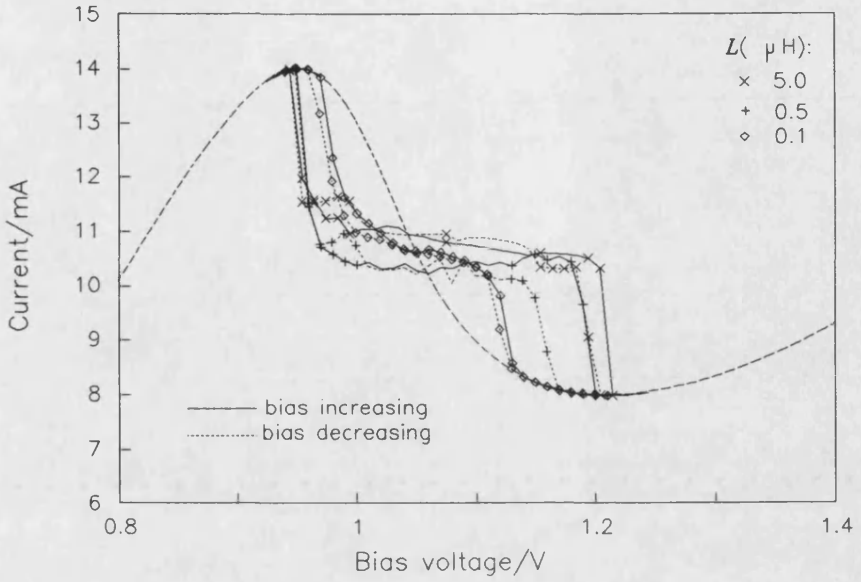


Figure 2.29 Simulated unstable dc characteristics of the $65\times65\mu m^2$ MOCVD DBRTD from wafer #421 using different values of L, C = 0.1 nF and $R = 10\Omega$. The bias voltage was increased (solid lines) and then decreased (dotted lines) by 0.01V increments in the calculation. The dashed line represents the 'measured' characteristic if the circuit were to be stable. Most of the point-labels have been removed from the central and peripheral regions for clarity.

the plateau. It is observed that the width of the hysteresis loops depends mainly on the relative values of L and C, and that around V_p the loops are narrower than the corresponding loops near V_v.

These effects may be explained as follows. For small L the prevailing circuit conditions with the device biased near the unstable region are those which support decaying sinusoids near V_p and V_v (to a greater extent near V_v because of the slower change in $G_d(V)$ in this vicinity) hence the circuit remains stable to within the extremities of the NDC region. When the bias reaches the middle region where $RG_d < G_d^2 L/C$, the circuit starts oscillating almost sinusoidally since with the maximum G_d of about 35 mS condition

(2.15a) is satisfied which implies growing sinusoids. The amplitude is limited as mentioned earlier, and steady-state waveforms are established and the dc circuit measures the time average of the circuit current. Now, for $L = 0.5\mu H$ and higher, conditions **(2.13a)** and **(2.13b)** are upheld for bias voltages within the middle of the NDC region. The resulting exponentially-growing voltage is then limited as described in the previous section, giving rise to relaxation oscillations. Thus it is the larger values of L/C that cause the circuit to become unstable at voltages relatively closer to the PDC sections and to quickly move into regions where **(2.13a)** and **(2.13b)** are satisfied, explaining the sharp demarcation between stable and unstable regions for higher L. It can therefore be appreciated that, in addition to defining the stability range for given circuit parameters, the shape of $G_d(V)$ controls the symmetry of the hysteresis loops near V_p and V_v. Thus, because of the steeper variation of $G_d(V)$ near V_p, the damping due to oscillatory excursions into the PDC region increases faster and oscillations cease sooner, resulting in a narrow loop in this vicinity. Near the valley, however, $G_d(V)$ varies more slowly, and oscillation is permitted at bias voltages closer to V_v. As a matter of fact, inspection of figure 2.25 reveals that the oscillation represented by the dashed line at a bias close to V_v has about 63% duty cycle as opposed to about 21% for the other oscillation (solid line). The frequency also increases slightly, as is observed from figures 2.25 and 2.21.

The extent to which oscillations are allowed to persist past V_v depends on whether the bias is increasing (i.e. $G_d(V)$ increasing) or decreasing ($G_d(V)$ decreasing) since the initial conditions at any bias voltage are determined by the steady-state conditions at the previous voltage.

Finally, figure 2.30 shows the calculated current through G_d, $i_g(V)$. This reproduces the stable NDC region faithfully. Now, from figure 2.18, i_g is given by

$$i_g(t) = I(t) - C\frac{dV}{dt} \qquad \textbf{(2.21)}$$

This suggests that if the total current waveform is measured in a real circuit along with the voltage waveform at **one** bias voltage where large-signal oscillations take place in the bias circuit, the 'stable' I-V characteristic in the NDC region can be extracted if the circuit parameters are accurately known. Thus, if the circuit series inductance and shunt capacitance are deliberately increased so as to make the device intrinsic capacitance and package and mount parasitics relatively negligible at the lower resultant oscillation frequencies, accuracy should be enhanced.

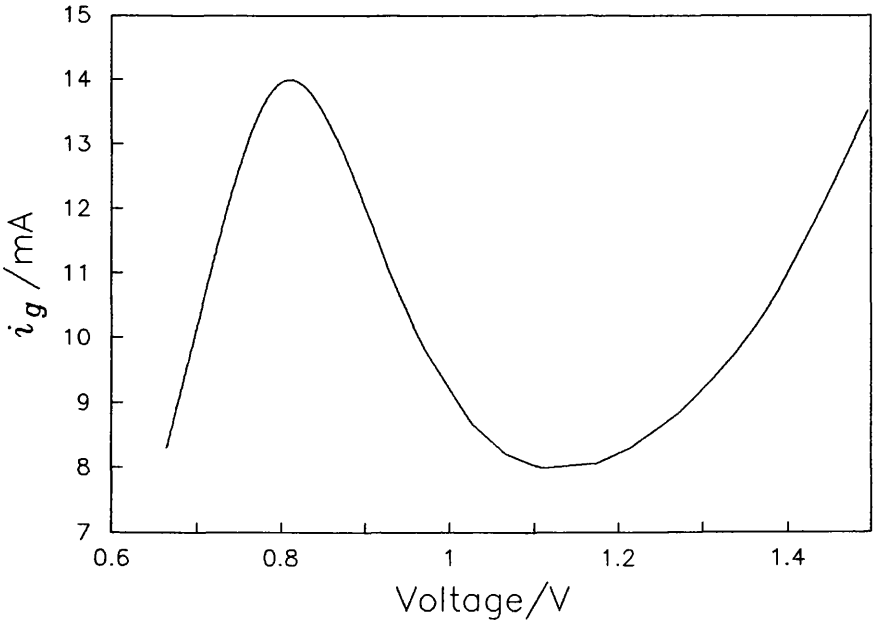


Figure 2.30 Current through G_d, i_g, plotted as a function of the voltage across G_d over one limit cycle calculated for a bias of 0.89V with the circuit conditions of table 2.2 for figure 2.25 (solid line).

2.4 Implications of dc stability criteria on rf power generation

It has been mentioned previously that bias circuit instabilities adversely affect the applicability of RTD's. Since the usefulness of these devices will be determined by functionality rather than interesting physics, it would be fruitful to assess the effects of stability criteria on power generation.

Condition **(2.18)** would require $L_s G_d^2 / C_d < 1$ in the rf section of a potential oscillator circuit. Assuming G_d and C_d scale linearly with device area, A, and writing these as the respective conductance and capacitance per unit area, this inequality can be re-written as

$$\frac{A G_D^2 L_s}{C_D} < 1 \qquad \textbf{(2.22)}$$

G_D is an intrinsic property of the device structure and can only be partially controlled by device design.

It is apparent that stability will be improved by reducing device area, which is consistent with requirements for high frequency devices. Reducing A results in smaller capacitance, which is beneficial in coupling these low-impedance devices to an rf load. However **(2.22)** also implies that the device capacitance should be increased to improve dc stability. This is in direct conflict with performance criteria for high-frequency devices [37]

The output power from a RTD may be calculated by assuming that the device is matched to a circuit with a load resistance R_L. Thus, from **(2.2)**

$$R_L = -R_s + A \frac{G_D}{G_D^2 + (\omega C_D)^2} \qquad \textbf{(2.23)}$$

where the conductance and capacitance per unit area have been used instead of G_d and C_d, since the power scales with device area and thus A has to be selected. In order to examine the effects of G_D and C_D on power generation, let us assume A to be unit area and R_s to be negligibly small. Under these conditions **(2.23)** reduces to

$$R_L \approx \frac{G_D}{G_D^2+(\omega C_D)^2} \qquad \textbf{(2.24)}$$

The power generated by a RTD of unit area is thus

$$P_{rf} = \frac{1}{2}\frac{|V_{rf}|^2}{R_L}$$

$$\approx \frac{1}{2}\frac{|V_{rf}|^2}{1+\left(\frac{\omega C_D}{G_D}\right)^2} \qquad \textbf{(2.25)}$$

where V_{rf} is the rf voltage amplitude across the RTD. Let us further assume G_D to be constant over the NDC region and the bias such that V_{rf} reaches V_p and V_v during the cycle. Thus V_{rf} will be assumed as $(V_v-V_p)/2=\Delta V/2$ and $G_D=(J_p-J_v)/\Delta V$, where J_p and J_v are the peak and valley current densities, respectively. With these assumptions, P_{rf} at very high frequencies reduces to

$$P_{rf} = \frac{1}{8}\left(\frac{\Delta J}{\omega C_D}\right)^2 \qquad \textbf{(2.26)}$$

This has encouraged efforts to increase J_p and decrease C_D, while maintaining a reasonably high PVR, in a bid to raise power output at high frequencies. If stability is considered, however, the analysis is not strictly valid except for the ideal situation with negligible L_s. Condition **(2.22)** must therefore be applied, which, for unit area, requires $C_D > G_D^2 L_s$. This imposes a lower bound on device intrinsic capacitance which is determined by G_D apart from L_s. It is therefore

obvious that ΔV cannot be ignored when designing devices for high frequency power generation, since the stability-limited power becomes[1] [29]

$$P_{rf} \leq \frac{1}{8}\Delta V \Delta J \frac{C_D}{L_s G_D^2} = \frac{1}{8}(\Delta V)^3 \frac{C_D}{\Delta J L_s} \qquad \textbf{(2.27)}$$

Where the device properties are concerned, the requirements for stability are therefore in direct conflict with those for high frequency power generation. When the device is limited by stability, the performance becomes related to the ratio $\Delta J L_s / C_D$. Stability considerations will **not** limit the output power of a device only if the maximum power from **(2.27)** exceeds the power from **(2.26)**.

Finally, the circuit parameters limiting dc-stable rf generation are the load resistance and the lead inductance. R_L has to be small for improved matching since RTD's have a relatively low impedance. This limits the usable device area through **(2.5)** especially for high frequencies. The minimum value of L_s necessary to prevent bias circuit oscillations limits the device area through **(2.23)**.

---

1 $P_{rf} = |V_{rf} I_{rf}^*| / 2$. Because $|V_{rf}|$ has been assumed to be $(V_p - V_v)/2 = \Delta V/2$, then $|I_{rf}| = (I_p - I_v)/2 = A(J_p - J_v)/2 = A\Delta J/2$. Thus $P_{rf} = A\Delta V \Delta J/8$.

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CHAPTER 3

DE-EMBEDDING TECHNIQUES

3.1 Introduction

The realisation of passive or active microwave components and systems requires, in the design stage, detailed knowledge of the behaviour of the incorporated solid state devices under varying dc bias and microwave operating conditions. Device characterisation is here taken to describe the process by which the microwave impedance (or admittance) of the device is recovered from impedance measurements carried out at a suitable reference plane close to the device. At microwave frequencies and above, it would be futile to attempt direct measurement on unmounted devices since the probe and mount parasitics seriously alter the measured impedance. An indirect method is therefore essential.

This chapter discusses some of the key techniques used in de-embedding device characteristics from microwave measurements. Particular reference is made to techniques as well as mounts and packages suitable for RTD microwave characterisation. Some of the techniques and the coaxial mounts described here were used with success, in particular the equivalent circuit representation of a hitherto uncharacterised package (the E10/A) housed in a novel mount, as is described in Chapter 4.

3.2 De-embedding devices

As with all other solid state devices such as IMPATT, GUNN, BARRIT, etc., a resonant tunnelling device has to be placed in a suitable microwave package (at least for operation below about 100GHz) for ease of handling and to prevent contamination of the chip by dust etc. One suitable, well-known package is the S4 shown schematically in figure 3.1 (some devices used in the present study were mounted in similar packages). In addition, the package must somehow be connected into the microwave circuit. That part of the circuit which connects the packaged device to a suitable reference plane in the microwave circuit is here referred to as the mount.

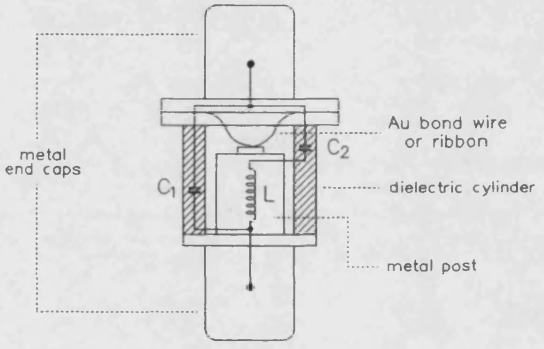


Figure 3.1. Cross-section of an S4 microwave package showing the equivalent circuit due to Roberts and Wilson (Ref. [3]).

The design of microwave circuits containing active devices (oscillators, mixers, multipliers, etc.) involves matching the impedance of the (sometimes packaged) device to a known load in a controlled fashion. Hence the input impedance presented by the active device must be known. Unfortunately, the combination of package and mount modifies the chip impedance considerably. As an example, figure 3.2 shows the active chip admittance of a hypothetical Gunn device

and the admittance seen at a reference plane in a 50Ω coaxial line with the device in an S4 package. These admittances were calculated assuming

a. the device admittance to be given by
   $Y_d = G + j\omega C$
   where G and C are respectively the device conductance and capacitance,
b. a lumped-element equivalent circuit for the package and mount discontinuities due to Owens [1].

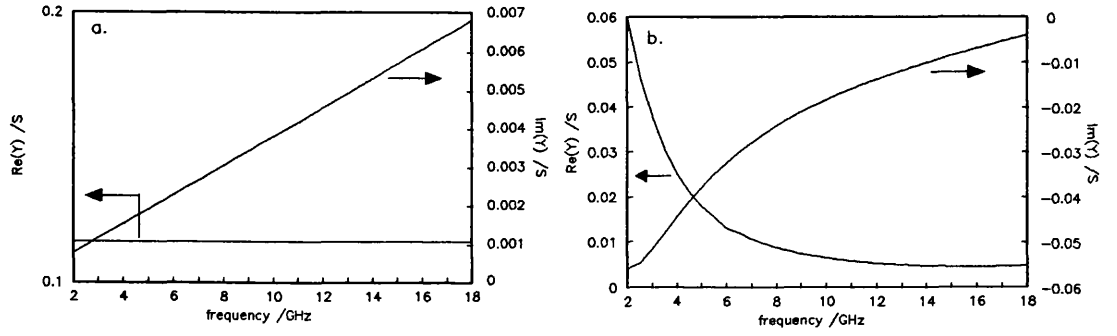


Figure 3.2. (a) Admittance of a Gunn device with low-field conductance 115mS and dielectric capacitance 0.06pF. (b) Admittance seen at a suitable reference plane in a 50Ω coaxial line with the device embedded in an S4 package mounted against a back short. The curve (b) was calculated assuming the package and mount equivalent circuit due to Owens (Ref. [1]).

The transformation due to package and mount is dramatic. A knowledge of the transformation is therefore required before the chip admittance can be inferred from microwave admittance measurements at a chosen reference plane, or before the input admittance of a packaged chip of known admittance can be determined.

De-embedding is the process of deducing the impedance of a device under test from measurements made at a distance, when the electrical properties of the intervening structure are known. Thus, the first problem encountered is that of

characterising the package and mount discontinuity. There are two main schools of thought as to how this problem may be approached. The first involves the synthesis of lumped-element equivalent circuits for the mount and the package. The second represents the package and mount by a two-port network where one port is at the reference plane and the device (essentially a two-terminal one) is connected across the other. In the former case, the synthesis of a representative equivalent circuit of the mount and package is no easy matter, especially if the circuit is to be used at high frequencies and/or over a wide band of frequencies. However, valuable knowledge about the relative contributions of mount and package to the overall transformation is gained in the process. Two-port network representation, on the other hand is unique to a specific mount configuration and package and by its very nature will not convey any notion of the relative importance of mount and package on the reference plane impedance. Indeed, this method will be suitable only if de-embedding the active device is the primary objective. In any case the intervening structure between the reference plane and the actual device must be characterised prior to attempting measurement of the device at microwave frequencies. If we refer to this process as unterminating, then unterminating the package and mount discontinuities can be achieved either by lumped-element equivalent circuit modelling or by determining the ABCD matrix of a two-port equivalent network. These two methods will now be briefly reviewed.

3.2.1 Lumped-element equivalent circuit synthesis

The S4 and similar microwave packages have been the most popular and most widely studied of all (dc to ~20GHz) packages presently available. Gunn devices mounted in S4 packages are available and are well suited to half-wave coaxial-cavity

oscillators [2]. It had originally been assumed that the package may be represented by a lumped element low-pass π-network of the form indicated in figure 3.1.

The physical significance of the individual components of figure 3.1 may be explained by reference to Roberts and Wilson [3]. C_1 is the capacitance between the lower portion of the post, through an air gap and the ceramic ring to the top cap, and C_2 is the capacitance from the top of the post, through an air gap and the ceramic ring to the top cap. According to Roberts and Wilson [3], the inductance of the lead wire appeared to be negligible, but Owens and Cawsey [4] found it necessary to include this effect in their proposed package equivalent circuit. The parameters of this circuit were shown to be variant with change in measuring frequency, mount geometry and active device impedance [4].

Getsinger [5] retained the basic π circuit and derived additional components for mount geometry. This was achieved by subdividing the volume between chip and measurement plane into small regions each described by a lumped element circuit. Figure 3.3a illustrates the sub-regions chosen by Getsinger in deriving the equivalent circuit for the coaxial mount shown in figure 3.3c.

The subregions comprise

- **A** - a coaxial line segment,
- B - a radial line segment, and
- C - a transition region with distorted electric and magnetic fields (figure 3.3b).

A. Coaxial line segment

Assuming a lossless coaxial segment of small volume, the equivalent circuit of figure 3.4a may be used with **L** and **C** being the coaxial inductance and capacitance per unit length [6].

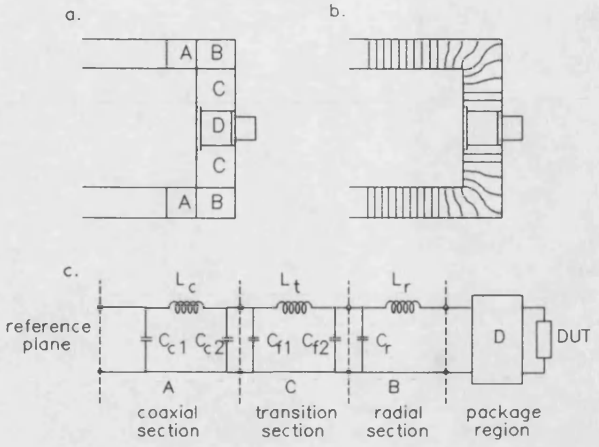


Figure 3.3. (a) Getsinger's sub-regions for the coaxial mount. (b) Electric fields in the sub-regions. (c) Coaxial mount equivalent circuit.

B. Radial line segment

Figure 3.4b represents a section of radial line. Assuming dominant mode propagation (i.e. TEM), the characteristic impedance is a function of radial position. Assuming an incremental model for a length of radial line much less than one wavelength, the equivalent circuit shown in figure 3.4c was derived to represent the resulting impedance transformation, with the circuit elements being the coaxial inductance and parallel capacitance [6].

C. Transition region

The electric field pattern in this region (figure 3.3b) is distorted, while the magnetic field can be assumed to approximately retain its coaxial form. Hence the equivalent circuit inductance for this region may be approximated by assuming a coaxial inductance as if the centre conductor were extended to the end wall. The fringing capacitances C_{f1} and C_{f2} (figure 3.3c) used to describe the electric fields in this region are difficult to calculate. Approximate equations are provided by Getsinger [5].

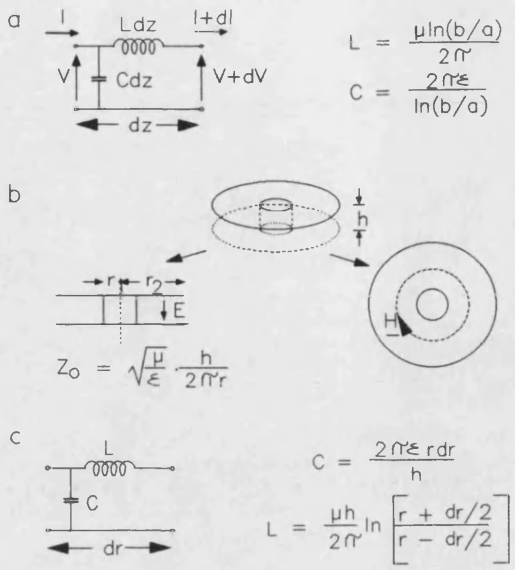


Figure 3.4. (a) Incremental coaxial line equivalent circuit. (b) Radial line section. (c) Incremental radial line equivalent circuit (Ref.[6]).

Combining the circuits just discussed results in the equivalent circuit of figure 3.3c for the complete mount. L_C and L_t are coaxial inductances. $(C_{c1} + C_{c2})$ is the equivalent coaxial capacitance. For a standard S4 package in a 50Ω 7mm coaxial line, Getsinger's equations [5] for C_{f1} and C_{f2} give 0.1pF and 0.043pF respectively. Owens [1] obtained values of 0.01pF and 0.043pF. An accurate finite difference method [6] gave a total capacitance of 0.067pF for this region. Hence, Owens' values are in better agreement with accurately computed values. Finally, L_r and C_r are the radial line elements since the radial line length is usually much smaller than a wavelength.

3.2.1.1 Package equivalent circuit

In general the greater the frequency range over which the equivalent circuit is to be applied, the more elements are required. The distorted package fields may be represented approximately by equivalent circuit elements related to

physical package features. It is not always possible and indeed desirable to do so but some justification for the common forms of the circuit can be obtained in this way.

Attention is here focussed on the form of package equivalent circuit used by Owens [1]. Figure 3.5a shows this circuit. L_1 represents the coaxial post and L_2 the bonding wire inductance. C_1 and C_2 refer respectively to the capacitance of the dielectric spacer bounded by the metal end caps and the capacitance from post to top cap. This circuit with the values determined by Owens (see table 3.1) was shown to be usable to 20GHz [1].

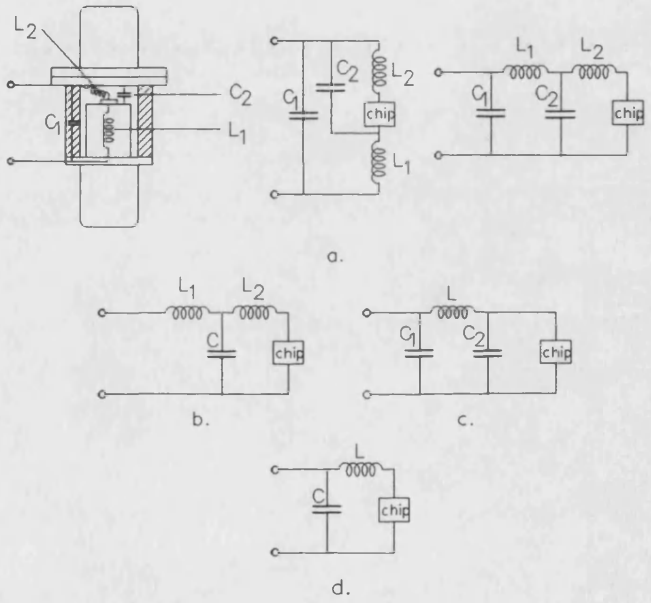


Figure 3.5. (a) S4 package equivalent circuit (Owens Ref. [1]) (b) T equivalent circuit obtained by interchanging the positions of L_1 and C_1 and combining C_1 with C_2 in (a) (Ref. [7]). (c) π equivalent circuit produced by interchanging L_2 with C_2; L represents the total package inductance. (d) interchanging L_1 and C_2 in (b) results in this L equivalent circuit [6].

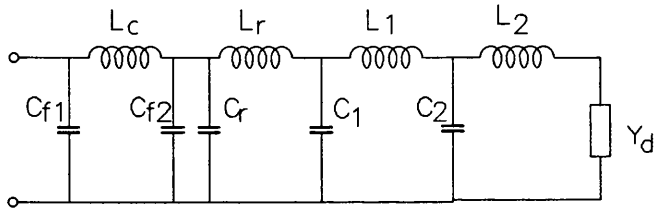
This circuit can be simplified at lower frequencies. The impedance transformation due to a series L and shunt C combination remains approximately invariant when the order in which they appear in a circuit is reversed, provided that $\omega^2 LC \ll 1$. Hence the positions of L_1 and C_1 in figure 3.5a were interchanged and C_1 combined with C_2 to produce the circuit of figure 3.5b [7]. Similarly, if the positional order of L_2 and C_2 is reversed in figure 3.5a, the circuit of figure 3.5c results in which L now represents the total package inductance.

Finally, by interchanging L_1 and C_2 in figure 3.5b, the simple circuit of figure 3.5d is obtained [6]. This circuit is only accurate over a narrow frequency range but may be utilised to identify the principal resonances in the device-package interaction.

Various methods have been used to determine the package equivalent circuit elements, the most frequently cited work being due to Owens and Cawsey [4]. They assumed that the S4 package was lossless and used various internally short- and open-circuited dummy packages to derive a lumped-element equivalent circuit which eventually led to figure 3.6. The values of L_c, L_r, C_{f1}, C_{f2} and L_d represent the mount and were estimated by calculations based on Getsinger's work [5], while the remaining values, representing the package itself, were derived by a process of curve-fitting to the dummy package measurements.

Table 3.1: Lumped-element S4 package equivalent circuit parameter values

Circuit element[1]	Owens' values [1]
C_1	0.030±0.010pF
C_2	0.195±0.010pF
L_1	0.186nH
L_2	0.167±0.007nH



L_c	0.224nH	C_{f1}	0.01pF
L_r	0.109	C_{f2}	0.043
L_1	0.186	C_r	0.027
L_2	0.167	C_1	0.030
		C_2	0.195

Figure 3.6. Lumped-element equivalent circuit of a coaxially mounted S4 package (Owens, Ref. [1]). Y_d is the device admittance.

3.2.2 Two-port network representation of package and mount discontinuities

Although the techniques outlined in section 3.2.1 give insight into the interactions between mount and package they have their disadvantages in actual practice. Dummy short- and open-circuited packages which closely emulate the embedding characteristics of actual packaged devices at microwave frequencies are difficult to construct. Tolerances in package manufacture and, lack of repeatability of bonding lead shape and length, as well as varying chip sizes and

1 See figure 3.5a.

shapes give rise to a spread in package parasitics. Hence, precise equivalence in dummy- and device-package constructions is difficult to obtain. These factors introduce errors and uncertainties which give rise to the derivation of inaccurate device equivalent circuits. Moreover, the usefulness of an equivalent circuit such as the one of figure 3.6 is limited by the fact that the mount-dependent part is only usable in the configuration of figure 3.3a.

Another measurement technique, suitable for oscillators, makes use of a short-circuted dummy package and direct network analyser measurements to establish the reference plane at the chip terminals [8,9]. Pollard et al. [10] used a 50Ω tapered coaxial line as a probe to measure the admittance looking into the circuit from the position normally occupied by the device. This was achieved by connecting the 7mm end of the probe to a network analyser reflection test unit with the narrow end inserted into an axial hole drilled into a dummy package pedestal. The dummy package was replaced with a packaged Gunn device biased to the required operating point and power and frequency measurements made. The device admittance was then calculated using the basic equation for stable oscillations given by Kurokawa [11].

The latter technique, elegant as it may seem, is quite difficult to apply and has some inherent disadvantages. Although it is technologically possible to construct the probe it is by no means a simple problem to achieve a smooth taper from standard 7mm to less than 1mm coaxial air line; the least non-uniformity gives rise to significant inaccuracies, especially at high frequencies. Furthermore, the geometry of the package is altered by the pedestal hole and the presence of the probe, giving rise to fringing fields which perturb the package parasitics.

3.2.2.1 Basic technique

The measurement techniques considered so far have been applied mainly for the characterisation of transferred electron devices (TED's). Their common feature is that the de-embedding procedure is based on measurements of particular configurations of dummy packages. An important technique which is described in detail in this section was proposed by McBretney and Howes [12]. This technique avoids the use of dummy packages and leaves the microwave circuit physically undisturbed throughout the measurement procedure.

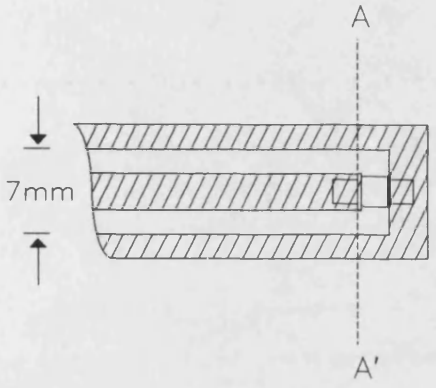


Figure 3.7. 7mm coaxial mount configuration for an S4 package. The package rests against a back short.

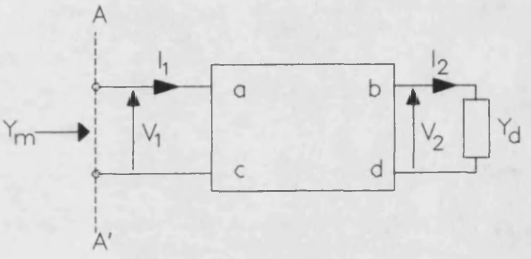


Figure 3.8. Equivalent two-port network representation of package and mount in figure 3.7. a, b, c and d constitute the transfer matrix which enables transformation of the device admittance from chip to measurement plane AA'.

A suitable mount configuration for an S4-packaged device is shown schematically in figure 3.7. It is relatively easy to modify a 7mm N-type female jack and male back short combination to take the S4 package as shown since the latter fits tightly into the centre conductor recess (see section 3.3). Now, by removing the package and terminating the mount with a standard back short, the reference plane AA' (figure 3.7) may be established by reflection measurements with a network analyser. The mount to the package side

along with the package itself may then be represented by the two-port network of figure 3.8, which is terminated by the device admittance Y_d [12,13]. $\begin{pmatrix} a & b \\ c & d \end{pmatrix}$ refer to the transfer matrix of the two-port network such that the currents and voltages are related by [12]

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} a & b \\ c & d \end{pmatrix} \begin{pmatrix} V_2 \\ I_2 \end{pmatrix} \qquad \textbf{(3.1)}$$

Expanding **(3.1)** and dividing to obtain the admittance Y_m looking into the plane AA' gives

$$Y_m = \frac{I_1}{V_1} = \frac{cV_2 + dI_2}{aV_2 + bI_2} \qquad \textbf{(3.1)}$$

Hence,

$$Y_m = \frac{c + dY_d}{a + bY_d} \qquad \textbf{(3.2)}$$

Dividing the right hand side of **(3.3)** by d reduces this equation to

$$Y_m = \frac{C + Y_d}{A + BY_d} \qquad \textbf{(3.3)}$$

where A, B and C are now the complex and frequency dependent transfer parameters characterising the two-port network. Y_m can be measured directly with a network analyser. If this is done for three known values of Y_d in the frequency range of interest, then A, B and C can be solved simultaneously at each frequency. The problem is thus reduced to establishing known reference chip admittances. For the case of TED's, McBretney and Howes used the geometric magnetoresistance effect [14,15,16] whereby the application of a transverse magnetic field to a bulk semiconductor of suitable aspect ratio [17] (see note at the end of this

section) results in a decrease in its low field conductance G_o. McBretney and Howes have demonstrated that G_o remains constant at least up to about 20GHz. The measurement technique consisted basically in obtaining Y_m in the frequency range of interest (2 - 18GHz) with the packaged and mounted device in a transverse magnetic field at three different flux densities between 0 and 2.5T. G_o was measured for each field setting using a resistance bridge.

If the Gunn device admittance can be modelled by a conductance G_o in parallel with a capacitance C_o, then from **(3.3)**,

$$Y_{m1}\{A+B(G_{01}+j\omega C_0)\} = C+G_{01}+j\omega C_0 \qquad \textbf{(3.4)}$$

$$Y_{m2}\{A+B(G_{02}+j\omega C_0)\} = C+G_{02}+j\omega C_0 \qquad \textbf{(3.5)}$$

$$Y_{m3}\{A+B(G_{03}+j\omega C_0)\} = C+G_{03}+j\omega C_0 \qquad \textbf{(3.6)}$$

where the numeric subscripts refer to the different magnetic field settings. Simultaneous solution of **(3.4)**, **(3.5)** and **(3.6)** at each measurement frequency effectively characterises the two port network, providing that a reasonable estimate of C_o is available. In this respect, McBretney and Howes assumed C_o to be the dielectric capacitance and estimated it from the electrical parameters of the device by using,

$$C_0 \approx \frac{\epsilon G_0}{e n_0 \mu_0} \qquad \textbf{(3.7)}$$

where μ_0 and G_0 are the low field mobility and conductance respectively (in the absence of a magnetic field), ϵ is the permittivity and n_0, the dopant concentration in the active layer.

If the device is removed from the magnetic field and biased to the required level, measurement of Y_m will enable the transformation to be made to the chip itself, thus determining Y_d.

The problem encountered in de-embedding a RTD in a microwave circuit by means of the two-port network representation is that of obtaining three known reference chip admittances. An identical approach to that used by McBretney and Howes cannot be used here because this approach pre-assumes the small-signal equivalent circuit model of the device. Furthermore, magnetotunnelling experiments with B parallel [18,19] and perpendicular [20,21,22] to J, carried out on double barrier RT heterostructures have demonstrated that there is little, if any, change in conductance, even at high magnetic fields, with the device biased below the resonant tunneling region. Indeed, these works have only shown a weakening and shifting to higher voltages of the features in the I-V characteristics. Moreover, since the capacitance varies appreciably with bias voltage, this situation is made even more difficult.

It may be possible and indeed fruitful, once an accurate device equivalent circuit has been established (at least at three distinct bias voltages), to apply a similar technique where the reference admittances are, instead, obtained by changing the device bias voltage. This would effectively eliminate the need for dummy packages and would lead to the determination of accurate small- and large-signal measurements.

Note: Aspect ratio for enhanced geometric magnetoresistance effect

Under strong magnetic fields, a significant increase in the resistivity of a bulk semiconductor is observed. For spherical energy surfaces the ratio of incremental resistivity to the bulk resistivity at zero magnetic field is approximately [15]

$$\frac{\Delta\rho}{\rho_0} \approx \mu_n^2 B^2 \qquad \text{(a)}$$

where μ_n is the drift mobility for a semiconductor with $n \gg p$ and B is the magnetic field component perpendicular to the direction of current flow.

Equation (a) should hold for a specimen of infinite extent. The effect of the shape of the specimen on $\Delta\rho/\rho_0$ is very significant [16]. It was shown by Willardson and Beer [17] that, for a square sample of side l and thickness d to give $\frac{\Delta\rho}{\rho_0}$ values approaching the theoretical, $l/d \ll 1$. Now, for most Gunn devices, the active layer thickness is between 2 and $8\mu m$ and the surface dimensions between about 50x50 and $100x100\mu m$. Hence, the aspect ratio of most TED's is suitable for the observation of marked geometric magnetoresistance effects with fields of below $\sim 2T$.

3.3 The S4-type package mount

The mounting arrangement shown schematically in figure 3.7 may in practice be obtained by a simple modification of a standard 7mm male N-type back short. Figure 3.9 shows the design. Use of 7mm N-type configurations facilitates design of coaxial mounts for S4 packages since the top and bottom caps fit tightly into the centre conductor recess on female jacks.

The centre pin of the standard back short was drilled out and substituted with the spring-loaded plunger arrangement shown. This plunger serves as a back short and pushes forward on the package so as to maintain good electrical contact.

The actual package used for mounting the first RTD's tested was the LEW Techniques[1] type E3 with C1/S covers, which is almost identical to the S4 package. Hence the lumped-element equivalent circuit of figure 3.6 was used with Owens' [1] parameter values, except for the value of L_2, the bond wire inductance, which was calculated from the known wire length and diameter.

1 **LEW Techniques Ltd**, 99 Taunton Trading Estates, Taunton, Somerset, England.

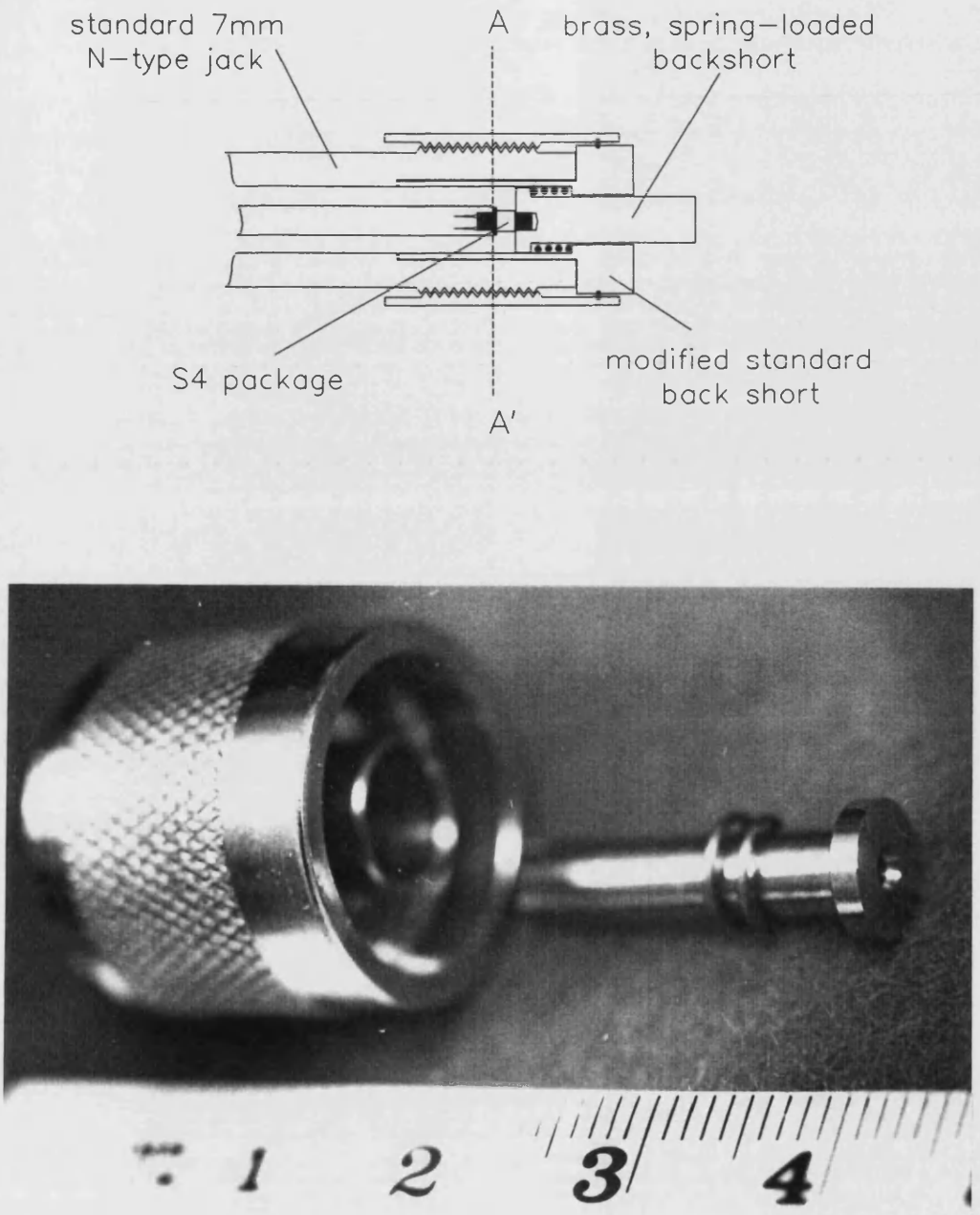


Figure 3.9. 7mm coaxial mount obtained by modifying a standard male N-type back short. The spring-loaded plunger pushes on the S4 package to ensure good electrical contact. Top: cross-section schematic, bottom: photograph of the actual mount.

3.4 The E10/A microwave package

Figure 3.10a shows details of the LEW Techniques E10/A microwave package used for mounting some of the later resonant tunneling devices tested. This package was chosen because its dimensions are such that it can be incorporated in a 3.5mm coaxial system. The main advantage of this system is a practical one since the HP8510B network analyser available for the reflection measurements on RTD's, as described in chapter 4, had 3.5mm test ports. However, another advantage stems from the diameter of the post flange (1.30 ± 0.05mm) which is almost identical to the standard 50Ω sma centre conductor diameter (1.27 ± 0.03mm). It was intended to mount this package so that the pedestal fitted into the centre conductor of an sma jack such that the package terminates the line. Thus, the dimensions of the mounting configuration were such that a radial mode could not be established as in the S4-type package terminating a 7mm line [1,5], a fact which would simplify the mount-package equivalent circuit.

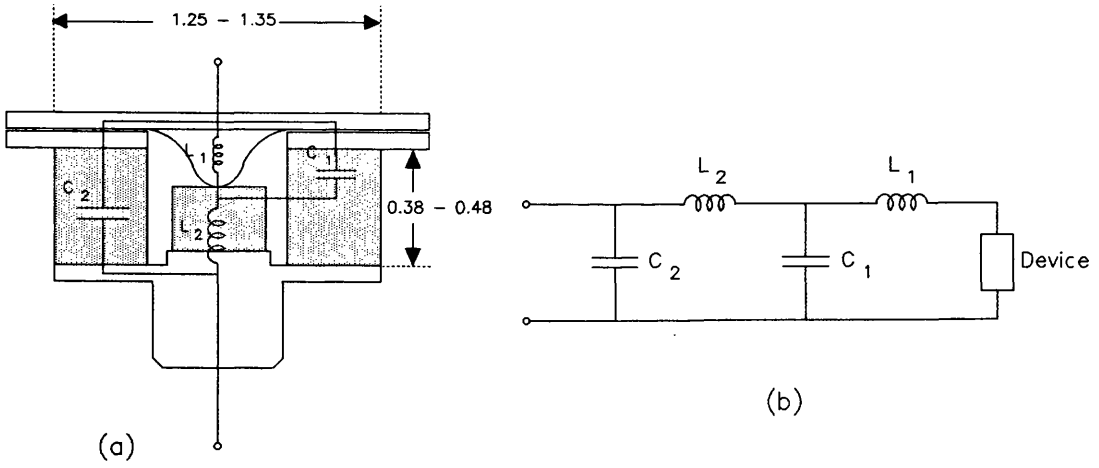


Figure 3.10. Cross-section of the LEW Techniques E10/A microwave package with chip mounted and stitch-bonded (a), dimensions are in millimetres. The figure shows idealised parasitic elements L_1, L_2, C_1 and C_2. The equivalent circuit is redrawn in (b) for clarity.

The following sections describe the construction of the backshort mount and the package-mount characterisation performed in order to establish an effective equivalent circuit.

3.4.1 The 3.5mm backshort mount

Figure 3.11 shows schematically the mounting configuration and gives technical details of the spring-loaded backshort constructed to house the E10/A package inside a 3.5mm system. The backshort presses the package down to make good electrical contact with the centre conductor and provide the other contact through the outer conductor.

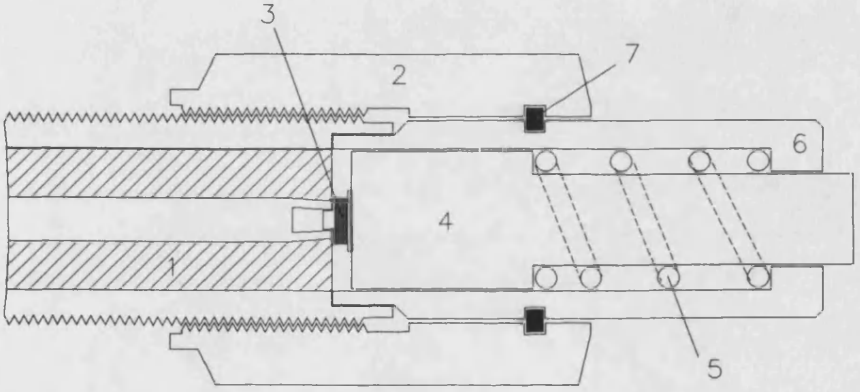


Figure 3.11. Schematic representation of the mounted E10/A package showing the spring-loaded backshort construction. Key: 1. standard sma jack; 2. standard sma nut; 3. package fitted into centre conductor; 4. backshort; 5. helical spring; 6. backshort housing; 7. spring washer.

The only drawback to the use of this package in this configuration is that the pedestal diameter is smaller than that specified for a standard sma plug (0.62 ± 0.01mm as opposed to 0.91 ± 0.01mm). Therefore the pedestal fits rather loosely inside the centre conductor, a fact which renders connection repeatability questionable.

3.4.2 Package-mount equivalent circuit

In early work on the S4 microwave package, Owens [1] established a mount-independent equivalent circuit which fitted well over the 4 to 23.5 GHz test frequency range with measured admittances of short- and open-circuited packages. His analysis was based on Getsinger's approach of subdividing the mount into regions. Figure 3.12a represents these regions schematically.

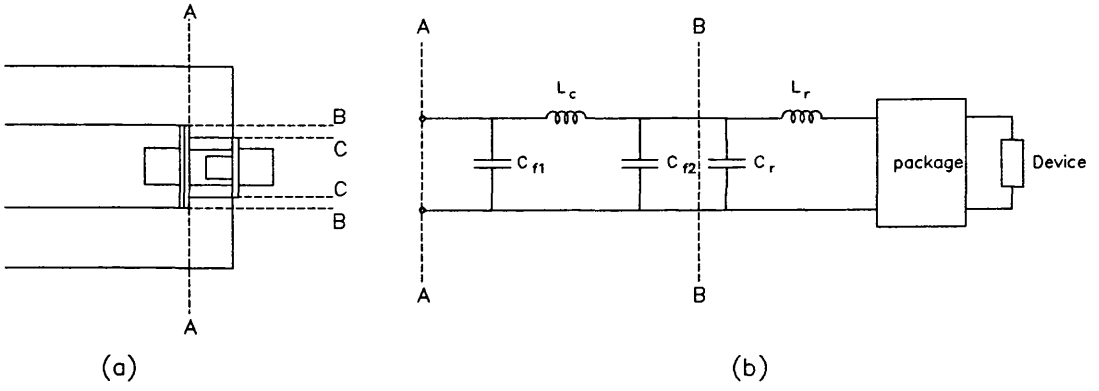


Figure 3.12. (a) Schematic representation of the S4 package in a 7mm coaxial system terminated by a backshort showing subdivision into coaxial (A-B) and radial (B-C) sections. (b) The lumped-element equivalent circuit (figure 3.6) proposed by Owens to represent these sections [1]; the package section is here represented by an unknown network.

According to Owens a radial mode exists within the region bounded by the surface BB whilst the fields transform into a coaxial mode between this surface and the plane AA. This approach suggests that if it is assumed that the radial mode is fully developed at the package boundary surface CC formed by the surface of the ceramic, then tangential **E** fields must exist either side of CC. Hence an equivalent circuit representation where all circuit elements inside CC are regarded as package-dependent and all elements outside as mount-dependent is possible [1]. This reasoning leads to the equivalent circuit of figure 3.12b. The coaxial line

section is represented by a coaxial inductance L_c flanked by fringing capacitances C_{f1} and C_{f2} and the radial-line section by an inductance L_r and capacitance C_r.

Now, in the case of the E10/A package in the mount of figure 3.11, the diameter of the ceramic ring is approximately equal to that of the 50Ω, 3.5mm coaxial line. Thus, although the E10/A and S4 packages and their respective mounts are similar (except for the dimensions), the assumption of a radial-line section for the E10/A mount is unjustifiable. Consequently it is not an easy matter to separate the equivalent circuit into a package-dependent part and a mount-dependent part, because there must be some interaction between the two along the ceramic ring surface.

The true field distribution within the package and in the area immediately surrounding must be extremely complex. However, one can still attempt to represent the package equivalent circuit as shown in figure 3.10b, where the package elements would have the following significance **assuming no mount-package interaction**:

- L_1: inductance of bond wire
- L_2: inductance of the protruding post and chip
- C_1: capacitance between the chip surface, through an air gap and the ceramic ring, and the top cap
- C_2: capacitance between the pedestal flange, through an air gap and the ceramic ring, and the top cap.

Since it has been assumed that there is no radial-line section in the E10/A package mount, the package equivalent circuit elements must be effected by the mount. The π-section including L_2 flanked by C_1 and C_2 would now represent a coaxial-line section. L_2, C_1 and C_2 for the package regarded as a purely radial-line structure would be different. The true field situation lies somewhere between these two extremes and is effected significantly by the presence of a device chip of dimensions comparable to the package internal

dimensions. It is therefore not unreasonable to assume the radial-line structure as a starting point and treat the equivalent circuit elements as perturbed values, specifically that the series inductances and shunt capacitances are distributed differently. In this case there would be no need to consider mount and package separately and the resulting lumped element equivalent circuit representation would be simplified considerably.

3.4.3 Determination of the lumped equivalent circuit elements

The experimental procedure adopted for the determination of the package-mount equivalent circuit parameter values was similar in principle to that of Refs. [1], [2], and [4]. Reflection measurements were made over 0.5 to 13 GHz on four types of structure using an HP8510B network analyser calibrated at the package plane using a broadband and a sliding load as well as standard open and short circuits. The structures tested were the following:

1. empty package
2. dummy solid package
3. dummy open-circuited package
4. dummy short-circuited package

3.4.3.1 Measurements on the empty packages

For this structure the equivalent circuit of figure 3.10b would be reduced to just the capacitance C_2. Hence, the admittance looking into the package from the measurement plane should be the susceptance of C_2.

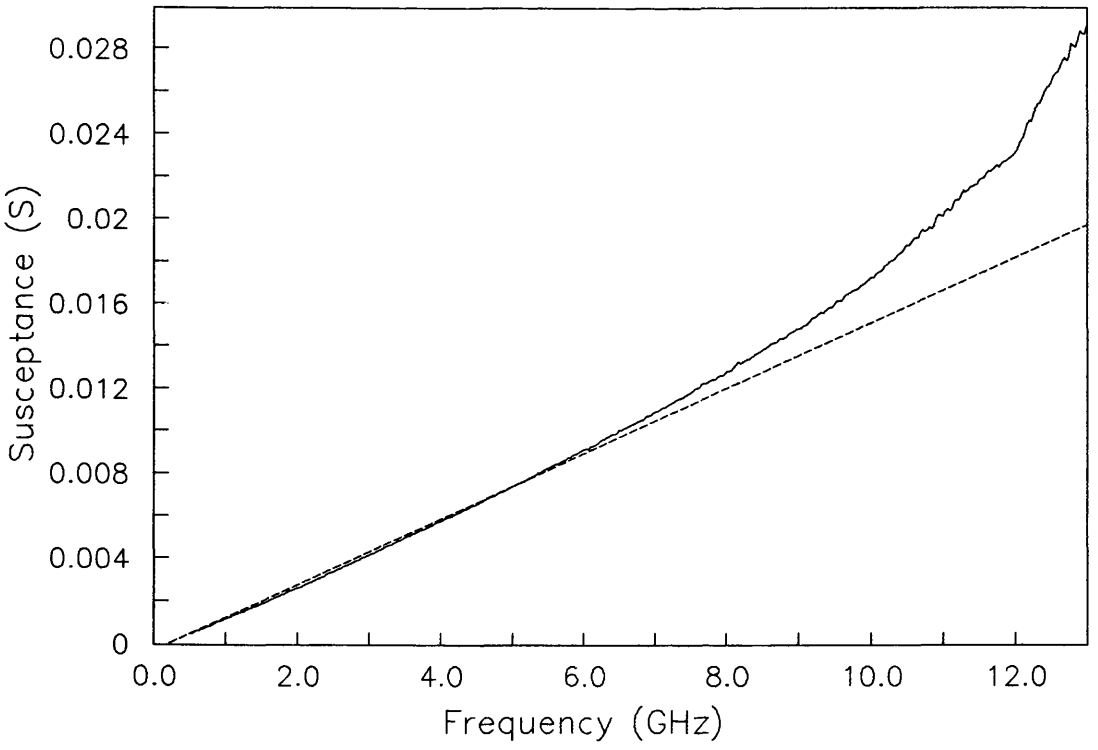


Figure 3.13. Measured susceptance of an empty E10/A package (mean over three packages). The dashed line represents the results of linear regression performed between 0.5 and 4 GHz.

Figure 3.13 shows measured susceptance of an empty E10/A package. Five packages were tested and the average of three of these is shown here. The measured data from the other two showed evidence of a parallel resonance between 8 and 10 GHz. Now, figure 3.13 shows a nonlinearity beyond about 6 GHz, an effect which may be due to a finite resistance path through the ceramic, weakly coupling L_2 across C_2. This would explain the presence of the observed resonances in the two above-mentioned packages as being due to relatively poorer insulation of the ceramic ring, possibly through surface contamination.

C_2 was found to be 0.0285 pF as a result of linear regression performed over 0.5 to 6 GHz

3.4.3.2 Measurements on the dummy solid package

The dummy solid package consisted of a gold plated brass cylinder of the same diameter as the E10/A. An LEW Techniques C10 cover (identical to the ones used for the packaged devices) was soldered to this structure which also had a plug on the other end to fit into the centre conductor of the network analyser 3.5mm test port jack. The purpose of this dummy package was to estimate the package inductance L_2, as proposed by Getsinger [5]. Thus, since the package diameter is practically the same as that of the centre conductor, the fringing capacitance at the measurement plane would be small and the other end would be in contact with the backshort. Thus, impedance measurements at the lower frequencies, where the effects of any fringing capacitances would be minimal, should yield L_2 approximately. Figure 3.14 shows the results of impedance measurements between 0.5 and 4.0 GHz. At these frequencies, the structure has an almost purely inductive nature. The slope in figure 3.14 gives L_2 as 0.252 nH.

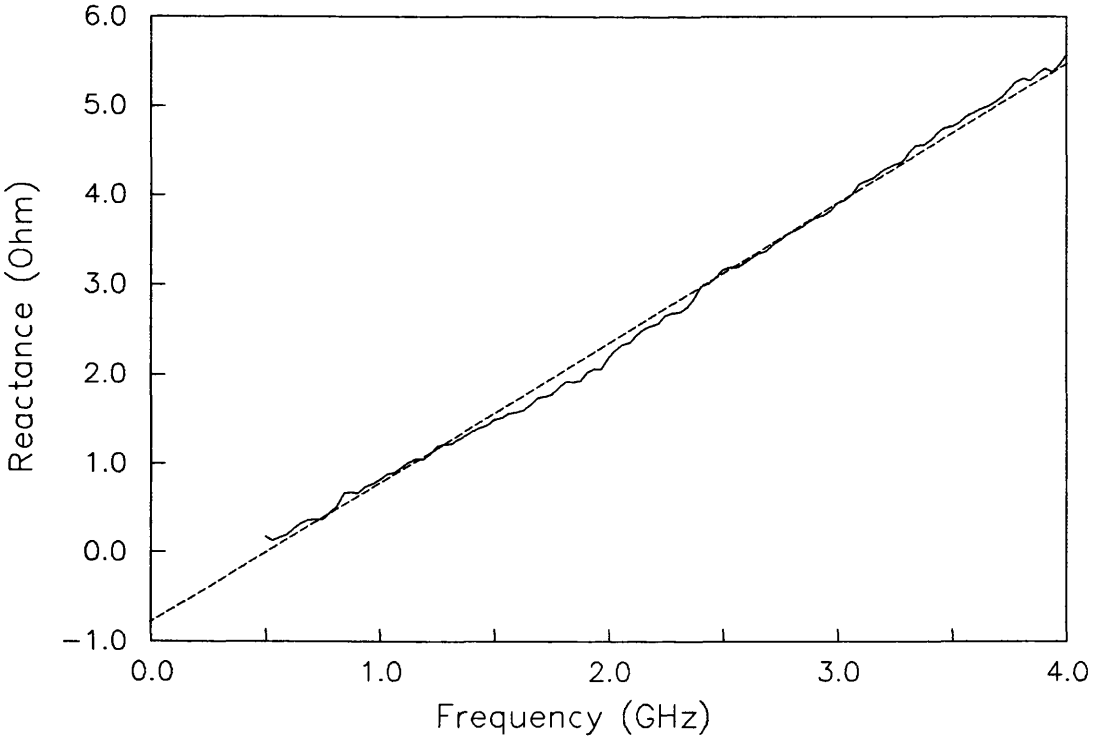


Figure 3.14. Measured reactance of the dummy solid package between 0.5 and 4 GHz. The dashed line represents the linear regression performed on the experimental data within this range. The inductive nature of the structure is evident.

3.4.3.3 Measurements on the dummy open-circuited package

An open-circuited dummy package was assembled where an attempt was made to emulate the real situation by soldering an actual test chip to the post. A 12.5μm diameter gold wire was bonded across the package flange and the middle left close to but not touching the central device area. The equivalent circuit of this configuration is represented in figure 3.15. In an actual packaged device, the bond wire perturbs the field in its vicinity. It was thus hoped that the presence of this wire in the open-circuited package would represent the real situation more closely.

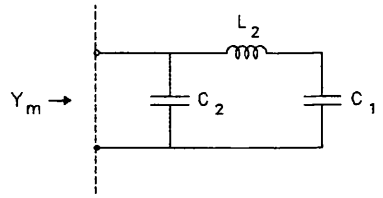


Figure 3.15. The lumped-element equivalent circuit of the dummy open-circuited package, obtained by eliminating L_1 and the device from the circuit of figure 3.10b.

From figure 3.15, the admittance measured at the reference plane is given by

$$Y_m = j\omega C_2 + \left(\frac{1}{j\omega C_1} + j\omega L_2 \right)^{-1}$$

Re-arranging, we have

$$\frac{1}{Y_m - j\omega C_2} - j\omega L_2 = -\frac{j}{\omega C_1} \qquad \textbf{(3.8)}$$

Figure 3.16 shows a plot of the left hand side of **(3.8)** versus $1/\omega$, the slope of which gives $1/C_1$. Linear regression was performed separately over the ranges 0.5 - 2, 2 - 6, 6 - 10, 10 - 13 and 0.5 - 13 GHz. The results are given in table 3.2.

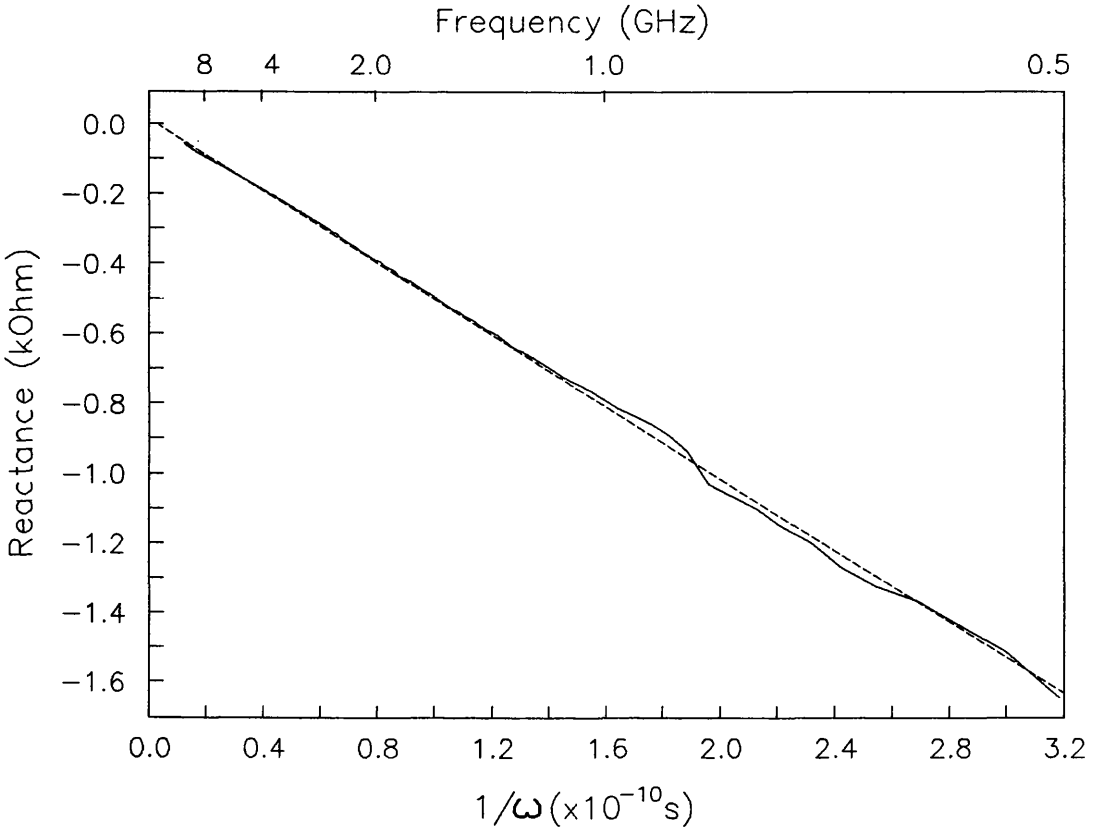


Figure 3.16. A plot of $1/(Y_m - j\omega C_2) - j\omega L_2$ versus $1/\omega$. The dashed line represents the result of linear regression over the entire frequency range (0.5 - 13 GHz). The slope is $-1/C_1$.

Table 3.2: Estimated values of C_1 in different frequency ranges

Range (GHz)	Value of C_1 from slope of fig. 7 (pF)
0.5 - 2	0.197
2 - 6	0.208
6 - 10	0.219
10 - 13	0.170
0.5 - 13	0.196

Figure 3.17 shows the measured open-circuited package admittance over the test frequency range. Also shown (dashed line) is the calculated admittance using the equivalent circuit of figure 3.15 with L_2 = 0.252 nH, C_1 = 0.196 pF and C_2 = 0.0285 pF. The fit to the experimental data is reasonably good up to about 8 GHz, beyond which the measured admittance curves upwards at a higher rate. The dotted line represents the result of the same calculation with values of L_2 = 0.285 nH, C_1 = 0.215 pF, C_2 = 0.0285 pF. On the basis of this model, these values gave the best fit to the experimental data; good agreement is observed between the measured and simulated admittance up to about 11 GHz. The reason for the marked divergence of the experimental admittance beyond about 12 GHz is not obvious. It may be due to improper optimization of the network analyser over the entire test frequency range or a poor quality connection at the test port (possibly the slightly loose fit of the package in the mount resulting in it not being properly centralised).

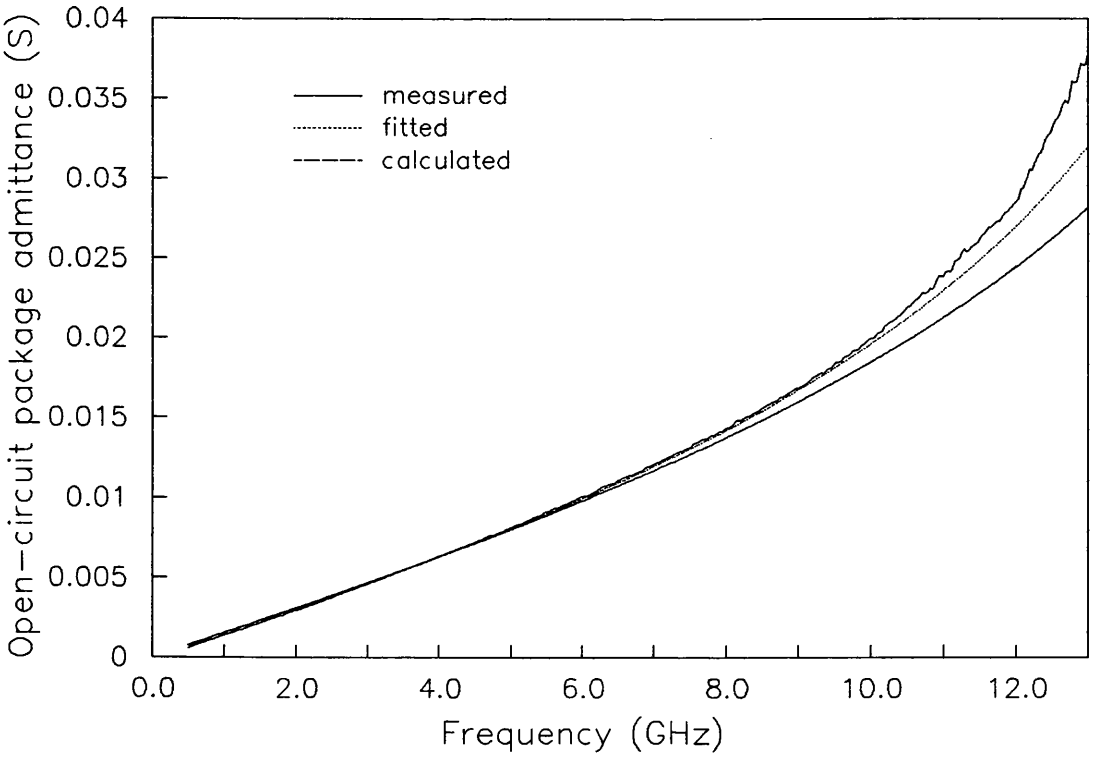


Figure 3.17. Measured admittance of the open-circuited dummy package (solid). The dashed curve was calculated using the previously determined values of L_2 = 0.252 nH, C_1 = 0.196 pF and C_2 = 0.0285 pF. The dotted line shows the fitted curve with L_2 = 0.285, C_1 = 0.215 pF and C_2 = 0.0285 pF.

3.4.3.4 Measurements on the dummy short-circuited package

The last set of measurements were made on a dummy short-circuited package. Gold was evaporated onto the surface and the four cleaved sidewalls of an actual test chip. The chip was then soldered (back ohmic contact face down) into an E10/A package. A 12.5 μm diameter gold wire was then attached in the usual stitch-bond manner spanning across the top package flange and fixed to the centre of the Au-coated chip surface. The package was completed by

capping it with the C10 cover (see Appendix III for details of device processing and packaging). The dc package resistance was found to be less than 1 Ω.

Figure 3.18a represents the short-circuited package equivalent circuit, which is the circuit of figure 3.10b with the device shunted. The impedance transformation due to a series **L** and shunt **C** combination remains approximately invariant when the order in which they appear in a circuit is reversed, provided that $\omega^2 L\,C \ll 1$. Now, for $\mathbf{L_2}$ and $\mathbf{C_1}$ as determined above, $\omega^2 L\,C \approx 0.008$ at 2 GHz. Hence, the positional order of $\mathbf{L_2}$ and $\mathbf{C_1}$ in figure 3.18a may be reversed to give figure 3.18b, where $\mathbf{L_1}$ and $\mathbf{L_2}$, and $\mathbf{C_1}$ and $\mathbf{C_2}$ have been lumped together into **L** and **C** respectively. Then, the reference plane impedance is given by

$$Z_m = \frac{j\omega L}{1-\omega^2 L\,C}$$

$$\text{i.e.,} \qquad Z_m = (j\omega + \omega^2 C Z_m)L \qquad \textbf{(3.9)}$$

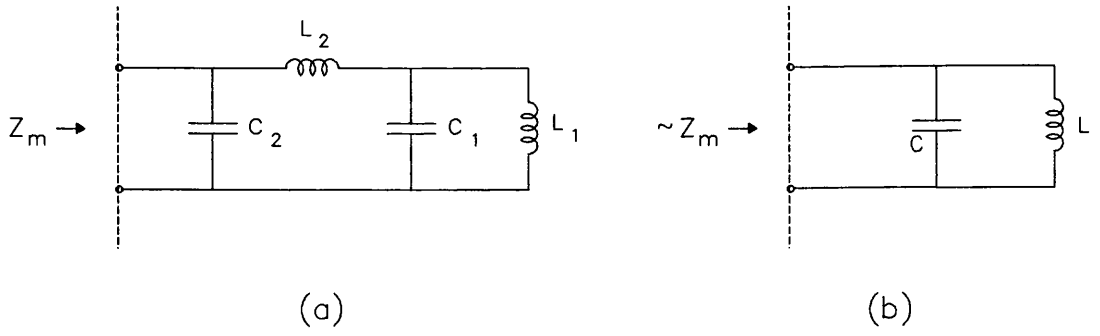


Figure 3.18. (a) The equivalent circuit of the dummy short-circuited package, (b) an approximation of (a) obtained by interchanging the positional order of $\mathbf{L_2}$ and $\mathbf{C_1}$.

A plot of **(3.9)** is shown in figure 10 giving $\mathbf{L}(=\mathbf{L_1}+\mathbf{L_2})$ = 0.373 nH. The value of $\mathbf{L_1}$ (≈ 0.12 nH) obtained by subtraction

of $\mathbf{L_2}$ as determined above is a useful estimate which can be used as an initial trial value in curve-fitting the parameters to simulate the measured short-circuit data.

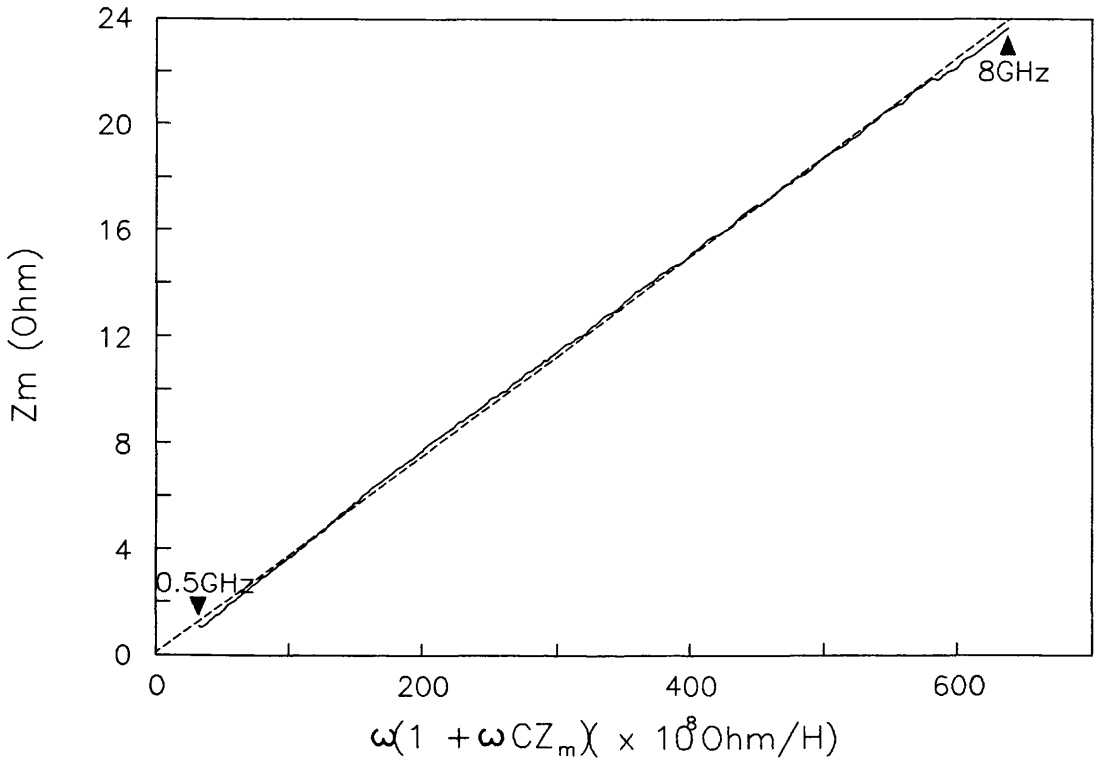


Figure 3.19. Measured reactance ($\Im(Z_m)$) versus $\Im\{\omega(1+\omega CZ_m)\}$, where $C = \mathbf{C_1} + \mathbf{C_2}$ are the determined package capacitances. The dotted line is the result of linear regression; the slope gives $\mathbf{L} = \mathbf{L_1} + \mathbf{L_2}$, the inductance associated with package and bond wire.

Finally, figure 3.20 shows the measured and simulated dummy short-circuited package admittance. The dashed curve was obtained using $\mathbf{L_1}$ = 0.12 nH, $\mathbf{L_2}$ = 0.285 nH, $\mathbf{C_2}$ = 0.0285pF and $\mathbf{C_1}$ = 0.215 pF. The dotted curve was obtained using $\mathbf{L_1}$ = 0.150 nH, $\mathbf{L_2}$ = 0.252 nH, $\mathbf{C_2}$ = 0.0285pF and $\mathbf{C_1}$ = 0.215 pF and assuming a finite conductance by adding 0.8 Ω resistance in series with $\mathbf{L_1}$. The simulated and measured susceptance are virtually coincident and there is also good agreement between the measured and simulated conductance over the test frequency range.

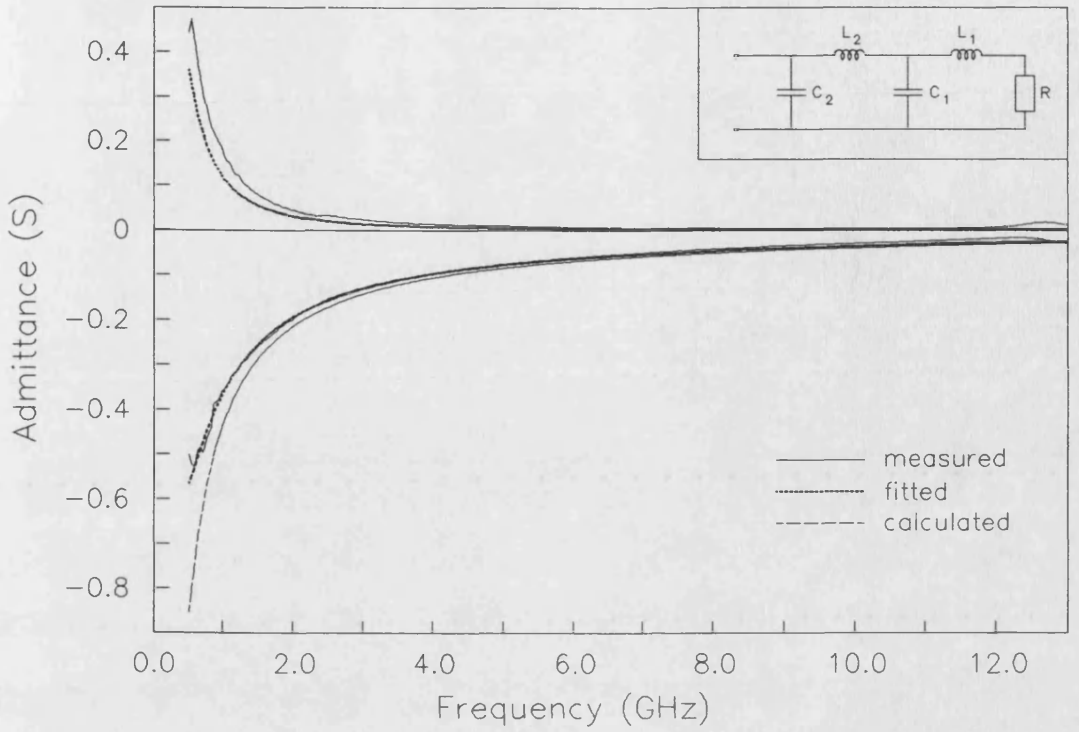


Figure 3.20. Measured admittance (solid line) versus frequency for the dummy short-circuited package. The dashed line was calculated using L_1 = 0.12 nH, L_2 = 0.285 nH, C_2 = 0.0285pF and C_1 = 0.215 pF. The dotted line was fitted to the experimental curve using L_1 = 0.150 nH, L_2 = 0.252 nH, C_2 = 0.0285pF and C_1 = 0.215 pF and R = 0.8 Ω in the circuit shown inset. **R** represents the package resistance, which is finite in practice.

3.4.3.5 Calculated estimates of the package parameters

The bond wire inductance can be estimated by assuming that it is a thin, straight, nonmagnetic conductor in free space with a length much greater than the diameter, but still electrically short (compared with the wavelength). Then, from Longford-Smith [23], the inductance L_w of such a wire is given by

$$L_w = 0.005l\left[2.3\log_{10}\left(4\frac{l}{d}-0.075\right)\right] \ \mu H$$

where l and d are the length and diameter of the wire in inches, or,

$$L_w = 0.453l\log_{10}\left(4\frac{l}{d}-0.075\right) \ nH \qquad \textbf{(3.10)}$$

with l and d in mm. l was estimated to be 0.40mm and d was 12.5 μm, giving $\mathbf{L_W}$ = 0.382 nH. Since a stitch-bond was used, $\mathbf{L_1}$ would be half this value, assuming the bond to the chip occurs in the middle of the wire. This sets $\mathbf{L_1}$ as 0.191 nH, which is of the same order of the fitted value of 0.150 nH.

Assuming $\mathbf{L_2}$ to be a purely coaxial inductance, independent of the ceramic, transmission line theory gives [24]

$$L_c = \frac{\mu h}{2\pi}\ln\left(\frac{d_o}{d_i}\right) \qquad \textbf{(3.11)}$$

where d_o and d_i are respectively the external and internal conductor diameters and h the package length (≈0.91 mm, complete with lid). An estimate of $\mathbf{L_2}$ as $\mathbf{L_C}$ in **(3.11)** gives $\mathbf{L_2}$ = 0.232 nH which agrees well with the measured value of 0.252 nH.

Now, the field situation within the package is bound to be highly complex especially when considering that (a) the internal geometry of the package is significantly altered by the inclusion of a device chip which is large compared with the package dimensions and (b) the presence of the alumina ring (relative permittivity ≈ 9) very close to the post and chip (100-110μm separation). The assumption of $\mathbf{L_C}$ being a coaxial inductance is thus not strictly valid

and should be treated with caution. Any calculation of C_1 and C_2 would, for similar reasons, serve only as a very rough estimate.

An order-of-magnitude estimate of C_1 and C_2 may be made by assuming the region within the package ceramic ring outer surface to be a radial line section. C_1 and C_2 can then be approximated as parallel plate capacitances as suggested by Getsinger [5]. Such estimates give C_1 = 0.34 pF and C_2 = 0.13 pF. Both, not surprisingly, differ significantly from the measured values.

3.4.4 Summary of results

In conclusion, a mount-dependent lumped element equivalent circuit of the LEW Techniques E10/A microwave package in a 50 Ω 3.5mm mount terminated by a backshort has been proposed. Reflection measurements between 0.5 and 13 GHz were made with a network analyser on empty, dummy solid, open- and short-circuited packages leading to estimates of the parasitic elements. The model agrees well with experimental data for the short-circuited package, especially when allowance is made for an imperfect short circuit. The parameter values which gave the best fit are listed in table 3.3.

Table 3.3: Equivalent circuit parameter values for the E10/A package in the mount of figure 3.11

L_1/nH	L_2/nH	C_1/pF	C_2/pF
0.150	0.252	0.215	0.0285

These values are subject to marginal changes from package to package due to manufacturing tolerances. Inconsistent bond wire length and shape is also bound to effect the value of L_1. However, for chips of dimensions comparable to the

internal package dimensions, these changes would be negligible compared with changes in the parameter values brought about by varying chip sizes and shapes. The effect will be mostly on C_1 and C_2 since L_2 has been shown to have a nearly coaxial nature. In this respect, the excellent agreement between the capacitances determined from the dummy open- and short-circuited packages is thought to be due to the choice of chips assembled in the respective packages. These were very carefully selected to have nearly identical dimensions and consequently the procedure was successful in pinning down fairly accurately the values of C_1 and C_2.

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CHAPTER 4

SMALL- AND LARGE-SIGNAL DEVICE EQUIVALENT CIRCUIT MODELS

4.1 Introduction

In this chapter, the measurement of small-signal and large-signal device admittance will be discussed with particular reference to the actual techniques used in this work. Thus, it is worthwhile to discuss briefly what is meant by the two terms.

4.1.1 Small- and large-signal admittance

The admittance (or impedance) of an active microwave solid state device is generally a function of frequency for high rf currents (I_{rf}). However, at very small rf drive levels, the admittance becomes virtually independent of I_{rf} such that the rf current and voltage are linearly related by

$$I_{rf} = Y_d V_{rf} \qquad (4.1)$$

In this region, the device is said to operate in its **small-signal** regime. Oscillators and amplifiers incorporating solid state devices operating under large-signal conditions are perhaps not best described by their small-signal admittance (or impedance) as this is obviously not a faithful description under these conditions. However, small-signal characterisation is useful:

a. for linear amplifier design,

b. for preliminary design of nonlinear circuits such as oscillators,

c. because the admittance is independent of I_{rf} and hence of incident microwave power,

d. the admittance requires low microwave power for its measurement which enables the use of standard network analysers,

e. the small-signal admittance of most solid-state devices can often be quite easily modelled and computed from known physical and electrical parameters, thus facilitating comparisons of theoretical predictions and small-signal measurements which may lead to greater understanding of the device,

f. small-signal equivalent circuits determined over a sufficiently wide bias voltage range may be used in large-signal combined time-frequency domain analysis (see chapter 5).

When I_{rf} is large enough such that any nonlinear region (or regions) of the device characteristic I-V relationship is (are) swept to any significant degree during the rf cycle, the device admittance may become a rapidly varying function of both frequency and signal amplitude. This is often the case with oscillators and frequency multipliers.

4.2 Small-signal measurements

Having distinguished between small- and large-signal device behaviour this section discusses small-signal equivalent circuits of resonant tunnelling devices. Experiments and

analysis leading to the successful determination of the small-signal equivalent circuit model elements between 45 MHz and 13 GHz over a wide range of bias voltages are described. The effect of test signal power upon the measurements is also discussed and shown to be an important consideration.

4.2.1 Small-signal equivalent circuit model of the RTD 523B

The subject of this study was the double barrier resonant tunnelling heterostructure No. 523. This is an MOCVD structure grown by Siemens, the details of which are given in chapter 2. The wafer sections available were 400 μm thick and had a back ohmic contact. They were thus not suitable for mounting into E10/A packages as the gap between the post and top cap is less than 500 μm.

Wafer sections of the 523 heterostructure were lapped down mechanically from the substrate side to about 200 μm thickness. A fresh Au-Ge ohmic contact layer was then evaporated to form the new back contact. The wafers were subsequently subjected to rapid thermal annealing and individual devices scribed and diced into ~300×300μm^2 chips. Devices with top contact areas of 50×50μm^2 and 20×20μm^2 were mounted into E10/A packages and bonded with 12.5 μm-diameter gold wire[1]. Re-processing of these wafers in most cases did not alter their dc characteristics significantly. The measurements described in this section were performed on a 20×20μm^2 device, henceforth to be referred to as the 523B.

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1 Details of the device processing are given in Appendix III.

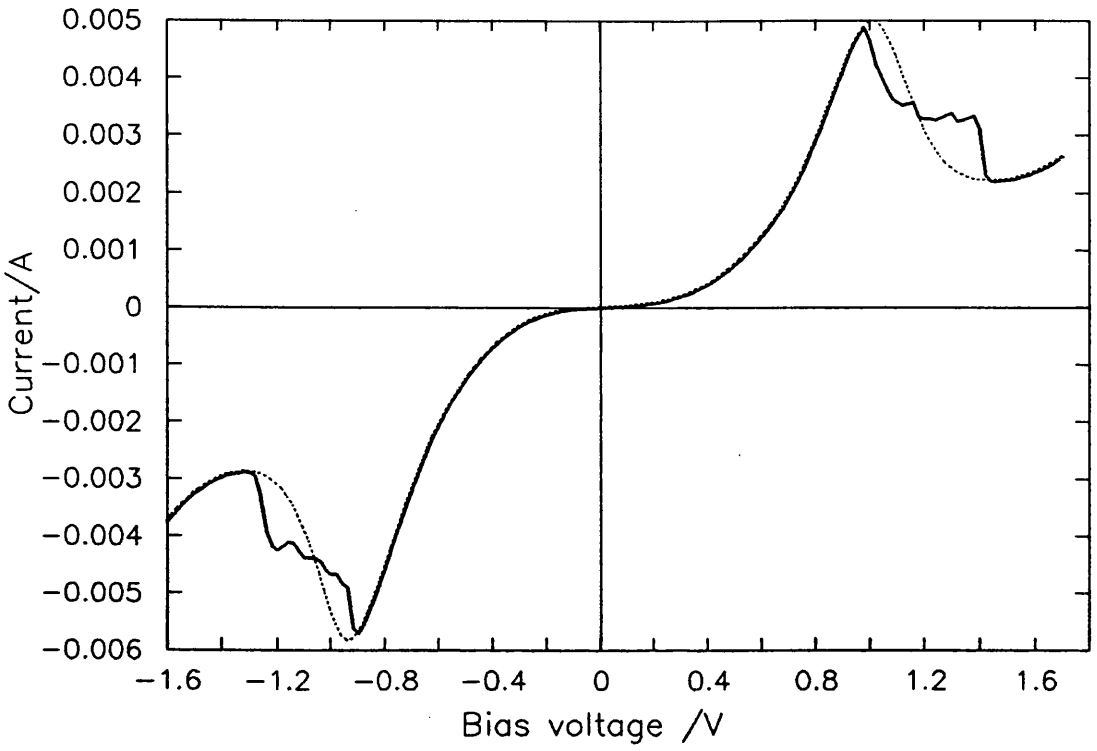

Figure 4.1 . The I-V characteristic of the 523B. The dashed curve represents the stable characteristic obtained with the packaged device in the mount described in chapter 3 and biased through the HP11612A bias network, the rf input port of which was terminated by a matched load.

Figure 4.1 shows the I-V characteristic of the 523B device after bonding and before capping the package. The device is unstable when biased within the NDC region and this is thought to be due to the relatively large inductance associated with the test probes. Also shown superimposed is the stable I-V characteristic obtained with the capped package in the 3.5mm coaxial mount described in chapter 3 assembled at the dc-rf output port of a HP11612A bias network with the input port terminated by a 50 Ω load. The device proved to be unstable when the input port was either short- or open-circuited.

The object of the experiments and subsequent analysis to be described here was to establish a simple equivalent circuit model which would adequately explain the observed small-signal behaviour of the 523B and in particular to determine the C-V characteristic for this device which would then be employed in computer simulations of multiplier performance based on large-signal analysis, as described in chapter 5.

4.2.1.1 Experimental procedure

The experiment consisted of successive reflection coefficient (S11) measurements over the frequency range 45 MHz to 13 GHz at 86 different bias voltages between -1.5 and 1.7 V, with relatively closer voltage steps within and just outside the NDC region where the nonlinearity is highest. For this purpose a HP8510B network analyser was used in conjunction with an external programmable voltage source (Time Electronics 9814) which provided bias through the analyser internal bias port.

The HP8510B was calibrated at the measurement plane using standard short and open circuits, fixed and sliding loads. The frequency step was 32.3875 MHz, such that 401 points were obtained within the test frequency range with the analyser phase-locked at each measurement frequency for improved accuracy. The test signal power was set to -20dBm.

Following calibration, the 523B device was fitted into the network analyser test port extension cable which terminated in an sma jack at which the calibration was performed. The package pedestal faced the generator side and was secured in place using the E10/A mount. The measurements and data

collection were automated using a pc with IEEE-488 interface capabilities as a controller, thus obtaining 86 data files corresponding to the respective bias voltages.

4.2.1.2 Results and analysis

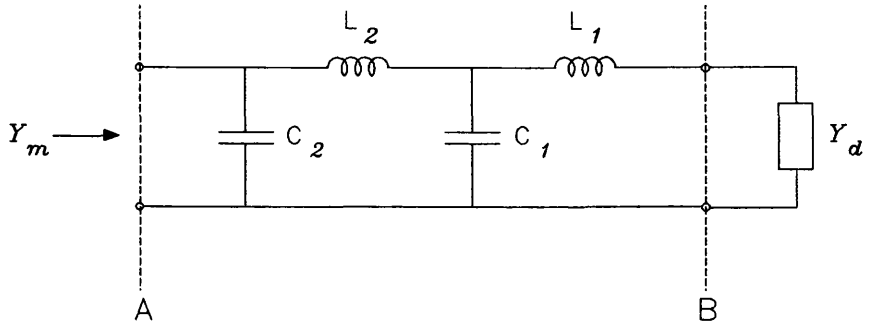

Figure 4.2. Equivalent circuit representation of the measured admittance Y_m at the reference plane **A**. The circuit consists of the package-mount equivalent circuit model for the E10/A package and mount determined in chapter 3, followed by the RTD with unknown admittance Y_d.

Consider figure 4.2 which represents the measured admittance $Y_m(f)$ at reference plane **A**. Beyond **A**, figure 4.2 represents the equivalent circuit model for the E10/A package and mount and the device admittance $Y_d(f)$. Since the package-mount model elements, L_1, L_2, C_1 and C_2 have been determined previously (chapter 3) it is possible to determine $Y_d(f)$, thus eliminating the parasitic effects. Now, since the simple tunnel diode equivalent circuit (figure 4.3) is the most widely applied to model the resonant tunnelling device, it is chosen here for the purpose of modelling and parameter extraction of the 523B RTD. If this circuit is shown to fit the experimental data well over the test frequency range, then, the differential resistance $R(V)$ in figure 4.3 may be

obtained from the dc I-V characteristic leaving R_s, the series resistance and $C(V)$ to be determined from the reflection measurements. R_s should be nominally independent of frequency while C in this model is assumed to depend only on bias voltage.

The first step in the analysis is to obtain an estimate of the series resistance R_s. Referring to figure 4.3, the device impedance, Z_d, has real and imaginary parts given by

$$\Re(Z_d) = R_s + \frac{R}{1+(\omega C R)^2} \qquad (4.2)$$

$$\Im(Z_d) = -\frac{\omega C R^2}{1+(\omega C R)^2} \qquad (4.3)$$

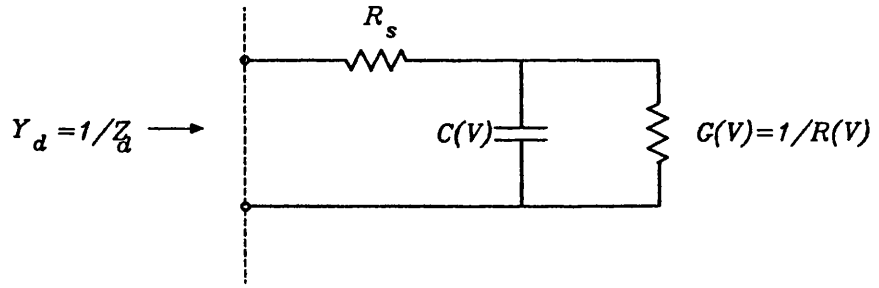

Figure 4.3 . Equivalent circuit model assumed for the RTD 523B. R_s is the series resistance, $G(V)$ the differential conductance and $C(V)$ the capacitance. Y_d is the device admittance.

Thus, C may be calculated from **(4.3)** by assuming the value of R obtained from the I-V characteristic at any bias voltage and frequency within the test ranges. R_s can then be estimated by substituting for R and C in **(4.2)**. This procedure was performed using the de-embedded measured impedance at the

minimum positive differential resistance bias points (prior to the current peaks in forward and reverse bias). A mean value of $4.4 \pm 0.5\Omega$ was obtained over the test frequency range.

A more convenient, and possibly more accurate, method of determining the capacitance is as follows. Having estimated the series resistance, and assuming this is approximately independent of frequency and bias voltage, the effect of R_s on Y_d is subtracted out, giving the intrinsic admittance Y_{intr} as

$$Y_{intr}^{-1} = Z_d - R_s$$

$$i.e., \quad Y_{intr}(\omega) = G(V) + j\omega C(V) \qquad \textbf{(4.4)}$$

where $G = 1/R$ is the differential conductance. Thus, the slope of the susceptance versus frequency plot gives $C(V)$. The mean value of $\Re\{Y_{intr}(\omega)\}$ over the frequency range gives another estimate of $G(V)$.

In practice, this procedure was coded in FORTRAN and the slope determined at each bias point over the test frequency range by using a linear regression algorithm. The percentage standard error of the slope was between less than 1% and up to about 3%. In each case the intercept was negligibly small and comparable in magnitude to its respective standard error. The results of these calculations are given in figure 4.4 which is a plot of the capacitance as a function of bias voltage. Since the small-signal analysis was based on measurements of S11, this is essentially a differential capacitance. The asymmetry in the C-V characteristic is probably due to unintentional asymmetry in the structure of the 523B. This is also evident from the I-V and G-V characteristics of figure 4.1 and 4.5, respectively.

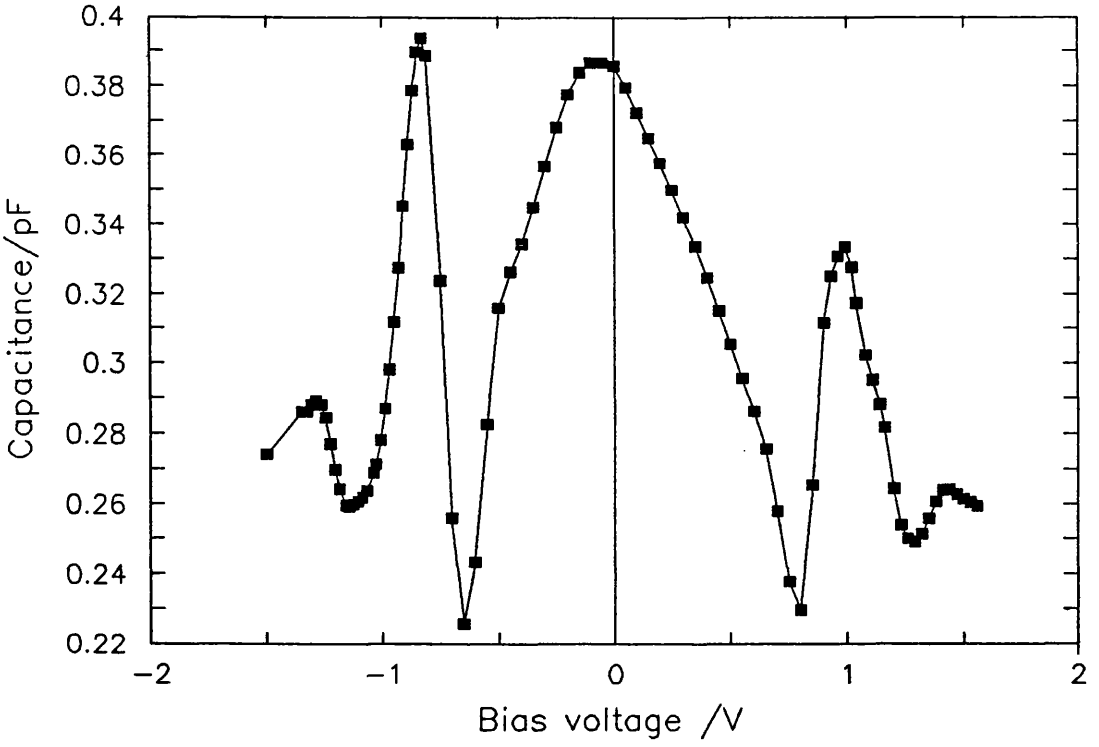

Figure 4.4 . Capacitance of the RTD 523B as a function of bias voltage determined by analysis of reflection measurements as described in the text.

The capacitance drops with bias voltage from about 0.39pF at 0 volts to about 0.23pF at the peak positive differential conductance points before the current peaks. A maximum in the C-V characteristic is reached at bias voltages corresponding to the current peaks in the I-V characteristic in both bias directions, followed by another minimum just before the valley current, at which point the capacitance peaks again. As the valley voltage is exceeded, the capacitance drops. This general behaviour of the capacitance of RTD's has been observed previously [1,2,3].

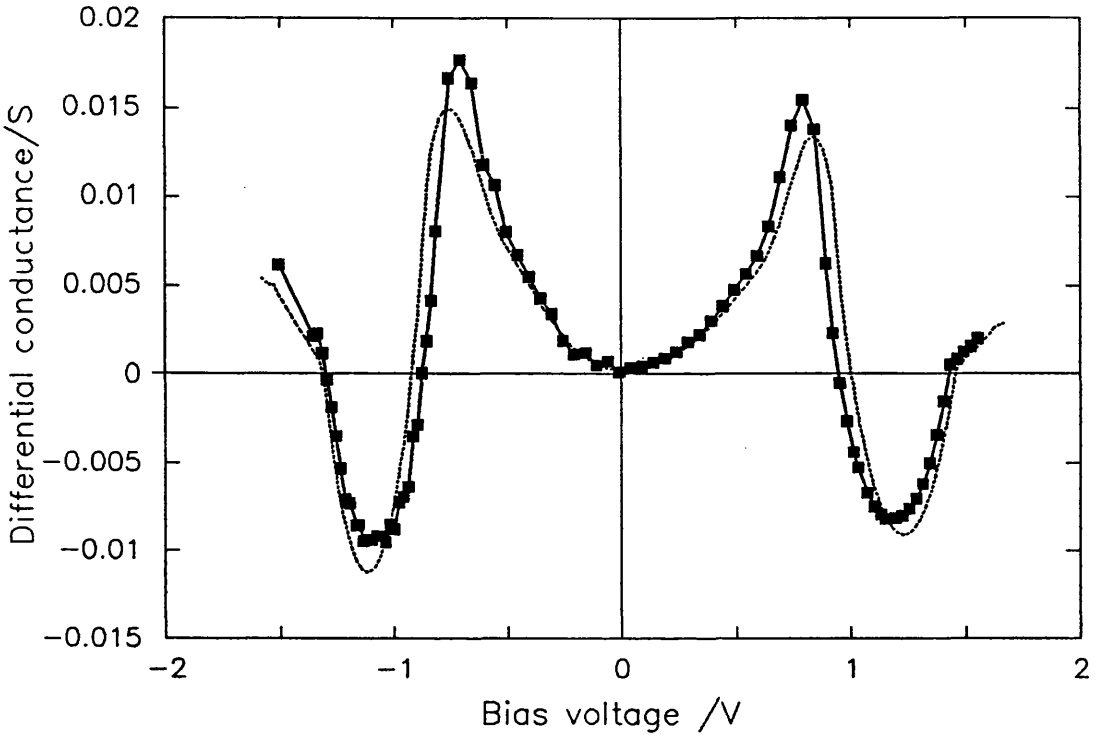

Figure 4.5 . Differential conductance of the RTD 523B as a function of bias voltage. The dashed line was obtained by differentiating the I-V characteristic, while the points represent experimental values obtained as described in the text from the reflection measurements.

Finally, figure 4.5 compares the differential conductance obtained from the small-signal analysis with that obtained by differentiating the I-V characteristic. It is seen that the small-signal values follow closely the variations obtained from the dc analysis. It is therefore adequate to accept $G(V)$ from dc characterisation data for the purpose of modelling the microwave properties at least within the test frequency range.

4.2.1.3 Simulation of experimental results

In this section, the frequency-independent equivalent circuit parameter values of $C(V)$, $R(V)$ and R_s obtained from the small-signal analysis are used to simulate the actual measured small-signal S11 as a function of frequency and the results compared with the experimental data.

The Smith chart plots shown in figure 4.6 were obtained by first calculating the device admittance using the equivalent circuit element values obtained as described in section 4.2.1.2 as a function of frequency. This admittance was then transformed back to the measurement plane A in figure 4.2 using the equivalent circuit of the E10/A package and mount, and these values subsequently converted to S11. The figures 4.6a-i show the measured S11 traces as solid lines together with the simulated plots represented by the dotted lines at some key bias voltages as follows:

a. at zero bias

b. at -0.70V, in the vicinity of the peak positive differential conductance point in reverse bias

c. at -0.87V, near the current peak in reverse bias

d. at -1.03V, near the minimum differential conductance in reverse bias

e. at -1.29, in the vicinity of the current valley in reverse bias

f. at 0.80V, as in b but in forward bias

g. at 0.96V, as in c but in forward bias

h. at 1.16V, as in d but in forward bias

i. at 1.41V, as in e but in forward bias.

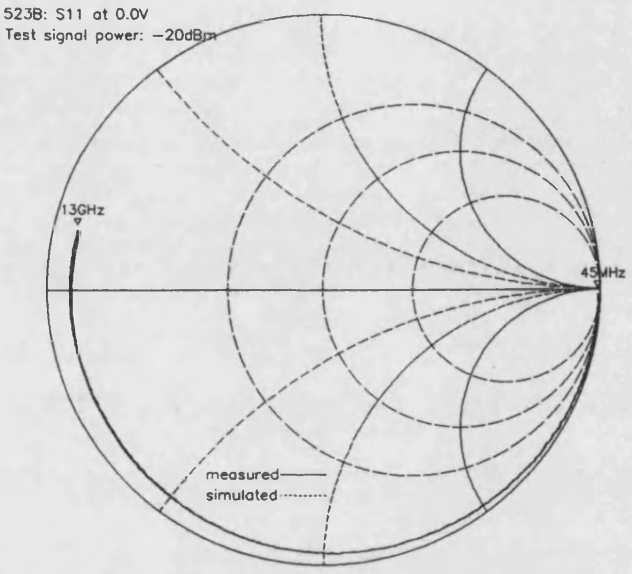

Figure 4.6 a.

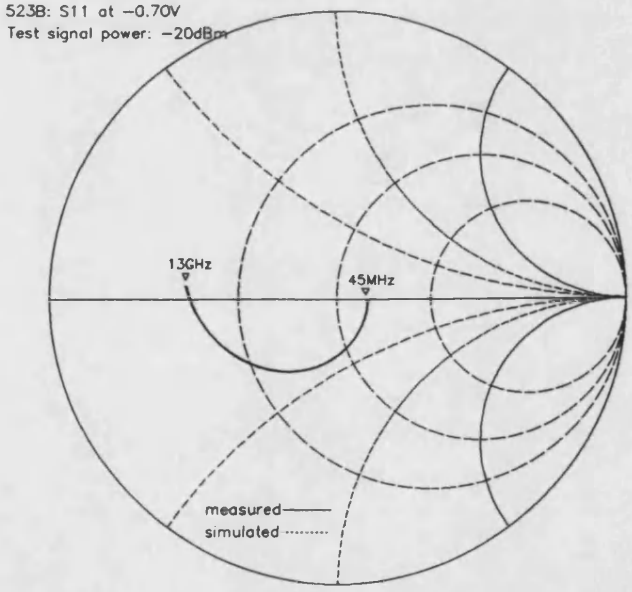

Figure 4.6b.

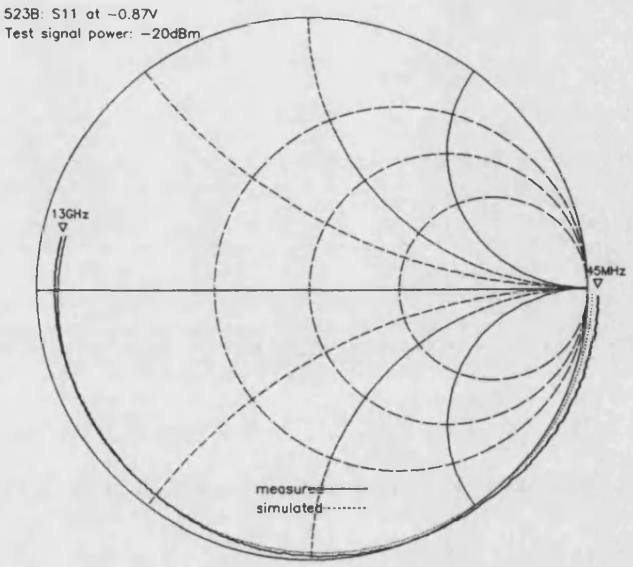

Figure 4.6c.

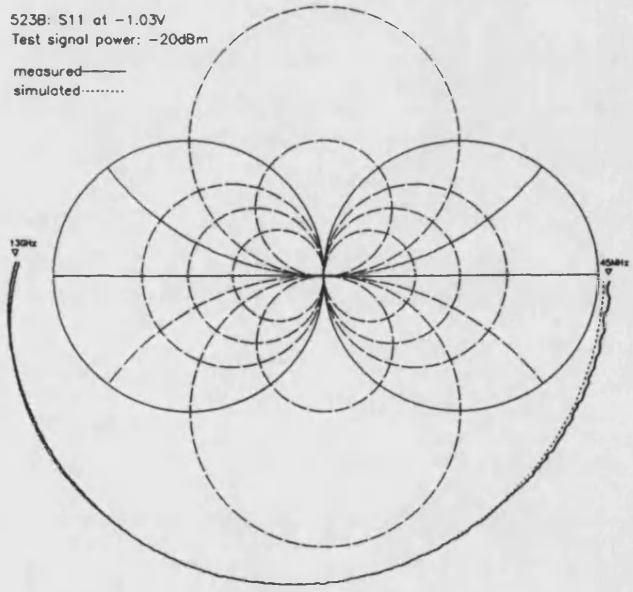

Figure 4.6d.

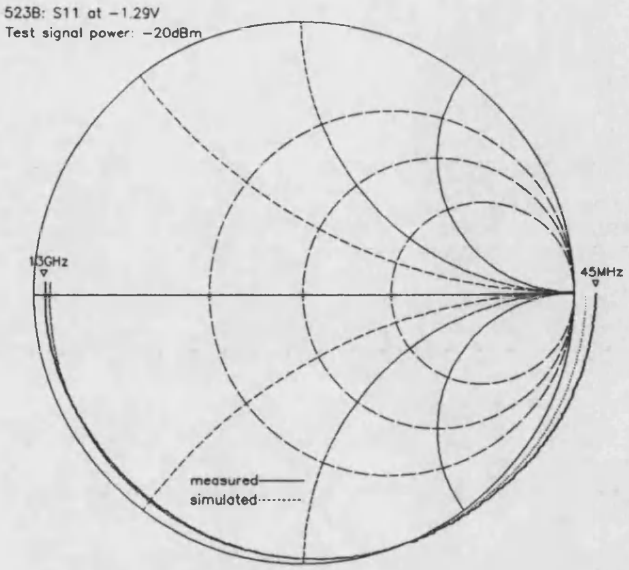

Figure 4.6e.

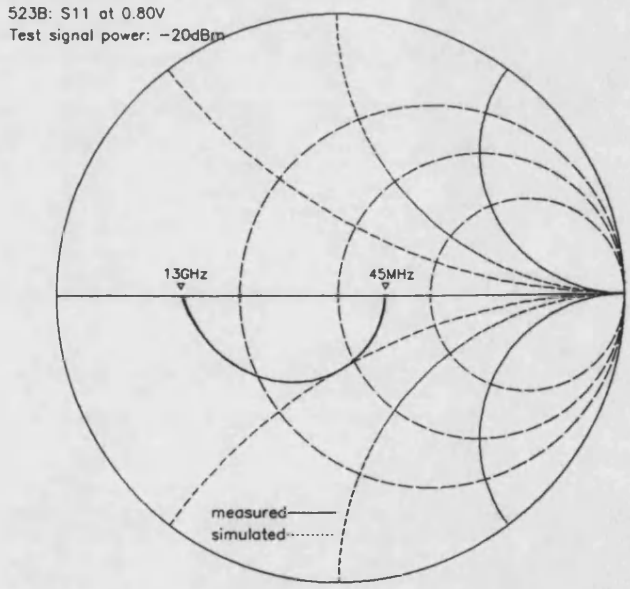

Figure 4.6f.

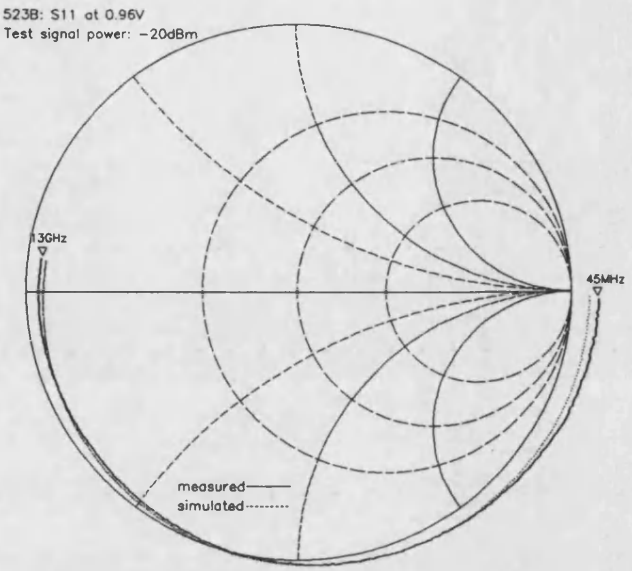

Figure 4.6g.

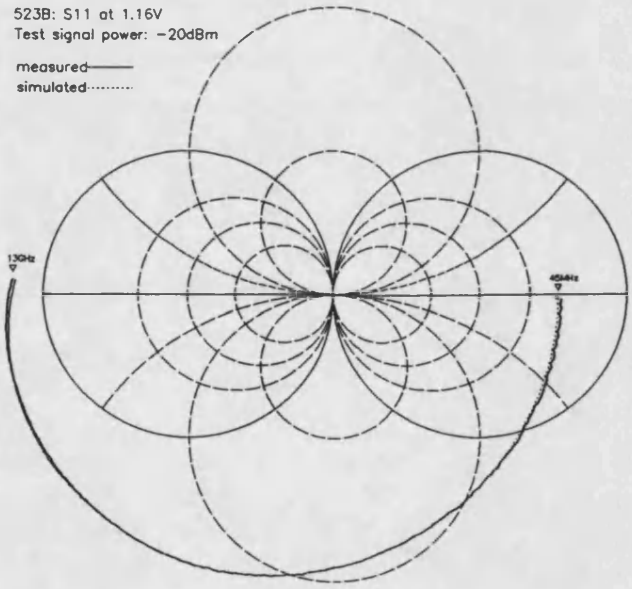

Figure 4.6h.

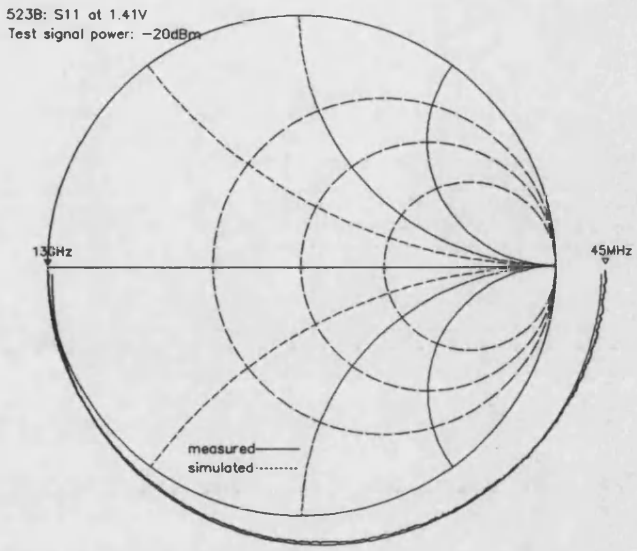

Figure 4.6i.

The quality of the fit is excellent and in most cases the measured traces are virtually coincident with their respective simulated plots over most of the frequency range. The maximum difference between experimental and simulated data was less than 5% over all bias voltages and within the test frequency range. This is the first small-signal study in which a resonant tunnelling device has been successfully analysed at microwave frequencies at such a large number of bias voltages and the results fitted with high accuracy to the simple model of figure 4.3. Other reports [4,5,3,6,7,8] have suggested more complex models involving at least an empirical series inductance which the authors have associated with the intrinsic device properties, while others [1,9,10,2,11] have lumped the bond-wire inductance with the device model of figure 4.3 in their analysis. In the case of Refs.[2],[7] and [8], CAD software was used to extract the equivalent circuit element values including at least the bond-wire inductance. This increases the number of degrees of freedom for the fit. The analysis which led to the results illustrated here makes use of the simplest model

and the accuracy obtained is mainly due to accurate de-embedding. This simple model, although not particularly illustrative of the complex intrinsic electrical processes of the device, has thus been shown to be applicable within at least the 45 MHz to 13 GHz frequency range. Providing careful and accurate de-embedding has been performed, the model will be useful in microwave circuit design involving the use of RTD's. In particular, the differential capacitance measurements are, to the best of the author's knowledge, the first to be obtained directly from measurements over such a relatively large bias voltage and frequency range.

Now, the internal resistive cutoff frequency f_{max} may be calculated by setting the real part of the device impedance equal to 0 in **(4.2)**, which gives

$$f_{max} = \frac{1}{2\pi C R}\sqrt{\frac{R}{R_s} - 1} \qquad \textbf{(4.5)}$$

where R is now the magnitude of the negative differential resistance. Figure 4.7 shows the values of f_{max} calculated using the measured small-signal capacitance and differential resistance. Cutoff frequencies corresponding to bias voltages close to the current peak and valley points were obtained from the measured reflection coefficient magnitudes by observing the frequency at which $|S11|$ crosses unity and are also shown in figure 4.7. Values well within the NDC region could not be measured as these were higher than the highest test frequency of 13 GHz. However, it is expected that the estimated values of f_{max} for this device are close to the actual values when bearing in mind the agreement obtained between observation and simulation.

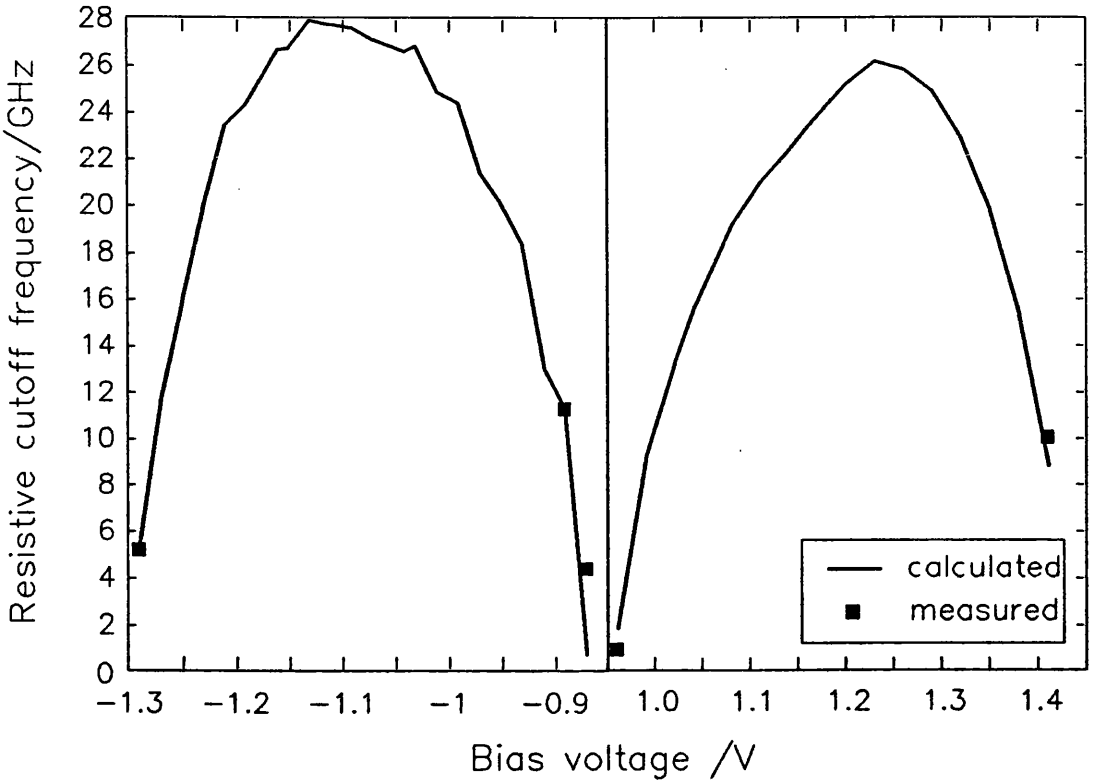

Figure 4.7 . Internal resistive cutoff frequency, f_{max}, for the RTD 523B as a function of bias voltage within the NDC region. The solid line was calculated from the extracted equivalent circuit parameters. The points represent the measured cutoff frequencies. It was not possible to obtain f_{max} from the experimental data for bias voltages well within the NDC regions as these were outside the test frequency range.

4.2.1.4 Effects of test-signal power

Many authors have published results of small-signal microwave characterisation of resonant tunnelling devices, however, although the experimental methods employed were essentially similar to those reported here, some have unfortunately not

mentioned the test signal levels used [10,2,8,14,12]. In fact, the effect of signal power on small-signal reflection measurements of RTD's has been all but overlooked in the literature. It will be shown here that considerations of test signal level are of the utmost importance and that these have a direct bearing on the accuracy of parameter extraction.

A digression is worthwhile at this point. The test signal power from the HP8510B used for the measurements described in section 4.2.1.1 was monitored over the test frequency range and found to fluctuate between about -22 and -25 dBm. The nominal power setting was -20 dBm and difficulties were experienced with phase locking when using lower signal levels. Ideally, as low a signal level as possible should be employed, however, the nominal value of -20 dBm actually used proved to be sufficiently low.

The experimental procedure described in section 4.2.1.1 was repeated with a nominal signal level of -10 dBm (actually found to be between about -11 and -13 dBm) and using the same device. Subsequent analysis using the methods described in section 4.2.1.2 revealed that it was impossible to extract frequency-independent parameter values at bias voltages close to regions were the I-V characteristic is highly nonlinear and within the NDC region. It was, however, found possible to obtain a relatively good fit to the experimental data at frequencies above about 4 GHz in most cases. Figure 4.8 shows some of the measured S11 traces plotted on Smith charts along with those calculated using the estimated parameter values derived from the analysis. In the cases where the bias voltage approached the NDC regions,

measurements at frequencies above about 4 GHz were used since here the traces approached the general shapes of the small-signal measurements.

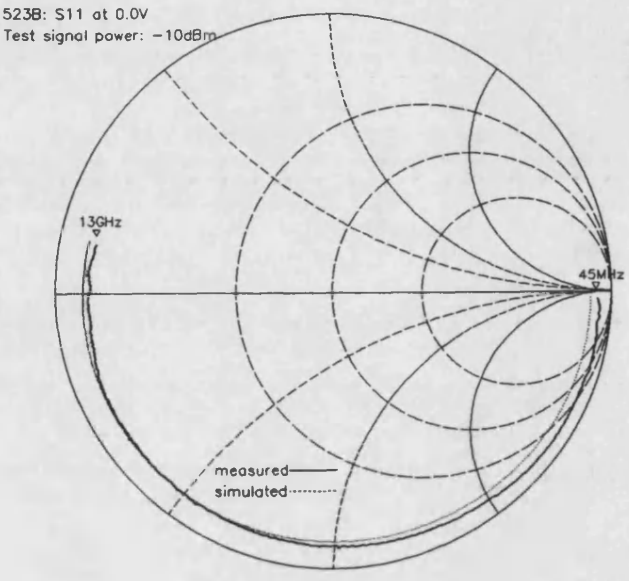

Figure 4.8 a.

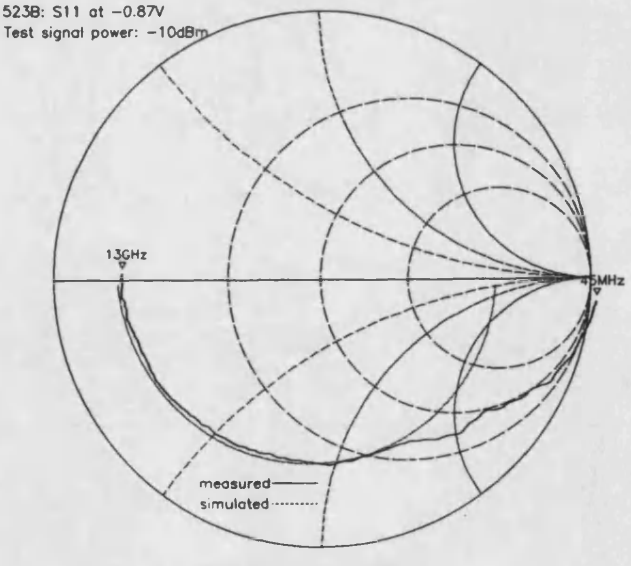

Figure 4.8b.

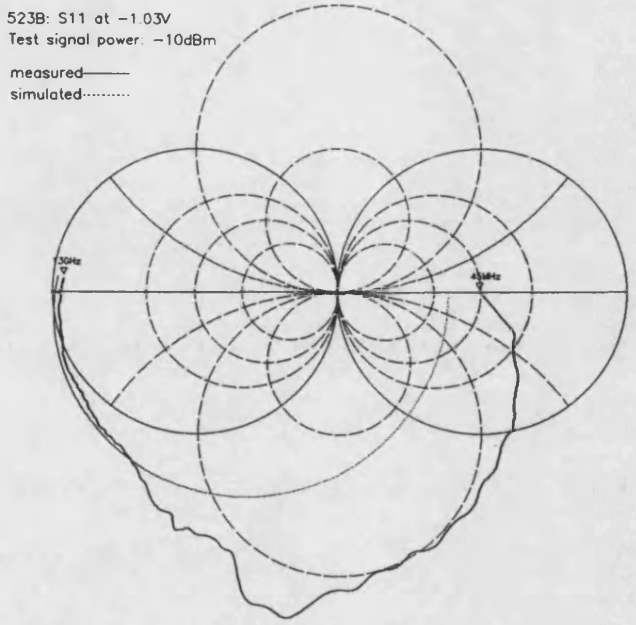

Figure 4.8c.

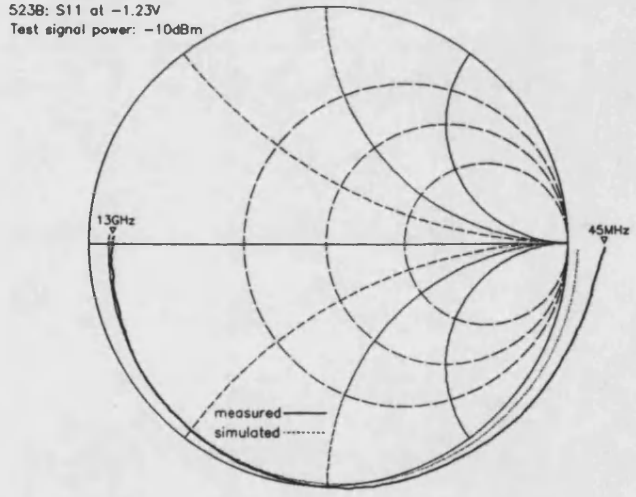

Figure 4.8d.

Figure 4.8a shows the results of measurement (solid line) and simulation (dotted line) based on the analysis described previously at zero bias. There is essentially little difference from the proper small-signal case of figure 4.6a,

except that the impedance level is generally slightly lower. There is also good agreement between the measured and simulated data.

As the bias voltage approaches the NDC region there is a marked change in behaviour, where the frequency-independent parameters extracted on the basis of the simple small-signal analysis no longer adequately explain the experimental results over the whole test frequency range. In fact, it can be observed from figure 4.8b that the experimental trace for a bias voltage of -0.87V starts just outside the unit circle at 45 MHz and quickly moves to within, where $|S11|<1$ at 336 MHz. In contrast, the previous small-signal measurements give f_{max} at -0.87V bias as 4.353 GHz. Similar behaviour is observed at bias voltages close to the valley current points, as for example in figure 4.8d at -1.23V. In this case the simulation gave a better fit to the experimental data than at -0.87V, this is probably because the nonlinearity in the valley region of the I-V characteristic is relatively smaller than that around the peak current point.

When the device is biased well within the NDC region as in the case of figure 4.8c, the observed behaviour is even more anomalous with the trace showing marked fluctuations as the test signal frequency increases. The cutoff frequency is 10.150 GHz while the calculated value from the small-signal parameters extracted from the measurements at -20dBm is 26.768 Ghz.

In order to understand the reasons behind such behaviour it is instructive to examine the calculated differential conductance and capacitance estimated from the analysis of the -10 dBm data. These values are to be treated with caution as their determination at bias voltages well within

the NDC region led to poor agreement with experimental data at frequencies below about 4 GHz and was thus not based on the full test frequency range. As a result of this the agreement between the experiment and simulation in, for example figure 4.8c, is only acceptable at frequencies above about 4 GHz.

Figure 4.9 is a plot of the capacitance as a function of bias voltage. The points indicate the values obtained from the -10 dBm data, while the dashed line represents the previously determined small-signal capacitance using the nominal -20 dBm test signal level. The second trough as the bias voltage increases now appears at a lower voltage in both bias directions and becomes almost insignificant, while the peaks move closer in voltage and are significantly attenuated. The behaviour of the capacitance between about -0.5 and 0.7V and beyond the current valley points remained essentially similar to the small-signal case.

The device conductance is shown in figure 4.10 as a function of bias voltage. The small-signal conductance is, as before, represented by the dashed line. Again it is seen that the general behaviour of $G(V)$ extracted from the data measured with the -10 dBm signal is essentially similar at bias voltages outside the NDC regions. There is a small but significant increase in conductance at and in the vicinity of zero bias, which would explain the slight lowering of impedance levels observed in figure 4.8a when compared with figure 4.6a. Furthermore, the negative differential conductance has a significantly lower magnitude and exhibits two local minima in both reverse and forward bias[1].

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1 In the forward bias case, these are not sufficiently resolved, but the trend is still manifest.

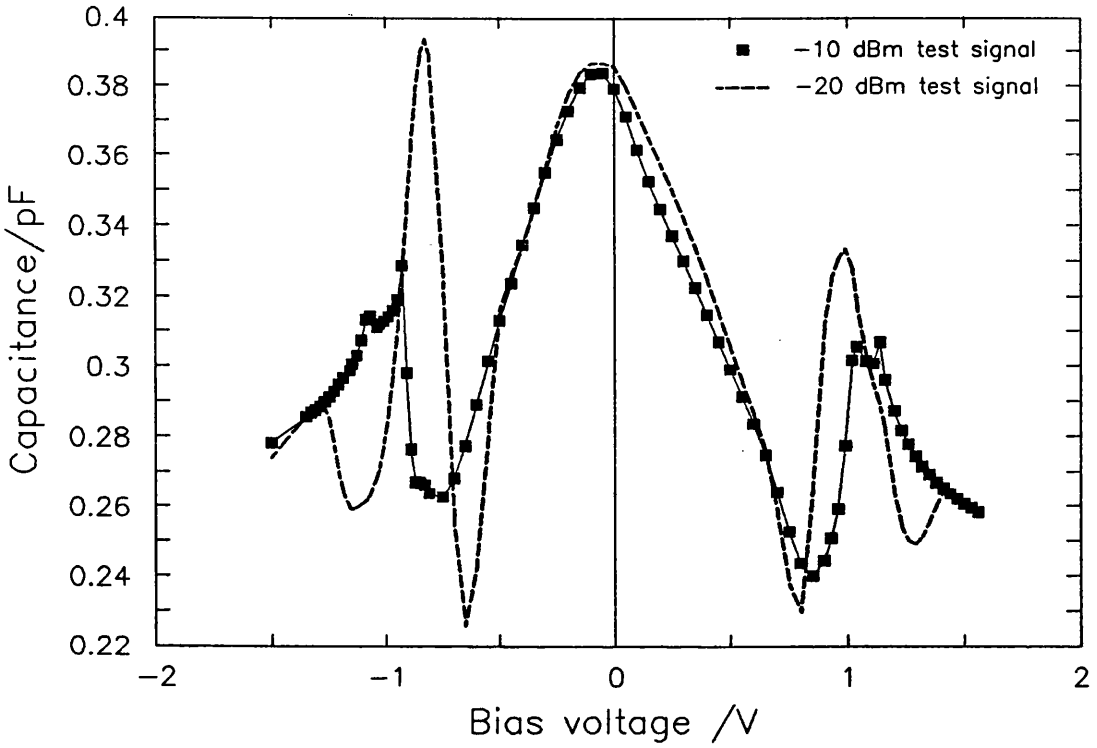

Figure 4.9 . Capacitance of the 523B as a function of bias voltage. The points represent the values obtained from measurements with a -10 dBm test signal level, while the dashed line represents the small-signal capacitance of the same device obtained from measurements with a nominal -20 dBm signal level.

The cutoff frequencies have been markedly reduced, mainly as a result of the lower NDC exhibited by the device at the higher test signal level. In fact, figure 4.11 shows that at most bias voltages in the NDC region, $f_{max} < 13$ GHz. The more drastic reductions occurred with bias voltages in the reverse bias NDC region as here the magnitude of the NDC has been subjected to a relatively higher attenuation (figure 4.10). The reason for this effect becomes apparent when one considers that the NDC region is wider in forward bias than in reverse. Now, the test signal causes the instan-

taneous terminal voltage of the device to sweep over the I-V characteristic to an extent determined by the signal amplitude and the degree of impedance match at any particular frequency and bias voltage. With bias voltages approximately in the middle of the forward bias NDC region the voltage excursion brought about by the application of the test signal does not encounter regions where the conductance is significantly different from the small-signal case. However, with a narrower NDC region and nominally similar voltage sweeps during the rf cycle, it would be more likely for the instantaneous voltage to encounter regions of greatly reduced conductance magnitudes or even cross into positive differential conductance regions. This would account for the smaller NDC magnitudes obtained in reverse bias. The reasons for the local maxima in the NDC magnitude are not apparent and would require detailed large-signal analysis to establish whether these are a result of inaccurate modelling or genuine features.

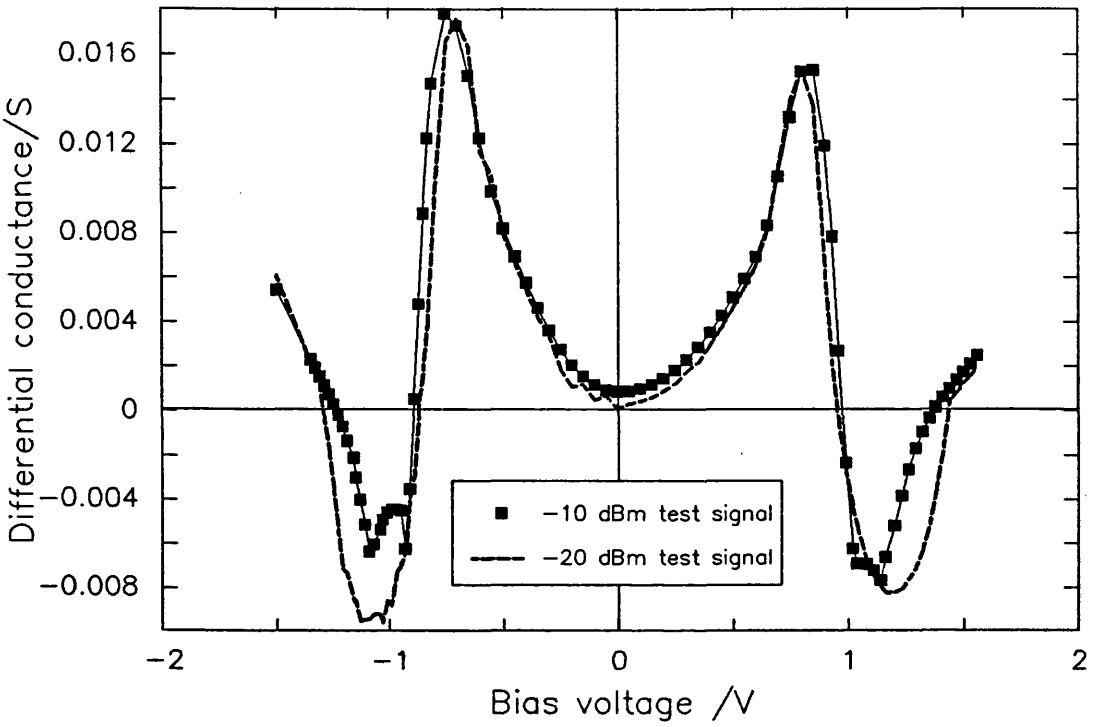

Figure 4.10 . Differential conductance of the 523B as a function of bias voltage. The points represent the values obtained from measurements with a -10 dBm test signal level, while the dashed line represents the small-signal differential conductance of the same device obtained from measurements with a nominal -20 dBm signal level.

The arguments which have been used above to explain the differences between the estimates of $G(V)$ from measurements at the two test signal levels should also explain the differences in the respective observed values of $C(V)$. In particular it would seem likely that the capacitance peaks at -.83V and 0.97V in the small-signal $C(V)$ (figure 4.4 and 4.9) were 'averaged out' as these lie very close to neighbouring minima. The minima at -1.15V and 1.28V would appear to have suffered the same fate.

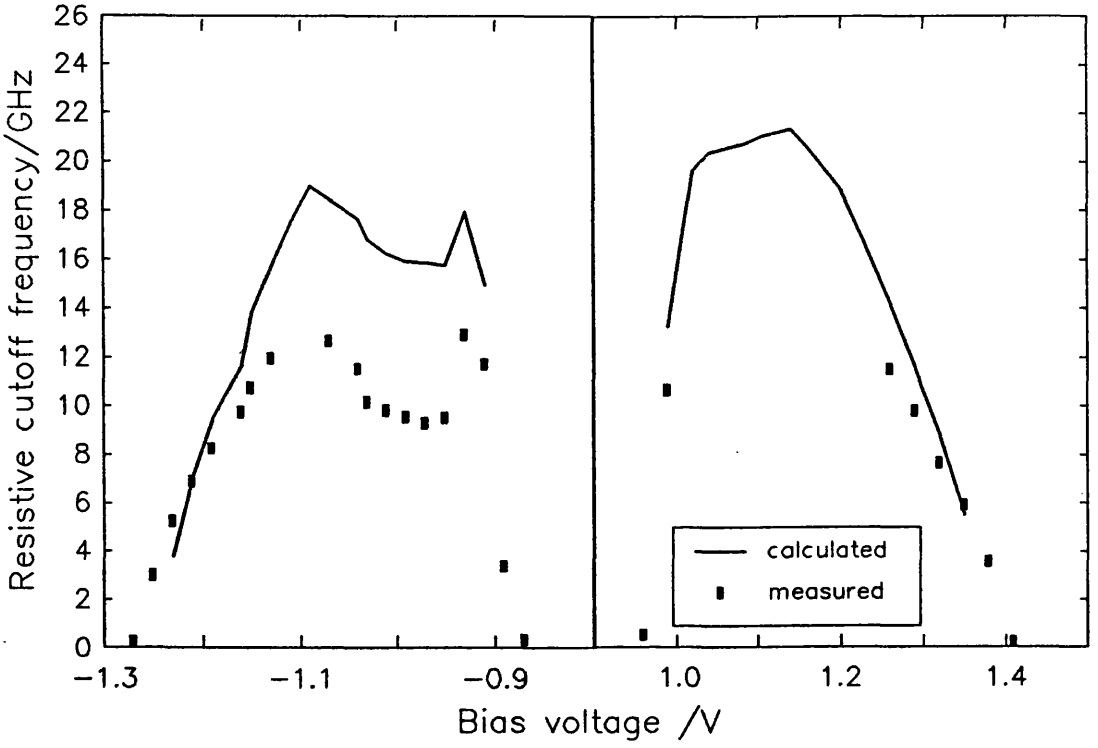

Figure 4.11 . Measured and calculated cutoff frequencies of the 523B with a test signal level of -10 dBm. The missing points corresponding to bias voltages approximately in the middle of the forward bias NDC region correspond to values of $f_{max} > 13$ GHz and thus outside the test frequency range.

The less significant capacitance maxima at -1.08V and -0.94 in reverse bias and 1.04V and 1.13V in forward bias coincide precisely with the anomalous minima in the respective NDC regions of figure 4.10, thus the two effects seem to be related. Evidence suggesting that these are genuine features may be obtained, at least for the reverse bias case, from figure 4.11 since the maxima in the **measured** f_{max} also occur at -1.08 and -0.94V, and also correspond with those obtained by the calculation using the values of $C(V)$ and $G(V)$ extracted from the -10 dBm signal data.

Finally, referring back to figures 4.8b and 4.8c, the marked divergence from the simulations at the lower end of the test frequency range as well as the fluctuations of the measured S11 may be attributed to the complex interaction of the dynamic device admittance with the test signal. The latter, being significantly stronger than in the true small-signal case, would in general give rise to higher rf voltage amplitudes, V_{rf}, across the device. However, V_{rf} is a function of both the device impedance and frequency for higher signal levels. Thus the effective voltage amplitude of the test signal across the intrinsic device is not uniform over the frequency range and hence adds to the complexity of the situation. The measured reflection coefficient thus becomes a highly complex function of device properties, frequency and signal power. Nevertheless, it may still be possible to make useful approximations at bias voltages outside the NDC regions and over restricted frequency ranges for voltages within.

4.3 Large-signal Measurements

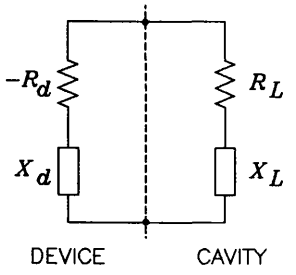

Figure 4.12. Oscillator equivalent circuit with R_d and X_d being the real and imaginary parts (functions of I_{rf} and I_0) of the device impedance, and, R_L and X_L, the real and imaginary parts of the embedding impedance.

Consider the circuit of figure 4.12. Here the device is represented as being simply a negative resistance $-R_d$ function of bias current I_0, or voltage V_0 and I_{rf} (or V_{rf}), in series with a reactance $X_d(I_0,I_{rf})$. The cavity here refers to the microwave circuit consisting of the package, mount,

etc. which loads the device with an embedding impedance $(R_L + jX_L)$. A basic requirement for a negative resistance oscillator active element is that at low I_{rf} the magnitude of the negative resistance (R_d) must exceed the real part of the embedding impedance (R_L). Thus, the net resistance in the circuit is negative and noise currents grow exponentially at a frequency determined by the reactive match of X_L and X_d. As the peak I_{rf} grows, $R_d \rightarrow R_L$ until the net circuit resistance becomes zero and steady-state oscillations ensue. Thus, stable oscillations **require** the device negative resistance magnitude to fall with increasing I_{rf}. So, the initial condition for the onset of oscillation is

$$R_d(small-signal) > R_L \qquad \textbf{(4.6)}$$

when

$$X_d(small-signal) = -X_L \qquad \textbf{(4.7)}$$

and the final condition for stable oscillation is

$$R_d(I_0, I_{rf}) = R_L \qquad \textbf{(4.8)}$$

In general the device reactance varies with I_{rf} such that the oscillation frequency shifts until I_{rf} stabilises.

At steady-state oscillation, the power made available by the device is given by

$$P = \frac{1}{2} I_{rf}^2 R_d \qquad \textbf{(4.9)}$$

assuming sinusoidal oscillations, where I_{rf} is the peak rf current.

From the above brief discussion one concludes that device large-signal impedance (or admittance) must be determined as a function of bias voltage, rf signal power and frequency, and that this information is consequential in any subsequent attempt at designing prototype microwave circuits for large-signal operation. The procedure for such measurements will now be outlined.

Various workers have used basically similar techniques for large-signal device impedance or admittance measurements [13,14,15] in that having first de-embedded the device by some means, the device is biased into oscillation at a convenient power and frequency. The conjugate admittance of the matching network is then measured with a network analyser which thus determines the large-signal device impedance or admittance. The method presented here was implemented using packaged RTD's and follows the same general outline. Consider the arrangement represented schematically in figure 4.13.

The device is suitably mounted in a microwave package (E3 or E10/A in this case) and placed in a coaxial mount such as the ones described in chapter 3. It is then biased in the negative conductance region and the double-stub tuner (Maury Microwave^{TM} model 2640D) adjusted for a convenient rf power output and frequency. These are measured on the spectrum analyser.

The mount, which is designed to be compatible with the test port connector on the network analyser reflection test unit, is removed and the rest of the circuit connected to the network analyser at reference plane AA'. The admittance

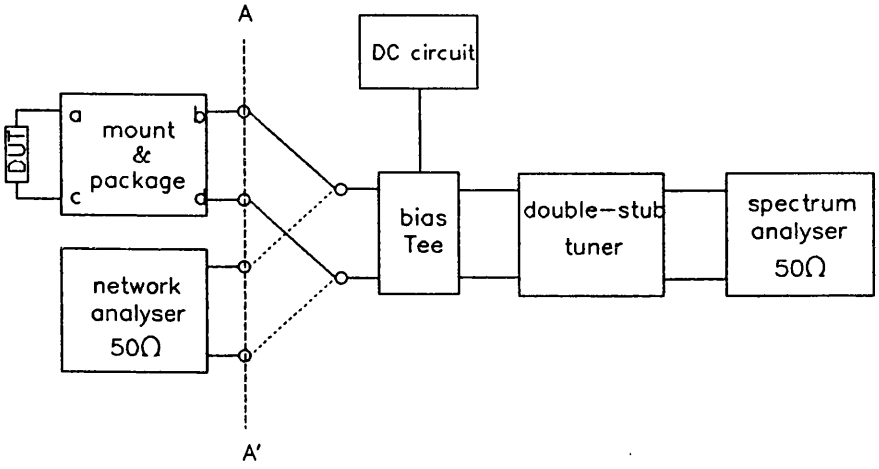

Figure 4.13 . Schematic of the microwave circuit for measuring the large-signal device admittance.

seen looking into AA' ($Y_{m'}(f_{osc})$) is then measured at the oscillation frequency. Now, since the oscillation is steady-state, at any reference plane in the circuit the sum of the impedances or admittances looking in either direction must be zero [16,17]. Hence, at AA',

$$Y_m(f_{osc}) + Y_{m'}(f_{osc}) = 0 \qquad \textbf{(4.10)}$$

Therefore, $Y_m(f_{osc})$, the admittance seen looking into the mount with the RTD in place, is determined from which the large-signal $Y_d(f_{osc})$ can be calculated by transforming through the equivalent circuit of the embedding network.

4.3.1 Large-signal impedance of the RTD GWS160

This section describes the first attempt in the present study at determining the large-signal impedance of a resonant tunnelling device. The structure tested was the DRA GWS160.

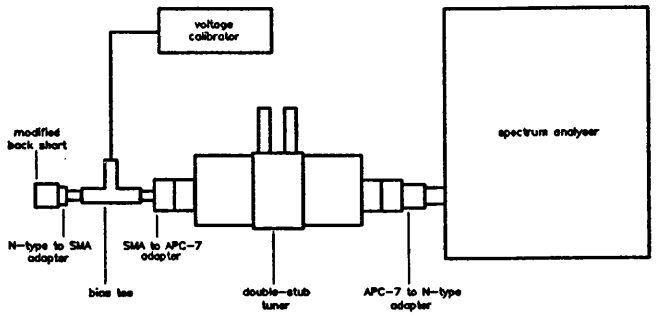

Figure 4.14 . Measurement set-up for determining large-signal device impedance.

Figure 4.14 shows the experimental set-up used for the measurement of large-signal impedance. The devices were assembled in S4-type microwave packages and fitted into the centre conductor recess of a female N-type-to-SMA adapter and secured in place by the 7mm modified backshort described in chapter 3. A HP11612A bias network provided the dc bias to the device from a Time Electronics 9814 voltage calibrator. The double-stub tuner altered the impedance seen by the device and also tuned the frequency and output power which were monitored on a HP8559A spectrum analyser.

The devices tested had top contact pads defining mesas of nominally square dimensions 90×90μm, 80×80μm, 65×65μm, 45×45μm and 15×15μm. They were biased in their respective NDC regions and the tuner adjusted for a match which resulted in coupled rf power into the spectrum analyser. It transpired that the only device which oscillated was the 45μm. The larger area devices showed evidence of low frequency (1 - 10 MHz) oscillations in the bias circuit which were not affected by tuner adjustment. The 15μm device showed no evidence of oscillation whatsoever; in fact, the I-V characteristic for this device was the only one which showed stability in the NDC region, even without any form of de-coupling. The reason for this may be that severe

undercutting during the wet chemical etch might have resulted in a very small-area device which is intrinsically stable at both dc and microwave frequencies (see chapter 2). The peak current density (assuming the nominal device area) for this device was found to be ~$9 A cm^{-2}$, much smaller than that of the others ($400-700 A cm^{-2}$).

Thus, the microwave measurements described above could only be performed on the 45μm device. Hence, with this device in the modified mount and using the configuration of figure 4.14, a forward bias voltage was set in the middle of the NDC region at 0.709V. The tuner was then adjusted to obtain the lowest oscillation frequency allowable. This was 810 MHz at about -13 dBm. The tuner adjustments were then noted. The output frequency was subsequently increased in approximately 50 MHz steps up to 1.13 GHz (the highest oscillation frequency obtainable), each time keeping output power approximately constant and noting the tuner adjustments. Higher power levels (about -10dBm) were achievable but could not be maintained constant over the tuning range. The fact that the output was so low may invalidate the claim for large-signal measurements, but nevertheless the procedure is still applicable.

The device was then removed from the mount and the spectrum analyser replaced by a 50Ω termination. Single frequency impedance measurements were then made by connecting the unknown port of a HP8410A network analyser to the N-type female-to-SMA adapter such that the reference plane coincided with the device position. The tuner settings which resulted in the stable oscillation conditions determined above were replicated and the impedance looking towards the tuner from the package plane was measured for each setting.

4.3.1.1 Some important observations

The oscillations observed were strongly effected by tuner adjustments. Moving the tuner stubs out by more than about 1mm resulted in spurious oscillations in the bias circuit which were not effected by tuner adjustments. The spectrum of these oscillations could not be observed on the spectrum analyser as the lower cutoff frequency of the bias network was 45 MHz. However, these oscillations were examined by connecting a wide-bandwidth oscilloscope across the dc circuit and found to have waveforms similar to relaxation oscillations as discussed in chapter 2. The frequency of these spurious oscillations was between about 500 kHz and 5 MHz and depended strongly on the applied bias.

Moving the tuner stubs back in resulted in a dramatic change in the output spectrum in that single frequency oscillations appeared suddenly at frequencies tuneable between about 800 MHz to just over 1 GHz. This spectrum consisted of a fundamental within this frequency range at a power level of about -13dBm with harmonics the highest of which was less than 30dB below the fundamental. The bandwidth was about 50 kHz.

The most important observation was that the bias circuit oscillations disappeared instantly with the onset of the single-frequency oscillations. To the best of the author's knowledge and at the time of writing, this is the first time that such observations have been reported in respect of resonant tunnelling devices. Indeed, with **all** oscillating devices tested during the course of this study, the bias circuit oscillations have been observed to disappear (outside measurable limits) irrespective of any de-coupling circuit on the dc arm as soon as the conditions for a well-defined

microwave spectrum with clearly discernible oscillations have been established[1]. The implications of this effect on high- and moderately high-Q potential applications would mean that dc and low-frequency stabilisation design would be greatly simplified; a significant advantage since RTD's are notoriously difficult to stabilise at low frequencies.

4.3.1.2 Results and Analysis

In a freely-running oscillator circuit generating a stable rf output, the sum of the impedances looking into either side of any reference plane along the circuit must be zero [18]. Thus, if the measured impedance at the packaged device plane is Z_m, then the impedance of the embedded device (i.e., including package and mount parasitic effects), Z_{emb}, may be obtained from

$$Z_m + Z_{emb} = 0 \qquad (4.11)$$

At this point, the device impedance may be de-embedded by transforming Z_{emb} through an appropriate equivalent circuit model for the package and mount combination. As the equivalent circuit due to Owens [19] is currently the best-available model for this package and mount combination, it was used to determine the device impedance at all test frequencies. The only parameter value changed was that due to the bonding wire inductance. The bonding wire stretches diametrically across the package flange and is bonded to the device top contact roughly at the middle of its length. This suggests an equivalent circuit for the lead inductance

1 See Appendix IV for examples of microwave spectral output of some of the tested devices.

as being two (assumed identical) inductors in parallel. Then, the inductance of this arrangement would be given by [1]

$$2L_w = 0.2l(\ln(4l/d) - 1)\,\text{nH} \qquad \textbf{(4.12)}$$

where l is the lead length, slightly longer than the internal flange radius, and d the bond-wire diameter, both in mm. l was found to be 0.8 mm, giving $L_w \approx 0.37\,\text{nH}$.

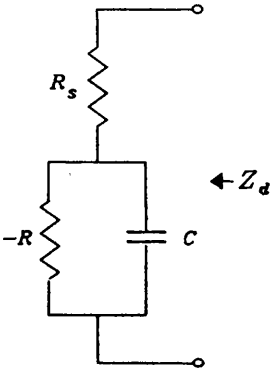

Figure 4.15 . Simple large-signal equivalent circuit model of a resonant tunnelling device based on the equivalent circuit of a tunnel diode. R_s is the series resistance, $-R$ is the negative resistance and C is the capacitance.

Now, consider the simple device equivalent circuit of figure 4.15, where $-R$ is the negative resistance, R_s is the series resistance and C is the device capacitance, all assumed independent of frequency. The real and imaginary parts of the device impedance Z_d are given by **(4.2)** and **(4.3)** with R replaced by $-R$:

$$\Re(Z_d) = R_s - \frac{R}{1+\omega^2 C^2 R^2} \qquad \textbf{(4.13)}$$

$$\Im(Z_d) = -\frac{\omega C R^2}{1+\omega^2 C^2 R^2} \qquad (4.14)$$

The I-V plot for this device showed evidence of dc instability in the NDC region, as can be seen from figure 4.16. Thus R was estimated from the slope of an artificially smoothed curve obtained by fitting and interpolating cubic splines between the peak and valley voltages of the experimental dc I-V characteristic. The dashed line in figure 4.16 represents the fitted curve. The series resistance upper limit was estimated from the highest slope which occurred at about 0.57V. The values obtained were R = 61 Ω and R_s = 30 Ω and were used as first estimates for curve fitting the results to the experimental data.

An initial value for C was obtained by assuming the product $(\omega CR)^2 \gg 1$ in **(4.14)** within the frequency range of interest. In this limit **(4.14)** reduces to $\Im(Z_d) \approx -1/\omega C$ which gave C ≈ 4pF.

The best simultaneous fit to the data using **(4.13)** and **(4.14)** was found with values of $C = 3.4$pF, $R = 107\Omega$ and $R_s = 4.7\Omega$. Figure 4.17 compares the measured and calculated device impedance. The fit is quite satisfactory for both real and imaginary parts. The error in the network analyser measurements is estimated to be about 10%. The curve-fitting procedure allowed mean differences between calculated and measured impedances of <10%. Although within this limit there were various different combinations of values of C, R and R_s which gave good fits to the data, it is possible to conclude that the equivalent circuit of figure 4.15 with the device parameter values given here is adequate to explain the observed behaviour of the large-signal device impedance

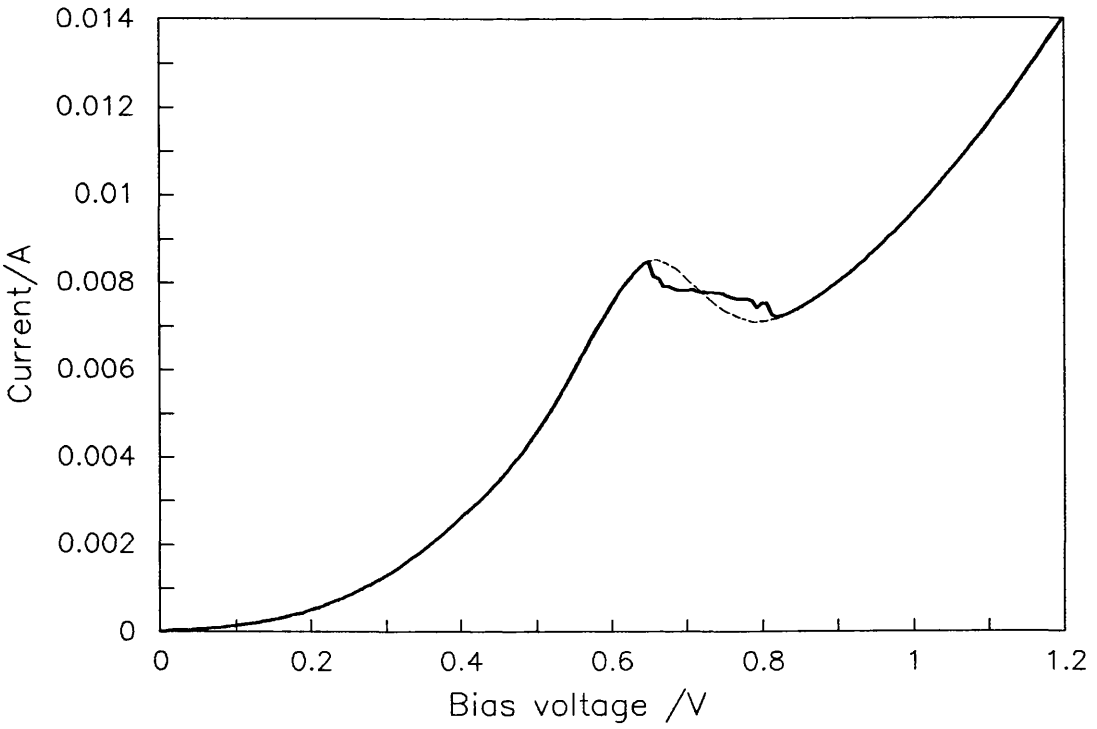

Figure 4.16. The I-V characteristic of the GWS160 $45\times45\mu m^2$ device. The solid line represents the experimental characteristic while the dashed line is the result of cubic spline fitting and interpolation to approximate a stable NDC region.

over the actual experimental frequency range. The uncertainty in the values of the device parameters should thus be of the same order as that of the measurement, i.e., 10%.

The main source of error involved repeatability of the tuner settings. This could have been avoided by using a high quality microwave switch as indicated in figure 4.13.

The theoretical maximum frequency of oscillation occurs when the real part of the device impedance vanishes. Thus, from (4.5), with $C=3.4$pF, $R=107\Omega$ and $R_s=4.7\Omega$ as determined,

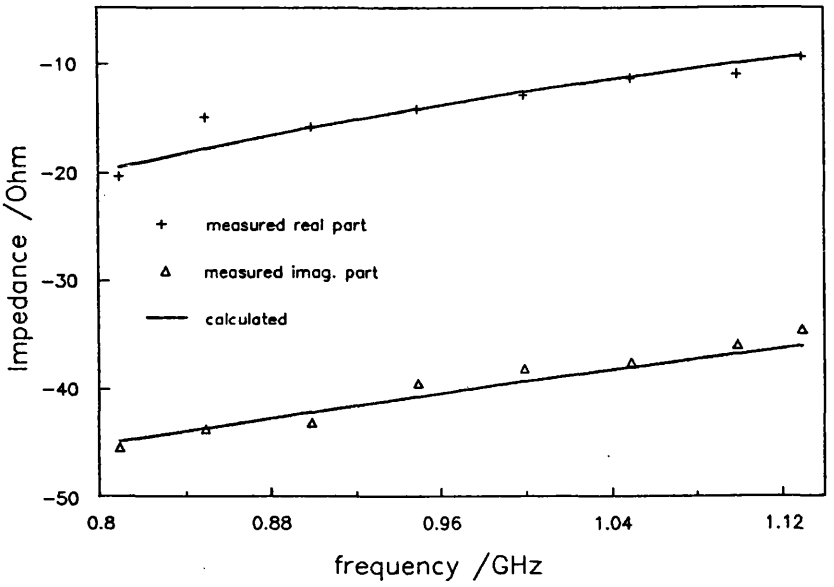

Figure 4.17 . Large-signal impedance of the 45μm device as a function of frequency. The curves are fitted to the data on the basis of the equivalent circuit model of figure 4.15, with $C = 3.4$pF, $R = 107\Omega$, $R_s = 4.7\Omega$ and a bonding wire inductance of 0.37nH.

f_{max} is about 2 GHz. As this is an **intrinsic** device limit to the oscillation frequency based on measurements at -13 dBm, it is in reasonably good agreement with observation.

Finally, having obtained an estimate of the device impedance, the voltage amplitude across the actual device can be estimated assuming purely sinusoidal oscillations from

$$P_{out} = \frac{|V_0|^2}{2\Re(-Z_d)} \qquad (4.15)$$

where P_{out}= -13dBm is the output power. This leads to a value of V_0 between about 45 and 30mV. One can thus understand, at least qualitatively, the reason for the difference between the differential resistance estimate from the dc characteristic and the value obtained by curve-fitting the rf

data. The bias point chosen for the impedance measurements coincides with the point where the negative differential resistance has the lowest magnitude of 61 Ω, from the spline-fitted line of figure 4.16. During the oscillation cycle the instantaneous bias point is swept by about $\pm V_0$ from the dc value, the oscillations about this point thus smear out the minimum value of R shifting it to higher values.

4.3.2 Large-signal impedance of the RTD 523B

The configuration used for the measurements was similar to the one of figure 4.14 but, in this case, the 3.5mm mount described in chapter 3 was used in order to house the E10/A package and a HP8593A spectrum analyser in place of the HP8559A. The measurement procedure was the same as described in section 4.2.1, however the network analyser used to measure the impedance looking into the tuner from the package plane was a HP8510B. This was calibrated using standard open and short circuits, a standard fixed load and a sliding load.

The harmonics observed were more than 20 dB below the fundamental, thus the oscillations were practically single frequency. Tuner adjustments were made to obtain a power level of -8.4 dBm at frequencies spaced by about 33 MHz between 2.149 and 3.403 GHz at a bias voltage of 1.30V.

For practical reasons it was not possible to employ a microwave switch as shown in figure 4.13 in order to avoid errors introduced by lack of accurate repeatability of the tuner settings for the impedance measurements.

4.3.2.1 Observations

The output spectrum from this device was similar in nature to that of the GWS160. However, the fundamental frequency could be tuned between about 2 and 4 GHz and maximum power levels of about -7 dBm were achieved with a voltage bias of 1.30V. The strongest harmonic observed was the third and this was less than 20 dB below the fundamental.

As the tuner stub assembly is moved, say towards the device, the output frequency increases linearly with the position of the stub assembly until at some point a mode hop occurs resulting in a sudden shift with the fundamental at a lower frequency and several harmonics. The original spectrum could be retrieved by moving the stub assembly well back, extracting the stubs by about 2 mm and pushing them back in. This is due to tuning hysteresis.

Mode hops were sometimes observed to occur of their own accord when the above-mentioned tuner settings were approached but not surpassed.

Bias circuit oscillations were confirmed to be relaxation oscillations and again observed to disappear instantly with the advent of sharp spectral lines at microwave frequencies.

4.3.2.2 Results and Analysis

The measured impedances looking towards the tuner from the package plane were transformed through the E10/A package-mount model established in chapter 3. Thus, the resulting impedances give $-Z_d(f)$.

Assuming the equivalent circuit model of figure 4.15, the values of C, R and R_s which gave the best fit to the experimental data were:

C	0.31 pF
R	640 Ω
R_s	4.4 Ω

Figure 4.18 compares the measured impedance with that calculated from **(4.13)** and **(4.14)** using the above equivalent circuit element values. The experimental errors evident in figure 4.18 are mainly due lack of repeatability in the tuner settings.

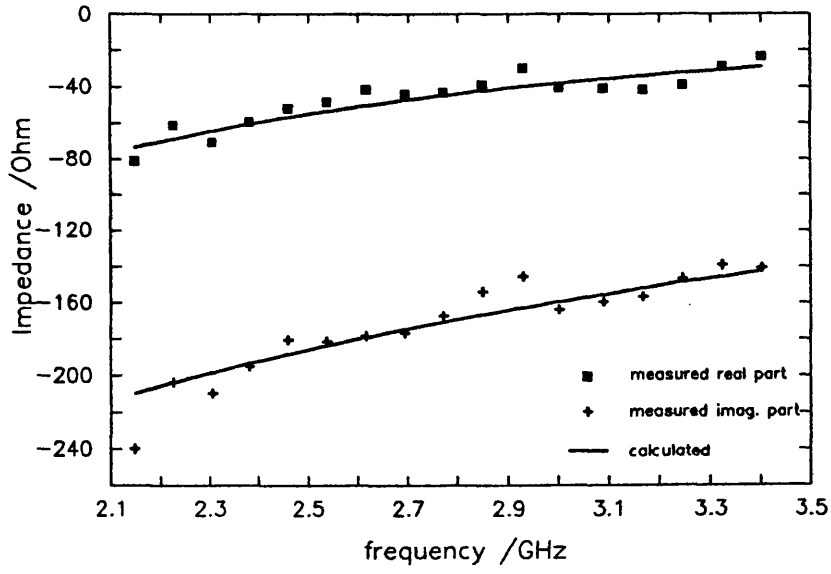

Figure 4.18 . Large-signal impedance of the 523B $20\times20\mu m^2$ device as a function of frequency. The curves are fitted to the data on the basis of the equivalent circuit model of figure 4.15, with $C=0.31$pF, $R=640\Omega$, $R_s=4.4\Omega$.

The maximum frequency of oscillation for the 523B estimated with the equivalent circuit element values determined here is 9.6 GHz which compares well with the value of 9.2 GHz

obtained by interpolating between the measured points in figure 4.11 of section 4.2.1.4 at 1.30V. However, the highest observed frequency was 4.2 GHz with an output power of -9 dBm. This is probably due to limitations of the tuning arrangement which did not allow it to support such high frequencies.

Applying **(4.15)** and with values of C, R and R_s as determined, it is possible to conclude that the rf voltage amplitude across the device was between about 150 and 90mV over the test frequency range.

The stable I-V characteristic of this device, shown in figure 4.1, gives the differential resistance magnitude at dc as 250 Ω at 1.30V bias. The fitted large-signal value was 640 Ω. Now, the differential conductance tends to zero as the voltage approaches 1.43V. Thus the voltage amplitude, as has been determined, would sweep the instantaneous voltage across the device into regions where the differential resistance greatly exceeds 250 Ω in magnitude and may even cross over into regions where this becomes positive. The average value of R during the cycle therefore increases.

Since the device capacitance is also voltage-dependent, it would behave in a similar way and one would expect the low frequency small-signal value to be considerably different from that determined from the large-signal measurements. In this case the small-signal capacitance was found to be 0.25pF at 1.30V from the results of section 4.2.1.2.

4.4 Summary of the main results and conclusions

The simple tunnel diode equivalent circuit has been applied to analyse the small-signal microwave properties of the RTD

523B. Results show that simulations based on this model are in excellent agreement with the experimental results. The device differential conductance and capacitance extracted by fitting this model to the small-signal admittance measurements are frequency-independent, at least up to 13 GHz, and will be useful in large-signal analysis.

The effect of signal power upon such measurements has also been investigated. It was shown that using a signal level of about -10 dBm gives results that cannot be accurately predicted by the model, especially with bias voltages within the NDC regions and over wide frequency ranges.

Impedance measurements on the GWS160 and 523B RTD's in a simple microwave oscillator circuit have confirmed that the use of this device equivalent circuit can be extended to the large-signal case with the conductance and capacitance values used being functions of bias voltage and rf output power. It was also observed that dc stability is not an important consideration when RTD's are used in high- or moderately high-Q cavities because when the devices are biased to oscillate and the impedance presented by the cavity is such as to support narrow bandwidth microwave oscillations, spurious oscillations in the bias line disappear.

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CHAPTER 5

LARGE-SIGNAL ANALYSIS OF A SIMPLE RTD MULTIPLIER

5.1 Introduction

A nonlinear impedance driven by a periodic source (the pump) gives rise to frequency multiplication. The main types of millimetre wave harmonic generators utilise either the nonlinear resistance of a forward biased Schottky barrier diode or the nonlinear capacitance of a reverse biased varactor diode.

Resistive multipliers have been in use since the early 1940's [1]. Since then, many workers have reported resistive diode multipliers operating in the millimetre-wave region with useful output powers [2,3,4,5,6,7,8,9,10,11,12]. The conversion efficiency for generating the nth harmonic of a resistive multiplier is fundamentally limited to n^{-2} [13,14,15]. In contrast, the Manley-Rowe relations [16] predict no limit below 100% efficiency for nonlinear reactance multipliers. The high efficiency of varactor multipliers has therefore made them attractive for use in solid state microwave power sources at frequencies up to about 100 GHz.

However, varactor multipliers have an inherent frequency limitation caused by the saturation velocity of the neutral space-charge boundary. At frequencies above about 100 GHz the usable nonlinearity of the transition capacitance diminishes because the carrier velocity in the space-charge layer cannot exceed the saturation velocity [17]. Hence, despite the excellent performance of some early varactor multipliers in the microwave region [18,19,20] the efficiencies of devices in the millimetre-wave band fell far below the levels predicted by theory [21]. It was not until quite recently that millimetre-wave reactive multipliers

began to achieve respectable output power levels and much of the improvement was due to advances in diode fabrication technology. Some recent state-of-the-art nonlinear reactance multipliers have found use as local oscillators in millimetre-wave mixers and heterodyne receivers where hitherto expensive and short-lived klystrons had been used. For example, Archer [22] reported a doubler exhibiting typically 10% conversion efficiency at an output frequency range of 100-260 GHz and a tripler at 215 GHz with 6% efficiency. Erickson [23] obtained a peak 6% efficiency at 266 GHz. Recently, a novel submillimetre wave tripler using a quantum-barrier-varactor diode [24] resulted in 5% conversion efficiency between 210 and 280 GHz and a quintupler efficiency of just below 0.2% at 310 GHz, comparable to state-of-the-art Schottky diode quintuplers.

5.2 Frequency multiplication with resonant tunnelling devices

5.2.1 Odd harmonic multiplier

The I-V curve of a RTD may be represented by a polynomial such as [25]

$$i(v) = \sum_{n=1}^{4} a_{2n-1} v^{2n-1} \qquad (v < 0.5\mathrm{V}) \qquad \textbf{(5.1)}$$

$a_1 = 0.32\mathrm{mAV}^{-1}$

$a_3 = 8.2\mathrm{mAV}^{-3}$

$a_5 = -124\mathrm{mAV}^{-5}$

$a_7 = 403\mathrm{mAV}^{-7}$

Suppose for simplicity we assume a purely sinusoidal pump voltage $v = v_o \cos\omega t$. Then, substituting for v in **(5.1)** and simplifying gives the time-dependent current in the RTD as

$$i(t)=\left(a_1 v_o+\frac{3}{4}a_3 v_o^3+\frac{5}{8}a_5 v_o^5+\frac{35}{64}a_7 v_o^7\right)\cos\omega t \qquad (5.2)$$
$$+\left(\frac{1}{4}a_3 v_o^3+\frac{5}{16}a_5 v_o^5+\frac{21}{64}a_7 v_o^7\right)\cos 3\omega t$$
$$+\left(\frac{1}{16}a_5 v_o^5+\frac{7}{64}a_7 v_o^7\right)\cos 5\omega t$$
$$+\frac{1}{64}a_7 v_o^7\cos 7\omega t$$

Only odd harmonics of i appear because of the point symmetry of the I-V relation. Figure 5.1 shows the calculated voltage and current across and in the RTD respectively over one cycle of the pump voltage. Figure 5.2 shows the calculated power spectrum assuming a 50Ω pump impedance. Several features of this spectrum are note-worthy. One of the most difficult problems in harmonic multiplier design is to terminate reactively all harmonics below the required output frequency. Since these harmonics are usually of larger amplitude than higher-order ones, power dissipation would be unacceptably high if they were to be resistively terminated. However, in the case of a RTD with an I-V characteristic of odd symmetry, the even harmonics are absent, leaving only odd harmonics to be considered. Moreover, according to the calculation, the largest component after the fundamental is the 5th harmonic. Thus, terminating the other harmonics resistively, about 9% conversion efficiency would still be theoretically possible. Sollner et al. [25,26] reported 1% conversion efficiency from 2 to 10 GHz in an unoptimised multiplying structure and 0.5% from 4.25 to 21.25 GHz in a coaxial circuit [27]. Fifth harmonic multiplication has been demonstrated with output at millimetre-wave frequencies [28]. A tripler with efficiency greater than 1.2% and 0.8 mW output power at about 250 GHz has been demonstrated [29]. Recently, a resonant tunnelling

device quintupler with output at 320 GHz was reported [30] to perform almost as well as current state-of-the-art Schottky barrier diodes.

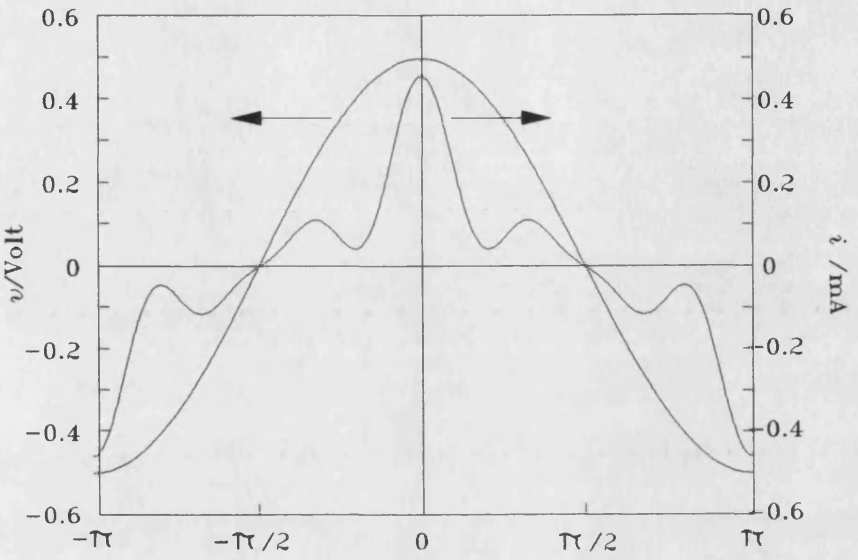


Figure 5.1. Calculated voltage and current across and in a hypothetical RTD, respectively, over one pump cycle.

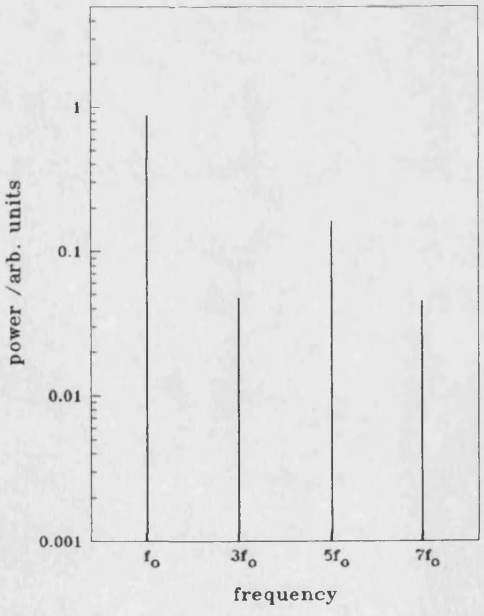


Figure 5.2. Calculated power spectrum assuming a 50Ω pump impedance. Note that the 5th harmonic output is the highest after the fundamental.

5.2.2 Doubler

Suppose that a RTD is biased at the peak current voltage V_p and a sinusoidal (pump) signal of frequency ω with amplitude v_0 is applied such that the excursion along the I-V characteristic over the pump cycle is $V_p \pm v_0$. If v_0 is small enough, the relevant part of the I-V curve may be approximated by a parabola:

$$\begin{aligned} i(v) &= I_0 + (I_p - I_0)\left[1 - \left(\frac{v - V_p}{V_p}\right)^2\right] \\ I_0 &= i(0) \\ &= \left\{ i(V_p \pm v_0) - I_p\left[1 - \frac{v_o^2}{V_p^2}\right]\right\}\frac{V_p^2}{v_o^2} \end{aligned} \qquad \textbf{(5.3)}$$

$i(V_p \pm v_0)$ may be determined from the I-V curve. Substituting for v in **(5.3)** gives

$$i(t) = I_0 + (I_p - I_0)\left(1 - \frac{v_0^2}{2V_p^2}\right) - \frac{v_0^2(I_p - I_0)}{2V_p^2}\cos 2\omega t \qquad \textbf{(5.4)}$$

Thus, the rf current in the RTD is also sinusoidal and has double the pump frequency. This simple analysis suggests that there is the potential of realising a frequency doubler based on the resonant tunnelling device. The attractive feature is that providing the pump amplitude is small enough, no harmonics are produced other than the second harmonic of the pump frequency, a fact which would greatly simplify its realisation.

The foregoing treatment completely neglects problems arising from the interaction of the pump signal and subsequent harmonics generated with the device parasitics and the embedding network. The signal power has to be effectively coupled from the input part of the circuit to the device and at the same time the harmonic of interest has to be coupled into another part of the circuit where it can be

utilised. Furthermore, the input and output circuits have to be effectively isolated from one another and a stable biasing arrangement designed to de-couple the dc and RF circuits over the entire operating frequency range.

In chapter 4, the influence of test signal power on microwave reflection measurements of an active device was investigated. It was concluded that the device-circuit-signal interaction is highly complex. A self-consistent method of large-signal analysis is therefore required in order to understand and simulate the behaviour of a RTD in a multiplier circuit. The following sections describe in detail the **multiple reflection technique** [31] and show how this can be used in the analysis of a simple RTD multiplier configuration.

5.3 Multiplier analysis

The analysis of the performance of a frequency multiplier involves only large signals, unlike mixers where both small- and large-signal analyses have to be performed. However, the large-signal analysis of both configurations need not differ significantly. In the present work, therefore, the mixer approach, which has been developed sufficiently well, will be adopted. As with mixers, the most difficult step in analysing multipliers is precisely that of determining the diode waveforms produced by the pump (or local oscillator in the case of mixers). High diode nonlinearities, the distributed nature of the elements comprising the multiplier and device parasitics only complicate matters.

Torrey and Whitmer [32] describe one of the first attempts at solving the large signal problem. They obtained analytical solutions by assuming a sinusoidal voltage at the diode terminals, i.e. that no harmonic voltages were present beyond the local oscillator (LO) frequency. In their analysis, Torrey and Whitmer considered both a purely resistive diode and one represented by a nonlinear conductance shunted by

a constant capacitance. The more complicated variable capacitance case was only considered qualitatively. Later analyses [33,34,35,36] included quantitative treatments of nonlinear capacitance, although making the same simplifying assumption of a sinusoidal driving voltage. Barber [37] indicated the necessity for removing this constraint at the LO frequency.

Fleri and Cohen [38] performed large signal analysis in a very simple lumped element embedding network. In their approach a numerical Runge-Kutta integration algorithm was used to solve the network state equations for the time-dependent diode voltage and current. Gwarek [39] extended this method to allow more general embedding circuits. He represented the embedding network as a simple lumped element circuit in series with a set of voltage sources, one at each LO harmonic. The amplitudes and phases of these generators are adjusted to keep the terminal impedance of the circuit equal to that of the actual embedding network. Although the scheme works well for many mixer circuits, it is strongly dependent on the guessed values of the lumped elements and does not converge for all embedding impedances [40].

An early form of the harmonic balance technique was used by Egami [41] to find the terminal voltage and current waveforms for a diode with constant capacitance. The mixer equivalent circuit was separated into two parts, one containing the linear embedding network, and the other containing the nonlinear diode elements. The voltages and currents in each half were then matched (or balanced) at all the LO harmonic frequencies using an iterative procedure. In this approach, the linear circuit problem (i.e. the embedding circuit) is solved in the frequency domain while a time domain solution is sought for the state equations representing the nonlinear

circuit. This method seemed to be effective when one or two LO harmonics were considered, but convergence to a steady state proved difficult when more harmonics were included.

Gupta and Lomax [42] described a method for large signal analysis of IMPATT oscillators where a pair of dual algorithms are used to update the estimates of either the diode voltage or current after each iteration. Convergence was reached once a stationary solution was obtained by this self-consistent approach. Hicks and Khan [43,44] have reported excellent results with a generalisation of the Gupta and Lomax procedure. The Hicks and Khan algorithms have since been used successfully on a variety of nonlinear circuits.

The large signal analysis technique used in the present work was originally developed by Kerr [31] and subsequently used by Siegel, Kerr and Hwang [40] in Schottky mixer and varactor multiplier analysis. It solves the nonlinear problem by iterating over a series of reflection cycles of the voltage waveforms between the diode and the embedding network. Like the harmonic balance methods, the algorithm operates in the time domain when considering the diode and in the frequency domain when dealing with the embedding network. This **multiple reflection technique** requires more computing time than either the methods of Gwarek [39] or Hicks and Khan [43,44], but solutions were obtained for all mixer and multiplier circuits which were studied by Siegel, Kerr and Hwang [40].

5.3.1 The multiple reflection technique

The large signal equivalent circuit of a nonlinear reactance multiplier is represented in figure 5.3. The intrinsic device is, as before, represented by a nonlinear conductance $g(v_d)$ shunted by a nonlinear capacitance $c(v_d)$, where v_d is the instantaneous voltage across the intrinsic device. The device series resistance, R_s, will here be assumed inde-

pendent of frequency[1] as this simplifies the analysis without any loss of generality. Since this equivalent circuit has been found to adequately represent large signal behaviour of resonant tunnelling devices at low frequencies (see chapter 4), this circuit was employed for specific RTD multiplier analyses and simulations to be described further on.

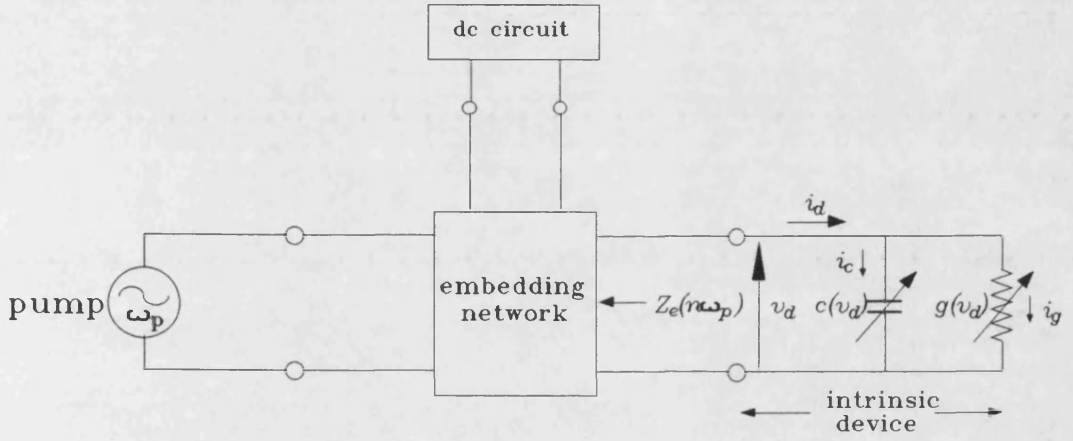


Figure 5.3. Large-signal equivalent circuit of a nonlinear reactance multiplier. Note that the intrinsic device does not include the series resistance.

Assuming that the device electrical characteristics $g(v_d)$, $c(v_d)$ and R_s, and the embedding network impedances at the pump frequency and a number of its harmonics are known, the analysis proceeds as follows.

According to Kerr [31], the circuit of figure 5.3 is modified by the insertion of a long transmission line of arbitrary impedance Z_0 between the embedding network and the intrinsic device as shown in figure 5.4. The reasons behind this

---

1 R_s will depend on frequency as this increases sufficiently such that there is a significant decrease in the skin depth. In general, R_s will also tend to be slightly reactive, especially at high frequencies.

artificial subdivision will soon become apparent. At any time there will be waves propagating in both directions along the transmission line. Once a steady state has been established, these waves will be of constant amplitudes and will contain frequency components at dc and many pump harmonics. If the length of the transmission line is chosen to be an integral number of wavelengths at the pump frequency, and hence also at the pump harmonics, the steady state waveforms at the two ends of the transmission line will be identical. Thus, the two representations of figures 5.3 and 5.4 are equivalent in this respect.

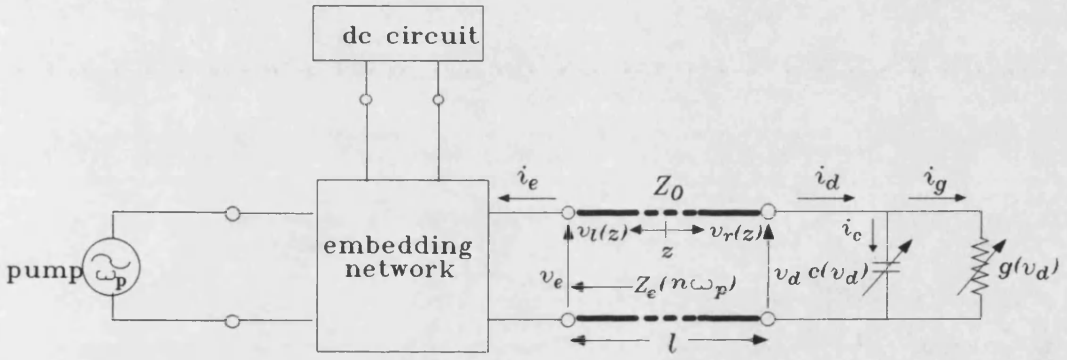


Figure 5.4. The large-signal equivalent circuit of the multiplier shown in figure **5.3** is here modified by the inclusion of a long transmission line of arbitrary characteristic impedance Z_0.

The insertion of the transmission line serves two purposes: firstly, it allows the device-transmission line subnetwork to be treated in the time domain for the determination of the device voltage and current, while treating the embedding subnetwork separately in the frequency domain, and, secondly, since the steady state is sought for the interaction of both the embedding network and intrinsic device **separately** with the transmission line, problems associated with transients generated upon reflection at the two ends are eliminated.

Thus, the device waveforms are determined from figure 5.4 by alternately solving two much simpler circuits, each of which is in steady state with the transmission line.

The analysis starts by determining the voltage and current waveforms in the time domain. The time-dependent voltage and current are then transformed to the frequency domain, where the waveforms at the two ends of the transmission line are compared. If these are the same then the large signal problem has been solved; i.e. v_d and i_d are respectively equal to v_e and i_e in figure 5.4. If the terminal conditions are not satisfied, then a new waveform reflected off the embedding network is determined and the circuit analysis repeated. The solution converges when waveforms from the last reflection cycle match the ones from the previous cycle to within a specified accuracy.

5.3.2 Details of the large signal analysis

Referring to figure 5.4, at a general point z along the line there will be a set of left- and right- travelling waves which are related to the total voltage (v) and current (i) at point z by

$$v(z) = v_r(z)+v_l(z) \qquad (5.5)$$

$$i(z) = i_r(z)-i_l(z) \qquad (5.6)$$

$$= \frac{v_r(z)-v_l(z)}{Z_0}$$

As the transmission line (of length l) is an integral number of wavelengths at all harmonics, the conditions that must prevail in steady state are:

$$v(0) = v(l) \qquad (5.7)$$

$$i(0) = i(l) \qquad (5.8)$$

Since a form of the harmonic balance technique will be used to assess the degree of convergence according to the conditions **(5.7)** and **(5.8)** in the frequency domain, v_d and i_d must be expanded into Fourier series:

$$v_d(t) = \sum_{n=0}^{\infty} \mathbf{V}_{d_n} \exp(jn\omega_p t) \qquad \textbf{(5.9a)}$$

$$\mathbf{V}_{d_n} = \frac{1}{T} \int_{-T/2}^{+T/2} v_d(t) \exp(-jn\omega_p t)\, dt \qquad \textbf{(5.9b)}$$

$$i_d(t) = \sum_{n=0}^{\infty} \mathbf{I}_{d_n} \exp(jn\omega_p t) \qquad \textbf{(5.10a)}$$

$$\mathbf{I}_{d_n} = \frac{1}{T} \int_{-T/2}^{+T/2} i_d(t) \exp(-jn\omega_p t)\, dt \qquad \textbf{(5.10b)}$$

where ω_p is the radian frequency of the pump. Using the Fourier coefficients $\mathbf{V}_{d_n}$ and $\mathbf{I}_{d_n}$ of the intrinsic device voltage and current, the conditions **(5.7)** and **(5.8)** may be expressed in the frequency domain by

$$-\frac{\mathbf{V}_{d_n}}{\mathbf{I}_{d_n}} = Z_e(n\omega_p) + R_s, \quad n = 2,3,..,\infty \qquad \textbf{(5.11)}$$

$$\frac{\mathbf{V}_p - \mathbf{V}_{d_1}}{\mathbf{I}_{d_1}} = Z_e(\omega_p) + R_s \qquad \textbf{(5.12)}$$

$$\frac{\mathbf{V}_{dc} - \mathbf{V}_{d_0}}{\mathbf{I}_{d_0}} = Z_e(0) + R_s \qquad \textbf{(5.13)}$$

where $\mathbf{V}_p$ and $\mathbf{V}_{dc}$ are the Thévenin equivalent pump and dc voltages, respectively, seen by the intrinsic device.

Now, assume that the transmission line in figure 5.4 is terminated by an impedance Z_0 until time $t=0$ when the device is first connected to the circuit. At time $t=0^+$ a right

propagating wave will exist on the line, with Fourier components at dc and at the pump frequency. On the device side of the transmission line ($z=l$), these are

$$\mathbf{V}_{r_0}(l) = \mathbf{I}_{r_0}(l) = \frac{\mathbf{V}_{dc}Z_0}{Z_0+R_s+Z_e(0)} \equiv \mathbf{V}_0 \tag{5.14}$$

for the dc component and,

$$\mathbf{V}_{r_1}(l) = \mathbf{I}_{r_1}(l) = \frac{\mathbf{V}_pZ_0}{Z_0+R_s+Z_e(1)} \equiv \mathbf{V}_1 \tag{5.15}$$

at the pump frequency.

Figure 5.5a represents the nonlinear subnetwork consisting of the intrinsic device and the transmission line in the time domain, with $\mathbf{V}_{r_0}$ and $\mathbf{V}_{r_1}$ given by **(5.14)** and **(5.15)**. The state equation for this circuit is

$$\frac{dv_d}{dt} = \frac{1}{c(v_d)}\left[\frac{v_s(t)-v_d(t)}{Z_0}-i_g(v_d)\right] \tag{5.16}$$

where $v_s(t)$ is the sum of the voltage sources across the transmission line. Equation **(5.16)** is a nonlinear differential equation which can be solved numerically over a number of pump cycles, starting from an initial value of $v_d(t=0)$, if $c(v_d)$ and $i_g(v_d)$ are known. This then gives the steady state voltage waveform $v_d(t)$ which will contain frequency components at all the pump harmonics. We now require the Fourier series coefficients of this new left-travelling wave. Solving **(5.5)** and **(5.6)** for $v_l(z)$ gives

$$v_l(z) = \frac{v(z)-i(z)Z_0}{2} \tag{5.17}$$

such that at the device-end of the transmission line,

$$v_l(l) = \frac{v_d(t) - i_d(t)Z_0}{2} \tag{5.18}$$

Now, since the transmission line is an integer number of wavelengths at all the pump harmonics, equation **(5.7)** holds. Thus, the Fourier series coefficients of the left-traveling wave incident on the embedding network are given by

$$\mathbf{V}_{l_n} = \frac{1}{2}(\mathbf{V}_{d_n} - \mathbf{I}_{d_n}Z_0), \quad n = 0, 1, 2, .., \infty \tag{5.19}$$

where $\mathbf{V}_{d_n}$ and $\mathbf{I}_{d_n}$ are the Fourier series coefficients of $v_d(t)$ and $i_d(t)$ taken over one pump cycle with period $T = 2\pi/\omega_p$. The frequency domain analysis proceeds by calculating the reflected amplitude components at each pump harmonic from a knowledge of the reflection coefficient, Γ_n, which is given by

$$\Gamma_n = \frac{Z_e(n) + R_s - Z_0}{Z_e(n) + R_s + Z_0} \tag{5.20}$$

The wave reflected from the embedding network becomes the new right-travelling wave on the transmission line and its Fourier coefficients at all harmonic frequencies above the pump are

$$\mathbf{V}_{r_n} = \Gamma_n \mathbf{V}_{l_n}, \quad (n > 1) \tag{5.21}$$

At dc and the pump frequency, the respective components are incremented by the dc and pump voltages:

$$\mathbf{V}_{r_0} = \Gamma_0 \mathbf{V}_{l_0} + \mathbf{V}_0 \tag{5.22}$$

$$\mathbf{V}_{r_1} = \Gamma_1 \mathbf{V}_{l_1} + \mathbf{V}_1 \tag{5.23}$$

Figure 5.5b represents the additional voltage components produced by the device over the previous pump cycle as a string of voltage sources, the sum of which defines the new

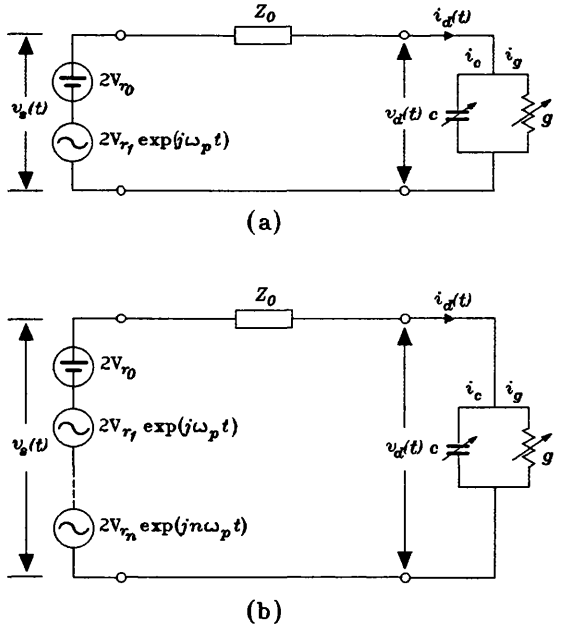


Figure 5.5. Equivalent circuit of the nonlinear subnetwork consisting of the intrinsic device and the transmission line to be analysed in the time domain; **(a)** at time $t=0$, and **(b)** $t>0$, after the first reflection cycle.

$v_s(t)$. This enables the state equation **(5.16)** to be restated in terms of this new voltage and solved for $v_d(t)$ over the next cycle. This procedure is repeated until the conjugate match condition is met at all the harmonic frequencies, i.e. from **(5.11) - (5.13),**

$$-\frac{\mathbf{V}_{d_n}}{\mathbf{I}_{d_n}} = \frac{\mathbf{V}_{e_n}}{\mathbf{I}_{e_n}} = Z_{e_n} + R_s, \qquad (n>1) \tag{5.24}$$

$$\frac{\mathbf{V}_p - \mathbf{V}_{d_1}}{\mathbf{I}_{d_1}} = Z_{e_1} + R_s, \qquad (n=1) \tag{5.25}$$

5.4 The multiplier analysis program

The performance of a multiplier can be assessed by its conversion efficiency which is defined here as:

$$\text{conversion efficiency to } n^{th} \text{ harmonic} = \frac{\text{output power at } n^{th} \text{ harmonic}}{\text{power absorbed at pump frequency}} \qquad (5.26)$$

This quantity depends upon the large signal waveforms at the diode and on the embedding impedance of the multiplier at the pump frequency and its harmonics. These intrinsic device voltage and current waveforms may be found using the multiple reflection technique described in section 5.3. The multiplier analysis program described here implements this technique to estimate the diode waveforms and the input and output impedances of the multiplier. This results in the calculation of conversion efficiency (or conversion loss[1]).

The program is a modification of an original developed by Siegel, Kerr and Hwang [40]. Section 5.4.1 outlines the large signal calculation which is carried out in subroutine LGSIG which forms the main body of the program and is responsible for calculating the steady state diode waveforms - the most fundamental procedure in the whole analysis. The program listing given in Appendix V is one particular version used to simulate the performance of a RTD multiplier over a range of pump powers and bias voltages. Some of these results are discussed in section 5.5.

5.4.1 The large signal analysis subroutine

The multiplier program begins with a call to subroutine **LGSIG** to perform the large signal analysis using the multiple reflection technique. The embedding network impedances $Z_{e_n} = Z_e(n\omega_p)$ from the pump frequency up to the highest

---

1 Defined as $10\log\left(\frac{\text{power absorbed at pump input port}}{\text{output power into the } n^{th} \text{ harmonic port impedance}}\right)$ in dB.

harmonic considered (of order **NH**, assumed even) are formed in subroutine **ZEMBED** which is called by **LGSIG**. The real and imaginary parts of the embedding impedances are stored in arrays **ZER** ($\equiv \Re(Z_{e_n})$) and **ZEI** ($\equiv \Im(Z_{e_n})$). The dc term is considered separately. The series resistance (**RS**), which is here assumed purely resistive[1], is added to each element of **ZER** and a complex array **ZEMB(I) = ZER(I) + RS + jZER(I), I=1,...,NH** is formed.

Following the calculation of the embedding impedances **ZEMB** and **ZEMBDC** (the dc embedding impedance), **ZEMBDC** is arbitrarily set equal to Z_0 (**Z0**), the characteristic impedance of the hypothetical transmission line. This has no effect on the final steady state solutions, as long as we adjust the dc Thévenin equivalent voltage source accordingly during the calculation of the actual bias voltage at the end of the large signal analysis. In fact, in the mixer program of Ref.[40], the embedding impedance at dc and the LO frequency are, at this stage, both equated to Z_0 as this modification speeds up the nonlinear analysis by reducing the number of constraints imposed on the device waveforms by the embedding network. In the case of a multiplier, however, the dc current is not generally known apriori.

At this point it is worthwhile digressing to describe how this problem is resolved in the subroutine **CALBIAS** which is called by **LGSIG** after the nonlinear analysis has been performed. With **ZEMBDC** set to Z_0, the dc bias voltage used in the program will be different from that which would actually be required to produce the calculated device rectified current (**IDCOS(1)**), unless the latter is negligibly small. Referring to figure 5.6a, which represents the dc equivalent circuit of the actual multiplier, the actual bias voltage can be written as

---

1 At high frequencies it would probably be necessary to include a reactive part with **RS**. This does not detract from the generality of the analysis.

$$V_{d_{bias}} = I_{d_0}(Z_{e_0}+R_s)+V_{d_0} \qquad \textbf{(5.27)}$$

where I_{d_0} = **IDCOS(1)**, $Z_{e_0}+R_s$ = **ZEMBDC** and V_{d_0} is the dc component of the device voltage (**VDCOS(1)**). The dc circuit solved in the multiplier analysis program is shown in figure 5.6b, where the Thévenin equivalent voltage, $V'_{d_{bias}}$, is given by

$$V'_{d_{bias}} = I_{d_0}Z_0+V_{d_0} \qquad \textbf{(5.28)}$$

Thus, form **(5.27)** and **(5.28)**,

$$V_{d_{bias}} = I_{d_0}(Z_{e_0}+R_s-Z_0)+V'_{d_{bias}} \qquad \textbf{(5.29)}$$

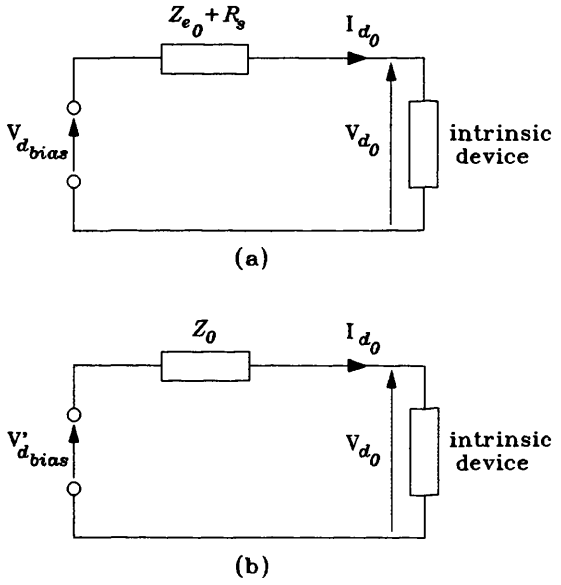


Figure 5.6. **(a)** The dc equivalent circuit of the actual multiplier. **(b)** The dc circuit solved in the multiplier analysis program where $V'_{d_{bias}}$ is the Thévenin equivalent voltage.

The reflection coefficients (**RHO**) between the transmission line and the embedding network are now calculated at the pump frequency and all harmonics up to **NH**, using equation **(5.20)**. The reflection coefficient at dc (**RHODC**) is zero since **ZEMBDC** has been set equal to the characteristic transmission line impedance. At this stage, the circuit of

figure 5.5a applies and the initial voltage wave (**VR**) on the transmission line propagating to the right towards the device is determined from equations **(5.14)** and **(5.15)**. The multiple reflection algorithm is now initiated.

LGSIG calls the subroutine **DRKGS**, an IBM SSP integration routine implementing a Runge-Kutta algorithm with adaptive stepsize control, to solve the state equation **(5.16)** by determining $v_d(t)$ (**Y(1)**) in the time domain. The period of the voltage waveform is scaled so that one pump cycle occurs in 2π seconds. Subroutine **FCT** is called by **DRKGS** to set up **(5.16)** and evaluate $dv_d(t)/dt$ using the appropriate instantaneous value of the transmission line voltage sources $v_s(t)$ (**VS**). The main modifications made to the program of Ref.[40] were in this particular subroutine. The original version evaluates the instantaneous values of $i_g(v_d)$, $c(v_d)$ and $g(v_d)$ by calculation using analytical expressions for these quantities. In the present work, these values are obtained by interpolation from tabulated experimental data. It is assumed here that the device being analysed in the multiplier configuration has been adequately characterised at dc and microwave frequencies to obtain $i_g(v_d)$ and $c(v_d)$, as has been described in chapter 4, over a suitable bias voltage range and that an adequately effective small-signal equivalent circuit model of the device has been established over the frequency range of interest. The program should thus be capable of simulating the behaviour of **particular** devices in the desired multiplier configuration. The merits of this technique are discussed in section 5.5, where results of actual simulation runs are compared with experiment.

The routine **DRKGS** makes periodic calls to the subroutine **OUTP** at the appropriate stages of the integration to store the values of $v_d(t)$, $i_d(t)$, $i_g(t)$, $i_c(t)$, $c(t)$ and $g(t)$. Thus, at the end of one complete pump cycle, these quantities have been stored at equally spaced time intervals in their respective arrays, **VDDATA**, **IDDATA**, **IGJDAT**, **ICJDAT**, **CJDATA**

and **GJDATA**. The Fourier series coefficients of $v_d(t)$ and $i_d(t)$ over the pump cycle are then determined by a call to subroutine **DFORIT**. The coefficients V_{d_n} and I_{d_n} were defined in equations **(5.9)** and **(5.10)** using the single ended exponential series representation. **DFORIT** uses the trigonometric series representation such that V_{d_n} = **VDCOS(N+1)** - *j***VDSIN(N+1)** and I_{d_n} = **IDCOS(N+1)** - *j***IDSIN(N+1)**, where **VDCOS(N+1)** and **IDCOS(N+1)** are the cosine coefficients and **VDSIN(N+1)** and **IDSIN(N+1)** are the sine coefficients of the device voltage at harmonic **N**. This establishes the components of the left propagating wave on the transmission line (**VL**) and hence convergence according to equations **(5.24)** and **(5.25)** can now be tested by forming the ratios $|V_{d_n}/I_{d_n}|/|(Z_{e_n}+R_s)|$ (**ZQMAG**) at all harmonics up to **NH**. An integer flag, **ZQFLAG**, is augmented by 1 for every harmonic that does not give a value of unity to within the specified accuracy (**ZQACC**) for this ratio. If the value of **ZQFLAG** is non-zero, the right-propagating wave coefficients (**VR**) are calculated using equations **(5.21)** - **(5.23)**. The time domain integration of the state equation **(5.16)** is repeated by calling **DRKGS** whence subroutine **FCT** would then use the new coefficients **VR** to determine the voltage sources v_s and hence restate **(5.16)** on demand.

This procedure is repeated until the value of **ZQFLAG** is established as zero, i.e., conditions **(5.24)** and **(5.25)** are satisfied at all pump harmonics considered. **LGSIG** then calls subroutine **MLTPER** to calculate the multiplier performance as described in section 5.4.2 and the subsequent call to **CALBIAS** calculates the actual multiplier voltage required (**VDCMLT**) to give the calculated rectified current **IDCOS(1)** from **(5.28)**.

5.4.2 Port impedances and conversion properties

The multiplier nonlinear analysis yields the device voltage, current, capacitance and conductance waveforms at a particular pump power level and dc bias. These waveforms can then be used to determine the input and output impedances and the conversion properties.

Figure 5.7 represents the equivalent circuit upon which is based the calculation of the multiplier conversion loss. The input impedance of the multiplier at any port is given by

$$Z_{in} = R_s + \frac{V_{d_n}}{I_{d_n}} \tag{5.30}$$

In the multiplier analysis program V_{d_n} and I_{d_n} are given by

$$V_{d_n} = \text{VDCOS(N+1)} - j\,\text{VDSIN(N+1)} \tag{5.31}$$

and

$$I_{d_n} = \text{IDCOS(N+1)} - j\,\text{IDSIN(N+1)} \tag{5.32}$$

The minus sign is required for the conversion from the trigonometric Fourier series representation generated by **DFORIT** into the complex form used elsewhere in the program.

The available pump power at port 1 is, from figure 5.7,

$$P_{avail} = \frac{|V'_{d_1}|^2}{8\Re(Z_{e_1})} \tag{5.33}$$

The program requires the value of V'_1, the pump amplitude, and this is calculated in subroutine **LGSIG** as **VLO** from equation **(5.33)**.

The source impedance is not, in general, matched to the input impedance at port 1. This means that only a portion of the available pump power is absorbed by the device, the rest being reflected. The absorbed power P_{abs} (**PABS**) is calculated using

$$P_{abs} = \frac{1}{2}\Re\left[(\mathbf{V}_{d_1}+\mathbf{I}_{d_1}R_s)\mathbf{I}_{d_1}^*\right] = \frac{1}{2}\Re[Z_{in}(1)]|\mathbf{I}_{d_1}|^2 \qquad \textbf{(5.34)}$$

The power output to port n depends on the output impedance of this port, i.e., the embedding impedance at harmonic n, such that from figure 5.7,

$$P_{out} = \frac{1}{2}|\mathbf{I}_{d_n}|^2\Re(Z_{e_n}) \qquad \textbf{(5.35)}$$

In terms of the intrinsic device voltage $\mathbf{V}_{d_n}$, the output power P_{out} (**POUT**) is

$$P_{out} = \frac{1}{2}\frac{|\mathbf{V}_{d_n}|^2\Re(Z_{e_n})}{|Z_{e_n}+R_s|^2} \qquad \textbf{(5.36)}$$

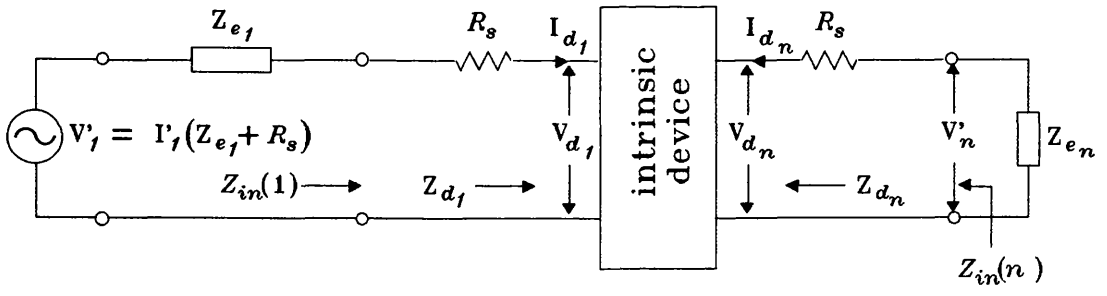


Figure 5.7. Equivalent circuit for the calculation of the multiplier conversion loss.

Finally, the conversion efficiency, defined as the ratio of the output power to the absorbed power at the pump frequency in equation **(5.26)**, enables us to express the multiplier efficiency $\eta_{i,k}$ in converting power from port i to port k as

$$\eta_{i,k} = \frac{P_{out}(k)}{P_{abs}(i)} = \frac{|\mathbf{I}_{d_k}|^2 \Re[Z_{in}(k)]}{|\mathbf{I}_{d_i}|^2 \Re[Z_{in}(i)]} \qquad \textbf{(5.37)}$$

Normally one is interested in the conversion efficiency from the pump port to the nth harmonic port, in which case the conversion loss at port n is expressed as

$$\mathbf{LOSS}(n) = 10\log\left(\frac{P_{abs}(1)}{P_{out}(n)}\right) = -10\log(\eta_{1,n}) \qquad \textbf{(5.38)}$$

The subroutine **MLTPER** is called at the end of the nonlinear analysis to perform the above calculations.

The definition of conversion efficiency (and consequently conversion loss) as stated in **(5.37)** is not strictly conventional. The object of the experiments and calculations described in section 5.5 was, however, to investigate the behaviour of a RTD when pumped with a microwave signal and not an attempt at designing and optimising a proper multiplier circuit. As such **(5.37)** expresses the conversion efficiency in a way which is effectively independent of the degree of mismatch at the input port.

In the case of a device, such as a RTD, exhibiting negative differential conductance, it is possible that the reflected power exceeds the incident. Hence, there might be gain at the fundamental frequency because the device acts as a reflection amplifier when biased in the NDC region. Thus, P_{abs} will be negative and equations **(5.37)** and **(5.38)** will become ambiguous. For this reason, it was elected to resort to convention in such cases by substituting P_{abs} by the incident power into a matched load in **(5.37)** and **(5.38)**.

5.5 Experiment and analysis

This section describes a simple multiplier configuration used with the RTD 523B as the active device. It compares some of the experimental results obtained, mainly output

power at the observed harmonics and rectified current as a function of bias voltage, with calculations performed using the computer program described in section 5.4 and listed in Appendix V. The device equivalent circuit model used was that derived in chapter 4 with the experimentally determined series resistance, differential conductance and capacitance.

5.5.1 Measurement of the harmonic output power

Figure 5.8 shows the multiplier circuit and measurement set-up used to determine the power generated at a number of harmonics when the device is pumped at a set frequency and power level. The coaxial circuit is simple and its practical implementation facilitates accurate measurements of the embedding impedance seen by the device under test (DUT) at the pump frequency and its harmonics, thus enabling accurate determination of the available input and output power levels.

The microwave pump signal source used was a HP8350B sweep oscillator which was coupled to a 10 dB coupler (Triangle Microwave^{TM} model CA-691) through an isolator (which transforms the source impedance to 50Ω). The pump signal then passes through the rf input port of the bias network (HP11612A) to reach the DUT, where some of the incident power is reflected and some absorbed. The device then generates harmonics because of the nonlinear nature of its I-V characteristic. These harmonics, along with the reflected part of the pump signal, then travel back along the input path through the coupler, which samples the output. The output power spectrum is then examined on the spectrum analyser (HP8593A) and the harmonic power levels measured. The dc circuit included a Time Electronics 9814 voltage calibrator in series with a Keithley 617 electrometer, both of which are programmable, thus enabling measurement of rectified current. In practice the measurement procedure was automated by using a pc with IEEE-488 interface capabilities as controller. This enabled a large number of

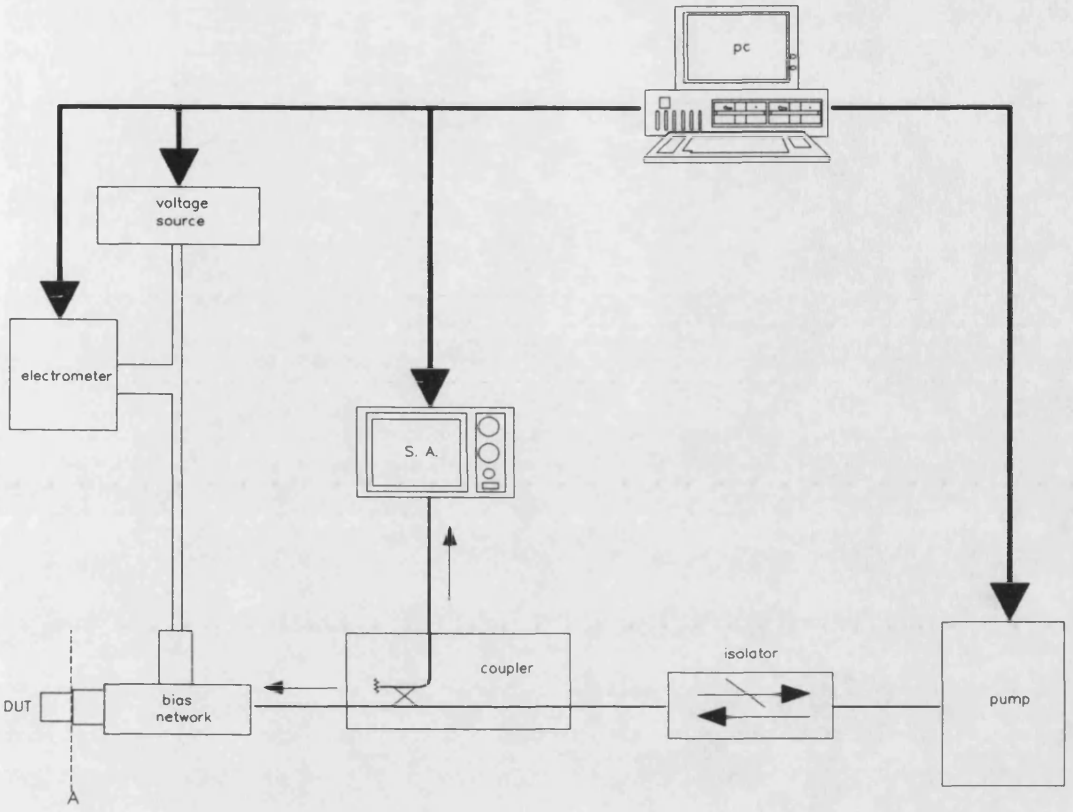


Figure 5.8. Simple multiplier circuit and measurement set-up used to determine the output power at the observed harmonics.

measurements of harmonic output and rectified current as a function of bias voltage at a number of different pump frequencies and power levels.

The microwave powers measured as described here are not the actual outputs from the device. In general the device is not matched to the input and output port impedances[1] and hence these must be determined at all frequencies of interest for two reasons:

---

1 The circuit is here regarded to consist of the device attached to the embedding network and thus there is only one physical port with a set of (generally) different impedances at different harmonics.

1. to determine the coupling between the device package plane and the spectrum analyser input port, this will enable calculation of the actual power delivered by the device into the embedding network beyond the package,

2. these impedances are required by the multiplier analysis program in order to perform the large-signal analysis and calculate the harmonic output power levels.

The coupling between the packaged device plane A (figure 5.8) and the spectrum analyser input port can be defined with reference to figure 5.9. Here the circuit between plane A, the coupler output port (2) and the spectrum analyser input port (3) is represented by a 3-port network. If a generator with source impedance equal to Z_0 is connected as shown to port 1 at reference plane A, then this sees the input impedance Z_{in} at this port, which will not always be matched to Z_0. In fact, it can be observed from figure 5.10, which represents the VSWR at the packaged device plane A as measured with a HP8510B network analyser, that port 1 is not matched to 50Ω within certain frequency bands above about 6 GHz. This is to be expected since the design frequency band of the coupler was about 2 - 5 GHz.

Now, the incident power P_{inc} in figure 5.9 is the power which would be delivered to a matched load and this can be accurately measured at all frequencies of interest. Part of the incident signal is reflected giving rise to P_{ref}. A sample of the power absorbed in Z_{in} will appear at port 3 to be measured by the spectrum analyser. This absorbed power, P_{in}, is the required quantity and is thus given by

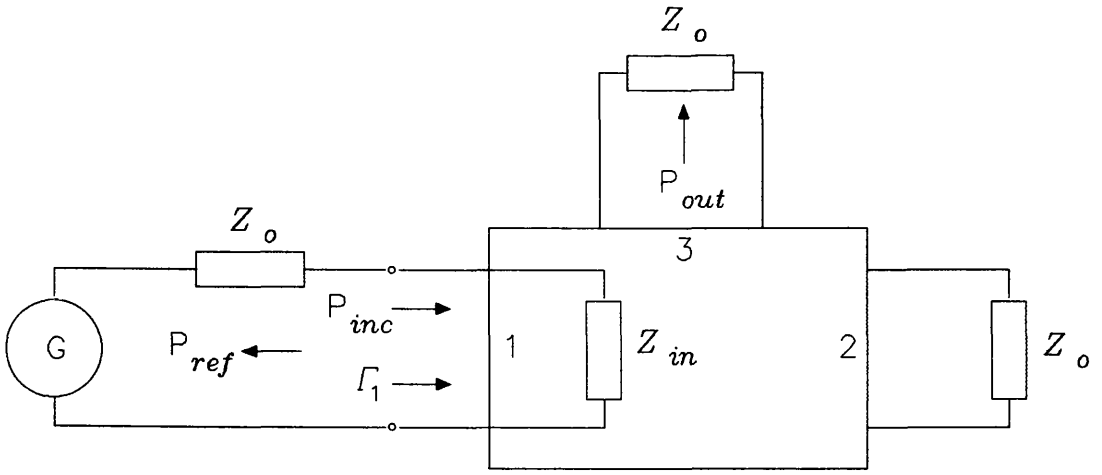


Figure 5.9. 3-port network representation of the microwave circuit used to establish the coupling between ports 1 and 3 of the multiplier configuration.

$$\begin{aligned} P_{in} &= P_{inc} - P_{ref} \\ P_{ref} &= P_{inc}|\Gamma_1|^2 \\ \therefore\ P_{in} &= P_{inc}(1-|\Gamma_1|^2) \end{aligned} \qquad \textbf{(5.39)}$$

where Γ_1 is the reflection coefficient at port 1 (reference plane A). The coupling κ between ports 1 and 3 is thus defined as

$$\kappa = 10\log_{10}\left(\frac{P_{in}}{P_{out}}\right)\text{dB} \qquad \textbf{(5.40)}$$

Hence, adding $\kappa(f_n)$ to the measured n^{th} harmonic output in dBm gives the power absorbed in Z_{in} at the frequency f_n, which is equivalent to the output power calculated in the program. κ was calculated at frequencies of interest (figure 5.11) from reflection coefficient measurements at reference plane A and from power measurements at port 3 with the HP8350B sweeper connected to port 1 through an isolator. The incident power for these measurements was determined separately on the HP8593A spectrum analyser.

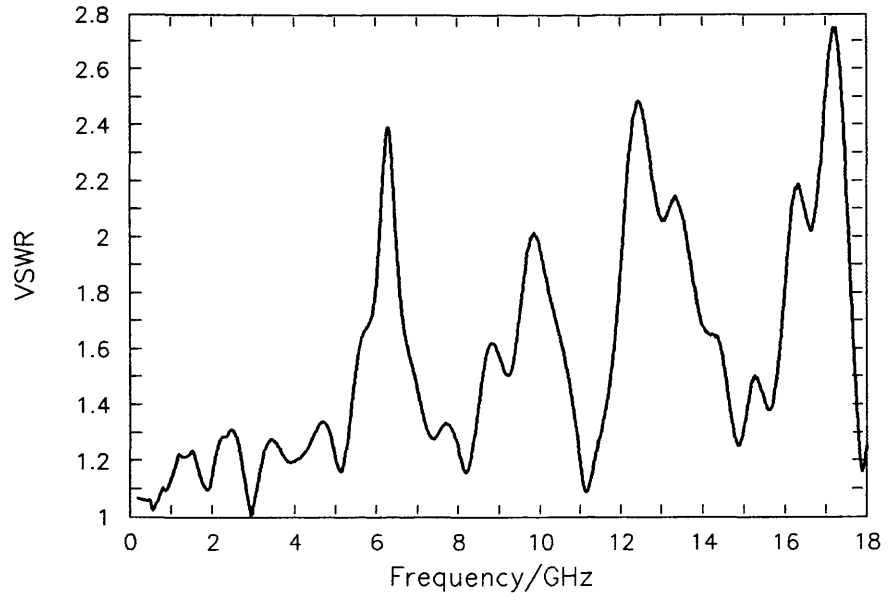


Figure 5.10. VSWR as a function of frequency as measured at reference plane A of figure 5.8.

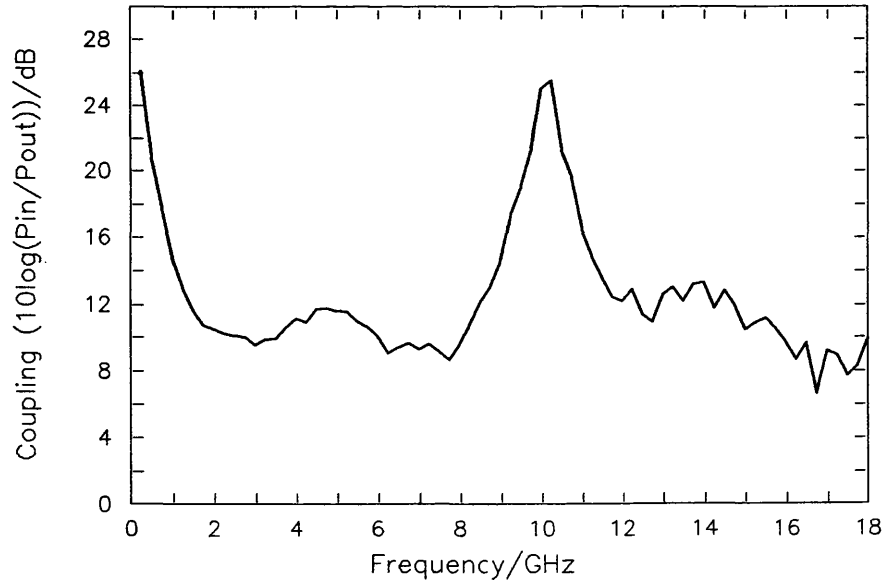


Figure 5.11. Coupling in dB between ports 1 and 3 of figure 5.9 as a function of frequency.

Figure 5.11 indicates that the coupling is about 10 dB between the frequency ranges 2 - 8 GHz and 12 - 18 GHz. At X-band frequencies and below about 2 GHz, κ rises up to about 25 dB. However, owing to the wide dynamic range of

the spectrum analyser, useful measurements can still be made within these bands, since the coupling has been determined accurately.

5.5.2 Experimental results and simulation for a 1 GHz pump signal

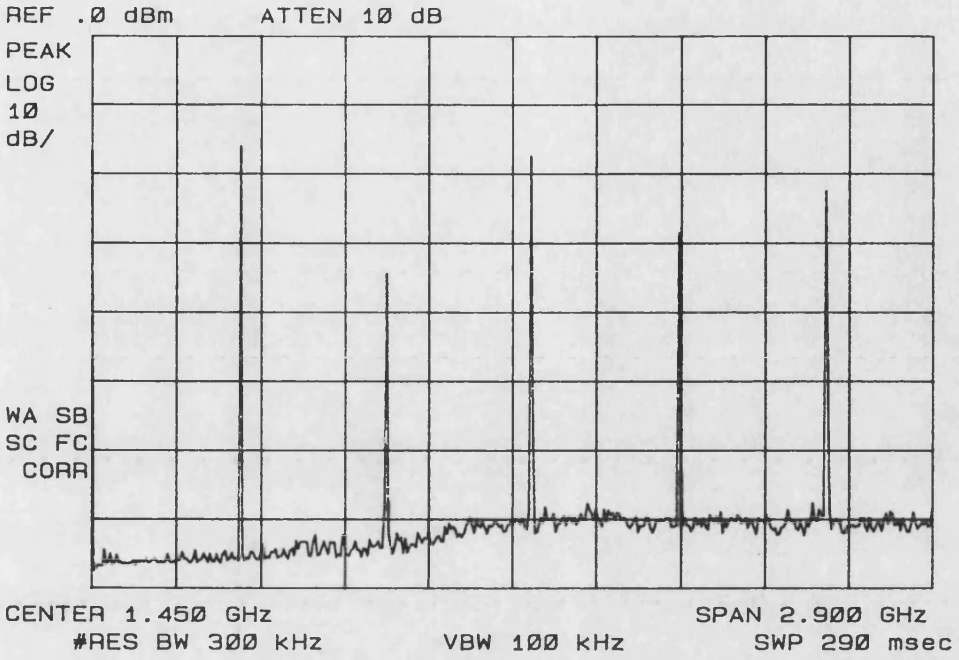
5.5.2.1 Harmonic output power

The test set-up shown schematically in figure 5.8 was used to measure the output power at the first 8 harmonics[1] at different pump frequencies and power levels as a function of bias voltage. At moderately high pump power levels (> 1 dBm) and/or bias voltages close to the NDC regions, higher harmonics right up to the highest measurable frequency were identified. Figure 5.12 shows a typical power spectrum of the RTD 523B pumped at 0.5 GHz at about 10 dBm, with the device at zero bias. The first line at 0.5 GHz represents the reflected signal. As can be expected, the odd harmonics are in general higher than the neighbouring even harmonics. This is due to the odd symmetry of the I-V characteristic.

For the purpose of simulation, the experimental results of chapter 4 were used to supply the multiplier program with the necessary data. Specifically, the device current and conductance, derived from the dc characteristic, and the capacitance c as well as dc/dv, obtained by numerical differentiation from the small-signal values of c, were tabulated in an input file together with all the other data elements required by the program. The voltages in the tabulation

1 The limitations imposed on frequency were partly due to the coaxial circuit and partly to the spectrum analyser. The measurement circuit included sma connectors which are specified up to 18 GHz, and the HP8593A maximum measurement frequency is 21 GHz.

a.



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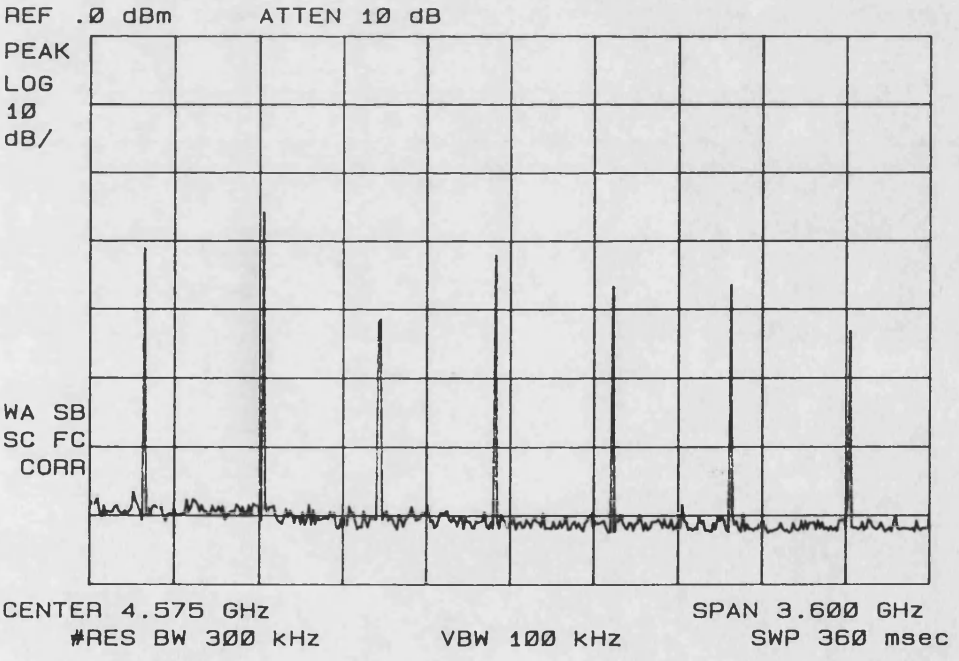

Figure 5.12. A typical power spectrum generated by the 523B in the circuit of figure 5.8 (b is a continuation of a). The pump frequency was 0.5 GHz at a pump power level of about 10 dBm with the device unbiased.

were adjusted for series resistance using the same value derived in chapter 4, namely 4.4Ω. Harmonics up to the eighth were considered in the analysis.

It was observed that with high power levels and/or high bias voltages, the time-domain integration of **(5.16)** demanded parameter values at voltages outside the measured range and as a consequence the convergence to the steady state solution could not be obtained. This was remedied by extrapolating the tabulated values as realistically as possible. For this purpose, the current beyond the tabulated points was assumed to increase in proportion to the square of the bias voltage, while the capacitance was assumed to approach zero exponentially. There is no experimental basis for these assumptions since the extrapolation was extended to ±50V [1] and therefore well outside the safe bias range of the device. The reason for such an apparently excessive extension of the tabulation range is that at certain instances during the derivative calculations, the integration algorithm might be required to calculate differences close to the machine precision. This might lead to instability. Clamping the voltage artificially to within the measured range did not prove to be effective at high bias voltages and/or pump power levels as either the analysis was inaccurate or convergence impossible. It was therefore hoped that by clamping the voltage to within the extended range would help to re-establish convergence more accurately. In fact, it was then found possible to obtain reasonably accurate simulations of multiplier performance at voltages right up to the extremes of the measured range and convergence was obtained in all the analyses performed.

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1 The extent of this extrapolation might seem excessive. However a similar technique is often used which clamps calculated parameters during numerical integration to below limits which are far beyond the expected ranges. For example Siegel et al. [40] clamp the device voltage to below 100V in their mixer analysis.

Figure 5.13a-g show the measured and calculated output powers at harmonics up to the 8^{th} for a pump signal of 1.30 dBm (available power) at 1.00 GHz, with the I-V characteristic of the 523B superimposed on figures 5.13a and b. The agreement between experiment and calculation is good, at least up to the 5^{th} harmonic. The simulated outputs diverge from measurement as higher bias voltages are reached. This may (at least partly) be due to inaccuracy in the extrapolated current, conductance and capacitance which was found necessary in order to artificially extend the range over which these values are input to the program. However, the calculated outputs still predict the same general trend of the measurements and mirror the slight divergence from odd-symmetry of the I-V and C-V characteristics. In particular refer to figure 5.13c and d. The point of inflection at about -0.3V occurring in the 4^{th} harmonic output is weaker than the corresponding one in forward bias. Although the calculated power in these regions is about 3 dB higher than the experimental value the same trend is evident. Similarly, the minimum power output at the 5^{th} harmonic at about -0.3V is higher than that at 0.2V; the calculations predict this difference, although not accurately.

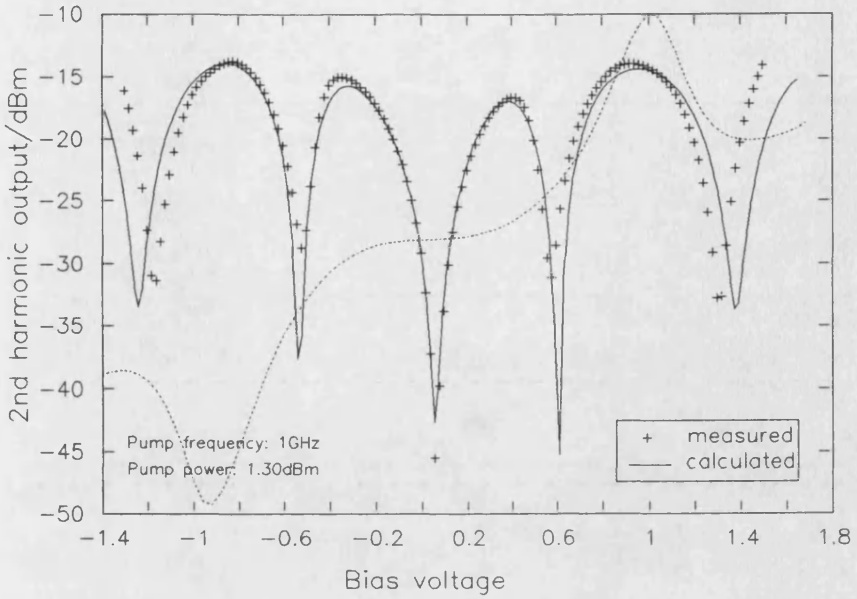

Figure 5.13. a

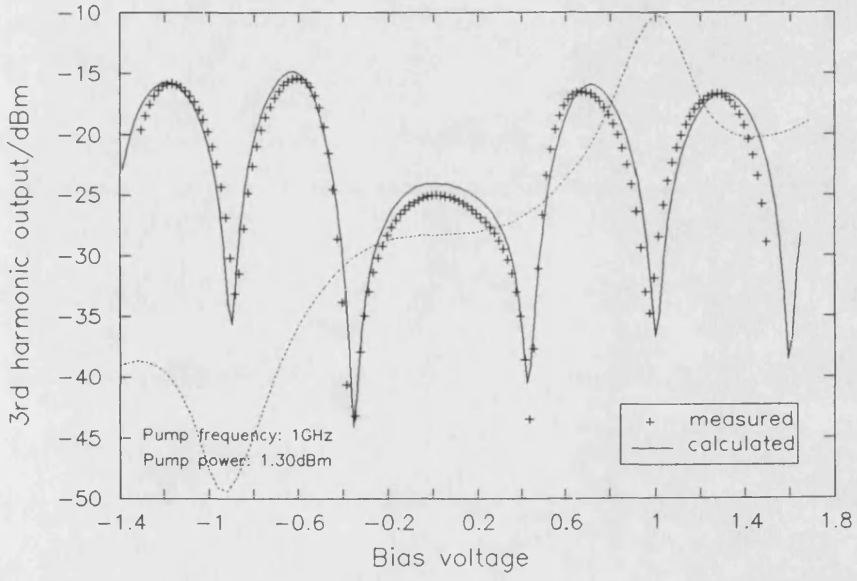

Figure 5.13b

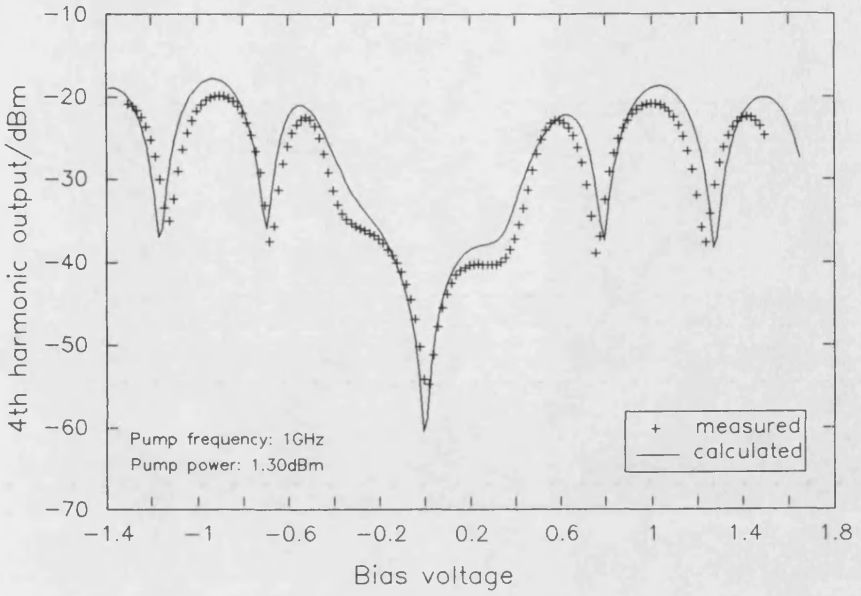

Figure 5.13c

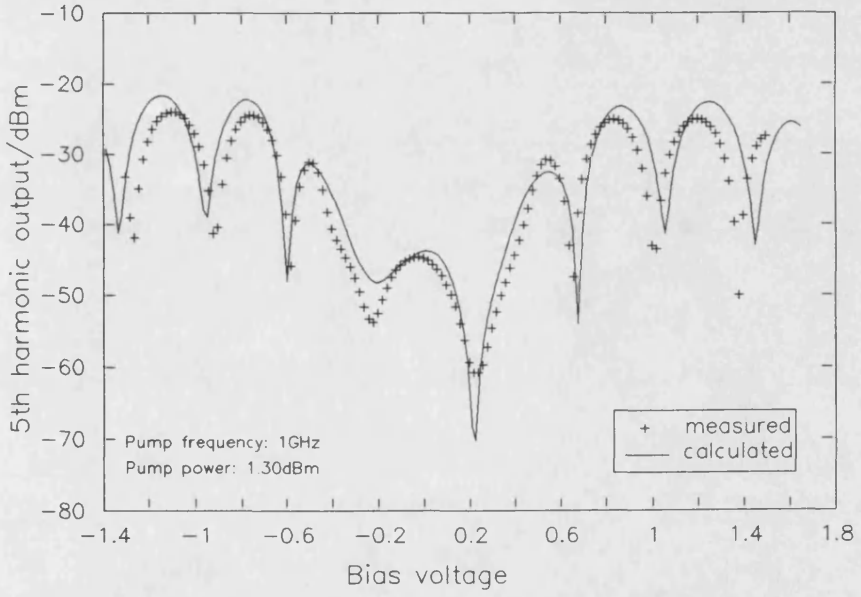

Figure 5.13d

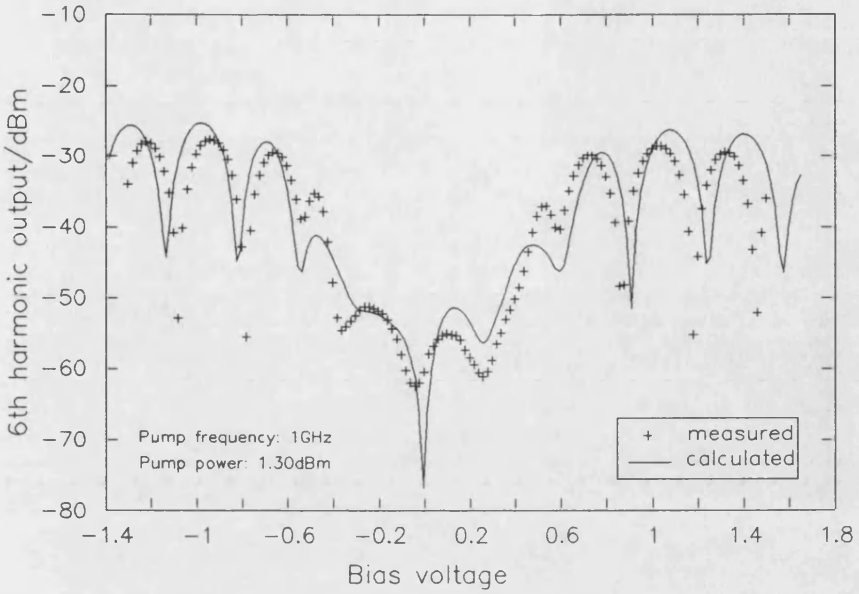

Figure 5.13e

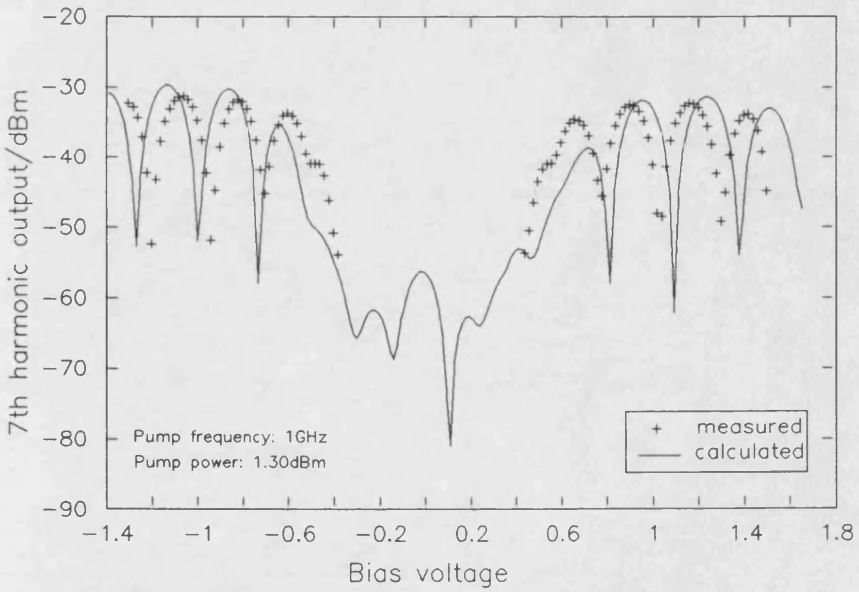

Figure 5.13f

Referring to the 2nd and 3rd harmonic power of figure 5.13a and b the relative positions of the maxima and minima can perhaps be understood as follows. At zero bias the voltage across the RTD makes roughly equal excursions from the bias point of about ±0.6V, as can be observed from figure 5.14, which represents the calculated voltage as a function of

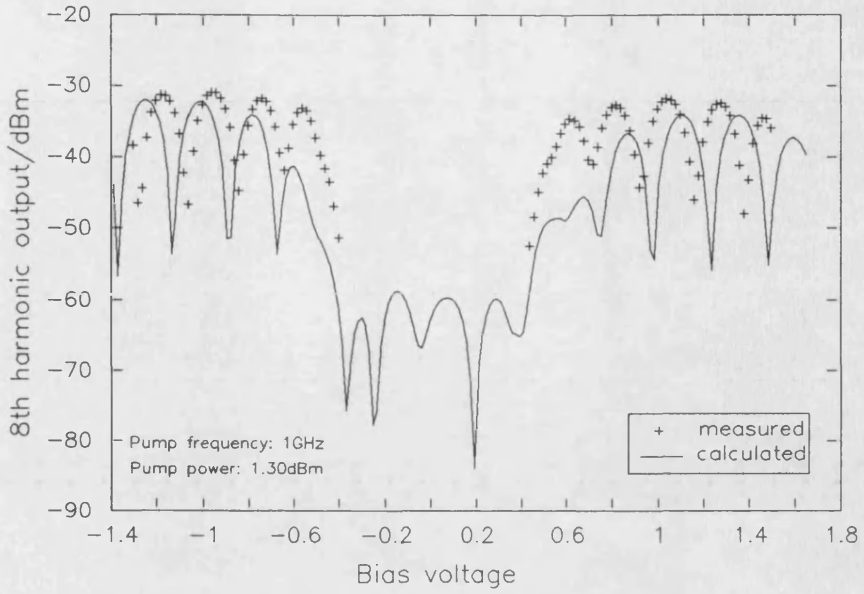

Figure 5.13g

time at 0, 0.43, 0.60 and 1.0V when the 523B is pumped at about 1.30 dBm at 1.0 GHz. The region of the I-V characteristic swept at zero bias has odd-symmetry, thus explaining the coincidence of the odd-harmonic maxima with the even-harmonic minima evident at zero bias in figure 5.13. As the bias voltage moves into the region before the peak positive differential conductance point at about 0.43V, the part of the I-V characteristic swept loses the odd-symmetric character as this part is nearly parabolic. Increasing the voltage still further (~0.6V) causes the peak positive voltage swing to sweep into the NDC region, thus spanning over an approximately cubic section of the characteristic. Biasing the device at the peak current point (~1V) will now cause the rf voltage sweep to sample an essentially even-symmetric part of the I-V characteristic and thus the even harmonics dominate.

In general, it was observed that correspondence between the bias voltages for maxima and minima in the output power at odd and even harmonics corresponds approximately to the following rule for pump power levels below about 2 dBm:

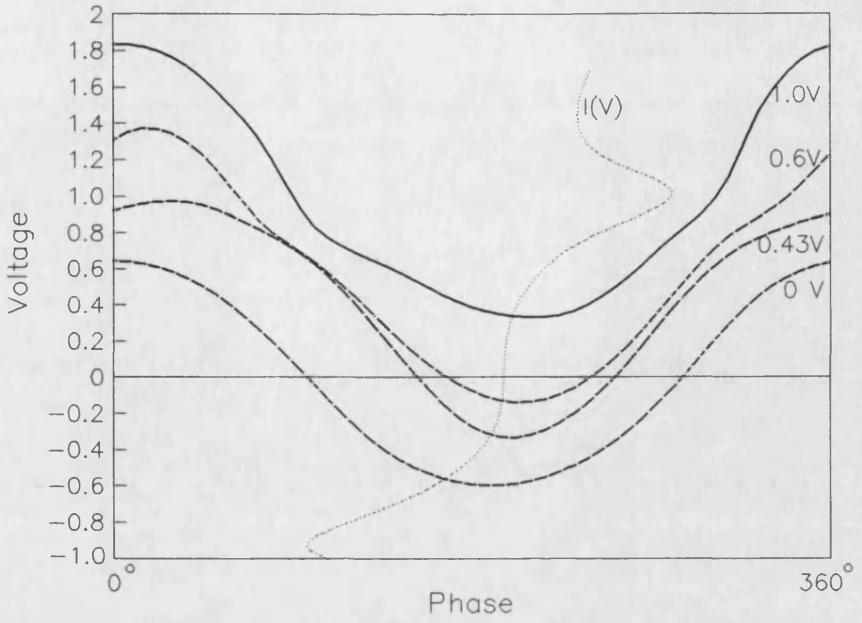

Figure 5.14. The calculated voltage across the 523B over one pump cycle at a frequency of 1 GHz and power level 1.30 dBm. Also shown is the I-V characteristic plotted on the same voltage axes for comparison; the current scale is arbitrary.

$$\begin{aligned} \mathbf{V}_{odd}^{max} &= \mathbf{V}_{even}^{min} \\ \mathbf{V}_{odd}^{min} &= \mathbf{V}_{even}^{max} \end{aligned} \qquad \textbf{(5.41)}$$

where $\mathbf{V}_{odd/even}^{max/min}$ is the column vector of bias voltages corresponding to the maxima / minima in the odd / even harmonic output.

5.5.2.2 Conversion loss and efficiency

The determination of conversion loss and efficiency as defined in equations **(5.38)** and **(5.37)** requires knowledge of the power absorbed by the device at the pump frequency. The multiplier program calculates this from **(5.34)** and the measurement set-up described in section 5.5.1 allows P_{abs} to

be estimated from the reflected power at the pump frequency, which also appears on the spectrum analyser display (see figure 5.12) and was measured for this purpose. The measured value of the reflected power is appropriately scaled by the coupling κ at the pump frequency as described in section 5.5.1 in order to determine the actual power reflected into port 1 of figure 5.9. The difference between the known incident power and the reflected power must then be the required power absorbed by the device.

Figure 5.15 shows the conversion loss to 2^{nd}, 3^{rd}, 4^{th}, 5^{th} and 6^{th} harmonics for a pump power level of 1.30 dBm at 1.0 GHz as a function of bias voltage. Again we see that the simulations predict the same general trends of the experimental results, with divergences between the two increasing with bias voltage. Figure 5.15 also shows that the maxima in conversion loss for odd harmonics coincide with the minima for the even harmonics and vice-versa as in the case of the output powers of figure 5.13.

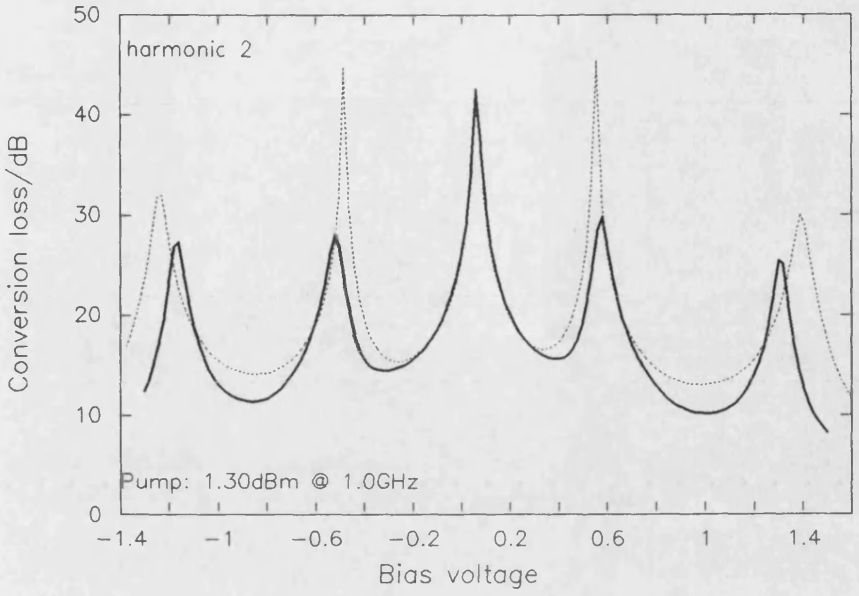

Figure 5.15. a

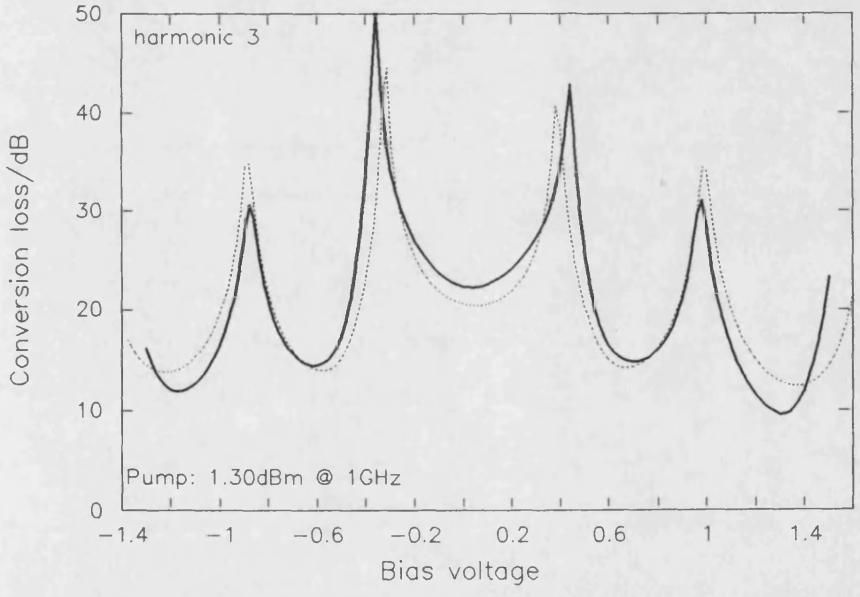

Figure 5.15b

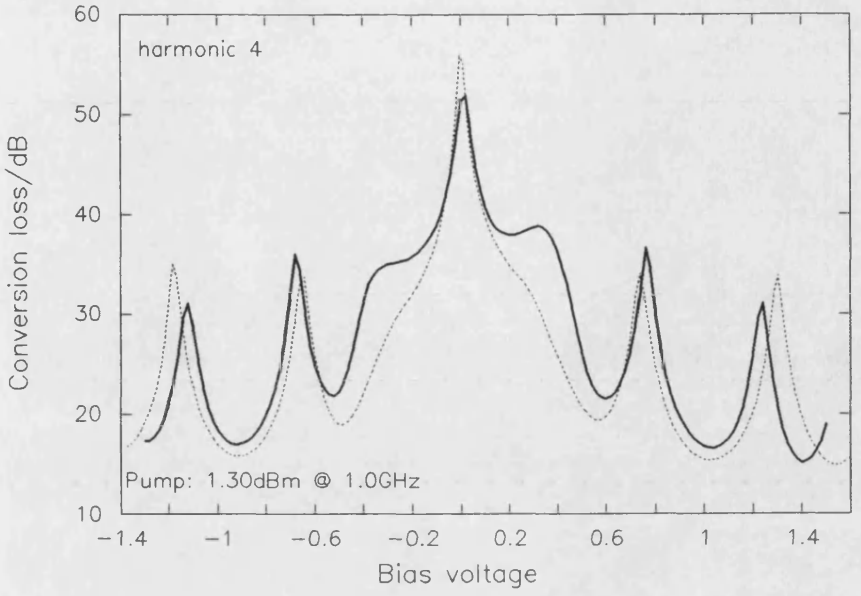

Figure 5.15c

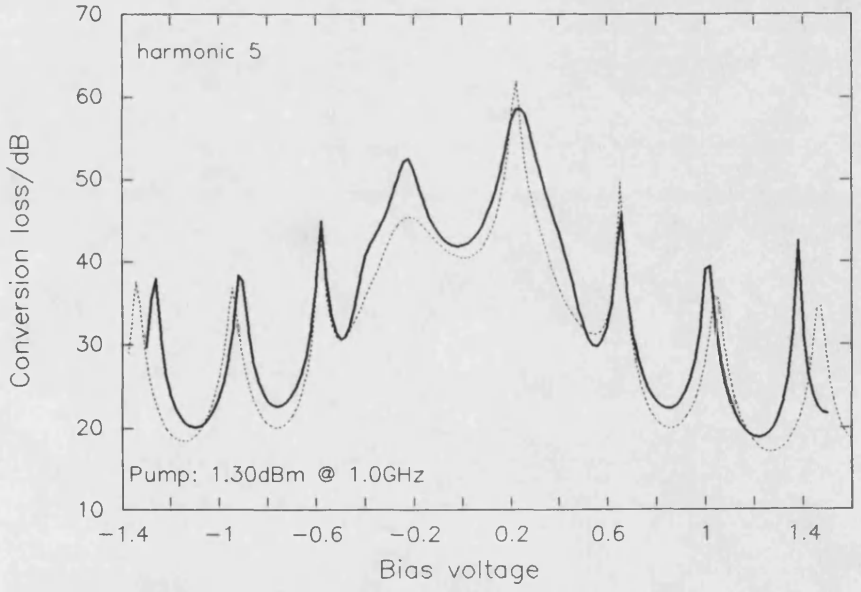

Figure 5.15d

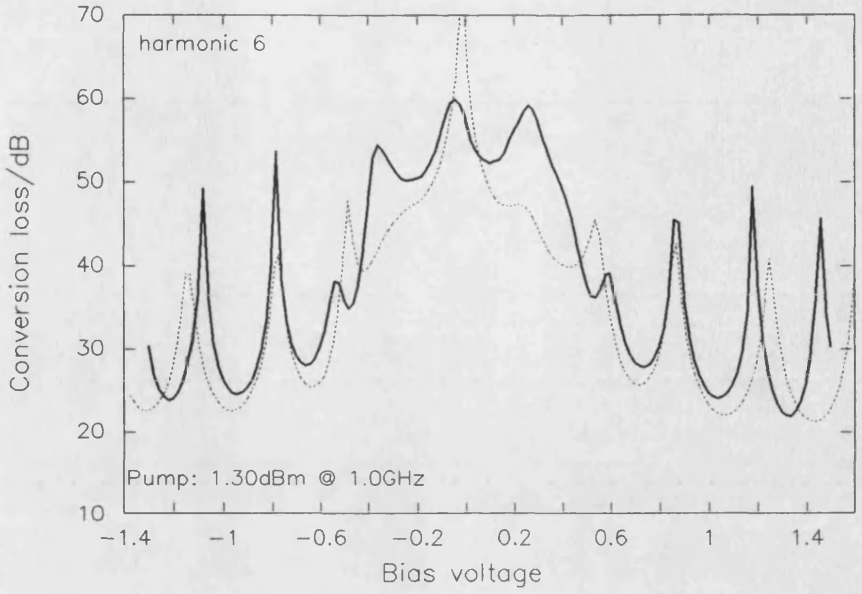

Figure 5.15e

Efficiencies of about 14% were measured for 2nd harmonic conversion with a pump power level of 1.30 dBm at 1 GHz at bias voltages corresponding to the minima of figure 5.15a and in excess of ±1.4V. For bias voltages within the NDC regions conversion efficiencies to the 3rd and 5th harmonics peaked to about 12% and 1.3%, respectively. The limit for purely resistive diode multipliers [13,14,15] would suggest 11.1% and 4.0% conversion efficiency for these harmonics, thus, even with the unoptimised test set-up described in section 5.5.1, the harmonic conversion properties of the RTD seem promising. Table 5.1 gives the maximum observed and calculated conversion efficiencies over three different pump power levels; 1.30, 5.28 and 10.53 dBm at 1.0 GHz. The power at which these efficiencies were measured is the lowest used (1.30 dBm) and in this respect, the large-signal analysis predicts basically the same result except for the 7th harmonic, where the maximum efficiency was obtained at 10.53 dBm.

The maximum conversion efficiencies obtained experimentally are shown in figure 5.16 compared with calculated values for a pump signal frequency of 1 GHz at the 1.30, 5.28 and

Table 5.1: Maximum conversion efficiencies for 1.0 GHz pump signal

Harm. (No.)	Meas. Eff. %	PPL* (dBm)	Calc. Eff. %	PPL* (dBm)
2	14.9	1.30	8.41	1.30
3	11.5	1.30	5.93	1.30
4	3.02	1.30	3.21	1.30
5	1.30	1.30	1.53	1.30
6	0.637	1.30	0.752	1.30
7	0.220	1.30	0.255	10.53
8	0.276	1.30	0.157	1.30

*Pump power level

10.53 dBm power levels. Measured and calculated data show the same trend (except for the 7^{th} harmonic) in that at the lowest pump power levels, conversion efficiency is markedly higher. Now, refer to figure 5.17, which represents the calculated device voltage and current over one pump cycle at a bias voltage of 1.43V for the three pump power levels. Both the voltage and, even more so, the current show evidence of relatively smaller harmonic content at the higher power levels. This is due to the larger voltage swings obtained in the latter cases (e.g., about ±1.9V for the 10.53 dBm pump signal) which result in the device voltage being swept over a region of the I-V characteristic which is significantly wider than the highly nonlinear region between about 0.9 and 1.4V during the pump cycle.

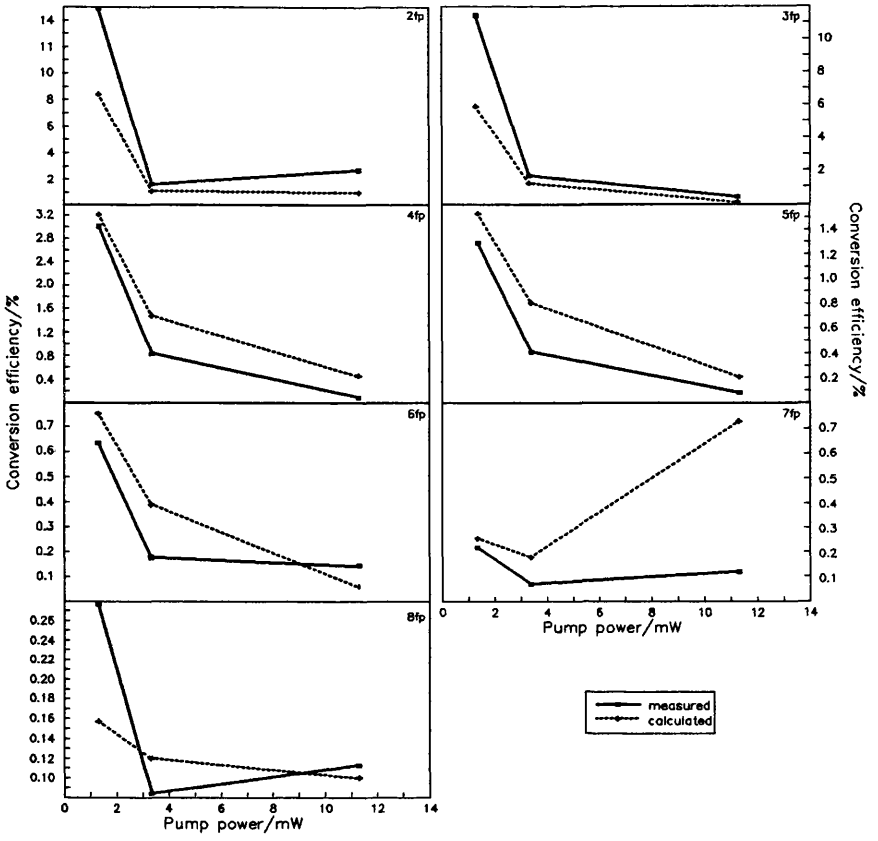

Figure 5.16. Measured and calculated maximum conversion efficiencies for pump power levels of 1.30, 5.28 and 10.53 dBm at 1.0 GHz.

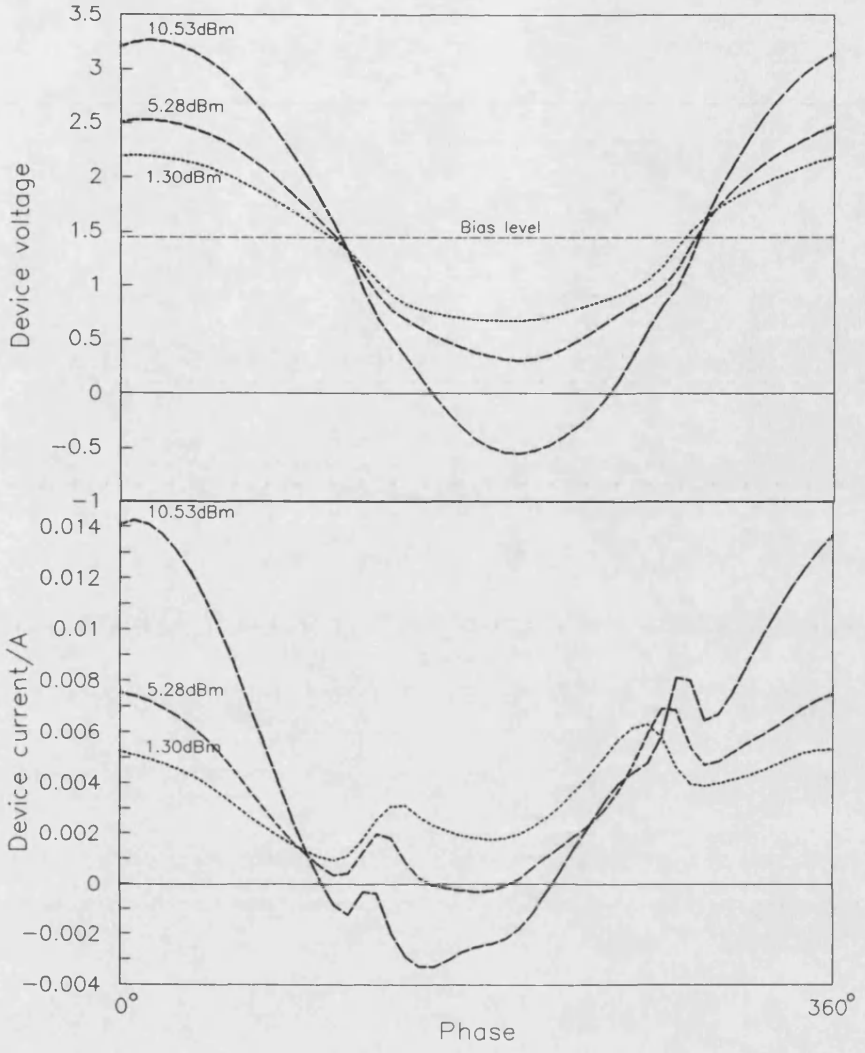

Figure 5.17. Calculated device voltage and current over one pump cycle for pump power levels of 1.30, 5.28 and 10.53 dBm at 1.0 GHz. The first eight harmonics were considered assuming a bias voltage of 1.43V for the calculation.

5.5.2.3 Rectified current

Since the resonant tunnelling device has a nonlinear I-V characteristic it will rectify an incident ac signal. The experimental set-up described in section 5.5.1 allows direct measurement of the rectified current and the multiplier

analysis program calculates this as **IDCOS(1)** which is the dc component of the Fourier coefficients of the device current. This allows a comparison to be made between the two.

Figure 5.18 shows the measured and calculated rectified currents as functions of bias voltage for a 1.0 GHz pump signal at six power levels ranging from -0.22 to 10.53 dBm. For high bias voltages, the calculated currents diverge markedly from the experimental values. This probably occurs because of inaccuracy in the extrapolated device parameter values beyond the measured range.

The sequence of events illustrated by figure 5.18a-f deserves comment. Considering the unpumped I-V characteristic for the 523B shown in figures 4.1 and 5.13a and b, figure 5.18a indicates that the presence of the pump signal at -0.22 dBm results in severe attenuation of the NDC regions and pulls the peak voltages closer to zero. At 1.30 dBm (figure 5.18b) the NDC virtually disappears leaving points of inflection, joined by an approximately linear region, and these move even closer to the origin. This trend persists as the pump power level increases (figure 5.18c) until at power levels in the neighbourhood of about 5 dBm (figure 5.18d) the points of inflection appear to merge into one-another with the region between about ±0.2V showing a weak single inflection occurring approximately at the origin. This inflection region widens with increasing pump levels, resulting in the rectified current characteristic being clearly divided into three, approximately linear, sections with the middle region showing the smallest slope.

These effects can be explained by considering the device voltage and time-averaged current over a complete pump cycle at different bias voltages. At low pump power, the amplitude, V_{rf0}, of the device voltage is small and the current is thus averaged over a correspondingly small range of the dc characteristic. As the bias point shifts, the rectified

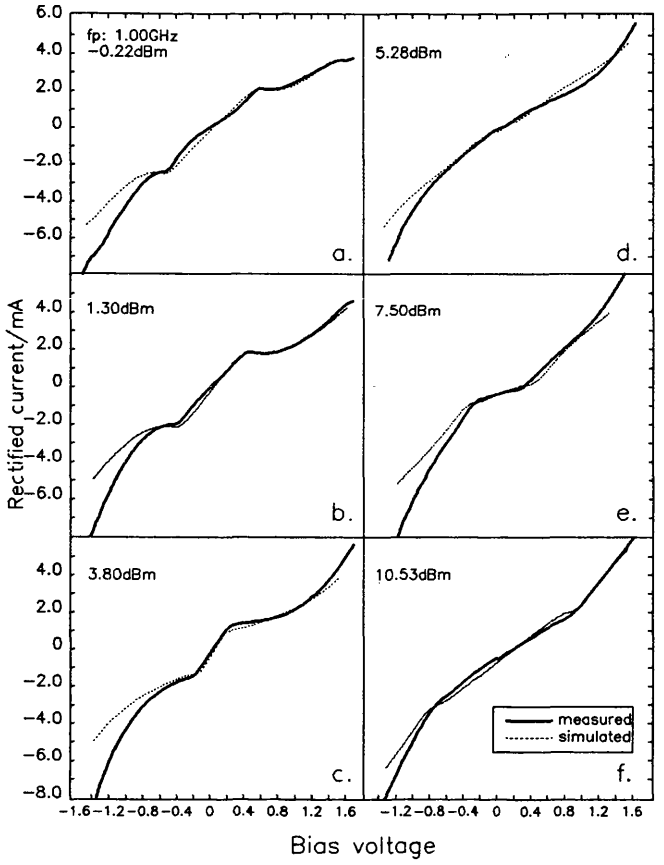

Figure 5.18. Measured (thick solid line) and simulated rectified current as a function of bias voltage for (a) -0.22, (b) 1.30, (c) 3.80, (d) 5.28, (e) 7.50 and (f) 10.53 dBm pump power levels at 1.0 GHz.

current becomes a moving average which is a function of both the bias voltage, V_0, and V_{rf0}. As V_0 moves through the NDC regions, these are averaged over, resulting in the observed weakening and shifting of the nonlinearity within about $V_0 \pm |V_{rf0}|$ of the dc characteristic. These simple arguments lead one to expect that by increasing V_{rf0} to a value where both NDC regions are sampled during the pump cycle at V_0=0, should result in an absolute negative conductance [45] region centred about this point, providing that $V_{rf0} < |V_v|$, where V_v is the valley voltage.

This effect has been observed by Sollner et al.[45] and explained qualitatively using similar arguments, assuming a square wave pump signal for simplicity. However, Sollner et al.'s device had a nearly perfect antisymmetric dc characteristic with peak and valley voltages of about ±0.23 and ±0.4V respectively. The device was therefore in the NDC region for almost half of the pump cycle and as a result the magnitude of the maximum NDC could be adjusted by varying the pump amplitude. The 523B, with a less than ideally antisymmetric dc characteristic, has peak voltages of about ±1V with the NDC regions occupying only about a quarter of the region between $\pm V_v$. The combination of these factors causes the smearing out of the differential negative conductance around zero bias (figure 5.18d). Calculation shows that at a pump power which gives a voltage swing of about $\pm V_v$ at zero bias, there is only a weak and relatively restricted region of absolute NDC between about -0.05 and 0.15V. As can be seen from figure 5.19, which shows the result of this calculation, the negative differential conductance reaches a maximum magnitude of about 1 mS. This is about an order of magnitude smaller than obtained for the unpumped device (see figure 4.5). The curves of figure 5.19 also exemplify the divergence from perfect antisymmetry of the dc characteristic; the rectified current at V_0=0 is about -0.2mA when it should be 0 for perfect antisymmetry. The latter effect occurs because the average conductance in reverse bias is higher than in forward bias. The difference in the magnitudes of the positive and negative rf voltage amplitudes was less than 0.1V and therefore does not account (at least fully) for the skewing of the conductance curve of figure 5.19 towards positive voltages. Now, the peak voltage for the unpumped device in forward bias, V_{p+}, is 1.02V while V_{p-} is -0.94V in reverse bias. The difference in magnitudes is 0.8V which agrees well with the shift in the minimum NDC point. Hence, the bias point will have to move to relatively higher positive voltages in order to average out the NDC.

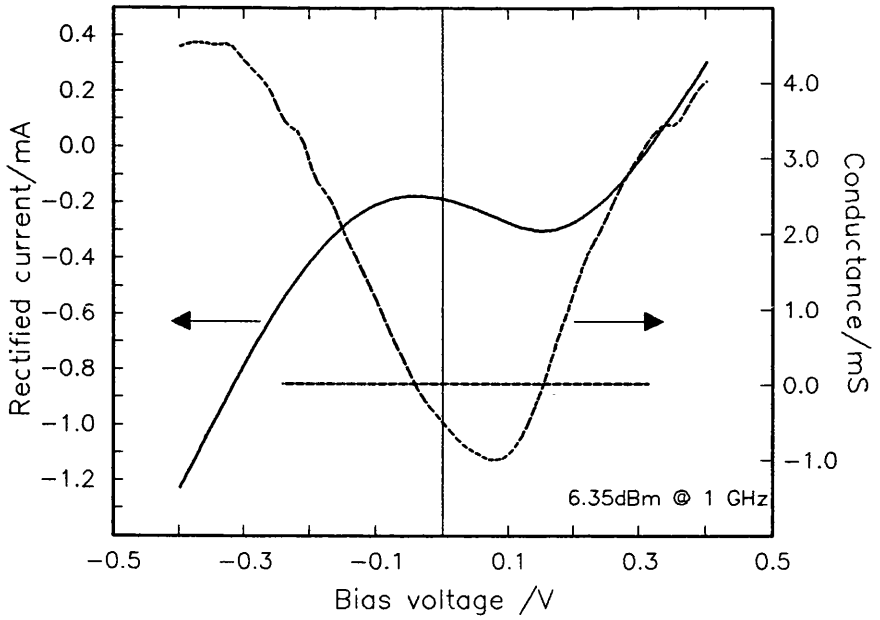

Figure 5.19. Rectified current and conductance calculated for a 1.0 GHz pump signal at 6.35 dBm.

For pump amplitudes higher than V_v, the occurrence of the lower slope central region in the characteristic can be understood as follows. As the bias starts increasing from zero, the portion of the I-V characteristic averaged over at first comprises both NDC regions, thus the net average conductance is reduced. As the bias shifts to higher, say positive, voltages, a stage will be reached where the negative-going voltage swing reaches a point just before V_{p-} and thus, the time averaged conductance over one pump cycle now increases since only the forward bias NDC region is encountered during the cycle. Similarly, for negative bias voltages the conductance increases as soon as the forward bias NDC region becomes inaccessible to the positive-going half-cycle. Thus the rectified current-voltage characteristic takes on the appearance of figure 5.18e.

As the pump amplitude increases, the bias voltage at which either NDC region is no longer sampled during the pump cycle also increases, hence accounting for the widening of the central region evident in figure 5.18f.

5.5.3 Experimental results at higher frequencies

5.5.3.1 Pump frequencies between 2 and 6 GHz

The output powers at harmonics up to 18 GHz were measured for pump frequencies between 2 and 6 GHz. These showed the same general behaviour with increasing bias voltage at low pump levels as did the results for 1 GHz discussed in the preceding sections and as such do not require further comment. However, it was observed that for a pump power level of 0.61 dBm at 2.0 GHz there was gain at the fundamental frequency, as can be seen from figure 5.20 which represents the magnitude of the reflected power under these conditions. The gain is only marginal and occurs between about 1.3 and 1.4V. This would have been considerably higher for smaller pump amplitudes as was the case for the small-signal reflection coefficients of chapter 4. As a consequence the n^{th} harmonic conversion efficiency for the 2 GHz, 0.61 dBm case was taken as the ratio of the output power at the n^{th} harmonic to the incident power into a matched load.

At higher pump power levels (figure 5.21), gain is no longer exhibited as the signal conductance at the fundamental frequency turns positive.

In summary, table 5.2 gives the maximum observed efficiencies for pump frequencies between 2 and 6 GHz at different power levels along with the bias voltages at which these were observed.

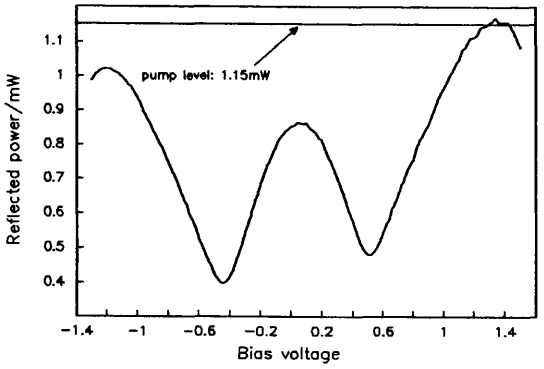

Figure 5.20. Reflected power at 2 GHz for pump level of 0.61 dBm.

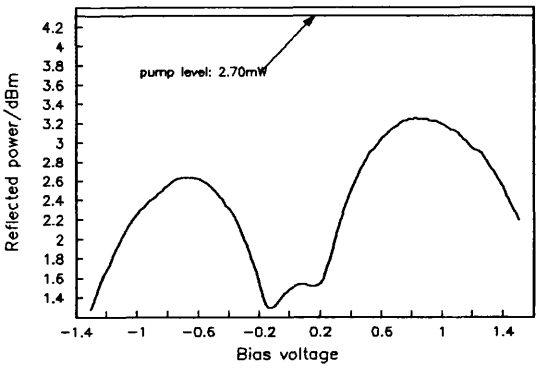

Figure 5.21. Reflected power at 2 GHz for pump level of 4.31 dBm.

Table 5.2: Maximum conversion efficiencies for pump frequencies between 2 and 6 GHz

fp (GHz)	PPL (dBm)	Maximum Conversion efficiency (%) at 2fp	3fp	4fp	5fp	6fp	7fp	8fp
2	0.61	2.86	1.16	0.578	0.102	0.075	0.066	0.031
	Bias voltage >	1.50	−1.14	−0.90	−1.08	−0.92	−0.82	−0.86
	4.31	2.75	1.96	1.65	0.224	0.155	0.207	0.110
	Bias voltage >	1.50	1.34	0.96	0.74	1.00	0.78	1.00
	10.26	2.16	0.326	0.129	0.042	0.081	0.185	0.057
	Bias voltage >	−1.30	−1.36	−0.80	−0.48	0.34	0.04	0.24
3	8.73	3.15	0.055	0.130	0.029	0.234	–	–
	Bias voltage >	−1.04	1.34	0.94	0.58	0.30	–	–
	14.64	5.49	0.103	0.083	0.025	0.037	–	–
	Bias voltage >	−0.78	0.24	0.62	0.12	0.58	–	–
4	9.12	1.65	0.351	0.092	–	–	–	–
	Bias voltage >	−1.40	1.34	0.32	–	–	–	–
	14.5	3.44	0.461	0.080	–	–	–	–
	Bias voltage >	−1.22	1.02	0.58	–	–	–	–
6	3	1.83	0.694	–	–	–	–	–
	Bias voltage >	−1.32	1.26	–	–	–	–	–
	8.37	1.28	0.548	–	–	–	–	–
	Bias voltage >	−1.40	0.02	–	–	–	–	–

N.B. The efficiencies at 2 GHz, 0.61 dBm were defined as the ratio $P_{out}(n)/P_{avail}$, all others were obtained using **(5.37)**.

5.5.4 Sweeping the pump power at zero bias

The experiments described in the preceding sections indicate that conversion efficiency depends on pump power as well, apart from other parameters such as bias voltage, matching conditions at the input and output ports and device properties. Since the data presented so far was generated by scanning the bias voltage at a few constant power levels the effect of input power on harmonic output cannot be assessed properly. Ideally, the effects of incident signal frequency, power and device bias voltage should be investigated by varying one parameter at a time while maintaining the remaining two constant. However each of these parameters is virtually infinitely variable and consequently such a task would not be practical and the information gained of no special value since the general behaviour can be predicted from a few experiments similar to those described in the preceding sections and/or by computer simulation. However, since one proposed application of a RTD multiplier requires the device to be unbiased [25] for the predominant generation of odd harmonics, it is worthwhile to investigate how the harmonic output power changes with increasing pump amplitude for this case.

Figure 5.22 shows the output power up to eighth harmonic for the RTD 523A, which is a $50\times50\mu m^2$ device taken from the same wafer as the 523B. For pump levels below about 11 dBm the even harmonic outputs are about 20 dB below their respective next-higher odd harmonics. For the even harmonics, there is a sharp increase of about 35 dB at pump levels beyond about 11.3 dBm. Similar behaviour has been observed at much higher frequencies [46] The odd harmonic outputs exhibit sharp minima (indicated by arrows in figure 5.22) coinciding approximately with the even harmonic maxima.

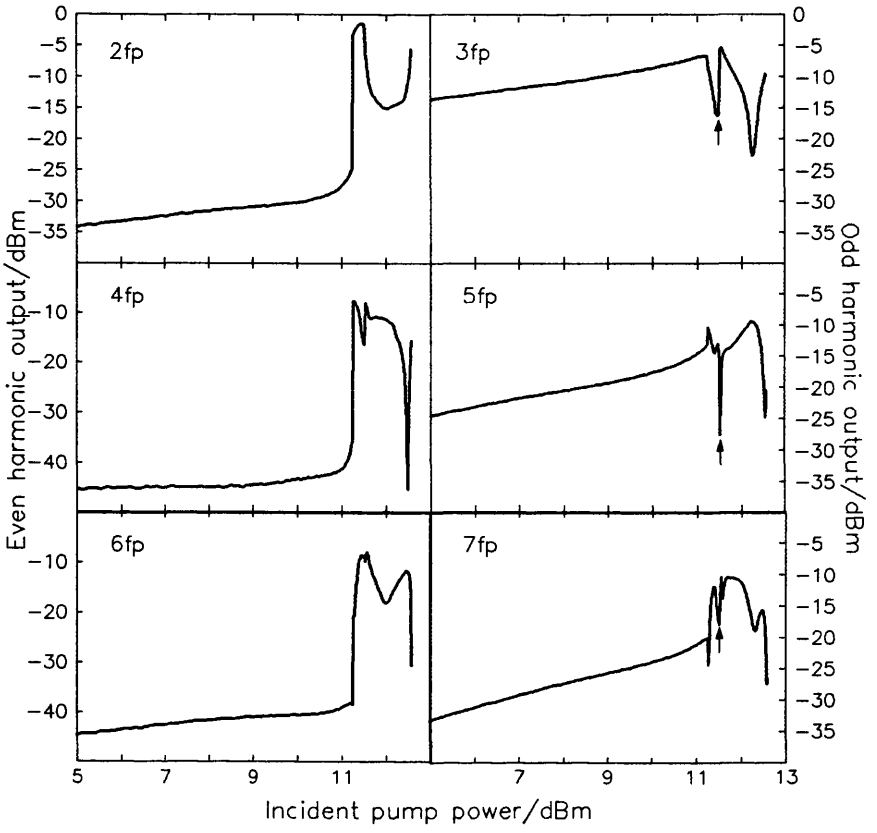

Figure 5.22. Even and odd harmonic output as a function of pump power for the unbiased 523A.

It is not self-evident why there should be such a sharp increase in even harmonic output within a limited pump power range above a certain level since the device was unbiased. This power range corresponds to pump amplitudes reaching to within the NDC region as it is here that the device conductance changes most rapidly. Sollner et al. [45] have predicted such behaviour by a simple analysis as due to persistence of negative conductance at frequencies higher than the pump signal; particularly, at the second harmonic, where, according to their analysis, the magnitude of the NDC is predicted to increase. Admittedly, this analysis [45] neglects the effects of higher harmonics which can only be treated in a self-consistent manner by the methods described in section 5.4.

Figure 5.23 shows the results of a power sweep at 1 GHz for the 523B as well as computer simulations using the multiplier program. The agreement between measurement and simulation is quite good, except at high power levels, where the pump amplitude treads into the extrapolated regions of the device differential conductance and capacitance. The sharp increase in the 2nd harmonic output does not occur, but the output increases by about 5 dB over the output at 0 dBm pump power. In contrast, the increase in the 4th harmonic is about 35 dB and that in the 5th is about 25 dB.

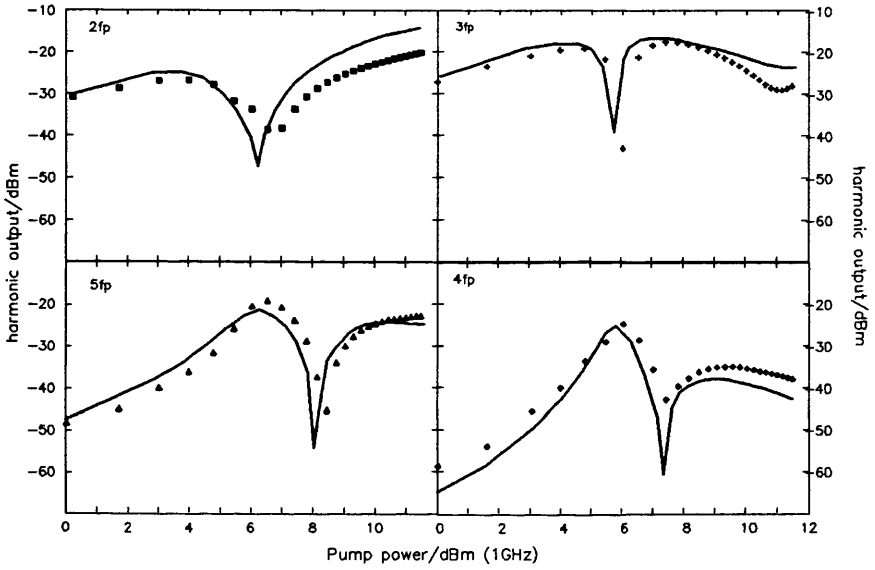

Figure 5.23. Even and odd harmonic output as a function of pump power for the unbiased 523B. The points are measured values while the lines represent the results of calculation using the multiplier program and considering harmonics up to the eighth.

The 2nd harmonic minimum coincides with the first maximum in the 5th harmonic as do the 3rd harmonic minimum and the 4th harmonic maximum. The signal conductance at these harmonics (figure 5.24) goes negative at pump power levels in the neighbourhood of 6 dBm. The 4th harmonic conductance starts going negative at about 2 dBm and reaches a lower minimum than the 2nd, this might explain the relatively

higher conversion efficiency to the former at these power levels. One can also observe that the even harmonic conductance minima occur before the corresponding odd harmonic minima.

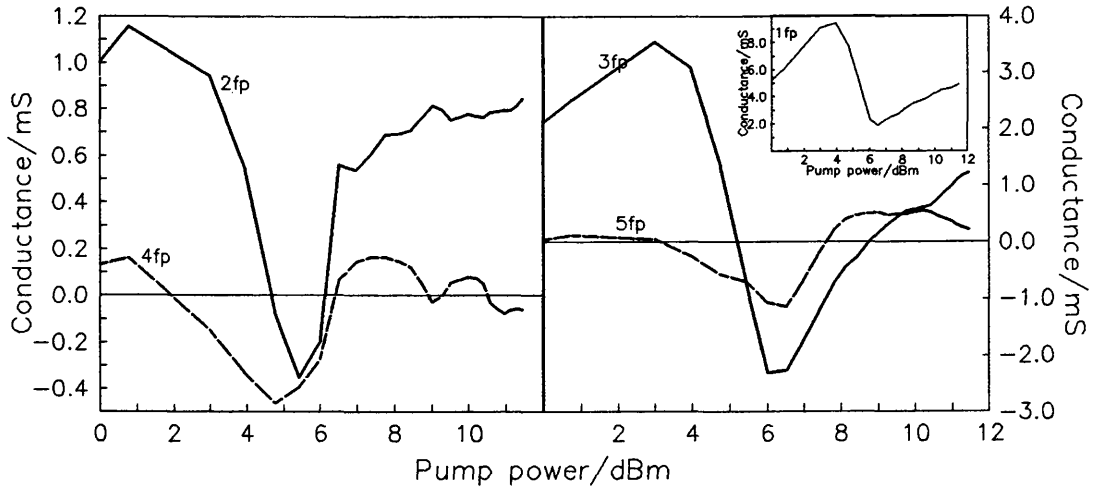

Figure 5.24. Signal conductance at the 2nd, 3rd, 4th and 5th harmonics calculated for the unbiased 523B as a function of pump power.

Finally, shown inset in figure 5.24 is the calculated signal conductance for the pump signal. The minimum corresponds in position with the others, but the interesting point is that the conductance remains positive throughout; thus signal amplification is not possible with the 523B at zero bias. However, the device still has potential as an unbiased multiplier.

5.6 Concluding remarks

A self-consistent method allowing large-signal analysis, the multiple reflection technique [31], has been discussed in detail. The multiplier program due to Siegel et al. [40] has been modified to take advantage of the small-signal characterisation of a RTD (the 523B; chapter 4) in such a

way as to allow actual experimental values of the device current and small-signal differential conductance and capacitance to be used during the analysis.

The same simple device equivalent circuit model of chapter 4 was used here and the program shown to simulate actual device behaviour in a simple multiplier configuration reasonably well. Thus, small-signal characterisation results can be used effectively in predicting the large-signal behaviour by the scheme outlined in the preceding sections.

The experimental set-up used did not allow any form of independent adjustment of the port impedances as it was kept as simple as possible in order to facilitate accurate measurement of embedding impedance at all harmonics of interest and thus be able to supply the necessary data for the computer simulations. However, the program could be used to home in on the optimum embedding impedances by iteration. For example if the required harmonic is the n^{th}, then the bias voltage could be determined approximately by supplying arbitrary embedding impedances as a start. After the first run, the device n^{th} harmonic impedance is noted and the n^{th} harmonic port matched accordingly, while terminating the other ports reactively. This procedure is then repeated until no further increase in the n^{th} harmonic output is achieved. The embedding impedances thus obtained could serve as the design specifications for a potential multiplier.

The experimental results did not reveal conversion gain at any of the test bias voltages and pump power levels used. This was most likely due to two factors; device characteristics and unoptimised embedding impedances. Computer simulations performed using idealised I-V characteristics in order to investigate the factors effecting the conversion properties predicted the following:

1. For low pump power levels harmonic generation favours the second and to a lesser degree the fourth harmonic at bias voltages corresponding to the peak current points on the I-V curve. In this respect, a high peak-to-valley ratio (PVR) increases the low-order even harmonic outputs roughly in proportion to the product of the PVR and the peak current density.

2. For odd harmonic generation, the device should be unbiased and ideally have a perfect antisymmetric I-V characteristic. It should also have low values of V_p, high PVR and peak current density but a NDC region which is wide relative to the pump amplitude so that the extremes of the voltage swings do not cross significantly into PDC regions where the signal conductance could revert to positive values.

Given these conditions and proper optimisation of the port impedances as described above, conversion gain is possible.

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CHAPTER 6

CONCLUDING NOTES

6.1 Introduction

Lack of time, funding and availability of devices suitable for high frequency operation were the main factors confining the experimental work discussed in this thesis to the lower microwave frequencies. However, some significant groundwork has yielded a number of useful results and indicated possible methods which may be employed in further investigation.

This final chapter discusses the main results presented and conclusions reached in the course of work which culminated in this thesis. The discussion on the various aspects of the microwave properties of resonant tunnelling devices and their small- and large-signal behaviour in different configurations indicates some of the areas for future investigation. The last section on techniques for improving the spectral purity and output power of RTD oscillators discusses some of the most recently reported novel ideas.

6.2 Summary and discussion of the main observations and conclusions

6.2.1 Bias circuit oscillations

The analysis of the device/bias-circuit interactions in chapter 2 indicates that experimentally observed behaviour can be well explained and predicted. Although it cannot be ruled out that some of the effects observed may be of

intrinsic origin, as yet there is no concrete evidence to support this view. This and similar works have shown the importance of device and circuit parameters in the analysis of extrinsic bistability. Indeed, it is possible to simulate the effects of extrinsic instability on I-V characteristics to the extent that qualitative agreement is achieved between the measured and calculated shape of the unstable NDC region and the extent of the hysteresis loops, and the dependence of these on circuit parameters, such as the series inductance, for a given device [1]. The lack of quantitative agreement is due to the over-simplified bias circuit assumed.

Consideration of stability criteria based on tunnel diode circuit analysis leads to two basic conditions for stability:

$$R_s G_d < 1 \qquad \textbf{(6.1)}$$

$$\frac{G_d^2 L_s}{C_d} < R_s G_d \qquad \textbf{(6.2)}$$

where R_s is the series resistance (circuit total), G_d the differential conductance magnitude, L_s the circuit inductance and C_d the equivalent circuit capacitance.

The effects of maintaining stability in the bias circuit upon the output power of RTD oscillators have also been investigated. The requirements for high frequency power generation are found to be in conflict with those ensuring dc stability. The former demand a high peak current density and peak-to-valley ratio with a small device capacitance, while dc stability concerns lead to the inverse with the quantity $\Delta V = V_p - V_v$ dominating. In fact, equation **(2.27)** shows a cubic dependence of the low-frequency stable rf power on ΔV. Thus, for stability, the maximum power calculated from stability considerations (equation **(2.27)**) must exceed the operating power output.

Now, in practice, the rf and dc circuits in a practical microwave oscillator are decoupled. This is usually achieved by biasing through a low-pass filter section. However, since the RTD exhibits negative conductance at all frequencies from dc to the oscillation frequency, the design of a bias circuit to suppress undesired oscillations over such a broad frequency range presents a formidable challenge. The solution to the problem may be to introduce lossy sections in the bias line rather than a low-loss reactive filter. This has been achieved for a 10 GHz RTD oscillator [2] by biasing through a parallel-plate transmission line constructed from fibreglass circuit board material. The high dielectric and metallic loss thus introduced lower significantly the Q of all resonances in the bias circuit. A conceptually similar arrangement is possible at millimetre and submillimetre-wave frequencies. In this instance, the RTD is typically contacted by a whisker inside a rectangular waveguide. The bias is supplied through a high-loss coaxial

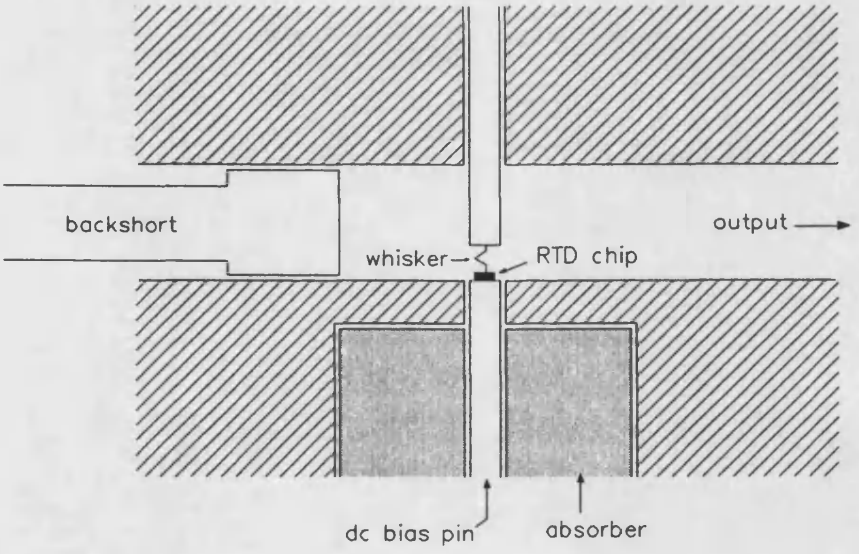

Figure 6.1. Schematic cross-section of a typical high frequency RTD oscillator used at the Lincoln Laboratory at M.I.T., showing the coaxial bias line with an iron-loaded high-loss section. (After Ref. [8])

line section, where the bias pin is effectively the centre conductor surrounded by iron-loaded epoxy [3,4,5,6,7,8], as shown in figure 6.1. The narrow gap between the top of the pin and the surrounding waveguide wall appears as a short circuit at high frequencies such that no rf power is lost down the bias line.

6.2.2 Small- and large-signal equivalent circuits and some useful observations

An understanding of device behaviour in microwave circuits is dependent on an effective model which adequately represents the device physics whilst being simple and amenable enough to allow parameter extraction from microwave measurements. In this respect work at lower frequencies is advantageous as in this regime device physical properties, package and mount parasitics are relatively simple to model by lumped-element equivalent circuits. Furthermore, inaccurate parasitic element estimation will affect experimental results much more at higher frequencies. Another advantage of low frequency characterisation is that test and measurement systems are readily available up to frequencies of about 25 GHz where simple coaxial systems permit versatile and repeatable circuit realisation. Once an adequate understanding of the microwave properties of a device has been achieved and an accurate model derived, high frequency analysis of the model parameters should then follow. Together with feedback from theoretical studies, the analysis could then lead to fine-tuning the device model itself in order to allow high frequency device behaviour to be predicted.

The foregoing has been the motivation behind the work described in chapters 3 and 4. The LEW Techniques E10/A microwave package used for most of the microwave characterisation had not previously been characterised itself. This package offers an inexpensive and effective way of

mounting devices for reflection measurements in a 3.5 mm coaxial system. An accurate equivalent circuit model for the package in the specially-designed 3.5 mm coaxial mount described in chapter 3 has been derived for the frequency range 45 MHz to 13 GHz. This model was used with success in de-embedding the device impedance of a $20\times20\mu m^2$ RTD bonded into an E10/A package mounted in a coaxial system.

Applying the equivalent circuit of a tunnel diode and fitting frequency independent parameters to the experimental data led to excellent agreement between measurement and simulation based on the extracted parameters. In particular, it was shown that the differential conductance obtained from dc characterisation can be used directly in the model. This allowed the determination of device capacitance over a wide range of bias voltages. For the first time it was found possible to fit a single-valued capacitance over the test frequency range of 45 MHz to 13 GHz, dependent only on bias voltage, as also was the case for the differential conductance. The small-signal equivalent circuit model thus constructed allows impedance estimates to within a difference of less than 5% of measurement.

This accuracy is thought to be due primarily to the accurate de-embedding procedures used. However other factors have influenced the results. In contrast to most published reports on microwave characterisation of RTD's employing basically the same technique of reflection measurements with a network analyser[9,10,11,12,13,13,14,15,16], the methods of parameter extraction used in the small-signal study did not make use of commercial CAD curve-fitting software. This type of analysis can result in a number of different equivalent circuit configurations which are all equally capable of generating a simulated frequency-response close to experimental observation. The lumped circuit elements thus extracted are, however, not always identifiable with the device physical properties. This is especially so in

cases where de-embedding is not accurate enough or part of the equivalent circuit representing the embedding network, such as the bonding wire inductance, is not determined beforehand thus leading to extra degrees of freedom for the fit. This type of analysis inevitably leads to attributing properties to the device which essentially pertain to the embedding network.

Another factor effecting the accuracy of small-signal characterisation is the test signal power used in the reflection measurements. An assessment has been made of this effect by repeating the measurements using a -10 dBm signal level instead of the original -20 dBm. This has led to the conclusion that at bias voltages corresponding to regions of relatively high nonlinearity in the I-V and C-V characteristics the equivalent circuit parameters exhibit frequency dependence. This is caused by the frequency-sensitive averaging effect of the pump signal through the varying degree of match between the device and the source. Since the device impedance is a function of frequency and is independent of the source impedance as seen through the embedding network, the degree of matching between the two is also a function of frequency. This means that the voltage amplitude across the device varies with frequency. Since at higher signal levels the voltage spans across an appreciable part of the I-V and C-V characteristics during the pump cycle, the differential conductance and capacitance will not be similar to the small-signal case and will, in turn, become frequency-dependent since they are effectively time-averaged values. The large-signal behaviour of a device can therefore become very complicated as the voltage amplitude across the device is self-consistently determined along with the impedance as stated here. Direct reflection measurements on the device using high test signal levels will therefore not reveal the true large-signal behaviour.

The solution is to allow the device to oscillate and attempt to adjust the output frequency independently of the power. In so doing, the steady-state condition for an oscillator, that is

$$Z_d(\omega)+Z_L(\omega) = 0 \qquad (6.3)$$

allows the device impedance Z_d to be determined from measurements of the load impedance Z_L which the device sees at the oscillation frequency. This method restricts the frequency range and is difficult in practice since tuning the circuit for the required frequency will in general alter the output power. In the case of the large-signal impedance measurements of chapter 4, the coaxial double-stub tuner used could be adjusted to give the desired frequency and power (within the respective allowable ranges) by iteratively sliding the stub assembly and moving either or both stubs. Adjustment of the stubs resulted in significant change in the output power accompanied by a slight frequency shift, and vice-versa for changes in the position of the stub-assembly.

Large-signal impedance measurements thus performed revealed that within a narrow frequency range, the experimental data fitted the tunnel diode equivalent circuit model reasonably well. The fit was obtained with the same value of series resistance and roughly time-averaged values of the capacitance and negative conductance as in the small-signal case at the corresponding bias voltage.

In the course of the large-signal experiments it was observed that when the tuner adjustments were such as to permit the generation of narrow bandwidth, essentially single-frequency oscillations, bias circuit oscillations ceased to exist. This implies that when the RTD locks onto a cavity mode with a sufficiently high loaded Q the restrictions placed on the

bias circuit by stability considerations are relaxed. Hence, it would appear that the design of RTD oscillators has to be based on the realisation of high-Q cavities.

Another possible course of action could be the use of injection locking techniques. Although injection locking of RTD oscillators was not properly investigated in the present work, it was observed that the quality of the output spectrum can be improved markedly when a spectrally pure signal of low intensity is incident on the device. In brief, the packaged RTD is mounted in a coaxial circuit similar to the one used for the large-signal impedance measurements described in chapter 4, but modified as shown in figure 6.2 for this particular case. The device is biased in its NDC region and the tuner adjusted so that nearly single frequency microwave oscillations are observed, at which point the bias circuit oscillations desist. The oscillation frequency is then noted and the tuner stubs retracted to the point where the spectral quality is degraded and bias circuit oscillations reappear. The sweep oscillator is then used to provide an injection signal, typically at about -5 dBm, at a frequency close to (within about ± 20 MHz) the observed oscillation frequency of the RTD. At this point the spectrum consists of the fundamental at the injected signal frequency and its harmonics since the RTD is now acting as a harmonic multiplier. Providing that the circuit is not extensively de-tuned prior to the injection signal, the bias instabilities subside. The most interesting effect observed in this experiment is that when the injection signal is switched off, the RTD oscillation spectrum reverts to nearly its original form before the de-tuning took place. Thus it would seem that the device stays locked onto a cavity mode even in the absence of the injection signal, notwithstanding the degraded Q of the circuit. It was, however, observed that this situation was not indefinitely stable since the spectrum was observed to revert to its de-tuned form

immediately before the application of the injection signal. This occurred quite randomly and might have been caused by voltage transients in the bias line.

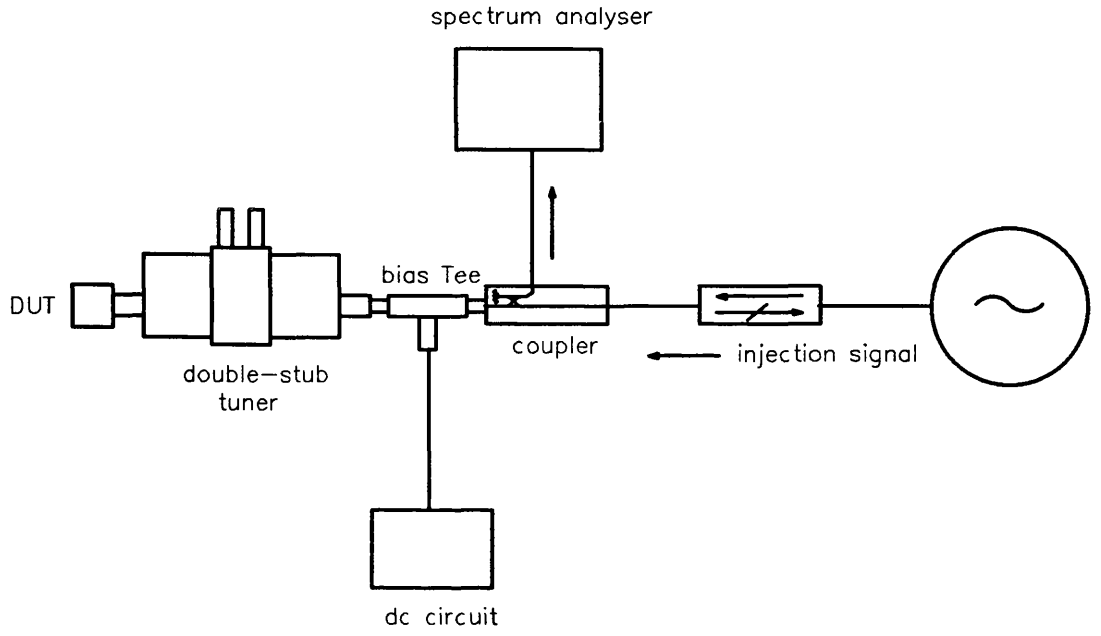

Figure 6.2. Experimental set-up for the observation of the effects of an injection signal on the output spectrum of an RTD oscillator.

Injection locking of RTD oscillators has been almost overlooked in the literature. Due to its promise of improved output characteristics which could lead to practical applications, this aspect is worthy of further investigation.

6.2.3 Large-signal analysis and harmonic multiplication

The preceding section outlines the difficulties encountered in attempting to predict the large-signal microwave characteristic properties of essentially any nonlinear device, but in particular a device, such as the RTD, which exhibits a negative real part of impedance over a broad frequency range. When a rf signal is incident on a device with a nonlinear I-V and/or C-V characteristic the device voltage

and current waveforms have to be calculated in a self-consistent manner, where the interaction of the device and its embedding circuit are duly considered at the pump frequency and its harmonics. The type of harmonic balance technique applied in chapter 5 is a powerful tool which allows such a nonlinear analysis to be performed. It requires the assumption of a device equivalent circuit model and knowledge of the embedding impedance seen by the device in the test circuit at the pump frequency and a number of harmonics.

A nonlinear analysis program [17] that uses the multiple reflection technique [18], a form of the harmonic balance technique, was modified in such a way as to allow direct use of the experimentally-determined I-V (and G-V) and C-V characteristics, assuming the simple tunnel diode model. The circuit elements of this model were assumed frequency-independent and were determined from small-signal reflection measurements as described in chapter 4. A simple microwave circuit which allows measurement of harmonic output powers was used to provide means for direct comparison of calculated and measured harmonic output and conversion efficiency. The resulting agreement was encouraging and showed that the small-signal equivalent circuit model with the measured $G(V)$ and $C(V)$ can be used as the basis for predicting large-signal device behaviour.

The harmonic conversion properties of a RTD were examined as a function of bias voltage and pump power without attempting to optimise the embedding impedance of the experimental circuit. The results indicate that at bias voltages such that the rf voltage amplitude spans over a region of the I-V characteristic which is approximately antisymmetric, the odd harmonics dominate. Conversely, the even harmonics dominate when the rf voltage covers regions of approximate symmetry about the bias point. Hence, the potential exists for the use of RTD's as multipliers of not

just odd but also even harmonic output depending on signal power and bias voltage. To date the accent has been on odd (particularly 5^{th}) harmonic multiplication [19,20,21,22,23], but the possibilities of efficient even (particularly 2^{nd}) harmonic generation with low-level pump signals, when the device is biased at the peak voltage, cannot be overlooked.

Comparative studies using the same DBRTD heterostructure [24] as a quintupler and fundamental oscillator have revealed that the multiplier power drops more slowly than that of the oscillator with increasing output frequency, since multiplication still occurs beyond the oscillation cutoff frequency. Another advantage of a millimetre/submillimetre-wave multiplier is that locking the pump input signal at a relatively low frequency is easier than locking the fundamental oscillator at some five times that frequency. This suggests that the multiplier may be a better source of power in the submillimetre spectrum than a RTD fundamental oscillator.

The nonlinear analysis of chapter 5 allows the calculation of device rectified current and the experimental circuit permits its direct measurement. These were compared for a range of bias voltages at a number of different pump power levels. The experimental results are in good agreement with the simulations and allow qualitative interpretation of the decreasing nonlinearities of the rectified current-voltage characteristic with increasing signal power. In particular, there will be a certain power level which results in an absolute negative differential conductance region centred about zero bias. This mode of operation may prove useful as will now be briefly outlined.

Sollner et al. [25] have predicted that if an unbiased RTD is pumped at a frequency ω_0, say, a low-level signal at a frequency $\omega_s \gg \omega_0$ can be amplified making use of the absolute

negative conductance. Furthermore, the magnitude of the negative conductance can be controlled by the pump amplitude, a very useful circuit property.

The predictions of Sollner et al. [25] were based on a very simple analysis which neglects the effects of pump harmonics higher than the second. A more accurate analysis performed with the modified multiplier program is described in chapter 5, and the results are shown in figure 5.24. This figure shows clearly that even though the conductance at the pump frequency is positive, the harmonics show regions of negative signal conductance within a range of pump power. The device is thus capable of amplifying signals at frequencies much higher than the pump. Now, if a resonant cavity is provided for the pump signal, the cavity Q controls the fraction of the pump signal energy stored per cycle. If Q is such that $Q\omega_0 > \omega_s$, oscillation at ω_s can be maintained in the absence of the original signal. Operation at zero dc bias implies that no dc connection need be made to the sample. Hence, the problem of dc stabilisation disappears since the dc circuit in which undesirable oscillations could occur is eliminated.

Finally, the optimisation of device electrical characteristics for frequency multiplication was investigated using the multiplier analysis. The results indicate that for small pump signals with the device biased at the peak voltage, low-order harmonic generation is enhanced by higher peak-to-valley ratios. For predominant odd-harmonic generation, the device I-V characteristic should be as perfectly antisymmetric as possible and should be unbiased. Conversion efficiency in this case will be improved if the peak voltages in forward and reverse bias are low and the respective NDC regions wide relative to the pump amplitude so that the rf voltage does not cross significantly into the PDC regions

beyond the valley points. In both cases, power output and efficiency are improved by increasing the peak current density and reducing series resistance.

6.3 Some recent novel designs for improving RTD oscillators

As has been mentioned previously, the main drawbacks of RTD oscillators for millimetre- and submillimetre-wave generation are the great difficulty of low-frequency stabilisation and the minute power outputs obtained so far. Some novel techniques have recently been proposed to tackle these problems. These will be discussed briefly here as they are all worthy of further investigation.

Stephan, et al. [2] incorporated a RTD in a planar X-band oscillator coupled to an open resonator. Figure 6.3 shows schematically the arrangement used.

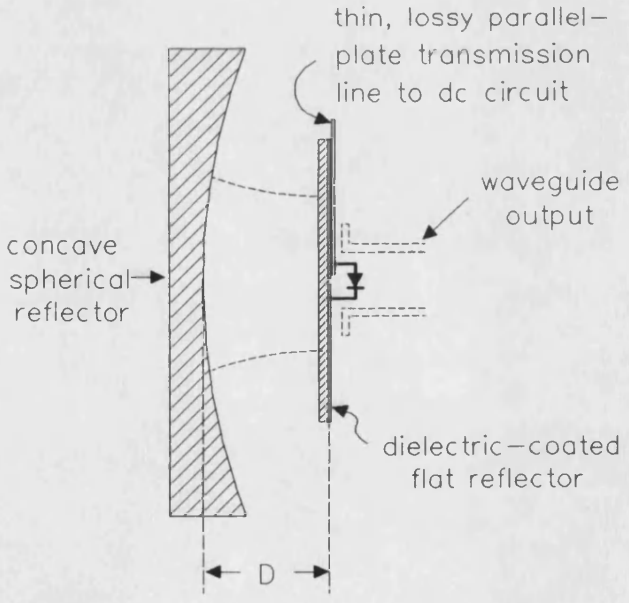

Figure 6.3. Schematic representation of the quasi-optical RTD oscillator of Ref. [2].

The open resonant cavity is defined between a concave spherical metal reflector and a flat dielectric coated thin copper sheet containing a narrow slot (0.13×6.3mm). The separation D between the reflectors (15 - 20 mm) and the small size of the slot allow only the lowest-order TEM_{000} mode of the open resonator to be excited [26] by the RTD which was mounted behind the slot as shown schematically in figure 6.3. The device was biased through a lossy parallel-plate transmission line in an attempt to suppress spurious oscillations in the bias circuit. The output was monitored by means of an X-band waveguide flange placed close to the diode side of the slot. In the absence of the concave reflector, the RTD and its package parasitics along with the slot inductance form a low-Q resonant circuit allowing broad spectrum X-band oscillations. It was observed [2] that as D is slowly varied so that the resonant frequency of the TEM_{000} mode sweeps past the free-running oscillator frequency, the oscillator locks onto the cavity mode. The spectrum is improved to the extent that the carrier-to-single-sideband noise decreases by about 36 dB, while the oscillation frequency was tuneable over 2.5% by adjusting D. This demonstrates that the much higher unloaded quality factor (Q_o) obtainable from open cavity resonators can be exploited for improving the spectral purity of RTD oscillators. The possibility of large circuit Q's could also relax the restrictions placed on oscillator design by bias circuit stability considerations in the same way as has been observed in the present study (section 6.2.2).

At millimetre- and submillimetre-wave frequencies, these quasi-optical techniques could prove even more advantageous. Conventional resonators such as those based on closed cavities or radial transmission lines exhibit a decrease in Q_o with increasing frequency because of increased ohmic loss from the metallic surfaces. Open resonators can provide a much higher Q_o which thus extends their use to much higher frequencies. In fact, Brown et al. [8] have recently reported

the application of the open resonator in the construction of a millimetre-wave RTD oscillator. They estimate a Q_o of about 1.2×10^4 at 103 GHz for their resonator which leads to a linewidth of approximately 10 kHz at 10 dB below the peak, an improvement by a factor of 100 over the same oscillator with a backshort replacing the quasi-optical arrangement.

Despite these and many previous efforts, however, the output powers from RTD oscillators are still too low for most practical applications. Brown et al.'s [8] quasi-optically stabilised oscillator has an output of only -19 dBm and at higher frequencies other efforts have reported much lower outputs [7]. Thus, it seems that with the device characteristics currently available the implementation of the RTD oscillator in microwave, millimetre- and submillimetre-wave systems is still not advantageous. However, it is expected that eventually its primary application could be as a low-noise local oscillator for high-sensitivity radiometers operating in the submillimetre-wave region [8].

In view of the foregoing, several power-combining schemes have recently been proposed. The classical approach to power combining involves placing a number of sources in a waveguide cavity with separate circuits for each source [27]. At high frequencies, however, this approach becomes impractical and expensive as the components become lossy and difficult to construct. Mink [28] suggested placing devices in a two-dimensional array in a Fabri-Pérot cavity in a configuration not unlike that of a laser. Rutlegde, et al. [29] have recently applied this method successfully with planar arrays of 4×4 Gunn diodes and 10×10 MESFET's to obtain effective radiated powers of 22 and 25 W respectively at X-band. As proposed by Stephan [2], this configuration can be applied to RTD's. One such configuration is shown schematically in figure 6.4.

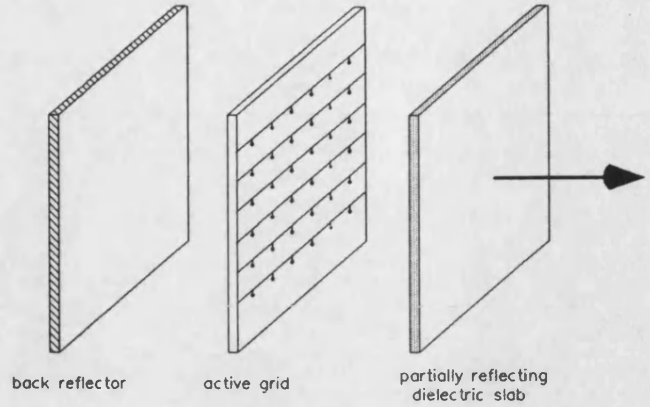

Figure 6.4. Schematic representation of a planar monolithic RTD array synchronised by a Fabri-Pérot cavity.

The devices could be formed in a monolithic grid pattern on a single GaAs substrate with the bias provided through lossy transmission lines defined on the surface by photolithography. Patch [29] or slot [2] antennas could prove useful techniques in coupling the output from each device to the cavity.

A grid of this type could easily contain hundreds of RTD's thus constituting a planar sheet with a reflection coefficient in excess of unity. The resonator provides feedback that couples the devices together and permits the active sheet to be used as an oscillator. The output from the partially-reflecting dielectric slab could be used directly or coupled into a rectangular waveguide by means of a feedhorn.

Another method of integrating several RTD's to enhance power output has recently been suggested by Yang and Pan [30]. In contrast to the planar integration schemes mentioned previously, Yang and Pan envisage the series integration of several RTD's resulting from growing several double barrier structures on the same substrate. These are separated by thin drift regions sufficient to destroy electron phase coherence between successive RTD's. Now, oscillation cannot be triggered in a circuit consisting of series connected

NDR devices unless the dc supply is switched on fast enough [31]. However, when the turn-on process is so fast that capacitive current components dominate, the initial distribution of the total voltage can be equally partitioned among the individual NDR elements and adjusted to reach into the NDR regions of the individual I-V characteristics, providing these are sufficiently similar [31]. Thus, rf oscillation can be initiated and sustained given a proper embedding circuit.

It is estimated that for a series-integrated RTD structure designed to operate in the millimetre-wave region, a turn-on time of the order of 1 ps is required [30]. It may be possible to provide these necessary switching conditions by applying the nonlinear transmission line technique [32] which has resulted in 6V-amplitude voltage shock waves with 1.6 ps fall times.

The maximum output power from vertically integrated devices has been shown to be proportional to the square of the number of integrated devices [33]. Yang and Pan estimate that about 0.1 W output at 100 GHz should be possible from 10 series-integrated RTD's, after allowing for 20% spread in peak currents and the degradation due to transit time effects. This is indeed a promising estimate.

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APPENDIX I

DESIGN AND CONSTRUCTION OF THE DC CHARACTERISATION STATION

A dc characterisation system was required from an early stage. Such a system was intended primarily for accurate determination of I-V characteristics of devices in the unmounted state.

Wafer-probing facilities were thus seen to be advantageous as such techniques would identify devices with promising characteristics at an early stage before subsequent packaging and bonding, a laborious and time-consuming process. A whisker probing station was therefore designed and constructed. The system was also designed to allow I-V measurements on cooled samples. An attempt to resolve the problem of frost formation on the chip surface at low temperatures involved the design of a special cold stage as described in section I.1. Subsequent sections describe the characterisation station design as well as the protection electronics and the thermocouple pre-amplifier.

At the start of this project there was available a computer programme designed by Mason and Azari [1] which controlled a programmable voltage source in conjunction with an electrometer for device characterisation. This programme was modified extensively and implemented with the system.

I.1 Device cooling assembly

I.2 The cold stage

Figure I.1 shows the cold stage which consists of a copper cold arm fitted to a flange at the top. At the head of the

arm a circular recess accommodates the sample mount (figure I.2). Not shown in figure I.2a is an inlet tube for liquid nitrogen.

The middle cover is a circular tufnol ring which bolts to the flange. This houses the probe port, nitrogen inlet and outlet purging tubes and the thermocouple port, apart from delineating the sample chamber. The thermocouple leads pass through a rubber sleeve press-fitted into a brass sleeve which screws into the middle cover; thus ensuring a hermetic seal. The leads then protrude into the sample chamber. They are then bent downward at right angles and the junction fitted into a small hole drilled half way into the circular copper sample mount. A smear of high thermal conductivity paste in the junction hole improves thermal contact.

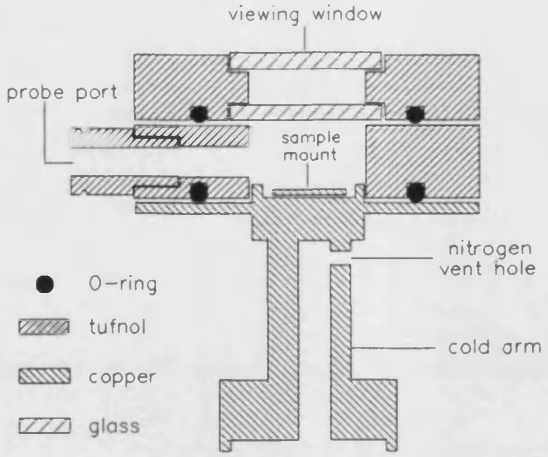
The top cover bolts to the middle cover and is essentially a viewing window. It consists of two glass plates separated by an evacuated space to minimise heat transfer from the outer to the inner plate and thus limit frosting on the surface of the former.

The whole assembly is then placed into a large polystyrene cup with recesses cut out in the side to accommodate the various protrusions described above (figure I.3). This, in turn, is then fitted into a small dewar which serves the double purpose of giving the whole assembly mechanical stability and surrounding the cold stage with a liquid nitrogen jacket to further minimise heat exchange.

I.3 The probe assembly

Figure I.4 shows the probe design. This consists of a support shaft which fits into a micro-manipulator arm. The flange at the end of the shaft mates with the flat end of the sleeve which is threaded to take the probe-end of the support shaft.

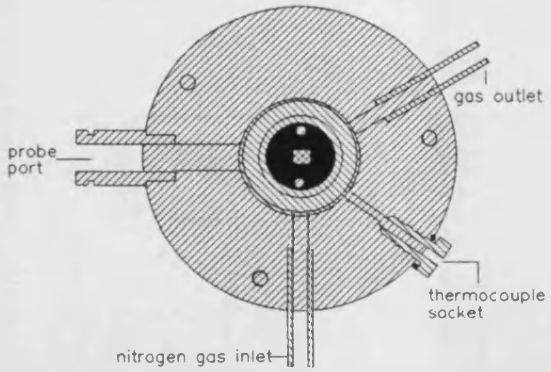
The probe itself consists of a 1.6mm diameter phosphor-bronze arm, 85mm long, fitted tightly into an axial hole in the support shaft. The other end is threaded to take the probe head (figure I.4).



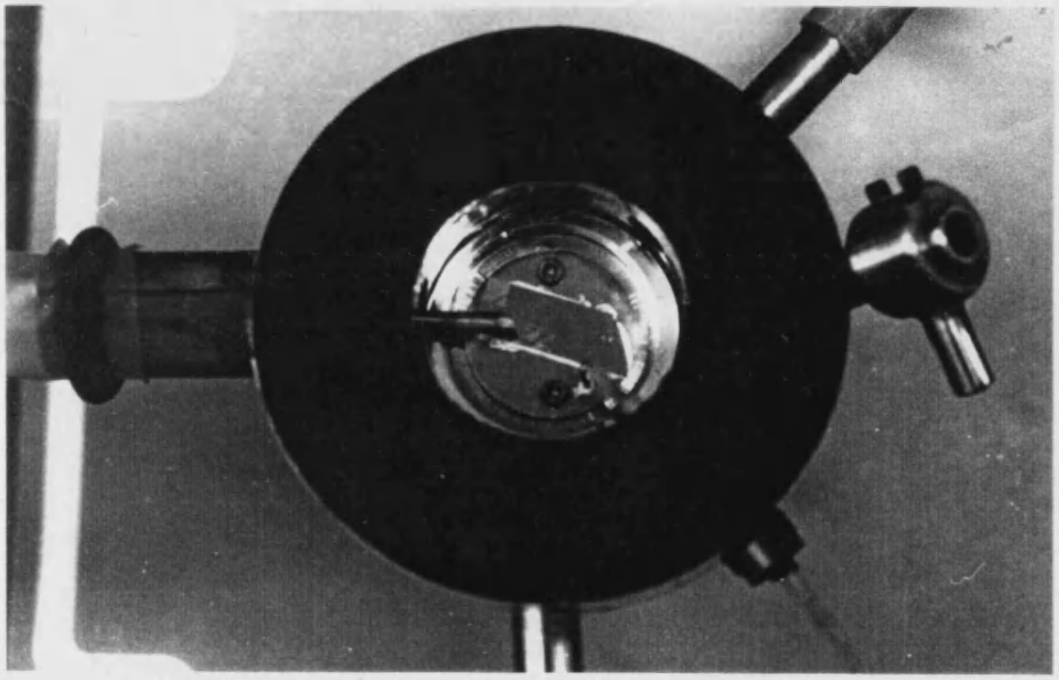
(a)

(b)

Figure I.1. The cold stage, consisting of a copper arm with flange at the top. (a) Schematic cross-section including the top and middle covers, (b) the actual cold stage; notice the slanting liquid nitrogen inlet tube not shown in (a).



(a)



(b)

Figure I.2. (a) Schematic top-view representation of the middle cover showing the probe port, nitrogen inlet and outlet purging tubes, and the thermocouple port. (b) actual top view of middle cover.

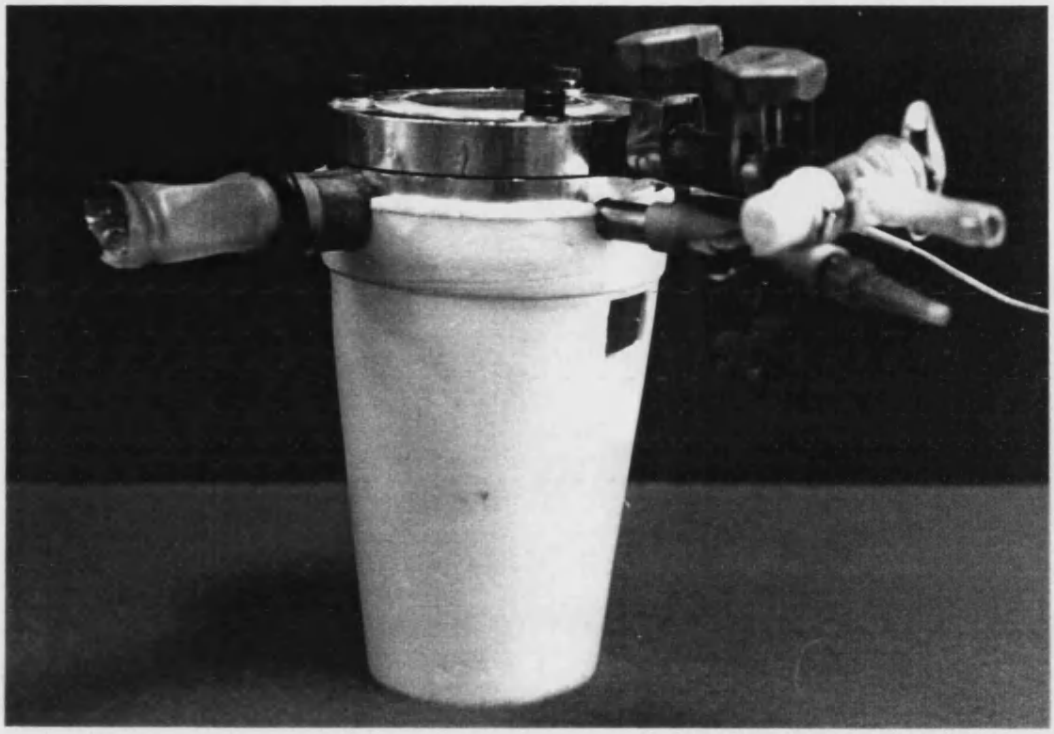


Figure I.3. The cold stage, fitted with the middle and top covers is shown here fitted into the polystyrene cup. This whole assembly fits into a small dewar which acts as a radiation shield and provides a liquid nitrogen jacket.

During use the probe assembly is clamped into the micro-manipulator arm. The probe is then levelled with and inserted into the probe port in the middle cover (figure I.5). A thin sheet-rubber shroud is then fitted over the probe sleeve at one end and the probe port at the other. Rubber O-rings are then slipped over both ends in the appropriate grooves to hold the shroud in place and ensure a hermetic seal. This allows limited three-dimensional freedom of movement of the probe whilst preventing the entry of moisture inside the sample chamber (figure I.5). A microscope positioned over the window then allows the individual devices on the sample chip to be identified and probed.

With the sample fixed as shown in figure I.2b and the structure assembled as in figure I.5, the sample chamber is purged with dry nitrogen gas for about 30 minutes before liquid nitrogen is slowly transferred into the polystyrene cup through the appropriate filling tube. Purging is maintained until a stable low temperature is reached, after which the outlet and inlet tubes are shut off in this order. Transfer of liquid nitrogen is continued until it overfills the polystyrene cup and fills most of the dewar beneath.

In actual practice, although tufnol is a very good insulator, the outer window plate cools sufficiently to allow frosting within about 45 minutes after the liquid nitrogen is transferred. It was, however, found possible to eliminate this temporarily by directing a stream of dry air at room temperature at the window.

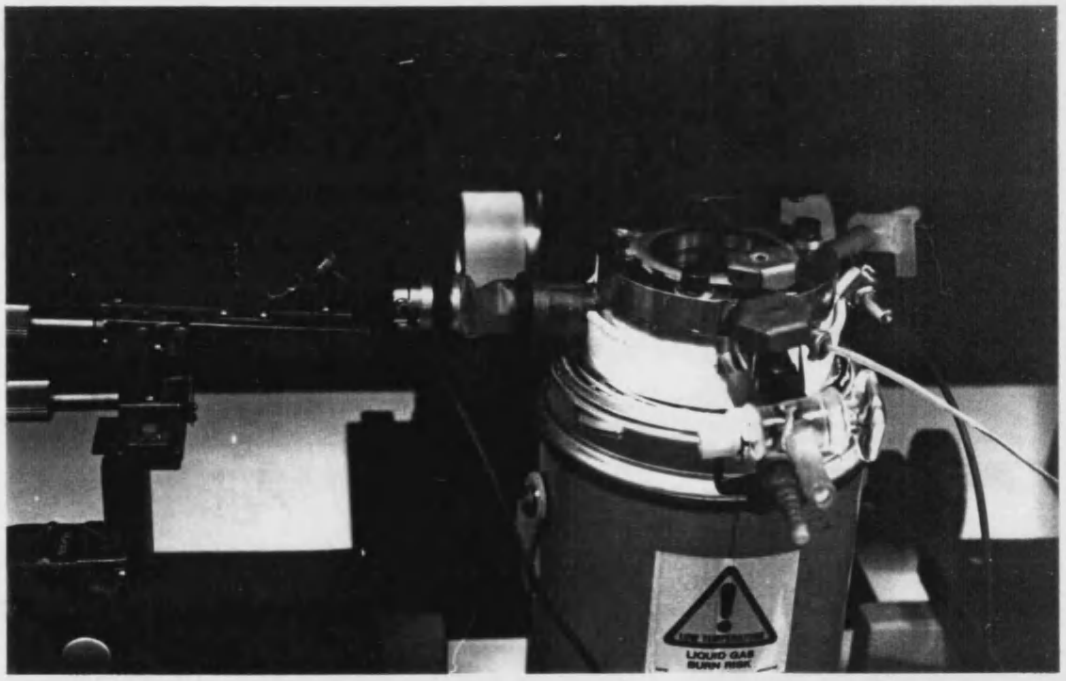
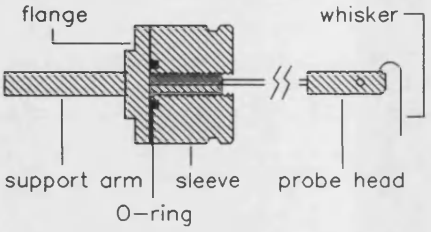
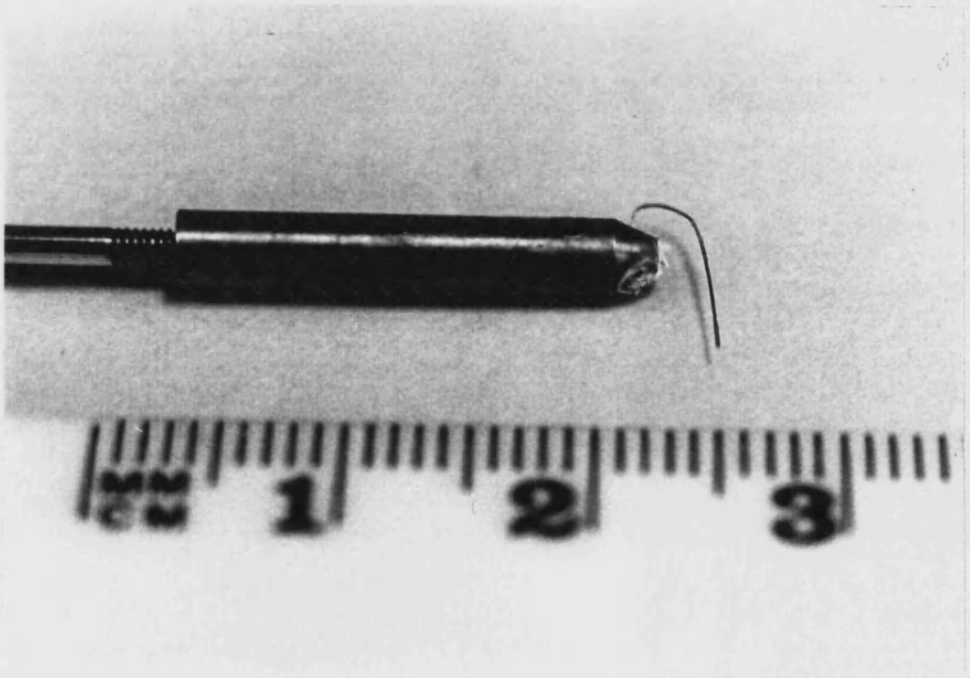


Figure I.5. The photograph shows the probe arm supported in the micro-manipulator. Notice the rubber sleeve secured by two O-rings at the port and the arm.



(a)



(b)

Figure I.4. (a) The probe design. (b) One of the actual probe heads used; the phosphor-bronze whisker shown here has a diameter of 125μm and is etched to a point in a sodium hydroxide solution.

I.4 The dc characterisation station

A schematic of the characterisation station is shown in figure I.6. A rigid blockboard base about 95 by 60 by 2.5 cm with a Formica surface serves as the base of the assembly. The platform tops have steel plates secured to their surface

to enable magnetic coupling of the micro-manipulator sub-assembly and are raised on spacers such that the probe-port level becomes accessible when the cold stage is mounted on the dewar. The two platforms thus offer the choice of left or right handed manipulation of the probe. The clamp and retaining bracket secure the dewar rigidly in place in between the platforms. The problem of viewing different sections of the chip was resolved by mounting the microscope on a rigid x-y platform bolted down to the base in the position shown. The microscope used was a Bausch & Lomb with binocular vision and ×15 magnification eye pieces.

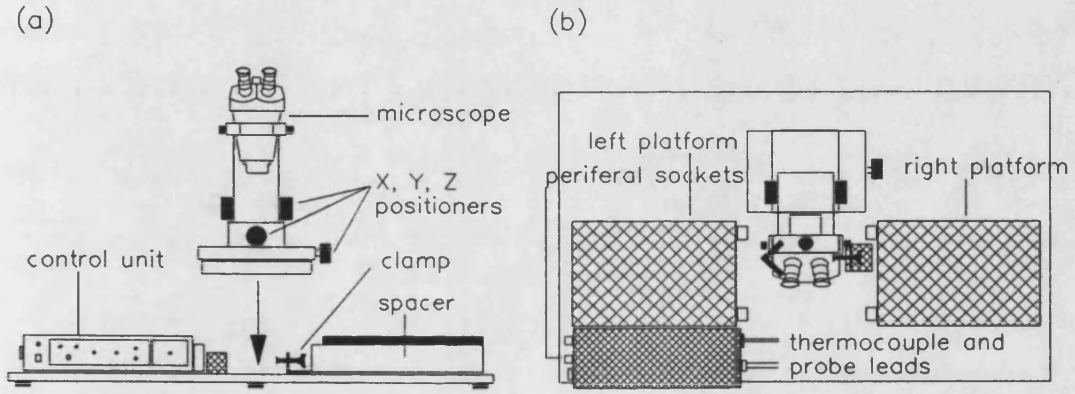


Figure I.6. Front (a) and top (b) view of the characterisation station. The microscope is mounted on an x-y platform to enable viewing of individual devices at different positions on the sample chip. The micro-manipulator and cold stage assembly are not shown.

I.4.1 The shunt control unit

When the voltage across the device under test (DUT) is changed voltage transients may occur. More seriously, when the voltage calibrator is switched off, a ±15*V* spike was observed across the DUT. This is enough to destroy most devices.

A protection circuit was designed which would remedy this situation by having the DUT short-circuited at all times except during the time required for the current to be recorded. Figure I.7 shows the resulting circuit. The mode select arrangement is effectively a latch which provides the option of having the DUT permanently connected in the measurement circuit (as would be required in the investigation of hysteresis) or alternately connected and short-circuited as required by the measurement software. LED indicators show the selected mode and actual circuit status of the DUT. The actual switching is carried out by the single pole changeover relay, the default state of which was such that the leads of the DUT were shunted. To protect against switching transients, the arrangement based on the 74107 JK flip-flop was devised. The master enable input was connected to the voltage calibrator mode-selector switch[1] such that a transition from remote to local control would produce a high-to-low transition at this input. This transition changes the state of the flip-flop output $\overline{Q}$ and will subsequently cause the base of the ZTX 653 transistor to be pulled low. This will stop the latter conducting and hence the actual state at the moment of switching is overridden by the default (i.e., the DUT is short circuited).

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1 The voltage calibrator used was a Time Electronics 9814. The mode selector switch in this unit is tri-positional and corresponds to "OFF", "LOCAL" and "REMOTE". Switching from LOCAL to OFF was producing the undesirable voltage spike, whilst transition from REMOTE to LOCAL produced no noticeable effect. Thus, to switch off from remote, one must flick through the LOCAL position. Since this operation is manual, the time delay necessary would automatically be provided.

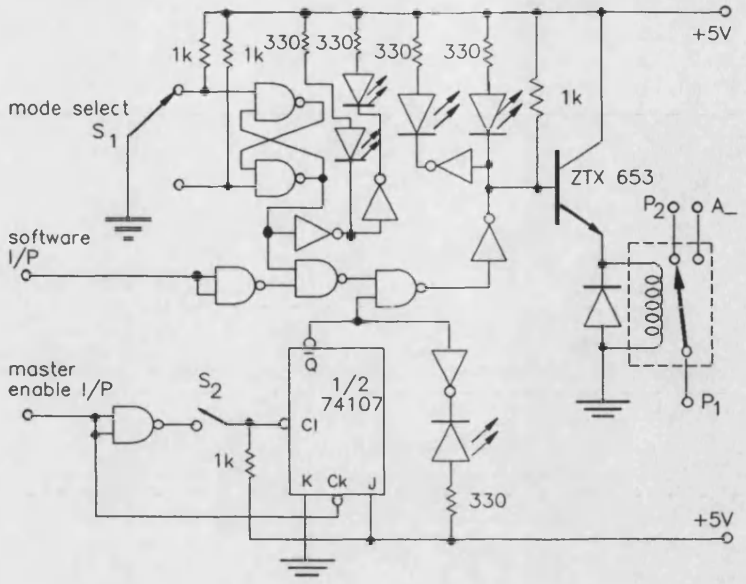


Figure I.7. The shunt control circuit.

I.4.2 The thermocouple pre-amplifier

The thermocouple used was a type-K. This was required to read temperatures between 77K and 300K and was to be interfaced with the pc to enable the characterisation software to act on the digitised data form the thermocouple. A PC-30 A-to-D/D-to-A converter was used to digitise the analogue signal from the pre-amplifier. The maximum input voltage swing for this model is $\pm 5V$. Figure I.8 shows the pre-amplifier circuit. The AD595AQ is a complete instrumentation amplifier and thermocouple cold junction compensator on a monolithic chip [2]. However, the expected output with the junction at 77K is about -1.45V. To utilise the full range of the A-D converter, a second stage was included, based on a non-inverting amplifier configuration using an OP-07A precision op-amp. $\mathbf{R_1}$ is a multi-turn cermet potentiometer which allows fine-tuning the second stage gain such that the output is -5.00V at 77K. An LED connected as shown to pin 12 on the AD595AQ lights up if there is a break in the thermocouple circuit.

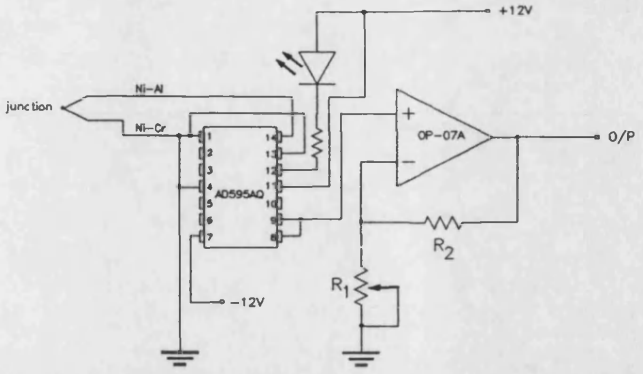


Figure I.8. The thermocouple pre-amplifier circuit.

I.4.2.1 Calibration

The thermocouple output is non-linear with temperature. The AD595AQ literature [2] contains a calibration table of the chip output versus temperature for a type-K thermocouple. Thus, an accurate knowledge of the second stage gain enabled a second calibration table to be calculated from the first by simple scaling. This resulted in a table of temperature versus pre-amplifier output voltage. The tabulated voltages were then converted to A-D converter readings and the subsequent table stored in a file on disk to enable temperature measurement by interpolation during programme execution.

I.4.3 Instrument layout

Figure I.9 is a schematic of the instrument layout. The system includes the Keithley 617 DMM by default, but allows the use of an alternative instrument for current measurement, a Thurlby 1905a DMM was used in this case. The dc characterisation is controlled by the pc via the measurement programme. The voltage bias leads from the voltage calibrator and the lead from the Thurlby 1905a plug into the shunt control unit (which also houses the thermocouple pre-am-

plifier). When the Thurlby 1905a lead is unplugged from the unit, the current circuit is automatically channelled through the Keithley 617, which is permanently wired in the system. Thus the action of plugging in the former automatically selects it as the current-measurement instrument.

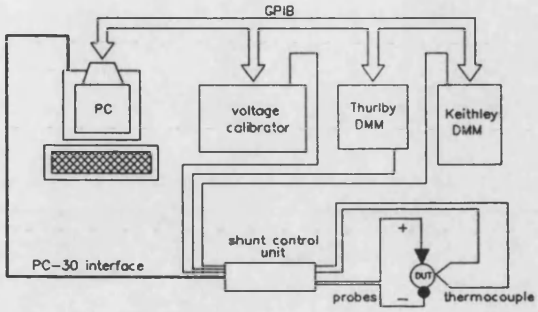


Figure I.9. Schematic representation of the instrument layout for the dc I-V characterisation.

The shunt control unit interfaces with the PC-30 card installed in the pc. When the programmable shunt mode is selected the pc instructs the control unit to connect the DUT during measurement and then to short circuit the probes and disconnect from the bias circuit when the bias voltage is being set. The thermocouple pre-amplifier voltages are read by the PC-30 and the measurement programme converts these to temperatures for subsequent processing.

References

1. H. Mason and J. Azari, unpublished.
2. RS Data Library, March 1988, **No. 6957**, pp. 1-7.

APPENDIX II

BIAS CIRCUIT INSTABILITY SIMULATION PROGRAMME

This appendix contains a listing of the programme mentioned in chapter 2. It traces the time-development of a voltage transient set up in the bias circuit of a resonant tunnelling device at a particular bias voltage and outputs the voltage across the nonlinear conductance, its derivative and the circuit current as a function of time. It is a simple matter to convert this programme to perform this calculation at successive bias steps by obtaining the initial conditions from the time-averaged voltage and current of the previous step. Modelling of the effects of bias circuit instabilities on the I-V characteristic of RTD's is thus possible. The simulated unstable characteristics shown in chapter 2 where computed in this way.

```
      program TST
      double precision l,c,r,vb,xa,ya,yla,y2a,dydx,eps,h,hdid,y,
     + htry,hnext,ci,gi,fy,fz,v,x,x0,curr,rdc
c The main parameters:
c      l: inductance/H
c      c: capacitance/F
c      r: series resistance/Ohm
c      vb: bias volatge/Volt
c      curr: total circuit current/A
c      v: (v(t)) the instantaneous voltage across the conductance/V
c      gi: differential conductance/S
c      ci: current in gi/A
c      rdc: v(t)/ci(t)
      external fy,fz
      dimension y(2),dydx(2)
      dimension xa(1000),ya(1000),yla(1000),y2a(1000)
      character*25 flnm
      common l,c,r,vb/inter/xa,ya,yla,y2a,n
c Fill in data arrays for with stable I-V data for interpolation
      open(1,file='stableiv.dat',status='old')
      read(1,*)n
      read(1,*) (xa(i),ya(i),yla(i),i=1,n)
      close (1)
c Obtain parameter values for calculation
      open(2,file='param.tst',status='old')
      read(2,*)l
      read(2,*)c
      read(2,*)r
      read(2,*)vb
      read(2,*)htry
      read(2,*)np
      read(2,*)eps
      read(2,'(a25)')flnm
      close (2)
c Establish cubic spline second derivative array
```

```
      call spline(y1a(1),y1a(n))
c Calculate initial conditions
      call splint(vb,ci,gi)
      rdc=vb/ci
      x0=0.d0
      y(1)=vb*(rdc/(rdc+r))
      y(2)=0.d0
      dydx(1)=fy(y(2))
      dydx(2)=fz(x0,y(1),dydx(1))
c Convert precision from % to fraction, open output file and print
c input parameters
      eps=eps/100.d0
      open(3,file=flnm,status='unknown')
      write(3,*) l,c,r,vb,a,dvb,vstop,htry,np,eps
 100  h=htry
c Do calculation
      do 12 i=1,np
      call rkqc(y,dydx,x0,htry,eps,hdid,hnext,curr)
      write(3,'(4e17.6)')x0,y(1),y(2),curr
      if (hnext.gt.h) then
      htry=h
      else
      htry=hnext
      endif
 12   continue
      close (3)
      end

      subroutine RKQC(y,dydx,x,htry,eps,hdid,hnext,curr)
c This subroutine together with RK4 forms a 4th-order Runge-Kutta integration
c algorithm with automatic adaptive step size control for improved accuracy.
c It was adapted from the routine published in Ref. [1].
      double precision x,y,dydx,ytemp,xsav,ysav,h,htry,eps,hdid,
     + hnext,hh,fy,fz,curr,id,dummy,l,c,r,vb,xa,ya,y1a,y2a
      parameter(nmax=2,pgrow=-0.2d0,pshrnk=-0.25d0,fcor=1.d0/15.d0,
     +          one=1.d0,safety=0.9d0,errcon=6.d-4)
      external fy,fz
      dimension y(2),dydx(2),ytemp(2),ysav(nmax),dysav(nmax),
     + xa(1000),ya(1000),y1a(1000),y2a(1000)
      common l,c,r,vb/inter/xa,ya,y1a,y2a,n
      xsav=x
      ysav(1)=y(1)
      ysav(2)=y(2)
      dysav(1)=dydx(1)
      dysav(2)=dydx(2)
      h=htry
 1    hh=0.5d0*h
      call rk4(ysav,xsav,hh,ytemp)
      x=xsav+hh
      dydx(1)=fy(ytemp(2))
      call rk4(ytemp,x,hh,y)
      x=xsav+h
      if (x.eq.xsav) pause 'Step size not significant in RKQC.'
      call rk4(ysav,xsav,h,ytemp)
      do 12 i=1,2
      ytemp(i)=y(i)-ytemp(i)
 12   continue
      if (ytemp(1).gt.ytemp(2)) then
      m=1
      else
      m=2
      endif
      errmax=ytemp(m)/(eps*y(m))
      if (errmax.gt.one) then
      h=safety*h*(errmax**pshrnk)
      go to 1
      else
      hdid=h
      if (errmax.gt.errcon) then
      hnext=safety*h*(errmax**pgrow)
      else
      hnext=4.d0*h
      endif
      endif
```

```
      do 13 i=1,2
      y(i)=y(i)+ytemp(i)*fcor
13    continue
      call splint (y(1),id,dummy)
      curr=c*y(2)+id
      return
      end

      subroutine RK4(y,x0,h,yout)

      double precision y,x0,y0,h,yout,z0,yk1,yk2,yk3,yk4,
     +         zk1,zk2,zk3,zk4,fy,fz
      external fy,fz
      dimension y(2),yout(2)
      y0=y(1)
      z0=y(2)
      yk1=h*fy(z0)
1     zk1=h*fz(x0,y0,z0)
2     yk2=h*fy(z0+.5d0*zk1)
3     zk2=h*fz(x0+.5d0*h,y0+.5d0*yk1,z0+.5d0*zk1)
4     yk3=h*fy(z0+.5d0*zk2)
5     zk3=h*fz(x0+.5d0*h,y0+.5d0*yk2,z0+.5d0*zk2)
6     yk4=h*fy(z0+zk3)
128   zk4=h*fz(x0+h,y0+yk3,z0+zk3)
      yout(1)=y0+(yk1+2.d0*yk2+2.d0*yk3+yk4)/6.d0
      yout(2)=z0+(zk1+2.d0*zk2+2.d0*zk3+zk4)/6.d0
      return
      end

      subroutine SPLINE(yp1,ypn)

c This subroutine fits cubic splines to a set of tabulated data.  It was
c adapted from the routine published in Ref. [1].  The common blocks have
c been added for ease of handling.

      double precision x,y,y1,y2,u,yp1,ypn,p,sig,qn,un
      parameter (nmax=1000)
      dimension x(1000),y(1000),y1(1000),y2(1000),u(nmax)
      common /inter/x,y,y1,y2,n
      if (yp1.gt..99d30) then
      y2(1)=0.d0
      u(1)=0.d0
      else
      y2(1)=-0.5d0
      u(1)=(3.d0/(x(2)-x(1)))*((y(2)-y(1))/(x(2)-x(1))-yp1)
      endif
      do 11 i=2,n-1
      sig=(x(i)-x(i-1))/(x(i+1)-x(i-1))
      p=sig*y2(i-1)+2.d0
      y2(i)=(sig-1.d0)/p
      u(i)=(6.d0*((y(i+1)-y(i))/(x(i+1)-x(i))-(y(i)-y(i-1))
     +              /(x(i)-x(i-1)))/(x(i+1)-x(i-1))-sig*u(i-1))/p
11    continue
      if (ypn.gt..99e30) then
      qn=0.d0
      un=0.d0
      else
      qn=0.5d0
      un=(3.d0/(x(n)-x(n-1)))*
     +    (ypn-(y(n)-y(n-1))/(x(n)-x(n-1)))
      endif
      y2(n)=(un-qn*u(n-1))/(qn*y2(n-1)+1.d0)
      do 12 k=n-1,1,-1
      y2(k)=y2(k)*y2(k+1)+u(k)
12    continue
      return
      end

      subroutine SPLINT(x,y,y1)

c This subroutine performs spline interpolation and is designed to be used
c in conjunction with SPLINE [1].  It was adapted in order to allow derivatives
c to be evaluated numerically and output.  The common blocks have been added
c for ease of handling.

      double precision xa,ya,y1a,y2a,x,y,y1,h,a,b
      dimension xa(1000),ya(1000),y1a(1000),y2a(1000)
      common /inter/xa,ya,y1a,y2a,n
      klo=1
      khi=n
1     if (khi-klo.gt.1) then
      k=(khi+klo)/2
      if (xa(k).gt.x) then
```

```
      khi=k
      else
      klo=k
      endif
      go to 1
      endif
      h=xa(khi)-xa(klo)
      if (h.eq.0.d0) pause 'Bad XA input in SPLINT.'
      a=(xa(khi)-x)/h
      b=(x-xa(klo))/h
      y=a*ya(klo)+b*ya(khi)+
     +  ((a**3-a)*y2a(klo)+(b**3-b)*y2a(khi))*(h**2)/6.d0
      y1=(ya(khi)-ya(klo))/h-
     +  ((3.d0*(a**2)-1.d0)*y2a(klo)-(3.d0*(b**2)-1.d0)*y2a(khi))*h/6.d0
      return
      end

 200  double precision function fy(z)
c Function subroutine to evaluate dV/dt (=z, in this case).

      double precision z
      fy=z
      return
      end

      double precision function fz(x,v,z)
c Function subroutine to evaluate d²V/dt² = dz/dt.

      double precision x,v,z,xa,ya,y1a,y2a,dcdv,ci,l,c,r,vb,fy,rdc
      common l,c,r,vb/inter/xa,ya,y1a,y2a,n
      dimension xa(1000),ya(1000),y1a(1000),y2a(1000)
      call splint(v,ci,dcdv)
      rdc=v/ci
 211  fz=vb/(l*c)-fy(z)*(dcdv/c+r/l)-v*(r+rdc)/(l*c*rdc)
      return
      end
```

References

1. W. H. Press, B. P. Flannery, S. A. Teukolsky, and W. T. Vetterling, "Numerical recipes: the art of scientific computing", Cambridge University Press, New York, 1987.

APPENDIX III

DEVICE PROCESSING AND PACKAGING

III.1 Substrate thinning and re-processing

As mentioned previously, some devices were packaged in the LEW Techniques E10/A microwave package. As the substrate thickness of the MOCVD heterostructures was 0.4 mm the wafers had to be thinned down in order to allow their assembly into such small dimensions (see chapter 3). The problem was that these structures had back contact ohmic metallisation and had been previously alloyed at a temperature of 400^{o}C for 12 minutes. This meant that after thinning the wafers, the back contacts would have to be re-formed.

The wafers were diced into $1 \times 1 cm^2$ chips for ease of handling and fixed face-down onto a manual lapping jig using cyanoacrilate adhesive. The substrate was then lapped down to about 150 - 200 μm on 1200-grit grinding paper mounted on a flat glass plate. This produced a flat surface with roughness of the order of 20 - 30 μm which promotes adhesion of the ohmic metal to the substrate. The chips were then detached from the lapping jig by dissolving the adhesive in acetone.

The chips were thoroughly cleaned by a 5 minute immersion in boiling acetone followed by another 5 minutes in boiling propanol, after which they were blow-dried under a jet of nitrogen. They were then mounted epilayer face-down on a glass microscope slide using a small quantity of photoresist. The assembly was then placed inside a conventional vacuum coating unit where a Au-Ge (12 at% Ge) layer was evaporated onto the substrate side of the chips to a thickness of about 0.1 μm. Immersion in acetone removed the chips from the backing plate.

III.1.1 Rapid thermal annealing

The new metallisation had to be 'activated' by alloying or annealing at elevated temperatures to permit (nearly) ohmic electrical behaviour of the contact. Figure III.1 shows a typical I-V characteristic of a $70\times70\mu m^2$ device from the #524 wafer before thermal activation of the new substrate contact. The high series resistance is evident from the high values of V_p. The substantial difference in V_p between the forward and reverse bias is mainly due to a large difference in the contact resistivity on the two faces of the chip.

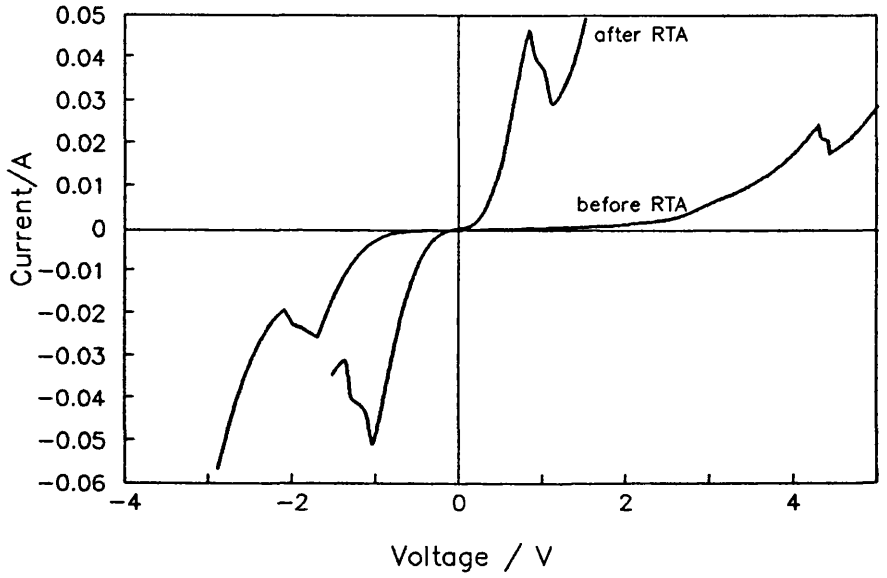


Figure III.1. I-V characteristics of a $70\times70\mu m^2$ device from the MOCVD #524 wafer with the new substrate metallisation measured before and after RTA.

Since the top metallisation containing the patterned devices had already been alloyed, this stage of the re-processing procedure was expected to cause problems by degrading the quality of the existent top contacts. It was then decided to adopt a rapid thermal annealing (RTA) process in the hope that the top contacts would not be effected significantly. For this purpose an RTA furnace was designed and constructed

as represented schematically in figure III.2. The chip is mounted substrate-down inside the pan and held in position by the spring clamp. The heater block, which is made of copper and has a polished surface, is heated to a temperature of about 470°C in a reducing atmosphere of dry forming gas (N_2-H_2 mixture, 96%:4%) which is maintained throughout the annealing cycle. The sample pan rests on the water-cooled copper block until the heated block reaches a steady temperature, and is then rotated through about 180° and lowered down onto the hot stage, where it is kept under slight pressure as long as required. A thermocouple is provided for monitoring the chip temperature during the cycle.

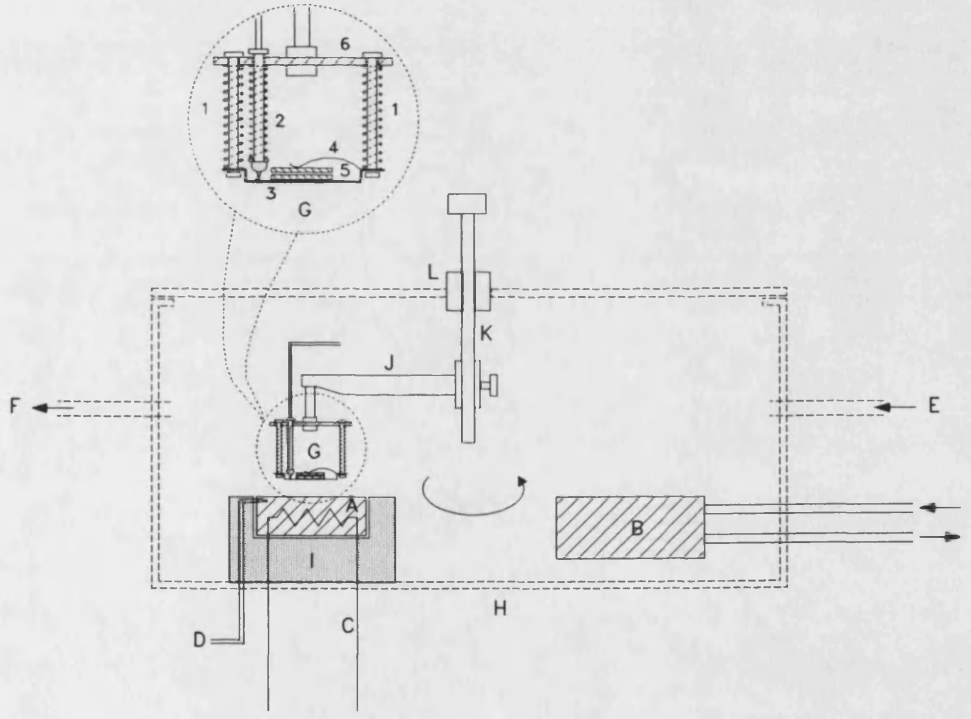


Figure III.2. Schematic of the rapid thermal annealing furnace. Key: (A) heated copper block, (B) water-cooled copper block, (C) heater powered from temperature controller, (D) temperature control thermocouple, (E)-(F) forming gas inlet and outlet, (G) sample holder: 1) spring-loaded hollow stainless steel supports, 2) spring-loaded sample temperature-monitoring thermocouple, 3) thin phosphor-bronze press-moulded sample pan, 4) spring clamp, 5) semiconductor wafer, 6) stainless steel supporting plate, (H) air-tight metal enclosure, (I) insulating block, (J) supporting beam, (K) control rod, (L) rotary shaft vacuum leadthrough.

When the temperature reaches the maximum desired, the sample is lifted off the hot stage, quickly rotated back over to the cold stage and pressed down to make intimate contact with the polished copper surface of the latter. Water cooling was found necessary since otherwise the cold block temperature would eventually exceed 100^{o}C. This simple design allows excellent, controllable temperature cycles with rise-times comparable to expensive state-of-the-art RTA systems and much shorter fall-times. A typical temperature cycle obtained with the prototype system is shown in figure III.3. It is observed that the temperature rises from an initial 27^{o}C to 370^{o}C in about 3 seconds. The maximum temperature allowed in this particular cycle was 400^{o}C, after which the sample holder was switched to the cooling stage, where a sample temperature drop of 250^{o}C is obtained in the first 2 seconds. The nearly straight portion of the curve between 400 and 370^{o}C on the falling edge corresponds to the switching interval between hot and cold stages.

Different temperature cycles were tried on a number of test chips in order to optimise the process. In each case the original I-V characteristic of a few sample devices were compared with the corresponding characteristics after processing. The optimum cycle which did not result in any significant change was found to be one which allowed the substrate temperature to vary between 380 and 402^{o}C in 21 seconds. The hot stage temperature for this cycle was set at 470^{o}C and the chip was covered with a piece of scrap GaAs wafer of roughly the same area and held in position substrate-down with the spring clamp, as shown in figure III.2.

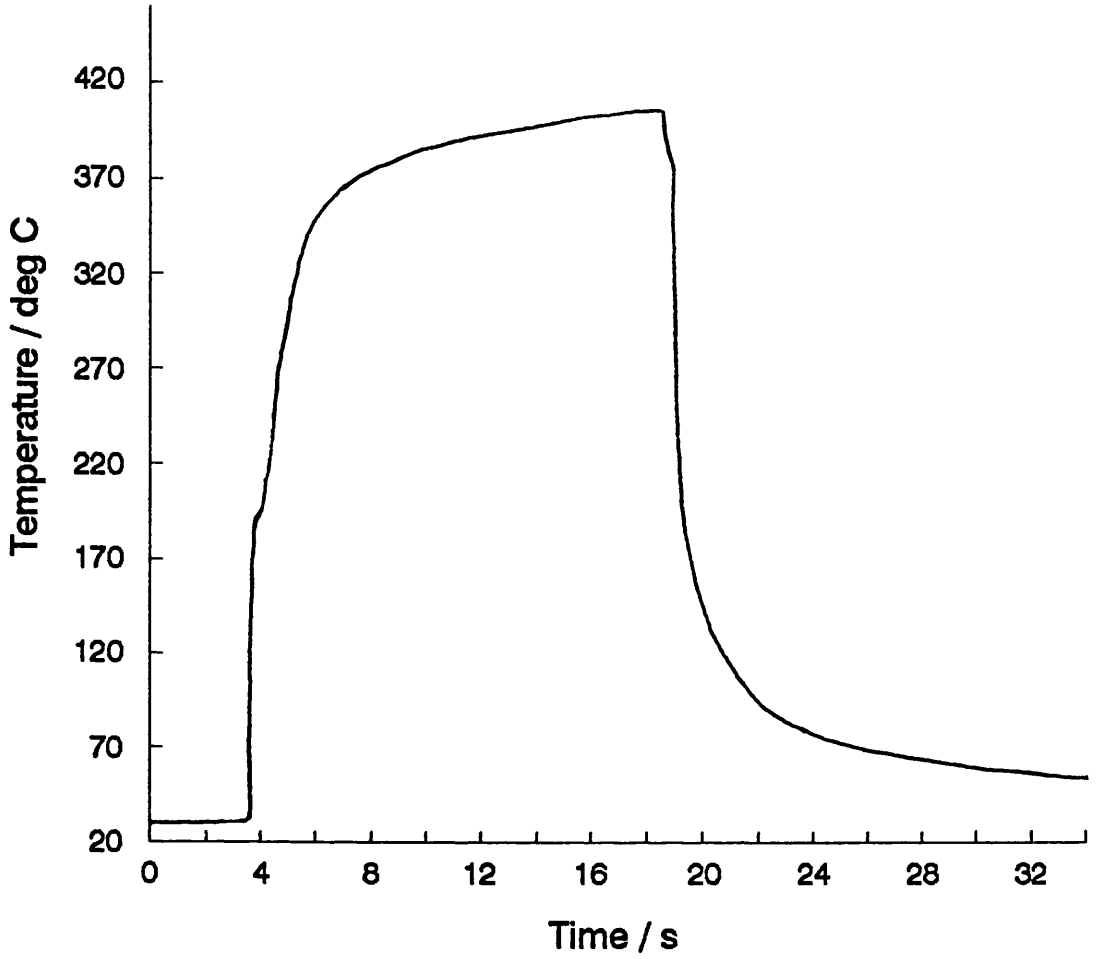


Figure III.3. A typical RTA cycle obtained with the prototype system described in the text.

III.2 Device packaging

The first devices tested were mounted in S4-type microwave packages, the LEW Techniques E3 with the C1/S covers. These packages are virtually identical to the S4 and can accommodate full-thickness chips. Thus the first batch to be packaged here at Bath were scribed and cleaved directly from the available wafers into roughly $500\times500\mu m^2$ pieces, each containing an individual device. In the case of the E10/A packages, the thinned wafers were scribed and cleaved into $300\times300\mu m^2$ chips for packaging. The devices ranged in mesa area from $70\times70\mu m^2$ to $20\times20\mu m^2$.

The first few chips were fixed to the post with silver-loaded epoxy and cured for 12 hours at a temperature of 80°C followed by 1 hour at 100°C. However the series resistance proved to be appreciably high. Subsequent tests on the epoxy revealed that this was at the root of the problem, as it was probably past its shelf life. It was thus decided to use indium-alloy solder both for attaching the chip and the cover, since this would provide better electrical contacts and result in improved mechanical strength of the completed package.

Indium Corporation of America alloy No. 2 (composition: 80% In, 15% Pb, 5% Ag), with a melting point of 149°C, was used to solder the chip substrate to the gold-plated package post. Thin slices of the solder (which is supplied in the form of ~0.6 mm-diameter wire) where cut by means of a scalpel blade and pressed even thinner (~50μm) between two flat glass sheets. The subsequent flattened dots where diced into rectangular pieces of sides roughly 500μm for the E3 and 300μm for the E10/A package.

The soldering procedure is delicate and especially tedious with the much smaller E10/A package. Special brass fixing jigs had to be constructed to hold the packages firmly in place for soldering and wire bonding. Both these operations were performed by mounting the fixing jigs on the heated work holder of a West Bond model 7400A ultrasonic wire bonder. The package post is first smeared with a tiny amount of the appropriate flux. A pre-formed piece of indium-alloy solder is then positioned on top of the post and made to flow by setting the work holder temperature to about 160°C. The heat is then turned down and the solder allowed to solidify. The chip is then placed substrate-down on top of the post and centralised. Heat is once more applied until the solder flows. At this point the bonding wedge is brought

down onto the chip surface and light pressure applied to push the chip down onto the post. This light pressure is maintained while the work holder is allowed to cool down.

The bonder used is equipped with a vertical feed wedge and is capable of bonding 12.5 μm-diameter gold wire. The top device contact is completed by means of a stich-bond that stretches diagonally across the top flange and is attached to the device in the middle of its length. This configuration reduces the parasitic inductance by about a half relative to the single-wire bond. Figure III.4 shows a photograph of one of the first devices mounted and bonded into an E3 package. In this particular case the chip is oblong.

Figure III.4. An RTD chip mounted in an E3 microwave package - top cover removed.

A lower melting point alloy was used for soldering the top cover. This was the alloy No. 1 (composition: 50% In, 50% Sn) with a melting point of 125°C and thus flows without effecting the previous alloy if heated to just above this temperature. Small pieces of No. 1 solder are cut and placed around the ridge of a top cover (placed on the work holder surface) which has been previously smeared with a small

quantity of flux. The E10/A package cover (C10) is assembled as follows. The work holder temperature is set to about 135^{o}C and the solder allowed to flow. The package flange is next smeared with flux and the cover positioned centrally and held in place until the solder re-flows. The assembled package is then allowed to cool and removed from the fixing jig.

The larger E3 package lids have a top-hat shape. This was exploited in the construction of an assembly tool which allows automatic alignment of the cover with the package flange. In this case a low temperature soldering iron with a narrow tip is used to re-flow the solder and thus fix the top and bottom parts of the package together accurately.

This method of mounting devices was found to be very effective, albeit laborious, as the finished package was mechanically strong and the series resistance introduced found to be negligibly small.

APPENDIX IV

TYPICAL RTD OSCILLATION SPECTRA

This appendix shows an example of some typical oscillation spectra observed as described in chapter 4. The spectra shown in figures IV.1 - IV.4 were obtained with a $50\times50\mu m^2$ device (the 524#B) from the #524 pseudomorphic MOCVD heterostructure described in chapter 2. The device was housed in an E10/A microwave package. Figure IV.1 shows the oscillation spectrum of this device at a bias of 1.03V with the tuner stubs moved fully in, an adjustment which resulted in the sharp spectral lines seen with the fundamental at 890 MHz. The third harmonic output is about 20 dB below the fundamental. The bias circuit was stable. Figure IV.2 represents the low-frequency spectrum taken with the device under the same conditions (compare with the system noise spectrum of figure IV.5).

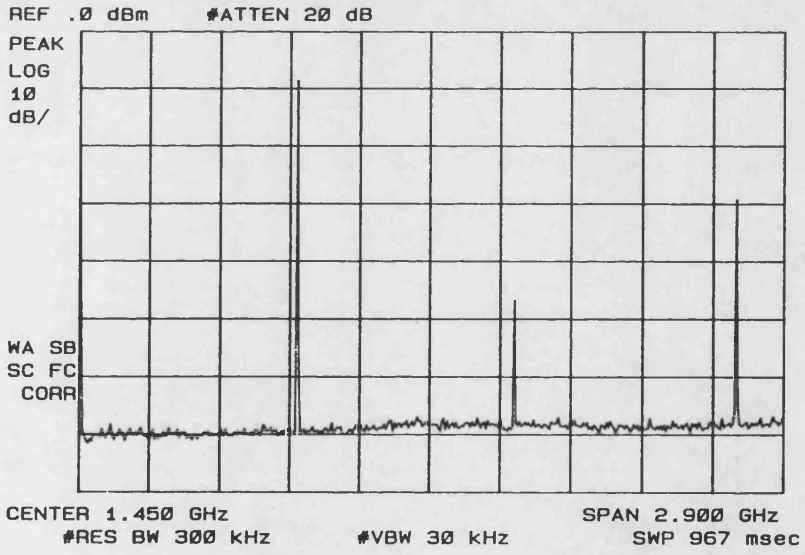


Figure IV.1. Spectral output of the 524#B device at 1.03V bias. Both tuner stubs were moved fully in.

The effect of de-tuning on the spectral output is shown in figure IV.3. This spectrum was measured after retracting one of the tuner stubs. Notice the broader lines and the slight frequency shift. With this tuner setting, spurious oscillations were observed in the bias line. Figure IV.4 shows the low-frequency spectrum resulting under the de-tuned conditions. Notice the peak at about 4 MHz. Even though the bias network dc arm cutoff frequency is 45 MHz, the spectrum of figure IV.4 still shows evidence of low-frequency instability.

Figure IV.6a and b show an example of mode hopping. The device in question was a $50\times50\mu m^2$ (the 421#B) from the #421 MOCVD wafer, also described in chapter 2. This device was mounted into an E3 package. Figure IV.6a shows the spectrum obtained by sliding the stub assembly towards the device with the stubs moved fully in. When the stub assembly crosses a certain point, say X, the spectrum suddenly changes to that of figure IV.6b. This mode hopping also occurs of its own accord if the stub assembly is left unadjusted at a point immedeately before X.

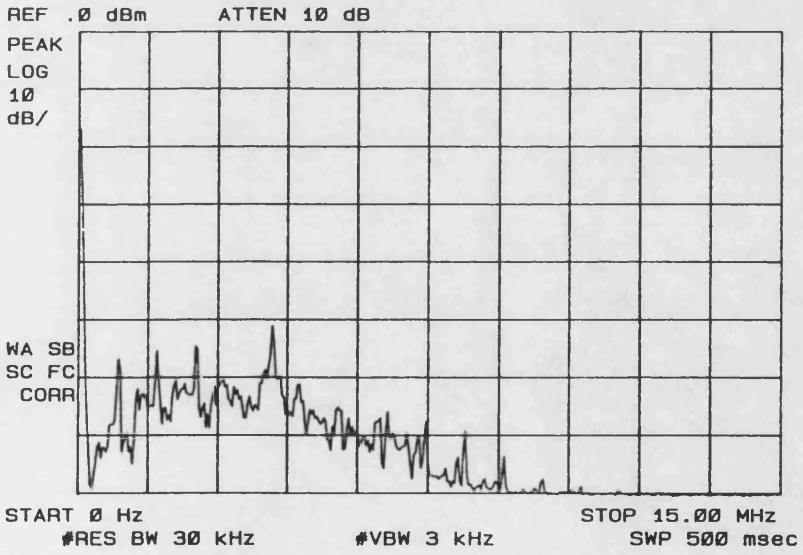


Figure IV.2. 0-15 MHz spectrum of the 524#B under the same conditions as in figure IV.1.

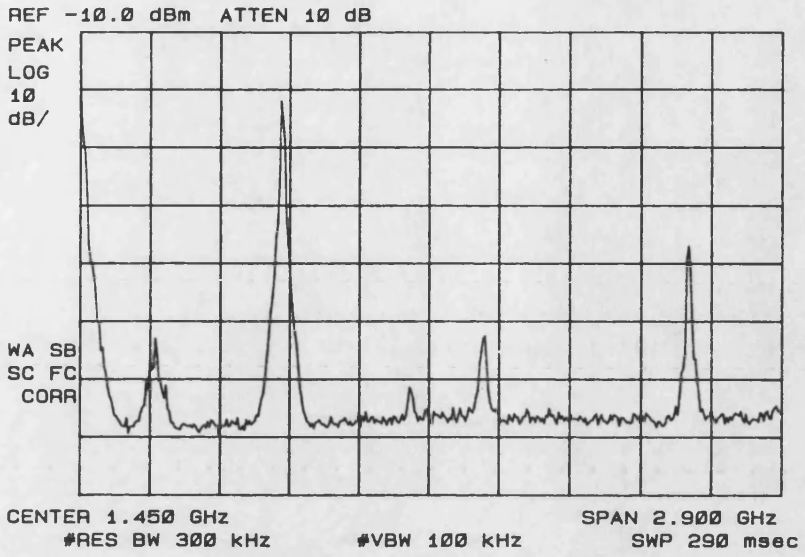


Figure IV.3. Spectral output of the 524#B at 1.03V bias. One of the tuner stubs was retracted.

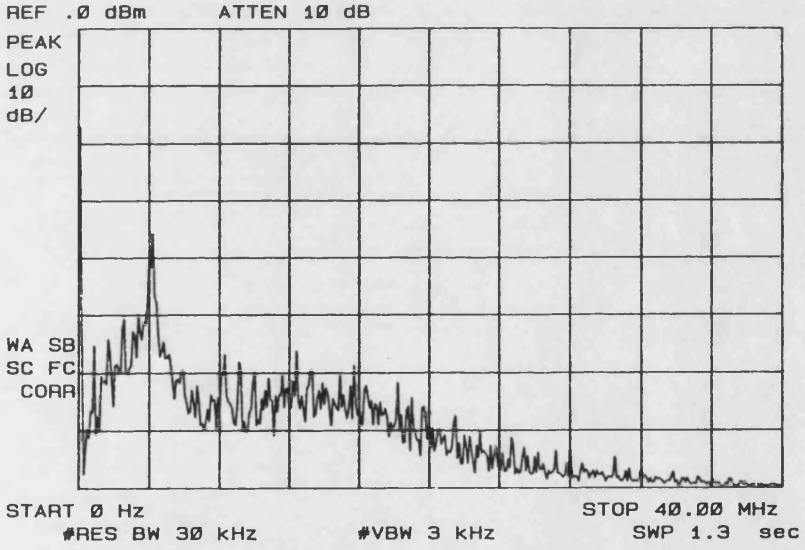


Figure IV.4. 0-40 MHz spectrum of the 524#B under the conditions of figure IV.3.

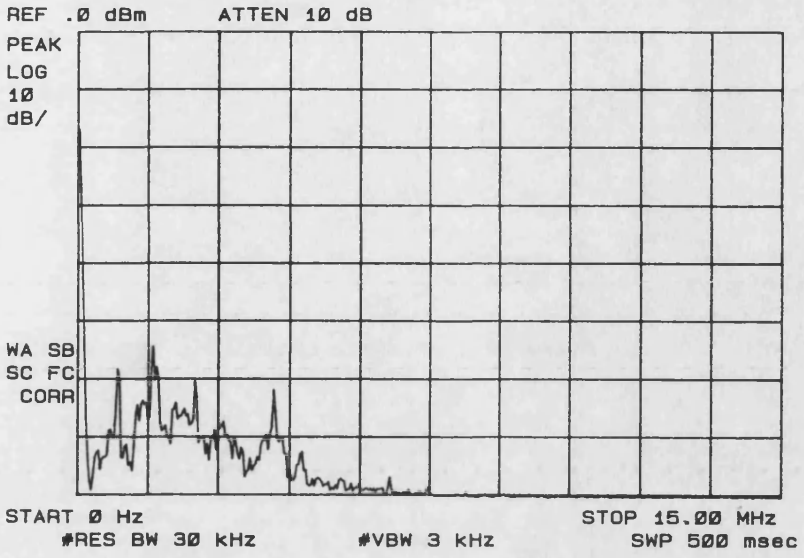
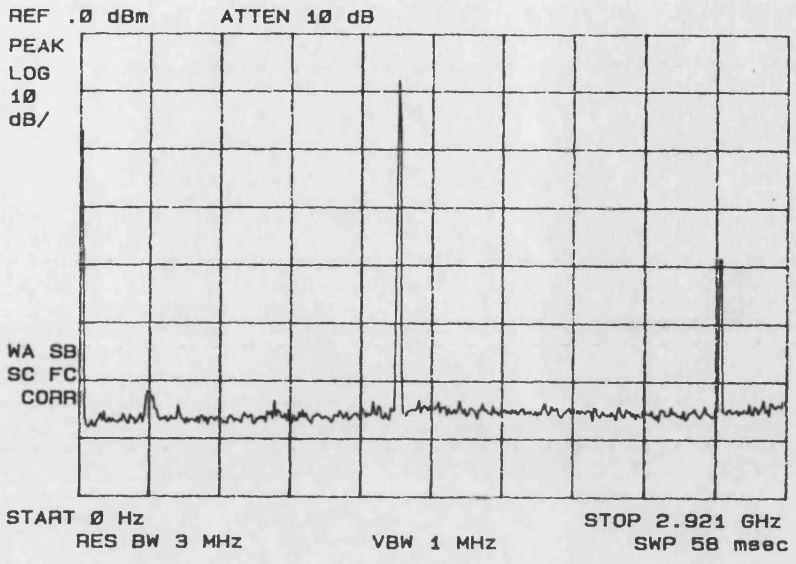


Figure IV.5. System noise spectrum between 0 and 15 MHz.

a.



b.

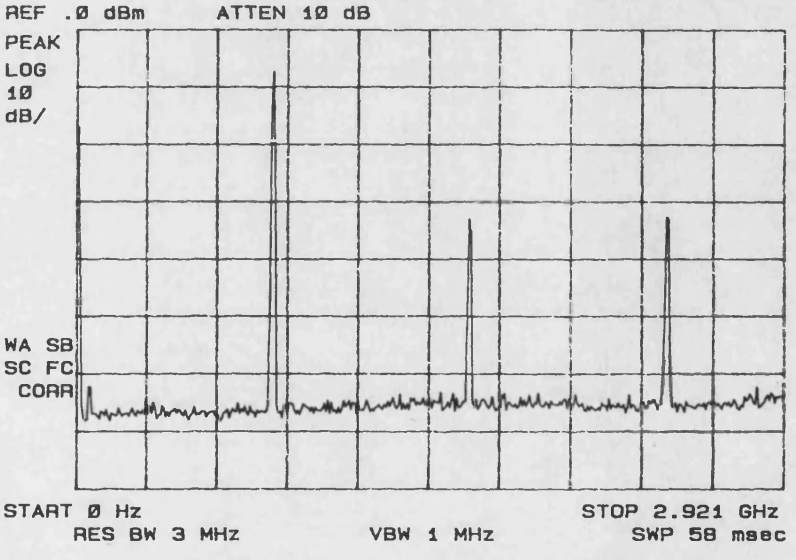


Figure IV.6. An example of mode hopping. (a) and (b) represent the spectral output of the 421#B device at a bias of 1.05V, respectively before and after a mode hop occurs.

APPENDIX V

NONLINEAR ANALYSIS PROGRAM

This appendix contains a listing of the nonlinear multiplier analysis program mentioned in chapter 5. The code has not been optimised. Write statements have been omitted, as has the evaluation of multiplier performance in subroutine MLTPER, since these depend upon the intended purpose of any particular version used. The progamme is well commented and the most important variable names have been retained from the original version by Siegel et al. and are explained in chapter 5, which discusses in detail the theory behind the calculations performed.

```
      PROGRAM MULE10A2

C---MULTIPLIER ANALYSIS PROGRAM BASED ON P.H.SIEGEL, A.R.KERR, AND
C---W.HWANG, "TOPICS IN THE OPTIMIZATION OF MILLIMETER-WAVE MIXERS",
C---NASA TECHNICAL PAPER 2287 (MARCH 1984).
C---THIS VERSION ENABLES ANALYSIS OF MULTIPLIER PERFORMANCE WITH AN
C---E10/A - PACKAGED DEVICE IN THE 3.5MM COAXIAL MOUNT DESCRIBED IN
C---CHAPTER 3.

C    BEGIN THE MULTIPLIER ANALYSIS

C---FOR COMMON/CONST/:
      REAL*8 PI
      INTEGER NINP
C---FOR COMMON/DIODE/:
      REAL*8 RS,FP,WP,VIN(500),IIN(500),GIN(500),CIN(500),DCDVIN(500),
     +GIN2(500),CIN2(500),IGJ,ICJ,GJ,CJ
C---FOR COMMON/IMPED/:
      REAL*8 LOPWR,ZER(16),ZEI(16),ZERDC
C---FOR COMMON/LOOPS/:
      INTEGER NH,NLO,JLO,NVLO,NPTS,NCURR,IPT,NPRINT,NITER
C---FOR COMMON/RKG/:
      REAL*8 ACC,VDINIT
      INTEGER NDIM
C---FOR COMMON/TLINE/:
      REAL*8 Z0,ZQACC
      INTEGER ZQFLAG
C---FOR COMMON/VOLTS/:
      COMPLEX*16 VR(16)
      REAL*8 VRDC,VLO,VDBIAS,IDBIAS,BIAS(1000)
```

```
      INTEGER NBIAS
C---FOR COMMON/MULT/:
      INTEGER NIN,NOUT
      REAL*8 PAVAIL,PABS,POUT
C---FOR COMMON/PUMP/:
      INTEGER NPUMP
      REAL*8 PMPPWR(200)
C---FOR COMMON/MNTPKG/:
      REAL*8 C(4),L(4)
C---FOR COMMON/ZMEAS/:
      COMPLEX*16 ZM(16)
      REAL*8 CC1,CC2,LW
C---THE COMMON BLOCKS USED ARE:
      COMMON/CONST/PI,NINP
      COMMON/DIODE/RS,FP,WP,VIN,IIN,GIN,CIN,DCDVIN,
     +GIN2,CIN2,IGJ,ICJ,GJ,CJ
      COMMON/IMPED/LOPWR,ZER,ZEI,ZERDC
      COMMON/LOOPS/NH,NLO,JLO,NVLO,NPTS,NCURR,IPT,NPRINT,NITER
      COMMON/RKG/ACC,VDINIT,NDIM
      COMMON/TLINE/ZO,ZQACC,ZQFLAG
      COMMON/VOLTS/VR,VRDC,VLO,VDBIAS,IDBIAS,NBIAS,BIAS
      COMMON/MULT/NIN,NOUT,PAVAIL,PABS,POUT
      COMMON/PUMP/NPUMP,PMPPWR
      COMMON/MNTPKG/C,L
      COMMON/ZMEAS/ZM,CC1,CC2,LW
      CALL DATAIN
C---CALL SPLINE TO OBTAIN SECOND DERIVATIVES OF THE DC CONDUCTANCE
C---AND CAPACITANCE WITH RESPECT TO VOLTAGE.  THESE ARE REQUIRED BY
C---SPLINT, WHICH INTERPOLATES CURRENT, CONDUCTANCE AND CAPACITANCE
C---VALUES AS REQUESTED IN FCT AND OUTP.
      CALL SPLINE(VIN,IIN,NINP,GIN(1),GIN(NINP),GIN2)
      CALL SPLINE(VIN,CIN,NINP,DCDVIN(1),DCDVIN(NINP),CIN2)
C---CALL LGSIG TO DO THE LARGE SIGNAL ANALYSIS
      CALL LGSIG

      END

      SUBROUTINE LGSIG

C---THE VARIABLES USED IN THIS SUBROUTINE ARE AS FOLLOWS:
C---FOR COMMON/CONST/:
      REAL*8 PI
      INTEGER NINP
C---FOR COMMON/DATA/:
      REAL*8 ICJDAT(51),IGJDAT(51),CJDATA(51),GJDATA(51)
      REAL*8  VDDATA(51),IDDATA(51)
C---FOR COMMON/DIODE/:
      REAL*8 RS,FP,WP,VIN(500),IIN(500),GIN(500),CIN(500),DCDVIN(500),
     +GIN2(500),CIN2(500),IGJ,ICJ,GJ,CJ
C---FOR COMMON/FORITS/:
      REAL*8 GJCOS(17),GJSIN(17),CJCOS(17),CJSIN(17),VDCOS(17)
      REAL*8 VDSIN(17),IDCOS(17),IDSIN(17)
      INTEGER IER
```

```
C---FOR COMMON/IMPED/:
      REAL*8 LOPWR,ZER(16),ZEI(16),ZERDC
C---FOR COMMON/LOOPS/:
      INTEGER NH,NLO,JLO,NVLO,NPTS,NCURR,IPT,NPRINT,NITER
C---FOR COMMOM/MULT/:
      INTEGER NIN,NOUT
      REAL*8 PAVAIL,PABS,POUT
C---FOR COMMON/RKG/:
      REAL*8 ACC,VDINIT
      INTEGER NDIM
C---FOR COMMON/TLINE/:
      REAL*8 ZO,ZQACC
      INTEGER ZQFLAG
C---FOR COMMON/VOLTS/:
      COMPLEX*16 VR(16)
      REAL*8 VRDC,VLO,VDBIAS,IDBIAS,BIAS(1000)
      INTEGER NBIAS
C---FOR COMMON/PUMP/:
      INTEGER NPUMP
      REAL*8 PMPPWR(200)
C---FOR VARIABLES NOT IN ANY COMMON BLOCKS:
      COMPLEX*16 RHO(16),ZEMB(16),VL(16),ID,VD,ZQ
      REAL*8 Y(1),DERY(1),PRMT(5),AUX(8,1)
      REAL*8 VLDC,VDC,RHODC,ZEMBDC,VDCMLT
      REAL*8  ZQMAG(16),ZQPHA(16)
      INTEGER IHLF,ITER,JPUMP,JPT,JH,NHP1,NHD2,NHD2P1
      CHARACTER*40 SPERR
C---THE COMMON BLOCKS USED ARE:
      COMMON/CONST/PI,NINP
      COMMON/DATA/ICJDAT,IGJDAT,CJDATA,GJDATA,VDDATA,IDDATA
      COMMON/DIODE/RS,FP,WP,VIN,IIN,GIN,CIN,DCDVIN,GIN2,CIN2,
     +IGJ,ICJ,GJ,CJ
      COMMON/FORITS/GJCOS,GJSIN,CJCOS,CJSIN,VDCOS,VDSIN,IDCOS,IDSIN,IER
      COMMON/IMPED/LOPWR,ZER,ZEI,ZERDC
      COMMON/LOOPS/NH,NLO,JLO,NVLO,NPTS,NCURR,IPT,NPRINT,NITER
      COMMON/MULT/NIN,NOUT,PAVAIL,PABS,POUT
      COMMON/RKG/ACC,VDINIT,NDIM
      COMMON/TLINE/ZO,ZQACC,ZQFLAG
      COMMON/VOLTS/VR,VRDC,VLO,VDBIAS,IDBIAS,NBIAS,BIAS
      COMMON/PUMP/NPUMP,PMPPWR
C---SINCE THE FCT AND OUTP SUBPROGRAMS ARE CALLED BY DRKGS THEY MUST BE
C---DEFINED EXTERNALLY.
      EXTERNAL FCT,OUTP
C---DEFINE SOME USEFUL CONSTANTS
      NHP1=NH+1
      NHD2=NH/2
      NHD2P1=NH/2+1
      WP=2.0D0*PI*FP
C---CAL ZEMBED TO FORM THE EMBEDDING IMPEDANCES
      CALL ZEMBED(ZER,ZEI,FP,NH)
C---CALL PRINT1 TO WRITE THE INITIAL CONDITIONS
      CALL PRINT1(ZEMB,ZERDC,ZEMBDC,ZER,ZEI,PRMT,Y,DERY,
```

```
     +VDBIAS,NH,NHD2)
C---OPEN OUTPUT FILE
      OPEN(6,FILE='multip.out',STATUS='NEW')
C---BEGIN THE LOOP OVER THE PUMP POWER, PAVAIL IN WATTS
      DO 30 JPUMP=1,NPUMP
C---BEGIN THE LOOP OVER THE DC BIAS VOLTAGE
      DO 20 JVDC=1,NBIAS
      VDBIAS=BIAS(JVDC)
C---SET THE IMPEDANCE AT DC TO Z0 TO SPEED THE ANALYSIS
      ZEMBDC=Z0
C---FORM THE SET OF COMPLEX IMPEDANCES WITH THE SERIES RESISTANCE ADDED
      DO 1 JH=1,NH
    1 ZEMB(JH)=DCMPLX(ZER(JH)+RS,ZEI(JH))
C---CALCULATE THE REFLECTION COEFFICIENT OF THE EMBEDDING NETWORK AT
C---EACH LO HARMONIC
      RHODC=(ZEMBDC-Z0)/(ZEMBDC+Z0)
      DO 13 JH=1,NH
   13 RHO(JH)=(ZEMB(JH)-Z0)/(ZEMB(JH)+Z0)
      PAVAIL=PMPPWR(JPUMP)/1000.0D0
C---INITIALIZE VARIABLES FOR THE INTEGRATION BY DRKGS
      VLO=DSQRT(PAVAIL*8.0D0*ZER(NIN))
      PRMT(1)=0.0D0
      PRMT(2)=2.0D0*PI
      PRMT(3)=PRMT(2)/DFLOAT(NPTS)
      PRMT(4)=ACC
      Y(1)=VDINIT
C---VDBIAS IS THE DC VOLTAGE APPLIED TO THE CIRCUIT IN WHICH
C---ZE(0)=Z0.  THE TRUE MULTIPLIER BIAS WILL BE FOUND LATER.
      VDC=VDBIAS
C---THE INITIAL LEFT AND RIGHT TRAVELING WAVES ON THE TRANSMISSION LINE
      DO 2 JH=1,NH
      VL(JH)=DCMPLX(0.0D0,0.0D0)
    2 VR(JH)=DCMPLX(0.0D0,0.0D0)
C---THE DC TERMS
      VLDC=0.0D0
      VRDC=VDC*Z0/(Z0+ZEMBDC)
      ITER=0
      VR(1)=VLO*Z0/(ZEMB(1)+Z0)
C---INITIALIZE DRKGS ERROR WEIGHT
      DERY(1)=1.0D0
C---START THE REFLECTION CYCLE
    3 ITER=ITER+1
C---PRINT ONLY AFTER MULTIPLES OF NPRINT CYCLES HAVE BEEN COMPLETED
      JPRINT=MOD(ITER,NPRINT)
C---SOLVE THE NETWORK STATE EQUATION OVER ONE LO CYCLE
C---THEN LOOP OVER THE NUMBER OF LO CYCLES TO REACH STEADY STATE
      DO 6 JLO=1,NLO
      IPT=1
      DERY(1)=1.0D0
      CALL DRKGS(PRMT,Y,DERY,NDIM,IHLF,FCT,OUTP,AUX)
    6 CONTINUE
C---CALL DFORIT TO FORM THE FOURIER COEFFICIENTS OF THE DIODE CURRENT
```

```
C---AND VOLTAGE.
      CALL DFORIT(VDDATA,NPTS/2,NH,VDCOS,VDSIN,IER)
      CALL DFORIT(IDDATA,NPTS/2,NH,IDCOS,IDSIN,IER)
C---SET THE FLAG FOR THE CONVERGENCE TESTS
      ZQFLAG=0
C---CALCULATE THE LEFT TRAVELING WAVE  ON THE TRANSMISSION LINE
C---THE MINUS SIGN COMES FROM THE CONVERSION OF THE TRIGONOMETRIC
C---FOURIER SERIES REPRESENTATION RETURNED BY DFORIT INTO THE SINGLE
C---ENDED COMPLEX EXPONENTIAL SERIES REPRESENTATION USED IN THE
C---LARGE SIGNAL ANALYSIS.
      DO 7 JH=1,NH
      VD=DCMPLX(VDCOS(JH+1),-VDSIN(JH+1))
      ID=DCMPLX(IDCOS(JH+1),-IDSIN(JH+1))
      VL(JH)=0.5D0*(VD-ID*Z0)
C---CALCULATE THE IMPEDANCE RATIOS AT EACH PUMP HARMONIC TO DETERMINE
C---THE DEGREE OF CONVERGENCE
      ZQ=VD/ID/ZEMB(JH)
      IF(JH.GT.1) GOTO 5
C---AT THE PUMP FREQUENCY THE CONVERGENCE PARAMETER IS MODIFIED BY VLO
      ZQ=(VLO-VD)/ID/ZEMB(1)
    5 ZQMAG(JH)=CDABS(ZQ)
      ZQPHA(JH)=DATAN2(DIMAG(ZQ),DREAL(ZQ))*57.29577951D0
      IF(ZQMAG(JH).GT.1.0D0+ZQACC) ZQFLAG=ZQFLAG+1
      IF(ZQMAG(JH).LT.1.0D0-ZQACC) ZQFLAG=ZQFLAG+1
    7 CONTINUE
C---THE LEFT TRAVELING WAVE AT DC
      VLDC=0.5D0*(VDCOS(1)-Z0*IDCOS(1))
    9 CONTINUE
C---THE NEW RIGHT TRAVELING WAVE INCIDENT ON THE DIODE
      DO 10 JH=2,NH
   10 VR(JH)=VL(JH)*RHO(JH)
C---THE RIGHT TRAVELING WAVE AT DC AND THE FIRST HARMONIC
      VR(1)=RHO(1)*VL(1)+VLO*Z0/(Z0+ZEMB(1))
      VRDC=RHODC*VLDC+VDC*Z0/(Z0+ZEMBDC)
C---WAS THIS THE LAST REFECTION CYCLE ALLOWED?
   11 IF(ITER.EQ.NITER) GOTO 12
C---HAS THE SOLUTION CONVERGED?
      IF(ZQFLAG.EQ.0) GOTO 12
C---GO ON TO THE NEXT REFLECTION CYCLE
      GOTO 3
C---UNSCALE THE CAPACITANCE VALUES (THEY WERE SCALED IN SUBROUTINE FCT
C---WHICH IS CALLED BY THE DRKGS INTEGRATION ROUTINE).
   12 DO 19 JPT=1,NPTS
   19 CJDATA(JPT)=CJDATA(JPT)/WP
C---FINISH THE ANALYSIS BY OBTAINING THE FOURIER COEFFICIENTS OF THE
C---DIODE CONDUCTANCE AND CAPACITANCE.
      CALL DFORIT(GJDATA,NPTS/2,NH,GJCOS,GJSIN,IER)
      CALL DFORIT(CJDATA,NPTS/2,NH,CJCOS,CJSIN,IER)
C---CALL CALBIAS TO CALCULATE THE ACTUAL BIAS VOLTAGE APPLIED (ALLOWING
C---FOR SERIES RESISTANCE)
      CALL CALBIAS(VDCOS(1),IDCOS(1),ZERDC,RS,Z0,VDCMLT,VDBIAS)
C---CALL MLTPER TO CALCULATE AND PRINT THE MULTIPLIER PERFORMANCE
```

```
      CALL MLTPER(ZER,RS,VDCOS,VDSIN,IDCOS,IDSIN,NHP1,ZQFLAG,FP,VDCMLT)
C---REPEAT THE ANALYSIS WITH A NEW PUMP POWER
   20 CONTINUE
C---REPEAT THE ANALYSIS WITH A NEW BIAS VOLTAGE
   30 CONTINUE
      RETURN
      END

       SUBROUTINE MLTPER(ZER,RS,VDCOS,VDSIN,IDCOS,IDSIN,NHP1,ZQFLAG,FP,VDBIAS)

C---MULTPER CALCULATES THE MULTIPLIER INPUT AND OUTPUT IMPEDANCES, ABSORBED
C---POWER AT THE PUMP FREQUENCY, OUTPUT POWER AT ALL HARMONICS CONSIDERED, ETC.
C---ACCORDING TO THE PURPOSE OF THE INVESTIGATION.  PRINT STATEMENTS HAVE BEEN
C---OMITTED FOR BREVITY.

       COMPLEX*16 ID(17),VD(17),ZIN(17)
       REAL*8 ZER(1),RS,EFF(17),PABS,PAVAIL,POUT,LOSSDB(16),FP,VDBIAS
       REAL*8 VDCOS(NHP1),VDSIN(NHP1),IDCOS(NHP1),IDSIN(NHP1),PODBM(16)
       INTEGER NIN,NOUT,ZQFLAG
       COMMON/MULT/NIN,NOUT,PAVAIL,PABS,POUT
       COMMON/LOOPS/NH,NLO,JLO,NVLO,NPTS,NCURR,IPT,NPRINT,NITER
C---INPUT IMPEDANCES
       DO 10 I=1,NH
       VD(I)=DCMPLX(VDCOS(I+1),-VDSIN(I+1))
       ID(I)=DCMPLX(IDCOS(I+1),-IDSIN(I+1))
       ZIN(I)=VD(I)/ID(I)+DCMPLX(RS,0.0D0)
   10 CONTINUE
C---ABSORBED POWER
       PABS=0.5D0*DREAL(ZIN(NIN)*ID(NIN)*DCONJG(ID(NIN)))
C---OUTPUT POWER
       DO 20 I=2,NH
       POUT=0.5D0*ZER(I)*ID(I)*DCONJG(ID(I))
C---AT THIS POINT, POUT CAN BE USED IN CONJUNCTION WITH PABS TO CALCULATE
C---AND PRINT CONVERSION EFFICIENCY AND CONVERSION LOSS IF REQUIRED
   20 CONTINUE
       RETURN
       END

      SUBROUTINE DRKGS(PRMT,Y,DERY,NDIM,IHLF,FCT,OUTP,AUX)

C---DRKGS IS AN IBM SSP PROGRAM WHICH SOLVES A SYSTEM OF DIFFERENTIAL
C---EQUATIONS BY THE RUNGE-KUTTA ALGORITHM. IT HAS NOT BEEN ALTERED
C---FOR THIS ANALYSIS.

      DIMENSION Y(1),DERY(1),AUX(8,1),A(4),B(4),C(4),PRMT(5)
      DOUBLE PRECISION PRMT,Y,DERY,AUX,A,B,C,X,XEND,H,AJ,BJ,CJ,R1,R2,
     1DELT
      EXTERNAL FCT,OUTP
      DO 1 I=1,NDIM
    1 AUX(8,I)=.06666666666666667D0*DERY(I)
      X=PRMT(1)
      XEND=PRMT(2)
      H=PRMT(3)
      PRMT(5)=0.D0
```

```
      CALL FCT(X,Y,DERY)
      IF(H*(XEND-X))38,37,2
    2 A(1)=.5D0
      A(2)=.2928932188134524 8D0
      A(3)=1.707106781186547 5D0
      A(4)=.1666666666666667D0
      B(1)=2.D0
      B(2)=1.D0
      B(3)=1.D0
      B(4)=2.D0
      C(1)=.5D0
      C(2)=.2928932188134524 8D0
      C(3)=1.707106781186547 5D0
      C(4)=.5D0
      DO 3 I=1,NDIM
      AUX(1,I)=Y(I)
      AUX(2,I)=DERY(I)
      AUX(3,I)=0.D0
    3 AUX(6,I)=0.D0
      IREC=0
      H=H+H
      IHLF=-1
      ISTEP=0
      IEND=0
    4 IF((X+H-XEND)*H)7,6,5
    5 H=XEND-X
    6 IEND=1
    7 CALL OUTP(X,Y,DERY,PRMT)
      IF(PRMT(5))40,8,40
    8 ITEST=0
    9 ISTEP=ISTEP+1
      J=1
   10 AJ=A(J)
      BJ=B(J)
      CJ=C(J)
      DO 11 I=1,NDIM
      R1=H*DERY(I)
      R2=AJ*(R1-BJ*AUX(6,I))
      Y(I)=Y(I)+R2
      R2=R2+R2+R2
   11 AUX(6,I)=AUX(6,I)+R2-CJ*R1
      IF(J-4)12,15,15
   12 J=J+1
      IF(J-3)13,14,13
   13 X=X+.5D0*H
   14 CALL FCT(X,Y,DERY)
      GOTO 10
   15 IF(ITEST)16,16,20
   16 DO 17 I=1,NDIM
   17 AUX(4,I)=Y(I)
      ITEST=1
      ISTEP=ISTEP+ISTEP-2
```

```
18 IHLF=IHLF+1
   X=X-H
   H=.5D0*H
   DO 19 I=1,NDIM
   Y(I)=AUX(1,I)
   DERY(I)=AUX(2,I)
19 AUX(6,I)=AUX(3,I)
   GOTO 9
20 IMOD=ISTEP/2
   IF(ISTEP-IMOD-IMOD)21,23,21
21 CALL FCT(X,Y,DERY)
   DO 22 I=1,NDIM
   AUX(5,I)=Y(I)
22 AUX(7,I)=DERY(I)
   GOTO 9
23 DELT=0.D0
   DO 24 I=1,NDIM
24 DELT=DELT+AUX(8,I)*DABS(AUX(4,I)-Y(I))
   IF(DELT-PRMT(4))28,28,25
25 IF (IHLF-10)26,36,36
26 DO 27 I=1,NDIM
27 AUX(4,I)=AUX(5,I)
   ISTEP=ISTEP+ISTEP-4
   X=X-H
   IEND=0
   GOTO 18
28 CALL FCT(X,Y,DERY)
   DO 29 I=1,NDIM
   AUX(1,I)=Y(I)
   AUX(2,I)=DERY(I)
   AUX(3,I)=AUX(6,I)
   Y(I)=AUX(5,I)
29 DERY(I)=AUX(7,I)
   CALL OUTP(X-H,Y,DERY,PRMT)
   IF(PRMT(5))40,30,40
30 DO 31 I=1,NDIM
   Y(I)=AUX(1,I)
31 DERY(I)=AUX(2,I)
   IREC=IHLF
   IF(IEND)32,32,39
32 IHLF=IHLF-1
   ISTEP=ISTEP/2
   H=H+H
   IF(IHLF)4,33,33
33 IMOD=ISTEP/2
   IF(ISTEP-IMOD-IMOD)4,34,4
34 IF(DELT-.02D0*PRMT(4))35,35,4
35 IHLF=IHLF-1
   ISTEP=ISTEP/2
   H=H+H
   GOTO 4
36 IHLF=11
```

```
      CALL FCT(X,Y,DERY)
      GOTO 39
   37 IHLF=12
      GOTO 39
   38 IHLF=13
   39 CALL OUTP(X,Y,DERY,PRMT)
   40 RETURN
      END

      SUBROUTINE FCT(X,Y,DERY)

C---FCT IS REQUIRED BY DRKGS AND SETS UP THE NETWORK STATE EQUATION FOR THE
C---DIODE AND TRANSMISSION LINE.
C---NOTE THAT THE JUNCTION CAPACITANCE HAS BEEN FREQUENCY SCALED BY 2*PI*FP
C---SO THAT ONE LO CYCLE OCCURS IN 2*PI SECONDS.

C---THE VARIABLE TYPES USED IN THIS SUBROUTINE ARE AS FOLLOWS:
C---FOR COMMON/CONST/:
      REAL*8 PI
      INTEGER NINP
C---FOR COMMON/DIODE/:
      REAL*8 RS,FP,WP,VIN(500),IIN(500),GIN(500),CIN(500),DCDVIN(500),
     +GIN2(500),CIN2(500),IGJ,ICJ,GJ,CJ
C---FOR COMMON/LOOPS/:
      INTEGER NH,NLO,JLO,NVLO,NPTS,NCURR,IPT,NPRINT,NITER
C---FOR COMMON/TLINE/:
      REAL*8 ZO,ZQACC
      INTEGER ZQFLAG
C---FOR COMMON/VOLTS/:
      COMPLEX*16 VR(16)
      REAL*8 VRDC,VLO,VDBIAS,IDBIAS,BIAS(1000)
      INTEGER NBIAS
C---FOR VARIABLES NOT IN ANY COMMON BLOCKS:
      REAL*8 X,Y(1),DERY(1),VS
      REAL*8 CN,SN,CNO,SNO,CN1,SN1,DCAP2
      INTEGER JH
C---THE COMMON BLOCKS USED ARE:
      COMMON/CONST/PI,NINP
      COMMON/DIODE/RS,FP,WP,VIN,IIN,GIN,CIN,DCDVIN,GIN2,CIN2,
     +IGJ,ICJ,GJ,CJ
      COMMON/LOOPS/NH,NLO,JLO,NVLO,NPTS,NCURR,IPT,NPRINT,NITER
      COMMON/TLINE/ZO,ZQACC,ZQFLAG
      COMMON/VOLTS/VR,VRDC,VLO,VDBIAS,IDBIAS,NBIAS,BIAS

C---CALCULATE THE TOTAL VOLTAGE ON THE TRANSMISSION LINE INCIDENT ON THE DIODE
C---USING A FAST TRIGIGONOMETRIC ALGORITHM TO FIND SINES AND COSINES.  THIS
C---ALGORITHM INCREASES THE SPEED OF THE PROGRAM AND WAS SUGGESTED TO THE
C---ORIGINAL AUTHORS BY O. GRONDIN OF THE UNIVERSITY OF MICHIGAN.  IT HAS BEEN
C---RETAINED IN THE PRESENT VERSION.
```

```
      VS=VRDC
      SN1=DSIN(X)
      CN1=DCOS(X)
      SN0=0.0D0
      CN0=1.0D0
      DO 1 JH=1,NH
      SN=SN1*CN0+CN1*SN0
      CN=CN1*CN0-SN1*SN0
      VS=VS+DREAL(VR(JH))*CN-DIMAG(VR(JH))*SN
      CN0=CN
    1 SN0=SN
C---MULTIPLY BY 2 TO CONVERT VS INTO AN EQUIVALENT TRANSMISSION LINE
C---VOLTAGE SOURCE
      VS=VS*2.0D0
C---INTERPOLATE TO FIND DIODE CAPACITANCE, CONDCTANCE AND CURRENT
      IF(DABS(Y(1)).GT.50.D0) Y(1)=DSIGN(50.D0,Y(1))
      CALL SPLINT(VIN,CIN,CIN2,NINP,Y(1),CJ,DCAP2)
      CJ=WP*CJ
      CALL SPLINT(VIN,IIN,GIN2,NINP,Y(1),IGJ,GJ)
C---DVD/DT
      DERY(1)=((VS-Y(1))/Z0-IGJ)/CJ
   40 RETURN
      END

      SUBROUTINE OUTP(X,Y,DERY,PRMT)

C---OUTP IS REQUIRED BY DRKGS AND IS USED TO OUTPUT THE RESULTS
C---OF THE INTEGRATION AT THE PROPER POINT ALONG AN LO CYCLE. WHEN
C---THE X VARIABLE IN THE DRKGS INTEGRATION REACHES THE END OF AN
C---INTERVAL OF LENGTH 1/(NPTS-1) THEN ALL THE WAVEFORM DATA (DIODE
C---CURRENTS AND VOTAGE) ARE SAVED IN DATA ARRAYS. OTHERWISE THE
C---INTEGRATION IS ALLOWED TO CONTINUE. THIS ROUTINE IS NEEDED SINCE
C---DRKGS AUTOMATICALLY HALVES AND DOUBLES THE INTEGRATION STEP SIZE
C---TO OBTAIN A GIVEN ACCURACY.
C---THE VARIABLE TYPES USED IN THIS SUBROUTINE ARE AS FOLLOWS:
C---FOR COMMON/CONST/:
      REAL*8 PI
      INTEGER NINP
C---FOR COMMON/DATA/:
      REAL*8 ICJDAT(51),IGJDAT(51),CJDATA(51),GJDATA(51)
      REAL*8 VDDATA(51),IDDATA(51)
C---FOR COMMON/DIODE/:
      REAL*8 RS,FP,WP,VIN(500),IIN(500),GIN(500),CIN(500),DCDVIN(500),
     +GIN2(500),CIN2(500),IGJ,ICJ,GJ,CJ
C---FOR COMMON/LOOPS/:
      INTEGER NH,NLO,JLO,NVLO,NPTS,NCURR,IPT,NPRINT,NITER
C---FOR VARIABLES NOT IN ANY COMMON BLOCKS:
      REAL*8 TX,X,Y(1),DERY(1),PRMT(5),DCAP2
C---THE COMMON BLOCKS USED ARE:
      COMMON/CONST/PI,NINP
      COMMON/DATA/ICJDAT,IGJDAT,CJDATA,GJDATA,VDDATA,IDDATA
```

```
      COMMON/DIODE/RS,FP,WP,VIN,IIN,GIN,CIN,DCDVIN,GIN2,CIN2,
     +IGJ,ICJ,GJ,CJ
      COMMON/LOOPS/NH,NLO,JLO,NVLO,NPTS,NCURR,IPT,NPRINT,NITER

C---TEST X TO SEE IF WE HAVE REACHED THE END OF AN INTERVAL
      TX=X-PRMT(1)-DFLOAT(IPT)*PRMT(3)
C---DON'T STORE ANYTHING IF THIS IS NOT THE END OF AN LO CYCLE INTERVAL
    1 IF(DABS(TX).GT.1.0D-7) GOTO 6
C---INCREMENT THE LO CYCLE INTERVAL COUNTER
    2 IPT=IPT+1
C---FIND THE DIODE CAPACITANCE, CONDUCTANCE AND THE CURRENT COMPONENTS.
      CALL SPLINT(VIN,CIN,CIN2,NINP,Y(1),CJ,DCAP2)
      CJ=CJ*WP
      CALL SPLINT(VIN,IIN,GIN2,NINP,Y(1),IGJ,GJ)
      ICJ=DERY(1)*CJ
C---SAVE THE LAST POINT (NPTS) AS THE FIRST LO CYCLE POINT.
      IF(IPT-NPTS-1) 3,4,6
    3 VDDATA(IPT)=Y(1)
      IDDATA(IPT)=IGJ+ICJ
      IGJDAT(IPT)=IGJ
      ICJDAT(IPT)=ICJ
      GJDATA(IPT)=GJ
      CJDATA(IPT)=CJ
      GOTO 6
    4 VDDATA(1)=Y(1)
      IDDATA(1)=IGJ+ICJ
      GJDATA(1)=GJ
      CJDATA(1)=CJ
      IGJDAT(1)=IGJ
      ICJDAT(1)=ICJ
    6 CONTINUE
   40 RETURN
      END

      SUBROUTINE DFORIT(FNT,N,M,A,B,IER)

C---DFORIT IS A DOUBLE PRECISION VERSION OF FORIT, AN IBM SSP ROUTINE
C---THAT PERFORMS A FOURIER ANALYSIS ON A PERIODIC FUNCTION.
C---IT COMPUTES THE COEFFICIENTS OF THE TERMS IN THE SERIES WHICH
C---IS GIVEN BY: A(1)+SUM(A(N)COS((N-1)X)+B(N)SIN((N-1)X)) N=2,3,4...
C---NOTE THAT THESE SINGLE ENDED SERIES COEFFICIENTS MUST BE CONVERTED
C---INTO THEIR EQUIVALENT COMPLEX DOUBLE ENDED FOURIER COEFFICIENTS
C---FOR USE IN THE REST OF THE ANALYSIS. IN DOING SO A(N) BECOMES A(N)/2
C---AND B(N) BECOMES -B(N)/2 FOR N>1. FOR N=1, A(N) REMAINS UNCHANGED
C---SINCE THE FACTOR OF 1/2 IS ALREADY INCLUDED IN THE VALUE RETURNED
C---BY THIS ROUTINE (SEE LABEL 100).

C---THE PARAMETERS USED ARE:
C---FNT/: TABULATED VALUES OF THE FUNCTION TO BE ANALYSED
C---       NOTE THAT FNT(1) CORRESPONDS TO TIME T=0
C---M/: THE MAXIMUM ORDER OF THE HARMONICS TO BE FITTED
C---N/: DEFINES THE INTERVAL OVER WHICH THE POINTS ARE TAKEN. THE
C---    INTERVAL GOES FROM 0 TO 2*PI AND 2N+1 POINTS ARE TAKEN AS DATA.
```

```
C---A/: THE FOURIER COSINE COEFFICIENTS
C---B/: THE FOURIER SINE COEFFICIENTS
C---IER/: THE RESULTANT ERROR  MESSAGE CODE WHERE IER=0 MEANS NO ERROR,
C---      IER=1 MEANS N IS LESS THAN M,  IER=2 MEANS M IS LESS THAN 0

      REAL*8 A(1),B(1),FNT(1),CONST
      REAL*8 COEF,C,S,C1,S1,AN,FNTZ,U0,U1,U2,Q
      INTEGER N,M
      IER=0
   20 IF(M) 30,40,40
   30 IER=2
      RETURN
   40 IF(M-N) 60,60,50
   50 IER=1
      RETURN
   60 AN=N
      COEF=2.0D0/(2.0D0*AN+1.0D0)
      CONST=3.14159265358979D0*COEF
      S1=DSIN(CONST)
      C1=DCOS(CONST)
      C=1.0D0
      S=0.0D0
      J=1
      FNTZ=FNT(1)
   70 U2=0.0D0
      U1=0.0D0
      I=2*N+1
   75 U0=FNT(I)+2.0D0*C*U1-U2
      U2=U1
      U1=U0
      I=I-1
      IF(I-1) 80,80,75
   80 A(J)=COEF*(FNTZ+C*U1-U2)
      B(J)=COEF*S*U1
      IF(J-(M+1)) 90,100,100
   90 Q=C1*C-S1*S
      S=C1*S+S1*C
      C=Q
      J=J+1
      GO TO 70
  100 A(1)=A(1)*0.5D0
      RETURN
      END

      SUBROUTINE PRINT1(ZEMB,ZERDC,ZEMBDC,ZER,ZEI,PRMT,Y,
     1DERY,VDBIAS,NHARM,NHD2)

C---PRINT1 WRITES THE VALUES OF THE INPUT VARIABLES AND THE INITIAL
C---CONDITIONS FOR THE NONLINEAR ANALYSIS SECTION OF THE PROGRAM.  ITS LISTING
C---HAS BEEN OMITTED FOR BREVITY

       SUBROUTINE SPLINE(X,Y,N,YP1,YPN,Y2)
```

```
C---THIS SUBROUTINE IS LISTED IN APPENDIX II AND IS THUS OMITTED HERE.  IN THIS
C---CASE NO COMMON BLOCKS ARE USED.

      SUBROUTINE SPLINT(XA,YA,Y2A,N,X,Y,Y1,NSP)

C---THIS SUBROUTINE IS LISTED IN APPENDIX II AND IS THUS OMITTED HERE.  IN THIS
C---CASE NO COMMON BLOCKS ARE USED.

      SUBROUTINE CALBIAS(VDO,IDO,ZERDC,RS,ZO,VDCMLT,VDBIAS)

C---CALBIAS CALCULATES THE ACTUAL DC VOLTAGE WHICH SHOULD BE APPLIED
C---TO THE MULTIPLIER IN ORDER TO OBTAIN THE DIODE RECTIFIED CURRENT
C---CALCULATED IN THIS PROGRAMME.

      REAL*8 VDO,IDO,ZERDC,RS,ZO,VDCMLT,VDBIAS
      VDCMLT=IDO*(ZERDC+RS-ZO)+VDBIAS
      RETURN
      END

      SUBROUTINE ZEMBED(ZER,ZEI,FP,NH)

C---THIS SUBROUTINE TRANSFORMS MEASURED LOAD IMPEDANCES THROUGH
C---AN EQUIVALENT CIRCUIT OF THE E10/A PACKAGE AND 3.5mm COAXIAL MOUNT
C---AS OBTAINED IN CHAPTER 3.  IT THEREFORE CALCULATES THE EMBEDDING
C---IMPEDANCES AT THE PUMP FREQUENCY AND ITS HARMONICS.

C---FOR COMMON/CONST/:
      REAL*8 PI
      INTEGER NINP
C---FOR COMMON/MNTPKG/:
      REAL*8 C(4),L(4)
C---FOR COMMON/ZMEAS/:
      COMPLEX*16 ZM(16)
      REAL*8 CC1,CC2,LW
C---THE COMMON BLOCKS USED ARE:
      COMMON/CONST/PI,NINP
      COMMON/MNTPKG/C,L
      COMMON/ZMEAS/ZM,CC1,CC2,LW
C---VARIABLES NOT IN ANY COMMON BLOCKS:
      INTEGER NF
      REAL*8 FP,W,ZER(16),ZEI(16)
      COMPLEX*16 Z(0:4),JW

      DO 1 NF=1,NH
      JW=DCMPLX(0.D0,1.D0)*DFLOAT(NF)*FP*2.0D0*PI
      Z(0)=ZM(NF)
      DO 2 J=2,1,-1
      Z(3-J)=JW*L(J)+(JW*C(J)+Z(2-J)**(-1))**(-1)
    2 CONTINUE
      ZER(NF)=DREAL(Z(2))
      ZEI(NF)=DIMAG(Z(2))
    1 CONTINUE
      RETURN
      END
```

```
      SUBROUTINE DATAIN

C---INPUTS ALL THE REQUIRED DATA FOR THE NONLINEAR ANALYSIS.

      CHARACTER*70 TITLE
C---FOR COMMON/CONST/:
      REAL*8 PI
      INTEGER NINP
C---FOR COMMON/DIODE/:
      REAL*8 RS,FP,WP,VIN(500),IIN(500),GIN(500),CIN(500),DCDVIN(500),
     +GIN2(500),CIN2(500),IGJ,ICJ,GJ,CJ
C---FOR COMMON/IMPED/:
      REAL*8 LOPWR,ZER(16),ZEI(16),ZERDC
C---FOR COMMON/LOOPS/:
      INTEGER NH,NLO,JLO,NVLO,NPTS,NCURR,IPT,NPRINT,NITER
C---FOR COMMON/RKG/:
      REAL*8 ACC,VDINIT
      INTEGER NDIM
C---FOR COMMON/TLINE/:
      REAL*8 Z0,ZQACC
      INTEGER ZQFLAG
C---FOR COMMON/VOLTS/:
      COMPLEX*16 VR(16)
      REAL*8 VRDC,VLO,VDBIAS,IDBIAS,BIAS(1000)
      INTEGER NBIAS
C---FOR COMMON/MNTPKG/:
      REAL*8 C(4),L(4)
C---FOR COMMON/ZMEAS/:
      COMPLEX*16 ZM(16)
      REAL*8 CC1,CC2,LW
C---FOR COMMON/PUMP/:
      INTEGER NPUMP
      REAL*8 PMPPWR(200)
C---FOR COMMON/MULT/:
      INTEGER NIN,NOUT
      REAL*8 PAVAIL,PABS,POUT
C---FOR VARIABLES NOT IN ANY COMMON BLOCKS:
      REAL*8 ZR,ZI,VSTART,VSTOP,VSTEP
C---THE COMMON BLOCKS USED ARE:
      COMMON/CONST/PI,NINP
      COMMON/DIODE/RS,FP,WP,VIN,IIN,GIN,CIN,DCDVIN,GIN2,CIN2,IGJ,ICJ,
     +GJ,CJ
      COMMON/IMPED/LOPWR,ZER,ZEI,ZERDC
      COMMON/LOOPS/NH,NLO,JLO,NVLO,NPTS,NCURR,IPT,NPRINT,NITER
      COMMON/RKG/ACC,VDINIT,NDIM
      COMMON/TLINE/Z0,ZQACC,ZQFLAG
      COMMON/VOLTS/VR,VRDC,VLO,VDBIAS,IDBIAS,NBIAS,BIAS
      COMMON/MNTPKG/C,L
      COMMON/ZMEAS/ZM,CC1,CC2,LW
      COMMON/PUMP/NPUMP,PMPPWR
      COMMON/MULT/NIN,NOUT,PAVAIL,PABS,POUT
```

```
C---OPEN INPUT FILE
      OPEN(5,FILE='rtd523b.dat',STATUS='OLD')
C---VARIABLES ARE INITIALIZED AS FOLLOWS:

      PI=3.14159265358979D0
C---LOOP LIMITS
      READ(5,'(a70)') TITLE
      READ(5,*) NH,NLO,NPTS,NCURR,NVLO,NITER,NPRINT
C---MULTIPLIER VARIABLES
      READ(5,'(A70)') TITLE
      READ(5,*) NIN,NOUT
C---RKG VARIABLES
      READ(5,'(a70)') TITLE
      READ(5,*) VDINIT,ACC,NDIM
C---CONVERGENCE PARAMETERS
      READ(5,'(a70)') TITLE
      READ(5,*) Z0,ZQACC
C---BIAS SETTINGS
      READ(5,'(a70)') TITLE
      READ(5,*) NBIAS
      DO 1 I=1,NBIAS
    1 READ(5,*) BIAS(I)
      READ(5,*) VSTART,VSTOP,VSTEP
      BIAS(1)=VSTART
      IF (VSTEP.EQ.0.0D0) THEN
      NBIAS=1
      ELSE
      NBIAS=ABS(IDINT((VSTOP-VSTART)/VSTEP)+2)
      DO 1 I=2,NBIAS
    1 BIAS(I)=BIAS(I-1)+VSTEP
      ENDIF
C---PUMP SETTINGS
      READ(5,'(a70)') TITLE
      READ(5,*) FP
      READ(5,*) NPUMP
      DO 2 I=1,NPUMP
   2  READ(5,*) PMPPWR(I)
C---PACKAGE AND MOUNT PARASITICS
      READ(5,'(a70)') TITLE
      DO 3 I=1,2
    3 READ(5,*) C(I),L(I)
C---MEASURED IMPEDANCES
      READ(5,'(a70)') TITLE
      READ(5,*) ZERDC
      DO 4 I=1,NH
      READ(5,*) ZR,ZI
    4 ZM(I)=DCMPLX(ZR,ZI)
C---DIODE DC DATA
      READ(5,'(a70)') TITLE
      READ(5,*) RS
      READ(5,*) NINP
```

```
      DO 5 I=1,NINP
      READ(5,*) VIN(I),IIN(I),GIN(I),CIN(I),DCDVIN(I)
    5 CONTINUE

      CLOSE(5)
      RETURN
      END
```

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