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**Design and testing of a new microprocessor-based current differential protection scheme for teed circuits**

Husseini, A. H.

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# DESIGN AND TESTING OF A NEW MICROPROCESSOR-BASED
# CURRENT DIFFERENTIAL PROTECTION
# SCHEME FOR TEED CIRCUITS

Submitted by  A.H. Husseini

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## SYNOPOSIS

The advantages of employing microprocessors in protective relaying for Power Systems are well known and a number of digitally based schemes are now available for protecting EHV plain feeders. Teed circuits are more difficult to protect than plain feeders and although differential protection is generally regarded as the method best suited to such circuits, however it is only recently that it has become feasible to be able to develop new high speed digital techniques for fault detection on such lines using Current Differential Principles. This has been made possible due to two main reasons which are:

1) the advent of fibre optical communication channels

2) the advancements made in high speed digital signal processing (DSP) chips.

This thesis describes in some detail the developments undergone in the design and building of the hardware for an EHV teed feeder protection scheme based on previously developed CAD techniques. The relay operating principle involves an advanced differential scheme based on Master and Slave principles. It utilizes wide-band fibre optic links for data transmission and signalling between local and remote ends. Novel techniques of digital processing and filtering along with their dedicated hardware are explained together with a sophisticated decision process. The relay has been tested in the laboratory using fault simulated current waveforms which are generated on a local programmable transmission line (PTL).

The relay offers a high performance and has various advantages over existing differential schemes, such as immunity to the presence of feed-around paths and CT saturation and an increased sensitivity to high resistance faults. Its operating times for a majority of faults are in the range of 4 to 6 ms.

The thesis clearly shows that the relay design based on CAD techniques can be engineered into practical model using DSP technology and this is vividly demonstrated by the very close correspondance between the Differtential and Bias signal waveforms attained from the practical and theoretical models.

# ACKNOWLEDGEMENTS

# LIST OF SYMBOLS

| | |
|---|---|
| $K_I$ | Current scaling factor |
| $K_S$ | Threshold voltage |
| CDP | Current differential protection |
| CT | Current transformer |
| P/M | Phase to modal transformation |
| FOL | Fiber optic link |
| EHV | Extra high voltage |
| CAD | Computer aided design |
| DSP | Digital signal processing |
| HS | High speed |
| CIM | Current interface module |
| Op | Operate signal |
| $\Delta T$ | Sampling interval used in descrete processing |
| Co, Cn | Software counters |
| ARO, AR1 | Hardware counter |
| N | Integer number |
| Quntom | One quantization level |
| $z^{-1}$ | Z-transform |
| S/H | Sample and hold |
| MUX | Multiplexer |
| A/D | Analog/Digital Converter |
| D/A | Digital/Analog Converter |
| DC | Direct current |
| $T_F$ | Point of fault |
| v(t) | Instantaneous value of system primary voltage |

| | |
|---|---|
| $i(t)$ | Instantaneous value of system primary current |
| $D_{1,2}(t)$ | Differential signals |
| $B_{1,2}(t)$ | Bias signals |
| $SD_{1,2}(t)$ | Superimposed Differential signals |
| $SB_{1,2}(t)$ | Superimposed Biased signals |
| DAS | Data acquisition unit |
| RAM | Random access memory |
| ROM | Read only memory |
| EVM | Evaluation module |
| PC | Programmable counter |
| I/O | Input/Output ports |
| EOC | End of conversion |
| S/C | Start of conversion |
| C/T | Conversion time |
| CLKOUT | Processor clock |
| CPU | Central Processing Unit |
| INT | Interrupt signal |
| RS | Reset signal |
| BIO | Branch on I/O |
| CS | Chip select |
| RD or IN | Read a digital value to the data ram |
| WR or OUT | Write a digital value to a peripheral device |
| LSB | Least significant bit |
| MSB | Most significant bit |
| PTL | Programmable transmission line |
| P/S | Parallel/serial converter |
| S/P | Serial/parallel converter |

DMPX          De-multiplexer

E/O           Electric/Optical conversion

O/E           Optical/ Electric  conversion

# CONTENTS

# CHAPTER 1

## INTRODUCTION

## 1.1 DEVELOPMENTS IN MULTI-TERMINAL LINES PROTECTION

Three terminal lines, (teed-feeders), in which a tee connects new circuits into an existing transmission system, offer considerable economic advantages and environmental benefits over two-terminal lines for Extra High Voltage (EHV) power transmission. This is more so due to the fact that there is a natural conflict between the ever increasing demand for power on one hand and the great difficulty in obtaining right of way for constructing new EHV lines. Coupled with the later is also the very high cost of building new power stations. In this respect, a teed circuit offers a cheap and an attractive alternative. It is well known such lines are difficult to protect by using conventional unit and non-unit power system protection schemes [1,2,3]. These references present a detailed account of the difficulties and limitations involved in the protection of teed circuits in relation to distance protection based on impedance measuring principles.

Recently some researchers [4,5] have resorted to new digital techniques in impedance measurement which employ adaptive relaying. Adaptive relaying can be simply defined as a type of protection which permits and seeks to make adjustments to various protection functions in order to make them more attuned to prevailing power system conditions. This is often achieved by dynamically changing the

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relay settings to accommodate the most conceivable network conditions. Considerations of various problems encountered on impedance protection systems as applied to teed-feeders make such adaptive approach sometimes deficient since not all possible system contingencies can be anticipated during the design of the protection system.

Many researchers have tried to address the problems distance relays by researching into protection techniques based on directional comparison principles and travelling wave principles. Originally such techniques have been applied to two terminal lines and investigations into their application to multi-terminal lines have been under consideration for a number of years.

Estergalyos and Rajendra [6,7] have proposed several schemes based on forming signals from voltage and current travelling waves generated during a fault. Although, such schemes can offer high speed (HS) protection for teed-feeders, their performance has, however, been examined for only a limited number of system and fault conditions. In particular, little reference has been made to the so-called "feed-around" problem, where, due to the presence of circuits external to the teed-feeder circuit, certain internal faults may cause the current and voltage sensed at one end to be similar to those experienced under external fault conditions. Furthermore, due to the complex nature of travelling wave transients at points of discontinuities of teed circuits, these schemes are sometimes prone to mal-operation. A review of some of such schemes applicable to teed-feeders protection are presented in Chapter 2.

Current differential protection (CDP) offers many advantages over the aforementioned relays and its principle of operation avoids many of the constraints imposed on impedance, directional comparison and travelling wave protection systems. In their simplest form, the algorithms for CDP rely upon deriving two relaying quantities, a differential quantity (operating quantity) which is usually formed from the vector sum of phasor terminal currents and a bias quantity (restraining quantity) which can be formed in different ways. The later is used to improve the relay security particularly where a significant differential signal is generated under healthy conditions e.g. due to current transformer (CT) saturation or shunt capacitance charging current. Its choice is thus very important from a relay stability point of view.

CDP schemes require that information (usually currents) from all terminals of the zone being protected be instantaneously available at the relaying point and be combined with each other in an appropriate form to be used in specially developed relaying algorithms. Thus a proper communication channel is essential and necessary for correct relay operation. This requirement can be considered to be the main disadvantage of differential relaying over impedance based relaying due to its full dependency on sophisticated communication links for current data transmission. This is more so when transmission line distances involved are relatively long.

In the past, the application of CDP had been confined to short distance power transmission lines [8], primarily because of technical and economic limitations imposed on data transmission links available

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then. For example, electrical links, such as pilot-wire lines, suffer from temperature rise and signals transmitted over such channels are often corrupted due to electrical and electromagnetic interference. Their use results in delayed operating times and inaccuracy due to their low bandwidth capacity.

Many of the problems encountered in conventional CDP of circuits have thus in the past arisen from inadequate communication links, and inherent time delays introduced by extensive use of filtering, but the continuous advancement in high speed digital data communication links such as light fibre optic links (FOL'S), high speed dedicated microprocessors, and fast analogue and digital circuitry has had a great impact on power system protection and has made the use of current differential protection for longer lines attractive and economically viable. Such techniques can, in principle, be applied to engineer new current differential schemes which, relative to conventional methods, enable high speed teed feeder relaying to be reliably and discriminately achieved.

A considerable amount of work has been reported on the application of FOL's to two terminal lines [9,10,11,12] and Kitagawa, Sekine and Akimoto [13,14,15] have extended the principles to differential protection of Teed circuits using a wideband microwave and fibre optic link.

The limited studies presented, however, show a relatively slow relay operating time, low coverage of high resistance faults, and again no reference has been made to the feed-around problem. Some of the well

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Known differential protection algorithms which have been applied to three terminal lines are reviewed in Chapter 2.

Recent years have seen a great deal of interest in high speed digital protection schemes for EHV transmission systems based on new operating principles and there is now strong evidence to suggest that a solution to adequately protecting teed circuits lies in the development of such new techniques.

A computer aided design (CAD) study at Bath university has been under development for some years [16] and has laid the theoretical basis for the hardware development of a digitally based high speed current differential relay scheme for the protection of three terminal lines and this is the subject of this thesis. The work performed has clearly shown that the relay design based on CAD techniques can be engineered into a practical model using digital signal processing (DSP) technology.

The scheme is based on master and slave principles and utilizes wide-band FOL communication channels. The proposed FOL will be discussed in some detail in Chapter 7. The basic relay operating principle hinges upon deriving a Differential quantity and a Bias quantity using the instantaneous values of the modal currents [17,18] at the three ends.

The relay can be arranged to compare either the total time variation of the Differential and Bias modal currents or their superimposed components. In this scheme the phase currents at each end are

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transformed into modal values because of economic and technical reasons. Only the two aerial modal values are utilized as this requires the transmission of only two signal components and avoids the problems encountered when using the earth mode particularly in parallel line configurations [17]. This approach also avoids the blind spot problems sometimes encountered when using a single summated quantity.

Because of wide band-width of receptibility necessary to obtain a reduction in operating time in HS relaying, the spill output (under external faults and CT saturation) can contain a very significant amount of high frequency components which, in turn, can cause relay mal-operation. Thus, the implementation of a moving window averaging filter for both the Differential and Bias signals and the basis of a novel decision process, in which the magnitude and polarity of the relaying signals are checked over a number of samples using a specially developed decision logic algorithm, is described.

Since this relay also makes use of superimposed components which are simply the difference between the total time variations of the signals and projections of their steady-state values, any deviation in power frequency from its nominal value during abnormal conditions such as load shedding can result in significant increase in the relaying signals. Hence a novel technique in frequency tracking to synchronize the sampling rate with the fundamental frequency is also described.

The results presented clearly show that there is a close

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correspondence between the results obtained from the practical and theoretical models of the relay. The special filtering and signal processing techniques developed in the software algorithm enable the relay to operate in the presence of transients and provides dynamic stability for external faults (both with and without a degree of CT saturation), without affecting its HS capability for internal faults. Tripping times of the order 4-6 ms for most practically encountered faults are obtained and it is shown that the relay version employing superimposed modal currents provides a much better high resistance fault coverage than that utilizing total time variation modal currents, this being so by virtue of the higher relay sensitivity possible when using the former.

## 1.2 OBJECTIVES

The main objectives of this thesis are:

**a)** to present the design and engineering of the proposed CDP scheme, operating to HS specification, using modern digital techniques and special purpose dedicated hardware and therefore to address any problems (such as those caused by practical noise) which are not apparent in the CAD design. Hardware technical description and theory of operation of the relay modules including, data acquisition unit (DAS), analog and digital filtering and software for the central processing unit (TMS32010) written in assembly will be introduced.

**b)** to establish the correct performance of the engineered equipment under most conceivable fault disturbances which can occur

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on some typical 400 kV teed circuit configurations. The verification

process comprises undertaking exhaustive laboratory testing using

simulated power system fault waveforms from a programmable

transmission line (PTL), the results and comparison with the CAD

scheme and conclusions are presented.

c) to lay the basis and make suggestions as to how the prototype

relay can be further improved.

## 1.3    SCOPE OF THE THESIS

Chapter 2

The most common teed-feeder protection algorithms with their merits

and demerits are described, the emphasis being on those implementing

the current differential principles, and superimposed components.

Also some of the schemes based on travelling-wave principles which

can be applied to teed circuits are introduced.

Chapter 3

The underlying and operating principles of the prototype relay are

outlined. Superimposed component extraction filter including its,

configuration and frequency response are discussed. A low pass

moving window filter which has been applied to the relaying signals

is described. Effect of power frequency deviation from its nominal

value on the extraction filter response, its implication on the relay

performance, concept of frequency tracking and its implementation are

explained.

Chapter 4

In this Chapter technical and functional descriptions of different
hardware modules of the relay with a special attention to the
interface of the data acquisition unit with the TMS32010
microprocessor are presented. Novel techniques in digital hardware
design, Efficient accessing of the external data RAM, and an
adaptive sampling rate control circuit are also described.

Chapter 5

Methods of reducing computational time of the algorithms and
optimization of the software routines are outlined. Due to the
restrictions imposed by the time available between samples at 4 kHz
sampling rate, assembly language and fast filtering techniques are
outlined.

Chapter 6

The laboratory testing system is briefly described with the aid of a
flow chart. Methods of testing are outlined. Arbitrary sinusoidal
waveforms of different amplitude and frequency are used to asses the
filter frequency response. Since single phase to earth faults are
the most common types which may be encountered on a transmission
line, the majority of tests to assess relay performance are carried
out for such faults. Internal and external fault simulated transient

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waveforms for different fault inception angles, fault position and different teed-feeder configurations are used to test the performance of the relay. Special attention is given to relay performance under (CT) current transformer saturation, for teed-feeder configuration with a feed-around path and for high resistance faults. Comparison of the results with those obtained from the simulation (CAD) study is performed.

Chapter 7

An invistigation into the digital data communication scheme based on fibre optic link for data transmission and signalling with the necessary synchronization is presented.

Chapter 8

The work described in this thesis is summarised, with conclusions. It also includes suggestions for future work to enhance the relay performance by the use of a new version microprocessor of the TMS family, and a plan is made as how the interaction between the remote ends and the master end can be achieved through optic fibre communication link.

CHAPETER  2


REVIEW OF TEED FEEDERS PROTECTION ALGORITHMS


## 2.1  INTRODUCTION

Considerable work has been done on developing digital algorithms for teed circuit protection mainly by modifying already existing algorithms developed for two terminal lines. These algorithms can be divided into three categories which are:

a)  distance protection algorithms based on  impedance  measurement

b)  algorithms based on travelling wave principles

c)  differential protection algorithms mostly based on terminal currents.


## 2.2. DISTANCE RELAYING ALGORITHMS

In conventional relays, many numerical techniques can be used to calculate the apparent impedance between a fault and relay location. These include  curve fitting techniques such as, least square error and sinusoidal curve fitting. Furthermore there are the well known methods which calculate the impedance by predicting the peak values of  the current and voltage waveforms presented to the relay assuming the signals to be sinusoidal, and the differential equation algorithms  based on Fourier series. The application of impedance measurement algorithms to teed feeders has many drawbacks such as:

a) *Fault location with respect to position of tee point:*

Consider the teed circuit line diagram shown in Fig. 2.1-a. The effect of moving the tee position from position close to end A (T) to a position close to end B (T') is to change the true impedance seen by the relay at end A for a fault at point F.

**b)** *Different arm lengths:*

Considering the teed circuit line diagram shown in Fig. 2.1-b. If the length of the arm TC is much longer than the arm TB, then the first zone coverage of line AB between ends A and B by a relay positioned at end A will protect only a small part of TC. An extended second zone will reach beyond the bus at B and may give false tripping for a fault outside the protected zone.

**c)** *Current infeed from other sources:*

Consider Fig. 2.1-c. The value of apparent impedance $Z_A$ (between end A and the fault location) seen by a relay located at end A for a fault at F will be given as:

$$Z_A = Z_{AT} + Z_{TF} (1 + \frac{I_B}{I_A}) \qquad (2.1)$$

where $Z_{AT}$ = the line impedance between end A and the T-point

$Z_{TF}$ = the line impedance between the T-point and the fault

$I_A$, $I_B$ = the line currents at ends A and B respectively

The effect of current infeed from terminal B will cause the relay to under-reach or over-reach depending on whether $I_B$ increases or decreases.

**d)** *External fault on a parallel branch:*

In double circuit lines, an external fault on a parallel branch

causes a relay to over-reach i.e. it sees a lower impedance than the base impedance it was originally set to.

Some remedy for these contingencies can be provided by incorporating blocking features through signalling between the three ends. To confine tripping to within the boundaries of teed interconnection, additional relays to inhibit protection operation through signalling channels during external faults have to be provided. Recently some authors [4,5] have proposed the concept of adaptive relaying to improve the reliability of impedance relays. Adaptive multi-terminal relay coverage can account for changes in infeed ratios, and the coverage can be improved by either increasing or decreasing reach when infeed is present. With this approach relay settings can also adapt to changes in the current distribution resulting from external power system changes.

## 2.3  PROTECTIVE SCHEMES BASED ON TRAVELLING WAVE PRINCIPLES

These schemes utilize information derived from travelling waves set up by disturbances on EHV transmission lines to achieve high speed fault clearance. Using the travelling wave concept [17,18,19,20] and observing the sign of the voltage wave with respect to the current wave or their superimposed components immediately after a fault, a directional discrimination to the fault can be determined. Also comparing the magnitudes of the forward incident wave and reverse wave in the time domain, the distance to a fault can be estimated. Originally, most travelling wave schemes have been developed to protect two terminal lines. Estergalyos [6] however, has extended the

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principles of travelling wave theory for the protection of teed-feeders. In this scheme, the voltage and current waves on a transmission line are linked together by the characteristic impedance of the line $Z_c$, as shown in the equation:

$$V = \pm I.Z_c \qquad (2.2)$$

The travelling wave theory can be usefully applied for relaying purposes by observing the sign of the voltage wave with respect to the current wave immediately after fault inception. An internal fault causes the voltages and currents at the three ends to be of opposite polarities at all the three terminal ends, whereas an external fault will indicate same polarities at the relay terminal closest to the fault. The above directional criterion coupled with the fact that the waves will be damped as they move along the line, enables a selective fault discrimination to be achieved by introducing an amplitude criterion on the current and voltage waves. To avoid confusion that could arise by multiple reflections of the incident waves, the relay at each terminal detects the first wave which reaches its direction of motion and then locks to that decision. In this scheme communication links between all terminals have to be adopted and a tripping signal is initiated if the aforementioned conditions for an internal fault are met. If the fault is external the relay closed to the fault will issue a blocking signal.

Rajendra and Mclaren [7] have proposed a teed circuit protection scheme based on superimposed components of current and voltage travelling waves. It is based on suppressing the voltage and current

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prefault values from postfault values. Removing the prefault power frequency component in general compresses the dynamic range of the signals to be processed and enhances the magnitude of travelling wave components in relation to the power frequency components. In this scheme, the voltage and current waves are decomposed into forward and backward travelling wave components and two composite signals, a forward signal $(S_f)$ and reverse signal $(S_r)$ can be formed as:

$$S_f(t) = v(t) + Z_c.i(t)$$
$$S_r(t) = v(t) - Z_c.i(t) \qquad (2.3)$$

When a fault occurs, the initial current and voltage approaching the local relay are related by:

$$i_r(t) = -\frac{v(t)}{Z_c} = -i(t) \qquad (2.4)$$

whereas for the initial surge moving away from the local relay, they are related by:

$$i_f(t) = +\frac{v(t)}{Z_c} = +i(t) \qquad (2.5)$$

The basic relay principle is based on the fact that when an incident wave $S_r$ exceeds a preset threshold setting, it initiates a distance algorithm which ascertains if the fault is within the local distance reach. The distance algorithm relies on polarity change criterion which enables the local end relay to distinguish between a fault on the local branch and that on one of the other tee branches by sensing the first and the second reverse travelling wave (Eqn. 2.3). The scheme incorporates local distance relays at the three ends designed to under-reach and uses communication links to transfer information

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between these relays to provide direct intertrip.

It is well known that although protection schemes based on travelling wave principles can provide HS fault clearance, their application to teed circuits is, however confined to only certain types of configurations. For example, their performance is unsatisfactory when one leg of the tee is very short making it virtually impossible, from a practical point of view, to be able to detect the transient times between reflections. Also when an external feed around path is present, there can be a reversal in the direction of current flow in one of the tee branches.

## 2.4 DIFFERENTIAL PROTECTION APPLIED TO TEED-FEEDERS

A few schemes based on differential protection principles have been proposed over the last decade [11,12,13,15,21,22]. A brief description for the operating principles of some of the existing schemes applicable to teed-feeder protection is presented.

### 2.4.1 Differential algorithms based on phasor relaying

Kwong et al [21] have proposed a current differential relay for protection of teed-feeder based on the principle of master and slave terminals. The sampling of the current signals at each end is controlled by a free running clock. Interpolation method has been used to predict the actual value of the sample at the slave end corresponding to the same time at the local end by taking into account the propagation delay over the communication channel. The transient embedded current waveforms have been sampled by using the

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one cycle window Fourier method. This process can be achieved by correlating the current data samples with stored samples of reference fundamental, sine and cosine waveforms. In numerical form, the algorithm is expressed as:

$$I_s = \frac{2}{N} \sum_{k=1}^{N-1} \sin(\omega k T_s) \cdot i(n-kT_s) \tag{2.6}$$

$$I_c = \frac{2}{N} \left( \frac{i_0}{2} + \frac{i_N}{2} + \sum_{k=1}^{N-1} \cos(\omega k T_s) \cdot i(n-kT_s) \right) \tag{2.7}$$

where  T = the sampling interval

N = the number of samples per cycle

k = integer number

W = fundamental angular frequency

$i_n$ = instantaneous value of signal i sampled at time n

$I_s$ = Fourier sine integral of signal i

$I_c$ = Fourier cosine integral of signal i

Given the vector components $I_s$ and $I_c$ of a current signal i, the amplitude $|I|$ is equal to:

$$|I| = \sqrt{I_s^2 + I_c^2} \tag{2.8}$$

If $I_A$, $I_B$, $I_C$ are the current vector signals measured at the three terminal ends  A, B, C  of a teed feeder, then the differential current $I_{diff}$ and the bias current $I_{bias}$ are :

$$I_{diff} = I_A + I_B + I_C$$

$$I_{bias} = \frac{1}{2} \left( |I_A| + |I_B| + |I_C| \right) \tag{2.9}$$

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A percentage biased differential characteristic is used and the tripping criterion is :

$$|I_{diff}| \quad > \quad K_b . \; |I_{bias}| \qquad\qquad (2.10)$$

where $K_b$ = percentage bias setting.

This relay has been designed to work with communication links which have wide bandwidth of 64 kbits/s and above. Eight samples per cycle have been used and its average operating time is about 26 ms.

## 2.4.2   Differential protection based on time variation comparison of terminal currents

Akimoto et al [15]  have developed a percentage differential protection system for teed feeders, in which a separate protection is provided for each phase. The operating quantity is the vector sum of terminal currents for a particular phase and the restraining quantity is proportional to the scalar sum of the currents for the same phase and the operating criterion is given as:

$$| \; I_1 + I_2 + I_3 \; | - K_1 . \; ( \; | \; I_1 \; | + | \; I_2 \; | + | \; I_3 \; | \; ) - K_0 > 0 \qquad (2.11)$$

where : $I_1$, $I_2$, $I_3$ are terminal current values for the phase being protected.

$K_1$   is the percentage bias ratio.

$K_0$   is a threshold value.

Sanderson et al   [22] have improved the performance of the scheme

proposed by Akimoto. The basic operating principle is amplitude comparison as above but the operating and restraining quantities are derived from incremental fault currents following a disturbance, by removing the initial load currents. The operating quantity is the vector summation of the incremental currents for each phase, but the restraining quantity is the maximum of each terminal current for the particular phase being protected. The method is such that for an internal fault, the fault current will exceed the largest of the terminal currents, but for an external fault condition, the vector sum of terminal currents will be less than the maximum of the terminal currents.

The operating criterion can be represented as:

$$| \, dI_1 + dI_2 + dI_3 \, | \; > \; \text{Max} \, (|dI_1|, \; |dI_2|, \; |dI_3|) \qquad (2.12)$$

where d indicates an incremental current which is the superimposed current due to a fault . This incremental current has been derived by subtracting the one cycle delayed prefault current value from the present current value as below:

$$dI \; = \; i(t) - i(t-T) \qquad (2.13)$$

where T is the period of power frequency.

In this scheme the amplitude of a certain phase current is calculated from its corresponding incremental wave form after its rectification by integrating over a half cycle window as follows:

$$|dI| \; = \; \sum_{j=k-n}^{j=k} |di_j| \qquad (2.14)$$

where $i_j$ is the jth sample of wave-form i, k is the sample number of the most recent sample and n is the number of samples in a half cycle of the fundamental frequency.

The scheme utilizes communication links for data transmission between the terminals of the teed-feeder and the average operating time is 20 ms.

It can be concluded from above that the differential schemes based on extracting the fundamental phasor components suffer from inherent time delay in their operation, and those based on amplitude comparison and incremental superimposed component principles, lack sensitivity firstly because the restraining quantity is arbitrarily chosen, and secondly because by considering the maximum phase load current as the restraining quantity, the relay is rendered to failure. This is particularly so in the case of a double circuit configuration where due to the mutual coupling effects, the bias would have to be high, resulting in a lower fault resistance coverage.
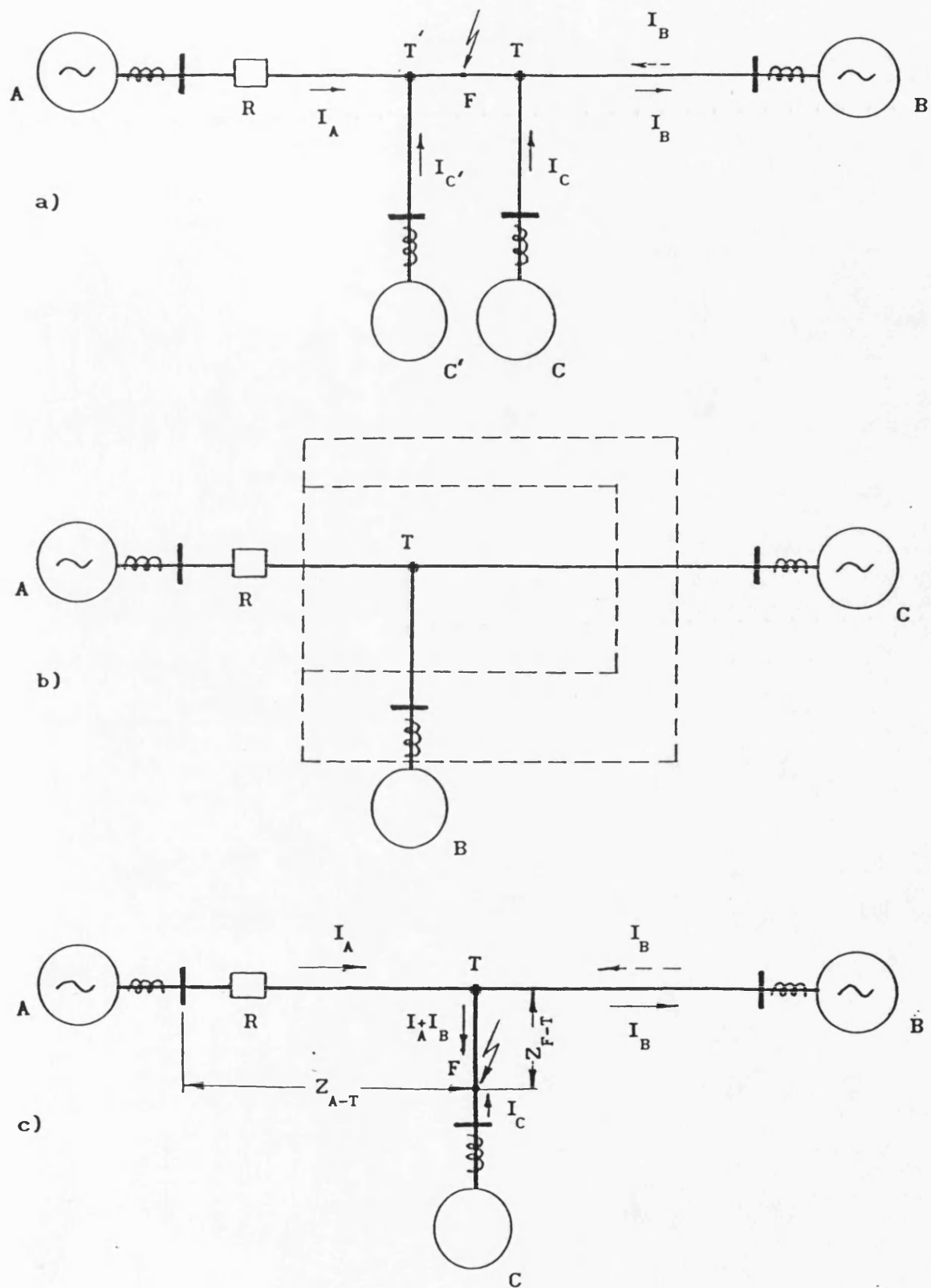
a) Effect of changing the T-point position

b) Effect of different arm length

c) Effect of different source capacities

Fig. 2.1 Drawbacks of impedance protection relays

CHAPTER 3

RELAY THEORETICAL DESIGN

## 3.1 INTRODUCTION

As mentioned previously in the introduction, the relay can be arranged to compare either the total time variation of the Differential and Bias signals or their superimposed components. Thus Before describing the relay operating principles, it is convenient to introduce the superposition concept, and its implication on the relay performance.

## 3.2 SUPERIMPOSED COMPONENTS CONCEPT

A fault occurrence on a transmission line can be considered as equivalent to superimposing a voltage at the point of fault which is equal and opposite to the prefault steady state voltage. The postfault voltage and current components may be considered as made up of the prefault steady-state components and fault injected components as follows:

$$Vpost = Vpre + \Delta V_f \qquad\qquad (3.1)$$

$$Ipost = Ipre + \Delta I_f \qquad\qquad (3.2)$$

Superimposed components $\Delta V_f$ and $\Delta I_f$ are simply the differences between the total time variation of the signals and a projection of their steady-state (pre-disturbance) values. They contain all the

essential information regarding the travelling wave components (that is if they are present) whose magnitude is considerably enhanced when the prefault signals are removed from the fault generated travelling waves. In the absence of any travelling waves i.e. for a fault near voltage minimum they are simply the postfault superimposed components minus the prefault values.

A protection relay algorithm based on superimposed components of signals rather than total variations has a number of distinct advantages over the former and they are:

a) faster operation

b) higher fault resistance coverage

c) immunity to errors caused by prefault loading

Advantages a) and b) are attained by virtue of the fact that the threshold levels associated with such a relay are lower. However, it has the disadvantage that the extraction of the superimposed components can introduce errors and a careful design of the digital extraction filter is therefore essential.


## 3.3 OUTLINE OF THE PROPOSED SCHEME

The CAD model of the complete protection scheme [16] with some essential modifications is shown in Fig. 3.1. The equipments at the slave end transmit local current data and receive any direct intertripping signal generated by the master end where the tripping decision is made. The output of the CT is passed through a current

interface module comprising one transformer-reactor and associated compensation circuits for each phase. This module is designed to have a constant current/voltage gain over a range of frequencies from approximately 0.1 Hz to 3 kHz. As such, it produces an output voltage which is proportional to the input current over the frequency range of receptability of the equipment the constant of proportionality being controlled by the gain constant $K_i$. The output voltage is limited by voltage clipping applied to the input so that the gain constant $K_i$ controls the maximum level of secondary current which is linearly converted. The later requirement is met by performing a simple steady-state study to determine the maximum possible external fault current for a particular tee configuration. The relay sensitivity setting factor $K_i$ has been chosen so that absolute stability for all external faults is guaranteed without sacrificing its sensitivity to low level internal faults.

The signal processing has been performed at 4 kHz and the pre-filter (PF) thus has a second-order low pass Butterworth characteristic with a 1.5 kHz cut-off frequency which is well within the limits to prevent aliasing. Some economy is gained by forming signals proportional to the aerial modes of currents (mode 1 and 2) rather than phase currents, as this requires the transmission and processing of only two signal components. This approach also avoids the blind spot problems sometimes encountered when using a single summated quantity.

The phase to modal transformation to form the two aerial mode signals is performed in unit P/M using simple analog signal differencing. The

transmission of the two modal signals from each of the remote ends at 4 kHz sampling rate and with an 11 bit word plus sign conversion requires a data transmission rate of at least 96 Kbits/s if the two signals are multiplexed. This transmission rate is the minimum required for the transmission of the modal current data only. The other information like parity check, code detection and error correction, circuit breaker status and other information, must be multiplexed with the current data. The sampling rate at the remote end can be provided either by a free running clock or by sending it from the master end . Synchronization between the local and remote clocks and delaying the local signals to compensate for the propagation time delays associated with the remote signals can be done inside the microcomputer by using digital delay filters. The reason behind implementing these filters is to avoid the necessity to increase the relay bias necessary to offset any increase in spill current as a result of data mismatch. Using a full duplex FOL link, a secure intertrip signal can be asserted at any slave end after a delay of typically 2 ms corresponding to modem delay and data transmission at the speed of light.

The functional processes performed in the equipment at the master end, are implemented in a 16/32 bit TMS32010 microcomputer using digital summation and difference functions. Fig. 3.1 shows that the final decision process can be applied to either the total time variation of the Differential and Bias signal or their superimposed components.

The superimposed components are extracted using specially developed

digital filters. The relaying signals are finally passed through a moving window averaging filter before the decision logic process is implemented. The final trip decision is asserted when either of the two modes satisfies the tripping criterion. A tripping signal resulting from the two modes is transmitted to the local and remote ends when there is an internal fault.

## 3.4  BASIC  OPERATING  PRINCIPLES

### 3.4.1  Differential and Bias signal formation

The relay operating principles  hinges upon deriving a Differential quantity $D(t)$ and a Bias quantity $B(t)$ proportional to the instantaneous values of the modal currents at the three ends. Consider first the simple single line diagram of Fig. 3.2. If $i_P(t)$, $i_Q(t)$, $i_R(t)$ are the instantaneous values of the CT secondary currents at terminals P, Q, and R respectively, then the two quantities $D(t)$ and $B(t)$ (for each mode)  at the master end are given in a continuous form by :

$$D_{1,2}(t) = i_{P1,2}(t) + i_{Q1,2}(t) + i_{R1,2}(t) \qquad (3.3)$$

$$B_{1,2}(t) = i_{P1,2}(t) - i_{Q1,2}(t) - i_{R1,2}(t) \qquad (3.4)$$

It is evident from Eqn. 1 that the particular combination considered gives a solution which is such that, under through fault conditions, the Differential signal $D(t)$ is very small and the Bias is of a relatively large value. Conversely, for internal faults, the Differential signal would be approximately equal to the fault path

current, and is large enough to cause tripping.

In its simplest form, the relay would operate for faults when the magnitude of the Differential quantity exceeds a percentage $K_B$ of the Bias by a certain pre-defined threshold value $K_S$ shown in:

$$\underbrace{\left|D_{1,2}(t)\right| - K_B\left|B_{1,2}(t)\right|}_{\longleftarrow \quad Op(t) \quad \longrightarrow} \geq K_S \qquad (3.5)$$

where Op(T) is the operate signal.

## 3.4.2 Bias constant $K_B$ and relay setting levels

These fixed levels have been largely determined by means of an extensive series of CAD studies so as to retain relay stability for the worst case out of zone fault and at the same time maintaining its HS quality for internal faults.

The basic sensitivity level setting $K_S$ must be sufficiently high to ensure that any noise in either the differential or bias signals is ignored. The principal noise sources are:

a)   Analog circuit noise and harmonics generated by the CT and current interface module including CT saturation

b)   Residual   Differential and Bias signal components caused by sampled   data   mismatch   due   principally   to   drifts   in   the compensation delays of the remote signals.

c)   Quantisation errors due to analog to digital conversion.

d)   Residual output resulting from the extraction filter due to the   deviation   of   power   frequency   from   its   nominal   value (this applies only to the relay based on superimposed components).

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A consideration of these factors, has led to the conclusion that the required settings should be 80 and 65 quantisation levels for the relay based upon total and superimposed components respectively. The lower setting associated with superimposed components is possible due largely to the steady-state harmonic rejection properties of the digital filter used. The high resolution 12 bit A/D converter used leads to a quantisation level of approximately 5mV and the resulting pick-up levels of 500 and 350 mV are well above the total noise levels expected. $K_B$ of 50% was largely determined by testing the relay response under conditions where the CT's are made to suffer a degree of saturation during high level external faults.

It should be mentioned that these levels are based purely on CAD studies and are therefore only used when assessing relay performance on a theoretical basis. However, as discussed later in Chapter 6 when testing the hardware model, the levels had to be raised in order to counteract the additional practical noise.

### 3.4.3 Phase to modal transformation

The relay phase quantities at each end of the teed-feeder are decoupled into three independent modal quantities using a transformation matrix Q. In this respect there are a number of transformations in use, but the one most suited to this relay particularly from relay stability point of view for certain types of external faults, is the Karrenbauer transformation given as:

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$$
\begin{vmatrix} I_0 \\ I_1 \\ I_2 \end{vmatrix} = \frac{1}{3} \begin{vmatrix} 1 & 1 & 1 \\ 1 & 0 & -1 \\ 1 & -1 & 0 \end{vmatrix} \cdot \begin{vmatrix} I_a \\ I_b \\ I_c \end{vmatrix} \qquad (3.6)
$$

$$
\longleftarrow Q^{-1} \longrightarrow
$$

For this relay, the protection algorithm is based only on the two Aerial modes. The use of the Earth mode is avoided as it can cause problems of relay instability on the healthy circuit in parallel line configurations.

Using the transformation in Eqn. 3.6 gives Eqns. 3.3 and 3.4 in an expanded form as:

For mode 1 we have

$$
D_1(t) = [I_{aP}(t) - I_{cP}(t)] + [I_{aQ}(t) - I_{cQ}(t)] + [I_{aR}(t) - I_{cR}(t)]
$$
$$(3.7)$$

$$
B_1(t) = [I_{aP}(t) - I_{cP}(t)] - [I_{aQ}(t) - I_{cQ}(t)] - [I_{aR}(t) - I_{cR}(t)]
$$
$$(3.8)$$

Similarly the relaying signals of mode 2 are given by :

$$
D_2(t) = [I_{aP}(t) - I_{bP}(t)] + [I_{aP}(t) - I_{bQ}(t)] + [I_{aR}(t) - I_{bR}(t)]
$$
$$(3.9)$$

$$
B_2(t) = [I_{aP}(t) - I_{bP}(t)] - [I_{aQ}(t) - I_{bQ}(t)] - [I_{aR}(t) - I_{bR}(t)]
$$
$$(3.10)$$

There are no fault conditions that in practice can simultaneously give rise to zero valued modal current signals, and tripping is

therefore initiated for internal faults by at least one modal signal.

### 3.4.4 Superimposed extraction filter

Fig. 3.3 shows the digital filter used for extracting the superimposed components. An extensive series of CAD studies [16,23] have shown that it is desirable to use a cascaded filter comprising a half-cycle and a full cycle of nominal power frequency delay. The first stage has a transfer function given by:

$$H_1(Z) = (1 + Z^{-m1}) \qquad\qquad (3.11)$$

where $Z = \exp(j\omega\Delta T)$, $\Delta T$ = sampling period

The delay which produces the superimposed output for a half-cycle of power frequency of period T is attained by setting the integer m1 equal to $\frac{T}{2\,\Delta T}$ . The first subfilter is seen to be such that a half-cycle of power frequency period delayed version of the input is added to the actual input at point A.

The second subfilter has a transfer function given by:

$$H_2(Z) = (1 - Z^{-m2}) \qquad\qquad (3.12)$$

The delay is made equal to one period of the nominal power frequency by setting the integer m2 equal to $\frac{T}{\Delta T}$ . It is arranged so that a one cycle delayed version of the input at A is subtracted from the present input at A. Thus for sampling frequency of 4 kHz, i.e $\Delta T = 0.25$ ms, the number of sample delays required in a 50 Hz application is such that m1 = 40 and m2 = 80 respectively, and the

cascaded filter response in the Z plane is given as:

$$I_0(Z)/ I_1(Z) = (1+ Z^{-40})(1- Z^{-80}) \qquad (3.13)$$

The half-cycle and full cycle filters when mapped from Z domain into frequency domain give frequency responses shown in Fig. 3.3-a, and Fig. 3.3-c. Their absolute magnitudes are derived as follows:

$$H_1(Z) = 1+ Z^{-m1} \qquad (3.14)$$

$$H_1(j\omega) = 1+ e^{-j\omega m1 \Delta T} = e^{-j\omega m1 \Delta T/2} e^{+j\omega m1 \Delta T/2} + e^{-j\omega m1 \Delta T/2}$$

$$\qquad (3.15)$$

$$|H_1(\omega)| = 2 \cos(\omega m1 \Delta T/2) \qquad (3.16)$$

Likewise we have:

$$|H_2(\omega)| = 2 \sin(\omega m2 \Delta T/2) \qquad (3.17)$$

The overall transfer function of the cascaded filter in the frequency domain is a direct multiplication of the two transfer functions and for 50 Hz power frequency it is given as:

$$|H(\omega)| = 4. \cos(\omega. 40. \Delta T/2). \sin(\omega. 80. \Delta T/2) \qquad (3.18)$$

As it can be seen from Fig. 3.3-a and Fig. 3.3-c the half-cycle delay filter attenuates the 50 Hz power frequency and its 'odd' harmonics, but there is a finite gain for DC and 'even' harmonics and this gain could reach to double the actual value. Using the full cycle extraction filter, DC and 50 Hz and 'odd' harmonics can be suppressed. In practice there is a problem in that the power system frequency is not constant and it may drift slowly in value as a result of mismatch between power supply and demand resulting in a residual component at the output of the filter. The arrangement of

the cascaded filter thus has the overall effect of reducing the residual components generated by any one of the two filters during frequency deviation from its nominal value (Fig. 3.4).

It is evident that the cascaded arrangement of Fig. 3.3-b produces any superimposed output for half a cycle of power frequency after a system disturbance. Beyond this time the output does not correspond exactly to the superimposed component. After the response time of 1.5 cycles, the output from the digital filters falls to near zero at a rate determined largely by the degree of symmetry attained by the Differential and Bias signals at the inputs. The one half cycle for which the output corresponds exactly to the superimposed value is more than sufficient for practical purposes because the protection algorithm can be executed and a trip decision made in an average time of approximately one quarter of power frequency cycle. Furthermore, the above mentioned decay of the output of the filters after the 1.5 cycle response time causes both the superimposed Bias and Differential signals to be nominally zero under healthy conditions. This is in marked contrast to the relay version that employs the total variations of the signals D(t) and B(t), because in this case the signals are always finite. Moreover in the former case, the signals only become finite on the inception of a disturbance. Furthermore, these signals are free from power system frequency harmonics which can be generated because of system and/or transducers non-linearities. This results in a scheme that is more stable and much more sensitive, in particular to high resistance earth faults.

### 3.4.5 Moving window average filter

During extensive testing of the relay under faults, variable threshold voltages were tried and it was concluded that in practice, for some high frequency embedded relaying signals, the threshold voltage had to be raised for the relay to produce a correct decision. This in turn would of course reduce the coverage of high resistive faults which produce low level relaying signals. However, the problem can be overcome by the implementation of a moving window digital filter to smooth the relaying signals before applying a decision process to them. This technique has a low pass filter effect because it attenuates the high frequency harmonics present in the signals, especially during external faults and current transformer saturation. Furthermore, it linearises the relaying signals and enables a lower threshold setting and therefore a higher fault resistance coverage to be achieved. The filter is applied to both the Differential and Bias signals derived for each mode, and its output is defined by:

$$Y_{iq}(K) = \frac{1}{M} \sum_{n=0}^{n=M-1} X_{iq}(k - n) \qquad (3.19)$$

where iq refers to $D_1$, $B_1$, $D_2$, $B_2$

$Y_{iq}(k)$ , $X_{iq}(k)$ are the present output and input respectively.

M is the length of filter

$X_{iq}(k - n)$ are the previous input samples,

where n = 1, 2,.....,M-1.    k = 0, 1,...

It has been found that a window length M of 8 samples gives

satisfactory performance.

The relatively small delay of the averaging filter on the operating time varies with the angle of inception of the fault and is more than adequately compensated for by being able to set a lower threshold level.


### 3.4.6 Decision logic process

The decision process operates on both the polarities and magnitudes of the filtered Differential and Bias relaying signals or their superimposed components as shown in Eqn. 3.5 so as to differentiate between an internal and external fault. The relative magnitudes of the two signals are of concern, since the Bias signal $B_{1,2}(t)$ is initially larger than $D_{1,2}(t)$ for prefault and external faults and the converse is true for a fault within the protected zone. However, as mentioned before, although these relaying signals are extensively filtered, they can still contain some significant transients. Also additional noise can be introduced by digital quantisation errors. The decision process therefore requires a degree of noise immunity and this is provided firstly, by comparing the operate signal $Op(t)$ (Eqn. 3.5) with a threshold value $K_s$ which must be exceeded before proceeding onto the next stage. Secondly, in order to give the process some immunity against the presence of any short duration spikes, apart from satisfying the first criterion, $Op(t)$ must also be of the same polarity over a consequtive number of samples, before any tripping decision can be initiated. A detailed description of the decision logic counter will be given in Chapter 6.

An extensive series of studies have revealed that if the aforementioned criteria are satisfied over four consecutive samples to effectively increment the decision counter by 1 and a trip decision is made when the counter attains a level of 4, then this approach is satisfactory for a majority of practically encountered fault conditions.
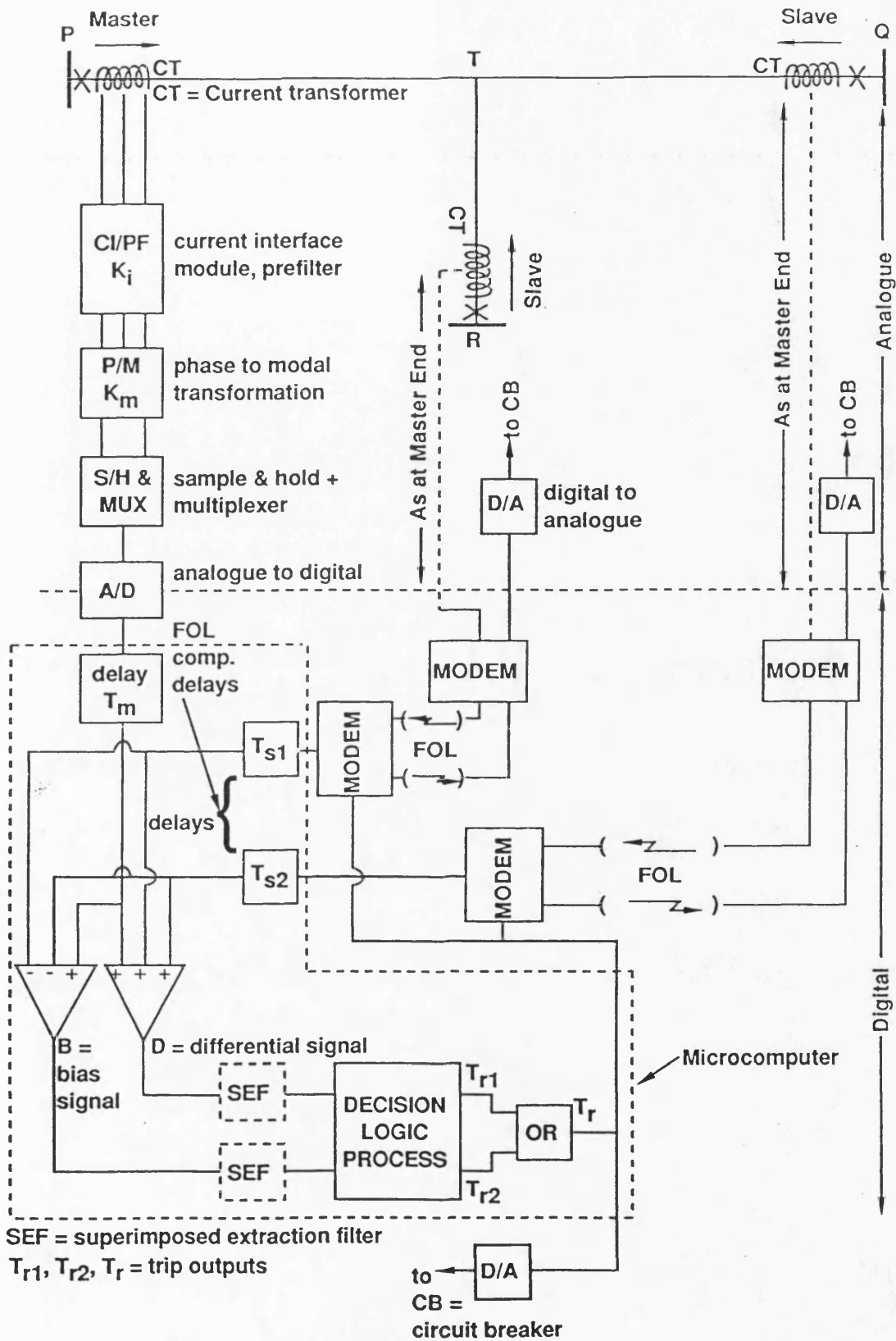
Fig. 3.1    A block schematic of the complete protection scheme
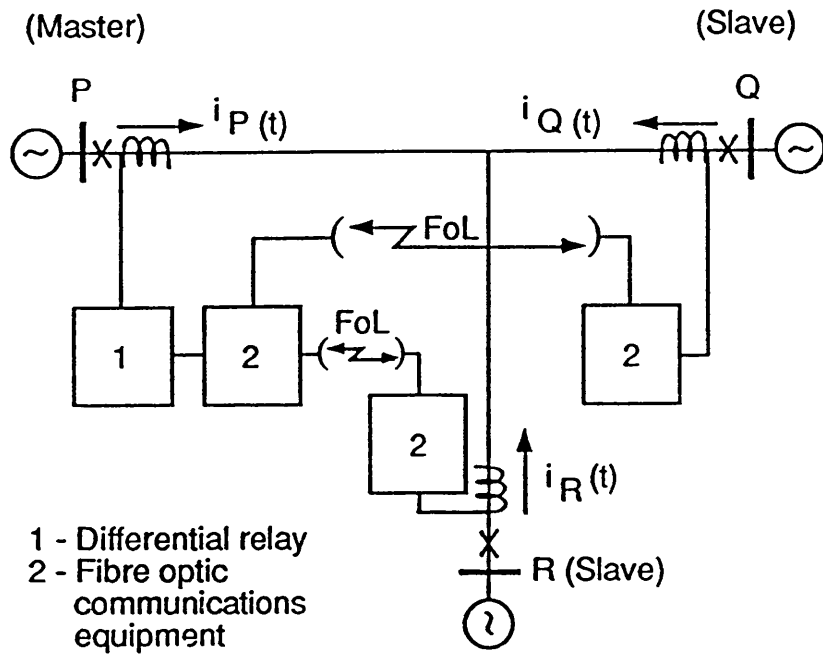
(Master)                                    (Slave)

P                                              Q

$i_P$ (t)                    $i_Q$ (t)

FoL

FoL

1 - Differential relay
2 - Fibre optic
    communications
    equipment

$i_R$ (t)

R (Slave)

Fig. 3.2    Single line representation of the basic system

MAGNITUDE-FREQUENCY RESPONSE
FOR "HALF-CYCLE" EXTRACTION FUNCTION



CASCADE EXTRACTION FILTER ARRANGEMENT
$H_z = (1 + Z^{-40})(1 - Z^{-80})$ ; $Z = e^{j\omega nt}$ ; $f_o = 50\,Hz$ ; $f_s = 4\,KHz$



MAGNITUDE-FREQUENCY RESPONSE
FOR FULL CYCLE EXTRACTION FUNCTION
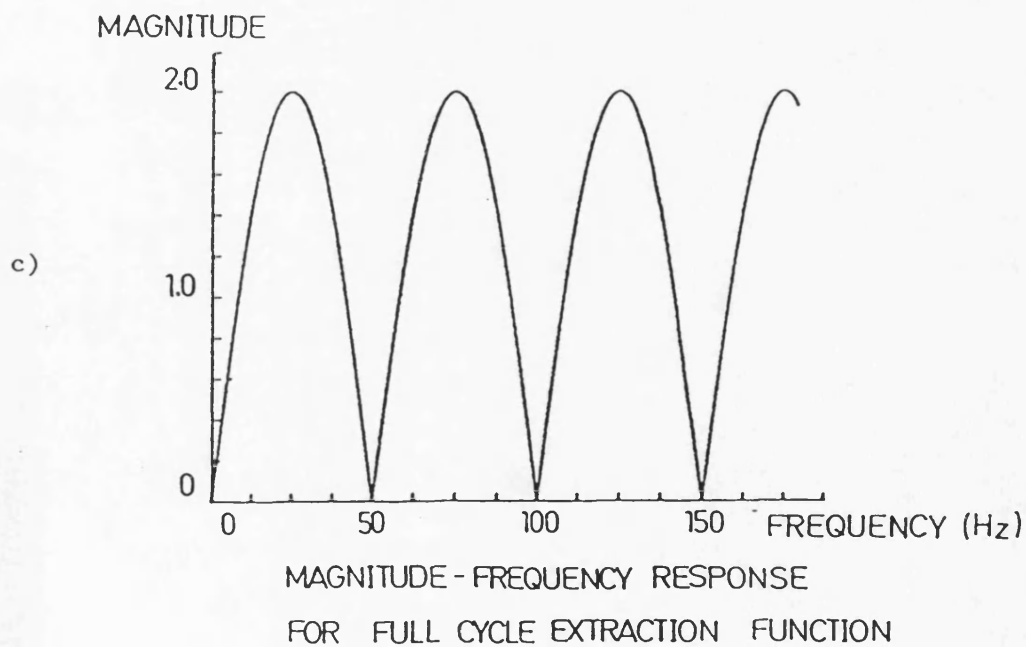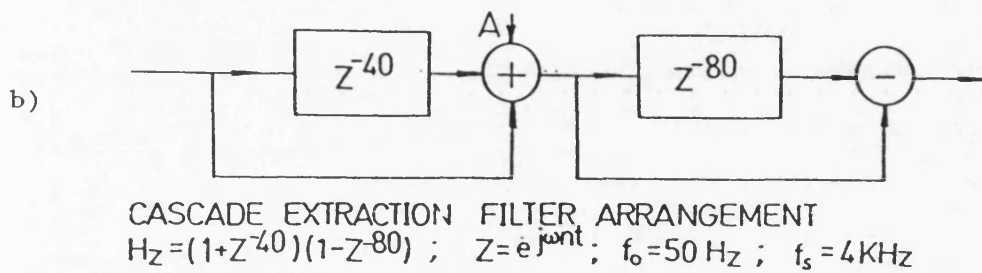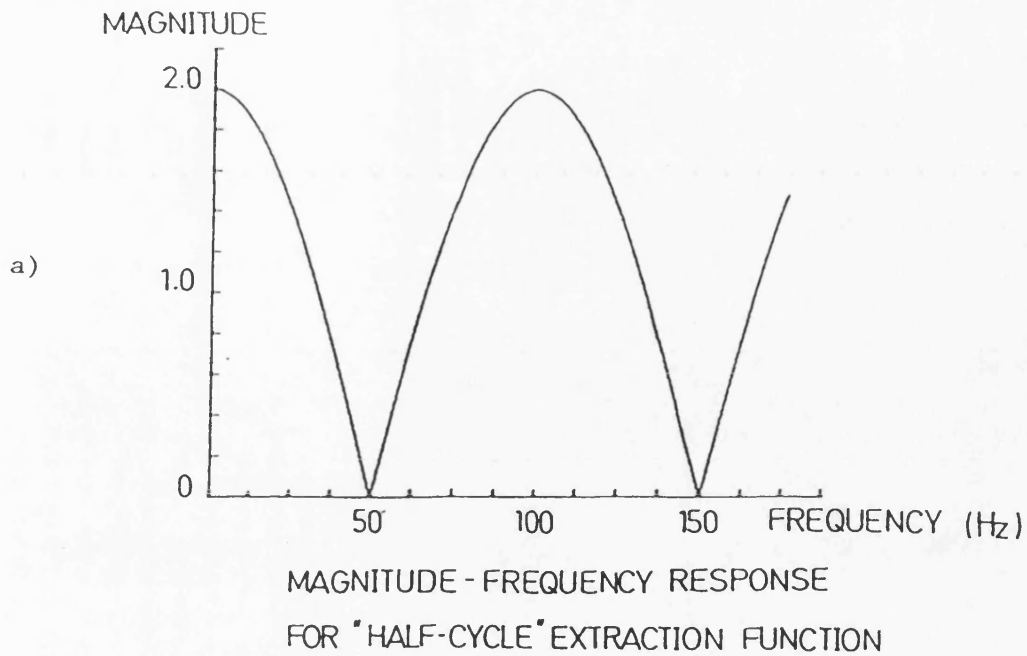
Superimposed component extraction filter diagram and response
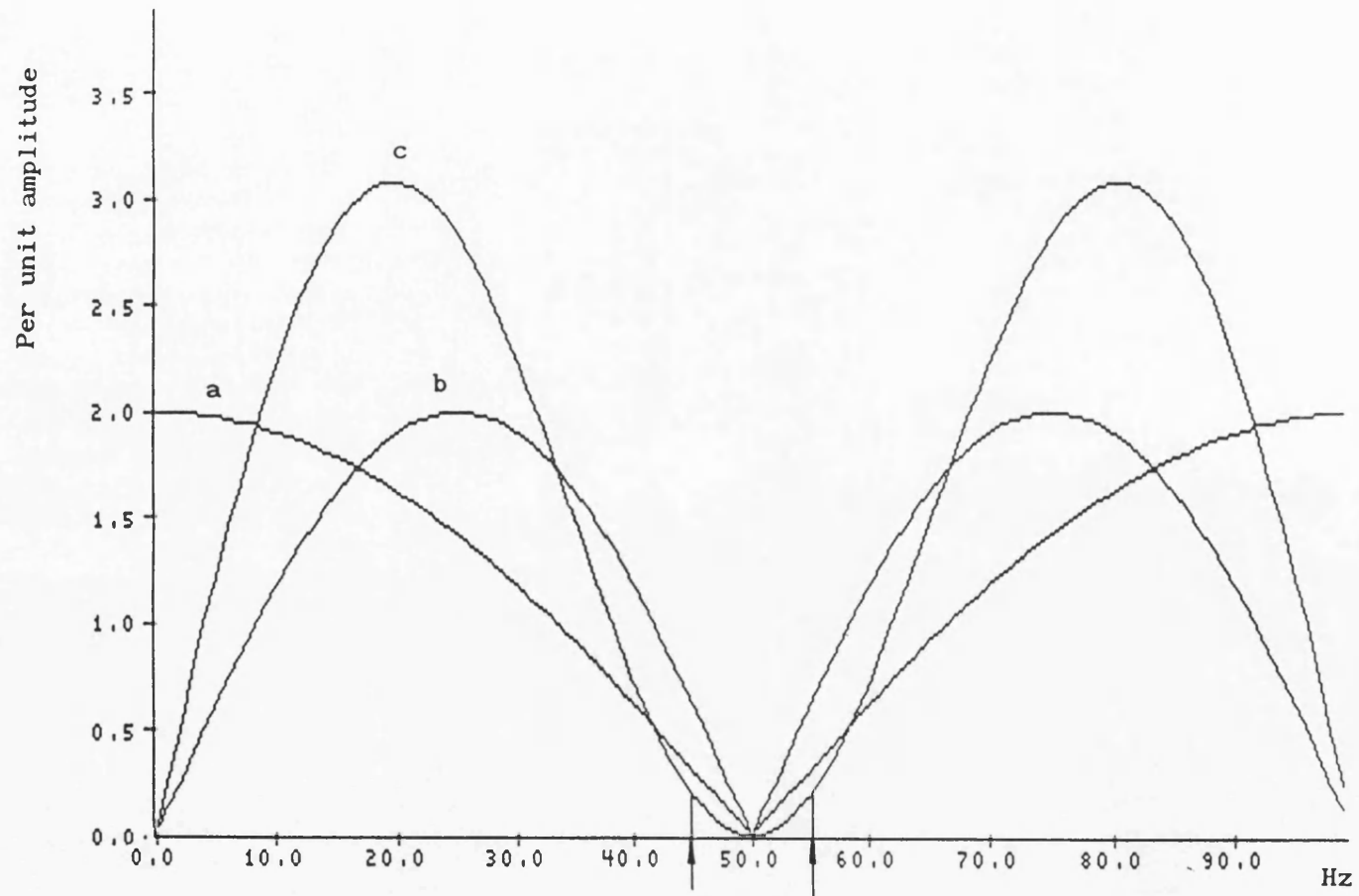
a) Half-cycle response

b) Full-cycle response

c) Overall response of the cascaded filter

Fig. 3.4    Comparison of subfilters and overall filter response

CHAPTER 4


RELAY HARDWARE DESIGN


4.1 INTRODUCTION

The application of microprocessor based digital equipment for the protection of EHV power transmission lines has many advantages over conventional equivalent analog types [24,25]. These can be summarized in terms of higher speed, better performance, reliability, flexibility, compact size, lower cost, in addition to cheap and easy maintenance. Digital relays have their functions realized mainly through software. Protection algorithms written normally in assembly language instruct the central processing unit of a digital system of the task to be performed. However, the usefulness of any digital protection algorithm based on off-line simulation depends on the ability to realize it in real time using the available digital hardware technology suitable for digital signal processing, with careful attention to its cost. This chapter describes in some detail the developments undergone in the design and building of the hardware prototype relay module shown in Fig.4.1. Essentially, it consists of 4 major elements:

a) A data acquisition unit (DAS) comprising low pass filters, sample and hold circuits, multiplexer and an analog to digital (A/D) converter.

b) A microcomputer unit which is based on a single Texas Instruments TMS32010 DSP processor. This includes the on-chip memory program ROM,

an internal data RAM, Input/Output interface and interrupt synchronization to the TMS32010. It also includes an adaptive sampling rate generator, an external data RAM and is equipped with a status register to hold information about the status of circuit breakers and communication links.

c) An analog display unit comprising a D/A converter whose output can be directed to the screen of a digital-storage oscilloscope and to a plotter, or it can be stored on a disk for future reference.

d) A test facility (as described later), comprising a programmable transmission line (PTL). This converts the fault transient waveforms generated on a main-frame computer to an analog form, suitable for relay testing and evaluation in real time.

## 4.2 LOW-PASS ANALOG FILTERS

For digital protection, the design of the filters between the primary transducers and the digital relay is vital. The filters can be analog or digital or hybrid to obtain the best performance from

es. The choice of a specific filter depends upon the

rate, cut-off frequency, frequency response required in the

nd and the restrictions on inherent time delay introduced by

tering process.

the sampling rate in this project has been chosen to be 4 kHz,

ore the maximum allowable frequency for the relay input signals

lot exceed the 2 kHz limit. The low pass filter band limits the

input signal to avoid aliasing caused by sampling the input at a rate less than twice the highest frequency of interest. Although the inputs for the relay model were provided by a PTL, the implementation of the filter herein was necessary because of the D/A conversion process within the PTL, where analog output is of staircase nature. Low pass filters have therefore to be employed to smooth the sharp pulses. Six parallel second order unity gain Butterworth filters of 1500 Hz cut-off frequency have been designed to give equal group delay within the allowed bandwidth. This allows a margin of about 0.5 kHz between the edge of the filter passband and the Nyquist frequency and it is necessary because reliable filters require a finite transition band between pass band and stop band. The Butterworth filter has been chosen because of its flat frequency response in the passband. Each analog low pass filter has been realized with an operational amplifier and passive components. Fig. 4.2 shows the filter as being configured for unity gain together with its frequency response for different order filters. The attenuation of the filter as a function of frequency can be calculated as in Eqn. 4.1.

$$dB = -10\log_{10}(1 + W_n)^{2m} \qquad (4.1)$$

where $W_n$ is the normalized frequency and m is the order of filter.


## 4.3 SAMPLE AND HOLD CIRCUITS (S/H)

A S/H circuit is an analog device, which holds an analog signal at a constant value during its conversion to a digital form. It is

normally required if the analog signal source which forms the input to A/D converter can change by more than 1/2 least significant bit during conversion. It is necessary to employ six S/H devices rather than execute the conversion serially through just one device. This approach is adopted so as to minimize errors in the sampled signals due to time stagger introduced between the sampling of the six signals. For example, if the signals were assumed to be pure sinusoids, then it can be proved that, when using the serial approach through just one S/H device, the error introduced due to time stagger may rise approximately to 50 quantum levels (based on 12-bit analog to digital conversion).

The six modal current inputs, provided by the PTL, after being band limited and smoothed by the filters are sampled at instants presented by the clock at a rate of 4 kHz six AD585 Monolithic high precision S/H operational amplifiers of wide bandwidth and 3 $\mu$s settling time are used. Fig. 4.3 shows a single S/H device configured for a unity gain together with the sampling rate driving circuit.

The sampling rate is a nominal 4 kHz signal which is derived by dividing the 5 MHz provided at the CLKOUT pin of the TMS32010 processor by a divide by N programmable counter (PC). The PC is loaded through the data bus by a suitable digital value N, which can be updated through software. The sampling rate is updated every 20 ms to perform frequency tracking. A flow chart of the software operation is presented in Chapter 5. The cascaded arrangement of 2 X 74LS74 flip-flop is a master and slave method suitable for

generating stable pulses of any required duty cycle. A high frequency clock having a period of the required pulse width of 4 $\mu$s provides the clock of the slave flip-flop while the 4 kHz sampling rate provides the clock of the master flip-flop. This cascaded arrangement of the flip-flops makes the generated pulses much more stable and immune to changes and flickering as would be the case when using a monostable. In the case of the latter, resistors and capacitors can be affected by temperature changes.

## 4.4 ANALOG MULTIPLEXER

When a single A/D converter is used for accessing more than one analog input, multiple analog switches (multiplexer) which share a common output are required. Fig. 4.4 shows a standard eight-channel multiplexer and its driving circuit. This comprises an FET switch with bipolar $\pm$ 10 volt level converters and 2 $\mu$s access time. The inputs of the multiplexer are the modal current signals and the output is routed to the A/D input pin. An on chip decoder selects the appropriate channel by means of a binary code. Only one channel is activated at a time, and all channels may be activated by an enable/disable control signal. The different channels are addressed by a (74LS93) binary counter which increments its value on the decreasing end of the conversion cycle provided by the A/D converter. The present value of the counter provides the address of the channel to be converted until the multiplexer sweeps all the six input channels and the counter then automatically resets the multiplexer, ready to receive the next set of six samples in the next cycle. The

presence of any spikes in the multiplexed signals is significantly reduced by providing a delay of 2 μs in the software before initiating the start of the conversion signal.

## 4.4 A/D CONVERTER

The conversion of an analog signal into digital form is necessary at the interface to a microprocessor system. For EHV power system applications, the A/D converters must have a dynamic range of at least 60 dB if an accurate digital representation of widely varying signal is to be achieved and consequently at least a 12-bit A/D is required. The most significant bit (MSB) is used as a sign bit, and the remaining 11-bits give a dynamic range of 66 dB. This effectively means that when a ±10 volt A/D converter is used, one quantization level (Q) corresponds to:

$$Q = \frac{V_{in}}{2^n} = \frac{10 \text{ V}}{2^{11}} = 4.88 \text{ mV}$$

where n is the number of bits representing the digital output

$V_{in}$ is the A/D analog input

The A/D as shown in Fig. 4.5 is a 12-bit successive approximation analog device ADC85 with 10 μs conversion time. It is configured for bipolar analog inputs between ± 10 volts. The A/D start of conversion rate is of 12 μs duration and is generated by a programmable counter arranged to count down. The data to the counter is loaded via software and latched in a buffer which keeps its value constant until the end of conversion of the six signals whereby the counter is then

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disabled. The start of conversion signal is a positive going pulse and it must go low and stay low during conversion cycle. The status end of conversion signal (EOC) goes high during conversion and returns low when the conversion is complete. EOC signal is routed to branch on input low BIO of the microprocessor and to the counter controlling the multiplexer. Also at the decreasing edge of the EOC signal, the A/D digital output is stored in two octal latches (2 X 74LS373) ready to be loaded onto the data bus. The A/D 12 bit digital value is stored from left to right and the least 4 bits of the octal latches are grounded to avoid software masking. Two trimmer resistors are used to control the offset to zero value and the gain to unity.

Data output from the A/D to the buffer is complementary Two's complement as required by the microprocessor, and this can be accomplished by inverting the most significant bit of the binary offset value.

## 4.5  PROCESSOR UNIT

A microprocessor in a digital equipment plays the main role in its operation. High speed microprocessors, along with efficient programming can substitute thousands of hardware analog or digital circuits. The choice of one particular type from a variety of microprocessors depends on a number of factors such as the type of application, the nature of the algorithm to be implemented, the required speed, the accuracy requirements and its ability to perform

the functions of the algorithm in real time in a duty cycle which does not usually exceed 70% of the sampling time interval. A Texas Instrument TMS32010 DSP processor (Fig. 4.6) which is specially designed for signal processing at a very high sample rate has been used.

A simulation program of the algorithm, written in assembly language of the TMS320 processor has revealed that the algorithm could be successfully executed within the required sampling interval. Moreover it has been established that a single processor is capable of performing the signal processing of the two Aerial mode current signals without the need to use two separate processors. This process has been carefully optimized by efficient multiplexing of the two modes through the complete algorithm, ranging from data acquisition and data storage to processing and decision logic.

The technique employed in implementing the relay algorithm has the effect of significantly reducing the duty cycle and is fully described in Chapter 5.

The key features of the TMS320 can be summarized as follows:

a)    execution of most instructions, including multiply and accumulate, requires only 200 ns

b)   16-bit instruction/data word, 16-bit data bus (D0-D16), 12-bit address bus (A11-A0)

c)   32-bit ALU/accumulator - signed Two's complement fixed point arithmetic

**d)** 2 built-in hardware counters, 2 hardware arithmetic shifters

**e)** eight input and eight output channels

**f)** 144 X 16 on-chip random access data memory (RAM)

**g)** 1536 X 16 on-chip read only program memory (ROM)

The TMS32010 is the first member of the TMS320 digital signal processing family, designed to support a wide range of high speed numeric intensive application. It is capable of executing five million instruction per second and utilizes Harvard architecture. Program and data memory lie in two separate spaces, permitting a full overlap of the instruction fetch and execution, thereby increasing the flexibility and speed of the device. The coefficients stored in the program ROM are read into the data RAM eliminating the need for a separate coefficient ROM. It also makes available immediate instructions and subroutines based on computed values resulting from on-time operations, These permit to perform adaptive operations by altering formerly preset values during initialization process. The TMS32010 utilizes hardware to implement functions that other processors typically perform in software, including a hardware multiplier. Arithmetic shift registers allow data scaling, thus reducing the duty cycle, as they can substitute the division and multiplication processes and can be performed as a part of one instruction.

The program ROM is a non-volatile store which is used to hold the sequence of program instructions. It also holds the relay setting

parameters which are transferred to the data RAM during run time. The program memory consists of 1.5 K words of 16-bit width and can be expanded up to 4K words.

The internal data memory RAM consists of 144 data words of 16-bit width present on chip; it is a read-write volatile store, and it is designed to hold the results of arithmetic and/or logical operations and variable data derived via the I/O interface. It is also used for intermediate data storage.

## 4.6  INPUT/OUTPUT INTERFACE

One of the challenges of designing a system based on I/O interfaces in real time is how to efficiently structure the algorithms to be implemented in accordance with externally  preset hardware operations and at the same time maintaining the process integrity. Tristate buffers, delay  elements, timing and control devices, logic circuits and decoders are commonly used in the interface  between a high speed processor and the lower speed external periphery devices. The function of the interface is to prevent data bus contention and to ensure proper selection of the  port which the CPU has to write to or read from.

Fig 4.7 shows that 8 Input/Output ports can be directly accessed by the three least significant bits of the address bus (A0-A2). These form the input of '3 to 8 ' decoder. The decoder generates the chip select signal of a port to be accessed, and this signal is then logically anded with  a read/write signal to recognize a port as an

input or output respectively.

The three LSBs of the address bus, A0-A2, are multiplexed as shown in Fig 4.6 and they can be designated to the I/O ports by the use of IN and OUT instructions. The remaining higher order bits of the address bus, A3-A11, are held at logic zero by specially designed logic circuit during execution of these instructions. Fig 4.7 shows that 4 of the the 8 input ports are assigned to read the data from the external devices and 6 of the 8 output ports are assigned to write data to the external devices. The remaining ports are kept for future expansion of the PCB board. The registers are 16 bit latches which hold the data of the external ports at a constant value. Using the decoder in conjunction with the control signals, only one single port is enabled at a time to load its information onto the data bus.

## 4.7 SYNCHRONIZATION OF THE TMS32010 WITH THE INTERRUPTS

When using asynchronous interrupts on the TMS32010, synchronization between the external hardware clocks and processor instruction cycle must be maintained. Software running in an interrupt environment can be fairly standard if masks are properly set within timing loops and the interrupt routines are independent of main program software, but as soon as interrupt routines and the main program start sharing utility routines, some unexpected events can occur. The external hardware shown in Fig. 4.8 is necessary to ensure proper execution of interrupts. The status of the BIO pin,

circuit breakers and communication channels are polled at regular time intervals without affecting the process flow of the algorithm. The status register is a 16 bits digital input port, each bit can be tested independently by the bit test instructions provided by the TMS32010. This register is essential for the security of the protected network since upon detection of an error in the COMS link, a backup protection system should be activated.

The INT signal is a maskable interrupt which is active low, which has been synchronized with the microprocessor CLK by using a D-type positive-edge triggered flip-flop. This arrangement ensures that the microprocessor is interrupted only at the end of a cycle execution. The application of INT signal resets the program counter to the second location of the program ROM.

The BIO pin is useful for monitoring peripheral device status, especially as an alternative to using an interrupt when it is necessary not to disturb time-critical loops. The J-K negative-edge-triggered flip-flop (74LS112) has normally its output $\overline{Q}$ toggled at high level when the CLK is high. At the end of conversion, the EOC goes low and $\overline{Q}$ is then forced low, whereby the digital value of the A/D is read. The chip select $\overline{CS}$ which enables the A/D register, resets the 74LS112 flip-flop forcing $\overline{Q}$, which is connected to BIO pin, to return high.

The reset function is enabled when an active low is placed on the RS pin for a minimum of five clock cycles. The reset signal is applied

through 2 Schmitt-trigger devices to prevent debounce action. When the push-button is pressed, all functions of the processor including the interrupt are disabled, the registers are cleared and the program counter resets to the first location of the program ROM.

## 4.8 DAS TIMING SIGNALS

The data acquisition timing signals shown in Fig. 4.9 are generated by specially designed hardware circuits in conjunction with processor software. The 5 MHz provided at TMS32010 CLKOUT is divided by a decade counter (74LS90) and the signal is then squared by a 74LS74 flip-flop, resulting in the 250 kHz cycle. The nominal 4 kHz sampling frequency is obtained by loading a 3 X 74LS193 programmable counter by an appropriate value N which divides the 5 MHz.

The INT signal is a direct inversion of the S/H signal and it performs two functions, the first of which is to acknowledge the microprocessor that a new cycle has started and the second is to reset the multiplexer to the first channel to be converted.

The S/C signal has a period of 12 μs. It is generated by dividing the 5 MHz processor clock provided at CLKOUT pin by a divide by N programmable counter. The microprocessor upon receiving the INT signal performs a software delay of 2 μs to allow the multiplexer to settle to the first channel before sending the S/C signal. The C/T is of 10 μs duration, which leaves a 2 μs time period after the end of conversion for the processor to read the converted channel. The BIO

status remains low until the digital value is read by using the instruction (IN), whereby the BIO is then forced high.

## 4.9. EXTERNAL DATA RAM

During the relay software development, it has been found that the capacity of the internal data RAM 144 words is not enough for the storage of data needed to implement the filtering processes.Therefore it was decided to add an external RAM as shown in Fig. 4.10. The TMS32010 accesses the external RAM using two of the eight parallel I/O ports. One of the ports is used to access the address counter for the RAM and another port is used to access the RAM. The external RAM can be accessed as an external port in 2 cycles (400 ns). This consists of 8 X 16 static RAM of 90 ns access time. It is supported by an address output register, an address input register, an address decoder and a programmable address counter. The address of any location in the data RAM can be loaded into the data bus and latched during a write instruction (OUT) into the address output register comprising of two 74LS373 octal latches. The address counter is a 16 bit programmable up/down counter consisting of (4 X 74LS193), which is automatically modified whenever a read or write operation is performed on the external RAM. The address input register consists of (2 X 74LS244) octal latches, and allows the current external data RAM address, which is pointed at by the address counter, to be read by the microprocessor, and stored in a temporary register as an index for the next cycle operation.

## 4.10    D/A CONVERTER

A 12-bit high speed digital to analog converter (D/A) as shown in
Fig. 4.11   has been included on the interface board to enable the
digital signals within the processor to be monitored in analog form.
Its function in the prototype relay is to convert a digitally set
trip signal to an analog form where it can be stored on an
oscilloscope and this can then be redirected either to a plotter to
be directly plotted or to  a host  microcomputer  to be archieved for
future reference. Furthermore,  when the relay is installed in the
substation, the function of the D/A converter  is to provide the
energizing signals of the actuators which control the circuit
breakers. The D/A converter is a high speed 12-bit digital to analog
converter AD565A  with a 250 ns setting time. It is configured for
bipolar outputs between $\pm 10$ volts. The least four bits of the 16-bits
output buffer holding the input to D/A are grounded to avoid using
software masking. The most significant bit of the D/A is inverted to
translate the Two's complement data provided by the data bus buffer
to offset binary required by the D/A converter.
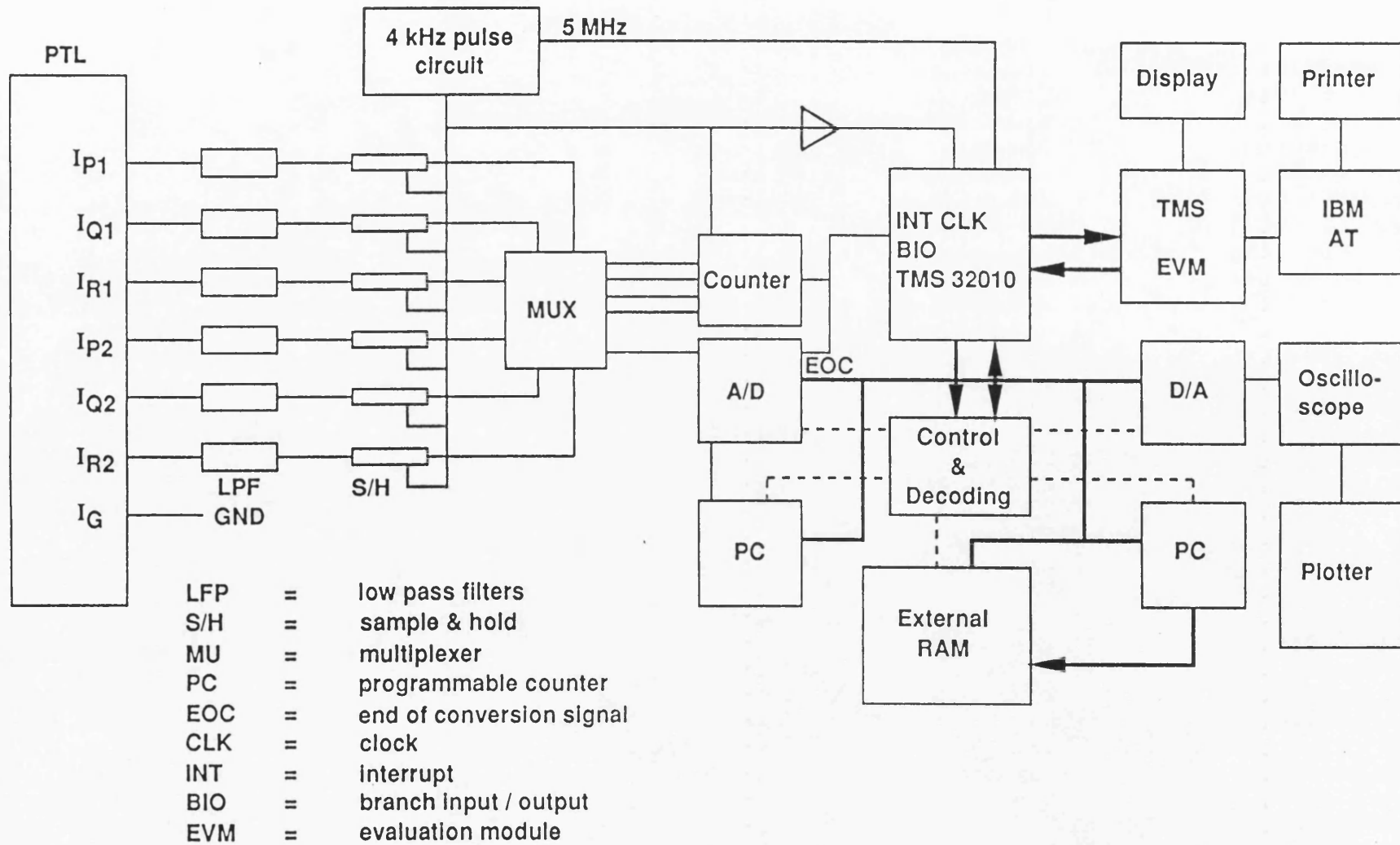
Fig. 4.1  Microprocessor differential relay block diagram
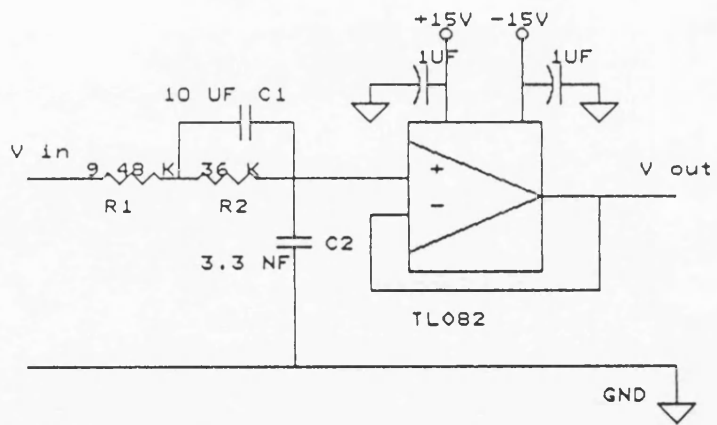
a)  Filter configuration
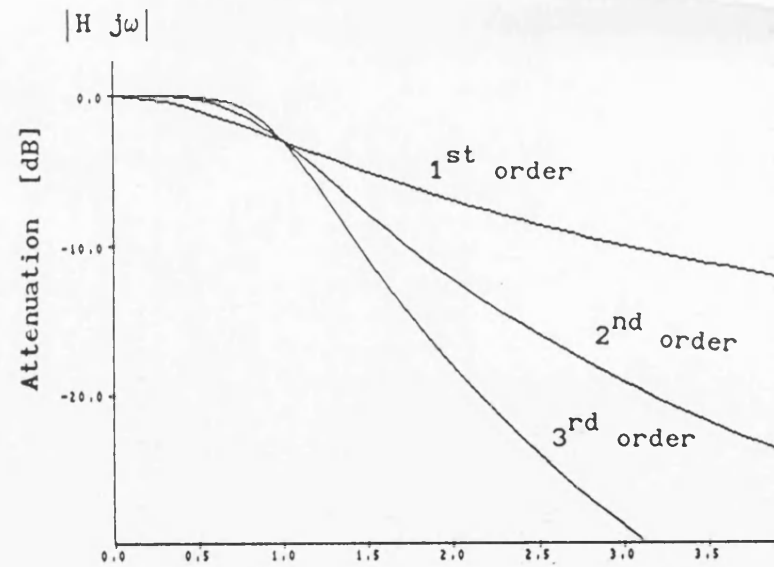
b)  Normalised frequency response

Fig. 4.2    Second  order  Butterworth  low  pass  filter  configuration  and response
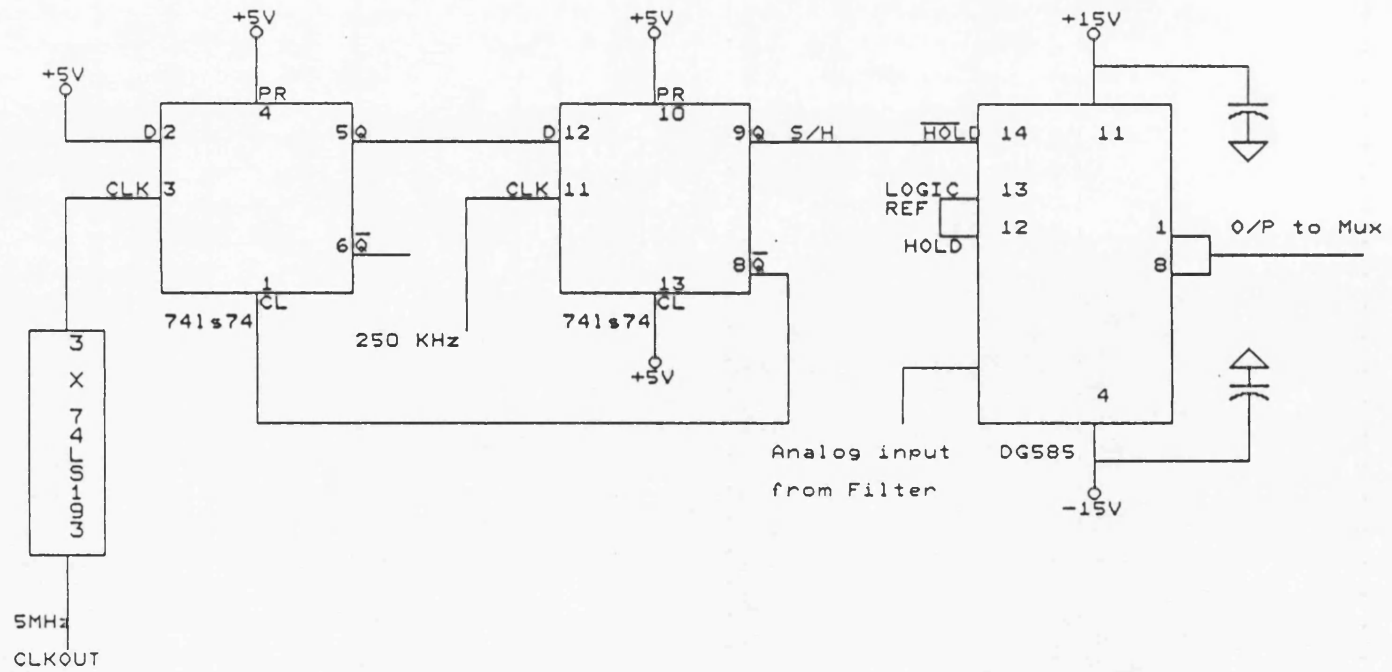
Fig. 4.3    Schematic diagram of S/H and its driving circuit
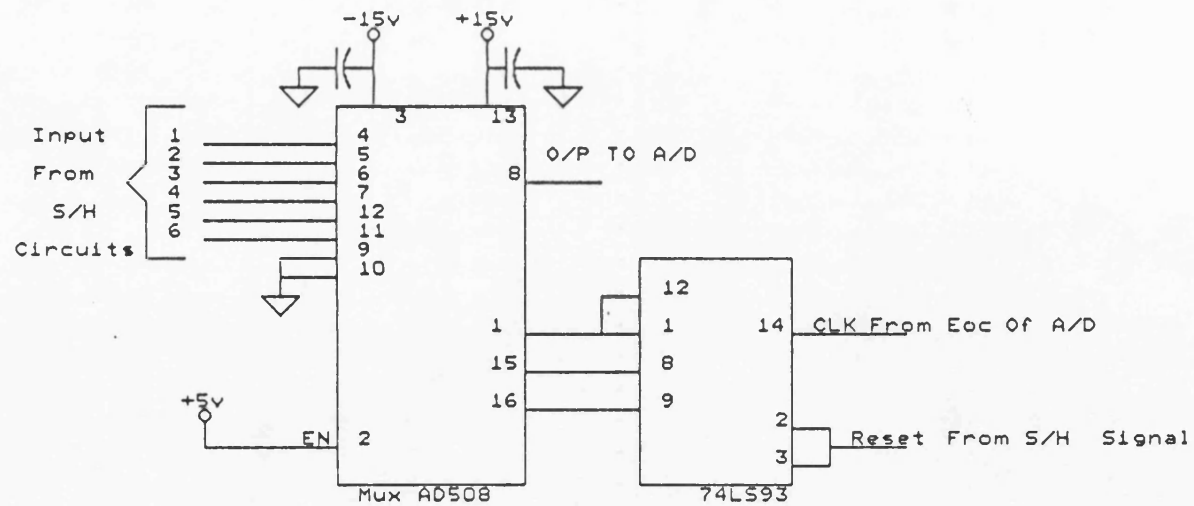
Fig. 4.4    Schematic diagram of the multiplexer and its driving circuit
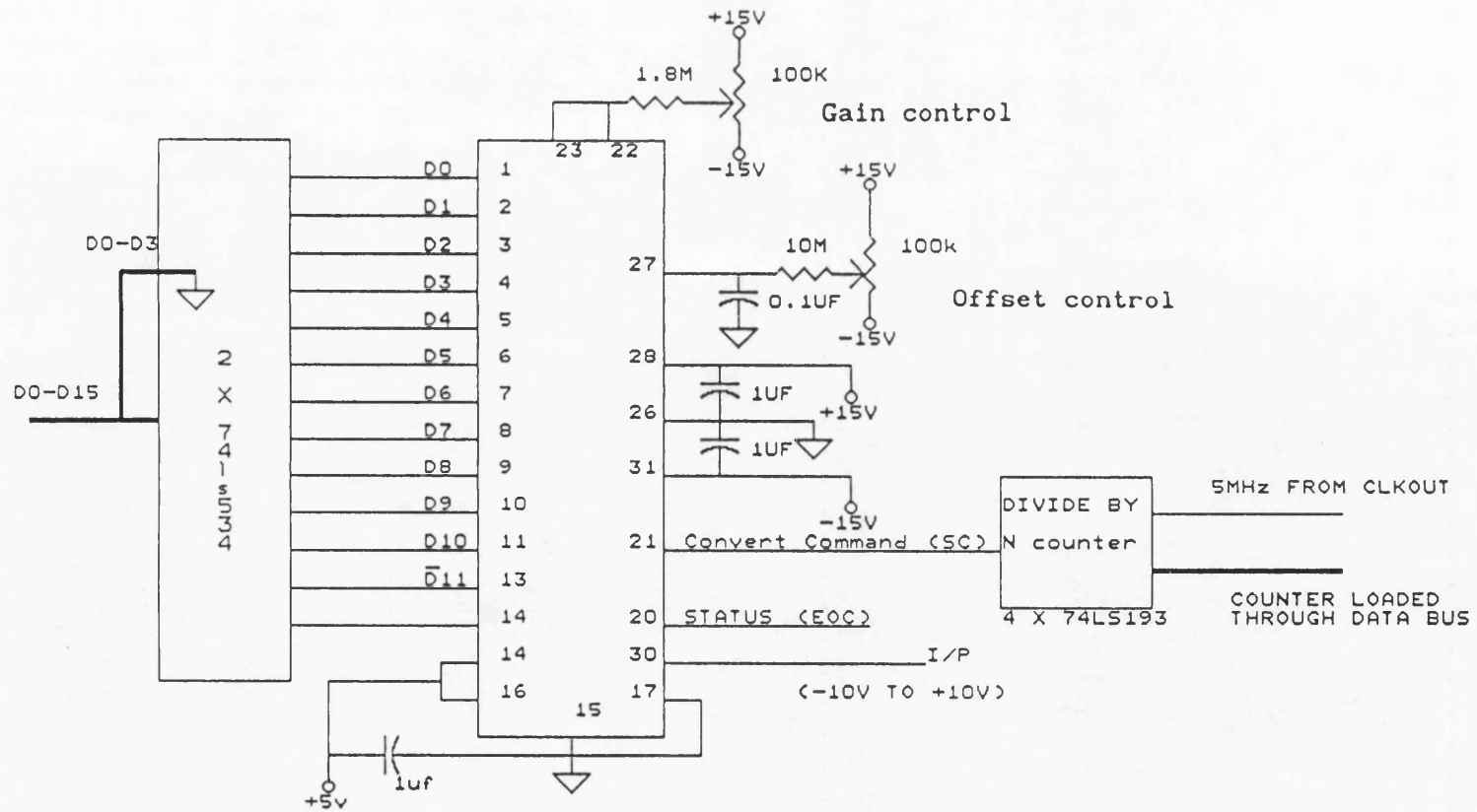
Fig. 4.5    Interface of A/D converter

Some of the key features of the TMS32010 are:

- 200-ns instruction cycle
- 1.5K words (3K bytes) of program ROM
- 144 words (288 bytes) of data RAM
- 16 x 16-bit parallel multiplier
- External memory expansion to 4K words (8K bytes) at full speed
- Interrupt with context save
- Barrel shifter
- On-chip clock
- Single 5-volt supply, NMOS technology, 40-pin DIP and 44-pin PLCC.
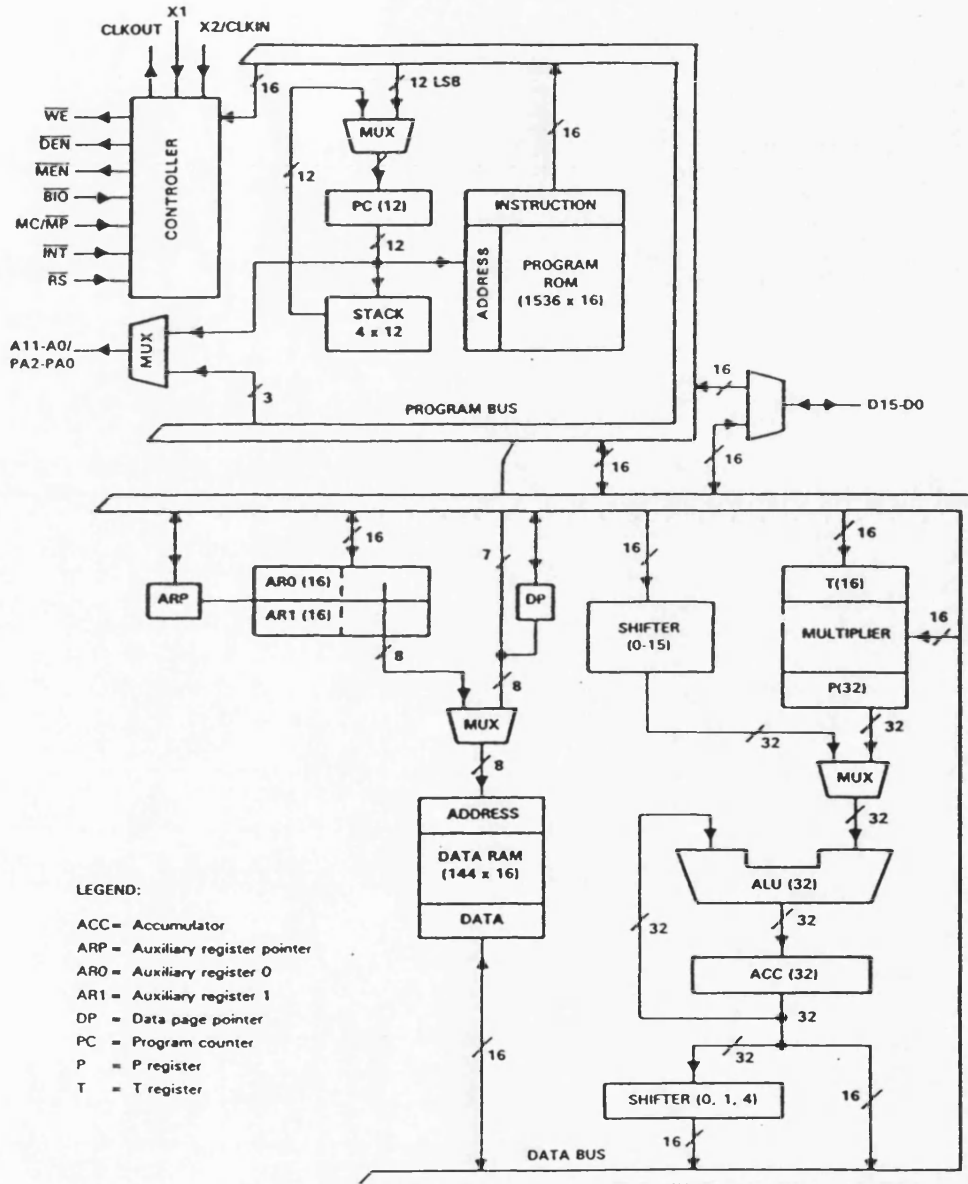


Fig. 4.6   Functional block diagram of the TMS32010
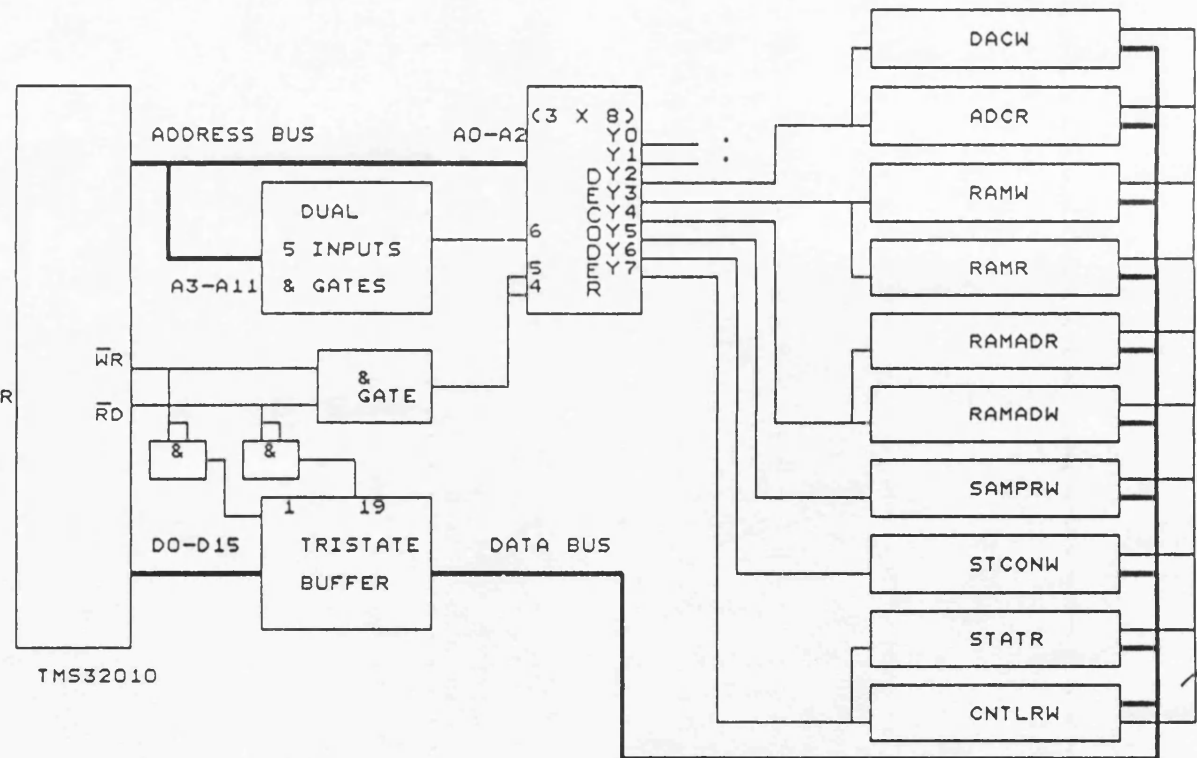
Fig. 4.7    Input/output interface to TMS32010 microprocessor
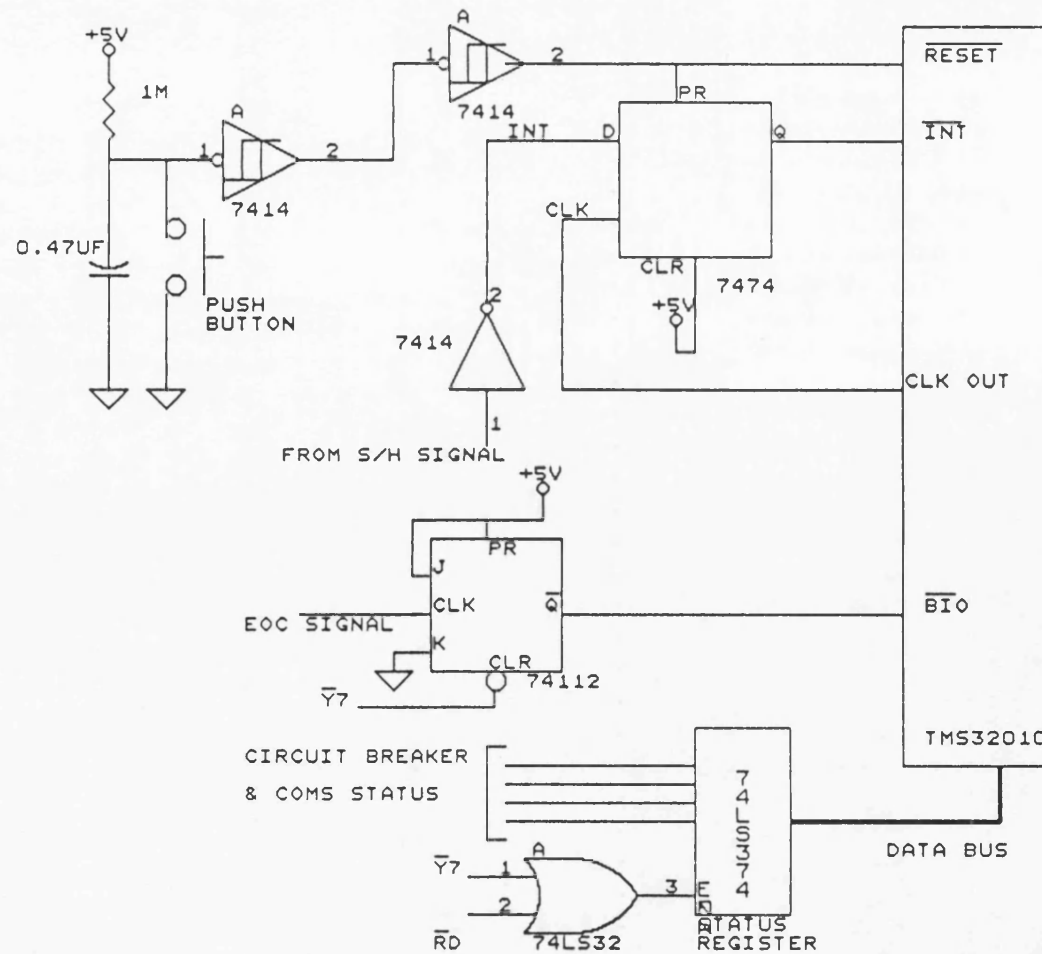
Fig. 4.8 Method of synchronizartion between TMS32010 and the interrupts
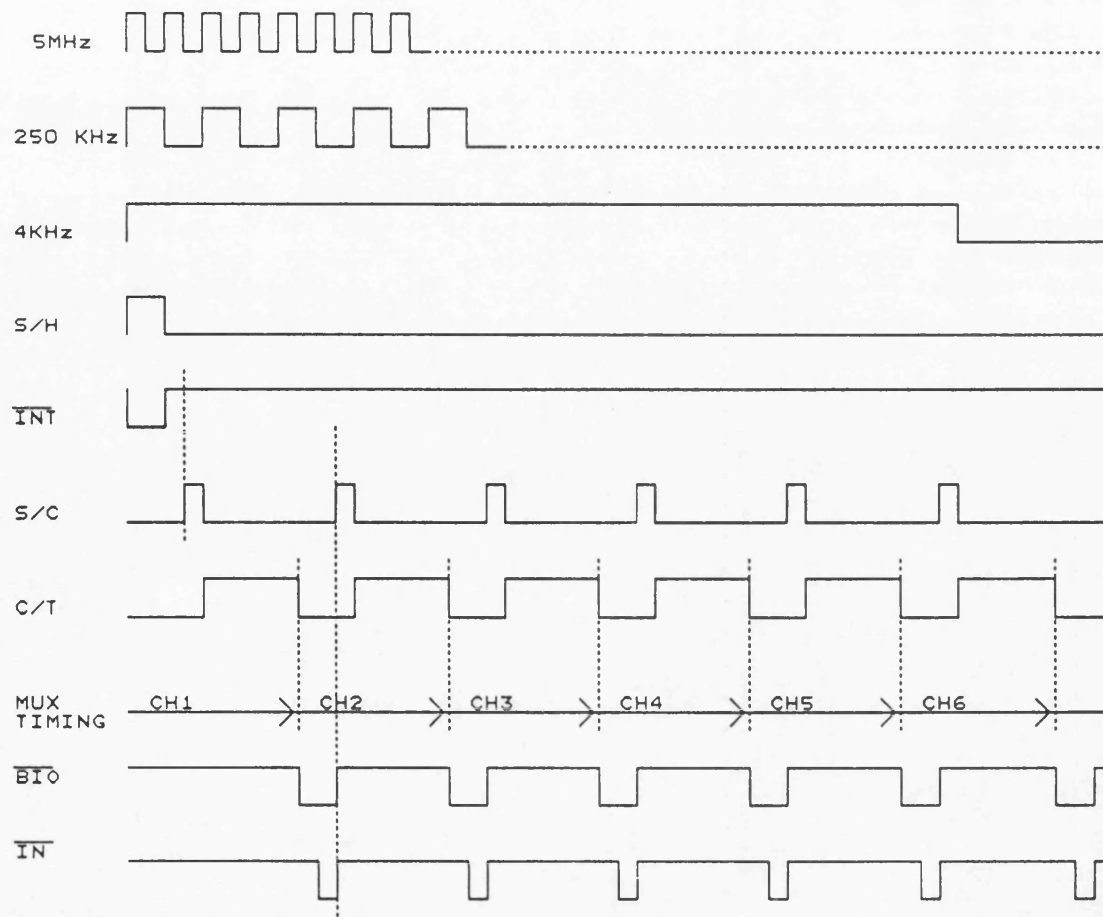
Fig. 4.9   Data acquisition timing diagram
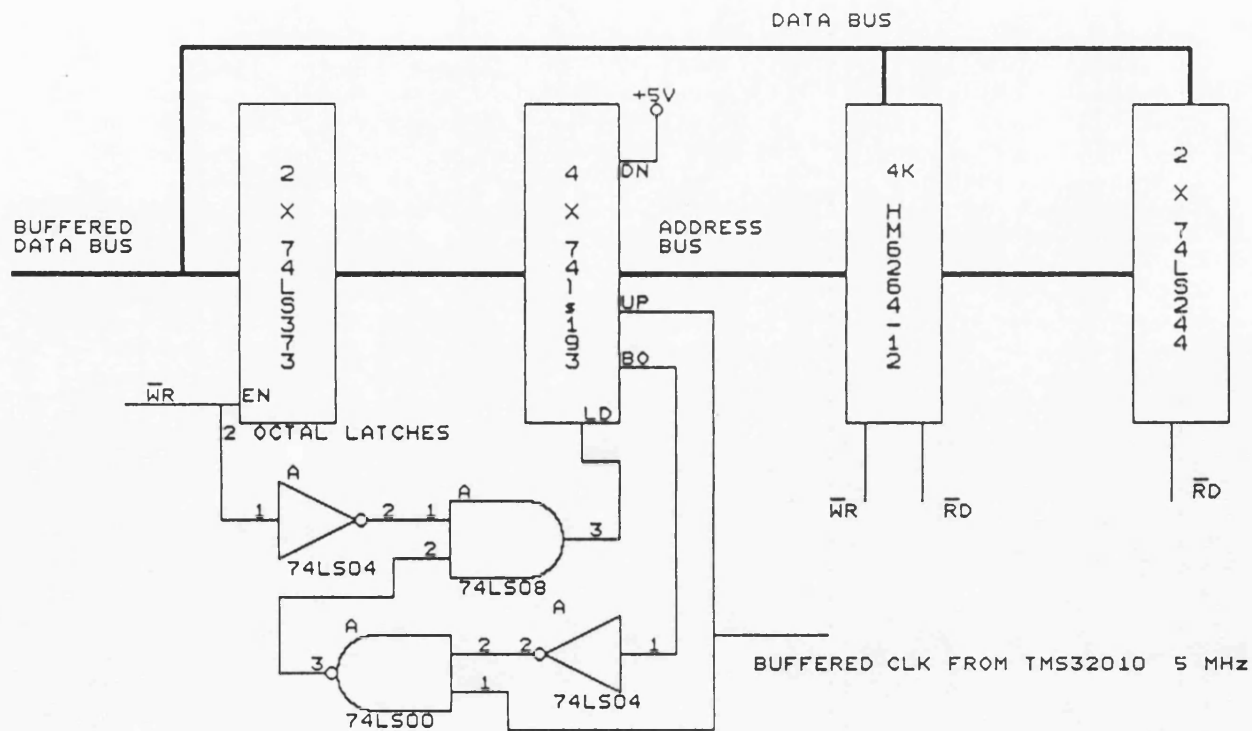
Fig. 4.10    External RAM block diagram
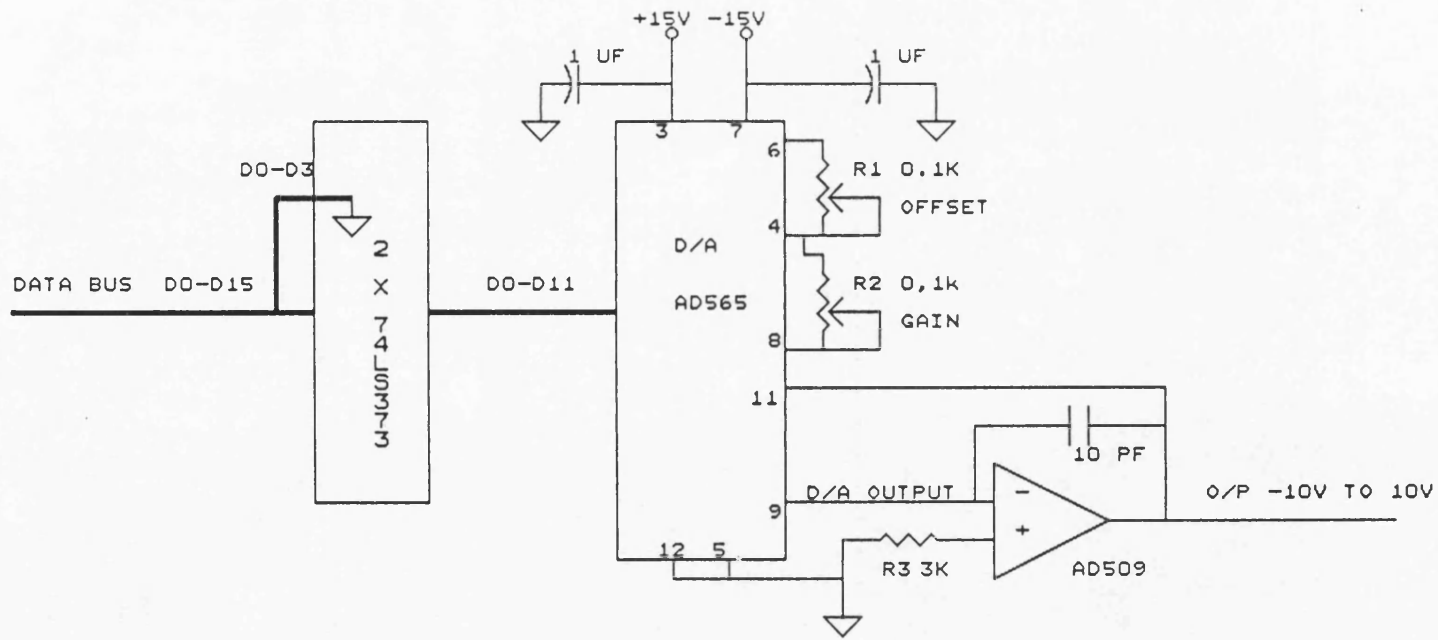
Fig. 4.11    Interface of D/A converter

CHAPTER 5


RELAY SOFTWARE DEVELOPMENT


## 5.1 INTRODUCTION

This chapter describes in some detail how the software control program developed works in conjunction with the hardware developed to perform the relay algorithm operation in real-time. However, before proceeding on to the real-time implementation of the relay algorithms, it is convenient to introduce the various stages undergone in the development of the microprocessor software as shown in Fig. 5.1.

When a high-level language is used for digital processing, an inherent disadvantage exists, namely the relatively long times involved in the calling processes of the various subroutines. Thus, in order to overcome the constraints imposed by the short sampling interval, an essential requirement for high speed protective systems, the program must be written either in machine language or in a low level language close to it such as assembly language.

In this project, a suite of programs were written in the TMS32010 assembly language on an IBM-AT host computer and these were then assembled and linked to produce object codes suitable for the microprocessor. Such programs can be tested and debugged either in the off-line software environment of a processor simulator for quick debug or in an on-line environment of the hardware, using a TMS32010

evaluation module board (EVM).

The simulator is a XDS/320 Texas Instruments software program that simulates the operation of the TMS32010 to allow program verification. The debug mode enables the programmer to monitor and modify the internal registers and memory of the simulated TMS32010. The object code generated for each module is stored in a virtual program memory and executed step by step using the instructions provided by the simulator software. The Texas instrument EVM is a single board which enables the programmer to determine if the TMS32010 meets the speed and timing requirements of the particular application. The EVM is a stand-alone module which contains all the tools necessary to provide full in-circuit emulation in a speed close to the real-time speed. It has the facility to communicate with the host computer via an RS-223 serial link and is also provided with a target connector to interface to external peripherals built on an I/O interface board.

The approach used for implementing the relay algorithm in real-time takes two main stages:

i) development of the steady-state performance for every single module.

ii) development of the dynamic performance of the relay as one unit.

In the first stage, different modules, which form the overall relay software, were tested for satisfactory functioning. For this the behaviour of each module was tested separately in conjunction with

its control program. Signals of known amplitude and frequencies were fed to the relay modules and the changes of these signals at different registers of the module were traced bysetting appropriate break points. Furthermore, the changes in the signals were monitored in analog form on a high resolution digital scope by directing the output of any required operation to a D/A converter and then to the scope.

The second stage of the relay hardware and software testing as a whole unit was carried out in real time under the control of the relay program contained in the program ROM, without any interruption by the EVM facility as this would seriously affect the speed of the microprocessor. The relay was initially tested with known waveforms generated from a signal generator. In order to facilitate comparison between CAD signals and those of the hardware, a software facility has also been incorporated within the relay to monitor the bias, differential, and operate signals via a D/A converter.

## 5.2   REAL-TIME RELAY ALGORITHM IMPLEMENTATION

An important factor which cannot be ignored when using a microprocessor for implementing a digital algorithm in real-time is the optimization of the software processing time. The salient features of the program software written in TMS32010 assembly language [26,27] and implemented in fixed point are:

a)   program instructions should be converted into machine code and stored in a non-volatile ROM ready for real-time execution.

b)   minimum use of interrupt signals, multi-cycle instructions, and division processes.

c)   efficient accessing of the external ports (peripheral devices).

d)   implementation of the circular filtering in transfer-replace mode rather than using the multiply (MPY) and data move (DMOV) instructions

e)   reduction of data storage and memory requirements by using common software and hardware address counters.

The effect of each of the above will be discussed at the appropriate point when describing  the implementation of the relay algorithm.

The sequence of processor instructions have been stored in a non-volatile memory  ready for execution in real-time as a single routine upon receiving a start signal. The start signal can be generated either on power-up of the equipment or by resetting the program pointer to zero value by an appropriate switch as shown in Fig 4.8. The algorithm operation can be divided into 6 logical parts, as follows:

i)    initialization process

ii)   data acquisition routine

iii)  computing of the relaying signals routine

iv)   frequency tracking and adaptive sample rate clock.

v)    superimposed components extraction routine

vvi)  implementation of the moving window average  filter

vii)  decision process routine.

## 5.2.1  Initialization process

On resetting the microprocessor, the program pointer starts the execution of the set of instructions stored in the program memory in a consecutive sequence, starting from memory location zero assigned as AORG 0. Location number 1 then instructs the program pointer to branch to the main program. The initialization process takes place in the main program. This consists of loading certain data memory locations from the program memory with preselected values, resetting flags and counters to zero and loading appropriate data to the control registers and decoders to initialize the external devices such as loading the programmable counters with the required sampling rate frequency and selecting the mode of the interface board i.e. writing or reading to/from a specific external device.

Upon completion of the initialization, the divisor value (N) which generates the default nominal sampling rate of 4 kHz is loaded into the sample rate PC which consists of 3 X 74LS193 as shown in Fig 4.3 and the interrupt mode is then enabled.

On receiving a hardware interrupt on the INT pin, (every 250 $\mu$s), the microprocessor instructs the program pointer to execute the instruction stored in location No 2 or 3 in the program ROM. From location No 2 program pointer branches to an interrupt routine where if necessary the status of the microprocessor registers is saved, the program pointer then executes the DAS routine.

## 5.2.2 Data acquisition routine (DAS)

In the DAS routine the program pointer executes some instructions which disable the hardware interrupt and initialise the I/O routine The data page, where the digitized samples of the input signals are to be stored, is then assigned and the TMS32010 two auxiliary counters (ARO,AR1) are initialized, ARO is used to hold the number of samples which are to be converted and the AR1 holds the first address where the digital values of the signals are to be stored.

The A/D conversion rate PC which consists of 4 X 74LS193 (see Fig. 4.5), is loaded through the data bus by a division value which generates the 12 $\mu$s start conversion cycle from the 5 MHz TMS32010 CLKOUT pin.

The branch on I/O 'low' BIO pin of the microprocessor is polled at regular intervals for a few micro seconds after the analog to digital conversion of a sample is complete, until all the samples have been converted into their digital values and stored in the internal data RAM. Each time a signal is converted and stored, ARO decrements by one and AR1 increments by one. The data acquisition process ends when ARO goes to 0, whereby the status of the BIO pin goes high through the remaining part of the duty cycle and the computation process begins. The conversion signal to the A/D is sent at regular intervals every 12 $\mu$s whereas the A/D conversion time is 10 $\mu$s. Therefore BIO pin remains low at the end of conversion for a period

of 2 $\mu$s within which the digital value stored in an external buffer must be read by the microprocessor and stored in the internal RAM. The process of polling the BIO at regular intervals has a time saving advantage on the usage of interrupt signal since the saving of the TMS32010 registers is not required when using the BIO method. Thus the overall process of implementing the data acquisition in this manner saves a considerable time of the duty cycle because:

a)    the interrupt process is used at the start of duty cycle, therefore there is no need to save the status of the microprocessor registers

b)    the input signals are not converted individually by sending the address of each channel at a time thus minimizing the addresses of the external devices

c)    the conversion time of the A/D converter is efficiently used, without letting the processor wait until the end of conversion time.

## 5.2.3    Computation of the relaying quantities

As previously mentioned in Chapter 3, the relay can work on either the total time variation principle of the modal currents or on their superimposed components. The total component Differential and Bias quantities for the 2 modes ($D_1$, $B_1$, $D_2$, $B_2$) are computed from the modal current waveforms as in the Eqns. 3.9 and 3.12 in Chapter 3. The superimposed component relaying quantities for the two modes are

then extracted from the 4 total component relaying measurands, rather than from the 6 modal currents, as in Eqns. 5.1 and 5.2 below.

This approach is adopted firstly, because it reduces the time and the storage space in the data RAM required for the implementation of the digital filters and secondly, it minimizes the errors introduced in the superimposed relaying signals due to analog and digital noise. The superimposed components for one-half cycle are extracted as:

$$
\left.
\begin{aligned}
SD_1(nT) &= D_1(nT) - D_1((n-40)T) \\
SB_1 nT) &= B_1(nT) - B_1((n-40)T)
\end{aligned}
\right] \text{ Mode 1} \qquad (5.1)
$$

$$
\left.
\begin{aligned}
SD_2(nT) &= D_2(nT) - D_2((n-40)T) \\
SB_2(nT) &= B_2(nT) - B_2((n-40)T)
\end{aligned}
\right] \text{ Mode 2} \qquad (5.2)
$$

where   S is the superimposed index

nT is the present sample in time.

(n-40)T is the 40th delayed sample in time

T is the sampling interval ($250\mu s$)

n is an integer greater than 40.

The extraction of the superimposed signals is carried out using specially designed digital filters, based on a cascaded arrangement (see Fig. 3.3). The basic theory behind these filters

is fully described in Chapter 3.

## 5.2.4 Implementation of the Superimposed components extraction filter

The conventional method of implementing a digital filter is to use a series of multiply, accumulate and shift stages. As the filter receives a new sample value at its input, the existing samples are simultaneously shifted towards the output, the oldest of which is discarded.

The cascaded digital filter arrangement employed for extracting the superimposed components has the advantage of having all the coefficients equal to ±1 and thus has the effect of adding the delayed half-cycle and subtracting the delayed full cycle to/from the present half -cycle and full cycle respectively. Using the conventional approach, a number of extra instructions such as load T register (LT), multiply (MPY) and data move (DMOV) equal to the length of the filter can push the duty cycle of the algorithm close to its limit.

An alternative approach is to implement a circular buffer in which a memory address pointer is modified for each new sample and used as reference for the the present and delayed sample in consecutive memory locations.

During the implementation of the superimposed component extraction filter, a problem arose due to a shortage of the available data memory locations in the internal RAM (144). This was overcome by

adding an external RAM to the interface board as shown in Fig. 4.10. The writing and reading from the external data RAM is controlled as explained in Chapter 3 by a hardware programmable counter which can be set to increment its value every time the external data RAM is accessed.

For a 4 kHz sampling rate the number of required locations to implement the one and half cycle filter for a 50 Hz frequency is 40 and 80 respectively for one relaying quantity. Thus for four i.e. Differential and Bias for each of the two modes, this will amount to:

$$(4 \times 40) + (4 \times 80) = 480 \text{ locations}$$

Since the software implementation of the half-cycle filter and the full cycle filter for the extraction of the superimposed components is very similar, it is therefore sufficient to explain in detail the technique used in implementing only one of them.

### 5.2.5 Half cycle and full cycle extraction filter

The filtering process must be applied on every relaying quantity, which effectively means implementing 4 filters, resulting in 4 external data RAMs where the filters can be implemented in parallel. This method is however, impractical and expensive from the hardware point of view. A second approach is to implement serially the four filters which in turn puts a heavy burden on the duty cycle, from a point of view of accessing serially the data RAM.

In order to have fast access of the data RAM , the filters for the

four relaying quantities are multiplexed and the data RAM is written to and read from in one go, with the aid of the hardware address pointer as shown in Figs. 4.10 and 5.2. The address of the first location in the data RAM is loaded to a programmable counter which increments its value by one at each writing cycle and pointing to the next higher address.

This means that every 250 $\mu$s the data RAM is accessed as an external device, four new samples each corresponding to one specific filter are written and the counter increments by 4 pointing to the first location of the next 4 samples. Furthermore, at every new sampling interval, the present hardware counter address value is read to a register in the internal data memory by the input address register and subtracted from a register which holds the length of the filter i.e. 160 samples. The writing process continues until forty samples of each signal are stored, whereby the data memory address counter counts up to the end address of the filter. The counter then resets to the start address of the filter.

The superimposed component half cycle extraction process begins by reading the first four delayed samples from the external RAM to the internal RAM and then it adds the delayed sample to the present sample (newly accessed from the present sampling interval) of the same signal. The present 4 samples which are in temporary registers in the internal data RAM, are then transferred to the external RAM to replace the 4 old samples and the process continues indefinitely until a fault is detected by the decision process whereby a trip flag

is issued.

The full cycle extraction filter follows the same procedure but this time the output of the half-cycle extraction filter is the input to the full cycle extraction filter and the filter length is doubled i.e. is 380 samples. The start address is one location above the end address of the half-cycle extraction filter and the extraction process is a differencing process.

A principal advantage of implementing the digital filter as circular ring buffers is in a significant saving in computation time. It should be mentioned that if the length of the extraction filter whose coefficients are simply ±1 is equal to N stages, then the conventional approach of implementing the filter would consist of instructions such as loading a register with a sample, multiplying and accumulating the product, shifting the sample to a high address and storing the computed value of the result for N samples.

Although the microprocessor has a built in multiplier and a powerful instruction (LTD) which can execute the first four operations of a conventional filter in one cycle i.e. 200 ns, however the above operations have to be carried out N times in every sampling period, whereby the processing in very short time interval becomes very difficult.

With the new circular ring buffer implemented in the prototype relay on the other hand, the operation can be done in simply reading the saved address register of the old sample stored in data RAM in 2

cycles and replacing it with a newly acquired sample, also in 2 cycles. Moreover, the address register of the location pointed to by the address counter can be saved and incremented any time the data RAM is accessed in one single clock cycle. The subtract or add process is performed in a further clock cycle and the result stored in another cycle. The overall time needed for the filter in one sampling interval is thus 7 clock cycles i.e. 1400 ns. This time is independent of the length of the filter while the time which is required for a conventional filter varies with its length. Another advantage of the new approach is the saving in the duty cycle which results from implementing the filter for the relaying signals in blocks of four data locations and this reduces the accessing time of the external data RAM counter by a factor of 1/4.

## 5.2.6 Effect of power frequency variation

The deviation of power frequency from its nominal value could affect the performance of the superimposed component extraction filter and result in a residual output error in the differential and bias signals during the prefault time. Although this effect can be made negligible for power frequency values of 50 ± 5 Hz when the sampling frequency is fixed at 4 kHz firstly because the operating signal is formed from the difference component of the relaying signals and secondly the threshold voltage value can be raised slightly to compensate for any spurious noise at the output of the filters, however, for a strong deviation of the power frequency from its

nominal value and also to retain the relay sensitivity to high resistance faults, a software method for frequency tracking has been implemented as below.

## 5.2.7 Frequency tracking and the adaptive sample rate clock

Frequency tracking and sample rate correction can be done by using hardware or software methods [23,28-32]. The method used for the relay developed here is a hybrid method. It consists of a programmable external counter whose input is the TMS320 5MHz CLKOUT signal , its output is the sampling rate and it is driven by adaptive loading (which is proportional to the power frequency) through the data bus.

The power frequency signal is formed from the digital values of two modal current inputs and scanned by a software counter $(C_n)$ which increments its value at each sampling interval, starting at the positive going zero crossing of the cycle and ending its counting on the next positive going zero crossing. During prefault time and when there is no deviation in the power frequency, the counter value $(C_o)$ must be equal to the power frequency period divided by the sampling interval i.e. for 50 Hz system

$$C_o = 20ms/250\mu s = 80 \text{ samples.}$$

When the power frequency decreases, its period increases, the counter value then increases and vice versa. Thus to keep the number of samples within a cycle to 80 ( this is the basic requirement of the digital filter), the sampling interval must vary proportional to

the power frequency period. The sampling interval is corrected and updated every power frequency cycle, i.e. every 20 ms as shown in Fig. 5.3.

## 5.2.8 Moving window average filter

In practice, high frequency embedded relaying currents can pose problems of relay instability particularly for external faults. This can be overcome by raising the threshold voltage levels. The latter would of course reduce the relay coverage to high resistive faults which produce low level relaying quantities. However, in this relay design the problem had been overcome by implementing a moving window digital filter to smooth the relaying quantities before applying a sophisticated decision logic process.

The averaging filter, whose function is shown in Fig. 5.4, has a low pass filter effect because it attenuates the high frequency harmonics present in the signals. As mentioned before, this is particularly important during external faults and current transformer saturation. Furthermore, it linearises the relaying signals and enables a lower threshold setting and, therefore, a higher fault resistance coverage to be achieved. The filter is applied to both the differential and bias signals derived for each mode and its output is defined by:

$$Y(k) = \frac{1}{M} \sum_{n=0}^{n=M-1} X(k-n) \qquad (5.3)$$

where  Y(k) ,  X(k)  are the present output and  input respectively

    M is the length of filter

    X (k - n)  are the previous input samples

    n = 1, 2,....,M-1.

Exhaustive tests on the relay  have shown that a window length M of 8 samples gives satisfactory performance without introducing a major delay.

The  technique  for  storing the data of  the  moving window digital filter is identical to that employed in the implementing of the previously described superimposed extraction filter. The process of Eqn. 5.1. has been performed on locations in the internal data RAM that holds the present and the seven previous computed values stored in the internal data memory during the present and  7 previous sampling intervals.

The relatively small group delay of the averaging filter on the relay operating time varies with the  fault inception angle and is compensated for by virtue of being able to set a lower threshold voltage level.

## 5.2.9  Decision process and logic counter

As mentioned before, in order to ensure relay stability for external faults, in particular under CT saturation conditions, it is necessary to apply a sophisticated decision process [16].

The relay decision process  is applied to the operating signal

derived from the Differential and Bias signals of the total current components or their superimposed values as shown in Fig. 5.5. It involves checking both the magnitudes and polarities of the Differential signal D(t) whereby a trip counter "P" is incremented by one only when four consecutive samples have the same polarities and , also at the same time greater than a threshold value. Failing to meet anyone of the two criteria, results in the counter being decremented by 1. The counter is not allowed to go below zero at any time.

The decision logic counter is implemented using 4 locations in the internal data RAM for each mode. The operating signal is checked over a moving window of 4 consecutive sampling intervals. The present sample value is stored in place of the oldest value which is discarded. Figures 5.6 and 5.7 show the decision logic counter operation for an internal and an external fault respectively.

For an internal fault , a trip signal is initiated when the counter attains a number of 4. This effectively means that the minimum number of samples over which a decision can be taken is 7, which corresponds to minimum trip time of 1.75 ms at the 4 kHz sampling rate.

As for the external fault, although the operating signal goes momentarily above the threshold voltage for 5 consecutive samples, the counter counts only to 2 and then decrements back to zero giving no trip signal.

The operating and tripping signals are presented in analog form by directing the output of the decision counter to the D/A converter.

The operating signal is shown as sampled and held  and as discrete samples, and the trip signal is indicated by a 5V flag for an internal fault and no flag for an external fault.   Once a decision has been taken that an internal fault exists, the tripping flag goes high and remains high at 5V and the relay enters into a delay routine of a preselected number of cycles. During this period, the relay keeps on checking the status of the circuit breaker by polling the data of a specially designed status register as shown in Fig 4.8, and once the fault is cleared and the CB's and COM's are in order, the relay resets and is ready to start again. If the fault has not been cleared, the relay waits for the time out signal at the end of the delay time whereby  it resets and starts again and repeats the aforementioned procedure until the fault is cleared. It is important to mention that the aforementioned 8 samples moving average filter and the decision process over 4 samples moving window were found to be satisfactory for the relay to be able to discriminate correctly between an internal and external fault for a wide variety of practically encountered system and fault conditions as discussed in the next chapter.
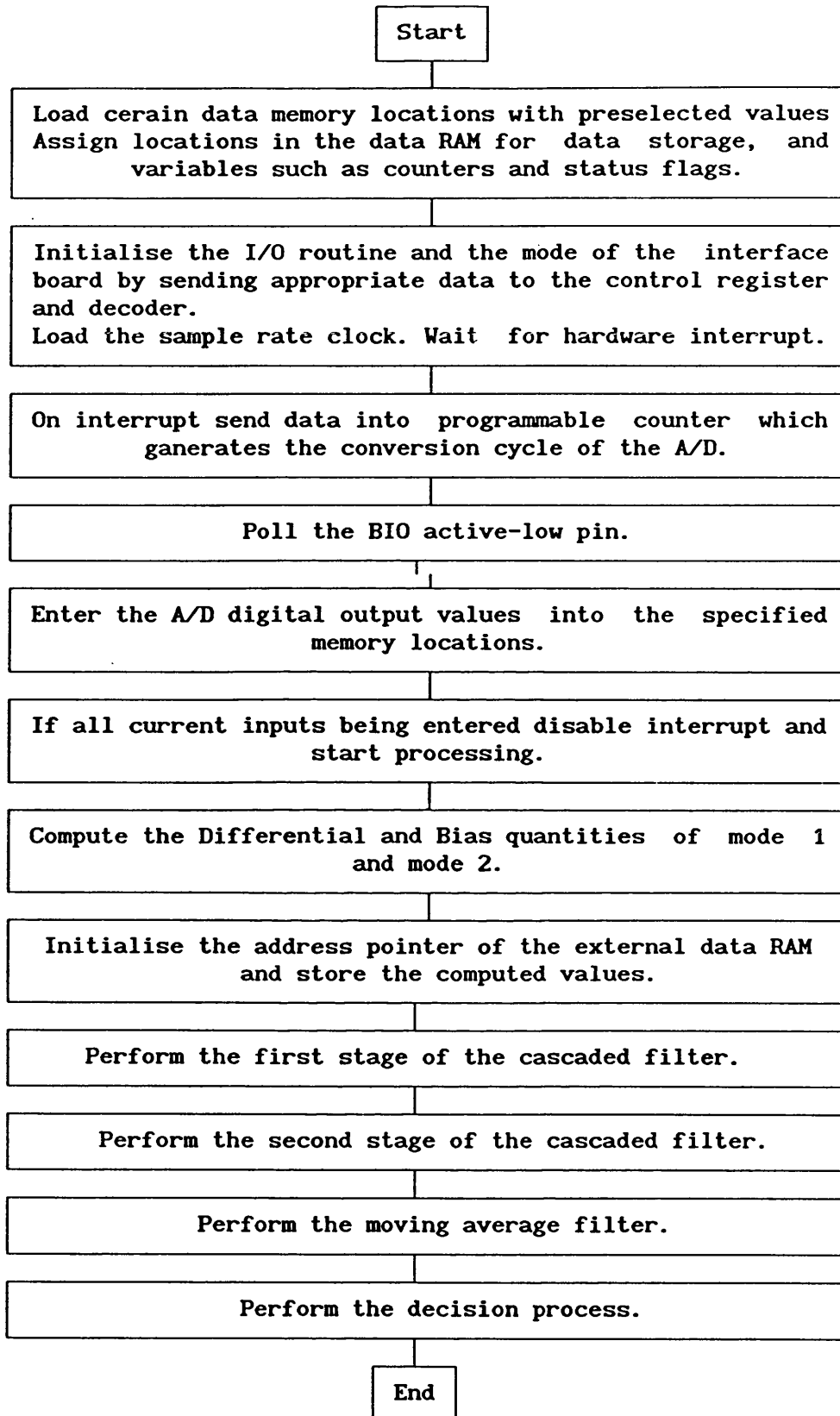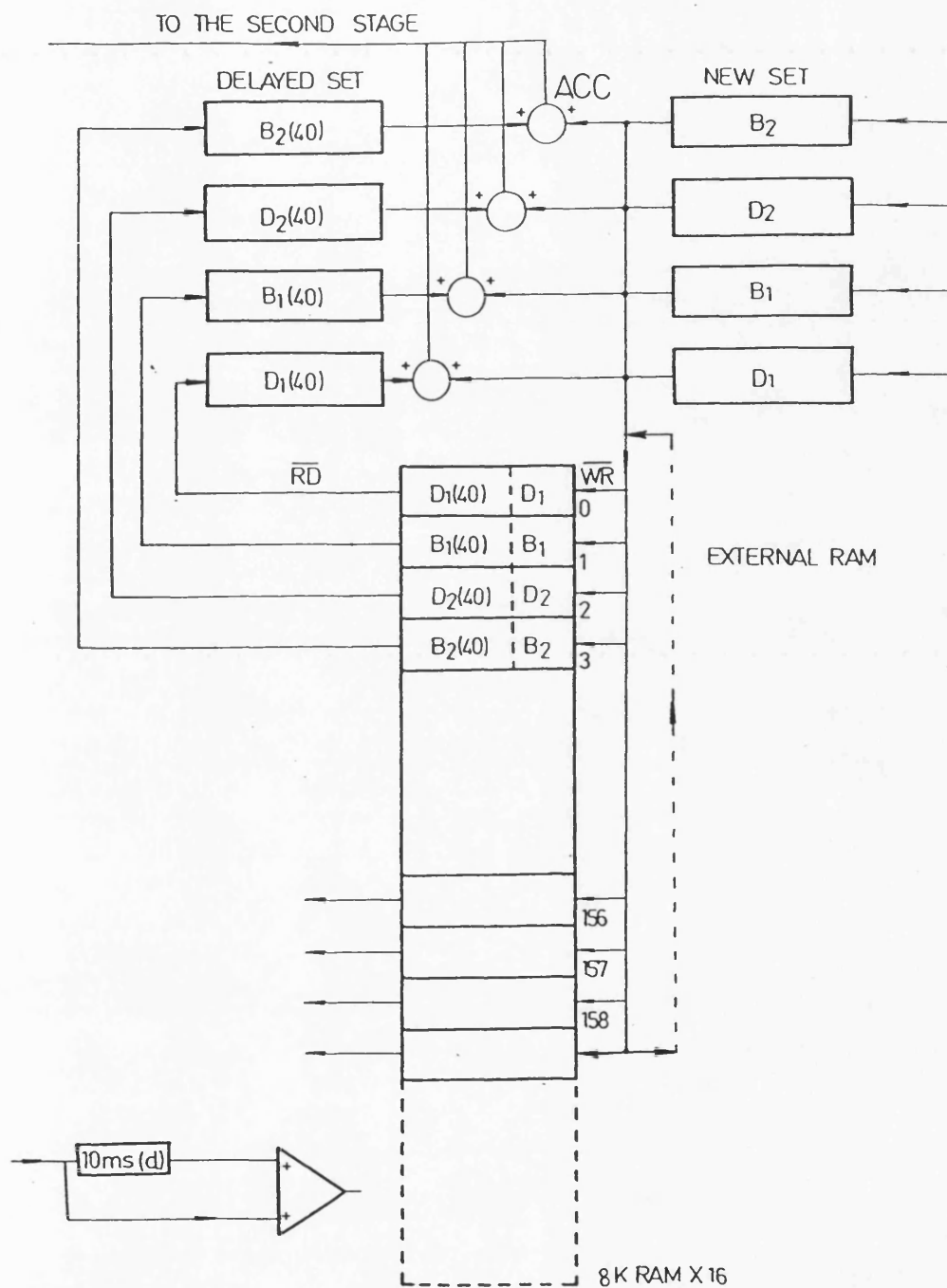
```
                      ┌─────────────┐
                      │    Start    │
                      └──────┬──────┘
                             │
┌────────────────────────────────────────────────────────────┐
│ Load cerain data memory locations with preselected values   │
│ Assign locations in the data RAM for  data   storage,   and │
│        variables such as counters and status flags.         │
└────────────────────────────┬───────────────────────────────┘
                             │
┌────────────────────────────────────────────────────────────┐
│ Initialise the I/O routine and the mode of the   interface  │
│ board by sending appropriate data to the control register   │
│ and decoder.                                                │
│ Load the sample rate clock. Wait  for hardware interrupt.   │
└────────────────────────────┬───────────────────────────────┘
                             │
┌────────────────────────────────────────────────────────────┐
│ On interrupt send data into  programmable   counter  which  │
│        ganerates the conversion cycle of the A/D.           │
└────────────────────────────┬───────────────────────────────┘
                             │
┌────────────────────────────────────────────────────────────┐
│              Poll the BIO active-low pin.                   │
└────────────────────────────┬───────────────────────────────┘
                             │
┌────────────────────────────────────────────────────────────┐
│ Enter the A/D digital output values  into   the   specified │
│                  memory locations.                          │
└────────────────────────────┬───────────────────────────────┘
                             │
┌────────────────────────────────────────────────────────────┐
│ If all current inputs being entered disable interrupt and   │
│                  start processing.                          │
└────────────────────────────┬───────────────────────────────┘
                             │
┌────────────────────────────────────────────────────────────┐
│ Compute the Differential and Bias quantities  of   mode  1  │
│                    and mode 2.                              │
└────────────────────────────┬───────────────────────────────┘
                             │
┌────────────────────────────────────────────────────────────┐
│ Initialise the address pointer of the external data RAM     │
│            and store the computed values.                   │
└────────────────────────────┬───────────────────────────────┘
                             │
┌────────────────────────────────────────────────────────────┐
│    Perform the first stage of the cascaded filter.         │
└────────────────────────────┬───────────────────────────────┘
                             │
┌────────────────────────────────────────────────────────────┐
│    Perform the second stage of the cascaded filter.        │
└────────────────────────────┬───────────────────────────────┘
                             │
┌────────────────────────────────────────────────────────────┐
│        Perform the moving average filter.                  │
└────────────────────────────┬───────────────────────────────┘
                             │
┌────────────────────────────────────────────────────────────┐
│           Perform the decision process.                    │
└────────────────────────────┬───────────────────────────────┘
                             │
                      ┌─────────────┐
                      │     End     │
                      └─────────────┘
```

Fig. 5.1    Relay algorithm flow-chart

TO THE SECOND STAGE

DELAYED SET     ACC     NEW SET

$B_2(40)$     +   +     $B_2$

$D_2(40)$     +   +     $D_2$

$B_1(40)$     +   +     $B_1$

$D_1(40)$     +   +     $D_1$

$\overline{RD}$     $\overline{WR}$

| | |
|---|---|
| $D_1(40)$ | $D_1$   0 |
| $B_1(40)$ | $B_1$   1 |
| $D_2(40)$ | $D_2$   2 |
| $B_2(40)$ | $B_2$   3 |

EXTERNAL RAM

156
157
158

10ms (d)

8K RAM X 16

$B_1$, $B_2$, $D_1$, $D_2$
are the present samples of the Bias
and Differential components of the
two modes

$B_1(40)$, $B_2(40)$, $D_1(40)$, $D_2(40)$
are the half cycle delayed samples
of the two modes.

Fig. 5.2   Half-cycle extraction circular filtering flow-chart
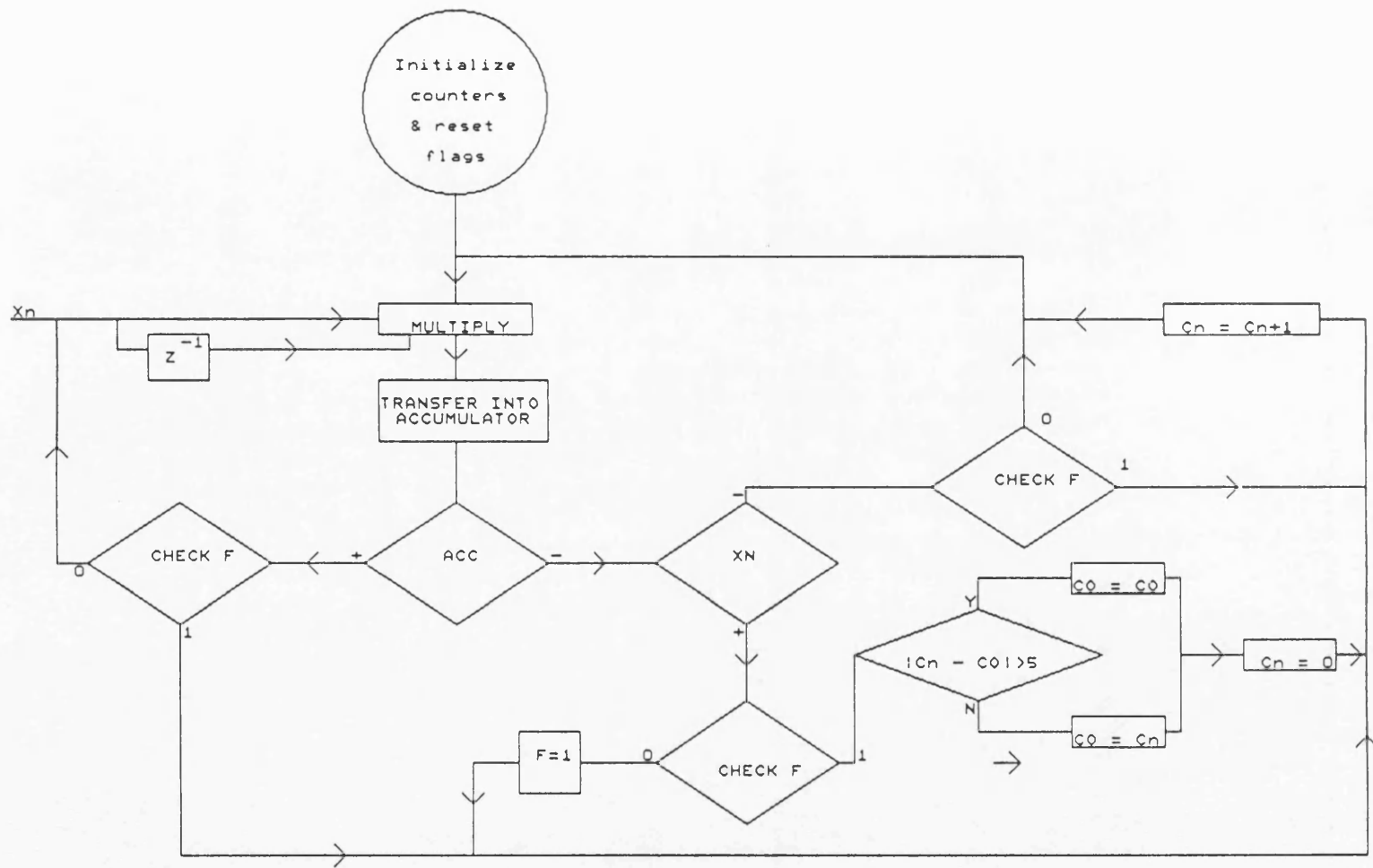
Fig. 5.3 Frequency tracking and sample rate correction flow-chart
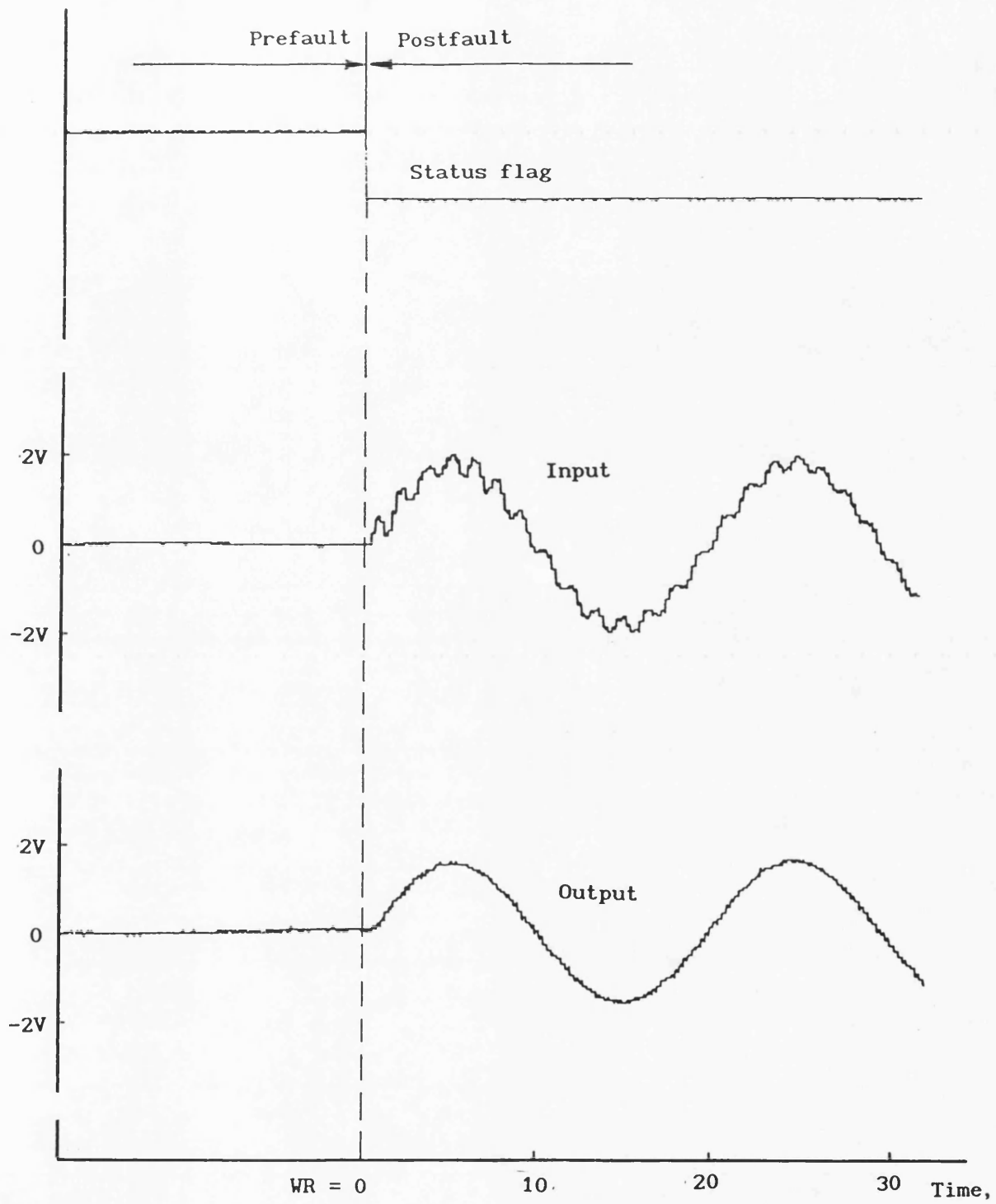
Fig. 5.4  Averaging filter function
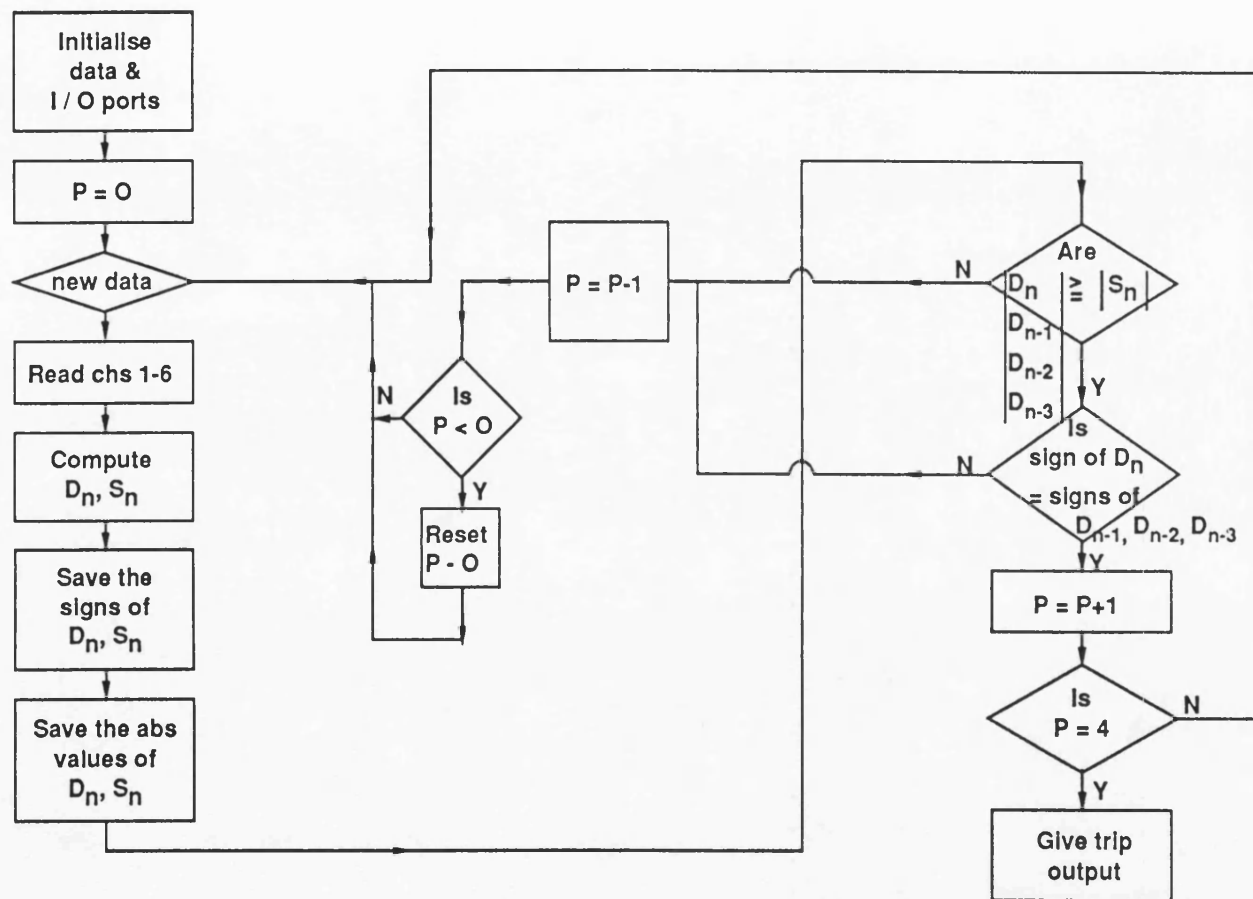
Fig. 5.5    Decision logic process flow-chart
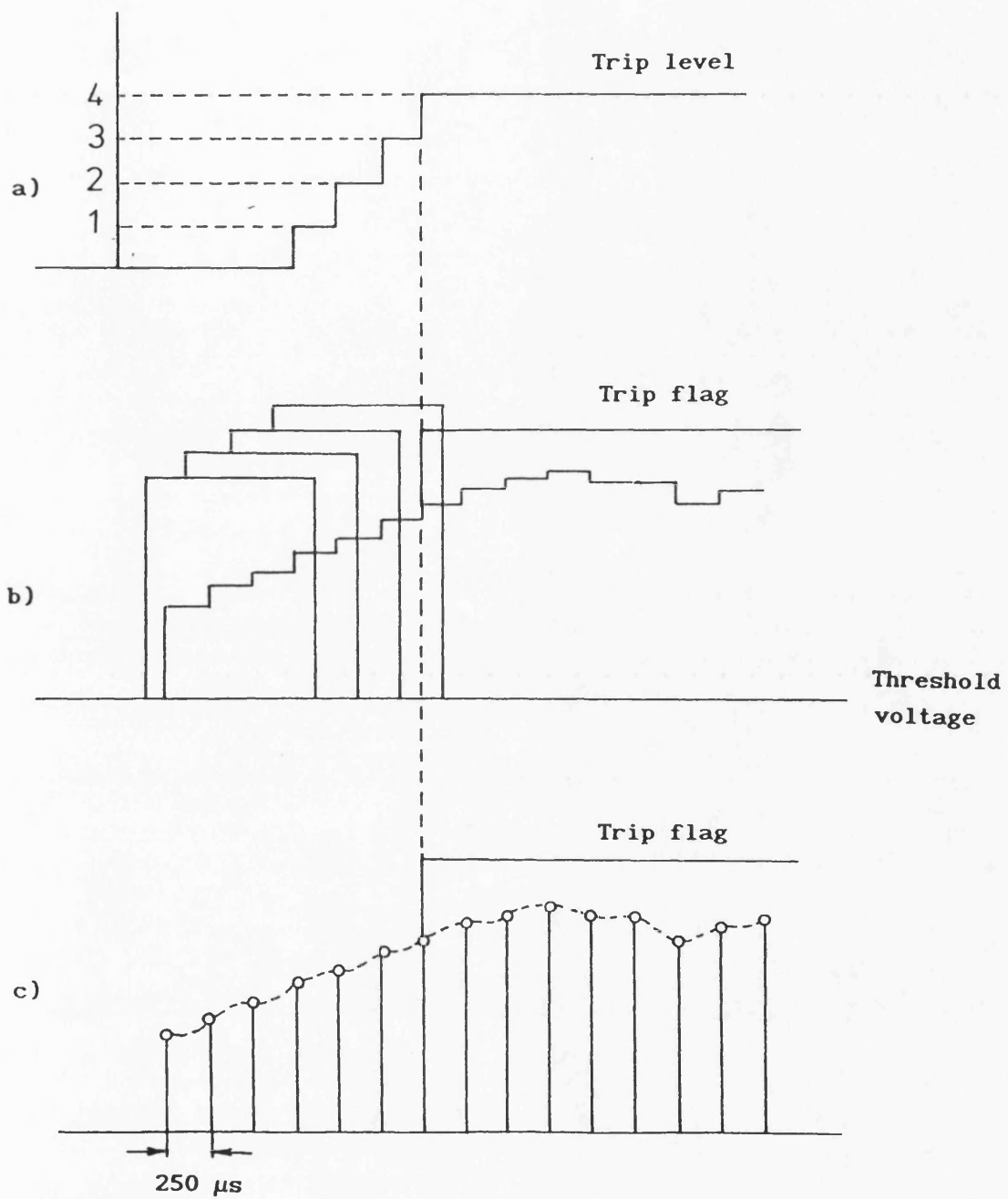
a) An internal fault counter

b) Sampled and held operating signal

c) Discrete samples operating signal

Fig. 5.6    Decision logic counter operation for an internal fault
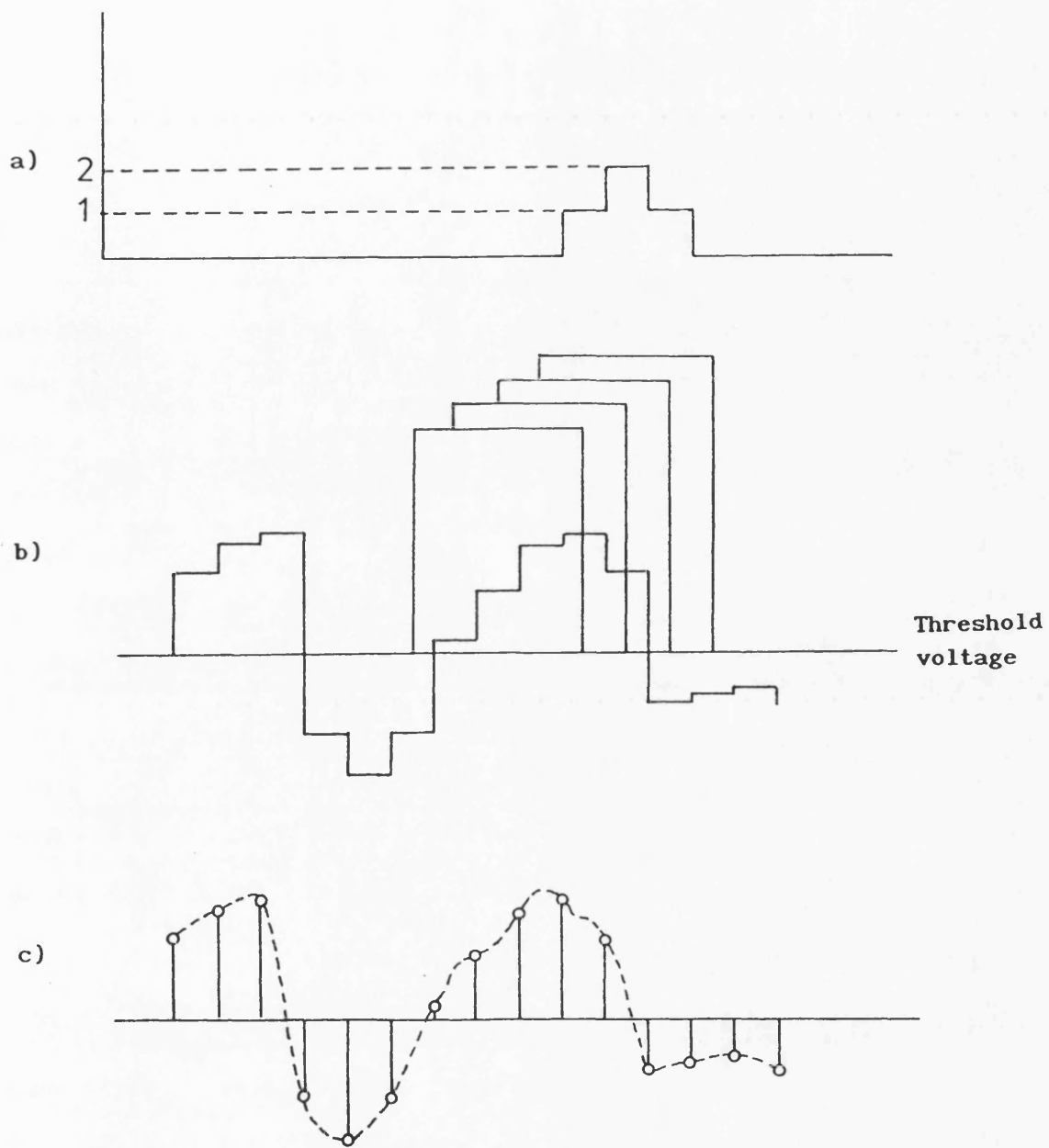
a) An external fault counter

b) Sampled and held operating signal

c) Discrete samples operating signal

Fig. 5.7   Decision logic counter operation for an external fault

CHAPTER 6


RELAY TESTING, PERFORMANCE AND EVALUATION


6.1  INTRODUCTION

Laboratory testing of the prototype relay has been divided into two
main parts. The first part is concerned with verifying that each
module functions correctly as a stand alone item, and the second part
involves testing the assembled equipment to ascertain whether it
gives correct decisions when it is subjected to current signals
corresponding to transmission line faults. This chapter outlines
briefly how each module has been verified and examines in detail the
protection performance as applied to typical teed-feeder transmission
lines, with special reference to the salient features which the relay
offers in comparison to conventional teed-feeder current differential
relays.


6.2  ANALOG AND DIGITAL CIRCUIT TESTS

The data acquisition unit as shown in  Fig. 4.1 forms the interface
between the transducers and the relay.  Firstly  the anti-aliasing
filters at the input of the relay were tested   to check whether they
gave an  identical performance in terms of frequency response, unity
gain, equal group delay and most importantly, a cut-off frequency of
1500 Hz. A signal generator provided the input for each filter and
the frequency was swept from DC  to 100 kHz and  since not all
resistors and capacitors adhere to their nominal percentage error,

it was necessary to alter some of these components to obtain similar responses for the individual filters. The S/H circuits, MUX, A/D and D/A were tested in two steps; firstly by directing their outputs to high precision equipments such as a digital voltmeter and and a digital analyzer as a primary test, and secondly with the aid of a microprocessor on which simple test programs were developed to verify their functions. The settling times of the S/H and MUX were taken care of by hardware logic and software delay element. The A/D was able to access the S/H output in the hold state for a number of times and the converted values were stored in the internal data RAM and read, and only the least significant bit of the A/D was found to fluctuate. This meant that the S/H did not experience a droop on its output value.

The A/D and D/A are provided by trimmer resistors for the control of their offset and gain circuits. The conversion process from analogue to digital has been initiated under program control at the nominal sampling rate and the resulting data is transferred from A/D output to the D/A input via the processor. This enables a direct comparison between signal input to the A/D and the output from the D/A, thus verifying that they function satisfactorily. The analog and digital circuitry are constructed on a single double layer P.C.B board; the analog and digital grounds have been isolated to ensure a system, free of noise. DC power supplies through voltage regulators and noise absorb capacitances provided the board with a range of DC voltages from - 15V to + 15V.

The external RAM has been tested by writing simple software programs

for the microprocessor under the control of the EVM. Data of known decimal or hexadecimal values stored in the program ROM were down loaded to the external data RAM and were then transferred to the internal data RAM at the nominal sampling rate. The program is then halted by applying a software break point just after the completion of the process. The registers of the internal data RAM are then compared with the prestored values. The two sets of values were identical, thus verifying the correct functioning of the process.

## 6.3  DIGITAL FILTERS AND ADAPTIVE SAMPLE RATE TESTS

In order to verify the correct functioning of the superimposed extraction filter, a constant 50 Hz sinusoidal frequency was generated and connected to one of the relay inputs. The relay operation was initiated under the nominal sampling rate of 4 kHz and the digital output of the cascaded digital filter was directed to the D/A converter and then displayed on the oscilloscope. A residual component of a few millivolts was found to be persistent on the filter output. In theory, the output should settle to zero value but for a practical filter, there is some noise at the output which can be attributed to two factors; these are analog circuitry noise and A/D quantization errors.

As for the frequency tracking, the adaptive sample rate test was verified by providing the relay with a variable sinusoidal frequency in the range of 40-60 Hz. The frequency was swept gradually in steps of 1 Hz and the sampling rate was found to adjust to the new frequency retaining the required number (80 ± 1) of samples per

cycle. For the verification of the averaging filter, the relay was tested under real-time operating signals obtained from a teed-feeder fault transient data which contains spikes and high frequency transients which, prior to the application of this filter, were significantly noticeable due to digital noise and truncation errors and in particular, noise incorporated on the relaying signals during external faults. The function of the filter is clearly seen to attenuate the transients on these signals (see Fig. 5.4). The decision process and decision counters were tested purely in the software and proved to perform satisfactorily.

## 6.4 PRIMARY SYSTEM WAVEFORMS

It is of paramount importance during the research and development of high speed digital protection systems, that the voltage and/or current waveforms presented at the relaying point can accurately represent the real signals presiding on a power system network.

The ultimate judgment of a relay operation is to test its performance under field trials, but during development of a prototype relay, this imposes economic and technical constraints. In the past, analog test benches were used and deliberate faults were thrown on the network to check the relay response. Such equipment, as developed for example by Hamilton and Ellis [34], comprises of lumped inductances, capacitances and resistances to represent the source and line impedances and some of the draw backs of this method are :

a)    It is quite impractical and expensive to create an analog model

for a variety of possible network configurations.

b) Unlike in conventional slow operating relays, HS relays make their decision in the presence of some transients which preside on power system networks. It is impossible for analog testing benches to accurately generate such transients.

c) Very often, during analog testing, errors may arise from CT saturation and power amplifiers overloading.

The test bench however, may be useful for testing equipments with relatively slow response time which are not particularly affected by high frequency transients.

Off line digital simulation is considered as the most appropriate method for power system modelling. A CAD simulation package for both three and two terminal transmission lines, has been developed at the University of Bath [34], with the aim to derive precise current and voltage information of different EHV power system network configurations before and after a fault. A detailed study of the simulation is beyond the scope of this thesis but some of the salient features which directly influence the performance of relay are outlined below.

In this simulation, modern transmission line theory is used to accurately predict the fault transient behavior of 3-terminal EHV overhead lines. Full advantage is taken of the many years of experience in the development of sophisticated simulation programs. These programs have been developed from the studies of Wedepohl [19]

which have been refined by several researchers. Initially, these studies were used to consider the effects of restriking voltages, switching overvoltages, radio interference and the propagation of transmission line carrier signals. Later they were expanded to cover the effects of fault induced transients on high speed protection apparatus for the protection of two terminal lines [ 6,7,16,20,23]. The programs are based on the solution of the wave equations using the Superposition and Thevenin theorems. Matrix analysis together with inverse fourier transform techniques are used to transform the solutions from the frequency domain to time domain, in a form suitable for digital computation. The techniques consider the physical arrangement of the conductors, the characteristics of the conductors, The effect of earth- return path, and the effects of frequency dependant parameters. The effect of frequency variance of EHV line parameters is established. The various factors such as effect of fault type, differing source capacities at the three ends, unequal line lengths up to the tee point, and feed-around paths, which influence the transient phenomena, are considered.

The current waveforms presented to the relay are related to some typical 400 kV 3-terminal line configurations. An outline of the theory behind the simulation is presented in Appendix A. The results of this simulation technique have been validated with actual field data  and the computer modelling is essentially an extension of that described by Johns and Aggarwal [33] for two terminal lines. The simulation programs are executed on a mainframe computer and the resultant data is  then transferred to the PTL for relay testing.

## 6.5 TEST EQUIPMENT (PTL)

So far, the PTL has been considered as a black box which provides the input current signals to the relay. The advances in digital computer simulation techniques in conjunction with the newly developed PTL test equipment can enable highly realistic power system waveforms to be accurately simulated and produced in analogue form in the time domain. This section gives some details about the PTL development, its structure and how it operates.

### 6.5.1 PTL development

A PTL is a programmable transmission line equipment based on a desk-top computer which transforms data generated by digital simulation program into current and voltage signals which can then be used to test various types of relays. Such equipment is a laboratory test facility which enables inexpensively, to evaluate the performance of a power protection system under fault conditions. A major advantage inherent in the PTL concept is that it uses a software rather than a hardware power system model.

The PTL current and voltage outputs can be made to correspond to signals found at any point in the power system. The power system configuration can be changed as desired. This overcomes many of the practical problems of the artificial transmission line (ATL) where the interaction between the ATL and the relay under test is limited and is liable to mains-borne interference.

Many researchers have been working on the development of PTL systems

[35-38]. However, until recently, most PTLs worked in a semi-automatic way.

Off-line fault simulation and computation is done separately on a powerful main frame computer, and the resultant data is arranged in a digital format suitable for running in real-time. With the advent of very high speed transputers, research is in progress for the integration of the two processes for full automation in real-time. The PTL used here for testing the relay was developed at Bath university laboratory [37,38] and a brief description of its operation is given below.

### 6.5.2 PTL hardware and software

A simplified block diagram of the system's hardware is shown in Fig. 6.1. It comprises a high speed IBM-AT desk-top microcomputer fitted with a specialised interface system which includes 12 bit D/A converters, 16 bit digital input and output channels, current and voltage amplifiers, control circuits and a relay status monitor. The system is based on an 80386 processor, is capable of directly addressing one megabyte of program memory in blocks of 64 kilobytes and provides a simple man-machine interaction.

The specialised interface unit is a third party interface card consisting of 6 parallel D/A converters which are configured to provide an output voltage in the range of ±10 V with a settling time of 3 μs. These are provided with latches which enable the synchronization of the output data with the PTL sampling clock.

The maximum sample rate which can be produced by the PTL is governed by the duty cycle of the control program which is responsible for running the data in real-time, and with the master clock capacity.

The control program was written in assembly language to give a minimum duty cycle. The sampling clock is derived from a master clock circuit which uses a crystal controlled oscillator. The oscillator runs at 12 MHz and this frequency is subsequently divided down to give variable sample rate. The divider is automatically set at run time to match the sample rate used in primary system program simulation.

The digital channels are provided for interfacing with the tested relay and for the control of the PTL operation in real time. The current and voltage amplifiers were designed to provide high fidelity outputs within a range of dc to 4kHz. The software process is shown in a simple flowchart as shown in Fig. 6.2. More details of the system hardware and software are given in the attached IEEE paper in Appendix C.

## 6.6 RELAY-PTL INTERFACE AND TESTING PROCEDURES

The simulated current waveforms produced as the output of the main-frame should be reproduced by the PTL at the same frequency they have been simulated, otherwise the data should be manipulated, to give correct information. The data manipulation can be performed either off-line or on-line. For example, if the current waveforms generated at a rate of 12 kHz are to be regenerated by a sample

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rate of 6 kHz, then every next sample of data generated at 12 kHz should be skipped during data preparation.

The primary system currents (results of program simulation) are regenerated in analogue form using 12,000 samples per second on each channel. This provides 240 samples per cycle for a 50 Hz system or 200 samples per cycle for a 60 Hz, and thus it ensures sufficient bandwidth for the reproduction of high frequency transients.

No software interpolation was performed on the PTL output to deal with the steppy nature of the waveforms produced by the D/A converters, for two reasons; one is that the sampling rate was high enough to reduce this effect and secondly because the Butterworth filters implemented at the input of the relay attenuate any harmonics above the cut-off frequency of 1500 Hz.

The primary system current waveforms were organized in data packs so that the size could be limited to manageable proportions. For periods when the current waveforms can be assumed to be steady state, (prefault or postfault) only one cycle of data i.e. 20 ms period for 50 Hz, is stored and this is recycled to produce a continuous signal. For the fault period which includes the fault point and the fault related transients, unique data is used. The data pack is therefore organized into a short directory of key addresses, the pre-fault steady-state data, the unique fault related data, and the postfault steady-state data.

The digital output of the PTL provides a logic output which acts as a status flag. This operates in parallel with the waveforms which are

fed to the relay under test. The logic high level indicates the relay is operating under prefault data and the low level indicates the relay operation under fault transient time and post fault data. The transition from high to low indicates the point of fault occurrence.

The data status flag logic of the PTL was routed to the status input register of the relay to provide a dynamic interaction and also to the oscilloscope which monitors the relay signals to act as a reference. The operating time is measured from the negative going edge which indicates the position of the fault point on the waveform.

The testing technique used for the total component version is common for testing protection relays. The presence of the status flag is not essential for the relay to start the DAS program and any duration of prefault data is acceptable.

For the superimposed component relay version, the relay requires at least one and half cycle of the prefault period for the response of superimposed extraction filter to settle to zero value. This means that for a 50 Hz transmission system, the relay requires a minimum of 30 ms of pre-fault data.

Moreover, the prefault data time must be well above 30 ms in order not to cause a false relay trip which may result from the convolution of the post fault data on the prefault data when the program is running without interruption during recycling of the waveforms. This is an essential procedure for most relays which require past history data.

## 6.7 RELAY SETTINGS AND DATA SCALING

Although in practice, The relay under test comprises a current interface module (CIM) to convert the outputs from the main line CTs into equivalent voltages, however, for the relay prototype model described here, emphasis has been placed on the relay hardware and software operation. The effects of both CTs and CIMs on the relay input signals have nonetheless been included by extending the primary system simulation of the fault transient current waveforms.

The frequency responses of the CTs and CIMs have been generated from tests carried out on a practical model of the equipment whose block diagram and frequency response are shown in Fig. 6.3. The CIM comprises a transformer-reactor (transactor) core which has an air-gap of 5 mm, so that the reluctance of the air-gap dominates that of the core material.

The CIM produces a flat response to within $\bar{+}$ o.5 dB from 2.5 Hz to 1kHz. This bandwidth was considered to be sufficient since current waveforms are generally dominated by low frequency components. It should be mentioned that this approach is justified and gives an accurate indication of what actually happens in practice.

Also the CIM comprises 2 back-to-back zener diodes at its output. These diodes clamp the feedback capacitor voltage to $\mp10$ volts. This arrangement is necessary during internal CT saturation.

## 6.7.1. Relay sensitivity setting factor $K_i$

The current gain of the interface module is the only application dependent setting that the scheme possesses. It is set so that there is no case where current clipping occurs at any end for external faults.

The latter requirement is met by first performing a simple steady state study to determine the maximum possible external fault current. For example, if in Fig. 6.4-b, the short circuit levels quoted are the respective absolute maximum levels, then the maximum possible through fault current would occur at end R for a solid three phase fault on the R busbar. This would give a maximum current through the end R CT of approximately 15kA in any one phase allowing for current doubling under conditions of full exponential transient offset. Thus, for a 2000/1 CT ratio, the interface gain $K_i$ will be set to a value of $10/(15.10^3/2.10^3) \simeq 1.3/secA$ in order to keep within the ±10V range of linearity. In this way, absolute stability for all external faults is guaranteed and the relay retains maximum sensitivity to all internal faults. The results herein presented are for two typical settings in 400kV, 2000/1 CT ratio applications of $K_i = 1$ and 2V/secA.

## 6.7.2. Modal sensitivity circuit gain

The modal mixing gain is a fixed internal gain equal to $1/\sqrt{3}$ which ensures that once the currents have been converted into voltages, the modal signals thus formed are always within the range ∓10V. The

necessity for this reduction by the factor of $1/\sqrt{3}$ arises because the modal signals, being the difference of phase values can be up to $\sqrt{3}$ times the latter. It thus ensures that the input to A/D converters never exceeds their 10V rating.

### 6.7.3. Bias constant and setting levels $K_B$, $K_S$

The Bias constant $K_B$ and the threshold value $K_S$ were raised slightly from their theoretical values of those as discussed earlier in chapter 3 to accommodate for the practical noise. Following an extensive series of tests on the relay module so as to maintain stability of the relay for a majority of external faults, it was found necessary to set $K_B$ to 50% (compared to 25% for the CAD model; see ref [16]) of the bias signal and $K_S$ was set equal to 80 quantum levels for the superimposed components and 100 quantum levels for the total components (compared to 65 and 80 levels for the CAD model). A direct consequence of these increased levels is that although the relay is stable for practically encountered external faults, however, it becomes less sensitive to high resistance faults.

In the relay design described here, the sensitivity/stability trade-off is improved with the use of an automatically variable scaling factor. This approach has the effect of a variable threshold voltage level and allows a lower setting of the threshold voltage thus increasing relay sensitivity to low levels of fault currents associated with high resistance faults, without affecting the relay stability. In practice, this is achieved by using the upper half of the accumulator to perform the computation whereby if one or both

relaying signals are of high value, an overflow will occur, causing the scaling routine to be invoked.

In order to keep the consistency of the comparison process between the relaying quantities, when the computation of one causes an overflow, the scaling is applied to both the Differential and the Bias signals. This method thus extends the coverage of faults occurring through high resistances and has a major advantage over the conventional approach in which the threshold levels are fixed.


## 6.8 LINE CONFIGURATION AND FAULT TYPES


### 6.8.1 Teed-circuit configurations

In a complex power network, a multitude of possible circuit configurations can be expected with faults occurring at various positions on the teed circuit. It is by no means possible to demonstrate the relay performance for all the possible circuit configurations but it will be sufficient to present the relay operation for a few internal and external faults, for two complicated configurations shown in Fig. 6.4. Such configurations have been specifically chosen because of their non-symmetrical nature in terms of source capacities, different line lengths up to the T-point, outfeeds paths which are likely to pose some of the difficult protection problems associated with teed-circuits. In this respect, it is worth pointing out that symmetrical teeds with equal lengths to the T-point and equal source capacity terminations can be relatively easily protected using present generation relays, some of which have

been introduced in Chapter 2. Also another reason for choosing these two configurations is to carry out a comparison between the results produced by the CAD model [16] which also concentrated on the same two configurations and those considered here in the relay hardware design, thus facilitating a validation of the hardware outputs.

### 6.8.2 Fault types

Since in practice, the fault levels on a system are affected by different system and fault conditions such as source capacities, types of faults, the presence of feed-around paths, etc., it is therefore very important to examine the protection performance, particularly in terms of reliability and sensitivity, under a whole variety of such practically encountered systems and fault conditions.

Furthermore, the correct relay performance must be verified by testing it on a variety of faults conditions both internal and external to the protected circuit.

The most common faults which occur on a transmission line are of the phase-earth faults. The relay described here will thus be subjected mainly to such faults and its performance examined in some detail for such faults. Also the relay will be tested for a few other important fault conditions which would demonstrate its distinct advantages and superiority in comparison to the conventional current differential relays.

### 6.9 RELAY PERFORMANCE AND EVALUATION

The relay overall performance must be judged on the fundamental

requirement that its output decision must be correct and a discrimination exists between internal faults and external faults. The output decision is a mere integration of the relay modules operation. A step by step evaluation of every module for every fault type is a cumbersome process, but it is possible to break down the evaluation of the relay into a limited number of illustrative studies, which are briefly described below.

In order to fully appreciate the measuring processes implemented and the operation of the scheme, it is useful firstly to present the primary system waveforms of some typical faults for a particular line configuration. Representation of the digital outputs of the relay in an analog form are obtained as mentioned before (see Fig.4.11) by directing these samples to the D/A converter and the plots are given here with a summary of fault conditions.

The Differential and Bias signals or their superimposed components are shown accompanied by a status flag, high on the prefault time and low on the fault and post fault time. The relay operating signals for internal faults are shown followed by a tripping signal and the value of the tripping signal is shown to be 5 volts. This value is chosen arbitrarily and it can be set to any value not exceeding 10 volts which is the limit of the D/A converter.

As previously mentioned, some intermediate scaling was necessary to prevent digital overflow and enhance the relay sensitivity. This process is carried out automatically inside the relay. Whenever this process is applied to a signal, it is also

applied to any other signal which is related to it, i.e. If the differential signal is scaled then the bias signal must also be scaled by the same factor in order not to affect the comparison process. Due to this pre-scaling process of the samples, any quantitative comparison must thus be done on a ratio basis.

### 6.9.1 Relay response for an internal fault ( Single phase-earth)

Figure 6.5 represents the line current waveforms for a fault at the T-point of the teed configuration shown in Fig 6.4a, the fault being at $V_{a90}$°

The system modal currents for such a fault are shown in Fig. 6.6 and for the sake of brevity, only the outputs corresponding to mode 1 of the relay measurands are presented. The relay outputs of the total components and superimposed components versions for this fault condition are shown in Fig 6.7. As expected, the signals remain small throughout the prefault period but become significantly finite on fault inception, the magnitude of the bias signal being much smaller than that of the differential signal.

In the case of the superimposed quantities, there is a finite output for only about half a cycle of power frequency, this being due to the nature of the extraction filter employed and it can be explained by the symmetry attained by the post fault waveform. The superimposed component filter outputs gradually die out after a half power frequency cycle has elapsed. This is so because in the postfault

data, the fundamental frequency is still dominant and it can be totally extracted by the cascaded filter.

The relay outputs also interestingly show the presence of some current clipping experienced for this strong fault condition, this being reflected in both the differential and bias components by the flat positive and negative peaks of the relaying quantities. The operate signal Op(t) stays below zero during the prefault period and rises sharply on fault inception to give a trip output at approximately 2 ms when the counter reaches a count of 4 for a moving window of 4 samples. This is a counter level which effectively corresponds to 7 sampling intervals. During this period, the operating signal is above the threshold voltage and is of the same polarity. The decision process and counter operation are as described in Figures 5.5, 5.6 in Chapter 5.

The trip signal is shown here of 5 volts and the tripping time of the superimposed component relay is slightly lower than that of the total component relay. It must be mentioned that these are the times taken by the decision logic counter to give a trip decision and in practice a time of approximately 2 ms must be added to in order to cater for the communication channel delay time.

On comparison with the CAD study outputs, it can be clearly seen that both the differential D(t) and bias B(t) signals from the hardware model very closely correspond to those produced from the simulation studies and this is true for both the total and the superimposed variations of the signals.

The slightly steppy nature of the of the outputs in the case of the former is due to the conversion process of the D/A converter when the digital information within the microprocessor is converted into an analog form, for the purposes of displaying the waveforms. In this respect, an output value is sent to the D/A at the end of every sampling interval and this gives a flat response on the signal until such time as the D/A responds to a new computed output value. ALso the tripping times are slightly higher than those attained from the CAD study, because as mentioned before, in the hardware design, the threshold levels had to be raised slightly so as to counteract the presence of small values of practical noise.

The results nonetheless prove the correct design of the hardware and its associated protection relay software.

It should be noted that a close inspection of the system modal currents have shown that the mode 2 currents for this type of fault are similar to those for mode 1 and the relay would therefore be expected to operate in a similar manner. with identical operating times.

## 6.9.2 Relay response for an external fault (Double phase)

Fig. 6.8 shows the primary system currents for an external phase-phase, $V_{b-c0}°$, fault close to the end Q of the circuit shown in Fig. 6.4b. The derived modal currents are also shown in Fig.6.9 and the relay measurands of the hardware are presented alongside those generated by the CAD model in Fig. 6.10, for comparison purposes.

Here again, the differential, bias and their superimposed components of mode 1 are shown with their respective operate signals. Again as expected, the signals become finite only on fault inception, the magnitudes of both the Differential and Bias signals, however, being much smaller than those for an internal fault. It is interesting to note that for this external fault condition, whilst the Bias signal is predominantly at power frequency, the much smaller Differential signal comprises very distinct high frequency components which rapidly change in polarity, the latter being a characteristic of the external fault differential current in high speed current differential relaying. There is of course no clipping of the signals because as mentioned before, the CIM gain has been carefully chosen to prevent clipping for the worst case external fault condition. However, the nature of the signals is such that the operate signal Op(t) never consistently exceeds zero in accordance with the trip logic, to assert a trip decision. On comparing the relaying signals with the CAD outputs, the figure again clearly shows a very close resemblance between the measurands, thus further verifying the correct function of the hardware model.

### 6.9.3    Phase a - earth faults at different points on wave

The phase a - earth faults were applied at the T point of the teed-feeder configuration shown in Fig. 6.4b. The Tests were performed for around the clock different inception angles ranging from 0 to $360^{\circ}$ in steps of $30^{\circ}$. Fig. 6.11 shows the variation of the relay operating time with point on wave of fault.

It can be seen that the relay operating time is nearly constant for the majority of fault inception angles but increases as the inception angle approaches the zero degree point on wave. This phenomenon can best be explained by considering the operating signals for three faults at $0°$ inception angle, $90°$ and $160°$ inception angles respectively. In the case of the first, (see Fig. 6.12, 6.13 and 6.14), the Differential quantity quickly exceeds the zero level to become positively finite and since the operating quantity is directly related to the Differential being finite and of the same polarity it gradually exceeds the threshold voltage. Likewise in the second case, again the Differential signal almost instantaneously exceeds the zero level, with a much higher magnitude than the Bias signal and thus the derived operating signal behaves similarly. However, for a fault inception angle of $160°$, the Differential signal suffers from a reversal in polarity in that it goes marginally positive for approximately 2ms before it becomes negatively finite, thus making the operating signal exceed the threshold voltage after some time delay to initiate an up count. On polarity reversal, however, the threshold level is exceeded which in turn then initiates tripping after an additional delay of approximately 2 ms. It should be mentioned that the relay operating times shown in Fig. 6.11 also indicate a communal delay time of 2 ms.

Generally speaking the relay operating times for different inception angles are more or less identical and the relay offers fast fault clearance; This is so because the relay works on the the difference of the absolute values of the relaying quantities ( the Differential

and the Bias) being greater than a threshold voltage and not on their relative difference only.


## 6.9.4 Relay response to other types of fault

### 1) An Internal three phase-earth fault

Although three phase faults are quite uncommon in power system transmission lines, it was nevertheless interesting to see the performance of the relay when subjected to such faults. Fig. 6.15, shows the primary system currents for an internal three-phase-earth fault at the T-point of the teed configuration shown in Fig. 6.4-a. The derived modal currents are shown in Fig. 6.16 and the clipping of the modal currents at end Q which is the high capacity source, can be clearly seen. Furthermore, it is evident that from figures 6.17-a that the differential quantity when derived within the hardware has caused an over-flow due to the system currents being high in the first instance. Fig. 6.17-c and 17-d however show both the Differential and Bias signals after being automatically scaled down to avoid any overflows. The over-flow of the accumulator when deriving the Differential signal for a three phase-earth fault is a clear indication of the severity of such faults.

From close inspection of the scaled superimposed relaying quantities shown in Fig. 6.18 it is evident that due to the extreme severity of this type of fault, there is no symmetry on the postfault signals between the positive and negative half cycles of the power frequency. Furthermore, unlike the case of less severe faults, such as a single

phase-earth, in which the superimposed components are finite for only half a cycle (see Fig. 6.7), the severity of the three phase fault manifests itself into giving a significant residual output for approximately one cycle after a fault, again as shown in the Fig. 6.18. This, however is of no consequence as far as this high speed relay is concerned.

## 2) Effect of CT saturation

Current distortion from CT saturation can cause maloperation of line protection relays. Such effects are generally more troublesome in slower conventional protection relays but it is nevertheless necessary to ensure that in HS protection, CT saturation caused for example under conditions where an external fault is slow to clear, does not cause relay instability. In order to determine the likely effect of CT saturation, the relay was subjected to fault waveforms causing an extreme degree of CT saturation and in order to induce saturation, an exceptionally high, pure resistive burden of the order of 150 VA (at rated 1A secondary current) was assumed. This caused the model CT (Fig. 6.3) co reflux to quickly reach saturation level. The saturation effect was studied for two typical faults, close to end Q of the teed-circuit configuration shown in Fig. 6.4-b one is internal to the protected zone and the other is external.

## a) an internal fault

Problems for internal faults are not anticipated because the HS relay operates well before the onset of CT saturation in any

practical situation. Figures 6.19-a and b, show respectively the core

flux and CT secondary output for a double phase fault (close to end

Q), between the phases b and C at $V_{bc0}0$ and it is evident that the

CT core flux at end Q very quickly reach the  saturation level.  The

CT output currents totally collapsed to zero, during saturation again

as shown in Fig. 6.19-b  thereby giving a more onerous test condition

than  is  actually  the  case  in  practice.  On  considering  the

Differential  quantities  of  the  total  current  variations  and  their

superimposed  components  shown  in  Figures  6.20-a  and  6.21-a

respectively, it can be clearly seen that a  correct decision    is

taken by the relay to recognize the fault as an internal fault in a

very short period of time, well before the magnitude of these signals

sharply decreases to near zero level, due to saturation, and this is

clearly shown by the decision counter reaching a the trip level of 5

volts in approximately 2 ms. These results thus also show the merit

of sampling at a higher sampling rate, clearly  a distinct advantage

over  the  slow  speed  conventional  protection  relays,  which  under

such conditions are likely to fail.


## b)  an external fault

In order to determine the likely effect of CT saturation caused by a

fault external to the protected zone, the relay was subjected to

fault waveforms causing an extreme degree of CT saturation again  at

end Q of the Tee configuration shown in Fig. 6.4-b.  The fault type

is similar to the aforementioned case in that  it is a  b-c- phase

fault at $V_{bc0}0$. The CT core flux gradually increases to saturation

level,    as shown by Figure 6.22-a, and   the CT   output currents totally collapse to zero for the short saturation period again as shown in Fig. 6.22-b.

First of all,  considering the differential signal as shown in Fig. 6.22-c it can be clearly seen that, as expected , it remains near zero even after fault inception, until such time as the onset of CT saturation, whereby large, short duration pulses are introduced into the signal. These pulses cause the differential signal to momentarily exceed the dynamic threshold signal, but the decision logic prevents the relay from giving a false trip decision. This is apparent from the Operate signal Op(t) (Fig. 22-e for the total components and Fig. 22-h for the superimposed components) which although can temporarily go positive, yet never sustain a positive value for a long enough time for the counter to attain the required level to give a trip decision.

Following some extensive investigations for  such faults on the hardware model, it was found that if the spike on the differential signal sustained a high level for a  duration longer than the minimum time required to issue a trip flag, there was a likelihood of a false trip. The following two solutions were thus considered in order to increase relay stability for such faults:

The first obvious solution is to increase the number of samples upon which  the relay takes a decision.  This however gave a slightly longer tripping time and the relay's  coverage to high resistance faults was considerably reduced.  An alternative solution, which did

not affect the coverage to high resistive faults, was to implement a moving window averaging filter whose design is explained in Chapter 5. Applying this new filter, the stability of the relay was significantly enhanced without sacrificing either its speed or its high resistive fault coverage. The effect of the averaging filter can be clearly seen in Fig 6.23 where only the high frequency components are attenuated and the spikes due to CT saturation have been largely reduced.

## 3) Effect of source capacity variation

Fig. 6.24 shows the relay performance for various source capacities. With respect to the teed configuration shown in Fig. 6.4-b, it can be clearly seen that with the relay setting based on 20 GVA, and with end P source capacity set to 20 GVA, high speed performance is attained for faults occurring between end P and the T point. However, as the end P source capacity is reduced the operating times become progressively longer and the HS performance is no longer achievable, if required for one cycle clearance, for a source capacity below about 2 GVA. In this respect, it should be noted that for systems terminated in weak sources (i.e < 2 GVA ), it is rather impractical to base the relay setting on very high short circuit levels terminations, such as 20 GVA. It would in fact be more appropriate to set the relay compatible with a system with absolute maximum source capacity terminations of say 10 GVA.

## 6.10 OTHER NOVEL FEATURES OF THE RELAY DESIGN

The relay has a number of distinct advantages over conventional current differential relaying and other types of protective schemes as applied to teed circuits. Besides its immunity to CT saturation, it also has the following distinctive features:

I) Immunity to the presence of feed around paths.

II) High fault resistance coverage.

Although, originally, these advantages were ascertained using CAD studies, nonetheless, it is important to verify that this is also true in practice.

### 1) Effect of a feed-around path

For certain internal fault conditions, a feed around path can cause non-unit type relays to see a fault as if it were external to the protected teed circuit. Consider the teed circuit configuration shown in Fig 6.4-a, for a fault at the T-point and at 1 km from end P. The primary system current waveforms are those shown in Fig. 6.25-d,e,f. It can be clearly seen that there is a reversal in the polarity of the phase currents at end R only, as the fault, which is an a-phase -earth fault at voltage maximum, moves from the T-point to a location close to end P. This is due to the current fed to end R via the feed-around path becoming stronger as the fault moves closer to end P.

This effectively means that in certain types of non-unit protection

relays and Directional comparison relays, the relay at end R would incorrectly indicate an out-of-zone fault condition. In the case of the relay described here, however, it can be seen from Fig. 6.26g-j that both the Differential and Bias signals are unaffected by the current reversal in that the relay gives high speed decision, this being so for both the total and superimposed current variations.

## 2) Relay fault resistance coverage

A series of resistive faults were applied to the prototype relay to examine its sensitivity to high resistance faults. It is clear from the results shown in Fig. 6.26, that the relay hardware performance in terms of operating times and fault resistance coverage, is more or less in accordance with that predicted by the theoretical design. The small differences in performances are however, expected by virtue of the fact that in the hardware design, the threshold levels are slightly higher than those for the relay based on CAD studies, this requirement be necessary to compensate for the generated practical noise. The relay performance based on superimposed components is nonetheless superior to that based on total components, again as evident from the figure.

## 6.11 RELAY PERFORMANCE ON DOUBLE CIRCUIT APPLICATIONS

In double-circuit line applications, there is a possibility of relay instability on a healthy circuit when a fault occurs on an adjacent circuit. This is particularly so for certain types of earth faults which can produce quite a strong mutual coupling effect between the

faulted and healthy circuits. This is a potential problem in HS applications where, due to the much wider bandwidth which must be employed, larger HF components of differential current are admitted into the healthy circuit relay. In this relay design, however, this problem is avoided by the use of only the Aerial mode signals since the aforementioned mutual coupling effect is predominantly associated with the earth mode component.

## 6.12 NOISE IMPACT ON RELAY PERFORMANCE

Although the effect of noise is substantially reduced by the input analog filter and by applying the moving window average filter and the sophisticated decision logic, it was, however, envisaged that since the relay could be subjected to any form of noise on its signals when operating in a practical system environment, particularly in the hostile environment of a substation, the impact of noise on its performance was also tested. For this test a source of white noise from a noise signal generator was incorporated on the relay currents and some of the relay tests were repeated. The relay operated correctly mainly because the noise was attenuated partly at the input analog filter and partly within the processor by the forementioned average filter and design logic.
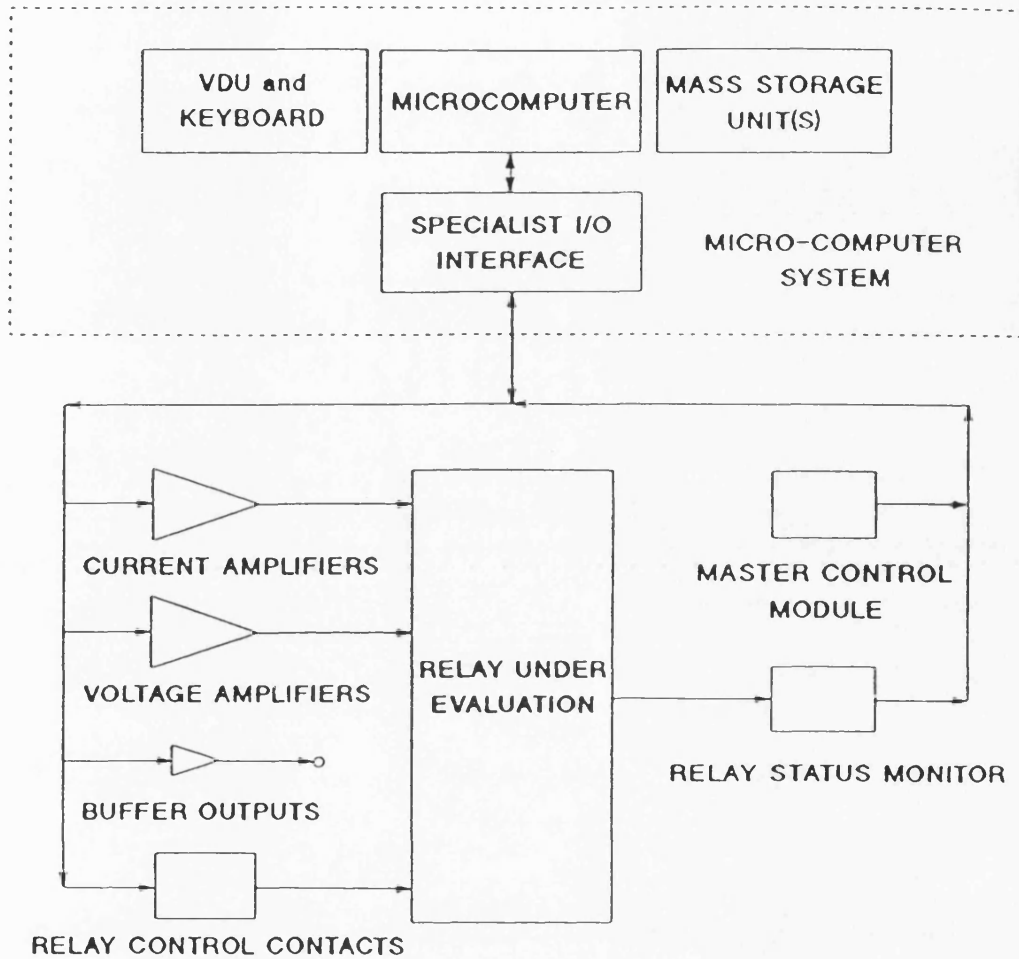
Fig. 6.1    The microcomputer programmable transmission line
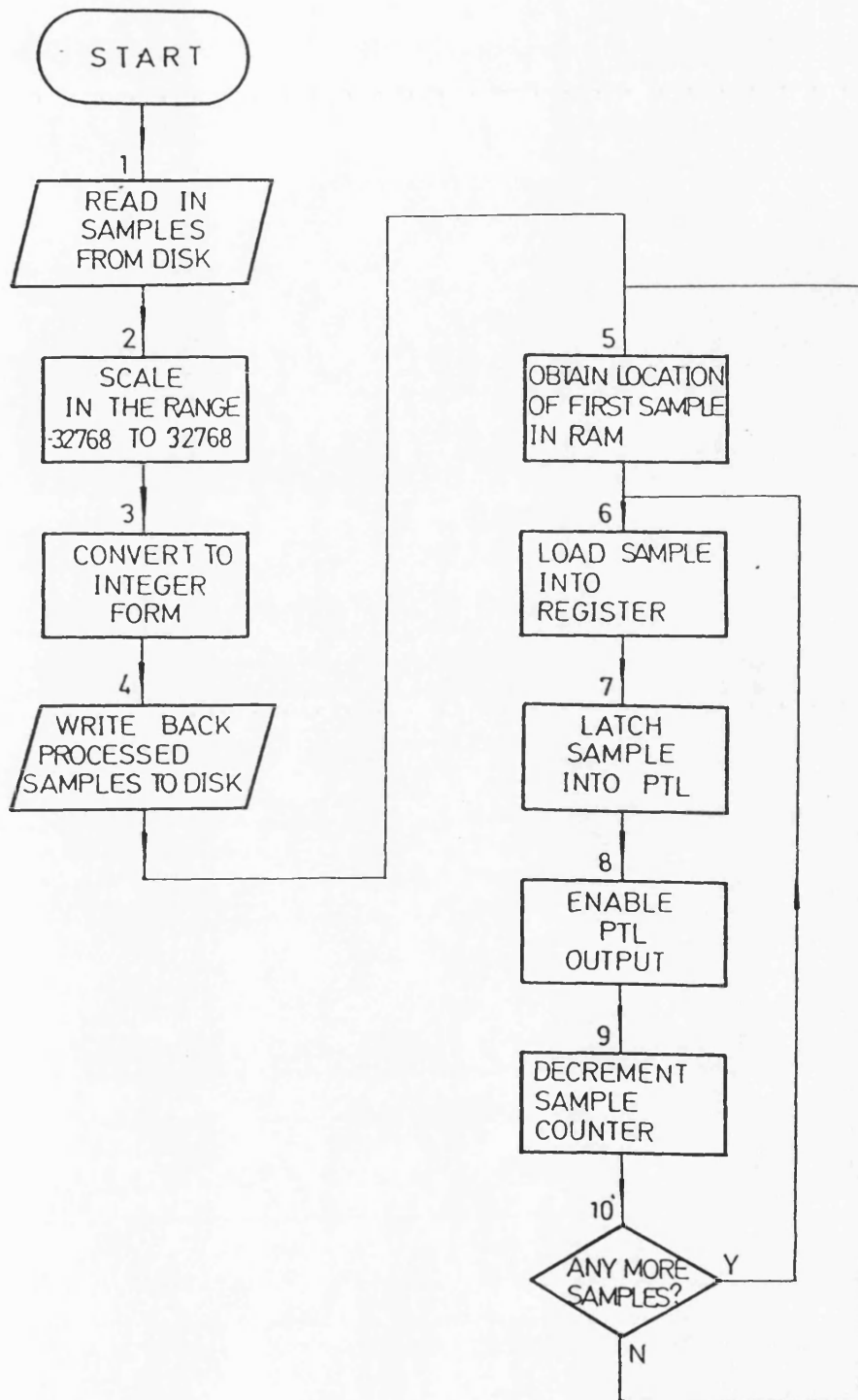
Fig. 6.2    Software flow-chart of the PTL
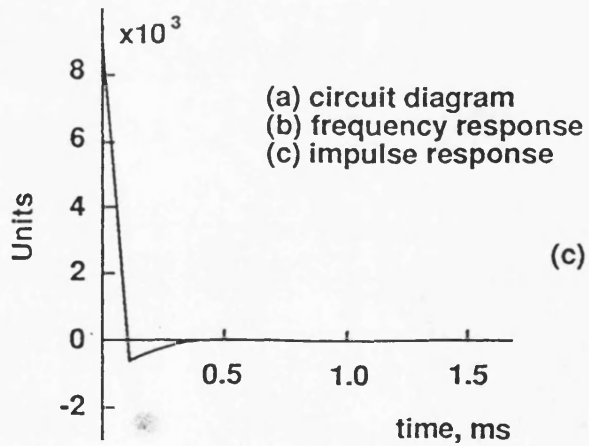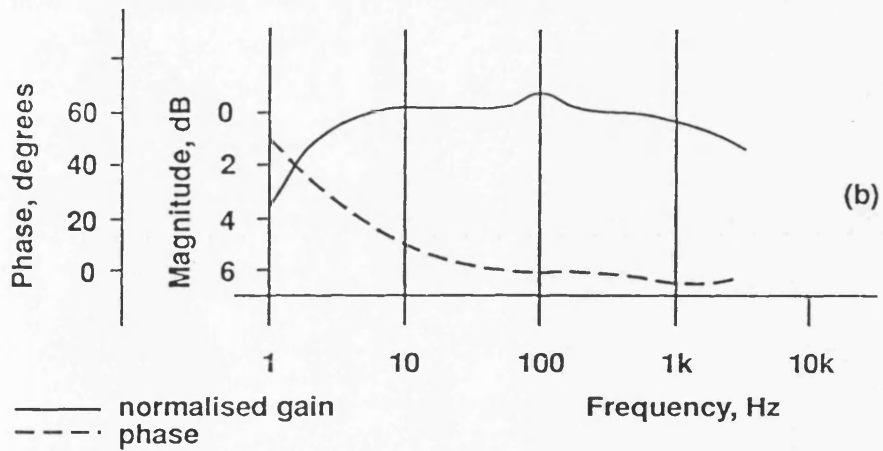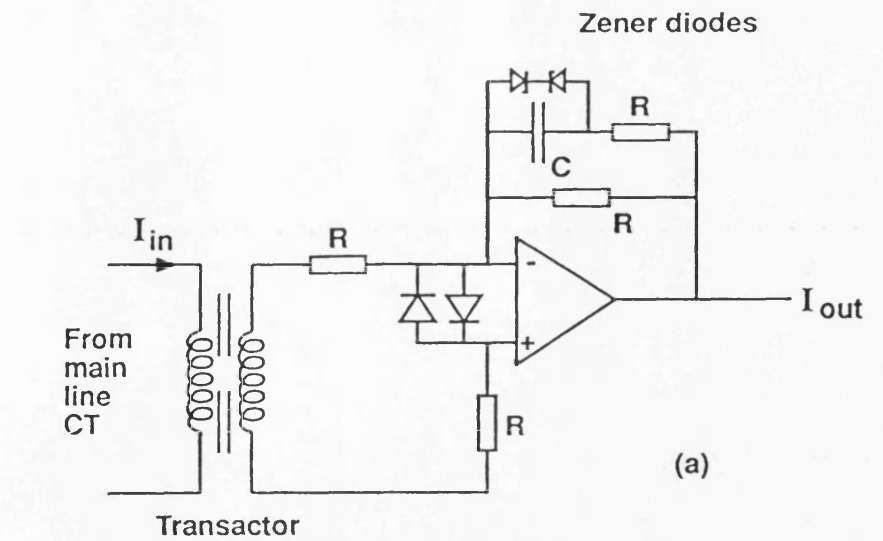
Zener diodes

(a)

$I_{in}$

From main line CT

R

Transactor

R

C

R

$I_{out}$

(b)

Phase, degrees

Magnitude, dB

Frequency, Hz

normalised gain
phase

(c)

x10³

Units

time, ms

(a) circuit diagram
(b) frequency response
(c) impulse response

Fig. 6.3    Current input module circuit and response
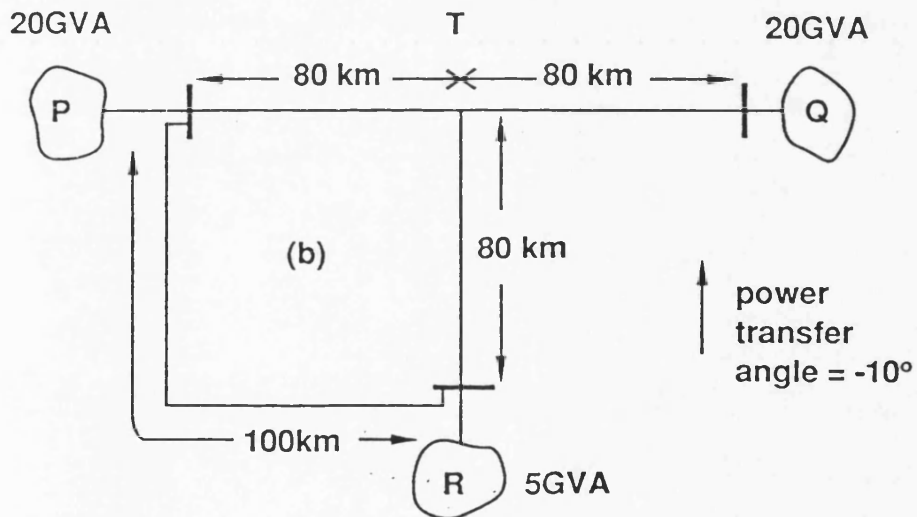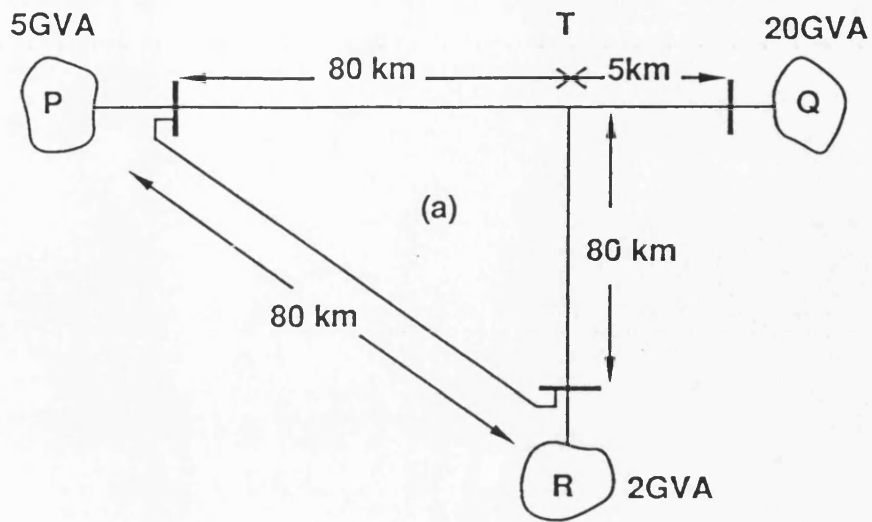
Fig. 6.4    Typical tee configurations studied
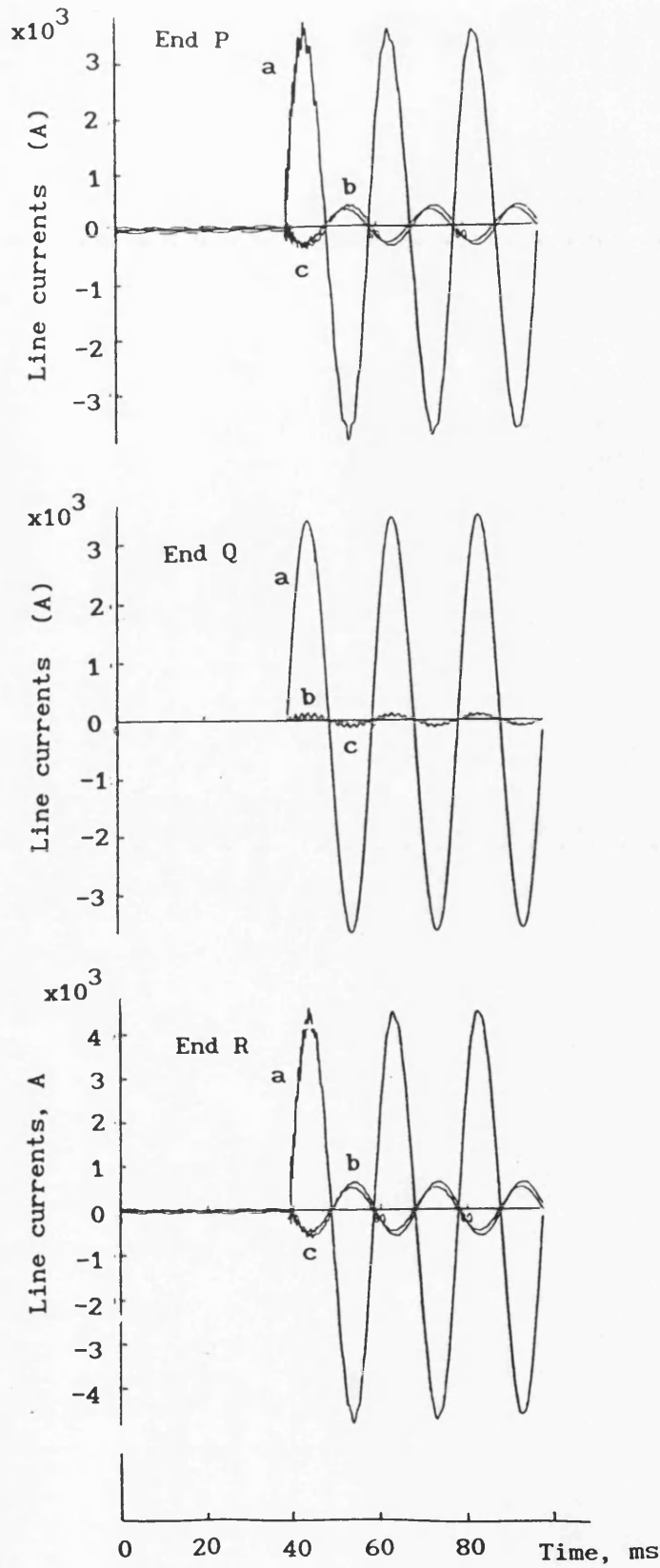
Fig. 6.5    System currents for an internal fault at the T-point

of the configuration shown in Fig. 4.6-b
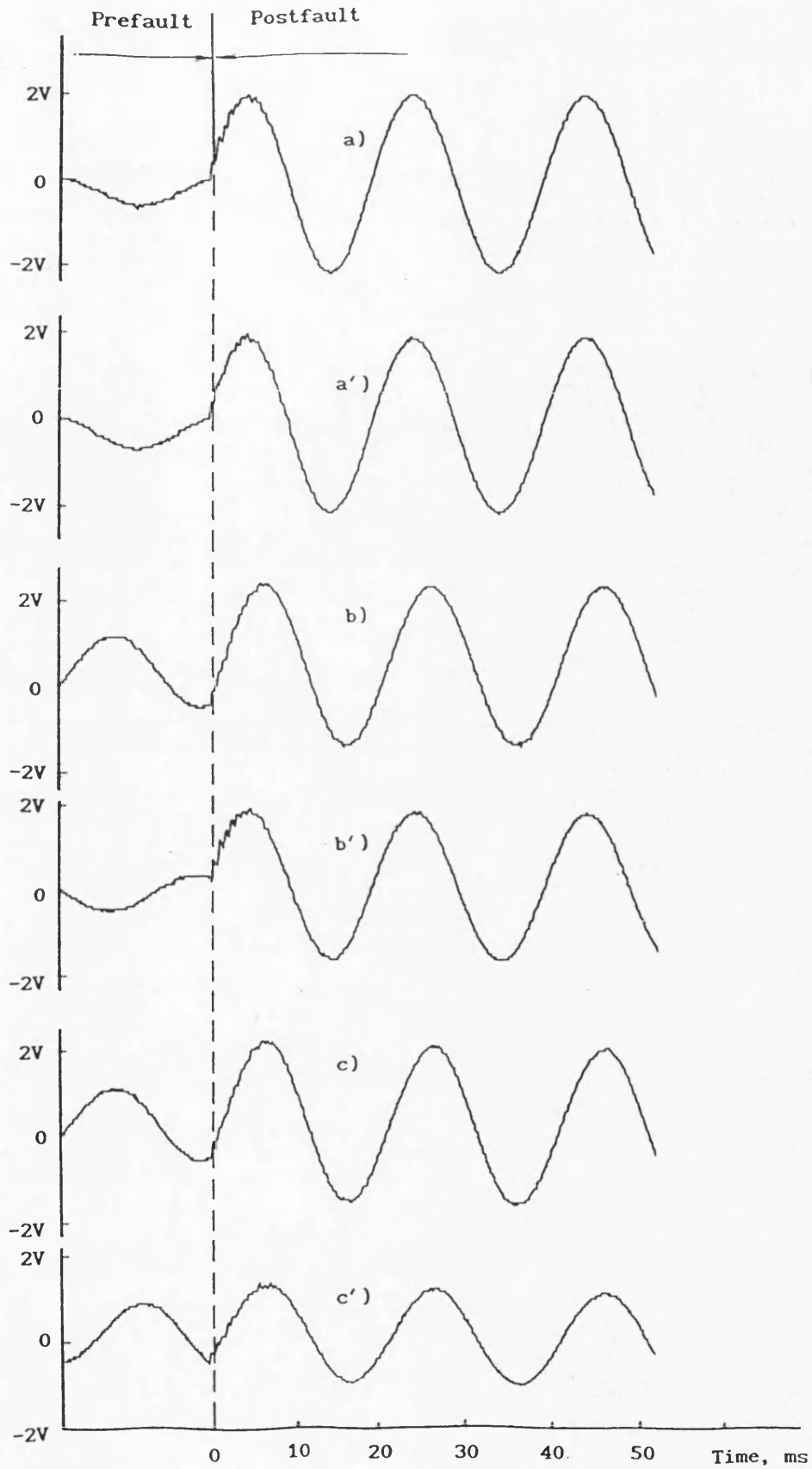
a, b, c - Currents of mode 1 at ends P, Q and R respectively

a′, b′, c′ - Currents of mode 2 at ends P, Q and R respectively

Fig. 6.6   Modal currents for a fault at T-point va 90°/earth
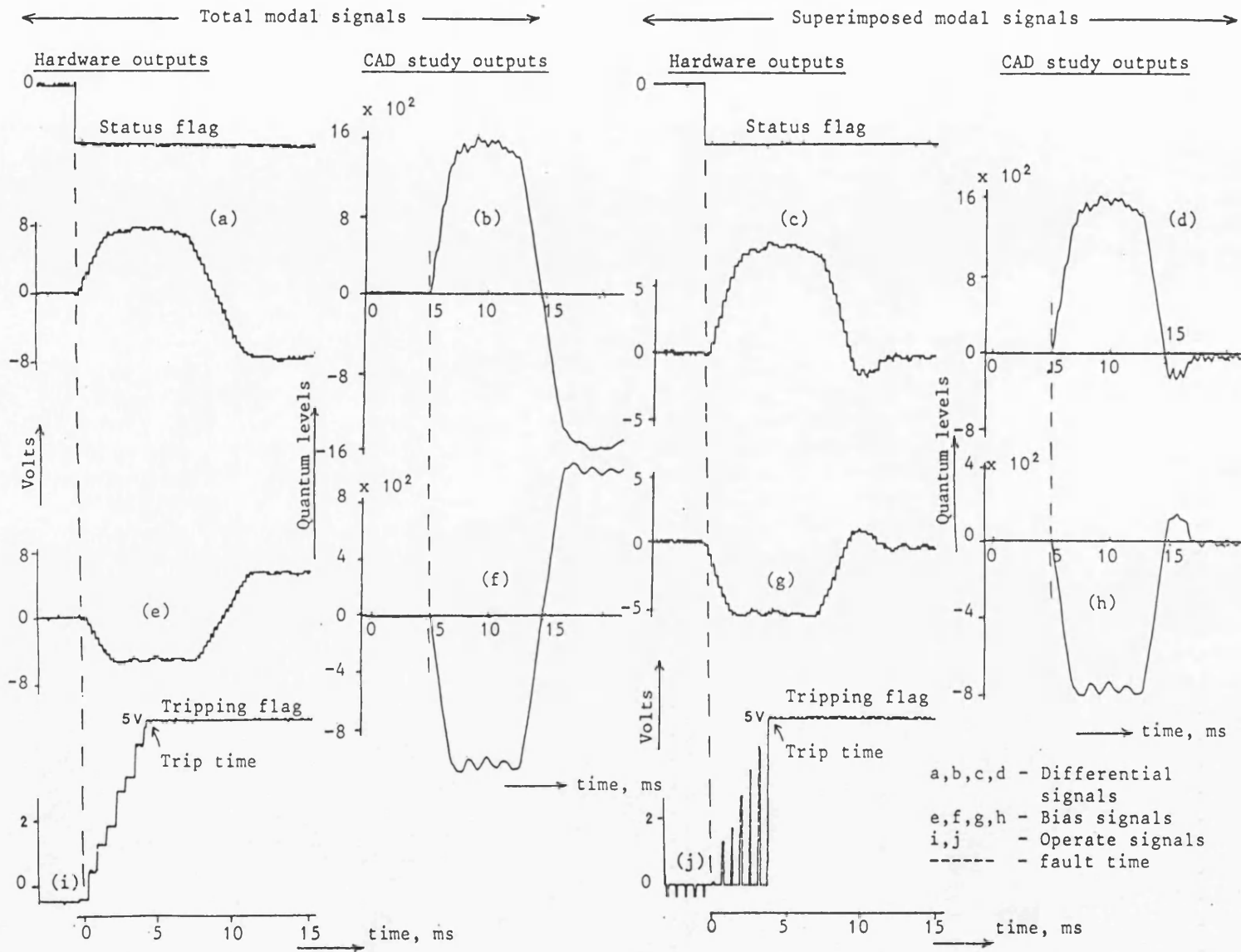
Fig. 6.7    Relay signals for an internal fault
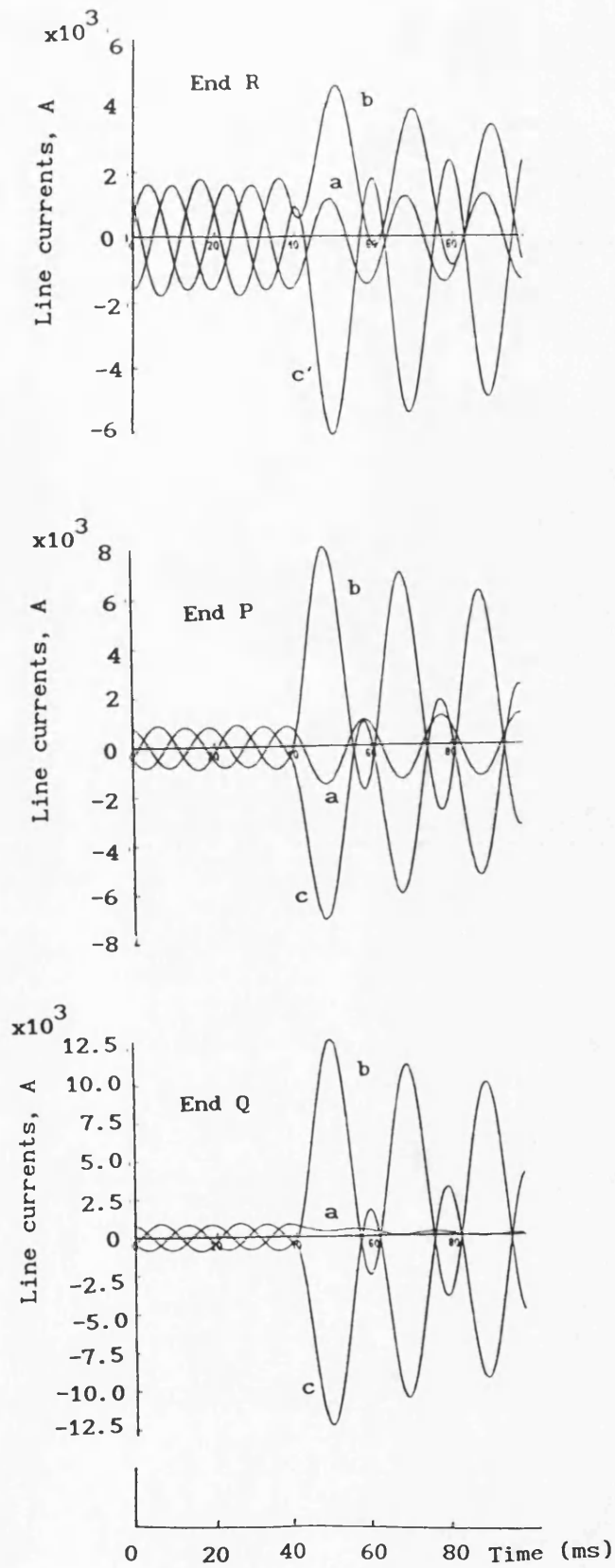
Fig. 6.8     Primary system currents for an external fault $V_{bc0}°$ without CT saturation
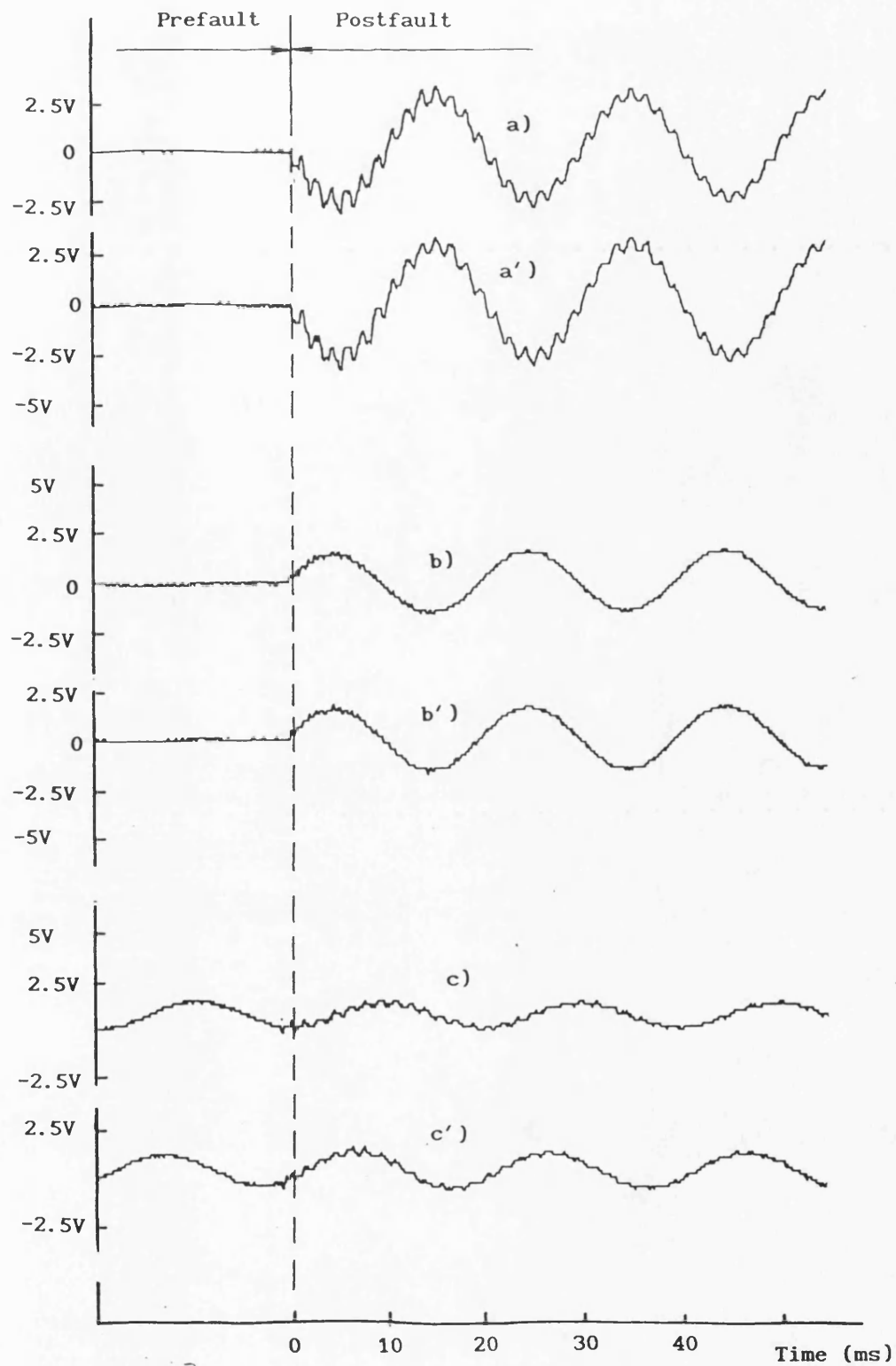
a, b, c - Currents of mode 2 at ends Q, P and R respectively

a', b', c' - Currents of mode 2 at ends Q, P and R respectively

Fig. 6.9 Modal currents for an external fault for the configuration shown in Fig. 6.4-b
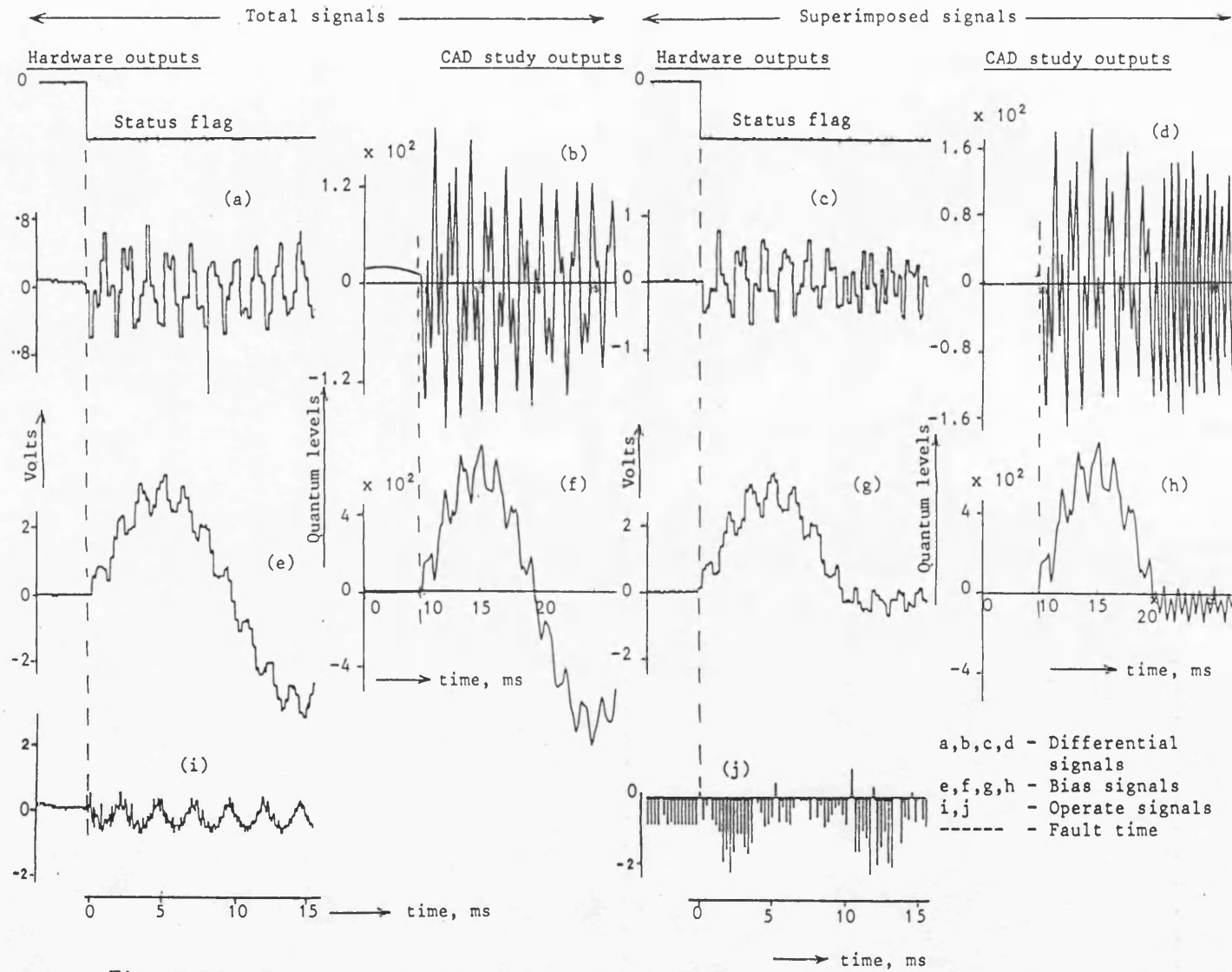
Fig. 6.10   Relay signals for an external fault

a-earth fault at T point

--- Relay operating times
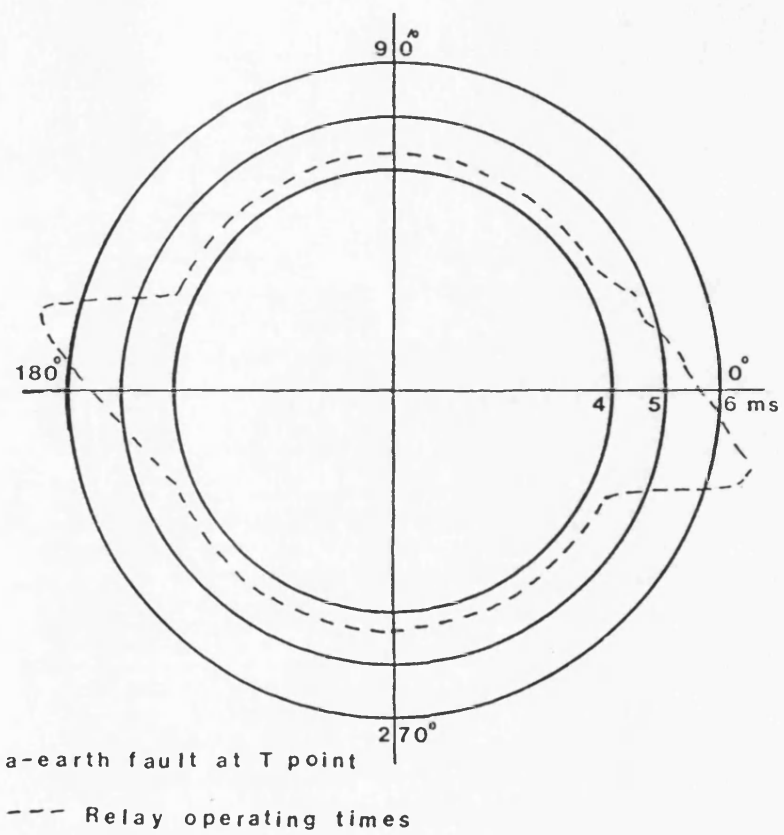
Fig. 6.11    Relay performance for internal faults

Total component currents
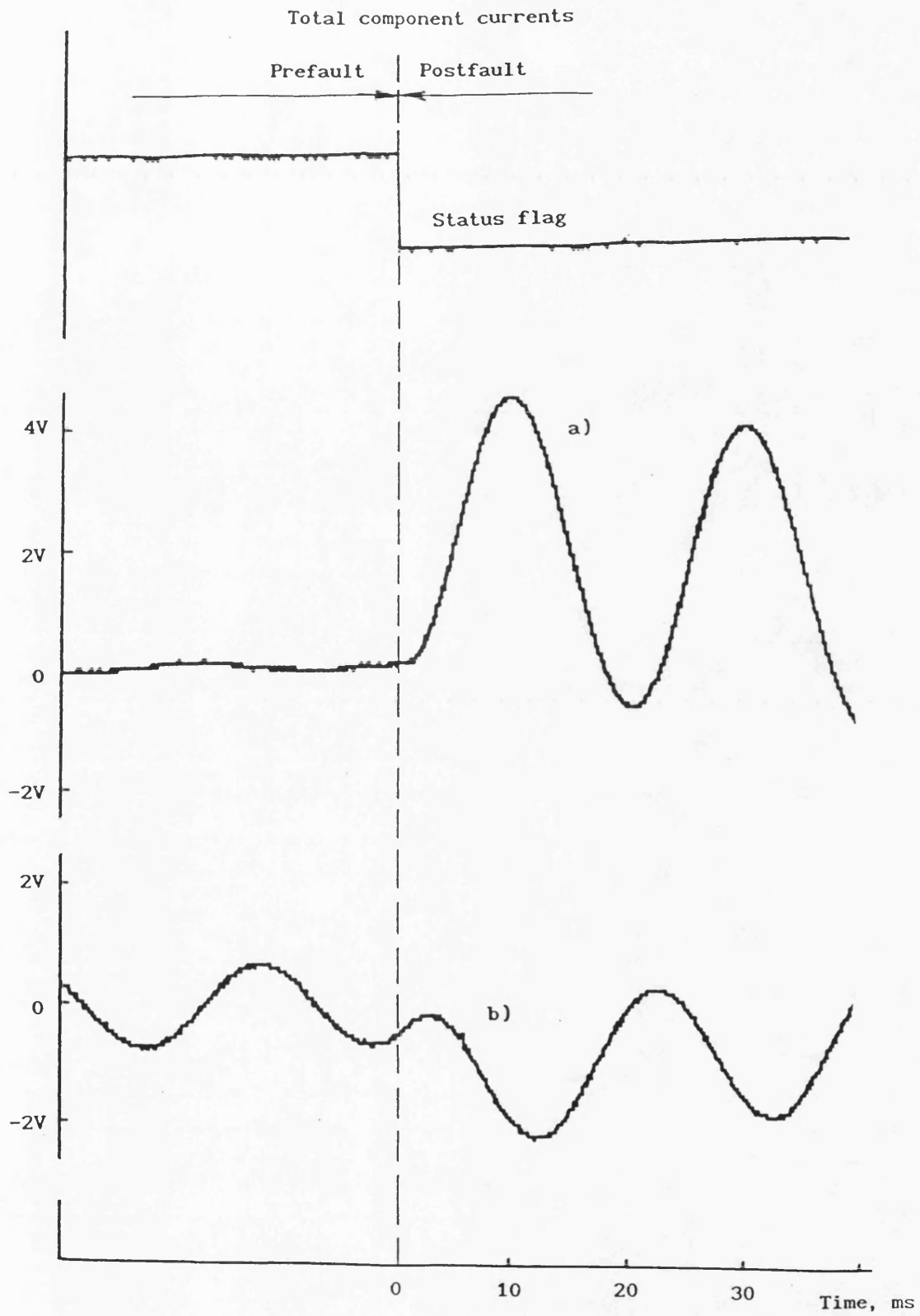
a) Differential signal

b) Bias signal

Fig. 6.12    Phase a-earth fault at $V_{a0}°$

Total component currents
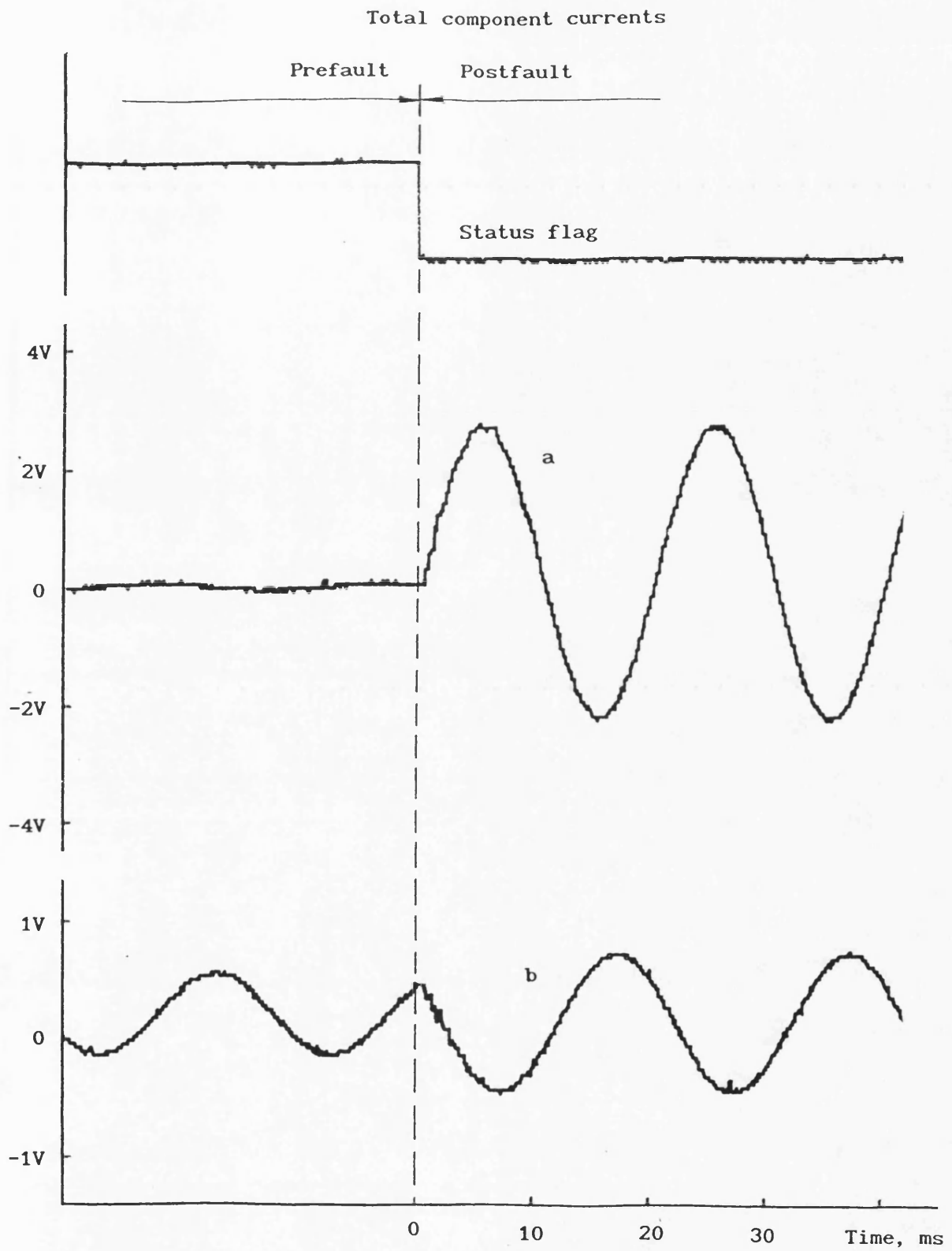
a) Differential signal

b) Bias signal

Fig. 6.13   Phase a-earth fault at $V_{a90°}$

Total component currents
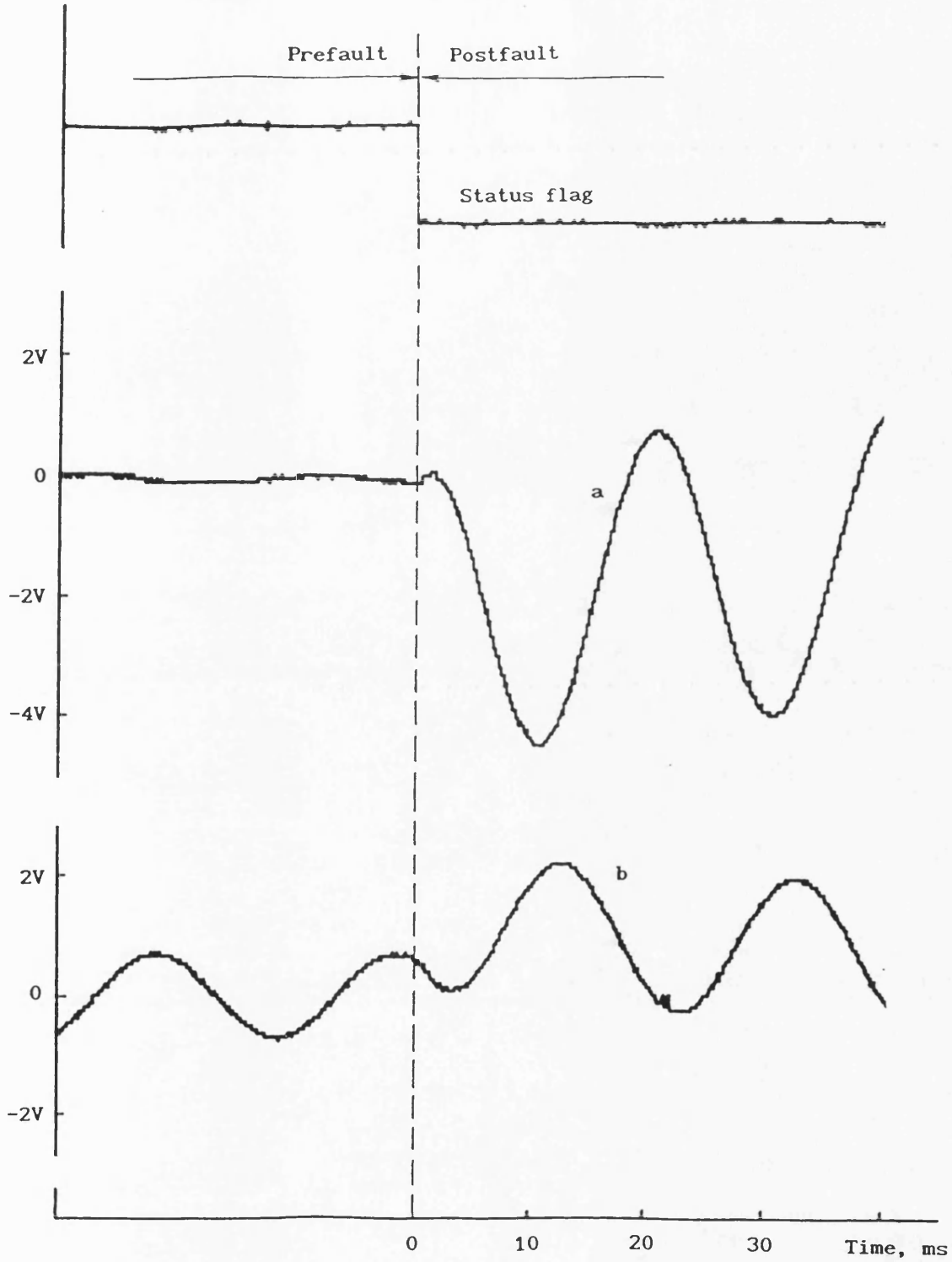
a) Differential signal

b) Bias signal

Fig. 6.14 Phase a-earth fault at $V_{a160°}$
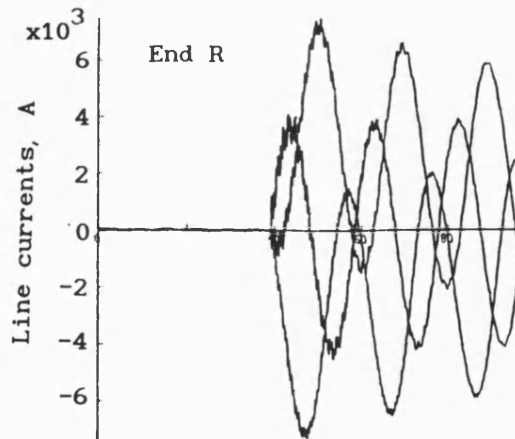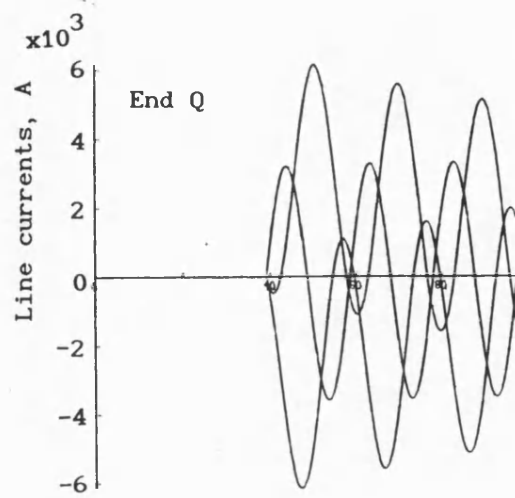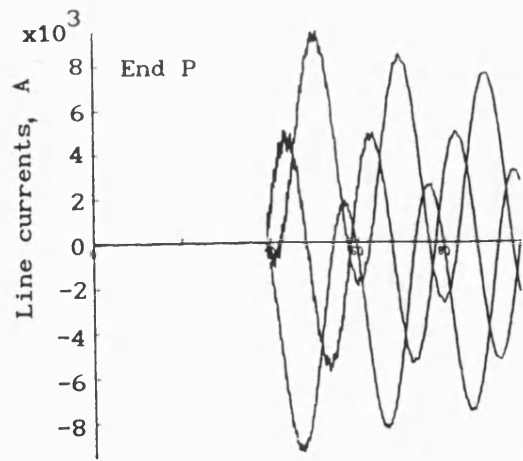
Fig. 6.15    System current of a three phase-earth fault at T-point
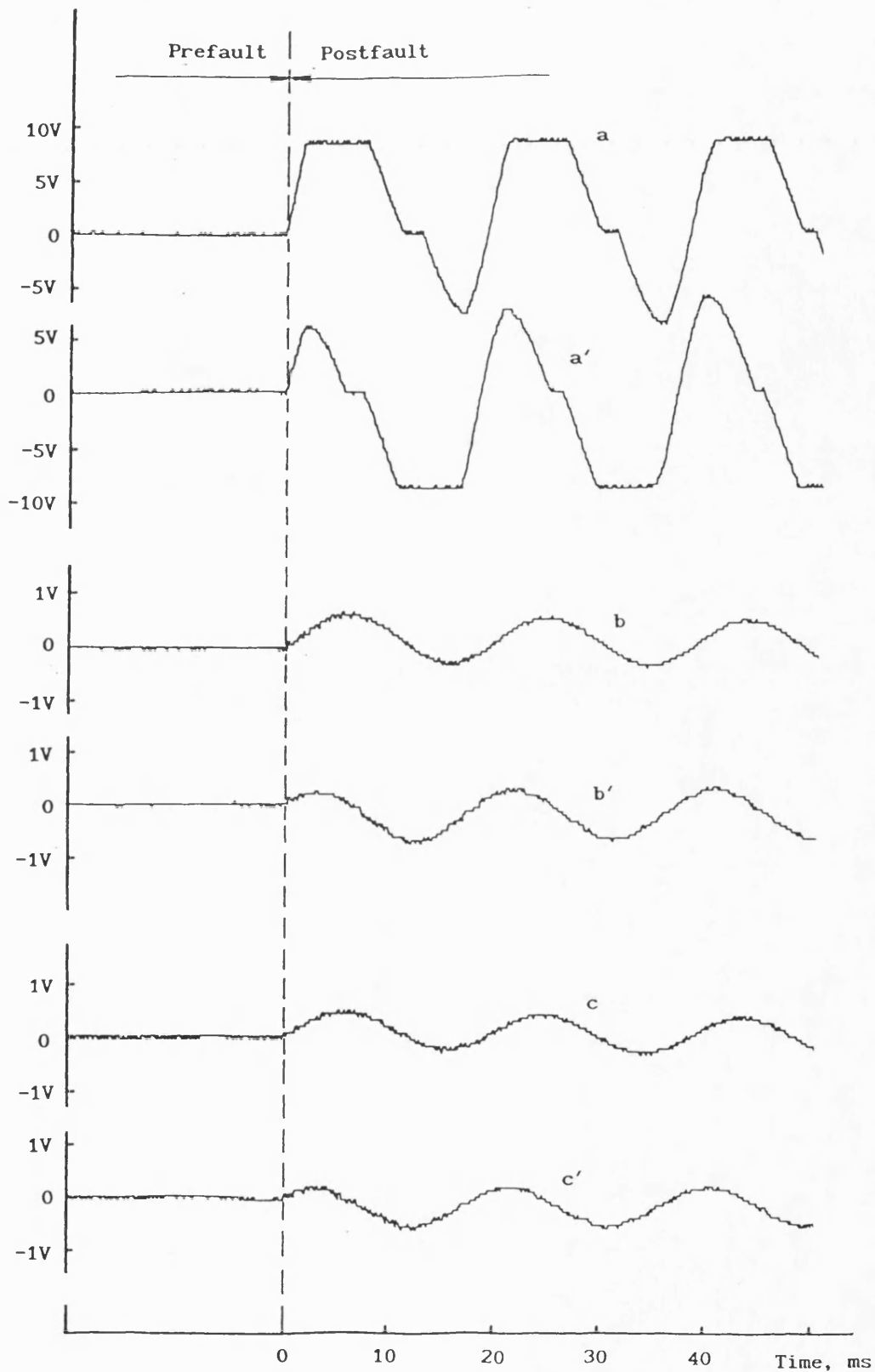
a, b, c - Currents of mode 1 at ends Q, P and R respectively

a', b', c' - Currents of mode 2 at ends Q, P and R respectively

Fig. 6.16   Modal currents for a three phase-earth fault at T-point

Total component currents
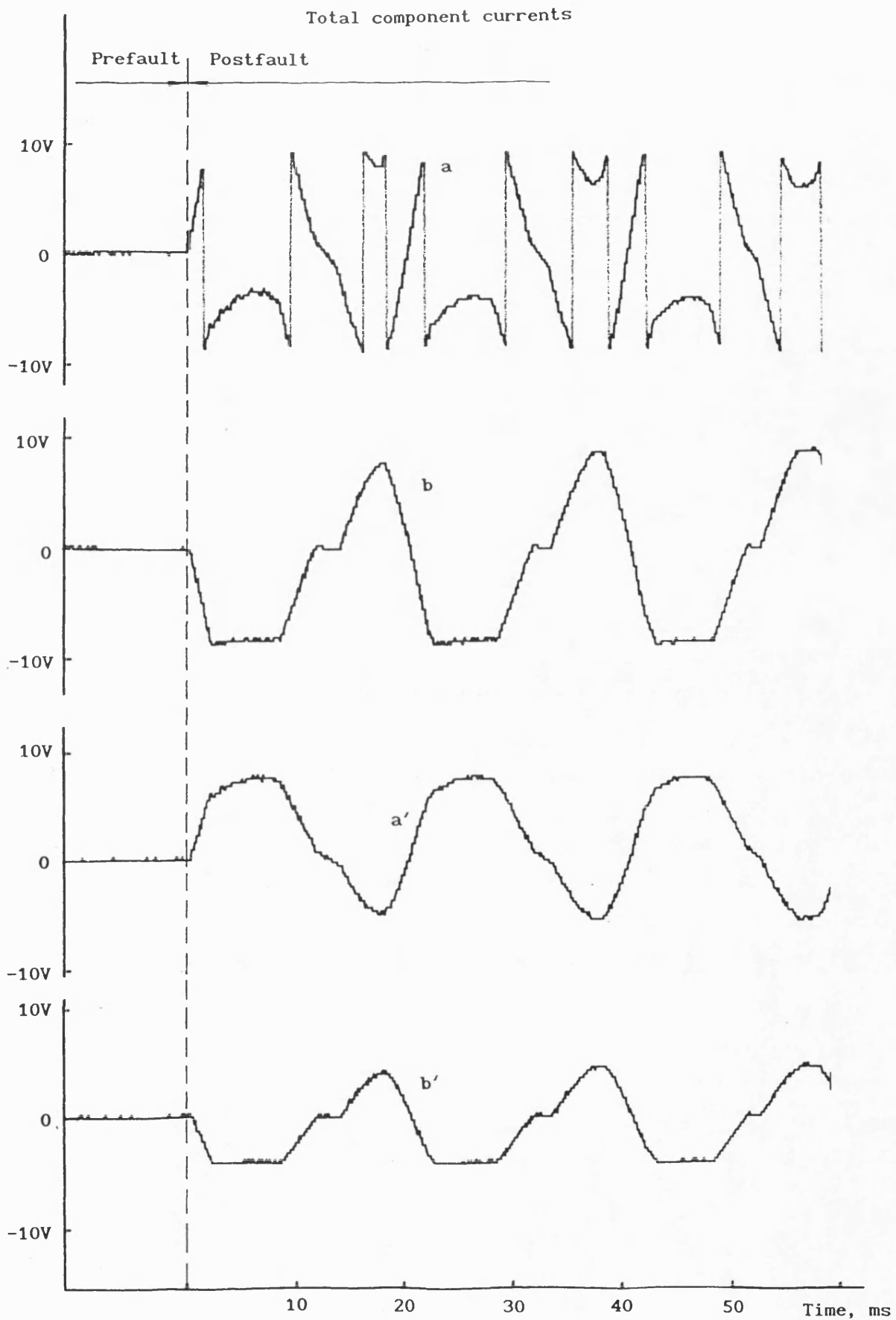
a, b — Differential and Bias quantities before scaling process

a′, b′ — Differential and Bias quantities after scaling process

Fig. 6.17 Effect of overflow for high level operating signal
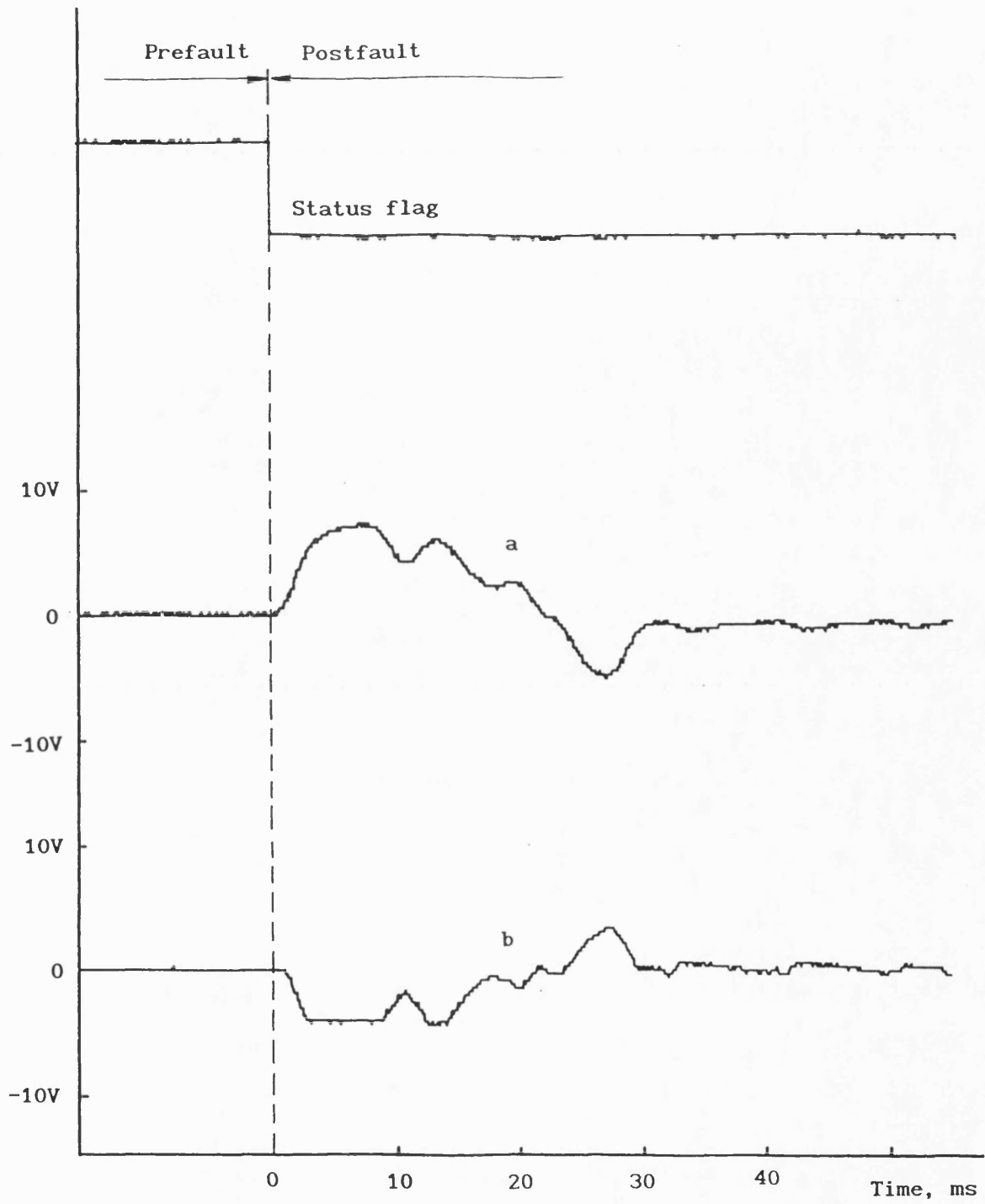
a)  Superimposed Differential quantity

b)  Superimposed Biased quantity

Fig. 6.18  Characteristics of superimposed components of a severe fault

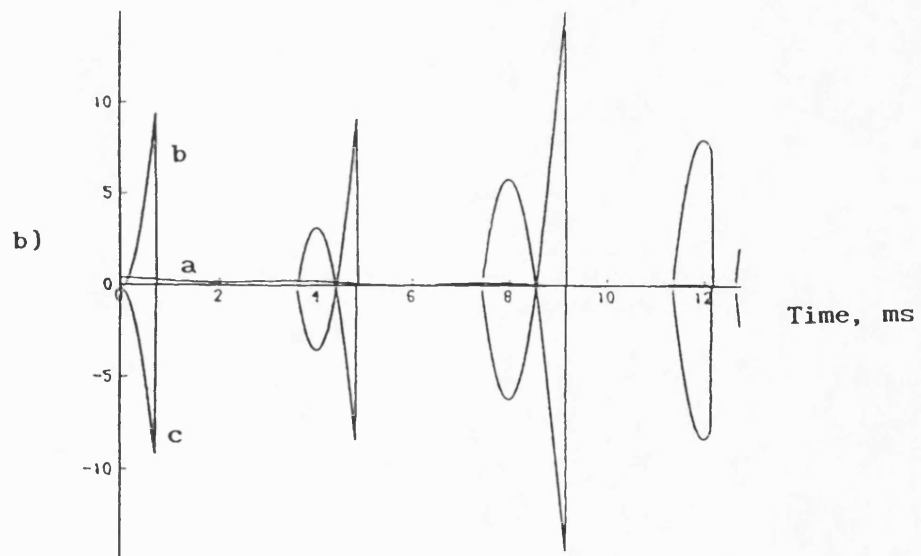CT core flux end Q, Wb



a)

CT secondary output, A
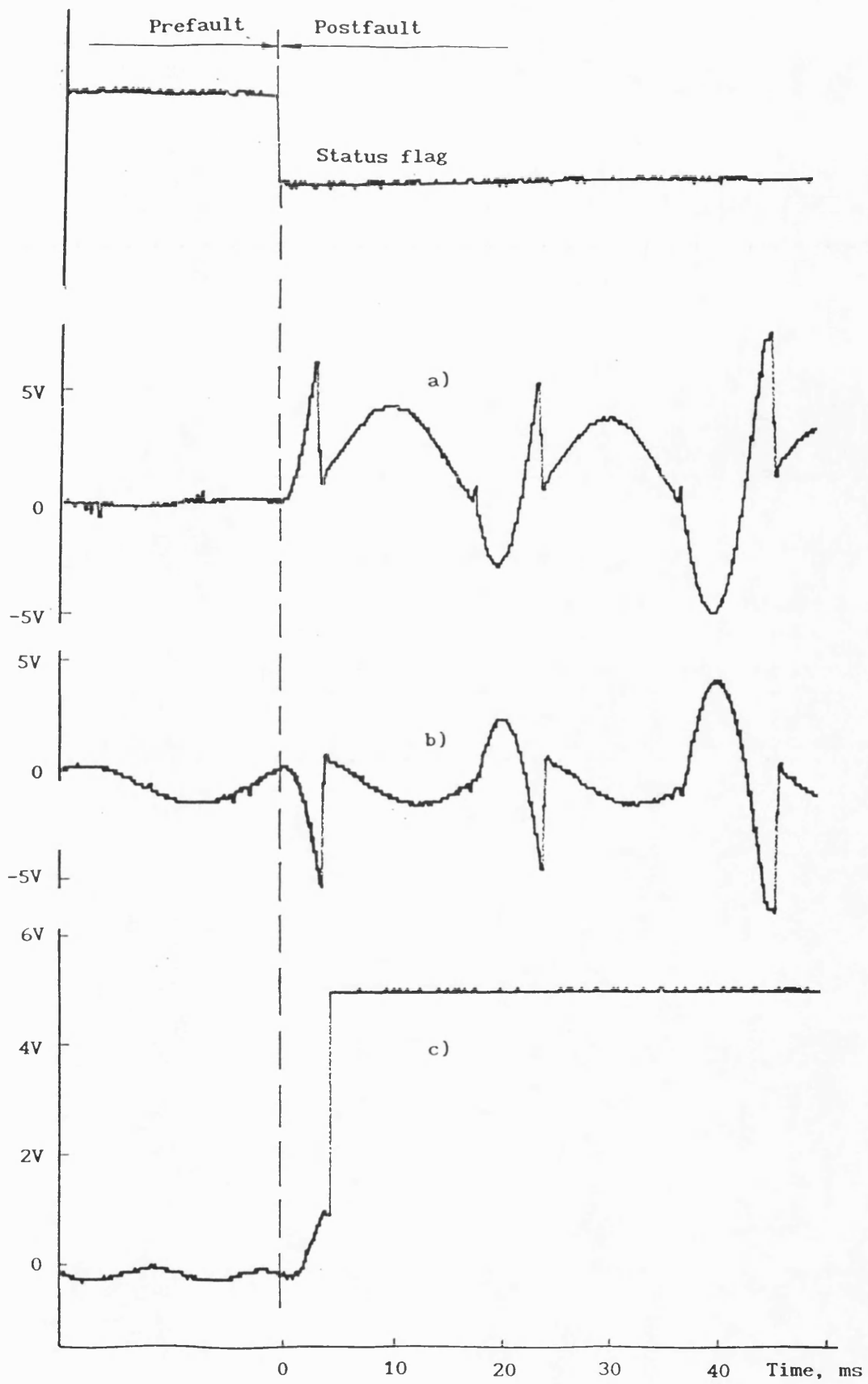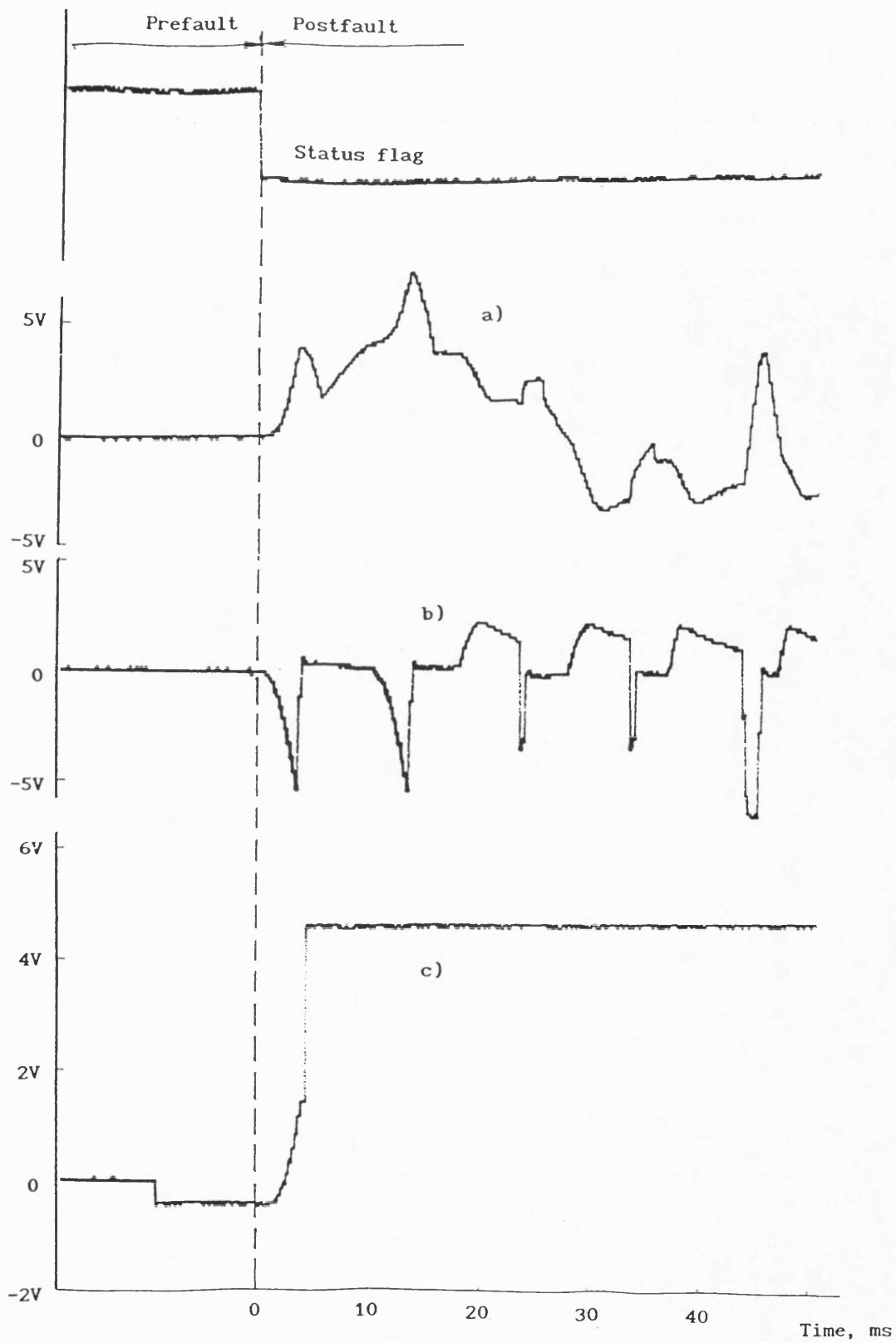


b)
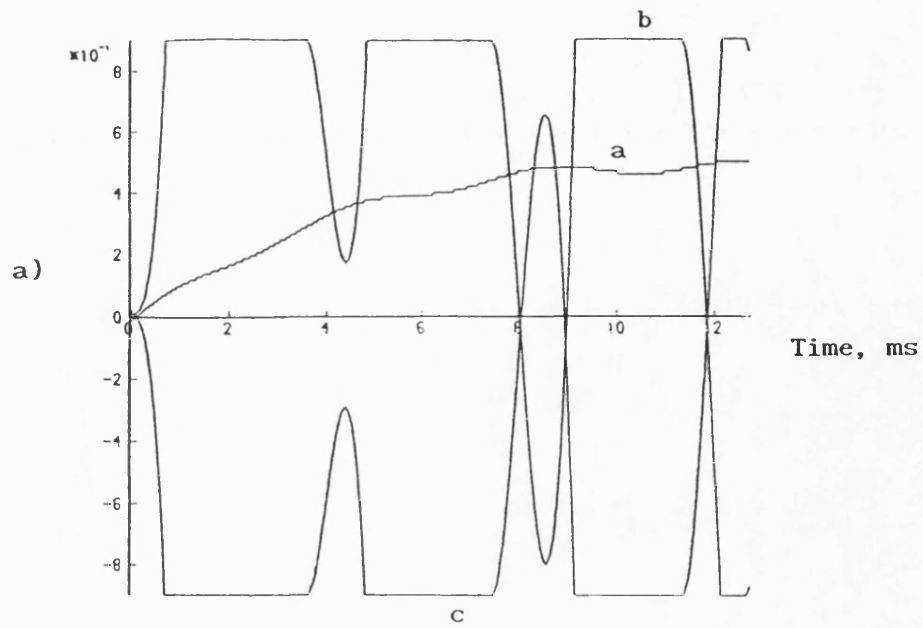
Fig. 6.19   Effect of CT saturation for an internal fault

a)  Differential component    b)  Bias component    c)  Operate  signal

Fig.  6.20    Total  modal  component

a) Superimposed Differential component    b) Superimposed Bias component

c) Operate signal

Fig. 6.21    Superimposed modal signals

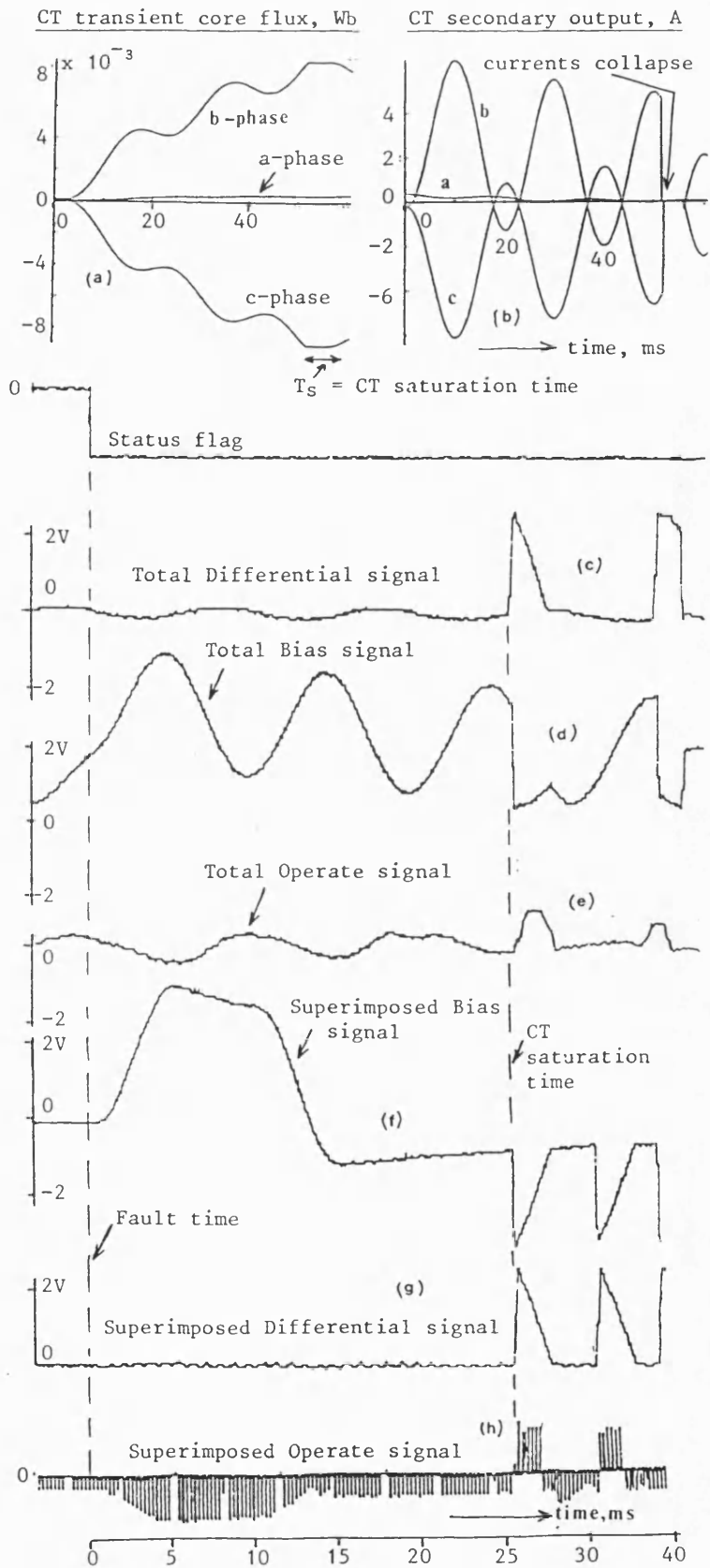CT transient core flux, Wb

CT secondary output, A



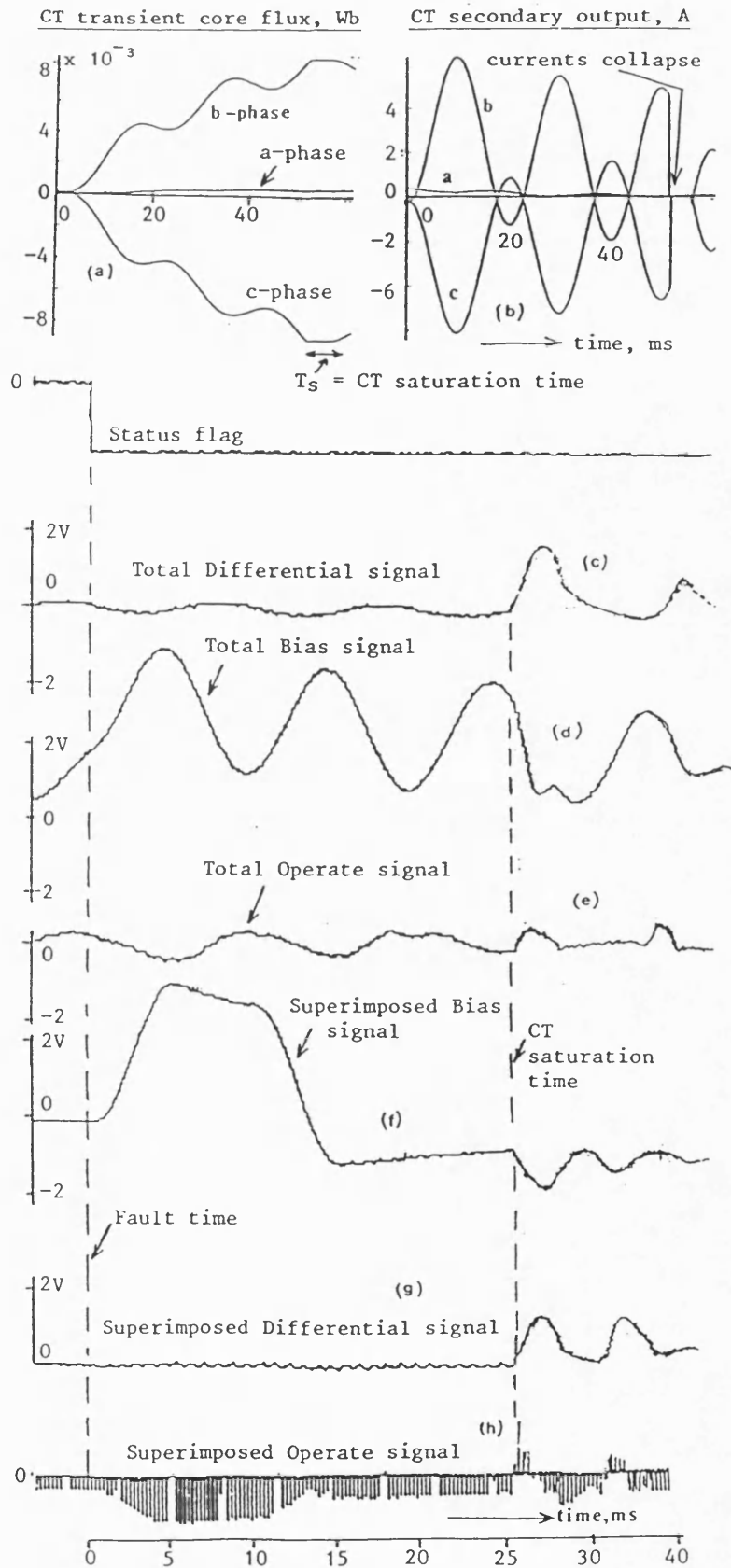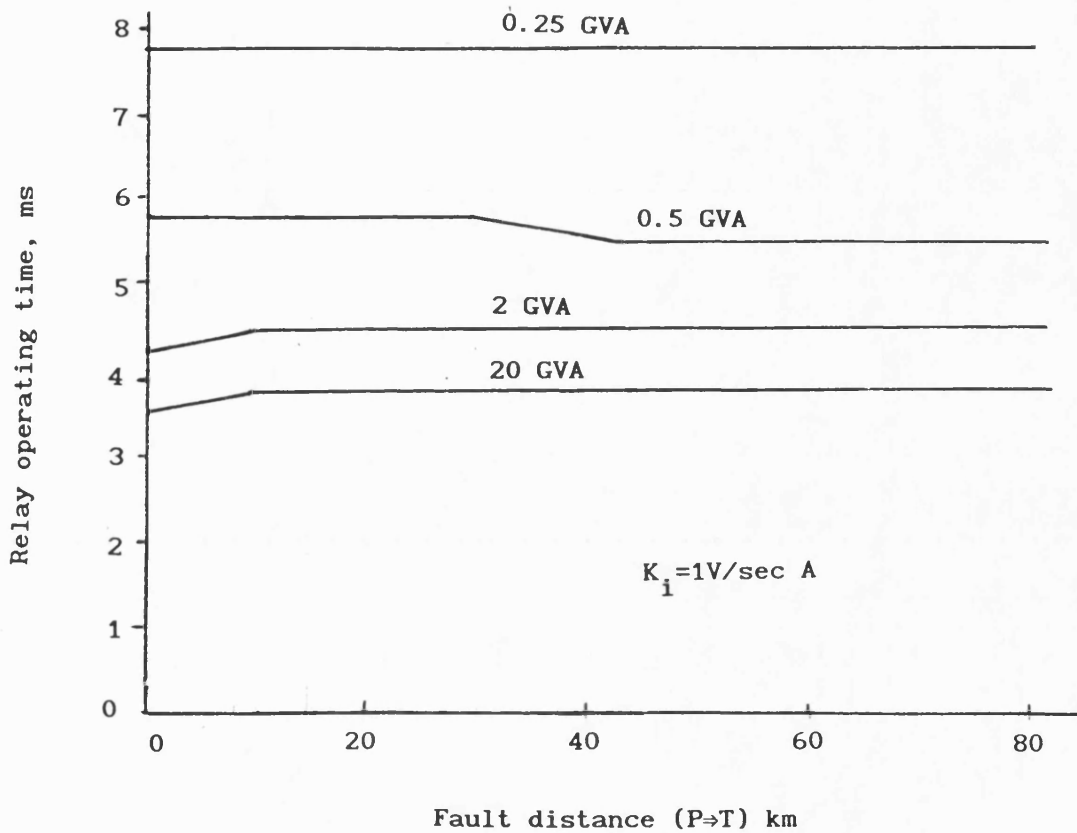Fig. 6.22    Effect of CT saturation for an external fault

Fig. 6.23 Effect of CT saturation for an external fault
with the moving window average filter employed

Relay setting based on 20 GVA trminations

a-earth fault ($V_{a0}$°) at the T-point

Fig. 6.24   Effect of source capacity variations
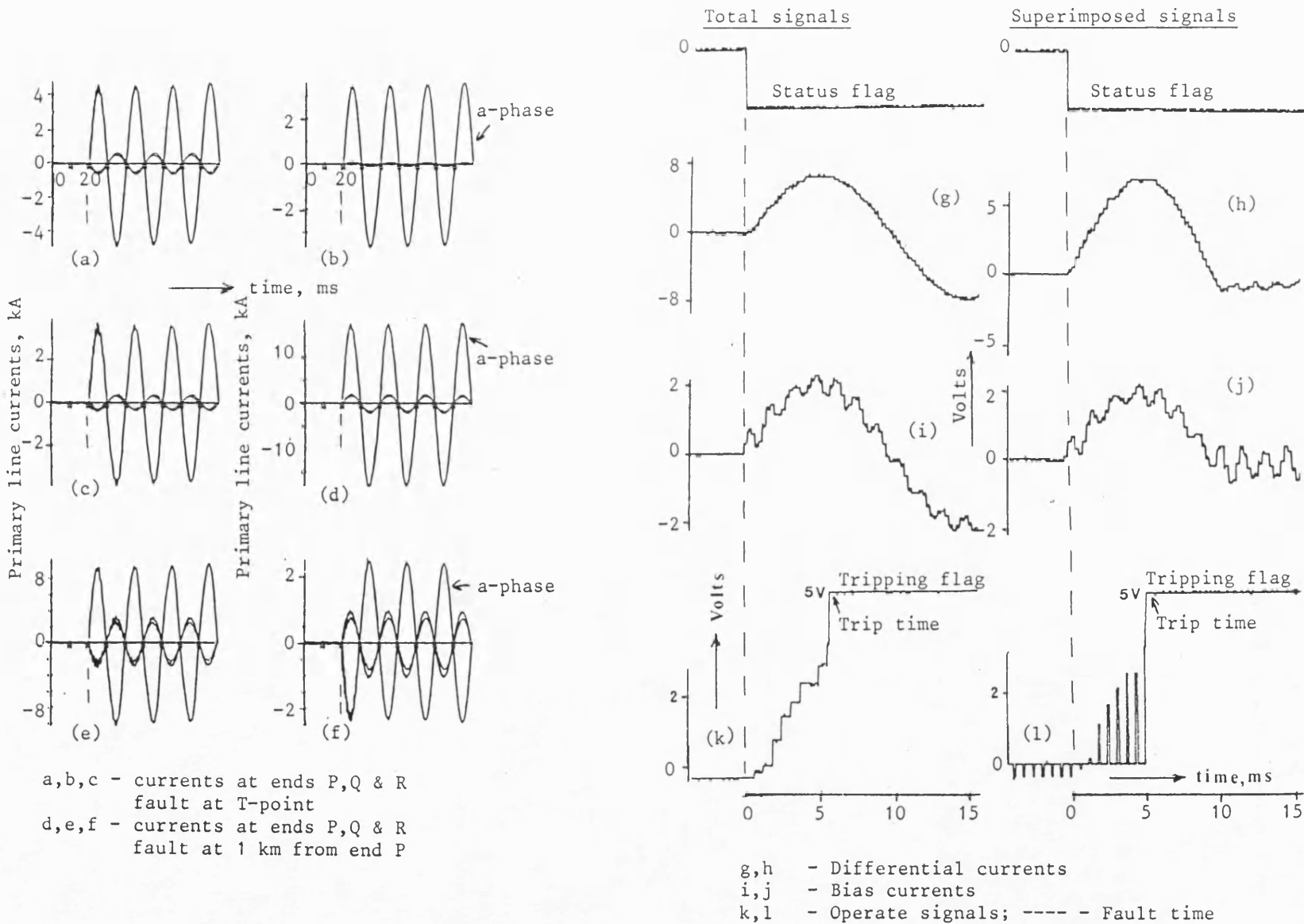
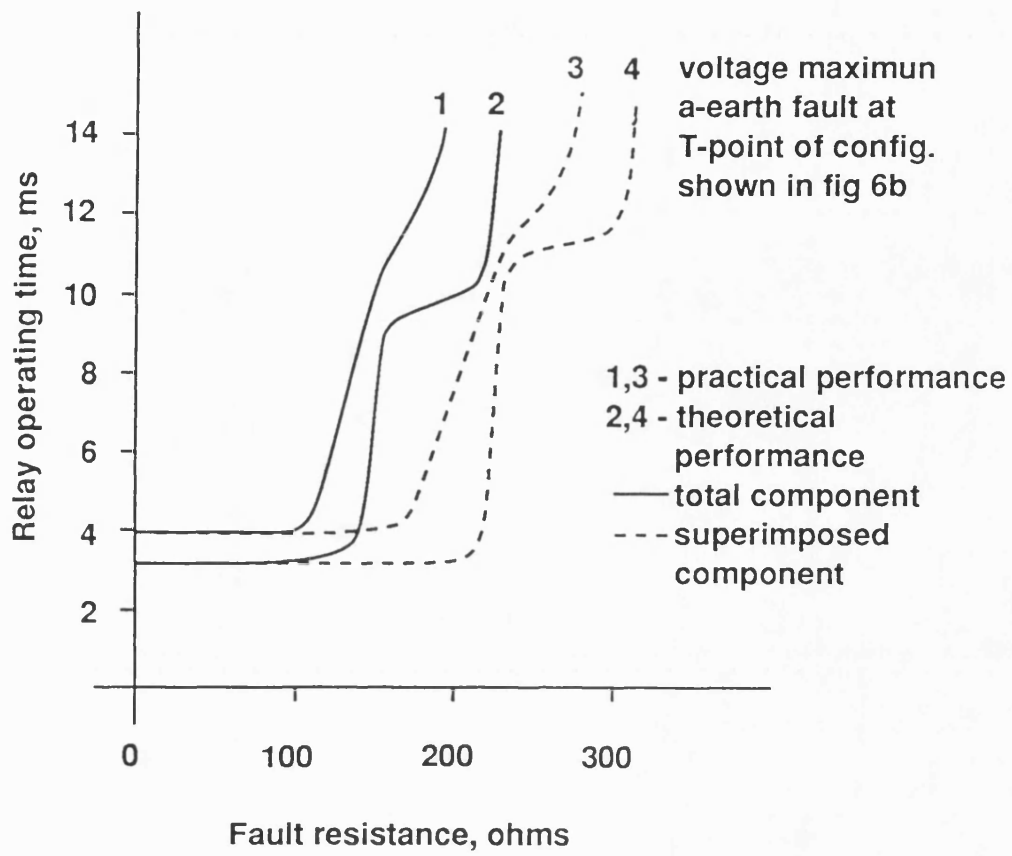Fig. 6.25     Effect of feed-around path for an internal fault

Fig. 6.26   Fault resistance coverage

CHAPTER 7

PROPOSED FIBRE OPTIC  COMMUNICATION CHANNEL

## 7.1  INTRODUCTION

One of the basic requirements of  the  engineered  prototype current differential relay is that, the  instantaneous  current  waveforms at the remote  and local ends  are converted into electronic levels at the point where CT's  are  installed.  Digital or analog data at the remote ends are transmitted from  the switch yard to the master end where  the  protective  equipment  is  located.  Thus,  the  transmission routes for the  data  information  system  pass  in  the  vicinity of the power apparatus  which  generate  large  electromagnetic  noise, which in  turn  could  corrupt  the  electronic  low  level  transmitted data.  Hence,  a  comprehensive  reliable  communication network is  an essential  requirement  for  the  efficient  operation  of  the  developed relay.

Over  the  years,  many  types  of  data  channels  have  been,  to  some degree,  successfully  applied  in  the  control  and  protection  of  power system  transmission  networks.  These  range  from  electrical channels such as  line  carriers,  pilot-wires  and  telephone  lines,  to microwave  radio  and  recently,  optic  fibres.  The  choice  of  one specific  channel  is  governed  by  various  factors  which  depend  on  the type  of  protection  and  the  requirements  of  certain  types  of application and most  importantly,  the  reliability  and  the  security

of the system.

Most of the aforementioned, except fibre optics, are to certain extent affected by the presence of power system faults, electrical and electromagnetic interference and most importantly, they suffer from restricted capacity and are usually suitable for short distances and lower speed protection mainly because of inherent time delays and signal attenuation. This is particularly so for metallic pilot wires and leased telephone circuits due to the effects of induced voltage and ground potential rise (GDR) [9,10,39,40]. Electromagnetic interference (EMI) on a data transmission system is thus anticipated to be a major problem from the view-point of system reliability, However the evolution in fibre optic industry and the advent of reliable and affordable fibre [41], optical communication channels provide a path that is impervious to EMI and GDR, has a wide bandwidth, and low attenuation. These characteristics make optical fibres potentially well-suited for EHV protection applications. The main advantages of optical-fibre transmission are as follows:

1) EMI immunity.

2) Electrical insulation.

3) Provide a HS protection for the distance lines.

4) Increase in transmitted information due to large transmission capacity.

5) Low weight and small cable space and therefore easy installation.

6) More security of communication channels than microwave channels.

Having outlined the advantages of using fibre optics as a transmission media, it is appropriate to give some details of the proposed fibre optic link, and to briefly outline the transmission techniques which are most suitable for this specific application.

Fig 7.1 shows the block diagram of the proposed PCM transmission system which can be used between the remote ends and the local end where the relay is located. It consists of three main parts; a transmitter, a receiver and a fibre optic link.

The transmitter consists of a prefilter, S/H device, multiplexer, A/D converter, a parallel to serial converter and an electrical to optical drive circuit. The receiver consists of an optical to electrical drive circuit, de-multiplexer, serial to parallel converter, D/A converter and an analog filter. The structures and transmission properties of optical fibres, a comparison between single mode and multimode applications, optic fibre system impairments, transmission limitations, calculation of transmission distance without repeaters and calculation of attenuation, and maximum bandwidth of fiber optic lines have been well documented in numerous publications [43-45]. Some of these are briefly detailed in Appendix B.

## 7.2 FIBRE OPTIC LINKS

Two kinds of optical digital data transmission systems are available on the market. One is an intrastation system, and the other an interstation system [10].

The intrastation optical data transmission system is different from the interstation system in terms of transmission distance and capacity. This system is suitable for short-distances, and it requires small capacity fibre optic channels, and low cost optical components.

On the other hand, an interstation optical data transmission system is more suited to medium and long transmission lines. This system supports long distance (>30km) and large capacity (>100Mb/s) transmission. Features such as non-inductive performance and wide bandwidth of interstation fibre optic systems are obviously most suitable for differential protection. Proto-type models of such systems have been field tested and good operational results for a number of systems have been reported [9-12,14].

## 7.3 ANALOG AND DIGITAL MODULATION

For the transmission of data over a communication channel, a modulation technique is used, the latter being the process of converting a signal from one form into another in order to make it more suitable for transmission of information over a selected medium. There are two modulation techniques for the transmission of data; analog or digital. Analog modulation comprises amplitude, phase, or frequency division modulation. However, common to all analog modulation is the need for good linearity in the modulation/demodulation circuits and transmission channels in order to produce adequate system performance. On the other hand, digital modulation is the representation of a sample discrete value of a

signal into a series of recurrent pulses. Coding/decoding and the transmission of these pulses can be very simple because it is a bit stream which has only two states "On" (binary one, pulse) and "Off" (binary zero, no pulse). Thus it is insensitive to the nonlinearities of the transmission system and can be transmitted over great distances without major degradation in the quality of the information signal. This is particularly true when it is used with fibre optic as a transmission media. One of the most practical and easily applied digital transmission technique is the pulse code modulation (PCM). There are two commercially available types of standardized PCM in primary group signal channels; one is PCM-32 providing 30 channels and two supervisory channels with the transmission data rate 2.048 Mb/s of this group, and the other is PCM-24 with the 1.544 Mb/s of transmission speed. The bandwidth of each channel of these two standard PCM's is the same with 64 kb/s of data rate. Every basic groups can be multiplexed together to provide more communication channels.

## 7.4 PCM BANDWIDTH CALCULATION

Considering that for this relay design the nominal sampling rate of 4 kHz has been chosen and the A/D used has 12 bits binary format, the bit rate (Br) necessary for one single modal channel without control bits is

$$Br = 4 \times 12 = 48 \text{ kHz} \tag{1}$$

At least 4 bits are necessary for bit error detection and correction

and are called redundancy bits, they must be added serially to the transmitted sample which results in a 16 bit format for one channel, it is thus equivalent to

$$Br = 4 \times 16 = 64 \text{ kHz} \qquad (2)$$

If a standard 64 kHz channel is to be used as a transmission modem, then three channels of the transmitting network must be hired for each one of the remote ends; two of them are for the transmission of the two modal currents and and a third one for the supervisory and control signals and other necessary information about the system. If no such transmission network is readily available for use, then it is preferable to multiplex serially the three streams of data in one frame, thus making most of the wide-band feature of the optical fibre channel, and a saving in the number of dedicated channels is achieved. This would result in a transmission bit-rate Br of

$$Br = 3 \times 16 \text{ bits} \times 4 \text{ kHz} = 192 \text{ kbit/s} \qquad (3)$$

## 7.5 PCM RECEIVER

The function of the receiver circuit is to convert the light pulses carried by the fibre link into useful binary information. It comprises three stages. In the first stage a light detector converts a stream of light pulses into electrical ones. The second stage is a low pass filter of bandwidth between 0 and the maximum bandwidth of the transmitted signal (i.e. 192/2 kbit), which rejects the noise frequencies greater than the maximum bandwidth frequency. The third

stage of the receiver is a comparator which compares the filter

output ($V_f$) with a threshold voltage which is equal to one half of

the original pulse amplitude ($V_p$), the comparator output voltage

($V_c$) is then given as:

$$V_c = V_p \quad \text{if } V_f > 1/2 \ V_p \qquad \qquad (4)$$
$$V_c = 0 \quad \text{if } V_f \leq 1/2 \ V_p \qquad \qquad (5)$$

The comparator output $V_c$ is then interpreted as a binary "1" in

equation 4 and as a binary "0" in equation 5.

The presence of noise on the transmitted signal causes some decisions

to be made incorrectly i.e. the receiver decides that a transmitted

1 is a 0 or a transmitted 0 is a 1. This error can vary from one

quantum value (LSB) to half the value of the transmitted analog

signal if the error is caused on the most significant bit (MSB) of

the digital value. This error must be corrected.


## 7.6  BIT ERROR CORRECTION

Due to the short sampling interval essential for the high speed of

the relay, the bit error correction must be done on the receiver side

of the transmission system by error-correcting codes rather than

sending a retrains signal to the remote end. The most common

erro-correcting codes are the Hamming Code and the binary cyclic

code [46]. The Hamming code relies on parity bits being interspersed

with data bits in a data word. By combining the data and parity bits

according to a strict set of parity equations, a small byte, formed

of the check bits, which contains a value that actually points to the bit in error, can be generated. Error correcting codes are very bit-wasteful; for example on comparing equations 1 and 2, the needed bandwidth was raised from 48 kHz to 64 kHz after the addition of the 4 redundancy bits. This is of no consequence on the transmission channel when using fibre optic because of the large attainable bandwidth.

## 7.7  LIGHT SOURCE

Light sources come under two main categories [39], light emitting diodes (LEDs) and laser diodes (LDs). LEDs are low in cost and are suitable for low bandwidth fibre. Lasers are faster, and can launch large amount of lights even with single mode fibres. Table 1. below shows some indication of relative cost of devices [39].

Table 1  Cost list of light sources in 1985. [39]

| Device | Cost ( | Min. | Max. | ) |
|--------|--------|------|------|---|
| Multimode; | | | | |
| 0.84-μm LED | | $ 5.00 | $ 300.00 | |
| 1.30-μm LED | | 450.00 | 800.00 | |
| 0.84-μm LD (Laser) | | 300.00 | 1,000.00 | |
| 1.30-μm LD | | 1,800.00 | 3,500.00 | |
| Single-mode; | | | | |
| 1.30-μm LD | | 2,200.00 | 4,000.00 | |

## 7.8 LIGHT DETECTOR

Two main devices currently in use are PIN photodiode and Avalanche photodiode. These devices operate on light wavelengths of 840-$\mu$m or 1300-$\mu$m. For low bandwidth and medium distance applications, PIN photodiodes are used with multimode optical channels. However, for very high capacity digital systems, Avalanche photodiodes are used with a single mode fibre link.

## 7.9 FIBRE OPTIC INSTALLATION

Fibre optic channels have been installed as aerial cables, directly buried, or cable conduits [39]. Each type of construction requires different types of fibre optic cables. The aerial cable construction can be one of two types:

a) composite with overhead ground wire, or one of the phases

b) helically-wrapped on one of the phases or ground conductor.

For the composite type construction, the maximum allowable sag of the power cable must be carefully calculated in order that the cable elongation will not cause strain on the optical fibres. If the allowable tension is exceeded, the optical attenuation will increase, and fibre damage can result.

As for the application of the helically-wrapped type, The fibre optic cable has no metallic component and it can be easily installed by helically wrapping it around a ground or phase wire. Thus its construction is faster and less expensive.

## 7.10 DELAY CIRCUIT

The time delay of the remote ends must be compensated for. The time delay compensation can be done by building an all-pass analog delay filter [47] or by software delay inside the processor. The software approach is more flexible and can give better results and hence this was the approach adopted in this relay design. The compensation delay filter flowchart is shown in Fig. 7.2. It was applied to the local channels over 8 samples corresponding to 2 ms time delay. The number of delay samples can be changed by the use of software to accommodate for different time delay if required. Two software counters were implemented, one to store data (WR) and one to read the data (RD) to and from the delay register. Also in the figure "F" is a logic flag and "N" is the length of the delay register equal to 16 samples as a result of multiplexing the two local channels. The delay process starts by writing to the register until it is full (WR - N = 0). The logic flag then is set equal to "1" whereby on the next coming cycle the read and then replace (write) process starts automatically, keeping a delay of 2 ms between the present samples and delayed samples of the local channels.
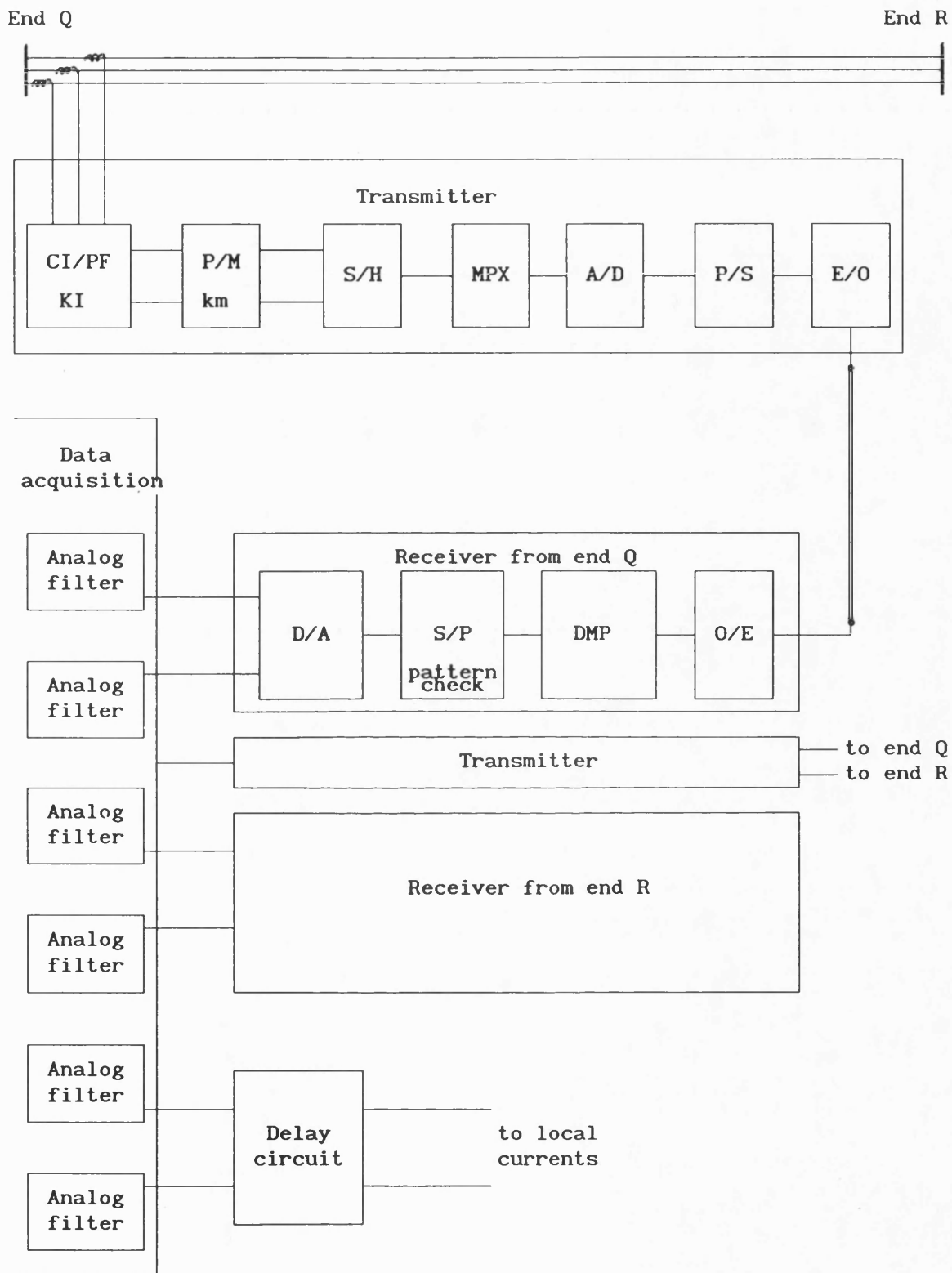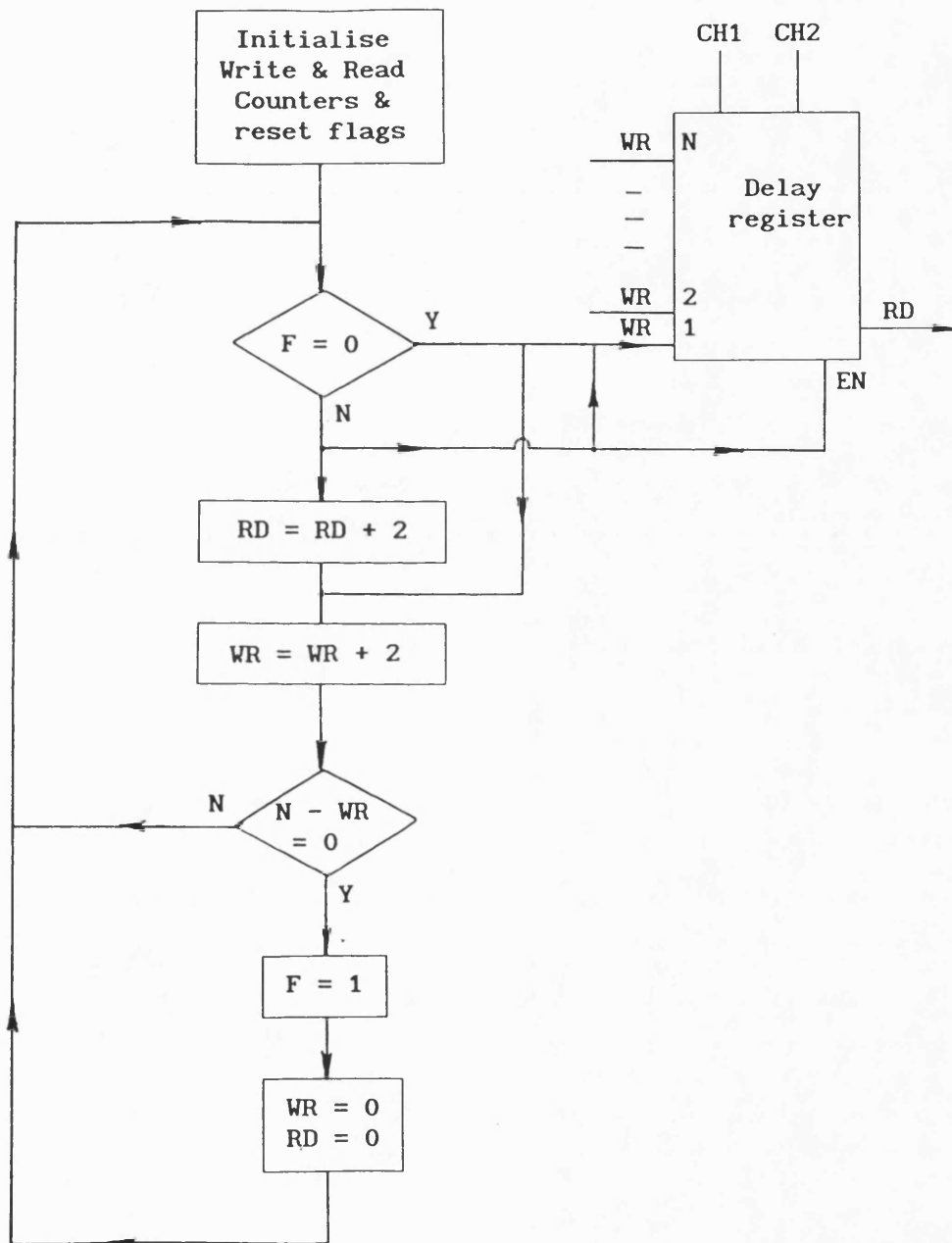
Fig. 7.1    Proposed communication link

Fig. 7.2    Delay routine flow-chart of local cuurent signals

# CHAPTER 8

## SUMMARY, CONCLUSION AND SUGGESTIONS FOR FUTURE WORK

### 8.1 SUMMARY OF WORK

A prototype microprocessor based current differential protection relay has been successfully implemented, based upon an existing CAD design study. This relay is designed to protect three terminal lines and can also be used on two terminal lines. The advantages of using the proposed current differential protection algorithm over impedance, directional and other conventional differential protection as outlined in Chapters 1 and 2 relate in the main to the substantial improvement in the speed of fault detection, stability for external faults and sensitivity to high resistive faults.

The relay employs two versions of signals; one based on total current variations and the other on their superimposed components. The operating signals of the latter are theoretically zero under normal operating conditions and become finite immediately following a power system fault or system disturbance. Furthermore, the relay utilises modal components as opposed to segregated phase currents, thereby virtually eliminating the effect of inter-phase mutual coupling in the relay measurands. The modal components are produced using Karrenbauer Transformation which is employed because its elements are linear, and can be practically employed because of better suitability to all practically encountered faults and also because it can be practically employed using simple differencing amplifiers.

Only the two aerial modes are employed and the earth mode is discarded, thus increasing relay stability in double circuit line applications. The operating principles of both versions i.e. total and superimposed components, are discussed in Chapter 3.

The techniques used to design and engineer the digitally based relay have been presented in Chapters 4 and 5 respectively. The relay equipment was implemented using digital signal processing techniques, for reasons of flexibility and accuracy. It also expands the possibilities of automatic diagnostic testing, thereby increasing the integrity of protection and overall scheme dependability. It is shown in Chapter 4 that the 16-bit TMS32010 processor system is appropriate for this application. The hardware built to interface to the processor is made up of independent modules which make the relay data acquisition unit very flexible, close to a general purpose unit. Up to 8 input/output ports can be used. In this relay only 6 of Them are used and the remaining two ports can be used for the communication channels between the relay and the remote ends. The input/output interface and the synchronization process of the hardware interrupt with the processor have been fully described.

The functions of this microprocessor based relay are software controlled. the basic functions can be identified as: data acquisition, signal processing and decision making. The relay acquires samples of currents every 250 $\mu$s interval and it then uses newly developed signal processing techniques to calculate the estimates of the relaying quantities of the transmission line. These techniques use a set of equations (Chapter 3) to provide a numerical estimate of

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the operating quantity and a sophisticated relay decision logic (Chapter 5) compares the operating quantity with a preset threshold level before giving a decision.

A novel technique developed within the relay is that, the data acquisition unit, with the exception of the analog filter, is fully controlled by the software. The sampling interval, multiplexer timing, A/D, D/A conversion rates and the external RAM are all controlled by programmable counters and the data to the counters is loaded through the data bus. The maximum sample rate which can be used is limited by the provision of enough time for the duty cycle and the maximum conversion rate is mainly limited by the A/D conversion time and time allowance for the S/H and multiplexer. The design of the analog Butterworth filter can be simply modified by the use of variable resistors and capacitors. The analog input filter also has another function (see Fig. 7.1) which makes the interface of the communication link to the microprocessor very simple and thus, the problem of building a sophisticated digital synchronization circuit between the remote samples and the local samples is obviated.

The construction of the DAS unit from separate hardware modules, controlled by software make it suitable for any other protection relays implementing different software algorithms. The hardware may function as one of several relays depending on the software modules used. The relay built using such a hardware would have lower production costs. This will also lead to a smaller inventory of spares for maintenance.

Novel software techniques are employed in implementing the relay algorithm and digital filters described in Chapter 3. A flowchart describing the various processes of the software is shown in Chapter 5.

The effect of power system frequency variations is studied and the implementation of an adaptive sample rate to counteract this effect when applying the superimposed component version is done in the software in conjunction with hardware programmable counter. Ring buffers (circular filters) employing the transfer-replace process used in the extraction of the superimposed components gives very good performance with a considerable savings in time as compared to normal filtering techniques which are implemented by using multiply shift and accumulate procedures.

In Chapter 6 the relay performance is tested by using a programmable transmission line test facility which was developed at the University of Bath power system laboratory, the details of which are given in an IEEE paper in Appendix C. The primary system waveforms were generated by a simulation package also locally developed. Since the relay is a digital type, system faults of electronic levels $\pm10$ volts were fed directly into the relay. The relay settings, stability and sensitivity factors are explained in Chapter 6 which also details The teed-feeder configurations studied. Relay performance for Various fault types, internal and external to the protected line, ranging from single phase faults to three phase faults, different locations and different fault inception angles, are also illustrated in Chapter 6. Also some of the distinctive novel features of the relay

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particularly when it was subjected to some onerous faults such as the effect of a feed around-path, and CT saturation are also included.

In Chapter 7 the characteristics of the proposed fibre optic communication link are outlined. PCM transmission was recommended because of its compatibility with optical fibre, Also LEDs and PIN diodes are recommended for application of the relay over short lines, while LDs and Avalanche photo diodes are recommended for long distance lines and higher transmission requirements. The calculation of the parameters such as the channel distance which can be used without the need of repeaters, bandwidth, and the attenuation on the signal due to the physical properties of the channel are detailed in Appendix B.

## 8.2 CONCLUSIONS

The first overall objective of the work presented in this thesis was to engineer a relaying equipment, in accordance with the basic frame work of a CAD model. This has been successfully accomplished employing state-of-the-art 16-bit microprocessor. Both versions of the relay, the total current version and the superimposed component version were tested and the relay operated correctly for all the tested fault-waveforms. A comparison of the signal waveforms, in particular the Differential and Bias signals has shown a very close correspondence between the signals attained from the practical and theoretical models of the relay.

Furthermore, an extensive series of tests carried out on the particular model using a PTL have shown that the performance obtained from the relay hardware design, both, for internal and external faults is nearly consistent with that obtained from the CAD model. The small differences observed, particularly in relay operating speed, are a direct result of the slightly higher threshold levels which have to be employed in the practical model in order to compensate for small levels of practical noise.

It should be noted that the results presented are mainly for the single-phase-earth fault type, due to the dominance of such type of faults on power system networks.

The ability of the relay to detect a disturbance and produce a decision is dependent on the difference between the absolute differential signal and a percentage of the absolute bias signal being greater than a threshold voltage for a sufficient period of time. The relay average operating time is 5 ms, The fastest times being produced by faults close to the measuring transducers as these result in the largest total or superimposed components.

The smallest total or superimposed currents are generated by faults remote from the relay location , faults at $0^{0}$ inception angles and by high resistive faults, but the minimum current signal levels observed during these investigations are still high enough to give a fast trip decision.

From close inspection of the relaying quantities it was found that the true super-imposed component output of the cascaded filter is

valid only for a half-cycle of power frequency when a symmetry is attained on the postfault data. On the other hand, when a severe fault such as an internal three-phase-earth fault occurs, there is a residual output from the superimposed extraction filter for a full cycle, the latter being a direct consequence of the unsymmetry caused on the postfault waveforms.

On comparing the two versions of the relay, it was found that: in terms of performance, the operating time of the total component version is slightly higher by about 1 ms in the majority of cases over the operating time of the superimposed version. This is so because in the superimposed component version, the relaying quantities become finite faster than those for the total component relay and also because the threshold voltage for the latter is slightly higher to cater for the prefault charging current. An advantage of the the total current variation version is that frequency tracking is not required, because since it is a current dependent relay only, it will not trip for system swings or frequency variations. However, in case of the superimposed version, any drifts in the steady-state frequency give rise to a residual output from the cascaded filter which in turn can affect relay performance. In order to counteract this adverse effect, an adaptive sampling rate for frequency tracking has been incorporated in the relay design.

On loss-of a channel, the channels are in a full duplex mode and there are local detectors at the three ends. If at one end, the detection logic senses a channel failure when not receiving a message from the master end, a standby overcurrent relay with time delay may

take over, or alternatively, a local impedance relays designed to underreach the T-point may be used to protect the three terminal ends.

The relay can be simply altered to protect two terminal feeders in the case of one of the terminal ends being out of service by incorporating a simple logic within the software to ascertain which terminal is idle. The relay algorithm can then be altered to take a decision on the quantities derived from the two remaining terminals only. For example, suppose the local terminal P is idle. Under such circumstance, the Differential and Bias quantities are formed from the modal currents at end Q and R as below:

$$D_{1,2}(t) = Q_{1,2}(t) + R_{1,2}(t)$$
$$B_{1,2}(t) = Q_{1,2}(t) - R_{1,2}(t)$$

The relaying equipment reported here employs a modal transformation which very significantly reduces mutual coupling effects when applying the relay to real untransposed lines. It has been shown that full protection of a transmission teed circuit can be achieved by the two aerial mode elements. This represents a significant saving in hardware over the three phase elements. This approach also allows the relay to be applied to double circuit teed circuits on a circuit-by-circuit basis since earth mode coupling is avoided.

Finally, from satisfactory experience of the newly developed microprocessor-based digital scheme, a number of advantages over more conventional ones become apparent. The most important of these are: a

reduction in operating times, a wide application range, a greater tolerance to fault resistance and an inherent immunity to problems caused by power swings and CT saturation.

Although the relay is recommended to work with fibre optics as a transmission media, however, it can also work equally well with already existing communication channels such as pilot relaying and telephone lines provided that the HS requirements are not essential Further more, with proper reliable microwave links, it can also maintainits full speed. However, a fibre optic communication channel provides the best path of data information transmission which is impervious to EMI and GDR, has a wide bandwidth, and low attenuation. In essence, no major changes in the hardware or software are required to be made to accommodate for the communication link, since the relay is equipped with analog inputs and digitally controlled input and output ports thus making it highly flexible.

## 8.3 RECOMMENDATION FOR FUTURE WORK.

### a) The processor

The TMS32010 has been shown to be an excellent processor inspite of some limitations imposed by the limited number of register pointers which had to be substituted by software counters and the small directly addressable RAM in this relay design. A disadvantage is the short length of the address mapped internal data memory and the absence of communication support. However, for more saving in the external hardware, such as the building of an external data RAM and for further reduction in the software duty cycle, the use of a

newer version of the TMS320 family is recommended. One such version is the The TMS32020. This is a texas instruments' second generation DSP chip. Its enhancements over the TMS32010 include a larger data memory (544 words), 64K program memory space, 64k data memory space, as compared to 144 data memory space and 4k program memory space in the TMS32010. It also includes an on-chip timer and serial port, and support for communication. There are additional addressing modes (5 auxiliary registers), a multiply and accumulate in one cycle operation of 200 ns and additional instructions such as "Compare", "Repeat" and "Wait" instructions which in the case of the TMS32010 these have to be implemented by a combination of instructions thus adding an extra burden on the duty cycle. One of the main advantages of of using the TMS32020 for future developments lies in its ability to be able to directly address 16 input and 16 output channels in comparison to 8 channels by the TMS32010. This feature can prove to be useful if the need arises to expand the interface to the microprocessor to implement full supervisory control of the communication channels within the processor. It should be noted that the change from the TMS32010 to TMS32020 is very simple since the latter is an improved version and most of the software instructions do not have to be changed.

**b) Computer simulation of the optical link.**

Before installing the fibre optic link, calculation of optical link transmission parameters, including fibre loss, splices, connectors, etc, and the effect of dispersion should be estimated. Thus using a computer simulation of electronic circuits and an interface between

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the computer and the communication   channel, some further studies must be carried out to test over what distances a signal data could be transmitted with a bit error rate   below 10E-9 for varying data rate up to 10 Mbit/s. Also the best method for coding and decoding should be decided by doing some experimentation on the transmitter and receiver sections.

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# APPENDIX A

## DIGITAL SIMULATION OF THE FAULT TRANSIENT PHENOMENA ON 3-TERMINAL EXTRA HIGH VOLTAGE TRANSMISSION LINE

### A.1 FUNDAMENTAL RELATIONSHIPS

Any multiconductor transmission line section is defined by its series impedance matrix per unit length Z and corresponding shunt admittance Y. Each element of Z varies with frequency and is determined by the conductor types, their physical geometry and the nature of the earth plane [33].

The theory of natural modes developed by Wedepohl [19] enables a solution to the system voltage steady-state equations given by Eqn. 1 to be transformed into a series of independent differential equations of the form of Eqn. 2.

$$\frac{d^2\bar{V}}{dx^2} = ZY\bar{V} \tag{1}$$

$$V = \exp(-\psi x).\bar{V}_1 + \exp(\psi x).\bar{V}_r \tag{2}$$

where $\psi = Q.\gamma.Q^{-1}$, $Q$ = voltage eigenvector matrix, $\gamma$ = propagation constant matrix.

Matrix function theory permits easy evaluation of the hyperbolic functions, the polyphase surge impedance and admittance necessary for a solution of the problem. For example, the polyphase surge admittance matrix is given by:

$$Y_o = (Q.\gamma^{-1}.Q^{-1}.Z)^{-1} \tag{3}$$

## A.1.1 Transmission line transfer-matrix function

A faulted transmission system essentially consists of a network of cascaded sections. Two-port transfer matrices are particularly useful in the solution of such a problem. For example, with reference to Fig. A.1, the transfer matrix representing a line section , say up to the fault point, is given by Eqn. 4.

$$
\begin{bmatrix} I_s \\ I_f \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \cdot \begin{bmatrix} V_s \\ V_f \end{bmatrix} \tag{4}
$$

where $y_{11} = Y_o.\text{Coth } (\psi x)$, $y_{12} = - Y_o.\text{Cosech } (\psi x)$

## A.1.2 Source-side network matrix

The source network considered here at each terminating busbar is a general source model comprising of some local generation and a number of infeeding parallel lines, each with its own generation, all the generations being based upon arbitrarily defined short circuit levels. This is shown in Fig. A.2.

It is relatively easy to define an equivalent source admittance matrix [YS] at each terminating busbar and this is then used in combination with the corresponding transmission line admittance matrices of Eqn. 4 to form the full fault transient model.

## A.1.3 Frequency-transform technique

The transient phenomenon associated with any disturbance, such as a fault, represents a wide frequency variation and it is therefore necessary to be able to evaluate the transient response over the

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whole frequency spectrum. The inverse Fourier transform given in eqn.5 forms the basis of the method by which the frequency spectrum is used to determine the corresponding time variation of any voltage or current of interest.

$$f(t) = \frac{1}{2\pi} \int_{-\infty}^{+\infty} f(\omega). \ \exp \ (j\omega t) \ d\omega \tag{5}$$

In these studies, a modified half-range form of the basic Fourier integral (Eqn.6), as has been successfully employed for plain feeder applications [33], is used.

$$f(t) = \text{Real} \left[ \exp \frac{(\alpha t)}{\pi} \int_{0}^{\Omega} \delta f(\omega - \psi \ \alpha). \ \exp \ (j\omega t) \ d\omega \right] \tag{6}$$

where $\delta = \dfrac{\sin \ (\pi\omega/\Omega)}{(\pi\omega/\Omega)}$ , $\alpha$ = frequency shift constant.

## A.2 SINGLE-CIRCUIT TEED FEEDER FORMULATION

A general teed feeder as shown in Fig. A.3 represents the system devised to investigate the fault transient phenomena on 3-terminal ehv transmission lines.

The behaviour of a teed feeder system under faulted conditions is as dependent upon the configuration of the surrounding system as upon the individual line lengths of the feeder up to the tee point. In this respect, of particular importance is the presence of feed-around paths between any two ends of the teed feeder. The system shown in Fig. A.3 can be configured so as to have one, two or three feed-around paths of arbitrary lengths. the source networks are

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completely general as discussed previously. The simulation includes the facility to fault the teed feeder on any leg or on a feed-around path.

To provide these facilities, the system is represented by the 5-node model of Fig. A.4. A general relationship for the system with a fault point between P and T, for example, can ba defined as:

$$
\begin{bmatrix} I_f \\ I_p \\ I_q \\ I_r \\ I_t \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} & Y_{15} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} & Y_{25} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} & Y_{35} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} & Y_{45} \\ Y_{51} & Y_{52} & Y_{53} & Y_{54} & Y_{55} \end{bmatrix} \cdot \begin{bmatrix} V_f \\ V_p \\ V_q \\ V_r \\ V_t \end{bmatrix} \qquad (7)
$$

The elements of the admittance matrix in Eqn. 7 are defined as:

$Y_{11} = yfp_{11} + yft_{11}$,  $Y_{12} = yfp_{12}$,  $Y_{13} = 0$,  $Y_{14} = yft_{12}$,  $Y_{15} = yft_{12}$

$Y_{21} = yfp_{12}$,  $Y_{22} = yps + ypq_{11} + yfp_{11} + ypr_{11}$,  $Y_{23} = ypq_{12}$,

$Y_{24} = ypr_{12}$,  $Y_{25} = 0$,  $Y_{31} = 0$,  $Y_{32} = ypq_{12}$,

$Y_{33} = yqs + ypq_{11} + yqt_{11} + yqr_{11}$,  $Y_{34} = yqr_{12}$,  $Y_{35} = yqt_{12}$,

$Y_{41} = 0$,  $Y_{42} = ypr_{12}$,  $Y_{43} = yrq_{12}$,  $Y_{44} = yrs + yrt_{11} + yrq_{11} + ypr_{11}$,

$Y_{45} = yrt_{12}$,  $Y_{51} = yft_{12}$,  $Y_{52} = 0$,  $Y_{53} = yqt_{12}$,  $Y_{54} = yrt_{12}$,

$Y_{55} = yqt_{11} + yft_{11} + yrt_{11}$

It should be noted that each element in equation 7 represents a 3 x 3 sub-matrix for a 3-phase system.

## A.2.1  Prefault calculation

The current constraint applied to the general relation is $I_f = I_t = 0$, where the voltages $V_p$, $V_q$ and $V_r$ are defined by a consideration of the system loading condition. Thus:

$$\begin{bmatrix} I_p \\ I_q \\ I_r \end{bmatrix} = \begin{bmatrix} Z_{22} & Z_{23} & Z_{24} \\ Z_{32} & Z_{33} & Z_{34} \\ Z_{42} & Z_{43} & Z_{44} \end{bmatrix} \cdot \begin{bmatrix} V_p \\ V_q \\ V_r \end{bmatrix} \qquad (8)$$

The elements of the impedance matrix in Eqn. 8 are attained by inverting the admittance matrix Y in Eqn. 7. $I_p$, $I_q$ and $I_r$ are then used to define $V_f$ from the inversion of Eqn. 7. The defined node voltages, combined with the two port admittance relations are then used to define all the prefault currents of interest.

## A.2.2 Fault transient component calculation

For this calculation, Eqn. 7 is constrained so that $I_p = I_p = I_r = 0$ and the system can then be reduced to a fault point relation as given by:

$$\begin{bmatrix} V_f \\ V_p \\ V_q \\ V_r \\ V_t \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} & Z_{15} \\ Z_{21} & Z_{22} & Z_{23} & Z_{24} & Z_{25} \\ Z_{31} & Z_{32} & Z_{33} & Z_{34} & Z_{35} \\ Z_{41} & Z_{42} & Z_{43} & Z_{44} & Z_{45} \\ Z_{51} & Z_{52} & Z_{53} & Z_{54} & Z_{55} \end{bmatrix} \cdot \begin{bmatrix} I_f \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \qquad (9)$$

where $Z = Y^{-1}$.

For a three-phase system, this gives:

$$\begin{bmatrix} V_{fa} \\ V_{fb} \\ V_{fc} \end{bmatrix} = \begin{bmatrix} Z \end{bmatrix} \cdot \begin{bmatrix} I_{fa} \\ I_{fb} \\ I_{fc} \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} \\ Z_{21} & Z_{22} & Z_{23} \\ Z_{31} & Z_{31} & Z_{32} \end{bmatrix} \cdot \begin{bmatrix} I_{fa} \\ I_{fb} \\ I_{fc} \end{bmatrix} \qquad (10)$$

Now considering a single-phase-earth fault involving the 'a' phase, the two healthy phase fault path currents $I_{fb}$ and $I_{fc}$ are zero. $V_{fa}$ is the known quantity and is the transform of a suddenly applied sinusoidal voltage of the form $-V_{fsa} \sin (\omega_o t + \beta)$. $h(t)$ i.e. is simply equal and opposite to the prefault voltage at the fault point as determined in section A.2.1. Thus:

$$I_{fa} = V_{fa} / Z_{11} \qquad\qquad (11)$$

The current $I_{fa}$ substituted in Eqn. 9 then defines the system transient voltages for the fault condition. It should be noted that although not shown here, the modelling of a double-circuit teed feeder is simply an extension of the single-circuit analysis.


## A.3  TYPICAL FAULT STUDIES

The results presented here typify the fault transient waveforms attained by faulting some typical 400 kV teed feeder applications as shown in Fig. A.5.

The commonly made assumption of constant line parameters results in waveforms which contain considerably more distortion than is the case in practice. Furthermore, the travelling-wave components exist for much longer period after fault inception than might otherwise be predicted. Both these latter points are evident from Fig. A.6 which is for an a-earth fault at the T-point on circuit shown in Fig. A.5-a. It can be clearly seen that the assumption of constant 50 Hz line parameters leads to the faulty-phase waveforms, in particular the voltage, being relatively very distorted.

The source parameters, particularly their capacities, significantly affect the fault transient waveforms. Fig. A.7 shows the waveforms,

again for an a-earth fault at the T-point, in which the end P capacity has been reduced to 5GVA. Comparing Figs. A.6 (c-d) and A.7, it can be seen that in the case of the former (larger source of 20GVA) the voltage transients are less significant than when the end P source capacity is small for the latter case. This is so because in the former case the source voltage is much stiffer than the latter. Similar effects are observed in the sound-phase voltages.

Faults not involving earth give rise to waveforms which are generally very noisy. Fig. A.8 shows the waveforms observed for a b-c-phase fault and by comparing these for an a-earth fault for similar source conditions shown in Figs. A.6c-d, it is clear that the travelling waves persist for considerably longer in the former case.

For certain internal fault conditions, a feed-around path can cause non-unit type line protection relays to see a fault as if it were external to the Tee. The feed-around problem is most severe in system configurations of the type shown in Fig. A.5b where the T-point is close to one end (in this case close to end Q). The primary-system current waveforms shown in Fig. A.9 clearly shows that for a fault close to end P, there is a reversal in the polarities of the phase currents at end R only when there is a feed-around path present in the system (Fig. A.1). This is due to a strong current being fed to end R via the feed-around path. The voltage polarities, on the other hand, remain unchanged in both the cases. This effectively means that in schemes which, for example, employ directional comparison protection relays, the relay at end R would incorrectly indicate an out-of-zone condition in the presence of a feed-around path.

In double-circuit Tee applications, there is a possibility of line protection relay instability on the healthy circuit when a fault occurs on an adjacent circuit. This is particularly so for certain types of earth faults which can produce a strong mutual coupling effect between the faulted and healthy circuits. The waveforms shown in Fig. A.10, which are for a b-c-earth fault on one circuit of the system shown in Fig. A.5-c, typify the problems that can be caused by the mutual coupling effect. The very significant transients admitted in the healthy circuit can, in certain high speed relay applications where a much wider bandwidth has to be employed, cause the healthy circuit relay to indicate an internal fault.
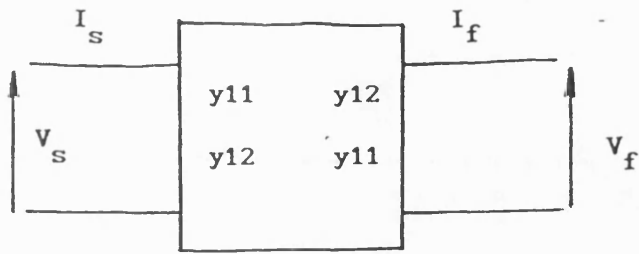
Fig. A.1   Two-port transfer matrix of the line



L1, L2 ...        Ln – infeeding lines

GL, G1, G2 ....Gn – source capacities
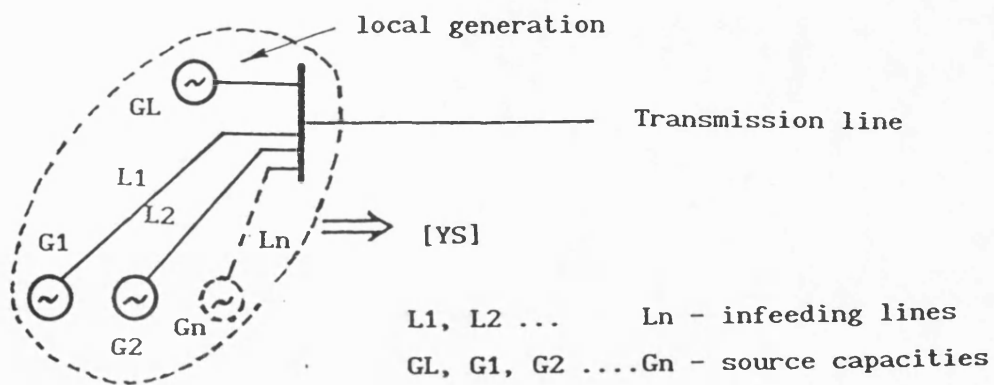
Fig. A.2   Genaral source network
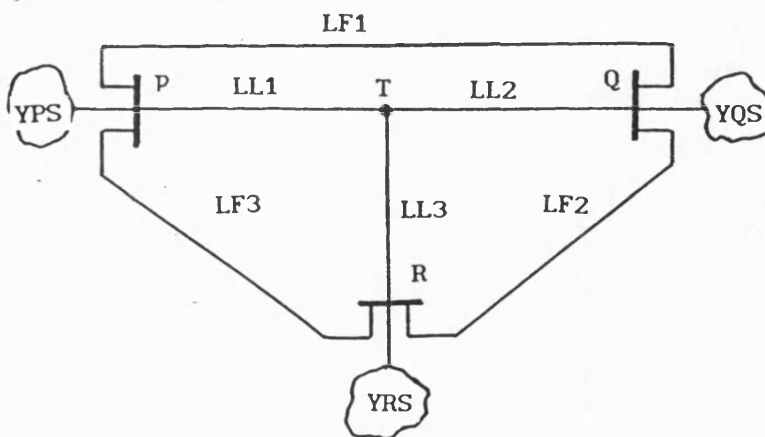


LF1, LF2, LF3 – lengths of feed-around paths

LL1, LL2, LL3 – transmission line lengths up to the tee-point

YSP, YSQ, YSR – equivalent source admittance matrices
                at the terminating busbars

Fig. A.3   Single circuit tee system
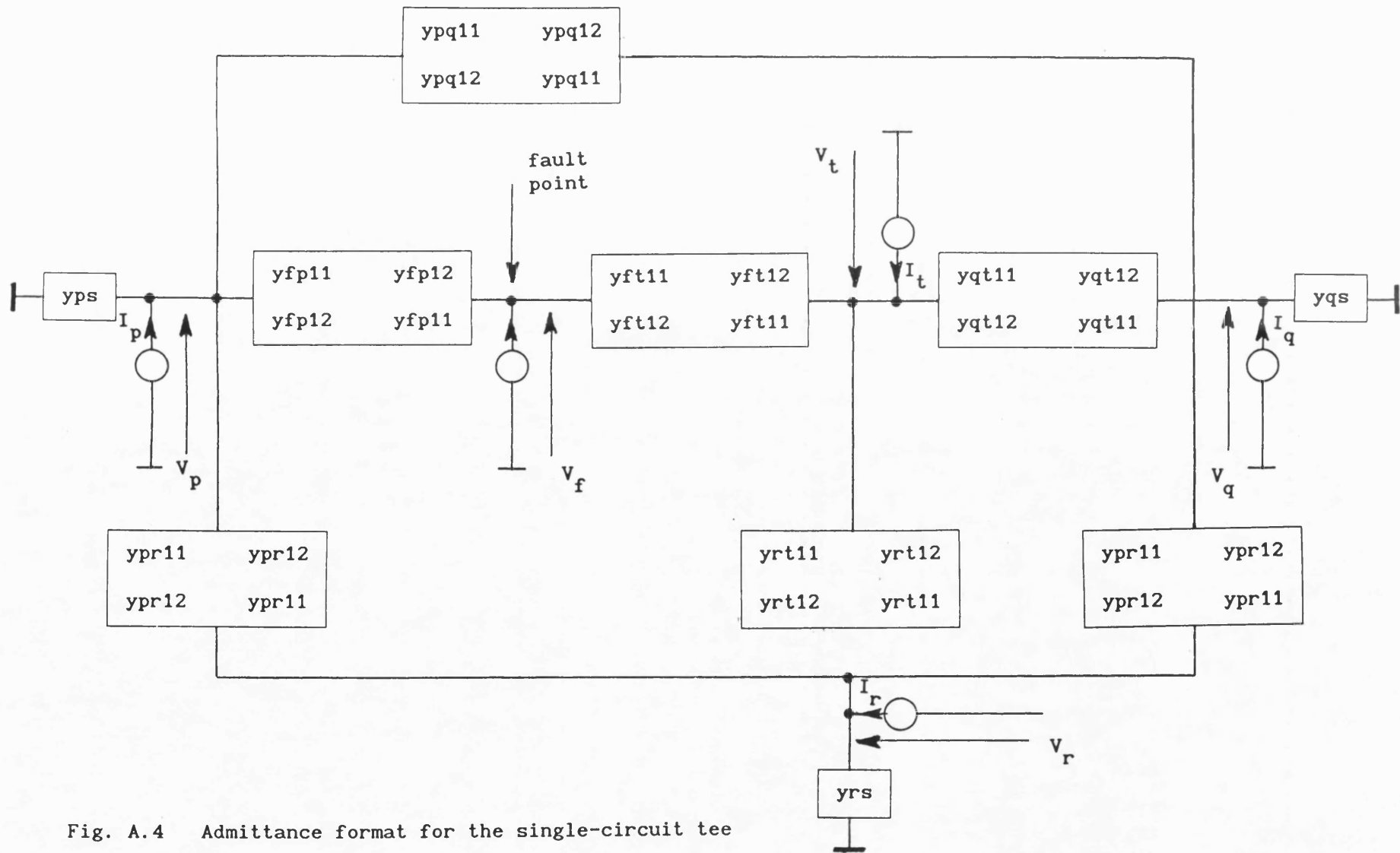
Fig. A.4  Admittance format for the single-circuit tee
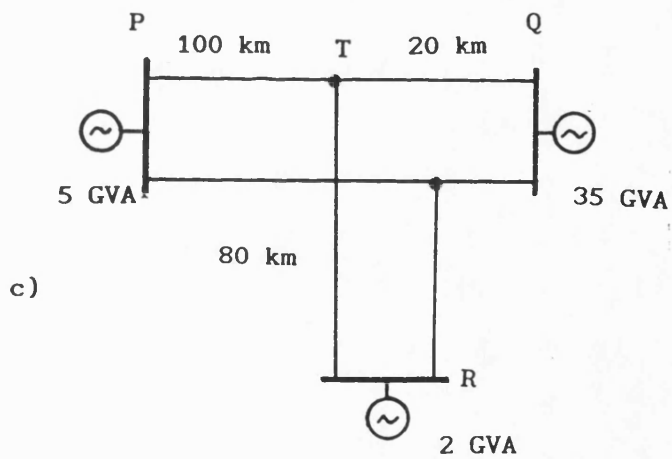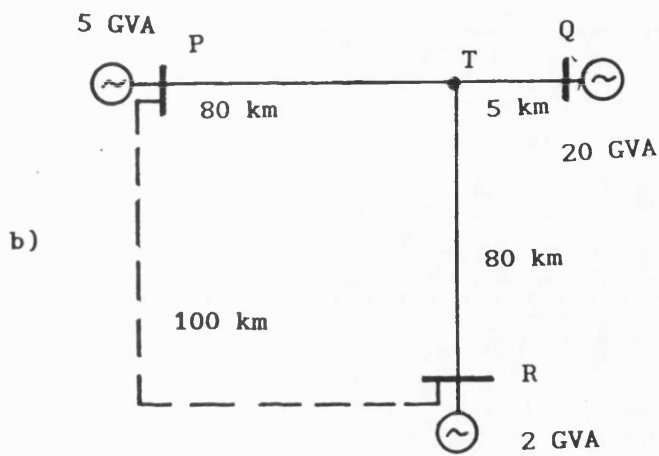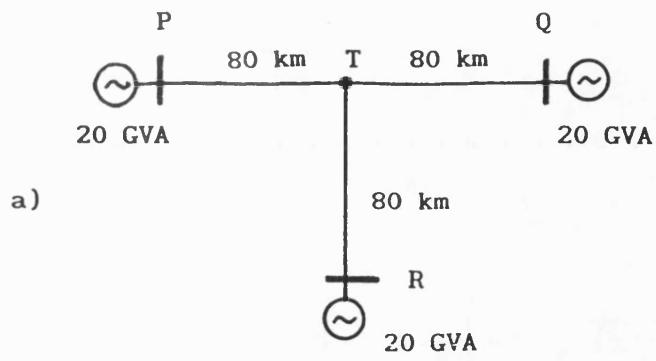
Fig. A.5    System configurations studied
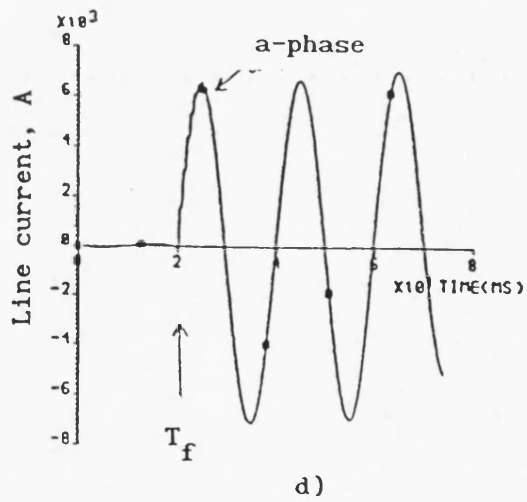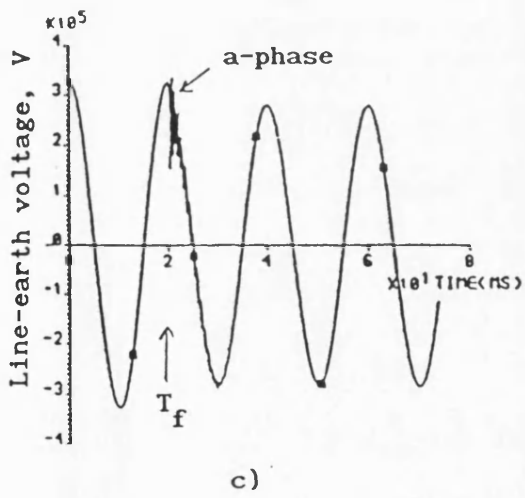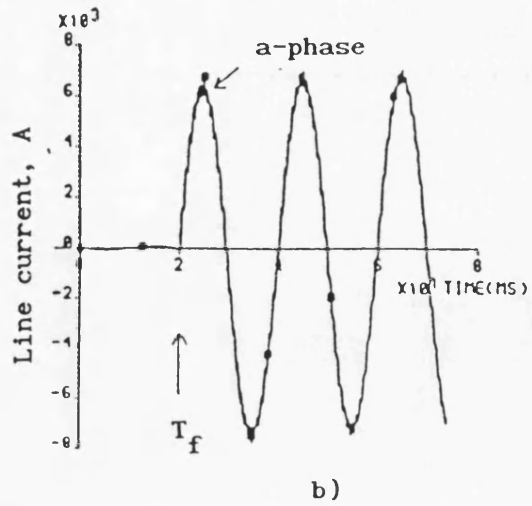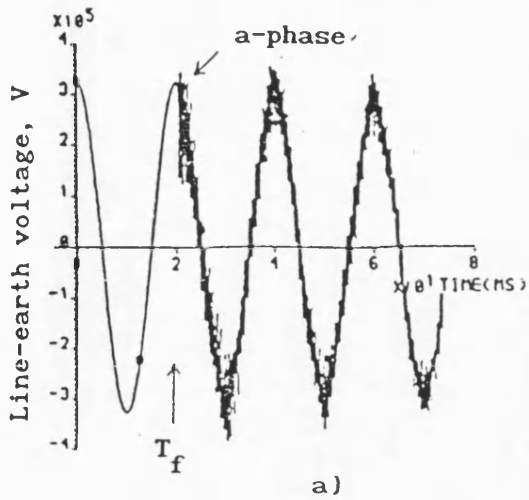
T     -   fault inception

a     -   earth fault at $V_{a}90°$ at T-point

a & b -   const 50 Hz parameters

c & d -   frequency variance of parameters

Fig. A.6   Effect of parameter variance on faulty-phase
transient waveforms; waveforms observed at end P
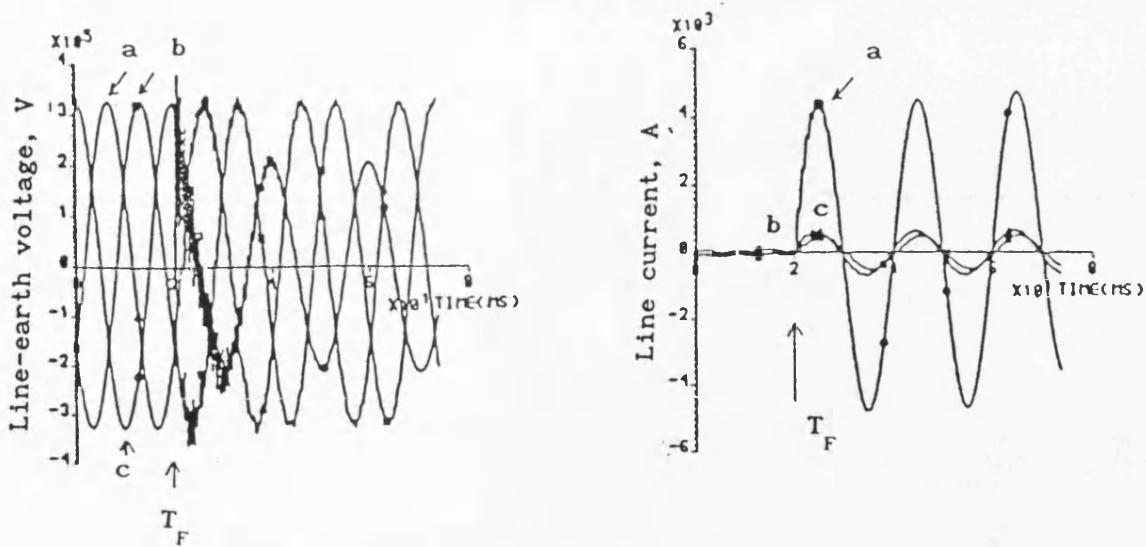
a-earth fault at Va90° at T-point

T - fault inception time

source capacity at end P = 5 GVA

waveforms observed at end P

Fig. A.7    Effect of source capacity on waveforms
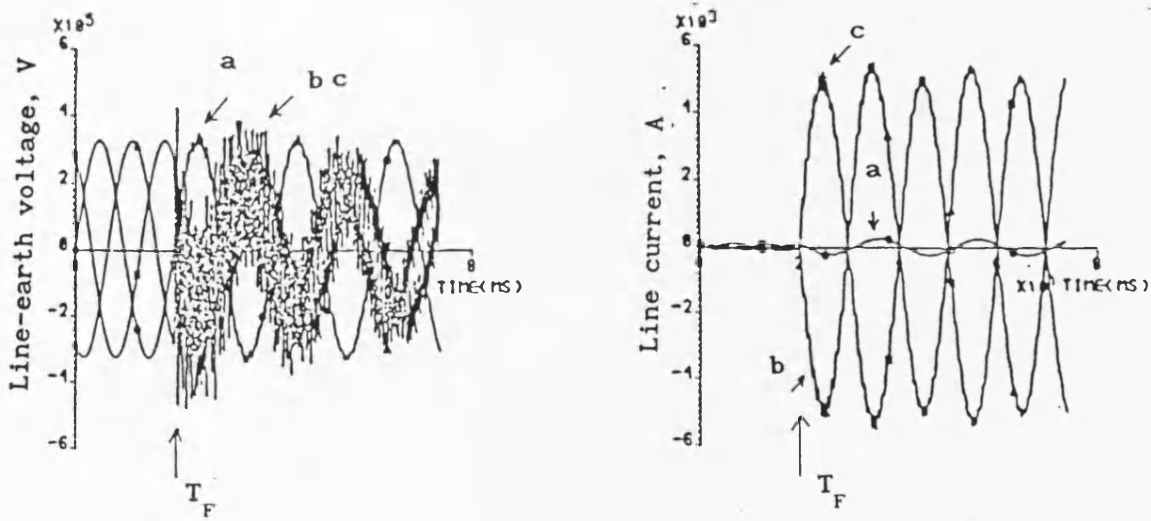


b-c phase fault at Vbc90° at T-point
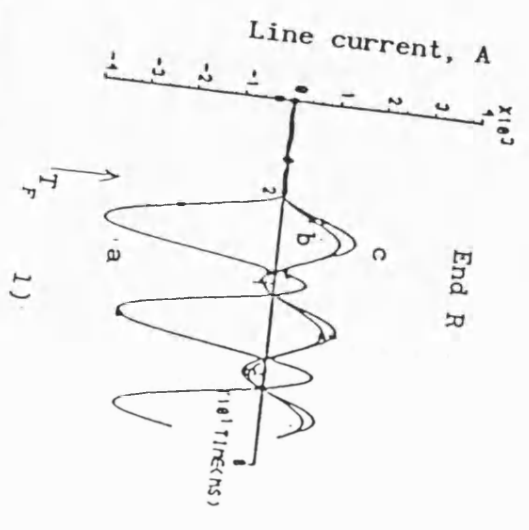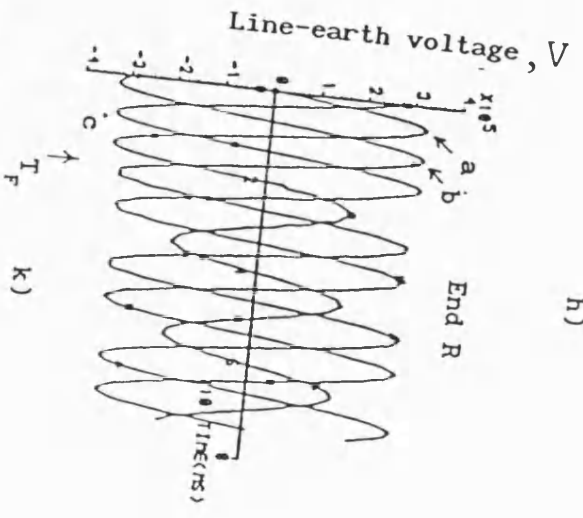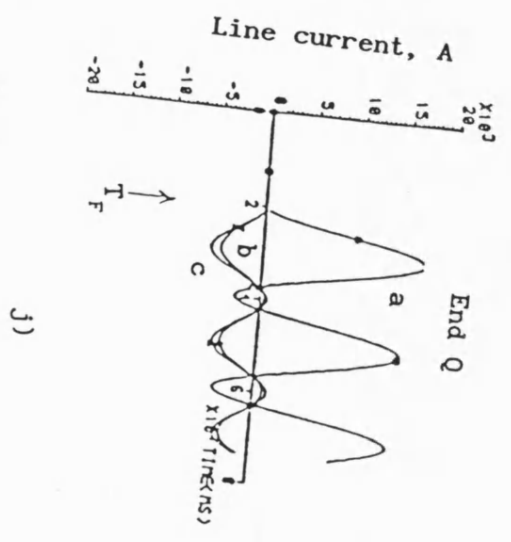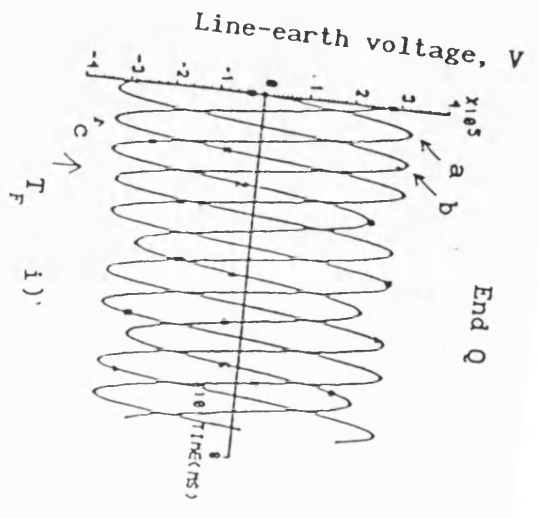
waveforms observed at end P

T - fault inception time
 F

Fig. A.8  Waveforms for a phase fault

Fig. A.9  Effect of a feed-around path on busbar waveforms
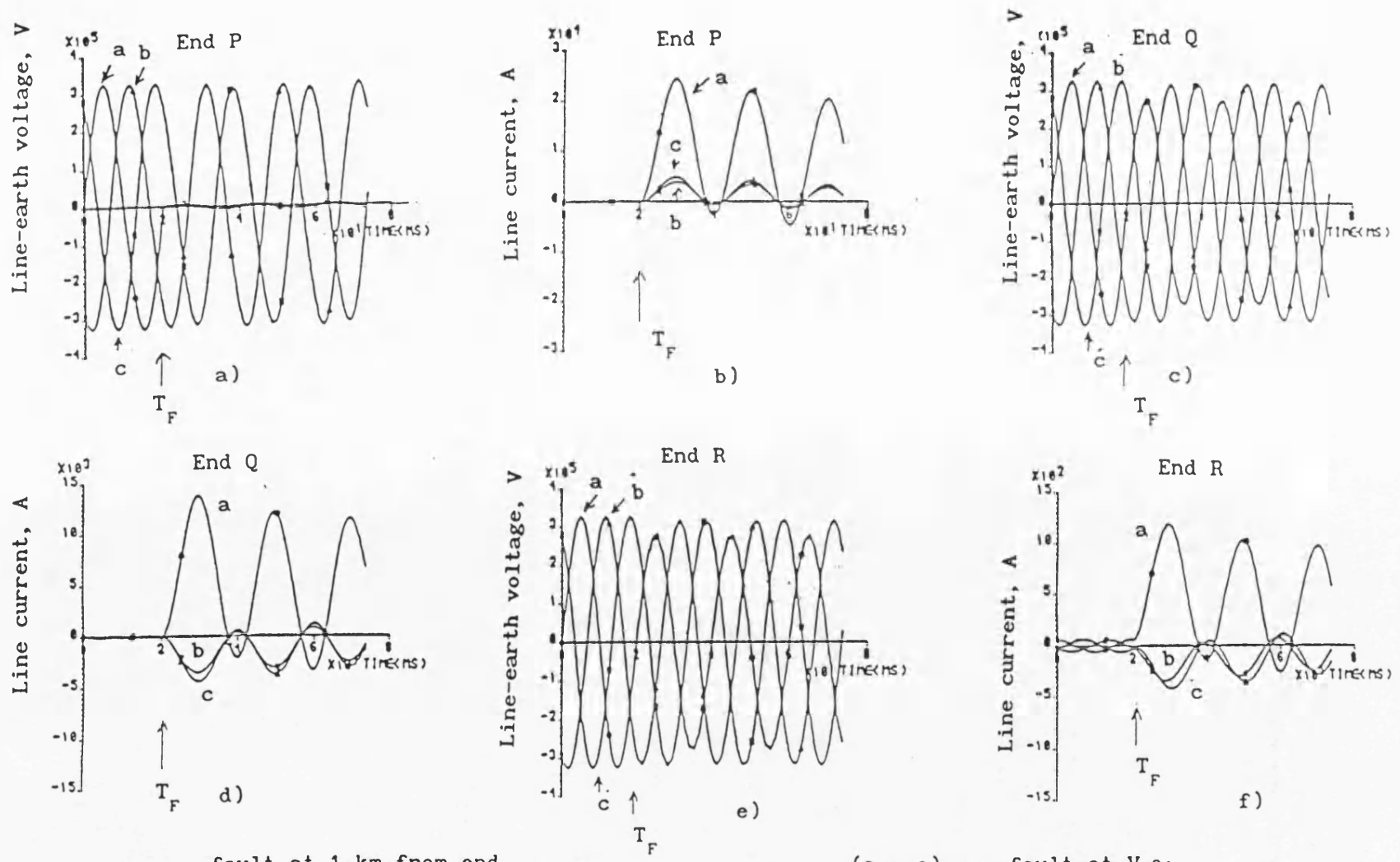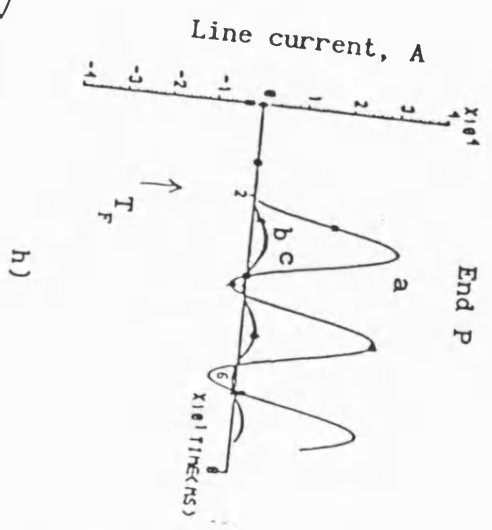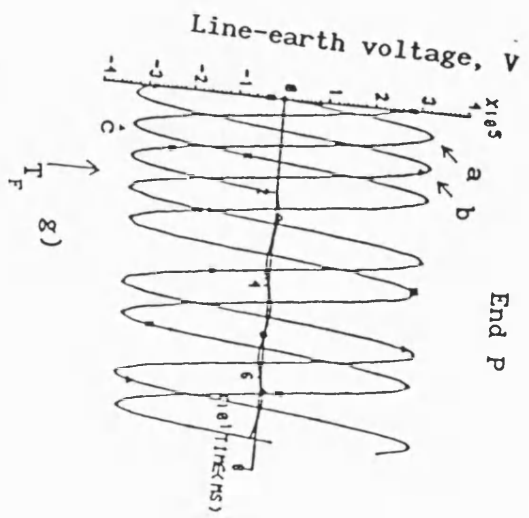
fault at 1 km from end

$T_F$ - fault inception time

(a - e)  -  fault at $V_{a0}°$

(a - f)  -  no feed around path

Fig. A.9 Effect of a feed-around path on busbar waveforms

Fault at 1km from end P; $T_F$ – fault inception time; (g – l) – with feed around path

# APPENDIX B

## STRUCTURES AND TRANSMISSION PROPERTIES OF OPTICAL FIBRES

### B.1 SINGLE MODE AND MULTI-MODE

Fibre optic transmission is made possible by a phenomenon called total internal reflection. Fibres act as waveguides, in which the light is confined to the inner part of the fibre called the core, and by an outer layer called cladding. The boundary between the core and cladding appears as a partial mirror, reflecting light rays which hit the boundary below a certain angle back into the core, thus causing it to propagate down the fibre.

Two main types of optical fibres are available in the market; those which have an abrupt change of refractive index between the core and cladding are called "step index fibre", and others which have the index of refraction maximum at the centre of the core and gradually decrease with radial distance from the centre are called "graded index fibre". The former are used for short distances because of their limited bandwidth, while the latter are suitable for long distances and high speed applications.

The various light paths, through a fibre are known as "transmission modes". A high order mode fibre is one where the reflection angle is near to critical angle and a low order mode is one where the path is near to parallel with the axis of the fibre. The number of modes which can propagate along a fiber is determined by the core diameter, the numerical aperture and the wavelength.

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## B.1.1  Single-mode Fibre

When the diameter equals the wavelength, only a single-mode will propagate. Therefore, the single-mode has a small core diameter. This means that little modal dispersion (pulse spreading) will occur in the fibre which in turn allows the signal bandwidth to be extremely large. However, due to the small core diameter, it is difficult to achieve and maintain efficient coupling between a light source and a single-mode fibre; in fact only the light source of laser diodes can achieve this successfully.

## B.1.2  Multimode fibres

These are characterized by a large core diameter than the single mode fibre. The number of mode scan propagate along the large core fibre. This permits more efficient coupling to the light source which can employ low cost light emitting diodes (LEDs) or laser diodes. In multi-mode, because of light travelling the different path length of different mode, Rayleigh scattering and dispersion are introduced, which both of them affect loss and bandwidth respectively for use at long distance.

However, compared with single-mode optical fibre systems, multimode optical fibre systems have two significant disadvantages: 1) Modal dispersion is large and difficult to control. 2) Modal noise is higher, due to time-varying, modal-distribution-related interference effects and so multimode optical fibre system are typically limited to short-distance and low-bit-rate optical transmission application. For EHV protection system, due to long

distance transmission, the single-mode optical fibre has distinct advantages over multimode these are:

1) The very-high-bandwidth potential of single-mode fibres ensures future new services can be easily adapted for a wide variety of applications and easily modified to cope with increasing demands.

2) Single-mode fibre technology is compatible with OEIC (optoelectronic integrated circuits ), which is promising for future low-cost, high reliability system applications.

3) Single-mode fibres have lower losses and are less expensive than multimode fibres.

## B.2    TRANSMISSION    LIMITATION    AND    FACTORS    CAUSING    SYSTEM    IMPAIRMENTS

The most obvious transmission limitations are due to fibre transmission loss and dispersion [44-46]. In addition, in a single-mode fibre transmission system, there are other important system degradation factors associated with the interaction of the optoelectronic devices and components with the transmission media that can cause system impairments. These factors, for example, include mode-partition noise, reflection-induced noise, etc. However, in the bit rate of optical fiber transmission system below 100 Mb/s, these factors, including the dispersion, can be negligible.

### B.2.1  Transmission attenuation

Signal attenuation in fibres is attributable to mechanisms that are

related to: a) material effects, b) geometrical effects, c) joint effects, d) cladding and jacketing effects, and e) leaky modes.

**a) Materials Effects (main loss effects).**

Loss mechanisms due to material effects include light absorption by impurities such as Hydroxyl (OH) and transition-metal ions, inherent absorption by the ultraviolet edge of the electronic bands and the infra red edge of the vibrational bands of the constituent glass materials, drawing-induced absorption, Rayleigh scattering by refractive-index inhomogeneities frozen into the glass lattice [40].

The technology for fibre fabrication is advanced to a level that, basically, only intrinsic effects like Rayleigh scattering and infrared absorption limit the losses. Spectral attenuation is the loss of useful signals along a fibre. Fig. B.1 shows the loss spectra of a low-loss silica fibre. It is clear that the low-loss transmission windows are around 1.3 $\mu$m region and 1.55 $\mu$m region. Typically these two wavelength regions are used for long-distance single-mode fibre transmission. The minimum loss is about 0.7dB/km near 1.3 $\mu$m and 0.5 dB/km near 1.56 $\mu$m for high-quality single-mode optical fibres.

**b) Geometrical Effects**

Loss mechanisms associated with geometrical effects include 1) irregularities like core-cladding interface imperfections and core geometry variations, 2) microbends (microscopic random bends) resulting from coatings and cabling, and 3) possible unavoidable curvatures or bends in the installed cable. However,

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with suitable design and careful fabrication, the added losses from these causes can be made very small.

c) Joint Effects.

Alignment problems geometry and refractive-index differences between fibres can lead to losses when joining or splicing fibers. At present, multimode-fiber splicing with average losses in the vicinity of 0.2 dB are obtained routinely in the field. Although splicing of single-mode fibres requires more care, however in a laboratory environment, an average loss of 0.1 dB has been achieved using the fusion techniques.

d) Cladding and Jacketing Effects.

Fibres often have cladding materials with higher loss than the core materials and also, jackets of very-high-loss material suppress unwanted cladding modes. The fibre technicals would result in a very small percent of the guided mode being effectively eliminated from the transmission process.

## B.2.2 Pulse Dispersion

The transmission bandwidth of a fibre is determined by its structural and physical parameters, as well as its material properties through chromatic and intermodal dispersion. Chromatic dispersion is caused by propagation delay differences amongst different spectral components of the signal and includes material dispersion and waveguide dispersion. Intermodal dispersion is caused by group delay differences amongst modes and is

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governed principally by the refractive-index profile of the multimode fibre.

## B.3    OPTICAL FIBER TRANSMISSION DISTANCE CALCULATION

The different implications of the loss-limited and dispersion-limited transmission has been briefly discussed in an early section. Here the calculation of optical transmission distance (Lm) is described. Loss-limited system operation means that the power-budgeting consideration limits the transmission distance. For example,

$$( \text{ transmitter power } )  = Pt \, [ \, dBm \, ]$$
$$( \text{ receiver sensitivity } ) = Pr \, [ \, dBm \, ]$$

Lm = ( Pt - Pr)[dB]/( average fibre link loss )[dB/km]        **(1)**

The fibre link loss includes fiber loss, splice loss, and the loss due to connectors, fiber couplers, and any other inter-connecting components. For example, assuming we have a single-mode fibre system operating at 1.3-um with Pt =  3 dBm, Pr = -34 dBm, and an average fibre link loss of 0.41  dB/km  (C-SMF at  1.3-um), the maximum loss-limited  transmission fibre length is:

Lm = (37/0.41 ) km =  90 km.                        **(2)**

Dispersion-limited  transmission   occurs  when the power budget allows for  transmission over  a length Lm, but the achievable transmission distance is  shorted  than  Lm  from  loss calculation alone,   because the dispersion-induced signal   pulse broadening causes significant intersymbol   interference between transmitted

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neighbouring pulses. This is usually the case with higher-bit-rate systems with large overall dispersion. Significant inter-symbol interference occurs when the pulse broadening is larger than half the bit period. This is of no consequence to the application described here because the transmission bit rate is much smaller.
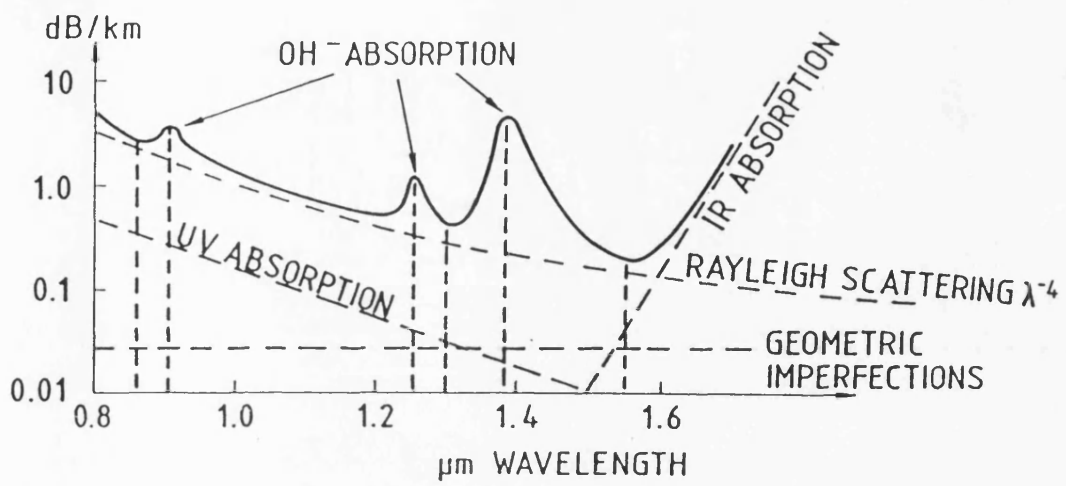
Fig. B.1   Typical spectral attenuation for commercially available fibre

APPENDIX C

# DESIGN AND TESTING OF A NEW MICROPROCESSOR-BASED CURRENT DIFFERENTIAL RELAY FOR EHV TEED FEEDERS

R.K. Aggarwal          A.H. Husseini          M.A. Redfern, MIEEE

School of Electrical Engineering,
University of Bath,
Claverton Down,
Bath, BA2 7AY, England.

Abstract – The hardware design and laboratory testing of a new high speed Current Differential protection scheme for application to EHV Teed Feeders is described. Special emphasis is placed on designing the relay comparator and its associated data acquisition units for inputing data into the comparator from a laboratory-based Programmable Transmission Line. The hardware is based on a high speed digital signal processing processor utilising a protection algorithm, previously developed using CAD techniques.

Key words – Current Differential Protection, digital relaying, EHV Teed feeders, three-terminal lines, microprocessor applications, power systems, fibre optical communications.

## INTRODUCTION

The advantages of employing microprocessors in protective relaying for power systems are well known [1,2]. These, for example, include i) standardization of hardware for many types of protective schemes, ii) higher sophistication in protection achieved by flexibility of software design, iii) smaller burdens for CT and CVT circuits, iv) easier interface with other digital communication and control systems, and v) reduction in size of equipment.

Microprocessor digital relaying equipment, developed and presented here, realises conventional Current Differential principles as applied to Teed feeders. Although such principles are generally regarded as the ones best suited for protecting such lines, it is only recently that communication channels, such as fibre optical links (FOLs), have become available that are capable of transmitting information with a sufficiently large dynamic range and over a distance compatible with requirements of EHV line protection. Furthermore, recent advances in microchip technology, such as high speed digital signal processing (DSP) chips, has made it feasible to be able to develop new high speed digital techniques for fault detection on such lines using Current Differential principles.

A paper by Aggarwal and Johns[3] describing the basis of a new high speed Current Differential protection scheme for three-terminal lines was first published in 1986. Although the equipment described was based on CAD studies, nevertheless, it clearly demonstrated the suitability of the techniques developed for Teed-feeder protection and also provided valuable information and experience for future hardware development of the digital relay. The experience gained, for example, included a knowledge of the accuracy requirements for analogue-to-digital conversion and also the type of DSP chip required, particularly in terms of speed and

on-chip memory.

In 1987, a full-scale development of the digital relay model using state-of-the-art hardware technology was initiated at Bath University. In this respect, because of the requirements for extensive high speed signal processing in real time, the Texas Instruments TMS32010 DSP chip[4] was chosen.

The protection algorithm for the aforementioned processor is based on an extensive series of simulation studies (as reported in reference [3]) which have resulted in the development of software both with high computational efficiency and excellent protection capability.

This paper describes in some detail the developments undergone in designing and building the hardware model, including the data acquisition units. It also briefly describes the relay algorithm and concludes by presenting some interesting test results of the relay performance. For the latter, analogue current waveforms from a Programmable Transmission Line (PTL) (see reference 5) for practically encountered faults on some 400kV applications are utilised.

The paper is divided into four sections:
i)    Relay hardware
ii)   Relay software
iii)  Test system
iv)   Tests, results and conclusions

## RELAY HARDWARE

A simplified representation of the Teed-feeder protection scheme as applied to a three-terminal line system is as shown in Fig. 1.
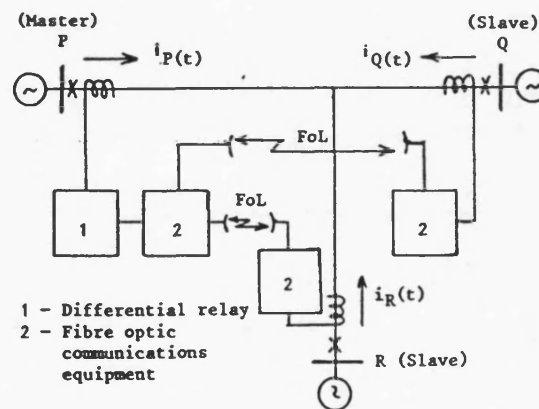


Fig. 1   Single line representation of the basic system

Although in practice, the front-end of the relay at the Master end comprises a current interface module (CIM) to convert the secondary

outputs from the main line CTs into equivalent voltages, however, for the relay hardware model described herein. the emphasis has been placed on designing the microprocessor-based relay comparator and its associated data acquistion units. The effects of both practical CTs and CIMs on the relay input signals have nontheless been included by extending the primary system simulation of the fault transient current waveforms, accordingly. As discussed later in some detail, the latter has been implemented via the impulse responses of the CTs and CIMs, which in turn have been generated from frequency response tests carried out on practical models of the equipment. It should be mentioned that this approach is justified and gives an accurate indication of what actually happens in practice.

The FOLs have been represented simply by time delays which depend upon the time taken for the Aerial mode signals to be transmitted from the Slave to the Master ends. This approach is again justified, firstly because of the electromagnetic noise immunity of the communication links and secondly because of their very wide bandwidths. For further details see Appendix A.

#### The current interface module (CIM)

Fig. 2a shows a block diagram of the practical model of a CIM. It comprises a transformer-reactor (Transactor) core which has an air gap of 5mm. Since the Transactor transfer function is an approximate differential function plus a single pole, an integrating circuit which has a complementary zero is included in the CIM design. The combined circuit then produces an essentially flat response to within ±0.5dB from 2.5Hz to 1kHz, as shown by the practical response of Fig. 2b. This bandwidth was considered to be sufficient since fault current waveforms are generally dominated by low frequency components.

As mentioned previously, for the relay described herein, the effect of the CIM on input signals is included via its impulse reponse shown in Fig. 2c and which is the inverse of the frequency response shown in Fig. 2b. Time domain Convolution Techniques based on impulse responses are then applied to the current waveforms from the main line CTs to produce the expected outputs from the CIMs. Anti-aliasing filters, which are 2nd order low-pass Butterworth, are also included as part of the CIM.

#### Modal mixing circuits

On an actual system, the relay scheme would be arranged such that the modal mixing to convert phase currents into Aerial mode values is exacted at the three ends of the Tee. This approach is adopted because it is then necessary to transmit only two signals over the FOLs from each Slave end to the Master end. In practice, each modal mixing circuit consists of summing amplifiers which are arranged to combine the outputs of current interphases (phase variations) to effect the phase-modal transformation. However, for the relay design described here, the transformation is effected as part of the primary system simulation so as to keep the front-end of the laboratory model of the relay, simple.

#### Designed relay hardware

Fig. 3 is a block diagram of the designed hardware. It consists of four major elements:

i)    Low-pass analogue filters
ii)   Sample and hold circuits, analogue multiplexer
iii)  Analogue to digital (A/D) converters
iv)   Microcomputer

The test facility (as described later), comprising a PTL, was designed to facilitate relay testing and evaluation in the laboratory.

Low-pass analogue filters: Because of the D/A conversion process within the PTL, its analogue output is of a staircase nature. Low-pass filters have therefore to be employed to smooth the sharp pulses. In order to avoid aliasing, the maximum bandwidth of these filters should be $f_s/2$Hz where $f_s$ is the sampling frequency. They must distinguish clearly between the frequencies below the Nyquist limit, which are required, and those above, which must be removed. For the relay described here, the input data is sampled
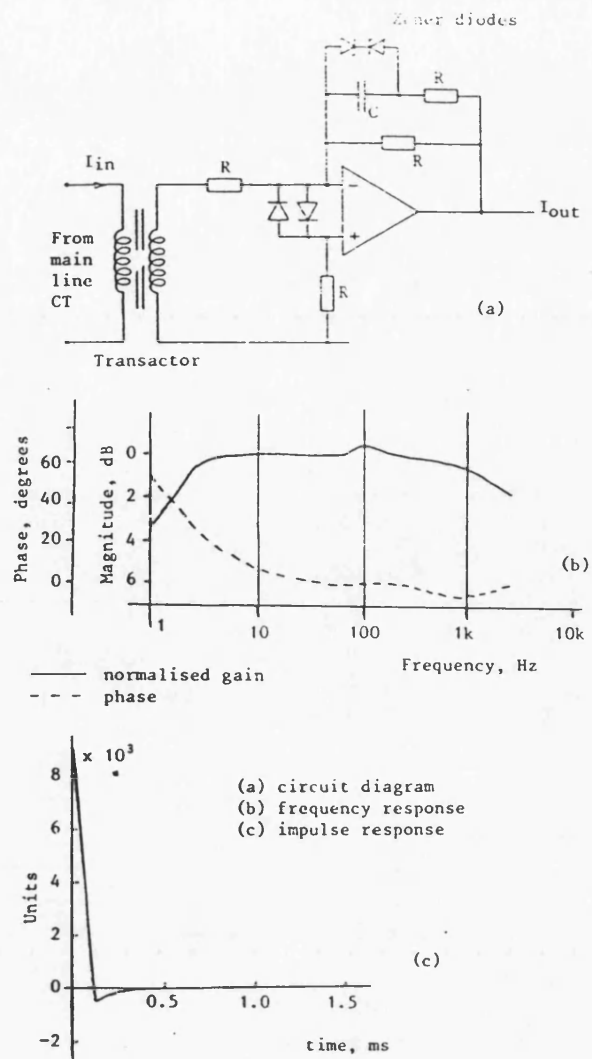


Fig. 2 Current input module circuit and response

at 4kHz and the bandwidth of the low-pass filters, which are 2nd order Butterworth, is about 1.5kHz. This allows a margin of about 0.5kHz between the edge of the filter passband and the Nyquist frequency and is necessary because realisable filters require a finite transition band between pass band and stop band.

Sample and hold circuits: The filter outputs are samples at instants presented by the clock at a rate of 4kHz. Six devices are used to sample and hold (S/H) instantly data from the six channels of the PTL. Monolithic S/H amplifiers with acquisition times of $4\mu s$ are used. It is necessary to employ six S/H devices rather than execute the conversion serially through just one device. This approach is adopted so as to minimise errors in the sampled signals due to time stagger introduced between the sampling of the six signals. For example, if the six signals are assumed to be pure sinusoids, then it can be shown that, using the serial approach through just one S/H device, the error introduced in the digitised signals (via a $10\mu s$, 12-bit A/D converter) would be approximately 50 quantum levels between the first and sixth signals.

Analogue multiplexer: A standard eight-channel multiplexer comprising an FET switch with bipolar level converters and drivers
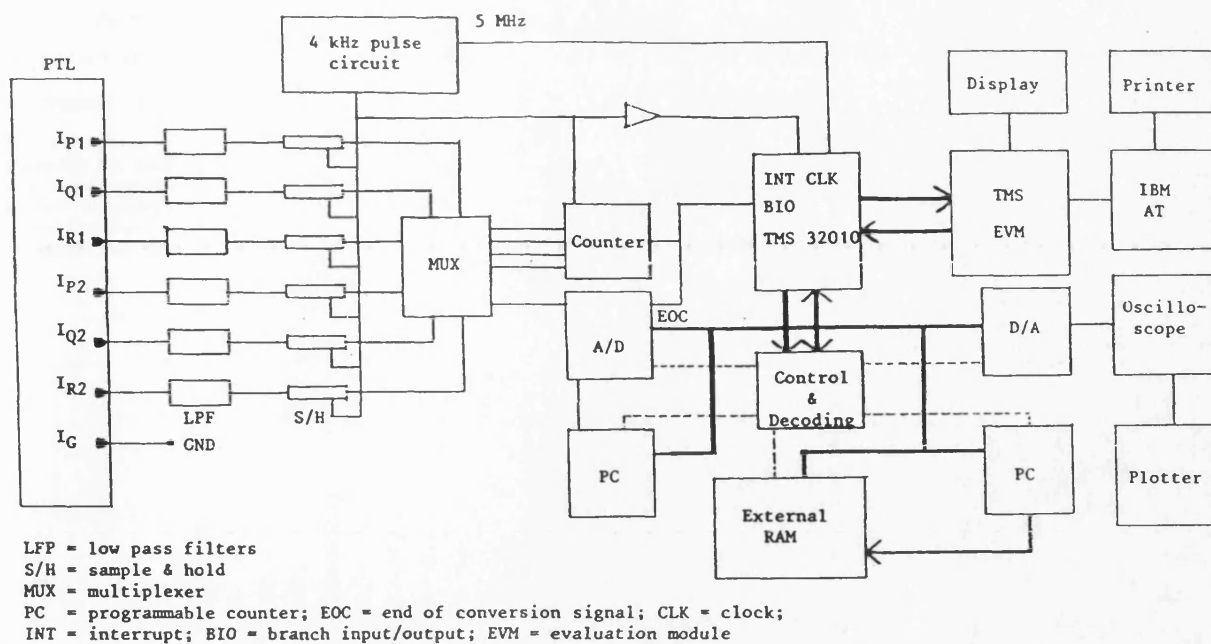
2

PTL

$I_{P1}$
$I_{Q1}$
$I_{R1}$
$I_{P2}$
$I_{Q2}$
$I_{R2}$
$I_G$

LFP = low pass filters
S/H = sample & hold
MUX = multiplexer
PC = programmable counter; EOC = end of conversion signal; CLK = clock;
INT = interrupt; BIO = branch input/output; EVM = evaluation module

Fig. 3 Microprocessor differential relay block diagram

and a conversion time of 3μs is used.    This is driven by a counter
which changes its state from one signal to the next depending upon
the completion of the conversion by the A/D converter.    The
presence of any spikes in the multiplexed signals is significantly
reduced by providing a delay of 2μs in the software before initiating
the start of the conversion signal.    Once all the six samples have
been converted, the counter then automatically resets the multiplexer,
ready to receive the next set of six samples.

A/D converter:    The muliplexed analogue data is converted into
binary data by a 12-bit A/D converter which has a conversion time
of 10μs and is configured for bipolar analogue inputs between ±10V.
The output is buffered and connected to the input BIO (branch on
input/output) port of the microprocessor.

Microcomputer:    The microcomputer is based on the Texas
Instruments TMS32010 DSP chip.    It accepts data from the A/D
converter, executes the protection algorithm and makes a decision
about the fault based on signals from the algorithm.    A DSP
processor is similar to a conventional microprocessor, but is designed
for signal processing at a very high sample rate.    The speed
improvements are due to a special internal architecture which enables
most instructions, including a 16 x 16 bit multiplication, to be
executed in one processor cycle (200ns).    In addition, the processor
is extensively pipelined, allowing one instruction to be executed and
a second read from memory simultaneously.    As a result, the
processor operates at 5 MIPs.    The module also includes 8k words
of EPROM program memory, 144 words of on-chip RAM data
memory and 2k words of external RAM data memory.

When the data acqusition system (DAS) is triggered by the start
pulse, the first input signal is sampled and converted by the 12-bit
A/D converter into an equivalent digital number.    The A/D
converter is connected to the BIO pin of the DSP processor and the
processor reads in the number, followed sequentially by the other
five sampled signals.    The sampled data from the six signals is thus
shuffled into internal registers of the microprocessor RAM in
approximately 60μs.    DAS is then disabled until a new start pulse
retriggers the conversion sequence.    A new set of samples for the
six signals are transmitted to the DSP processor every $1/80^{th}$ of
power frequency period.

RELAY SOFTWARE

Operating principle

The protection algorithm is based on the principle as outline in
reference [3].    Essentially it hinges upon deriving a Differential
quantity D(t) and a Bias quantity B(t) at the Master end and these
are given in continuous form by

$$D(t) = i_P(t) + i_Q(t) + i_R(t) \qquad (1)$$

$$B(t) = i_P(t) - i_Q(t) - i_R(t) \qquad (2)$$

In these equations, the currents are the instantaneous values at the
three ends P, Q and R of the Teed circuit.    In its simplest form,
the relay would operate for faults when the magnitude of the
Differential quantity exceeds that of the Bias by a certain
pre-defined threshold value $K_S$ as shown in equ. 3.

$$\left|D(t)\right| - \left\{K_B\left|B(t)\right| + K_S\right\} - O_P(t) > 0 \qquad (3)$$

$$\leftarrow \quad \left|S(t)\right| \quad \rightarrow$$

However, in order to ensure dynamic stability for faults external to
the Teed circuit, a specially developed trip logic algorithm, in which
both the magnitudes and polarities of the signals are checked over a
number of samples, is employed.

The protection algorithm is based on the two Aerial modes of
currents rather than phase values[3].    The formation of the modal
signals is based on the Karrenbauer transformation (see Appendix B)
and the signals are of the form:

$$I_1 - \frac{1}{3} \quad (I_a - I_c) \qquad (4)$$

$$I_2 - \frac{1}{3} \quad (I_a - I_b) \qquad (5)$$

The Differential and Bias signals at the Master end then become:

$$D_k = I_{Pk} + I_{Qk} + I_{Rk} \qquad (6)$$

3

$$B_k = I_{Pk} - I_{Qk} - I_{Rk} \qquad (7)$$

where $k = 1$ or 2.

## Superimposed extraction filter

The relay protection algorithm must have the flexibility of either comparing the total variation of the Differential and Bias signals or their superimposed components[3]. In order to attain the latter, it is thus necessary to devise a circuit function to extract these components from the total signal variations. The use of a cascade arrangement of the type shown in Fig. 4, comprising full cycle and
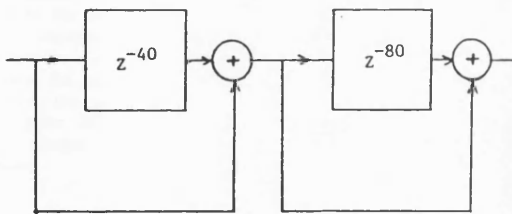


Fig. 4   Cascade extraction filter arrangement

half cycle extraction filters, provides the exact superimposed component for half a cycle of power frequency after a disturbance and has a frequency response which makes the relay virtually immune to errors caused by frequency drifts of up to $\pm$ 5% in the nominal power frequency. The filter has a Z-plane transfer function of the form:

$$H(Z) = (1 + Z^{-40})(1 - Z^{-80}) \qquad (8)$$

In the relay described here, this filter is included as part of the protection algorithm and is implemented as a finite Impulse Response filter. The latter involves realising the function shown in equ. 8, to attain its time-domain impulse response and then, applying convolution techniques, to obtain the required outputs.

## The trip logic

As mentioned before, in order to ensure relay stability for external faults, in particular under CT saturation conditions, it is necessary to apply a sophisticated trip logic[3]. If involves checking both the magnitudes and polarities of the Differential signal D whereby a trip counter is incremented by one only when four consecutive samples have the same polarities and, also at the same time, when their magnitudes exceed the magnitude of signal S (equ. 3). A trip decision is asserted when the counter attains a value of 4. Failing to meet any one of the two criteria, results in the counter being decremented by 1. The counter is not allowed to go below zero at any time.

## Protection algorithm implementation

For the relay described herein, the protection relay algorithm based on equs. 1 – 7 was implemented and tested. The algorithm consists of a power–up initialisation sequence, the protection algorithm loop and the A/D interrupt routine. The operating structure of the program is described in Fig. 5. Execution of the protection algorithm loop, which runs once every 250$\mu$s, begins when the sample rate counter activates the start pulse. At the start of a loop, the data is acquired, converted from A → D and processed, the total processing time for all the operations being approximately 170$\mu$s. This is well within the 250$\mu$s period of the 4kHz sampling rate, i.e. 70% of the duty cycle, and thus allows for a comfortable safety margin. The process is then repeated until a tripping decision is reached. This is indicated by a 5V flag on the output
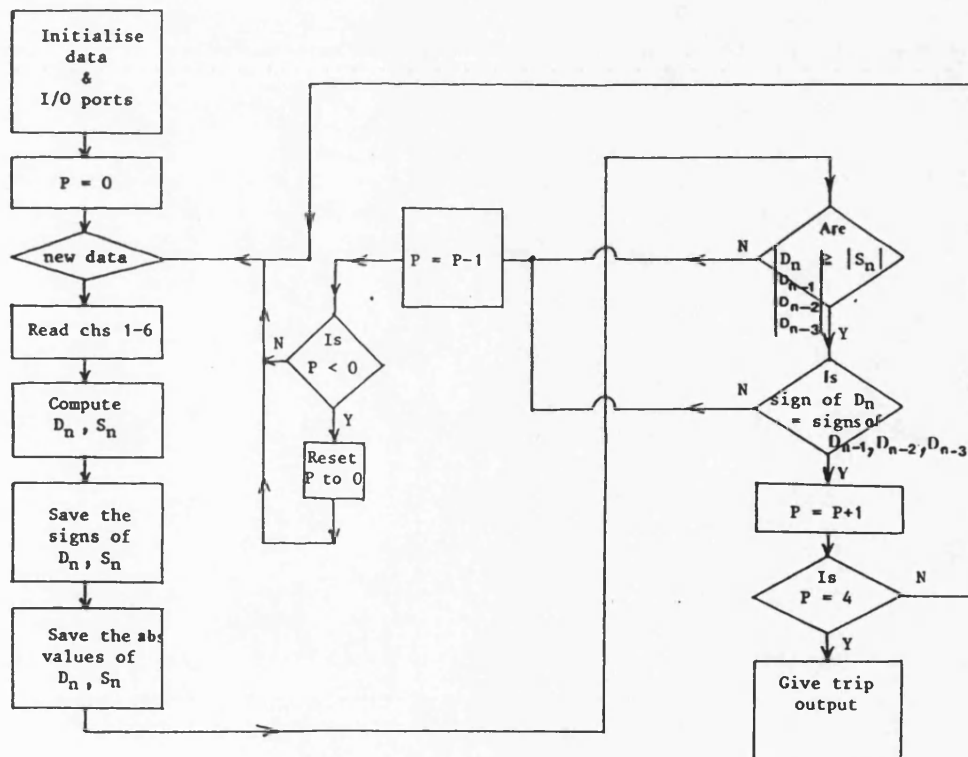


Fig. 5   Differential relay software flowchart

4

port for an internal fault and 0V for an external fault. Once a decision has been taken, the relay then resets and is ready to start again.

## TEST SYSTEM

The relaying hardware was tested using a microcomputer PTL. Details of the system are given in reference [5]. Briefly, the PTL concept is based on storing fault transient data from a power system software simulation on a microcomputer and playing it out in real time, using a specialised interface system which includes D/A converters. In this respect, it should be mentioned that the power system simulation, which is based on Frequency Domain techniques[6], is a well proven technique and has been extensively used in the development and testing of a number of other protection relay algorithms. The desk-top microcomputer provides a convenient man-machine interface and mass data storage facilities for storing the simulation results. With this approach, the current outputs can be made to accurately correspond to signals found at any point in the power system. Moreover, the power system configuration and system conditions can be changed as and when desired.

## TESTS AND RESULTS

The relay hardware and software were tested using simulation results for faults on typical Tee configurations of the type shown in Fig. 6.
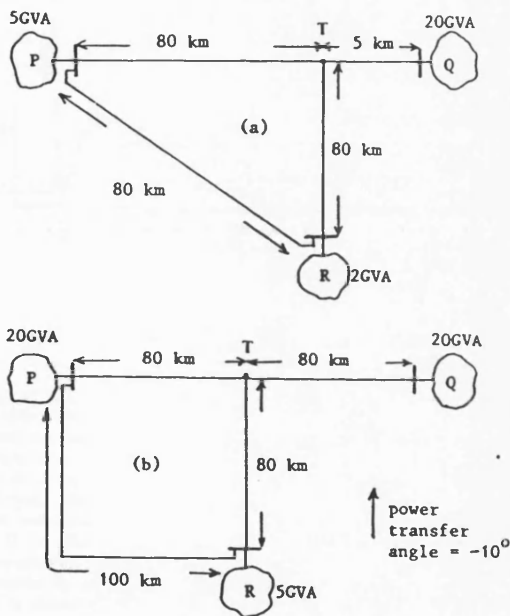


System voltage = 400 kV
X/R ratio = 30; $Z_{s0}/Z_{s1}$ = 0.5

Fig. 6 Typical tee configurations studied

### Typical outputs from relay hardware

Since the relay hardware design described here is based on CAD techniques, it is important to validate the hardware outputs using results attained from the simulation studies.

An internal fault study: Fig. 7 typifies the relay outputs for an a-phase-earth fault at voltage maximum and at the T-point of configuration shown in Fig. 6a. It can be clearly seen that both the Differential D(t) and Bias B(t) signals from the hardware model very closely correspond to those produced from the simulation studies and this is true for both the total and superimposed variations of the signals. The slightly 'steppy' nature of the outputs in the case of the former is due to the conversion of the digital information within the microprocessor into an analogue form, for the purposes of displaying the waveforms. The results nonetheless prove the correct design of the relay hardware and its associated protection relay software.

As expected, the signals remain small throughout the prefault period but become significantly finite on fault inception, the magnitude of the Bias signal being much smaller than that of the Differential signal. In the case of the superimposed quantities, there is a finite output for only about half a cycle of power frequency, this being due to the nature of the extraction filter employed. The figure also interestingly shows the presence of current clipping experienced for this strong internal fault condition, this being reflected in both the Differential and Bias signal components. The Operate signal Op(t) stays below zero during the prefault period and gives a trip output at approximately 4.0 and 3.5ms after fault inception, for the total and superimposed signals, respectively. These tripping times are slightly higher than those attained from the CAD studies, these being 3.5 and 3.0ms respectively for the latter. This is so because, in the hardware design, the threshold levels had to be raised slightly so as to counteract the presence of small levels of practical noise.

An external fault study: Fig. 8 shows typical relay outputs for an external b-c-phase fault at $V_{bco}$0, close to the end Q of the circuit shown in Fig. 6b. First of all, comparing the hardware output signals with those from the simulation studies, it is apparent that, like the case for the internal fault, there is again a very close correspondance between the signals from the two outputs, thus providing further proof of the correct operation of the relay hardware. Again as expected, the signals become finite only on fault inception, the magnitudes of both the Differential and Bias signals, however, being much smaller than those for an internal fault. It is interesting to note that for this external fault condition, whilst the Bias signal is predominently at power frequency, the much smaller Differential signal comprises very distinct high frequency components which rapidly change in polarity, the latter being a characteristic of the external fault Differential current in high speed Current Differential relaying. There is of course no clipping of the signals because the CIM gain has been carefully chosen to prevent clipping for the worst case external fault condition[3]. However, the nature of the signals is such that the Operate signal Op(t) never consistently exceeds zero in accordance with the trip logic, to assert a trip decision.

### Some novel features of the relay design

This relay design has a number of distinct advantages over conventional Current Differential relaying and other types of protective schemes as applied to Teed circuits. These include
i) immunity to the presence of feed-around paths and CT saturation;
ii) high fault resistance coverage. Although, originally, these advantages were ascertained using CAD studies, nonetheless, it is important to verify that this is also true in practice.

Effect of a feed-around path: The primary system current waveforms shown in Fig. 9 clearly show that for the Tee configuration shown in Fig. 6a, there is a reversal in the polarity of the phase currents at end R only, as the fault, which is an a-phase-earth fault at voltage maximum, moves from the T-point to that close to end P. This is due to the current fed to end R via the feed-around path becoming stronger as the fault moves closer to end P. This effectively means that in certain types of non-unit type and Directional Comparision relays, the relay at end R would incorrectly indicate an out-of-zone fault condition. In the case of the relay described here, however, it can be clearly seen that the relay hardware gives high speed reponse when employing either total or superimposed components and this conforms to the performance attained from the relay design based on CAD techniques.
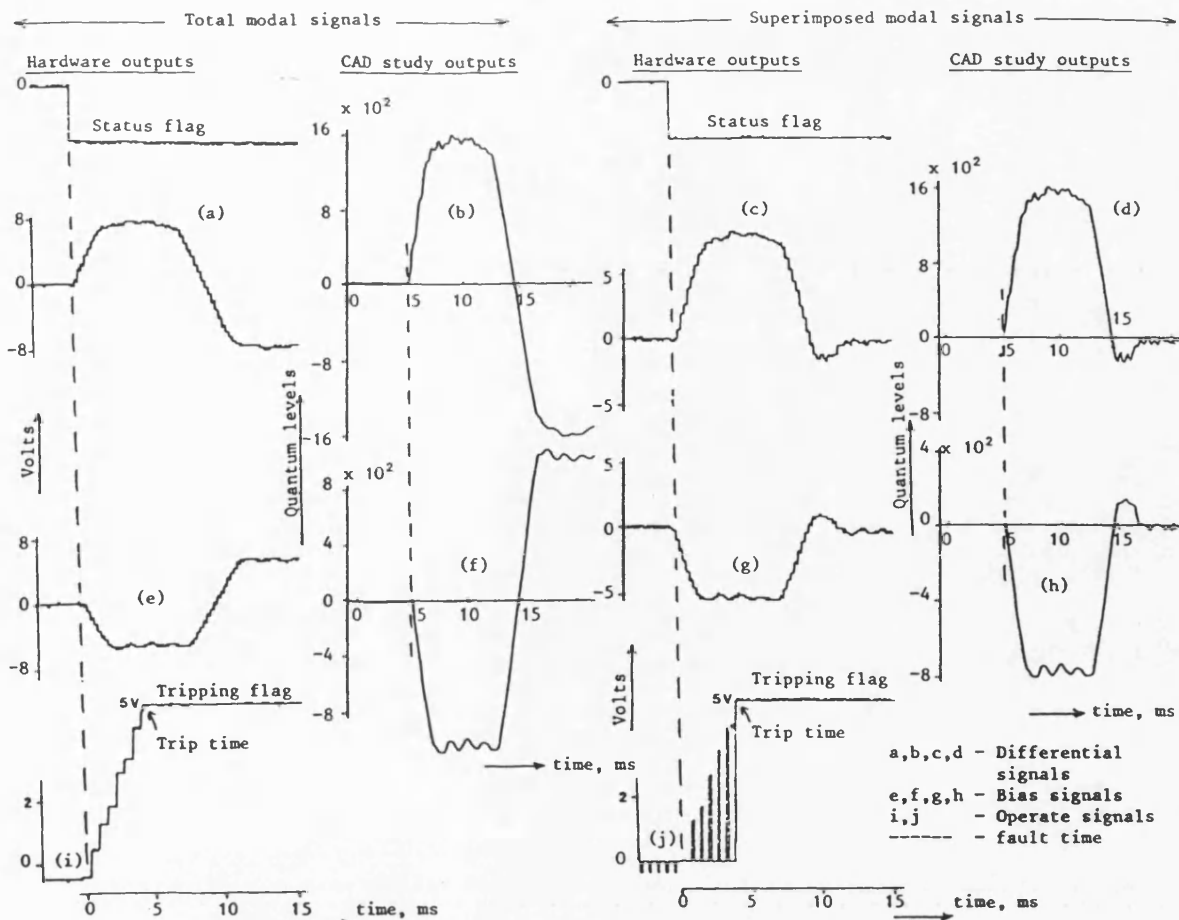
Fig. 7 Relay signals for an internal fault

**Effect of CT saturation:** In order to determine the likely effect of CT saturation, the relay hardware was subjected to fault waveforms causing an extreme degree of CT saturation at end Q of the Tee configuration shown in Fig. 6b. In the CT model, a purely resistive burden of 150VA (at rated 1A secondary current) was employed, the latter causing the model CT coreflux at end Q to reach saturation during an external b-c-phase fault at $V_{bco}$ near end Q, as shown by Fig. 10. The CT model was arranged so that on saturation, the CT output currents totally collapsed to zero, again as shown in Fig. 10b, thereby giving a more onerous test condition than is actually the case in practice.

First of all, considering the Differential signal (Fig. 10c), it can be clearly seen that, as expected, it remains near zero even after fault inception, until such time as the onset of CT saturation, whereby large, short duration pulses are introduced into the signal. Although these pulses cause the Differential signal to momentarily exceed the dynamic threshold signal, however, the nature of the trip logic prevents the relay from giving a trip output. This is apparent from the Operate signal Op(t) (Fig. 10e) which although can temporarily go positive, yet never sustains a positive value for long enough time for the counter to attain the required level to give a trip decision. This performance again is in line with that attained from the CAD studies.

**Relay fault resistance coverage:** An extensive series of tests using fault transient simulation results from the PTL have shown that the hardware designed relay gives a performance consistent with that attained from the relay design based on CAD techniques, as proposed in ref [3]. Some of these have been already highlighted in the aforementioned sections and another test sequence performed was to examine the sensitivity of the relay to fault resistance. It is evident from the results shown in Fig. 11 that the performance of the hardware design is slightly inferior, in terms of both operating times and fault resistance coverage, than that attained from the theoretical model. These small differences in performances are, however, expected by virtue of the fact that in the hardware design, the threshold levels are slightly higher than those for the relay based on CAD studies. The relay performance based on superimposed components is nonetheless superior to that based on total components, again as evident from the figure.

## CONCLUSIONS

This paper has shown that a high speed, Teed-feeder Current Differential protection relay based on CAD techniques can be engineered into a practical model using digital signal processing technology. The protection algorithm, which includes all the necessary filtering and a sophisticated trip logic, has been implemented on a single DSP processor.
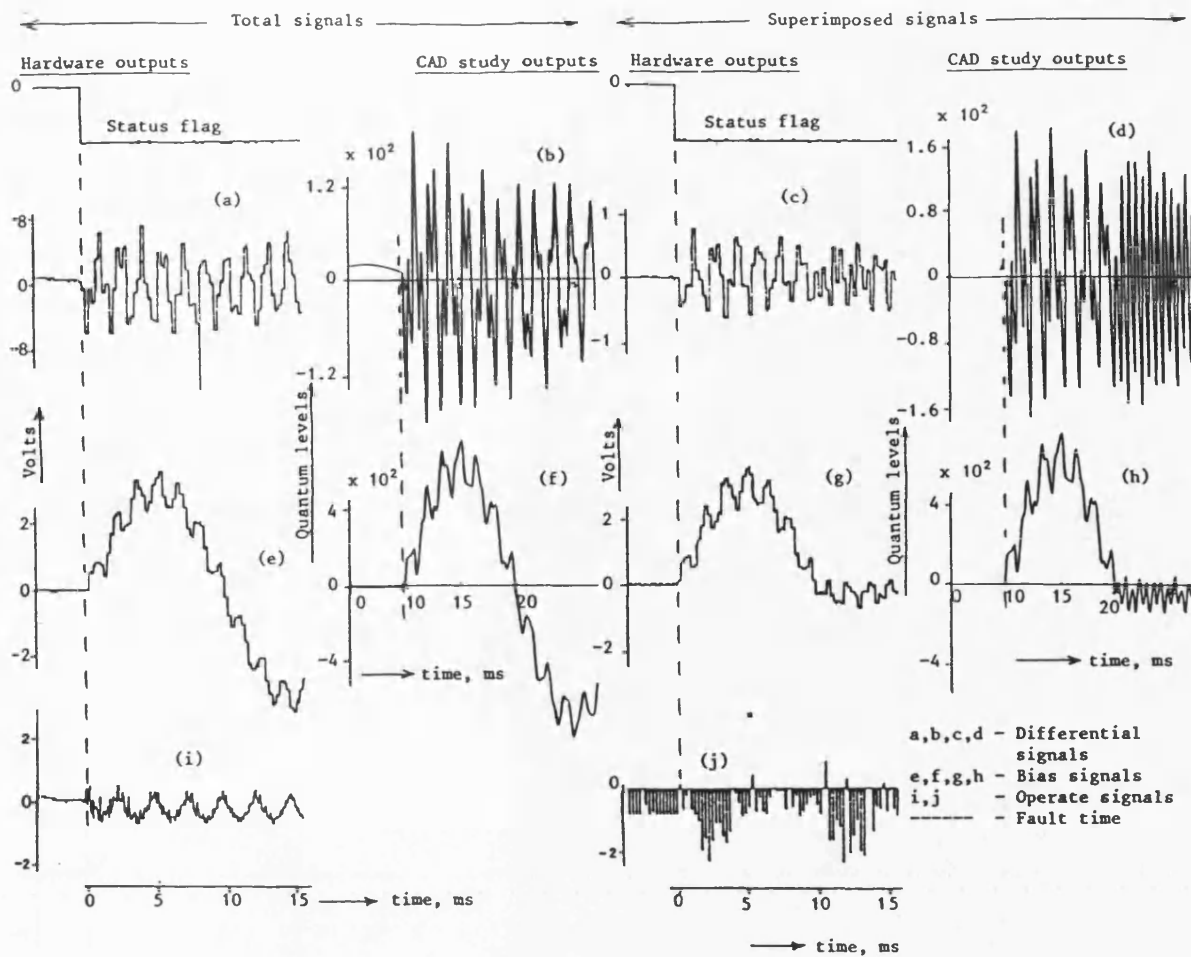
6

Fig. 8 Relay signals for an external fault

A comparision of the signal waveforms, in particular the Differential and Bias signals, has shown a very close correspondence between the signals attained · from practical and theoretical models· of the relay. Furthermore, an extensive series of tests carried out on the practical model using a Programmable Transmission Line, has shown that the performance attained from the hardware design, both for internal and external faults, is nearly consistent with that obtained from the CAD techniques. The small differences observed, particularly in relay operating speeds and fault resistance coverage, are a direct result of the slightly higher threshold levels which have to be employed in the practical model in order to cope with small levels of practical noise.

From the satisfactory experience of the above described development, the authors conclude that this newly developed microprocessor-based digital relaying scheme is highly viable from a commercial point of view.

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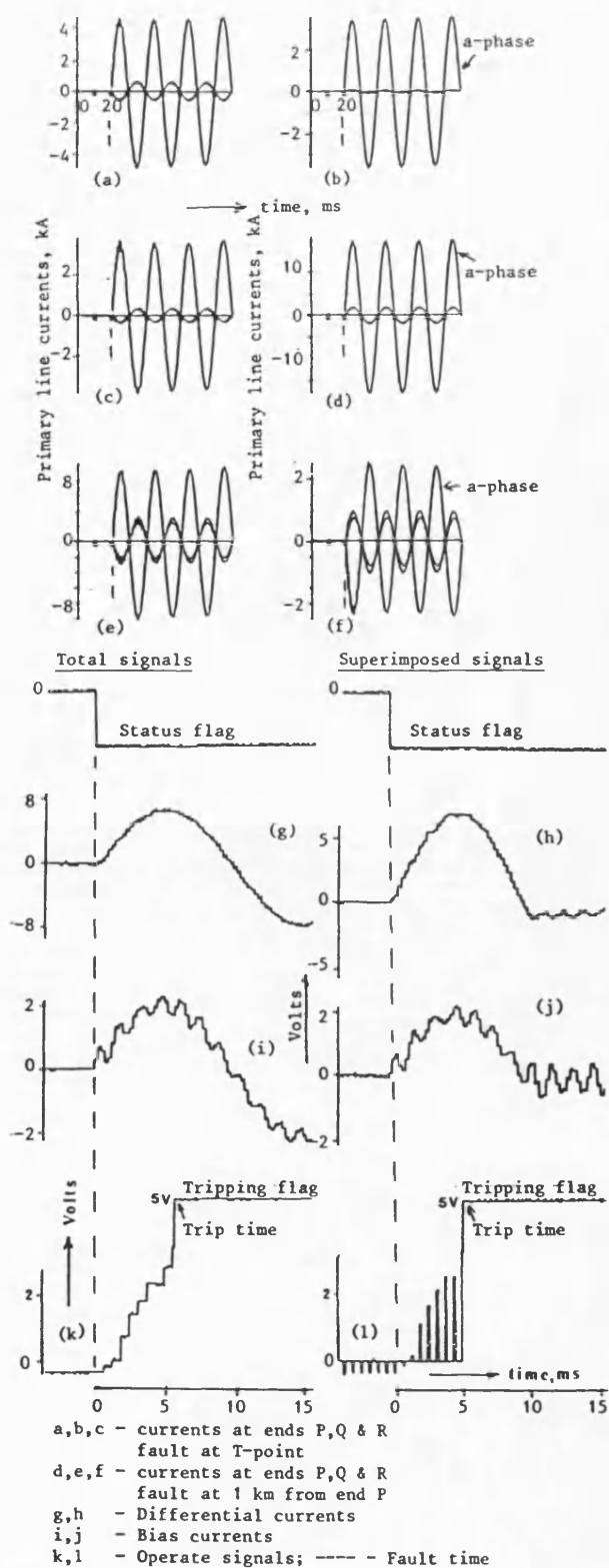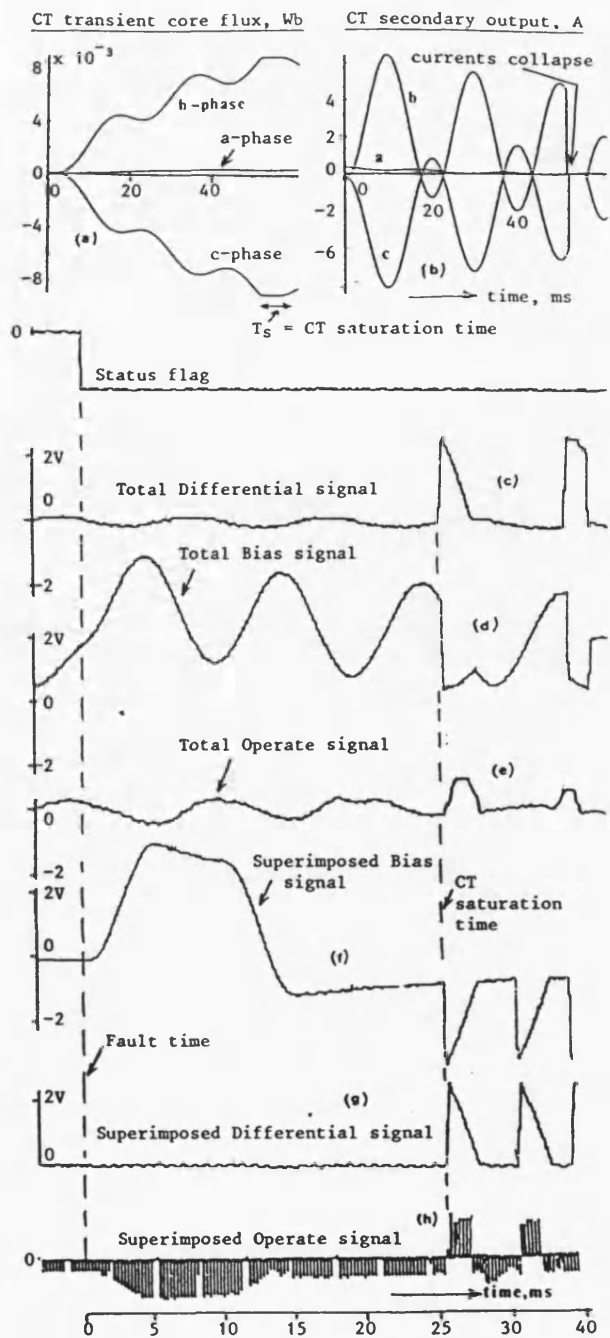
Fig. 10  Effect of CT saturation for an external fault

a,b,c – currents at ends P,Q & R
fault at T-point
d,e,f – currents at ends P,Q & R
fault at 1 km from end P
g,h – Differential currents
i,j – Bias currents
k,l – Operate signals; ———– Fault time

Fig. 9  Effect of feed-around path for an internal fault

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Fig 11. Fault resistance coverage

In the figure:
- voltage maximum a-earth fault at T-point of config. shown in Fig. 6b.
- 1,3 – practical performance
- 2,4 – theoretical performance
- —— total component
- ----- superimposed component

Axes: Relay operating time, ms (vertical, 2–14); Fault resistance, ohms (horizontal, 0–300)

## APPENDIX

### Appendix A

Digital data communications: A sampling rate of 4kHz coupled with a 12 bit A/D conversion, requires a data transmission rate of at least 96k bits/s for the two Aerial mode current signals to be transmitted from each Slave end to the Master end. In practice, this would be achieved over two channels of a standard modem comprising multiplexed PCM data transmission equipment, each with a capability of transmitting 64k bits/s. The remaining 32k bits/s are sufficient for error detection and byte synchronisation.

For the relay described herein, typical trip times of 3–4ms are attained and these would be the decision times at the Master end. However, because of the additional trip signal conversion and transmission times, trip decisions at the two Slave ends would be asserted in typically 5–6ms. It should be mentioned that the relay scheme developed here works equally well at lower sampling rates, except that the response would be slower for the latter. This makes the relay highly flexible and it can be adapted to work with alternative communication channels such as microwave, by minor changes in the interfacing hardware.

### Appendix B

The Karrenbauer transformation: The relay signals are based on decoupling the phase quantities into modal quantities using a transformation matrix Q. There are a number of transformations in use, but the one most suited to this relay, particularly from relay stability point of view for certain types of external faults, is the Karrenbauer transformation given as:

$$
\begin{bmatrix} I_0 \\ I_1 \\ I_2 \end{bmatrix} = 1/3 \begin{bmatrix} 1 & 1 & 1 \\ 1 & 0 & -1 \\ 1 & -1 & 0 \end{bmatrix} \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \qquad (9)
$$

$\longleftarrow Q^{-1} \longrightarrow$

In equ. 9, $I_0$ is the Earth mode of propagation and $I_1$, $I_2$ are the two Aerial modes of propagation. For this relay, the protection algorithm is based only on the two Aerial modes. The use of the Earth mode is avoided as it can cause problems of relay instability on the healthy circuit in parallel line configurations.

## BIOGRAPHY



Raj Aggarwal was born in Kenya. He obtained the degrees of BEng and PhD in Electrical Engineering from the University of Liverpool, England in 1970 and 1973 respectively and joined the Electrical Engineering Department at Bath University soon after graduating. His main areas of research interest are fault transient modelling and development of new protection systems for EHV Power Systems. He is the author and co-author of some 40 papers on these topics.



Ali Husseini was born in Lebanon in 1952. He obtained his Master of Science degree in Electrical and Electromagnetic Engineering from the University College Cardiff, UK in January 1987. He joined the Power Systems protection research team at Bath University in July 1987 and is at present working towards his PhD. His main area of interest is Power System protection, in particular development of microprocessor-based digital relaying for EHV transmission systems.

Miles Redfern – for details see companion paper entitled 'Personal Computer-based System for the Laboratory Evaluation of High Performance Power System Protection Relays' (ref. 5).
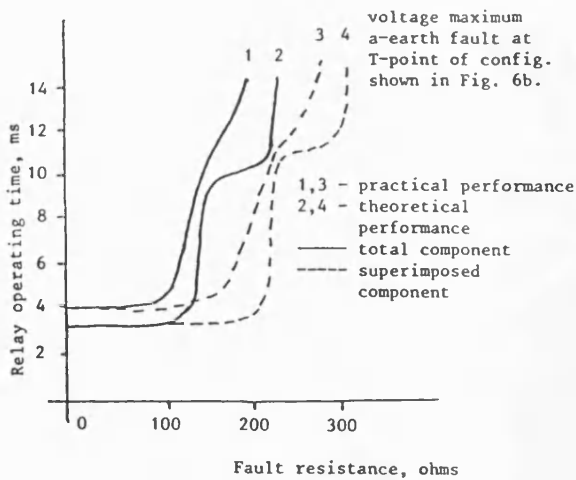
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APPENDIX    D

# A PERSONAL COMPUTER BASED SYSTEM FOR THE LABORATORY EVALUATION OF HIGH PERFORMANCE POWER SYSTEM PROTECTION RELAYS.

M A Redfern, Member IEEE      R K Aggarwal      A H Husseini.

School of Electronic and Electrical Engineering,
University of Bath,
Bath, BA2 7AY, U.K.

Abstract: The power system simulation system described in this paper provides a relay under evaluation with current and voltage inputs similar to those that it would encounter under service and fault conditions. Using digital transient simulation programmes to model power system behaviour, the facility provides an effective bandwidth of from dc to 4 kHz for both the current and voltage relay inputs. The relay's outputs are automatically monitored during the test, enabling a detailed report of its response to be produced. The application of the system is illustrated by the evaluation of a new EHV Teed feeder relaying system.

Keywords: Power systems, Protection relaying, Relay evaluation systems, Power system simulation.

## INTRODUCTION.

The development of high performance protection relays and their application to complex power system configurations has led to the introduction of increasingly more sophisticated systems to evaluate their capabilities. Modern relay evaluation systems are required to provide an accurate simulation of the electrical power system, and must faithfully reproduce the power system frequency currents and voltages, together with the high and low frequency transients caused by faults and system switching.

Several researchers have been working on systems to provide laboratory facilities which simulate power system behaviour for evaluating protection relay performance. These include the Programmable Transmission Line (PTL)[1,2,3], Morgat[4], and the Dyna-Test Simulator[5]. These systems all use off-line modelling, since using the dedicated mini- or micro- computers on which they have been based, it is not possible to execute the established power system transient simulation programmes[4,5,6,7,8] in real-time and provide the outputs at the sample rates required to generate the higher frequency transients needed for evaluating high performance relays. Bornard et al[4] calculated that a one second simulation of a section of an EHV network with a time step of 100 μsec, would require 1580 seconds of CPU time on a VAX 11-750 computer.

The Microcomputer PTL uses an off-line simulator and employs concepts developed from the PTL[1,2,3] to provide current and voltage signals to the relay under

evaluation. A fundamental feature of the approach is that the host computer is not only used for power system simulations and data manipulation, but also directly controls the flow of data to the output D/A converters. This is achieved using a time critical data handling programme which provides 12000 samples/sec on all output channels. The original PTL concept has also been extended to enable the system to operate on a range of widely available, low cost micro-computer systems instead of the specialist minicomputer used previously. This has enabled several new facilities to be included, taking advantage of the powerful data handling features of the family of microprocessor used.

The inherent features of this approach are:-

- both low and high frequency transients are accurately reproduced within the constraints of the digitising bandwidth of the power system simulation and the output amplifiers.

- the relay input currents and voltages can be obtained from any desired point in the power system configuration.

- the power system configuration can be modified to evaluate the performance of the relay under a wide variety of fault and switching conditions.

- the latest refinements in power system simulation can be added when available thus avoiding system obsolescence.

- the system can be used at most power system frequencies. These include the standard 50 Hz and 60 Hz as well as other frequencies used in railway and marine systems.

- the system can be enhanced to use data collected in the field.

The PTL output current and voltage levels required to evaluate the relay's performance, are provided using high fidelity current and voltage power amplifiers. The current amplifiers can provide up to 100 amps (peak), and the voltage amplifiers can provide 140 volts rms.

## RELAY EVALUATION MICROCOMPUTER PTL.

The power system is modelled using off-line simulation programmes which accurately simulate its behaviour under fault and switching conditions. These programmes provide the instantaneous values of the currents and voltages measured at the required relaying points for the period during which the response of the relay is to be evaluated.

The variety of power system configurations which can be modelled for relay evaluation using the microcomputer PTL are limited only by the capabilities of the digital

power system simulator programmes used. The system is not tied to any particular simulation package and can therefore be enhanced as new software becomes available.

The relay evaluation system consists of the desk-top microcomputer together with a specialised interface unit, a precision master control unit, current and voltage amplifiers, and the digital input and output circuits used for interfacing with the control and output relays used in the protection scheme. The specialised interface unit contains the D/A converters and digital input and output ports. A simplified schematic diagram of the system is shown in figure 1.
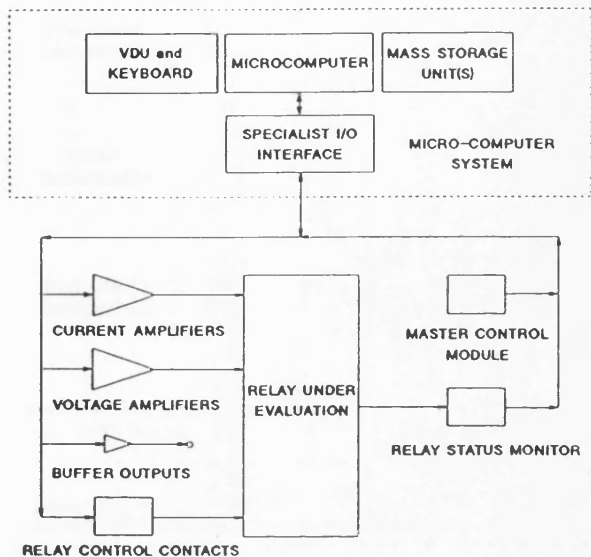


FIGURE 1. THE MICRO-COMPUTER PROGRAMMABLE TRANSMISSION LINE.

For research into new designs of relay comparators or signal processing systems, it is not always appropriate to use the high power outputs from the main amplifiers. Low power buffer amplifiers have therefore been included in the Microcomputer PTL which provide ±10 volt outputs and contain anti-aliasing filters.

The Microcomputer PTL was initially designed to use a 12 MHz, 80286 based IBM-AT compatible micro-computer. This has been recently upgraded to an 80386 based computer, since this enables more sophisticated simulation programmes to be executed on the host computer system.

The laboratory Microcomputer PTL has been configured to provide a combination of three current and three voltage high power outputs making it suitable for the evaluation of a single relaying point transmission line relay, for example a distance relay. The system can be re-configured to provide any combination of six analogue outputs, three of which can be supported with high power current amplifiers and three with voltage amplifiers. The six low power buffer outputs can be used for either current or voltage signal outputs.

Power System Simulation Programmes.

The choice of power system simulation programme depends on the level of sophistication and accuracy required for the particular relay evaluation. For basic testing of protection systems operation, a simple power system simulation may be appropriate. One such programme uses a lumped parameter model of a transmission system and models the sinusoidal and exponentially decaying dc components of the current and voltage waveforms. For more detailed work, the system uses data from the frequency domain simulation programmes developed by Johns and Aggarwal[6] and the now internationally accepted Electromagnetic Transients Programmes (EMTP)[7].

The Johns and Aggarwal[6] simulation programmes are executed on an ICL series 39 level 80 main frame computer and the output data is then transferred to the laboratory micro-computer system using the University network. The Alternative Transients Programme (ATP)[8] version of the EMTP programme is executed on the Microcomputer PTL's desk-top computer. A short conversion file is required when using the EMTP simulation programmes to convert the data to the required format for the data preparation programmes.

In addition to using data obtained for digital simulation, the Microcomputer PTL can use data obtained from digital disturbance recorders to generate the current and voltage waveforms. This enables the facility to be used for post fault investigations into events occurring on the network.

Data Preparation Programmes.

The data preparation programmes convert the data obtained from the simulation programmes into the format required by the data handler. At each sampling instant, the data handler programme uses a data group containing eight 16 bit data words. The first six of these correspond to the analogue signal outputs. The seventh is used to provide electrical contact outputs to the relay under test and to provide gain control for the current amplifiers. The final data word, the control data word, is used for the internal data handling programme control.

The data preparation programme scales the current and voltage data using current transformer and voltage transformer ratios defined by the application. Linear transducers are assumed. The minimum and maximum instantaneous values of the output data are checked against the dynamic range of the D/A converters and the output amplifiers to ensure that signal clipping problems are avoided. For the current outputs an automatic gain switching process is used when the output exceeds 20 Amps (peak). In these cases the signal is further scaled by a factor of ten and the relevant control bit is set in the gain control data word.

The data file produced by this programme is divided into three files corresponding to the pre-fault, the fault, and the post-fault data blocks. The pre-fault and post-fault data blocks contain the instantaneous current and voltage signal values for one cycle period and define the steady state pre-fault and post-fault conditions respectively. The fault data block contains the unique data defining fault incidence, the faulted waveforms and the fault induced transients. This division of the test data is illustrated in figure 2.

When the facility is being used to evaluate relay stability or relatively slow relays, a major consideration in selecting the size of the fault data

2

block is to ensure that it is large enough to cover the time period required to contain all the fault induced transients. It is desirable that these transients will have died away before the end of the fault data block. This ensures that when the post-fault data block is recycled to generate the steady state post-fault conditions, no transients remain in the recycled data which would cause corruptions.

The direct addressing of the Intel 8086 family enables a single data block to occupy 64 Kbytes of memory. With the sampling rate set to 12 kHz and 16 bytes of data used at each sampling instant, one 64 Kbyte data block enables the Microcomputer PTL to provide 0.3413 seconds of continuous, unique output waveforms. The enhanced addressing of the 80386 has not yet been implemented.
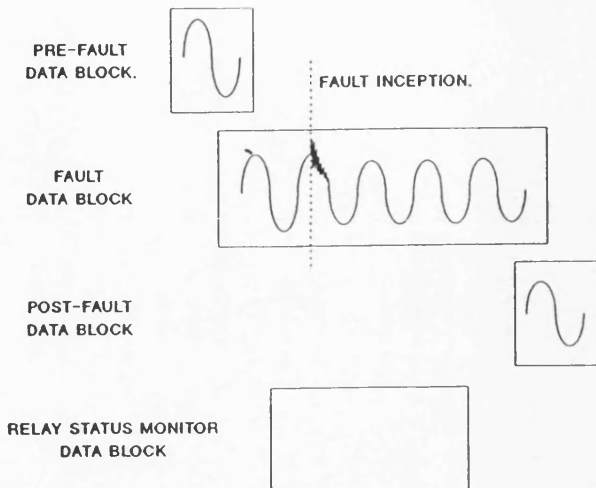


FIGURE 2. TEST DATA BLOCK ORGANISATION.

For fault and switching operations on most power system configurations, the high frequency transients are quickly attenuated. The exponentially decaying dc components, however, persist for a much longer period. For example, considering a system with an X/R ratio of 20, the exponentially decaying dc offset decays to 0.47% of its initial value in the 0.3413 seconds derived from a 64 kByte data block. This attenuation reduces the level of exponentially decaying dc component to within the PTL's working accuracy of ± 1%. If the transients are more persistent, they can be accommodated by modifying the data handler programme to use additional data blocks for the unique fault data period[9] or by reducing the sampling rate.

The data handler programme also adds control data and marker flags to the programme control word. The first programme control word in each data block specifies the number of times the data block is to be recycled under automatic control. Where the contents of the data block are to be used to provide nearly continuous steady state conditions, the recycle number is set to '0'. In the case of blocks containing unique data and which are used only once, the recycle number is set to '1'. Where a specific time limit is required, as for example with high current faults which if applied continuously will damage the relay, the appropriate recycling data is set to the integer number of cycles involved.

The last stage of the data preparation process is to convert the files into a binary format which can be directly loaded into the computer's memory before running the test.

Data Handler Programmes.

The data handler programme uses the information in the data blocks located at specific locations in the computer's memory to directly generate the current and voltage output waveforms, provide control outputs to the power amplifiers and the relay under test, and to monitor the response of the relay to the simulated power system conditions. The programme operates in 'real-time' under the control of the precision master clock, the frequency of which is set to match that of the sampling period used in the original simulation programme. A simplified flow diagram of the data handler programme is shown in figure 3.
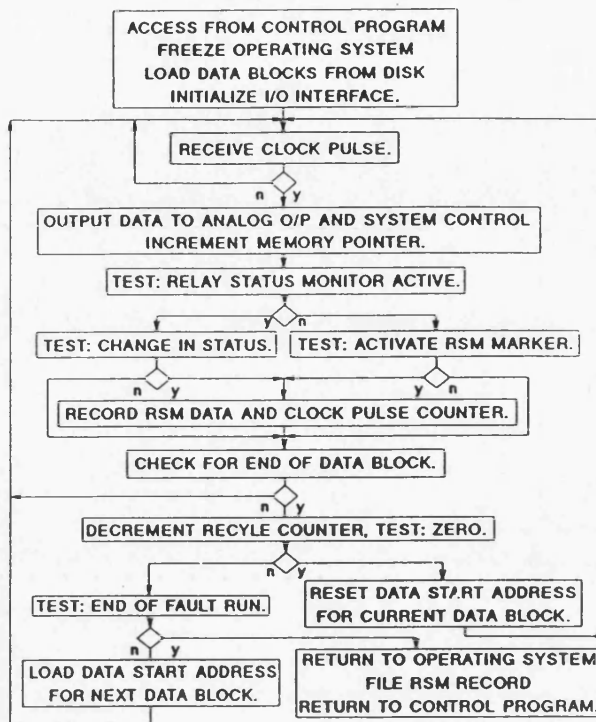


FIGURE 3. DATA HANDLER PROGRAMME.

A unique feature of this approach is that while executing the data handler programme, the computer is dedicated to performing the PTL function and all data transfers are executed directly under programme control. The system does not require large external buffers to provide intermediate storage between the host computer and the D/A converters. Although this makes the data handler programme execution time critical, it maximises system flexibility and minimises the design and construction of system specific hardware. The data handler programme must complete its data transfers and control functions before the next pulse from the master clock, otherwise it produces a glitch in the output waveforms and distortions result.

The master clock frequency can be set to a variety of settings as required by particular test situations. The standard setting is 12 kHz since this provides the most appropriate bandwidth for high speed transmission line relaying. It also provides a convenient basis for operating with power system frequencies of either 50 Hz or 60 Hz, being equivalent to 240 samples per cycle for

50 Hz and 200 samples per cycle at 60 Hz. Other power system frequencies can also be accommodated; for example, 400 Hz marine power systems using 30 samples per cycle, and 25 Hz and 16.67 Hz railway power systems using 480 and 720 samples per cycle respectively.

The data handler programme can be controlled either by using control words in the data blocks which define the number of times the pre-fault and post-fault data blocks are recycled, by a set of operator control buttons, or by the operation of selected output contacts of the relay under evaluation.

A control flag in the programme control word marks the fault incidence and is used to start the relay status monitor (RSM) subroutine. To reduce the amount of data stored by this subroutine, records are only taken at fault incidence, when there is a change to the status of any of the contacts being monitored, and when the clock counter cycles through zero. Each record consists of the current state of the monitored contacts and the contents of a clock counter. This counter is incremented each time a clock pulse is received. The record is stored in the RSM data block as shown in figure 2. At the end of the test this data block is filed to disc for later analysis using a results analysis programme.

## SYSTEM HARDWARE.

### Micro-computer System.

When executing the data handler programme, the system uses its computer system as a programmable mass data storage handler between the power system simulation programme and the real-time environment of the relay under evaluation. It is essential therefore that the computer system is capable of providing adequate random access memory for the data required to define the current and voltage waveforms for the test's duration, and it can execute the programme control functions and output the data to the D/A converters at the required rate. Several machines were rejected before the 12 MHz 80286 based micro-computer was examined and found to provide the required data handling capabilities. This type of computer also provides a convenient man-machine interface and the facilities required to handle the file management functions.

Basing the system on the IBM-AT standard computer provided access to a wide selection of third party interface systems, co-processor systems and software. This simplified the development of the base system and facilitates future development. Also, with the recent availability of the ATP version of the EMTP simulation package, the Microcomputer PTL's processor is used to support powerful transient simulation programmes.

The specialised interface unit is a third party interface card mounted in the micro-computer and contains six 12 bit D/A converters together with 32 bits of digital I/O. The D/A converter outputs can be strobed simultaneously and provide an output voltage within the range of ± 10 volts with a settling time of 3 μsec. For this application, 16 bits of the digital I/O interface have been programmed as outputs to provide contact inputs to the relay and the PTL control systems, and 16 bits have been programmed as inputs for the relay status monitor and operator control.

### Current Amplifiers.

The current amplifiers were designed to provide high fidelity output currents capable of testing most modern static protection relays. Although the amplifiers and the system were designed to provide 200 Amps peak, with the limitations of dc power supply used, they are able to provide 60 Amps rms and 100 Amps peak. The output bandwidth is limited to dc to 4 kHz with fourth order Butterworth low pass filters. The three amplifiers are connected in star to give Ia, Ib, Ic and In.

The amplifiers use a linear design and are directly coupled throughout. With a dc supply of -36v 0v +36v, the output voltage swing is up to ± 32 volts. Although this has not caused difficulties for the evaluation of a wide range of modern static relays, it does limit the system's capabilities for evaluating relays with high current burdens or for evaluating a scheme of several relays connected in series. When using high current tests with such relays, output voltage clipping can occur and results in a saturation type effect. Similar effects can also result when evaluating relays with non-linear current input circuits. Possible problems with relays which have highly inductive current inputs are minimised by having a high open loop bandwidth.

The accuracy of the current amplifiers is enhanced by using a gain switching facility. In the normal setting, a ± 10 volt input provides an output of ± 20 amps. For high current tests, the gain of the amplifier is increased by a factor of ten. This feature is controlled by the data handling programme using a dedicated output bit in the programme control data word for each current amplifier.

### Voltage Amplifiers.

The voltage amplifiers are of a similar design to the current amplifiers but rated at 100 VA and use an output transformer to provide an output voltage swing of ± 200 volts. This provides for a nominal output voltage of 63.5 volts rms, a voltage factor of 1.9 and a suitable margin for fault induced transients. Since the transformer outputs are floating, they can also be connected phase to phase providing a nominal output of 110 volts. The frequency bandwidth is limited to 0.1 Hz to 4 kHz by fourth order Butterworth low pass filters.

### Low Level Buffered Outputs.

The low level buffered outputs provide unity gain outputs with fourth order Butterworth, low pass anti-aliasing filters to give an output bandwidth of dc to 4 kHz. These filters remove the digitising and sampling effects from the output waveforms, which is particularly important when investigating the capabilities of high sampling rate, digital processing relays. The output voltage can vary between ± 10 volts.

### Relay Status Monitor (RSM).

The relay status monitor provides the interface between the computer and the PTL control systems, the auxiliary inputs to and the outputs from the relay under evaluation. Digital outputs from the PTL are buffered using high speed reed relays with suitable drive circuits. The monitored relay outputs and the operator control buttons are interfaced to the digital input port using opto-isolators.

## GENERAL APPLICATIONS.

The application of the microcomputer PTL to testing high performance transmission line relaying is illustrated using the tapped EHV feeder shown in figure 4. This 400 kV system connects the three power systems P, R and Q, represented by their source capacity. The plain feeder connecting P and Q represents a parallel interconnection between the two systems.

The waveforms in figure 5 show the a-phase currents and

voltages measured at the local end relaying point (P) for an a-phase to earth fault at the centre point, $F_1$, of the tapped feeder. The fault considered in figure 5(a) is applied at the a-phase voltage maximum; i.e. at 90 degrees point on the voltage waveform. Figure 5(a.i) shows the waveforms obtained plotting the results from the simulation programme and figure 5(a.ii) shows the output waveforms monitored on the PTL's a-phase current and voltage outputs. Figure 5(b) shows the corresponding waveforms for a fault applied at a voltage zero; i.e. at zero degrees point on the voltage waveform. The comparison of these waveforms illustrates the system's ability to provide a faithful reproduction of the computed waveform including both high and low frequency transients.



Primary Voltage Va.          Primary Current Ia.

(a.i) COMPUTER SIMULATION WAVEFORMS.



(a.ii) PTL OUTPUT WAVEFORMS.



**FIGURE 4. EHV TEED FEEDER NETWORK USED FOR RELAY EVALUATION.**

Linear primary CTs and VTs have been used in these examples. When required, non-linear transducer characteristics can be included in the simulation programme and further work is in progress to provide a hardware simulation of the primary transducers. The hardware transducer simulation will accommodate load dependant characteristics.

TEED FEEDER DIFFERENTIAL PROTECTION EVALUATION.

The teed feeder protection[10] has been designed to provide high speed protection for multi-terminal EHV transmission lines using current differential techniques. The hardware implementation of the protection scheme's comparator is described in a companion paper[11].
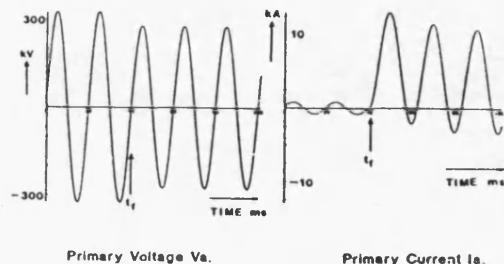
A simplified representation of the teed feeder protection scheme as applied to a three terminal line is shown in figure 6(a). The scheme consists of a master relaying unit and two slave units. The master unit contains current input circuits, a fibre optic communication system, a trip output device and the protection scheme's differential comparator. The slave units pre-condition their local input current signals, transmit the digitised values to the master unit, and on receipt of a trip command, provide the local trip output. The slave units operate as remote terminal units to the master unit, in which the protection decision making is performed.
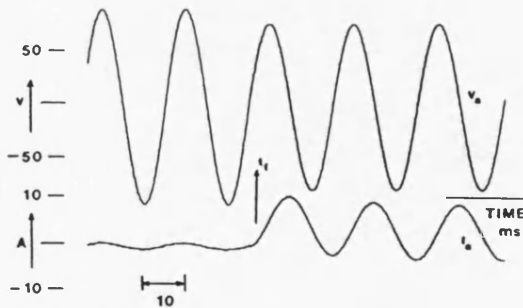


Primary Voltage Va.          Primary Current Ia.
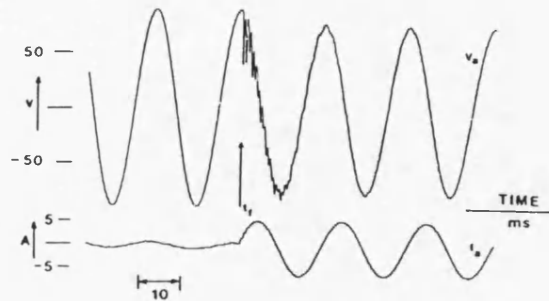
(b.i) COMPUTER SIMULATION WAVEFORMS.



(b.ii) PTL OUTPUT WAVEFORMS.

(a) Point on wave 90 degs.    (b) Point on wave 0 d

FIGURE 5. PHASE TO EARTH FAULT TEST WAVEFOF

To evaluate the differential comparator, the scheme's decision making performance was of particular interest. It was not necessary to build the full protection scheme and the system was reconfigured as shown in figure 6(b). The primary system model of the three terminal transmission line and associated generation was extended to include the current transformers, the relay's current interface modules, the relay's mixing circuits used to derive the aerial mode currents from the phase quantities, and the communications systems. The nine phase current inputs to the scheme were therefore reduced to six aerial mode currents. This simulation used idealised primary CTs and current interface modules as described in a companion paper[11]. Appropriate time delays were added to the current signals obtained from the remote terminals to represent delays introduced by the communication systems.
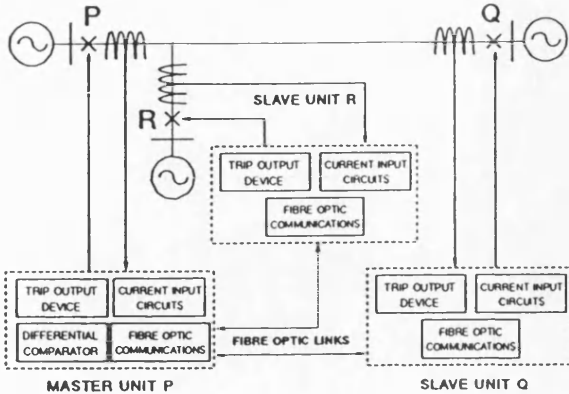


(a). SINGLE LINE REPRESENTATION OF TEED FEEDER PROTECTION.
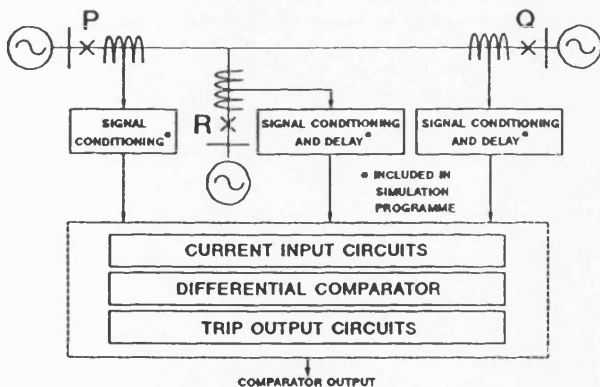


(b). SINGLE LINE REPRESENTATION OF TEED FEEDER PROTECTION USED FOR COMPARATOR EVALUATION.

FIGURE 6. EHV TEED FEEDER PROTECTION SCHEME.

Several power system configurations were used for the evaluation including the 400 kV teed feeder system shown in figure 4. The relay was subjected to fault conditions representing short circuit faults at a variety of points on the teed feeder, including both in zone and out of zone faults at the terminal points.

The test waveforms for an internal fault at the centre point of the teed feeder, $F_1$ in figure 4, together with the relay's output response are shown in figure 7. For this a-phase to earth fault at 80 degrees point on the voltage wave, the differential comparator's trip

command was given 3.2 msecs after fault incidence. Ideal communications were assumed in this test and data transfer delays were set to zero. The curves show the two aerial mode currents measured at each terminal of the teed circuit as provided by the PTL's buffered outputs.

The test waveforms for an external fault are shown in figure 8. In this example, the fault is on the parallel plane feeder, 40 km from terminal P as shown by fault point $F_2$ in figure 4. The waveforms are in the same combination as in figure 7. For this fault, the contents of the trip register are forced to the restrain level after each sampling interval and the relay does not operate.

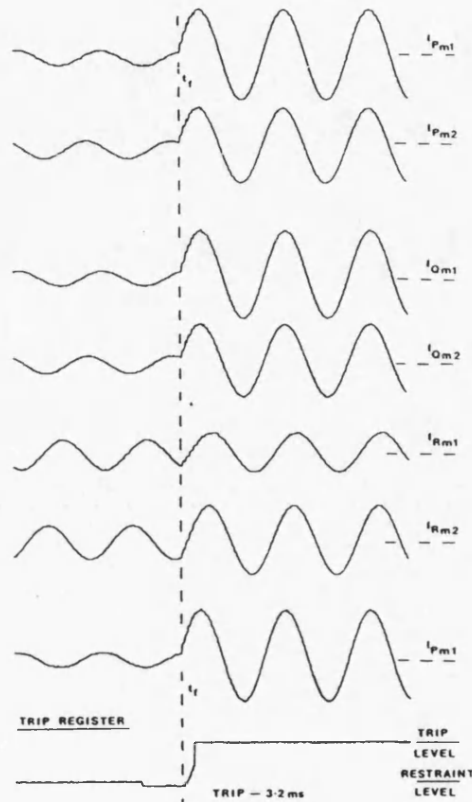The evaluation of the EHV Teed Feeder protection is presented in the companion paper[11].



FIGURE 7. PTL MODAL CURRENT WAVEFORMS AND TEED FEEDER COMPARATOR OUTPUT FOR AN IN ZONE FAULT.

CONCLUSIONS.

The Microcomputer PTL provides a powerful laboratory facility for evaluating a wide range of protection systems. The ability to model a large variety of power system configurations and phenomena using off-line simulations, enable the facility for developing new relay designs and their certification. The system can also be used to investigate unexplained protection operations either by modelling the fault conditions or by using data from digital fault recorders. '

The facility provides current and voltage signals corresponding to those experienced under actual service

conditions and hence reduces the need to test protection relay systems in the field.

The use of the IBM–AT family of microcomputers for the host computer, enables the system to be used to execute powerful transient simulation packages as well as the wealth of compatible proprietary software available. The facility quickly becomes the focus for research into power system protection relaying.
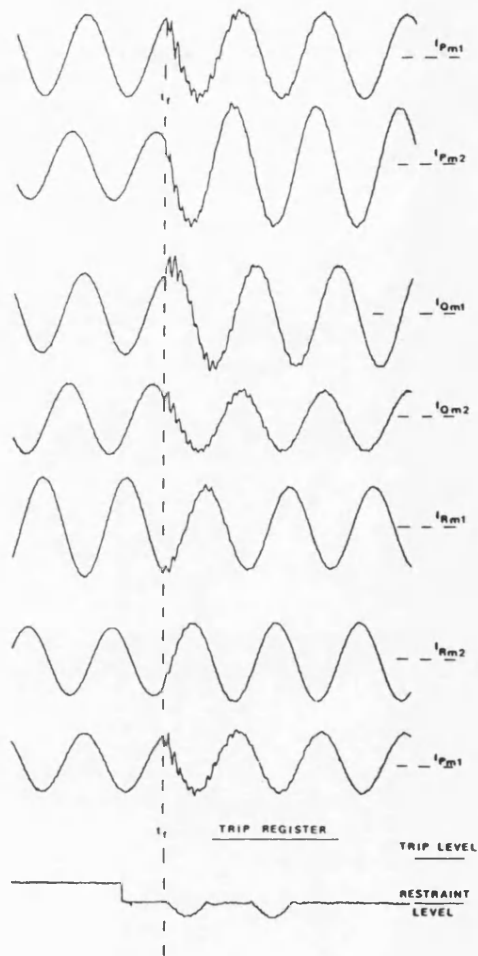


FIGURE 8. PTL MODAL CURRENT WAVEFORMS AND TEED FEEDER COMPARATOR OUTPUT FOR AN OUT OF ZONE FAULT.

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Miles A Redfern (M'79) was born in Kelowna BC Canada on December 25, 1948. He received the BSc degree in Electrical Engineering from Nottingham University UK, and the PhD degree from Cambridge University in 1970 and 1976 respectively.

From 1970 to 1972 was employed by British Railways Research, Derby, in the Machines Research Section. In 1975 he joined GEC Measurements, Stafford and held various positions including Head of Applied Research and Long Term Development (77-80) and Overseas Sales Manager (82-86). In 1975 he started research into power system simulation for relay evaluation and in 1977 commissioned the first Programmable Transmission Line. His research in this field is continuing.

In 1986 he joined the University of Bath with research and teaching interests in Electrical Power Systems, Protection, Simulation and Engineering Management. He is involved with several co-operative research projects with industry.

Raj K Aggarwal and, Ali H Husseini - for details see companion paper: 'Design and Testing of a New Microprocessor Based Teed Feeder Protection for EHV systems.' (reference 11).