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**PHD**

**Modelling, fabrication and development of GaN-based sensors and substrates for high strain environments**

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# **Modelling, fabrication and development of GaN-based sensors and substrates for high strain environments**

**Submitted by Michael John Edwards**

For the degree of PhD  
At the University of Bath  
Department of Mechanical Engineering  
2012

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## ABSTRACT

GaN is a monocrystalline material that can be grown using metallo-organic chemical vapour deposition (MOCVD), and has desirable mechanical and semiconducting properties for operating as a sensor. It has a Young's modulus of 250 to 350 GPa, which shows little decrease with respect to temperature beyond 400°C. GaN also exhibits piezoelectric and piezoresistive effects, meaning that it will generate a charge and its electrical resistance will change when the material is strained respectively. In this PhD, GaN has been used as the base material for pressure sensors that potentially can be used in excess of 400°C and at a pressure in excess of 50 bar (5 MPa), with potential applications in aerospace and oil exploration. The pressure sensor is a circular diaphragm created from a GaN/sapphire wafer, and was designed and tested in order to determine if GaN can act as a sensing material in these environments.

In addition to the diaphragm sensor, GaN templates that can potentially be used for sensors were grown using an epitaxial layer overgrowth (ELOG) method. These sensors are potentially more mechanically robust than similar templates etched out of GaN/sapphire wafers because they will have less inbuilt strain due to lower dislocation densities. It was possible to release beams and cantilevers from GaN ELOG templates. Mechanical probe tests were undertaken on these devices to see if they were fully released and robust.

GaN single crystal growth requires a substrate material, such as (111) silicon or (0001) sapphire, meaning that the thermal properties of the substrate are important for a device operating in excess of 400°C. GaN high electron mobility transistors are heat sensitive, experiencing a decrease in current between the drain and source terminals as the temperature increases. Therefore a GaN-based sensor needs a substrate with the highest possible thermal conductivity to act as a heat sink, which means removing as much heat as possible from the GaN sensor. Diamond has superior thermal conductivity to both sapphire and silicon, so a novel silicon/polycrystalline diamond composite substrate has been developed as a potential GaN substrate. Polycrystalline diamond (PD) can be grown on 4 inch diameter wafers using hot filament chemical vapour deposition (CVD), on (111) silicon (Si) from which single crystal GaN epitaxy can also be grown.

In order for the (111) Si/PD composite substrates to be useful heat sinks, the Si layer needs to be less than 2 µm. PD was initially grown on 525 to 625 µm thick Si wafers that required thinning to 2 µm. Achieving this Si layer thickness is difficult due to the presence of tensile stress in the Si caused by a mismatch in the coefficients of thermal expansion (CTEs) between Si and PD. This stress causes the wafer to bow significantly and has been modelled using ANSYS FE software. The models show that the bow of the wafer increases when it is thinned, which will eventually cause the Si layer to delaminate at the Si/PD interface due to poor adhesion and a build up for shear stress. When the Si layer is mechanically thinned, the Si layer can crack due to clamping. The experimental wafer bow and micro-Raman measurements validate the model for when the silicon layer is thicker than 100 µm and these results show that an alternative processing route is required.



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## NOMENCLATURE.

Symbol	Definition	SI unit
$a, c$	Lattice constants	m
$b$	Bow	m
$C$	Capacitance	F
$c$	Uniform strain component	-
$c_{ij}$	Stiffness coefficients	Pa
$c_T$	Temperature coefficient	$K^{-1}$
$d$	Diameter	m
$D$	Electronic displacement	$C\ m^{-2}$
$E$	Stiffness	Pa
$\varepsilon$	Strain	-
$\varepsilon_0$	Permittivity of free space	$F\ m^{-1}$
$\varepsilon_i$	Permittivity	$F\ m^{-1}$



$e_{ij}$	Piezoelectric stress coefficients	$C\ m^{-1}$
$E_{RT}$	Room temperature stiffness	Pa
$G$	Shear modulus	Pa
$I$	Current	A
$I_{DS}$	Drain-source current	A
$I_{DSat}$	Drain-source saturation current	A
$I_{GS}$	Gate-source current	A
$\kappa$	Gauge factor	-
$M$	Peeling moment	$N\ m^2$
$\nu$	Poisson's ratio	-
$R$	Resistance	$\Omega$
$r$	Radius of curvature	$m^{-1}$
$\sigma, S$	Stress	Pa
$s_{ij}$	Compliance coefficients	$Pa^{-1}$

$T$	Temperature	K
$t_b$	Bending axis	m
$t_f$	Film thickness	m
$t_s$	Substrate thickness	m
$V$	Voltage	V
$V_{DS}$	Drain-source Voltage	V
$V_{DSat}$	Drain-source saturation voltage	V
$V_{GS}$	Gate-source voltage	V
$\alpha, \alpha_a, \alpha_c$	Coefficient of thermal expansion	K <sup>-1</sup>

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## LIST OF DEFINITIONS.

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<b>Name</b>	<b>Definition</b>
BIPEC	Backside illuminated photo electrochemical etch
CE	Cantilever epitaxy
CTE	Coefficient of thermal expansion
DMTA	Dynamic mechanical thermal analysis
EBL	Electron beam lithography
ELOG, ELO, LEO	Epitaxial layer overgrowth
FET	Field effect transistor
FE	Finite element
FIB	Focussed ion beam
HEMT	High electron mobility transistor
ICP	Inductively coupled plasma
IPA	Iso-propanol
LED	Light emitting diode

MORGaN	Materials for robust GaN
MIS	metal-insulator-semiconductor
MOCVD	Metallo-organic chemical vapour deposition
MOVPE	Metallo-organic vapour-phase epitaxy
MEMS	Micro-electromechanical systems
NPE	Nano-pendeo epitaxy
PECVD	Plasma-enhanced chemical vapour deposition
PD	Polycrystalline CVD diamond
PEB	Post exposure bake
PLOG	Pulsed epitaxial layer overgrowth
RIE	Reactive ion etching
SEM	Scanning electron microscopy
SFB	Silicon fusion bonding
SIMOX	Silicon implantation of oxide
SOI	Silicon-on-insulator

TD	Threading dislocation
III-V	Three-five semiconductor
TMA	Tri-methyl aluminium
TMG	Tri-methyl gallium
TMI	Tri-methyl indium
2DEG	Two-dimensional electron gas
UV	Ultra-violet

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## CHAPTER 1: MOTIVATION AND LITERATURE REVIEW

### 1.1 Introduction and Motivation

#### 1.1.1 Introduction

The work to be undertaken as part of this PhD will be based on the design and fabrication of Gallium nitride (GaN)-based cantilever and membrane devices that can be used as a sensor at temperatures in excess of 300°C. The devices can potentially be used in areas such as space exploration [1], where present electronic devices degrade when exposed to extreme changes in temperature and large doses of radiation [1]. GaN-based sensors will suffer less mechanical degradation and can be used to measure pressure in extreme conditions [1].

GaN is an ideal material for a sensor in harsh environments since it is a robust material that is stable at temperatures up to 1000°C, has a wide band-gap of 3.6 eV [2] and a Young's modulus of ~288 GPa at room temperature [3]. Both cantilevers and membranes can based on GaN be used as strain gauges that respond to changes of pressure, temperature (see chapter 7) and stress. GaN is piezoelectric, which means that the material produces a charge when a strain is applied (the 'direct' piezoelectric effect) and an applied bias will result in the development of a strain in the material (the 'converse' piezoelectric effect) [4]. It is the piezoelectric properties of GaN that will allow strain on the device to be measured using either a metal-insulator-semiconductor (MIS) capacitor [4] or a high electron mobility transistor (HEMT) [2].

When a HEMT device is operating at high power, there are self-heating effects and this causes the electrical performance of the device to degrade [5]. This effect will also occur when a sensor is operating in high ambient temperatures. The most commonly used substrates for GaN growth are (111) silicon and sapphire, which are both relatively poor thermal conductors. The resulting heat gets trapped in the GaN surface, which reduces the channel conductivity and impairs the performance of the device (see chapter 7). GaN is now routinely grown on SiC substrates [6, 7], but these are very expensive (~\$760 for a 3 inch substrate in 2010 [8]) and have a thermal conductivity of  $387 \text{ Wm}^{-1}\text{K}^{-1}$  at room temperature [9], which although reasonable is

lower than that of diamond. The material with the highest thermal conductivity is diamond ( $4000 \text{ W m}^{-1}\text{K}^{-1}$  at  $20^\circ\text{C}$  [10]), which can be produced straightforwardly using a chemical vapour deposition (CVD) process [11-13] and will be less expensive to produce than SiC.

A (111) silicon (Si) / polycrystalline diamond (PD) composite substrate has been proposed as part of the Framework 7 (FP7) MORGaN (**M**aterials for **R**obust **G**allium **N**itride) project [14, 15] and such a composite substrate has the potential to combine the high thermal conductivity of diamond with the epitaxial compatibility of GaN and (111) Si. We will see in the thesis that this composite substrate will consist of a  $\sim 2 \mu\text{m}$  layer of Si and a  $\sim 50$  to  $100 \mu\text{m}$  layer of PD. The PD will be synthesised on a bulk (111) Si wafer with a thickness of  $\sim 525 \mu\text{m}$  and the Si will be subsequently lapped down to the desired thickness. However, due to thermal mismatch effects, the wafer becomes highly bowed and stressed during the lapping process. These issues and potential methods for creating a viable composite substrate are discussed in chapters 3 and 4.

### ***1.1.2 Motivation***

This project concerns the effect of stress on GaN structures and their piezoelectric response in order to create a pressure sensor using either a field effect transistor (FET) or a high electron mobility transistor (HEMT) as a transducer. GaN and related III-V nitride materials, such as AlN and InN, are piezoelectric and semiconducting, hence suitable materials for creating strain sensors. GaN research is a large and varied research area, as discussed later in sections 1.2 to 1.5, meaning that this project can only concentrate on a few specific areas. These areas are the mechanical and piezoelectric behaviour of GaN and related substrate materials (Si, sapphire and PD are used as substrates in this project) when placed under mechanical and thermal stress. Additionally some knowledge of the workings of a GaN high electron mobility transistor (HEMT) is also needed so that they can be effectively utilised as sensing elements.

GaN also has a monocrystalline structure, rather than consisting of randomly orientated domains like PZT (lead zirconate titanate), which means that it does not require poling and this is an advantage for a strain sensor that potentially operates in environments that are difficult to access, such as in an oil well, jet engine or on a satellite. Theoretically [3] the elastic modulus of GaN shows little decrease with respect to temperature when heated to 625°C, meaning that GaN is potential sensing base material in what are defined in this project as ‘harsh environments’. For the purpose of this thesis a ‘harsh environment’ is defined as an environment where the ambient temperature exceeds 300°C and the pressure is in the range of 10 to 60 bar. The sensors designed and discussed in this thesis are intended for eventual use in these kind of environments

The objectives of this project are:

- Provide accurate finite element (FE) models using ANSYS that can be used to predict the behaviour of silicon/polycrystalline diamond (PD) composite substrates. These models will provide the MORGaN processing team with data that can be used to help overcome technical issues with these substrates.
- Have the Young’s modulus of GaN measured up to the highest available temperature to verify that GaN maintains structural integrity. This will be done in this project using dynamic mechanical thermal analysis (DMTA) and the GaN samples will be sent to an external company for impulse excitation analysis to verify the DMTA measurements.
- Model, design and test, in conjunction with other MORGaN project partners, a GaN HEMT diaphragm sensor that has the potential to be used in harsh environments, verify that the sensor is sufficiently strain sensitive and follows trend behaviour predicted by the FE model. ANSYS will be used to provide predictions of the stress distribution and piezo-electric response of the sensor. This information will then be used to determine the position of the HEMT sensing elements at the design phase and the sensor testing will determine the accuracy of the model.



- Design templates that can be used by the in-house metallo-organic vapour phase epitaxy (MOVPE) expert to laterally overgrow GaN material, using an epitaxial lateral overgrowth (ELOG) method, which can be potentially used as a sensor beyond this project. After MOVPE growth, there will be an attempt to release the laterally overgrown material from the designed template using nanofabrication methods: creating free-standing structures that can be converted into strain sensors in the future.

### *1.1.2 Thesis Structure*

This thesis concerns the work undertaken developing novel substrates that are compatible with GaN growth and the development of new GaN-based pressure sensors for extreme environments. The work was undertaken as part of the MORGaN (**M**aterials for **R**obust **G**allium Nitride) project, which funded this PhD. The thesis consists of eight chapters, with the concluding chapter discussing future work and appendices at the end.

Chapter 1 consists of a literature review that shows the motivation of this project and the current state of the art of GaN sensing and substrate technology. The relative merits of current substrates and other examples of GaN sensors will be discussed. The shortcomings of the current technology in the literature will be determined and there will be an outline of how this thesis will improve on the current state of the art. The stiffness and piezoelectric coefficients of GaN and the substrate materials used in this project will be discussed and derived from first principles; these are very important quantities when modelling new substrates and sensors. There will also be a discussion of how some these properties will be measured experimentally as part of this project.

Chapter 2 is an additional review chapter that concerns the experimental techniques used in this project. Although there is a significant amount of modelling in this PhD, it is speculative unless it receives some validation. This chapter describes the methodology of the experimental techniques that have been used to validate the model. The details of how wafer bow, layer thicknesses and strains in a wafer are measured will be described in this chapter. Furthermore, the measurement of the

stiffness of GaN, Si and sapphire at high temperature are discussed. Understanding how these materials behave at high temperatures is of high importance to this project and the design of extreme sensing devices. Finally, the nanofabrication techniques used to develop GaN sensors will also be discussed.

The development of a Si/PD composite substrate wafer will be the overriding topic of chapters 3 and 4. The potential of this substrate technology is high and is a key output of the MORGaN project. However there are many issues to overcome, such as delamination, cracking and excessive bow caused by thermal mismatch. Chapter 3 will consider the validation of the finite element (FE) model developed to examine this problem and the issues caused by the mismatch of the coefficients of thermal expansion (CTEs). Chapter 4 will discuss various methods for overcoming issues caused by CTE mismatch and diamond synthesis will be discussed, and the merits of these methods will be determined. The main method for overcoming Si/PD processing issues was to use silicon-on-insulator (SOI) wafers and this work will be discussed in detail in chapter 4. Potential solutions to these methods will also be discussed, as well as the viability of this technology.

The high temperature measurements of Si, GaN and sapphire will be discussed in chapter 5. These measurements were undertaken using dynamic mechanical thermal analysis (DMTA), which can measure the stiffness of a material up to 500°C, and impulse excitation at IMCE, which can measure the stiffness up to 1000°C. The stiffness of Si at high temperature is well-known in the literature and this data will be used to discuss the validity of using DMTA for these measurements. The stiffness of sapphire was then measured and there is a discussion of the results. Free-standing GaN wafers were laser cut, so that precise test pieces could be formed and the error in geometry was minimised. Understanding how GaN, Si and sapphire behave at high temperature is a requirement for extreme sensing.

Chapter 6 details the progress in the production of a small GaN strain sensor templates fashioned from Epitaxial Layer Overgrowth (ELO or ELOG) material. ELOG material has a very low dislocation density, and therefore has superior electrical and mechanical properties [16]. This chapter will describe the design process, with fabricated photoelectric masks and any issues that manifested themselves during this stage. The process was iterative and multiple types of ELOG

device were trialled, the merits of each type of device will be determined. The ELOG fabrication process will be discussed in detail, along with any associated technical issues.

Chapter 7 will describe the development of a GaN membrane pressure sensor known as the “drumskin” in the MORGaN project. This chapter begins by discussing the initial FE modelling of the concept, followed by the design of the sensor. The relative merits of all three different types of drumskin that were considered will be discussed. An experimental test rig for this sensor was then designed and built at Bath. The drumskin testing methodology will be outlined and the results will be discussed in detail. Finally, there will be a discussion of future possible improvements to this sensor.

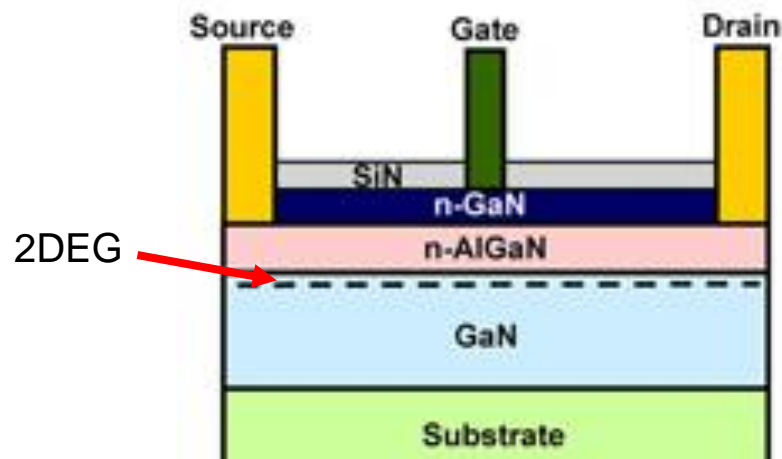
The final chapter of the thesis will discuss concluding remarks. In these remarks the key results and novelty of the thesis will be outlined. There will be a discussion of potential future work that can result from this project. The thesis will then provide appendices and publications that have resulted from this PhD project after the main body of work. A review of the current state of GaN sensing technology will now be discussed.

## **1.2 Applications of GaN**

The traditional use for GaN in the semiconductor industry is for blue-light emitting diodes (LEDs) for solid state lighting [17-19]. These LEDs emit light at a shorter wavelength than traditional red LEDs, increasing the memory capacity of a disk; these are used to read blu-ray disks [19]. This application is not important to this project because in order to make good-quality high-temperature strain gauges, the understanding of the thermal, physical and structural properties of GaN is more important. The strain gauge application has more in common with another common use for GaN, field-effect transistors (FETs) and high electron mobility transistors (HEMTs) in particular [6, 20].

A HEMT is also known as a heterojunction FET, where a heterojunction is the interface between two different solid-state materials. A HEMT works because at the

heterojunction, a 2D electron gas (2DEG) forms and this gives HEMTs high electron mobility. In the growth and fabrication of a GaN device, HEMTs are typically made by depositing a metallic alloy layer, such as AlGaN, on top of a GaN layer. A diagram of a generic GaN/AlGaN HEMT from [21] is shown in figure 1.1.



**Figure 1.1** Schematic of a GaN / AlGaN HEMT [21].

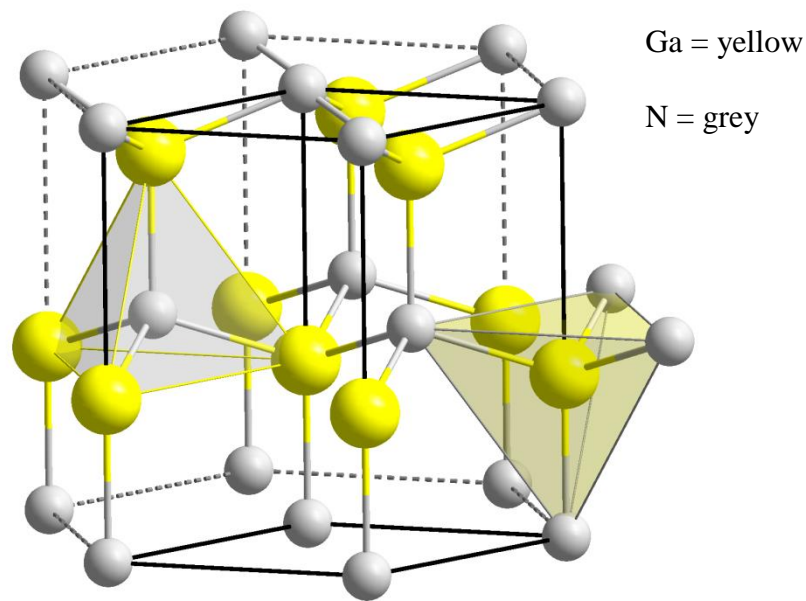
A GaN-based HEMT generally looks similar to the HEMT in figure 1.1, although a InAlN layer is sometimes used in place of AlGaN due to the fact it is lattice matched with GaN [22]. A HEMT has been proposed [23] as a potential sensor for measuring the piezoelectric and piezoresistive response to changes in stress applied to a MEMS GaN cantilever. The addition of the AlGaN layer also has the effect of lowering the potential barrier of GaN, improving the semiconducting properties of the device and simplifying the process of fabricating contacts. The background theory of HEMTs will be briefly discussed in section 1.5. GaN is piezoelectric and piezoresistive, hence it is a potential material for sensing applications. The following section will discuss the piezoelectric and piezoresistive properties of GaN.

## **1.3 Introduction to Piezoelectricity and Piezoresistivity**

### ***1.3.1 Piezoelectricity***

A piezoelectric material exhibits time-varying dipole moments and voltages when subjected to time-varying mechanical stress [24]. Piezoelectric materials tend to be single crystalline or ceramic, with unsymmetrical crystal lattices and an even distribution of positive and negative charges. There are two types of piezoelectric effects the direct piezoelectric effect, where a strain applied to the material causes a potential, and the converse piezoelectric effect, where a potential causes mechanical strain in the material. GaN demonstrates both the direct and converse piezoelectric effect [4, 25].

GaN is a binary compound in a wurtzite crystal structure, where wurtzite is a hexagonal crystal lattice system. Wurtzite crystals generally exhibit the piezoelectric effect [26] and GaN is no exception. Other examples of materials with a wurtzite crystal structure include other nitrides, such as Aluminium Nitride (AlN), Boron Nitride (BN) and Indium Nitride (InN), and sulphides such as CdS and ZnS [2]. The elements in a wurtzite lattice are bonded ionically and arranged in the lattice shown in figure 1.2.



**Figure 1.2** Schematic of the Wurtzite Crystal Structure [27].

A piezoelectric material consists of numerous charges in a crystalline structure, with the positive and negative charges distributed throughout the crystal. In monocrystalline GaN all of the dipoles are naturally orientated in the same direction, unlike a ferroelectric material (such as lead zirconia titanate (PZT)) that consists of randomly orientated domains, and this means that GaN has the advantage of not requiring an external bias, a process known as ‘poling’. Ferroelectric materials consist of randomly orientated piezoelectric domains that typically cancel each other out and require an external bias to align the domains in the same direction, making the material practical to use for piezoelectric applications.

When a piezoelectric material is placed under compressive strain, the dipoles are deformed, disturbing the charge symmetry, and this causes an electric charge separation across the crystal lattice. This charge separation causes an electric potential in response to the applied strain. In all piezoelectric materials, the piezoelectric effect is anisotropic in nature and its coefficients vary according to the direction along the crystal plane. Therefore, the piezoelectric strain and stiffness matrix coefficients need to be known for the purposes of modelling; this will be discussed in section 1.6.

### 1.3.2 Piezoresistivity

As well as having piezoelectric properties, GaN also exhibits a small piezoresistive effect [28, 29]. The piezoresistive effect is a change in resistance due to the application of a mechanical stress to a material. Unlike the piezoelectric effect, the piezoresistive effect only changes the electrical resistance of the material and does not produce a potential. This basically means that the piezoresistive effect refers to a small perturbation in current with respect to a constant voltage when a mechanical stress is applied to the sensor. The piezoresistor is the most common piezoresistive device and is used for measuring strain in mechanical devices [29, 30]. One of the aims of this project is to design, build and characterise a microelectro-mechanical system (MEMS) device that uses the piezoelectric and/or piezoresistive properties of GaN to measure stress/strain changes in harsh environments.

The sensitivity to piezoresistivity and piezoelectricity in a device is defined by its gauge factor  $\kappa$  [30].

$$\kappa = \frac{dR/R}{\varepsilon} \quad (1.1)$$

Where  $dR$  is the change in resistance due to mechanical deformation,  $R$  is the initial resistance, and  $\varepsilon$  is the strain. An alternative to Equation (1.1) is to calculate the gauge factor using the applied strain and changes in capacitance [30]:

$$\kappa = \frac{\Delta C/C}{S_1} \quad (1.2)$$

Where  $C$  is the initial capacitance at zero strain,  $\Delta C$  is the change in capacitance, and  $S_1$  is the applied strain [30]. The gauge factor is also a measure of the sensitivity of a device.

### ***1.3.3 Piezoelectric and piezoresistive measurements in the literature.***

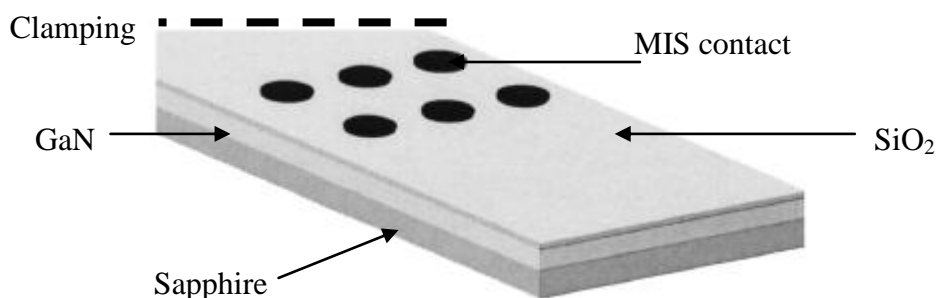
The piezoelectric and piezoresistive properties of GaN are difficult to measure because the charges dissipate over time after a static strain is applied [28]. It only takes approximately a second for most of the piezoelectric charges in GaN generated from an applied strain to dissipate [28] since the material is a semiconductor; the charges are eventually neutralised by free-carriers in the material and background extrinsic charges [28]. This is in contrast to conventional piezoelectric ceramics such as lead zirconate titanate (PZT) which are excellent insulators. Therefore, it is possible that GaN is better suited to sensing dynamic, rather than static environments. A dynamic gauge factor of 130 was measured for the GaN/sapphire sample in [28] when it was deformed longitudinally, which is four times greater than the gauge factor of SiC. These samples consisted of a 3 – 5  $\mu\text{m}$  layer of GaN epitaxially grown slightly off-axis from a (0001) sapphire substrate [28]. The GaN/sapphire sample also exhibited a small static gauge factor of four [28], suggesting that GaN is weakly piezoresistive and can be used as a static sensor in extreme environments in the absence of another suitable material. Further evidence in support of GaN being a viable static sensing material will be discussed in chapter 7. This small piezoresistive effect is caused by the electron donor energy being shifted closer to the conduction band by applying a stress [28].

A method for measuring piezoelectric and piezoresistive effects and the gauge factor of GaN sensors is shown in figure 1.3, as described by Strittmatter [31] and in three papers by Tilak [30, 32, 33]. The basic process is to clamp a section of a GaN/substrate and use capacitive contacts for taking electrical measurements. In the cases of [30-33] the type of capacitive contacts are known as metal-insulator-semiconductor (MIS) capacitors. Using equation (1.2), it is possible to measure the gauge factor of a GaN sensor and determine its piezoelectric and piezoresistive behaviour. Therefore a capacitor is a suitable sensing element for GaN, but it does have the drawback of needing to be typically 40 to 50  $\mu\text{m}$  in gate length and 50  $\mu\text{m}$  in gate width [34-36] in order to retrieve a significant signal, which is a significant handicap when fabricating a MEMS sensor. The type of cantilever structure, shown in



figure 1.3, can also be used to measure the piezoelectric coefficients of GaN, for which there are no agreed measurements in the literature; in addition to being a potential viable strain gauge device.

In reference [30], GaN-based strain gauges with GaN epitaxially grown on (111) Si and c-plane (0001) sapphire were fabricated. These relatively large cantilevers were 17 x 5 mm long, with a ~2  $\mu\text{m}$  n-doped GaN layer deposited on the sapphire substrate; which is left unaltered and at its original thickness. When the substrate is sapphire, two MIS capacitive contacts were deposited directly onto a 2  $\mu\text{m}$  thick n-doped GaN layer. When silicon was used as a substrate, a 20 nm AlGaN layer was grown on top of a 1  $\mu\text{m}$  thick layer of GaN; the contacts were then fabricated on the AlGaN. As discussed earlier, the purpose of the n-type doping and the use of AlGaN in the respective cantilevers are to lower the potential barrier of GaN to improve the reliability of the capacitive contacts. Lowering the potential barrier means that it will take less energy for an electron to pass from the metallic contact to the conduction band in the AlGaN and vice versa. This means in the case of the GaN cantilevers in [30], the semiconductor component of the device is the GaN or GaN/AlGaN layer. An insulating layer of 100 nm  $\text{SiO}_2$  was then deposited on the GaN/sapphire wafer, and 30 nm of the same material was deposited on the AlGaN/GaN/Si wafer to create a capacitive contact. A 30 nm layer of  $\text{SiN}_x$  was then deposited on both types of wafer, completing the insulator layer [30]. Two differing metal contacts were then deposited on the insulating layer [30].



**Figure 1.3** Schematic of the MIS diode cantilever used in Strittmatter *et al* [4]. The cantilevers described in [30] are similar.

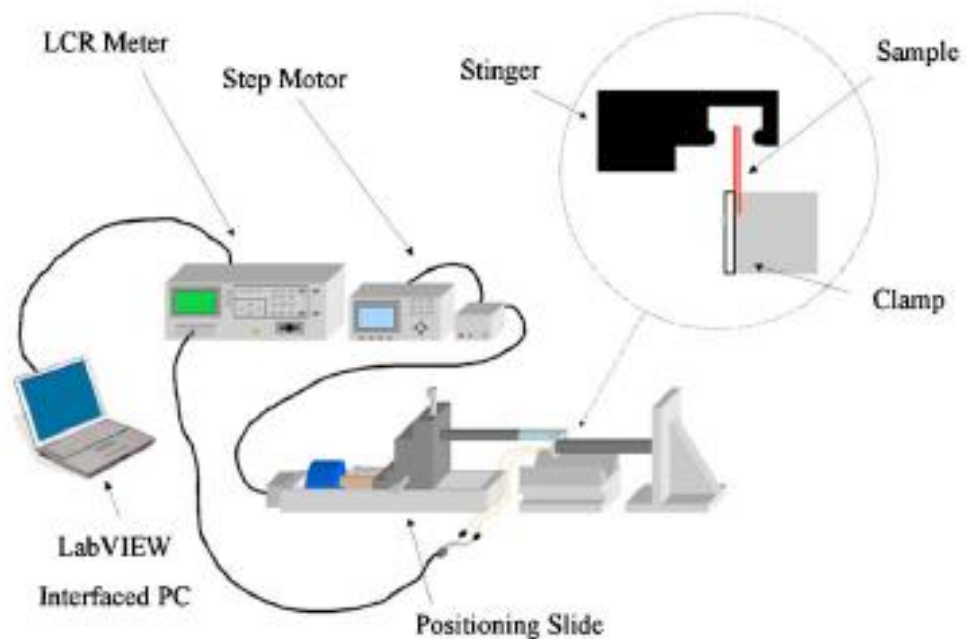
For a MIS capacitor, one of the contacts has Ohmic current-voltage (IV) characteristics and the other contact has Schottky barrier characteristics. The main difference between the two types of barriers is that a Schottky barrier rectifies the current and an ohmic contact does not. This means that the I-V characteristic curve of an ohmic device is linear and symmetric, with the opposite being the case in a Schottky device. An Ohmic contact is defined as a metal-semiconductor contact that has a minimal resistance in relation to the total resistance of the semiconductor device [2]. Every semiconductor device requires at least two metal-semiconductor interfaces, so at least one good ohmic contact is required for the majority of semiconductor devices. For GaN-based devices, it is difficult to make good ohmic contacts because it has a wide band gap of 3.6 eV. This means that this band gap has to be lowered at the surface. Possible methods for doing this include heavily doping the GaN device layer, severely impacting on the performance of the device, or by creating heterojunctions by growing thin epitaxial layers of a metallic alloy such as AlGaIn. Examples of both methods are contained in the literature [30], using both doping and epitaxial layers to help fabricate an ohmic contact. The two different types of devices in [32] use different levels of doping. Table 1.1 below shows the relative performances of the cantilever devices in [30] and [32].

**Table 1.1** Gauge factors of different cantilever devices.

<b>Data Source</b>	<b>Structure</b>	<b>Operating Temperature (K)</b>	<b>Gauge Factor</b>	<b>Dimensions (mm)</b>
[30]	AlGaIn/GaN MIS capacitor (n-type doping $<10^{16} \text{ cm}^{-3}$ )	298	575	17 x 5
		673	361	
[30]	GaN MIS capacitor (n-type doping $<10^{16} \text{ cm}^{-3}$ )	298	75	17 x 5
[32]	$7 \times 10^{16} \text{ cm}^{-3}$ n-type doped 2 $\mu\text{m}$ thick GaN MIS capacitor	298	167	$8 \times 5$
		523	104	
[32]	$10^{18} \text{ cm}^{-3}$ n-type doped 250 $\mu\text{m}$ thick GaN MIS capacitor	298	25	$8 \times 5$
		398	17	

Table 1.1 shows that the cantilever with an AlGaN epitaxial layer has the largest gauge factor and is the most sensitive to changes in stress. All of the cantilevers in table 1.1 were designed to be used as capacitors that could be used to measure either the piezoelectric coefficients of GaN or the gauge factor of the device. The application of the cantilevers in [30] is for high temperature strain gauges, which is similar to the application of the devices in this PhD; although the cantilevers or membranes are likely to be smaller [23]. The AlGaN device performs well at 400°C (673K), indicating that the devices created during this PhD may also function well at similar temperatures. The ohmic contact fabricated for both types of cantilever in [30] was a stack of Ti/Al/Mo/Au with thicknesses of 10 nm/100 nm/50 nm/50 nm, and the Schottky gate was Ni (50 nm)/Au (300 nm). A 500 nm gold layer was finally deposited on both contacts to allow wires to be bonded.

A schematic from reference [33], in figure 1.4, shows a method employed for measuring the piezoelectric coefficients of GaN.



**Figure 1.4** Schematic of an experiment used in reference [33] to determine the piezoelectric coefficient of GaN.

It should be mentioned that to date, no evidence has been found for the high temperature testing of the piezoelectric properties of these types of devices. In [33] all of the measurements were carried out at room temperature.

## **1.4 GaN HEMTs**

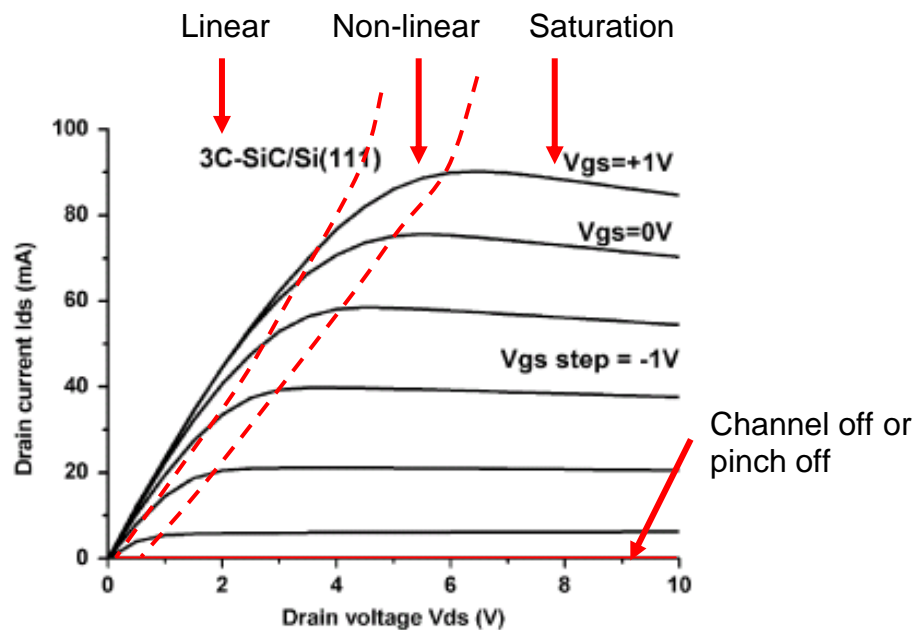
### ***1.4.1 HEMT Terminology***

GaN HEMTs are used as sensing elements for the sensor described in chapter 7 and in this literature review. To help with the interpretation of the results in this chapter, the basics of HEMT operation and terminology will be described in this section. The High Electron Mobility Transistor (HEMT), also known as a Heterojunction Field Effect Transistor (HFET). HEMTs are often used in modern electronics as they have high carrier concentrations and superior electron mobilities [2]. A HEMT belongs to the metal semiconductor field effect transistors (MESFET) group of field effect transistors (FETs). HEMTs are often used instead of Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) as they have high carrier concentrations and superior electron mobilities. At the interface between the semiconducting materials, known as a heterojunction, a 2D electron gas (2DEG) forms and this is the cause of the HEMT's high electron mobility [2].

In order to allow conduction in a semiconductor, it needs to be doped with impurities such as iron or silicon. Electrons tend to collide with the impurity atoms, slowing them down, and reducing both the efficiency and electron mobility of the device [2]. In the case of a simple GaN/AlGa<sub>N</sub> HEMT (figure 1.1), where the heterojunction consists of an n-doped epitaxial layer of AlGa<sub>N</sub> on top of a GaN layer with no deliberate dopants (unintentionally doped GaN is slightly n-doped due to the crystal growth process); the electrons produced in the n-AlGa<sub>N</sub> epitaxial layer will diffuse into the top of the GaN layer because a quantum well is created in its conduction band. If a heterojunction is allowed to reach chemical and thermal equilibrium, then the Fermi level of both materials aligns and this means that it is constant throughout the system. This means that electrons will leave some regions, causing depletion and

will accumulate in others in order to find equilibrium. The depletion and accumulation of electrons causes the bending of conduction and valence bands near the interface. In the case of a heterojunction between AlGa<sub>N</sub> and GaN, the band bending means that the electrons accumulate in a quantum well on the GaN conduction band near the AlGa<sub>N</sub>/GaN interface.

In practice, this quantum well exists as a thin layer between the n-AlGa<sub>N</sub> and GaN layers and is known as a 2DEG. Inside the 2DEG, there is a very high concentration of highly mobile electrons and the electrons can move quickly without colliding into any impurity atoms; the position of the 2DEG is marked in figure 1.1. Therefore, the HEMT overcomes the impurity collision problem because electrons can travel unhindered along the 2DEG: leading to very low resistivity in the device. Furthermore, the impurity concentration of a HEMT device has little impact on its performance.



**Figure 1.5**  $I_{DS}$ - $V_{DS}$  of a AlGa<sub>N</sub>/GaN HEMT with a 3 x 150  $\mu$ m gate grown on a SiC substrate from [6].

The IV curve shown in figure 1.5 is fairly typical for an AlGa<sub>N</sub>/GaN HEMT. Every  $I_{DS}$ - $V_{DS}$  curve shown for each respective  $V_{GS}$  firstly consists of a linear region, where

both  $I_{DS}$  and  $V_{DS}$  increase linearly (Ohm's law). When the  $I_{DS}$ - $V_{DS}$  characteristic becomes non-linear, caused by the 2DEG becoming saturated with charge carriers,  $I_{DS}$  then reaches a peak and this point is known as the saturation point.  $I_{DSat}$  and  $V_{DSat}$  are defined as the saturation current and voltage respectively. If  $V_{GS}$  is sufficiently high, a decrease in current is observed beyond  $V_{DSat}$  and this is caused by the self-heating of the device. Self-heating occurs due to the HEMT producing large amounts of power, which is usually dissipated as heat and this increases the working temperature of the device. Increasing the working temperature of an AlGaIn/GaN HEMT reduces the concentration of charge carriers, which are electrons in a n-doped HEMT and holes in a p-doped HEMT, in the 2DEG thereby reducing  $I_{DS}$ .

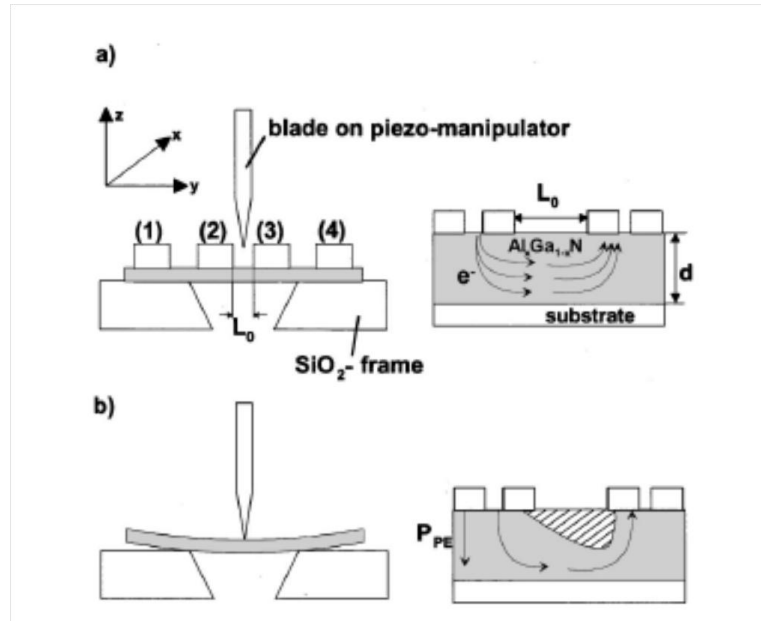
The effects of self-heating can be reduced in an n-doped depletion mode semiconductor by applying more negative bias on  $V_{GS}$ , as shown in figure 1.5, since this reduces the current flowing through the device [2]. If enough negative bias is applied on  $V_{GS}$ , then  $I_{DS}$  can be reduced to zero, a condition known as 'channel off' or 'pinch off'. This type of behaviour is typical to FETs and is basically caused by the following mechanism. As more negative bias is applied the 2DEG channel it creates a depletion region, which narrows the channel in which the 2DEG operates. The depletion region causes the resistance between the drain and source to increase, lowering  $I_{DS}$  [2]. If enough negative  $V_{GS}$  is applied, the source-drain resistance becomes large enough to effectively stop the current flow and switch off the device [2].

The final key point with AlGaIn/GaN HEMTs is that the piezoelectric and piezoresistive effects that occur in GaN when strained cause a perturbation in  $I_{DS}$ , which could be used for pressure sensing. Some literature examples of AlGaIn/GaN HEMTs being used for strain sensing will be described in the next sub-section and a diaphragm AlGaIn/GaN pressure sensor designed and tested in this project will be described in chapter 7.

### ***1.4.2 GaN HEMTs in the literature***

GaN HEMTs have significant potential for measuring mechanical strain in extreme environments. As mentioned previously, GaN has excellent thermal and mechanical properties meaning that it can withstand high ambient pressures and temperatures, potentially up to 1000°C. However, GaN needs a suitable transducer so that the piezoelectric polarisation charge caused by the strain can be transformed into a measurable electrical signal. GaN HEMTs appear to be a suitable transducer for doing this because they are sensitive to perturbations in capacitance, current and voltage caused by piezoelectric polarisation [37].

Dynamic strain measurements undertaken by Eickhoff *et al* [37] on AlGaIn/GaN HEMTs with varying Al content in the AlGaIn layer. These HEMTs were grown on c-plane (0001) sapphire, meaning that the epitaxial GaN would also be c-plane orientated [38]. This means that both GaN and AlGaIn are correctly orientated to emit the piezoelectric charge vertically with respect to the GaN surface. The GaN/AlGaIn/GaN HEMT structure was grown N-face, rather than the typical Ga-face, and this meant that the HEMT was ‘inverted’. The HEMT was inverted because this meant that the 2DEG would be confined by the upper GaN channel and AlGaIn barrier [37]. The HEMTs in [37] were probed by a piezomanipulator at 30 Hz on the HEMT side, forcing the piezoelectric polarisation into the 2DEG as shown in the experimental schematic from [37] contained in figure 1.6.



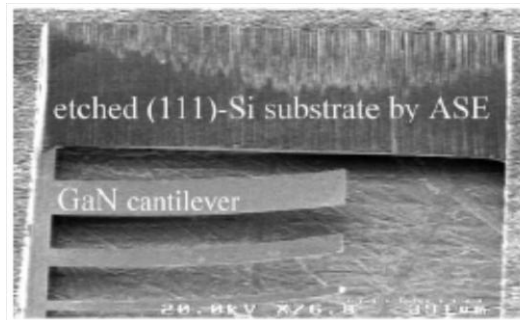
**Figure 1.6** Experimental schematic used in [37] a) shows the sample with out strain and b) shows the sample strained. The current was measured between contacts (1) and (4), whilst the change in voltage was measured between (2) and (3).

As figure 1.6 shows, the piezo-manipulator blade imparts a compressive stress on the N-face HEMT structure and this forces the piezoelectric polarisation charge towards the 2DEG channel. This causes the 2DEG channel to thin, increasing its resistance. This causes a small drop in voltage at constant current and this change in voltage was used to determine the gauge factor of the device [37]. This experiment was repeated on four samples with varying Al content in the AlGaN layer. The conclusion of reference [37] was that increasing the Al content increased the gauge factor of the HEMT, from 3.8 when the Al content was zero to 25.8 when the Al content was 35%. In addition, it was found that increasing the carrier concentration increased the gauge factor even further. These results ultimately compared well with the results produced by more-expensive SiC piezosensors [37]. The work in reference [37] demonstrates that AlGaN/GaN HEMTs have the potential to be highly sensitive mechanical sensors in extreme environments.

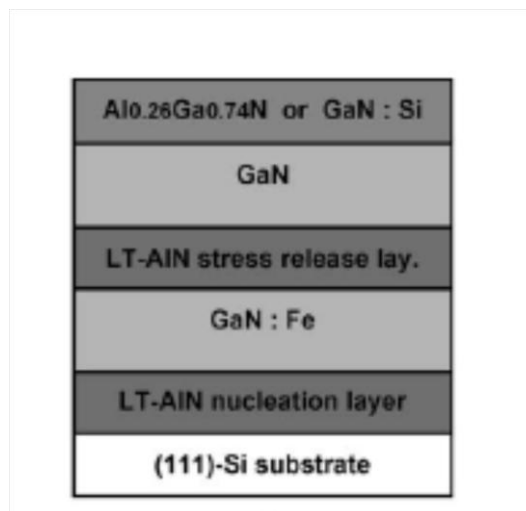
Zimmermann *et al* [29] described how a cantilever could be fabricated from a AlGaN/GaN wafer grown on a (111) Si substrate, with a HEMT as a sensing element. A HEMT was placed on the point of maximum sensitivity, where the cantilever is clamped and can pivot [29]. The GaN cantilevers in reference [29] were grown from a



bulk (111) Si wafer and where etched out by dry etching, after the HEMT sensing element was fabricated. The dry etching method used was determined by whether the wafer was etched from the front (GaN) or rear (substrate) side. Front side etching of Si was achieved by reactive ion etching (RIE) using a  $\text{CF}_4$  plasma and rear side etching was done by anisotropic Si etching (ASE) method known as the “Bosch” process. Figure 1.7 (b) shows an image of the released cantilevers.



(a)



(b)

**Figure 1.7** Where (a) is the image of the GaN cantilevers produced and (b) is the stack of materials grown to create the HEMT cantilever sensor [29].

Figure 1.7 (b) shows the wafers used in [29] stack of materials. It is interesting to note that the AlN nucleation layer deposited between the GaN and Si was deposited at an unspecified low temperature (LT). LT nucleation layers are deposited at between  $\sim 550$  [39] to  $800^\circ\text{C}$  [39-41], therefore it would be reasonable to expect that these layers are deposited at this temperature range in reference [29]. GaN and AlN layers are usually deposited at temperatures in the range of  $1000$  to  $1100^\circ\text{C}$  by Metal

Organic Vapour Phase Epitaxy (MOVPE), which is the method used by the University of Bath. The purpose of depositing the LT-AlN layers was to increase the maximum thickness of the GaN layer. Without any strain relief, such as using LT-AlN layers, GaN cracks at thicknesses exceeding  $\sim 1 \mu\text{m}$  [29] which is due to the thermal and lattice mismatch between GaN and Si. Since Si has a lower thermal expansion than GaN, the GaN film is highly tensile and liable to crack once it exceeds the critical thickness of  $1 \mu\text{m}$ . The effects of thermal and lattice mismatch will be discussed in more detail later in this chapter (section 1.6). In reference [29] crack-free GaN layers of  $1.5 \mu\text{m}$  were grown, although it was stated that it was possible to grow  $6 \mu\text{m}$  layers using multiple LT-AlN/GaN stacks. The benefit of growing thicker GaN layers is that it reduces the dislocation density and allows the fabrication of better quality devices [29, 42]. An additional effect of the stresses of the wafers in reference [29] is that they curl downwards when etched, this is caused by the stress profile of the wafer and Poisson effects and will be discussed in section 1.7. The practical effect of this was that the cantilevers had to be probed from the Si side to reduce the risk of fracturing the cantilevers [29].

The HEMT sensing element on [29] was fabricated using a commonly used field effect transistor (FET) fabrication methods. Firstly, the HEMT region is isolated using a mesa, which was created using an argon dry etch [29]. The Ohmic and Schottky contacts were then deposited; in a HEMT the source and drain are Ohmic because they require linear I-V characteristics, and the gate consists of a Schottky contact. In reference [29], the Schottky gate consisted of a metallic stack of Ni/Au and the Ohmic stack was Ti/Al/Ni/Au.

After fabrication, the GaN cantilever devices were probed using a needle attached to a high precision motor, allowing an accurate measurement of deflection. Unusually, the piezoresponse of the sensor was not measured at the moment when strain was applied and the dynamic piezoresponse was greatest; the change in current was measured in the dark, because GaN is UV sensitive, after 10 minutes in order to allow the material to settle down and for a static measurement. Other static measurements in the literature have indicated that most of the piezoelectric and spontaneous polarisation charges dissipate and the sensors have a low gauge factor [28]. However the measurements showed was a device with good sensitivity and a gauge factor of 90

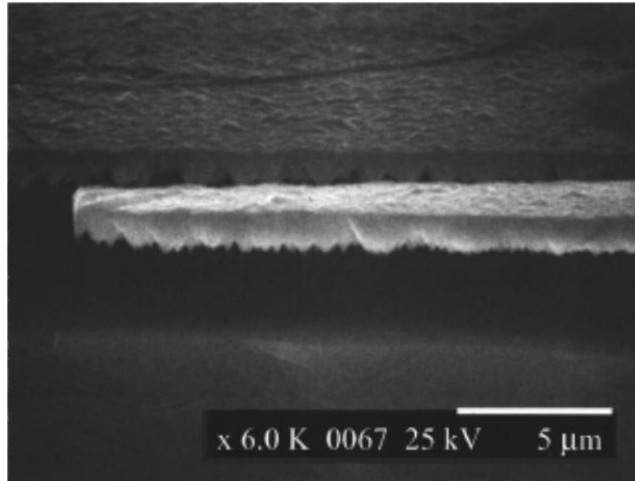
[29]. There is an improvement in static gauge factor that is caused by the removal of the substrate in [29] and this results in a less stiff and more sensitive cantilever, which could be used as a static strain sensor.

### **1.5 GaN-based cantilever devices**

Over the past decade, a variety of GaN-based cantilever devices for potential sensor applications have been fabricated by different research groups [4, 29-33, 43-45]. The GaN-based cantilevers are usually either grown on (111) silicon or (0001) sapphire substrates. In this section, recent published research into the creation of viable cantilever devices will be described.

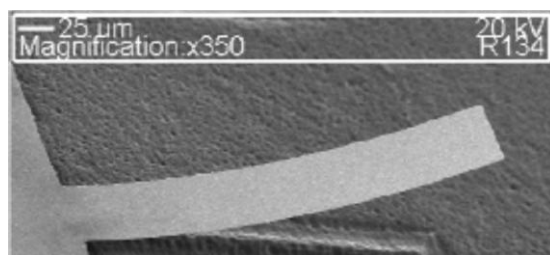
Stonas *et al* [43], a team from the University of California – Santa Barbara, created freestanding GaN MEMS cantilevers on a sapphire substrate. These cantilevers were fabricated using a backside illuminated photo electrochemical (BIPEC) wet etch method, that obtained a lateral etch rate of 5  $\mu\text{m}/\text{min}$ ; creating deeply undercut cantilever structures. BIPEC is a photo-electric wet etch process, where electrolysis and light are used to etch the wafer. GaN is an inert material that is difficult to wet etch in normal circumstances. The GaN/sapphire wafer was immersed in a 2.2M KOH electrolyte solution, with a Pt cathode and the wafer sample acting as an anode [43]. An electrical contact was achieved by pressing a wire against a Ti/Au contact. The sapphire side of the sample was illuminated with a Xe/Hg lamp (backside illumination) and this started the etching process [43]. It was possible to create cantilevers that were around 100  $\mu\text{m}$  in length using BIPEC [43].

This method is an example of a ‘top-down’ method where a GaN layer of a few microns is deposited on a sapphire substrate, the wafer was then patterned and the unmasked regions are etched away thus creating free-standing GaN cantilever templates. This template was then undercut using BIPEC, creating the free standing cantilevers. Figure 1.8 shows an image of the tip of a cantilever fabricated by BIPEC from [43]. The cantilevers were successfully actuated and their resonance spectra were measured [43].



**Figure 1.8** Image of a cantilever tip from reference [43], clearly showing the surface morphology.

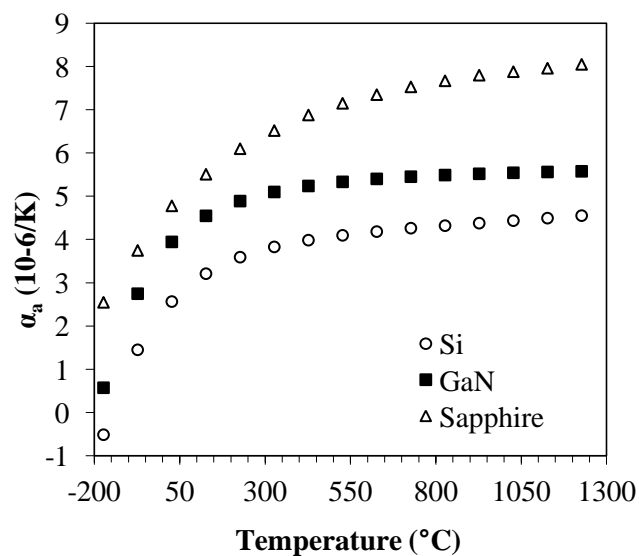
This method does have some disadvantages; with figure 1.8 showing a rough etch morphology of the cantilever with islands and whiskers on the surface. These imperfections are caused by a reduced etch rate around lattice dislocations [43], and this in turn means that the BIPEC produced cantilevers had residual sources of strain. In the following papers [44, 46], the GaN cantilevers are described as having a strain gradient that causes them to curl upwards when detached from the sapphire substrate. Furthermore, the addition of an InGaN epitaxial layer on the cantilever causes a small downwards curvature [44, 46]. An identical effect is described in Sillero *et al* [45], and shown in figure 1.9 where AlGaN/GaN cantilevers, this time grown on a silicon substrate, also curl upwards when released by a wet under-etching method. This observed curvature is thought to be due to an uneven strain relaxation effect that occurs as the cantilever is released from its substrate. The curvature is in the opposite direction to what is expected from the mismatch of the coefficients of thermal expansion (CTEs) between GaN and silicon.



**Figure 1.9** An example of a MEMS GaN cantilever grown on a (111) Si substrate curling downwards from reference [45].

### 1.5.1 Extrinsic stress due to CTE mismatch

In a bi-layered wafer, such as GaN/silicon or GaN/sapphire, strain builds up in the system as it cools from the growth temperature ( $\sim 1000^\circ\text{C}$ ) to room temperature due to a thermal expansion mismatch between GaN and the substrate. Figure 1.10 shows that the a-axis CTE of GaN is greater than that of silicon and less than that of sapphire. Therefore, GaN/Si composite wafers would be expected to bow in the opposite direction of GaN/sapphire wafers. This CTE mismatch is an important source of extrinsic strain in a pre-released cantilever; with other important sources of strain including material defects and lattice dislocations resulting from a lattice misfit. This build-up of strain can significantly affect the performance of the device [45] and can reduce the lifetime of the device by increasing the risk of failure and reducing the safety factor. To release the accumulated stress of GaN on silicon, Zimmermann *et al* [17] introduced AlN stress release interlayers to enable the growth of thick GaN layers and cantilevers. The AlN interlayers introduced a high compressive stress, which by overcompensation, lead to convex bowing of the Si wafer. A gauge factor of  $\sim 90$  was measured [17] and gauge factors in excess of 1000 have been reported for GaN MIS diodes on cantilevers [3].



**Figure 1.10** Comparison between the CTEs of GaN, Si and sapphire along the interfacial (a-) axis. [47-51]

### ***1.5.2 Intrinsic stress due to lattice mismatch***

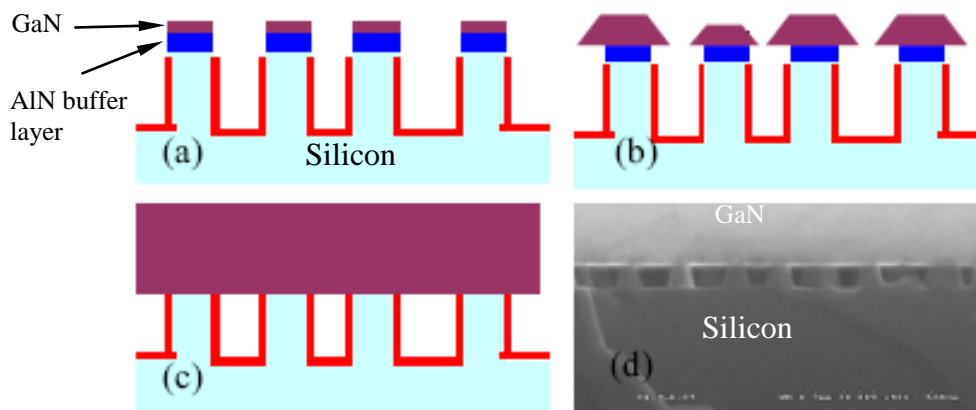
In addition to the CTE mismatch, GaN layers grown on substrates such as sapphire and silicon can have high dislocation densities due to a lattice parameter mismatch between GaN and the substrate (intrinsic stress). A lattice mismatch induces a tensile strain component into the wafer if the lattice constant of the film ( $a_f$ ) is greater than that of the substrate ( $a_s$ ) [52]. A compressive strain will be introduced into the system if the lattice constant of the film is smaller than that of the substrate. When the film is sufficiently thin (~10 nm) the crystal lattice of the film is strained to match that of the substrate [2]; however, for thicker films the lattice mismatch introduces dislocations at the interface [2].

Assuming that the lattice constants of GaN ( $a = 0.3189$  nm;  $c = 0.5185$  nm), silicon ( $a = 0.54309$  nm) and sapphire ( $a = 0.4758$  nm;  $c = 1.2991$  nm) do not change from bulk values during the growth process, the misfit parameters  $f = (a_f - a_s)/a_s$  of GaN/Si and GaN/sapphire at 250K are -16.98% [22] and 16.09% [23], respectively. An experimental measurement of the misfit in a GaN/sapphire wafer yielded  $15.0 \pm 0.3\%$  [53] and the GaN film layer is in compression [52]. For GaN/Si wafers the misfit is opposite in sign and the strain on the GaN layer is in tension. The combination of CTE and lattice mismatch leads to a complex stress state in the system.

### ***1.5.3 Reducing internal stress***

Large extrinsic and intrinsic stresses within the system mean that cantilevers fabricated by dry and wet etch techniques suffer from a poor performance due to high dislocation densities, making them less suitable in high temperature and pressure environments and high power applications. Therefore a new approach is needed to produce a viable cantilever, meaning that a more bottom-up approach is required when fabricating the cantilevers: with the devices grown directly on top of a patterned wafer of GaN/substrate. It is possible to grow GaN laterally outwards using either epitaxial lateral overgrowth, defined in the literature as either ELO, LEO or ELOG

[24], or pendeo-epitaxy (PE [25]); both can significantly reduce stress in the GaN film layer [54] and are produced in a similar way. These methods are used to create a compliant GaN layer which helps to relieve the thermal mismatch stress, and reduce dislocation densities and related strain profiles. The practical implications for GaN cantilever research are that the devices are less likely to fracture or deform when released. A simple diagram of the nano-pendeo epitaxy (NPE) process for growing GaN on Si from [54] is shown in figure 1.11 and will now be discussed.



**Figure 1.11** (a – c) Schematic drawings of the NPE growth process. (d) SEM cross-sectional image of a GaN NPE film [54].

When growing a layer of GaN by NPE, firstly an ultrathin 10 nm AlN/GaN layer is deposited on a (111) Si substrate using a pulsed growth technique [54]. The next step is to deposit a silicon nitride ( $\text{SiN}_x$ ) mask by plasma enhanced chemical vapour deposition (PECVD). A 5 nm layer of nickel is deposited on the  $\text{SiN}_x$  and nickel nanodots are formed by annealing the wafer in  $\text{N}_2$  gas at  $\sim 830^\circ\text{C}$  for 30 seconds [54]. The nickel nanodots and  $\text{SiN}_x$  mask protects the ultrathin AlN/GaN layer underneath from the ICP-RIE etch. This process produces a random pattern of nanocolumns from which high-quality GaN material can be grown. If the substrate is Si, then the nanocolumns are predominantly Si with a  $\sim 10\text{nm}$  AlN/GaN buffer layer on the top [54]. A small amount of GaN is then deposited on top of the nanocolumn, as in figure 1.11(a). The GaN deposits are then grow vertically and laterally, as shown in figure 1.11(b), in a trapezoidal fashion [54]. This growth will continue until the GaN film is fully-coalesced on top of the nanocolumns, as shown in figure 1.11(c – d) [54]. Since

the thermal stress ( $\sigma$ ) in the film is related to stiffness ( $E$ ), CTE ( $\alpha$ ), temperature change ( $\Delta T$ ) by  $\sigma = E\alpha\Delta T$ , the high compliance (low stiffness) of the nanocolumn structure can help reduce the thermal stresses when the wafer is exposed to large fluctuations in temperatures [54].

Barabash *et al* [55] examined the effect of dislocations, thermal expansion and lattice mismatch on laterally overgrown GaN cantilevers made using cantilever epitaxy; a form of epitaxial lateral overgrowth (ELOG). GaN grown using cantilever epitaxy (CE) has a typical threading dislocation density of  $<10^7/\text{cm}^2$  and this compares favourably with typical dislocation densities of  $10^8 - 10^{10}/\text{cm}^2$  for GaN layers grown directly on Si, SiC or sapphire [16]. Finite element (FE) simulations in reference [55] predict that the stress in GaN cantilevers etched out of a Si substrate becomes compressive as the distance increases from the GaN/Si interface, and tensile stresses remain on the GaN grown on the Si column due to lattice parameter misfit and thermal expansion. However, experimental measurements using polychromatic x-ray micro-diffraction in reference [55] showed that there was an upward tilt in the laterally overgrown GaN wings perpendicular to the stripes and another tilt was found parallel in direction to the stripes. Neither of the tilts could be fully explained by thermal expansion. The tilt perpendicular to the stripes was a consequence of misfit dislocations and the tilt parallel to the stripes was caused by a miscut of the substrate [55].

Based on the papers already in the literature [45, 56], GaN-based MEMS cantilevers etched from both GaN/silicon and GaN/sapphire wafers can both curl upwards [43, 44]. However this is not always the case [29], particularly when strain relief techniques such as LT-AlN layers have been used. These results and experimental data from reference [55] show that the curvature and strain of the cantilever is not caused by purely thermal and lattice mismatch. Poisson effects, linked to the geometry to the cantilever, and crystallographic misalignment can cause the cantilever to deform in an unexpected direction. Crystallographic misalignment introduces more dislocations into a system, an example being the substrate miscut in reference [55]. Both NPE and CE reduce lattice dislocations in the GaN epitaxial layer because they minimise contact between GaN and the substrate. Similar approaches are being explored by a European Framework 7 Project ‘MORGaN’ (FP7)



[15] that aim to develop new electronic sensors and devices to operate in extreme conditions by exploiting and combining the physical properties of diamond and GaN-based heterostructures [14, 15].

The following section provides an overview of the key materials to be examined in this thesis. This includes GaN and the potential substrates (Si and sapphire). As the thesis also involves Si (111)/polycrystalline diamond (PD) composites substrates, the properties of PD will also be discussed. A review of the properties is particularly important since it will be used to model thermal stresses in composite substrates and the response the sensors to applied mechanical stress. The raw data has been presented in tables rather than graphs to allow any materials modellers to use this data in the future.

## **1.6 Properties of GaN and Substrate Materials (Polycrystalline Diamond, Silicon and Sapphire)**

### ***1.6.1 Elastic matrices and their variants***

The response of a material to a mechanical stress can be defined by their elasticity, when within the elastic limit as defined by Hooke's Law. Hooke's law states that the strain is directly proportional to the magnitude of the applied stress, when the stresses are sufficiently small and below the elastic limit [57]. Hooke's Law for an elastic isotropic material can be written in either of the following forms.

$$\varepsilon = s\sigma \quad \text{or} \quad \sigma = c\varepsilon \quad (1.3)$$

Where  $s$  is the compliance constant and the stiffness constant is  $c$ . Stress and strain are given the symbols  $\sigma$  and  $\varepsilon$  respectively. In a simple isotropic system,  $c$  is also the material's Young's modulus. Some materials, such as single crystals or epitaxially grown materials have anisotropic properties; this means that a more generalised version of Hooke's law needs to be defined.

$$\begin{aligned} \varepsilon_{ij} &= s_{ijkl}\sigma_{kl} & \text{or} & & \sigma_{ij} &= c_{ijkl}\varepsilon_{kl} & (1.4) \\ i, j, k, l &= 1, 2, 3 \end{aligned}$$

Equation (1.4) shows that  $\sigma$  and  $\varepsilon$  are rank two tensors in the generalised form of Hooke's Law. This means that they each have nine separate terms, but this can be reduced to six using a matrix notation as below [57].

$$\begin{bmatrix} \sigma_{11} & \sigma_{12} & \sigma_{31} \\ \sigma_{12} & \sigma_{22} & \sigma_{23} \\ \sigma_{31} & \sigma_{23} & \sigma_{33} \end{bmatrix} \rightarrow \begin{bmatrix} \sigma_1 & \sigma_6 & \sigma_5 \\ \sigma_6 & \sigma_2 & \sigma_4 \\ \sigma_5 & \sigma_4 & \sigma_3 \end{bmatrix} \quad \begin{bmatrix} \varepsilon_{11} & \varepsilon_{12} & \varepsilon_{31} \\ \varepsilon_{12} & \varepsilon_{22} & \varepsilon_{23} \\ \varepsilon_{31} & \varepsilon_{23} & \varepsilon_{33} \end{bmatrix} \rightarrow \begin{bmatrix} \varepsilon_1 & \varepsilon_6 & \varepsilon_5 \\ \varepsilon_6 & \varepsilon_2 & \varepsilon_4 \\ \varepsilon_5 & \varepsilon_4 & \varepsilon_3 \end{bmatrix} \quad (1.5)$$

The matrix notation is valid because the vast majority of materials are orthogonal. Similarly, the rank four stiffness and compliance tensors can be reduced from 81 to 36 terms using matrix notation. Therefore, elasticity can be denoted as a 6 x 6 matrix in one of the following forms.

$$\begin{pmatrix} s_{11} & s_{12} & s_{13} & s_{14} & s_{15} & s_{16} \\ s_{21} & s_{22} & s_{23} & s_{24} & s_{25} & s_{26} \\ s_{31} & s_{32} & s_{33} & s_{34} & s_{35} & s_{36} \\ s_{41} & s_{42} & s_{43} & s_{44} & s_{45} & s_{46} \\ s_{51} & s_{52} & s_{53} & s_{54} & s_{55} & s_{56} \\ s_{61} & s_{62} & s_{63} & s_{64} & s_{65} & s_{66} \end{pmatrix} \quad \text{Or} \quad \begin{pmatrix} c_{11} & c_{12} & c_{13} & c_{14} & c_{15} & c_{16} \\ c_{21} & c_{22} & c_{23} & c_{24} & c_{25} & c_{26} \\ c_{31} & c_{32} & c_{33} & c_{34} & c_{35} & c_{36} \\ c_{41} & c_{42} & c_{43} & c_{44} & c_{45} & c_{46} \\ c_{51} & c_{52} & c_{53} & c_{54} & c_{55} & c_{56} \\ c_{61} & c_{62} & c_{63} & c_{64} & c_{65} & c_{66} \end{pmatrix} \quad (1.6)$$

Where  $s_{ij}$  is the compliance matrix form and  $c_{ij}$  is the stiffness matrix form. In this thesis, all materials have been defined using the stiffness matrix form. There are potentially 36 separate coefficients in each matrix, but this is usually simplified by lattice symmetry conditions. Firstly, all of the materials (GaN, Si, sapphire) discussed in this section are skew symmetric, where  $c_{ij} = c_{ji}$ . The total number of coefficients are then reduced to 21 and a material with this number of elasticity coefficients is

defined as triclinic [57]. The stiffness matrix arrangement for a triclinic material is shown below.

$$\begin{pmatrix} c_{11} & c_{12} & c_{13} & c_{14} & c_{15} & c_{16} \\ & c_{22} & c_{23} & c_{24} & c_{25} & c_{26} \\ & & c_{33} & c_{34} & c_{35} & c_{36} \\ & & & c_{44} & c_{45} & c_{46} \\ & & & & c_{55} & c_{56} \\ & & & & & c_{66} \end{pmatrix} \quad (1.7)$$

However, planes of symmetry reduce the number of independent stiffness coefficients for all of the materials used in this thesis. The most simply defined material is an isotropic material, which has two independent stiffness or compliance coefficients. These coefficients are  $c_{11}$  and  $c_{12}$  in the case of a stiffness matrix. The stiffness matrix of an isotropic material takes the following form:

$$c_{ij} = \begin{pmatrix} c_{11} & c_{12} & c_{12} & 0 & 0 & 0 \\ c_{12} & c_{11} & c_{12} & 0 & 0 & 0 \\ c_{12} & c_{12} & c_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{2(c_{11}-c_{12})} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{2(c_{11}-c_{12})} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{2(c_{11}-c_{12})} \end{pmatrix} \quad (1.8)$$

where  $\frac{1}{2(c_{11}-c_{12})}$  can be referred to as  $c_{44}$ , or the shear modulus  $G$ . Firstly, in order to determine the Young's modulus and Poisson's ratio of the material the stiffness coefficients need to be converted into their compliance form. The formulae for undertaking this conversion are [57]:

$$s_{11} = \frac{c_{11} + c_{12}}{(c_{11} - c_{12})(c_{11} + 2c_{12})} \quad (1.9)$$

$$s_{12} = \frac{-c_{12}}{(c_{11} - c_{12})(c_{11} + 2c_{12})} \quad (1.10)$$

$$s_{44} = \frac{1}{c_{44}} \quad (1.11)$$

From (1.9 – 1.11), it is possible to calculate the Young's modulus  $E$  and Poisson ratio  $\nu$  from the following.

$$E = \frac{1}{s_{11}} \quad (1.12)$$

$$\nu = -E \cdot s_{12} \quad (1.13)$$

Therefore, the  $G$  is related to  $E$  and  $\nu$  by the following formula.

$$G = \frac{E}{2(1-\nu)} \quad (1.14)$$

Although most materials have some form of elastic anisotropy, in particular single crystal substrates and epitaxially grown materials, it is often valid to assume that the material is isotropic because the anisotropic behaviour has little impact on the results; for example in the case for (111) silicon [58] (see chapter 3) where the shear modulus has two components, but the overall shear is close to that in the isotropic case.

The most simple anisotropic stiffness matrix is for a material with cubic symmetry. The main difference between isotropic and cubic materials is that  $c_{44}$  is independent of  $c_{11}$  and  $c_{12}$ . Therefore, cubic materials are defined using only three independent stiffness coefficients  $c_{11}$ ,  $c_{12}$  and  $c_{44}$  in the following matrix form.

$$c_{ij} = \begin{pmatrix} c_{11} & c_{12} & c_{12} & 0 & 0 & 0 \\ c_{12} & c_{11} & c_{12} & 0 & 0 & 0 \\ c_{12} & c_{12} & c_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & c_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & c_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & c_{44} \end{pmatrix} \quad (1.15)$$

Formulae (1.9 – 1.13) hold for a cubic stiffness matrix and  $G = c_{44}$ . Materials with cubic symmetry include those with face-centred cubic (fcc) lattice structures. These materials include Group IV materials such as Si, Ge and diamond. These materials are used in this project and the semiconductor industry in general.

Transversely isotropic or hexagonal symmetry materials require five independent stiffness coefficients. These coefficients are  $c_{11}$ ,  $c_{12}$ ,  $c_{13}$ ,  $c_{33}$  and  $c_{44}$  are arranged in the following form.

$$c_{ij} = \begin{pmatrix} c_{11} & c_{12} & c_{13} & 0 & 0 & 0 \\ c_{12} & c_{11} & c_{13} & 0 & 0 & 0 \\ c_{13} & c_{13} & c_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & c_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & c_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{2(c_{11} - c_{12})} \end{pmatrix} \quad (1.16)$$

The added complication of a transversely isotropic material is that  $E$ ,  $G$  and  $\nu$  become direction dependent because although  $x = y$ ,  $x, y \neq z$ : meaning  $z$  is now independent of  $x$  and  $y$ . Therefore,  $E$ ,  $G$  and  $\nu$  have separate terms in the  $x$  and  $z$  co-ordinates. In similarity to isotropic and cubic materials, the  $E$ ,  $G$  and  $\nu$  are calculated from their equivalent compliance coefficients (1.17 – 1.22).

$$s_{11} = \frac{1}{2} \left( \frac{c_{33}}{c_{33}(c_{11} + c_{12}) - 2c_{13}^2} + \frac{1}{c_{11} - c_{12}} \right) \quad (1.17)$$

$$s_{12} = \frac{c_{33}}{c_{33}(c_{11} + c_{12}) - 2c_{13}^2} \quad (1.18)$$

$$s_{33} = \frac{c_{11} + c_{12}}{c_{33}(c_{11} + c_{12}) - 2c_{13}^2} \quad (1.19)$$

$$s_{13} = \frac{c_{13}}{c_{33}(c_{11} + c_{12}) - 2c_{13}^2} \quad (1.20)$$

$$s_{44} = \frac{1}{c_{44}} \quad (1.21)$$

$$s_{66} = 2(s_{11} - s_{12}) \quad (1.22)$$

The engineering constants of  $E$ ,  $G$  and  $\nu$  in the x- and z-directions can be written in a form of the compliance matrix, shown as follows.

$$\begin{pmatrix} s_{11} & s_{12} & s_{13} & 0 & 0 & 0 \\ s_{12} & s_{11} & s_{13} & 0 & 0 & 0 \\ s_{13} & s_{13} & s_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & s_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & s_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & s_{66} \end{pmatrix} = \begin{pmatrix} \frac{1}{E_x} & \frac{-\nu_{xy}}{E_x} & \frac{-\nu_{yz}}{E_z} & 0 & 0 & 0 \\ \frac{-\nu_{xy}}{E_x} & \frac{1}{E_x} & \frac{-\nu_{yz}}{E_z} & 0 & 0 & 0 \\ \frac{-\nu_{yz}}{E_z} & \frac{-\nu_{yz}}{E_z} & \frac{1}{E_z} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{G_{xy}} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{G_{xy}} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{G_{yz}} \end{pmatrix} \quad (1.23)$$

Wurtzite structured materials, such as GaN, are examples of transversely isotropic stiffness matrices.

Materials with a rhombohedral or trigonal class 3m crystal system can be defined using six independent elastic coefficients, but are complexly arranged in the stiffness matrix. The six elastic coefficients are  $c_{11}$ ,  $c_{12}$ ,  $c_{13}$ ,  $c_{14}$ ,  $c_{33}$  and  $c_{44}$  are given as follows.

$$c_{ij} = \begin{pmatrix} c_{11} & c_{12} & c_{13} & c_{14} & 0 & 0 \\ & c_{11} & c_{13} & -c_{14} & 0 & 0 \\ & & c_{33} & 0 & 0 & 0 \\ & & & c_{44} & 0 & 0 \\ & & & & c_{44} & -c_{14} \\ & & & & & \frac{1}{2(c_{11} - c_{12})} \end{pmatrix} \quad (1.24)$$

Materials with a trigonal crystal system include sapphire, (111) silicon and quartz. Where appropriate, these materials have been assumed to have stiffness matrices that are isotropic, as in the case of (111) silicon, or hexagonal, which is closely related and has one less term. The shear terms for trigonal materials tend to be complex and have multiple components.

Other lattice types include orthorhombic, tetragonal and monoclinic. Orthorhombic, tetragonal and monoclinic stiffness matrices are relatively rare in nature. No materials used in this project have had these structures reported, so have not been included in this thesis, but details on these structures can be found in reference [57].

In order to undertake the modelling part of this PhD, the relevant material properties for GaN and substrate materials (sapphire, diamond and Si) have been collated and these will now be described.

## **1.6.2. GaN materials data**

### *1.6.2.1 Elastic coefficients*

As mentioned previously, GaN has a hexagonal stiffness matrix, as shown in (1.16), meaning that it has five independent elastic coefficients,  $c_{11}$ ,  $c_{12}$ ,  $c_{13}$ ,  $c_{33}$  and  $c_{44}$ . There are various values for these coefficients found in the literature, and have been summarised in table 1.2.

**Table 1.2** Room temperature values for the elastic coefficients of GaN.

$c_{11}$ (GPa)	$c_{12}$ (GPa)	$c_{13}$ (GPa)	$c_{33}$ (GPa)	$c_{44}$ (GPa)	Ref
370	145	110	390	90	[59]
296±18	130±10	158±5	267±17	24±2	[60]
390±15	145±20	106±20	398±20	105±10	[61]
374	106	70	379	101	[62]
396	144	100	392	91	[63, 64]
367	135	103	405	95	[65]
365	135	114	381	189	[66]
377	160	114	209	81.4	[67]
373	141	80.4	387	93.6	[68]
373	141	80	387	94	[69]
374.2	141.4	98.1	388.6	98.3	[48]
368.7	138.5	103.0	362.1	96.6	Average

(All measurements taken at or near 300K.)

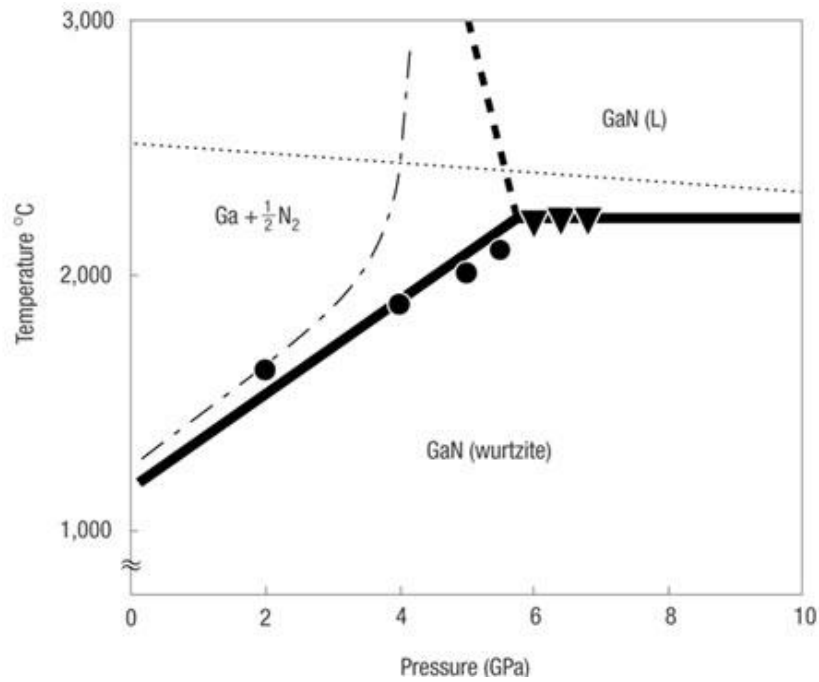
There is a significant variation in the literature values for the room temperature values of the elastic coefficients of GaN. There are two good reasons for this. Firstly, imperfections in the material, such as dopants and lattice dislocations, can change the stiffness of a material [70]. The geometries required to measure some of the stiffness coefficients are achieved using shear tests and it is difficult to constrain the material in such a way as to measure a pure shear. All measurements suffer from this problem, even though the quality of the semiconductor samples has improved over the years. One way of defining the room temperature stiffness coefficients of GaN is to take a literature average with outliers' neglected using statistical analysis (See appendix A1.5 for details). The literature average is shown in the bottom column of table 1.2. As GaN expands as it is heated, the temperature dependent elastic coefficients decrease in value and the material becomes less stiff. Reeber and Wang [3] have determined the temperature dependent elastic coefficients of GaN up to 900K and within 7% of their probable value and data is summarised in table 1.3.



**Table 1.3** Temperature dependent GaN elastic coefficients [3].

T (K)	$c_{11}$ (GPa)	$c_{33}$ (GPa)	$c_{12}$ (GPa)	$c_{13}$ (GPa)	$c_{44}$ (GPa)
0	376.4	387.1	142.4	99.1	98.5
50	376.4	387.1	142.4	99.1	98.5
100	376.1	386.8	142.3	99.0	98.5
150	375.7	386.5	142.1	98.9	98.5
200	375.4	385.8	141.9	98.7	98.4
250	374.8	385.2	141.7	98.4	98.4
300	374.2	384.4	141.4	98.1	98.3
400	372.6	382.3	140.6	97.4	98.1
500	370.7	380.0	139.8	96.7	97.9
600	368.5	377.8	138.8	96.0	97.7
700	366.3	375.5	137.7	95.3	97.5
800	364.1	373.3	136.7	94.5	97.3
900	362.0	371.1	135.6	93.8	97.1

Table 1.3 shows that the changes in elastic coefficients with temperature are small when considering the variation in literature values at room temperature. However, these values are not complete because GaN is usually deposited at 1050 °C (1323K). This problem has been overcome by converting the stiffness coefficients into their engineering constant equivalents  $E$ ,  $G$  and  $\nu$ . The thermal decay of these constants was plotted as part of this thesis and it was observed that they decay approximately linearly beyond 500K. This meant the engineering constants could be extrapolated up to 1050°C, assuming that there were no phase changes or melting as indicated in figure 1.12. High temperature measurements of some of the elastic properties of GaN are shown in chapter 5. A table containing the appropriate engineering constants up to 1400K is included in table 1.4. The Poisson ratios were also calculated and the values for  $\nu_{xy}$  and  $\nu_{xz}$ , to 2 significant figures, are 0.33 and 0.19 respectively, for all temperatures between 0 and 1400 K.



**Figure 1.12** Phase diagram of GaN [71].

**Table 1.4** The temperature dependent engineering constants up to 1400K.

Temp (K)	$E_x$ (GPa)	$E_z$ (GPa)	$G_{xy}$ (GPa)	$G_{xz}$ (GPa)	$\nu_{xy}$	$\nu_{xz}$
0	312.0	349.2	98.5	117.0	0.333	0.191
250	310.8	347.7	98.4	116.6	0.333	0.191
300	310.4	347.1	98.3	116.4	0.333	0.190
400	309.2	345.3	98.1	116.0	0.333	0.190
500	307.7	343.4	97.9	115.4	0.333	0.189
600	306.0	341.5	97.7	114.8	0.333	0.189
700	304.4	339.5	97.5	114.3	0.332	0.189
800	302.8	337.6	97.3	113.7	0.332	0.189
900	301.3	335.7	97.1	113.2	0.331	0.189
1000	299.7	333.8	96.9	112.6	0.330	0.188
1100	298.1	331.9	96.7	112.1	0.330	0.188
1200	296.5	330.0	96.5	111.5	0.329	0.188
1300	294.9	328.1	96.3	111.0	0.329	0.187
1400	293.3	326.1	96.1	110.4	0.329	0.187

*(Interpolated values in italics)*

#### 1.6.2.2 Coefficients of thermal expansion (CTEs)

GaN has two coefficients of thermal expansion (CTEs), one for the c-axis (x, y directions) and another for the a-axis (z direction) because it has hexagonal lattice

symmetry. Both CTEs are temperature dependent, with more rapid expansion at higher temperatures. Reeber and Wang [48] includes data showing temperature dependence of the CTEs, as well as the equivalent lattice constants. The lattice constants are included for reference and are not used for any modelling in this project.

**Table 1.5** Recommended temperature dependent lattice constants and CTEs for GaN [48].

Temperature (K)	$\alpha_a$ ( $10^{-6}/\text{K}$ )	$\alpha_c$ ( $10^{-6}/\text{K}$ )	$a_0$ (Å)	$c_0$ (Å)
0	0.0000	0.0000	3.1868	5.1828
25	0.0242	0.0308	3.1868	5.1828
50	0.0468	0.0565	3.1868	5.1828
75	0.1799	0.1688	3.1868	5.1828
100	0.5765	0.5110	3.1868	5.1829
125	1.1465	1.0141	3.1869	5.1830
150	1.7433	1.5486	3.1870	5.1831
175	2.2861	2.0389	3.1871	5.1834
200	2.7501	2.4596	3.1873	5.1837
225	3.1370	2.8104	3.1876	5.1840
250	3.4577	3.0991	3.1878	5.1844
275	3.7241	3.3372	3.1881	5.1848
300	3.9469	3.5342	3.1884	5.1852
350	4.2945	3.8356	3.1891	5.1862
400	4.5495	4.0506	3.1898	5.1872
450	4.7420	4.2083	3.1905	5.1883
500	4.8906	4.3270	3.1913	5.1894
550	5.0077	4.4183	3.1921	5.1905
600	5.1013	4.4900	3.1929	5.1917
650	5.1773	4.5472	3.1937	5.1929
700	5.2398	4.5936	3.1946	5.1941
800	5.3351	4.6632	3.1962	5.1965
900	5.4033	4.7120	3.1980	5.1989
1000	5.4537	4.7476	3.1997	5.2014
1100	5.4918	4.7743	3.2015	5.2038
1200	5.5213	4.7948	3.2032	5.2063
1300	5.5446	4.8109	3.2050	5.2088
1400	5.5633	4.8238	3.2068	5.2113
1500	5.5786	4.8342	3.2086	5.2139
1600	5.5911	4.8427	3.2103	5.2164
1700	5.6016	4.8498	3.2121	5.2189
1800	5.6104	4.8558	3.2139	5.2214
1900	5.6179	4.8609	3.2158	5.2240

### 1.6.2.3 Piezoelectric coefficients of GaN

GaN is a piezoelectric material, a property which is defined by a piezoelectric stress matrix. The piezoelectric stress matrix is derived from a rank three piezoelectric tensor using a similar matrix notation method. The literature definition for the direct piezoelectric effect is that if a stress is applied to certain crystals they will develop an electric moment with a magnitude that is proportional to the stress applied [57]. This means that if a uniaxial tensile stress is applied along one of the axes of a piezoelectric crystal, then the polarization charge per unit area  $P$  is given by

$$P = e\sigma \quad (1.25)$$

where  $e$  is the piezoelectric modulus. As implied in (1.25), an equal and opposite strain will reverse the direction of polarization. The generalised form of the direct piezoelectric effect is

$$P_i = e_{ijk}\sigma_{jk} \quad (1.26)$$

where the piezoelectric moduli are  $e_{ijk}$  [57]. The reason why  $e$  is a rank three tensor is that  $P$  is a vector with three terms and  $\sigma$  is a 2<sup>nd</sup> rank tensor with nine terms: therefore  $e$  has to be a rank three tensor.

As with the elasticity, it is possible to quantify the direct piezoelectric effect in matrix notation. In the full tensor form,  $e_{ijk}$  would have to be written out in a cubic array; since it is symmetrical in  $j$  and  $k$  the terms shown in brackets below are eliminated.

Cubic Array Layers								
Layer 1 $i = 1$			Layer 2 $i = 2$			Layer 3 $i = 3$		
$e_{111}$	$e_{112}$	$e_{113}$	$e_{211}$	$e_{212}$	$e_{213}$	$e_{311}$	$e_{312}$	$e_{313}$
$(e_{121})$	$e_{122}$	$e_{123}$	$(e_{221})$	$e_{222}$	$e_{223}$	$(e_{321})$	$e_{322}$	$e_{323}$
$(e_{131})$	$(e_{132})$	$e_{133}$	$(e_{231})$	$(e_{232})$	$e_{233}$	$(e_{331})$	$(e_{332})$	$e_{333}$

**Figure 1.13** Schematic showing the reduction of piezoelectric tensor terms for the matrix notation in a skew symmetric material [57].

This removes nine coefficients from the tensor, indicated in figure 1.13, leaving 18 independent terms in the tensor and allows for the use of matrix notation. Although tensor notation is useful when doing transformations, it makes sense to calculate quantities such as stress or polarization using as few coefficients as possible: facilitating the use of matrix notation, which reduces the number of coefficients used to define a material to a minimum [57]. Matrix notation takes advantage of the symmetry along  $j$  and  $k$ , and defines the coefficients with new symbols. For example,  $e_{111}$  becomes  $e_{11}$  and  $e_{113}$  becomes  $\frac{1}{2}e_{15}$ . As a result of matrix notation, the tensor layers in figure 1.13 can be rewritten as follows [57] in figure 1.14.

Cubic Array Layers								
Layer 1 $i = 1$			Layer 2 $i = 2$			Layer 3 $i = 3$		
$e_{11}$	$\frac{1}{2}e_{16}$	$\frac{1}{2}e_{15}$	$e_{21}$	$\frac{1}{2}e_{26}$	$\frac{1}{2}e_{25}$	$e_{31}$	$\frac{1}{2}e_{36}$	$\frac{1}{2}e_{35}$
	$e_{12}$	$\frac{1}{2}e_{14}$		$e_{22}$	$\frac{1}{2}e_{24}$		$e_{32}$	$\frac{1}{2}e_{34}$
		$e_{13}$			$e_{23}$			$e_{33}$

**Figure 1.14** Diagram showing the piezoelectric stress coefficients in matrix notation [57].

In order to convert a coefficient from tensor to matrix notation the first suffix is kept the same, but the second and third suffixes in tensor notation are converted to a single

suffix in matrix notation. In matrix notation, the converted suffix runs from 1 to 6 rather than from 1 to 3. The relationships the tensor and matrix notations are displayed in figure 1.15.

<b>Tensor Notation</b>	11	22	33	23, 32	31, 13	12, 21
<b>Matrix Notation</b>	1	2	3	4	5	6

**Figure 1.15** Conversion chart for matrix and tensor notations [57].

The conversion chart in figure 1.15 can also be used for elastic stiffness or compliance, and stress or strain coefficients, as shown in (1.5) and (1.6). Using matrix notation, it is possible to rewrite the direct piezoelectric effect as shown in (1.27) [57].

$$P_i = e_{ij}\sigma_j \quad (i = 1,2,3; j = 1,\dots,6) \quad (1.27)$$

Using the matrix notation, the piezoelectric matrix  $e_{ij}$  can be arranged as a 3 x 6 matrix in the following form.

$$e_{ij} = \begin{pmatrix} e_{11} & e_{12} & e_{13} & e_{14} & e_{15} & e_{16} \\ e_{21} & e_{22} & e_{23} & e_{24} & e_{25} & e_{26} \\ e_{31} & e_{32} & e_{33} & e_{34} & e_{35} & e_{36} \end{pmatrix} \quad (1.28)$$

The actual terms for the piezoelectric stress matrix are determined by its elastic symmetry, with isotropic and some classes of cubic materials not showing any piezoelectric properties. The crystal lattice of a piezoelectric material needs order and some asymmetry; GaN is the perfect example with a hexagonal lattice type. Further diagrams of different piezoelectric matrix types can be found in reference [57].

As GaN is a wurtzite material, its piezoelectric stress matrix is class 6mm hexagonal [57]. Therefore, the piezoelectric behaviour of GaN can be described in the following stress matrix.

$$e_{ij} = \begin{pmatrix} 0 & 0 & 0 & 0 & e_{15} & 0 \\ 0 & 0 & 0 & e_{15} & 0 & 0 \\ e_{31} & e_{31} & e_{33} & 0 & 0 & 0 \end{pmatrix} \quad (1.29)$$

As the piezoelectric stress matrix (1.29) shows, there are three piezoelectric stress coefficients  $e_{31}$ ,  $e_{33}$  and  $e_{15}$ . There are various numeric values for these coefficients found in the literature.

**Table 1.6** Piezoelectric stress coefficients of GaN.

$e_{31}$	$e_{33}$	$e_{15}$	Ref
-0.22	0.44	-0.21	[72]
-0.33	0.65	-0.3	
-0.36	0.73	-0.33	
-0.49	1.00		
-0.33	0.67	-0.37	[73]
-0.36	1	-0.3	[74]
-0.22	0.44	-0.22	[28]
-0.33	0.70	0.29	Average

There are no agreed values for the piezoelectric stress coefficients in the literature, so a literature average value has been included for completeness. The reason for this is that measuring piezoelectric coefficients is very difficult due to the intrinsic properties of GaN. GaN polarises both spontaneously and piezoelectrically because it has both semiconducting and piezoelectric characteristics. Additionally, the presence of dopants in GaN or stress within the GaN crystal can also change the piezoelectric characteristics. The literature averages in table 1.6 show that the piezoelectric stress coefficients are approximately linked by the following two relations.

$$e_{33}/|e_{31}| \approx 2 \qquad e_{15} \approx |e_{31}| \quad (1.30)$$

The relationships shown in (1.30) indicate that the piezoelectric anisotropy inside the crystal is small. In addition to the piezoelectric coefficients, the dielectric constants are required to fulfil the piezoelectric constitutive relation (see sub-section 2.6.1) and these are  $\epsilon_x = \epsilon_y = 10.4 \epsilon_0$  and  $\epsilon_z = 9.5 \epsilon_0$  [2], where  $\epsilon_0$  is the permittivity of free space.

### ***1.6.3 Thermo-mechanical properties of (111) silicon***

In this project, silicon is orientated in the (111) plane; because it is the preferred crystallographic plane for growing CVD diamond [10] and is also suitable for c-plane GaN epitaxial growth [54]. (111) silicon has a high degree of thermal stability, with a small decrease in both Young's modulus and Poisson's ratio as the temperature increases [75]. The usual practice [58, 76] for determining the elastic material properties of (111) Si is to calculate its  $E$  and  $\nu$ , by transforming the stiffness coefficients of (100) oriented Si. The Si crystal lattice has a cubic structure and therefore has three independent stiffness coefficients.

The elastic moduli of (100) silicon and their temperature dependence are determined using the approach of Varshni [75], which is derived from the Einstein model for a solid and are given by

$$c_{ij} = c_{ij}^0 - u/(e^{t/T} - 1) \quad (1.31)$$

where  $u$  and  $t$  are fitting parameters and  $c_{ij}^0$  is the value for the elastic constant at 0K. The 0K elastic moduli values are based on the work in McSkimin [49], who measured the elastic moduli between 78 and 300K. The elastic moduli 0K values and fitting constants used in this work are shown in table 1.7. Further similar elastic (Young's) modulus data can be found in Cho [58], which is described and used in chapter 5.



**Table 1.7** 0K Elastic moduli and fitting constants of (100) silicon [75].

$c_{ij}$	$c_{ij}^0$ (GPa)	$u$ (GPa)	$t$ (K)
$c_{11}$	167.5	5.33	407.0
$c_{12}$	65.0	2.31	334.8
$c_{44}$	80.0	2.25	497.4

From (1.30) and table 1.7, it is possible to calculate the stiffness coefficients of Si between 100 and 1400K (-173 to 1127 °C), the entire temperature range used in this project. These are then converted to compliance coefficients using the formulae in (1.9 – 1.11). The temperature dependent compliance coefficients are presented in table 1.8.

**Table 1.8** The compliance coefficients of (100) Si.

Temp (K)	$s_{11}$ ( $10^{-12}$ Pa $^{-1}$ )	$s_{12}$ ( $10^{-12}$ Pa $^{-1}$ )	$s_{44}$ ( $10^{-12}$ Pa $^{-1}$ )
100	7.61016	-2.12395	0.124464
200	7.63269	-2.12609	0.124757
273	7.65932	-2.13021	0.125116
280	7.66212	-2.13067	0.125154
298	7.66945	-2.13189	0.125254
300	7.67028	-2.13203	0.125266
373	7.70179	-2.13743	0.1257
400	7.71397	-2.13956	0.125868
500	7.76077	-2.14785	0.126519
600	7.80955	-2.15655	0.127199
700	7.85978	-2.16553	0.127899
800	7.91121	-2.17468	0.128617
900	7.9637	-2.18398	0.129348
1000	8.01717	-2.19338	0.130092
1100	8.07158	-2.20288	0.130848
1200	8.12691	-2.21245	0.131615
1300	8.18313	-2.22208	0.132393
1400	8.24026	-2.23178	0.133181

As the silicon is (111) orientated, when used as a substrate material, the compliance coefficients  $s_{ij}$  of (100) Si in table 1.8 have to be transformed into  $E$  and  $\nu$  along the (111) plane. Using the compliance coefficients calculated from table 1.8 the Young's modulus ( $E$  (111)) and Poisson's ratio ( $\nu$  (111)) of silicon along the (111) plane is

calculated using a transformation in Cho [58] and Wortman and Evans [76]. Firstly, in order to correctly rotate the matrix, the directional cosines,  $l$ ,  $m$  and  $n$ , need to be determined. The directional cosines are determined from the rotation tensor and for a (111) orientation crystal are given in Cho [58] and they are;

$$\begin{pmatrix} l_1 & m_1 & n_1 \\ l_2 & m_2 & n_2 \\ l_3 & m_3 & n_3 \end{pmatrix} = \begin{pmatrix} \frac{\sin \phi}{\sqrt{6}} + \frac{\cos \phi}{\sqrt{2}} & \frac{\sin \phi}{\sqrt{6}} - \frac{\cos \phi}{\sqrt{2}} & \frac{-2 \sin \phi}{\sqrt{6}} \\ -\frac{\sin \phi}{\sqrt{2}} + \frac{\cos \phi}{\sqrt{6}} & \frac{\sin \phi}{\sqrt{2}} + \frac{\cos \phi}{\sqrt{6}} & \frac{-2 \cos \phi}{\sqrt{6}} \\ 1 & 1 & 1 \end{pmatrix} \quad (1.32)$$

Where  $\phi$  is the angle of counter clockwise rotation or angle of misalignment. When a material is perfectly aligned on the (111) plane where,  $\phi = 0$ . Therefore, the direction cosines become:

$$\begin{pmatrix} l_1 & m_1 & n_1 \\ l_2 & m_2 & n_2 \\ l_3 & m_3 & n_3 \end{pmatrix} = \begin{pmatrix} \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} & 0 \\ \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} & -\frac{2}{\sqrt{6}} \\ 1 & 1 & 1 \end{pmatrix} \quad (1.33)$$

Equation (1.34) is the direction cosine tensor and can be converted into a 6x6 matrix, with the following form [58].

$$T_{\alpha\beta} = \begin{pmatrix} l_1^2 & m_1^2 & n_1^2 & 2l_1n_1 & 2m_1n_1 & 2l_1m_1 \\ l_2^2 & m_2^2 & n_2^2 & 2l_2n_2 & 2m_2n_2 & 2l_2m_2 \\ l_3^2 & m_3^2 & n_3^2 & 2l_3n_3 & 2m_3n_3 & 2l_3m_3 \\ l_1l_3 & m_1m_3 & n_1n_3 & l_1n_3 + l_3n_1 & m_1n_3 + m_3n_1 & l_1m_3 + l_3m_1 \\ l_2l_3 & m_2m_3 & n_2n_3 & l_2n_3 + l_3n_2 & m_2n_3 + m_3n_2 & l_2m_3 + l_3m_2 \\ l_1l_2 & m_1m_2 & n_1n_2 & l_1n_2 + l_2n_1 & m_1n_2 + m_2n_1 & l_1m_2 + l_2m_1 \end{pmatrix} \quad (1.34)$$

Using the stress-strain relationship in a rotated system from [58]

$$E' = (T_{\alpha\beta}^t)^{-1} s_{ij} T_{\alpha\beta}^{-1} \sigma' \quad (1.35)$$

It is possible to derive the formulae for the  $E$  (111) and  $\nu$  (111) of Si, and these formulae are written below.

$$E(111) = \frac{4}{2s_{11} + 2s_{12} + s_{44}} \quad (1.36)$$

$$\nu(111) = \frac{2s_{11} + 10s_{12} - s_{44}}{6s_{11} + 6s_{12} + 3s_{44}} \quad (1.37)$$

Although (111) silicon has an independent shear modulus, it is usually treated as an isotropic material [58]. (111) silicon has a non-zero  $s_{14}$  coefficient, which indicates that it has a triclinic lattice. Initial exploration of this problem has indicated that the error caused by assuming that (111) silicon is isotropic is negligible. Therefore, it has been assumed that (111) silicon has isotropic mechanical properties. The temperature dependent Young's moduli and Poisson's ratios calculated using equations (1.36) and (1.37) and used in this work are presented in table 1.9 for (111) silicon alongside its temperature dependent CTEs [50].

**Table 1.9** Structural and thermal properties of silicon used in the model [49-51, 58, 75, 76].

Temp (°C)	$E$ (111) (GPa)	$\nu$ (111)	$\alpha$ ( $10^{-6}\text{K}^{-1}$ )
-173	170.3	0.26	-0.509
-73	169.8	0.26	1.453
7	169.2	0.26	2.392
27	169.0	0.26	2.568
127	168.1	0.26	3.212
227	167.1	0.26	3.594
327	166.0	0.26	3.831
427	165.0	0.26	3.987
527	163.9	0.26	4.099
627	162.8	0.26	4.185
727	161.8	0.26	4.264
827	160.7	0.26	4.322
927	159.6	0.25	4.380
1027	158.5	0.25	4.438
1127	157.4	0.25	4.496
1227	156.3	0.25	4.554

The data in table 1.9 shows that (111) silicon has a high degree of thermal stability, with only a small decrease in both  $E$  and  $\nu$  as the temperature increases. The Poisson's ratio,  $\nu$ , decreases from 0.26 at  $-173^\circ\text{C}$  to 0.25 at  $1227^\circ\text{C}$  and also stays stable with respect to temperature.

#### ***1.6.4 Thermo-mechanical properties of polycrystalline CVD diamond***

Unlike GaN or Si described earlier, polycrystalline diamond (PD) consists of grains of nominally randomly orientated diamond material, with little variation in the elastic modulus along any crystalline plane. Sources [10] and [77] report relatively low elastic coefficients for polycrystalline diamond due to imperfections and impurities. Furthermore, the experimental data of Szuecs *et al* [78] shows that the Young's modulus of CVD polycrystalline diamond is not affected by the grain size if the defect density is constant. Modern growth techniques now used to grow polycrystalline diamond produce significantly reduced defect densities and its Young's modulus can approach that of optical grade diamonds [78].

The properties used for polycrystalline diamond used in this thesis are based on measurements obtained from Element Six [79, 80] and the literature [51, 78, 80-82]. The method used assumes that polycrystalline diamond behaves approximately similar to monocrystalline diamond until room temperature, from which the material will go through a faster than expected thermal degradation. It has been assumed that the material is perfectly isotropic, because it has a polycrystalline structure consisting of randomly orientated crystals. The values for the elastic moduli of diamond at room temperature were taken from McSkimin and Andreatch [81] a commonly cited source and are quoted in table 1.10.

**Table 1.10** Elastic moduli of diamond at room temperature (25°C) [81].

Modulus	(GPa)
$c_{11}$	1079
$c_{12}$	124
$c_{44}$	578

The Young's modulus and Poisson's ratio at room temperature (25°C) for diamond were calculated using the elastic moduli values in table 1.10 and standard formulae (1.9 – 1.14) [81] to be  $E_{RT} = 1050$  GPa and  $\nu = 0.1$ . However, it has been found that the Young's modulus of CVD diamond degrades faster with respect to temperature than predicted in McSkimin and Andreatch [81] due to the presence of contaminants, such as graphite and other organic material, and grain boundaries within the material. It has been shown experimentally by Szuecs *et al* [78] that the variation of Young's modulus ( $E$ ) with temperature,  $T$ , of CVD diamond undergoes a linear regression of the form shown in (1.38).

$$E = E_{RT} [1 + c_T (T - 25)] \quad (1.38)$$

Where the temperature coefficient,  $c_T$ , has an average value of  $-1.027 \times 10^{-4} \text{ K}^{-1}$  in the case of CVD diamond. Using a room temperature Young's modulus,  $E_{RT}$  [49],

equation (1.37), and the average value for  $c_T$  from [78]; the temperature dependent Young's moduli for polycrystalline CVD diamond were calculated and are shown in table 1.11.

**Table 1.11** Structural and thermal properties of CVD diamond used in the model [51, 78, 80-82] .

Temp (°C)	$E$ (GPa)	$\nu$	$\alpha$ ( $10^{-6} \text{ K}^{-1}$ )
-100	1062	0.1	0.4
0	1052	0.1	0.8
20	1050	0.1	1
25	1050	0.1	1
50	1048	0.1	1.4
100	1043	0.1	1.7
200	1034	0.1	2.3
300	1025	0.1	3.1
400	1015	0.1	3.7
500	1006	0.1	4.0
600	997	0.1	4.3
700	988	0.1	4.5
800	978	0.1	4.6
900	969	0.1	4.8
1000	960	0.1	4.9

The Poisson's ratio is assumed constant, at  $\nu = 0.1$ , between -100 and 1000°C, to an accuracy of one significant figure. This is a reasonable assumption because the material still experiences a relatively small amount of thermal degradation of elastic properties, from 1062 to 960 GPa between -100 and 1000 °C.

### ***1.6.5 Thermo-mechanical properties of sapphire***

Sapphire will be used as a substrate material in this project because it has good thermal properties and has a crystal lattice that is compatible with GaN for epitaxial growth. Throughout the thesis, the sapphire material properties will always be (0001) rotated; which is the standard rotation used for GaN growth. Sapphire is already commonly used as a substrate material with GaN for blue LEDs [83]. Sapphire has a melting point of 2053°C and thermal conductivity of 42 W / (m.K) at room

temperature [84]. However, its thermal conductivity is not as good as diamond: meaning that it will not be as efficient as a heat sink for high power applications.

Nominally, sapphire has a trigonal crystal structure (1.24) with six independent elastic coefficients. Measurements of these constants at 27°C was undertaken by Bernstein [85] and others [86, 87], and the results in this paper are shown in table 1.12.

**Table 1.12** Elastic constants for sapphire measured by various sources in [85].

Stiffness Coefficient (GPa)	Bernstein [85]		Wachtman et al [86]	Mayer and Hiedemann [87, 88]
	Pulse-echo	CW resonance		
c <sub>11</sub>	490.2	492.0	496	496.8
c <sub>33</sub>	490.2	492.0	502	498.1
c <sub>44</sub>	145.4	146.8	141	147.4
c <sub>12</sub>	165.4	168.4	135	163.6
c <sub>13</sub>	113.0	116.4	117	110.9
c <sub>14</sub>	-23.2	-23.4	-23	-23.5

Further measurements of the room temperature elastic constants of sapphire have been taken over the years and are included in table 1.13.

**Table 1.13** Further literature values for the room temperature elastic constants of sapphire.

Stiffness Coefficient (GPa)	Gladden <i>et al</i> [88, 89]		Gieske and Barsche [88, 90, 91]	Literature Average
	Experimental	Theoretical		
c <sub>11</sub>	497.5	495	497.6	495.0
c <sub>33</sub>	503.3	486	501.8	496.2
c <sub>44</sub>	147.4	148	147.2	146.2
c <sub>12</sub>	162.7	171	162.6	165.6
c <sub>13</sub>	115.5	130	117.2	115.0
c <sub>14</sub>	22.5	20	22.9 *	22.6

\* Correction in [91] as earlier papers presumed the sign was negative because it was not possible to measure the sign at the time.

The literature values for the elasticity coefficients of sapphire in tables 1.12 and 1.13 are very consistent; this means that it is reasonable to take an average of all these

values, as shown in the final column of table 1.13. For the literature average, it has been assumed that  $c_{14}$  has a positive sign because it is the result from more recent measurements.

Tables 1.12 and 1.13 show that  $c_{14}$  is much smaller than the other elastic coefficients. This is because  $c_{14}$  is a correction that results from sapphire's rhomboidal lattice structure. By assuming that sapphire is transversely isotropic, its engineering constants  $E$ ,  $G$  and  $\nu$  can be determined using the equations (1.16 – 1.23). Therefore, the room temperature values for the engineering constants of sapphire, based on the literature average, are as follows.

**Table 1.14** Values for the engineering constants of sapphire at ~ 300K.

Constant	Value based on literature average [84-90]
$E_x$	427 GPa
$E_z$	456 GPa
$G_{xy}$	165 GPa
$G_{yz}$	146 GPa
$\nu_{xy}$	0.30
$\nu_{yz}$	0.17

(Directions : 11 = x, 22 = y, 33 = z, 44 = xy, 55 = xz, 66 = yz)

However, unlike the other materials in this review, it has not so far been possible to find significant high temperature values for the elasticity of sapphire. Although a paper by Wachtman *et al* [92] shows that the Young's modulus of sapphire degrades as temperature increases, it does not include absolute values. However, this degradation is expected to be small in line with the expected behaviour of GaN, Si and PD.

In common with the other materials in this project, sapphire has non-linear CTEs. The CTEs of sapphire are directional dependent, like GaN, because its lattice structure is approximately hexagonal. In the literature, the CTEs of sapphire have been measured parallel and perpendicular to its c-axis.



**Table 1.15** Coefficients of thermal expansion for (0001) orientated sapphire [47].

Temp (°C)	$\alpha$ parallel to c-axis ( $10^{-6} \text{ }^\circ\text{C}^{-1}$ )	$\alpha$ perpendicular to c-axis ( $10^{-6} \text{ }^\circ\text{C}^{-1}$ )
-273	1.95	1.65
-173	3.01	2.55
-73	4.39	3.75
27	5.31	4.78
127	6.26	5.51
227	6.86	6.10
327	7.31	6.52
427	7.68	6.88
527	7.96	7.15
627	8.19	7.35
727	8.38	7.53
827	8.52	7.67
927	8.65	7.80
1027	8.75	7.88
1127	8.84	7.96

Table 1.15 shows that sapphire thermally expands less along the  $x$  and  $y$  axes; this is expected because  $E_x$  is smaller than  $E_z$ . The data in table 1.15 also shows that sapphire has the largest CTEs out of all the materials used in this project, meaning that GaN-based wafer systems with a sapphire substrate will be convex and the GaN will have a compressive stress profile.

### ***1.6.6 Thermal Conductivity of the Materials used in the PhD***

Although thermal conductivity is not directly covered in this project, it is important to know the relative thermal conductivities of all of the potential materials used in this project because the sensors are to be eventually used at temperatures approaching 600°C. Therefore, in order to select an appropriate substrate material for a GaN sensor or GaN power HEMT, the thermal conductivities of the available substrates (PD, Si, sapphire) and III-V nitride materials (GaN, AlN) need to be known. Table 1.16 contains details of the thermal conductivities of PD, Si, sapphire, GaN and AlN.

**Table 1.16** Thermal conductivities of PD, Si, sapphire, GaN and AlN around room temperature

Material	Thermal Conductivity (W/mK)	Reference
PD	2270 at 20°C	[80, 93]
Si	10 to 20 at 25°C	[94]
Sapphire	42 at 25°C	[84]
AlN	200 at 25°C	[18]
GaN	130 at 25°C	[18]
SiC	387 at 25°C	[9]

### 1.7 Aims of the PhD

After a review of the literature and taking into account the targets of the MORGaN project, this PhD project has the following aims.

- i. Use finite element (FE) modelling to predict behaviour of Si (111)/polycrystalline diamond (PD) composite substrates. Theoretically, these substrates have the advantages of high stiffness, high thermal conductivity, increased strength and compatibility between GaN grown by MOCVD and (111) Si. However, there are some serious thermal mismatch issues in processing Si (111)/PD wafers with a thin (~2µm) Si layer; a requirement to maintain a high thermal conductivity. These issues will be shown using the model and experimental data, and potential solutions will be explored using the FE analysis and validated with experimental data.
- ii. Undertake measurements of the stiffness of GaN, Si and sapphire from room temperature to ~500°C by DMTA and compare with the literature. Experimental high temperature properties of all of these materials are sparse and will be useful for FE modelling and the operation of GaN devices at elevated temperatures.
- iii. Develop a GaN-based strain sensor, utilising the piezoelectric effect. In this PhD two approaches will be taken, a lower risk top-down approach using a GaN/sapphire membrane sensor using multiple HEMTs as sensors and higher risk bottom-up approach where the sensors are grown by ELOG. The GaN/sapphire membrane sensor will be designed to work in high pressure (50 bar) and temperature (~400°C) environments. The GaN membrane sensor is a potential

application for the Si/PD composite substrate in the future. The ELOG sensor will be fabricated from low defect material, which should offer superior electrical and mechanical performance. This PhD will report on all of the progress made in developing a sensor with these approaches.

**The following chapter will review and discuss the experimental methods employed in the PhD.**

## CHAPTER 2: EXPERIMENTAL METHODS

### 2.1 Introduction

This chapter will describe the experimental methods used to produce the results in this thesis. The experimental methods in this chapter will be separated into multiple sections, denoted in the following points.

- Section 2.2 will describe the methods used for measuring the surface profile of samples produced in this project. The two key methods used in this PhD are the Veeco Dektak and the Proscan 2000 profilometer. As chapters 3, 4 and 6 will show later in this thesis, accurate surface scans are required for determining the properties of novel substrate materials (chapters 3 and 4) and measuring the topography of the GaN structures that are produced by ELOG (chapter 6).
- Section 2.3 concerns methods for measuring the stiffness (Young's modulus) of materials with respect to temperature, namely dynamic mechanical thermal analysis (DMTA) and impulse excitation, which were used in this project to achieve these measurements. These measurements are required to determine the suitability of GaN as a base material for high temperature sensors. Chapter 5 contains experimental measurements using these methods.
- There will be a description of micro-Raman analysis, a direct method for measuring stress, and scanning electron microscopy (SEM) in section 2.4. The micro-Raman measurements were an extremely useful tool for validating the finite element (FE) models developed in this thesis and improving our understanding of the stress state in the materials used in this PhD. The micro-Raman analysis in this project was done at the Slovakian Technical University (STU), where the equipment is based. Chapters 3 and 4 contain analysis based on micro-Raman measurements. SEM is used in chapters 3, 4 and 6 for the imaging, characterisation and analysis of samples.

- There will also be a discussion of the nanofabrication methods in section 2.5. The nanofabrication methods described will be photolithography, plasma etching, electron beam evaporation and plasma-enhanced chemical vapour deposition (PECVD). These methods were used because they were readily available in the university nanofabrication centre. All of the nanofabrication methods described in this section are required for the creation of GaN-based sensors and sensing templates described in chapters 6 and 7 of this thesis.
- As well as the experimental methods there will a description of the theory of finite element analysis in section 2.6. ANSYS was the particular finite element package used in this thesis. Finite element models are very useful for determining the underlying thermo-mechanical response of the (111) Si/polycrystalline diamond (PD) substrates developed as part of this PhD, shown in chapters 3 and 4.

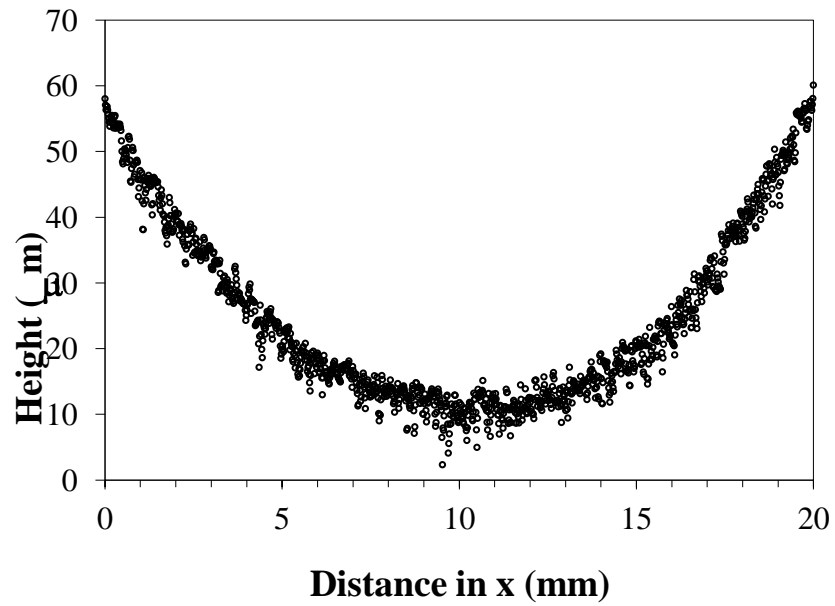
## **2.2 Experimental measurements of wafer bow**

Two different experimental methods for measuring wafer bow were used in this PhD, the Dektak and the Proscan 2000 profilometer; with each machine having positive and negative aspects. The Proscan and Dektak can both be used to directly measure the bow of a wafer, with the Proscan using a white light or laser source to measure height changes in a contactless manner and the Dektak doing the same with a diamond scribe that is in contact with the surface being characterised. The Proscan is able to scan the surface topography of a full 2 inch wafer in less than two hours, but the resolution is poor in comparison ( $\sim 0.1\mu\text{m}$ ). The Dektak can quickly scan along the surface of an entire sample, is high resolution and accurate. However, as the Dektak measures the surface directly using a diamond scribe, it can leave the surface slightly damaged. The Dektak can also only take one line scan at a time, making it impractical for producing topographical images. The experimental set up of both pieces of equipment is partially automated and a computer records the measurements.

### ***2.2.1 Experimental method and initial results for the Proscan 2000 profilometer***

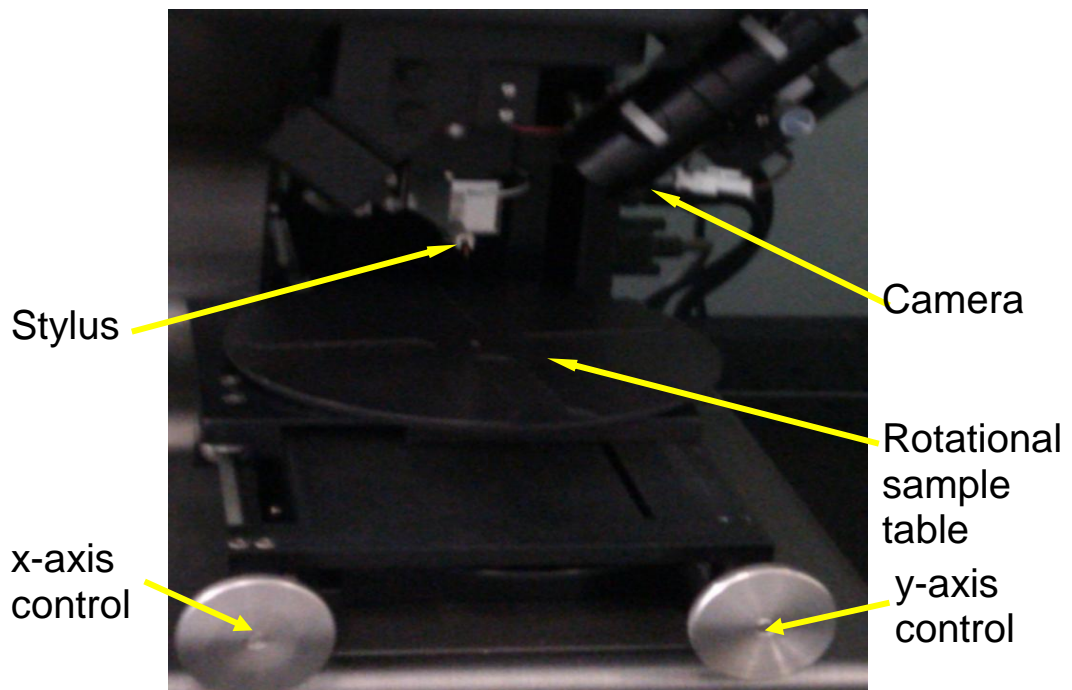
The profilometer height measurement emits white light with a specific chromatic aberration and the colour of the reflected light can be used to measure the surface topography of a bowed wafer, as shown in chapters 3 and 4. White light consists of light over the full visible spectrum and this can be used to measure height changes, with different colours being detected at different heights. The probe used to scan the wafer has a range of 2 mm, which is more than adequate for scanning the entire wafer depth; although the height resolution is low ( $\sim 0.1\mu\text{m}$ ) in comparison to accuracy of the Dektak ( $\sim 1\text{ nm}$ ). Despite the poorer resolution, the profilometer directly measures height changes over an entire wafer, rather than just a line scan, and the only source of error is the resolution limit of the probe.

Since the Proscan uses reflected light to measure height it is most effectively used on darker samples, such as GaN/Si and Si/PD wafers, rather than translucent samples such as GaN/sapphire wafers, although translucent samples can be scanned at a slower rate. The Proscan works more effectively for dark materials because the majority of the light does not pass through the sample, hence the reason for running tests using the Si side of Si/PD samples. The bow of a wafer can be measured across the diameter of the sample. The probe scans at fixed periodic intervals across the profile of the wafer; this interval is typically set to 0.1 mm, but can be reduced to  $1\mu\text{m}$ , the practical resolution limit of the system, before the scan starts. Figure 2.1 contains a line scan along an axis of a Si/PD wafer. This shows that the scan is almost an exact parabola, suggesting that the bow of this composite substrate is proportional to the radius squared. In this case, it means that the bow curve can be approximated as a quadratic equation. This has processing implications and the topic of the bow of these composite substrates will be discussed in chapter 3.



**Figure 2.1** Line scan of a Si/PD wafer using Proscan 2000 profilometer.

*2.2.2 Scanning samples with the Veeco Dektak 4.1 to determine the height of MEMS devices and wafer curvature*



**Figure 2.2** Image of the Dektak used for profile measurements in this PhD.

The Dektak is a surface profilometer that uses a diamond stylus to measure surface topography of a planar surface, such as a silicon wafer. Although designed primarily for the silicon chip industry, the Dektak can also be used on GaN, PD and sapphire surfaces. The stylus is a semi manual instrument that can be programmed to scan horizontally across a pre-defined part of a sample. The sample is aligned into the appropriate region manually using dials and fine motors. Once the sample is aligned the stylus will then be brought down by motors until it touches the sample and then it will scan along the sample, measuring height changes in the surface topography. An image of the Dektak is shown in figure 2.2.

This approach yields very high resolution results, the maximum resolvable distance is 20 nm, but the diamond stylus leaves minor damage on the surface and a single line scan across an entire 100 mm diameter wafer is time consuming. Therefore the Dektak is most useful for scanning small regions, such as the topography of a MEMS device. This means that the Dektak can be used to scan the GaN epitaxial layer overgrowth (ELOG) structures, shown in chapter 6, fabricated as part of this PhD.

## **2.3 Modulus measurements of semiconducting materials**

In this thesis, two possible methods for the measurement of the Young's modulus of semiconducting materials were explored, dynamic mechanical thermal analysis (DMTA) and impulse excitation. Both impulse excitation and DMTA have the ability to measure the modulus change with respect to temperature, so it is possible to directly compare the effectiveness of both methods. The results obtained using these methods will be shown in chapter 5, after a brief discussion of the experimental methods in this section.

### ***2.3.1 Dynamic mechanical thermal analysis of semiconductor wafers***

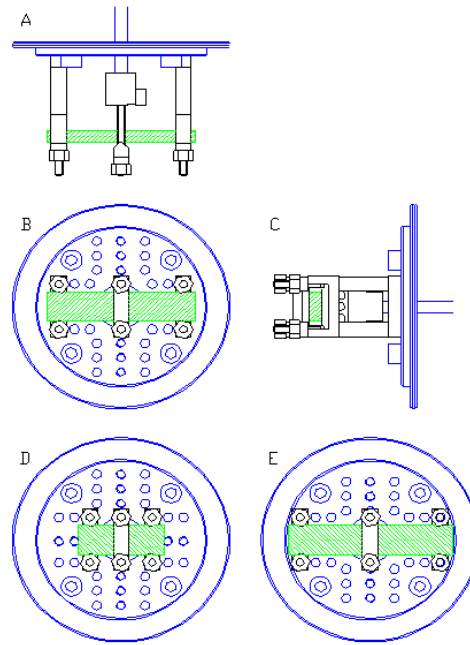
Dynamic mechanical thermal analysis (DMTA), also known as dynamic mechanic analysis (DMA) or thermal mechanical analysis (TMA), is a technique used to measure the properties of a material through the cyclical application of small



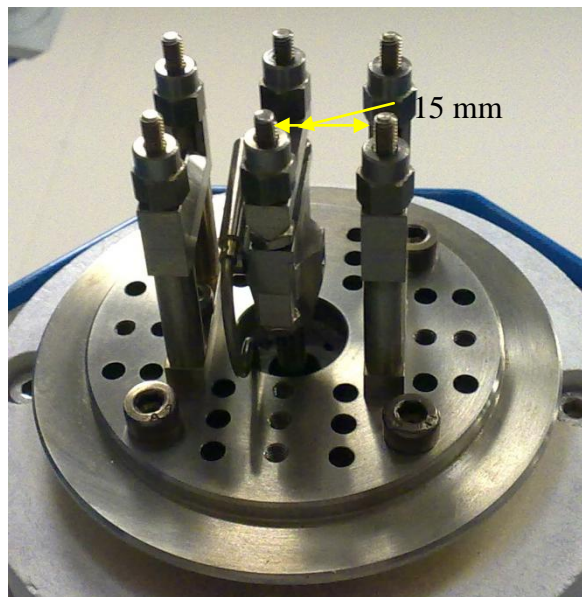
deformations [95]. Amongst the properties that can be measured using DMTA is the elastic modulus of a material with respect to temperature. DMTA is used extensively with polymers, but is also suitable for use with stiffer semiconducting materials used in this product including GaN, silicon and sapphire as shown by the work in chapter 5. The machines used to perform DMTA are also described using the same term.

DMTA applies small cyclical deformations to a sample with a known geometry. The geometry used is dependent on the clamp arrangement used, with different clamp arrangements being more suitable for materials with certain stiffness. The different geometric arrangements include single cantilever, dual cantilever, tension, shear and three-point bend [96]. The tension clamp arrangement is best for materials with a relatively low Young's modulus, like most polymers. The single and dual cantilever arrangements are suitable for most materials, but they tend to produce inaccurate results because they are very difficult to set up properly and use a large number of clamps. The cantilever arrangements are not strictly suitable for stiff samples due to the high risk of sample damage. Unfortunately, the shear clamp arrangement cannot be used with stiff materials because for similar reasons.

For this research, the three-point bend geometry has been used exclusively because it is most suitable for use with high stiffness materials such as GaN and Si [96]. However, as the three-point bend set up only constrains the sample under the central tower, it is difficult to set up properly as the samples are prone to slippage during testing. One of the ways to reduce slippage and improve the accuracy of the results is to apply a small static force to the sample, but this increases the risk of fracturing the sample during the experiment. A schematic for the three point bend clamp arrangement is shown in figure 2.3.



(a)



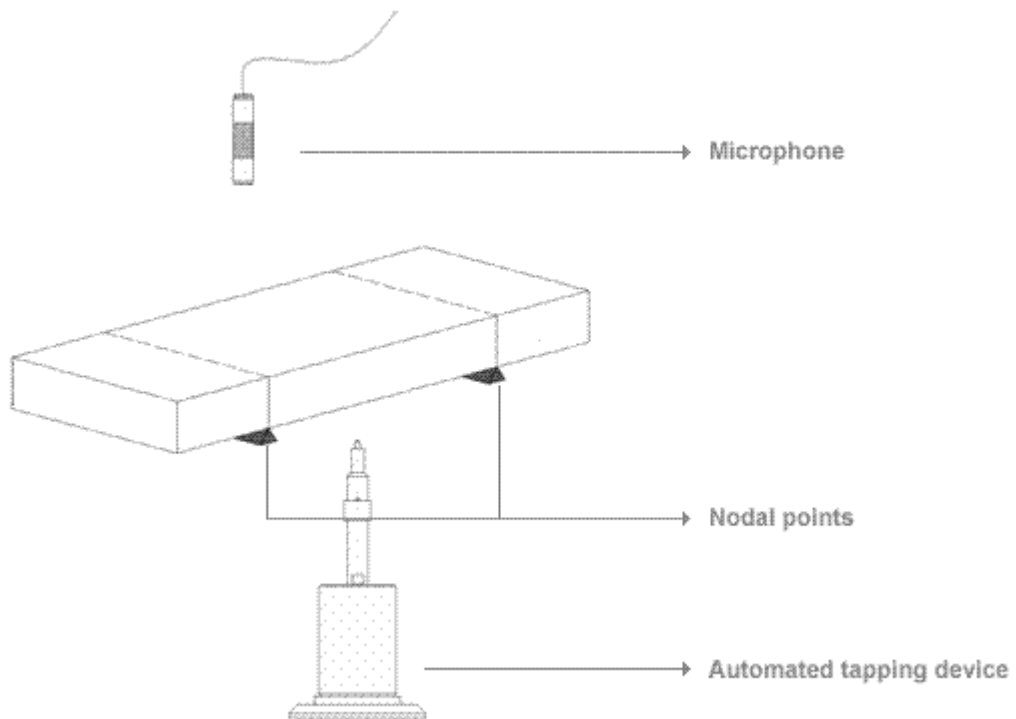
(b)

**Figure 2.3** Schematic of the DMTA in three-point bending mode. (a) Diagram of three-point bending mode from the DMTA instruction manual [96]. B, D and E are top-down views of the possible clamp positions. C is a side-view of the three-point bending clamping and A shows a reverse angle of the clamping arrangement. (b) Photograph of the three-point bend experimental setup.

In order to accurately FE model the stress profiles of GaN/substrate wafers, detailed temperature dependent material properties are required. The most important initial

properties for modelling are the elastic moduli and coefficients of thermal expansion (CTEs) of a material. The temperature dependent CTEs of GaN and the majority of substrate materials are complete in the literature, but there is a lack of data in the literature for the high temperature elastic moduli of GaN. These will be measured in three point bending mode using the DMTA, using different orientation GaN samples. However, in order to accurately measure elastic moduli of materials in the DMTA it needs to be correctly calibrated. DMTA calibration and measurements will be discussed in chapter 5.

### 2.3.2 Impulse excitation



**Figure 2.4** Experimental schematic of the impulse excitation technique [97].

In addition to DMTA, impulse excitation offers another simple method for measuring the modulus of materials. A schematic of the impulse excitation experimental set up is shown in figure 2.4. Once a material with well-defined dimensions is obtained, it is struck with a tapping device, causing the material to vibrate. One of the advantages of the tapping device is that it can be automated. These vibrations are detected by a

sensitive microphone sitting close to the sample; these microphones are inexpensive and readily available. By recording the vibrations, the resonant frequency of the material can be calculated using specialist software [97].

These calculations are done in this case using the RFDA (Resonant Frequency and Damping Analysis) software, produced by IMCE, on a computer connected to the microphone [97]. The RFDA software firstly applies a fast Fourier transformation to the vibration's signal, from which an initial estimate of the resonant frequency can be calculated, and the vibration can be reinterpreted as a mathematical equation [97]. This analysis is an iterative process, with the equation being adjusted until it resembles the measured vibration as closely as possible [97]. In doing this more detailed analysis, rather than just a fast-Fourier transform, the software determines the resonant frequency to a high degree of accuracy [97]. For a sample of known mass and dimensions, it is possible to calculate the elastic properties from the resonant frequency. Impulse excitation was used for additional measurements because facilities at IMCE allow testing up to 1000°C while the DMTA at University of Bath is limited to 600°C.

## **2.4 Analysis Methods**

### ***2.4.1 Micro-Raman***

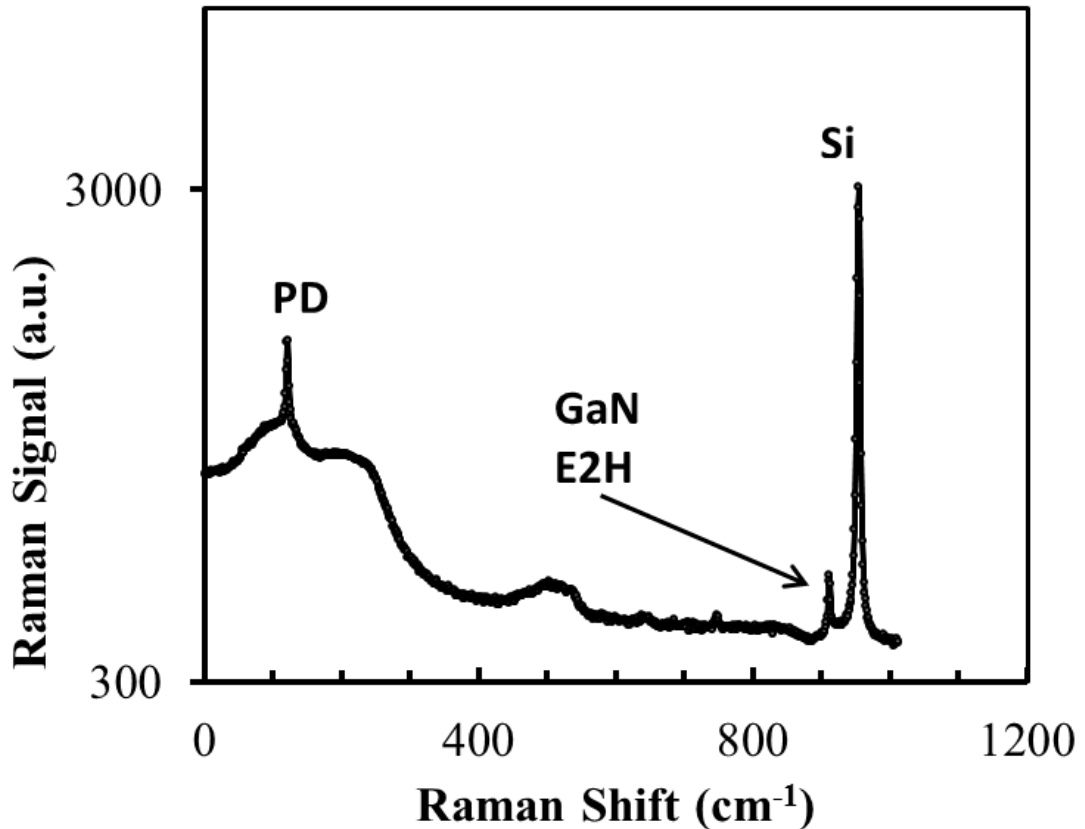
The accurate characterisation of stress in micro-electro-mechanical systems (MEMS) structures and semiconducting wafers is an important aspect of this project. Achieving this measurement is made difficult by the small size of the structures created. One method for measuring these stresses at a fine resolution is using micro-Raman spectroscopy, which offers a high accuracy method for measuring stress up to a 1  $\mu\text{m}$  resolution. All micro-Raman measurements reported in this thesis were undertaken using a system based at the Slovak Technical University (STU) in Bratislava, who performed these measurements on our behalf as partners of the MORGaN consortium. The micro-Raman spectrometer used at STU consists of a He-Ne laser beam (wavelength: 632.8nm), which scans across the cross-section of a cleaved sample. The laser beam is focused to a 1  $\mu\text{m}$  resolution in order to resolve the

scattered photons from different layers. These scattered photons are then focused and their spectra are collected with a Horiba-Dilor LabRam spectrometer.

#### ***2.4.2 Basic concepts of micro-Raman spectroscopy***

Micro-Raman spectrometers utilise the Raman Effect [98] to take measurements of the spectra of photons that are scattered when they come into contact with the nucleus of an atom. In a Raman spectroscopy experiment a monochromatic light source, in this case a 632.8 nm He-Ne laser, is aimed at the material. A monochromatic light source consists of photons of equal wavelength and these interact with the material as they strike its atoms in a crystal lattice. There are three methods in which a photon can interact with an atom and these are through reflectance, absorption or by scattering.

Photonic scattering can be either elastic or inelastic, which is known as Rayleigh scattering and results from the Raman Effect. Only a ratio of  $\sim 1:10^6$  photons interacts with an atom through Rayleigh scattering and these photons have their wavelengths shifted by their interaction with matter. This interaction causes the photons to lose energy to surrounding electrons causing them to change energy state, resulting in a Stokes-Raman wavelength shift [98]. This shift in wavelength varies according to which atomic element is struck meaning that different materials can be detected according to their respective wavelength shift. The shifts in wavelength are collated in spectra, using a spectrometer. A typical micro-Raman spectra of the materials in a GaN/Si/PD sample is shown in figure 2.5, showing the shift in wavelength that occurs when a photon is inelastically scattered off these materials.

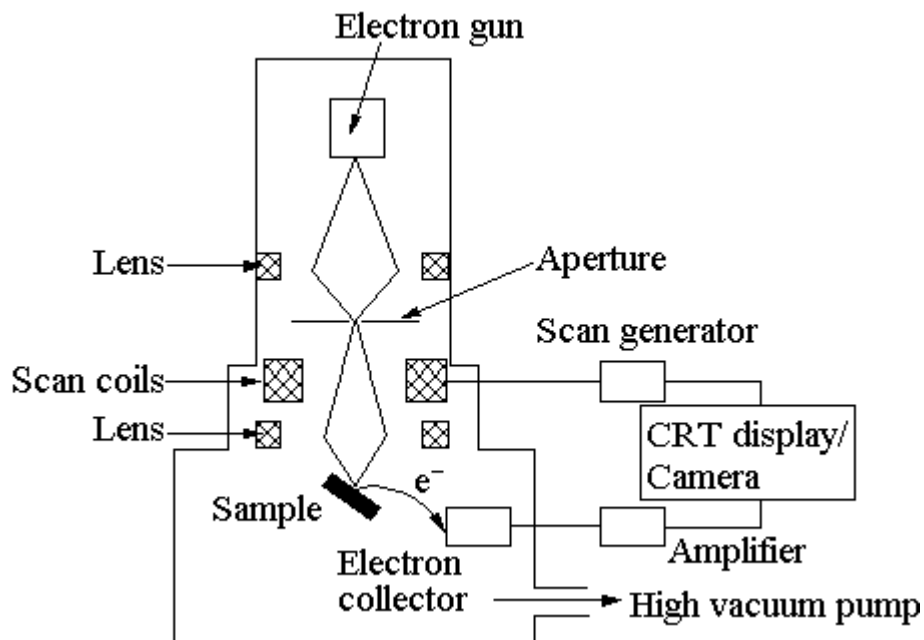


**Figure 2.5** Micro-Raman spectra of a Si/PD/GaN sample cross-section (see appendix A.4)

The strain in materials causes additional small perturbations in the Raman spectra, that are caused by small changes in lattice vibrations and these can be quantified if the Raman experiment has sufficient resolution. It is possible to improve the resolution by focussing the laser beam to a spot size of  $\sim 1 \mu\text{m}$ . By reducing the spot size, a smaller area of the sample is scanned and this helps gain a detailed image of the stress in a material. This additional resolution is one of the differences between a Raman and micro-Raman experiment. At these high resolutions, micro-Raman spectroscopy can detect changes in the strain of semiconducting crystalline materials measured in strain-sensitive lattice vibrations. Therefore, micro-Raman spectroscopy can be used to build a detailed picture of the stress in semiconducting materials and is a very valuable tool in achieving the targets set out in this PhD.

### 2.4.3 Scanning Electron Microscopy (SEM)

Scanning electron microscopy is used to image, characterise and analyse samples with characteristics in the micro- and nano-scale. In this project SEM used to measure the thicknesses of layers of different materials, the dimensions of samples and for physical images indicating the quality of sample's surfaces. A scanning electron microscope basically works by scanning a sample with a finely focussed (up to ~1 nm) beam of electrons. These electrons interact with any electrons on the sample to produce the image, meaning that it is important that the sample has a highly conductive surface for the best images. A thin layer of gold is typically sputtered onto poorly conductive surfaces to overcome this problem. There are three different types of intra-electron interaction that can be detected by the SEM and each interaction produces its own image. These interactions are secondary electrons, backscattered electrons and characteristic x-rays. In this project all the images were taken using secondary electrons, which is the most commonly used imaging process. Figure 2.SEM contains a schematic diagram of a SEM.



**Figure 2.SEM.** A schematic diagram of a scanning electron microscope [99].

Firstly, before the electron beam commences, the SEM chamber has to be evacuated and pumped down until a vacuum of sufficient quality is formed. The tungsten electron gun is then switched on and is filtered through a series of lenses to ensure that the beam is finely focussed and can take good quality high resolution images. High quality SEMs are capable of an imaging resolution of 1 nm. Once the beam of electrons strikes the sample, it can be tilted and moved into such a position using motors to allow the correct region of the sample to be imaged using the appropriate detector.

## **2.5 Nanofabrication methods**

The creation of GaN-based sensors requires extensive use of nanofabrication methods. All the nanofabrication methods described in this section were used in this PhD because the appropriate equipment resided in the University of Bath nanofabrication centre, meaning it was readily available to use and there were staff available for equipment training. The key nanofabrication methods used in this thesis are described in this section which are photolithography, ICP plasma etching, plasma enhanced chemical vapour deposition (PECVD) and electron beam evaporation. Photolithography is used to pattern samples before they are processed by wet or dry etching. An ICP plasma etcher is used to undertake the dry plasma etching; plasmas are used to etch through layers of material, such as  $\text{SiN}_x$ ,  $\text{SiO}_2$  and GaN. PECVD is the preferred method for deposition of  $\text{SiO}_2$  and  $\text{SiN}_x$ , which are used for compliant layers and masks in this project. Finally, electron beam evaporation is a good method for depositing metals such as Ti, Ni and Au onto a sample; these metals can be used as electrical contacts or masks in this project. Although these methods are being used for research and development purposes in this thesis, it should be possible to use very similar methods industrially in device production once the sensing technologies described in this thesis have been developed.



### ***2.5.1 Photolithography***

Photolithography is the process used to pattern semiconductor devices before fabrication. The advantage of using photolithography to pattern a sample is that it is a top-down process that can be used to pattern large numbers of devices at low cost, rather than focused ion beam (FIB) or electron beam lithography (EBL) methods, which are slow, expensive processes that can only reasonably be expected to pattern only a few devices. The basic photolithography process contains multiple steps and is described in the following points.

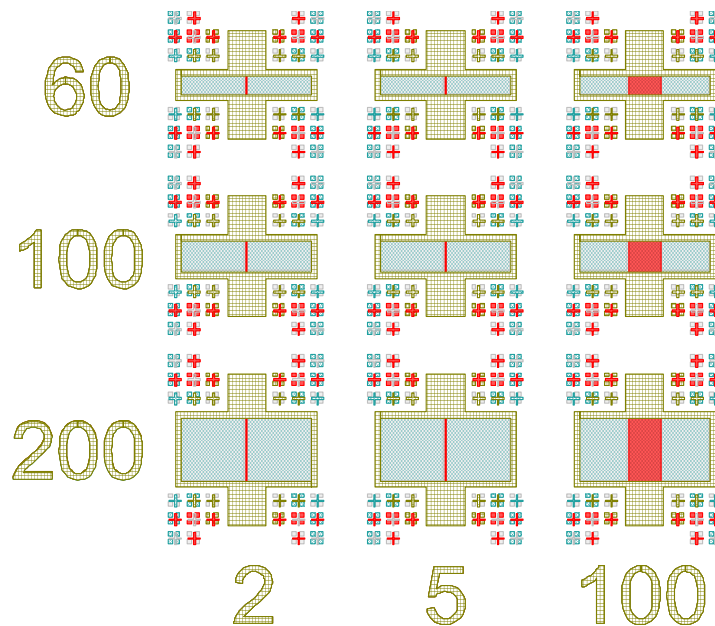
1. Intensively clean samples using solvents, such as acetone and iso-propanol (IPA), or an oxygen plasma clean. As photolithography is a type of printing process, the samples are required to be very clean with few contaminants.
2. Spin coat a layer of photosensitive resist onto the sample. Choosing the correct resist is very important because it can affect the resolution of the photolithography, with thinner resists generally offering the best resolution. There are two types of resist, positive working, where the UV-exposed resist is dissolved during development, and negative-working, where the resist not exposed to UV light is removed during development. The '1813' resist is an example of a positive working resist and 'AZ nlof 2070' is a negative resist example, with both used in this project.
3. Soft bake the resist on a heat plate to remove excess solvents, this part of the process is important because the sample needs to be sufficiently dry for alignment.
4. Align the sample to a specifically designed photoelectric mask in a mask aligner. Once the sample is well-aligned, expose the sample to UV light for a predetermined amount of time (typically 10 to 60 seconds)
5. Once exposed, samples patterned with negative working resist require a post-exposure bake (PEB) to cross-link the polymers in the resist. Positive working resists usually do not require this bake and can be developed straight after UV exposure. Once ready, all samples are placed in a developer fluid for a pre-

specified amount of time in order to dissolve the predefined regions of resist. Once the sample is developed, the photolithography process is complete.

### ***2.5.2 Design of masks***

In order to create bespoke semiconductor devices by photolithography, the photoelectric masks have to be specifically designed and fabricated. The masks used in this project were designed using commercial 'CleWin 4' mask design software, which is used to design masks in industry. Masks are typically designed in groups of multiple interlinked masks, known as 'sets'. Figure 2.6 shows the design of a mask set that can be used to fabricate HEMTs and a potential use for this specific mask set will be described in chapter 8. Each individual mask is known as a layer, with each layer being denoted as a separate colour or pattern in the CleWin 4 software.

In figure 2.6 the light blue crosshatched pattern corresponds to the 1<sup>st</sup> layer, which is mesa isolation and is achieved by reactive ion etching. Mesa isolation is a small etch around an electronic device to prevent it from interacting with neighbouring devices through the transfer of parasitic charges. The grey layer corresponds to the deposition of Ohmic contacts; these contacts will be deposited by electron beam deposition. The Schottky contacts are denoted by the red layer and will also be deposited by electron beam deposition. The yellow square outlines corresponds to a passivation layer. The passivation layer is a protective layer of an insulating material, such as SiO<sub>2</sub>, that is deposited by plasma enhanced chemical vapour deposition (PECVD). Reactive ion etching, electron beam evaporation and PECVD will be described later in this chapter. Alignment marks are typically added to the mask layers so that it is possible to align different layers to a sample that has already been patterned and processed using another layer. Figure 2.6 contains a large number of alignment marks to ensure that the four mask layers can be used as interchangeably as possible.

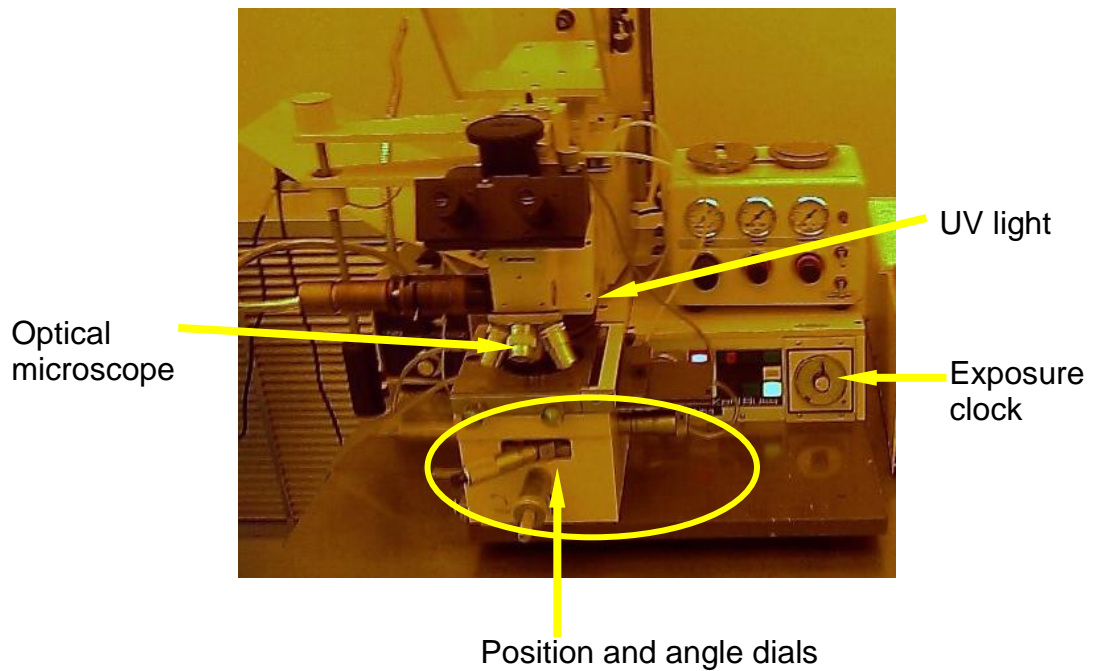


**Figure 2.6** An example of a mask set designed using CleWin 4 that can be used to fabricate AlGaIn/GaN HEMTs.

A photoelectric mask typically is made from quartz or soda lime, with the mask pattern printed onto the mask in chromium. The chromium prevents the UV light from penetrating the resist on the sample. Each mask has a surface area of four square inches in order to properly fit in the mask aligner and is 6 mm thick; this thickness allows the UV light to pass through the mask and ensures it is strong enough to withstand handling. The masks made for use in this project were produced externally by Compugraphics because the University of Bath lacks these facilities and they offer a faster service than MORGaN project partners.

### 2.5.3 Mask aligner

The mask aligner is the machine used to align the sample to the relevant photoelectric mask and perform the UV exposure. The moving parts of the aligner run pneumatically and are powered by nitrogen gas. The Karl Suss MJB3 mask aligner used at the University of Bath consists of five components: the mask holder, dials for adjusting the position and angle of the sample, a vacuum pump, an optical microscope and the UV lamp. A schematic diagram of the mask aligner used in this project is shown in figure 2.7.



**Figure 2.7** Diagram of the mask aligner used in the photolithography done in this project [100].

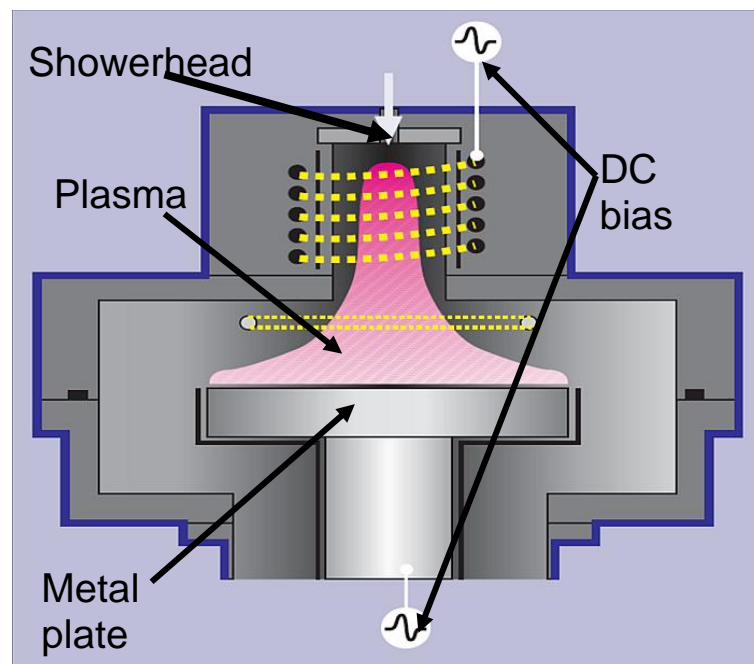
The photoelectric mask is placed onto the holder and is held in place with a vacuum provided by the vacuum pump. The vacuum pump is also used to hold the sample securely; the sample requires secure clamping because any small movements in it or the mask means that the sample requires realignment. The sample is aligned to the mask using four dials that control the x- and y- position, height and angle of the sample. The position and angle dials are capable of aligning the samples to an accuracy of  $\sim 2 \mu\text{m}$ , which although is not as high as electron beam lithography (EBL) that has a 2 nm resolution, is sufficient for the applications in this project. The height dial is extremely important because a sample needs to be in contact with the mask during the UV exposure to ensure the highest possible resolution and additionally, for the same reason, the mask is placed in the mask holder with the chrome side at the bottom so that it is in contact with the sample. The mask aligner also has a separation lever, which lowers the sample by  $4 \mu\text{m}$  and allows the sample to be moved into the best possible alignment.

In order to align the sample with the highest possible accuracy, an optical microscope is attached to the mask aligner and sits directly above the sample and mask when they

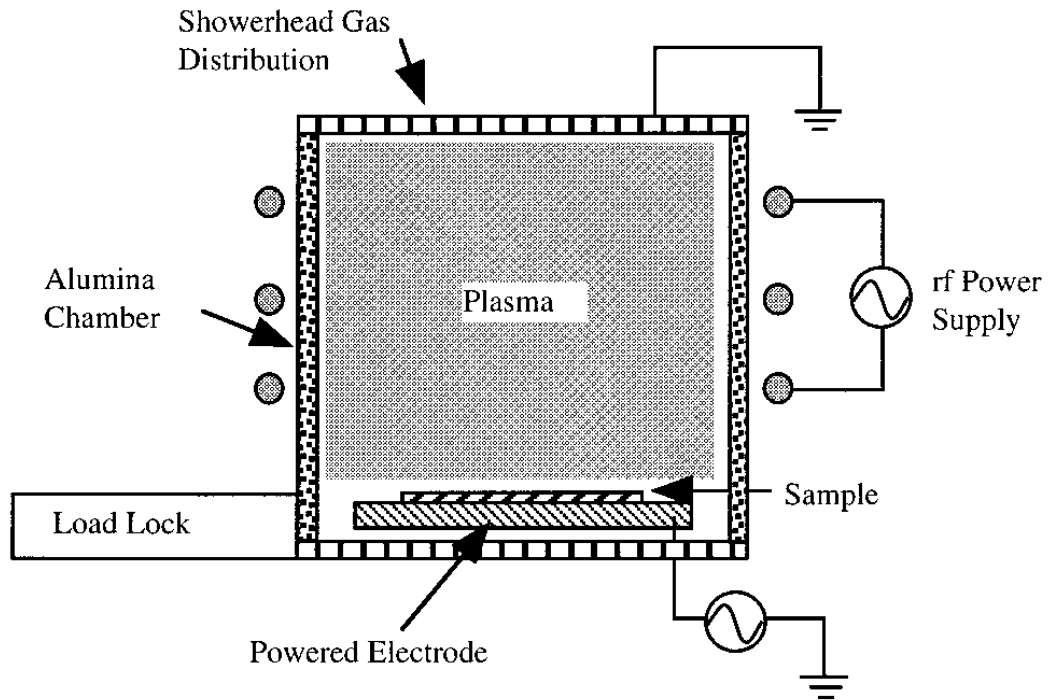
are not being exposed to UV light. The optical microscope allows the user to align the sample with an accuracy of  $\sim 2 \mu\text{m}$ . Once the sample is aligned, the pneumatic mechanism inside the mask aligner then moves the UV lamp over the mask and the microscope out of the way. The UV exposure time varies according to the thickness of the resist and the power of the UV lamp because the resist requires a certain amount of energy, as a function of resist thickness, in order to be fully exposed. This time has to be calculated for each sample using spin coating charts for the resist used.

#### 2.5.4 ICP etching

The Inductively Coupled Plasma (ICP) system at the University of Bath is an Oxford Instruments Plasmalab 80 series. This system has the capability of doing two different kinds of dry etching, ICP etching and reactive ion etching (RIE). Additional benefits to using an ICP etching system is that it achieves high etch rates due to very high ion densities, but the actual ion energy is low and this minimises damage to a sample. In this project ICP has been used to etch GaN because it is the standard process used in the nanofabrication centre, has higher plasma densities [101] and is more economical than RIE [102].



(a)



(b)

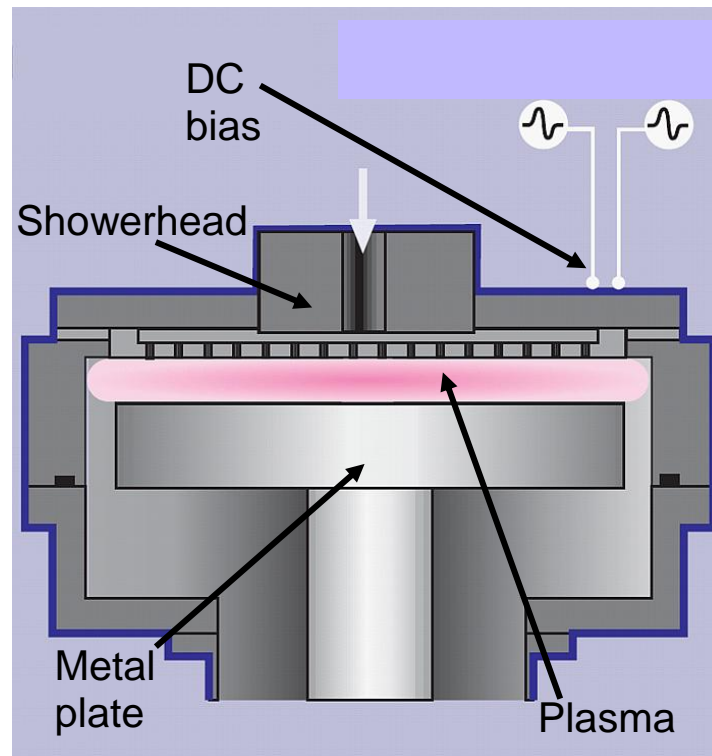
**Figure 2.8** Basic schematic diagrams of ICP etchers from (a) [103] and (b) [101].

The ICP etcher used in this project is a small-scale etcher, with a 240 mm diameter plate, which is typically used for research and development purposes. It consists of showerhead at the top (see figure 2.8) through which the etchant gases enter the chamber, in addition to another metal plate. Two large RF fields are produced by separate generators, are used to produce a plasma with a high degree of control over both ion energy and density. As the chemical reactions needed for ICP GaN etching are inhibited by even small amounts of contaminants, due to the use of a plasma, the reaction requires high vacuum conditions of  $\sim 10^{-4}$  Torr. In order to achieve this level of vacuum, two different pumps are used, a roughing pump, used to remove enough air to prevent the turbo pump from overheating. The turbo pump is also water-cooled because the risk of overheating is high.

The ICP etching of GaN typically occurs in a  $\text{Cl}_2/\text{H}_2$  plasma and this can achieve a GaN etch rate of  $700 \text{ \AA}/\text{min}$  for a DC bias of  $-150\text{V}$  [101]. The addition of Ar to the plasma and further increases in DC bias can further increase the etch rate, at the expense of a poor surface morphology [101]. The DC bias of the plasma is a function of the ion's energy and is a measurement of the voltage between the metal plate and showerhead, shown in figure 2.8. Furthermore, the inclusion of an RF bias can make the etch anisotropic, which means that the plasma will etch the desired crystal plane at a rate faster than the others and will produce a smoother surface morphology [101]. Smooth surfaces are desirable because they improve device reliability when fabricating MEMS devices. The final point note is that the GaN plasma etch process will produce by-products, some of which are harmful and require appropriate storage and disposal. These by-products include  $\text{GaCl}_3$ ,  $\text{N}_2$ ,  $\text{NH}_3$  and  $\text{NCl}_3$ .

#### ***2.5.5 Plasma-enhanced chemical vapour deposition (PECVD)***

Plasma-enhanced chemical vapour deposition (PECVD) is primarily used to deposit thin layers of  $\text{SiN}_x$  or  $\text{SiO}_2$  typically at  $300^\circ\text{C}$ , although it is possible to do this process at room temperature if necessary. PECVD produces conformal films with good electrical and mechanical properties at relatively low temperatures, reducing the amount of thermal mismatch. The ionised plasma produced in the PECVD process increases the flow of electrons between two electrodes in the system, allowing a good deposition rate at lower temperatures.



**Figure 2.9** Diagram of a PECVD reaction chamber [104].

Although ICP systems generally have the capability to do PECVD depositions [103, 105], the depositions were done using a Plasma-Therm 790 series machine [106]. The ICP system at the nanofabrication centre is optimised for dry etching and does not have all the required gases connected for PECVD. The PECVD system consists of a large plate with enough space for a 16-inch wafer [106], although depositions are typically on multiple 2-inch wafers. There is a showerhead and metal plate at the top of the chamber, like the ICP etcher and shown in figure 2.9. The main differences between the PECVD and ICP etcher are the precursor gases that are connected to the system and the operating conditions. The PECVD process can operate at 0.5-1.0 Torr with no RF bias is applied to the bottom plate, which is preheated. When doing an etch in the ICP, the gases used are  $O_2$ ,  $H_2$ ,  $Cl_2$ ,  $CHF_3$  and  $CCl_4$ , whereas the gases used in the PECVD deposition process are  $SiH_4$ ,  $NH_3$ ,  $N_2O$ , Ar,  $N_2$ ,  $CHF_3$  and  $O_2$ , where  $CHF_3$  and  $O_2$  gases are also used for cleaning the chamber and Ar as a catalyst. Using the PECVD process, it is possible to deposit up to 1  $\mu m$  layers of  $SiO_2/SiN_x$ .

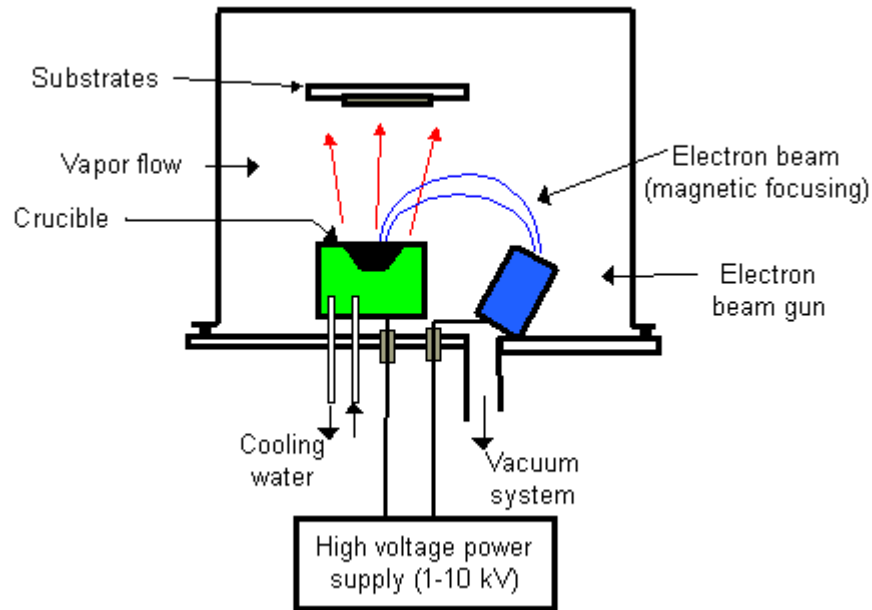


To produce a layer of SiO<sub>2</sub>, the plasma consists of SiH<sub>4</sub> and O<sub>2</sub> with the optional presence of an Ar catalyst [107]. SiN<sub>x</sub> is produced using a plasma of SiH<sub>4</sub>, N<sub>2</sub> and ammonia, with the possible addition of an Ar catalyst [108]. In this project the Ar catalyst was not needed as the films being deposited were small (100's of nanometres). These reactions occur at 300°C under a DC bias of ~300 V using Plasma-Therm 790 series PECVD in the nanocentre.

### ***2.5.6 E-beam evaporation***

Electron beam evaporation is commonly used to deposit metals with high boiling points onto semiconductor samples, by evaporating these metals with a high temperature electron beam. Typical metals deposited by this method include gold, tungsten, nickel and titanium. In common with ICP etching, the electron beam evaporation needs to take place in a good quality vacuum with a maximum pressure 10<sup>-5</sup> Torr. In order to pump down the vacuum chamber down to these levels, the vacuum pump requires cooling with a cryogenic fluid, like liquid nitrogen, to prevent overheating.

An electron beam evaporator consists of a vacuum chamber, a tungsten filament, a temperature controller, a shutter, magnets, crucibles and a sample target. The shutter blocks the path of the metal to the target when closed, controlling the deposition rate and thickness. The magnets are used to guide the beam of electrons to the crucible containing the target metal. The source of the beam of electrons is the tungsten filament.



**Figure 2.10** Schematic of an electron beam evaporator [109].

The process starts with the heating of a hot filament typically made from tungsten, which produces a beam of electrons through thermionic emission and acts like a gun of electrons. These electrons are then aimed at a crucible containing the deposition metal using magnets. The magnets can be moved with a fine degree of accuracy to optimise the deposition rate of the metal. Once the electrons strike the metal, some of the metal in the crucible is released in vapour form and strike the sample, when the shutter is open, which is placed in a target at the top of the chamber. Once the desired layer thickness is reached, the shutter is closed and the power of the tungsten filament is reduced down to zero.

## 2.6 Finite element (FE) analysis

The material properties discussed in the literature review are fully programmable into the Finite-Element (FE) and analytical models used in this project. These models can be used to predict bow, wafer failure and the stress profile of wafers. The FE models were used in this project to accurately predict the stresses within a silicon/polycrystalline diamond composite wafer that can be used for future GaN

growth. The purpose of the polycrystalline diamond is to improve the thermo-mechanical properties of current substrate technology, particularly at high temperatures. Outside of this project, there is no in-depth FE analysis of the stresses developed in a silicon/polycrystalline diamond composite wafer in the literature; although there is some experimental data by Zimmer *et al* [13]. The main purpose of a finite element model is to undertake elastic stress analysis of a body, where the body is divided up into discrete, connected blocks known as finite elements. These elements will either be triangles or quads for a two-dimensional body, or tetrahedra or parallelepipeds for a three-dimensional system. The elements are connected together with nodes, which are typically located at the corners and sometimes in the side walls of elements. The elements are arranged into a pattern known as a mesh and this covers the entire body in the model. The selection of an appropriate mesh and element size is difficult, and requires judgement and experience. Many commercial FE software packages, like ANSYS, have features that can be used to automatically create a mesh [110].

The first step in FE model is to determine the forces applied and the resultant displacement on each node, and these are linked by the stiffness matrix. In ANSYS, the FE package used in this project, the elastic moduli and Poisson's ratios are automatically converted into the full stiffness matrix form. The formula that links the nodal force and displacement to the stiffness matrix is as follows in (2.1).

$$(\text{nodal forces}) = [\text{stiffness matrix}] \times (\text{nodal displacement}) \quad (2.1)$$

This formula can be inverted in certain circumstances, such as when an external force is applied to the body, and is a very important aspect of FE analysis. All of the elemental stiffness matrices are then combined to form a global stiffness matrix for the entire body, in a process known as assembly. It is then possible to determine the stresses of individual elements at certain points [110]. This ability of FE analysis to predict the build up of stress in a specific point of a structure is very valuable and will be used extensively in proceeding chapters.

### 2.6.1 Piezoelectric constitutive relation

The piezoelectric constitutive relation is used in finite element software to predict the piezoelectric response of a material to an applied strain. In ANSYS, the linear piezoelectric constitutive relation for solving piezoelectric problems is shown in the following equation [111].

$$\begin{Bmatrix} T \\ D \end{Bmatrix} = \begin{bmatrix} c^E & -e^t \\ e & \varepsilon^S \end{bmatrix} \begin{Bmatrix} S \\ E \end{Bmatrix} \quad (2.2)$$

The definitions for the symbols in 2.2 are as follows, with  $T$  being the stress,  $D$  being the electronic displacement,  $S$  is the strain and  $E$  is the electric field [111]. The other mechanical properties in this relation, that are related through the material properties are the stiffness under constant field  $c^E$ , the piezoelectric stress coefficient  $e$  and the dielectric constant under constant strain  $\varepsilon^S$ . The lower case ‘ $t$ ’ denotes a matrix transpose [111].

In ANSYS, a full piezoelectric model requires a user to input the dielectric constants ( $\varepsilon^S$ ), the piezoelectric stress coefficients ( $e$ ) and the stiffness of the material under a constant field ( $c^E$ ) [111]. The piezoelectric constitutive relation is reason why all of the data in section 1.6 is required to produce accurate piezoelectric FE models used in chapters 3 and 4.

**The next chapter will discuss the development of a silicon/polycrystalline diamond (Si/PD) composite substrates that have applications in GaN-based technologies. This chapter will discuss the difficulties in realising Si/PD substrates due to the mismatch in thermal expansion coefficients (CTEs), which causes stress and bow in the wafers as they are cooled from a high processing temperature.**

## CHAPTER 3: OVERCOMING ISSUES RELATED TO THE DEVELOPMENT OF A SILICON/POLYCRYSTALLINE CVD DIAMOND SUBSTRATE

### 3.1 Motivation

In order to create a viable GaN sensor, high power diode or transistor, a suitable substrate is required to support the device in harsh operating conditions. High-power GaN HEMT devices quickly produce large amounts of energy, mostly in the form of heat [5, 112] (and see chapter 7). This heat energy needs to be removed quickly because otherwise it will have a large impact on the operation of the device [113]. One way in which heat can be effectively removed from a power-HEMT is by fabricating the device on a thermally conductive substrate. The thermally conductive substrate will act as a heat sink, by allowing the heat to be quickly conducted from the device and through the substrate [14, 15, 114]. The material forming the substrate must ideally be thermally conducting and electrically insulating. Single-crystal diamond is a highly effective thermal conductor [10] with a thermal conductivity of  $4000 \text{ J K}^{-1}\text{m}^{-1}\text{s}^{-1}$  at  $20^\circ\text{C}$ , but it is extremely expensive and only available in relatively small sections. Polycrystalline diamond is also an excellent thermal conductor, with a conductivity of  $2270 \text{ J K}^{-1}\text{m}^{-1}\text{s}^{-1}$  at  $20^\circ\text{C}$  is potentially available at lower cost than SiC (see chapter 1 for details of SiC cost) and can be grown on larger areas on silicon wafers [11-13, 115]. Therefore, using a diamond or diamond-based substrate for GaN growth would offer a significant improvement in heat sinking properties over commercially available substrates used for GaN-growth, such as silicon ( $10$  to  $20 \text{ Wm}^{-1}\text{K}^{-1}$  at room temperature [94]), sapphire ( $25$  to  $50 \text{ Wm}^{-1}\text{K}^{-1}$  at room temperature [84]) or silicon carbide ( $387 \text{ Wm}^{-1}\text{K}^{-1}$  at room temperature [9]).

Other advantages to using diamond are increased stiffness and thermal stability. Single-crystal diamond has a Young's modulus of  $1050 \text{ GPa}$  at room temperature. Recent improvements in chemical vapour deposition (CVD) diamond technology means that optical-quality CVD diamond has a Young's modulus approaching that of single crystal diamond [78]. Silicon, sapphire and SiC substrates have a lower stiffness and lower fracture stress [47], meaning that a diamond-based substrate

would be potentially better for pressure sensing applications at high pressure and temperature.

Although (0001) GaN has been epitaxially grown on single-crystal (110) diamond [116], the lattice mismatches between the two materials is 11.8% [117], similar to Si and single-crystal diamond substrates are expensive. The large lattice mismatch between GaN and diamond induces threading dislocations (TDs) in the GaN epitaxial layer once the thickness of this layer exceeds a critical value [118]. TDs are undesirable in semiconductors because they led to interface traps, which impair the flow of charge carriers and dramatically decrease the performance of the material [2].

The method proposed to overcome the price and performance issues associated with GaN/diamond wafers is to develop a GaN/Si/polycrystalline CVD diamond (PD) composite wafer. Silicon/PD substrates are potentially advantageous under high pressure or at high temperatures in inert environments, since both materials have high melting points, good mechanical and chemical stability. Silicon has a large lattice mismatch of 17% [119] between itself and GaN, but has the advantage that polycrystalline diamond can be readily grown on its backside by CVD. Additionally, this wafer would be desirable because it can be easily integrated with silicon-based integrated circuits and would offer similar performance characteristics to a single-crystal diamond substrate at a cheaper price.

The single crystal silicon provides a substrate for the growth of the polycrystalline diamond and, if thinned to a few microns, provides a base from which epitaxial GaN can be grown without significantly impairing the thermal performance of the substrate. The growth of diamond on Si has been studied previously and Si/PD composite wafers are observed to bow when the substrate is cooled from the CVD diamond growth temperature (~700-800°C) [13] to room temperature (25°C). The main cause of the bowing is a mismatch in the coefficients of thermal expansion (CTE),  $\alpha$ , between silicon and polycrystalline diamond. Excessive bow can cause the wafer to delaminate [120-122] or crack when an attempt is made to flatten the wafer.

### **3.2 Aims of this chapter**

The aim of this chapter is to provide modelling data of the thermal stresses that develop in Si/PD composite wafers. This will help realise composite wafers for subsequent growth. It will involve modelling the thermo-mechanical behaviour of silicon–polycrystalline diamond wafers, using finite-element (FE) simulations and predicting the bowing behaviour of silicon-polycrystalline wafers as a function of temperature and geometry. This chapter will show that the bow of a 100 mm diameter wafer can be predicted to significantly exceed 1mm; making it unsuitable for use as a substrate for the subsequent epitaxial growth of GaN, potentially leading to the fracture/failure of the wafer unless the geometry and processing conditions are optimized.

The initial FE model will be compared and validated with an analytical method derived from Hsueh [123]. This method will use linearly averaged materials data with respect to temperature material properties based on the properties contained in the literature review (See section 1.6). If the FE model approach is valid, it should closely match the analytical method when programmed with linearly averaged mechanical properties, where the average of the Si and PD mechanical properties data has been averaged between 25 and 800°C.

The FE model will also be tested against experimental data on Si/PD composite wafers found in the literature and results presented in this chapter. The accuracy and validity of the model will then be discussed and determined. The FE model will be used to predict the stresses in a Si/PD wafer and this will predict how a wafer will fail or fracture as a function of geometry. Stress profile measurements of the wafer will be generated and these will be experimentally validated using micro Raman measurements.

Possible methods for alleviating stress will be simulated using the FE model and the merits of these methods will be discussed. Some of these methods will be trialled and the results will be compared to the model. Failed experimental attempts at relieving stress will be modelled retrospectively and the model will be used to help explain why this attempt failed.

The effects of epitaxially growing III-V nitride structure on the Si/PD composite wafer will also be explored using the model. The stress profile of this system will be simulated and this will be used to predict any potential issues with growing GaN on the composite wafer. The model will then be compared with experimental data and the merits of the FE approach will be discussed.

The accuracy and potential improvements to the model will be discussed and there will be a discussion on future methods to improve the model's accuracy and neglected physical mechanisms that can be added.

### **3.3 Analytical Model and Comparison with FE**

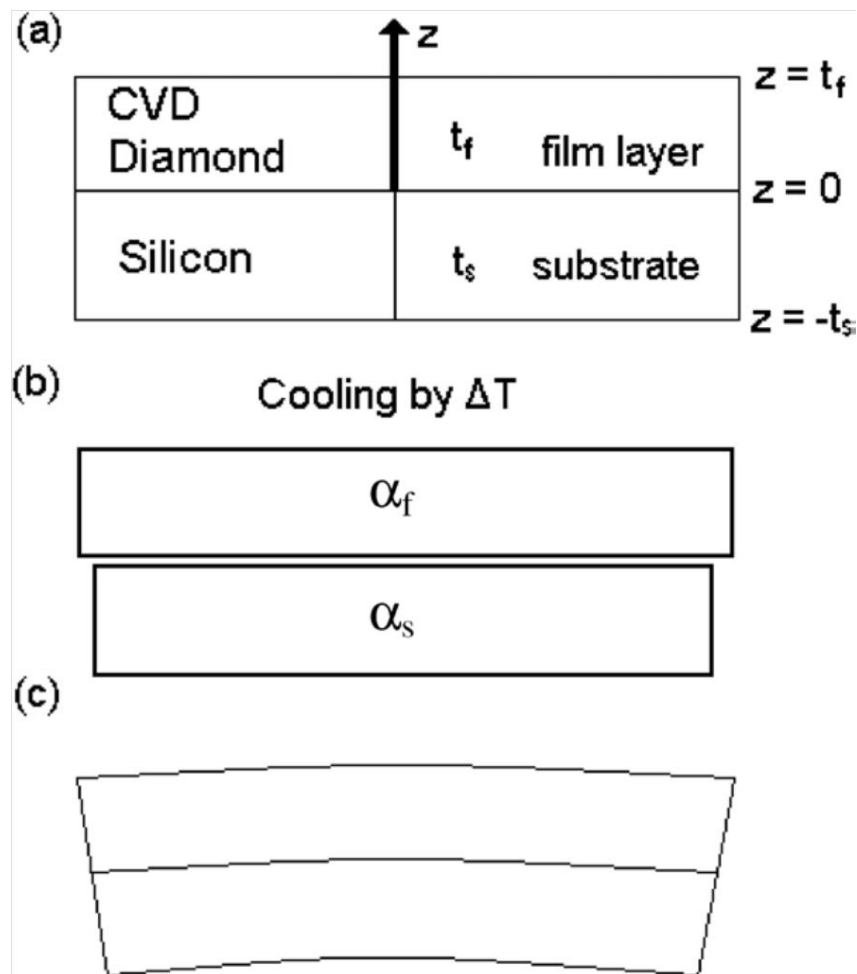
Detailed experimental and modelling of bowing measurements of the bowing of polycrystalline diamond - (111) silicon composite wafers is rather limited in the literature [13]. This means that a method of confirming the prediction of the FE model is required. In order to do this a comparison is made with the predictions of an analytical model based on the theory of thermal stresses in elastic multilayer structures described by Hsueh [123] and figure 3.1.

#### ***3.3.1 Analytical model***

In the analytical method, it is assumed that the silicon–polycrystalline diamond wafer is 100 mm in diameter, perfectly elastic and cooled to room temperature (25°C) from a growth temperature of 800°C ( $\Delta T = 775^\circ\text{C}$ ); this is similar to the deposition temperatures used in Zimmer *et al* [13]. A mismatch in the coefficients of thermal expansion (CTEs) cause the film and substrate contract by differing amounts (figure 3.1 (b)) and as the strain in the wafer is constrained it bows due to asymmetric stresses (figure 3.1 (c)). If the silicon substrate contracts to a greater degree than the diamond, the silicon is under tension while the diamond film is under compression.



The stress-strain distribution in such a bi-layered system is dependent on three parameters.



**Figure 3.1** Bowing behaviour of the bi-layer wafer. (a) The polycrystalline CVD diamond film is grown at 800°C and the wafer is at thermal and structural equilibrium. (b) The wafer is cooled to room temperature and the film and substrate have contracted by differing amounts due to a mismatch in CTEs. (c) As the strain in the wafer is constrained, it bows due to asymmetric stresses [123].

These parameters are the uniform strain component,  $c$ , the bending axis,  $t_b$ , and the radius of curvature,  $r$ . The stress-strain parameters can be determined through the total strain in the system,  $\epsilon$ , the normalized biaxial stresses,  $\sigma_{Sb}$  and  $\sigma_{Fb}$ , and three sequential boundary conditions discussed in [123]. Firstly, the analytical model assumes that both silicon and polycrystalline diamond have isotropic properties to simplify the derivation. The orientation of the silicon wafer is (111) and that is

assumed to be isotropic. Secondly, as the wafer undergoes biaxial strain it has planar geometry and the Young's moduli of the substrate (silicon) and film (polycrystalline diamond) have to be adjusted according to [123] such that

$$E_{Sb} = \frac{E_S}{1-\nu_s} \quad (3.1)$$

$$E_{Fb} = \frac{E_F}{1-\nu_F} \quad (3.2)$$

Where  $E_S$  and  $E_F$  are the Young's moduli of the film and substrate respectively, with  $E_{Sb}$  and  $E_{Fb}$  being the adjusted Young's moduli that take the biaxial strain of the system into account. The Poisson's ratios of the film and substrate are  $\nu_F$  and  $\nu_S$  respectively. Polycrystalline diamond is the film material and silicon is the substrate material in this model.

The normalized biaxial stresses on film and substrate materials and the total strain in the system are

$$\varepsilon = c + \frac{z - t_b}{r} \quad (3.3)$$

$$\sigma_{Sb} = E_{Sb}(\varepsilon - \alpha_S \Delta T) \quad (3.4)$$

$$\sigma_{Fb} = E_{Fb}(\varepsilon - \alpha_F \Delta T) \quad (3.5)$$

Using boundary conditions derived from equations (3.3) – (3.5) ,[123], it is possible to derive the universal strain component,  $c$ , the bending axis,  $t_b$ , and the radius of curvature,  $r$ , for an elastic bi-layered strip.

$$c = \frac{(E_{Sb}t_S\alpha_S + E_{Fb}t_F\alpha_F)\Delta T}{E_{Sb}t_S + E_{Fb}t_F} \quad (3.6)$$

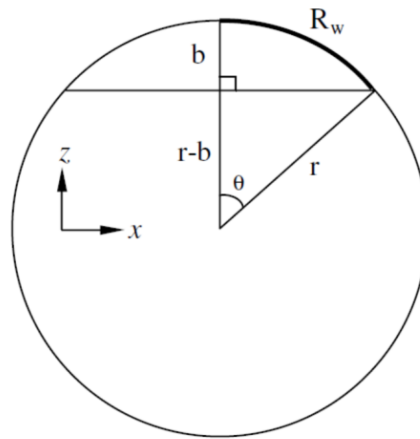
$$t_b = \frac{E_{Fb}t_F^2 - E_{Sb}t_S^2}{2(E_{Sb}t_S E_{Fb}t_F)} \quad (3.7)$$

$$r = \frac{E_{Sb}t_S^2(2t_S + 3t_b) + E_{Fb}t_F^2(2t_F - 3t_b)}{3[E_{Sb}t_S^2(c - \alpha_S\Delta T) - E_{Fb}t_F^2(c - \alpha_F\Delta T)]} \quad (3.8)$$

With  $r$  derived it is possible to calculate the bow,  $b$ , of the wafer using geometry.

It is possible using simple geometry to determine the bow,  $b$ , of the silicon-polycrystalline diamond wafer from its radius of curvature,  $r$ , and radius of the wafer,  $R_w$ . Wafer bow is defined here as the change in displacement in the  $z$ -direction, shown in figure 3.2. It is assumed in the model that the wafer is a perfect circle and therefore has rotational symmetry; this means that using a two-dimensional derivation as shown in figure 3.1 is acceptable. Figure 3.2 shows the geometry used to derive the resultant equation for determining wafer bow and is

$$b = r \left[ 1 - \cos\left(\frac{R_w}{r}\right) \right] \quad (3.9)$$

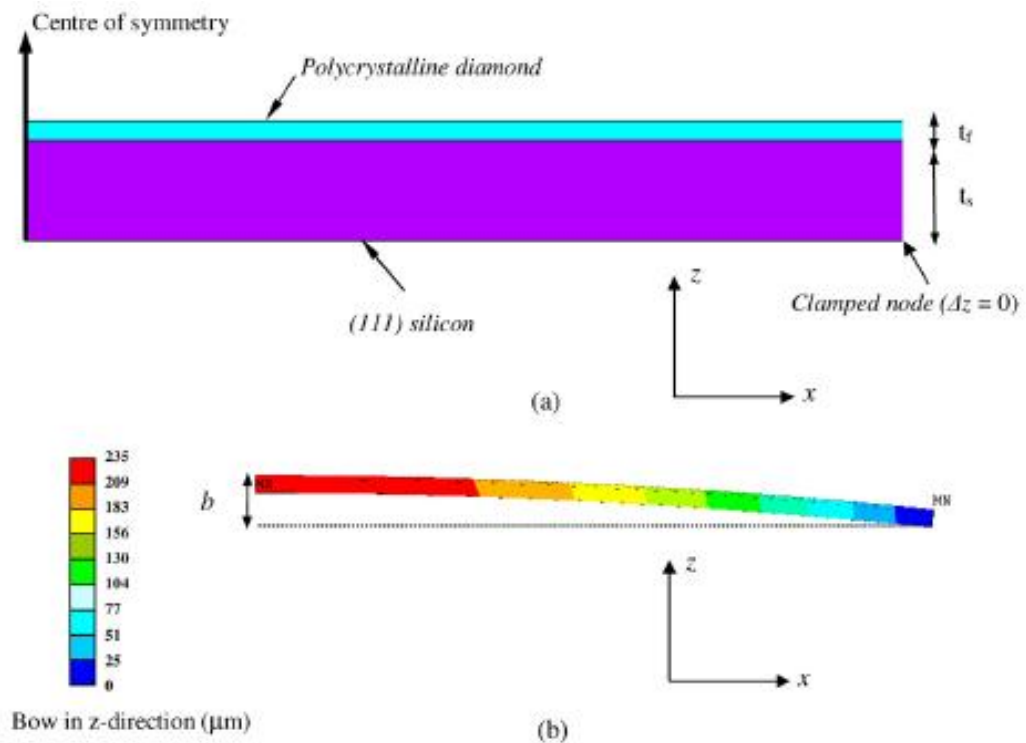


**Figure 3.2** Geometry used to determine wafer bow from the radius of curvature

### 3.4 The Finite Element (FE) Model

The FE model was developed using commercial software (ANSYS 11.0), chosen for its multi-physics capacity that allows the temperature dependent behaviour of the structural properties to be considered. The model assumes that the wafer obeys simple linear elasticity with no plastic deformation of the substrate or the presence of intrinsic stress within the diamond film. Before a FE model can be used it needs to be tested against either measured data or a rigorous analytical method. As there was initially only limited experimental data on the bow of silicon–polycrystalline diamond wafers [11, 13], a method of validating the model was to compare its results with those of the above analytical approach in which the wafer is assumed to act as an elastic bi-layered strip under biaxial strain. This is a reasonable assumption because the wafer has rotational symmetry and can be assumed elastic over a wide range of stresses. Zimmer *et al* [11, 13] indicated that a non-uniform temperature distribution across the silicon–polycrystalline diamond wafer during processing leads to asymmetric stress distributions that can distort the wafer to a saddle shape. By using hot filament CVD technology, Zimmer *et al* [13] produced a thermally uniform wafer [13], with a radial stress profile, and more symmetric wafer bow. One of the disadvantages of the analytical method is that it assumes that the stiffness and CTEs do not change with respect to temperature.

Figure 3.3 (a) shows schematically the structure modelled using FE analysis; it consists of a top film layer of polycrystalline CVD diamond and a bottom substrate layer of (111) silicon and is modelled in ANSYS using PLANE42 elements [124]. For efficient computation, axisymmetric boundary conditions were used, as shown in figure 3.3 (a). The PLANE42 element type was chosen because it is fully axisymmetric and its degrees of freedom include the two required spatial dimensions and was temperature sensitive. The wafer was clamped at the bottom edge to provide a simple measure of wafer bow.



**Figure 3.3** (a) Schematic of the wafer model. (b) FE model calculation of wafer bow, which is the displacement in the- $Z$ -direction.

The bow of the wafer was calculated for different thicknesses of the silicon substrate,  $t_s$ , between 1000 and  $3\mu\text{m}$ . The underlying interest in composite polycrystalline diamond–silicon wafers is their potential as substrates with superior heat sinking for high power GaN electronic and optoelectronic devices, exploiting the superior thermal conduction of polycrystalline diamond. As such, a thick silicon layer is

undesirable as it would impair the performance of any potential device. Thus, the primary purpose of the FE model is to model the bowing behaviour of the wafer as it is cooled and subsequently mechanically thinned down to the required silicon thickness. The bow,  $b$ , as measured experimentally and in all the models, is defined in figure 3.1 (c).

### 3.4.1 Comparison between FE model and Analytical Method

The main limitation of the analytical model is that it assumes that Young's moduli, Poisson's ratios and CTEs of both polycrystalline CVD diamond and silicon do not vary with temperature, which could lead to errors in predicted bow. However, it is possible to include the temperature dependence of properties using a linear average of the temperature dependent material properties from tables 1.9 and 1.11. The temperature independent averages of Young's moduli, Poisson's ratios and CTEs of silicon and polycrystalline diamond between 25 and 800°C used in the analytical and FE model are in table 3.1. The higher linearly averaged CTE of silicon, compared with diamond, leads to the wafer bowing as in figure 3.3 (b) with the silicon under tension and diamond in compression.

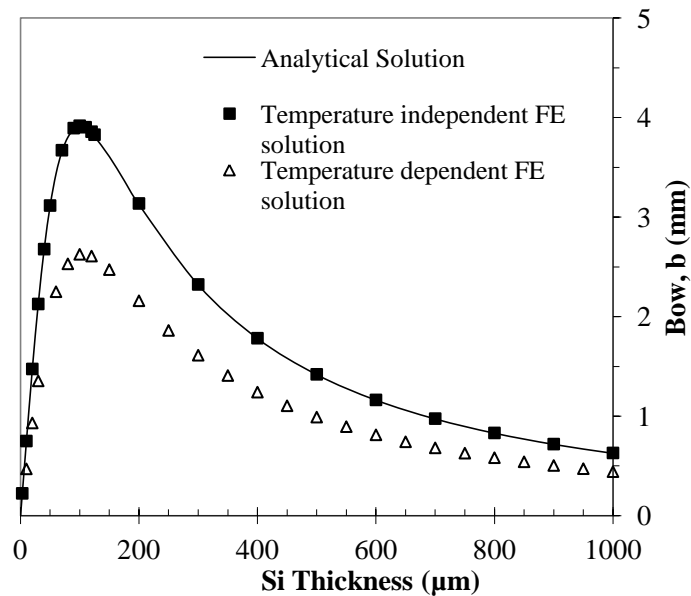
**Table 3.1** Temperature independent (linearly averaged) material properties of silicon and polycrystalline CVD diamond between the temperatures of 25 and 800°C.

Material	$E$ (25 - 800°C) / GPa	$\nu$ (25 - 800°C)	$\alpha$ (25 - 800°C) / $10^{-6} \text{ K}^{-1}$
Silicon	165.5	0.26	3.45
Polycrystalline Diamond	1014.0	0.1	2.8

In the example used in this work the bowing behaviour of a 100mm diameter composite silicon–polycrystalline CVD diamond wafer, with a polycrystalline CVD diamond thickness  $t_f = 100 \mu\text{m}$  and the temperature independent properties from table 3.1, has been calculated using the analytical and FE method. The properties used are valid because the Young's moduli of both materials shows almost a linear decay and

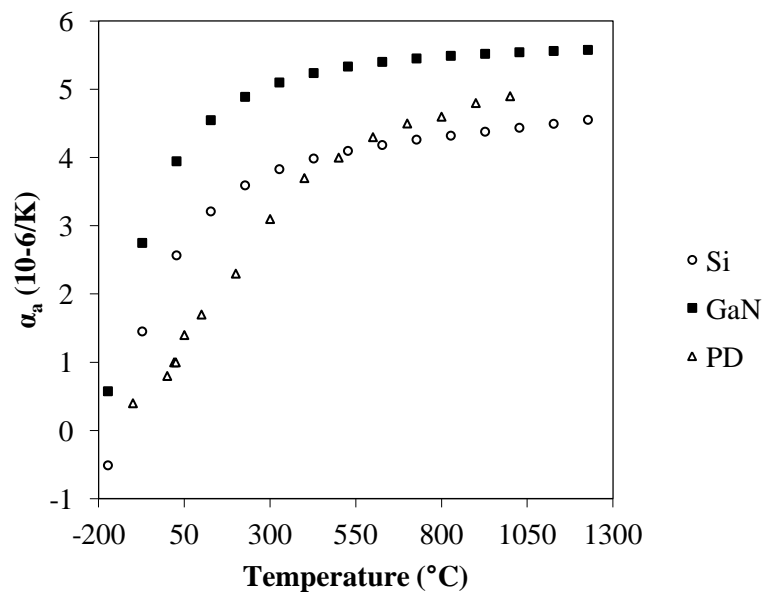
the Poisson's ratios remain roughly constant. The CTEs were determined this way because it was simple and at this stage identical CTE properties between the FE and analytical models, rather than exact numbers were required to validate the FE model analysis. An alternative method would be to calculate and use the secant CTEs rather than the linearly averaged CTEs.

The thickness of the silicon substrate,  $t_s$ , was varied between 3 and 1000  $\mu\text{m}$  and the wafer bow was measured after cooling the composite substrate from 800 to 25  $^\circ\text{C}$  ( $\Delta T = 775$   $^\circ\text{C}$ ). Figure 3.4 shows a comparison of the predicted wafer bow found from the FE model and the analytical model. The bowing values calculated from the analytical model are shown by the continuous line, whilst those found from the temperature independent FE model are shown by the square data points (■).



**Figure 3.4** Graph comparing the bow measured in both the temperature independent and temperature dependent FE models with the bow predicted in the analytical solution for a 100 mm wafer with a 100 $\mu\text{m}$  thin film layer of polycrystalline CVD diamond.

Excellent agreement is observed between the analytical and temperature independent FE models, indicating mutual consistency and implies that the boundary conditions and mesh densities employed in the FE approach are appropriate. Good agreement is expected because both models use identical material properties and have identical geometries. It is of interest to note that both models predict that the bowing is a maximum when the thickness of the silicon almost equals that of the polycrystalline diamond film ( $t_S \sim t_F$ ), with the bow then falling as the silicon thickness decreases to zero. The bowing is also reduced, but with a monotonically decreasing rate as the silicon substrate thickness is increased to 1000  $\mu\text{m}$ . This behaviour is readily understood at the two extremes, the composite wafer bow is governed by the stiffness of the silicon ( $t_S \gg t_F$ ) or the stiffness of the polycrystalline diamond ( $t_S \ll t_F$ ) at these conditions.

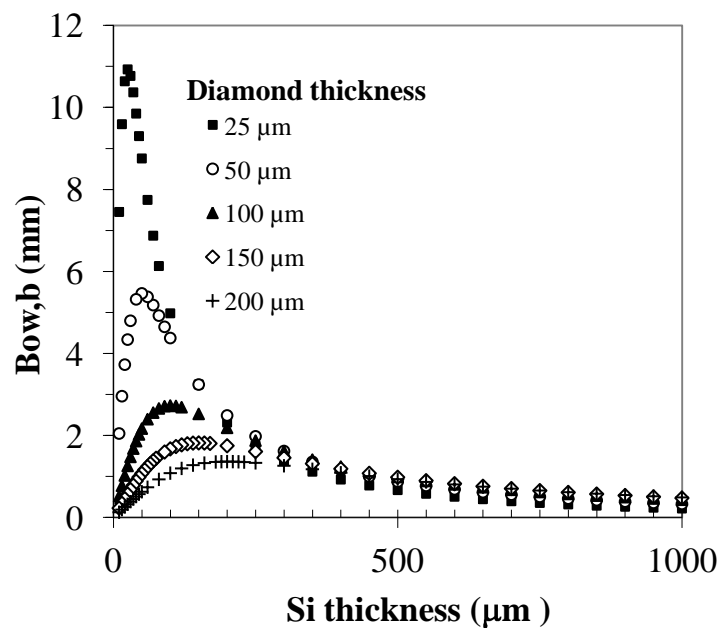


**Figure 3.5** CTEs of PD, Si and a-plane (0001) GaN [47-51, 82]

The results from figure 3.4 expose a problem likely to arise if a thick silicon substrate (typically 500 to 650  $\mu\text{m}$ ) is to be thinned by etching or polishing after growth of the CVD polycrystalline diamond to enable optimum heat extraction of any GaN semiconductor device grown on the free silicon surface. The increase in bow as the silicon is thinned will increase the likelihood of wafer breakage in the silicon.



One of the advantages of the FE model is that it can be readily extended to include the temperature dependent material properties from tables 1.9 and 1.11 as shown by open triangular data points ( $\Delta$ ) in figure 3.4. The most significant result from the temperature dependent FE model is that it predicts a lower degree of wafer bowing in comparison with the results from the analytical and temperature independent FE models. In fact at low temperatures the CTE of diamond is lower than silicon while at higher temperatures the CTE of diamond is higher than silicon as shown in figure 3.5. This is significant because this suggests that the temperature independent models overestimate the degree of bowing. Understanding these effects is vital because it is important to engineer the degree of bow to be as small as possible. One of the ways the bowing effects have been explored using the temperature dependent FE model is by varying the thickness of the polycrystalline diamond film, as shown in figure 3.6.



**Figure 3.6** Wafer bow in a composite (111) Si/polycrystalline diamond wafer versus thickness of the Si substrate for five thicknesses of polycrystalline diamond using the temperature dependent FE model.

Figure 3.6 shows the predicted bow of five different wafers with diamond film thicknesses between 25 and 200  $\mu\text{m}$ . The same process of simulating the thinning of

the silicon layer from 1000 to 10  $\mu\text{m}$  was applied to each wafer. Figure 3.6 reveals that the maximum bow is smaller as the polycrystalline diamond layer thickens. The temperature dependent FE model predicts that increasing the thickness of the polycrystalline diamond from 100 to 200  $\mu\text{m}$  approximately halves the wafer bow. The maximum bow is reduced when the polycrystalline diamond thickness is increased due to the diamond having a stiffening effect on the wafer. When the thickness of the polycrystalline diamond layer approaches 200  $\mu\text{m}$ , the 100 mm diameter wafer will have a predicted maximum bow of  $\sim 1$  mm from centre to edge. The breadth of this maximum means that the wafer will not see the dramatic increases in bow associated with thinning the silicon layer of wafers with a polycrystalline diamond thickness of  $\leq 100$   $\mu\text{m}$ . Referring to Figure 3.5, the CTE of GaN is greater than both diamond and silicon. If GaN is epitaxially grown on the free silicon surface, i.e. the underside of the silicon in figures 3.1 (c) and 3.3 (b), then the higher CTE of GaN could increase bow; although the GaN device layers are expected to be relatively thin (a few microns) [12].

A final point is that the analytical and FE models explored in this thesis assume that the wafer is perfectly elastic with no plastic deformation of the silicon substrate. Lattice dislocations can partially relax the wafer, reducing the overall amount of bow; however experimental measurements by Zimmer *et al* [13] show that on removal of the diamond by oxidation there was no observable plastic deformation of the silicon.

### **3.5 Prediction of wafer failure through interfacial peeling**

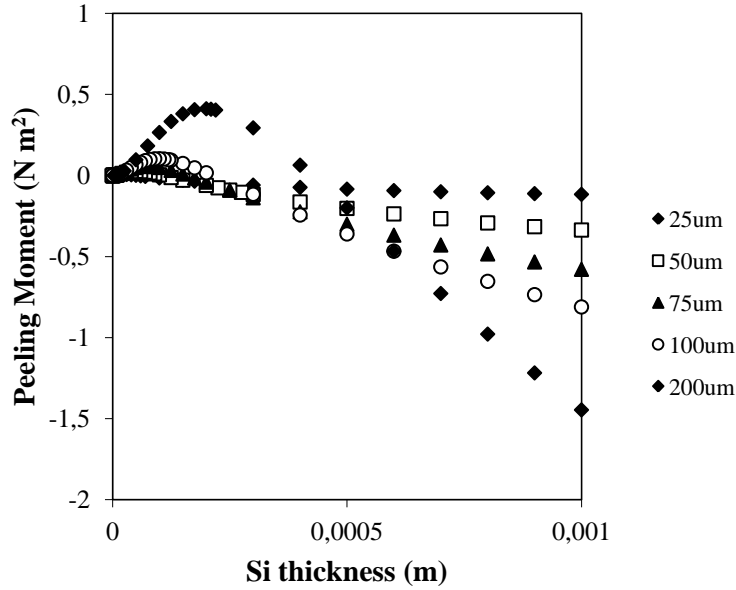
In the theory of bimaterial beams and plates, the systems are weak at the interface between the two materials with horizontal cracks forming at free ends. The Si/polydiamond composite wafer is effectively a bimaterial plate under biaxial stress. This means that interfacial cracks can form at the outer edges of the wafer when sufficient thermal stresses are applied. If the interfacial cracks are sufficiently large and the thermal stresses in the system are high, the crack will spread across the entire interface in a process known as delamination. Delamination is a common type of failure in MEMS semiconductor devices. Delamination occurs due to the mismatch in the CTEs, in materials that are epitaxially bonded are cooled from the deposition

temperature. The mismatch in CTEs means that the materials contract at different rates, causing large interfacial shear stresses at the free edges of the structure. For large shear stresses, the materials will start to separate at the free edges creating horizontal interfacial cracks.

The likelihood of delamination can be determined by the peeling moment and its derivation follows on from the derivation of the analytical method and is covered in papers by Moore and Jarvis (2003) [121] and Hsueh et al (2006) [125]. The FE work done by Moore and Jarvis and the work done so far in this chapter indicates that this can be used as a simple design tool. The formula for the peeling moment  $M$  in a bilayered plate is derived in references [121] and [125], and is quoted as follows.

$$M = \frac{t_s t_f (E_{sb} t_s^2 - E_{fb} t_f^2)}{12(t_s + t_f)r} \quad (3.10)$$

In the case of a bimaterial system with a negative radius of curvature, the peeling moment is negative when the interfacial bond is strong; and when the peeling moment is positive the interfacial bond is weakened, with peeling and eventual delamination being the likely outcome. The likelihood of complete delamination is increased, as the magnitude of a positive peeling gets greater.



**Figure 3.7** The peeling moment of a 100mm diameter Si/PD wafer at different PD thicknesses.

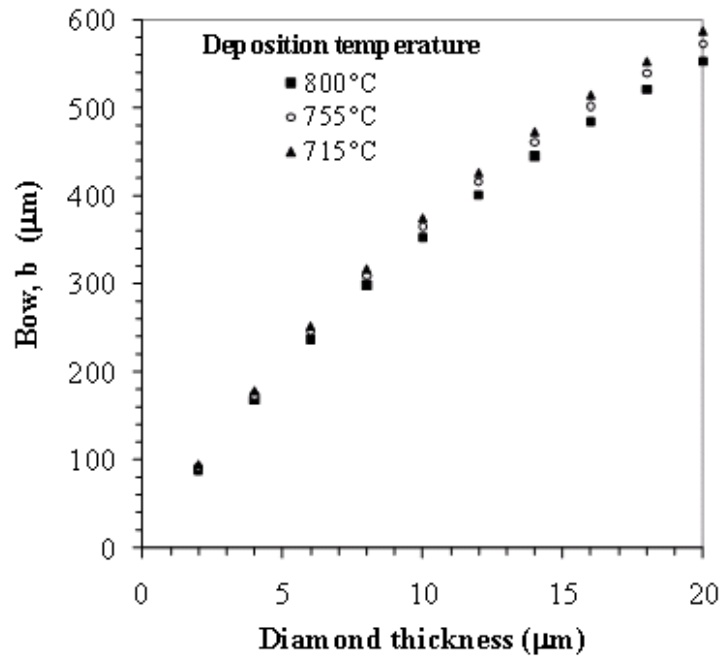
It is theoretically possible to determine the peeling moment using the analytical model, as shown in figure 3.7. The most interesting outcome of these results is that wafers with a thicker layer of PD appear to be more likely to fail by delamination. Furthermore, the results from the analytical model also show that delamination is most likely to occur when the thicknesses of both Si and PD materials is about equal for all PD thicknesses. Although the peeling moment results do not show where the wafer will actually fail, they show a critical region where failure is possible and show that it would be good experimental practice to minimise the peeling moment.

### 3.6 Comparison of FE Model with Experimental Data

#### 3.6.1 Comparison with the Literature

The only available experimental data found in the literature for bow of silicon / polycrystalline diamond wafers is in Zimmer *et al* [13]. The thickness of the silicon layer was 525  $\mu\text{m}$  [126] and the wafer diameter was 100 mm [13]. The deposition layer of polycrystalline diamond was increased from 2 to 20  $\mu\text{m}$  at 2  $\mu\text{m}$  intervals. FE models of the diamond-silicon wafer were generated at three different temperatures

(715, 755 and 800°C) to compare with the experimental observations; where 715 and 755 °C are the growth temperatures used in reference [13]. The temperature dependent elastic and CTE data of silicon and diamond were used in the model and figure 3.8 indicates the model predictions.

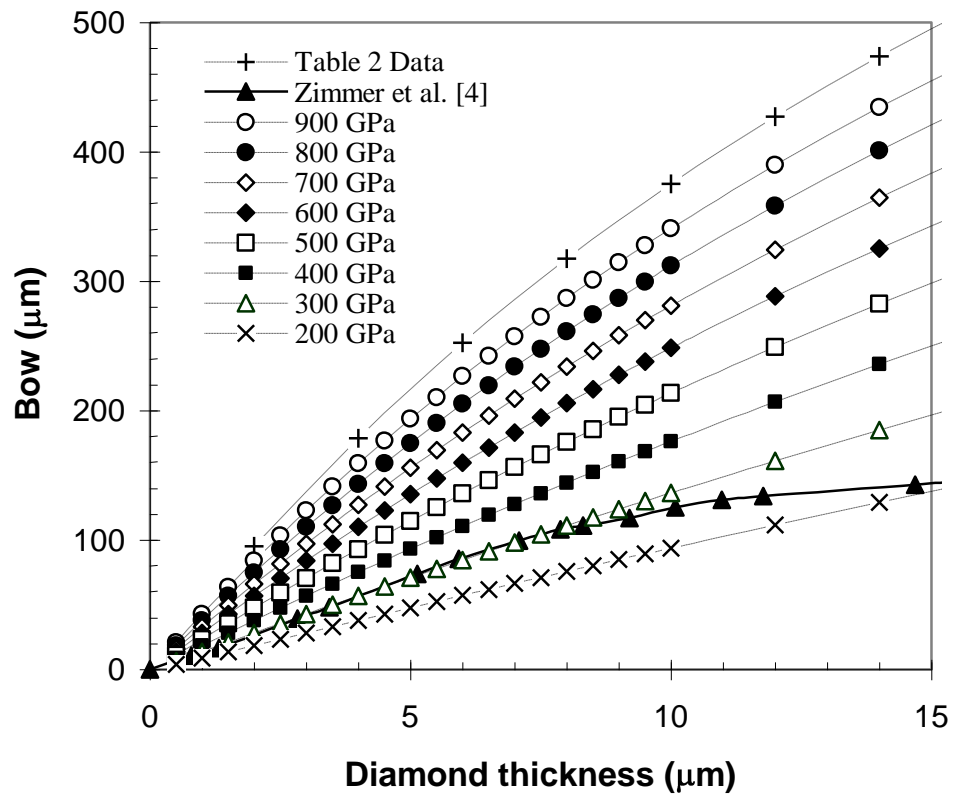


**Figure 3.8** Wafer bow at different growth temperatures based on dimensions in reference [13].

Zimmer *et al* [13] highlighted that a cooler processing temperature (e.g. 715°C) leads to a higher compressive stress in the diamond films and a higher degree of bow compared to 755°C. It was stated that this observation did not correlate with published CTE data for diamond and silicon. However the modelling results in figure 3.8, where bow is only generated by CTE mismatch, clearly demonstrate that higher processing temperatures can lead to reduced bow due to the CTE of diamond being larger than silicon at higher temperatures (Figure 3.5). It was also experimentally observed that the rate of change of stress, and bow, decreased as the diamond film becomes thicker. This is also observed in figure 3.6 and is related to the overall stiffness of the diamond-silicon wafer increasing with increasing diamond thickness. The absolute value of bow in the model is greater than the experimental measurements by a factor of three to four. This could be related to the plastic

deformation of silicon, the diamond film exhibiting a lower elastic modulus compared to the model values or intrinsic stress within the diamond layer. For example, reference [10] reported relatively low elastic coefficients for polycrystalline diamond due to imperfections and impurities.

To examine the influence of changes in the elastic modulus of diamond on bow, the experimental data of Zimmer *et al* [13] was compared with model data for diamond grown at 715°C at different thicknesses on a silicon wafer 525 μm thick and 100 mm diameter [5], figure 3.8. As observed in figure 3.6, the rate of change of bow decreases as the diamond film becomes thicker as observed with the experimental data in figure 3.9 (▲).



**Figure 3.9** Bow as function of diamond stiffness for 525 μm thick Si at 715°C

The best agreement corresponds to a low diamond elastic modulus of 300 GPa, as shown in figure 3.9. Chiu *et al* [127] and Kim *et al* [128] demonstrated that the elastic modulus of diamond CVD films decreased considerably (from 1000 to 300 GPa) with increasing CH<sub>4</sub>/H<sub>2</sub>. Windischmann *et al* [129] indicated that an intrinsic and residual

tensile stress can be present in diamond films grown on silicon which could also influence bow and the level of stress varies with process temperatures and CH<sub>4</sub>/H<sub>2</sub> ratio [29]. Zimmer *et al* [13] reported a decrease in bow with increased diamond thickness as a result of intrinsic stress [12]; the level of the intrinsic stress can depend on quality, growth conditions, microstructure, texture and surface state (roughness) along with non-uniform heating.

### 3.6.2 Experimental Measurements of Wafer Bow at Room Temperature

Forty Si/PD samples were obtained from Element Six (a partner of the MORGaN project) for wafer bow analysis. These wafers were either 15 or 20 mm in diameter, five to six times smaller than the diameter of the FE model wafers. Despite being smaller, these wafers will be suitable for model validation because bow is approximately inversely proportional to the square of the radius and it is straightforward to change the geometry in the model. The PD growth conditions used to fabricate the samples are similar, with the same method being used for PD depositions between 715 and 800°C. However, the geometries vary with each sample having a different PD thickness, Si thickness and wafer radius. The ranges of PD and Si thicknesses, as well as the wafer radii, are contained in table 3.2.

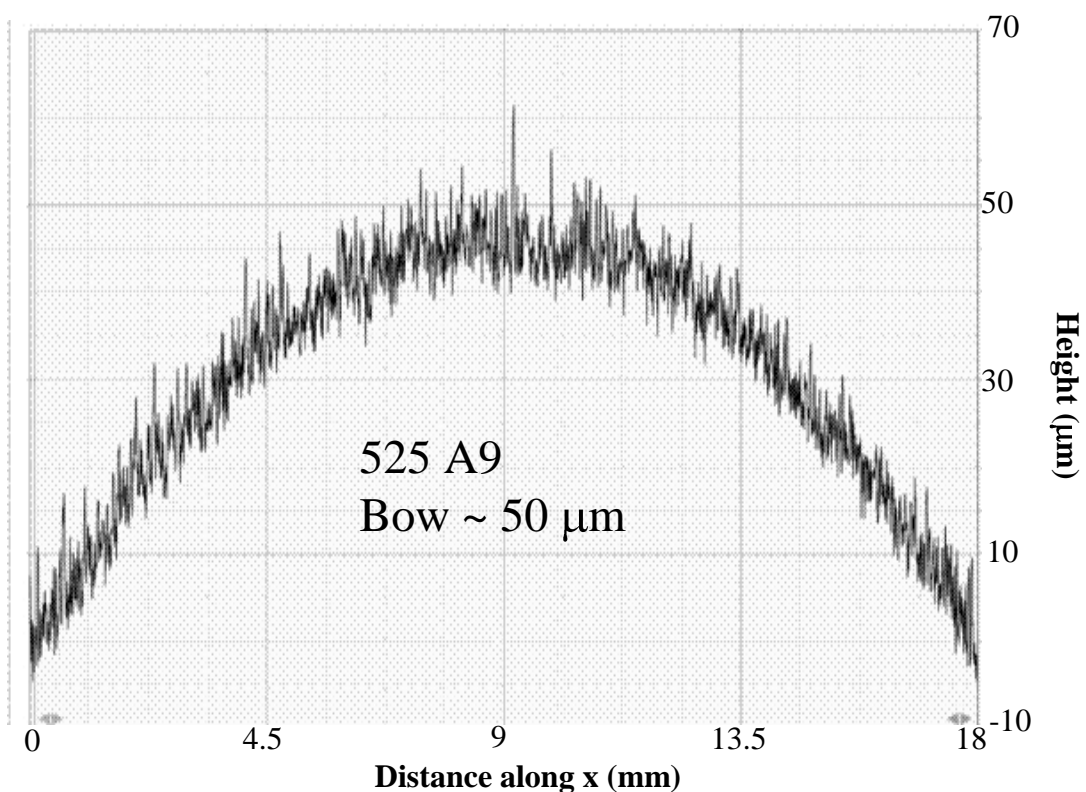
**Table 3.2** Different processing conditions of the Si/PD wafers.

Quantity	Range
PD deposition temperature	715 to 800°C
PD thickness	50 to 110 μm
Si thickness	500 to 550 μm and 600 to 650 μm
Wafer Diameter	15, 20 mm

Firstly, the initial bow of these samples was measured with the chromatic sensor of the Proscan 2000 profilometer and the thickness of the PD layer was then measured using an optical microscope. The profilometer bow measurements were validated with Veeco Dektak measurements taken at the Slovakian University of Technology (STU) in Bratislava. One of the advantages of using a profilometer is that it can scan and measure height differences over an entire wafer over a short period of time (10 to

30 minutes, depending on the size of the wafer). Therefore every wafer obtained from E6 had its entire Si surface scanned and bow measured using a chromatic sensor.

It was impractical to scan the PD surface with the chromatic sensor because it is very rough and clear, meaning that the reflection is weak and a low scan rate is required. Lowering the scan rate reduces the speed at which the wafer can be scanned and high surface roughness also dramatically increases the error in the bow measurement as it produces noise. Directly measuring bow from the PD side using the Dektak is easier because the wafer surface is convex, meaning that the sample is easier to clamp and will not be tilted. At STU, Dektak measurements were successfully taken from the PD side as shown in figure 3.10. The result in figure 3.10 closely agrees with the profilometer measurement, which yielded a bow of  $54.5 \mu\text{m}$ , meaning that both approaches are valid for measuring bow.



**Figure 3.10** Dektak measurement of PD side of sample 525 A9 and agrees with the measurement ( $54.5 \mu\text{m}$ ) taken using the profilometer from the Si side.

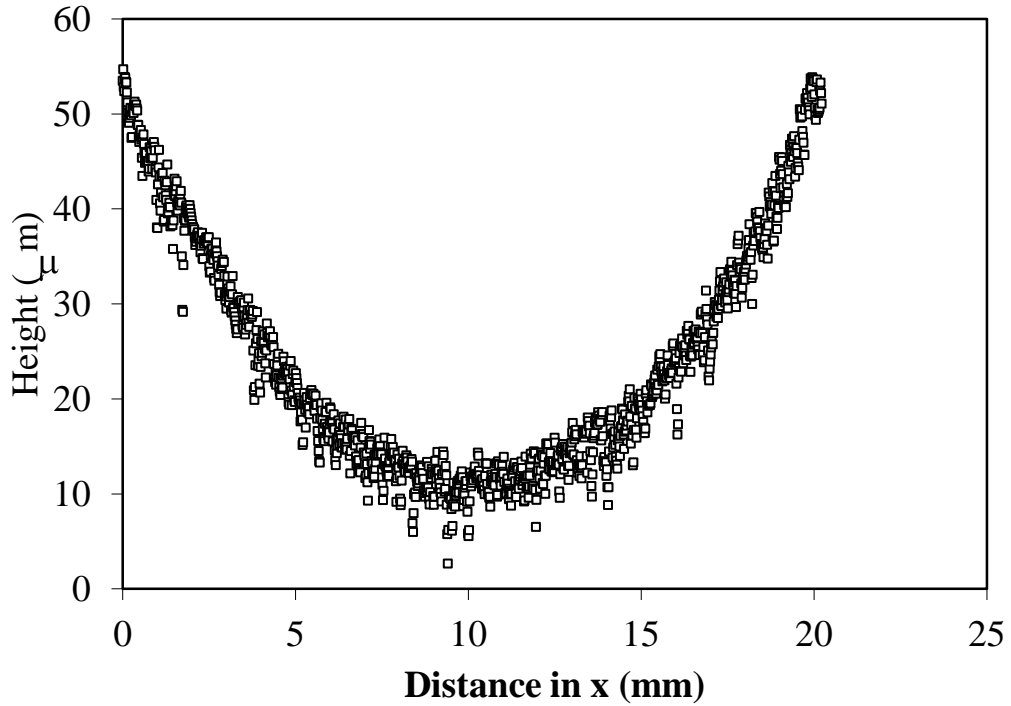


Once a wafer was scanned, a text file was exported from the Proscan 2000 software. The text file contained the height measurements from the wafer as a function of the co-ordinates in the x- and y-directions. The profilometer scans the sample from left to right in the x-axis, before one moving unit (usually about 10 to 20  $\mu\text{m}$ ) downwards. Therefore each full-wafer measurement produces thousands of line scans that can be used to determine the bow. Five random line scans, taken close to the centre of the wafer, were taken from the text file and exported into Microsoft Excel for bow measurement and data analysis.

Figure 3.11 shows a typical line scan of a Si/PD wafer used to determine wafer bow. The bow in figure 3.11 is almost a parabola and the bow could be calculated from the equation for a parabola, which is quadratic and simplifies the bow measurement. This is a reasonable approximation because the model predicts that the bow is proportional to the radius squared, indicating parabolic bow. Two bow measurements are taken from each line scan, one from the left hand side of the wafer and one from the right hand side of the wafer; this is done to cancel out any tilt on the wafer when it is secured onto the Proscan 2000 table. Therefore ten bow measurements were taken from each wafer in total. However, all of the lines had slightly different lengths, these lengths needed to be standardised and bows corrected before the mean bow could be calculated. As bow is proportional to the diameter squared of the wafer, it is straightforward to determine the bow as a function of the standard diameter using equation (3.11).

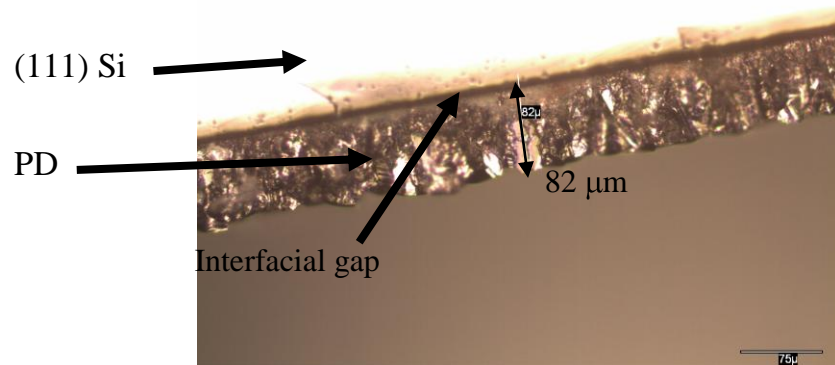
$$b_s = b \left( \frac{d^2}{d_s^2} \right) \quad (3.11)$$

Where  $b$  and  $b_s$  are the measured and standardised bow respectively, and  $d$  and  $d_s$  are the measured line scan length and standardised diameter respectively. These measurements were then standardised to the same wafer diameter so that they were directly comparable and then averaged to give an overall measurement of the wafer's bow.

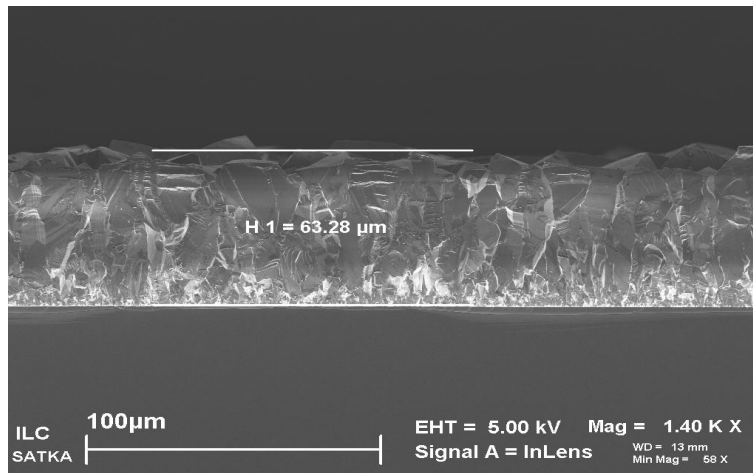


**Figure 3.11** Line scan of a Si/PD wafer taken by the profilometer.

After the bow of every sample was measured, the PD thickness of each sample was measured using an optical telescope, as shown in figure 3.12. The PD thickness was measured so that the bowing data could be directly compared with the FE model. In order to keep the wafers intact for further analysis, the PD thickness was measured from the edge of the wafer. The edges of all of the wafers were dirty, sometimes obscuring the Si/PD interface and making measurement difficult. Therefore the wafer edges were polished by hand using fine, damp SiC paper. This polish was sufficient to remove the dirt residue without significantly damaging the edge of the wafer. As PD has a granular structure, the height of each grain varies and means that multiple height measurements from different regions around the edge of the wafer are required. After 10 height measurements are taken, the height was averaged and the variation (error) in height was noted.



(a)



(b)

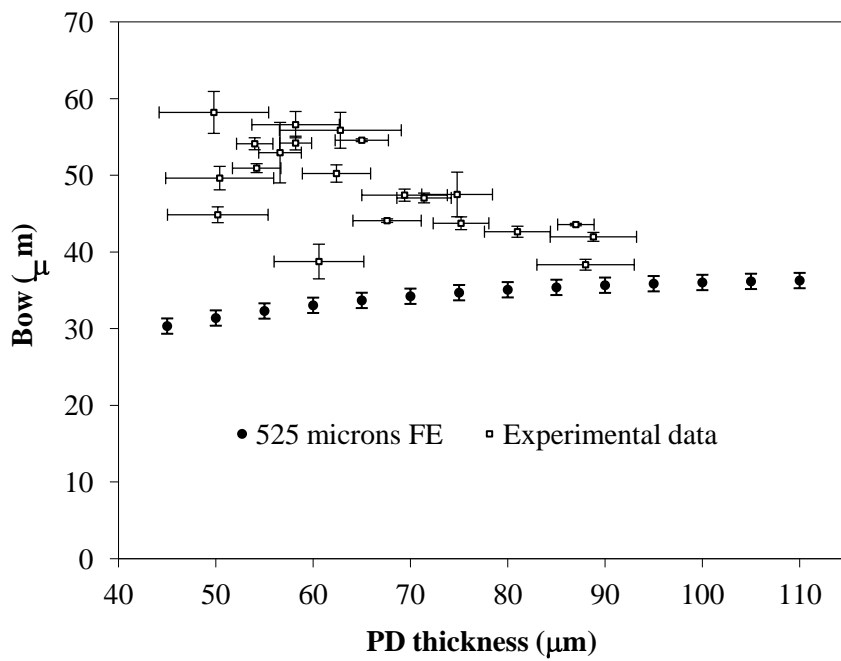
**Figure 3.12** Images of a Si/PD cross-section, where (a) is an optical image, showing a gap between the Si and PD, indicating delamination at the interface and (b) is an SEM image, courtesy of STU, showing the Si and PD bonded at the interface.

As Element 6 provided the Si thicknesses of each sample, meaning that the geometry and bow of each wafer was known, the bow measurements were directly compared with the FE model. The geometry ranges of each sample are described in table 3.2 and the samples were divided into three groups according to geometry to simplify

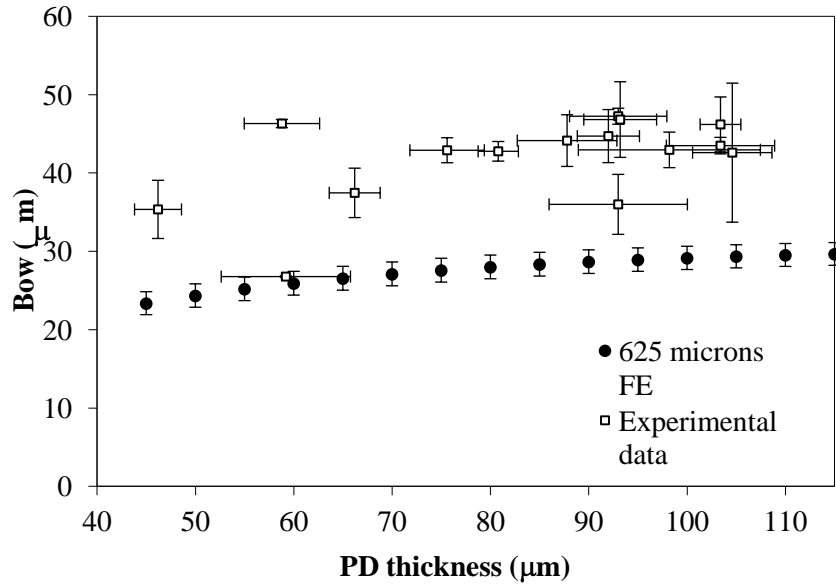
analysis. The results from these three groups are plotted in figure 3.13 and are defined as follows:

- 500 to 550  $\mu\text{m}$  Si thickness, 20 mm wafer diameter
- 600 to 650  $\mu\text{m}$  Si thickness, 20 mm wafer diameter
- 600 to 650  $\mu\text{m}$  Si thickness, 15 mm wafer diameter

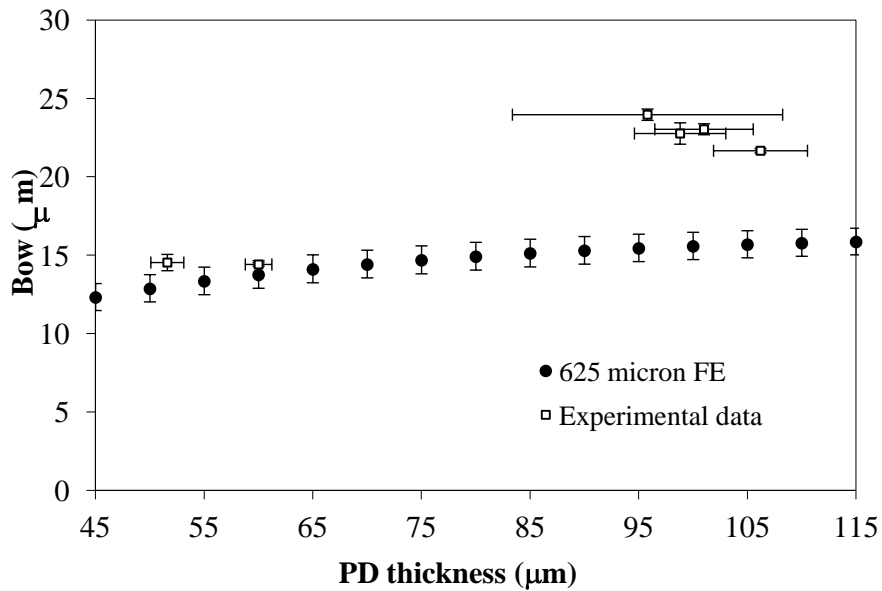
The comparisons between the experimental measurements and FE models are shown in the following graphs.



(a)



(b)

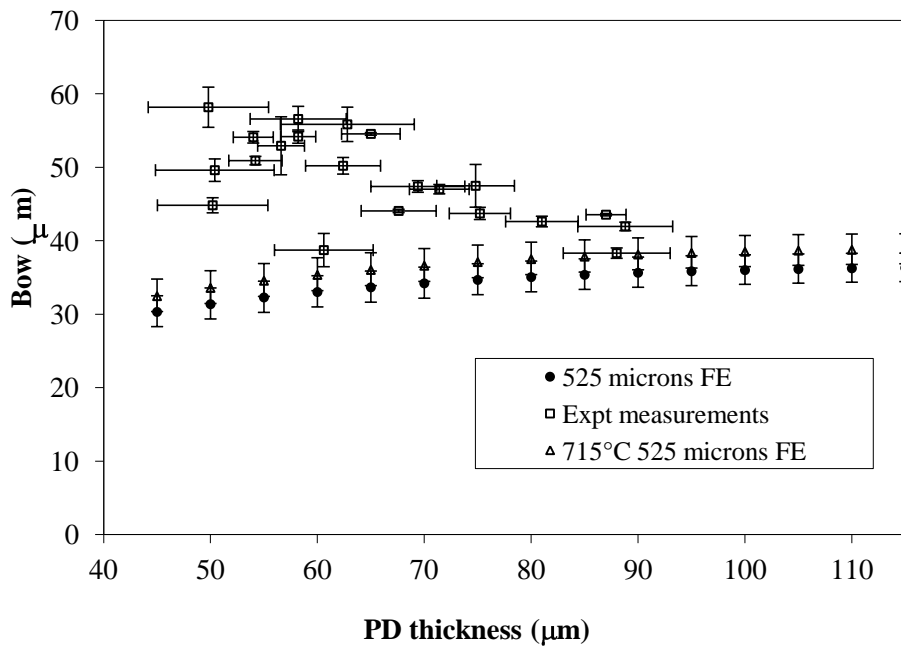


(c)

**Figure 3.13** Comparison between the wafer bows predicted by the FE model and experimentally measured by the profilometer for different geometries. (a) 20 mm diameter 500 to 550 μm Si thickness (b) 20 mm diameter 600 to 650 μm Si thickness (c) 15 mm diameter 600 to 650 μm Si thickness

The results in figure 3.13 show that the FE model consistently under predicts the bow measured experimentally. There are reasons to explain this discrepancy and the model produces results sufficiently close enough to the experimental results for it to be useful for the materials processors. Firstly, the model assumes that the PD was

deposited at exactly 800°C although it could have been deposited at a minimum of 715°C [13]. CTE analysis from figure 3.5 and the results shown in figure 3.8 shows that depositing the diamond at 715°C will actually increase the thermally-induced stress and bow, this is because the CTEs of diamond and silicon overlap, as shown in figure 3.5. Figure 3.14 contains a plot of figure 3.13 (a) with the model's predicted bowing outcome at a PD deposition temperature of 715°C.



**Figure 3.14** Comparison between the wafer bows predicted by the FE model and experimentally measured by the profilometer for different PD thicknesses and deposition temperatures where the wafer has a 20 mm diameter and a 525 micron Si layer thickness.

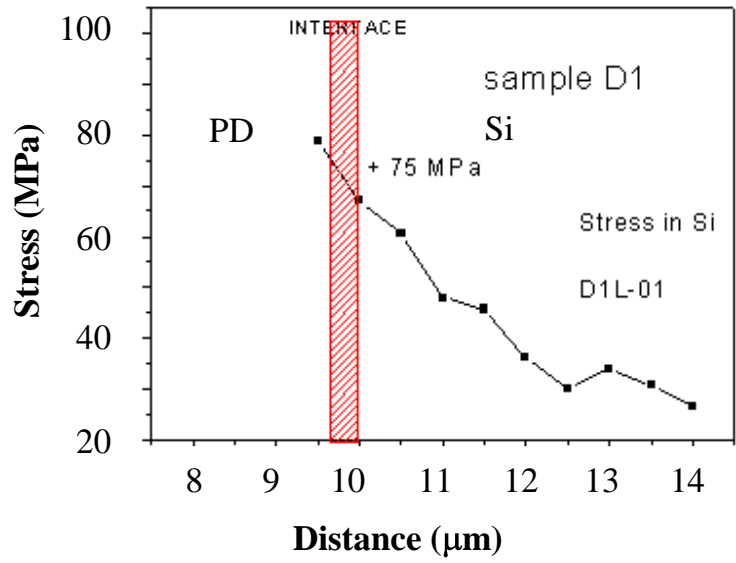
Figure 3.14 shows that reducing the deposition temperature from 800 to 715°C in the FE model is only predicted to increase the bow by 3 to 4 microns, not enough to significantly change the outcome of the model. However, the FE model neglects a few key contributions to the stress in the wafer. Intrinsic stresses develop in the PD layer [13] and these stresses will have an impact on the bow of the wafer. Sources of intrinsic stress include thermal gradients in the composite substrate during CVD growth, interactions between PD grains and the diamond nucleation process [13]. Intrinsic stresses are very difficult to predict and model because they are difficult to

control and vary significantly between samples; so were impractical to incorporate to this work. Overall, the FE model appears to be a good tool for predicting the bow of Si/PD wafers because its bow predictions are within tolerance of the experimentally measured bow and demonstrates that CTE mismatch is a serious challenge with this technology and the resultant bow is a serious issue that needs to be overcome to make Si/PD substrates suitable for GaN-based technologies.

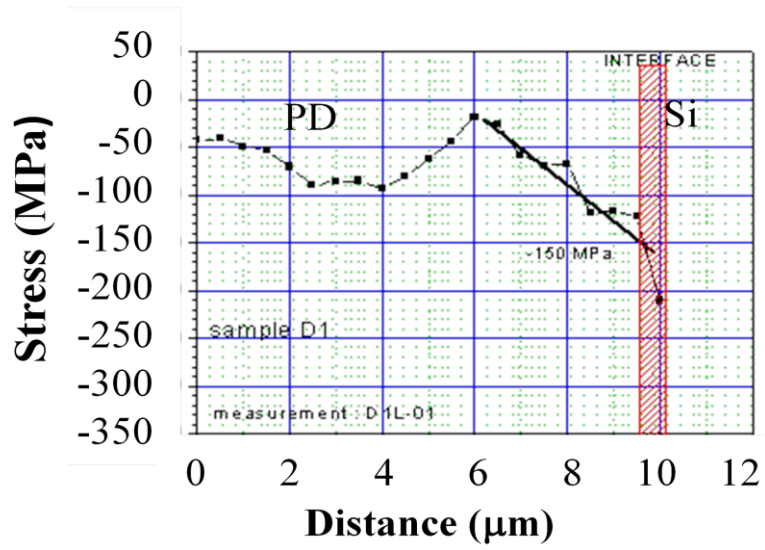
### **3.7 Micro-Raman measurements of Si/PD wafers**

As well as predicting bow, the FE model can also be used to predict stress in a Si/PD wafer. It is excessive stress that causes wafers to fail through cracking. Stress in a Si/PD wafer was also measured using micro-Raman spectroscopy (see section 2.4), which is housed at STU in Bratislava. Five Si/PD samples were sent to STU for micro-Raman analysis. Therefore it is possible to directly compare theoretical and experimental results, as done in figure 3.15.

Three of the samples sent to STU were cleaved in half so that their cross-sections were accessible; this was a requirement in order to measure the cross-sectional stress inside the wafer. The cross-sectional stress is the same as the stress parallel to the interface predicted by the FE model. In micro-Raman spectroscopy, the stress along the cross-section of a wafer is determined by measuring the shift in the characteristic Raman spectra of the material. This shift occurs because strain causes the crystal lattice to deform, slightly increasing the inter-atomic distance for a crystal under tension and vice versa. In brittle elastic crystalline materials, such as those used in this project, the stress in the material lattice can be calculated using Hooke's law. In order to measure the Raman spectra to a sufficient resolution that the strain-induced wavelength shifts are clearly measurable, the laser has to be finely focussed. The laser used by STU for micro-Raman spectroscopy has a minimum spot size of 1  $\mu\text{m}$ , meaning that it has high enough resolution for stress measurements.

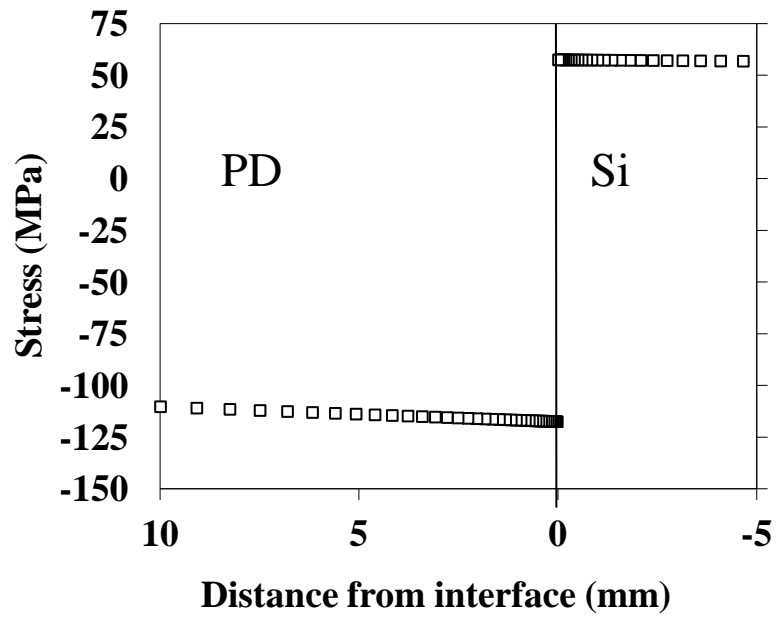


(a)



(b)





(c)

**Figure 3.15** Comparison between the cross-sectional stress measured by micro-Raman spectroscopy and the stress predicted by the FE model. (a) Cross-sectional stress in Si measured by micro-Raman. (b) Cross-sectional stress in PD measured by micro-Raman. (c) Cross-sectional stress in Si and PD predicted by the FE model of the same geometry.

The micro-Raman measurements of sample 15/100/625A1 were compared with the predicted results from the FE model for a wafer of near identical geometry and the results are shown in figure 3.15. As the individual grain heights in the PD vary by 10 to 15%, it is impossible to use the exact geometry in the FE model. After measuring the grain heights and Si thickness of the sample by optical microscopy, the dimensions used for the model were 100  $\mu\text{m}$  PD, 625  $\mu\text{m}$  Si and a wafer diameter of 15 mm. Table 3.3 contains the maximum stress measured by micro-Raman and predicted by the model.

**Table 3.3** Comparison between the maximum magnitude of stress in the Si and PD predicted by the FE model and measured by micro-Raman model. A positive stress denotes tension and a negative stress denotes compression

<b>Material</b>	<b>Micro-Raman maximum stress (MPa)</b>	<b>FE model maximum stress (MPa)</b>
Si	+75	+57.5
PD	-150	-118

The model assumes that the interface between Si and PD is perfect. This means that the bond adhesion strength is infinite and there are no voids at the Si/PD interface, whereas in reality the bond adhesion is finite and there are voids in the Si/PD interface. However, there is reasonable agreement between the maximum stress magnitudes measured experimentally by micro-Raman and theoretically by FE analysis, which considering the idealised assumptions made by the FE model, is a good result. This, coupled with the wafer bow results, implies that the assumptions made when programming the FE model are acceptable and produce reasonably accurate predictions. Therefore the FE model can be used to predict the experimental behaviour of Si/PD wafers to a good degree of accuracy.

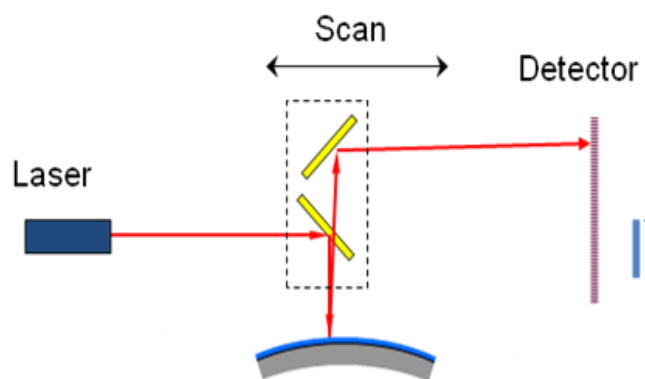
However, figure 3.15 does show a divergence between predicted and experiment behaviour in the wafer. The stress in both the Si and PD layer shows a more rapid than expected decay in stress. The PD layer in particular shows significant fluctuations in stress within the material, which can be explained by its polycrystalline, composite structure. PD consists of diamond grains interspersed with small amounts of graphite, and the diamond grains have some freedom of movement because they are relatively weakly bonded to each other and graphite is much less stiff. Therefore this movement of diamond grains leads to random areas where excessive stress can build up or areas where the stress is much lower than expected. Additional effects such as an imperfect interface will also lead to some divergence between the theoretical and experimental results. The imperfect interface partially explains why the stress is higher than expected at the interface and then goes through a steeper than expected decay in both the Si and PD. The lower stresses in the FE model are correlated with the lower bow predicted by the model.

### 3.8 FE and experimental measurements of wafer bow above room temperature

Further validation of the model was performed by using the model to predict the stress profile and bowing behaviour of a Si/PD wafer. A Si/PD sample was then subjected to heating from room temperature to 450°C at ITE in Poland, who were also part of the MORGaN consortium. The high temperature measurements were undertaken on 20 mm diameter Si/PD samples and a 1 cm<sup>2</sup> Si/PD sample released from an SOI wafer, described in section 4.7.

#### 3.8.1 High Temperature Measurement System

The high temperature bow measurement system is a Tencor FLX 2320 system that employs a 750 nm wavelength laser to take the measurement. The tool scans the surface of the sample with a laser beam and measures the angle of deflection of the laser beam as it scans along the sample, allowing it to determine the shape and bow of the sample. An experimental schematic of the high temperature bow system is shown in figure 3.16. This experiment takes place in a furnace so that measurements can be taken up to a maximum of 500°C.



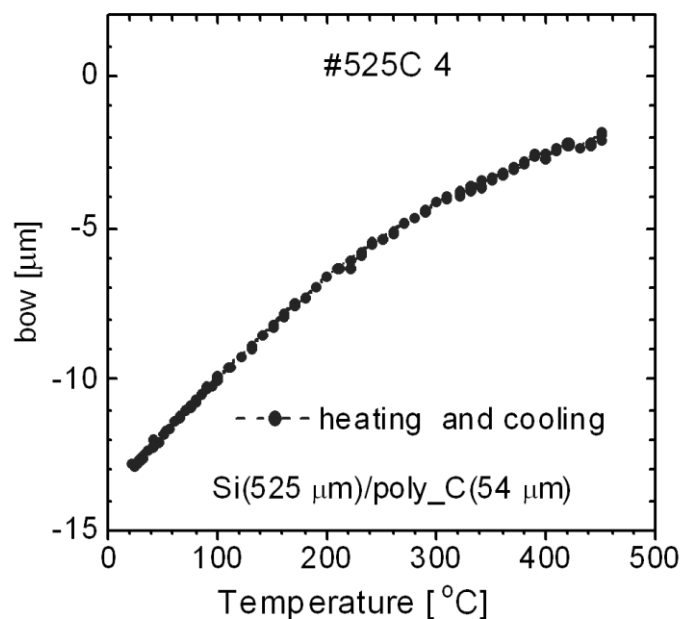
**Figure 3.16** Experimental schematic for the high temperature wafer bow measurements taken at ITE. (Image courtesy of ITE)

### 3.8.2 Results of the high temperature wafer bow measurements.

Si/PD samples 20/100/525C1 and 20/100/525C4 had their Si surfaces polished using fine SiC paper to ensure a smooth, reflective surface. These samples were then sent to ITE for high temperature wafer bow analysis using a laser-based system. This work was done externally because the University of Bath does not possess similar equipment. The PD layer thicknesses were measured using the optical microscopy method described in sub-section 3.6.2 and the total thickness was measured after polishing using a micrometer to determine the average thickness of the Si. These measurements are shown in table 3.4.

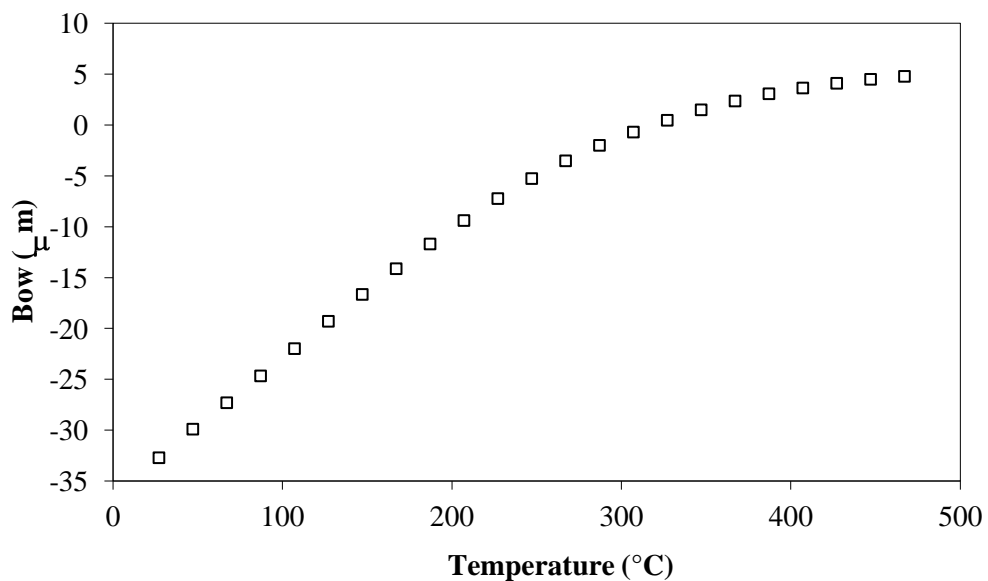
**Table 3.4** The respective layer thicknesses of the Si/PD samples used for the HT wafer bow measurements

Sample	Average Si thickness ( $\mu\text{m}$ )	Average PD thickness( $\mu\text{m}$ )
20/100/525C1	460	54.2
20/100/525C4	525	54.0



**Figure 3.17** Measurement of the change in wafer bow for Si/PD for sample 20/100/525C4 between room temperature and 450 $^{\circ}\text{C}$ .

Figure 3.17 contains wafer bow measurements for the two Si/PD samples taken between room temperature and 450°C during both the heating and cooling cycles. Figure 3.17 shows that there is little discrepancy between the heating and cooling measurements; this strongly indicates that both materials exhibit very little plastic deformation. The bow of 20/100/525C1 changes from -3 μm (Si tensile) to 14 μm (Si compressive) and from -13 to -2 μm for 20/100/525C4 as the temperature is increased to 450°C. The bow of samples 20/100/525C1 and 20/100/525C4 before polishing were measured as 50.93 and 54.11 μm respectively. The initial bow of both samples was quite low because the Si polishing was uneven due to pre-existing bow, with the wafer edges having more material removed. Therefore polishing the Si to a smooth surface had a flattening effect on the wafer and means that the wafer will not be flat at the point where the Si and PD CTEs cancel each other out. However, it is still possible to further validate the model through the experimental results by directly comparing the change in values and the curve of the graphs in figures 3.16 and 3.17.



**Figure 3.18** FE wafer bow simulations of a wafer with similar dimensions to 20/100/525C4 at temperatures between 27 and 467°C.

Comparison between experimental results, shown in figure 3.17, and FE model predictions, shown in figure 3.18, show that although the FE model clearly shows the experimental trend, it predicts a change in bow of 38 μm for sample 20/100/525C4.

This compares to an experimental bow change of 13  $\mu\text{m}$  for 20/100/525C4, showing that in this case the FE model over-predicts the change in bow by an approximate factor of 3.

Although this initial discrepancy appears to be large, it can be explained by the same mechanism described previously. The FE model assumes that the PD layer is one continuous solid perfectly bonded to the Si, whereas in reality this PD consists of small grains a few microns in size that are nucleated on a specifically prepared Si surface. Therefore PD will behave differently to a homogenous layer of bulk diamond. The CVD process used for PD growth and the interaction of PD grains cause large amounts of intrinsic stress in the PD layer that cannot be accurately modelled at present, as mentioned in section 3.6. These intrinsic stresses can be either net tensile or compressive and will have a significant bearing on wafer bow, resulting in deviations between the results predicted by the FE model and what is actually measured experimentally. Furthermore, due to the difficulty of obtaining these properties experimentally, the FE model relies on material properties found in the literature and these properties naturally vary between two samples of identical materials due to imperfections such as voids and grain boundaries. These changes are usually small, but in the case of Si and PD where the CTEs are relatively small and overlap, any differences in the agreed CTEs of bulk diamond and the actual CTEs of the PD on the samples will be exaggerated. Over large temperature ranges, this could lead to noticeable differences in predicted and experimentally observed bow. PD is a very strong and stiff material that is extremely rigid compared to Si; this additional comparable strength to Si may have a damping effect on the bow that the model does not take into account.

### **3.9 Concluding Remarks**

This chapter describes a FE model developed to describe the bowing behaviour and stress/strain distribution within a Si/PD composite wafer. The model can be used to demonstrate and predict processing issues with this new type of substrate. In order for the substrate to be compliant with GaN power HEMT technologies, the PD layer needs to be at least 40  $\mu\text{m}$  thick and a Si layer thickness of 1 – 5  $\mu\text{m}$ . In reality,

getting a substrate with suitable layer thicknesses for GaN-based technology is difficult due to large stresses resulting from CTE mismatch and intrinsic stresses within the PD. As the wafer is thinned at room temperature, it starts to bow excessively in order to reduce stress in the system and this eventually leads to delamination or the wafer cracking if forced flat. The FE model confirms these experimental observations.

The FE model is a modification of the principles behind a bimetallic strip. These concepts have successfully been applied to the Si/PD composite wafer that consists of new, more modern materials. The FE model obtains near-perfect agreement with an analytical method devised from Hsueh's papers [123, 125] on thermal stresses in multi-layers, successfully demonstrating self-consistency. Additionally, micro-Raman stress measurements have shown that the FE model predicts stress values in both the Si and PD layers close to the interface. Bow measurements taken of 40 samples at room temperature, show that the model is good at predicting the bow when the Si layer is thick. Additionally, laser measurements taken of bow taken between room temperature and 450°C show the model correctly predicts that the wafer bow decreases when heated.

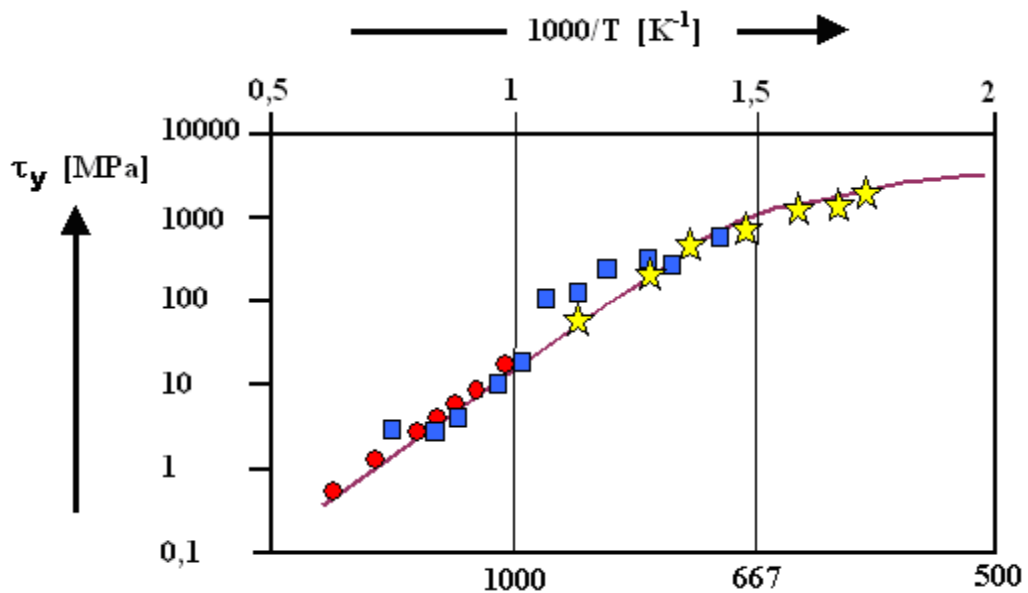
As with most models, there were some simplifications and assumptions were made due to the difficulty of modelling some of the effects that actually occurs inside the wafer. The model assumes that both the materials are perfectly elastic, has a perfectly bonded interface, consists of two continuous layers of material and is stress free at a uniform PD nucleation temperature. Most of these assumptions are inaccurate, but on balance the experimental results suggest that the relatively simple FE model is a very useful tool for predicting processing issues and explaining the experimentally observed behaviour of new, novel substrates.

**The next chapter will discuss possible methods for overcoming problems related to creating viable Si/PD composite substrates described in this chapter.**

**CHAPTER 4: CREATION OF SI/PD WAFERS SUITABLE FOR GAN  
GROWTH AND DEVELOPMENT OF A SILICON ON INSULATOR (SOI)  
APPROACH FOR OVERCOMING DELAMINATION AND SI CRACKING**

**4.1 Introduction and Motivation**

Lapping silicon wafers with a polycrystalline diamond layer from a bulk thickness of 500 to 650  $\mu\text{m}$  to the desired thickness of approximately 2  $\mu\text{m}$ , is difficult because the wafer will delaminate due to poor surface adhesion between the silicon and PD, or crack due to the stresses in the silicon (discussed in chapter 3). The silicon could also crack because the wafer has to be clamped for lapping and the material is significantly weakened by the preparation process for diamond nucleation. The nucleation process reduces the yield strength of the silicon (Si) layer from 2 GPa (see figure 4.1(a)) to around 100 MPa at room temperature [130]. Therefore, a method for controlling the stresses and bow of the composite Si/PD wafer had to be developed and silicon-on-insulator (SOI) provides a route for achieving this goal. The basic schematic of an SOI wafer is shown in figure 4.2.



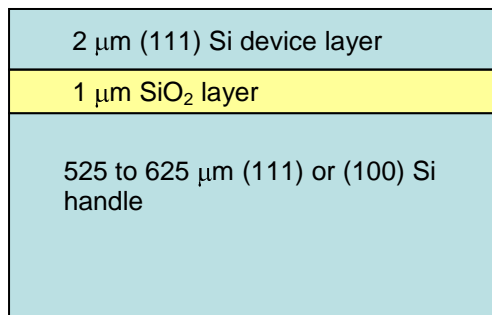
(a)





(b)

**Figure 4.1** (a) Yield strength of silicon with respect to temperature and (b) a Si/PD wafer damaged during processing (images courtesy of Element Six Ltd).



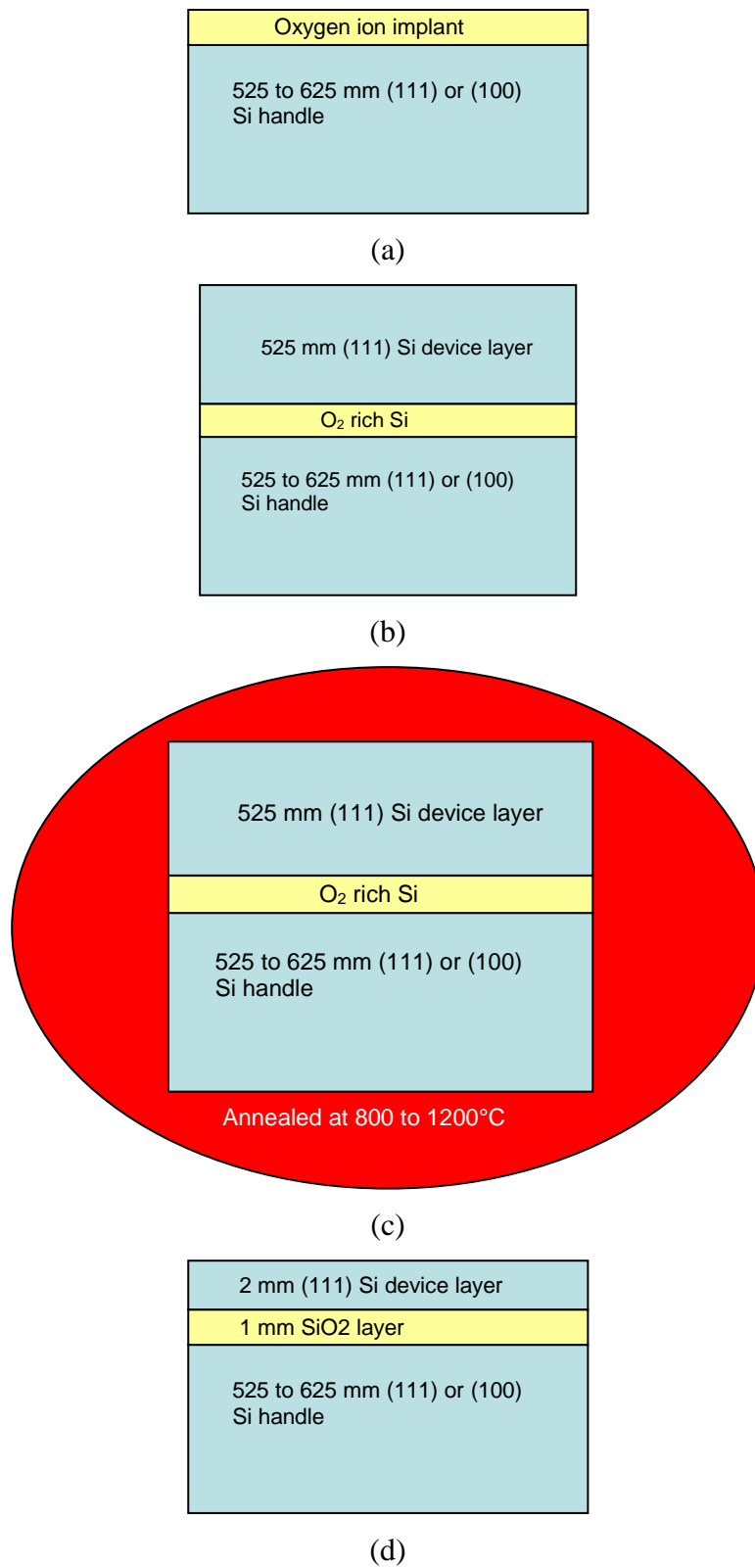
**Figure 4.2** A schematic drawing of the SOI wafer structure.

This chapter will describe the development of crack-free Si/PD composite substrates through the use of SOI wafers, starting with the attempt to separate the thin Si device layer from the much thicker Si handle using HF acid to etch through the SiO<sub>2</sub> interlayer. This method caused the Si device layer to radially crack and the underlying reason for the cracking is understood using finite element (FE) modelling. The FE model is used to consider alternative methods aimed at controlling the cracking and delamination in these structures. This means that promising methods of stress mitigation can be attempted experimentally, and less promising methods are discarded.

Ultimately, through improvements in the polycrystalline diamond nucleation process and the acquisition of SOI wafers with a (100) orientated handle and (111) device layer it is possible to fabricate Si/PD composite wafers with a 2  $\mu\text{m}$  thick (111) Si layer. Such a structure would be ideal for high power devices based of GaN since the GaN can be epitaxially grown on the (111) Si layer and high thermal conductivity of the diamond can be utilised for heat extraction. This composite Si/PD substrate can be realised using an anisotropic wet KOH etch, which will be used to remove the (100) Si handle. It will be shown that it is possible to grow a crack free layer of III-nitride, indicating that it is possible to fabricate a HEMT structure on these substrates. From the point of view of this project, developing HEMT material on a diamond-based substrate will be extremely beneficial and have numerous applications in harsh environment sensing.

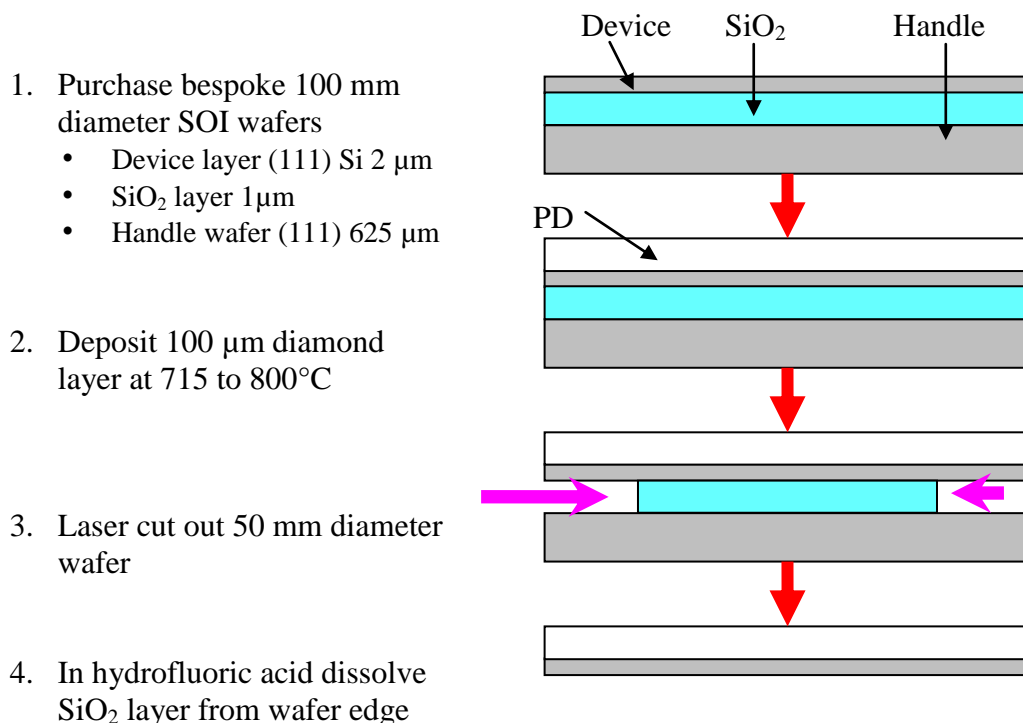
#### ***4.1.1 Basic Description of the SOI process***

A basic schematic of the SOI creation process is shown in figure 4.3. An SOI wafer consists of a 'handle' of 625  $\mu\text{m}$  of (100) or (111) orientated Si, a 1  $\mu\text{m}$  layer of thermally produced  $\text{SiO}_2$  and a  $2 \pm 0.5$   $\mu\text{m}$  (111) Si 'device' layer. These wafers are typically produced by a process called SIMOX [131], or alternatively by silicon fusion bonding (SFB) [132, 133] or 'smart cut' [134]. There are variations in how SIMOX wafers are produced by different companies [135-137], but the basic process is similar. Firstly, the top of the Si handle wafer is oxidised by  $\text{O}_2$  implantation, as shown in figure 4.3 (a) at 800 to 1200°C, producing an  $\text{O}_2$  rich layer. The Si/ $\text{O}_2$  rich layered wafer is then bonded to another Si wafer at room temperature typically by Van der Waals forces, indicated in figure 4.3 (b) [135-137]. This bonded double-wafer structure is then annealed at a high temperature of approximately 800 to 1200°C, as shown in figure 4.3 (c), to strengthen the bonds between the layers and to convert the  $\text{O}_2$  rich layer into  $\text{SiO}_2$  [135-137]. After annealing, the top device layer is reduced to the desired thickness either by using either a mechanical or chemical thinning method depending on how the SOI wafer was produced, see figure 4.3 (d).



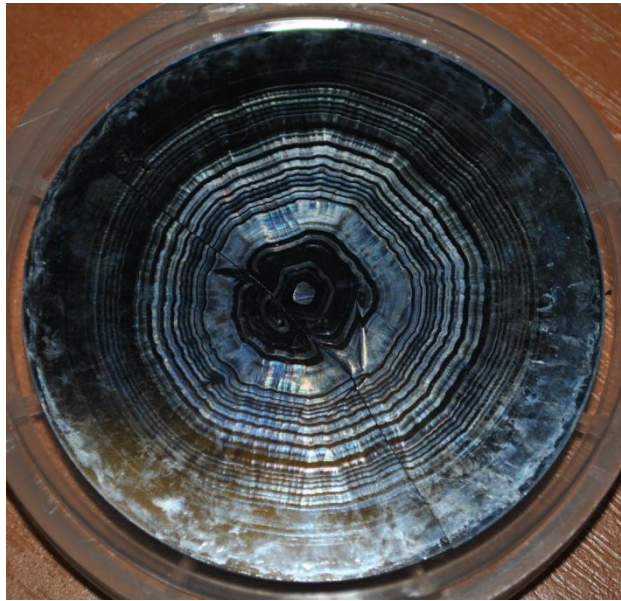
**Figure 4.3** Schematic of the basic silicon-on-insulator (SOI) fabrication process.

## 4.2 Initial SOI process for realising Si/PD substrates



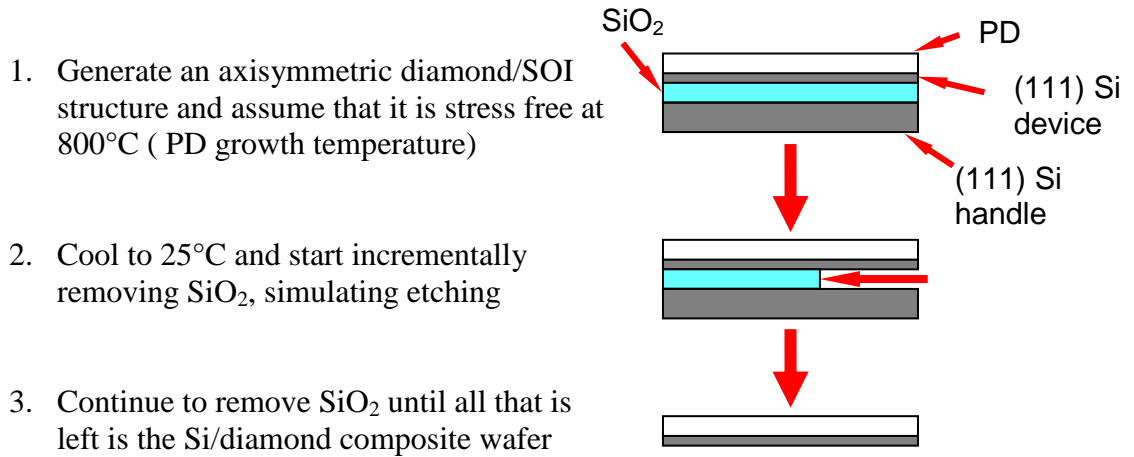
**Figure 4.4** Experimental method for the initial attempt at producing thin (111) Si/PD substrates.

Initially, a layer of PD between 50 and 100  $\mu\text{m}$  was deposited by chemical vapour deposition (CVD) on the (111) Si device layer at  $\sim 800^\circ\text{C}$ . This was undertaken by Element 6, a partner of the MORGaN project. The SOI wafer had a diameter of 100 mm, which is the size required by the CVD reactor. After the CVD deposition of the PD, the SiO<sub>2</sub> layer of the SOI substrate was etched from the side using a buffered HF solution. As the etching process was operating on such a small surface area, it took roughly two weeks to complete. Although it was possible to release a Si/PD wafer with a thin Si handle layer, the Si surface was significantly damaged with circular rings of cracking, which had a 'tree-ring' like appearance, and some delamination at the centre. This meant that the surface quality of the silicon surface was too poor for GaN epitaxial growth. Figure 4.5 contains an image of the surface of one of the released wafers and demonstrates why overcoming this problem is important.



**Figure 4.5** Image of a 50 mm diameter Si/PD wafer released for a SOI wafer, showing the damage done to the Si device layer in the form of circular cracks.

It was therefore important to understand why the substrate gets damaged as it is released. The approach chosen for determining the cause of the ‘tree ring’ cracks and central delamination was to apply the FE model to the problem. The FE model has been successfully applied to the wafer bow problem and micro-Raman measurements in chapter 3 and these show that it predicts sensible values for the stress distribution within the Si/PD wafer. A suitable method for modelling the HF etching process was devised and schematic of this is shown in figure 4.6, with table 4.1 containing details of the dimensions used in the model.



**Figure 4.6** Schematic of the method used to model the removal of SiO<sub>2</sub> and predict stress development in the wafer.

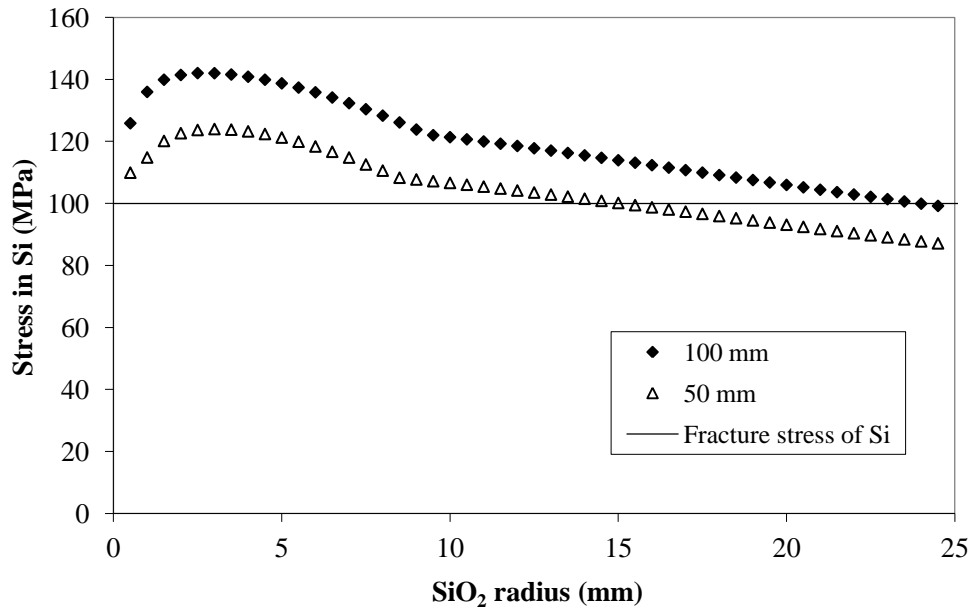
**Table 4.1** Layer thicknesses and wafer dimensions used in SiO<sub>2</sub> removal model (courtesy of confidential data from Element Six Ltd)

Quantity	Dimensions
Wafer diameter	50 mm
PD thickness	50 or 100 μm
(111) Si device layer thickness	2 μm
Thermal SiO <sub>2</sub> thickness	1 μm
(100) Si handle thickness	625 μm

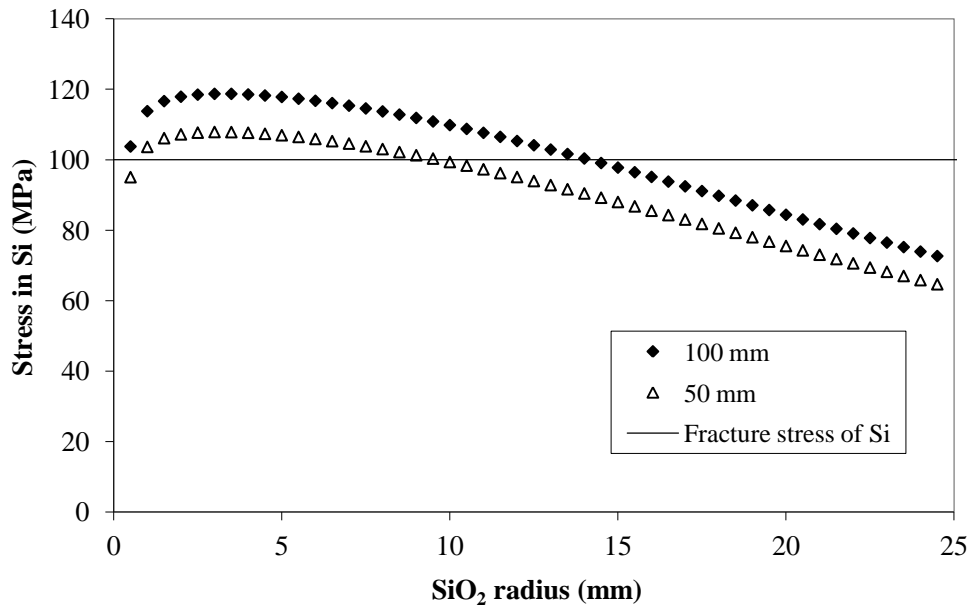
The model shown in figure 4.6 assumes that the thermal SiO<sub>2</sub> layer is formed at 800°C and there are no residual stresses in the SOI wafer prior to PD growth. This is reasonable assumption because this layer is usually produced at 800 – 1200°C and is relatively compliant [138]. The dimensions shown in table 4.1 are those of the experimental wafer’s dimensions as possible, to ensure that the model is accurate. Using the SiO<sub>2</sub> removal model it is possible to predict the stress in the entire wafer as the SiO<sub>2</sub> is removed by the KOH etching, with particular interest in measuring the stress of the device layer where the failure occurs. The SiO<sub>2</sub> was removed in sequential steps in the model and the peak stress in the device layer was measured as a function of the remaining SiO<sub>2</sub>. Figure 4.7 shows plots of the stress parallel to the interface, which causes cracking if sufficiently large, and shear stress, which can cause delamination particularly when bond adhesion is poor.

For guidance a line has been added to the graph at 100 MPa [130] to indicate where the Si device layer is likely to fail. This is a factor of 20 lower than conventional failure stress of Si in the literature, as shown in figure 4.1. The reason for this is that in order to achieve diamond nucleation on the surface of the (111) Si, it is scratched with a diamond-based grit. This process introduces imperfections and fracture initiation sites into the Si, dramatically lowering its fracture strength. Measurements by Element Six suggest that the nucleation process reduces the fracture strength of the Si to 100 MPa [130]; hence why the Si cracks easily after being bonded to diamond at 800°C and cooled to room temperature.

As figure 4.7 (a) shows, stress builds up in the (111) Si as the SiO<sub>2</sub> is etched i.e. as the SiO<sub>2</sub> radius is reduced from its initial value of 25 mm to 0 mm. When the polycrystalline diamond is 100 µm thick, the stress exceeds 100 MPa once 2 µm of SiO<sub>2</sub> has been removed from the edge. Beyond this period the tensile stress causes cracks in the thin Si film. This correlates with what is seen experimentally in figure 4.5, where the edge of the wafer is free of tree ring cracks. In addition, the model predicts that stress increases in the wafer as etching moves towards the centre, this correlates with the higher density of rings near the centre of the wafer as shown in figure 4.5. The situation is improved when the diamond thickness is reduced to 50 µm, where cracking should not start to occur until 10 µm has been removed from the wafer's edge and the peak stress is 12% lower. This suggests that reducing the diamond thickness reduces the density of tree ring cracks and there will be a large enough region around the edge that is not affected by cracking. However, this situation is not ideal and an alternative processing method is required.



(a)



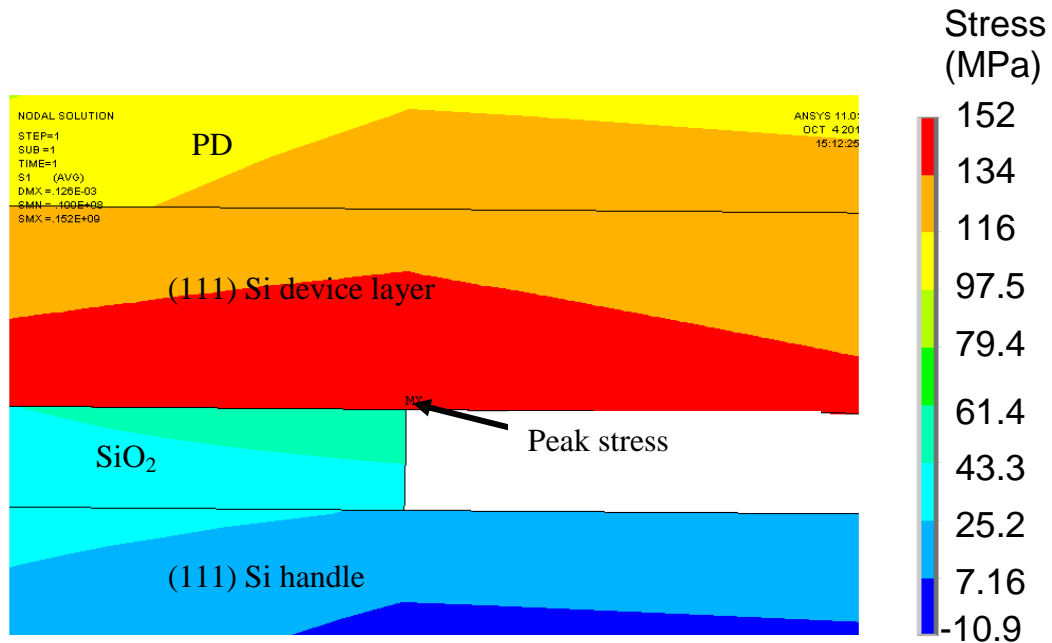
(b)

**Figure 4.7** Maximum predicted stress in the (111) Si device layer in the FE model (a) Stress parallel to the interface (b) Shear stress.

Figure 4.7 (b) suggests that there is a large enough build up of shear stress near the centre of the wafer to cause delamination. Figure 4.5 shows that the Si layer has a

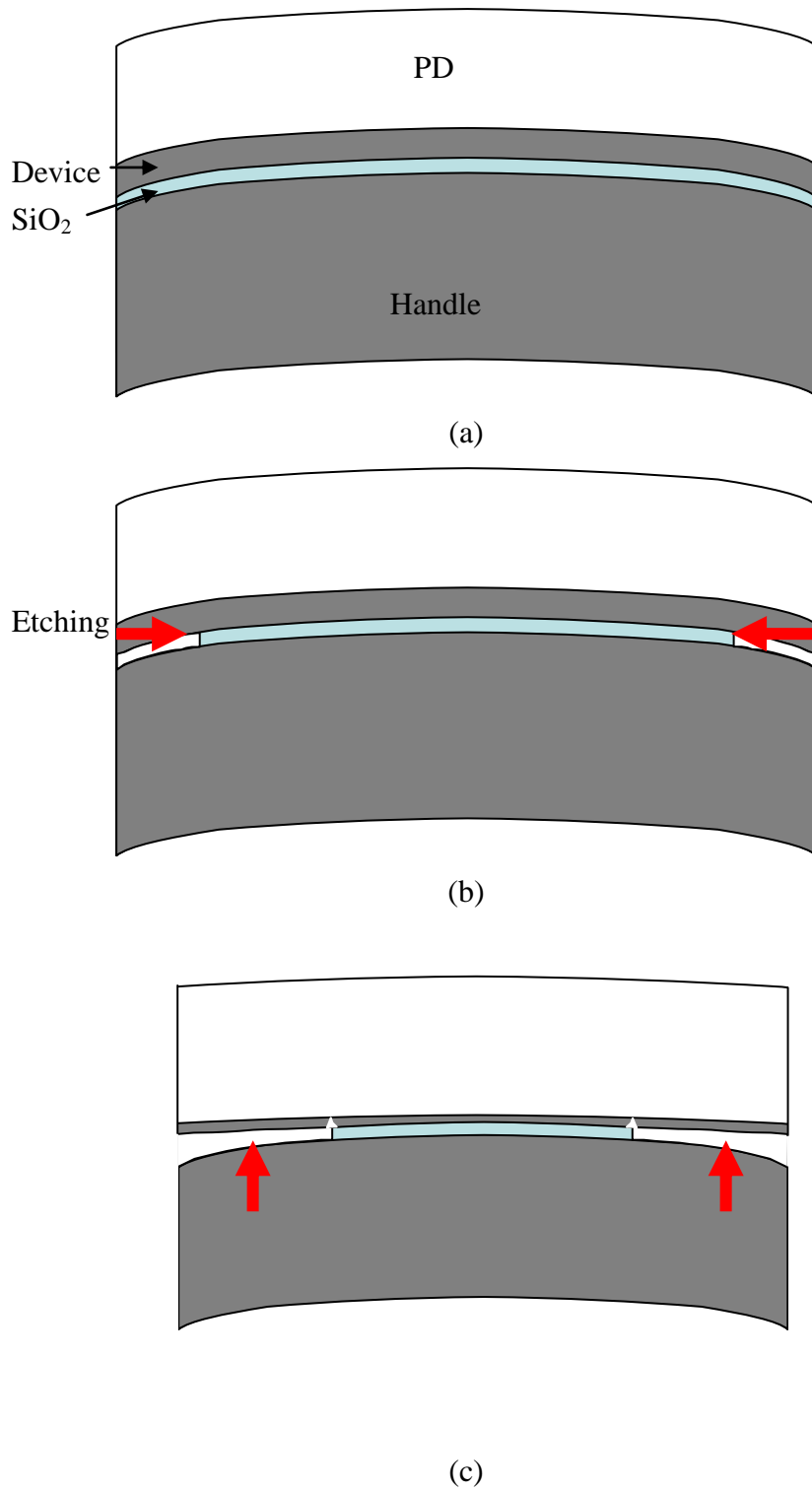


hole in the centre, meaning that the silicon has delaminated. This indicates that the Si/PD interface is weak in this region and liable to delaminate under a small amount of force. The Si/PD interface is liable to delamination due to poor bond adhesion between Si and PD [120].



**Figure 4.8** Image from the SiO<sub>2</sub> HF etch model, showing the peak stress in the direction parallel to the interface.

The peak stress in the wafer occurs in the Si device layer where it meets the outer edge of SiO<sub>2</sub> as it is being etched, as shown in figure 4.8. This shows that the tree ring cracks are directly caused by the HF etching method. The reason why the HF method causes the wafer to crack is drawn in figure 4.9, figure 4.9 (a) shows that the wafer is bowed at room temperature before the start of the HF etch. The wafer is then placed in an HF solution, with starts to etch through the SiO<sub>2</sub> (see figure 4.9 (b)). The PD and Si device layers above where the SiO<sub>2</sub> has been etched straightens because a structure with 2 μm of Si and 100 μm of PD bows less than a structure with 625 μm of Si and 100 μm of PD, as shown in figure 3.6. This effect causes a large build up of stress where the outer edge of the etched SiO<sub>2</sub> is in contact with the Si device layer, as shown in figure 4.8.



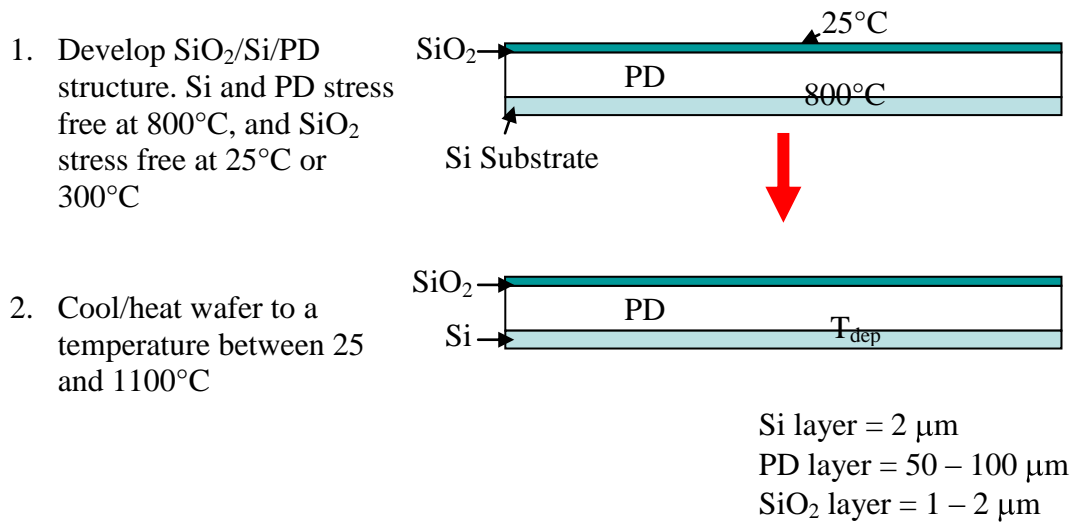
**Figure 4.9** Diagram showing why the wafer fails during the HF etch. In (a), the wafer has just cooled to room temperature after PD nucleation. The HF etch starts to remove the SiO<sub>2</sub>, as shown in (b). Eventually the progression of the HF etch causes the Si device layer to crack as shown in (c).

This stress can be large enough for cracks to form in the Si device layer, as shown in figures 4.8 and 4.9 (c). These cracks are likely to be circular, as shown in figure 4.5, because the wafer is circular and different geometries change the shape of the cracks. Therefore an alternative method for releasing the device layer; or a way to protect the device layer from either the HF etch or diamond nucleation needs to be found. Additionally a method for improving Si/PD bond adhesion is required to reduce the risk of delamination.

### **4.3 Potential methods for releasing an intact (111) Si layer from a Si/SOI wafer**

Although it has been shown that it is possible to produce a (111) Si layer on PD with the target thickness, the damage to this layer is too significant and unpredictable to grow GaN for sensors or power-HEMTs. Therefore either a method to crack the Si device layer in a controllable manner or completely protect the Si from damage needs to be devised. A potential method for protecting the Si device layer is to deposit a layer of SiO<sub>2</sub> on the free PD surface. The Si device layer could also be protected from nucleation and wafer release damage by using a thin layer of compliant material between the Si and PD. This layer would need to be compatible with PD nucleation, have low CTEs and be relatively compliant.

### 4.3.1 Method 1: Depositing SiO<sub>2</sub> on free PD surface



**Figure 4.10** Schematic of method used to model the effect of depositing a layer of SiO<sub>2</sub> on the free PD side, for simplicity the SOI wafer was treated like a continuous Si wafer.

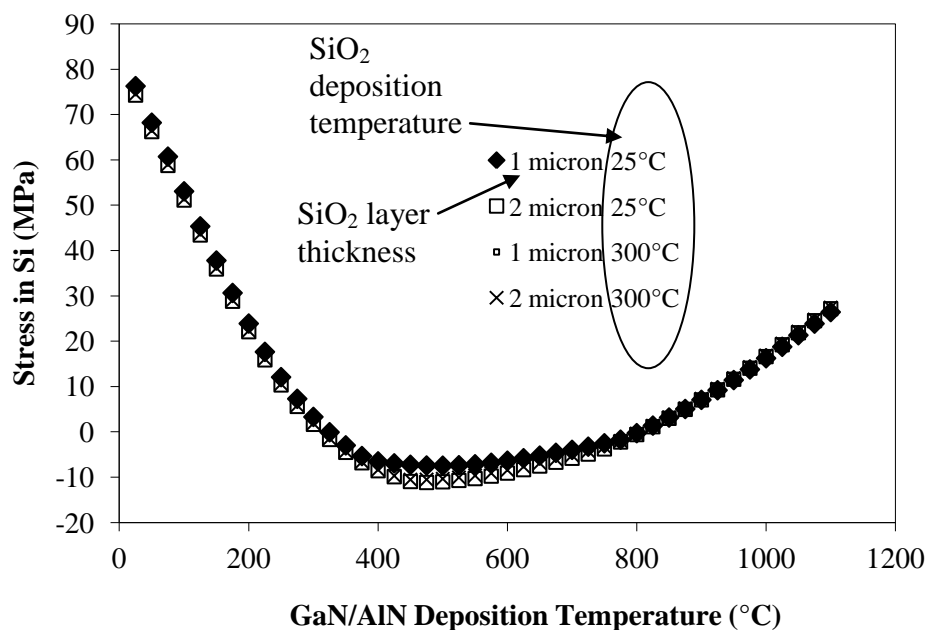
Figure 4.10 shows a schematic of the method used to model the effect of SiO<sub>2</sub> on the free PD side. In the model schematic shown in figure 4.10, only the Si device layer of the SOI wafer has been included for simplicity. The assumption is that due to the low CTEs of SiO<sub>2</sub>, this layer will add a tensile stress component to the PD and this will in turn reduce the tensile stress in the Si device layer. Therefore, this model will be used to determine if this method provides a potentially viable route for producing thin Si layers. A literature search yielded the material property values of SiO<sub>2</sub> and SiN<sub>x</sub>, which is investigated in sub-section 4.3.2, and these values are contained in table 4.2.

**Table 4.2** Materials properties used for modelling SiO<sub>2</sub> and SiN<sub>x</sub>. [139-144]  
 (See tables 1.9 and 1.11 for the Si and PD materials data)

Material	SiO <sub>2</sub>	SiN <sub>x</sub>
E (GPa)	60	160
$\nu$	0.24	0.3
$\alpha$ (10 <sup>-6</sup> /K)	CTE (Si) – 1.61	1.017 @ 27°C to 4.344 @ 1127°C

Figure 4.11 does show that depositing a layer of SiO<sub>2</sub> on the PD side does enhance the compressive stress in the Si layer. Increasing the thickness of the SiO<sub>2</sub> from 1 to 2

$\mu\text{m}$  imparts more compressive strain on the Si, but the  $\text{SiO}_2$  is not sufficiently thick to make more than a subtle change to the stress. It is impractical to deposit more than a 2  $\mu\text{m}$  layer of  $\text{SiO}_2$  by plasma enhanced chemical vapour deposition (PECVD) because the showerhead at the top of the reactor, described in section 2.5 will become blocked with reagents, preventing it from depositing any more material. Significant amounts (order of 100  $\mu\text{m}$ ) of  $\text{SiO}_2$  will need to be deposited to remove most of the bow and minimise the tensile stress imparted on Si, at this thickness the  $\text{SiO}_2$  will reduce the thermal conductivity of the substrate to unacceptable levels. Therefore this approach will not work and an alternative method needs to be sought.

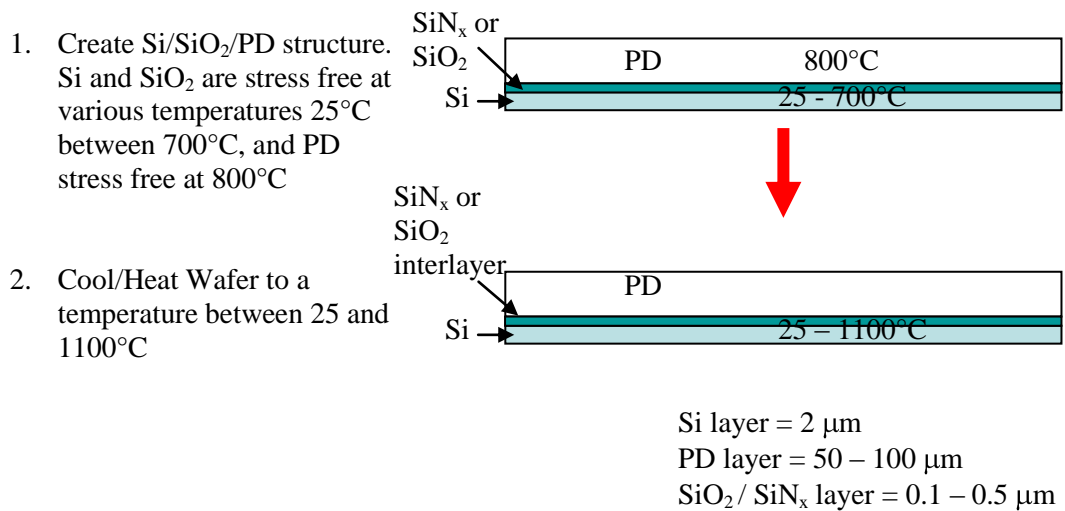


**Figure 4.11** Stress with respect to GaN/AlN deposition temperature in the Si layer with a 1 or 2  $\mu\text{m}$  layer of  $\text{SiO}_2$  deposited on the free PD side.

#### 4.3.2 Method 2: Depositing a $\text{SiO}_2$ or $\text{SiN}_x$ interlayer

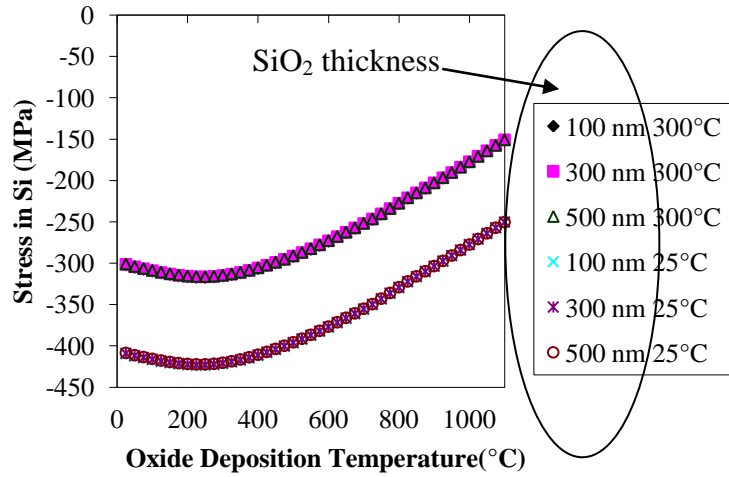
An alternative is to deposit a compliant interlayer material between the silicon device layer and diamond was modelled in an attempt to reduce the stresses associated with both SOI removal and CTE mismatch. For Si/PD wafers, the suitable materials for a compliant interlayer are  $\text{SiN}_x$ ,  $\text{SiO}_2$  or an alloy of both known as  $\text{SiN}_x\text{O}_y$ . A compliant

interlayer will also protect the Si from diamond nucleation damage. Thin (~100 nm) amorphous layers of SiN<sub>x</sub> and SiO<sub>2</sub> can be deposited onto SOI wafers at temperatures from ambient room temperature up to 300°C using PECVD [104]. In order to determine the likely effectiveness of SiN<sub>x</sub> or SiO<sub>2</sub> interlayers, they were also modelled using ANSYS FE software. Figure 4.12 shows the modelling method used to predict the behaviour of the wafer with an addition of an interlayer.

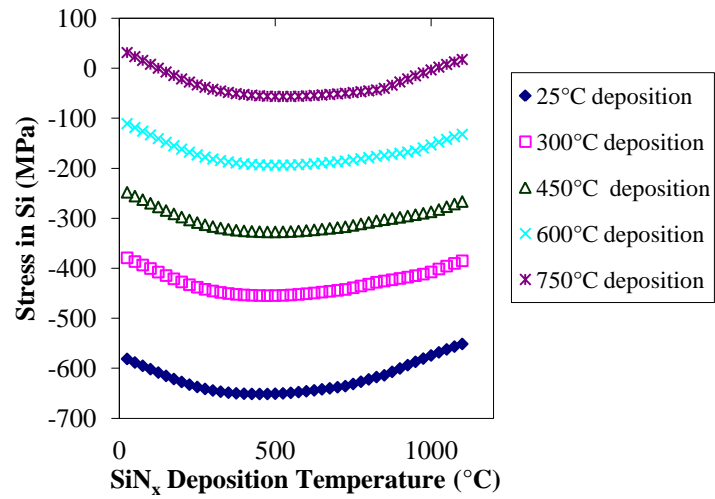


**Figure 4.12** Schematic of ANSYS FE model used to investigate the addition of a SiN<sub>x</sub> or SiO<sub>2</sub> interlayer to the Si/PD composite substrate.

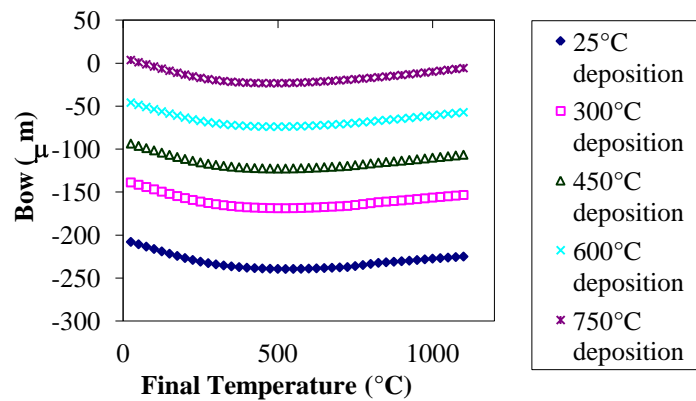
The results from the FE model, using both SiO<sub>2</sub> and SiN<sub>x</sub> as interlayers, are shown in figure 4.13. The purpose of the model was to explore the stress in the Si device layer between 25°C, room temperature, and 1100°C, the maximum III-V nitride growth temperature. The key point to note from the results in figure 4.13 is that the addition of both materials as an interlayer inverts the stress profile, putting the Si layer in compression. The degree of compression in Si varies according to the interlayer deposition temperature and the final temperature.



(a)



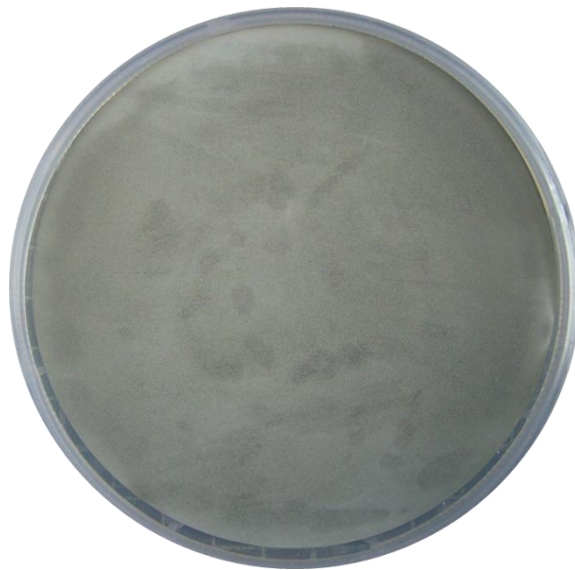
(b)



(c)

**Figure 4.13** Plots showing the predicted stress in the Si layer with an interlayer 100 nm thick of (a) SiO<sub>2</sub> and (b) SiN<sub>x</sub>. (c) is a plot of wafer bow for the SiN<sub>x</sub> interlayer.

The FE modelling indicates that this method could be a potential method for creating viable substrates. In order to test this method, an attempt was made to nucleate PD on the SiO<sub>2</sub> surface of a SOI/SiO<sub>2</sub> wafer. The SOI wafer consisted of a 625 μm (111) Si handle, 1 μm SiO<sub>2</sub> layer and a 2 μm (111) Si device layer. An 80 nm SiO<sub>2</sub> layer was deposited onto the Si device layer by PECVD at 300°C and the wafer was sent to Element Six for PD nucleation. Element Six attempted nucleation on this wafer and an image of the resulting wafer is shown in figure 4.14. Unfortunately, the PD nucleation was unsuccessful with the PD delaminating from the rest of the wafer. A possible cause of this delamination could be the result of the oxidation of the SiO<sub>2</sub> layer, creating a gap between the PD and the rest of the wafer. The outcome of this work is that an alternative method for creating viable GaN on Si/PD substrates needs to be trialled.



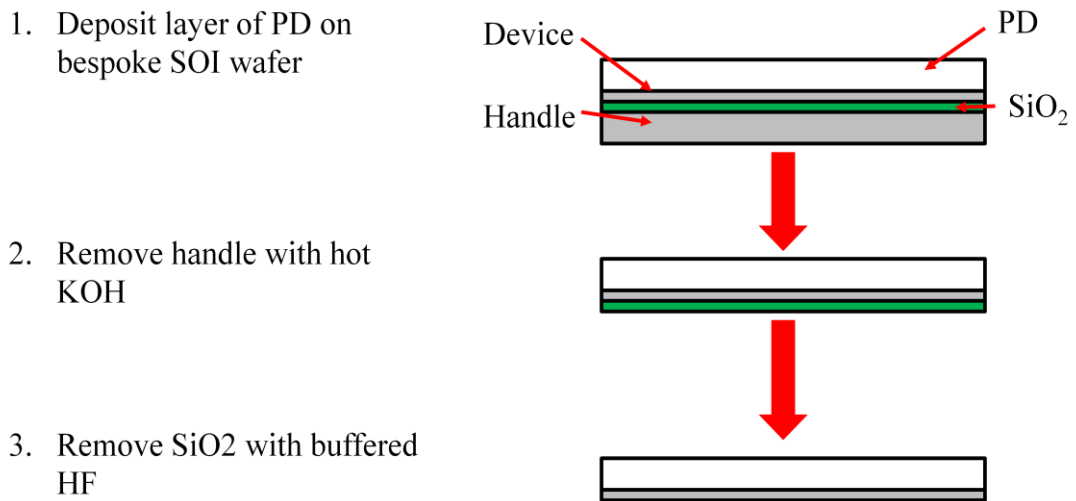
**Figure 4.14** Image of an attempt to nucleate PD on SOI/SiO<sub>2</sub> wafer, showing the delamination.

#### **4.4 Method 3: Anisotropic etching of the Si handle layer**

Another option for processing suitable Si/PD substrates using SOI wafers is to etch through the thick Si handle layer using a KOH etchant solution. The KOH etchant solution is simple to produce in a fume cupboard by dissolving KOH crystals in



water. This solution is most effective as an etchant when heated to ~60 to 80°C and ultrasonic excitement [145, 146], so the PD/SOI wafer was placed into the solution at this temperature. This method is most effective when the SOI handle is (100) orientated because KOH is an anisotropic etchant of Si. An anisotropic etchant is a chemical that etches through different planes of a crystalline material at different rates [145, 147], with the different KOH etch rates of Si shown in table 4.3. Table 4.3 shows that for this process to be viable, the Si handle wafer needs to be (100) orientated. Unfortunately, the early PD/SOI wafers were produced on SOI wafers with a (111) handle, an orientation where the KOH etch rate is too slow for it to be a practical process (see table 4.3). This meant that SOI wafers with (100) orientated Si handles had to be purchased for trials of this process. Table 4.3 suggests that it takes between 8.5 to 10.5 hours to etch through the 525 μm handle when Si is (100) orientated, which is a big improvement on the two weeks it takes for the buffered HF to etch through the SiO<sub>2</sub>. Figure 4.15 shows a simple schematic of how to produce Si/PD substrates using the KOH etching method.



**Figure 4.15** Basic schematic of the process used to create suitable Si/PD wafers for GaN using a chemical etching method.

**Table 4.3** Various 30% KOH solution etch rates for different Si orientations at 70°C.  
[145]

<b>Orientation</b>	<b>Etch Rate</b>
(100)	0.797 $\mu\text{m}/\text{minute}$
(110)	1.45 $\mu\text{m}/\text{minute}$
(111)	0.005 1 $\mu\text{m}/\text{minute}$

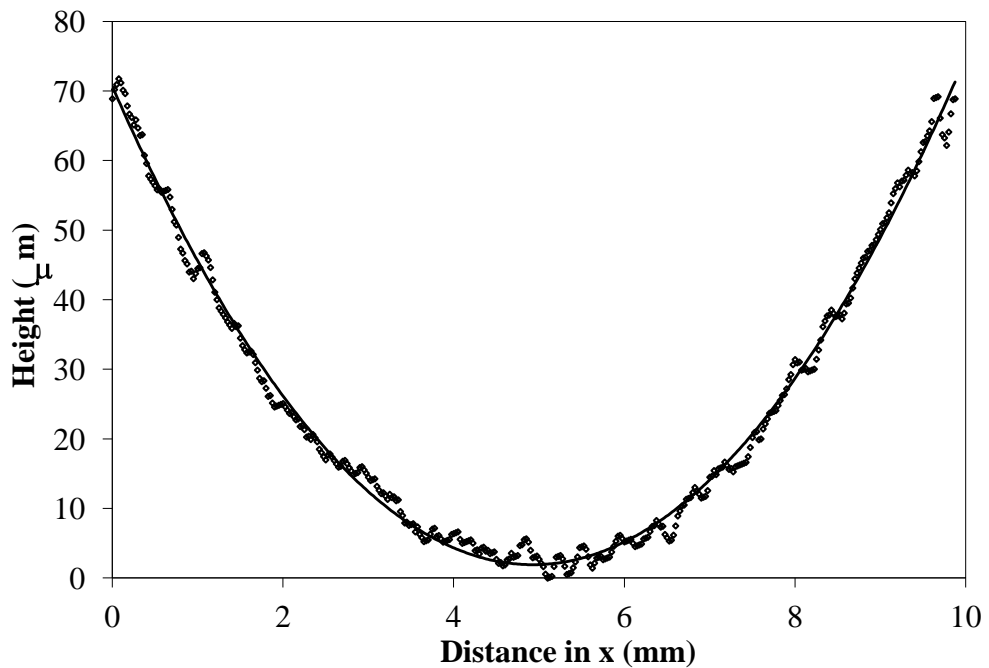
The advantages for etching the handle over both lapping the handle and etching the thermal oxide in this situation is that it should prevent the Si device layer from getting damaged during processing and allowing the best possible III-V nitride layer to be grown. However, peeling/delamination at the Si/PD interface could still occur during the KOH etch because this method does not address the large shear stress that is a direct result of the thermal mismatch. At this stage, Element Six began to develop a new nucleation method that aimed to improve Si/PD adhesion.

#### **4.5 Experimental Characterisation of Si/PD SOI wafers**

As well as measuring the wafer bow on thick Si/PD wafers, as shown in chapter 3, the profilometer was used to measure the bow on a sample with a thinned Si layer. The sample originated from a 4-inch diameter wafer that was a mixture of layers of (100) and (111) Si separated by a thin layers of SiO<sub>2</sub>. Once all of the (100) Si and SiO<sub>2</sub> layers were etched away using KOH and HF respectively, the wafer consisted of a 60  $\mu\text{m}$  layer of (111) Si and 40  $\mu\text{m}$  of PD. The surviving parts of the wafer were then cleaved into more manageable squares between 100 and 400 mm<sup>2</sup> in surface area. The bow of two of the almost square 100 mm<sup>2</sup> samples was then measured using the Proscan 2000 profilometer. Both samples had their entire surface scanned with the Proscan 2000 and the results from these measurements, alongside the result from an FE model with the same dimensions, are shown in table 4.4.

**Table 4.4.** Bow measurements taken from three cleaved samples from a thin Si/PD wafer.

Sample	Area (mm <sup>2</sup> )	Sample measured width (mm)	Bow (μm)	Error (μm)
1	100	9.725	75	4
2	100	9.825	70	2
FE model	100	10	63	



**Figure 4.16** Line scan taken from a thinned Si/PD sample.

The results from the bow measurements are shown in table 4.4 and figure 4.16 shows a typical line scan from sample 2. The bow measurements from samples 1 and 2 are similar, as shown in table 4.4, as expected. The main source of error in the bow measurements is caused by the difference in measurements from each individual line scan. Si/PD wafers are difficult to cleave because the PD has no cleavage planes because it is polycrystalline. The plot in figure 4.16 shows that the bow curves of the 60 μm Si / 40 μm PD samples is almost a perfect parabola, the same shape as the thicker Si/PD samples in chapter 3. This result is because CTE mismatch is biaxial and the lengths and widths of both samples are comparable.

#### 4.6 Production of suitable Si/PD substrates for GaN growth

It was discussed in section 4.2 that the silicon is heavily abraded by Element 6 prior to diamond growth to help nucleation of diamond during their process. The abrasion introduces significant damage into the silicon and also leads to relatively poor adhesion between the diamond and silicon. A new PD nano-nucleation process, using smaller diamond crystals, was developed by Element 6 and this offered improved adhesion between Si and PD. The new nucleation process also does less damage to the Si surface, meaning that it can withstand more stress before cracking; thereby reducing the risk of full delamination and strengthening the Si device layer. The previous nucleation process damaged the Si layer, leaving it liable to crack during the mechanical thinning process. The advantage of hot KOH etching is that it requires minimal clamping, reducing the risk of the Si cracking. Additionally, bespoke SOI wafers were acquired and these wafers consisted of a 525 to 625  $\mu\text{m}$  (100) Si handle, a 1  $\mu\text{m}$   $\text{SiO}_2$  interlayer and a 1 to 2  $\mu\text{m}$  (111) Si device layer, as shown in figure 4.1, meaning that the bulk of the Si layer can be removed with hot KOH. Before KOH etching, a  $\sim 50$   $\mu\text{m}$  PD layer was grown on the top of the (111) Si device layer. This is a reduction in PD thickness from the target thickness of  $\sim 80$  to 100  $\mu\text{m}$  of the previous substrate generation. An analytical study on delamination and interfacial peeling, shown in section 3.5, demonstrated that this risk could be reduced by growing a thinner layer of PD.

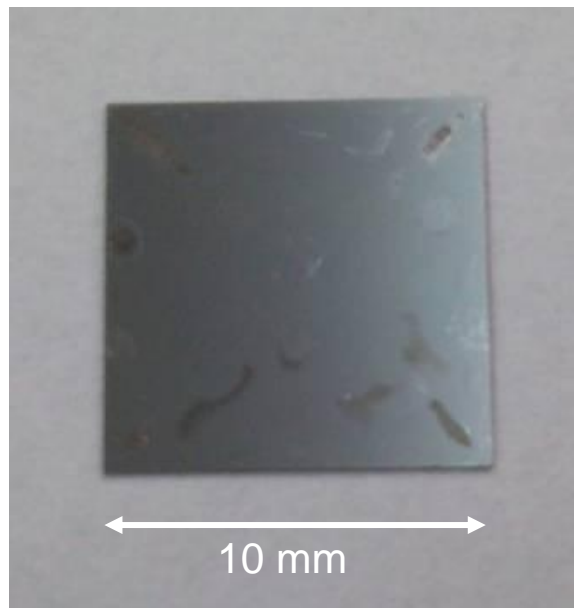
The hot KOH etch process successfully produced viable Si/PD samples when the PD nano-nucleation process was used. It has been possible to produce samples up to 2 inches in diameter using this method, with an image of a 2 inch diameter sample being shown in figure 4.17. This image shows that the hot KOH etching, in conjunction with improved Si/PD adhesion, overcomes the Si cracking and delamination issues. However, as the image in figure 4.17 shows, the hot KOH etching process does not stop the wafer from bowing during processing. There is also evidence of peeling on the edge of the substrate and this shows that the wafer is still subjected to high shear stresses during KOH etching.



**Figure 4.17** Image of a 2 inch (111) Si/PD wafer with a 2  $\mu\text{m}$  Si device layer produced using hot KOH etching.

An interesting point of note is that the substrate in figure 4.17 is noticeably bowed and this sample is actually bowed in the opposite direction to what is expected from the FE model and measurements from thick Si/PD samples. This change in bow direction is due to the tensile intrinsic stresses in the PD [129, 148-150]. When the Si is sufficiently thin, it has much less influence on the PD because it is thin and a less stiff material (see section 1.6). Therefore, the intrinsic stresses in the PD dominate the stress profile in the substrate rather than thermal mismatch and effectively mean that the Si acts like a compliant layer when sufficiently thin. Net tensile intrinsic stress in PD also protects the Si from damage by making enhancing the compressive stress in this layer. However, in the case of the wafer in figure 4.17 the intrinsic stresses have induced too much bow for the wafer to fit properly in the MOCVD growth reactor and this means that initial GaN growth trials were done on smaller samples. The bowing issues can potentially be overcome by strain engineering the intrinsic stresses in the PD.

#### 4.7 Thermal effects on thin Si/PD samples released from SOI wafers

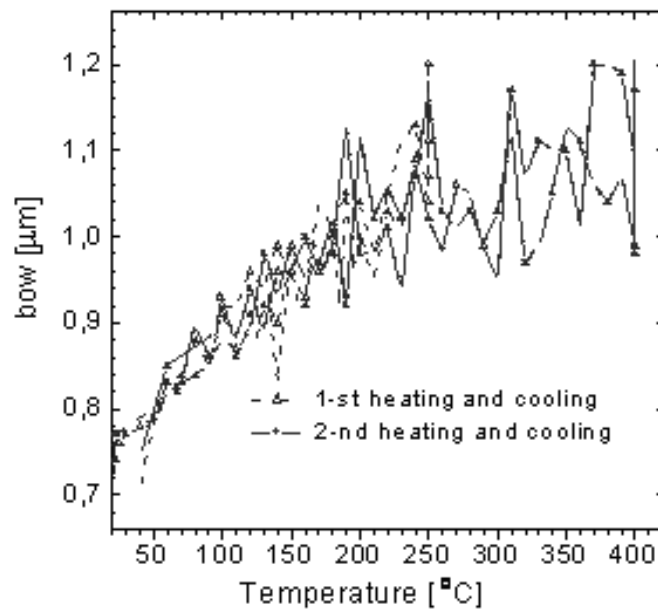


**Figure 4.18** Image of the sample sent to ITE, Warsaw, Poland for high temperature bow analysis. The Si surface of this sample was damaged so was unsuitable for III-V nitride growth.

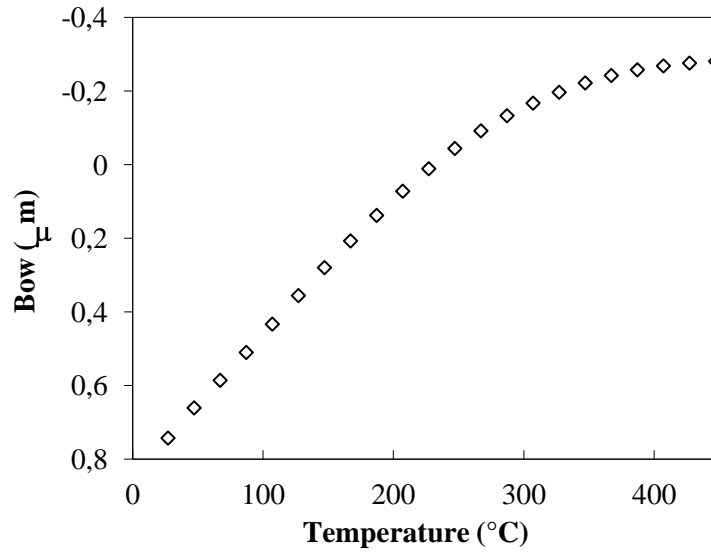
A 10 mm<sup>2</sup> Si/PD wafer released from a (111) Si handle SOI/PD wafer by HF etching was sent to MORGaN colleagues at ITE in Warsaw, Poland to measure its bow with respect to temperature. The wafer bow measurement system is briefly described in sub-section 3.8.1. This sample was sent because its surface was too damaged for GaN growth, as figure 4.18 shows. The damage pattern shown in figure 4.18 appear different to that shown in figure 4.5, this is because of sample geometry. Square samples have a characteristic cross-shaped damage pattern, rather than the ‘tree rings’ pattern on circular samples, this is because the stress caused by the release method builds up in the corners of the sample. All samples that retained a good quality Si surface were retained for III-V nitride growth trials because the number of these samples was very limited.

The bow of the Si/PD sample was measured twice from room temperature to 400°C and down to room temperature and the results from these measurements are shown in figure 4.19. The plot in figure 4.19 shows that both measurements follow very similar paths on heating up and cooling down, with near identical bow measurements and this

provides evidence that the amount of plastic deformation is small. The amount of bow with respect to temperature is increasing as the temperature increases. Since the experiment was set up with the laser striking the more reflective Si side, an increase in bow means that the Si is becoming more compressive, due to a decrease in tensile stress resulting from less CTE mismatch and the FE model agrees with this result (see figure 4.19). Therefore the reduction of tensile stress of the Si with respect to temperature is due to a reduction of the CTE mismatch, as demonstrated by figure 4.19 (b). The final point is that the Si layer on this sample started under a compressive stress at room temperature; this behaviour was not predicted by the FE model but this is caused by intrinsic stresses that occur in the PD material during nucleation [129]. These stresses are dominant when the less stiff Si layer is thinner than the PD, reducing its overall influence on the structure. These results support the observation in the previous section that intrinsic stresses in the PD are the dominant stress contribution in thin Si/PD samples and the temperature dependent bow measurements show that CTE mismatch is still influential, with the FE modelling still valuable.



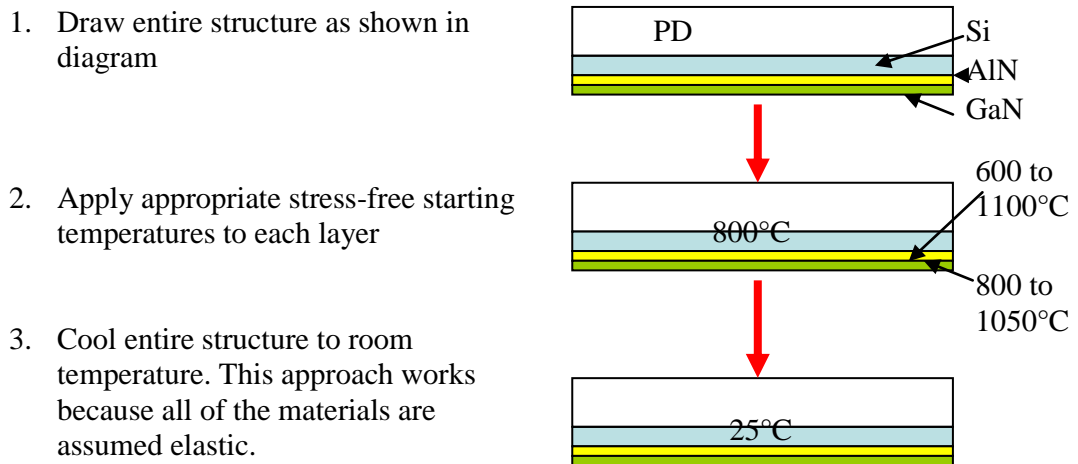
(a)



(b)

**Figure 4.19** Measurement of the bow of a 2 μm (111) Si / 140 μm PD sample where (a) are the experimental measurements at ITE and are (b) results from the FE model programmed with the same dimensions.

#### 4.8 Initial FE Modelling of GaN on Si/PD composite substrates

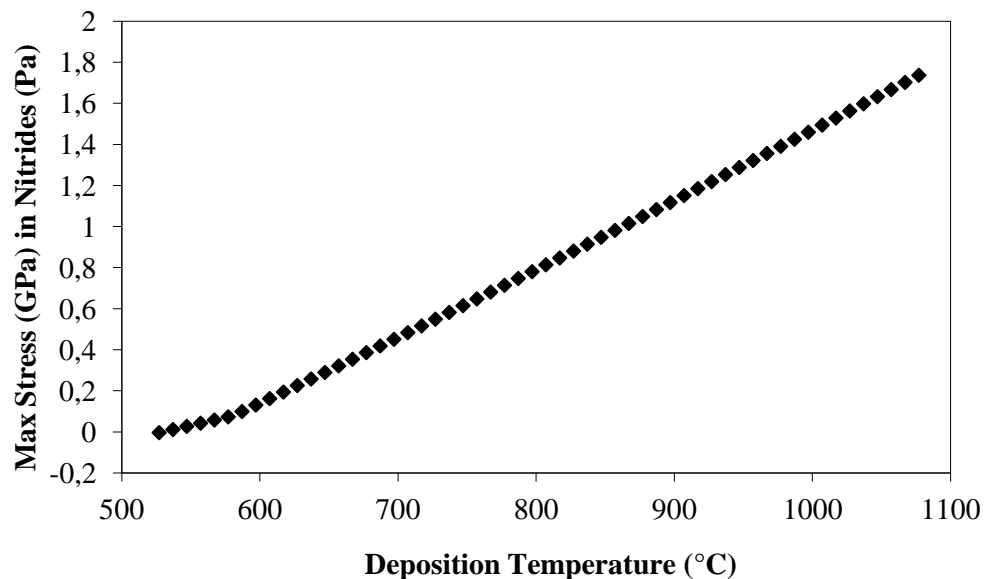


**Figure 4.20** Schematic of FE model used to predict the effects of adding a GaN/AlN layer to the Si/PD composite wafer.

As the various CTE plots in chapter 1 show, the III-V nitrides of AlN and GaN have larger CTEs than either Si or PD. This means that an AlN/GaN layer grown on a



Si/PD substrate will be under large amounts of tensile thermal mismatch stress, which could lead to cracking in the III-V nitride layer. A FE model, shown in figure 4.20, was devised to show the effect a III-V nitride layer of 50 nm of AlN and 200 nm of GaN will have on the thermal stresses in the wafer system. Unfortunately, the model was unable to include the additional stresses exerted on the system by the dominant intrinsic stresses in the PD as these are variable and very difficult to accurately model [129, 148]. The addition of tensile intrinsic PD stress is likely to reduce the stress in both the Si and III-V nitride layer. An additional large stress contribution comes from lattice mismatch between the Si and III-V nitrides and the associated strain relief that is induced through lattice dislocations. Both intrinsic and lattice dislocation strain are temperature independent and although they will change the net stress profile, they will make little change to the trend that occurs when varying the nitride deposition temperature and the model will therefore demonstrate good experimental practice. The effects of varying the AlN/GaN deposition temperatures were explored, as this can be used as a method for mitigating stress [39-41].



**Figure 4.21** Peak stress in the III-V nitride layer with respect to deposition temperature.

Figure 4.21 suggests that reducing the nitride deposition temperature to as low a temperature as possible will reduce the stress in the nitride, reducing the risk of cracking. The FE model suggests that the nitride layer will be compressive at room

temperature if deposited at less than 550°C. Unfortunately, it is not possible to deposit single crystal GaN below 550°C by MOVPE and the growth rate is poor until the temperature reaches 800°C [151]. Therefore, the best experimental practice is to reduce the deposition temperature as much as reasonably possible when using MOVPE. A summary of the MOVPE growth method can be found in sub-section 6.3.2.

#### **4.9 GaN on Si/PD substrates**

Using the work detailed in this chapter and chapter 3, it is now possible to grow crack-free GaN on Si/PD composite substrates. The crack-free GaN layer was produced using epitaxial strain engineering techniques that is not suitable for ANSYS FE software, so has not been included in the main body of the thesis. A paper detailing the process that was used to produce this layer can be found in appendix A1.4. Now that it has been proven that crack-free GaN can be grown on Si/PD substrates, the next stage will be to fabricate a HEMT on this substrate and this will be described in chapter 8. Despite the successful creation of a viable substrate, problems do remain. The bow of the substrate still cannot be controlled and this limits the size of the substrate 20mm in diameter at present. As the intrinsic stresses in the PD are the dominant causes of the bow in the substrate at these thicknesses, the solution might be to manipulate the PD grains during nucleation and produce a favourable stress distribution. However, this represents a significant technical challenge as the PD growth conditions will require a lot of optimisation. The main technical challenge appears to be how to control the intrinsic stresses in PD so that the wafer bows favourably when the Si layer is thin. Further information on the technical challenges can be found in the appendices A1.1, A1.4 A1.6, A1.8 and A1.9.

#### **4.10 Concluding Remarks**

Viable GaN on Si/PD structures have been produced based on the research undertaken in this and the previous chapter. Based on the results from the FE model

shown in chapter 3, a change of approach was taken in attempting to produce Si/PD composite substrates. PD was nucleated on SOI wafers that consisted of a 525  $\mu\text{m}$  (111) Si handle, a 1  $\mu\text{m}$   $\text{SiO}_2$  interlayer and a 2  $\mu\text{m}$  (111) Si device layer, rather than a bulk 525 to 625  $\mu\text{m}$  thick (111) Si wafer. Initial attempts to release a wafer from its handle using an HF etch of the  $\text{SiO}_2$  failed due to significant damage to the Si. The FE model showed that the failure in the Si was caused by an excessive build up of tensile stress above the  $\text{SiO}_2$  layer, which occurred during the etching process. The FE model showed that attempts to control this damage by depositing  $\text{SiO}_2$  on the free PD side would not work. The addition of a compliant  $\text{SiO}_2$  or  $\text{SiN}_x$  interlayer looked promising and was attempted experimentally, but this method failed with the PD delaminating with the most likely reason being a chemical reaction between the  $\text{SiO}_2$  and PD during nucleation. Chemical etching using hot KOH, an anisotropic Si etchant, was found to be a possible method if the orientation of the Si handle was changed from (111) to (100). Chemical etching is superior to mechanical lapping because the wafers required minimal clamping and the modelling work indicated that this approach would not crack the Si. The only issue that needed overcoming was delamination caused by the heavy build up of shear stresses at the peak of the bowing phase. The two ways to avoid delamination in a bilayered Si/PD structure is to improve adhesion between the two layers and to reduce the PD thickness.

Improved Si/PD adhesion, courtesy of a new nano-nucleation process, a small reduction in PD thickness to  $\sim 50 \mu\text{m}$  and hot KOH etching allowed the processing of PD/SOI wafers with a (100) handle into thin (111) Si/PD composite substrates that were suitable for GaN growth. Through the use of graded AlGaIn layers, see appendix A1.4, it was possible to grow crack-free GaN on these substrates and this material can be used as the basis for high power HEMTs and GaN-based sensors in the future. A graded AlGaIn layer is where the deposition material starts as AlN and the Ga content is increased and Al content is reduced until the top of the graded structure is wholly GaN. However, there are still some issues remaining with the substrates that need to be solved. The main outstanding issue is that the bow of the Si/PD substrates is still not under control, currently limiting GaN growth to 20 mm diameter round substrates and 20  $\text{mm}^2$  square substrates. This issue is affecting the overall substrate yield and this leads to increased substrate costs, meaning that eventually controlling the bow is paramount. The two dominant stress contributions that cause the bow are CTE

mismatch, which can be modelled to a good degree of accuracy, and intrinsic stresses in the PD layer, which are variable and not possible to model accurately using current methods employed in this project. A suggested method for controlling bow include developing a method for ensuring favourable intrinsic stresses in the PD, which represents a significant technical challenge, or using a compliant interlayer that absorbs the strain produced by both materials and survives nucleation. Ultimately, it is possible to grow viable crack-free III-V nitride layers on a thin (111) Si/PD substrate collaboratively within the MORGaN project and this represents a breakthrough in GaN substrate technology that will allow the development of the next generation of power devices and extreme sensors. Due to the timescales and technical challenges in developing (111) Si/PD substrates, the devices fabricated later in this thesis will use either sapphire or (111) Si substrates.

**The next chapter concerns the measurement of the Young's Modulus of GaN up to 1000°C using dynamic mechanical thermal analysis (DMTA) and impulse excitation.**

## CHAPTER 5: EXPERIMENTAL DETERMINATION OF THE ELASTIC PROPERTIES OF GAN AND SUBSTRATE MATERIALS

### 5.1 Motivation

The GaN-based sensors described in this thesis will need to operate at temperatures in excess of 400°C and therefore the behaviour GaN and its substrate materials at these temperatures needs to be understood. The literature review of Chapter 1 found little experimental data on the elastic properties of GaN and its substrates (sapphire and silicon) at high temperatures. Additionally, nothing was found in the literature on using DMTA to measure the Young's modulus of GaN because suitable free-standing GaN samples are very new to the market and expensive. Tilak [30, 32, 33] used DMTA for finding the Young's modulus of sapphire, but did not publish these findings and Cho [58] employed a similar four point bend method in Si. Therefore the  $E_{33}$  or Young's modulus of (0001) GaN, (111) Si and (0001) sapphire were measured with respect to temperature by dynamic mechanical thermal analysis (DMTA). DMTA is usually used to measure modulus changes in polymers, but can be theoretically used for stiffer materials. DMTA has been successfully used to measure the stiffness of high stiffness materials such as Ce-TZP ceramics [152]. Although these measurements are simple, they offer some understanding of the changes in elastic properties of materials used for high-temperature sensors and are useful in achieving the objectives of the MORGaN project.

### 5.2 Outline of Chapter

This chapter will briefly discuss the progress in measuring the Young's modulus of GaN, sapphire and silicon. Firstly, some initial measurements on silicon and sapphire will be shown and there will be a brief analysis of the results. These were initially undertaken to compare with the limited data sets found in the literature. Issues found when taking these measurements will be discussed and improvements to the experimental method will be determined. These improvements in the measurement method will be compared with available literature data. As the temperature dependent

modulus of silicon is the most well reported in the literature, it will be used to calibrate the modulus data of GaN and sapphire. This data will then be compared to any data that exists in the literature to see if this approach is valid.

In addition to measuring the high temperature  $E_{33}$  modulus of GaN, its isotropy along the basal plane was tested to confirm that the material was (0001) orientated. GaN has a wurtzite crystal structure and therefore  $E_{33}$  is isotropic along (0001) plane [3, 48, 57, 72]. In order to test the isotropy, a freestanding GaN wafer was laser cut with samples orientated in different directions. Additionally, DMTA was compared with impact excitation [97], another method for measuring the modulus of materials, and there was a brief discussion on the relative merits of both methods. Further information on DMTA and impulse excitation is contained in section 2.3.

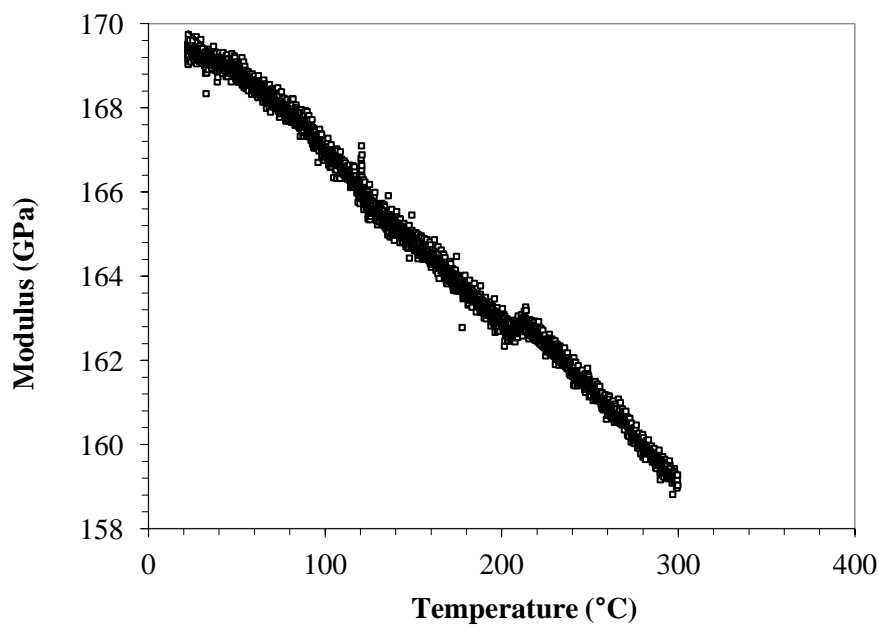
### **5.3 Initial Measurements**

In order to accurately finite element model the stress profiles of GaN/substrate wafers, detailed temperature dependent material properties are required. The most important initial properties for modelling are the elastic moduli and coefficients of thermal expansion (CTEs) of a material. The temperature dependent CTEs of GaN and the majority of substrate materials are complete in the literature, but there are some missing high temperature elastic moduli data in the literature for GaN, silicon and sapphire, materials used in this thesis. A Tritec 2000 DMA (Triton Technology) equipped with a furnace head was used in three-point bending mode and the  $E_{33}$  modulus of these materials was measured. The DMTA computed the modulus from the applied cyclic stress, the measured strain and deflection of the sample. The sizes of the samples that can be tested using this system are between 22 and 40 mm long, up to 8 mm wide and thicknesses from 0.25 to 5 mm. The samples used in this project are 0.3 to 0.5 mm thick because they are cut or cleaved from semiconductor wafers. However, in order to accurately measure elastic moduli of materials in the DMTA it needs to be correctly calibrated to minimise error. Correct calibration and well-defined geometry are required for accurate DMTA measurements. This is a difficult technique to perfect and has to be done for every individual measurement; with a high risk of fracture if too much static force is applied to a thin delicate brittle material

during the measurement of the sample. The temperature dependent elastic properties of silicon are the most well-defined in the literature and its elasticity is typical for a semiconductor, making it a suitable test sample for this project. The orientation of the silicon used for the test measurements is (111) because that is the most common orientation for GaN growth.

### 5.3.1 Measurements of silicon and sapphire

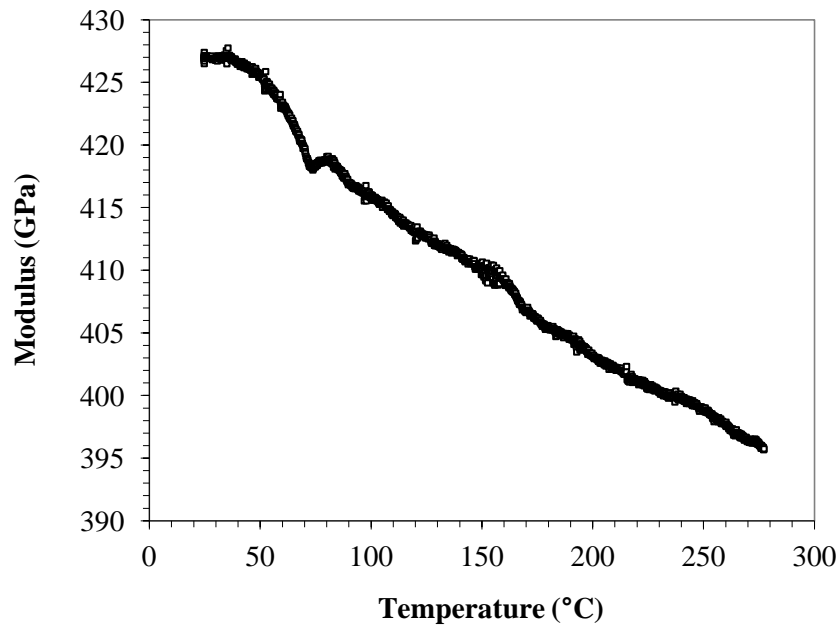
Figure 5.1 shows the measurement of the Young's modulus of (111) silicon from room temperature (25°C) up to 300°C. Initially, it was only possible to measure the Young's modulus  $E$  of a material up to 300°C because the DMTA was equipped with a lower temperature furnace at the time. The decrease in the modulus with respect to temperature is larger than expected from the literature values [58] shown in table 5.1.



**Figure 5.1** A typical initial measurement of the variation of elastic modulus of (111) Si with respect to temperature.

Figure 5.2 shows a typical initial measurement of the variation of the Young's modulus of a cleaved (0001) sapphire sample with temperature. The measurements of sapphire follow a similar pattern with the room temperature measurements comparing well with the literature (see tables 1.12 to 1.14) but the DMTA showing a higher than

expected decrease in stiffness with temperature. Sapphire is a stiffer material than silicon, as discussed in chapter 1 and shown in figures 5.1 to 5.2, and has a melting point of nearly 2000°C [153], suggesting that the decrease in temperature is expected to be small and similar to that of silicon.



**Figure 5.2** Typical measurement of the variation of the elastic modulus of sapphire with temperature.

### **5.3.2 Experimental issues identified with initial DMTA testing**

The possible reasons for the larger than expected decrease in modulus with temperature in figures 5.1 and 5.2 are errors in the dimensions of the sample, imperfections on the sample surface, thermal expansion of the stainless steel clamps used to hold the sample and poor experimental technique. The measured room temperature  $E_{33}$  modulus of sapphire is similar to the literature values, as shown in tables 1.12 to 1.14. However, these initial samples currently used are subject to an error caused by the irregular geometry of the manually cleaved samples. It will not be



possible to use the DMTA to take absolute modulus measurements until samples with clearly defined, rectangular geometries are cut.

The stiffness of GaN will also be measured using this method. GaN in its freestanding form costs ~£1500 per 2 inch diameter wafer so the number of available samples was limited, meaning that the experimental technique will need to be initially perfected. Therefore, the work done with free-standing GaN will be done once the method has been refined using silicon and sapphire. Another issue with GaN, silicon and sapphire is that they tend to be very brittle, meaning that they tend to break soon after the yield stress is reached.

As stated earlier, the elastic modulus of silicon decreases faster than expected with temperature when compared to the literature [58]. This is potentially a systematic error in the DMTA that occurs due to the thermal expansion of the steel clamp and the fact that the instrument is operating close to its stiffness limit (i.e. the stiffness of the samples used here are higher than polymers typically measured in this system). Table 5.1 shows the difference in decrease in modulus with temperature between the literature values for silicon and the initial measurements in figure 5.1.

**Table 5.1** Comparison between literature and initial DMTA measurements of the modulus decay of (111) Si (The error on the raw values of the DMTA modulus measurements is  $\pm 5\%$ )

<b>Sample/Reference</b>	<b>Initial <i>E</i> (GPa)</b>	<b>Final <i>E</i> (GPa)</b>	<b>Initial T (°C)</b>	<b>Final T (°C)</b>	<b>% change per °C</b>
<b>Cho [110] [58]</b>	169	166.2	25.1	151.5	-0.013
<b>Cho [1-10] (001) [58]</b>	168.5	166.8	25.1	151.5	-0.008
<b>Cho [1-10] (111) [58]</b>	169.3	167.9	25.1	151.5	-0.007
<b>Cho [11-2] [58]</b>	168.8	166.5	25.1	151.5	-0.011
<b>DMTA 1</b>	169.4	165	22.5	151.5	-0.020
<b>DMTA 2</b>	168.9	163.3	40.8	151.5	-0.030
<b>DMTA 3</b>	169.8	164.9	28.6	151.5	-0.023

The designations DMTA 1 to 3 refers to the different Si samples measured using the DMTA using the early method. The key point to note from Table 5.1 is that the DMTA measures the rate of decrease of stiffness with temperature as approximately double the data in the literature, suggesting that the experimental technique requires

improvement or the DMTA measurements require calibration. The measurements in the remainder of the chapter will modify the experimental method and use calibration, with the merits of both approaches being discussed.

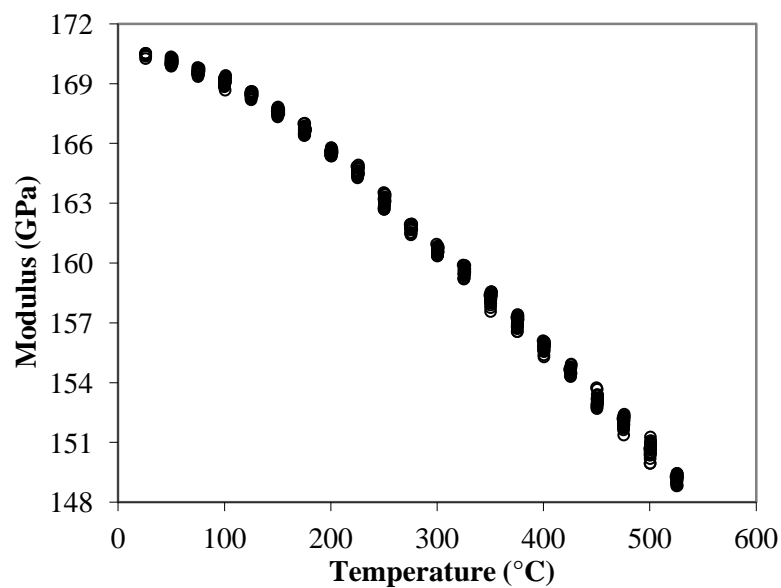
### ***5.3.3 Methods for improving the DMTA measurements and further tests with silicon and sapphire***

After the initial testing of silicon and sapphire the furnace was replaced with a version that can handle temperatures up to 600°C, which is close to target operating temperature of the GaN sensors proposed in the MORGaN project. In addition to the furnace upgrade, one day of DMTA training was provided by the manufacturers Triton. The purpose of the training was to demonstrate effective techniques and methods for obtaining absolute stiffness measurements. These techniques require practice and careful use of the clamps in order to obtain absolute measurements without damaging the sample. In order to achieve a good experimental measurement, the clamps need to be level and just touching the sample, to prevent the accidental tilting of a sample during measurement, and a small static force needs to be applied to ensure good constraint. Therefore, DMTA measurements of modulus improved during the course of this project and the limitations of the equipment were determined.

The silicon samples were retested after improvements to the experimental method were applied and are designated improved DMTA 1 to 4 in table 5.2. One of these improvements was to apply a small static force on the centre of the sample to improve clamping and prevent the sample from slipping. Poor clamping leads to inaccurate modulus measurements. However, applying additional static force can lead to the fracture of the test specimen. This problem was mitigated experimentally by adding the static force gradually until the sample was sufficiently constrained to measure the decrease in modulus accurately. Additionally, measurements of modulus were taken five minutes at a constant temperature in 25°C intervals from room temperature to 600°C. Measuring the modulus for a few minutes at a constant temperature meant that

the sample reached thermal equilibrium and there were more measurements of modulus at that temperature.

Figure 5.3 shows one of the scans taken using the improved experimental method, corresponding to the scan 'DMTA 3' in table 5.1. The degree of decrease in  $E_{33}$  is similar to that in the literature, as shown in table 5.2 [58], and this suggests that the changes made to the experimental method have improved the accuracy of the measurements. Therefore, it is good experimental practice to take measurements at thermal equilibrium and make sure that the sample is adequately constrained, using additional static force if necessary.

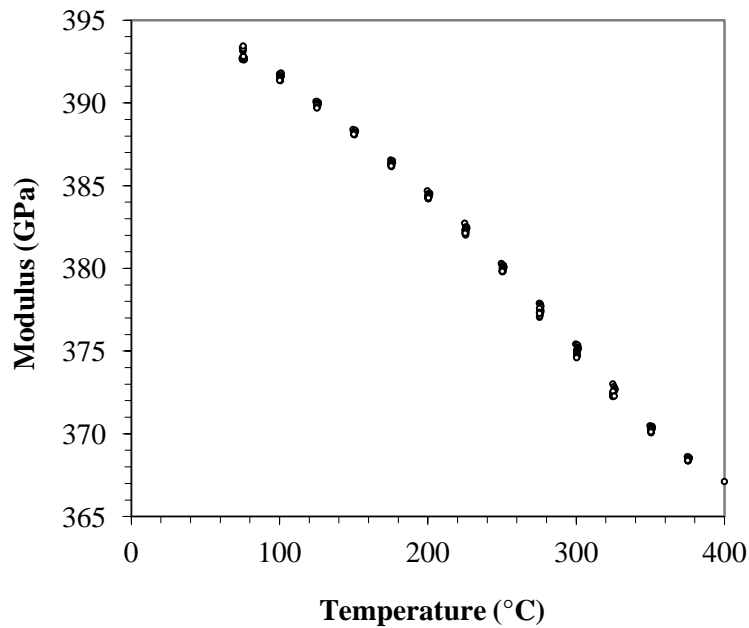


**Figure 5.3** Typical initial measurement of the variation of elastic modulus of (111) Si with temperature from 26°C to 525°C.

**Table 5.2** Comparison between literature and improved DMTA measurements of the variation of modulus of (111) Si with temperature.

Work name	Initial $E$ (GPa)	Final $E$ (GPa)	Initial T (°C)	Final T (°C)	% change / °C
Cho [110] [58]	169	166.2	25.1	151.5	-0.013
Cho [1-10] (001) [58]	168.5	166.8	25.1	151.5	-0.008
Cho [1-10] (111) [58]	169.3	167.9	25.1	151.5	-0.007
Cho [11-2] [58]	168.8	166.5	25.1	151.5	-0.011
Improved DMTA 1	168.5	167	63.9	151.8	-0.010
Improved DMTA 2	169.7	166.5	27.4	150.5	-0.015
Improved DMTA 3	170.7	167.7	28.9	150.5	-0.014
Improved DMTA 4	172.2	170.6	29	150.4	-0.008

The same experimental technique was applied to cleaved sapphire and the results from one of the scans are shown in figure 5.4. However, the changes in experimental method made little difference to decrease in stiffness with temperature, as shown in table 5.3. The probable explanation is that (0001) sapphire has a stiffness of approximately 425 GPa (see tables 1.12 to 1.14) compared to ~170 GPa for (111) Si, meaning that sapphire is potentially too stiff for the DMTA fixture to measure the  $E_{33}$  decrease with temperature without breaking the sample because too high a static force needs to be applied. The  $E_{33}$  of GaN from the literature is typically between 250 and 350 GPa, as shown in table 1.4, which may suggest that directly measuring the temperature dependant  $E_{33}$  by DMTA will be difficult. Therefore an alternative method for correcting the  $E_{33}$  of GaN needs to be sought.



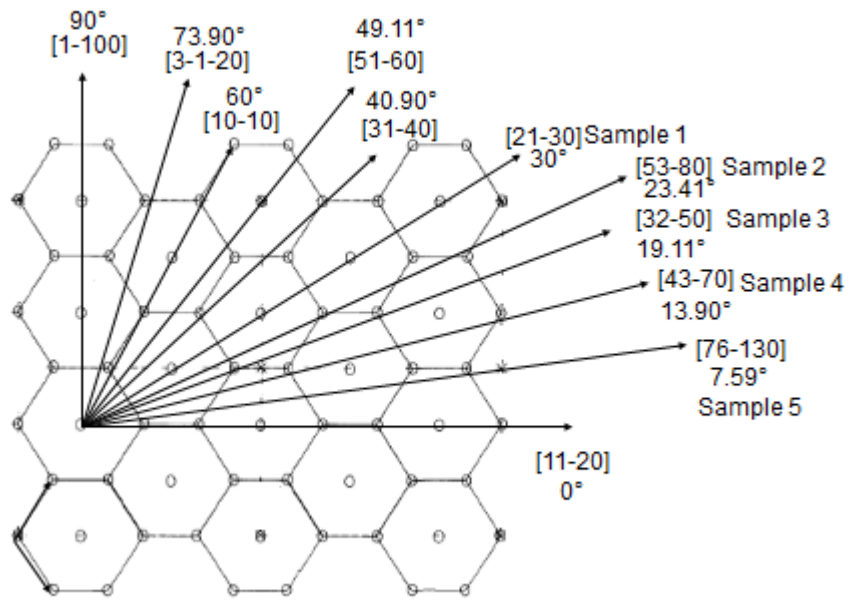
**Figure 5.4** Measured variation of the  $E_{33}$  of sapphire from 75°C to 400°C.

**Table 5.3** Measurements of the  $E_{33}$  decrease of sapphire with respect to temperature in sapphire before and after improvements in experimental method.

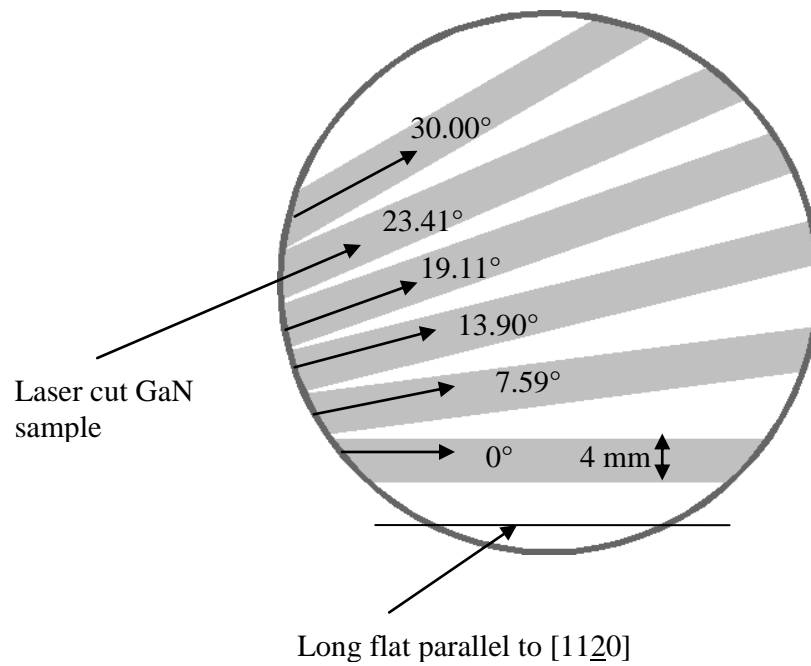
<b>Sapphire Sample No.</b>	<b>Initial <math>E</math> (GPa)</b>	<b>Final <math>E</math> (GPa)</b>	<b>Initial T (°C)</b>	<b>Final T (°C)</b>	<b>% change/°C</b>
<b>DMTA 1</b>	319.9	313.2	40.2	147.7	-0.019
<b>DMTA 2</b>	394.1	378.7	29.8	299.1	-0.015
<b>DMTA 3</b>	426.7	416.4	24.3	177.4	-0.016
<b>DMTA 4</b>	380.3	362.9	52.7	299.5	-0.019
<b>DMTA 5</b>	425.6	408.7	24.4	212.1	-0.021
<b>DMTA 6</b>	424.5	399.5	27.7	276.9	-0.024
<b>DMTA 7</b>	427.1	395.7	25.5	277.3	-0.029
<b>DMTA 8</b>	425.8	401.4	26.4	276.9	-0.023
<b>DMTA 9</b>	367.4	344.9	27.7	299.5	-0.023
<b>Improved DMTA 1</b>	401.8	376.6	50	300	-0.025
<b>Improved DMTA 2</b>	393.4	375	75	300	-0.021
<b>Improved DMTA 3</b>	393.8	375	27	300	-0.017
<b>Improved DMTA 4</b>	400.7	375.8	26	300	-0.023

#### 5.4 DMTA testing of free-standing GaN

Free-standing GaN samples, produced by Lumilog, were purchased and were n-doped LED quality epi-finished wafers. These samples were grown by metal-organic vapour phase epitaxy (MOVPE) on a sapphire substrate and were subsequently separated from the substrate, then cleaned and polished. The wafer is orientated to the (0001) plane with an error of  $0.25 \pm 0.1^\circ$ , meaning that is well-orientated from the point of view of measuring  $E_{33}$ . As the initial measurements showed that having well-defined geometry dramatically reduced error in the modulus, two GaN wafers were sent for laser cutting at an external contractor (Laser Micromachining Limited). One wafer was cut into 5 mm wide strips parallel to the major flat of the wafer at [11-20] and the other wafer was laser-cut into 4 mm wide strips at different angles, between  $0^\circ$  and  $30^\circ$ , corresponding to the directions presented in figure 5.5



(a)



(b)

**Figure 5.5** (a) Directions in the (0001) Plane and corresponding angles with respect to the crystalline structure. (b) Diagram showing how the GaN wafer was laser cut.

The first method used to measure the elastic modulus of GaN was DMTA, using the same techniques used with Si and sapphire. Firstly, each was tested at room temperature for 30 minutes. The modulus of the sample was measured up to 600°C with a heating rate of 2°C/min. Every 50°C, the sample was held at that temperature for 5 minutes. Due to the expense incurred in purchasing the free-standing GaN and laser cutting and the high risk of breakage, additional static force was not used with the laser cut GaN measurements. Therefore a calibration method, based on additionally measuring Si, will be used to correct the GaN measurement.

#### ***5.4.1 Room temperature measurements of GaN sample***

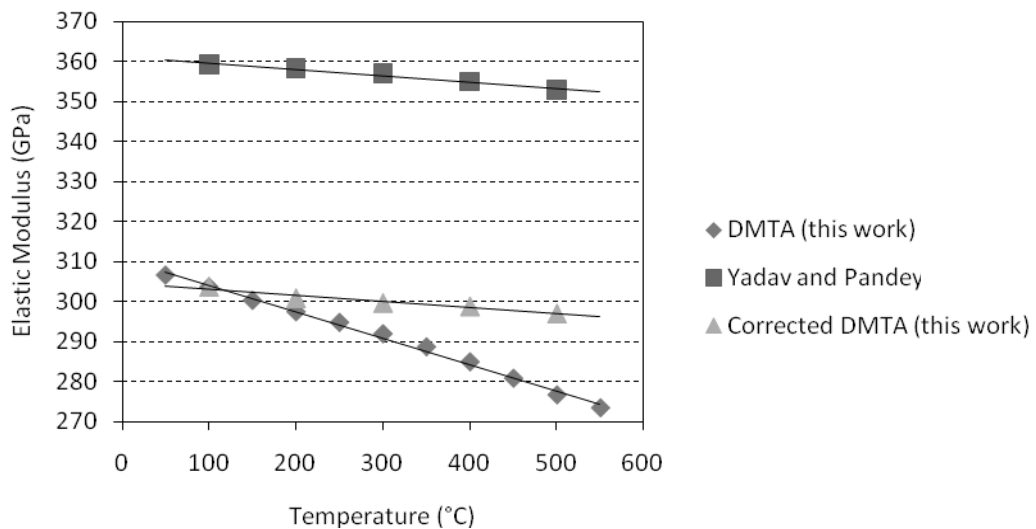
The elastic moduli of two similar GaN wafers were measured; one being the laser cut samples from the same wafer with the DMTA and the other wafer was tested using impulse excitation [97]. The advantage that the impact excitation method has over the DMTA is that it can test both an entire wafer and individual laser cut strips, see figure 5.5 (b), non-destructively, whereas the DMTA requires a wafer to be cut into strips. The samples tested with the DMTA at room temperature had a measured elastic modulus of 304 GPa and the wafer tested by impact excitation had an elastic modulus of 279 GPa. This may be due to variation in material or the measurement method. Additionally, there are some geometrical errors in the impact excitation measurement because the presence of the wafer flat in figure 5.5 (b), used to determine the wafer orientation, was ignored.

#### ***5.4.2 GaN high temperature elastic modulus measurements and calibration approach***

The elastic modulus of GaN was measured up to 500°C using the DMTA method. The elastic modulus decreased by 27 GPa between 100°C and 500°C, corresponding to a decrease of 8.89%. Using the Yadav and Pandey data as a comparison [27], it was clear that the elastic modulus decreased more rapidly than expected with temperature using the DMTA. For Yadav and Pandey, the modulus decreased by 6

GPa, corresponding to a decrease of only 1.76%. As discussed in section 5.3, initial measurements on silicon also showed a larger than expected decrease in modulus, and this suggests that the larger than expected modulus decrease is due to a systematic error in the DMTA. The likely cause of this systematic error is the thermal expansion of the steel clamps. Steel has much larger CTEs than both GaN and Si [154] and this causes inaccuracies in the DMTA's strain measurements.

In order to account for the systematic error of the DMTA, the most characterised material (Si) was used as a calibration material. Assuming that the error should remain roughly constant throughout the experiment, it was possible to recalibrate the values obtained by devising a simple equation. This equation is based on the modulus decrease seen in Si as measured by Cho [58]. After recalibration, the elastic modulus of GaN decreased by only 6.58GPa or 2.17% between 100°C and 500°C with good agreement with the limited data in the literature. Figure 5.6 shows the change in the  $E_{33}$  modulus of GaN with respect to temperature for the literature data, uncorrected DMTA data and corrected DMTA data.

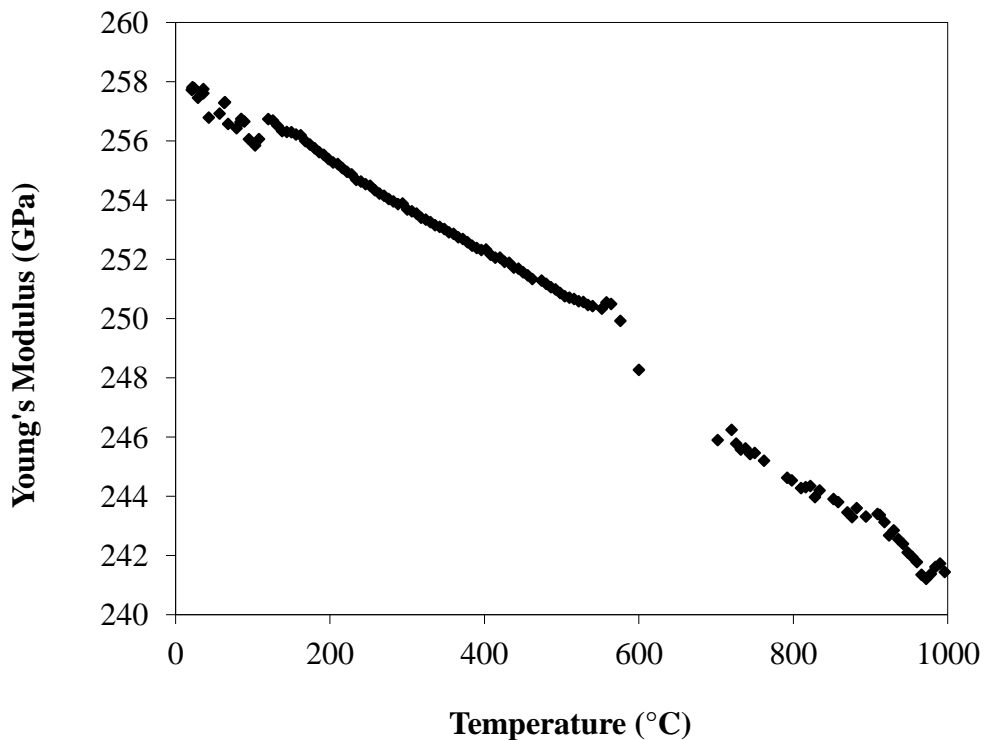


**Figure 5.6**  $E_{33}$  modulus as a function of temperature for (0001) GaN [155]

In addition to these measurements, a complete 2 inch diameter, 0.3 mm thick GaN wafer was sent to IMCE [97], for impact vibration testing between room temperature and 1000°C. As figure 5.7 shows, the modulus of GaN decreases from 255.9GPa at



103°C to 250.8GPa at 504°C and this corresponds to a 1.99% decrease. This is very close to the result obtained from the DMTA after using the silicon calibration method, providing further evidence that using the calibration approach with GaN in the DMTA is valid and a good, simple approach to take. The impact excitation data is also available up to 1000°C, as shown in figure 5.7, which has yet to be reported in the literature. This data shows that the total decay in modulus from 25 to 1000°C is 7% from 258 to 240 GPa, which is very low and suggests that the material remains mechanically stable. However, the data remains patchy between 575 and 650°C and coincides with a peak in internal friction.



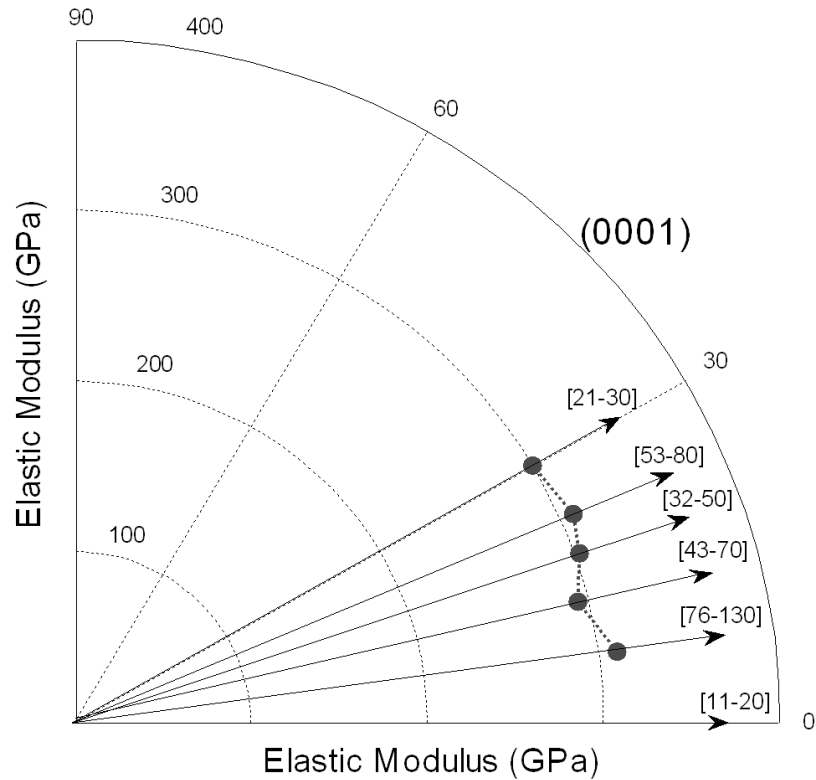
**Figure 5.7** The  $E_{33}$  modulus as a function of temperature for (0001) GaN measured by impact vibration at IMCE.

Some research has been done into ways of improving the accuracy of DMTA measurements [156-159]. Potential methods for improving the accuracy of the DMTA include using a different clamping system and running the experiment in an inert gas, such as Ar rather than air. Additional sources of variation between literature and experimental data are subtle differences between substrates including dislocation density, growth conditions and doping. The wafers were n-doped and the addition of

dopants is known to change both the elastic modulus and its temperature dependency, through changing the intrinsic strain in the material [160-162].

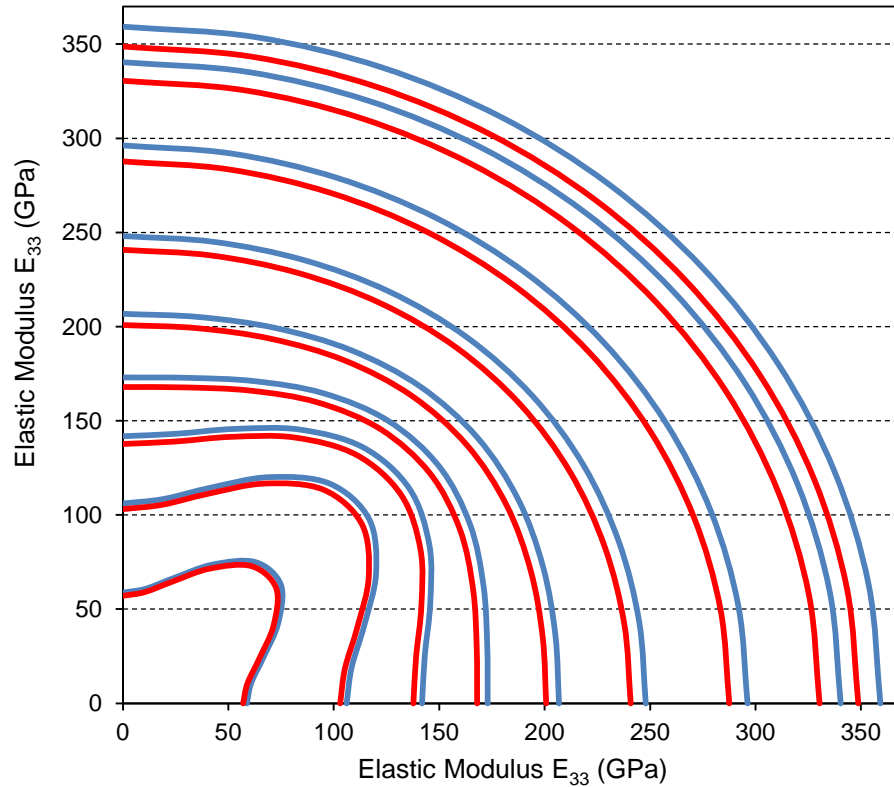
#### ***5.4.3 Isotropy of GaN in the (0001) Plane***

GaN, like other wurtzite crystal structure materials, is considered to be isotropic in the basal (0001) plane [163-165]. The isotropy of GaN along the (0001) plane was evaluated using the DMTA on differently orientated pieces from the specifically cut Lumilog GaN wafer. Five samples laser cut from this wafer corresponded to five orientations in the (0001) plane, which are [76-130], [43-70], [32-50], [53-80] and [21-30], see figure 5.5 (a) for more details. All of these samples were tested at room temperature for 30 minutes and the average modulus was calculated. These results show that the mean elastic modulus was  $304 \pm 2.58$  GPa. Figure 5.8 shows a polar plot of the elastic modulus of the GaN wafer as a function of orientation. Figure 5.8 shows that GaN does indeed appear to be isotropic along the basal plane and the small variations between the modulus of each sample are expected due to measurement error or variation in material.



**Figure 5.8** Polar Plot of the Elastic Modulus at Room Temperature (DMTA Results).

A polar plot of the  $E_{33}$  of GaN, presented in figure 5.9, was computed from the Yadav and Pandey data [155] by rotating the stiffness matrix. Figure 5.9 describes a plane and the orientations from  $0^\circ$  to  $90^\circ$  with respect to the (0001) plane in the  $c$ -axis. The outer curve corresponds to the (0001) plane; each curve closer to the origin is a plane at an angle increasing from  $10^\circ$  to  $90^\circ$ . The blue line corresponds to  $E_{33}$  at  $100^\circ\text{C}$  and the red line corresponds to  $700^\circ\text{C}$ . Figure 5.9 does not calculate the modulus from the crystal structure of GaN, but provides valuable information about the orientation dependent isotropy and anisotropy of the material's modulus.



**Figure 5.9** Polar Plot of  $E_{33}$  depending on Temperature and Orientation [155].

Both plots reveal an isotropic behaviour in the (0001) plane showing that as the plane changes the elastic behaviour of GaN becomes increasingly anisotropic. Additionally, the isotropy of the (0001) plane is temperature independent. This isotropic behaviour of the (0001) GaN plane makes it a very useful material for MEMS and NEMS applications because the device will not be sensitive to orientation, therefore simplifying design of cantilevers and GaN/sapphire diaphragm sensors. This is analogous to (111) orientated Si [166] whose stiffness is nearly-isotropic and it the orientation of choice for similar Si-based devices.

## 5.5 Conclusions

DMTA has been used to successfully measure the  $E_{33}$  of GaN and silicon, and their respective decrease with respect to temperature. Using DMTA, it is relatively straightforward to get a measurement of the modulus of stiff, brittle materials and

their modulus decrease as a function of temperature. However, obtaining an accurate measurement requires more work due to the difficulty of correctly constraining the sample without damaging it and the need for the sample to have well-defined geometry. For less stiff materials, such as silicon, it is possible to obtain results that are close to the literature. For very stiff materials, such as GaN, the percentage decrease in  $E_{33}$  using the DMTA is close to the literature after calibration using silicon data. Further measurement of the modulus variation with respect to temperature using impact excitation supported the DMTA result and this approach provides the first measurement of GaN at temperatures up to 1000°C.

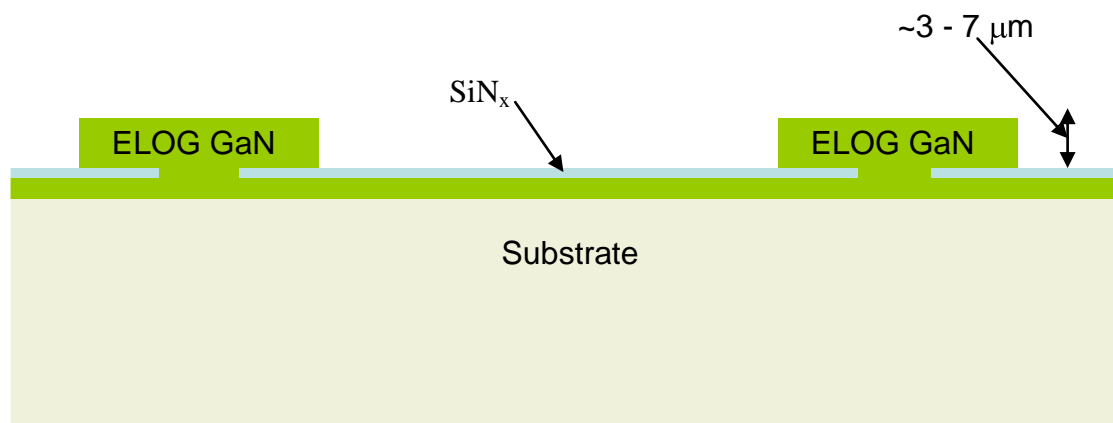
Ultimately these results show that the moduli of silicon, sapphire and GaN are very stable with respect to temperature and show little decay. In fact, the variation in the measured stiffness from room temperature to 1000°C is much smaller than the variation in wide range of room temperature data reported in the literature, shown in table 1.2. The work in this chapter suggests that these materials will work well as MEMS sensors at high temperatures because their stiffness does not vary significantly with temperatures. The work done in this chapter will support the modelling, design and fabrication work that is done in the remainder of this thesis.

**The next chapter will discuss the progress made in developing cantilever and beam templates for potential GaN sensors using an epitaxial layer overgrowth (ELOG) method.**

## CHAPTER 6: REALISATION OF A GAN-SENSOR MADE USING AN EPITAXIAL LAYER OVERGROWTH (ELOG) TECHNIQUE

### 6.1 Motivation

High-quality, low-defect GaN material is the motivating reason behind the fabrication of ELOG cantilevers. Although it is straight forward to etch cantilevers out of GaN grown epitaxially from a bulk substrate [43-46], the cantilevers that are formed are often poor quality as shown in section 1.5. Traditional GaN layers grown epitaxially on a sapphire, silicon or SiC substrate typically have dislocation densities between  $10^8 - 10^{10}$  dislocations/  $\text{cm}^2$  [55]. High dislocation densities are caused by the material relieving strain caused by lattice mismatch. The effects of lattice mismatch can be reduced by the device not being in full contact with the substrate during growth. For example, GaN grown by near-identical lateral overgrowth techniques known as epitaxial layer overgrowth (ELOG), pendeo-epitaxy (PE), or cantilever epitaxy (CE) have lower dislocation densities of  $10^6 - 10^8$  dislocations/  $\text{cm}^2$  [16, 167]. Decreased defect densities have the potential to improve the performance of any potential sensing device, as well as improved reliability due to greatly reduced strain profile. Using epitaxial layer overgrowth (LEO, ELO or ELOG); will allow the fabrication of higher quality MEMS devices.



**Figure 6.1** Schematic showing the result of the ELOG GaN growth process.

The basic ELOG process starts with a ~40 nm of SiN<sub>x</sub> (silicon nitride) being deposited on a 2-inch GaN/sapphire wafer by plasma-enhanced chemical vapour deposition (PECVD). A photosensitive mask was used to pattern the SiN<sub>x</sub> and this pattern was plasma etched, creating GaN growth windows. GaN grows firstly vertically, until it reaches the height of the SiN<sub>x</sub> mask. Once the GaN reaches the height of the SiN<sub>x</sub>, it will start to overgrow laterally over the SiN<sub>x</sub> as it increases in thickness: this is what is known as ELOG. This process will be described in detail in sub-section 6.3.1 and a schematic image of the resultant growth from this process is shown in figure 6.1.

GaN has a typical misfit of 13 – 17% with a substrate such as (111) silicon or sapphire [119, 168, 169], causing a large density of threading dislocations at the interface, as discussed in chapter 1. Although threading dislocations reduce the amount of strain in the GaN layer, they trap electrons reducing performance. Less threading dislocations are expected in an ELOG based device because only the GaN growth column is in contact with the substrate or buffer layer. Strains as a result of a lattice misfit are intrinsic, meaning they result in plastic deformation [170], and cannot be removed by etching away the substrate. Dislocations result in the released cantilever having a rough surface when etched from a bulk substrate [43], making it difficult to fabricate a transducer directly on the device. Dislocations cause interface traps in the conduction channel, where charge carriers get trapped [2] and this reduces the efficiency of the device. Tests show that GaN LEDs made using ELOG have a 10000 hours longer lifetime than expected [171, 172]. Experimental measurements have shown that high-quality ELOG GaN films exhibit no measurable current leakage [173]. Additionally, current leakage does not occur in the wing, or lateral overgrowth, area [173]. Therefore, better quality sensors can be fabricated from ELOG GaN material.

Due to their small size and desirable material properties, there are numerous potential applications for ELOG sensors. ELOG sensors have the advantage of being small and can be fabricated in arrays. ELOG cantilevers can also be used as accelerometer sensors in harsh environments such as on satellites, aeroplane and car engines, or oil rigs. ELOG devices in [167] were shown to have less noise due to a lower density of threading dislocations. As the sensors will be approximately 3 to 6 μm thick and have

a low dislocation density; they are likely to have a large gauge factor, and will be suitable for use as either a dynamic and static sensor [29].

The MEMS devices can then be etched out of suitable overgrown ELOG templates and have a transducer deposited on them, creating a small mechanical sensor. A HEMT is a possible sensing element for the ELOG cantilevers. However, creating a working device from ELOG growth is a difficult, iterative process because the potential of this method for producing sensing templates is not fully known. This chapter will show proof of concept and the thought process that went into the design of the ELOG sensor. The ELOG growth process have previously been used to growth low-defect GaN for LEDs [171, 172], but little work has been done in making a MEMS mechanical sensor.

## **6.2 Aims of the chapter**

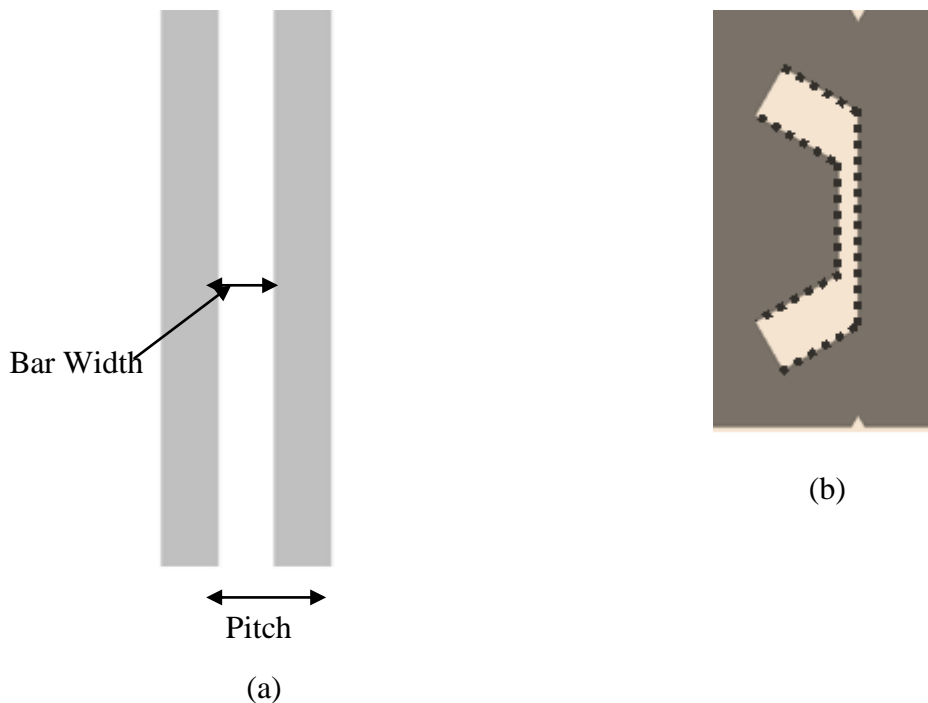
The over-riding aim of this chapter is to show proof of the ELOG sensor concept. Firstly, a prototype mask set was designed in order to determine the overgrowth behaviour of GaN and potential ELOG templates. The results from the first ELOG growth will be analysed using both SEM and optical microscopy to determine the amount of lateral overgrowth and quality of the material. The information gathered from these images will be used to inform the design of the second mask set.

The design process for the second mask set will then be described and improvements on the previous design will be discussed. There will also be a detailed critique of the first mask design. The second mask set is a full set of five photolithographic masks, designed to create fully functional ELOG devices. Therefore a process flow was devised that will allow the release of the MEMS devices from templates and the fabrication on a HEMT-style transducer. The second mask set was designed based on this process flow and there will be a brief discussion on this work. The ELOG cantilevers will then be released, demonstrating the viability of creating a sensor by ELOG. The release process will be described and the resulting ELOG devices will be described. This chapter aims to show a novel approach for creating GaN harsh environment sensors.



### 6.3 Design of the first mask set for cantilever devices.

The first practical step in fabricating viable MEMS devices is to design a mask set. A mask set is designed using a computer-aided design (CAD) program called ‘CleWin 4’, which is the industry standard software described in section 2.5. Initially, a prototype mask set was designed in order to test potential devices; with the most successfully grown devices being used in the final mask sets. Therefore the mask and device design process will be iterative, going through several stages before the final devices are decided upon. The geometric shape of the devices will have a significant effect on their performance because the cantilevers are being created by epitaxial layer overgrowth (LEO, ELO or ELOG). In the first prototype mask set, two types of device were trialled, the ‘stripe’ and ‘double-dogleg’ cantilevers, with different dimensions and fill factors. A schematic of the two different designs is shown in the figure 6.2.



**Figure 6.2** Schematic of the cantilever device designs from the first prototype mask set. (a) ‘Stripe’ design. (b) ‘Double-dogleg’ design with dotted lines. (See tables 6.1 and 6.2, and figure 6.3 for appropriate scales.)

The two key dimensions for the stripe design in figure 6.2 (a) are the bar width  $w$  and the pitch  $p$ , which is the total width of the device. Four different  $w$  dimensions were used in the prototype design and these were 3, 5, 7 and 9  $\mu\text{m}$ . The reason for the dimension variation was to see the impact of the width of the GaN bars on the ELOG structure. The different pitch ratios are  $3w$ ,  $4w$ ,  $5w$  and  $6w$  for each respective bar width; this was undertaken to test the impact of different fill factors on the growth. The fill factors, which is defined as the pitch subtracted by the bar width, are important because ELOG growth occurs because of a gas diffusion mechanism, meaning that the degree of overgrowth is affected by the distance between GaN growth windows. There are 16 variations of stripe devices on the mask set as a result, as shown in table 6.1. The analysis of the results from the initial growth runs on the stripe patterns will be used in the design of future cantilever mask set.

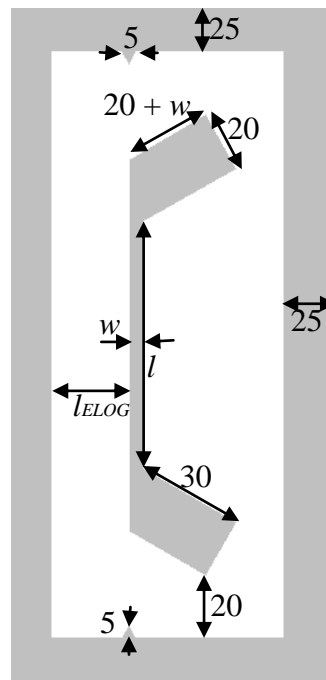
**Table 6.1** Different variations of ELOG stripe templates (dimensions in  $\mu\text{m}$ )

<b>Bar width</b>	<b>Pitch 1</b>	<b>Pitch 2</b>	<b>Pitch 3</b>	<b>Pitch 4</b>
3	9	12	15	18
5	15	20	25	30
7	21	28	35	42
9	27	36	45	54

GaN has a natural tendency to grow in hexagonal facets when orientated in the (0001) direction due to its lattice structure [174, 175], which is why the double dogleg design in figure 6.2 (b) consists of two overlaid semi-hexagons (marked by the dotted lines in figure 6.2 (b)). The dimensions of the double-doglegs were varied in order to test their impact on the lateral overgrowth of the device. The dimensions to be varied are the bar length  $l$ , the bar width  $w$ , the ELOG growth window length, and the fill factor  $l_{ELOG}$ . The growth window length is determined the fill factor, and these are  $3w$ ,  $4w$  or  $5w$ . A schematic of a double-dogleg labelled with the fixed and variable dimensions is included in figure 6.2.

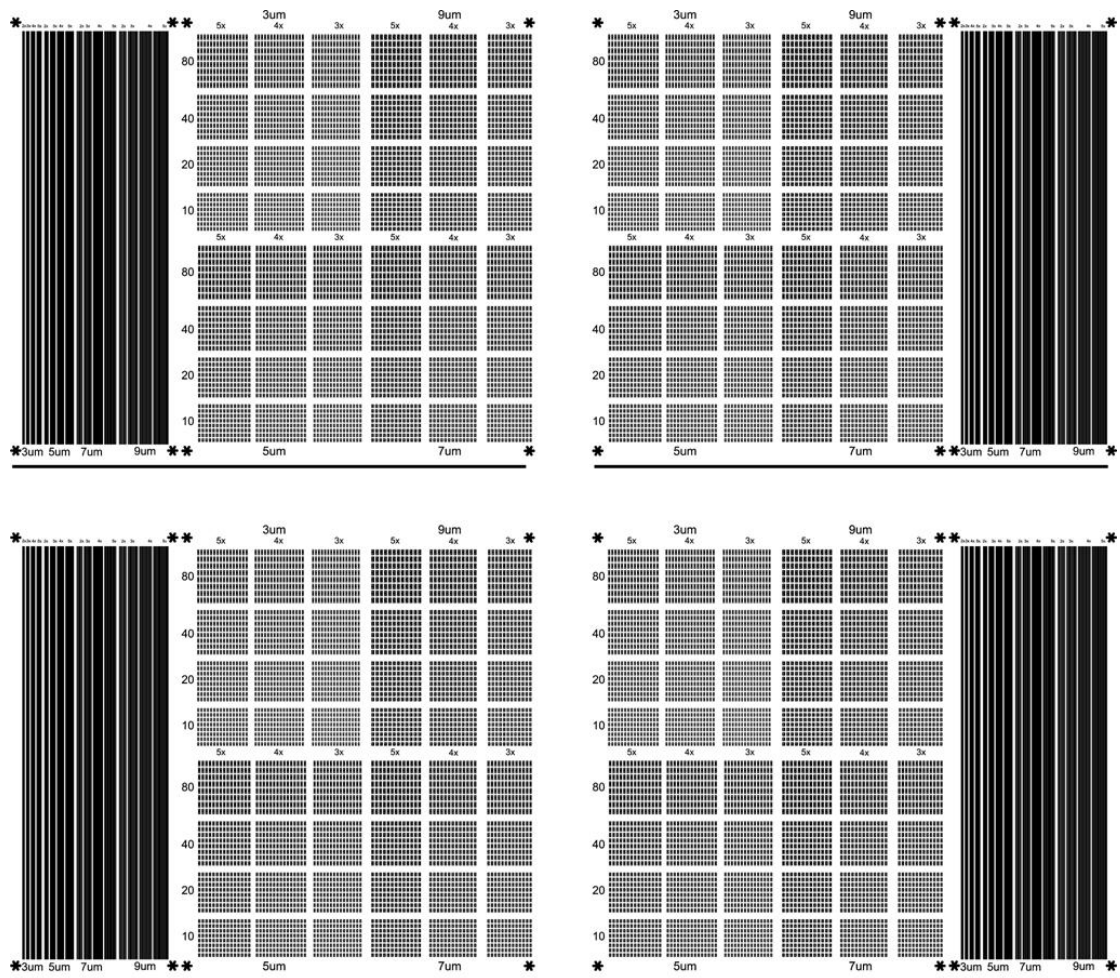
**Table 6.2** Different variations of ELOG double dogleg templates (dimensions in  $\mu\text{m}$ )

Bar width ( $w$ )	Bar length ( $l$ )	Fill factor 1	Fill factor 2	Fill factor 3
3	10	9	12	15
3	20	9	12	15
3	40	9	12	15
3	80	9	12	15
5	10	15	20	25
5	20	15	20	25
5	40	15	20	25
5	80	15	20	25
7	10	21	28	35
7	20	21	28	35
7	40	21	28	35
7	80	21	28	35
9	10	27	36	45
9	20	27	36	45
9	40	27	36	45
9	80	27	36	45



**Figure 6.3** Double dogleg cantilever labelled with the various dimensions, with the numeric values in  $\mu\text{m}$ .

The four different  $l$  variables used on the first prototype mask set were 10, 20, 40 and 80  $\mu\text{m}$ , whilst 3, 5, 7 and 9  $\mu\text{m}$  are the different  $w$  options. Combining this with the three different fill factors gives 48 independent combinations of double-dogleg cantilevers in the initial prototype mask set, shown in table 6.2. This gives 64 different sub-types of devices, stated in tables 6.1 and 6.2, and each will behave differently under GaN-ELOG conditions. The growth behaviour of each different device sub-type will need to be analysed using optical and electron microscopy, discussed later in sub-section 6.3.2.



**Figure 6.4** First Prototype Mask Set design.

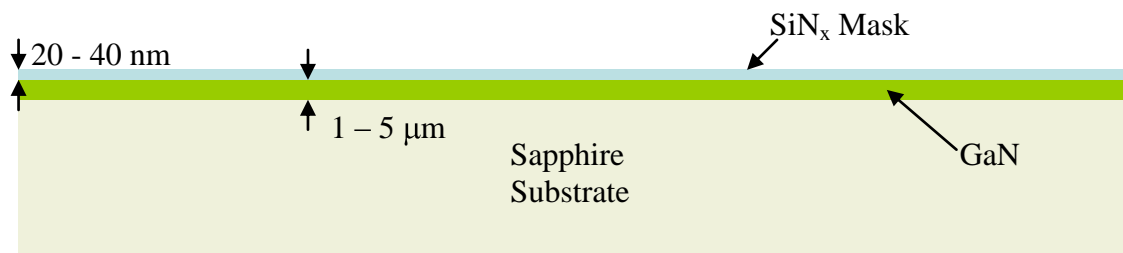
The stripe and double dogleg devices were arranged into the design shown in figure 6.3, and this is the first prototype growth mask. The design consists of four chips, with the stripe designs always on the outer edge. The stripes are always placed on the

outer edge because the design is a tight fit on a 50 mm wafer and the stripes are partially sacrificial because they are 20 mm long. The mask design also provides the provision for four chips on a wafer, this means the wafer can be cleaved into quarters before the ELOG GaN growth and this allows more growth trials. The cantilevers grown using ELOG aim to be comparable in size to those fabricated by Stonas *et al* [43, 44, 46] that have typical lengths of  $\sim 100 \mu\text{m}$ . Larger cantilevers of  $17 \times 5 \text{ mm}$  were produced by Vilak *et al* [30, 32, 33] and Strittmatter *et al* [4, 31]. Initial results from the fabrication and ELOG growth trials on a GaN/sapphire wafer, used because the Si/PD wafers were not ready, will be discussed in section 6.4.

### 6.3.1 Method for Patterning GaN/Sapphire wafers for ELOG growth

The prototype cantilevers were initially grown on GaN/sapphire substrates because GaN is compressively stressed at room temperature and sapphire is the most commonly used substrate for GaN growth. Alternative wafers for this process are GaN/Si and GaN/Si/PD; but the GaN layers on both types of wafer liable to crack after ELOG GaN growth due to CTE mismatch (see figure 1.10) and the GaN/Si/PD wafers discussed in chapter 3 were still in development. The patterning of the wafer was done at the nanofabrication facilities at the University of Bath. The mask material used for the patterning will be  $\text{SiN}_x$  because it is known to encourage ELOG GaN growth [176]. The following section describes the process required to pattern a wafer for ELOG growth.

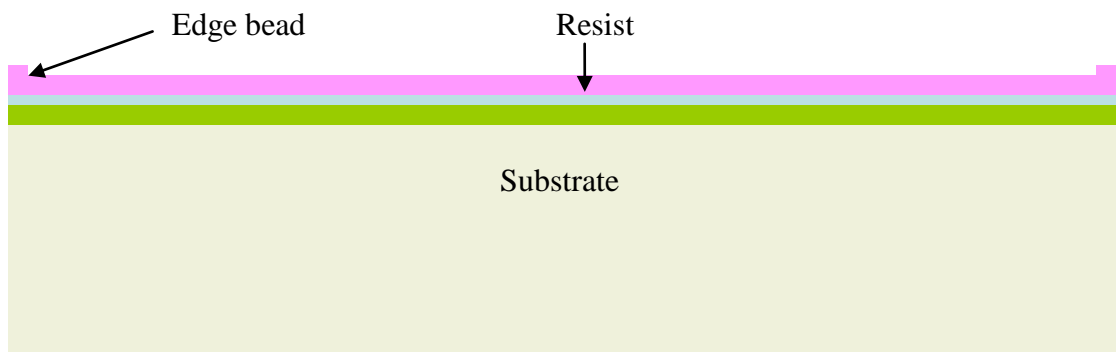
1. Coat a GaN/Sapphire wafer with a thin layer of  $\text{SiN}_x$  using PECVD



**Figure 6.5** Schematic of a Sapphire/GaN/ $\text{SiN}_x$  wafer used for ELOG growth.

Ideally, the SiN<sub>x</sub> layer should be between 20 and 40 nm thick and uniformly cover the entire wafer. The thickness and uniformity of the SiN<sub>x</sub> layer can be measured to a high degree of accuracy using reflectance measurements. Any SiN<sub>x</sub> layer found to be non-uniform or of the wrong thickness was removed using a plasma etch in the ICP etcher.

2. *Spin coat, then soft bake a layer of 1813 resist on top of the SiN<sub>x</sub>*



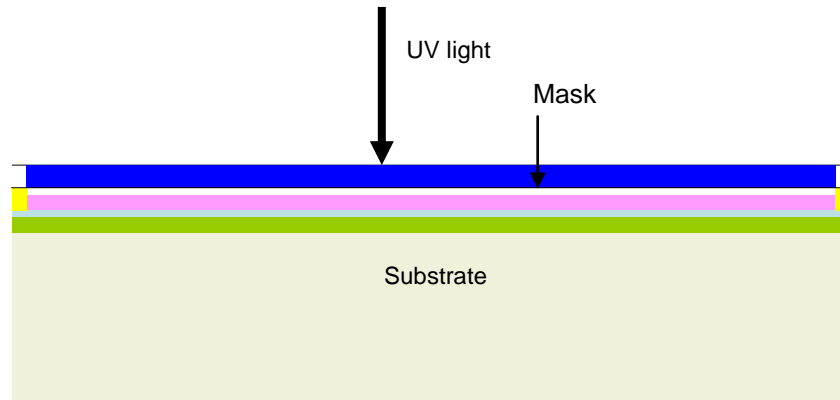
**Figure 6.6** Sapphire/GaN/SiN<sub>x</sub> wafer coated with 1813 resist and edge bead.

The wafer was placed on a spin coater under a vacuum and was coated with 1813 positive working resist with a pipette. This resist was used because it is compatible with the current mask and first layer of the second generation mask set (see section 6.4) and a standard spin coating recipe was used. Once the spin coating was finished, the wafer was soft baked for three minutes at 115°C to cure the resist.

3. *Remove the edge bead*

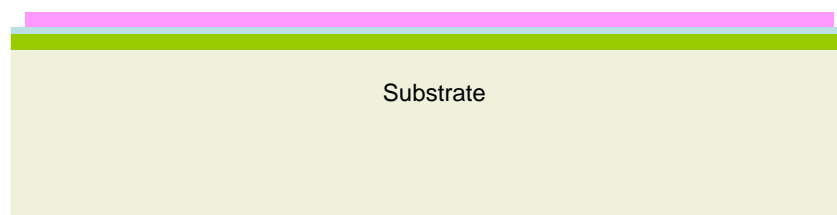
The problem with the spin-coating process is that it causes a build up of resist at the edge of the wafer, known as the 'edge bead'. The edge bead is easily removed and this is done using the following process.

- i. Place the edge bead removal photolithography mask into the mask aligner and align the wafer to the mask. The edge bead removal mask is the shape of a wafer of the wafer but slightly smaller, allowing the resist at the edge to be exposed and removed.
- ii. Expose the pattern to UV light for one minute



**Figure 6.7** Exposure of edge bead to UV light.

- iii. Place wafer in a 351 developer solution (1 part developer: 3.5 parts distilled wafer) for 45 seconds. 351 developer is the standard developer used with 1813 resist.



**Figure 6.8** ELOG wafer with edge bead removed.

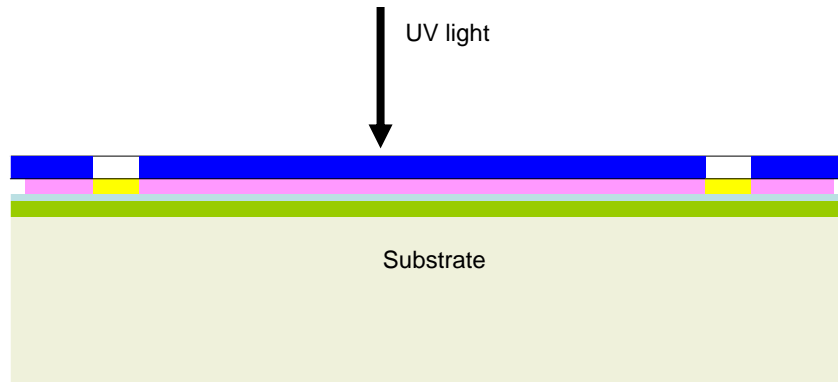
4. *Pattern the wafer using first photolithography mask and mask aligner*

Ultimately, a five stage mask set will be designed and fabricated for processing ELOG cantilevers. However as the first prototype mask was only to be used in growth trials, it consisted of a single mask. The first prototype mask, as shown in figure 6.3,

and for later iterations the first stage mask (see figure 6.19), was inserted into the mask aligner.

The following process was used to pattern the wafer:

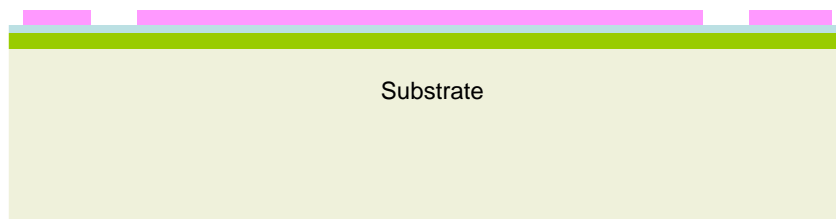
- i. Use the alignment marks on the mask to align the wafer into position.
- ii. Bring the mask and wafer into contact. Good contact is achieved when an interference pattern is visible on the mask. Care was taken not to apply too much force on the wafer when bringing the wafer into contact to avoid breaking the mask.
- iii. Expose the mask and wafer to UV light for 10 seconds when the UV intensity is  $4.5 \text{ mW}/\text{cm}^2$ .



**Figure 6.9** First ELOG pattern being imprinted using UV light.

- iv. Place wafer in a 351 developer solution (1 part developer: 3.5 parts distilled wafer) for 45 seconds.





**Figure 6.10** The ELOG pattern after UV patterning and development.

5. *Repeat process for all wafers and then check wafer surface quality using an optical microscope*

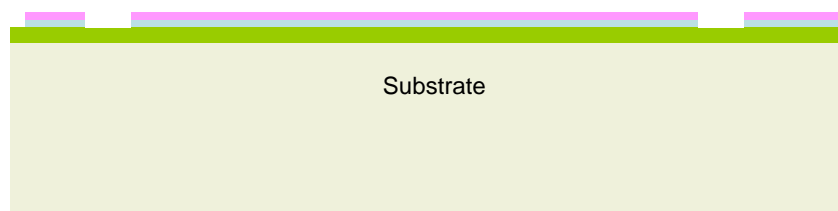
Once all of the wafers have been patterned with resist, they have to have their surfaces checked by optical microscopy in order to determine whether the photolithography was successful. Wafers with a large amount of surface roughness were deemed unsuitable for ELOG and had to be discarded. Wafers are sometimes covered in excess resist; these wafers are usually underdeveloped and are placed in the 351 developer for an additional 30 seconds. If additional time in the developer fails to remove all of the excess resist, then the resist is underexposed and is removed with acetone. The wafer is then cleaned and the patterning process starts again from step 2.

6. *Perform an O<sub>2</sub> de-scum and check pattern uniformity using a Veeco Dektak*

Even after time in the developer, small amounts of residual resist remain on unintended parts of the wafer. Performing an O<sub>2</sub> de-scum in the ICP etcher removes the residual resist fragments, but at the expense of reducing the thickness of resist over the pattern. The de-scum time has to be calculated carefully so that the pattern is not damaged, although a small reduction in the thickness of the resist is acceptable. Once a de-scum cycle is completed, the thickness of the resist is checked using a Dektak profilometer (see section 2.2). If the layer of resist over the pattern becomes too thin, then all the resist on the wafer will have to be stripped from the wafer and the wafer will need to be patterned again following steps 2 – 5.

7. *Etch through uncovered SiN<sub>x</sub> using CHF<sub>3</sub> gas in the ICP*

Once all residual resist has been removed from the unpatterned regions of the wafer, the SiN<sub>x</sub> can be etched using the ICP. The time required to etch through the SiN<sub>x</sub> is determined by the thickness of this layer when measured in step 1. The wafers to be etched are placed on an ICP plate and held in place with pieces of a silicon wafer held to the plate using hot wax. The wafers are etched in batches of 4-5, with a piece of SiN<sub>x</sub> on Si with a known thickness is placed in the centre. The piece of SiN<sub>x</sub> on Si is needed to determine etch depth and uniformity. The plate is then placed in the ICP and the chamber is brought down to vacuum.



**Figure 6.11** ELOG wafer after SiN<sub>x</sub> etch.

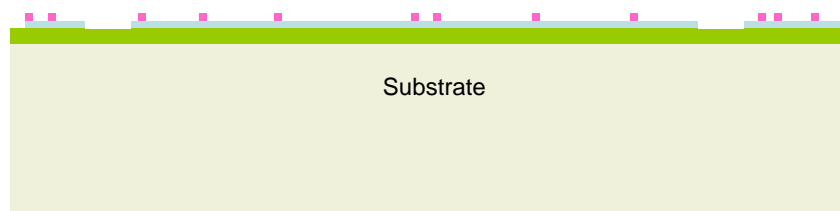
Once the etch cycle is complete, the piece of Si on SiN<sub>x</sub> is removed from the plate and the new SiN<sub>x</sub> thickness and uniformity is measured using reflectance. If the reflectance measurements show that more SiN<sub>x</sub> was removed than was present on the ELOG wafers, then they have been successfully etched. Otherwise, the wafers will require an additional etch cycle.

8. *Remove exposed resist using a resist stripper solution in a ultrasonic heat bath*

ELOG GaN will not grow on regions covered by resist, so the resist needs to be stripped in a manner that does not damage the pattern. However, 1813 resist exposed

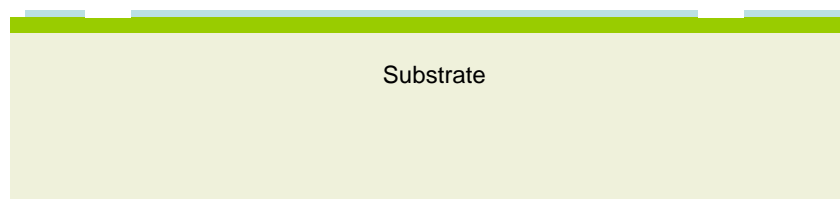
to UV light is difficult to remove. The bulk of the resist is removed using 1165 resist stripper in an ultrasonic heat bath. The stripper is poured into a beaker and heated to 65°C in a heat bath. The wafer is placed in the beaker and the ultrasound is switched on for 10 minutes at 30% intensity. The wafers are then checked for excessive resist using an optical microscope and the stripping process will continue the bulk of the resist is removed.

9. *Remove residual resist with an O<sub>2</sub> plasma etch*

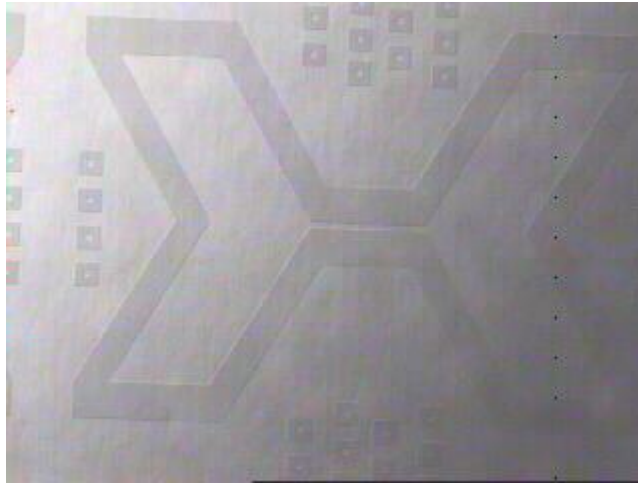


**Figure 6.12** ELOG wafer after stripping, with residual resist still remaining.

It is very difficult to remove all of the resist using stripper and ultrasound without damaging the pattern, so a final cleaning step is needed to remove any resist residue. The remaining resist is removed using an O<sub>2</sub> de-scum in an ICP etcher.



(a)



(b)

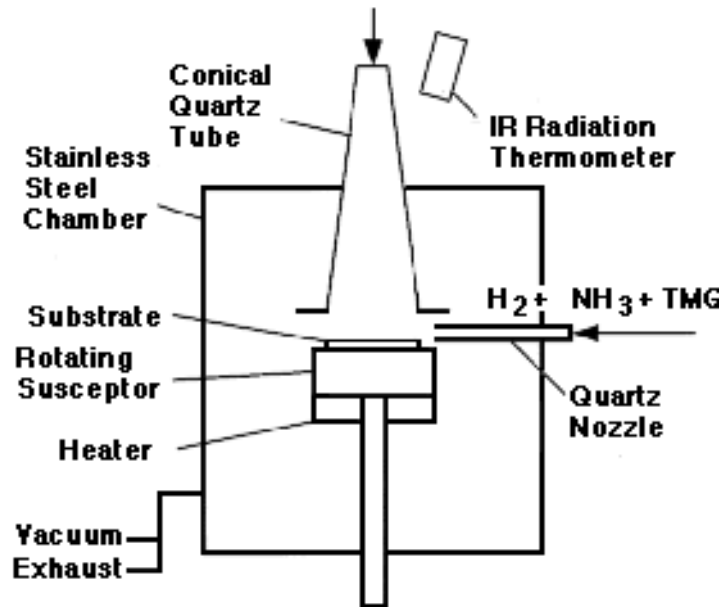
**Figure 6.13** ELOG wafer after O<sub>2</sub> de-scumming etch, where (a) is a schematic side view diagram and (b) is an optical image of a sample that has been patterned, CHF<sub>3</sub> etched and had all of its resist stripped (The growth results from this sample are shown in figure 6.20).

Once the O<sub>2</sub> descum etch was completed, the wafer surface was checked for any remaining resist and the wafer is subjected to another de-scum if any resist remains. Once the wafer is resist free, it is ready for an HCl dip and ELOG growth. The HCl dip is performed to remove surface oxides from the GaN because they affect the quality of the ELOG growth. GaN epitaxial growth is a specialist activity and this was undertaken by an in-house post-doctoral researcher who specialises in this activity.

### ***6.3.2 Description of the MOCVD/MOVPE process***

In this project, all GaN growths are done internally by a specialist III-V nitrides grower due to time constraints and access issues. However, the reader needs to know some basic knowledge of the GaN crystal growth process to interpret the results shown later in this chapter. The process for growing monocrystalline, wurtzite GaN grown for this PhD is described interchangeably using either of two acronyms, metallo-organic chemical vapour deposition (MOCVD) or metallo-organic vapour

phase epitaxy (MOVPE). A basic schematic of a MOVPE reactor is shown in figure 6.14.

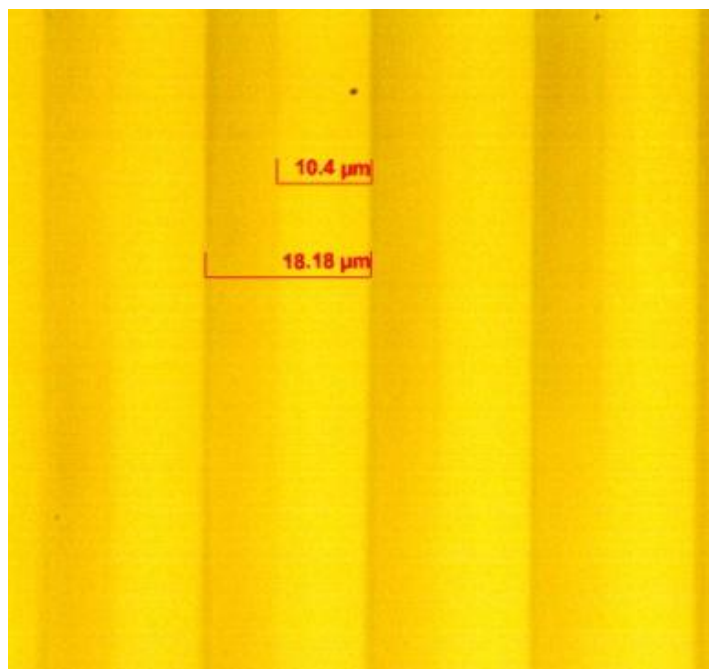


**Figure 6.14** A schematic diagram of a MOVPE reactor [177].

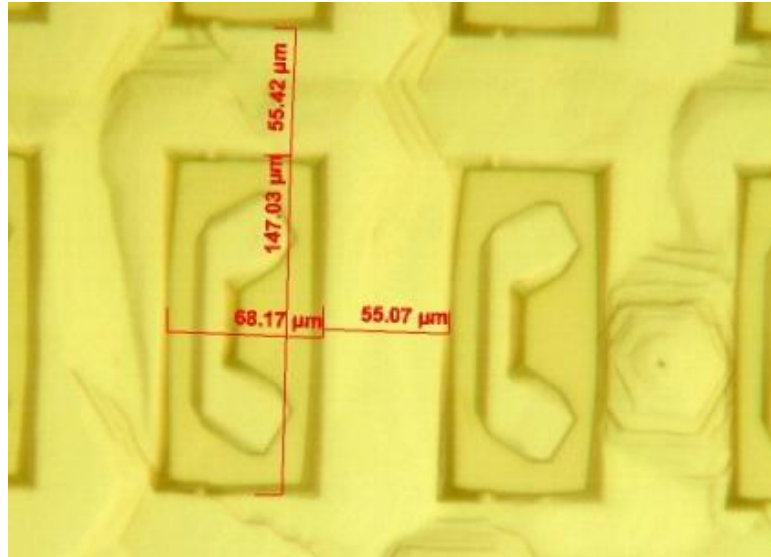
The premise of a MOCVD reactor is similar to that of ICP and PECVD, in that it consists of a heated vacuum chamber, with entry points for the plasma reagent gases. In a MOCVD reactor, the reagent gases are ammonia, tri-methyl gallium (TMG) and tri-methyl aluminium (TMA) [177]. Hydrogen gas is used for the cleaning of the reactor and some reactors also have the capability of using tri-methyl indium (TMI) for InN growth. GaN is produced using TMG and ammonia as the reagent gases, with AlN produced using TMA and ammonia. The production of AlGa<sub>x</sub>N uses TMA, TMG and ammonia. Typical by-products of MOCVD growth are hydrogen and methane. MOCVD growth of GaN on Si and sapphire occurs at 1000 to 1100°C [177] in order to maximise the crystal growth rate and produces high-quality single crystal GaN with a wurtzite crystalline structure.

### ***6.3.3 Results of the growth of ELOG cantilevers from the first mask set***

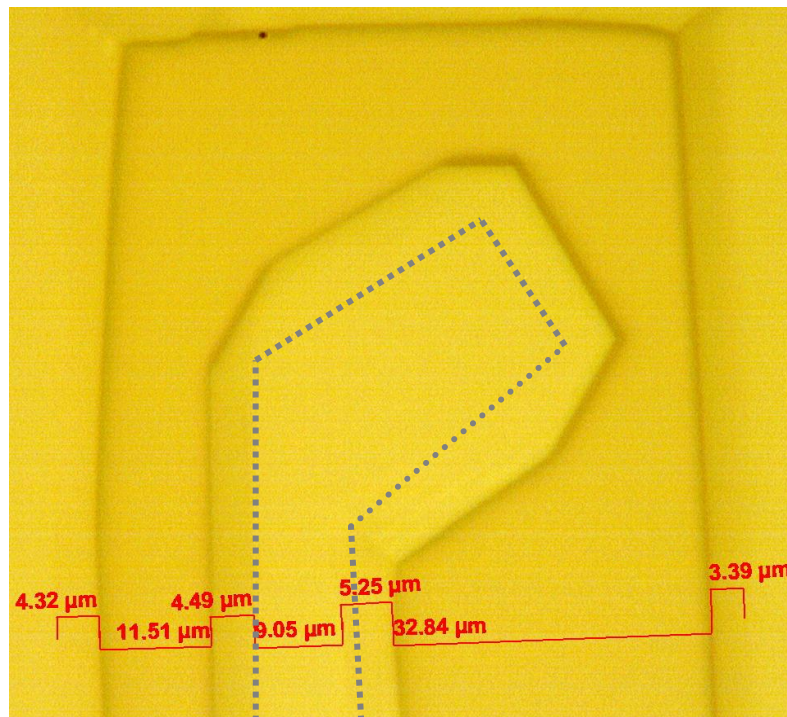
Once the wafer was patterned and laterally overgrown with GaN a wafer quadrant was analysed. This showed the ELOG growth on each sub-type of prototype device to be successful. The analysis was done using optical microscopy and scanning electron microscopy (SEM). The following figures shows optical images of typical ELOG cantilever designs with relevant dimensions.



(a)



(b)

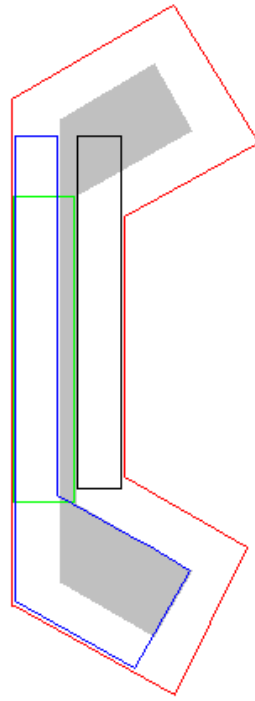


(c)

**Figure 6.15** Optical images of different ELOG cantilever designs at different magnifications. (a) 40x magnification of a typical strip cantilever design. (b) 10x magnification of a double-dogleg cantilever design. (c) 40x magnification of the same type of double-dogleg cantilever design with outline of original growth window in grey.

The images in figure 6.15 do show clear evidence of lateral overgrowth, the first step toward a viable device. Figure 6.15 shows some lateral overgrowth from the double

dogleg design, and devices can be released from this template in numerous different ways as shown in figure 6.16.



**Figure 6.16** Schematic of the double dogleg cantilever with ELO growth (red) and cut-outs of three possible cantilevers (red, green and black).

One of the dimensions, either the proposed length or width of a device, is limited by the amount of ELOG growth possible. This means that it is only possible to grow either short and wide or long and narrow cantilevers using ELOG. Long and narrow cantilevers are more suitable for as a sensor because they will achieve suitable levels of deflection. However, long and narrow cantilevers lack width potentially making it difficult to deposit sensors to the structure. Short and wide cantilevers do not suffer from the sensor deposition issue, but they will be much smaller than most other GaN cantilevers [4, 30, 31, 43, 44, 46] and the deflections will be small: this suggests that they will not be viable sensors.

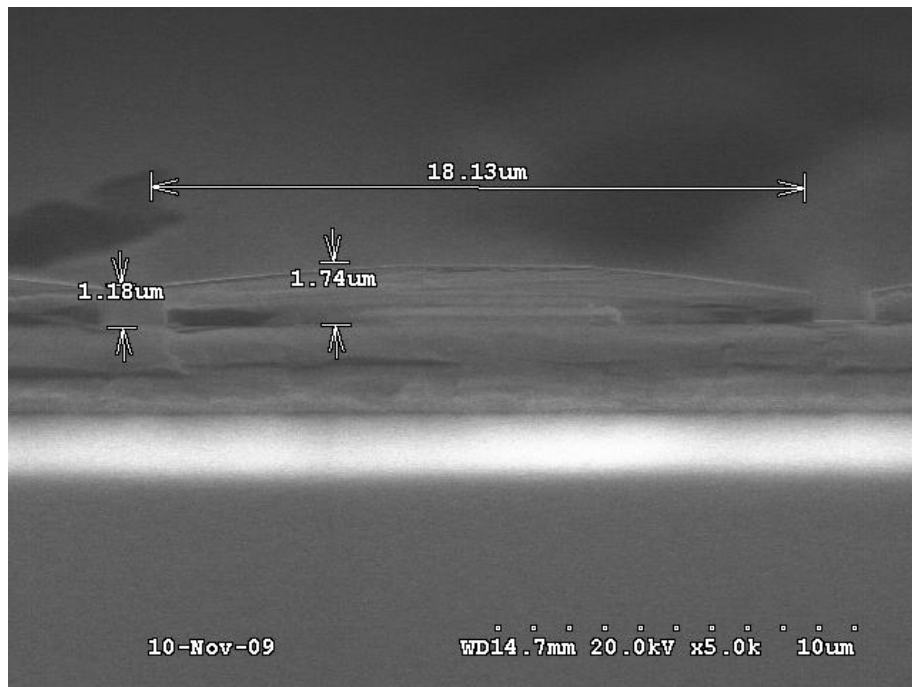


### 6.3.4 Issues with first mask and ELOG growth

**Table 6.3** Amount of lateral overgrowth on the various stripe ELOG structures  
(All dimensions in  $\mu\text{m}$ ) taken using an optical microscope.

<b>Stripe width</b>	<b>Pitch</b>	<b>Cantilever width</b>	<b>Wing width</b>	<b>Central bar height</b>	<b>Edge bar height</b>	<b>Minimum Aspect ratio</b>
5	15	15	5	1.5	1.02	3.33:1
5	20	17.925	6.36	1.74	1.18	3.66:1
5	25	18.805	6.805	2.01	1.62	3.39:1
5	30	18.46	6.655	2.37	2.01	2.81:1
9	27	22.27	6.635	2.01	1.14	3.30:1
9	36	22.8	6.9	2.29	1.98	3.01:1
9	45	22.81	6.905	2.67	2.52	2.59:1
9	54	23.06	7.03	3.16	2.85	2.22:1

Good ELOG GaN growth was achieved using the first mask; there was too little overgrowth for the fabrication of a sensing transducer. Although the size of the GaN growth window appears to be effectively unlimited, the amount of lateral overgrowth appears to be limited by the fill factor. This suggests that increasing the fill factor increases the amount of lateral overgrowth. Table 6.3 shows that the typical minimum aspect ratio between the width and thickness of the cantilever are between 2.2:1 and 3.4:1. If these aspect ratios are typical of ELOG growth, the final cantilevers are likely to be 20 – 30  $\mu\text{m}$  wide and 5.8 – 13.6  $\mu\text{m}$  thick. This makes it difficult to fabricate sensing contacts (HEMT, resistor, and capacitor) onto the ELOG structure.



**Figure 6.17** SEM image showing the faceting that can occur on ELOG growths.

Some ELOG cantilevers had significant faceting. Faceting is the downward tilt on the edge of the ELOG growth, shown in figure 6.17, and is undesirable when processing the ELOG structures. Faceting further limits the amount of ELOG cantilever material available for a sensor and therefore needs to be minimised. Analysis of the cantilevers showed that those fabricated with a large fill factor had much reduced faceting and were thicker. Growing thicker cantilevers should reduce this problem, caused by the preferred shape of growth at the wafer's orientation [174, 175].

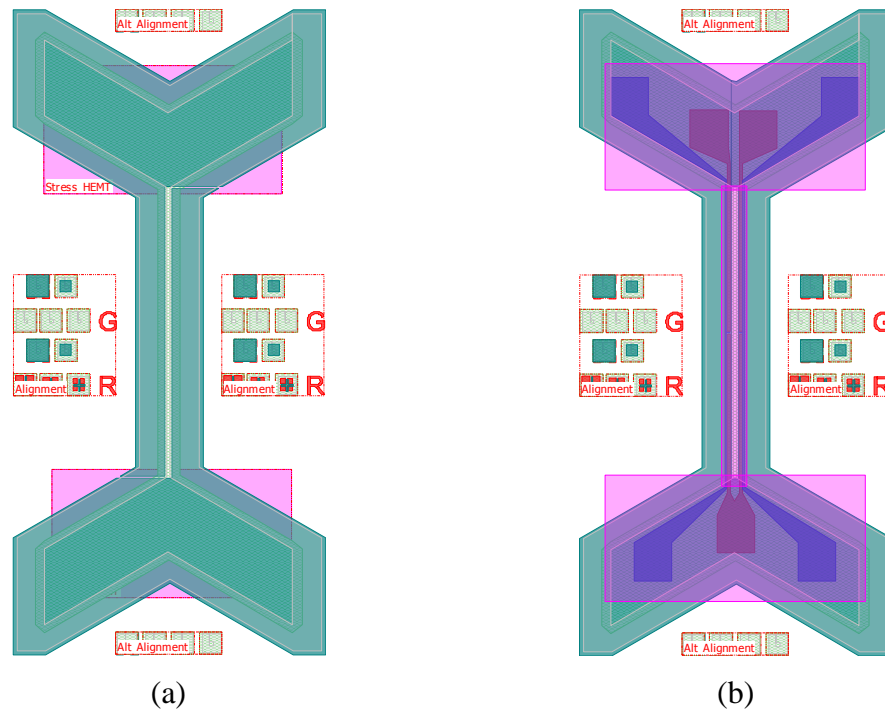
An ELOG cantilever is connected to the ELOG growth window or 'anchored' on 3 of the 6 edges of the device, as shown in figure 6.16, meaning that it will need to be released along two of the edges to produce a cantilever. An ELOG growth window is the area of the wafer through which the SiN<sub>x</sub> mask has been etched, leaving the GaN surface exposed. GaN can then be grown upwards and then laterally outwards from the exposed GaN surface, hence the definition 'growth window'. The anchor is part of the growth window that remains after etching, connecting the cantilever to the substrate. Therefore, as the amount of lateral overgrowth is small, the cantilevers need to be released with a 2 μm degree of accuracy. This problem is unavoidable with ELOG growth, but can be mitigated by increasing the amount of overgrowth. In conclusion this means that the amount of overgrowth required needs to be increased

to at least 20  $\mu\text{m}$ . In order to get at least 20  $\mu\text{m}$  of overgrowth, the growth conditions will need to be optimised.

The maximum length of a double-dogleg cantilever was 80  $\mu\text{m}$ . In addition, the anchors are only about 20  $\mu\text{m}^2$  and this is too small for a single contact pad. A contact pad needs to be at least 40  $\mu\text{m}^2$ , with three contact pads needed for a gated FET sensing element and two contact pads for a gateless FET. The pads have to be on the ELOG template because the metallic contacts are a few hundred nanometres thick and this means that their deposition is very sensitive to changes in height. Therefore the cantilever devices in the second mask set will need to be much longer and at least 100  $\mu\text{m}^2$  of space is required on each anchor.

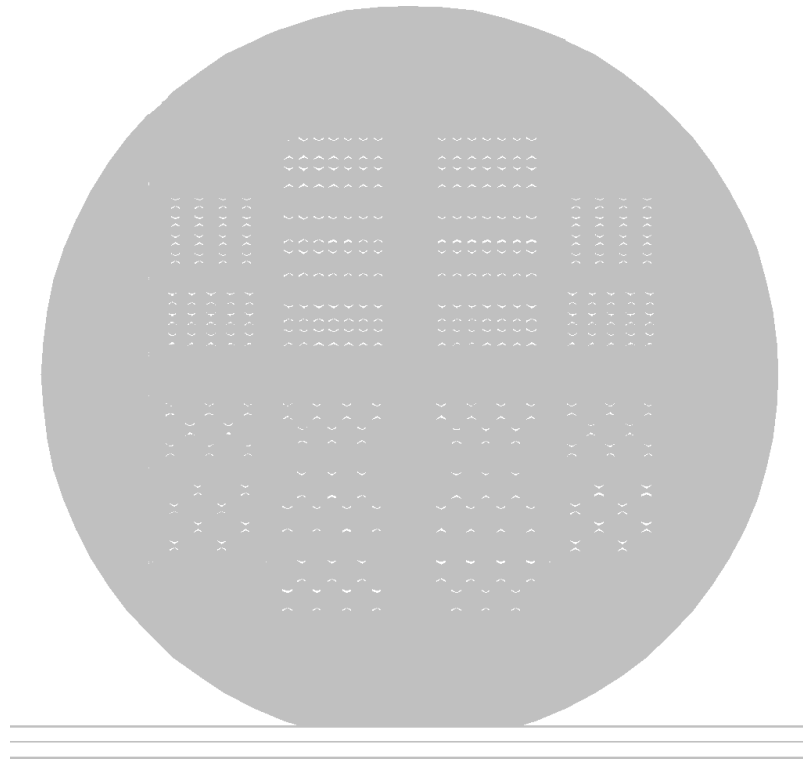
#### **6.4 Design of the second Mask Set**

Based on the first trials, a second mask set was designed. As the ELOG structures grown from the first mask were too small for any practical use, the mask required a significant redesign. The redesigned devices are loosely based on the double-dogleg design, but much larger in order to accommodate contact pads for the sensing elements and to allow more overgrowth of material. The regions on the top and bottom on each device are large enough to fit three 100  $\mu\text{m}^2$  contact pads. These regions will also act as anchors for the fabricated devices. Each device consists of a central bar that connects the two contact pad regions. There are five possible lengths for the central bar in the mask set, 120, 240, 480, 780 and 1080  $\mu\text{m}$ . The variation in central bar length is quite large because the optimal bar length was uncertain at the time the mask was designed and can only be determined experimentally. Additionally the device templates are symmetric, making it possible to fabricate two devices from a single template.



**Figure 6.18** Schematic images of (a) gateless dual cantilever and (b) gateless dual beam devices that can be fabricated using the second generation mask set.

It is possible to fabricate two different types of devices from the ELOG template, dual cantilevers and dual beams, as shown in figure 6.18. The dual cantilever arrangement consists of two single-clamped cantilever devices released and fabricated from the template, as demonstrated in figure 6.18 (a). The cantilevers are released by the removal of the central bar and cantilever beam edges by GaN etching, denoted by the gaps in the release mask in 6.15 (b). Each device has separate sources, gates and drains, explaining why there needs to be enough space on the anchor for three contact pads. However, figure 6.18 (a) shows a gateless device and this reduces the number of contact pads on each anchor to two. The dual beam device, shown in figure 6.18 (b), is a double clamped device with two released beams between the two chevrons. The concept behind the dual beam device is that it can be used as a sensing element on a larger sensor, because it will move as the substrate is deflected. In order to optimise the amount of space available, both beams share a common source reducing the number of contact pads required. The drain and gate (where applicable) contacts for each beam were kept separate. These devices were then arranged onto the mask set with the dual cantilever devices being fabricated from the left hand side of the wafer and the dual beam devices from the right hand side.

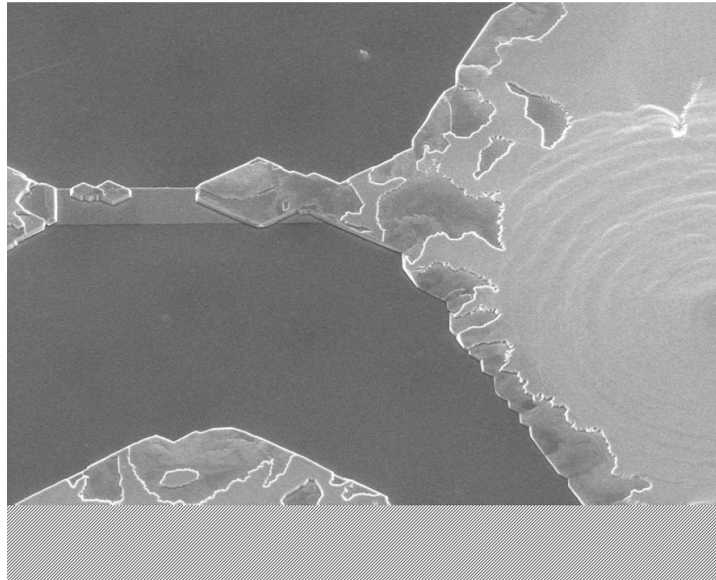


**Figure 6.19** First Layer of the second generation ELOG mask.

As figure 6.19 shows, the mask is dark with windows open for the devices and alignment marks. This mask is subject to the same lithography process described in sub-section 6.3.1 to facilitate ELOG growth. The lower half of the wafer in figure 6.19 has half the number of devices as the top half of the wafer. This was done in order to see if a further reduction in growth windows in the mask noticeably increased the fill factor, producing significant improvements in the amount of lateral overgrowth.

It was found that opening excessive numbers of growth windows limited the possible amount of lateral overgrowth because the ELOG mechanism is a gas diffusion effect [176]. During ELOG growth, the Ga and N pre-cursor gases of TMG (tri-methyl Gallium) and  $\text{NH}_3$  respectively travel along the mask until they find a gap in the mask, which is exposed GaN. The Ga and N atoms are deposited on the surface in a wurtzite arrangement, as in traditional GaN growth. Once the growth in the GaN growth window has reached the top of the mask, it starts to grow upwards and outwards, over the top of the mask. Therefore, in theory [176], minimising the

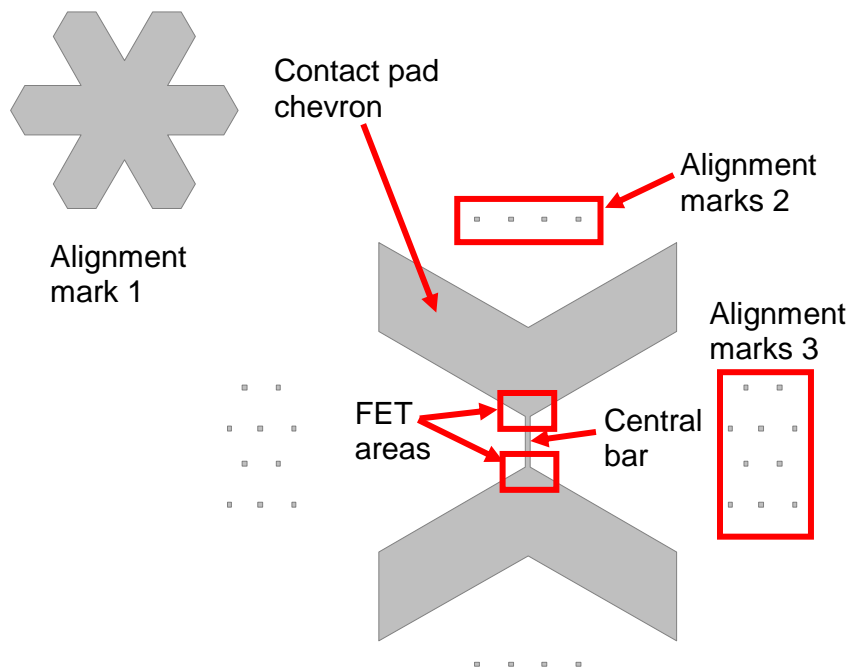
number of growth windows maximises the rate of overgrowth because all of the GaN material will diffuse towards the available growth windows.



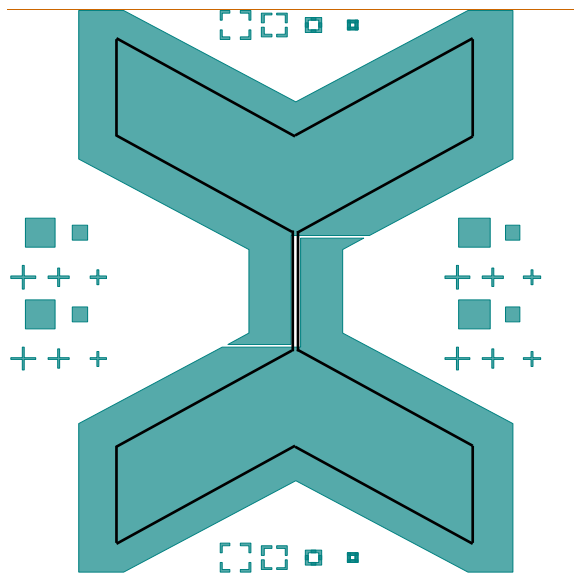
**Figure 6.20** Image of attempt at growing ELOG devices on a mask with a high number of growth windows.

In order to demonstrate this problem, an attempt was made to fabricate identical devices on a mask where the  $\text{SiN}_x$  mask was etched, apart from some trenches around the devices and alignment marks. As the mask was mostly clear, it was simpler to align. As figure 6.20 shows, the ELOG growth was patchy and erratic, with poor surface quality. This is caused by the large growth windows absorbing all of the material and this meant there was limited material left for the relatively small central bar. This result shows the importance of achieving a good mask design by controlling the growth windows.

### 6.4.1 ELOG device terminology



(a)



(b)

**Figure 6.21** Schematic diagram of the ELOG growth template with (a) definitions of the different regions and (b) second layer or ‘release’ mask.

Figure 6.21 (a) contains an image of the ELOG growth template designed for the second generation mask with alignment marks compatible with later mask layers.

Alignment marks are patterns that are added to mask layers in order to allow the perfect alignment between multiple mask layers. Since the amount of lateral overgrowth cannot be predetermined, three different types of alignment marks have been trialled. The first type of alignment mark shown in figure 6.21 (a) has six-fold symmetry and aligned along the slow growth plane, meaning that it should retain its shape during lateral overgrowth and can be used to align the release mask to the ELOG growth template. The second set of alignment marks consist of four  $5 \mu\text{m}^2$  squares above and below each ELOG template. These alignment marks will laterally overgrow, meaning that different sized square boxes had been drawn outside them on the release mask, shown in figure 6.21 (b). Finally, there is a third set of alignment marks on the left and right hand sides of each ELOG growth template. The third set of alignment marks have been designed for the deposition of the Ohmic and Schottky contacts for the FET sensing elements required for a future device.

The different regions of the ELOG growth or sensing template have also been marked on figure 6.21 (a). The contact pad chevrons on the top and bottom of the template have a dual purpose, to house the contact pads for the sensing elements and to act as the anchor point for the cantilevers/beams, connecting them to the substrate. The contact pads are a  $40$  to  $100 \mu\text{m}^2$  metallic region from which a gold wire can be bonded onto the sensing template, allowing the external transport of the electrical signal from the sensing elements. The sensing template anchor has been designed with enough space for the deposition of three  $100 \mu\text{m}^2$  contact pads. The FET regions, marked by the two boxes on the template are where the ELOG cantilever will be most strain sensitive. A gated or gateless FET will be placed in this region and ohmic and Schottky wires will be deposited between the FET and the contact pads. The central bar, which runs between the two contact pad chevrons, will be etched through during the release process as shown in figure 6.21. Therefore, the peak height of the central bar will determine the etch time required to release an ELOG device. The terminology referred to in this section will be used in the rest of this chapter.



#### ***6.4.2 Second generation ELOG mask methodology***

Three GaN/Sapphire and three silicon wafers were patterned using the second generation mask and lithography process described in section 6.3.1. The silicon wafers were used for growth optimisation and experimentation. It has been found experimentally on the previous generation of ELOG growths that a small misalignment can cause faceting problems, with slow growth planes interfering with the ELOG epitaxy (see figure 6.15 (b) and (c)). All of the GaN/sapphire wafers were aligned such that the wafer flat was in perfect alignment with the mask, achieved using the straight lines drawn at the bottom of the mask shown in figure 6.19. As GaN has a hexagonal crystal structure, its fast growth planes are  $60^\circ$  apart and one of which is parallel in direction to the main flat when grown on (0001) sapphire [178], meaning it is beneficial to align the wafers in this fashion.

A 45 nm  $\text{SiN}_x$  mask was deposited on the GaN/sapphire wafer by PECVD. A thicker 90 nm  $\text{SiN}_x$  mask was deposited on the Si wafers to account for the deposition of a thin AlN nucleation layer. After wafer patterning, each wafer was divided into quarters in order to maximise the opportunity of obtaining good ELOG growth. Before growth, each quarter wafer sample was pre-treated for 90 seconds in 5:1 water: HCl solution to remove oxidants from the surface of the sample. Each sample was then placed in the MOCVD growth reactor for ELOG epitaxy. Two types of ELOG epitaxy were attempted on the samples: traditional ELOG and a mixture of pulsed ELOG, also known as PLOG, and traditional ELOG. In PLOG, the precursor gases tri-methyl Gallium (TMG) and ammonia enter the growth reactor in pulses rather than continuously [179, 180]. Pulsed growth is used for producing nanowires as it produces highly quality, low defect nanostructured material [179, 180]. Both methods were attempted in this work in order to offer a comparison between the two techniques and determine what method is best for fabricating ELOG sensors.

## 6.5 Results from second generation ELOG templates

The ELOG growth on the samples was done by the MOVPE growth specialist within the department and MORGaN project. He determined the optimal growth conditions for producing ELOG sensors and grew templates that were analysed using various imaging and topographical techniques. These techniques were optical and SEM imaging and topographical scans using both the Proscan 2000 chromatic and Dektak profilometers. These results were used to determine the suitability and difficulty of fabricating a sensor from these samples. Table 6.4 contains details of the GaN/sapphire ELOG samples analysed in this section.

**Table 6.4** Details of the GaN/sapphire ELOG samples analysed and later used in release trials

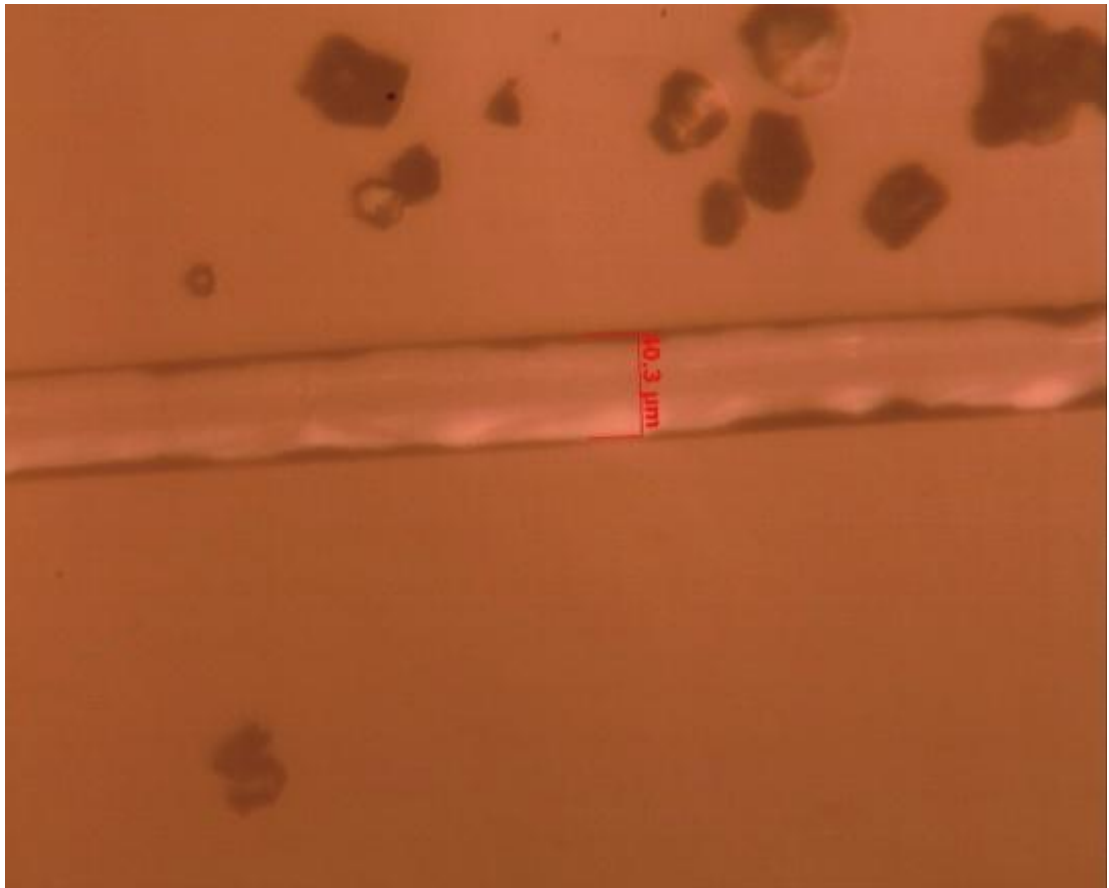
<b>Sample Number</b>	<b>Growth Method</b>
2226	Normal ELOG
2828	Normal ELOG
2846	Normal ELOG
2847	Normal ELOG
2848	Normal ELOG
2849	Mixture of pulsed ELOG and normal ELOG

### 6.5.1 Optical Imaging

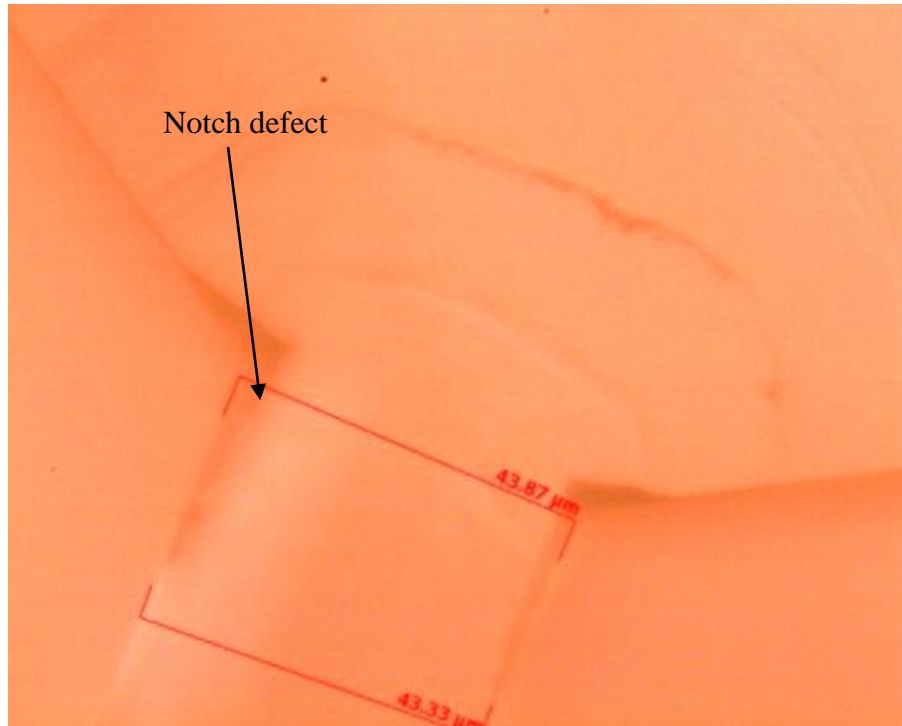
#### 6.5.1.1 Sample 2828 (From first layer of the second generation mask set)

Sample 2828 consists of GaN ELOG growth on a GaN/sapphire template wafer. Figure 6.22 (a) and (b) show that the amount of lateral overgrowth is good, with the central bar width increasing from 10 to 40 – 44  $\mu\text{m}$ : this equates to 15 to 17  $\mu\text{m}$  of lateral overgrowth on each wing. Therefore the amount of overgrowth is sufficient for releasing cantilevers/beams and there is possibly enough material to also deposit metallic contacts. Additionally, the alignment mark in figure 6.22 (c) has held its shape after lateral overgrowth and this means that aligning the sample to the release mask will be possible.

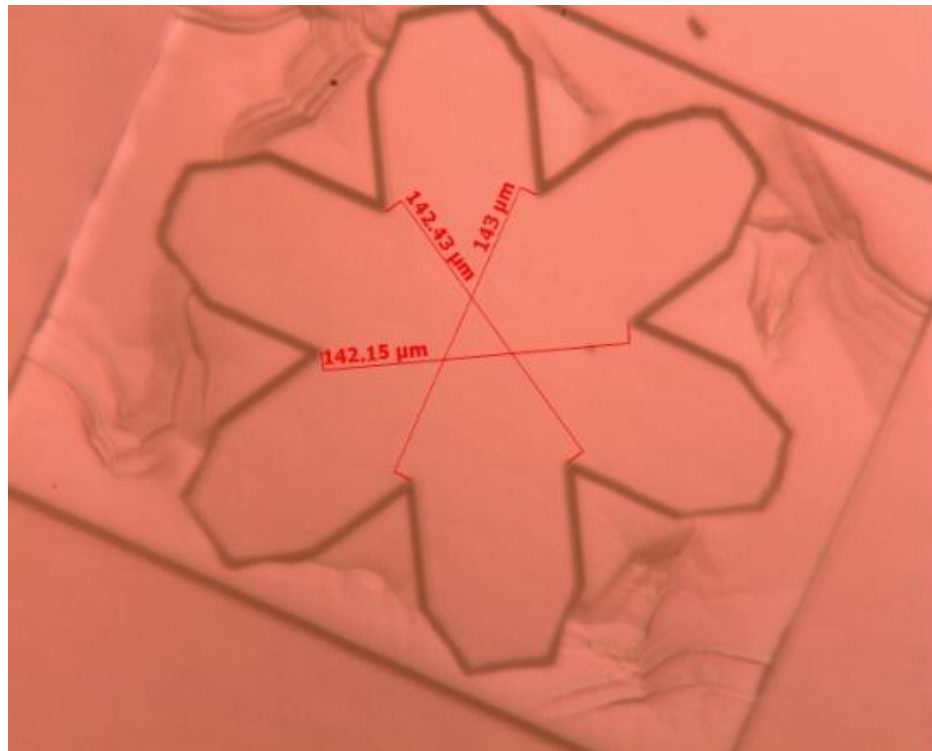
However, figure 6.22 (a) shows parasitic growths on top of the SiN<sub>x</sub> mask and these are a potential processing issue because the parasitic growths could potentially be higher than the ELOG templates. This reduces the resolution of the release mask because it will be further away from the ELOG templates. Additionally there are ‘notch’ defects at the point where the central bar meets the contact pad chevron, as shown in figure 6.22 (b), appearing to slightly reduce the amount of available material in the most strain-sensitive region on a dual cantilever device and where the sensing element will be placed. A notch defect is defined as the small indent that occurs where the central bar meets the contact pad chevron. Finally figure 6.22 (c) shows creases on the contact pad chevron, suggesting that presence of atomic steps and uneven topography.



(a)



(b)

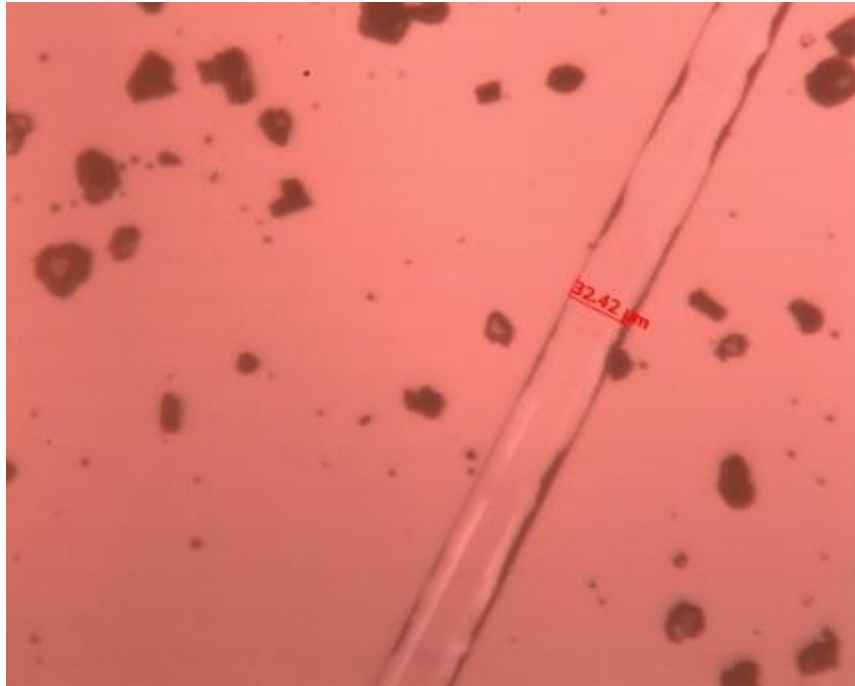


(c)

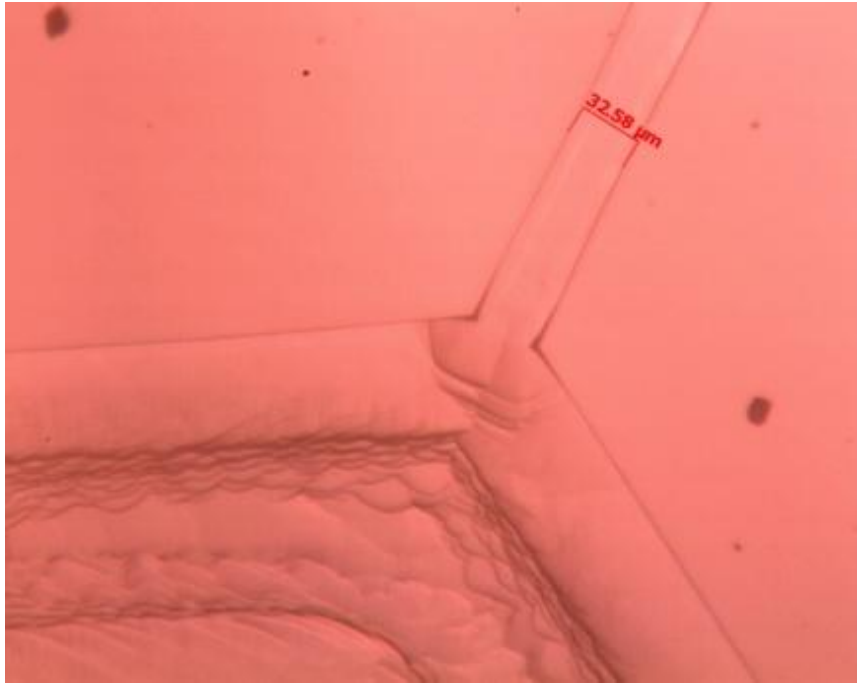
**Figure 6.22** Optical images from sample 2828. (a) Central bar, showing parasitic growths on top of the mask. (b) Image of where central bar meets contact pad chevron, showing notch defect. (c) Image of ELOG alignment mark.

6.5.1.2 GaN/sapphire samples numbers 2226, 2846, 2847 and 2848

Other GaN/sapphire ELOG samples were imaged optically and they all show similar surfaces, but with varying amounts of lateral overgrowth. All of these samples were grown by traditional ELOG growth methods, rather than additionally using pulsing. Figure 6.23 shows various optical images GaN/sapphire samples.



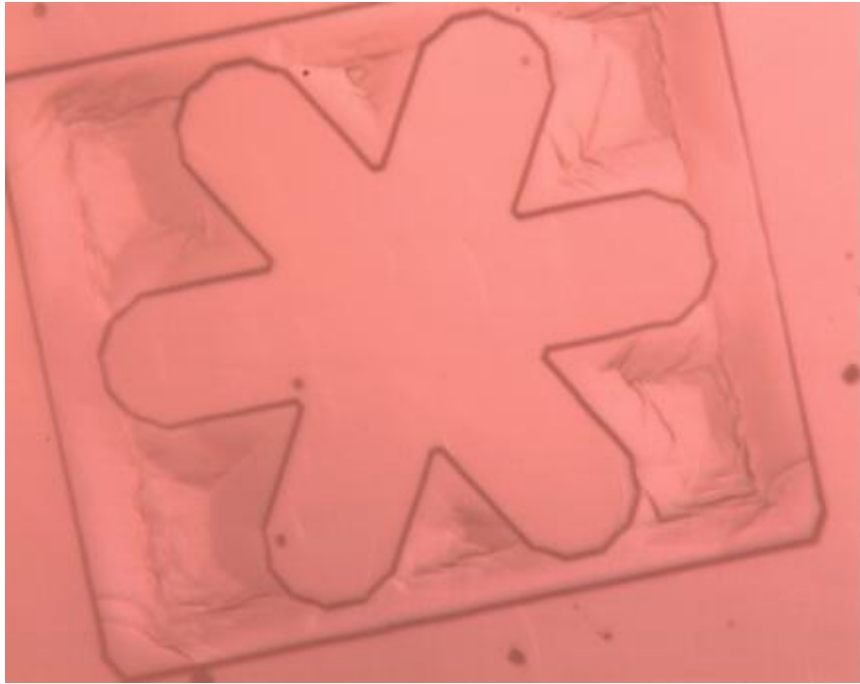
(a)



(b)



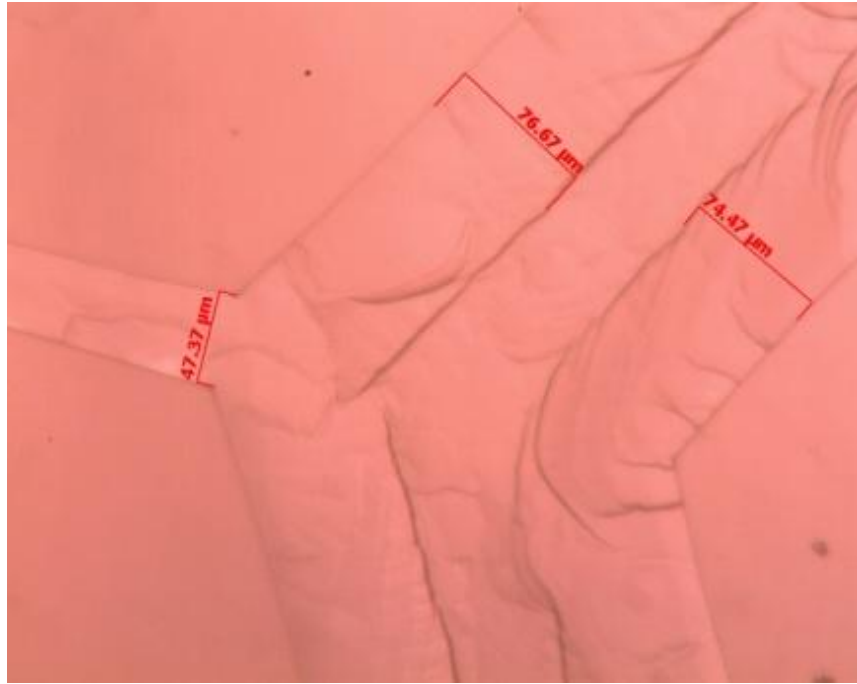
(c)



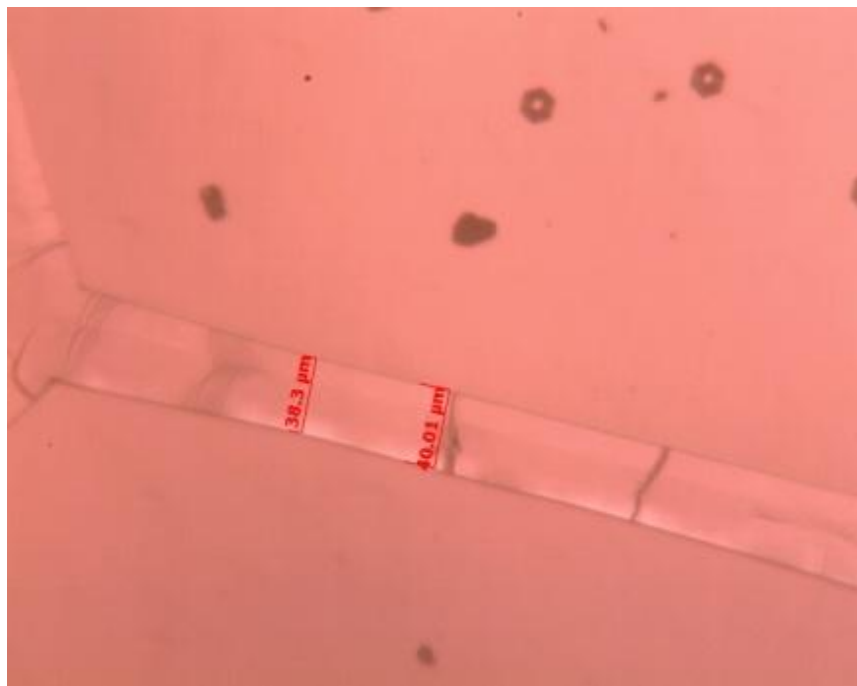
(d)



(e)



(f)



(g)

**Figure 6.23** Optical images of GaN/sapphire ELOG samples. (a-b) Sample 2226 (c-d) Sample 2846 (e) Sample 2847 (f-g) Sample 2848.

The main point of note is that it has been possible to achieve approximately 25 μm of lateral wing growth, as shown in figures 6.19 (c) and (f), which exceeds the target of

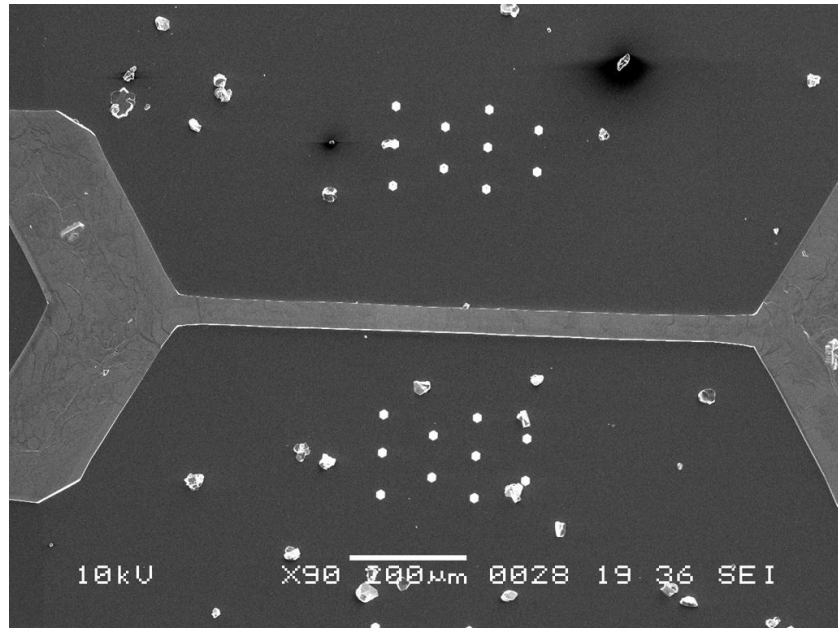


20  $\mu\text{m}$  overgrowth for a sensor. Therefore these results indicate that it is possible to grow ELOG templates that are wide enough for sensing applications. However, the surface quality appears to be poor on some of the samples and there is further evidence of large amounts of topographic variation. These results show that the initial findings on sample 2828 are typical, meaning that all these samples will require topographical analysis.

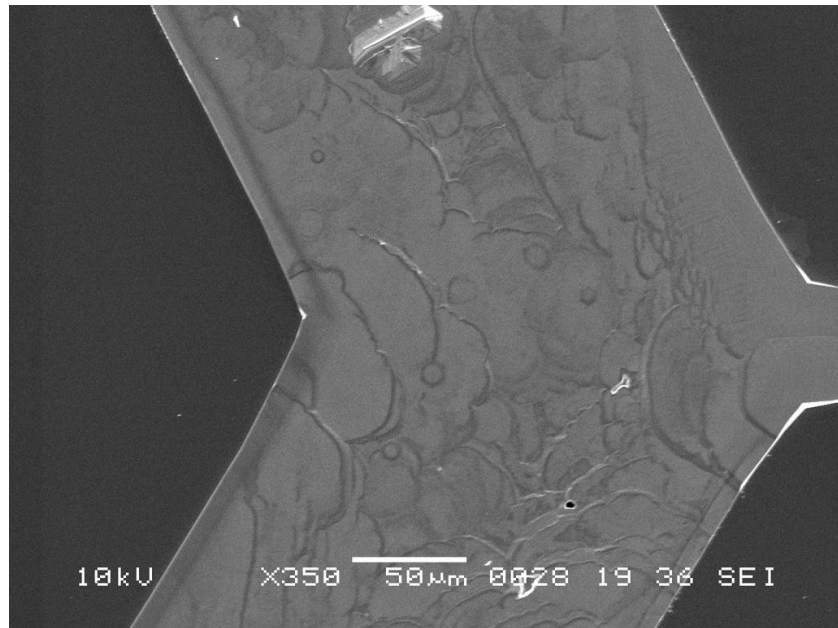
### ***6.5.2 SEM Imaging***

In addition to the optical images, higher resolution SEM images were taken of samples in order to investigate surface quality, faceting and other growth issues. The SEM also has a limited tilt function that can be used to do some analysis on the edge of the cantilever/beam of a template, as shown in section 6.6. Some typical SEM images of various GaN/sapphire ELOG samples are shown in figure 6.24.

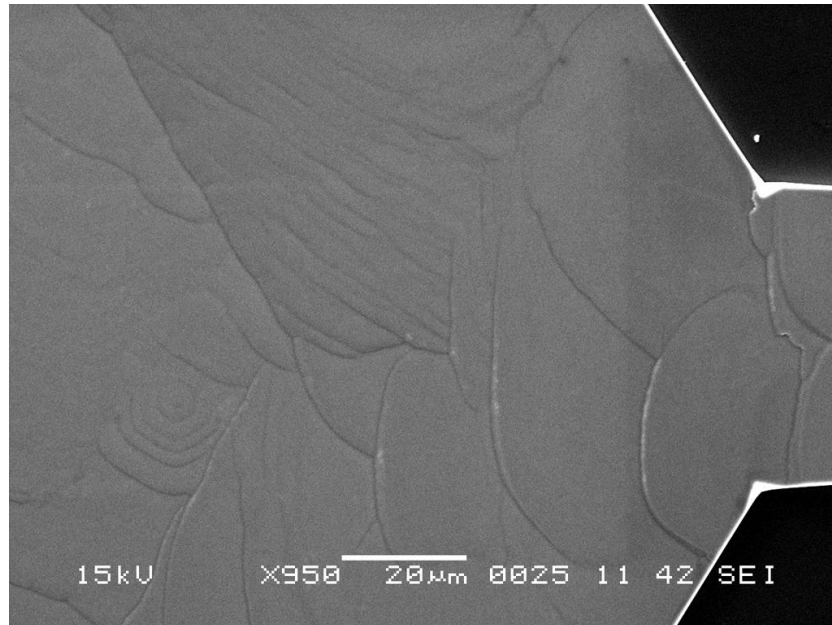
The SEM images in figure 6.24 contain SEM images taken of samples 2846 and 2847. Figure 6.24 (b-d) shows the ELOG template surfaces have a large number of atomic steps on both the central bar and contact pads, suggesting a very uneven surface. These images suggest that ELOG templates have a very uneven topography. Additionally, figure 6.24 (d) appears to show a parasitic growth on the central bar and this means that a thicker layer of resist will be needed to process the sample. All of the evidence from the SEM images agrees with the main conclusion of the optical microscopy, all the samples will need their surface topography scanned before processing.



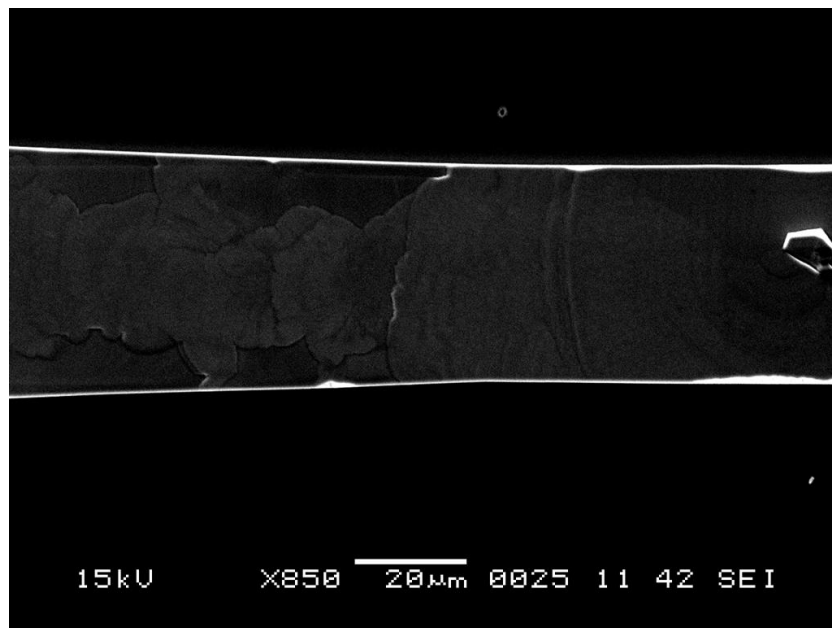
(a)



(b)



(c)



(d)

**Figure 6.24** SEM images of various GaN/sapphire ELOG samples. (a-b) Sample 2846, (c-d) sample 2847.

The SEM images in figure 6.24 contain SEM images taken of samples 2846 and 2847. Figure 6.24 (b-d) shows the ELOG template surfaces have a large number of atomic steps on both the central bar and contact pads, suggesting a very uneven surface. These images suggest that ELOG templates have a very uneven topography. Additionally, figure 6.24 (d) appears to show a parasitic growth on the central bar and this means that a thicker layer of resist will be needed to process the sample. All of the evidence from the SEM images means that all the samples will need their surface topography scanned before processing.

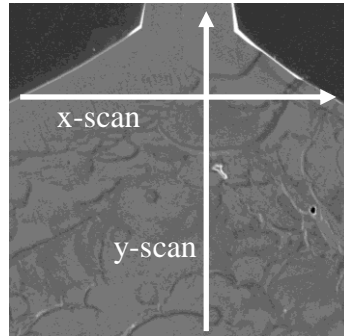
### ***6.5.3 Proscan 2000 and Dektak Measurements***

The optical and SEM images show that some of the samples exceeded the lateral overgrowth target of 20  $\mu\text{m}$ , but the images seem to suggest that the surface topography is uneven. It is very important to know the height and topography of each sample because the GaN etch time and resist thickness needs to be determined on a sample by sample basis. Furthermore, the height of the parasitic growths is unknown, and if they are higher than the template, they become an additional processing issue.

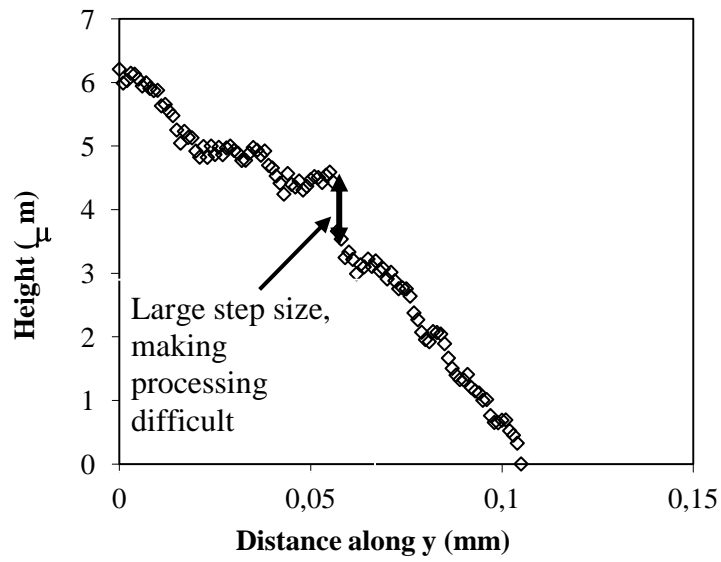
Firstly, sample 2828 was scanned using the chromatic sensor on the Proscan 2000 profilometer. Figure 6.25 shows an SEM image and topographical scans taken of a template in the area where a FET sensing element will be deposited. The surface in the FET region needs to as smooth as possible, because metallic Ohmic and Schottky contacts need be deposited onto the surface with 2  $\mu\text{m}$  precision in a limited amount of space.

The results in figure 6.25 show significant variations in surface topography on a device template on sample 2828, complicating processing. The height increases by 0.9  $\mu\text{m}$  over 1  $\mu\text{m}$  in the FET region where the sensing elements will be deposited. However, as the surface is fairly smooth, an attempt will be made to deposit a layer of Ti/Ni metals onto the surface for GaN etching. An additional issue is that the device is in excess of 10  $\mu\text{m}$  in height, meaning that it will take a long time to plasma etch

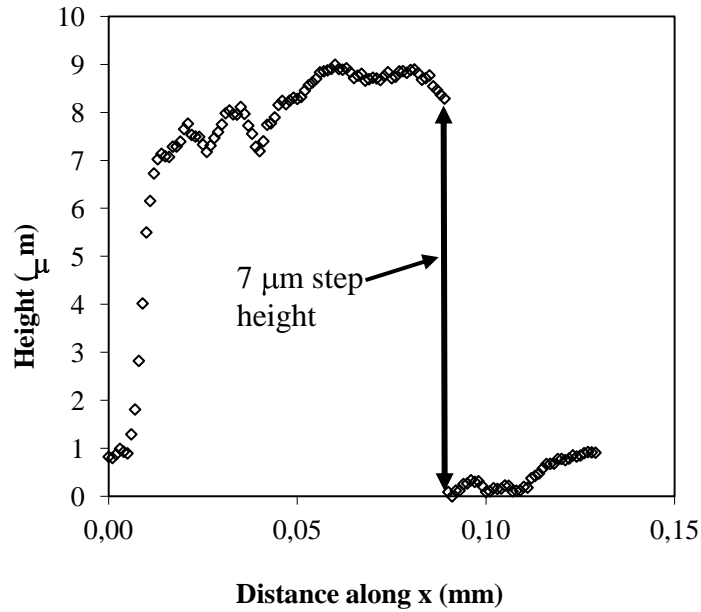
through the central beam. As all of the GaN/sapphire samples appear to be similar, it is important to measure the topography of every sample.



(a)



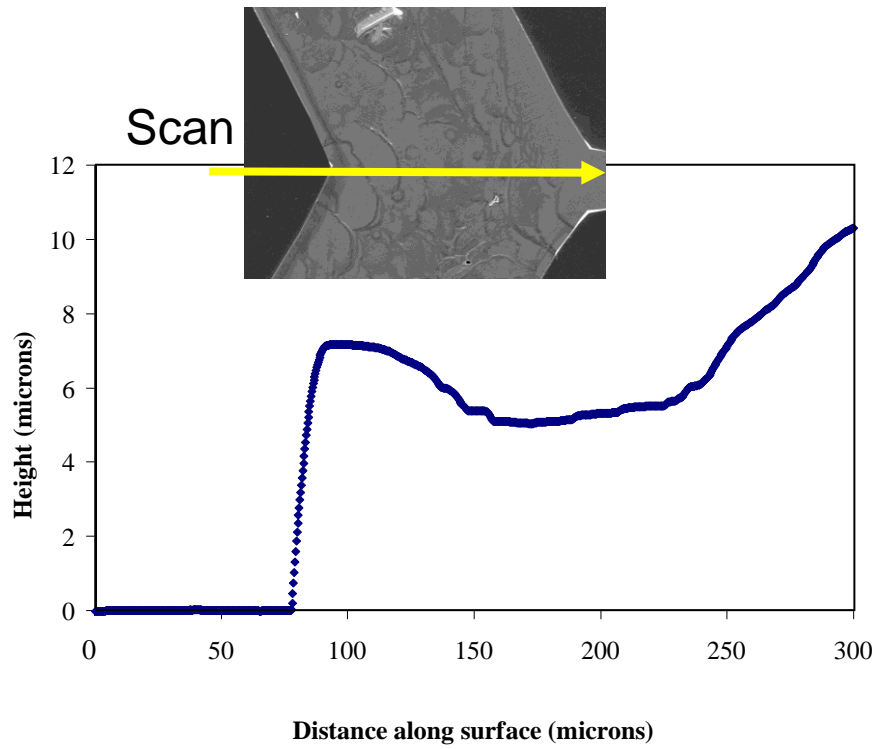
(b)



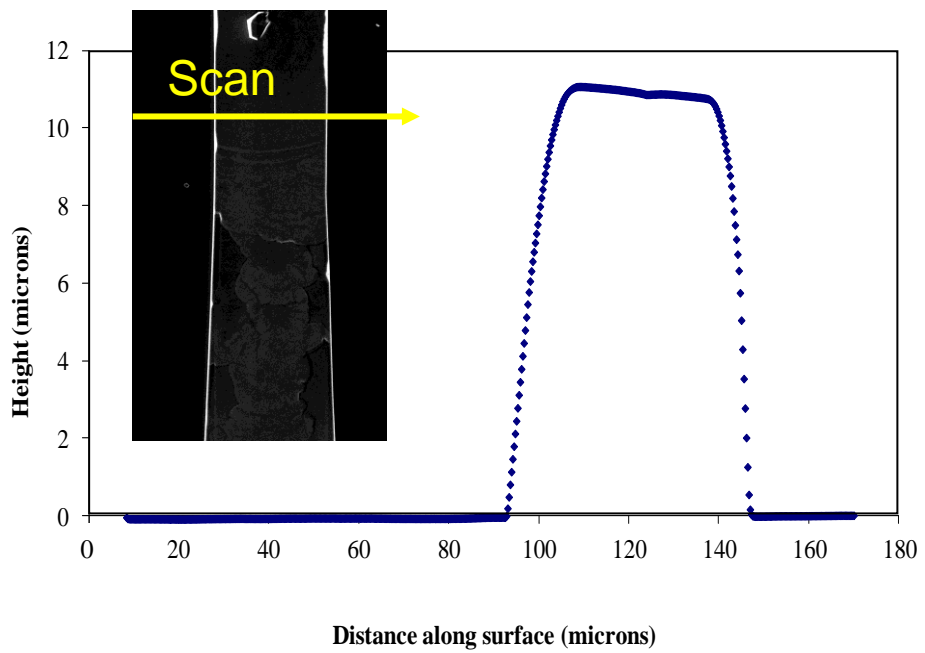
(c)

**Figure 6.25** Scan of an ELOG template on sample 2828 taken using the Proscan 2000 profilometer. (a) Schematic diagram showing the position of the highlighted line scans. (b) Plot of line scan taken along the y-direction. (c) Plot of line scan along the x-direction.

The Dektak scans in figure 6.26 confirm the topographical measurements using the Proscan 2000 chromatic scan. The topography of all the samples was measured using the Dektak and a scan of sample 2848 is shown in figure 6.27. This scan shows that the uneven topography follows a characteristic curve. The characteristic curve shows that the surface at the bottom edge of the contact pad chevron starts reasonably high and then decreases towards the centre of the contact pad. The surface height then increases as the probe travels towards the central bar, reaching its maximum in the middle of the bar.

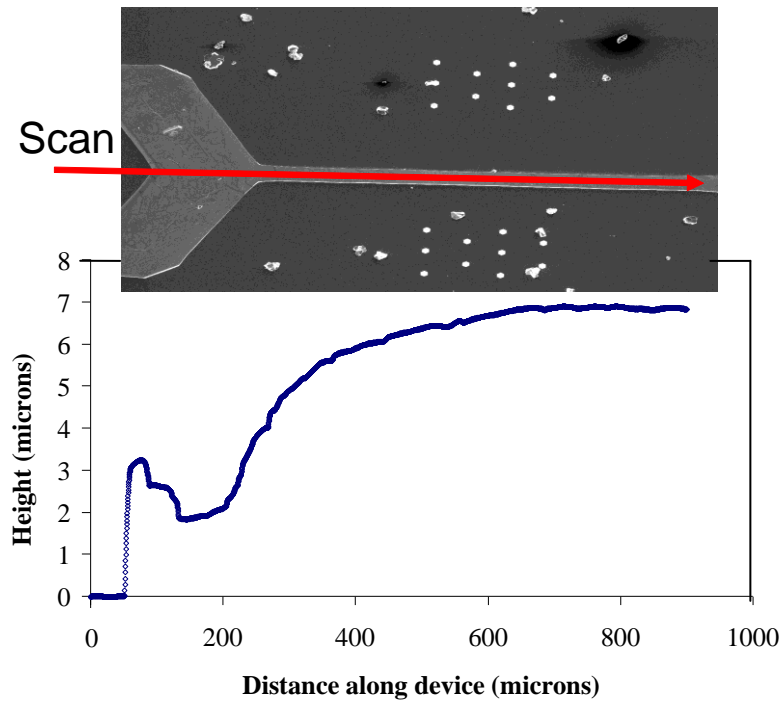


(a)



(b)

**Figure 6.26** Dektak scans of sample 2828. (a) Scan of contact pad chevron. (b) Scan of central bar.



**Figure 6.27** Dektak scan of Sample 2848.

However, despite the topographical issues, some of the samples achieve the combination of reasonable overgrowth and a sensible maximum bar height (see table 6.5). Sample 2847 has the least amount of topographical variation, a maximum template height of 3 mm and 10  $\mu\text{m}$  of lateral overgrowth. Sample 2848 also shows a reasonable balance between maximum height and lateral overgrowth.

#### **6.5.4 Results from mixed ELOG/Pulsed ELOG (PLOG) growths**

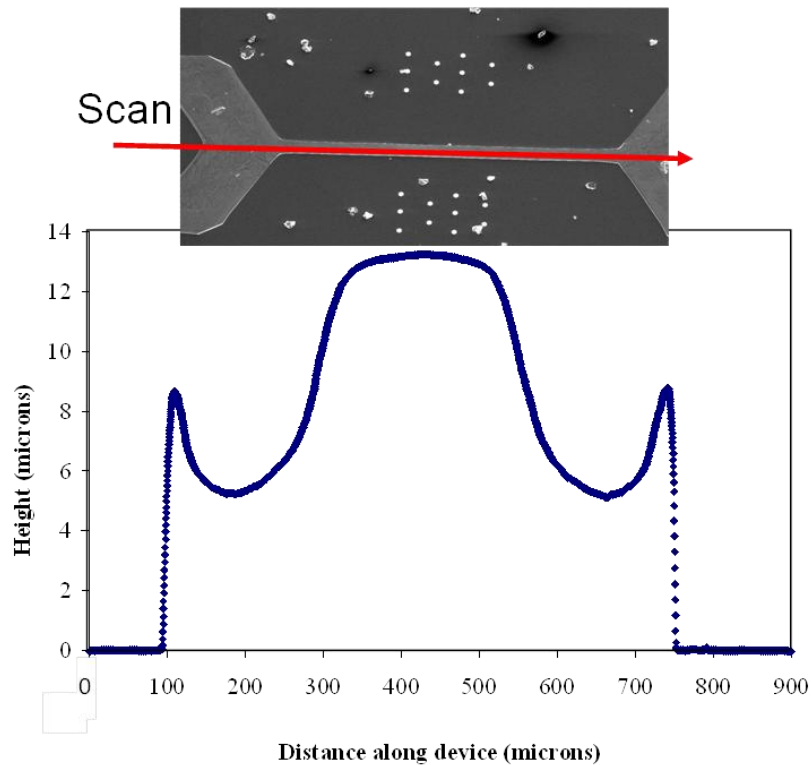
One of the GaN/sapphire samples was subjected to a mixed ELOG/PLOG growth process, and this sub-section will report on the results produced from this method. The mixed growth method is when the growth reactor is alternated between the reagent gases (TMG and ammonia) entering the chamber continuously and the gases entering the chamber in pulses. The motivation of using the mixed growth method was to see if it improved the material quality and reduced topographical variation.



Figure 6.28 shows an optical image and dektak scan of sample 2849, produced using the mixed growth method, and highlights the difference between using the normal and mixed growth methods. The mixed growth method produces higher ELOG templates and less lateral overgrowth with faceting, as shown in figure 6.26. The faceting, coupled with very little overgrowth, means that releasing a cantilever from sample 2849 will be difficult. Additionally, figure 6.28 (a) shows pit formation on the template surface and pits appear to be particularly dense in the proposed electrode region for the cantilever device. The surface of the template does appear to be far smoother than the surface on the traditionally-grown devices. A smooth surface means that the deposition of metals on the template will be more reliable and means that a thinner layer can be used. Therefore, based on the evidence found from the current collection of ELOG samples, both methods have their merits and further investigation is required.



(a)



(b)

**Figure 6.28** (a) Optical image of mixed ELOG/PLOG growth on GaN/sapphire sample 2849 and (b) a dektak scan of sample 2849.

### 6.5.5 Discussion of second generation ELOG analysis

All of the key topographical and lateral overgrowth dimensions have been collated in table 6.5. The key points to note is that samples 2828, 2846 and 2848 have lateral overgrowth of 15  $\mu\text{m}$  or greater, which is theoretically enough to fit a HEMT-style sensing element on a dual cantilever. All of the samples have enough lateral overgrowth to attempt release as the central bar on the release mask is 18  $\mu\text{m}$ . The central bar on the release mask is slightly wider than the ELOG growth window to ensure that the device will be released in the event of a small misalignment or poor resolution.

All samples show significant topographical variation, with samples 2828 and 2849 showing the most variation. These samples are also the highest, so will take the longest to GaN etch. For these reasons, they will also need a thick layer of nickel to

protect the cantilevers/beams from the GaN etch. The nickel deposition on 2828 will be additionally problematic due to wing faceting. However, despite these potential issues, it may be possible to release cantilevers from all of the samples.

**Table 6.5** Key measurements of GaN/sapphire ELOG samples (dimensions in  $\mu\text{m}$ )

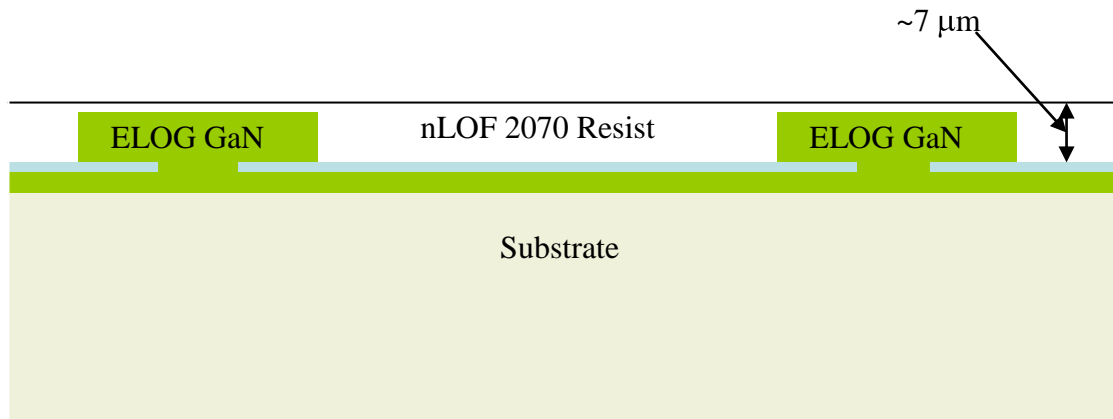
<b>Sample</b>	<b>Bar width</b>	<b>Growth method</b>	<b>Amount of ELOG growth</b>	<b>Max central bar height</b>	<b>Min contact pad height</b>	<b>Edge contact pad height</b>
2828	44	ELOG	17	12	6	8
2846	50	ELOG	20	5.5	2	3.67
2847	28	ELOG	7	2.8	1.5	2.7
2848	40	ELOG	15	7	2	3.5
2849	34	mixed	12	13	6	8.5

The rest of this chapter and part of chapter 8 will describe the approach taken in order to release good quality MEMS templates that demonstrate the viability of using ELOG technologies for GaN strain sensors. These approaches are:

- Attempting release of the current generation of ELOG templates. If release is successful, these templates can have metallic contacts deposited and be tested in the future to determine any strain sensitivity.
- Design new masks, using knowledge obtained from the current generation of templates, which have minimal topographical variation. The redesign will also attempt to deal with the notch defects that reduce lateral overgrowth in a critical area. The sensing elements and contact pads also require a redesign to reflect the lack of space on the new contact pads. New ELOG templates will be patterned and grown using the same methods; these templates will be then be characterised. This work is proposed for the future and will therefore be described in chapter 8 (sub-section 8.2.1).

## 6.6 Proposed method for releasing ELOG MEMS structures from their template

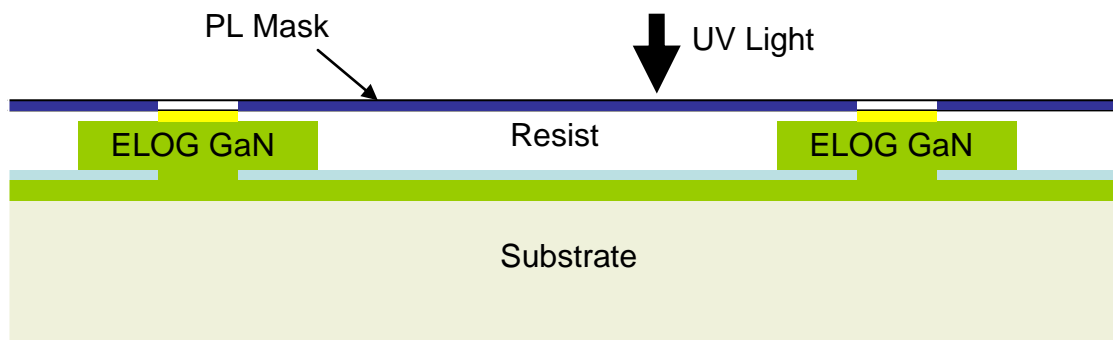
1. Deposit layer of nlof 2070 resist onto the sample



**Figure 6.29** Sample with ELOG sensor templates grown by MOCVD, with a thick layer of nlof 2070 resist deposited.

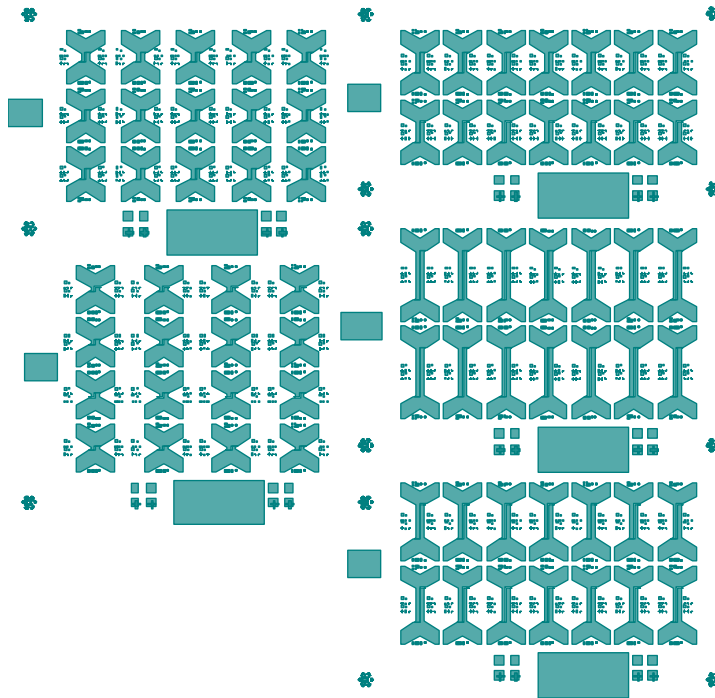
Firstly a thick layer of nlof 2070 resist is deposited onto the sample and this layer needs to be thick enough to ensure that the entire sample is coated. Nlof 2070 is a negative working resist, which means that the UV exposed parts remain after development. This causes an additional problem of a thick edge bead resulting from the spin coating. The edge bead from negative working resists is usually removed carefully using a razor and macroscopic lens.

2. Place release mask onto the structure and expose to UV light

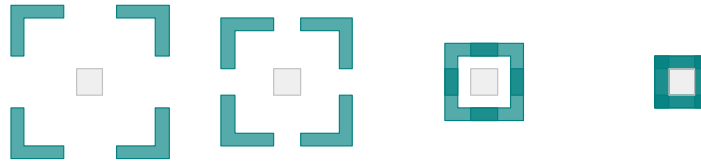


**Figure 6.30** Sample with release mask aligned to pattern during UV exposure.

Once the edge bead has been removed, the resist can be patterned using photolithography, as shown in figure 6.30. The second stage photolithography mask, known as the release mask, is used for this process. This mask, shown in figure 6.31, is used to allow selective etching of GaN until the ELOG devices are successfully released from their templates. The main issue at this stage is that the sample requires precise alignment with the sample in order to successfully release a cantilever or a beam, meaning that good alignment marks are required. Figure 6.31 shows the box alignment mark designed to align the sample to the mask. The box alignment marks (alignment mark 2 in figure 6.21) have been specifically designed to surround four  $5\ \mu\text{m}^2$  squares on the top and bottom of the ELOG template and are also shown in figure 6.21. The squares are holes deliberately placed in the first mask to allow the simple alignment of the sample. The four box outlines are all different sizes because the degree of lateral overgrowth from the holes was unknown.



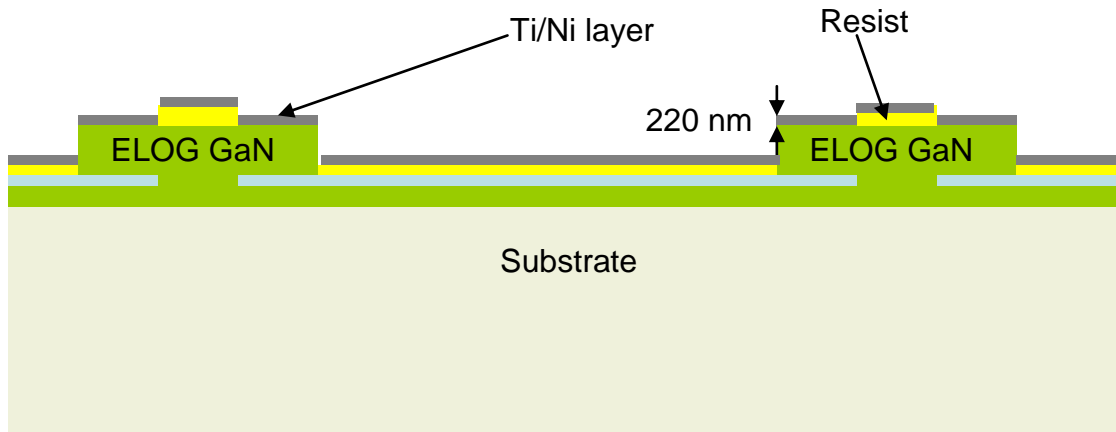
(a)



(b)

**Figure 6.31** (a) Second stage mask used to pattern wafer before the release of ELOG devices. (b) Chevron alignment mark used to precisely align ELOG sample with the mask.

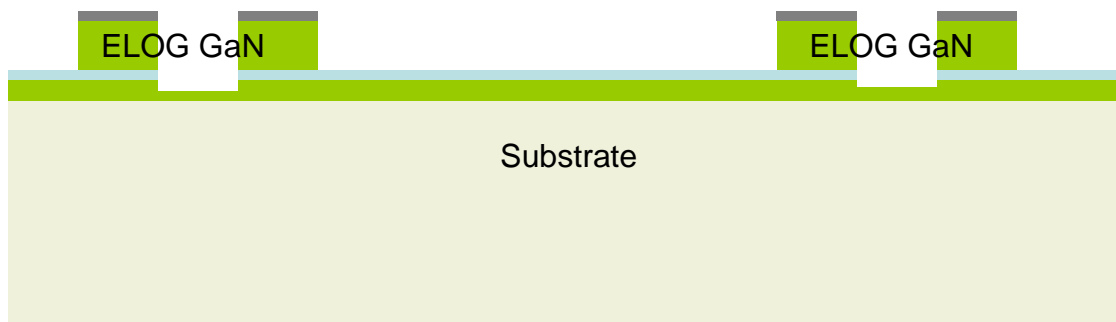
3. *Remove unexposed resist and deposit Ti/Ni*



**Figure 6.32** Sample after resist development and Ti/Ni deposition.

After the resist was exposed to UV light, the sample is post exposure baked (PEB) for 1 minute at 110°C. The sample is then placed into a solution of nlof resist developer, which removes the unexposed resist from the sample. Following the development of mask pattern and an O<sub>2</sub> plasma etch, a ~20 nm layer of Ti followed by a ~200 nm layer of Ni is deposited onto the sample by electron beam evaporation. The exposed resist is then stripped from the sample by lift-off using Microposit 1165 NMP remover, leaving a patterned layer of Ni protecting the devices from being GaN etched. Figure 6.34 (a) shows an optical image of sample 2846 after the successful deposition of the Ti/Ni mask.

4. *GaN etch the ELOG template*



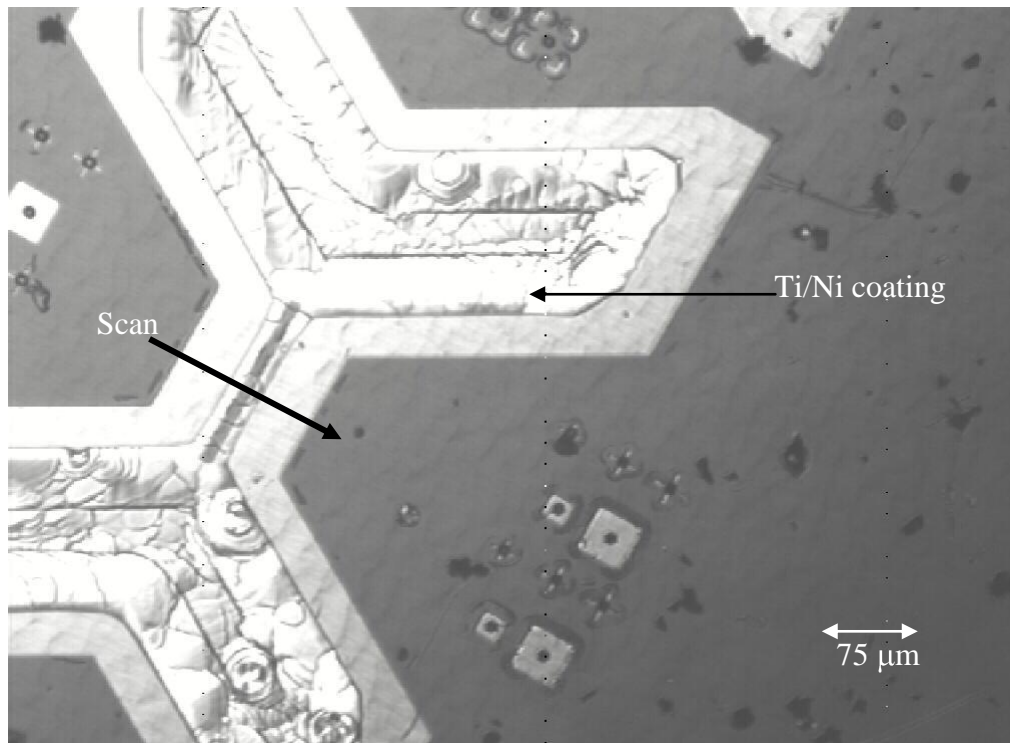
**Figure 6.33** Sample showing released GaN devices after GaN etching.

The sample is then placed in the ICP etcher for an Ar/Cl etch of the GaN. This will remove the central bar leaving two MEMS devices side by side. Excessive GaN etching can remove the Ni mask and remove the top GaN surface, as shown in figure 6.35, so timing the etch is important if the Ohmic and Schottky contacts required for a sensor are to be deposited afterwards. There are two options for the following steps, option 1 is to remove the SiN<sub>x</sub> mask using a buffered oxide etch and option two is to deposit the Ohmic and Schottky contacts using a similar process to steps 1 to 3. As the samples shown in the next section were the first to be released, option 1 was taken to confirm the release.

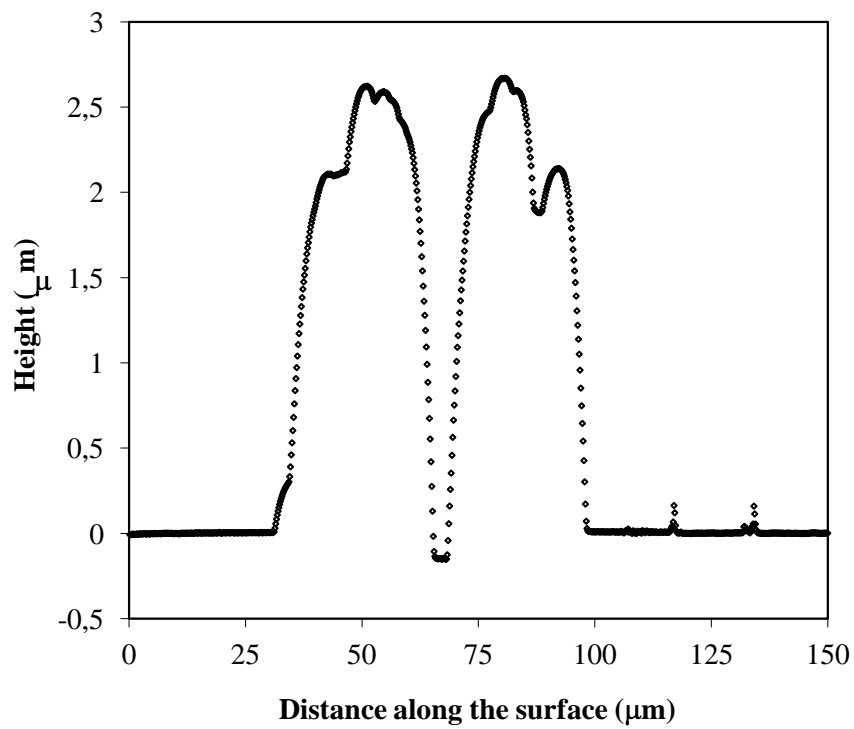
### **6.7 Release of ELOG templates**

Six microns of nlof 2070 resist was spun coated onto sample 2846, the sample was then aligned and exposed to UV light. All the devices on sample 2846 are double-clamped beams due to their position of the wafer and the design of the mask. After the post-exposure bake and development, the sample was given an O<sub>2</sub> plasma clean for 3 minutes and then dipped in hydrochloric acid for 5 minutes. The sample was then placed in the electron beam evaporator for the deposition of the metallic mask, which was 20 nm Ti and 200 nm Ni. The Ni was deposited in four 50 nm steps at a starting temperature of between 40°C and 50°C to control the amount of CTE mismatch and minimise the risk of delamination. Lift-off was then performed on the sample, which removed the resist and revealed the pattern on the ELOG templates. The image in figure 6.34 (a) shows that lift-off was successful on sample 2846.





(a)

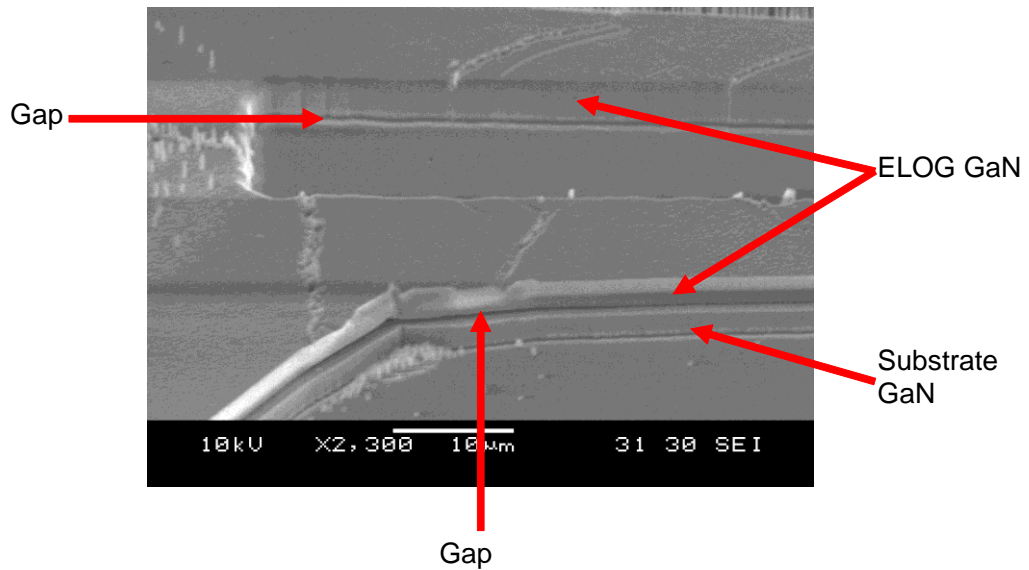


(b)

**Figure 6.34** (a) Optical image of sample 2846 after the lift-off of the resist, with arrow marking direction of Dektak scan. (b) Dektak scan of a double-beam ELOG device from sample 2846b.

Once good lift-off on the majority of devices was confirmed, the sample was cleaved in half in order to get two opportunities at releasing the beams. The first sample, 2846a, was Ar (5 sccm) / Cl (15 sccm) etched for 20 minutes and the second sample, 2846b, was etched for 27.5 minutes to ensure that the central beam was fully etched. The etch depth on sample 2846b was measured using the Dektak and this measurement, in figure 6.34 (b), shows that the GaN has been etched beyond the depth of the ELOG growths. The Dektak measurement also shows that the bars are lower in height than previously, this was caused by the etching of the top of the GaN beams because the Ti/Ni mask completely degraded due to the long etching time.

As the Dektak scan indicated that the central bar have been successfully etched away, the sample was subjected to a two hour buffered oxide etch to remove the SiN<sub>x</sub> mask under the beam. The sample then requires a buffered oxide etch to ensure that the beam is suspended and the release has been successful. In order to check if the release has been successful, the sample was analysed with the SEM. Figure 6.35 shows a tilted image of an ELOG device and the image is inconclusive. There appears to be gaps between the ELOG GaN and the substrate, indicating partial release. However, the gap between the GaN and the substrate on the top beam in figure 6.35 could be the result of the GaN. These images do not prove whether or not the release has been successful because they do not show if the SiN<sub>x</sub> has been completely removed by the buffered oxide etch. Additionally, there may be parasitic growths under the beams preventing a full release. Therefore, the sample required further investigation and was placed in a buffered oxide etch for a further three days to ensure that the entire SiN<sub>x</sub> mask was removed.

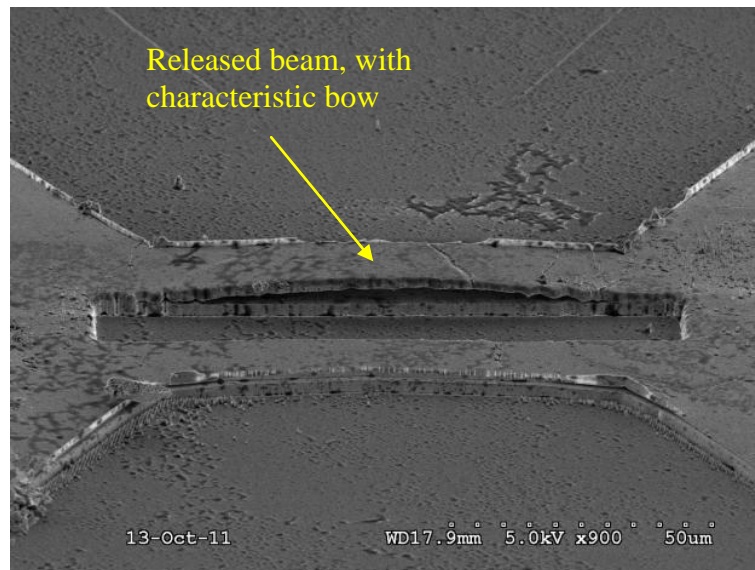


**Figure 6.35** A tilted SEM image of the ELOG beams.

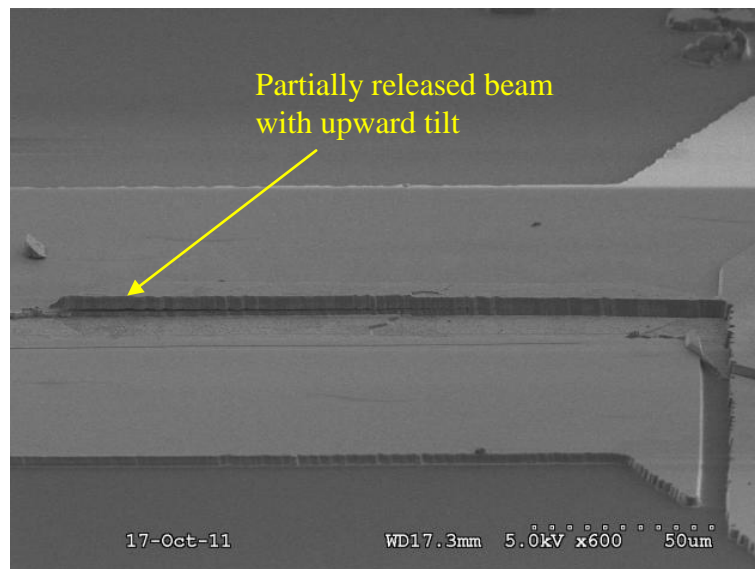
The same sample was analysed once again using a SEM after the three-day buffered oxide etch. The SEM used was field-emission, meaning that the sample did not require a sputtered gold coating. The sample was therefore placed on a clamped stand and placed straight into the SEM. As figure 6.36 shows the release was successful on one of the beams and partially successful some of the cantilever devices, with the beam becoming deformed and the cantilevers tilting slightly upwards due to strain relaxation resulting from the release. The beam sample (2846b) shows a lot of evidence of over-etching resulting from the degradation of the Ti/Ni mask and the sample was deliberately over-etched to ensure release of a thick sample in this case. The evidence for over-etching is the rough appearance of the ELOG template's surface, shown in figure 6.35. Samples consisting of less thick cantilevers need less etching time, ensuring the survival of the Ti/Ni mask.

In order to test this hypothesis, ELOG cantilevers were released from sample 2847. As table 6.5 shows, the central bar thickness of the ELOG templates on 2847 is 2.8  $\mu\text{m}$  rather than 5.5  $\mu\text{m}$  for sample 2846b. This allowed the central column to be completely etched away, after 12 minutes in the ICP, without the full degradation of the Ti/Ni mask. This resulted in the partial release of cantilevers with much smoother surfaces seen in figure 6.36 (b).

These results demonstrate the processes designed to create ELOG cantilevers are suitable and show that it is indeed possible to create GaN MEMS structures through the ELOG method. However, it should be noted that the protective mask requires significant improvement if it is to protect the surface of the ELOG sensing templates during the release etch. Despite this issue, it should be possible to create sensors from similar structures in the near future.



(a)

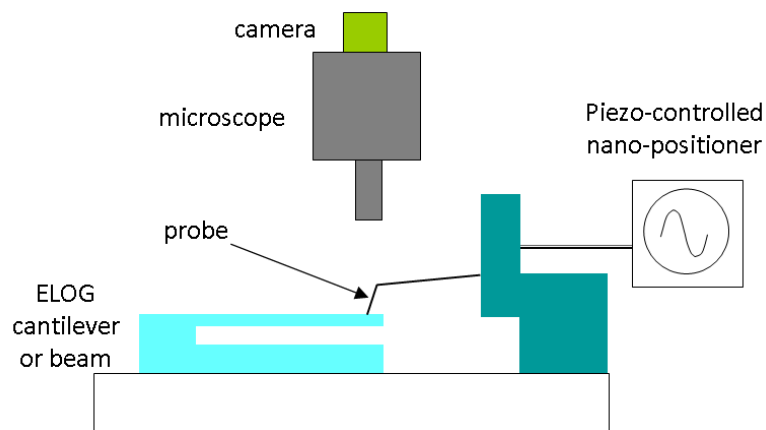


(b)

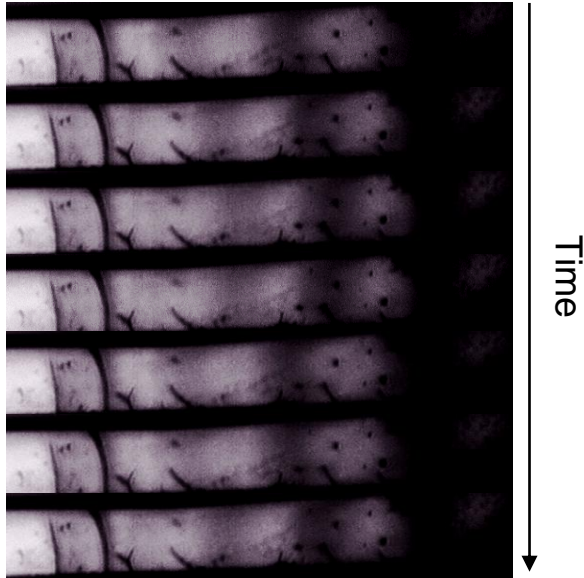
**Figure 6.36** (a) A SEM image of the ELOG beams taken after 3 days in a buffered oxide etch, showing a released beam. (b) A SEM image of a partially released cantilever produced using the same process as the beams.

## 6.8 Experimental deflection of the ELOG beams and cantilevers

Figure 6.37 shows the experimental set-up used to evaluate the beams and cantilevers as potential sensors. The piezo-controlled nano-positioner was programmed to oscillate up and down by  $\sim 1-5 \mu\text{m}$  and deflect either the cantilever or the beam. The sinusoidal motion of the probe caused the devices to move both laterally and vertically, due to the forces subjected by the nano-positioner. The movement of the beams and cantilever could then be detected by the camera in two ways: by its physical movement in the case of the cantilever or in the case of the beam device by shifts in the interference fringes arising from reflections from the GaN template both below the beam and within the beam itself, as shown in figure 6.38. Both device types readily oscillated and remained undamaged. The combined vertical and lateral movement of the cantilever was up to  $1-5 \mu\text{m}$ , representing  $\sim 5\%$  deflections of the length of the structure. These results suggest that the ELOG cantilevers and beams not only have little in-built strain, but are also mechanically robust as desired.



**Figure 6.37** Experimental apparatus used to deflect and assess the movement of the cantilevers and beams when subjected to a force.



**Figure 6.38** Shifts in the interference fringes with time when a beam was driven up and down by a probe mounted on a piezo-controlled nano-positioner.

## 6.9 Concluding Remarks

The ELOG method appears to be a promising approach to creating GaN cantilevers using the process described in this chapter. Such cantilevers could form the basis of sensors. This chapter describes the evolution in design, from the first generation of growths that were too small for a sensor to the current generation from which a double clamped beam was cut out by dry etching. However, the release process over-etched the GaN and suggests that the release process would benefit from a thicker Ti/Ni mask. It was found that Ni layers above 200 nm tend to delaminate whilst attempting to process some of the ELOG samples. Therefore devising a thicker metallic mask for ELOG MEMS release is not trivial. The uneven topography follows a characteristic pattern and this is most likely due to the ELOG growth method: suggesting a redesign of the contact pads is required. A small layer of molybdenum under the SiN<sub>x</sub> mask is a possible method for removing the parasitic growths, which are most likely caused by Ga diffusion. A proposed redesign of the contact pads will be briefly discussed in chapter 8.

Despite the issues, it is very promising that both cantilevers and beams were released using a photolithography process, as shown in figure 6.36, and this suggests that arrays of ELOG GaN sensors can be created using a top-down process offering more sensing flexibility and lowering costs. Initial mechanical oscillation tests show that the ELOG sensing templates are mechanically robust and have low in-built strain, which is a very promising result at this stage of development. The next stage is to deposit Ohmic and Schottky contacts onto a template in order to test its suitability as a sensor. Although the initial results appear to be promising, there is a lot of work still to do if an ELOG sensor is to be realised.

**The next chapter will describe the modelling, design and testing of a working GaN/sapphire HEMT diaphragm sensor. The work done on this sensor will demonstrate a lower risk method for creating a novel GaN sensor.**

## CHAPTER 7: MODELLING, DESIGN, DEVELOPMENT AND TESTING OF A GAN/SAPPHIRE DRUMSKIN PRESSURE SENSOR

### 7.1 Motivation of Chapter

Silicon diaphragm pressure sensors have been used since the discovery of piezoresistivity in silicon by Smith in 1954 [181, 182]. Although there are a number of examples of silicon-based ‘drumskin’ or circular diaphragm pressure sensors [181, 182], little work has examined GaN/sapphire based diaphragms. One of the advantages of using a GaN/sapphire structure, rather than silicon, is that the flexural rigidity will be increased due to both GaN and sapphire having a higher Young’s (or  $E_{33}$ ) modulus than silicon (see section 1.6). The reduction in deflection under an applied load and the superior mechanical properties of sapphire compared to silicon [4] offers the possibility to develop a sensor for operation at higher pressures than Si-based diaphragm devices. Patents were filed in the early 1990’s where sapphire based diaphragm sensors were used in conjunction with silicon piezoresistive sensors to take advantage of the piezoresistive properties of silicon and the superior structural properties of sapphire [183, 184]. There are potential benefits in replacing the silicon with GaN to create a GaN/sapphire based device. While the piezoresistive effect of GaN is small compared to its piezoelectric effect when directly attached to a substrate [31], it is a chemically inert material, stable up to 1000°C and has large piezoelectric coefficients. This suggests that this type of sensor has the potential to be sensitive to dynamic rather as well as static pressures.

Numerous devices in the literature have used transducers such as metal-insulator-semiconductor (MIS) diodes [4, 33] or HEMTs [29, 185] to measure the piezoresistive and piezoelectric properties of GaN, or determine strain, stress or pressure. Recently, circular AlGaIn/GaN HEMT structures have also been developed for strain sensing and piezoelectric characterisation [186, 187]. In this chapter, a pressure sensor using AlGaIn/GaN HEMT sensing elements on a robust sapphire membrane is designed, manufactured and tested. Six HEMTs have been strategically placed at different locations along the sensor membrane in order to characterise the piezoelectric effect induced by an applied pressure on different areas of the chip.



The sensor has been designed to operate in pressures exceeding 50 bar (5 MPa) and temperatures exceeding 450°C. This represents a significant improvement on Si-based technologies that has an upper operating temperature of 450°C [114, 188] due to Si having a lower band gap [2]. The ultimate target for the GaN pressure sensors is to operate in environments beyond the limits of Si metal oxide semiconductor field effect transistor (MOSFET) technology, which are defined as harsh environments in this project (see sub-section 1.1.2). GaN can operate in these environments because it has a larger band gap than Si [2] and is mechanically stable at high temperatures (see chapter 5). GaN HEMT pressure sensor applications are varied, from oil wells to aeroplane engines [114, 188]. Extracting crude oil and natural is a high risk, potentially fatal exercise due to the unpredictable conditions in the oil well. The GaN sensor has been designed to operate in conditions similar to an oil well, meaning that they can be used to sense the conditions inside the well itself.

## **7.2 Aims of Chapter**

This chapter describes the modelling design and testing GaN/AlGaN/sapphire based device using HEMTs as the sensing element. By using HEMTs as sensing elements along the diaphragm, the piezoelectric and semiconducting properties of GaN could be harnessed into a pressure sensor for harsh environments; examples of HEMTs being used as a pressure sensor can be found in sub-section 1.4.2.

Once the concept for the sensor was devised, it was modelled using commercially available ANSYS V11.0 FE software. The purpose of the modelling was to predict the stress distribution and piezoelectric sensitivity of the entire sensor and this can be used to determine the optimal position for the sensing HEMTs on the diaphragm. The model will also help investigate the influence of the bond layer between the sensor element and its packaging, and at what pressure the sensor is likely to fracture with respect to geometry. Since the sensor will need to survive at least 50 bar of pressure, optimising the geometry is important.

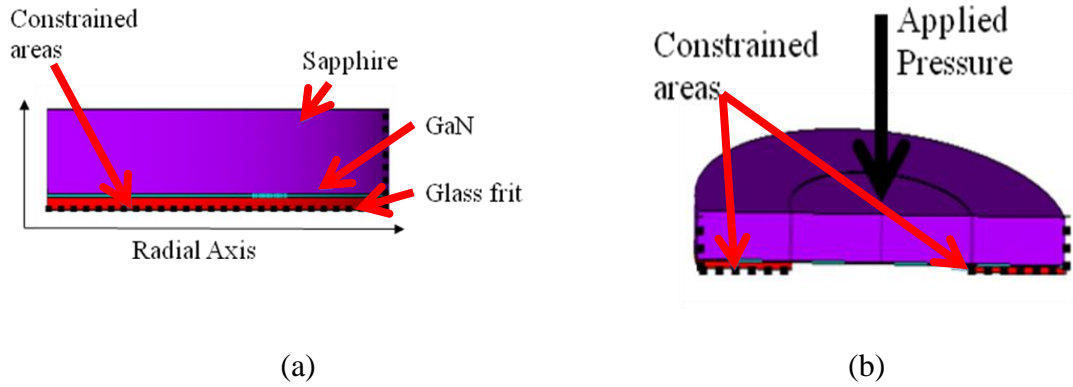
Once the geometry and position of the HEMT sensors were determined, they had to be incorporated into a photosensitive mask set so that the sensors could be fabricated.

During mask design, the geometry of the HEMTs was confirmed and in particular the size of the Schottky gate. A HEMT with a large gate size can also be used as a capacitive sensor [34-36]. Based on the modelling results, three different HEMT arrangements were chosen and incorporated in the mask; there will be a brief discussion about the reasons why each HEMT arrangement was chosen. Finally, the basic fabrication process and the metallisation scheme used on the Ohmic contacts and Schottky gate will be described.

The fabricated sensor was then tested at high pressure, which was undertaken in an in-house designed test rig at Bath. The test rig needs to be able to operate safely at 100 bar of pressure, which is potentially hazardous. There is will be a brief discussion of the safety features incorporated into the design of the test rig. The design and equipment used for the test rig will be described, as well as the methodology used to test the final sensors. The results from the diaphragm sensor (the 'drumskin') tests will be analysed and compared with the FE model. This chapter will be concluded with some comments about how the design of the sensor can be improved and optimised further in the future, in addition to a comparison with other high temperature pressure sensing solutions in the literature.

### **7.3 Modelling**

The proposed device was modelled using ANSYS V11.0 finite element (FE) software [182] because it has suitable 3D coupled-field elements (SOLID 98) that combine the structural, thermal and piezoelectric behaviour of the device. Figure 7.1 shows a schematic of the drumskin device; without an outer alumina package that is bonded to the device by the glass frit. The model assumes that the alumina casing is rigid and constraints have been applied to take this into account, as shown in figure 7.1. Creating the model in this way allows an improved mesh density around the GaN/sapphire drumskin sensor element. It is assumed that the structure is perfectly elastic since GaN and sapphire are linearly elastic and brittle materials.



**Figure 7.1** Schematic of the GaN/Sapphire drumskin pressure sensor. Sapphire, GaN and the glass frit are purple, turquoise and red respectively. Where (a) is the side view and (b) is the cross-sectional view. Total diameter of the sensor is 8mm.

The model consists of an 8 mm diameter GaN/sapphire disk, where the GaN layer is fixed to a glass frit that is constrained in all dimensions at the base. The glass frit radially covers the outer 2 mm of the device, as shown in figure 7.1; resulting in an effective diaphragm diameter of 4 mm. Computational constraints have limited the GaN layer thickness to 15  $\mu\text{m}$ , approximately three times greater than the likely layer thickness. In the case of figure 7.1, the thicknesses for the sapphire substrate and glass frit were 350 and 50  $\mu\text{m}$  respectively. The room temperature material properties used for GaN and sapphire are reviewed and discussed in chapter 1; although higher temperature operation is anticipated. The glass frit was assumed to have a Young's modulus of 55 GPa and a Poisson's ratio of 0.3 [189].

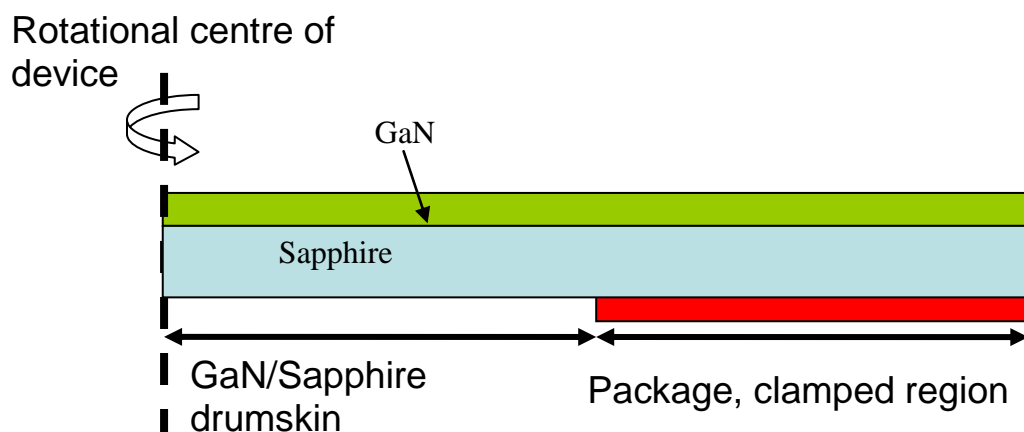
The purpose of the model was to determine the piezoelectric response of the GaN layer with respect to pressure and the resulting stress exerted on the sensor. Although increasing the pressure will increase the piezoelectric response, it will also increase the strain on the sensor and increase the likelihood of failure by brittle fracture. The sensor was modelled two ways, one with the GaN below the sapphire and in contact with the glass frit and with the GaN above the sapphire. The position of the thin GaN layer has a small effect on the piezoelectric response of the sensor, because the overall stress profile of the sensor changes very little because the thick sapphire is the dominant material and the sign of the piezoelectric polarisation says the same. The piezoelectric polarisation sign does not change because both the sensor and crystal orientation are reversed. Therefore the model results shown are valid for a sensor working either way up. This is useful information because the pressure will be

applied to the GaN side in the test rig and to the sapphire side once the sensor is fully packaged.

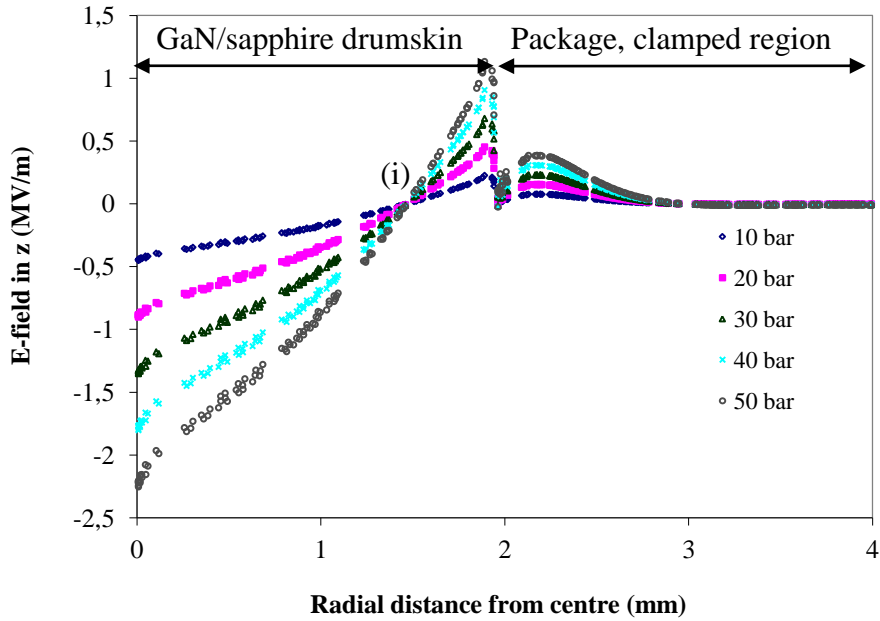
## 7.4 Results from modelling and design considerations

### 7.4.1 Piezoelectric polarisation and optimisation of positions for the HEMT sensors

Initially, the drumskin behaviour was modelled at pressures of 10 - 50 bar (1-5MPa) and the resultant electric-field perpendicular to the radial direction formed by the piezoelectric polarisation of GaN was calculated. It was assumed that the sensor was operating at room temperature and internal stresses in the GaN/sapphire wafer caused by lattice and thermal mismatch were neglected. The results, shown in figure 7.2, follow a set pattern and this is useful when devising the final sensor design. For all pressure models, there is a point approximately 1.5 mm from the centre of the drumskin where there is no piezoelectric charge, point (i) in figure 7.2. This is analogous to the point of zero strain in piezoresistive diaphragm sensors [182] and is present since the piezoelectric polarisation is directly caused by the stress applied to the drumskin. From this result, HEMTs should ideally be placed at regions of maximum electric field which correspond to the centre of the drumskin; although at this development stage HEMTs can be positioned at a number of locations on the drumskin to compare theory with experiment.



(a)



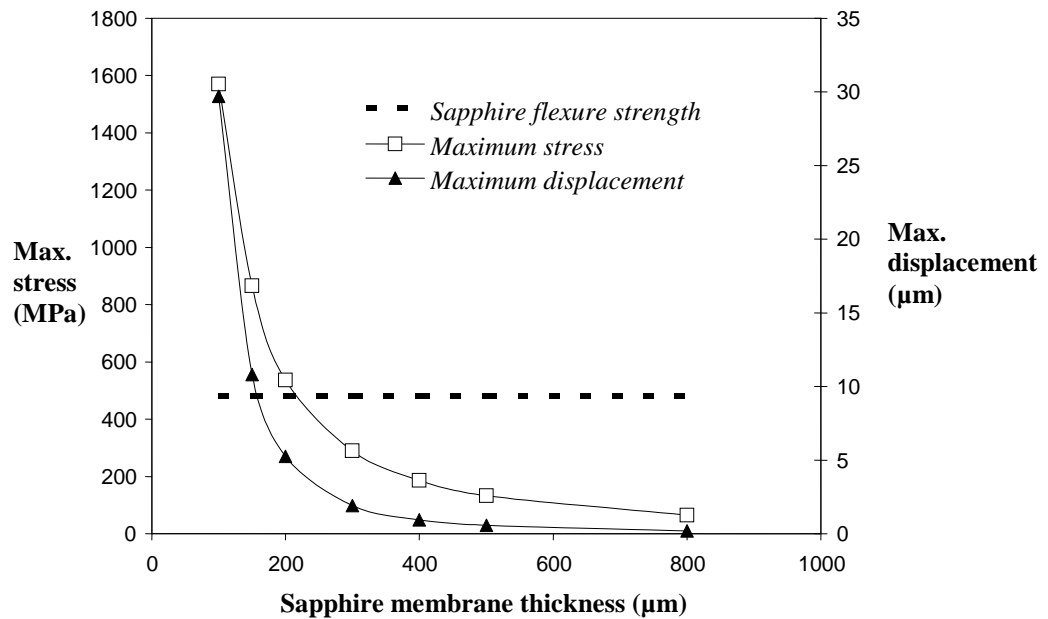
(b)

**Figure 7.2** (a) Model schematic (b) Piezoelectric E-field from drumskin sensor at room temperature and 10 - 50 bar pressures.

#### 7.4.2 Optimisation of sapphire membrane thickness

By studying the maximum displacement of the membrane under a fixed pressure, the mechanical response of the device can be optimized to provide high sensitivity. To improve sensitivity it would be desirable to have maximum strain but not have mechanical failure of the sensor element. As would be expected, the maximum displacement of the membrane is located at the centre of the membrane and the easiest way to increase the deflection, and sensitivity, of the sensor is to reduce the sapphire layer thickness. However, as the sapphire thickness is reduced the stress in the structure is accordingly increased. As a result, a compromise must be found between maximum displacement and maximum stress of the membrane. To examine the influence of sapphire thickness, a study of the mechanical response of the pressure sensing structure under a fixed pressure of 50.66 bar (50 atm) has been undertaken, knowing that the flexural strength of sapphire is  $\sim 450$  MPa [190]. Figure 7.3 shows that a good compromise between sensitivity and stress level can be achieved with a membrane thickness between 250-350 $\mu\text{m}$ . When the sapphire substrate is much

thicker the stress and centre displacement is small. When the sapphire substrate is less than 200  $\mu\text{m}$ , the tensile stress level is much higher and can exceed the failure stress of 450MPa as indicated by the dashed line in figure 7.3. A further increase in the membrane thickness reduces the displacement unnecessarily because the non-failure stress condition is fulfilled.



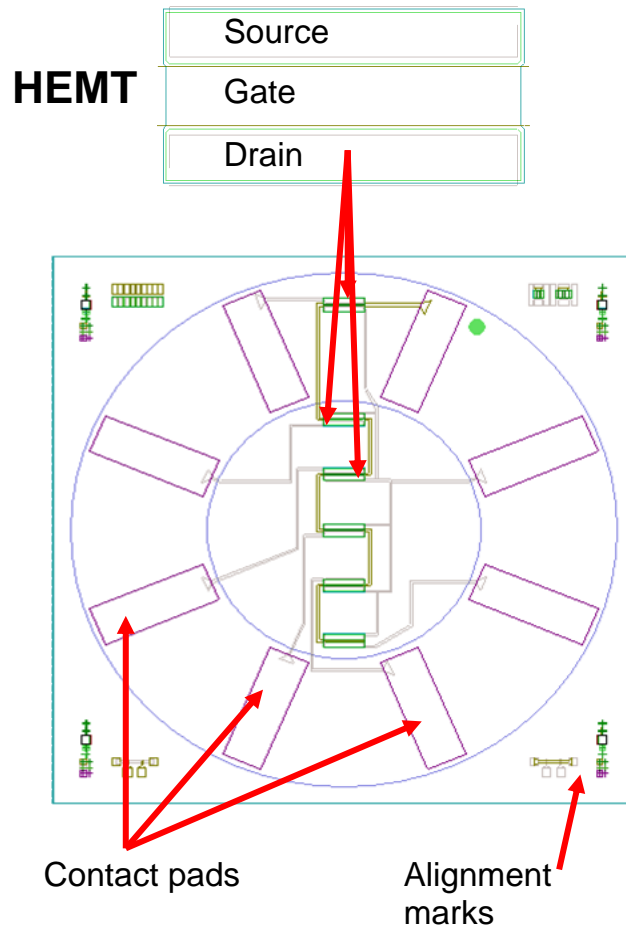
**Figure 7.3** Maximum displacement and maximum tensile stress against the sapphire membrane thickness. The sapphire flexural strength is indicated at 450 MPa (Plot courtesy of TIMA Laboratory, UJF, Grenoble, France).

### 7.5 Design of the drumskin sensor mask set

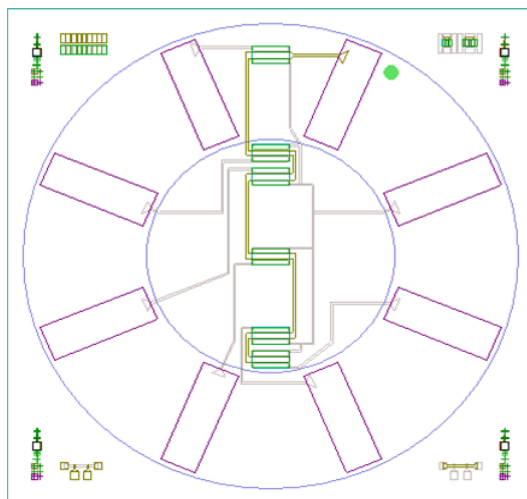
Now that the mechanical piezoelectric response of the sensor element is known, a mask set was designed for the purpose of fabricating drumskin sensors. The mask design was undertaken in collaboration with IEE-SAS in Bratislava, who were in charge of fabricating the drumskin sensors for the MORGaN consortium. Each drumskin sensor element was 8 mm in diameter, with the central 4 mm consisting of the sensing membrane, as in the FE model shown in figure 7.1. After drawing the sensor to scale, there was sufficient space for eight contact pads 1.8 mm in length and 0.2 mm in width around the outer region bonded to the packaging. This meant that

there was sufficient space for six HEMT transducers on the sensor: each with individual drains, and a common source and gate.

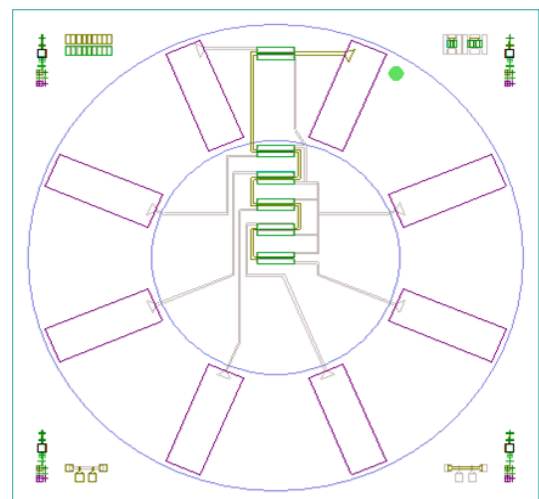
The mask set consisted of five layers, which were used to pattern the wafer and create drumskin sensors. The first layer was a mesa isolation layer required to separate the HEMT region from the rest of the wafer and minimise parasitic charges. The second layer was for depositing the metal for the contact pads, which were made of Ti/Au due to their high electrical conductivity. The next two layers were the Ohmic and Schottky contacts, the Schottky contacts were Ni/Au and the Ohmic contacts were Nb/Ti/Al. In a HEMT the source and drain contacts are Ohmic and the gate is Schottky (see section 1.4.1). As the gate was common to all HEMTs, the gate metal ran in series through all of the sensors and connected directly to the common source contact pad. Finally, the fifth layer was for the metallic wires that connected the Ohmic and Schottky HEMT contacts to the contact pads. The metallic wires had the same metallic composition as the contact pads.



(a)



(b)



(c)

**Figure 7.4** The drumskin sensor designs, where (a) is the evenly spaced design, (b) is the zero signal finder and (c) is the high resolution design



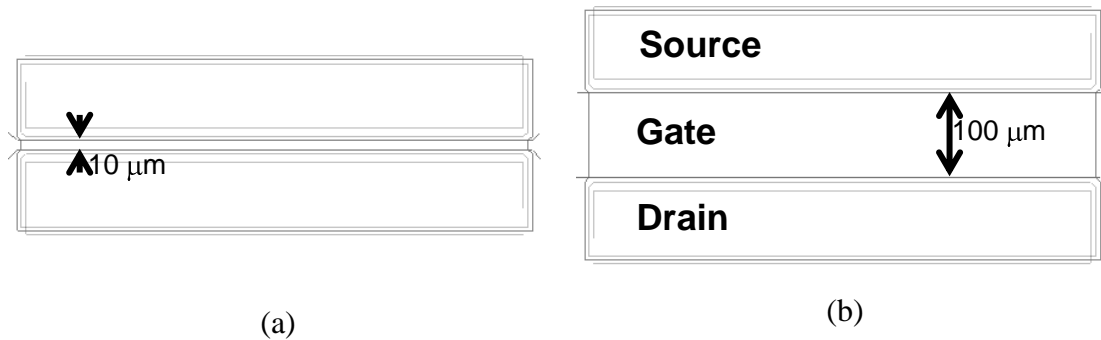
As figure 7.4 shows, three types of drumskin sensor were designed, each with different HEMT arrangements. Every design has a HEMT placed outside of the membrane region, known as the reference HEMT, where the sensor is stress-free, in order to calibrate the sensor. The signal from GaN HEMTs degrades when the temperature is increased [5] and the first law of thermodynamics state that increasing pressure in an enclosed area also increases temperature. Therefore a stress-free calibration HEMT is required in order to monitor the influence of temperature (and not stress).

**Design I:** (Figure 7.4(a)) The five sensing HEMTs have been spaced evenly across the membrane. This was undertaken to test the symmetry of the sensor and provide data to compare with the model predictions. The drumskin should be a symmetric device, but HEMT contacts are easily damaged and a symmetric arrangement means that there is a secondary sensing element should a HEMT fail during manufacture or testing. For this design, the central HEMT is expected to have the strongest signal change (change in voltage when current is kept constant or vice versa) when strain is applied and the HEMTs at the edge of the membrane having reasonably strong signal changes of the opposite polarity. The HEMTs positioned halfway between the edge and the centre are expected to have the weakest signal changes, but these will be of the same polarity as the signal change of the central HEMT.

**Design II:** Figure 7.4 (b) shows an alternative HEMT arrangement, although still symmetrical, with the two HEMTs halfway between the edges and centre of the membrane in figure 7.4 (a) being moved more towards the edge of the membrane. These HEMTs were moved in order to find evidence for the region of the membrane shown on figure 7.2 that has no signal, which is important for validating the model. The HEMTs that have been moved in relation to design I are are expected to see little or no signal change.

**Design III:** Finally figure 7.4 (c) is a high resolution arrangement, where all of the HEMTs are in one half of the sensor. This sensor arrangement will produce five independent measurements of strain and this data is valuable for comparing the model

with experimental data. The signal changes produced by this HEMT arrangement should closely follow the plot in figure 7.2.



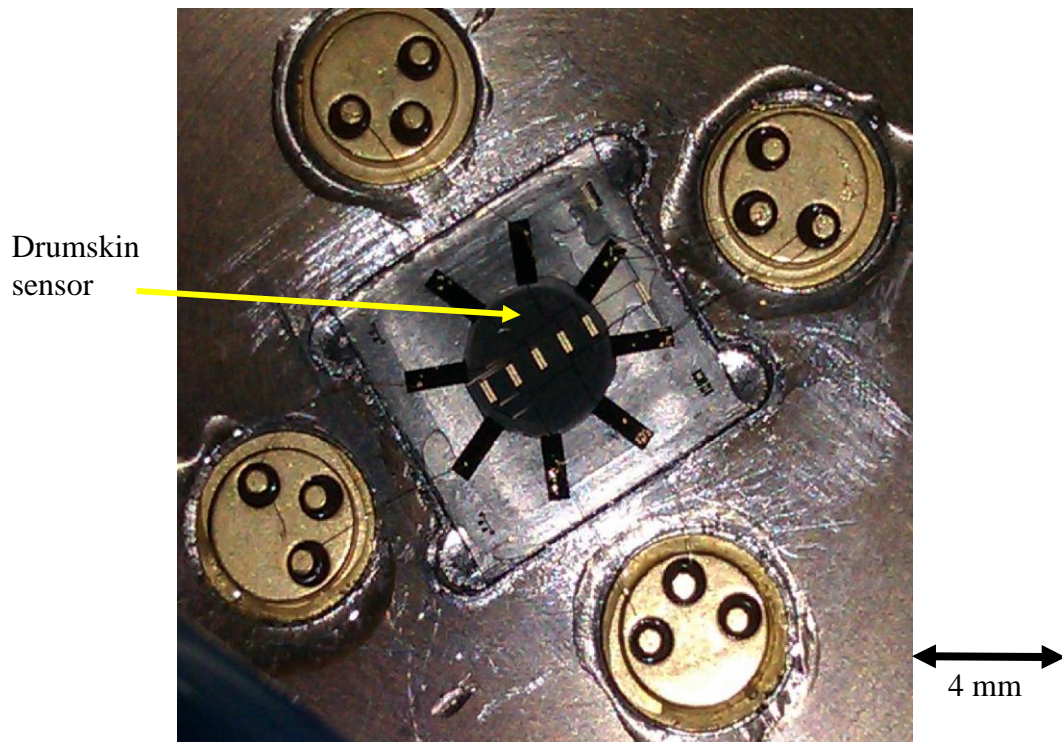
**Figure 7.5** Different HEMT sizes used on the drumskin sensors, where (a) is a 10 μm gate length HEMT and (b) is a 100 μm gate length HEMT (also known as a FATFET).

In addition to the three different sensor arrangements, two different types of HEMTs were used as shown in figure 7.5. The two different types of HEMT are differentiated by their gate lengths that are 10 μm, shown in figure 7.5 (a), and 100 μm (also known as a FATFET [34-36, 191]), shown in figure 7.5 (b). The 10 μm gate length HEMT is smaller in width than the FATFET and this means that either more HEMTs can be placed on the sensor or it can be used as a sensing element on a miniaturised sensor. Although the FATFET is not as flexible in terms of positioning as the 10 mm gate width HEMT, it is sufficiently small so that five FATFETs fit comfortably on the 4 mm diameter membrane. The motivation for creating FATFET versions of the sensor is that they can be used for capacitance-voltage (C-V), as well as current-voltage (I-V) measurements, giving the scope for additional gauge factor measurements. However, this chapter only discusses the operation of a 10 μm gate length device because the FATFET devices were unavailable at the time. It is hoped that C-V measurements of a FATFET will be attempted in the future.

## 7.6 Design of a high-pressure drumskin test rig

Once the design of the drumskin and composition of the mask set had been agreed amongst MORGaN project partners, the drumskin chips were then fabricated by IEE-

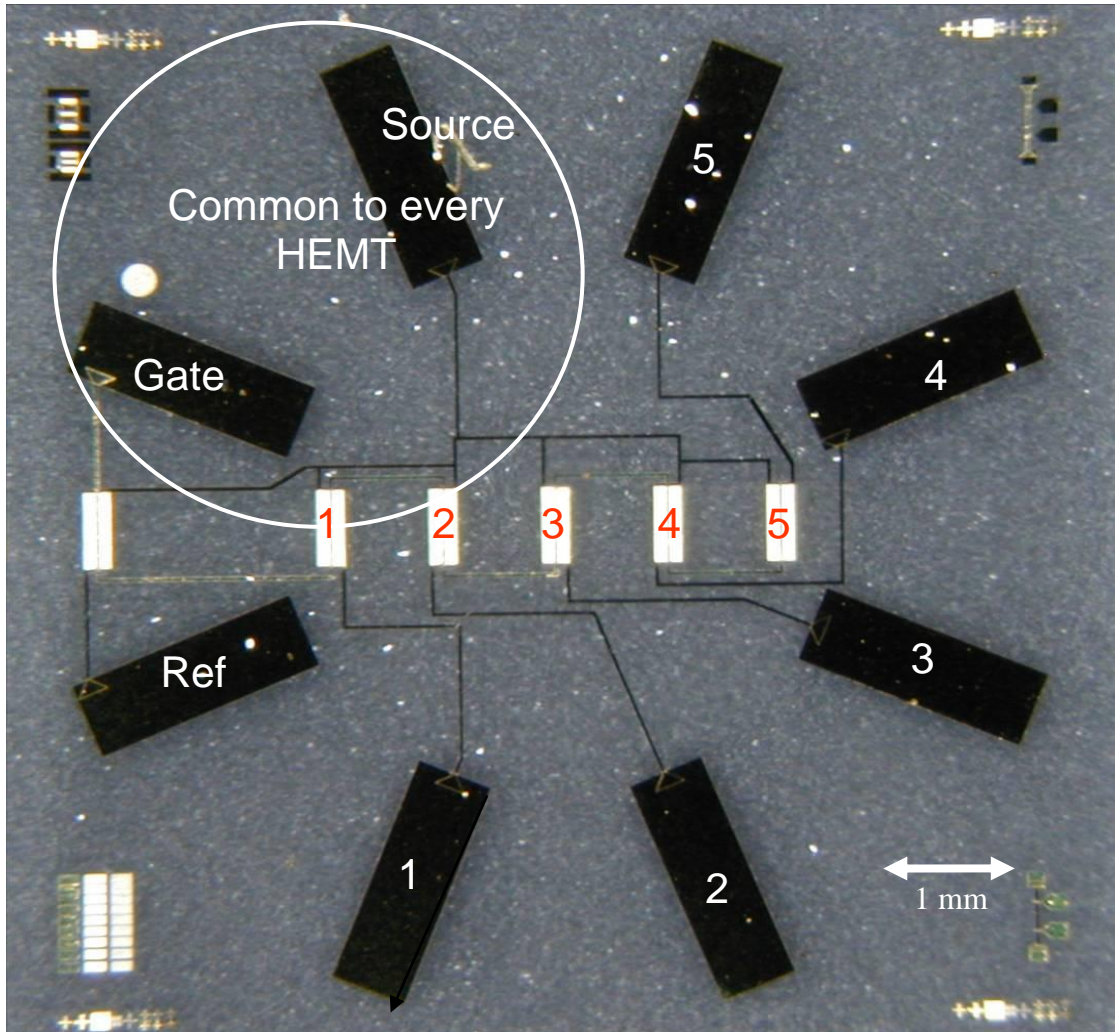
SAS. At Bath, the emphasis was on modelling, design (informed from model), mask set creation and creating a test rig capable of testing the drumskin at >50 bar and up to 60°C. The rig was built using parts and flanges from previous test rigs. The test rig was cylindrical and made out of steel, and the pressure was provided by a regulated N<sub>2</sub> gas cylinder.



**Figure 7.6** Image of mounted drumskin sensor and T/O headers, which have been wire bonded to the contact pads.

A standard flange was initially modified by drilling five 4 mm diameter holes into a flange. Secondly, an 8 mm<sup>2</sup> mounting area was cut into the centre of the flange so that the drumskin could be mounted into position. The drumskin sensor was mounted onto the modified flange shown in figure 7.6 using cyano-acrylate adhesive. In order to simplify the wire-bonding, the sapphire face of the drumskin chip was glued to the flange. The T/O headers, which provide the signal from the sensor with a route out of the test rig, were mounted using an epoxy. T/O headers consist of pins (in this case three pins) and metal wires exiting the rear of each pin, which are used to provide encased electrical components with wiring a connection to an external power source. The contact pads were connected to the T/O headers by wire-bonded gold wires.

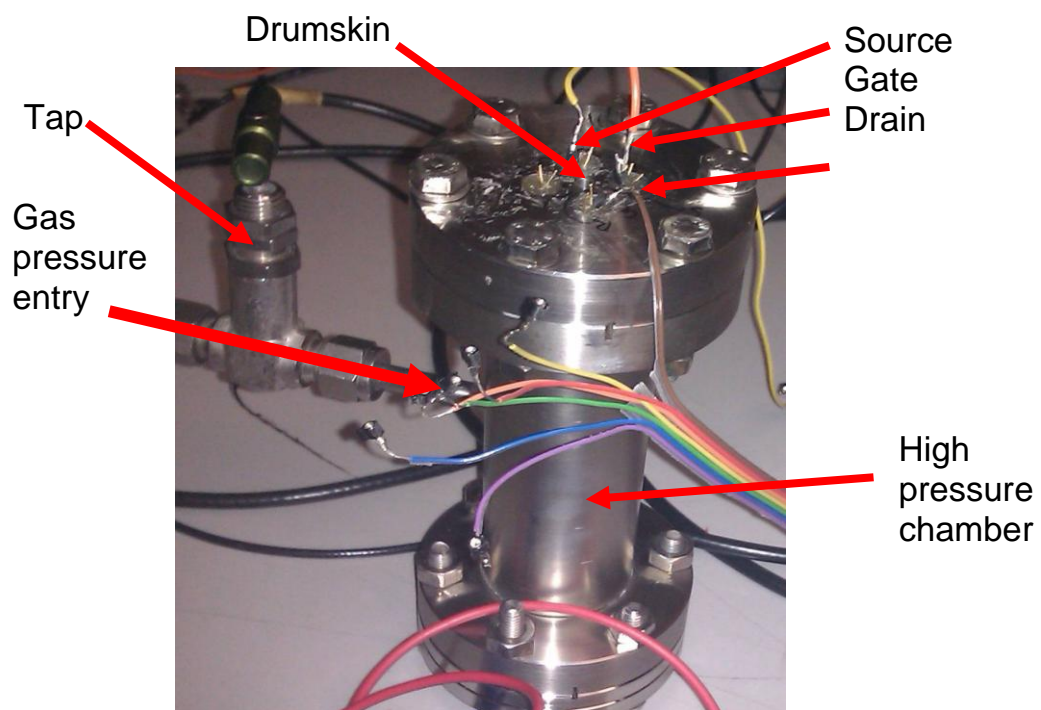
Every contact pad was given the designation shown in figure 7.7. The calibration HEMT was designated HEMT Ref and the HEMTs on the membrane were numbered 1 to 5; with HEMT 1 being the closest to the calibration HEMT and HEMT 5 being the furthest away.



**Figure 7.7** An image of the 1<sup>st</sup> drumskin sensor mounted onto the test rig, with the HEMTs and corresponding contact pads labelled.

The drumskin test rig, shown in figure 7.8, consisted of a cylindrical tube with a valve at the side to allow gas in and out. The cylindrical tube was secured at either end by flanges, lined with brass O-rings to help prevent the leakage of gas. One of the flanges was the drumskin-mounted flange. The drumskin-mounted flange was securely bolted onto the cylindrical test rig using six heavy duty screws and bolts, as

shown in figure 7.8. The screws were heavily tightened to ensure that there was no gas leakage. The flange on the opposite side of the test rig was fastened in the same fashion. The test rig was then securely fastened to a tap. The tap was when connected to the gas cylinder using initially plastic tubing of the lower pressure measurements up to 10 bar. Stainless steel tubing was used for the measurements up to 60 bar because plastic tubing is not designed for use above 20 bar. The reverse side of the drumskin flange was labelled so that the electrical wires could be easily connected to the corresponding contact pad.

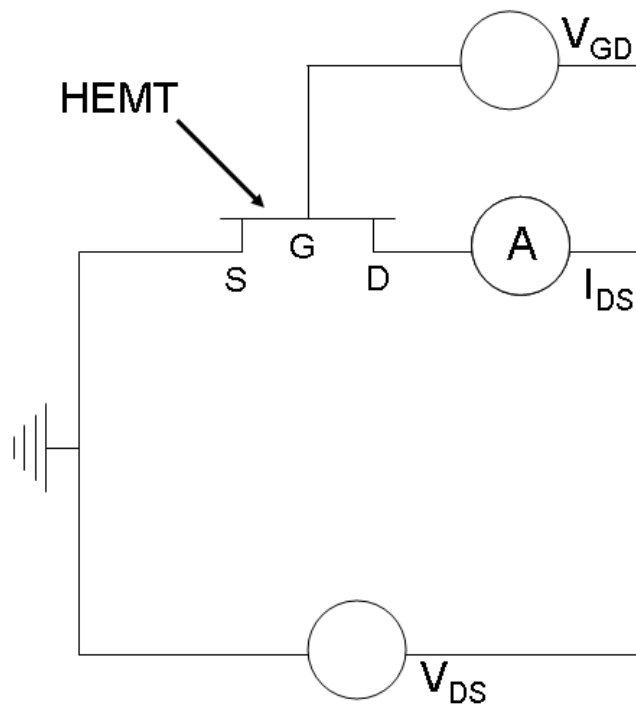


**Figure 7.8** An image of the high pressure test cylinder used to test the drumskin sensor.

A K-type thermocouple and a pressure transducer were added to the rig and used to monitor both temperature and pressure inside the chamber. A small hole was drilled into flange for the insertation of the thermocouple and the hole was then filled with an epoxy. The pressure transducer was placed between the gas cylinder and the tap at the base of the test rig, which controls gas flow into the chamber. The pressure transducer and thermocouple were added to the test rig to explore the effects of adiabatic heating

in the gas chamber, as indicated by the initial measurements. Additionally, a pressure release valve was inserted near the tap to allow the quick evacuation of air from the chamber. Electrical measurements were also carried out with a pulsed  $I_{DS}$  or  $V_{DS}$  rather than continuously, to reduce the degree of self-heating on the chip. All of the measurements were done by applying  $V_{DS}$  or  $I_{DS}$  for 10ms and switching it off for 90ms. Measurements were performed on all HEMTs as a function of temperature and pressure, for both static and dynamic pressure applications. Finally, the test rig was placed into another stainless steel chamber for safety purposes.

### 7.7 Initial results from the drumskin sensor test rig

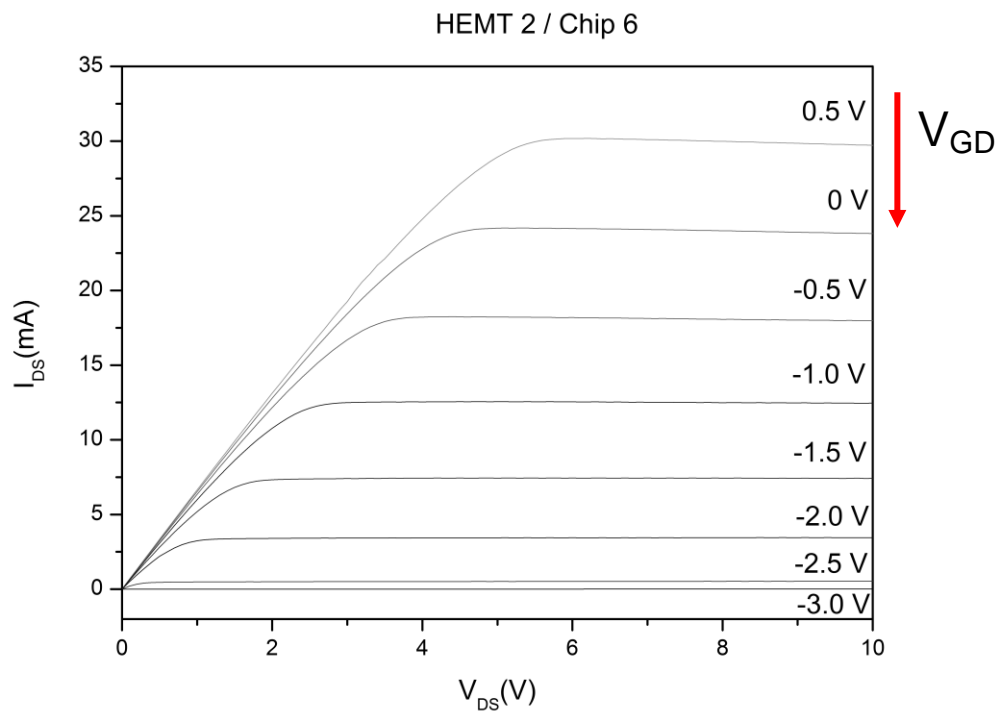


**Figure 7.9** Circuit diagram showing how the drumskin sensor was electrically connected.

Initially, the  $I$ - $V_{DS}$  curve of every HEMT was measured at atmospheric pressure to make sure that the HEMT sensing elements were working correctly. The  $I$ - $V_{DS}$  measurements were undertaken using a Keithley 236 current-voltage source



integrated with Labview, which automated the measurement and collated the output data into spreadsheet. When appropriate, a gate voltage was applied using a Keithley 2400 sourcemeter. The circuit diagram in figure 7.9 shows the experimental set up.  $I_{DS}$  -  $V_{DS}$  sweeps were repeated at initially atmospheric pressure for different  $V_{GS}$  in order to ensure that the gate was functional. A sensor was mounted in its place using cyanoacrylate glue and with its contacts where wire-bonded to the T/O headers. The mounted sensor's  $I_{DS}$  -  $V_{DS}$  characteristics were then measured and are plotted in figure 7.10. These measurements show that the gate is functional in this sensor, and mean that a bias on the gate can be used to control the sensor characteristics.

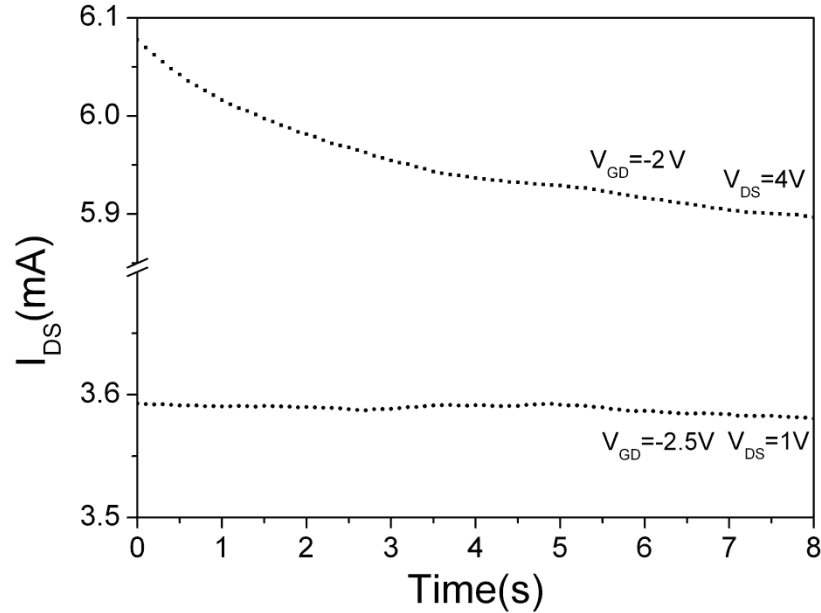


**Figure 7.10**  $I_{DS}$  -  $V_{DS}$  characteristics of HEMT 2 on second chip, showing a functional gate and good HEMT behaviour.

## 7.8 Results from drumskin

### 7.8.1 Temperature dependency

#### 7.8.1.1 Removing Self-Heating



**Figure 7.11** Time dependence of  $I_{DS}$  on HEMT 3 measured at atmospheric pressure for drain-source voltages of  $V_{DS} = 4V$  and  $V_{DS} = 1V$  and gate voltages of  $V_{GD} = -2V$  and  $V_{GD} = -2.5V$  respectively.

High power operation of devices, especially GaN/AlGaN HEMTs grown on sapphire, can induce an increase in the operating temperature in the device known as self-heating. This suggests that  $I_{DS}$  will decrease with respect to temperature when a constant or pulsed voltage is applied [5, 192]. The potential causes of the thermal effects are from self-heating of the device, resulting from applying a bias, and changes in the temperature inside the test rig caused primarily by adiabatic changes in pressure. Figure 7.11 shows data of the central HEMT (HEMT 3) operating at two different drain voltages  $V_{DS} = 4V$  and  $V_{DS} = 1V$ , with gate voltages of  $V_{GD} = -2V$  and  $V_{GD} = -2.5V$  respectively and these values were chosen to show that self-heating can simply be reduced to negligible levels. This experiment shows the impact that higher power operation has on current characteristics over time, despite using a pulsed voltage.

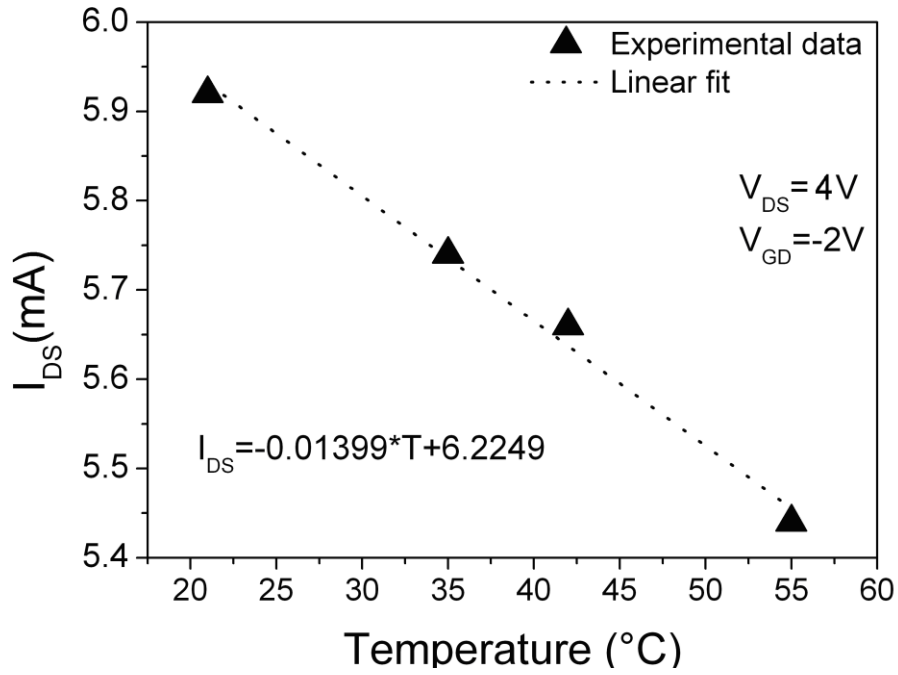


Time-resolved measurements performed whilst running the device at  $V_{DS} = 4V$  and  $V_{GD} = -2V$  for 8 seconds showed a decrease in  $I_{DS}$  from 6.08mA to 5.91 mA, a 3.5% decrease. Similar measurements carried out at  $V_{DS} = 1V$  and  $V_{GD} = -2.5V$  showed a smaller decrease of approximately 0.002mA, corresponding to a 0.05% decrease. The behaviour obtained at  $V_{DS} = 4V$  and  $V_{GD} = -2V$  was as a result of self-heating. As the impact of the piezoelectric effect on the HEMT characteristics could be small, performing measurements with negligible self-heating is essential to de-couple these effects. What these measurements show is that the self-heating can be minimised by keeping  $V_{DS}$  low and running the sensor just above channel off, which is achieved by applying significant negative bias (in this case -2.5V) to  $V_{GD}$ .

#### *7.8.1.2 Heating the Sensor*

As the sensor is required to operate at elevated temperatures, a method for applying heat onto the sensor without increasing the pressure had to be devised. This was undertaken experimentally by disconnecting the test rig from the gas cylinder and wrapping it with heating tape (Thermo Fisher Scientific, HT95503 Heating Tape). A k-type thermocouple was implanted into the flange, near the sensor, and was sealed into place using an epoxy. This allowed the thermal characterisation of the behaviour of the sensor with respect to temperature. The thermal response all of the HEMT sensing elements were measured at atmospheric pressure for a  $V_{GD}$  of -2V and  $V_{DS}$  of 0.1, 1 and 4V.

Figure 7.12 shows the effect of a gradual increase of temperature from ambient temperature to 55°C and shows a linear decrease of  $I_{DS}$  with increasing temperature. This shows the effect of a temperature increase on the HEMT characteristics and agrees with figure 7.11 in that  $I_{DS}$  decreases with increase in temperature. As a rapid increase of pressure in the chamber results in a temperature rise, dynamic pressure measurements of gas pressure would have to be corrected by the temperature dependency of the HEMT for a specific  $V_{DS}$  and  $V_{GD}$  in this type of application.



**Figure 7.12** Variation of mean  $I_{DS}$  as a function of temperature for HEMT 3 at atmospheric pressure for  $V_{GD} = -2V$  and  $V_{DS} = 4V$ .

### 7.8.2 Static pressure dependency

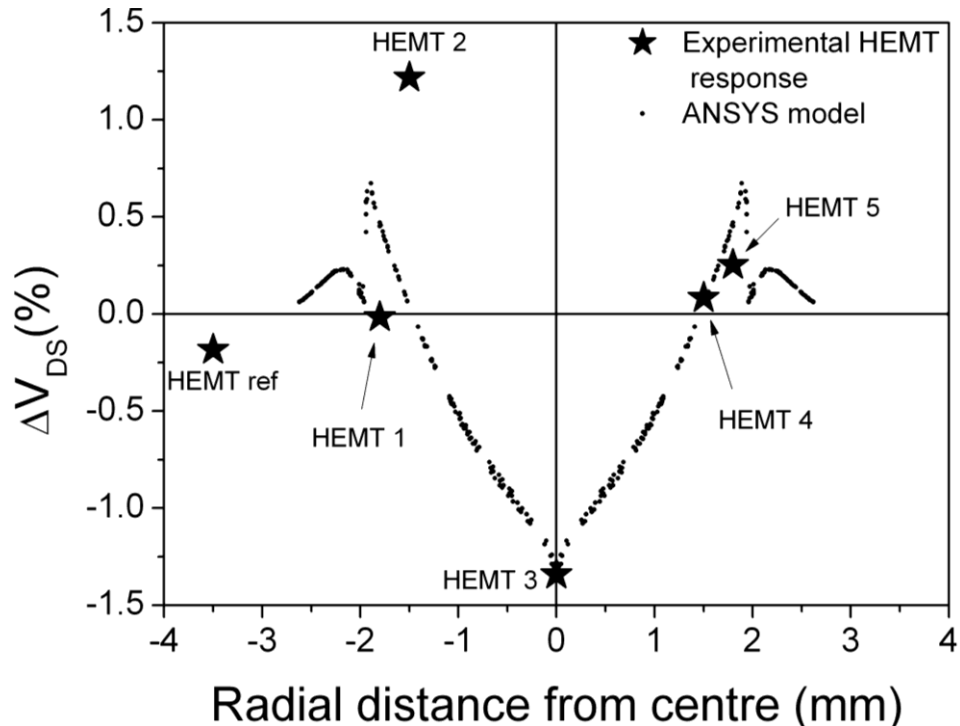
Similar measurements were performed on all HEMTs across the drumskin diameter at a constant pulsed current where  $I_{DS} = 3mA$  and  $V_{GD} = -2.5V$  for static gas pressure, allowing time for the sensor to recover back to the ambient temperature.  $\Delta V_{DS}$  of each HEMT with respect to applied pressure was calculated in (4.1).

$$\Delta V_{DS} = V_{DSatm} - V_{DSpressure} / V_{DSatm} \quad (4.1)$$

Where  $V_{DSatm}$  is equal to  $V_{DS}$  at atmospheric pressure and  $V_{DSpressure}$  is equal to  $V_{DS}$  at the applied pressure.

Assuming that HEMT 3 at the drumskin centre has the largest response, the piezoelectric response was calculated over the radial distance in [193]. The dashed lines compare the data the results shown in figure 7.2. The data from the FE model [193] was then modified from electric field to percentage change, in order to compare

predictions of the model with experimental data. A comparison between the FE model and experimental measurements is shown in figure 7.13.

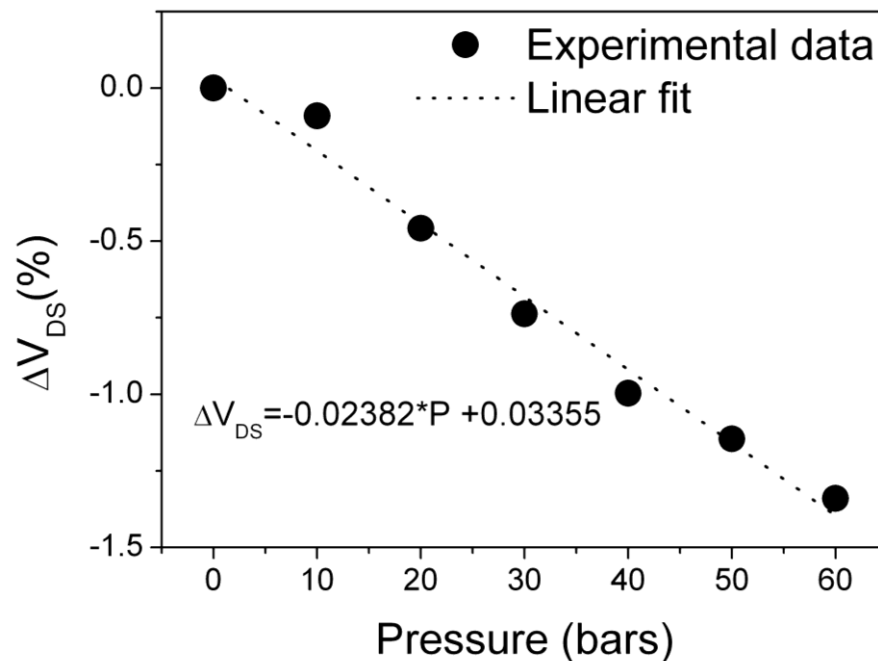


**Figure 7.13** Representation and comparison of experimental HEMT response to an application of 60 bar static gas pressure (stars) with the FE model prediction (dots) [193].

The response of each HEMT to applied pressure closely follows the model prediction. The biggest change in signal was measured for central HEMT 3, as predicted. The deviation between the model and experimental data on HEMTs 1 and 2 may be due to a small misalignment of the chip and the chip may not have been perfectly level due to the thick glue used. The small change of signal measured at the stress-free reference HEMT (HEMT ref in figure 7.7) is ideally zero and is likely to be due to imperfect clamping by the cyano-acrylate glue. The voltage changes of HEMTs 2, 4 and 5 were positive. This is due to a change of sign at the edge of the drumskin, caused by a transition from compressive to tensile behaviour, as predicted by the FE model (see figure 7.2).

### 7.8.3 Linearity of sensor response to pressure

The voltage characteristics at  $I_{DS} = 3\text{mA}$  and  $V_{GD} = -2.5\text{V}$  of HEMT 3 were measured from atmospheric pressure to 60 bar in 10 bar intervals and compared with the model, to assess its linear conformity with the model. The results are shown in figure 7.14. A linear  $V_{DS}$  decrease of 0.02%/bar was found. This linear behaviour is reasonable and agrees with the FE model data in figure 7.2 and any deviations from linearity may be due to piezoelectric relaxation and imperfect clamping.

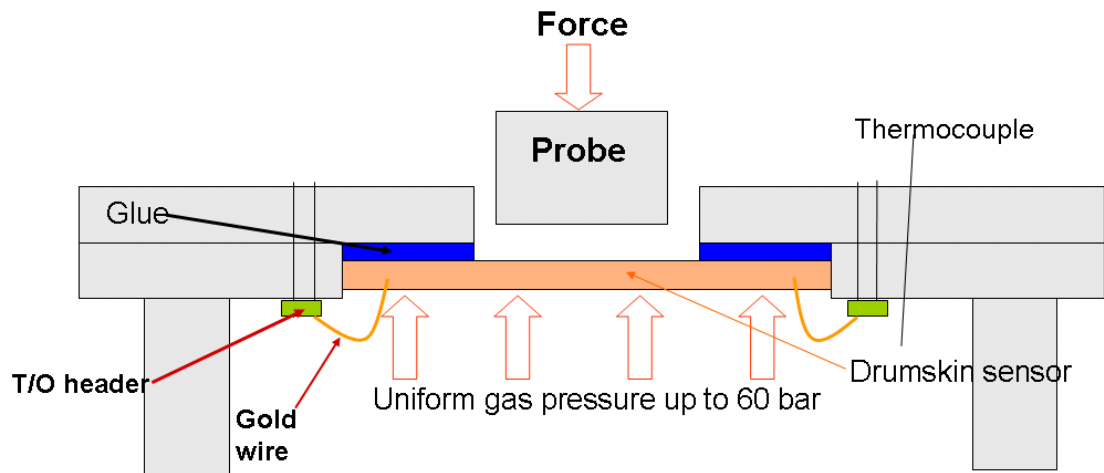


**Figure 7.14** Experimental response of the most sensitive sensing element (HEMT 3) with mechanically applied pressure

### 7.8.4 Addition of a Mechanical Probe

As discussed previously, a rapid pressure change can also lead to a temperature change in the chamber. One method to decouple pressure and temperature is to apply a mechanical load. In order to apply an additional mechanical pressure on the drumskin, a 3.5mm diameter mechanical probe was inserted on the other side of the sensor, outside of the pressure chamber. This means that it applies force onto the sapphire substrate. Previous measurements done using just the gas pressure system

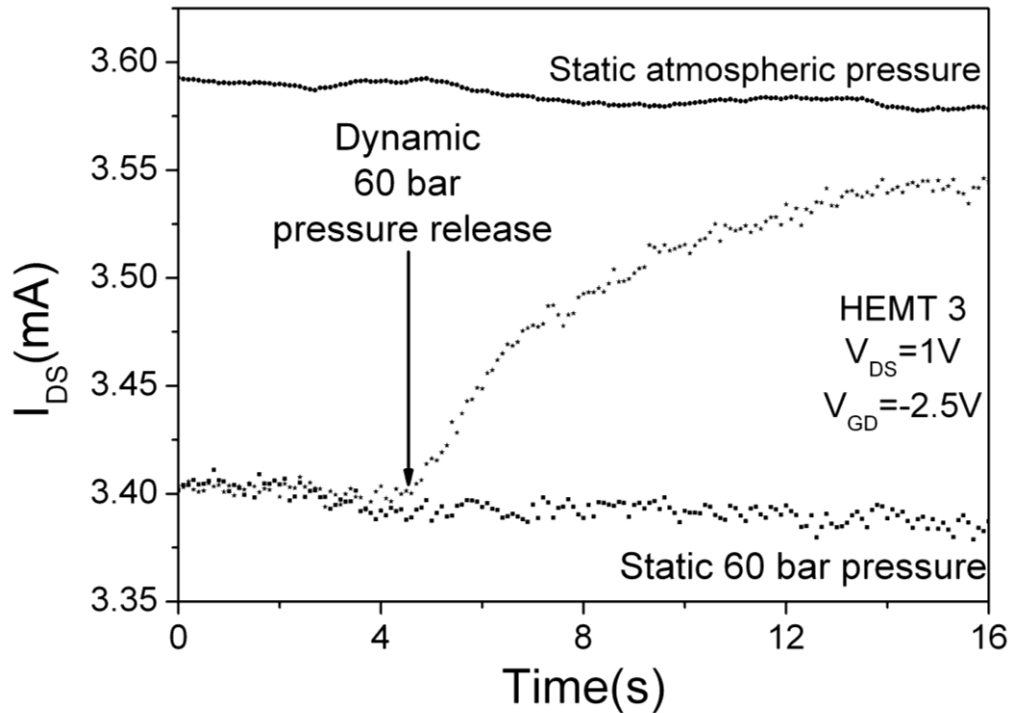
were affected by adiabatic heating, so measurements could only be taken hydrostatically once the temperature inside the pressure chamber had reached equilibrium with the surrounding environment. A schematic diagram of the experimental set up is shown in figure 7.15.



**Figure 7.15** Schematic diagram of pressure sensor test rig with the addition of the mechanical probe.

Time-resolved pulsed V-I measurements were recorded for central HEMT 3 at  $V_{DS} = 1V$  and  $V_{GD} = -2.5V$  at atmospheric pressure and for a mechanical pressure of 60N, which was approximately 60 bar according to calculations. As demonstrated in figure 7.16, an increase of pressure leads to a decrease of  $I_{DS}$ . A measurement of the mechanical pressure being removed from the sensor was also conducted to demonstrate the time-dependent behaviour of the sensor. The  $I_{DS}$  recovered to values similar to the static atmospheric pressure level. However, figure 7.16 shows that the sensor requires at least 16s to return to equilibrium. The slow recovery may be explained by the material used to fix the chip to the flange. The cyano-acrylate glue used to bond the chip to the flange is a relatively soft polymer material that has a damping/viscoelastic effect on the system, thus inducing a slow release of the chip curvature. In any practical application, this type of sensor requires a low compliance adhesive for sealant and to hold it in place, such as a glass or solder. Nevertheless, the results in figure 7.16 conclusively show that a pressure change causes a change in

current when  $V_{DS}$  remains constant because the mechanical probe measurements are free of adiabatic effects.



**Figure 7.16** Time dependence of the  $I_{DS}$  of HEMT 3 for  $V_{GD} = -2.5V$  and  $V_{DS} = 1V$  at atmospheric pressure, for 60 bar static pressure, and its change when the mechanical pressure is varied from 60 bar to atmospheric pressure.

## 7.9 Concluding Remarks

This chapter has described the process of design and manufacture for a GaN/sapphire membrane sensor from initial FE models to building a test rig, ultimately demonstrating a working sensor. After a concept for the sensor was devised, it was modelled using ANSYS FE software. The purpose of the FE modelling was to predict the piezoelectric/strain behaviour of the sensing membrane and to determine the optimal working conditions of the sensor. The results from the modelling fed through into the mask design of the sensor. The modelling was used to determine the optimal HEMT positions, where the strain was predicted to be high or of interest. HEMTs were placed in these positions in three sensor design variants

The second part of the chapter describes the high pressure and force testing of the sensor. A high pressure test rig, which later had a mechanical probe incorporated, was designed and built in order to test the sensor at pressures between 1 atm and 60 bars. After removing thermal effects from the pressure measurements, it was conclusively shown that the sensor worked as designed and the FE model offers good agreement. The strain measurements, made using a mechanical probe, show that the sensor responds dynamically to strain change, although the reaction time needs to be improved. Finally, it was found that the sensor is most sensitive near the current saturation region, just above channel off (see section 1.4). The mechanical probe measurements taken using optimised I-V characteristics showed that the membrane has good sensitivity despite the presence of a thick sapphire substrate.

### ***7.9.1 Comparison with other high temperature pressure sensors.***

At present, the GaN/sapphire sensor is at an early stage of development and the high temperature limit of this type of sensor has not been fully determined over the course of this PhD project. In the literature, there are more developed high temperature pressure sensing concepts, and they will be described in this sub-section concluding this chapter. A brief description of each type sensor is included in table 7.1.

**Table 7.1.** Brief information on alternative high temperature pressure sensors in the literature.

<b>Reference</b>	[194]	[195-199]	[200]	[201, 202]
<b>Sensing Material</b>	SOI	SiC	n-GaN/Al <sub>x</sub> Ga <sub>1-x</sub> N/n-GaN heterostructures	Boron-doped polycrystalline diamond on Si substrate
<b>Maximum Temperature</b>	600°C	600°C	280K	500°C
<b>Pressure Range</b>	0.5 to 25 psi 16 to 6000 psi	0 to 50 psi	0-500 MPa	0-0.07 Mpa
<b>Gauge Factor</b>	-	-	236 - 807	5 – 241
<b>Sensing Element</b>	Piezoresistive Wheatstone bridge	Piezoresistive Wheatstone bridge	HEMT	Piezoresistive Wheatstone bridge

The brief comparison of other sensors in table 7.1 shows that there are other high temperature pressure sensing concepts being developed around the world aimed at various applications. At present the sensors displayed in the table 7.1 are more developed and have more mature processes, as shown in table 7.2, so will try to determine the potential of a GaN pressure sensor in comparison to the others. What the data in tables 7.1 and 7.2 show is that it is possible to create a piezoresistive sensor that works at temperatures in the range of 500 to 600°C using SOI, SiC and Si/PD. SOI, SiC and Si/PD can all be used as GaN substrates, suggesting that an expensive sensor could be created combining GaN with one of these materials. GaN grown on sapphire is cheaper, particularly there is an available MOCVD reactor to grow the GaN. Firstly, it should be possible to create a high temperature GaN HEMT sensor using a Si/PD or SiC substrate if appropriate Ohmic contacts are developed. Secondly, the competing high temperature sensors are only piezoresistive and the advantage that GaN offers is that it is both piezoelectric and piezoresistive. Therefore, with further development and improvements to the test rig aimed at improving the response time of the sensor, it should be possible to create a GaN sensor that can be used both dynamically and statically with good degrees of sensitivity and high gauge factors. This would give GaN sensors a larger potential market, suggesting that they have a strong chance of becoming an industry standard.



Semiconductor	Bandgap (eV)	Electronic maximum operating temperature (°C)	Process maturity	Key technical issues and limitations
Si	1.1	150	Very high	<ul style="list-style-type: none"> <li>• Not suitable for aggressive environments</li> </ul>
SOI	1.1	300	High	<ul style="list-style-type: none"> <li>• Not suitable for aggressive environments</li> </ul>
GaAs	1.43	350	High	<ul style="list-style-type: none"> <li>• Contact stability at high temperatures</li> <li>• Not suitable for aggressive environments</li> </ul>
3C-SiC	2.39	600	Low	<ul style="list-style-type: none"> <li>• Not available as bulk material</li> </ul>
6H-SiC	3.02	700	Medium	<ul style="list-style-type: none"> <li>• Bulk material quality</li> <li>• Ohmic contacts to p-type material</li> </ul>
4H-SiC	3.26	750	Medium	<ul style="list-style-type: none"> <li>• Bulk material quality</li> <li>• Ohmic contacts to p-type material</li> </ul>
Group nitrides	III- 1.89 - 6.20**	>700	Very low	<ul style="list-style-type: none"> <li>• Material quality, reproducibility</li> <li>• Ohmic contacts</li> </ul>
Diamond	5.48	1100	Medium	<ul style="list-style-type: none"> <li>• n-type doping</li> <li>• Material quality (only polycrystalline material available)</li> </ul>

\*GaN

\*\*AlN

**Table 7.2** Table detailing the band gaps, maximum operating temperatures, technical issues and process maturity [202, 203]

A point of note is that a similar sensor to the GaN sapphire diaphragm has been developed and tested at low temperatures [200]. This work, together with other work in the literature and in this project suggests that GaN potentially has a very large thermal operating range if suitable Ohmic metallic contacts are developed. This also indicates that GaN sensors would be very valuable to the space industry where they need to survive the high launch temperatures and direct heating from the sun, as well as the extreme cold of space. Ultimately, the development of GaN sensors is still worth pursuing because the work shown in this thesis and the literature show that is possible to create working sensors from GaN and the main issue with the technology remains the Ohmic contacts and suitable substrates.

## **CHAPTER 8: PROJECT CONCLUSIONS AND FUTURE WORK.**

### **8.1 Thesis summary and overall conclusions from the project.**

This thesis has examined the issues related to the development of novel technologies for GaN applications. Chapter 1 contains a literature review detailing the current position of GaN sensor research and contains a list of the lattice, piezoelectric, thermal expansion and stiffness properties of the key materials used in this PhD. Chapter 2 describes the methods used in chapters 3 to 7 to analyse the Si/PD substrates and develop GaN sensors and sensing structures. The experimental conclusions from this project will be discussed in sub-sections 8.1.1 to 8.1.5.

#### ***8.1.1 Measurements of the elastic properties of GaN with respect to temperature***

GaN is a mechanically stable material at temperatures between 300 and 1000°C, demonstrating a very small decrease in elastic modulus. The modulus decrease between 25 and 600°C was approximately 2% when measured using both the DMTA and impulse excitation methods. Therefore these measurements support the idea that GaN is stiff enough to be used as the base material for high temperature sensors, with low modulus decay. These measurements, shown in chapter 5, are the first time that the modulus decrease of GaN has been measured using both DMTA and impulse excitation. The impulse excitation measurements continue to 1000°C, showing a total decay in modulus of 17 GPa or 7% from a starting temperature of 25°C. These results should prove useful for future high temperature GaN sensing research.

#### ***8.1.2 Development of a Si/PD substrate for use with GaN applications***

The novel development of (111) silicon/polycrystalline diamond (PD) substrates were a significant technical challenge, with excessive substrate bow hampering processing and leading to the eventual delamination of silicon from the PD. Numerous attempts at processing suitable substrates for GaN applications using lapping and HF etching methods failed, with the silicon device layer suffering from cracking and mechanical

failure. The finite element (FE) and analytical thermal stress modelling approaches developed in chapter 3 demonstrated the underlying mechanism causing these failures and was used to direct experimental work. The modelling demonstrated that improving the adhesion between the silicon and PD, and reducing the PD thickness would reduce the risk of delamination. The idea of reducing the PD thickness is counterintuitive because in that it actually increases the degree of bow, but analytical and FE models were proven accurate experimentally when comparing the model with micro-Raman stress and experimental bow measurements.

The delamination issues were mostly solved by one of the MORGaN project partners, Element Six, by improving the PD nucleation process and therefore the adhesion. The FE models also suggested that the bowing was less of an issue when the silicon layer is at a thickness of less than 2  $\mu\text{m}$ , but the material is highly stressed (60 to 80 MPa in model, the silicon layer stress found to be variable experimentally due to the large amounts of intrinsic stress in the PD). The improved nano-nucleation process developed by Element Six, which uses nanocrystalline diamond, also reduced the amount of damage done to the silicon device layer and meant that it was less liable to crack, hence improving the chances of processing a viable substrate.

Improved PD growth processes coupled with using an SOI wafer with a (100) handle, described in chapter 4, now means it is now possible to process a suitable Si/PD substrate through KOH etching the (100) Si handle. This process is far more reliable than the previous mechanical thinning attempts because the wafer requires little mechanical clamping. However, bowing problems remain and are difficult to control when the silicon is thin because the intrinsic stresses in the PD dominate. The next technical issues to solve on these substrates are to consistently produce flat wafers and to grow a layer of AlGaIn or InAlIn on top of the III-V nitride layer, to allow a HEMT to be fabricated from the material. A potential method for doing this is to strain engineer the PD grains for favourable stress profiles.

### ***8.1.3 ELOG templates for sensing applications***

It is possible to create free standing GaN MEMS structures using ELOG, and is a potentially new method for creating GaN sensors. Chapter 6 in this thesis describes the design and fabrication process used to create released ELOG templates, from the initial results from the double-dogleg and stripe design concepts to the beam and cantilever devices released from a common template. The final ELOG template is a hybrid of the initial double-dogleg and stripe designs, using the 60° growth principle from the double-dogleg design and the long central column from the stripe design concept. ELOG GaN growth can produce straight, consistent lines in excess of one millimetre and preferentially grows at 60° angles due to its hexagonal lattice structure. These principles were incorporated into the 2<sup>nd</sup> generation sensor template designs from which the cantilevers and beams were released.

Although this technology is in its early stages at present, it should be possible to create ELOG devices wide enough for a HEMT or resistor sensing element judging by the amount of lateral overgrowth achieved. However there are still many problems to overcome, such as growing a layer of AlGa<sub>N</sub> on the templates to create the heterojunction and depositing a thick enough metal mask to protect the ELOG cantilevers/beams from damage. The ELOG growth method also produces a large number of parasitic growths and an uneven topography. A potential solution for the uneven topography will be shown in sub-section 8.2.1, through a modification to the mask design. Depositing a ~10 nm layer of molybdenum under the SiN<sub>x</sub> mask could potentially prevent the parasitic growths that are a by-product of Ga diffusing through the SiN<sub>x</sub> mask. Ultimately, this work shows that creating small GaN sensors or energy harvesters could be possible using the ELOG technique, demonstrating proof of concept.

### ***8.1.4 GaN/sapphire diaphragm sensor***

When using a HEMT as a sensing element, it is possible to make a viable sensor out of a standard GaN/sapphire substrate. The 'drumskin' sensor, described in chapter 7,

has been shown to be sensitive to both changes in strain and temperature, with both perturbing the current along the source-drain channel. Therefore, it was necessary to separate these effects during measurements. These measurements showed that applying a pneumatic pressure and heat to the HEMT side of the sensor both caused a decrease in current. This issue was overcome by taking a static measurement of current once the pressure chamber reached thermal equilibrium with the surrounding environment. This meant that the sensor was piezoresistive, rather than piezoelectric, and potentially limiting sensitivity. An additional problem was the self-heating of the device resulting from the applied voltage between the source and drain, causing additional decreases  $I_{DS}$ . It was found that applying a large amount of negative bias on the gate not only minimised the self-heating, but improved device sensitivity. By using gated HEMTs as sensing elements, it is possible to create a piezoresistive GaN sensor with a ~10% change of current over 50 bar.

This demonstrates that GaN is a strain sensitive material and that a viable static sensor can be created using it as the base sensing material. The results in chapter 7 show that it was possible to create a novel working GaN-based sensor as part of this PhD project. The diaphragm sensor is not yet a complete product and continues to be an active research project. Sub-section 8.2.3 contains a discussion of the future research being undertaken on the sensor, with the aim of creating a mature sensing technology that can be used in industry.

### ***8.1.5 General outcomes of all experimental work in this PhD***

The work presented in this thesis demonstrates the potential GaN has in becoming the base material for the next generation of harsh environment devices. High temperature measurements of the elastic modulus of GaN have shown that it is mechanically stable at 500°C, with just a 2% decrease in elastic modulus from room temperature. GaN does indeed work well as a strain sensitive material, as shown by the diaphragm sensor in chapter 7. The work undertaken on the ELOG structures indicates that it could well be possible to create miniature sensing elements from good quality material that is relatively strain-free. Therefore, based on these conclusions, GaN does appear to be a very suitable material for harsh environment sensors.

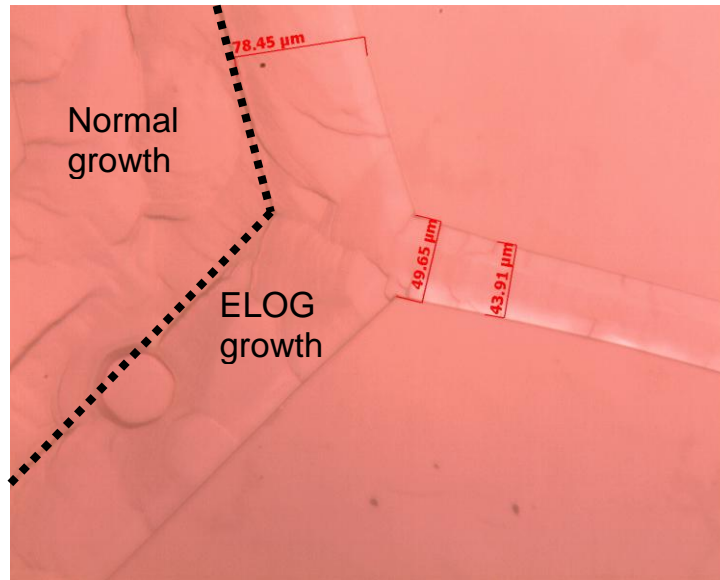
However, the measurements in chapter 7 show a serious issue with GaN/sapphire sensors in that their  $I_{DS}$  degrades with respect to temperature. Eventually this thermal degradation leads to situation where  $I_{DS}$  is zero above a certain temperature, a condition known as thermal breakdown. This issue is a particular issue with GaN/sapphire HEMTs because sapphire has a much lower thermal conductivity than PD. Chapters 3 and 4 detail the development of a Si/PD composite substrate on which it was possible to grow crack-free III-V nitride layers. The development of this substrate is potentially important to the advancement of semiconductor technology because it offers improved thermal conductivity, which should offer an improvement in GaN HEMT breakdown temperatures allowing the operation of GaN devices at higher temperatures. Ultimately, in the near future, the logical step is to fabricate a GaN HEMT diaphragm sensor on a Si/PD substrate. This sensor should offer the ideal combination of strain sensitivity, good mechanical properties and less thermal degradation of current.

## **8.2 Future Work**

### ***8.2.1 Third generation ELOG sensor templates***

Every ELOG template produced with the 2<sup>nd</sup> generation mask had similar undesirable topographical characteristics, with the centre of the contact pads region being much lower than the edge of the contact pads and the central bar. The probable reason for this is that the GaN growth in the centre of the contact pad region is sufficiently far from an edge to grow in a more typical epitaxial fashion. During ELOG growth, the material tends to congregate around the edge of a growth window. This eventually leads to the material growing outwards from the growth window, on top of the mask. Therefore less material is deposited on the centre of the window, causing the topographical features seen in chapter 6 (See figures 6.24 – 6.28 and 6.34). As the topographical features are undesirable, the ELOG and metallic contact masks require a redesign in order to reduce topographical variation. Reducing the amount of

topographical variation should simplify fabrication and in turn make the fabrication process more reliable.



**Figure 8.1** Optical image of an ELOG device template on sample 2848, showing 78.5  $\mu\text{m}$  ELOG growth region on the chevron or contact pad region.

The optical images of the ELOG structures, shown in figure 8.1, show a clear boundary between ELOG and normal GaN growth on the contact pads, as shown in figure 8.1. The ELOG growth region is nearly 80  $\mu\text{m}$  long on the template shown on figure 8.1, suggesting that the chevrons require a reduction in size. In order to achieve this, the contact pads were reduced in size from 100  $\mu\text{m}^2$  to 40  $\mu\text{m}^2$ . The gate contacts were discarded in this design in order to save space, despite being useful experimentally. It is still possible within this design to incorporate a gate into the sensor using electron beam lithography should these devices require the additional control that a gate brings. The removal of the gate and reduction in size of the contact pads mean that the electrical contacts of the cantilevers and beams have also been redesigned, as shown in figure 8.2. Figure 8.2 (b) shows a redesigned dual beam device with smaller contacts and contact pad chevrons. The smaller chevrons in figure 8.2 (b) should ensure the topographical variation is small, but could potentially be improved upon using the principles of ELOG growth on the chevrons. The grid has been designed in order to both minimise topographical variation and ensure that the

Ohmic metallisation remains in continuous contact with the device; this is important because the ELOG growth on the contact region will be unlikely to be fully coalesced. This design minimises topographic variation because there will be purely ELOG growth around the contact pad, keeping this area at about the same height as the central beam.



**Figure 8.2** Redesigned ELOG templates, contact pads and sensing elements. Where (a) is a dual cantilever device with ‘grid-structured’ contact pad areas and (b) is a dual beam device with reduced size contact pad regions.

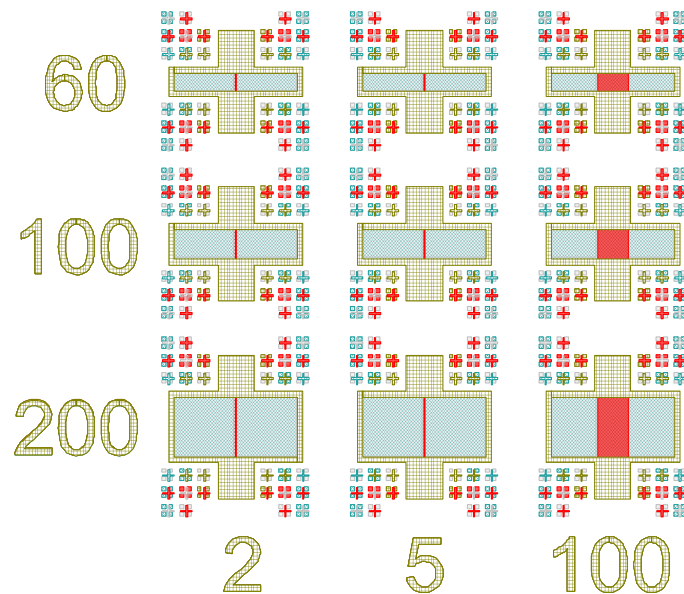
### 8.2.2 GaN HEMTs on Si/PD substrates

The mask set in figure 8.3 has been designed so that it can be used to create HEMTs on GaN on Si/PD substrates once the material is available. HEMTs grown and fabricated on a GaN on Si/PD substrate should look similar to the design in figure 8.3. The various mask layers of are denoted as follows with the mask layer number corresponding to the numbered bullet point.

- 1) The light blue crosshatched pattern is the MESA isolation, needed to prevent the HEMTs interacting with each other.
- 2) The grey layer corresponds to the deposition of Ohmic contacts; these contacts will be deposited by electron beam deposition.



- 3) The Schottky contacts are denoted by the red layer and will also be deposited by electron beam deposition.
- 4) The yellow square outlines correspond to a passivation layer. The passivation layer is a protective layer of an insulating material, such as SiO<sub>2</sub>, that is deposited by plasma enhanced chemical vapour deposition (PECVD). The purpose of the passivation layer is to stop current leakage.



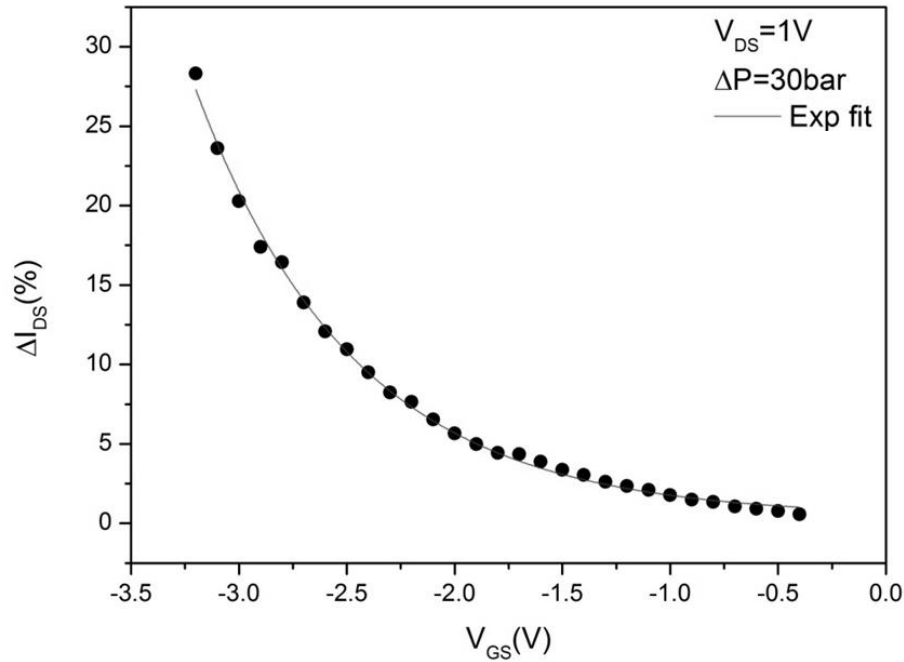
**Figure 8.3** The design of the mask set that can be used to fabricate HEMTs in GaN on Si/PD wafers.

Different sized HEMTs, with different gate lengths of 2, 5 and 100  $\mu\text{m}$ , have been included in this design in order to help determine the optimal HEMT design. The HEMT widths have also been varied and the widths tested will be 60, 100 and 200  $\mu\text{m}$ , in order to maximise the strength of the signal. The devices with the 100  $\mu\text{m}$  gate lengths are FATFETs, which can also be used for capacitive measurements if desired.

### *8.2.3. Diaphragm sensor*

The diaphragm continues to be an active research project, being worked on at the University of Bath and by research groups in Sweden, France, Slovakia and Germany who were also previously involved in the MORGaN project. This work includes maximising the percentage signal change caused by changing the pressure, designing packaging for the sensor and finding a material that acts as a good seal between the sensor and the packaging. Additionally, the Ohmic contact metallisation needs modification to ensure that the sensor has Ohmic characteristics at 500°C and this is required for a sensor that is genuinely suited to harsh environments. Some of the current effort is to find the regime for the maximum sensitivity of the sensor and some initial results are shown in figure 8.4. The result in figure 8.4 is being shown in this chapter rather than chapter 7 in order to demonstrate that the research into the GaN/sapphire drumskin sensor remains active and the outcome is potentially a viable sensor product that can be used industrially.

The sensor used for the experiment, the results of which are shown in figure 8.4, was sealed to the test flange with an epoxy rather than cyano-acrylate glue. Using epoxy improved the quality of the seal and improved the reliability of the experiments. The result shown in figure 8.4 shows that the central HEMT becomes more strain sensitive as more negative bias is applied on  $V_{GS}$ . An exponential increase in strain sensitivity is seen, confirming that the HEMT is most strain sensitive just above pinch off. The additional advantage of testing in this regime is that it also minimises self heating.



**Figure 8.4** Impact of changing the gate bias ( $V_{GS}$ ) has on the HEMT sensitivity for a pressure change from atmospheric pressure to 30 bar.

The next step with this sensor is to develop a version with high temperature Ohmic metallisation and test the sensor up to thermal breakdown in order to determine the maximum operating temperature of this type of sensor. Thermal breakdown is the minimum temperature where no current can flow between the source and drain because the 2DEG breaks down due to very low carrier density. Carrier density decreases with respect to temperature because the carriers, which are electrons if n-doped and holes if p-doped, are excited out of the 2DEG. The MORGAN project has targeted a minimum temperature limit for 400°C for this sensor and could be higher if a mature Si/PD substrate technology is used rather than sapphire.

In summary, future research should be concentrated on the following areas:

- i. Further development of the ELOG sensors and demonstrate its potential as a sensor through the fabrication of functional Ohmic contacts.
- ii. Demonstrate the high temperature capability of the drumskin sensor through the choice of packaging and metallisation.

- iii. Combine Si/PD technology with the ELOG and/or drumskin sensor to fabricate robust high temperature sensors.
- iv. Use Si/PD technology to enhance current high-power GaN devices.

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# Appendices

**Appendix 1: Meetings, conferences and publications**

**Appendix 2: Example ANSYS code used in chapters 3, 4 and 7**

## APPENDIX 1: MEETINGS, CONFERENCES AND PUBLICATIONS

Appendix 1 contains a list of the MORGaN project meetings and conferences attended, alongside related posters and publications. The list of MORGaN project meetings attended is as follows.

- M6 Progress meeting, Bath, 4<sup>th</sup> to 6<sup>th</sup> May 2009
- M12 Progress meeting, Aachen, 18<sup>th</sup> to 20<sup>th</sup> November 2009
- 1<sup>st</sup> MORGaN sensors meeting, London, 19<sup>th</sup> to 20<sup>th</sup> January 2010
- MORGaN summer school, Bratislava, May 2010
- M18 Progress meeting, Gothenburg, 28<sup>th</sup> to 30<sup>th</sup> June 2010
- M24 Progress meeting, Ulm, 15<sup>th</sup> to 17<sup>th</sup> November 2010
- 2<sup>nd</sup> MORGaN sensors meeting, London, 8<sup>th</sup> to 9<sup>th</sup> February 2011
- M30 Progress meeting, Vienna, 20<sup>th</sup> to 22<sup>nd</sup> June 2011
- M36 Final meeting, Paris, 21<sup>st</sup> October 2011

The following conferences were attended, where work contained in this thesis was presented.

- Dielectrics 2009, Reading, 15<sup>th</sup> April 2009 (Poster Presentation)
- De Beers Diamond conference, Warwick, 12<sup>th</sup> and 13<sup>th</sup> July 2010 (Poster Presentation)
- ASDAM 2010, Smolenice, Slovakia, 25<sup>th</sup> to 27<sup>th</sup> October 2010 (Oral Presentation)
- ICNS 2011, Glasgow, 10<sup>th</sup> to 15<sup>th</sup> July 2011 (Oral Presentation)

- The following publications have been submitted to peer-reviewed journals and conferences as part of this project.

A1.1: M. J. Edwards, C. R. Bowen, D. W. E. Allsopp and A. C. E. Dent, Modelling wafer bow in silicon–polycrystalline CVD diamond substrates for GaN-based devices, *J. Phys. D: Appl. Phys.* 43 (2010), 385502.

A1.2: M. J. Edwards, S. Vittoz, R. Amen, L. Rufer, P. Johander, C. R. Bowen and D. W. E. Allsopp, Modelling and optimisation of a sapphire/GaN-based diaphragm structure for pressure sensing in harsh environments, *Advanced Semiconductor Devices & Microsystems (ASDAM), 8th International Conference on*, (2010) p.127 to 130.

A1.3: M. J. Edwards, E. D. Le Boulbar, S. Vittoz, G. Vanko, K. Brinkfeldt, L. Rufer, P. Johander, T. Lalinský, C. R. Bowen and D. W. E. Allsopp, Pressure and temperature dependence of GaN/AlGaN High Electron Mobility Transistor based sensors on a sapphire membrane, *9<sup>th</sup> International Conference on Nitride Semiconductors* (2012), *Physica Status Solidi (c)*, DOI: 10.1022/pssc.20110371.

A1.4: Quanzhong Jiang, Michael J. Edwards, Philip A. Shields, Duncan W.E. Allsopp, Christopher R. Bowen, Wang N. Wang, Lajos Tóth, Bela Pécz, Rudolf Srnanek, Alexander Satka, and Jaroslav Kovac, Growth of Crack-free GaN Epitaxial Thin Films on Composite Si(111)/Polycrystalline Diamond Substrates by MOVPE, *9<sup>th</sup> International Conference on Nitride Semiconductors* (2012), *Physica Status Solidi (c)*, DOI: 10.1022/pssc.20110368.

A1.5: M.-L. Hicks, J. Tabcart, M. J. Edwards, E. D. Le Boulbar, D. W. E. Allsopp, C. R. Bowen and A. C. E. Dent, High Temperature Measurement of Elastic Moduli of Bulk (0001) Free-Standing Gallium Nitride, ISIF 2011 (2012), Integrated Ferroelectrics, DOI: 10.1080/10584587.

A 1.6: Mollart, T.P., Wilman, J.J., Dodson, J.M., Balmer, R.S., Edwards, M.J., Bowen, C.R., Allsop, D.W.E., Liu, C., Substrates for Semiconductor Devices. 2011, WO Patent WO/2011/161,190: United Kingdom.

A 1.7: Duncan W.E. Allsopp, Christopher R. Bowen, Michael J. Edwards, Quanzhong Jiang, Philip A. Shields, Sivapathasundaram Sivaraya, Wang N. Wang, Lajos Tóth and Bela Pécz, GaN-based Cantilevers Prepared by Efficient Epitaxial Lateral Overgrowth, Submitted to IEEE Device Letters March 2012

The following posters were presented at Dielectrics 2009 and the 61<sup>st</sup> De Beers Diamond conference 2010.

A 1.8: M. J. Edwards, C. R. Bowen, A. C. E. Dent and D. W. E. Allsopp, Modelling Silicon/Polycrystalline CVD Diamond Composite Substrates for use with GaN-based Devices, Presented at Dielectrics 2009, April 2009.

A1.9: M. J. Edwards, C. R. Bowen, A. C. E. Dent and D. W. E. Allsopp, Wafer bow and nanostructuring in composite silicon polycrystalline CVD diamond substrates. Presented at the 61<sup>st</sup> Diamond Conference, Warwick 12<sup>th</sup> and 13<sup>th</sup> July 2010

**A1.8:**

M. J. Edwards, C. R. Bowen, A. C. E. Dent and D. W. E. Allsopp, Modelling Silicon/Polycrystalline CVD Diamond Composite Substrates for use with GaN-based Devices, Presented at Dielectrics 2009, April 2009.

# Modelling Silicon/Polycrystalline CVD Diamond Composite Substrates for use with GaN-based Devices.

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## Aim

To develop and validate a finite element (FE) model that can be used to measure the bow of a silicon/polycrystalline CVD diamond wafers caused by the mismatch in the coefficients of thermal expansion (CTEs).

## Introduction

Polycrystalline CVD diamond has very high thermal conductivity and has a Young's modulus of about 1000 GPa, even at temperatures in excess of 1000° C. The lattice mismatch between polycrystalline diamond, silicon and GaN is small, meaning that the lattice dislocation density is small. Therefore, silicon/polycrystalline CVD diamond composites seem to be the ideal substrate material for use with GaN-based devices designed for use in extreme environments. However, there is a significant difference between the CTEs of polycrystalline diamond and silicon; this causes the wafer to bow significantly. A finite element model (FEM) has been designed to predict the wafer bow and how the bow changes as the thickness of silicon is reduced. An analytical method was also derived, with the purpose to validate the FEM and determine the radius of curvature of a wafer.

### Analytical Method

- In order to validate the FE model, an analytical technique for determining wafer bow needs to be derived.
- The derivation is in two parts, with the radius of curvature determined by work based on thermal stresses in multilayer systems, described in Hsueh<sup>1</sup>, and with the bow finally being derived using trigonometry.
- The three formulae that are needed to calculate the radius of curvature are:

$$c = \frac{(E_{33}t_3\alpha_3 + E_{22}t_2\alpha_2)\Delta T}{E_{33}t_3 + E_{22}t_2} \quad t_b = \frac{E_{22}t_2^2 - E_{33}t_3^2}{2(E_{22}t_2 + E_{33}t_3)} \quad r = \frac{E_{33}t_3^2(2t_2 + 3t_3) + E_{22}t_2^2(2t_3 - 3t_2)}{3[E_{33}t_3^2(c - \alpha_3\Delta T) - E_{22}t_2^2(c - \alpha_2\Delta T)]}$$

- Where  $c$  is the universal strain constant,  $t_i$  is the bending axis and  $r$  is the radius of curvature.
- The geometry of the system is shown in figure 1, where  $b$  is the bow,  $R_W$  is the radius of the wafer and  $r$  remains the radius of curvature.
- Due to triangle  $OAB$  being isosceles,  $\theta$  is exactly half the angle of curvature,  $\varphi$ .

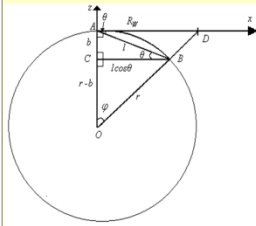


Figure 1: The geometry of the bow of a silicon/polycrystalline CVD diamond composite wafer.

- $l$  can be determined using the sine rule and it equals:

$$l = R_W \frac{\cos(3\theta)}{\cos(2\theta)} \quad \text{Where } \theta = \frac{R_W}{4r}$$

- The bow can now be determined using Pythagoras theorem and the quadratic formula, this gives:

$$b = -r - \sqrt{r^2 - R_W^2 \left( \frac{\cos\left(\frac{3R_W}{4r}\right)}{\cos\left(\frac{R_W}{2r}\right)} \right)^2 \cos^2\left(\frac{R_W}{4r}\right)}$$

- The small angles approximation for the bow is:

$$b = -r - \sqrt{r^2 - R_W^2}$$

<sup>1</sup>Reference: Hsueh, C. H. "Thermal stresses in elastic multilayer systems." Thin Solid Films, 2002: 182-188

## Results.

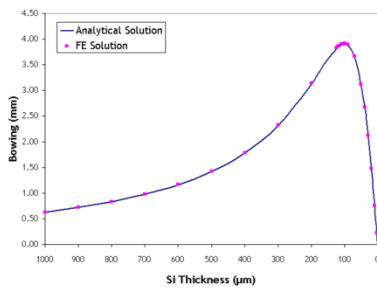


Figure 3: A graph comparing the results from the FE model with the analytical method, as the thickness of silicon is reduced from 1000 to 3 µm. The thickness of the polycrystalline CVD diamond layer is kept constant at 100 µm.

### Finite Element Analysis

- Model consists of a top layer of polycrystalline CVD diamond and a bottom layer of silicon orientated on the (111) crystallographic plane.
- Temperature dependent material properties, such as CTEs, Poisson's ratios and Young's moduli, can be programmed into the model; an advantage over the analytical method.
- Constructed and modelled ANSYS 11.0 with a 3D coupled field element type, SOLID 5. This element type was chosen because it can process thermal and piezoelectric behaviour.
- To save computational power and processing time, only one quarter of the substrate wafer was modelled with symmetry boundary conditions applied along the straight edges.
- The thickness of the polycrystalline diamond layer was kept constant at 100 µm, but the thickness of the silicon was varied between 1000 and 3 µm.

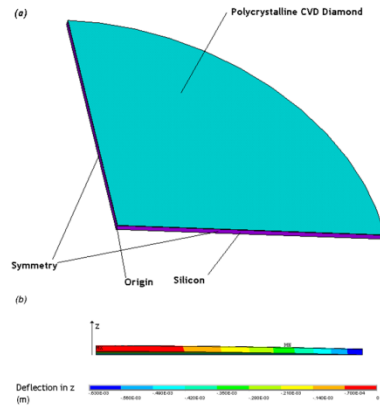


Figure 2: Images from the FE model of the silicon/polycrystalline CVD diamond wafer. (a) Schematic of the FE model from ANSYS. (b) ANSYS image demonstrating the bow of half a wafer, similar images to this are used to measure the wafer bow directly.

## Conclusions

- Very close agreement between the results of the finite element analysis and analytical method, as shown in Figure 3.
- This means that the analytical method has theoretically validated the FE model.
- The peak in wafer bow occurs near the point where the thicknesses of silicon and polycrystalline CVD diamond are almost equal.
- Experimental data is required to determine the accuracy of the theoretical results.
- This model can adapted for use with other materials, such as SiC and GaN.



Acknowledgement: This work has been funded by MORGAN, part of the European Commission's Framework 7.



**A1.9:**

M. J. Edwards, C. R. Bowen, A. C. E. Dent and D. W. E. Allsopp, Wafer bow and nanostructuring in composite silicon polycrystalline CVD diamond substrates. Presented at the 61<sup>st</sup> Diamond Conference, Warwick 12<sup>th</sup> and 13<sup>th</sup> July 2010

# Wafer bow and nanostructuring in composite silicon polycrystalline CVD diamond substrates.

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## Aim

To overcome the problem of excessive bow and high stresses in diamond on silicon composite (DOSC) wafers as the Si layer is thinned from 525  $\mu\text{m}$  to a target thickness  $<3 \mu\text{m}$ , so they can be used for GaN-based devices.

## Introduction

Polycrystalline CVD diamond has very high thermal conductivity and has a Young's modulus of about 1000 GPa, even at temperatures in excess of 1000° C. The lattice mismatch between polycrystalline diamond, silicon and GaN is small. Silicon and diamond have similar lattice structures and the lattice mismatch is low. Therefore, silicon/polycrystalline CVD diamond composites or diamond on silicon composites (DOSC) seem to be the ideal substrate material for use with GaN-based devices designed for use in extreme environments. However, there is a difference between the CTEs of polycrystalline diamond and silicon: causing the wafer to bow significantly. A finite element model (FEM) has been designed to predict the bow and stress distribution changes as the thickness of silicon is reduced. This information can be used to determine potential nanostructuring processes for overcoming problems associated with obtaining DOSC wafers compatible with GaN devices for harsh environments.

### Introduction to Finite Element Model

- Model consists of a top layer of polycrystalline CVD diamond and a bottom layer of silicon orientated on the (111) crystallographic plane.
- Temperature dependent material properties, such as CTEs, Poisson's ratios and Young's moduli, can be programmed into the model; an advantage over the analytical methods used to verify the model.
- Constructed and modelled ANSYS 11.0 with a 2D axisymmetric coupled field element type, PLANE 13. This element type was chosen because it can process thermally dependent stress/strain behaviour and axisymmetry reduces computation time without compromising accuracy.
- The thickness of the polycrystalline diamond layer was kept constant at 100  $\mu\text{m}$ , but the thickness of the silicon was varied between 1000 and 0.5  $\mu\text{m}$ .

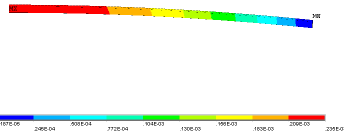


Figure 1: ANSYS image demonstrating the bow of half a wafer, similar images can be used to measure wafer bow

### Full Wafer Scans

- In order to determine the accuracy of the FE model, three near identical DOSC wafers were obtained from Element Six.
- The dimensions of the three wafers were:  $\Phi = 20\text{mm}$ ,  $t_{\text{Si}} = 525 \mu\text{m}$  and  $t_{\text{CVD}} = 80 \mu\text{m}$
- Each wafer was scanned using a SCANTRON PROSCAN 2000 profilometer and it measured bow across an entire wafer surface. Figure 1 contains the surface topography of a DOSC wafer scan.

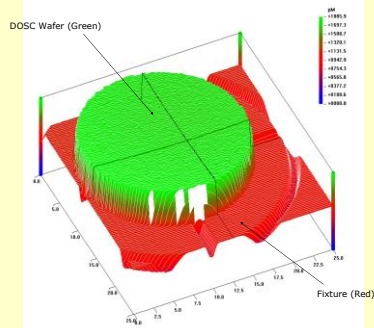


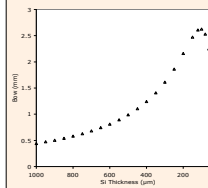
Figure 3: Profile scan of a  $\Phi = 20\text{mm}$  DOSC wafer using SCANTRON PROSCAN 2000 profilometer

- The bow of each wafer was determined using five line scans taken close to the wafer's centre, which were averaged and then compared with the prediction from the FE model

Sample	Measured Bow ( $\mu\text{m}$ )
FE Model (700 – 900°C growth temp)	33.1 – 39.3
Sample 1	42.1
Sample 2	52.9
Sample 3	56.2

- FE model slightly underestimates wafer bow, but the deviation is  $<20 \mu\text{m}$ 
  - Causes in of deviation experimental and FE wafer bow are lattice mismatch, grain boundaries and intrinsic stresses produced by the synthesis process
  - Lattice mismatch between diamond and silicon is small, resulting in low threading dislocation (TD) densities and explains why the deviation between experimental and FE bow measurements is relatively small

### FE Predictions of Wafer Bow



- Bow measurements taken for a 50 mm diameter DOSC wafer with a 100  $\mu\text{m}$  layer of polycrystalline diamond and (111) orientated Si
- Model predicts a peak in bow of 2.6 mm close to the point where the thicknesses of the two layers is equal (100  $\mu\text{m}$ )
- This bow is excessive and makes it impossible to process DOSC wafers without some form of clamping
- Clamping will increase stress on the wafer, increasing the risk of failure
  - Polishing Si down to desired thickness on a clamped wafer is a risky/impossible method, with Si failure highly likely

### Predicted Stress Profiles through clamped DOSC wafers

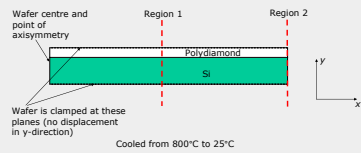


Figure 4: Schematic of clamped FE model of DOSC wafers

- In order to process the Si down to a suitable thickness for GaN applications, the wafer requires some form of clamping
- Stress profiles were measured in a region between centre and edge of the wafer (Region 1) and the edge of the wafer (Region 2)

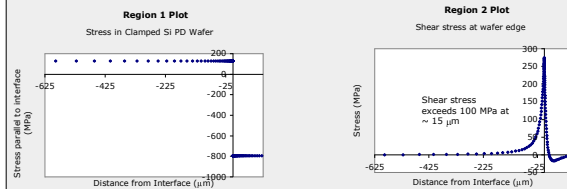


Figure 5: (a) Stress parallel to interface in Region 1. (b) Shear stress build up at interface of Region 2

- Large tensile stress in Si layer exceeds yield stress in Region 1
  - Potential cracking anywhere in Si layer
  - In reality, cracking risk mitigated by the formation of threading dislocations in Si, caused by lattice mismatch, during synthesis and grain boundaries in polycrystalline diamond.
- Shear stress exceeds yield stress of Si between the interface and a depth of 15  $\mu\text{m}$  in Si layer
  - Caused by CTE mismatch between Si and polycrystalline diamond.
  - Interfacial cracking and eventual delamination along the cleavage plane may occur at any point between these depths
  - May offer potential route to obtaining desirable Si thicknesses of  $<3 \mu\text{m}$ , and can be used as a substrate/heat sink for high temperature GaN-based devices

## Conclusions

- The peak in wafer bow occurs near the point where the thicknesses of silicon and polycrystalline CVD diamond are almost equal.
- FE model slightly underestimates wafer bow when the Si is thick
  - However, deviation is small and likely causes are lattice mismatch, intrinsic stresses induced in synthesis and grain boundaries in diamond
  - No experimental measurements of bow where Si is thinned to  $\sim$  diamond thickness, the predicted peak in the model
  - Accuracy of FE model helped by low TD densities caused relatively low lattice mismatch
- Clamping the wafer induces large tensile stresses in the Si layer and large shear stresses close to the interface
  - Wafer liable to crack in Si layer or delaminate close to the interface
  - Controlled delamination may be a method of obtaining desirable Si thicknesses of  $<3 \text{nm}$

Acknowledgement: The research leading to these results has received funding from the European Community's Seventh Framework Programme FP7/2007-2011 under grant agreement n°214610, project MORaGaN. This publication reflects only the author's views and that the Community is not liable for any use that may be made of the information contained therein. The Author would like to thank Element Six for their support in this work





## APPENDIX 2: EXAMPLE ANSYS CODE USED IN CHAPTERS 3, 4 AND 7

This appendix contains examples of the code used by the ANSYS FE model to predict the behaviour of Si/PD. The first set of code consists of the slave and master code used

The master code for the model is in figure A1.1 and was used to FE model the bow of Si/polycrystalline wafers. It consists of two parts, master and slave code; this was done to avoid having to re-input variables for each run of the model. The model was given the name “pl42\_si\_diamond\_bow” in ANSYS, a requirement in linking together the slave and master codes. The five variables substrate and film thicknesses, growth and room temperatures, and wafer radius are controlled by the master. These values are then inputted to the slave, which contains the working model and annotations.

```

! -----
! Parameters:
! - Arg1: Substrate thickness (thk)
! - Arg2: Film thickness (tf)
! - Arg3: Initial temperature (Ti)
! - Arg4: Room Temperature (Tr)
! - Arg5: Wafer Radius (rw)
! -----

*DO,x,125,525,50
  *USE,pl42_si_diamond_bow.txt,(x/1e6),2e-4,1073,298,5e-2
*ENDDO

*DO,x,170,220,10
  *USE,pl42_si_diamond_bow.txt,(x/1e6),2e-4,1073,298,5e-2
*ENDDO

*DO,x,10,100,10
  *USE,pl42_si_diamond_bow.txt,(x/1e6),2e-4,1073,298,5e-2
*ENDDO

*DO,x,125,525,50
  *USE,pl42_si_diamond_bow.txt,(x/1e6),1e-4,1073,298,5e-2
*ENDDO

*DO,x,10,120,10
  *USE,pl42_si_diamond_bow.txt,(x/1e6),0.25e-4,1073,298,5e-2
*ENDDO

*DO,x,10,120,10
  *USE,pl42_si_diamond_bow.txt,(x/1e6),0.75e-4,1073,298,5e-2
*ENDDO

*DO,x,10,120,10
  *USE,pl42_si_diamond_bow.txt,(x/1e6),0.5e-4,1073,298,5e-2
*ENDDO

*DO,x,10,120,10
  *USE,pl42_si_diamond_bow.txt,(x/1e6),0.5e-4,1073,298,5e-2
*ENDDO

*DO,x,10,120,10
  *USE,pl42_si_diamond_bow.txt,(x/1e6),0.75e-4,1073,298,5e-2
*ENDDO

*DO,x,10,120,10
  *USE,pl42_si_diamond_bow.txt,(x/1e6),0.75e-4,1073,298,5e-2
*ENDDO

*DO,x,10,120,10
  *USE,pl42_si_diamond_bow.txt,(x/1e6),0.25e-4,1073,298,5e-2
*ENDDO

*DO,x,10,120,10
  *USE,pl42_si_diamond_bow.txt,(x/1e6),0.25e-4,1073,298,5e-2
*ENDDO

```

```

*USE,pl42_si_diamond_bow.txt,(x/1e6),1e-      4,1073,298,5e-2
4,1073,298,5e-2                               *ENDDO

```

**Figure A2.1** Master code for the Si/polycrystalline diamond wafer bow model.

The slave code used for running this is contained in figure A2.2. This code contains all of the materials properties to allow ANSYS to produce an axisymmetric thermal stress model. The variables defined in the master have dummy values in the slave and these are used for debugging, as figure A2.2 shows. The slave builds the model, inputs the material properties, defines boundary conditions, adds (thermal) loads and solves the model. The element type used in this model is PLANE 42, chosen because it is the efficient type to solve thermal stress models. The output, or results, from the model are then appended to a spreadsheet for further analysis.

```

! *****
! Model details ...
! ...
! ...
! *****
! Version: 1.00
! Author: M.J. Edwards 2011, mje27@bath.ac.uk
! *****
! -----
! Parameters:
! - Arg1: Substrate thickness (thk)
! - Arg2: Film thickness (tf)
! - Arg3: Initial temperature (Ti)
! - Arg4: Room Temperature (Tr)
! - Arg5: Wafer Radius (rw)
! -----

! Start-up
FINISH                                ! Exits from previous work
*DEL,ALL                               ! Deletes previous variables/arrays
/CLEAR, START                          ! Clears current data and reads default start.ans
file
/FILNAME, WARIO, 1                      ! Job name (32char) and Job details
/TITLE, Temp Dep Axisym model
/STITLE,1,M. J. Edwards,2011
/UNITS, SI                              ! Model in SI units
SELTOL,1E-9                            ! Set small absolute tolerance for selection (xSEL) 1nm

! *****
! Display Options
! *****

/GRA,POWER

```

```

/GST,ON
/PLO,INFO,3
/GRO,CURL,ON
/CPLANE,1
/REPLOT,RESIZE
WPSTYLE,,,,,,,,0
!*
/XTRE,FILE,88,'ANSYS UoB background','bmp','\\rumba\homes\dos\My Pictures\'
/COLOR,PBAK,ON,-1,88
/REP
!*
/UDOC,1,TYPE,LEFT
!*
/REPLOT
/RGB,INDEX,100,100,100,0
/RGB,INDEX,80,80,80,13
/RGB,INDEX,60,60,60,14
/RGB,INDEX,0,0,0,15
/REPLOT
!/DEV,FONT,LEGEND,MENU
/dev,font,1,Arial,400,0,-16,0,0,,
/PLOPTS,INFO,3
/PLOPTS,LEG1,1
/PLOPTS,LEG2,1
/PLOPTS,LEG3,1
/PLOPTS,FRAME,0
/PLOPTS,TITLE,1
/PLOPTS,MINM,1
/PLOPTS,FILE,0
/PLOPTS,LOGO,0
/PLOPTS,WINS,1
/PLOPTS,WP,0
/PLOPTS,DATE,2
/TRIAD,OFF
/REPLOT
!*
/NUMBER,1                                ! Display numbered items by colour only
/PNUM,MAT,1                               ! Set numbered items to materials

! *****
! Enter pre-processor mode
! *****

/PREP7

/WINDOW,1,OFF                             ! Turn graphics window off while processing
/UIS,MSGPOP,3                             ! Turns Off note & warning messages
SHPP,OFF                                  ! Shape checking on (will produce warnings)

ET,1,PLANE42
!*
KEYOPT,1,1,0
KEYOPT,1,2,0
KEYOPT,1,3,1
KEYOPT,1,5,0
KEYOPT,1,6,0
EMUNIT,EPZRO,8.854E-12                   ! Set more accurate value for free-space
permittivity

```

```

! *****
! Variables
! *****

Ti=1173                !Initial Temp
Tr=298                 !Room Temp
thk=625E-6            !Substrate thickness
tf=1E-4               !Film thickness
rw=2.5e-2             !Wafer Radius

! If arguments have been passed, overwrite default parameters
*IF,arg1,GT,0,AND,arg1,LT,0.01,THEN
  thk = arg1 $ tf = arg2 $ Ti = arg3 $ Tr = arg4 $ rw = arg5
*ENDIF

! -----
! Material Properties
! -----

! *****
! Benchmarking
! *****

*GET,time_start,ACTIVE,0,TIME,WALL ! Start time for benchmarking
time = 0                          ! Stores current time and the benchmark time

!Properties of CVD Diamond

!*
MPTEMP,,,,,,,,        !Temperature Table
MPTEMP,1,83
MPTEMP,2,173
MPTEMP,3,273
MPTEMP,4,293
MPTEMP,5,298
MPTEMP,6,323
MPTEMP,7,373
MPTEMP,8,473
MPTEMP,9,573
MPTEMP,10,673
MPTEMP,11,773
MPTEMP,12,873
MPTEMP,13,973
MPTEMP,14,1073
MPTEMP,15,1173
MPTEMP,16,1273
MPTEMP,17,1323
MPDATA,EX,1,,1.076E+012 !Youngs Modulus
MPDATA,EX,1,,1.066E+012
MPDATA,EX,1,,1.057E+012
MPDATA,EX,1,,1.05E+012
MPDATA,EX,1,,1.05E+012
MPDATA,EX,1,,1.048E+012
MPDATA,EX,1,,1.042E+012
MPDATA,EX,1,,1.031E+012
MPDATA,EX,1,,1.021E+012
MPDATA,EX,1,,1.01E+012
MPDATA,EX,1,,1E+012
MPDATA,EX,1,,9.9E+011

```

MPDATA,EX,1,,9.8E+011  
 MPDATA,EX,1,,9.7E+011  
 MPDATA,EX,1,,9.6E+011  
 MPDATA,EX,1,,9.5E+011  
 MPDATA,EX,1,,9.43E+11  
 MPDATA,PRXY,1,,0.10 !Poisson Ratio  
 MPDATA,PRXY,1,,0.10  
 MPDATA,PRXY,1,,0.10  
 MPDATA,PRXY,1,,0.10  
 MPDATA,PRXY,1,,0.10  
 MPDATA,PRXY,1,,0.10  
 MPDATA,PRXY,1,,0.10  
 MPDATA,PRXY,1,,0.10  
 MPDATA,PRXY,1,,0.10  
 MPDATA,PRXY,1,,0.10  
 MPDATA,PRXY,1,,0.10  
 MPDATA,PRXY,1,,0.10  
 MPDATA,PRXY,1,,0.10  
 MPDATA,PRXY,1,,0.10  
 MPDATA,PRXY,1,,0.10  
 MPDATA,PRXY,1,,0.10  
 MPDATA,PRXY,1,,0.10  
 !\*  
 MPTEMP,,,,,,,,, !Temperature Table  
 MPTEMP,1,173  
 MPTEMP,2,273  
 MPTEMP,3,293  
 MPTEMP,4,298  
 MPTEMP,5,323  
 MPTEMP,6,373  
 MPTEMP,7,473  
 MPTEMP,8,573  
 MPTEMP,9,673  
 MPTEMP,10,773  
 MPTEMP,11,873  
 MPTEMP,12,973  
 MPTEMP,13,1073  
 MPTEMP,14,1173  
 MPTEMP,15,1273  
 MPTEMP,16,1323  
 UIMP,1,REFT,,Ti !Reference temp  
 MPDE,CTEX,1  
 MPDATA,CTEX,1,,0.37E-6 !CTEs  
 MPDATA,CTEX,1,,0.8E-6  
 MPDATA,CTEX,1,,1E-6  
 MPDATA,CTEX,1,,1E-6  
 MPDATA,CTEX,1,,1.4E-6  
 MPDATA,CTEX,1,,1.65E-6  
 MPDATA,CTEX,1,,2.3E-6  
 MPDATA,CTEX,1,,3.1E-6  
 MPDATA,CTEX,1,,3.65E-6  
 MPDATA,CTEX,1,,4E-6  
 MPDATA,CTEX,1,,4.3E-6  
 MPDATA,CTEX,1,,4.45E-6  
 MPDATA,CTEX,1,,4.6E-6  
 MPDATA,CTEX,1,,4.75E-6  
 MPDATA,CTEX,1,,4.9E-6  
 MPDATA,CTEX,1,,4.94E-6  
 !\*  
 MPTEMP,1,173 !Temperature Table

MPTEMP,2,273  
 MPTEMP,3,293  
 MPTEMP,4,298  
 MPTEMP,5,323  
 MPTEMP,6,373  
 MPTEMP,7,473  
 MPTEMP,8,573  
 MPTEMP,9,673  
 MPTEMP,10,773  
 MPTEMP,11,873  
 MPTEMP,12,973  
 MPTEMP,13,1073  
 MPTEMP,14,1173  
 MPTEMP,15,1273  
 MPTEMP,16,1323  
 MPDATA,KXX,1,,4500                   !Thermal conductivity  
 MPDATA,KXX,1,,2496  
 MPDATA,KXX,1,,2270  
 MPDATA,KXX,1,,2242  
 MPDATA,KXX,1,,2003  
 MPDATA,KXX,1,,1815  
 MPDATA,KXX,1,,1324.5  
 MPDATA,KXX,1,,1043.1  
 MPDATA,KXX,1,,853.8  
 MPDATA,KXX,1,,718.6  
 MPDATA,KXX,1,,617.6  
 MPDATA,KXX,1,,539.6  
 MPDATA,KXX,1,,477.7  
 MPDATA,KXX,1,,427.5  
 MPDATA,KXX,1,,386.1  
 MPDATA,KXX,1,,368.0  
 !\*

! Material Properties of (111) Si

FINISH  
 /PREP7  
 MPTEMP,,,,,,,,                   !Temperature Table  
 MPTEMP,1,100  
 MPTEMP,2,200  
 MPTEMP,3,280  
 MPTEMP,4,300  
 MPTEMP,5,400  
 MPTEMP,6,500  
 MPTEMP,7,600  
 MPTEMP,8,700  
 MPTEMP,9,800  
 MPTEMP,10,900  
 MPTEMP,11,1000  
 MPTEMP,12,1100  
 MPTEMP,13,1200  
 MPTEMP,14,1300  
 MPTEMP,15,1400  
 MPTEMP,16,1500  
 MPTEMP,17,1600  
 MPDATA,EX,2,,1.708E+11           !Young's Modulus  
 MPDATA,EX,2,,1.703E+011  
 MPDATA,EX,2,,1.696E+011  
 MPDATA,EX,2,,1.695E+011  
 MPDATA,EX,2,,1.685E+011

```

MPDATA,EX,2,,1.675E+011
MPDATA,EX,2,,1.665E+011
MPDATA,EX,2,,1.654E+011
MPDATA,EX,2,,1.644E+011
MPDATA,EX,2,,1.633E+011
MPDATA,EX,2,,1.622E+011
MPDATA,EX,2,,1.611E+011
MPDATA,EX,2,,1.601E+011
MPDATA,EX,2,,1.590E+011
MPDATA,EX,2,,1.579E+011
MPDATA,EX,2,,1.568E+011
MPDATA,EX,2,,1.557E+011
MPDATA,PRXY,2,,0.26          !Poisson Ratio
MPDATA,PRXY,2,,0.26
MPDATA,PRXY,2,,0.26
MPDATA,PRXY,2,,0.26
MPDATA,PRXY,2,,0.26
MPDATA,PRXY,2,,0.26
MPDATA,PRXY,2,,0.26
MPDATA,PRXY,2,,0.26
MPDATA,PRXY,2,,0.26
MPDATA,PRXY,2,,0.26
MPDATA,PRXY,2,,0.26
MPDATA,PRXY,2,,0.25
MPDATA,PRXY,2,,0.25
MPDATA,PRXY,2,,0.25
MPDATA,PRXY,2,,0.25
MPDATA,PRXY,2,,0.25
MPDATA,PRXY,2,,0.25
MPTEMP,,,,,,,,             !Temperature Table
MPTEMP,1,100
MPTEMP,2,200
MPTEMP,3,280
MPTEMP,4,300
MPTEMP,5,400
MPTEMP,6,500
MPTEMP,7,600
MPTEMP,8,700
MPTEMP,9,800
MPTEMP,10,900
MPTEMP,11,1000
MPTEMP,12,1100
MPTEMP,13,1200
MPTEMP,14,1300
MPTEMP,15,1400
MPTEMP,16,1500
MPTEMP,17,1600
UIMP,2,REFT,,Ti          ! Reference temp
MPDE,CTEX,2
MPDATA,CTEX,2,,-0.509E-6   ! CTEs
MPDATA,CTEX,2,,1.453E-6
MPDATA,CTEX,2,,2.392E-6
MPDATA,CTEX,2,,2.568E-6
MPDATA,CTEX,2,,3.212E-6
MPDATA,CTEX,2,,3.594E-6
MPDATA,CTEX,2,,3.831E-6
MPDATA,CTEX,2,,3.987E-6
MPDATA,CTEX,2,,4.099E-6
MPDATA,CTEX,2,,4.185E-6
MPDATA,CTEX,2,,4.264E-6

```

```

MPDATA,CTEX,2,,4.322E-6
MPDATA,CTEX,2,,4.380E-6
MPDATA,CTEX,2,,4.438E-6
MPDATA,CTEX,2,,4.496E-6
MPDATA,CTEX,2,,4.554E-6
MPDATA,CTEX,2,,4.612E-6
MPTEMP,,,,,,,,          !Temperature table
MPTEMP,1,100
MPTEMP,2,200
MPTEMP,3,300
MPTEMP,4,400
MPTEMP,5,500
MPTEMP,6,600
MPTEMP,7,700
MPTEMP,8,800
MPTEMP,9,900
MPTEMP,10,1000
MPTEMP,11,1100
MPTEMP,12,1200
MPTEMP,13,1300
MPTEMP,14,1400
MPTEMP,15,1500
MPTEMP,16,1600
MPDATA,KXX,2,,913          !Thermal conductivity
MPDATA,KXX,2,,266
MPDATA,KXX,2,,156
MPDATA,KXX,2,,105
MPDATA,KXX,2,,80
MPDATA,KXX,2,,64
MPDATA,KXX,2,,52
MPDATA,KXX,2,,43
MPDATA,KXX,2,,36
MPDATA,KXX,2,,31
MPDATA,KXX,2,,28
MPDATA,KXX,2,,26
MPDATA,KXX,2,,25
MPDATA,KXX,2,,24
MPDATA,KXX,2,,23
MPDATA,KXX,2,,22

! -----
! Define solid geometry
! -----

!*
RECTNG,0,rw,0,-thk,
RECTNG,0,rw,0,tf,
!*

! Assemble area units by glueing
BOPTN,KEEP,NO              ! Boolean ops delete original geometry (default)
! BTOL,smallno/2          ! Point distance tolerance for bool ops
!ASEL,ALL                 ! Select all areas
!AGLUE,ALL                ! Glue areas
NUMCMP,KP $ NUMCMP,LINE $ NUMCMP,AREA      ! Compress entity numbers
ALLSEL,ALL                ! Select all entities (effectively removes selection)

!Select materials for areas

```



```

ASEL,S,LOC,Y,(tf/2)           ! Select Substrate area and define as CVD Diamond
AATT,1,,1
ASEL,S,LOC,Y,-(thk/2)        ! Select Substrate area and define as Si
AATT,2,,1
ALLSEL,ALL                    ! Select all entities (effectively removes selection)

! Mesh the solid geometry
MSHKEY,2                      ! Mesh type: Mapped where possible, no smart size
!x-direction
LSEL,S,LOC,Y,0               ! Select interfacial lines
LESIZE,ALL,2e-5              ! Set coarser mesh size
ALLSEL,ALL                    ! Select all entities (effectively removes selection)
LSEL,S,LOC,Y,tf              ! Select top line
LESIZE,ALL,2e-5              ! Set coarser mesh size
ALLSEL,ALL                    ! Select all entities (effectively removes selection)
LSEL,S,LOC,Y,-thk            ! Select bottom line
LESIZE,ALL,2e-5              ! Set coarser mesh size
ALLSEL,ALL                    ! Select all entities (effectively removes selection)

!y-direction

LSEL,S,LOC,X,0               ! Select inside PD edge
LSEL,R,LOC,Y,0,tf
LESIZE,ALL,1.6E-6,,,0.003125
ALLSEL,ALL                    ! Select all entities (effectively removes selection)
LSEL,S,LOC,X,rw              ! Select outside PD edge
LSEL,R,LOC,Y,0,tf
LESIZE,ALL,1.6E-6,,,320
ALLSEL,ALL                    ! Select all entities (effectively removes selection)

LSEL,S,LOC,X,0
LSEL,R,LOC,Y,0,-thk          ! Select inside Si sub edge
LESIZE,ALL,(1E-5*(thk/6.25E-4)),,(2000*(thk/6.25E-4))
ALLSEL,ALL                    ! Select all entities (effectively removes selection)
LSEL,S,LOC,X,rw
LSEL,R,LOC,Y,0,-thk          ! Select outside Si sub edge
LESIZE,ALL,(1E-5*(thk/6.25E-4)),,(0.0005*(6.25E-4/thk))
ALLSEL,ALL                    ! Select all entities (effectively removes selection)

ASEL,S,LOC,Y,(tf/2)         ! Select Film area
AMESH,ALL                    ! Mesh all selected volumes
ALLSEL,ALL

ASEL,S,LOC,Y,-(thk/2)       ! Select Substrate area
AMESH,ALL                    ! Mesh all selected volumes
ALLSEL,ALL

NUMMRG,ALL,1E-10,,,
*SET,a,NODE(0,0,0)          ! Glue everything
! -----
! Apply loads and constraints
! -----

NSEL,S,LOC,X,rw              ! Select outer edge node
NSEL,R,LOC,Y,-thk           ! Re-select just bottom corner of outer edge
D,ALL,UY,0                  ! Constrain displacement in Y (clamped at edge)
ALLSEL,ALL                    ! Select all entities (effectively removes selection)

)

```

```

FINISH
/SOL

/NOPR                                ! Supress printout of command log

TREF,Tr

SOLVE
FINISH

/POST1
*SET,bow,(UY(a)*1E3)                 ! Calculate bow in millimetres

NSEL,S,LOC,Y,0,-1E-5
NSEL,R,LOC,X,1E-4,(rw-1E-4)         !Select nodes sufficiently far enough away from the free
edge
!*
NSORT,S,X
*GET,sxmax,SORT,,MAX                 !Get max and min stresses in the x-direction
*GET,sxmin,SORT,,MIN
NSORT,S,1
*GET,s1max,SORT,,MAX                 !Get max 1st principal stress

NSORT,S,3
*GET,s3min,SORT,,MIN                 !Get min 3rd principal stress

ALLSEL,ALL

NSEL,S,LOC,Y,0,-1E-5
NSORT,S,XY
*GET,sxmax,SORT,,MAX                 !Get max shear stress
*GET,sxmin,SORT,,MIN                 !Get min shear stress

ALLSEL,ALL

! -----
! Save input parameters and results
! -----
PARSAV,ALL,debug,parm                ! Save parameters for debugging use

*CFOPEN,si_diamond_bow_pl42thesis_20111123,csv,,APPEND           ! Append results to 'si
diamond bow' Control File

!Output results data for each iteration
*VWRITE,(rw*1000),(thk*1e6),(tf*1e6),Ti,Tr,(bow*1000),(sxmax/1e6),(sxmin/1e6),(s1max/1e6),(s3
min/1e6),(sxmax/1e6),(sxymin/1e6),
%0.3G, %0.4G, %0.4G, %0.4G, %0.4G, %0.4G, %0.6G, %0.6G, %0.6G, %0.6G, %0.6G, %0.6G

*CFCLOS                                ! Close results file

FINISH

! *****

! End of batch clean-up

/DELETE,,rst                          ! Delete file jobname.rst (solution results)
!/DELETE,,err                          ! Delete file jobname.err (error and warning log)

```

```

!/DELETE,,log                ! Delete file jobname.log (batch command log)

/GOPR                        ! Restore command line printout
FINISH                       ! Exit current Processor mode
/EOF                          ! End of File

```

```
! ~~~~~
```

**Figure A2.2** Slave code used to model the stresses and bowing behaviour of a Si/PD composite substrate.

The SOI removal used in chapter 4 works in a similar way, using the same element type, but its master has additional variables such as the amount of SiO<sub>2</sub> etched and the handle wafer thickness. The slave also uses the SiO<sub>2</sub> materials data in table 4.2.

Finally, the code used to model the drumskin sensor will be shown in figure A2.3 and this includes all the required materials properties to fulfil the piezoelectric constitutive relation shown in section 2.6.1. These materials properties are the stiffness of the material, the piezoelectric stress coefficients and the dielectric constants, as the model is temperature independent.

```

! *****
! Authors: P.F.Giddings en1pfg@bath.ac.uk
!          R. Amen      rafael.amen@swerea.se
!          S. Vittoz    stephane.vittoz@imag.fr
!          M.J.Edwards  m.j.edwards2@bath.ac.uk
! *****

! Start-up
FINISH                ! Exits from previous work
*DEL,ALL
/CLEAR,START         ! Clears current data and reads default start.ans
file
/FILNAME,GaN_Sapphire_Membrane ! Job name (32char) and Job details
/TITLE,GaN Pressure Sensor
/UNITS, SI

! *****
! Display Options
! *****

/GRA,POWER
/GST,ON
/PLO,INFO,3
/GRO,CURL,ON
/CPLANE,1
/REPLOT,RESIZE
WPSTYLE,,,,,,,,,0
!*
/TXTRE,FILE,88,'ANSYS UoB background','bmp','\\rumba\homes\dos\My Pictures\'
/COLOR,PBAK,ON,-1,88

```

```

/REP
!*
/UDOC,1,TYPE,LEFT
!*
/REPLOT
/RGB,INDEX,100,100,100,0
/RGB,INDEX,80,80,80,13
/RGB,INDEX,60,60,60,14
/RGB,INDEX,0,0,0,15
/REPLOT
!/DEV,FONT,LEGEND,MENU
/dev,font,1,Arial,400,0,-16,0,0,,
/PLOPTS,INFO,3
/PLOPTS,LEG1,1
/PLOPTS,LEG2,1
/PLOPTS,LEG3,1
/PLOPTS,FRAME,0
/PLOPTS,TITLE,1
/PLOPTS,MINM,1
/PLOPTS,FILE,0
/PLOPTS,LOGO,0
/PLOPTS,WINS,1
/PLOPTS,WP,0
/PLOPTS,DATE,2
/TRIAD,OFF
/REPLOT
!*
/NUMBER,1                                ! Display numbered items by colour only
/PNUM,MAT,1                              ! Set numbered items to materials

! *****
! Key Dimensions
! *****

rad=2E-3                                !Diaphragm radius
thk=0.4E-3                              !Sapphire thickness
wid=4E-5                                !GaN block half width
gan=15E-6                                !GaN thickness
a1=-90                                  !1st cylinder angle (in degrees)
a2=90                                    !2nd cylinder angle (in degrees)
frit = 350e-6                            !Radius of curvature of the glass frit
radx = 4e-3                              !Diaphragm outer radius
rads = 1e-3                              !Steel fixture outer radius
base = 2e-4                              !Base height
bar = 10
!d = rgf*sin(3.14159/4)  !Geometrical parameter. Needed for glass frit

! *****
! Enter pre-processor mode
! *****

/PREP7
SHPP,ON                                ! Shape checking will Warn on error limits & bad
meshing
ET,1,SOLID98,3
!BTOL, 1e-11

!-----
! Material 1: GaN

```

```

!-----
!*****
! Defines permittivity
!*****

MP,PERX,1,10.4      !Sets relative permittivity at constant strain
MP,PERY,1,10.4
MP,PERZ,1,9.5

!*****
! Defines compliance matrix
!*****

TB,ANEL,1,1,,0
tbtemp,0
TBDATA,1,390e9,145e9,106e9
TBDATA,7,390e9,106e9
TBDATA,12,398e9
TBDATA,16,122.5e9
TBDATA,19,105e9
TBDATA,21,105e9

!*****
! Defines piezoelectric 'e' matrix
!*****

!The initial script used the IEEE convention for the piezo matrix. ANSYS uses its own convention, as
follows:
!
! [c11 c12 c13 0 0 0]   [0 0 e13]   [ep11 0 0 ]
! [c12 c11 c13 0 0 0]   [0 0 e13]   [ 0 ep11 0 ]
! [c13 c13 c33 0 0 0]   [0 0 e33]   [ 0 0 ep33]
! [ 0 0 0 c66 0 0]     [0 0 0]
! [ 0 0 0 0 c44 0]     [0 e15 0]
! [ 0 0 0 0 0 c44]     [e15 0 0]

TB,PIEZ,1,,0
TBMODIF,1,1,0
TBMODIF,1,2,0
TBMODIF,1,3,-0.33
TBMODIF,2,1,0
TBMODIF,2,2,0
TBMODIF,2,3,-0.33
TBMODIF,3,1,0
TBMODIF,3,2,0
TBMODIF,3,3,0.66
TBMODIF,4,1,0
TBMODIF,4,2,0
TBMODIF,4,3,0
TBMODIF,5,1,0
TBMODIF,5,2,0.33
TBMODIF,5,3,0
TBMODIF,6,1,0.33
TBMODIF,6,2,0
TBMODIF,6,3,0

!-----

```

```

! Material 2: Sapphire
!-----

TB,ANEL,2,1,,0
tbtemp,0
TBDATA,1,495e9,171e9,130e9,20e9
TBDATA,7,390e9,130e9,-20e9
TBDATA,12,486e9
TBDATA,16,162e9
TBDATA,19,130e9,20e9
TBDATA,21,130e9

!MP,EX,2,365e9                !Sets linear isotropic

!-----
! Material 3: Glass Frit
!-----

MP,EX,3,4e9

!-----
! Material 4: Steel
!-----

      mp,ex,4,210e9
      mp,nuxy,4,0.3
      mp,dens,4,7900

! -----
! Glassfrit
! -----

!k, 1,0, (rad-frit), 0
!k, 2, -2, (rad-frit), -frit
!k, 3, 2, (rad-frit), -frit
!k, 4, 0, rad, 0
!k, 5, 0, 0, 1
!k, 6, 0, 0, -1

!lrotat,1,,,,,3,2,-45,1
!l, 1,4
!l, 4,7
!*get, gl_thk, kp, 7, loc, z

!al,1,2,3

!vdele,all,,,0
!allsel,all
!BTOL,1E-10

! -----
! Create model part 1
! -----

CYLIND,0,(rad-frit),thk,(thk+gan),a1,a2                !GaN

CYLIND,(rad-frit),rad,thk,(thk+gan),a1,a2                !GaN

CYLIND,rad,radx,thk,(thk+gan),a1,a2                !GaN

!*****

```

CYLIND,0,(rad-frit),0,thk,a1,a2 !Sapphire

CYLIND,(rad-frit),rad,0,thk,a1,a2 !Sapphire

CYLIND,rad,radx,0,thk,a1,a2 !Sapphire

!\*\*\*\*\*

CYLIND,(rad-frit),rad,0,-frit,a1,a2 !Frit

CYLIND,rad,radx,0,-frit,a1,a2 !Frit

CYLIND,radx,(radx+frit),0,-frit,a1,a2 !Frit

CYLIND,radx,(radx+frit),0,thk,a1,a2 !Frit

CYLIND,radx,(radx+frit),thk,(thk+gan),a1,a2 !Frit

!\*\*\*\*\*

!CYLIND,rad,radx,-frit,-base,a1,a2 !Steel

!CYLIND,radx,rads,-frit,-base,a1,a2 !Steel

!CYLIND,radx,rads,0,-frit,a1,a2 !Steel

!CYLIND,radx,rads,0,thk,a1,a2 !Steel

!CYLIND,radx,rads,thk,(thk+gan),a1,a2 !Steel

!\*\*\*\*\*

! -----  
! Glue together (It has to be done now, not later!)  
! -----

ALLSEL  
!nummrg,all,1e-10  
VGLUE,ALL ! GaN becomes V1 and sapphire V3(!?)

! -----  
! Assign Materials  
! -----

ALLSEL,ALL  
csys,1  
  
VSEL,S,LOC,Z,0,thk !  
VSEL,R,LOC,X,0,radx  
VATT,2 ! material 2 (Sapphire)  
ALLSEL,ALL

VSEL,S,LOC,Z,thk,(thk+gan) !  
VSEL,R,LOC,X,0,radx  
VATT,1 ! material 1 (GaN)  
ALLSEL,ALL

VSEL,S,LOC,Z,0,-frit !

```

!VSEL,R,LOC,X,(radx-frit),radx      ! Glass frit is assigned...
VATT,3
ALLSEL,ALL

VSEL,s,LOC,X,radx,(radx+frit)      ! Glass frit is assigned...
VATT,3
ALLSEL,ALL

!VSEL,S,LOC,Z,-frit,-base,          !Steel base assigned
!VSEL,A,LOC,X,radx,rads
!VATT,4

ALLSEL,ALL

! -----
! Mesh everything at a time
! -----

ALLSEL,ALL
SMRTSIZE,8                          ! Smart element size, 6 is default
MSHAPE,1,3D                          ! The smallest dimension of the model (here the GaN thickness) determines
VMESH,ALL                             ! the fineness of the meshing
ALLSEL,ALL

! -----
! Boundary conditions
! -----

ALLSEL,ALL
csys,0
ASEL,S,LOC,Y,-(radx+frit),(radx+frit)
ASEL,R,LOC,X,0
ASEL,R,LOC,Z,-base,(thk+gan)
NSLA,S,1
D,ALL,UX,0

ALLSEL,ALL
csys,1
!ASEL,S,LOC,X,rad
!ASEL,R,LOC,Y,a1,a2
!ASEL,R,LOC,Z,-thk,gan
!ASEL,S,LOC,Z,-base
ASEL,S,LOC,Z,-frit
NSLA,S,1
D,ALL,UX,0                          !Fix all displacement DOFs on every node of the lateral areas of half the
perimeter
D,ALL,UY,0                          !
D,ALL,Uz,0                          !
ALLSEL,ALL

csys,1
ASEL,S,LOC,X,(radx+frit)
ASEL,R,LOC,Y,a1,a2
NSLA,S,1
D,ALL,UX,0                          !Fix all displacement DOFs on every node of the lateral areas of half the
perimeter
D,ALL,UY,0                          !
D,ALL,Uz,0                          !

```



ALLSEL,ALL

! -----

! Apply pressure on surface A8, whereas all BCs are applied on nodes.

! This makes ANSYS issue a warning. Disregard it!

! -----

ALLSEL

csys,1

!NSEL,S,LOC,X,0,radx

!NSEL,S,LOC,Y,a1,a2

NSEL,S,LOC,Z,(thk+gan)

sf,, pres, -(bar\*1E5)

! The pressure is applied node by node, like we do for the

DOFs,

! so as to avoid warning messages

ALLSEL,ALL

!!

!Static analysis

! if linear analysis

! \_\_\_\_\_

/gopr

/solu

antype, static, new

kbc, 1

pstres, on

outres, all, all

eqslv, sparse

solve

finish

! The meshing is optimised (thanks to smartsizing). There are over 450000 eqs to solve. It takes 15-20 minutes on our machines.

! But for higher pressure, non linear analysis should be used, which results in hours-long analysis !!

/POST1

csys,0

NSEL,S,LOC,Z,thk,(thk+gan)

NSEL,R,LOC,Y,-wid,wid

ESLN,S,1

/OUTPUT,'Drumskin E-Field gan\_sapphire\_frit20110523','txt'

AVPRIN,0, ,

ETABLE, ,EF,X

AVPRIN,0, ,

ETABLE, ,EF,Y

AVPRIN,0, ,

ETABLE, ,EF,Z

AVPRIN,0, ,

ETABLE, ,CENT,X

AVPRIN,0, ,

ETABLE, ,CENT,Y

AVPRIN,0, ,

```
ETABLE, ,CENT,Z  
PRETAB,EFZ,CENTX,EFY,CENTY,EFX,CENTZ
```

```
/OUTPUT,TERM
```

```
FINISH
```

**Figure A2.3** Code used to model the stresses and piezoelectric behaviour of GaN/sapphire drumskin sensor.