A Minimum-Energy-Based Capacitor Voltage Balancing Control Strategy For MPC Conversion Systems

Mario Marchesoni
Universita' di Cagliari
Dipartimento di Ingegneria Elettrica ed Elettronica
Piazza d'Armi 09123
Cagliari-Italy
Tel: +39-070-6755885
Fax: +39-070-6755900
marcheso@diee.unica.it

Maurizio Mazzucchelli
Universita' di Genova
Dipartimento di Ingegneria Elettrica
Via all'Opera Pia 11a 16145
Genova-Italy
Tel: +39-010-3532714
Fax: +39-010-3532700
mm@die.unige.it

Francis V.P. Robinson
University of Bath
Dept of Electronic & Electrical Engineering
Bath BA2 7AY
UK
Tel: +44-(0)1225-323899
Fax: +44-(0)1225-826305
f.v.p.robinson@bath.ac.uk

Pierluigi Tenca
Universita' di Genova
Dipartimento di Ingegneria Elettrica
Via all'Opera Pia 11a 16145
Genova-Italy
Tel: +39-010-3532741
Fax: +39-010-3532700
tenca@die.unige.it

Abstract - **In AC/DC/AC power conversion, the connection of a Multi Point Clamped (MPC) rectifier with an MPC inverter simplifies the balancing of the voltages on the series-connected DC link capacitors as well as giving input power-factor correction capability. This is only true provided that an alternative balancing PWM control strategy is adopted instead of the standard PWM one. A control strategy is proposed which is based on the development of an energy function which may be minimized in real time by exploiting the existing redundancies in power-converter switching states. This strategy may be easily implemented in a DSP controller and is usable with any number of voltage levels and input/output phases. A validation has been performed by simulating a 5-levels 3-phase MPC system and significant waveforms are presented.**

I. INTRODUCTION

Multilevel converters have much to offer in the field of high-power conversion, especially in high-power motor drives and static var compensator applications. The multilevel conversion approach has several well known advantages. Namely, it gives waveforms with very low harmonic distortion at low switching-frequency operation; it allows high-power and high-voltage conversion using medium-power switches (e.g. IGBTs); and gives reduced electromagnetic interference when compared with two-level converters.

Three multilevel topologies are presently of most interest. These are the cascaded multilevel converter with separate DC sources [1]; the Multi Point Clamped (MPC) multilevel converter (known also as the diode clamped multilevel converter) [2]; and the flying capacitor multilevel converter [3]. For AC/DC/AC conversion, which is a common requirement in many high-power drives, the MPC topology is the best because it offers the easiest way to interconnect two AC ends [4] using a common capacitor bank. It also allows the number of input and ouput phases to be different. However, the proper use of this topology requires a correct balance of the DC-link capacitor voltages when non-zero real power is exchanged between the two AC ends.

It has previously been thought that capacitor voltage balance may be achieved with a class of loads which manage active power; particularly, high power AC drives [5]-[6]. That is to say, that the interconnection of an MPC rectifier and an MPC inverter would lead to a natural compensation of the capacitor-voltage unbalancing tendency which is otherwise observed (with opposite signs) when the inverter and rectifier are operated separately. But in the technical literature it has not been pointed out adequately that correct voltage sharing is really only possible when a suitable modulation strategy is adopted. In this paper, it will be shown that, when standard PWM modulation is used on both sides of the whole conversion system to convert a non-zero real power, voltage balance is not possible if different values of modulation index are adopted at the two AC ends. A fundamental requirement that every balancing strategy must satisfy, if balance is possible, will be presented. This requirement is a generalization of a similar one presented previously in [8]. It is that every balancing strategy must lead to equal average current in every couple of capacitor bank taps belonging to the same level.

Finally, a balancing control strategy that is valid for any number of voltage levels will be presented. The balancing technique proposed is based on using the redundancies in converter switching states that are allowed in the synthesis of line-to-line voltages, both on the line side and on the load side of the conversion system. The key idea of the balancing method is the representation of the unbalance phenomena in a suitable energy-based cost function so that an optimal control approach can be used to minimize the goal function and to achieve the correct capacitor voltage balance.

II. STANDARD PWM MODULATION IN AC/DC/AC MPC CONVERTER

To investigate the potential performance and the limitations of using separate standard PWM modulation strategies at the two ends of an MPC AC/DC/AC converter, a suitable model of these converters has been developed. The model allows the computation of the average current that flows into each capacitor and the quantities involved in it are shown in Fig. 1. To obtain a general result, which will be applicable to any standard PWM modulation type despite differing carrier waveform characteristics (mainly phasing) [7], the intermediate DC-link voltage V_{DC} (i.e. the total voltage measured between the two extremes of the capacitor bank) has been considered to be composed of the sum of an infinite number of uniformly distributed voltage levels, indexed by a real valued abscissa y whose origin is A. The average current of the capacitor at the abscissa y is given by the difference between the sum of all average currents injected by the line and the sum of all average currents drawn by the load, both computed between A and y,

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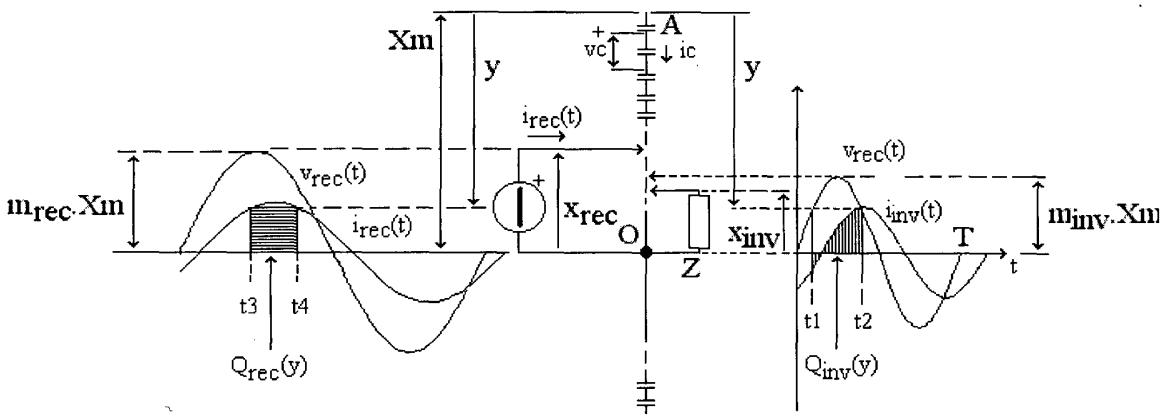

Fig. 1 – Generalized DC-link capacitor bank model

during the sliding of the phase taps imposed by the PWM strategy. In general, the frequencies of the waveforms can be different provided that their ratio is rational in order to ensure the periodicity of the phenomena under study. This assumption does not lead to a lack of generality because in practice any real frequency ratio is assumed to be close to a rational one. We have named T_{rec} the period of the waveforms at the left side of the converter and T_{inv} the period of the waveforms at the right side. Their ratio is $T_{rec} / T_{inv} = N / M$, with M, N non-zero natural numbers. The load at the right side of the converter is here assumed to comprise per-phase linear impedances of modulus Z and phase φ, but similar computations can be easily performed if the load is an electric motor that includes a voltage source in the equivalent circuit. The line current $i_{rec}(t)$ is assumed to have a displacement angle δ with respect to the corresponding synthesized voltage $v_{rec}(t)$ on the rectifier side. This angle depends on the desired displacement angle ψ between $i_{rec}(t)$ and the corresponding line voltage that is required to achieve power-factor correction of the converter. δ also depends on $i_{rec}(t)$ amplitude itself because of the series impedances on the line side of the converter. The amplitude of $i_{rec}(t)$ is consequently derived from the equivalence between the real power delivered to the load and that drawn from the mains supply. In this analysis the power losses in the whole system will be neglected. Both synthesized waveforms on the two sides of the converter can be pulse width modulated by independent modulation indexes m_{rec} and m_{inv}. With these assumptions, the analytical expression for the average capacitor current at the abscissa y, $I_{av}(y)$, due to one phase only, is given by (1). When (1) is computed with equal modulation indexes, it reduces to zero regardless of the frequency values confirming that when equal modulation indexes are used the capacitor voltage balance is possible for every load type. More interesting results are observed when m_{inv} is different from m_{rec}. Fig. 2 shows the plot of three times (1) when the following parameters are used: X_m = 20 m (by convention adopted); V_{DC} = 11.2 kV; Z = 0.6 Ω; m_{inv} = 0.4; $\varphi = \cos^{-1}(0.8)$ rad; m_{rec} = 1; ψ = 0 rad; T_{rec} = 0.02 s; M = 1; N = 1. With the three-phase load, this leads to a real load-power of 10MW. Fig. 2 clearly shows the diverging behaviour of the capacitor voltage because the capacitor's average current inside the [a,b] interval is negative and decreases their voltages.

$$I_{av}(y) = \begin{cases} 0 \\ \text{for } y \in S_o m_{rec} \\ \left(\dfrac{m_{inv}}{m_{rec}}\right)^2 \beta(m_{rec}) \\ \text{for } y \in S_i m_{rec} \end{cases} - \begin{cases} 0 \\ \text{for } y \in S_o m_{inv} \\ \beta(m_{inv}) \\ \text{for } y \in S_i m_{inv} \end{cases} \quad (1)$$

where

$$S_o m_{rec} = [y < (1 - m_{rec})X_m] \cup [y > (1 + m_{rec})X_m]$$
$$S_o m_{inv} = [y < (1 - m_{inv})X_m] \cup [y > (1 + m_{inv})X_m]$$
$$S_i m_{rec} = [y \geq (1 - m_{rec})X_m] \cap [y \leq (1 + m_{rec})X_m]$$
$$S_i m_{inv} = [y \geq (1 - m_{inv})X_m] \cap [y \leq (1 + m_{inv})X_m]$$

$$\beta(m) = \frac{V_{DC}\cos(\varphi)}{2\pi Z}\sqrt{\left(\frac{y}{X_m} - 1 + m\right)\left(1 + m - \frac{y}{X_m}\right)}$$

The capacitors experience opposite behaviour outside the [a,b] interval. From the analysis of (1) it is evident that, in practice, it is generally not possible to reach a perfect capacitor voltage balance with different modulation indexes at the two converter ends, using a simple standard PWM modulation scheme. Therefore, in general, more complex modulation strategies must be used to achieve voltage balance when $m_{rec} \neq m_{inv}$, even though this type of AC/DC/AC converter appears to have intrinsic balance capability at first glance. In the next sections the authors present a fundamental prerequisite that every balancing modulation strategy must satisfy provided balance is possible. Then an energy-based balancing strategy suitable for a wide range of load modulation-index values is presented.

III. PREREQUISITE FOR CAPACITOR VOLTAGE BALANCE

To deduce the necessary balancing condition it is useful to consider Fig. 3 which shows a generic AC/DC/AC MPC capacitor-bank with n (finite or infinite) capacitors. This

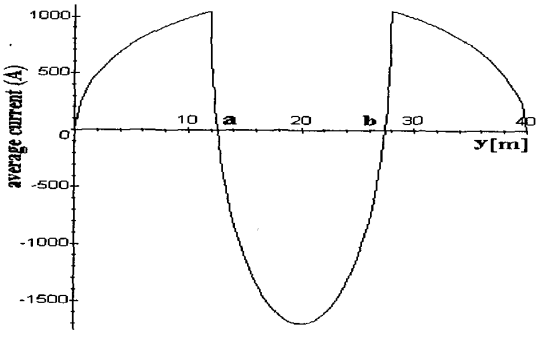

Fig. 2 The average capacitor current as a function of position in the DC-link capacitor chain

configuration has *2n+2* taps connected to the two sides of the DC-link. *n+1* of these taps are on to the mains side of the converter, the other *n*+1 taps are on the load side. Capacitors are connected between successive pairs of taps as shown in Fig.3. A prerequisite to be satisfied by every balancing modulation strategy is that the average tap currents, indicated with the symbol < >, must obey (2) when assumed to have the direction shown in Fig. 3

$$\langle i_j(r)\rangle = \langle i_j(i)\rangle \quad \forall j,\ j = 0..n \tag{2}$$

Proving this assertion is straightforward. To be sure that the capacitor voltages have reached a steady state, it is necessary that, first of all, these voltages remain bounded within some limits. This implies that the average current in every capacitor must be zero. Then by considering a group of *n* cutsets *S1..Sj..Sn,* where *Sj* contains the tap currents of both sides from i_j to i_n, and applying Kirchhoff's Current Law (KCL) to any of these cutsets with the current directions shown in Fig. 3, equation (3) is derived:

$$i_{cj} = \sum_{k=j}^{n} i_k(r) - \sum_{p=j}^{n} i_p(i) \tag{3}$$

Averaging both sides of (3) and imposing the above mentioned prerequisite, i.e. $< i_{cj} > = 0$, $\forall j$ gives (4)

$$\langle i_{cj}\rangle = \sum_{k=j}^{n} \langle i_k(r)\rangle - \sum_{p=j}^{n} \langle i_p(i)\rangle = 0 \tag{4}$$

Then for *Sn* and all subsequent cutsets:

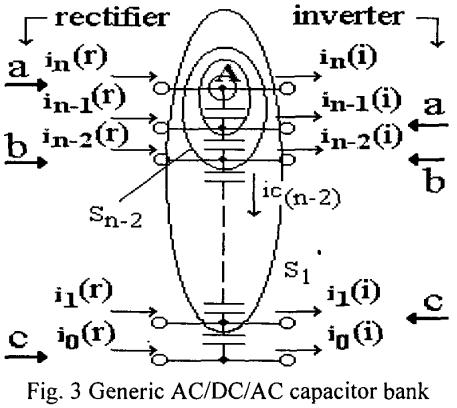

Fig. 3 Generic AC/DC/AC capacitor bank

$$\begin{cases} \langle i_n(r)\rangle = \langle i_n(i)\rangle \\ \langle i_{n-1}(r)\rangle = -\langle i_n(r)\rangle + \langle i_n(i)\rangle + \langle i_{n-1}(i)\rangle = \\ \qquad = \langle i_{n-1}(i)\rangle \\ \langle i_{n-2}(r)\rangle = -\langle i_n(r)\rangle - \langle i_{n-1}(r)\rangle + \langle i_n(i)\rangle + \\ \qquad + \langle i_{n-1}(i)\rangle + \langle i_{n-2}(i)\rangle = \\ \qquad = \langle i_{n-2}(i)\rangle \\ \vdots \\ \langle i_0(r)\rangle = -\langle i_n(r)\rangle + \ldots - \langle i_1(r)\rangle + \langle i_n(i)\rangle + \ldots \\ \qquad + \langle i_1(i)\rangle + \langle i_0(i)\rangle = \\ \qquad = \langle i_0(i)\rangle \end{cases} \tag{5}$$

Relationships developed in (5) validate the previous stated voltage balancing prerequisite With reference to Fig. 2, it is apparent that this is not satisfied by the standard PWM modulation strategy analyzed in the previous section, which does not exploit switching state redundancies in the synthesis of inverter and rectifier voltages.

IV. CAPACITOR BANK ENERGY CONSIDERATIONS

The previous results have shown that it is necessary to use a more complicated PWM modulation strategy, different from the standard one, in order to achieve the correct capacitor voltage balance when different modulation indexes are used at each side of the converter. The authors have developed a balancing strategy suitable for any number of levels which is easily implemented using a DSP controller. The idea in developing this balancing strategy has come from the observation that the total energy, E_b,of the *n*-capacitor capacitor-bank, expressed in (6), has a constrained minimum when all capacitor voltages are equal (provided capacitor- bank capacitors have the same capacitance). The equality constraint is that the sum of all capacitor voltages is equal to the desired DC value and can be expressed as in (7). In (6), C_j is the capacitance of the *j*-th capacitor and v_{cj} is its voltage.

$$E_b = \frac{1}{2}\sum_{j=1}^{n} C_j\, v_{cj}^2 \tag{6}$$

$$\sum_{j=1}^{n} v_{cj} - V_{DC} = 0 \tag{7}$$

In the following computation we assume equal capacitances (*C*) for all capacitors. This corresponds to the practical situation. To prove the previous prerequisite we substitute constraint (7) into (6) expressing v_{c1} as a function of the remaining *n-1* capacitor voltages. Doing so lowers by one the number of free variables and gives a new function (8) with which we search for an unconstrained minimum in the *n-1* dimensional real space. Vector $\mathbf{v}$ is defined as in (8).

$$\mathbf{v} = [\, v_{c2}, v_{c3}, v_{c4}, \cdots, v_{cn}\,]$$

$$f(\mathbf{v}) = \frac{1}{2}C\left(-\sum_{j=2}^{n} v_{cj} + Vdc\right)^2 + \frac{1}{2}C\sum_{p=2}^{n} v_{cp}^2 \tag{8}$$

Expanding (8) as in (9) leads easily to the gradient vector computation for the *f(v)* function. The first partial derivatives of (9) are given by (10).

$$f(\mathbf{v}) = \frac{C}{2}\left[\left(\sum_{j=2}^{n} v_{cj}\right)^2 - 2V_{DC}\sum_{k=2}^{n} v_{ck} + V_{DC}^2 + \sum_{p=2}^{n} v_{cp}^2\right] \quad (9)$$

$$\frac{\partial f(\mathbf{v})}{\partial v_{cj}} = C\left(\sum_{\substack{q=2 \\ q\neq j}}^{n} v_{cq} + 2\,v_{cj} - V_{DC}\right) \qquad \forall j,\ j = 2..n \quad (10)$$

By equating all partial derivatives given by (10) to zero and transferring the constant term $C\,V_{DC}$ to the right hand side of these equations, it is evident that all gradient elements must be equal to this same constant. It is therefore possible to write (11) which is valid for any γ and δ values belonging to the set {2..n}.

$$\sum_{\substack{q=2 \\ q\neq\gamma}}^{n} v_{cq} + 2\,v_{c\gamma} = \sum_{\substack{h=2 \\ h\neq\delta}}^{n} v_{ch} + 2\,v_{c\delta} \quad (11)$$

(11) reduces to (12), and then by using (10) equation (13) is obtained.

$$v_{c\delta} + 2\,v_{c\gamma} = v_{c\gamma} + 2\,v_{c\delta} \quad (12)$$

$$v_{c\delta} = v_{c\gamma} = V_{DC}/n \qquad \forall\,\delta,\gamma \in \{2..n\} \quad (13)$$

This proves that the only relative extrema is defined by equivalence among all capacitor voltages. The function *f(v)* is everywhere differentiable inside its domain (∇^n). This is also the only absolute extrema which is a minimum. Indeed, the Hessian of *f(v)* is the *n-1* by *n-1* matrix in (14).

$$\begin{bmatrix} 2 & 1 & 1 & \cdots & 1 \\ 1 & 2 & 1 & \cdots & 1 \\ 1 & 1 & 2 & \cdots & 1 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & 1 & 1 & \cdots & 2 \end{bmatrix} \quad (14)$$

Its *k*-th principal minors ($k \in \{1..n\text{-}1\}$) have positive determinants whose value is *k+1*. This satisfies the necessary and sufficient condition for the positive definitiveness of the matrix and verifies the minimum nature of the extrema found.

V. BALANCING STRATEGY

In the previous section the authors showed that the total energy of the capacitor bank as defined in (6) has a minimum with the total DC-link voltage constrained to assume a desired value. The minimum of this energy is expressed in (15), and the most interesting aspect is that E_b assumes $E_{b(min)}$ exactly when all capacitor voltages are equal during voltage balance.

$$E_{b(min)} = \frac{1}{2} C \frac{V_{DC}^2}{n} \quad (15)$$

This minimum energy aspect is of interest for use as a goal criterion for an optimal control strategy that tries to drive the MPC converter capacitor-bank towards the condition of minimum energy, thus achieving the desired voltage balance. But to deal with an easier control implementation it is better to have a positive definite goal function that has zero as an absolute minimum value, in order to implement a strategy that must only try to drive the function towards this value. If we perform a suitable variable substitution in (6), it is possible to write a new function with the same properties of (6) but with zero as an absolute minimum. This function which will be our control goal is stated in (16) where it should be noted that it is ultimately time-dependent. In (16) the positive scale factor ½*C* has been neglected because it does not affect the principle of the control strategy.

$$G(t) = \sum_{j=1}^{n}\left(v_{cj}(t) - \frac{V_{DC}}{n}\right)^2 \quad (16)$$

This goal function has a positive definite quadratic form that reduces to zero only at the point $v_{cj}(t) = V_{DC}/n$ for every value of index *j*. Its total time-derivative is given by (17).

$$\frac{dG(t)}{dt} = 2\cdot\sum_{j=1}^{n}\left(v_{cj}(t) - \frac{V_{DC}}{n}\right)\cdot\frac{d\,v_{cj}(t)}{dt} \quad (17)$$

The line-to-line synthesized voltages are constrained to be the difference between suitable standard PWM synthesized phase voltages, in order to preserve the desired harmonic contents in line-to-line voltages. The control strategy proposed tries to minimize (16) by choosing on-line one among a few redundant switching states which are able to give the required line-to-line voltages at the converter line side and at the load side. Minimization of (16) is achieved by choosing the switching state that gives the minimum value of derivative (17). When the operating conditions of the whole conversion system make possible the balance, the derivative (17) becomes negative for most of the time and consequently the goal function (16) converges towards its absolute minimum, i.e. the capacitor voltages converge towards a balanced state. Multiplying (16) and then (17) by a real positive constant does not alter the previous reasoning. For this reason it is useful to choose as a constant the capacitance *C* of the capacitor bank because this choice simplifies the computation of the derivative in (17), now scaled by *C*. Indeed by multiplying (17) by *C*, the last term in the summation argument becomes the current that flows in the *j*-th capacitor, as (18) shows. The value of current i_{cj} is strongly dependent on the couple of redundant switching configurations chosen and it constitutes the term that mainly differentiates the value of (5) among the different set of redundancies.

$$C\cdot\frac{dG(t)}{dt} = 2\cdot\sum_{j=1}^{n}\left(v_{cj}(t) - \frac{V_{DC}}{n}\right)\cdot i_{cj}(t) \quad (18)$$

To better explain this concept, it is useful to consider again Fig. 3 from which it is seen that the currents flowing in every capacitor are determined only by the non–zero tap currents included in the appropriate cutset for every capacitor. The non-zero tap currents are those of the load-side and mains-side movable taps included in the appropriate cutsets. Different choices among the possible pairs of

redundant switching states leads to different currents included in the cutsets and then different capacitor currents i_{cj}. From this reasoning it is also clear that number of sensors required to monitor all the electrical quantities to implement the control strategy in practice, is at a minimum and comprises n voltage sensors (one for every capacitor in the bank) and 4 current sensors. This is verified by thinking about the possibility to compute all i_{cj} currents only using the four independent phase currents (two at the load side and the other two at the mains side) and by applying KCL to all the S_j cutset. This computation can be easily performed by the DSP controller software which selects the optimum tap positions for the next sampling instant. Ideally the minimization of (18) should be made at every time instant but this is impossible from a practical point of view and also when considering only the sampling instants of the DSP controller. Indeed, the DSP sampling frequency can be much higher than the maximum switching frequency allowed by the high-power semiconductor technology used; mainly because this choice would lead to an unacceptably high number of commutations of the taps, which means an unacceptable fall in converter efficiency. For this reason the authors have made the important choice to search for the optimal redundant switching states that minimize (18) only when a change in any of the six synthesized phase-voltage levels is detected. The aforementioned DSP choice is theoretically profoundly different from the continuous-time implementation of the strategy, because it unavoidably shifts the control technique to a discrete-time basis evaluated. To test the devised balancing strategy, a dynamic model of a five-level MPC converter and the related control system has been developed using SIMULINK. The control system comprises an inner loop that ensures the four capacitor voltages balance and an outer loop that ensures the line-side power-factor is near unity. Figs. 4, 5, 6 and 7 show some simulation results computed with the following operating conditions:

- Four 10mF capacitors. Carrier frequency of 1050Hz.
- Three-phase load with star-connected impedance of $|Z|$= 2.21 Ω and displacement power factor of 0.99 at 50Hz.
- Three-phase mains with line resistance R_S = 1mΩ and line inductance L_S = 0.5mH.
- Mains line-voltages of 3990 V and 50 Hz.
- Desired total DC-link voltage of 8 kV.

Fig. 4 shows the transient behaviour and the steady-state balanced value (2 kV) of the four DC-link capacitor voltages, when the PFC controller starts with zero amplitude line currents. The PFC controller also injects a suitable third harmonic contribution into every rectifier phase-voltage to maximize the line-to-line voltage for a given DC-link voltage. For this reason the modulation index, that here is always referred to the phase voltages, can be greater than one; up to 1.15. The upper graph in Fig. 4 shows the results when a high modulation-index, m_{inv} = 1.1, is used at the load side and the lower one shows the results when m_{inv} = 0.8. It is worth noting that it is difficult to achieve the balance with high modulation indexes because there are less redundant switching states to exploit. The strategy has been tested with an almost purely resistive load because this is the worst type of load for capacitor voltage balancing, as confirmed by the analysis in section II.

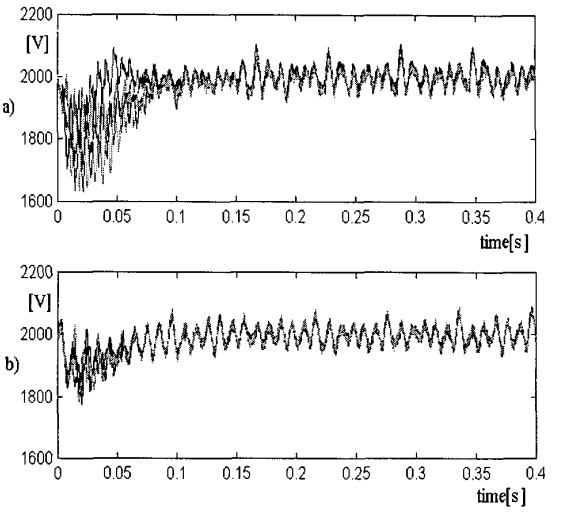

Fig. 4 The four DC-link capacitor voltages balanced by the strategy, a) with m_{inv}=1.1 , b) with m_{inv}=0.8

Some tests have been made and results are shown in Fig. 4. The converter control system also has power factor correction (PFC) capability, as illustrated in Fig.5 where *phase-a* voltage and current are displayed. To implement PFC, the controller takes information about the actual energy of the capacitor bank and compares it with the energy that the bank should possess in a balanced condition, in order to synthesize the opportune multi-level voltage at the converter line-side and to draw mains current with the correct amplitude and phase. Fig. 6 shows the derivative (18) in the two modulation-index cases plotted in Fig. 4. Graph (a) in Fig. 6 is (18) when m_{inv} is 1.1 and graph (b) is the time moving average of (a) defined as $M(t)$ in equation (19).

$$M(t) = \frac{1}{t}\int_0^t \left(2 \cdot \sum_{j=1}^{n} \left(v_{cj}(\tau) - \frac{V_{DC}}{n} \right) \cdot i_{cj}(\tau) \right) d\tau \qquad (19)$$

In the steady state, (19) converges for $t \rightarrow \infty$ to the constant average value of (18). It is evident from Fig. 6

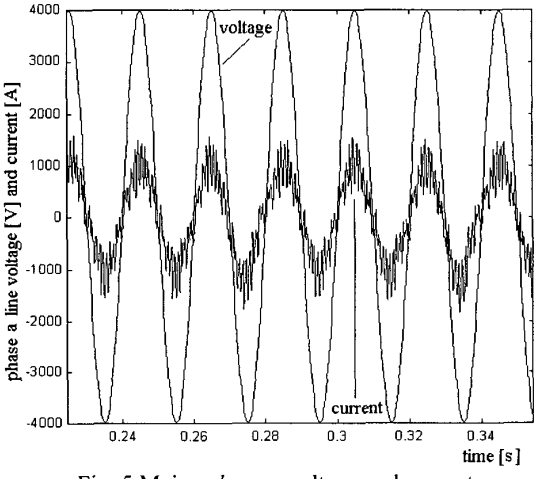

Fig. 5 Mains *phase-a* voltage and current

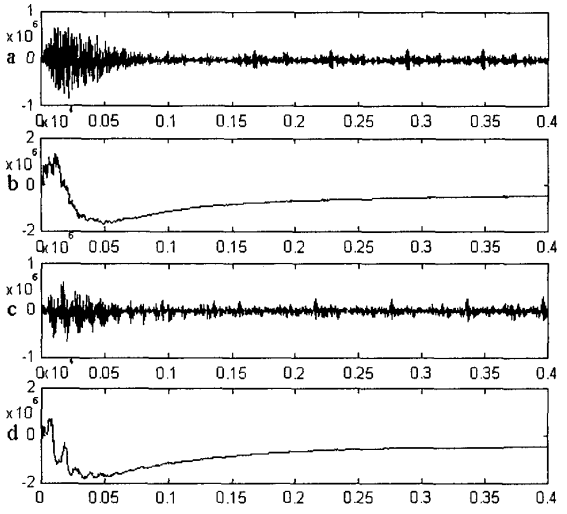

Fig. 6 Expression (18) together with its moving average for a,b) m_{inv} =1.1 and c,d) m_{inv} = 0.8 [V·A vs. s axis]

that, although the search for the negative minimum of (18) and consequently the satisfaction of the goal balancing function (16) is performed on a discrete time basis instead of a continuous one, the moving average value of (18) proves that the strategy is effective in achieving the capacitor voltage balance, especially as this applies at high modulation index values. Fig. 7 shows the V_{ab} line-to-line voltage applied to the load together with its absolute error from the ideal waveform, which is defined as: $V_{ab(real)}$-$V_{ab(ideal)}$. From Fig. 7 it is evident that the balancing strategy gives 3.75% maximum error in the line-to-line voltage, and this is achieved at high modulation index values. Fig. 8 shows the set of moving averages of the tap currents $i_j(r)$, $i_j(i)$ (excluding the lower ones); and from the graphs it is evident how the averages converge to the same values proving that the necessary condition expressed in section III is satisfied by this modulation strategy.

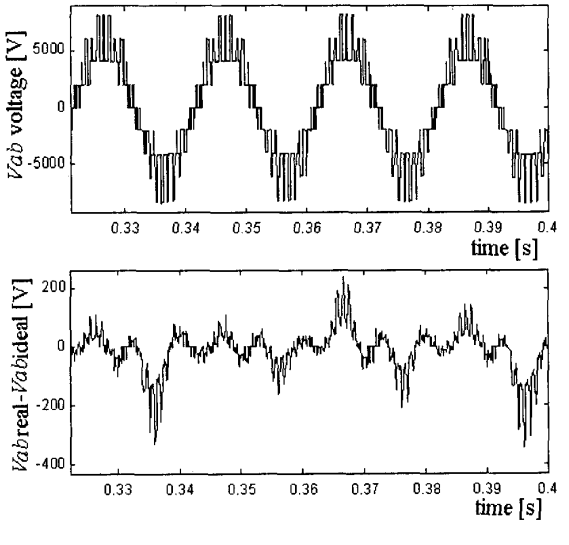

Fig. 7 V_{ab} line-to-line voltage and its error from the ideal.

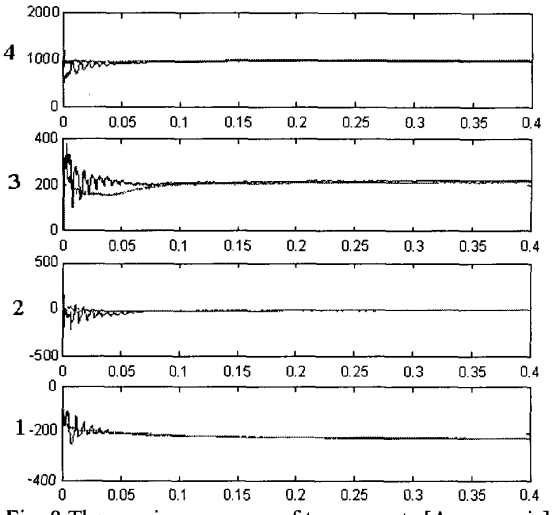

Fig. 8 The moving averages of tap currents [A vs. s axis]

VI. CONCLUSIONS

In this paper a modulation strategy for an AC/DC/AC MPC converter has been presented together with the proof that, as a rule, it is not possible to achieve DC-link capacitor-voltage balance using standard PWM modulation at both converter sides. The PWM strategy presented here is based on the representation of the unbalance problem in a goal function suitable for an on-line optimal control method which can be implemented using DSP controllers. The underlying principle of the strategy comes from a minimum energy property of the capacitors bank when a desired DC voltage is imposed. From simulation results it has been confirmed that the strategy gives good balancing even under worst-case conditions (high m_{inv} and resistive load) while preserving low load-voltage distortion.

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