

Citation for published version: Robinson, FV & Hamidi, V 2007, 'Series connecting devices for high-voltage power conversion' Paper presented at Universities Power Engineering Conference, 2007. UPEC 2007. 42nd International, 1/01/07, pp. 1134-1139. 42nd International Universities Power Engineering Conference.. https://doi.org/10.1109/UPEC.2007.4469110

DOI: 10.1109/UPEC.2007.4469110

Publication date: 2007

Document Version Early version, also known as pre-print

Link to publication

University of Bath

General rights

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

Take down policy If you believe that this document breaches copyright please contact us providing details, and we will remove access to the work immediately and investigate your claim.

SERIES CONNECTING DEVICES FOR HIGH-VOLTAGE POWER CONVERSION

F. V. Robinson and V. Hamidi

University of Bath, UK

ABSTRACT

Novel dynamic voltage-sharing schemes have been developed to allow any high-voltage power-semiconductor device, e.g. thyristor, IGCT, IGBT or power MOSFET, to be series-connected in strings, and switched as simply and rapidly in high-voltage applications as single devices. The circuits have many of the advantages of simply using RC or RCD snubbers, including being easily applicable to both low- and high-side switches. However, because the snubber capacitors are not fully discharged their associated reset current and power-losses are minimized. To illustrate the principle of operation experimentally, a string of three series-connected power MOSFETs switching 100A from 330 V has been used to obtain practical waveforms. The schemes are discussed and illustrated, using SPICE simulation results. The new, relatively simple voltage-sharing schemes are much easier to design and optimize than recently reported active gate-control and regenerative-snubber methods, allow very rapid turn-on and turn-off switching, and give composite-device switches a usable voltage rating similar to the aggregated voltage ratings of the string.

Keywords: voltage sharing, voltage balancing, series connected IGBT, series connected IGCT, series connection.

1 INTRODUCTION

A snubber scheme has been developed for controlling the switching voltage transients of individual devices, and providing dynamic voltage sharing within strings of series-connected power-semiconductors. It is intended for application in high-voltage chopper and inverter bridge-legs, in which series-connected devices are used as single switches. The circuit retains many of the advantages of simply using RC or RCD snubbers across each device in a string, and does not have the complexity, the requirement to modify gate drives, slower switching or other disadvantages of recently investigated active voltage-balancing methods.

With the new method, snubber capacitors are not completely discharged during operation, their associated reset current surge and power-losses are considerably reduced. Like RCD snubbers, the proposed scheme may be used with strings of any number of thyristor or transistor power device operated from a high-voltage DC supply and may be designed to accommodate significant differences in switching characteristics. Snubber circuit development is discussed and illustrated using simulation and experimental results. Experimental operation is investigated at 100A using series-connected power MOSFETs operating from a 330V supply.

2 PREVIOUSLY REPORTED METHODS

Previously reported experimental investigations have shown that modern power-semiconductor devices, such as IGCTs, IGBTs and power MOSFETs, may be series connected and operated synchronously as single switches in high-voltage chopper, inverter and pulsedpower applications [1-6], and series-connected devices are now being used in IGCT and IGBT applications [8] What makes possible direct series operation is the use of an effective voltage balancing scheme, which ensures that the composite switch voltage drop is evenly distributed between the devices in a string during blocking (static voltage balancing) and during switching (dynamic voltage balancing). Without enforced voltage balancing, repeated device breakdown within strings would almost certainly occur because of the variability in off-state leakage current and switching characteristics which arise in practical circuits; not only due to production spread in device characteristics, but also due to imperfect synchronisation of isolated drive signals, imbalance in common-mode voltage effects, and imperfect matching of the electrical and thermal impedances of device packages and other related hardware [2,3]. By using an effective voltage balancing scheme, compositedevice switches have been shown to have a usable voltage rating comparable to the aggregated voltage ratings of the string.

Voltage balancing is most easily provided by connecting voltage sharing resistors and RC snubbers across each device in a string as successfully applied for many decades in the thyristor strings that constitute the rectifier valves of HVDC-power-transmission converter stations. However, in high-voltage inverter, chopper, and pulsed power applications, it is usually important that devices be switched more rapidly to implement PWM control at carrier frequencies closer to 1 kHz than linefrequency, and to provide effective electronic over-With faster higher-frequency current protection. switching, the relatively high power-loss and resetcurrent transient of snubbers have a greater impact on converter efficiency and device utilisation than in thyristor circuits. In recent work on series device operation, a number of efficient innovative voltage-balancing schemes have been developed. Although, no single method outperforms all others in ease of implementation and minimising device switching-loss and -stress, there is some convergence towards using active voltage balancing with IGBTs [3-6] and using refined passive voltage balancing with IGCTs [1,2]. The active voltage balancing methods involve applying collector voltage feedback to the gate drive of each device, and thus prolonging or retriggering partial reconduction of individual devices to limit voltage drop during blocking, or to clamp voltage overshoot during the final stages of switching. Refined passive voltage balancing methods, developed for IGCTs, generally use RCD snubbers in which the capacitor is fully discharged regeneratively, or discharged to approximately V_{DC}/N where V_{DC} is the converter supply voltage and N the device-string length [1,2].

An important advantage of these schemes is their improved capability to provide voltage equalisation or clamping only when required, and to thus avoid the continuous power loss of conventional snubbers which are designed and operated as if worst-case conditions of device mismatch and high load-current are continually prevalent. Alternative voltage balancing schemes do, however, lack the ease of application and scalability of simple passive methods. Active voltage balancing, in particular, requires modification of gate-drive circuits to enable devices to respond to anode-cathode voltage feedback; and a greater optimisation and validation effort seems unavoidable if consistent device protection is to be assured despite variation in device characteristics and operating conditions, perhaps even after the future replacement of a failed device. It seems possible to overcome the disadvantages of active snubbing and still achieve efficient protection of any power semiconductor device using essentially passive voltage-balancing schemes. The new method proposed, essentially, comprises placing biased RCD-snubbers across each device in a series string. Snubber reset losses are minimal when snubber capacitors are biased at V_{DC}/N ; however, the method allows the bias level to be adjusted to any value between 0V and V_{DC} . The novelty of the method lies in the cellular nature of the snubber-capacitor discharge circuit which may be easily expanded to protect relatively long device strings. The proposed form of protection allows series-connected devices to be switched as rapidly as in conventional bridge-legs, without significantly increasing switching stress. The development of the scheme is first discussed and illustrated using circuit simulation results. The results of an

experimental evaluation of the method are then presented.



Figure 1 Chopper with biased RCD snubber.



Figure 2 Simulated turn-off switching waveforms.

3 BIASED RCD SNUBBER

A single-ended chopper comprising transistor (or gateturn-off thyristor) Q and diode D_{FW} may be connected to a DC supply and used as a switching regulator to control current in an inductive load, as shown in Fig. 1. However, even with careful layout, the parasitic inductance in loop C_{S} - D_{FW} -Q, the effect of which may be represented by L_S if D_{FW} is very close to Q, produces overshoot and high-frequency ringing in the transistor turnoff voltage waveform. A number of methods may be used to clamp the overshoot and suppress the resonance between $L_{\rm S}$ and the parasitic output capacitance of Q [7]. One with the lowest loss is a biased RCD snubber, comprising D_C , C_C and R_R in Fig.1. In this, the reset resistor is connected across D_{FW} rather than D_C , so that the capacitor remains charged at approximately V_{DC} during transistor conduction. To be effective, D_C and C_C must be placed very close to Q to provide a low inductance path to which transistor current can commutate to at turn off. L_S can then reset more slowly by resonating C_C above V_{DC} . R_R then discharges C_C back to V_{DC} . Circuit operation may be understood from the simulated turn-off switching waveforms shown in Fig. 2. Between t_1 and t_2 , transistor voltage, v_Q , rises to V_{DC} and D_C becomes forward biased. Transistor current, i_Q , commutates to D_C and C_C , i_{DC} . During t_3 and t_4 , L_S resets resonantly into C_C , increasing the capacitor voltage to a peak of ΔV above V_{DC} . As L_S is reset and its current i_{LS} falls to zero, current rises in the freewheel-diode at the same rate since i_{LS} and i_{FW} sum to zero at any instant. Because the bulk of the parasitic inductance, L_S , typically lies between C_S and D_{FW} -Q, the transfer of energy from L_S to C_C is completed before i_{RR} increases from zero and R_R discharges C_C to V_{DC} . In practice, a voltage transient occurs in v_Q at t_4 due to the reverse-recovery of D_C , and is relatively well damped if R_R is a lowinductance low-value resistor.

$$\frac{1}{2}L_{S}I_{O,MAX}^{2} = \frac{1}{2}C_{C}(\Delta V)^{2} = W$$
(1)

If idealised device switching and clamp diode operation are assumed, such that all the energy trapped in L_S is transferred to C_C and then all dissipated in R_R at Q turnoff, then Equation 1 may be used to estimate worst-case overshoot, ΔV , and resistor dissipation, W. Additional energy is dissipated for a brief period in R_R when Q is switched on; however, snubber efficiency may be compared using turn-off loss alone. Energies associated with resetting L_S using a conventional, fully discharging RCD snubber, and using active voltage clamping whereby the transistor is controlled to clamp at V_{DC} + $\Delta V_{\rm r}$, as if having repetitive avalanche capability, may be approximated in terms of the original trapped energy as in Table 1 [7]. From the normalised values, W_N , determined by assuming constant-current operation and 25% voltage overshoot, it is apparent that the biased RCD snubber is potentially a very efficient method of controlling the reset of unclamped series switch inductance. It should be noted that, in the case of the conventional snubber, the $V_{DC}/\Delta V$ term equates to $\frac{1}{2} C_C V_{DC}^2$, which unlike the others does not reduce with current and results in an even lower efficiency [7].

	Biased	Conventional	Active Voltage
	RCD	RCD Snubber	Clamp
W	$\frac{1}{2}L_{s}I_{o}^{2}$	$\left[1 + \left(\frac{V_{DC}}{\Delta V}\right)^2\right] \frac{1}{2} L_s I_o^2$	$\left[1 + \frac{V_{DC}}{\Delta V}\right] \frac{1}{2} L_S I_O^2$
W_N	1	17	15

Table 1 Normalised energy loss for ΔV at 25% of V_{DC}

4 SERIES-CONNECTED RCD SNUBBERS

4.1 Basic requirements

With series connected devices, equal voltage clamping and thus dynamic voltage sharing is dependent upon the capacitors being discharged to approximately equal voltage, V_{DC}/N (or as required), prior to synchronised transistor switching. Fig.3 shows, in principle, what is required. However, the circuit is impractical because of the need for multiple, matched, mostly floating discharge sources. A method of resetting snubber capacitors into one voltage rail is required to make the snubber scheme practical.



Figure 3 Impractical RCD scheme for series devices.

4.2 Practical scheme of biased series snubbers

Two practical cellular snubber schemes and simulated operating waveforms are shown in Figs. 4 to 7, in which C_1 to C_N are effectively discharged in parallel to the same source, which may be set to V_{DC}/N or a higher or lower value. In the Fig. 4 scheme, auxiliary switchable devices are required (represented with thyristor symbols), which have the same forward voltage-blocking capability as Q_1 to Q_N , but the reset-source voltage polarity required is likely to be available as part of the high-voltage DC supply system.

The need for auxiliary switches is avoided in the Fig. 6 self-commutating scheme; only auxiliary reset diodes are required. However, a purpose-built auxiliary reset source is required because of its polarity. In both schemes, the reset of snubber capacitors is performed when the composite switch turns on.

Simulated turn-off waveforms are shown in Figs. 5 and 7, for a three-device composite switch and freewheel diode, applied in a single-ended chopper, such as Fig.1, and protected by Fig. 4 and 6 snubber schemes. The chopper is assumed to be delivering a constant current to an inductive load. A relatively low DC supply voltage of 300 V is used to allow voltage overshoot features to be clearly seen. The waveforms are for synchronous, balanced operation of Q_1 to Q_3 . At turn off, just after 0μ s, individual transistor voltages, v_{O1} to v_{O3} rise above $V_{DC}/3$ and transistor currents commutate to D_{C1} to D_{C3} , and L_S resonates up the series-connected snubber capacitors, C_1 to C_3 , which were previously discharged to $V_{DC}/3$. As the reset of L_S completes i_{LS} falls to zero and v_{C1} to v_{C3} reach a peak overshoot value of $\Delta V/3$. Although the snubber capacitors remain charged above $V_{DC}/3$ until the transistors are next turned on, the transistor voltages fall back to $V_{DC}/3$ due to discharge of junction capacitance and clamp-diode reverse-recovery into the DC supply and static voltage sharing resistors which are used but omitted from the circuit for clarity.



Figure 4 Series RCD scheme with reset switches.



When Q_1 to Q_3 turn back on at 108µs, v_{O1} to v_{O3} fall, and load current commutates to them from the composite freewheel diode at a rate governed by L_S . Freewheel diode reverse-recovery is allowed to complete before S_1 to S_3 are switched (or D_{R1} to D_{R3} forward biased in Fig.6) to discharge C_1 to C_3 into V_{RST} , and back to $V_{DC}/3$, in readiness for the next composite-switch turn off. L_{RST} is added in series with the discharge path to control the rate-of-rise and peak value of reset current in S_1 to S_3 . The snubber reset currents in R_{R1} to R_{R3} are all approximately equal. However, reset currents accumulate as they cascade down through the reset switches, as evident from the reset current waveforms in Figs. 5 and 7. The duration of the reset period may be reduced at the expense of increased peak current by reducing R_{RI} to R_{R3} and L_{RST} values.



Figure 6 Series RCD scheme without switches.





Figure 8 Asymmetric switching waveforms for Fig.4.

In practice, differences in device characteristics, component values, discharge paths etc will cause asymmetry in the switching behaviour of devices within a string. However, device voltages are effectively clamped by the energy absorption capacity of the RCD snubber effect. For example, Fig.8 shows that the peak voltage arising across Q_2 and Q_3 (or Q_1) when the turn off (turn on) of Q_1 is delayed by 200ns in the string of three devices switching 100A.

5 EXPERIMENTAL RESULTS

The viability of both Fig.4 and 6 snubber schemes was proved experimentally using a string of three series connected power MOSFET modules switching 100A from a 330V supply. Static voltage-sharing resistors and small RC snubbers were added in the practical circuits. In the oscilloscope traces shown in Figs.9 to 14, turn on of the devices occurs first followed by turn off and the following scaling factors apply: voltage scale 25V/div, current scale 20A/div, time base 500ns/div. In Figs. 5, 7 and 8, turn off precedes turn on. A single current waveform corresponding to i_{LS} is shown, which first rises to 120A due to diode reverse recovery, because of the difficulty of measuring individual device currents within a circuit which has been highly integrated to minimise stray inductance. Figs.10 and 11 shows that Fig.6, the simpler self-commutating scheme provides just as satisfactory uniform voltage clamping effect as the more complex Fig.4 scheme. In both schemes, the initial voltage transient at device turn off, of a duration approximating to the power MOSFET current fall time, arises when device current commutates to D_{Cl} and C_{l} due to D_{Cl} forward recovery and D_{Cl} - C_l stray inductance.



Figure 9 Current and v_{Q1} , $v_{Q1}+v_{Q2}$ and $v_{Q1}+v_{Q2}+v_{Q3}$ waveforms for a practical implementation of Fig.4.

The following voltage rise, lasting less that 1µs, is controlled by the snubber capacitors. It is worth noting that the magnitude of voltage overshoot may be reduced by increasing the value of capacitor. However, because the capacitor charges and discharges to V_{DC}/N as shown in Fig.12, turn-off-associated snubber-reset loss remains relatively constant at about $1/2L_s I^2$. Snubber capacitor and L_s value determine the L_s reset time at turn-off and snubber capacitor reset time at turn-on. The composite capacitor-reset-current is shown in Fig.12, reaching 60A and lasting 3µs.



Figure 10 Current and individual v_{Q1} , v_{Q2} and v_{Q3} waveforms for a practical implementation of Fig.4.







Figure 12 Current v_{QI} , v_{CI} and i_{DI} waveforms for a practical implementation of Fig.6.

To confirm the tolerance of the snubber scheme to asymmetry in gate-drive and power-semiconductor switching transients, Q_1 was switched off 200ns before

 Q_2 and Q_3 in Fig.6. The resulting device voltage waveforms are shown in Fig.13. During the interval between Q_1 and Q_2,Q_3 switching off, D_{CI} and C_1 conduct the full load current and limit the voltage across Q_1 to below its rated value. It should be noted that 200ns has previously been used as a safe worst-case difference due to differences in the drive circuits and gate-drive circuits of 2.5kV, 1.8kA flat-packaged IGBTs [8]. Snubber capacitor value must therefore be chosen by anticipating the worst case difference in switching times. As previously noted a conservative design results in longer reset time, but not excessive reset power loss. Turn off conditions were the same as for Fig.8; however, cumulative device voltages are given there.



Figure 13 Current and v_{Q1} , v_{Q2} and v_{Q3} waveforms for Fig.6 with Q_1 turn off 200ns before Q2 and Q3.

In inverter-pole applications, similar voltage sharing action would be produced across the freewheel diodes which are connected in parallel with the switching devices, as shown in Figs. 4 and 6, when they turn off at the conclusion of reverse recovery.

CONCLUSIONS

Two dynamic voltage sharing schemes have been developed which may be use to protect any series connected power-semiconductor device. The schemes have the potential to give significantly less switching loss than active and simpler passive schemes provided that energy returned to the reset sources is regenerated to the main supply or otherwise used. Then, only energy trapped in unclamped inductance at turn off and diode recovery is dissipated. Both schemes may be made fully regenerative by removing resistance in the capacitor reset paths. Circuit operation has been investigated by circuit simulation and an experimental investigation. Results have been shown to be in good agreement.

REFERENCES

1. Roesner, R.; Holtz, J.; Kennel, R.; Cellular driver/snubber scheme for series connection of

IGCTs, IEEE Power Electronics Specialists Conference, 2001, PESC. 2001, Volume 2, Page(s):637 – 641, 17-21 June 2001.

- Ito, H.; Iwata, A.; Suzuki, A.; Novel low loss active voltage clamp circuit for series connection of GCT thyristors, IEEE Power Electronics Specialists Conference, PESC2002, Volume 2, Page(s):636 - 641, 23-27 June 2002.
- Raciti, A.; Belverde, G.; Galluzzo, A.; Greco, G.; Melito, M.; Musumeci, S.; Control of the switching transients of IGBT series strings by highperformance drive units, IEEE Transactions on Industrial Electronics, Volume 48, Issue 3, Page(s):482 – 490, June 2001.
- Soonwook Hong; Venkatesh Chitta; Torrey, D.A.; Series connection of IGBT's with active voltage balancing, IEEE Transactions on Industry Applications Volume 35, Issue 4, Page(s):917 – 923, July-Aug. 1999.
- Palmer, P.R.; Rajamani, H.S.; Active Voltage control of IGBTs for high power applications, IEEE Transactions on Power Electronics, Volume 19, Issue 4, Page(s):894 – 901, July 2004.
- Palmer, P.R.; Rajamani, H.S.; Dutton, N.; Experimental comparison of methods of employing IGBTs connected in series, Electric Power Applications, IEE Proceedings-Volume 151, Issue 5, Page(s):576 582, Sept. 2004.
- Robinson, F.V.P.; Williams, B.W.; Active-Snubbing Or Passive-Snubbing for Fast Switches?, IEEE Industrial Electronics Society, IECON '88. Proceedings., Volume 3, Page(s):617 – 622, October 1988.
- Fujii, K.; Kunomura, K.; Yoshida, K.; Suzuki, A.; Konishi, S.; Daiguji, M.; Baba, K.; STATCOM applying flat-packaged IGBTs connected in series, IEEE Transactions on Power Electronics, Volume 20, Issue 5, Page(s):1125 – 1132, Sept. 2005.

AUTHOR'S ADDRESS

The first author can be contacted at

Department of electronic & electrical engineering. University of Bath Claverton Road Bath United Kingdom email f.v.p.robinson@bath.ac.uk