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An Adaptive Sampling System for Sensor Nodes in Body Area Networks

Robert Rieger, *Senior Member, IEEE*, and John T. Taylor, *Member, IEEE*

***Abstract*—The importance of body sensor networks to monitor patients over a prolonged period of time has increased with an advance in home healthcare applications. Sensor nodes need to operate with very low-power consumption and under the constraint of limited memory capacity. Therefore, it is wasteful to digitize the sensor signal at a constant sample rate, given that the frequency contents of the signals vary with time. Adaptive sampling is established as a practical method to reduce the sample data volume. In this paper a low-power analog system is proposed, which adjusts the converter clock rate to perform a peak-picking algorithm on the second derivative of the input signal. The presented implementation does not require an analog-to-digital converter or a digital processor in the sample selection process. The criteria for selecting a suitable detection threshold are discussed, so that the maximum sampling error can be limited. A circuit level implementation is presented. Measured results exhibit a significant reduction in the average sample frequency and data rate of over 50% and 38%, respectively.**

***Index Terms*—Adaptive sampling, analog electronics, analog signal processing, bio-signal recording, sensor networks.**

I. INTRODUCTION

WITH increasing cost awareness in health care and a steadily ageing population ambulatory health monitoring has become important in modern medicine. Miniaturization of sensors and systems for the acquisition of body functions enables the interconnection of several sensors to form a network to collect and process data from different recording sites on the body. A typical network consists of a number of physiology and environment sensors such as electrocardiographs (ECG), pressure or motion sensors [1]–[4]. The top trace of Fig. 3 shows an example of an ECG after amplification, with its main features marked by letters P-T. The signals obtained by the sensors are transmitted to a base station or a central communication node [1]. In a system which records data over a prolonged period of time and that can be worn on the body, data rate and power consumption are critical design issues. Before the stages of storage and data transfer, the signal is converted from the analog to the digital domain. Generally, conversion at moderate speed and resolution is sufficient for this type of application and is readily provided by algorithmic analog-to-digital converters (ADC). Very low-power converters have recently become available [5], [6], which can help to reduce the overall power consumption of the recording system. Notably, the sample rate has a direct effect on the power consumption and size of the system blocks following the converter; lower data rates allow any digital postprocessing and transmission or storage stages to run at a lower speed, thereby conserving power. In addition, the area consumed by memory can be reduced. To decrease the data rate in long-term recording, various compression methods can be applied to the signal. Some methods require feature extraction, such as QRS peak detection, to achieve optimum performance [7]–[9]. Interpolation algorithms, such as *AZTEC* [10], *CORTES* [11], *SLOPE* [12], or *Fan* [13], have been developed specifically for ECG data compression. They are based on interpolation and a tolerance-comparison method, fitting additional data points around a sample using polynomials. A new sample point is stored only if the interpolated approximation exceeds a predetermined error level. Data compression is performed in the digital domain, after sampling the signal at a constant rate [14] or with a rate controlled by a digital processor [15]. Both implementations require a relatively fast digital processor for real-time data reduction. This adds to the overall power consumption and is not desirable in a wearable network sensor node [16], [17].

The proposed ADC clocking scheme operates the converter at minimum sampling frequency and increases the clock rate only during phases of high *curvature* (i.e., second derivative) of the signal, essentially performing a peak-picking algorithm on this derivative [18]. The system employs low-power analog circuits to set dynamically the required sample rate without involving the ADC or digital circuitry. While fully optimized sample timing using digital control may achieve higher compression ratio than an analog implementation, it should be noted that a *maximum* compression ratio is not essential in the sensor node. After the data has been transmitted to a less restricted central node, further processing and additional compression can be performed. If straight lines are used for curve fitting, it is observed that the error between the original and reconstructed signal is small as long as the slope (i.e., first derivative) of the input signal remains constant between any two sample points. Therefore, using the signal slope as an indicator to determine sample rate (as proposed in [20]) may not yield optimum performance in this type of system. However, during intervals of *varying* slope a potentially large error occurs between the reconstructed signal and the input waveform, as peaks become clipped. A preliminary version of this system was previously reported in [21], which differs from the one reported here. Previously, the first and second derivatives were used to detect *peaks* in the signal instead of *curvature*. The solution presented here is a more efficient approach for linear fitting and also

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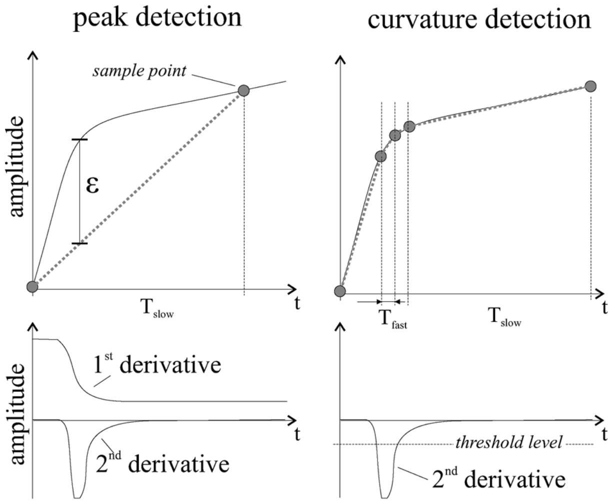

Fig. 1. Comparison of peak and curvature based sampling for an input signal with changing slope.

results in a simpler circuit implementation. Consider a segment of signal featuring an initial high slope followed by a less steep section. An example of such a curve is shown in Fig. 1. The signal does not contain a peak in the interval considered so that its first derivative never crosses the zero line. Hence, the sample rate remains low and a straight line interpolation leads to a relatively large error. This is in contrast with curvature based sampling also shown in Fig. 1. The second derivative of the signal yields a detectable amplitude spike in the curved signal region and the sample rate around this interval is increased from an initial (*slow*) rate to a second (*fast*) rate whenever the signal curvature exceeds a preset threshold. The error resulting from interpolation is significantly reduced compared to the peak-detection approach. The threshold determines the maximum sampling error as discussed in Section II, allowing a limit level to be set in order to achieve a given error rate. A comparison in terms of circuit complexity shows that peak and curvature detection both require two orders of derivation. However, a peak detecting system must evaluate both derivatives whereas the curvature based system only considers the second derivative. Consequently, the count of comparators comparing the derivatives with the threshold level is halved in the latter approach. Also, a higher degree-of-freedom is allowed when only the second-order derivative has to be implemented. In principle, any structure can be used, e.g., also an active filter in which the first derivative is not explicitly accessible. Overall, sampling quality and circuit simplicity suggest a system using curvature detection. Section III describes a circuit realization for the required analog control front-end using standard components and reports measured results. The discussion in Section IV is followed by conclusions in Section V.

II. SYSTEM DESCRIPTION

A. Principle of Operation

The proposed clocking system is examined first using the ECG as a typical body sensor signal. The concept is generally applicable to signals containing periods of low curvature interspersed with periods of high activity. Examples with other types of signal are described in Section II-C.

It is clear that an increased oversampling rate is required around the signal peaks to prevent their clipping. Fewer samples may be taken elsewhere while still preserving sharp edges in the sampled signal [22]. Clearly, the sampling error increases with higher peak amplitudes, higher signal frequency and lower sampling rate. The potentially largest error ε results from clipping a signal with maximum amplitude V_p and maximum frequency ω_m. Spectral decomposition yields the cosine wave as describing this extreme case. In general, sampling error ε is the amplitude difference between the signal peak V_p and its amplitude V_{in} at the sample instant t_s

$$\varepsilon(t) = V_p - V_{\text{in}}(t_s). \tag{1}$$

For a small sample interval Δt around the signal peak, the cosine is approximated by its Taylor expansion, truncated after the second term

$$V_{\text{in}}(t) = V_p \left(1 - \frac{\omega_m^2 t^2}{2} + \text{higher order terms}\right). \tag{2}$$

Using this approximation in (1) yields

$$\varepsilon(\Delta t \to 0) \approx V_p - V_p \left(1 - \frac{\omega_m^2 t^2}{2}\right) = V_p \frac{\omega_m^2 t^2}{2}. \tag{3}$$

The second derivative of (2) is given by

$$\frac{\delta^2 V_{\text{in}}}{\delta t^2} \approx -V_p \omega_m^2 \tag{4}$$

which is used in (3) to write

$$\varepsilon(t) \approx -\frac{\delta^2 V_{\text{in}}}{\delta t^2} \cdot \frac{t^2}{2}. \tag{5}$$

From (1) it is clear that the maximum error $\varepsilon_{\max}$ occurs when $t = +/-\Delta t/2$. Dropping the minus sign in (5) results in

$$\varepsilon_{\max} \approx \frac{\delta^2 V_{\text{in}}}{\delta t^2} \cdot \frac{(\Delta t)^2}{8}. \tag{6}$$

Since $\varepsilon_{\max}$ decreases as the sample frequency increases, (6) can be used to generate a metric to set the sampling rate which limits the sampling error to a preset maximum, i.e., to set a variable frequency clock generator [20]. However, in the proposed implementation only two distinct frequencies are used to simplify the implementation of the circuit (optimum values for these frequencies are discussed in Section IV). Initially, the signal is sampled at the lower frequency. Only if the evaluation of (6) indicates that the predicted error exceeds a predetermined level the higher sample clock is used.

To reconstruct the sampled signal, the current sample spacing is recorded in addition to the signal amplitude as follows. The higher speed clock is used as a time base, each cycle incrementing a digital counter. Reading the counter at the start of a new conversion yields the present sample spacing if the counter is subsequently reset to zero. Therefore, the maximum counter reading n is given as the ratio between the respective frequencies of the fast and slow clock

$$n \leq \frac{f_{\text{fast}}}{f_{\text{slow}}} - 1. \tag{7}$$

The effect of storing this timing information on the overall memory requirement is discussed in Section III.

B. Circuit Implementation

In general, the derivative of a sinusoidal signal is expressed in the frequency domain as multiplication by angular frequency ω and the operator j

$$\frac{d^2}{dt^2}V \rightarrow V \cdot (j\omega)^2 = -V\omega^2 \tag{8}$$

which is a function providing 180° phase shift and a gain proportional to ω^2. It can thus be approximated by a second-order filter with a suitably high cutoff frequency ω_0. In the prototype system to be described, which was constructed on a printed circuit board (PCB), a cascade of two passive resistance-capacitance (*RC*) high-pass filters, separated by a buffer amplifier was chosen to implement the second derivative. Other second-order implementations, such as one of the Sallen–Key structures, are possible in principle [23]. However, active implementations may introduce offset voltages which have to be taken into account, resulting in a potentially more complex circuit. At frequencies well below the filter cutoff the second-order transfer function approximates to

$$\left|\frac{V_o}{V_{\text{in}}}\right| = \left(\frac{\omega}{\omega_0}\right)^2; \quad \angle 180^\circ. \tag{9}$$

This transfer function differs from the ideal second derivative (8) by a factor ω_0^{-2}. Thus, although the filter implements the derivative function, it yields constant attenuation determined by the filter cutoff frequency. As the maximum filter gain is unity, potential high-frequency interference does not lead to clipping of the signal at the supply rails. Using (8) and (9) we can rewrite (6) as follows:

$$|\varepsilon_{\max}| \approx \omega_o^2 V_o \frac{(\Delta t_{\text{slow}})^2}{8}. \tag{10}$$

And so the criterion for switching to the higher clock speed is given by (11)

$$V_o < |\varepsilon_{\max}| \cdot \frac{1}{\omega_o^2} \cdot \frac{8}{(\Delta t_{\text{slow}})^2} = V_{\text{th}}. \tag{11}$$

It is customary to oversample medical data such as ECG by a factor typically around 4–5 [24]. The oversampling factor (OSF) determines the required *fast* sample rate. The maximum error at the *fast* rate is then given by (3)

$$\varepsilon_{\text{fast}} = \frac{(2\pi)^2 \cdot V_p}{32 \cdot \text{OSF}^2}. \tag{12}$$

Consequently, the choice of optimum *fast* and *slow* clock frequencies is guided by the given signal parameters, i.e., the highest input signal frequency ω_m, peak amplitude V_p, the targeted maximum sampling errors $\varepsilon_{\max}$ and $\varepsilon_{\text{fast}}$, the maximum desired counter reading n and the smallest convenient threshold level V_{th}. The relation between V_{th} and n through (7) and (11) may require an iterative optimization process to determine the most suitable combination.

TABLE I
PERFORMANCE WITH DIFFERENT TYPES OF INPUT SIGNAL

Data set	Calculated ε (12)	Simulated ε	Simulated f_{avg}	Simulated V_{th}	f_{fix}/f_{avg}	$^{+)}SNR_{imp}$
*) Blood pressure	34mV	35mV	27	5-7mV	1.5	1.45
*)Normal ECG	88mV	85mV	76	2-3mV	3.2	5.8
**) Gait pressure	83mV	72mV	37	7-9mV	2.8	1.48
*) EEG	302mV	300mV	38	60mV	1.4	1.19

For all data $\varepsilon_{\max} = \varepsilon_{\text{fast}}$.
*)MIT-BIH Polysomnographic Database, record slpdb/slp01a [18b].
**) Gait in Neurodegenerative Disease Database, record als1 [18b].

$$^{+)}\; SNR_{imp} = \frac{SNR_{\text{var}}}{SNR_{fix}} = \frac{\varepsilon_{rms\_fix}}{\varepsilon_{rms\_\text{var}}}$$

C. Performance Estimate

To evaluate the performance the system was simulated with different types of input signal using Matlab software. Recordings obtained from the *PhysioBank* database were used, including ECG, blood pressure, EEG, and gait pressure [19]. Initially, the optimum threshold levels and the associated maximum sampling errors are determined from the simulations. The results are given in Table I together with the approximated error from (12), showing good agreement. Then, the average sample rate is calculated and another set of simulations is performed using the conventional constant rate approach. The constant sample rate is set so that the maximum sampling error is identical to the error previously obtained with the variable approach. The ratio between constant sample rate and average variable rate is the effective sample rate reduction, which is also presented in Table I. Finally, the improvement in the signal-to-noise ratio (SNR) is also reported in the table.

For all examined signals the proposed system yields a performance advantage. As expected, sample rate reduction is most efficient for the ECG and gait pressure signals, both containing linear sections and shorter bursts of high curvature events.

Finally, simulations are carried out to determine the effect of increased noise and interference. White noise with a bandwidth from dc to 100 Hz and peak amplitudes of 20 and 50 μV, respectively, is added to the normal ECG (which already contains an original portion of recording noise). Predictably, a drop in the compression rate is observed for increasing noise amplitudes as shown in Table II. To simulate artifacts due to power line interference, a sinusoidal signal of 50 Hz is superimposed on the normal ECG. A significant decrease in compression ratio is visible for high interference amplitudes of 20 μV or more (around 20 mV in the amplified ECG). Interference and wanted signal are indistinguishable for the compression circuit, so that care must be taken to limit or filter interference pickup to a level normally achieved in ECG monitoring. Alternatively, the compressor sensitivity can be lowered by increasing the threshold

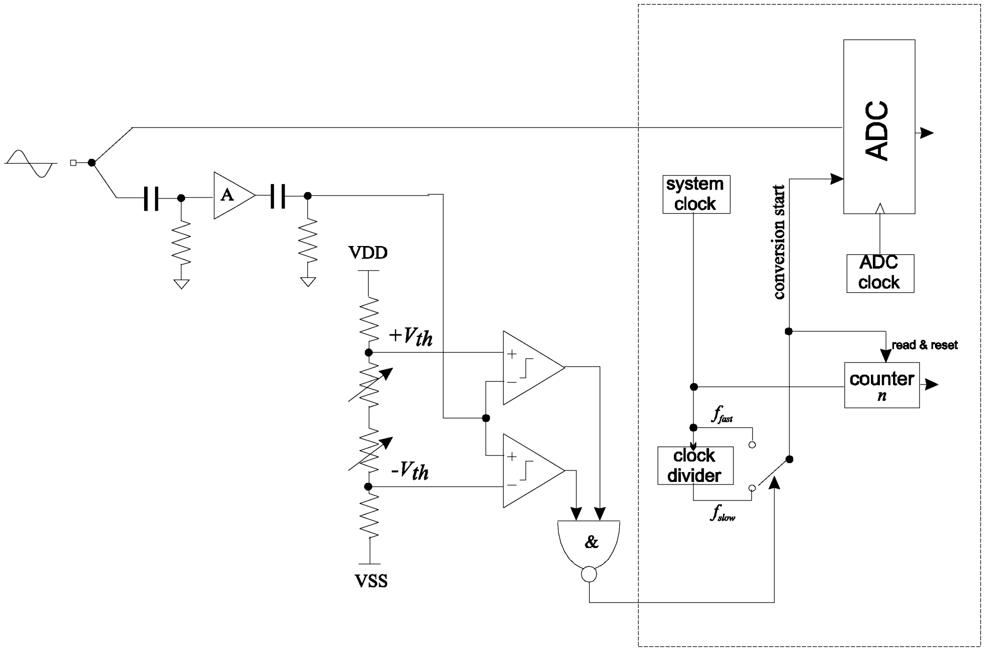

Fig. 2. Circuit diagram of the implemented clock selection system.

TABLE II
PERFORMANCE WITH NOISE AND INTERFERENCE

Data set	Simulated ε	f_{fix}/f_{avg}
Original ECG	80mV	3.2
20µV white noise	109mV	2.3
50µV white noise	84mV	1.2
20µV sine	91mV	1.4
100µV sine	70mV	0.9
40µV sine	47mV	1.0
40µV sine V_{th} =12mV	298mV	2.0

All V_{th} =3 mV except last entry.
All sinewaves were at 50 Hz.

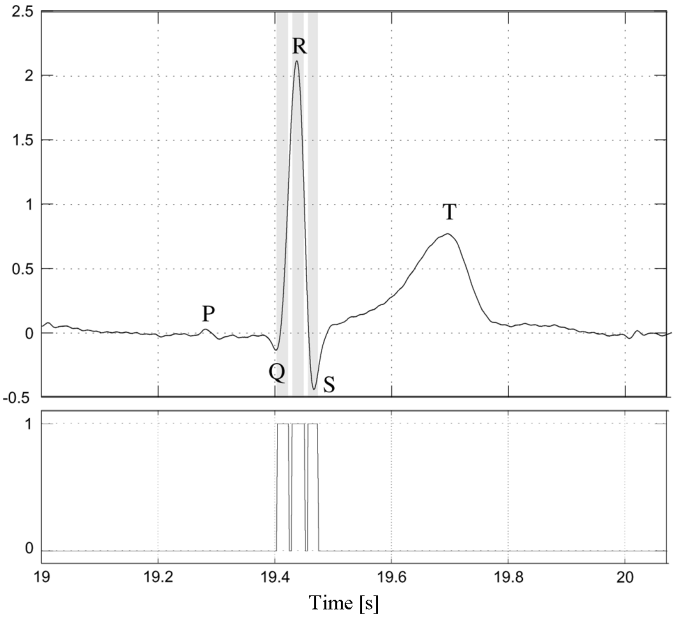

Fig. 3. ECG input signal and measured logic output of the clock selection stage.

level. As Table II shows, this results in higher sampling error but restores good compression even at high interference levels.

III. MEASURED RESULTS

A circuit-level diagram of the proposed clock controller is shown in Fig. 2. It is also suitable for realization as an integrated circuit, where the filter stages can be implemented using low-power, active filter techniques. For bench-testing a discrete version of the control circuit was built. The circuit was assembled from standard components and included *RC* filters with a cutoff frequency of 120 Hz. Power to the circuit was supplied by a 9 V battery. For data acquisition a National Instruments analog input–output (I/O) card was used (the ADC and clock circuit were available on the I/O board and were used to realize the converter part). The threshold levels were tapped from a resistive divider between the supply voltages. For easier trimming of these voltages, a low-gain amplifier stage was inserted between the *RC* filters, providing a signal gain of 20, the additional gain increasing the required threshold level from 5 mV to around 100 mV. The amplifier was inserted *between* the filter stages to remove offsets introduced by the amplifier before the level comparison. Instead of computing absolute values, two comparators are employed to test for condition (11). Depending on the comparator decision, either the slow or fast clock is applied as the ADC trigger signal. Synchronisation between the converter clock and the rest of the system is not mandatory, as long as each conversion is completed in time.

An ECG trace (Lead II) was recorded using disposable gel electrodes from a subject working at an office desk. A conventional INA2 instrumentation amplifier [25] was used in the front-end, providing a gain of 500 and band limiting the signal to within 0.2–40 Hz. The output of the amplifier was connected to a PC via an optical isolation stage to ensure electrical safety. A 60-s stretch of the signal was digitized at 10-kHz sample frequency and 16 bits resolution (LSB $\sim$ 152 uV) and stored on

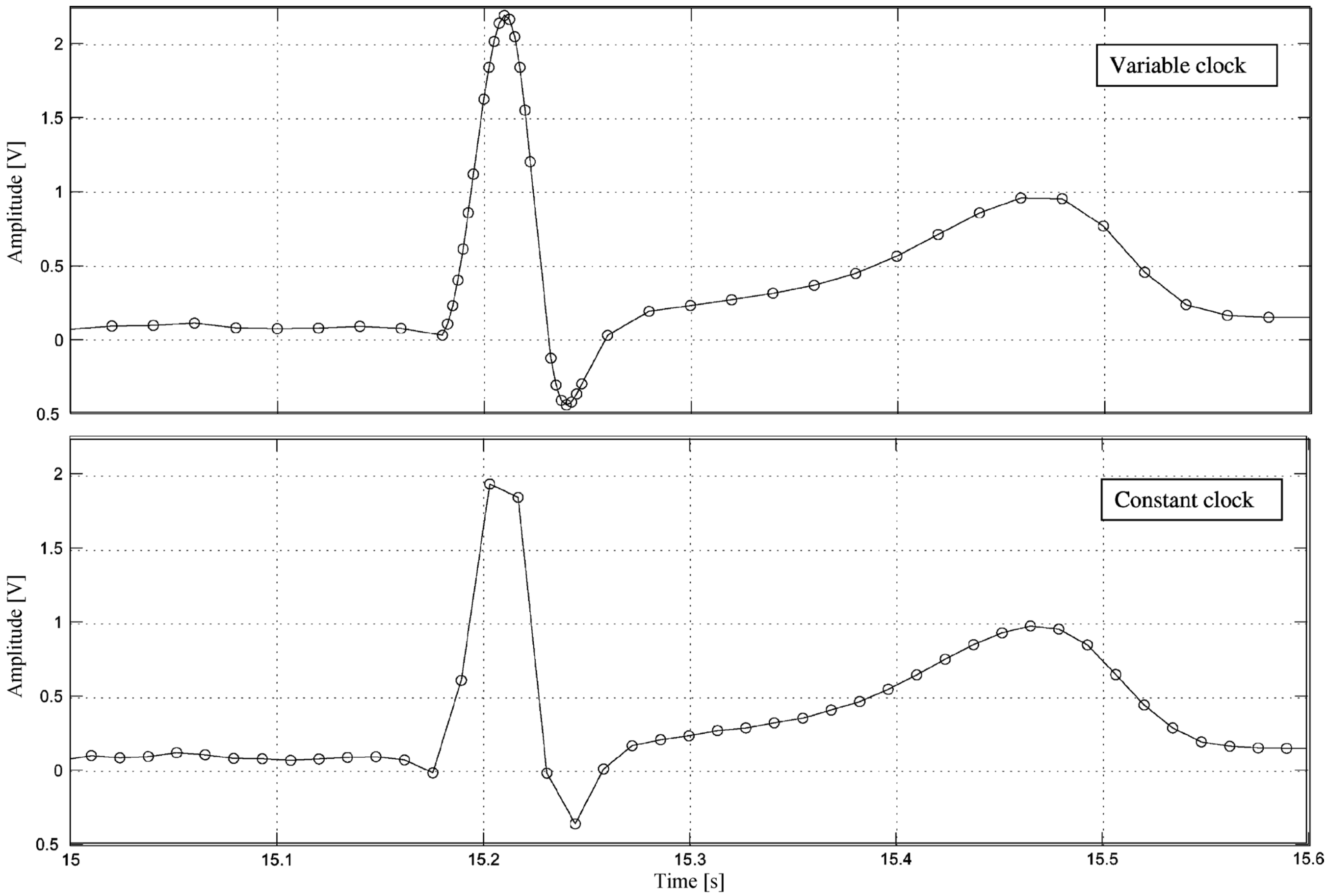

Fig. 4. Measured signal sampled with varying clock cycle (top) and equivalent fixed interval (bottom). The average clock rate is 72 Hz in both cases.

hard disc as a reference signal. This signal was then played back through the analog output of the I/O card and passed through an *RC* high-pass filter with a cutoff frequency of 500 Hz to reject high-frequency interference from the I/O card clock. The analog signal thus obtained was used as the input to the system under test. This setup guarantees reproducible results and allows for the comparison of the proposed system with a fixed clock approach under identical signal conditions.

In a first measurement, the prerecorded ECG signal was applied to the input of the system and to the input of the ADC on the acquisition card in parallel as shown in Fig. 2, again digitizing the signal at 10 kHz and 16 bit resolution. At the same time, the output of the NAND gate was recorded, which is the selection signal for the fast or slow converter clock. The clock was generated by the acquisition software, applying a 400-Hz clock if the logic gate output was high or a 50-Hz clock for a logic zero, respectively. A section of the ECG input signal is graphed in Fig. 3 together with the recorded digital clock selection output. The digital signal is high around the peaks of the QRS complex where a higher sample rate was required and low between the peaks, where the signal exhibits a nearly constant slope. Also, a slow clock is selected between QRS complexes, as expected. Over the 60-s signal period observed, the clock rate averaged 72 Hz (f_{avg}). For the same signal digitized at a constant rate (72 Hz), the error in the recorded signal is much higher, as the direct comparison in Fig. 4 shows. Visual inspection reveals that the implemented variable clock sampling avoids clipping of large signal peaks by placing more sample points around these instances. The measured maximum difference between the reconstructed and the input signal is 139 mV. Clearly, the amount of error that can be tolerated is eventually determined by the application and the parameters to be collected, and sample rates must be chosen accordingly. The proposed scheme can reduce the required storage size as follows. Consider a converter having a resolution of d bit. In addition to d, the timing information is stored for the asynchronous sample scheme. The maximum timer counter reading is given as n by (7). The ratio between the memory space required for the variable and the constant clocking scheme is given by

$$\frac{\text{memory variable}}{\text{memory constant}} = (n+d) f_{\text{avg}} d \cdot f_{\text{fix}}. \tag{13}$$

Thus, using an 8-bit converter and the recorded ECG signal results in 38% data reduction compared to the constant clock approach. Table III is a summary of this performance comparison.

IV. DISCUSSION

The maximum error found by measurement (139 mV) differs slightly from the target value of 123 mV calculated from (12). Clearly, the observed difference lies within the tolerance expected for the prototype PCB and approximation (12). Errors associated with the manual adjustment of the threshold

TABLE III
MEASURED PERFORMANCE COMPARISON BETWEEN CONSTANT AND VARIABLE SAMPLE RATE

	Constant sampling	Variable sampling
Required average clock rate for ε =139mV	160 Hz	72 Hz
Maximum ε at 72 Hz	440 mV	139 mV
Data size	8 bit	11 bit
Data rate for ε =139mV	1280 bit/s	792 bit/s

level would be less prominent in an integrated design, where automatic trimming can be implemented, and where better component matching is achieved. In general, the sampling error is trimmable to the desired level (within the limits set by the *fast* clock frequency). Additional sources of error are briefly discussed.

A. Sampling Error Approximation

If terms up to the eighth order are considered in the approximation of the sampling error in (2), it becomes clear that expression (6) overestimates the sampling error slightly. Using higher order terms and the relation $1/\Delta t = 2\ f_s$, (6) is more precisely written as

$$\varepsilon_{\max} \approx \frac{\delta^2 V_{\text{in}}}{\delta t^2} \cdot \frac{(\Delta t)^2}{8} - V_p \left(\frac{1.268}{\text{OSF}^4} - \frac{0.292}{\text{OSF}^6} + \text{higher order terms} \right) \quad (14)$$

where OSF is $f_s/(2f_m)$ as before. Thus, the error incurred by truncating the expression ultimately depends on the oversampling factor and signal amplitude. For the chosen design parameters, $\varepsilon_{\max}$ is overestimated by around 5 mV (about 4%).

B. Filter Effect on the Threshold Level

Equation (9) simplifies the filter transfer function under the assumption that the filter cutoff is at a very high frequency. The error made in this approximation increases for high input signal frequencies and affects the calculation of the threshold voltage in (11). Implementing a higher filter cutoff frequency reduces this effect at the cost of increased signal attenuation (ω_0^{-2}). The error is partially offset by the overestimation of $\varepsilon_{\max}$, so that the total deviation of the calculated threshold level from its ideal value remains well below 10% for the chosen design parameters.

C. Error Modeling

Equation (6) describing the sampling error was derived for two samples taken symmetrically around the signal peak. In general, the straight line interpolated between sample points taken asymmetrically with respect to the peak is not in parallel with the horizontal axis of the graph. For simplicity of calculation, the maximum measured sampling error presented in Section III is determined as the amplitude difference between input signal and reconstruction. As a consequence, the measured error is generally larger than the modeled error.

V. CONCLUSION

An analog method for signal dependent ADC clocking is proposed, using the second derivative to implement a peak-picking algorithm for linear signal interpolation. The presented circuit contains only basic circuit blocks, allowing for a low-power and small-size implementation that can ultimately be integrated as part of a body-area network sensor. To limit the conversion error, the threshold level must be chosen carefully. The presented analysis leads to a practical approximation of this level. Simulated and measured results are reported and sources contributing to performance variation and to differences between calculated and measured sampling error are discussed. It is demonstrated that an over 50% clock frequency reduction and 38% memory saving can be achieved compared to a constant sampling approach using an ECG recorded with a standard amplifier.

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