TANLOCK BASED LOOP WITH IMPROVED PERFORMANCE

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Declaration

No portion of the work referred to in this thesis has been submitted in support of an application for another degree or qualification at this, or any other university, or institute of learning

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Abstract
This thesis is focused on the design, analysis, simulation and implementation of new improved architectures of the Time Delay Digital Tanlock Loop (TDTL) based digital phase-locked loop (DPLL). The proposed architectures overcome some fundamental limitations exhibited by the original TDTL. These limitations include the presence of nonlinearity in the phase detector (PD), the non-zero phase error of the first-order loop, the restricted locking range, particularly of the second-order loop, the limited acquisition speed and the noise performance. Two approaches were adopted in this work to alleviate these limitations: the first involved modifying the original TDTL through the incorporation of auxiliary circuit blocks that enhance its performance, whilst the second involved designing new tanlock-based architectures. The proposed architectures, which resulted from the above approaches, were tested under various input signal conditions and their performance was compared with the original TDTL. The proposed architectures demonstrated an improvement of up to fourfold in terms of the acquisition times, twofold in noise performance and a marked enhancement in the linearity and in the locking range. The effectiveness of the proposed tanlock-based architectures was also assessed and demonstrated by using them in various applications, which included FM demodulation, FM threshold extension, FM demodulation with improved THD (total harmonic distortion), and Doppler effect improvement. The results from these applications showed that the performance of the new architectures outperformed the original TDTL. Real-time performance of these architectures was evaluated through implementation of some of them on an FPGA (field-programmable gate array) based system. Practical results from the prototype FPGA based implementations confirmed the simulation results obtained from MATLAB/Simulink.

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Nomenclature

4Q-DPLL	Four-quadrant Tanlock PD Based DPLL
AC-TDTL	Adaptive Comparison TDTL
ADC	Analogue-to-Digital Converter
APLL	Analogue Phase-Locked Loop
AS-TDTL	Adaptive Second-order TDTL
ATDTL-ZPE	Adaptive TDTL with Zero Phase Error
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BPSK	Binary Phase Shift-Keying
CEOFD	Constant Envelope Orthogonal Frequency Division Multiplexing
CDTL	Conventional Digital Tanlock Loop
CNR	Carrier-to-Noise Ratio
CORDIC	Coordinate Rotation Digital Computer
CPD	Composite Phase Detector
CPD-DPLL	DPLL with Composite Phase Detector
DAC	Digital-to-Analogue Converter
DCO	Digital Controlled Oscillator
DQPSK	Differential quadrature phase shift keying
DPLL	Digital Phase-locked Loop
DPD-TDTL	TDTL with Dual Phase Detector
D-TDTL	Dual Loop TDTL
DTL	Digital Tanlock Loop
FB	Feedback
FE	Frequency Estimator
FF	Feedforward
FLL	Frequency Lock Loop
FM	Frequency Modulation
FPGA	Field Programmable Gate Array
FSK	Frequency Shift Keying
GPS	Global Positioning System
HT	Hilbert Transformer
iid	Independent and Identical Disturbances
L-DCO	Loop Digital Controlled Oscillator
LF	Loop Filter

Linlock	Linear Phase-locked Loop
LMS	Least Mean Square
LUT	Lookup Table
MFSK	Multiple Frequency Shift Keying
NCO	Numerically Controlled Oscillator
NDTL	No Delay Digital Tanlock Loop
OFDM	Orthogonal Frequency Division Multiplexing
PA	Power Amplifier
PAPR	Peak-to-Average Power Ratio
PD	Phase Detector
PDF	Probability Density Function
PLL	Phase-locked Loop
PSK	Phase Shift Keying
PV	Photovoltaic
RLS	Recursive Least Square
SOC	Systems-on-chip
SNR	Signal-to-Noise Ratio
TDTL	Time Delay Digital Tanlock Loop
TDTL-DI	TDTL with Dual Input
TDTL-LPD	TDTL Architecture with a Linearized Phase Detector
TDTL-WFA	TDTL with Wide Locking Range and Fast Acquisition
THD	Total Harmonic Distortion
U-DTL	Uniform Digital Tanlock Loop
VCO	Voltage Controlled Oscillator
ZC-DPLL	Zero-crossing Digital Phase-locked Loop

List of Matmatical variablis and notiation

Kd	The Phase Detector gain factor
Ko	VCO gain factor
F(s)	loop filter transfer function
To	Free-running period of the DCO
A	amplitude of the signal
ωo	Free running frequency of the DCO
θt	Information-bearing phase in radians
D(z)	Digital Filter transfer function
G1	Digital Filter coefficient
G2	Digital Filter coefficient
K1'	Loop gain
ϕk	Phase error
r	Digital Filter coefficient ratio
ϕss	Steady state phase error
τ	Time delay unit
ψ	Phase shift
ψo	Nominal phase shift
ek	Loop error signal
Λo	Characteristic equation constant
hψϕ	Characteristic function
W	Frequency ratio
L	Lipschitz constant
Gnwf	Power spectrum density
δτ	Dirac Delta function

η(k)	Noise samples
σn2	Gaussian random variable variance
xk	Input signal
yk	Shifted version of input signal
E	Expectation (mean) of random process
gψ,ϕx,y	Combined probability density function
Rk	Random variables amplitude
ϵ	Random variables phase
pϕ	Probability density function
pψ,ϕRk,ϵ	Joint probability density function of Rk and ϵ
erfx	Error function of probability density function
α	Signal to noise ratio
ξ	Non-Gaussian random variable
ϕ(0)	Initial phase error
pψ,kϕϕo	Probability density function of the ϕ(k+1)
given ϕo	
qψ,kϕu	Transition Probability density function
δ	Pre-distortion nonlinearity factor
R	Rounding re-scaling factor
en	Error signal of the adaptive filter
yn	Reference signal of the adaptive filter
d[n]	Desired signal of the adaptive filter
a, b	weighting factor
αk	Time offset
t0	Initial timing offset

wk	Filter coefficients matrix
αk'	Corrupted time offset
αk	Zero crossing time carrier phase
βk	Zero crossing carrier phase offset
N	Adaptive filter order
λ	Forgetting factor
X	Adaptive controller output
G	Eigenvalues matrix

1 GENERAL INTRODUCTION

Phase-locked loops (PLLs) are used for synchronization, frequency synthesis, clock recovery and generation, jitter and noise reduction in communication systems as well as in a multitude of applications in other signal processing and control systems. The PLL is a feedback system that generates an output signal whose phase is locked to that of an input reference 'incoming' signal.
The early generation of PLLs were analogue devices and suffered some drawbacks such as component tolerance, sensitivity to DC drift, difficulties in creating higher loop orders and complication in designing for low frequency applications. Many of these problems were alleviated by the introduction of digital PLLs (DPLLs). As one of the major processes in a DPLL is sampling of the analogue signals, through the analogue-to-digital converter (ADC), DPLLs are classified according to the nature of the sampling process as uniform or non-uniform DPLLs.
The non-uniform DPLLs achieve better acquisition speed performance with reduced circuit complexity compared with their uniform counterparts. The fast acquisition speed can be achieved by the non-uniform types due to the fact that the acquisition process of this type is not constrained by a uniform clock cycles. Therefore, less complex circuitry is needed to build the non-uniform type.
There are two main DPLL categories that use the non-uniform sampling scheme, namely the zero-crossing DPLL (ZC-DPLL) and the digital tanlock loop (DTL). The work presented in this thesis is focused on designing new DTL architectures with improved performance parameters.
This chapter sets the motivation for the research work. This is followed by the objectives that the research set out to achieve. The organization of the thesis is then outlined. This work resulted in a number of research papers, which are listed in this chapter.

Motivation

The DTL is more attractive than the ZC-DPLL due to many desirable characteristics such as good linearity and insensitivity to variations in the power of the reference 'input' signal. However, despite having such desirable attributes the success of the DTL was impeded by the fact that it uses a Hilbert Transformer (HT), which is complex to implement with similar performance for a band of frequencies. The time-delay digital tanlock loop (TDTL) resolved the HT implementation complexity issue by replacing it with a fixed time delay unit that is easy to implement. Despite the improvement in implementation complexity, the TDTL still has a number of limitations that can be improved to enhance the overall system performance. The TDTL performance parameters that are the focus of improvement in this thesis include linearity, acquisition time, locking range, implementation complexity, and noise.

Objectives

The main objectives of this research are:

- Develop new architectures that incorporate auxiliary circuit blocks to improve the original TDTL performance in the following four areas:
  - Phase detector linearity.
  - Acquisition time.
  - Locking range.
  - Noise performance.
- Develop new DTL architectures and assess their performance as in the case of improved TDTL ones.
- Develop simulation models of all proposed tanlock-based architectures to enable evaluation of their performance.
- Test acquisition performance of the new tanlock-based loop architectures in comparison with the original TDTL under rapid changes in the input signal frequency.
- Evaluate the noise performance of the newly proposed architectures under Additive White Gaussian Noise (AWGN) conditions by measuring the probability density function (pdf) and jitter
- Use the newly proposed DTL architectures in a variety of applications and compare their performance to that of the original TDTL.
- Implement some of the proposed DTL architectures on an FPGA (Field Programmable Gate Array) based system and evaluate their real-time performance.

Thesis Organisation

This thesis is organized as follows:

Chapter 2 provides the background and literature review of the PLLs. It covers the basic analogue PLL through to DPLLs and leads to the TDTL. The overview of both the first- and second-order TDTL and their limitations is presented in Chapter 3. Chapter 4 and 5 present improvements to the limitations discussed in Chapter 3 through the incorporation of additional circuit blocks. Chapters 6 and 7 discuss the major changes in the architecture of the original TDTL to provide new DPLLs for the enhancement purposes.

Chapter 8 presents a number of applications that use the proposed improved DTL architectures and an evaluation of their performance. Chapter 9 presents prototype implementations of some of the improved architectures on an FPGA based system. This enables comparison of the simulation results with the real-time ones achieved from the FPGA

implementations. Finally, the conclusions and suggestions for future work are presented in Chapter 10.

List of Publications

Journal Papers

1. O. Al-Kharji Al-Ali, N. Anani, S. Al-Araji, and M. Al-Qutayri," A Non-uniform DPLL Architecture for Optimized Performance," *IEE Japan Transactions on Electrical and Electronic Engineering.* In press.

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Conference Papers

1. .M.A Al-Qutayri S. R. Al-Araji, and J. Jeedella, O. Al-Kharji Al-Ali, N.Anani, "Second-order TDTL with Initialization Process," *The IEEE International Conference on Electronics, Circuits, and Systems (ICECS),*2012. Published.

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7. O. Al-Kharji Al-Ali, N.Anani, P.V.S. Ponnapalli, M.A. Al-Qutayri and S.R. Al-Araji, "TDTL architecture with fast error correction technique," in *17th IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, Athens , 2010, pp. 475 - 478.

8. O. Al-Kharji Al-Ali, N. Anani, M.A. Al-Qutayri, S. R. Al-Araji and P. V. S. Ponnapalli, "Time delay digital tanlock loop with acquisition-aided circuit," in *7th International Symposium on Communication Systems Networks and Digital Signal Processing (CSNDSP)*, Newcastle upon Tyne, UK, 2010, pp. 373-376.

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13. M. A. Al-Qutayri, S. R. Al-Araji, O. Al-Kharji Al-Ali and N. A. Anani, "Time delay digital tanlock loop with linearized phase detector," in *16th IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, Tunisia, 2009, pp. 555-558.

Contributions to Knowledge

The research work presented in this thesis led to the development of new Time Delay Digital Tanlock Loop based DPLL systems for improving various performance parameters of the original First- and Second-order TDTL, such as linearity, acquisition, noise and locking range. In summary, this thesis presents:

- A solution to reduce the problem of nonlinearity in the original First- and Second-order TDTLs by the introduction of the TDTL with Linearized Phase Detector and the TDTL with Pre-distortion architectures.
- A methodology to improve acquisition characteristics by the new TDTL with Adaptive Filtering, TDTL with initialization and TDTL with Acquisition-aided circuits.
- A method to enhance noise immunity by the development of the TDTL with Optimised Phase Detector, which as a result led to improving the locking range.
- A methodological discussion of different performance criteria for TDTL systems and a variety of TDTL design techniques that can be chosen based on the applications.
- An evaluation of the real-time effectiveness of selected TDTL systems using FPGA-based implementations.

2 OVERVIEW OF DIGITAL TANLOCK LOOP

Introduction

This chapter presents a methodical review of the research work reported in the literature that relates to the architectural developments of PLL systems with due account of their applications, mainly, for signal synchronization in communication systems. The emphasis of the review is on a special type of PLL; the time delay digital tanlock loop (TDTL) which is the main subject of this thesis. The performance of any PLL system is usually assessed in terms of its acquisition time, locking range, and noise and jitter performance. These parameters determine the quality of the achievable synchronization process which is a fundamental requirement for most forms of electronic communications systems including wired, mobiles, and satellite systems [1, 2, 3]. Consequently, extensive efforts continue to be spent in order to improve these parameters as modern communication systems strive for wider bandwidths, and better noise immunity.
Synchronization is also required in digital integrated circuits (ICs) and systems, such as microcontrollers and digital signal processing ICs and systems. Clock distribution in a synchronized manner across modern sophisticated devices such as system-on-chip (SOC) ones is a demanding task [1, 3]. Networks of synchronized oscillators are an alternative approach to classical tree-like clock distribution methods in large-scale synchronous SOC. Each node of the network may, for example, consist of a PLL trying to match the phase to its nearest neighbours [4, 5].
Noise immunity is an important factor in assessing the integrity and performance of a communication system as it affects the quality of the received signals. For example, in digital communication systems, noise degrades the overall system because it requires re-transmission of data or extra coding to recover the data in the presence of noise and errors. Therefore, extra cost will be added to the overall communication process to maintain the system bit error rate (BER) at an acceptable level. PLLs have an important role in mitigating the effects of noise by enabling the recovery of a received signal from a noisy communication channel [1, 2, 6, 7, 8, 9].

Classifications of PLLs

As shown in Figure 2.1, phase-locked loops are broadly classified as analogue (APLL) or digital (DPLL). DPLLs may classified as uniform or non-uniform DPLLs. Uniform and non-uniform DPLLs are subdivided into different types as will be briefly explained below.

Figure 2. Classification of PLLs.

Analogue PLLs

The PLL is a negative feedback control system that produces a signal, which has a fixed relation to the phase and frequency of an incoming "reference" signal [7]. The block diagram of a generic analogue PLL (APLL) system is shown in Figure 2.. It consists of a phase detector (PD), a loop filter (LF) and a voltage controlled oscillator (VCO).

Figure 2. Block diagram of a basic analogue PLL.
The PD compares the phase of the input "reference" signal (Fref) with the phase of the output signal (Fvco). The output of the PD is low-pass filtered and then used to drive the VCO in such a direction so as to reduce the phase error and reach the steady state i.e. achieve the locking state. When a PLL is in lock, the VCO output is in phase with the incoming reference signal. If the low-pass filter is simply a gain block, the PLL is a first-order type and the phase error in the steady state is a small constant. Otherwise, the PLL is a second-order device and the phase error is zero when in lock.
$$Hs=\theta o(s)\theta i(s)= KdKoF(s)s+ KdKoF(s) \quad (2.1)$$
where Kd is the PD gain factor, Ko is the VCO gain factor, F(s) is the loop filter transfer function and s is the complex frequency Laplace variable [1, 7].
APLL implementations have several disadvantages compared with DPLL. These include sensitivity of the centre frequency to temperature and power supply variations. In addition, analogue multipliers which are used as PDs are very sensitive to DC drift and the non-sinusoidal phase detectors are very sensitive to noise with an extended acquisition time [7]. Moreover, the saturation of components in APLL is common when the input Signal-to-Noise Ratio (SNR) is low enough to induce noise spikes. When this type of input is present, then VCO will saturate and new acquisition begins for the input. In addition, for higher order APLL stray capacitance inserts additional poles which may adversely affect the stability of the system especially in the presence of noise. Also, it is difficult to design filters for analogue PLLs in the low frequencies. Finally, APLL has a slow and unreliable self-acquisition, which requires the use of additional aided acquisition circuits to get acceptable performance [10]. With the rise of digital integrated circuit technologies in the early 1970s and the advantages it offered, most electronic systems started moving into the digital domain including communication systems. Consequently, APLLs followed suit and evolved into the digital PLL (DPLL) [1, 7, 11].

Digital PLLs

A block diagram of a generic DPLL is shown in Figure 2.3. This is similar to the APLL of Figure 2.2 but with the analogue blocks replaced by their digital counterparts. The digital phase detector (DPD) senses the phase difference between input signal frequency F_{ref} and the divided version (F_N) of the digitally controlled oscillator (DCO) output signal (F_{DCO}). The output of DPD is filtered by the digital loop filter (DLF) and then used to drive the DCO in the direction of achieving the locking state [10, 12, 13].

Figure 2. Block diagram of a typical digital PLL.
As mentioned above, DPLLs may be classified as uniform and non-uniform types according to the type of the sampling they use. The sampling process influences the modelling complexities and acquisition time of the DPLL. Uniform DPLLs are harder to model and implement, and their acquisition performance is inferior to the non-uniform DPLLs. This explains the reason for the non-uniform DPLLs getting the focus of researchers. DPLLs may also be classified according to the type of the phase detector they use. This classification includes flip-flop DPLLs, Nyquist rate DPLLs, lead–lag DPLLs or binary quantized DPLLs, Exclusive-OR DPLLs (or triangular), bang-bang DPLLs (or rectangular), sinusoidal DPLLs, arctan (or sawtooth), etc. [13, 12]. A PD is characterized by a graph of its output voltage against the phase error (s-curve) as shown in Figure 2.4 for four different PDs. Clearly, the arctan PD possesses the best linearity of all PD types.

Figure 2. PD s-curve for four different types of DPLLs [7].
This thesis focuses on the time delay digital tanlock loop (TDTL) which is a special type of DPLL that uses the arctan as PD, due to its good linearity characteristics, with a non-uniform zero crossing sampling that offers simplified modelling and enables further performance improvements. The following subsection reviews the major DPLLs developments reported in the literature with particular focus on those using the arctan PD. It also provides a brief explanation and analysis of the basic zero crossing non-uniform DPLL. The development of the DPLL starting from the uniform arctan loop and ending up with the non-uniform TDTL is presented. The ultimate aim of the development is to improve the TDTL loop in terms of implementation complexity, acquisition speed, locking range, and noise immunity.

DPLL Architecture

Digital PLLs that use arctan PDs may also be categorized as uniform or non-uniform types. The uniform type may be subdivided into two categories: the uniform digital tanlock loop (U-DTL) and the 4-quadrant tanlock PD based DPLL (4Q-DPLL). The non-uniform may also be subdivided into two categories: digital tanlock loop (DTL) and the time delay digital tanlock (TDTL).

Uniform DPLL

This subsection reviews the development of different uniform DPLL types especially the ones that use arctan phase detectors.

Bang-Bang PLL

The Bang-bang PLL started as an analogue device, which consists of a PD, charge pump (CP), loop filter and a VCO as shown Figure 2.. The CP simply carries out the conversion of the information from PD into a suitable form for the loop filter.

The binary Bang-Bang PLL exhibits similar behaviour to digital system by utilizing a binary type PD or Bang-Bang PD (BBPD). While most PDs produce an output, which is proportional to the phase error, BBPD returns its output from the polarity of the phase error, which generates additional timing jitter due to quantization error.
There are many attempts in the literature aimed at improving the acquisition performance of this type of PLL clearly, because it uses uniform sampling, which tends to degrade the acquisition speed. For example, in [14] an additional CP and frequency controller are added to the conventional Bang-Bang PLL for frequency synthesises application. This controls the capacitance of the CP according to incoming frequency, hence, improves the acquisition time. An improvement of 40 per cent has been reported.
Another way to enhance the acquisition time of the Bang-Bang PLL was by introducing a bank of CPs [15]. This improved the linearity of the system and decreased the quantization error, thus improving the acquisition.

Figure 2. Bang-bang PLL block diagram.

Costas Loop

Costas loop is a uniform DPLL that is generally composed of three PDs, two low-pass filters, one loop-filter, a VCO and 90o phase shifter (HT) as shown in Figure 2. . This is, i.e. the HT, to provide quadrature outputs. Each one of these two quadrature outputs is fed as an input to one of the two phase detectors. The other input for each phase detector is derived from the same input signal, Figure 2.6. The output of each phase detector is passed through a low-pass filter. The outputs of the two low-pass filters are fed to the third PD whose output is used to drive the VCO through the loop filter. This type of DPLL is used mostly as a demodulator [16, 17].
A scheme that uses a control signal that is proportional to the phase error to improve the acquisition speed is described in [18]. However, there is a limitation to this improvement due to the uniform sampling nature and the nonlinearity of the PD.

Figure 2. Costas PLL block diagram.

Uniform Digital Tanlock Loop (U-DTL)

The U-DTL is a type of DPLLs, which consists of a 90o phase shifter (HT), two multipliers, arctan PD, two integrators, a loop filter, and a DCO as shown in Figure 2..

Figure 2. General block diagram of the uniform digital Tanlock loop.
In [19] a U-DTL, also known as linear phase-locked loop (Linlock) is proposed with the arctan, formerly called known as a sawtooth PD. This type of loop uses an arctan PD to enhance the linearity and consequently the locking range as well as the acquisition compared with the conventional phase-locked loop. This Linlock is a uniform type of the PLL, which requires

complex circuit implementation and has relatively low performance in a noisy environment i.e. when the SNR is low.
The transfer characteristic of a linear PD when a small SNR is used is proposed in [20]. The research explains the effect of low SNR on the linearity of the PD when it is used in a uniform PLL. For small SNR, the arctan PD degenerates into a sinusoidal characteristic. Thus, the average value of the PD output is proportional to the sine of the phase difference between the output signal and reference signal, and to the input SNR. Under small SNR, the sawtooth relationship is lost and the performance deteriorates.
In [21] the results of a DPLL with modified n^{th}-order arctan PD are proposed. The research explains that when the SNR is high, the locking range of PLL systems with modified n^{th}-order tanlock PD characteristics exceeds that of conventional systems employing sinusoidal PDs. However, as the SNR approaches certain threshold, the locking range of the tanlock systems falls off faster than that of the conventional sinusoidal systems.
The acquisition performance of the second-order PLL with sawtooth PD is discussed in [22]. The challenges posed by the conflicting requirements of fast acquisition and wide locking range are also explained. The advantage of using linear PD that generates sawtooth phase characteristics is highlighted. The linear range is extended by simply increasing the gain and dynamic range of the loop filter and DCO combination by a factor of N. While the main disadvantage is the amount of interference which merely perturbs the pulse positions, causing excess phase jitter. Therefore, low SNR can cause deletion or addition of pulses, which may results in malfunctioning or complete failure of the phase detector.
The S method for analysing the acquisition behaviour of a second-order generalized tracking system in the absence of noise is proposed in [23]. This method allows a closed form expression of the locking range and of the frequency acquisition time for any type of loop nonlinearity. The results of analysis are compared with those already in the literature and with others obtained via the numerical solution of the system equations.
In [24] a computerized procedure for obtaining the locking range of a PLL for different PDs topologies, such as sinusoidal, triangle and sawtooth is proposed. The procedure is quite general with respect to the PD function and loop filter. In addition, an experimental study is described which produced results that were in good agreement with those predicted by the analysis. However, the study is only applicable to uniform DPLL types.
In [25] an analysis of the locking range and acquisition time for third-order loop with sinusoidal, sawtooth, and triangular PD characteristic under the hypothesis of ideal integrators in the loop filter is proposed. The use of the third-order is to track a frequency ramp eliminating the increase in the probability of cycle slipping of the second-order loop. The main disadvantage of the third-order is the increased risk of instability.
A phase shift-keying (PSK) demodulator using a uniform tanlock loop with a performance evaluation in the presence and absence of noise is presented in [26, 27]. The PSK tanlock loop has a wider tracking range and faster phase acquisition compared with both Costas or squaring loops that are usually used for PSK suppressed carrier tracking, but it has a greater tendency to lock to a wrong state i.e. false locking. The improvement in the performance of the proposed design is achieved using an adaptive controller that controls the PD. The wider locking range, faster phase acquisition and

reduced tendency to hang-up, and insensitivity to input signal amplitude of the proposed system are offset by its poorer noise performance at low SNR ratios, and by a somewhat greater liability to lock to the wrong state.
In [28, 29, 30] an open-loop uniform tanlock carrier recovery structure for binary phase shift-keying (BPSK) is proposed and discussed. The noise performance is investigated in terms of BER of the detected BPSK. The system shows reasonable performance compared with conventional uniform loops.
There is a type of DPLL called uniform four-quadrant arctan PD based DPLL (4Q-DPLL) [31, 32]. It accepts at its input a complex single-sinusoid signal. The 4Q-DPLL consists of a multiplier (i.e. mixer), arctan function, a loop filter, and a numerically controlled oscillator (NCO) which is equivalent to a DCO as shown in Figure 2.. The PD consists of both multiplier and arctan function where the arctan function maps the complex output produced by the multiplier to the four quadrant phase angle. The remaining part of this subsection shows the development of the 4Q-DPLL architecture.

Figure 2. General block diagram of the uniform four-quadrant arctan PD based DPLL.
In [31, 32] frequency tracking and acquisition with a four-quadrant arctan PD based DPLL is proposed. The tracking performance is similar to that of the APLL at high loop gains and the acquisition is linear compared with the sinusoidal PD. The open-loop analysis of the four-quadrant arctan PD output under noisy environment is presented. Acquisition is treated as a complete linear process under noise-free conditions and the performance degradation is studied using computer simulations. The disadvantages of four-quadrant arctan PD based DPLL is its sensitivity to the input power variation.
In [33] the performance analysis of a four-quadrant arctan PD based DPLL with modified PD using hyperbolic nonlinearity of the system proposed in [31, 32] is investigated. The nonlinearity is deliberately introduced for improved performance of the closed-loop system but the system still has sensitivity to the input signal power.
In [34] the performance analysis of a four-quadrant arctan PD based DPLL with modified PD using logarithmic function as modification of the system proposed in [31, 32] is investigated. The logarithmic nonlinearity is intentionally introduced to improve phase noise performance during the steady state tracking mode, however the system was still sensitive to variations in input signal power. In addition, the loop has a narrower locking range when compared to the linear model in [31, 32], which is clearly, a drawback.
In [35] a frequency estimation technique, assisted by a second-order four-quadrant arctan PD based DPLL, for complex single sinusoidal signals in additive white Gaussian noise (AWGN) is introduced. The loop contains the frequency information in its phase error process, at steady state, which is then used to estimate the frequency after the signal has been acquired by the four-quadrant arctan PD based DPLL. The frequency estimation shows good jitter performances, but still the system was sensitive to variation in the input signal power.

Non-Uniform DPLL

This subsection section reviews the development of the non-uniform PLL that uses the arctan phase detector.

Digital Tanlock Loop (DTL)

In [36] a non-uniform sampling DTL which uses an arctan PD with linear phase characteristic is proposed. The DTL consists of 90ophase shifter, two sample and hold blocks, arctan PD, a loop filter, and a DCO as shown in Figure 2.. The main feature of the DTL is that the phase error detector, using the arctan function with a phase and quadrature samples of the incoming signal, has a linear phase characteristic with a period of 2π. Accordingly, the DTL can be easily characterized by a linear difference equation, thereby making it possible to analyse the loop easily, without approximation of nonlinearity as is usually done in the analysis of a conventional DPLL with sinusoidal PD characteristic. The performances of the first- and second-order DTLs in noisy and noise-free environments have been investigated by analysis and computer simulation. It is shown that the linear PD characteristic results in many attractive features in comparison with the conventional DPLL with the sinusoidal phase characteristic. These include insensitivity of the locking conditions to variation in input signal power; improved noise immunity, wider locking range and smaller steady state phase error of the first-order loop for an input with frequency offset, and reduced sensitivity to initial phase errors in convergence of the second-order loop. The double arms of this topology helps in cancelling the amplitude effect of the incoming signal and hence results in robust immunity to power variations. However, despite having many desirable attributes such as linearity and insensitivity to input signal power, the success of the DTL was impeded by the fact that it uses a HT block, which is rather complex to implement.

Figure 2. General block diagram of the non-uniform digital Tanlock loop.

In [37] an N-phase DTL, where N is an integer, for tracking suppressed-carrier N-array PSK signals is proposed. The main feature of the N-phase DTL is that the phase error has linear phase characteristics in the modulo 2πN sense because of using an arctan PD. The performance of the N-phase DTL has been compared to that of the digital N-phase I-Q loop. It has been found that the first-order N-phase DTL has wider locking range than the first-order N-phase I-Q loop in the absence of noise.
In [38] a method to demodulate both stereophonic FM and monophonic FM using digital signal processing DTL improved architecture is proposed. The proposed stereo FM receiver system using DTL is very simple interims of implementation compared with conventional receivers.
An improvement of the performance of a DTL based on a multi-sampling Scheme is proposed in [39, 40]. It yields extended locking range, and reduced steady state mean and variance of phase error as compared to the conventional DTL. The performance of the first-order DTL is analysed in the presence of AWGN, and compared to the conventional DTL, which shows better noise performance.

In [41] the convergence behaviour of the first-order multisampling DTL (MSDTL) proposed in [39, 40] with phase and frequency step inputs is investigated. The MSDTL yields extended locking range, and reduced steady state mean and variance of phase error as compared with a conventional DTL. It is shown that as the number of samples taken in one period of the received signal increases, the convergence time of the first-order MSDTL decreases sharply.
In [42] noise analysis of a non-uniform DTL is investigated using both analytic and computer simulation methods. These results are presented in terms of phase error probability density function (pdf) versus input SNR. It is found that for low to moderate input SNR, the DTL has only a slight improvement over the DPLL. The DTL, however, has larger linear phase characteristics than the conventional DPLL, which makes it attractive for applications that require an increased tracking range or as a first stage in carrier tracking systems based on optimum estimation procedures such as a Kalman smoother.
An extended range "tanlock" PD is derived from the iterated extended Kalman filter in [43]. A slight improvement in the acquisition compared with original DPLL using arctan as well as sinusoidal PD was achieved at the expense of large circuit implementation of the proposed architecture and the system is more prone to noise.
An analysis of DTL with adaptive filtering is proposed in [44]. This research uses a filter with third-order whereas the coefficients of the loop filter are modified adaptively using Least Mean Square (LMS) algorithm. Furthermore, using a multisampling structure gives a good locking range and better noise immunity. In order to maintain optimum detection, adjustments in the filter coefficients are needed. This is achieved using a LMS adaptive detection filter.
In [45] a coherent detector selection diversity system used in fading channels is proposed. This uses a DTL and conventional DPLL. The DTL is used to provide the phase error whilst the DPLL is used to synchronize this phase error. The proposed system uses two PLLs with different bandwidths; one with the narrow loop bandwidth and the other with a wider bandwidth. This is in order to cope with fading channels by switching between two PLLs.
In [46] a study of the application of the N-phase DTL in digital cellular radio with π4- Differential quadrature phase shift keying (DQPSK) modulation is proposed. The performance degradation due to fading effect is investigated in terms of the BER and the steady state phase error variance by computer simulation. It is shown that, in the digital cellular radio systems, the performances on both BER and phase error variance using DTL are far better than that using the traditional digital N-phase I-Q loop.

Zero-crossing ZC-DPLL

To ease the mathematical analysis of the TDTL architecture in the following section, the mathematical analysis of the ZC-DPLL is discussed first. This is because the TDTL has similar analysis to the TDTL.
The ZC-DPLL type of DPLL accepts sinusoidal input signals and performs sampling near the zero crossing. It is simply generates varying sampling intervals that control the ADC until it locks to the zero crossing (either positive going or the negative going or both) [10, 47]. The block diagram is

shown in Figure 2.. It simply consists of input sampler ADC, digital low-pass filter (LF) and a DCO.

Figure 2. block diagram of the sinusoidal ZC-DPLL [11].

The ADC sampler acts as a PD for the incoming signal and the output of the DCO, and produces a phase difference term at the zero crossing point. The LF alters the amplitude of the samples produced by the ADC in a way that drives the DCO to produce a signal that has the same frequency as the input signal but with a small phase difference with respect to the phase of the input signal. The loop filter consists of proportional and accumulation paths with an order that represents the order of the loop difference equation; hence the n^{th}-order loop filter can be described in the z-domain by the following transfer function [10]

$$Dz=z+c1z+c2...z+cnz+p1z+p2...z+pn \quad (2.2)$$

Since the presence of the phase error depends on the previous value, the order of the loop equals the order of the loop plus one. For this reason, in the first-order loop the digital filter is just a proportional path, while the second-order loop utilizes a first-order digital filter with a transfer function of the form

$$Dz=kz+c1z+c2z+p1z+p2 \quad (2.3)$$

As shown in [10] the condition for the second-order ZC-DPLL to lock on zero phase error, p1 must equal to -1, therefore (2.3) can be written as follows

$$Dz=G1+G2(1-z-1) \quad (2.4)$$

This provides a time domain input-output relationship as

$$yk=G1xn+G2k=0nxk \quad (2.5)$$

where x (k) and y (n) are the discrete input and output signals respectively.

The the ZC-DPLL system shown in Figure 2. receives a continuous sinusoidal signal yt with a frequency offset $\Delta\omega=(\omega-\omega o)$, and this is translated as a phase shift, from the free running frequency ωo of DCO as follows

$$yt=A\sin\omega ot+\theta t \quad (2.6)$$

where A is the amplitude of the signal, ωo(rads) is the free running frequency of the DCO, and θtis the information-bearing phase in radians. Assuming a frequency step at the input, the phase of the phase process will be

θt=ω-ωot+θo
(2.7)

where ω(rads) is the angular frequency of the input signal, and θo(rad) is a constant.

The sampling interval of the DCO between the sampling instants t(k+1) and t(k) is given by

Tk=To-ck-1
(2.8)

where To=2πωo (s) is the free-running period of the DCO, whilst c(k-1) is the output of the digital filter at the previous sampling instant. The total time up to the k^{th} sampling instant can be defined as

tk=i=1kTi=kTo-i=0k-1ci
(2.9)

Under such condition the nonlinear difference equations representing the first-order loop (with D(z)=G1) and the second-order loop (withDz=G1+G2(1-z-1) can be respectively given by [48, 49]

ϕk+1=ϕk-K1'sinϕk+Λo (2.10)

and

ϕk+1=2ϕk-ϕk-1K1'sinϕk-r{ΛoK1'sinϕk] (2.11)

where ϕk is the phase error at the instant k, K1'=ωG1A, K2'=ωG1, Λo=2πω-ωoωo, and r=1+G2G1. From (2.6), (2.7) and (2.10) , the steady state error of the first-order loop can be shown as follows and both ϕk and ϕk+1 at the steady state are

ϕss=ϕk=ϕk+1
(2.12)

Therefore (2.10) will be

ϕss= ϕss- K1'sinϕss+Λo

(2.13)

Therefore, the steady state error of the first-order loop is

ϕss=sin-1ΛoK1'
(2.14)

while the second-order loop locks on zero phase error due to the accumulated path of the first-order loop filter.

Time Delay Digital Tanlock Loop (TDTL)

As previously mentioned, the success of the DTL was impeded due to the fact that it uses HT (Hilbert Transformer), which is fairly complex to implement. The TDTL replaced HT with a simple fixed time delay unit, which act as a PD [50]. The TDTL will be explained in details in the coming sections.
In [51, 52, 53] a new approach that enhances the locking and acquisition characteristics of the TDTL loop is developed. The idea revolves around replacing the single time delay with dual time delay blocks controlled using a Finite State Machine (FSM). This approach extends the tracking range of the loop due to partial enhancement in the linearity of the PD.
In [52, 54] an adaptive gain architecture, which uses the error produced by the PD to modify the gain of the loop filter is proposed. This method enhanced the locking range and the cycle slipping immunity of the loop for sudden changes in the input frequency signal.
In [55] an early error sensing adaptive TDTL architecture is proposed. This architecture uses a feedforward arm to modify the loop filter coefficient so as to enhance the locking range and the cycle slipping immunity of the loop. The system has better performance compared with adaptive gain sample sensing architectures, which uses a feedback arm to modify the loop filter for the same purpose [56].

Time Delay Digital Tanlock Loop Disadvantages

A thorough literature review covering both first and second-order TDTL revealed a number of factors that limited the performance of the TDTL with a scope for alleviating them. These limitations are:

- The nonlinearity of both first- and second-order TDTL caused by the fixed time delay unit which produces different phase shifts for different incoming frequency.
- A narrow locking range, especially for the second-order TDTL, that can be more enhanced.

- Relatively slow acquisition speed in the first-order TDTL.
- Slow acquisition speed of the second-order TDTL to reach the steady state zero phase error, which limited its adoption for applications requiring fast acquisitions.
- The inability of the first-order TDTL to converge to a zero phase error when in lock. This has adverse effects for applications that use coherent demodulation.

The aim of the research in this thesis is to develop TDTL architectures with enhanced performance primarily for applications in communication and signal processing systems by alleviating the above limitations. This will enable the identification of the TDTL system parameters that impose constraints on the system and hinder its performance.

Summary

This chapter reviewed the research published in the literature that governs the development of DPLLs, which use the arctan as a phase detector. A brief explanation of the basic zero crossing non-uniform DPLL and its mathematical analysis were also presented. The emphases were placed on the non-uniform TDTL and its limitations which adversely affects it performance in terms of linearity, acquisition speed, noise immunity, and locking range.

3 ANALYSIS AND MODELLING OF THE TDTL SYSTEM

Introduction

This chapter describes in details the mathematical model and analysis of the TDTL in noisy and noise free environment. It also highlights the limitations of the original TDTL system in terms of the performance parameters such as PD linearity, acquisition time, locking range and noise immunity.

The uniform DPLL type uses a fixed clock sampling process, which limits the speed of the loop. The non-uniform DPLL type achieves better speed performance with less circuit complexity than their uniform counterpart [11, 36, 50, 52, 55].
There are two main DPLL categories that use the non-uniform sampling technique namely ZC-DPLL and DTL. The latter is more attractive due to many desirable characteristics such as good linearity and insensitivity to variations in the power of the reference 'input' signal [36, 44]. However, despite having such desirable attributes, the success of the DTL was impeded by the fact that it uses an HT, which is fairly complex to implement [36]. The TDTL proposed in [50] resolved the HT implementation complexity issue by replacing it with a fixed time delay unit that is easy to implement. While, most desirable features of the DTL were preserved in the TDTL, linearity was slightly degraded which consequently affected other performance parameters, such as acquisition time and noise immunity.
In this chapter the TDTL mathematical analyses and limitations are discussed.

Mathematical Model and Analysis of the First-order TDTL

This section details the mathematical model of the TDTL under noise free condition. This will then be used to introduce the improved architectures. The TDTL analysis in this section follows the same procedure given in [50] as illustrated below.

Figure 3. Block Diagram of the first-order TDTL.

The TDTL system receives a continuous sinusoidal signal yt with a frequency offset $\Delta\omega=(\omega-\omega o)$, and this is translated as a phase shift, from the free running frequency ωo of DCO as follows

$$yt=A\sin\omega ot+\theta t \quad (3.1)$$

where A is the amplitude of the input signal, $\theta t=\Delta\omega t+\theta o$ is its phase process, and θo is a constant. As depicted in Figure 3., the incoming signal is passed through a time delay unit τ that will induce a variable phase shift ' lag' $\psi=\omega\tau$ which depends on the frequency of the input signal. Therefore, a phase shifted signal xt of the input signal is generated as

$$xt=A\sin\omega ot+\theta t-\psi \quad (3.2)$$

The incoming input signal and its phase shifted version pass through their respective sample and hold blocks, as shown in Figure 3., thereby sampled versions of both signal (3.1) and (3.2) are produced and can be expressed as

$$yk=A\sin\omega ot(k)+\theta k \quad (3.3)$$

and

$$xk=A\sin\omega ot(k)+\theta k-\psi \quad (3.4)$$

where $\theta k=\theta tk$

The sampling interval between the sampling instants tk and tk-1 is given by

$$Tk=To-ck-1 \quad (3.5)$$

where $To=2\pi\omega o$ is the nominal period of the DCO and ci is the output of the digital loop filter at the i^{th} sampling instant. By assuming t0=0, the required time to reach the k^{th} sampling instant is

$$tk=i=1kT(i)=kTo-i=0k-1c(i) \quad (3.6)$$

As a result, both yk and xk may be re-written as

$$yk=A\sin\theta(k)-\omega oi=0k-1c(i) \quad (3.7)$$

and

$$xk=A\sin\theta(k)-\omega oi=0k-1c(i)-\psi \quad (3.8)$$

Consequently, the phase error difference between the incoming input signal and the DCO can be defined as

$$\phi k=\theta(k)-\omega oi=0k-1ci-\psi \quad (3.9)$$

Therefore, both (3.7) and (3.8) can be expressed in terms of the phase error as

$$yk=A\sin\phi k+\psi \quad (3.10)$$

and

$$xk=A\sin\phi(k) \quad (3.11)$$

The loop error signal ek produced by the arctan phase detector can be expressed as

ek=ftan-1sinϕ(k)sinϕk+ψ
(3.12)
where fγ=-π+[γ+πmod 2π]. This error signal ek represents a version of the phase error whose nonlinearity increases as the phase shift ψ goes away from the value of π2 (rad). The digital loop filter with a transfer function Dk receives the error signal ek and produces the signal ck that derives the DCO to the required frequency. Consequently, the system difference equation can be derived from (3.6) and (3.9). This is done by evaluating the phase difference ϕ for both consequence samplesk and k+1, then substitute both phase difference consequence samples with each other to arrive to the following as
ϕk+1=ϕk-ωck+Λo
(3.13)
where Λo=2πΔωωo and ck is the output of the loop filter that has Dz as a transfer function Therefore, ck=hDk*e(k) where D(z) is the z transfer of hDk and e(k) is the output of the phase error detector at the k^{th} sampling instant.
Due to the nonlinearity produced by the variation in the phase shift ψ due to variation in the frequency of the input signal, the system difference equation cannot be solved by Z-transform to find the locking range as in the case for the Conventional Digital Tanlock loop (CDTL) [36]. Consequently, the difference equation is solved numerically using the fixed-point theorem [11, 50] as the in the case of the ZC-DPLLs [48, 49].
The characteristic function of the phase detector can be derived by defining the function fγ=-π+(γ+πmodulo(2π) due to the four quadrant nature of the arctan phase detector to distinguish between the four quadrants. Therefore, e(k)is given by
ek=ftan-1sinϕ(k)sinϕk+ψ
(3.14)
Thus, the characteristic function hψϕof the phase detector is nonlinear and depends on the input frequency ω and the time delay τ it is given by
hψϕ=ftan-1sinϕsinϕ+ψ
(3.15)
The function hψϕ can equivalently be expressed in terms of the ratio W=ωoω and nominal phase shift ψo=ωoτ as follows
hψϕ=ftan-1sinϕsinϕ+hψW
(3.16)
The mathematical analyses for both first- and second-order TDTL loops are presented next in this section. Starting with a first-order TDTL loop, the digital filter transfer function Dk is simply a gain block G1; therefore, the system difference equation is given by the following equation which is evaluated by direct substitution of the digital loop filter into (3.13)
ϕk+1=ϕk-K1'hϕk+Λo
(3.17)
where K1'=ωG1, if K1 defined as ωoG1 ,therefore K1'=K1W where W=ωoω.

The steady state phase error for the first-order loop at the input of the phase error detector was derived by seeking the fixed-point of (3.17) as shown below

gϕ=ϕ-K1'tan-1sinϕ(k)sinϕk+ψ+Λo 3.18

which is

ϕss=g ϕss
3.19

The sequence ϕk defined by the (3.16) will converge locally to the solution ϕss if

g'ϕss <1
(3.20)

From (3.14) to (3.20) the steady state output of the phase detector ess is

ess=ftan-1sinϕsssinϕss+ψ=Λo K1'
(3.21)

Since f.<π . Therefore

Λo K1' <π
(3.22)

From (3.21) it can be shown that

tan-1ϕss=sinψtannη1-cosψtannη
(3.23)
Where η=Λo K1'. The exact expression of the steady state ϕss is

ϕss=α, αsinη≥0 fα+π, otherwise.
3.24

Where both α and β are defined as

β=sinψtannη1-cosψtannη=sinψcotη-cosψ
(3.25)

α=tan-1β
(3.26)

From (3.15), (3.18) and (3.19) the following can be derived

1-K1'sinψsin2ϕss+sin2(ϕss+ψ) <1

(3.27)

Using (3.26) therefore (3.27) will be

1-K1'sinψsin2α+sin2(α+ψ) <1

(3.28)

Using both (3.28) and(3.22) inequalities. Therefore, the locking range can be given as

21-W<K1<2W sin2α+sin2(α+ψ)sin(ψ)
(3.29)
21-W<K1<2W sin2α+sin2(α+ψoW)sin(ψoW)
(3.30)
where ψo is the nominal phase lag induced on the incoming signal by the time delay unit, α=tan-1β , β=sinψtannη1-cosψtannη=sinψcotη-cosψ and η=Λo K1' . The steady state value of the phase error is given by ϕss=α+jπ where j∈{1,0,-1}. The locking range of the first-order with a nominal phase shift π2 is shown in Figure 3.. The figure shows that wider locking range can be achieved by setting the loop filter gain to K1=1.

Figure 3. Locking range of the first-order TDTL, $K_1 = G_1\ \omega_o$ and $W=\omega_o / \omega$.
The characteristic function of the phase detector and its first derivative are continuously differentiable in the principal interval –π,π, hence fixed-point analysis is applicable to the TDTL. Following fixed-point analysis developed in [57, 58, 59] for the sinusoidal digital phase-locked loop to define the convergence time, the Lipschitz constant can be given by
L=maxgϕ-gϕss ϕ-ϕss
3.31
where gϕ as expressed in (3.18). The asymptotic estimate (upper bound) to the number of steps required for convergence of the phase error ϕk within a radius ϵ of the fixed point ϕss is given by
m=int lnϵϕ-ϕsslnL+1
3.32
where int . is the integer function.
It can be shown that the time required to reach the fixed-point steady state ϕss is given by
Tc=mToW+ϕm-θoω≈mToW
3.33
where ϕm-θoω≪mT0W

Mathematical Model and Analysis of the Second-order TDTL

The second-order TDTL loop has similar architecture to that of the first-order loop that is controlled by a DCO as shown in Figure 3..

Figure 3. Block diagram of the second-order TDTL.
The second-order loop, as shown in Figure 3., utilizes a proportional plus accumulation digital filter with a transfer function Dz
Dz=G1+G2(1-z-1)
(3.34)

where G1and G2 are positive constants. From (3.13), (3.14) and (3.34), the system difference equation of the second-order TDTL can be achieved as follows in (3.35). This is done by evaluating the phase difference ϕ for a three consequence samples k ,k+1 and k+2 then substitute the phase difference of consequence samples with each other to arrive to the following as

ϕk+2=2ϕk+1-ϕk-rK1'hϕk+1+K1'hϕk (3.35)

where r=1+G2G1 and K1'=G1ω.

In the steady state all consequence samples are equals ϕk+2=ϕk+1=ϕk, consequently hϕk+1=hϕk and ek+1=ek. Therefore, the steady state value of the phase detector output ess is equal to zero. From (3.13) it is clear that the phase error ϕss is nπ (where n is an integer). As fϕss≠±π consequently fϕss is equal to zero, therefore ϕss=2mπ (where m is an integer).

Following the same procedure as in [11, 36] with a fixed-point analysis as in [60] the second-order TDTL locking condition can be obtained from the condition that the eigenvalues of the matrix G given by

01-1+K1'csc(ψ)2-rK1'csc(ψ)<1

(3.36)

If 0<fψ< π, then the matrix G in (3.36) is similar to the matrix (2.9) in [60] with only replacing K1' with K1'csc(ψ). Thus the second-order TDTL locking range is given by

0<K1< 41+r W sinψoW

(3.37)

If-π<fψ< 0, then the matrix G in (3.36) is similar to the matrix (2.11) in [60] with only replacing K1' with -K1'csc(ψ) and the condition that are mutually exclusive with (3.35) are achieved.

The locking range of the second-order with a nominal phase shift π2 (rad) is shown in Figure 3.. The locking range for both first- and second-order TDTL dependent of the initial phase error effect are studied in more details in [50]. Different width of the looking range can be easily obtained by changing the loop gain up and down. This can be demonstrated by different enhanced arctan based architectures in the following chapters.

Figure 3. Second-order TDTL locking range with r =1.2, $K_1 = G_1$ ω_o and $W = \omega_o / \omega$.

The convergence of the second-order loop is directly controlled by the samples produced by the DCO which are used to control the loop filter. This is due to the fact the accumulation process of the proportional plus accumulation loop filter to reach the steady state is directly work with the DCO samples. Therefore, without the DCO samples the filter won't be able to approach the steady state.

TDTL Loop Noise Analysis

For the purpose of the noise analysis, it is assumed that the signal is corrupted by an AWGN with a zero mean and two sided power spectrum density of Gnwf=no/2, where no represents the noise power which is the same at all frequencies. Therefore, the autocorrelation can be given by the

inverse Fourier Transform of Gnwf as $R\tau=n_o\delta(\tau)/2$ [2, 7, 61, 62] , where $\delta\tau$ represents the Dirac Delta function. As a result, $R\tau=0$ for $\tau\neq0$ so any two different samples of this kind of noise are uncorrelated and for this reason they are statistically independent [2, 62, 63]. The noise samples $\eta(k)$'s are mutually independent at any k instant. Therefore, the phase error process ϕk can be regarded as a first-order, discrete time, and continuously variable Markov process which is also governed by modulo2π. The variable Markov process states that the first-order Markov process depends only on the previous state. As a result with a given initial phase error $\phi0$, the pdf of ϕk will satisfy the Chapman-Kolmogorov equation [11, 36, 50].
Assuming that the sampled noise process $\{\eta(k)\}$ is a sequence of independent and identical disturbance (i.i.d) Gaussian random variables with zero mean and a variance $\sigma n2$ it follows that the phase shifted noise process $\{\eta'(k)\}$ is also a sequence of i.i.d with the same mean and variance. Both input xk and its shifted version yk are independent Gaussian random variables [36], Therefore, both can be express as follows

$$Exk=A\sin\phi k \quad (3.38)$$

$$Eyk=A\sin\phi k+\psi \quad (3.39)$$

E Represents the expectation (mean)

Consequently, the combined probability density function (pdf) g(x,y) at any sampling instant k of the Gaussian random variables x and y is given by [11]

$$g\psi,\phi x,y=\frac{1}{2\pi\sigma n2}\exp-\frac{1}{2\sigma n2}(x-A\sin(\phi k)2+y-A\sin\phi k+\psi2 \quad (3.40)$$

where for simplicity x and y are used to represent x(k) and y(k) respectively.
In the conventional CDTL the characteristic function is linear and there is no phase transformation as the case for the TDTL which has nonlinear transformation characteristics of the input phase. In the presence of AGWN noise both x and y has a disturbance effect on both amplitude and phase. [11]. To find the probability density function (pdf) of the random phase of both x and y and their relation to the deterministic phase, they should be written in terms of new random variables Rk (for Amplitude) and ϵ (for phase) such that the random variables x and y keep the same relationship between them as in the deterministic case. This provides for the TDTL the following transformation

$$xk=Rk\sin\epsilon \quad (3.41)$$

$$yk=Rk\sin\epsilon+\psi \quad (3.42)$$

where both random variables Rkand ϵ have the following limits $0<Rk<\infty$ and $-\pi<ek<\pi$. Therefore, the joint pdf of Rk and ϵ is give by [63]

$$p\psi,\phi Rk,\epsilon=g\psi,\phi Rk\sin\epsilon,Rk\sin\epsilon+\psi\ \sin\epsilon Rk\cos\psi\sin\epsilon+\psi Rk\cos\epsilon+\psi \quad (3.43)$$

Usually in DPLLs, the concentration is on phase rather than the amplitude. Therefore, the pdf of the input phase random variable ϵ can be computed by integrating the joint pdf of Rk and ϵ from zero to infinity with respect to Rk as given by

$$p\psi,\phi\epsilon = \int_{0}^{\infty} p\psi,\phi Rk,\epsilon dRk$$
(3.44)
which can be given in the following form
$$p\psi,\phi\epsilon = h\psi'\epsilon \frac{1}{2\pi} \exp{-\mu\psi,u\alpha} + \mu\psi,u\alpha\pi\cos H\psi,\phi\epsilon \times \exp{-\mu\psi,u\alpha} \sin 2H\psi,\phi\epsilon \times \frac{1}{2} + \operatorname{erf}\sqrt{2}\mu\psi,u\alpha\cos H\psi,\phi\epsilon$$ (3.45)
where
$$\alpha = \frac{A^2}{2\sigma n^2}$$ Signal to Noise Ratio SNR
(3.46)
$$h\psi'\epsilon = \frac{dh\psi(\epsilon)}{dek} = \frac{\sin(\psi)}{\sin 2\epsilon + \sin 2(\epsilon+\psi)}$$
(3.47)
$$\mu\psi,u = \sin\psi h\psi'\phi$$
(3.48)
$$H\psi,\phi\epsilon = h\psi\epsilon - h\psi\phi$$
(3.49)
$$\operatorname{erf} x = \frac{1}{2\pi} \int_{0}^{x} e^{-\frac{t^2}{2}} dt$$
(3.50)
where $h\psi.$ is defined in (3.16) and $f\gamma = -\pi + (\gamma + \pi \text{ modulo } (2\pi)$
It is clear that $p\psi,\phi\epsilon$ is non-Gaussian and periodic in ϵ and ϕk with a period of 2π as it is function of $f\gamma$. It is also non-symmetric about the plane $\epsilon = \phi k$ for $\psi \neq \frac{\pi}{2}$. For $\psi = \frac{\pi}{2}$ therefore $h\psi'\epsilon = 1$, $H\psi,\phi ek = f\epsilon - f\phi(k) = \epsilon - \phi(k)$ in the principal interval $(-\pi,\pi)$ and $\mu\psi,u = 1$, consequently (3.45) is reduced to the equation as in [36] which is also will be shown in chapter 6.
As a result, from the above analysis, the output of the phase detector is also non-Gaussian random variable ξ which is given by
$$\xi = h\psi'\epsilon = f\tan^{-1}\frac{\sin e k \sin e k + \psi}{}$$
(3.51)
As the function was shown to be continuous over the principal interval $(-\pi,\pi)$ [11]. Also $dh\psi(\phi)d\phi > 0$ since $0 < \sin\psi < 1$. Therefore, $h\psi\phi$ is increasing in the principle interval consequently the pdf of ξ can be given by [64]
$$P\psi,\phi\xi = ph\psi^{-1}\xi d\epsilon d\xi$$
(3.52)
From equations (3.15), (3.45), (3.51) and (3.52) the following can be obtain
$$P\psi,\phi\xi = \frac{1}{2\pi} \exp{-\mu\psi,u\alpha} + \mu\psi,u\alpha\pi\cos\xi - h\psi\phi \times \exp{-\mu\psi,u\alpha}\sin 2\xi - h\psi\phi \times \frac{1}{2} + \operatorname{erf}\sqrt{2}\mu\psi,u\alpha\cos(\xi - h\psi\phi)$$
(3.53)
which is periodic in ξ of period 2π. When $\xi = h\psi\phi$ equation (3.53) has it maximum value, hence $\xi - h\psi\phi$ has zero expected value irrespective of ϕ and ψ. Therefore, ξ can be decomposed as follows
$$\xi = \epsilon + \eta$$
(3.54)
where $\epsilon = h\psi\phi$ is the deterministic transformed phase and η is non-Gaussian phase noise with a mean of zero. If ξ is considered in the interval $(-\pi,\pi)$, therefore the phase noise lies in the interval of $(-\pi-\epsilon,\pi-\epsilon)$. As a result, the pdf of the phase noise can be given explicitly as follows [11]
$$P\psi,\epsilon\eta = \frac{1}{2\pi} \exp{-m\psi,\epsilon\alpha} + m\psi,\epsilon\alpha\pi\cos\eta \exp{-m\psi,\epsilon}\sin 2\eta \times \frac{1}{2} + \operatorname{erf}\sqrt{2}m\psi,\epsilon\alpha\cos\eta$$
(3.55)
where $m\psi,\epsilon = \mu\psi,h\psi^{-1}(\epsilon)$
This pdf has similar results obtained for the CDTL, except for the additional factor $m\psi,\epsilon$. The additional factor will not affect the expected value, which

will always be zero as in the case for the CDTL, but the variance will depends on both ψ and ϵ [11].

The system steady state equation of the first-order TDTL in the presence of noise can be obtained from equations (3.13) and (3.17) with the addition noise to these equations [11, 36]

$$\phi k+1=\phi k-K1'h\psi\phi k+\Lambda o+K1'\eta k \quad (3.56)$$

where ϕk is the phase error at the input of the phase detector and hψϕk=e(k) is the phase error at the output of the PD. As noted previously that η(k)'s are mutually independent for different k. Thus, one can regards that the phase error ϕk as a first order, discrete time, continually variable Markov process. Accordingly, giving the initial phase error ϕ(0), the pdf of ϕk satisfies the following Chapman-Kolmogorov equation [11, 36, 65] :

$$p\psi,k+1\phi\phi o=-\infty\infty q\psi,k\phi up\psi,ku\phi odu \quad (3.57)$$

where ϕo=ϕ(0) initial phase error, pψ,kϕϕo is the pdf of the ϕ(k+1) given ϕoand qψ,kϕu is the pdf of ϕ(k+1) given ϕk=u , which is given in case of the TDTL by

$$q\psi,k\phi u=12\pi K1'\exp-\mu\psi,u\alpha +1K1'\mu\psi,u\alpha\pi\cos(\phi-vK1')\exp-\mu\psi,u\alpha\sin2\phi-vK1' \times12+\operatorname{erf}2\mu\psi,u\alpha\cos\phi-vK1' \quad (3.58)$$

where all parameters are defined from (3.45) to (3.51), v=u-K1'hψu+Λo and the range of ϕ is the interval (u+Λo-K1'π,u+Λo+K1'π).

This iteration can be solved numerically using the Weinberg-Liu method explained in [11, 36, 64]. This is to get the steady state error at the PD input Pψϕ. As a results the steady state error at the PD output is given by

$$P\psi e=P\psi h\psi-1(e)d\phi/de \quad (3.59)$$

Where e=hψ(ϕ)

From the above analysis it is deduced that both input and output steady state phase error pdfs are dependent on Λo, ψ=ψo/W, K1'=K1/W and SNR. In contrast for the conventional CDTL phase error pdf depends only on Λo, K1' and SNR [36] .

At the input of the PD in the steady state the expectation E[ϕk+1]=E[ϕk]. Also it is the same at the PD output E[ek+1]=E[ek]. As it is know that at the presence noise, the steady state phase errors ϕss and ess are random variable, therefore, the expectation ε of both side of equation (3.56) under the steady state and solving for E[ϕss]

$$Eess=Eh\psi\phi ss=\Lambda o-K1' E\eta/K1' \quad (3.60)$$

where essis the steady state output of the PD. Since the pdf of the phase noise is symmetric about zero, therefore E[η]=0, hence the expectation

$$Eess=\Lambda oK1' \quad (3.61)$$

which is the same as the noise free expression of ess, therefore in AGWN, the first-order TDTL will not lose tracking of the input phase error since the expected value of the phase error equals its deterministic value.

When the first-order TDTL is in the tracking mode then tan-1sinϕ(k)sinϕk+ψ≈ϕ for small ϕ which results in

$$\sigma\phi2=E\phi2-\phi12=Kn'2\sigma n2\ K1'\cos\phi12-\cos\phi1 \quad 3.62$$

Where ϕ1 is the locked state phase error.

This is a linearised variance of the phase error with a mean of ϕ1 which results in a phase error pdf of

pϕ=1σn2πexp-ϕ-ϕ122σn2

(3.63)

The theoretical pdf for different values of signal-to-noise ratio (SNR) is illustrated in Figure 3. using (3.63). This figure shows the effect of the AWGN on the steady state phase error of the PD. It is clearly shown that as SNR increases the steady state pdf increases.

Figure 3. Steady state phase error PDF of the first-order TDTL for different SNR values, K_1 =1 and without frequency step.

The system steady state equation of the second-order TDTL, in the presence of noise, can be obtained from equations (3.13, 3.17, 3.35 and 3.56) with addition of noise [11] .

ϕk+2=2ϕk+1-ϕk-rK1'hϕk+1+ηk+1

+K1'hϕk+ηk

(3.64)

Applying the same previous procedure and taking the expectation of both sides with noting that the E[η]=0 at the sampling instant k, therefore the expected value of the phase error at the phase detector output will be

Eess=0

(3.65)

which is exactly the same case for the free noise situation, therefore, in AGWN, the second-order TDTL also will not lose tracking of the input phase error since the expected value of the phase error equals its deterministic value.

When the second-order TDTL in tracking mode therefore tan-1sinϕ(k)sinϕk+ψ≈ϕ which results in

Eϕ2=r2+12-K1'-2r(2-rK1')K1'(2-K1')2-(2-rK1')2Kn2σn2

(3.66)

This result in a linearized variance of Eϕ2 with a zero mean Eϕ=0, therefore the pdf is

p(ϕ)=1σn2πexp-ϕ22σn2

(3.67)

The theoretical pdf for different SNR ratio was illustrated as shown in Figure 3..

Figure 3. Steady state phase error PDF of the second-order TDTL for different SNR values, K1=1, r=1.2 and without frequency step.

TDTL Loop Limitations

The performance of the TDTL has been assessed by testing it in noise-free and noisy environments. In noise-free environment, the system was tested by subjecting it to sudden changes in frequency either above or below the DCO free running frequency using positive and negative frequency steps. The time delay and DCO free running frequency values are selected so that the initial phase-lag parameter ψo=ωoτ=π2 and the gain K1=G1ωo=1. The effect of applying a positive input frequency step of 0.5 V with respect to the DCO frequency (i.e. W=ωoωin=0.667) to the loop is shown in Figure 3..

Similarly, the effect of a negative input step of -0.3 V, corresponding to W=ωoωin=1.428, is depicted in Figure 3.. Both figures show that the phase response of the first-order loop reached the steady state within the time of few samples reached to 5 cycles for the positive step and 10 samples for the negative step. Depending on the particular application this number of samples may not be acceptable. Therefore, reducing the time to reach steady state, i.e. the acquisition time, is a worthwhile objective for a PLL designer.

(a)

(b)

Figure 3. (a) Positive input frequency step of 0.5 V and (b) Phase error response of the first-order TDTL.

(a)

(b)

Figure 3. (a) Negative input frequency step of -0.3 V and (b) Phase error response of the first-order TDTL.

Another significant limitation of the first-order TDTL, which is worth considering, is the non-zero phase error in the steady state. This limitation can be overcome by using a second-order loop. However, this leads to degradation in the loop acquisition time and locking range as will be shown later. In a noisy environment test, the input signal is corrupted by an AWGN and both pdf and the average jitter were evaluated for an input with a SNR of 10 dB and different frequency steps with regards to the DCO free running frequency as shown in Figure 3. and Figure 3. respectively. Both figures show that there is a good scope for improving the noise immunity of the TDTL system.

Figure 3. Variations of the noise performance of the first-order systems with the SNR=10 dB, K_1 =1 with different frequency steps.

Figure 3. First-order jitter performance for a range of SNR, frequency step of 0.1 V, and K_1 =1.

The same performance tests were also applied to the second-order TDTL system. The output phase error performance following the application of a positive step of 0.3 V then a negative step of -0.3 V is shown in Figure 3. and Figure 3. respectively. These figures show that the steady state phase error of the second-order loop does converge to zero. Again, improving the loop locking speed is a desirable parameter as some applications require fast synchronization such as FM and FSK demodulations.

(a)

(b)

Figure 3. (a) Positive input frequency step of 0.3 V and (b) Phase error response of the second-order TDTL.

(a)

(b)

Figure 3. (a) Negative input frequency step of -0.3 V and (b) Phase error response of the second-order TDTL.

Further the input signal is corrupted by AWGN and both pdf and the average jitter are evaluated for an input SNR of 10 dB and different frequency steps as in with the first-order which is shown in Figure 3. and Figure 3. respectively. Both figures show that the noise immunity of the second-order TDTL also requires enhancement.

Figure 3. Variations of the noise performance of the first-order systems with the SNR=10 dB, K_1 =1 and different frequency steps.

Figure 3. Second-order jitter performance for a range of SNR values, frequency step of 0.1 V, and K_1 =1.

The above mathematical models and subsequent simulation results, for both the first-and second-order TDTL, highlighted some limitations of the present TDTL system. Overcoming these limitations will obviously result in improvements in the system performance for both loop orders i.e. first- and second order TDTLs. The limitations to be overcome are:

- The nonlinearity problem in both the first- and second-order TDTL loops caused by the fixed delay unit due to variations in the phase error with the frequency of the input signal. This is shown in equations (3.30) and (3.37) and illustrated in Figure 3. and Figure 3..
- The locking range of the second-order TDTL is somewhat restricted and can be enhanced.
- From Equations (3.23) and (3.24) and as can be deduced from Figure 3. and Figure 3., the acquisition speed of the first-order TDTL is rather low and can be enhanced.
- The phase error in the second-order TDTL takes relatively long time to reach to zero, as depicted in Figure 3. and Figure 3., due to the fact that the first-order loop filter is controlled by the samples produced by the DCO as it has an accumulative nature that is controlled by the samples produced by the DCO.
- The first-order TDTL has a non-zero steady state phase error.
- From Equation (3.30) and as can be deduced from Figure 3. , Figure 3., Figure 3. and Figure 3., the TDTL noise immunity is limited and an improvement would be gainful.

Conclusions

This chapter presented a detailed mathematical analysis and modelling of the digital phase-locked loop (DPLL) based on the time delay digital tanlock loop (TDTL) in both noisy and noise free environments. It also highlighted the limitations of the original time delay digital tanlock loop architecture in terms of performance parameters, such as the linearity of the phase detector, acquisition time, locking range and noise immunity. These performance parameters were evaluated by conducting different tests such as step functions and an input with a corrupted signal with additive white Gaussian noise (AWGN). From the preceding mathematical models and subsequent simulation results, it is clear that the TDTL architecture has some limitations mainly in the areas of linearity, acquisition speed and noise performance. Alleviating these limitations is the focus of the research work described in this thesis.

4 FIRST-ORDER TDTL WITH ENHANCED ARCHITECTURES

Introduction

This chapter describes the techniques developed during the research work described by this thesis so as to improve the performance of the original TDTL by alleviating the limitations discussed in the previous chapter; locking range, acquisition speed, and noise performance. The chapter also discusses the selection of the optimum design upon a required application. The improvements to the TDTL presented in this chapter are based on designing auxiliary aided circuits. In addition, every new TDTL system is analysed using as systematic test tool which consists of the following procedure:

- Demonstrate and illustrate the effect of system linearity on the locking range of the proposed architecture;
- Evaluate the acquisition performance of each new TDTL architecture by applying positive and negative step frequency changes to the input signal frequency relative to the free running frequency of the DCO using a positive of 0.3 V and negative of -0.3 V frequency steps respectively.
- Assess the acquisition performance by applying a frequency shift keying (FSK) and frequency modulation (FM).
- Appraise the noise performance by evaluating the effect of AWGN on the performance of the proposed architectures and gauge the effects using pdf and jitter with a frequency step of 0.1 V. For the pdf test the input signal of SNR= 10 dB was used, while for the jitter evaluation a range of input SNRs between 0 dB to 20 dB were used.

TDTL with a Linearized Phase Detector (TDTL-LPD)

As previously mentioned, the nonlinearity problem in first-order TDTL limits the performance of the loop. This is caused by using of a fixed time delay unit which produces different phase shifts for similar changes in the input signal frequency. It affects both the system characteristic phase detector and consequently the locking range. To reduce this nonlinearity, an improved TDTL architecture with a linearized phase detector (TDTL-LPD) has been introduced in which the fixed time delay is replaced by a variable time delay unit [60]. The architecture of the TDTL-LPD is shown in Figure 4. which shows that the system resembles the original TDTL in all of its components except for the phase linearization controller and the variable ‘adaptive’ time delay blocks.
In the TDTL-LPD system, the phase linearization controller assesses the value of the error resulting from changes in the frequency of the input signal, while the loop is in locked state. This is used to compensate for the

nonlinear variations in the phase by adjusting the adaptive time delay block so that y(t) and x(t) maintain their quadrature relationship.

Figure 4. Block diagram of the first-order TDTL-LPD.

The basic concept of the TDTL-LPD can be clarified further by studying the phase shift relationship as explained below.

$$\psi=\omega\tau \quad (4.1)$$

where ψ (rad) is the phase shift, ω is the angular frequency (rad/s) and τ (s) is the time delay introduced by the variable time delay unit. The phase linearization controller block, compensates for changes in the input frequency in such a way so as to produce a fixed phase shift ψ as long as the system is operating within its locking range. Therefore, changes in the frequency of the incoming signal will be compensated for by a specific value of delay that is produced by the controller in order to maintain the $\pi 2$ (rad) phase shift all the time as in (4.1). Equation (4.1) shows that for any increase in the input signal frequency there should a decrease in the time delay to have a phase shift ψ fixed at $\pi 2$ (rad) as it is clearly illustrated in Figure 4..

$$\psi=\omega\tau=2\times\pi\times f\times\tau=\pi 2 \text{ rad} \quad (4.2)$$

Figure 4. Effect of change in the input signal frequency on the required time delay to provide a fixed phase shift of π/2 (rad).

Figure 4. shows a comparison between the conventional TDTL and the TDTL-LPD phase detector characteristics. The nonlinear parts of the graphs in Figure 4. correspond to the TDTL while the straight one for the TDTL-LPD.

Figure 4. Phase detector characteristics of both TDTL-LPD and TDTL.

By fixing the phase shift ψ value to $\pi 2$, the phase shifted signal xk, given by (3.4), can be re-written as

$$xk=A\sin\omega otk+\theta k-\pi 2$$
$$=A\cos\omega ot(k)+\theta k \quad (4.3)$$

This is similar to the CDTL [36], therefore, the discretized signals generated by the samplers are

$$yk=A\sin\theta(k)-\omega oi=0k-1c(i) \quad (4.4)$$

and

$$xk=A\cos\theta(k)-\omega oi=0k-1c(i) \quad (4.5)$$

Consequently, both Equations (4.4) and (4.5) can be expressed in term of the phase error as

$$yk=A\sin\phi k \quad (4.6)$$

And the shifted signal

$$xk=A\cos\phi(k) \quad (4.7)$$

The loop error signal ek produced by the phase detector can be evaluated as

$$ek=f\tan-1\sin\phi(k)\cos\phi k=f\phi(k) \quad (4.8)$$

where fγ=-π+[γ+πmod 2π]. As a result, the locking range of the first-order TDTL, which was analyzed in details in [36, 66], can be given as

21-W<K1<2W sin2α+sin2(α+π2)sin(π2)

21-W<K1<2W -2-2+cosα+cosπ+2α (4.9)

which is simplified to

21-W<K1<2W

(4.10)

where ϕss=α+jπ and j∈{1,0,-1} is the steady state phase error.

Figure 4. Locking range of the first-order TDTL-LPD, $K_1 = G_1 \omega_o$,$W=\omega_o / \omega$ and ψ=п/2 (rad).

As shown below, the response of the TDTL-LPD shows marked improvement compared to the original TDTL by a reduction of three cycles. This means that the TDTL-LPD took 2 cycles to reach the steady state compared with 5 cycles for the original TDTL for the positive step. While for negative step the TDTL-LPD took 3 cycles compared with 6 cycles for the original TDTL.

Figure 4. and Figure 4.; illustrate the response of the TDTL-LPD and the TDTL to positive of 0.3 V and negative of -0.3 V frequency steps respectively. In both cases, it can be shown that TDTL-LPD requires less number of samples to achieve locking state. The phase plane plots is also a different way to evaluate the acquisition responses which is also shows the same results, as depicted in Figure 4..

(a)

(b)

Figure 4. First-order response for a positive input frequency step of 0.3 (a) TDTL-LPD phase error response and (b) TDTL phase error response $K_1 = 1$ and ψ=п/2 (rad).

(a)

(b)

Figure 4. First-order response for a negative input frequency step of -0.3 (a) TDTL-LPD phase error response and (b) TDTL phase error response, $K_1 = 1$ and ψ=п/2 (rad).

(a)

(b)

Figure 4. First-order phase planes of (a) TDTL-LPD and (b) TDTL for a positive frequency step of 0.3 V, $K_1 = 1$ and ψ=п/2 (rad).

Figure 4., Figure 4. and Figure 4. show improvements in the acquisition time of the first-order TDTL by using the TDTL-LPD architecture. This is due to the fact that this architecture is using a fixed phase shift value for all incoming signal frequencies which will linearize the PD.

This noise performance test presents the effect of AWGN on the performance of the proposed loop architecture and the performances are measured using pdf with a frequency step of 0.1 V affect. The effect of

AWGN, with an input signal of SNR=10dB, on the performance of both TDTL-LPD and TDTL was tested with a simulation results shown in Figure 4.. It is shown from the plots that the TDTL-LPD outperforms TDTL, by a value of 0.4 in pdf scale, due to the nonlinearity produced by the original TDTL that affects its noise performance. The impact of noise on the jitter performance of both TDTL-LPD and TDTL loops was tested and the results are shown in Figure 4.. As can be seen from the figure, the average jitter for TDTL-LPD is lower by 0.8 seconds on the best case than the one produced by TDTL. This proves that the loop is used only to enhance the reduction in phase noise. This improvement is decreased as the SNR increases.

Figure 4. TDTL-LPD and TDTL noise performance for SNR=10dB and frequency step 0.1 V.

Figure 4. TDTL-LPD and TDTL jitter performance for a range of SNR, frequency step 0.1 V.

TDTL with Pre-Distortion Technique

Nonlinearity is a problem that has a severe effect on the performance of different communication system blocks especially power amplifiers (PA). The output signal of a PA is splatter onto adjacent radio frequencies due to the nonlinearity affecting the signal demodulation process at the receiver. Therefore, a linearization technique could be used to solve this issue. Among the different possible linearization techniques, pre-distortion is popular. It consists of adding a pre-distortion function, usually a look-up table (LUT), before the PA which is complementary to the PA one in such a way that the cascade of the two distortions leads to a linear response. It simply pre-distorts the input of the implemented PA to cancel the nonlinearity and is ideally the inverse of the PA transfer function [67, 68, 69].

Due to the nonlinearity of the original TDTL, a feedforward pre-distortion is used to linearize the PD characteristics as depicted in Figure 4.. This figure shows the block diagram of the proposed architecture using a LUT [70]. The LUT matching input/output data can be achieved by mapping the values of TDTL-LPD in comparison with the pre-distortion TDTL as depicted in Figure 4.. The figure illustrated the sampled signal x(k) response of a ramp frequency changes in the input signal for both TDTL-LPD and TDTL. Using this figure an input/output data can be stored in the LUT. Figure 4. shows a comparison between the pre-distortion TDTL and the TDTL-LPD phase detector characteristics. The figure shows a close similarity between pre-distortion TDTL and the TDTL-LPD. The slight nonlinearity generated when using the pre-distortion method can be controlled by the number of points taken to match the input/output of the LUT i.e. by improving the resolution of the lookup table.

Figure 4. Architecture of the modified TDTL using a feedforward pre-distortion technique.

Figure 4. x(k) value for a ramp frequency changes in the input signal of both TDTL-LPD and TDTL with pre-distortion.

Figure 4. Phase detector characteristics of both pre-distortion TDTL and TDTL-LPD.

Referring to Figure 4.10, and following the same analysis procedure of the TDTL both digitized yk and xk can be written as

yk=Asinθ(k)-ωoi=0k-1c(i)

(4.11)

and

xk=Acosθ(k)-ωoi=0k-1c(i) ±δ

(4.12)

where δ is the nonlinearity factor that comes from LUT input/output accuracy matching. Consequently, the phase error difference between the input incoming signal and the DCO can be defined as

ϕk=θ(k)-ωoi=0k-1ci-ψ

(4.13)

where ψ= π2 ,therefore, both (4.11) and (4.12) can be expressed in term of the phase error as

yk=Acosϕk ±δ

(4.14)

and

xk=Asinϕ(k)

(4.15)

The loop error signal ek produced by the PD can be expressed as

ek=ftan-1sinϕ(k)cosϕk±δ

(4.16)

where fγ=-π+[γ+πmod 2π].

The mathematical analyses for both first- and second-order loops are given below. Starting with a first-order TDTL loop, the digital filter transfer function Dk is simply a gain blockG1, therefore the system difference equation is given by

ϕk+1=ϕk-K1'hϕk+Λo (4.17)

where K1'=ωG1, if K1 defined as ωoG1 ,therefore K1'=K1W where W=ωoω. Therefore, the locking range can be given as

21-W<K1<2W sin2α +sin2(α+π2)±δ (4.18)

where ϕss=α+jπ , j∈{1,0,-1} is the steady state phase error and δ is a tolerance factor decreases as the number of points stored in the LUT are increases. The locking range for the first-order pre-distortion TDTL is shown in Figure 4..

Figure 4. Locking range of the first-order pre-distortion TDTL K_1 =1 and ψ=π/2 (rad) and δ=0.01.

The same performance acquisition used for the original TDTL, by applying rapid changes in the input signal frequency, was performed to assess the effect of pre-distortion. As shown below, the response of the pre-distortion TDTL shows good improvement compared to the TDTL due to the nonlinearity.

Figure 4. and Figure 4., illustrate the response of the pre-distortion TDTL and the original TDTL to positive 0.3 V and negative -0.3 V frequency steps respectively. In Figure 4. the pre-distortion TDTL required 3 cycles compared with 5 for the original TDTL to reach the steady state, while for a negative step, Figure 4., the original TDTL requires 6 cycles compared to 4 cycles for the pre-distortion TDTL. The phase plane plots of both loops, when they are in lock, are depicted in Figure 4. which shows the same results illustrated by Figure 4. and Figure 4..

(a)

(b)
Figure 4. First-order response for a positive input frequency step of 0.3 V (a) Pre-distortion TDTL phase error response and (b) TDTL phase error response, K_1 =1 and ψ=π/2 (rad).

(a)

(b)
Figure 4. First-order response for negative input frequency step of -0.3 V (a) Pre-distortion TDTL phase error response and (b) TDTL phase error response, K_1 =1 and ψ=π/2 (rad).

(a)

(b)
Figure 4. First-order phase planes of (a) Pre-distortion TDTL and (b) TDTL with a positive frequency step of 0.3 V, K_1 =1 and ψ=π/2 (rad).
The effect of AWGN, with an input signal pdf of SNR=10dB and with a frequency step of 0.1 V, on the performance of both pre-distortion TDTL and TDTL was tested and the simulation results are presented in Figure 4.. These show that the pre-distortion TDTL outperforms TDTL, by a value of 0.5 in pdf scale which means that is is less spread compared with the original TDTL pdf. The impact of noise on the jitter performance of both pre-distortion TDTL and TDTL loops was tested and the results are shown in Figure 4.. The average jitter for pre-distortion TDTL is lower by 0.09 second on average than the one produced by TDTL. This indicates that the pre-distortion scheme simply reduces the phase noise by improving the linearity of the TDTL loop.

Figure 4. pre-distortion TDTL and TDTL noise performance for SNR=10 dB and frequency step 0.1 V.

Figure 4. pre-distortion TDTL and TDTL jitter performance for a range of SNR, frequency step 0.1 V.

Fast Feedback using Rounding

The proposed topology is a feedback (FB) method that depends on the rounding procedure, i.e. rounding the error pulses to the nearest integer

steady state value. The block diagram of the proposed system is shown in Figure 4.. The proposed architecture is a TDTL loop with an added controller after the digital filter. Therefore, it has similar linearity and locking range of the original TDTL.
The controller consists of a gain factor R, its reciprocal gain and a rounding block as shown in Figure 4..

Figure 4. Architecture of the modified TDTL using Fast Feedback using rounding
Rounding is a method used to convert a fractional value to the nearest integer number. Since values produced by the digital loop filter are usually fractional i.e. less than unity, a gain of value R is used to scale up these values to ease rounding. This ensures that the steady state will have a integer number and all ripples to be round. As a result, the rounding block will convert all ripples to the same steady state value. Then the 1/R gain will re-scale the results down to the original steady state values. This method helps the system reach the steady state for both over and under damping even when the system operates near the edges of the locking range due to the fact it eliminates the ripples produced by the system in the transient state which might through the system outside the locking range. This type of design is suitable for Frequency Shift Keying demodulation (FSK) due its discrete nature. Therefore; the R factor is selected upon the number of levels the FSK signal designed for. As an example, if there are ten different frequencies i.e. ten levels, therefore it is required to have R equal to ten. Figure 4. and Figure 4., shows the responses of the both FB rounding and the original TDTL to positive and negative steps respectively. The response of the fast feedback rounding shows a huge improvement compared to the original TDTL which reached steady state in one cycle compared with 5 and 6 cycles for the original TDTL.

(a)

(b)
Figure 4. First-order response for a positive input frequency step of 0.3 V (a) response of the original TDTL (b) Response of the feedback with rounding , K_1=1 and ψ=π/2 (rad).

(a)

(b)
Figure 4. First-order response for Negative input frequency step of -0.3 V (a) TDTL phase error response and (b) Feedback rounding concept phase error response, K_1 =1 and ψ=π/2 (rad).
The performance of the fast feedback with rounding system was also tested using a FSK with different states and the results are compared with the original TDTL system as shown in Figure 4.. A marked improvement is added to the TDTL due to the rounding scheme.

(a)

(b)

(c)
Figure 4. (a) FSK input (b) Feedback Fast concept phase error (c) TDTL phase error, $K_1=1$ and $\psi=\pi/2$ (rad).
As it is shown from Figure 4.(c) and highlighted by a circle, the original TDTL system oscillates as it approaches the locking range edge, which is not the case with the proposed system as it is clearly shown in Figure 4. which is an enlargement of Figure 4.. Consequently, this type of FB method is most suited for FSK demodulation.

(a)

(b)
Figure 4. Enlargement of (a) Feedback fast concept phase error (b) TDTL phase error, $K_1=1$ and $\psi=\pi/2$ (rad).
The noise performance of the feedback rounding concept in comparison with the original TDTL is shown in Figure 4.. It is shown from the plots that the feedback rounding concept outperforms TDTL, by a value of 0.2 in pdf scale. The impact of noise on the jitter performance of both feedback rounding concept and TDTL loops was also tested and the results are shown in Figure 4.. The average jitter for pre-distortion TDTL is slightly lower by 0.05 at the best case.

Figure 4. Feedback fast rounding concept and TDTL noise performance for SNR=10dB and frequency step 0.1 V.

Figure 4. Feedback fast rounding concept and TDTL jitter performance for a range of SNR, frequency step 0.1 V.

Adaptive TDTL Structure Based on Error Correction

A new technique for fast error correction of the TDTL is proposed which is based on early comparison of the input signal frequency with that of the loop filter output. The result of this comparison is then used to select an optimum value for the loop filter output. This technique eliminates the need for continuously changing the loop filter coefficient as it is the case in previous designs [55, 56]. This reduces the complexity of the TDTL structure and improves the acquisition time.
The proposed adaptive TDTL system is shown in Figure 4. [71, 72, 73]. It consists of a time delay unit, two samplers, arctan PD, DCO, controller, and a combined block comprising a FSM and digital loop filter.

Figure 4. Block diagram of the AEC-TDTL.
The controller is used to compare the incoming input signal frequency and the DCO frequency as illustrated in Figure 4.. The proposed system AEC-TDTL (adaptive error correction TDTL) relieves the loop from the burden caused by continuous alteration of the loop filter coefficients as the input frequency changes [55] .

The controller consists of two frequency estimators and a subtractor as shown in Figure 4.. The controller generates two output signals, namely CN and IN. The CN signal is used to control the FSM, as shown in Figure 4. and Figure 4., to either produce a fixed value that emulates the loop filter coefficient or to pass the IN signal which represents the exact value needed by the DCO to immediately reach the steady state value. This approach eliminates cycle slipping, which results from the difference between the incoming signal and the DCO frequency values.

Figure 4. Controller block diagram.

The block diagram of the frequency estimator (FE) is depicted in Figure 4.. It consists of a derivative, gain block, and envelope detector. The envelope detector produces the envelope of the input signal derivative to evaluate the frequency value.

Figure 4. Frequency estimator block diagram.

AEC-TDTL system has similar locking range of the original TDTL. The acquisition performance presented in both Figure 4. and Figure 4. show the effect of AEC-TDTL on the performance of the original TDTL. These figures show that for both negative and positive frequency steps, the AEC-TDTL outperforms the original TDTL.

The phase plane plots of both loops, when they are in lock, are depicted in Figure 4..

(a)

(b)

Figure 4. First-order response for positive input frequency step of 0.3 V (a) TDTL phase error response and (b) AEC-TDTL phase error response, K_1 =1 and ψ=π/2 (rad).

(a)

(b)

Figure 4. First-order response for negative input frequency step of -0.3 V (a) TDTL phase error response and (b) AEC-TDTL phase error response,, K_1 =1 and ψ=π/2 (rad).

(a)

(b)

Figure 4. First-order phase planes of (a) TDTL and (b) AEC-TDTL with a positive frequency step of 0.3 V, K_1 =1 and ψ=π/2 (rad).

Another acquisition performance test of system depicted in Figure 4. was evaluated by injecting an FSK modulated input signal which emulates a train of consecutive frequency steps. Monitoring the system transient response at

the output of the loop filter, for input signals with various parameters, indicates that the proposed AEC-TDTL architecture is capable of achieving a steady state locked condition within a relatively short time. A representative set of the results is demonstrated in Figure 4. that represents the results of AEC-TDTL compared with the original TDTL. It shows that the AEC-TDTL achieves a substantial improvement in acquisition time compared with the original TDTL.

(a)

(b)

(c)
Figure 4. (a) FSK input signal (b) FSK demodulation using conventional TDTL (c) FSK demodulation using AEC-TDTL, K_1 =1 and ψ=π/2 (rad).
The noise performance of the AEC-TDTL in comparison with the original TDTL is shown in Figure 4.. It is shown from the plots that the performance of the AEC-TDTL is worse compared with TDTL, by a value of 0.45 in pdf scale. The impact of noise on the jitter performance of both AEC-TDTL and TDTL loops was tested and the results are shown in Figure 4.. As can be seen from the figure, the average jitter for AEC-TDTL TDTL is higher by 0.05 at the best case. This indicates that the loop is good at enhancing the acquisition time, while it fails to improve the noise performance. The reason is that this kind of architecture used to adapt the loop filter coefficient, has a direct impact on the locking range and consequently the noise performance. As the changes in the locking range size will have a direct effect in the amount of noise entered the loop system.

Figure 4. AEC-TDTL and TDTL noise performance for SNR=10dB and frequency step 0.1 V.

Figure 4. AEC-TDTL and TDTL jitter performance for a range of SNR, frequency step 0.1 V.

Fast Acquisition TDTL using Adaptive Filter

Predicting a signal requires some key assumptions, e.g. assuming that the signal is either steady or slowly varying one with time, periodic, etc. As well accommodating these assumptions lead to fact that the adaptive filter must predict the future values of the desired signal based on past values [74, 75].
When the input signal is periodic and the filter is long enough to remember, previous values can perform the prediction with an addition of a delay to the input signal. In the proposed system, the delay is not required due to the existing delay of the signal produced by the DCO compared with the incoming signal.
The new adaptive TDTL system consists of a time delay unit, two samplers, arctan PD, DCO, digital loop filter, multiplier and adaptive algorithm controller. In other words, without the adaptive algorithm controller and the multiplier, the proposed systems are similar to the original TDTL. This

means that this proposed system has the same difference equation and locking range of the original TDTL.
The adaptive controller block diagram shown in Figure 4. consists of transversal digital filter, LMS adaptive algorithm, adders and a constant of unity.

Figure 4. Block diagram of adaptive algorithm controller.
The LMS algorithm, used in this system, approximates the steepest descent algorithm, which uses an immediate estimate of the gradient vector of a cost-weighted function. Steepest descent algorithm is a first-order optimization algorithm that is used to find the local minimum of a function using gradient descent; one takes steps proportional to the negative of the gradient, or of the approximate gradient, of the function at the current point. The estimate of the gradient is based on sample values of the tap input vector and an error signal. The algorithm iterates over each coefficient in the filter, moving it in the direction of the approximated gradient [65].
It is necessary for the LMS algorithm to have a reference desired signal d[n], which represents the desired filter output. The difference between the reference signal and the actual output of the filter is the error signal
en=dn-y[n]
(4.19)
where d[n] is the desired signal and yn is the reference signal. The desired signal is selected to be the signal coming from the DCO and the input signal represented by the reference incoming signal. In the TDTL or any PLL, there is a slight delay between the incoming signal and the signal produced by the DCO system. Therefore, the delay block depicted in the prediction topology is emulated by this delay between the incoming and the DCO.
Usually, and within the locking range in the steady state, the incoming signal has similar frequency and fixed phase, but it differs in the transient state. Therefore, due to this difference the adaptive filter produces an error that later helps in speeding up the acquisition process. Since the DCO output is selected to be the desired signal, the error produced has an opposite polarity to the ripples produced by the system in the transient response (in dotted blue) as shown in Figure 4.. Adding one to this error will provide the ability to use the multiplier in the feedback loop.

Figure 4. Error produced by the adaptive filter and the transient response ripples.
The proposed new adaptive TDTL system using adaptive filters prediction is shown in Figure 4..

Figure 4. Block diagram of fast acquisition TDTL using adaptive filters.

The response of the TDTL using an adaptive filter in comparison with the original TDTL using the acquisition performance test is shown in both Figure 4. and Figure 4.. As will be shown below, the response of the TDTL using an adaptive filter shows an improvement compared to the original TDTL Figure 4. shows that the adaptive TDTL system requires less number of samples to achieve locking state; one cycle in comparison with 5 cycles for the original

TDTL. Figure 4. illustrates the effect of the negative frequency step, which needs 3 cycles for the TDTL system using adaptive filters in comparison with 5 cycles for the original TDTL. The phase plane plots of both loops, when they are in lock, are depicted in Figure 4..

(a)

(b)
Figure 4. First-order response for positive input frequency step of 0.3 V (a) TDTL phase error response and (b) Fast acquisition TDTL using adaptive filters phase error response, K_1 =1 and ψ=п/2 (rad).

(a)

(b)
Figure 4. First-order response for negative input frequency step of -0.3 V (a) TDTL phase error response and (b) Fast acquisition TDTL using adaptive filters phase error response, K_1 =1 and ψ=п/2 (rad).

(a)

(b)
Figure 4. First-order phase planes of (a) TDTL and (b) Fast acquisition TDTL using adaptive filters phase error response with a positive frequency step of 0.3 V,
K_1 =1 and ψ=п/2 (rad).
A further evaluation of the system is required to evaluate and compare it with the original TDTL. This is done by subjecting the system to an FSK signal with a frequency step as shown in Figure 4.a. This test provides evidence that the proposed system gives better acquisition compared with the original TDTL as shown in Figure 4.b and Figure 4.c.

(a)

(b)

(c)
Figure 4. (a) FSK input signal, (b) FSK demodulation using conventional TDTL,
(c) FSK demodulation using fast acquisition TDTL using adaptive filters, K_1 =1 and ψ=п/2 (rad).
The noise performance of the fast acquisition TDTL using adaptive filters in comparison with the original TDTL is shown in Figure 4.. It is shown from the plots that the TDTL outperforms fast acquisition TDTL using adaptive filters, by a value of 0.2 in pdf scale. The impact of noise on the jitter performance of both fast acquisition TDTL using adaptive filters and TDTL loops was tested and the results are shown in Figure 4.. As can be seen from the figure, the average jitter for fast acquisition TDTL using adaptive filters is slightly higher by 0.025 at the best case.

Figure 4. TDTL using an adaptive filter and TDTL noise performance for SNR=10dB and frequency step 0.1 V.

Figure 4. TDTL using an adaptive filter and TDTL jitter performance for a range of SNR, frequency step 0.1 V.

Tanlock Loop Noise Reduction using an Optimized PD

This section proposes a modified TDTL system which uses a new PD design, which is optimized for noise reduction making it amenable for applications that require wide locking range without loss of noise immunity [76]. The proposed TDTL architecture, with the modified PD, uses a feedback mechanism that can reduce the amplitudes of the second- and higher-order harmonics by at least 50% even under high level of noise distortion [77]. It follows the same procedure used to improve the mixer-type PD by estimating the feedback variable for harmonics reduction. In addition, further enhancement to the noise performance of the proposed system can be achieved using two weighting factors which can be set to achieve a given factor for the noise enhancement loop as will be explained in the following

sections.

The simulation results indicate considerable improvement in the noise performance of the proposed system over the original TDTL architecture. The design architecture of the proposed structure, which composed of dual PD topology henceforth, called DPD-TDTL is shown in Figure 4.. In the figure it is shown that there are two PD with quadrature phase detection with different weighting factors a and b. The second complementary PD (lower) used to reduce the amplitudes of the second- and higher-order harmonics by at least 50% even under high level of noise distortion. The mathematical analysis of the DPD-TDTL follows the first-order TDTL previously discussed with different phase error as

etotalk=aek+be1k

(4.20)

where ek is defined in (3.12) e1k is a delayed version of ek by ψ (rad) and a and b are weighting factors, which show the contribution of each PD that are shown in Figure 4.. From (4.20) and following both (3.13) and (3.14) the DPD-TDTL system difference equation is given by

ϕk+1=ϕk-K1'[aek+be1k]+Λo (4.21)

ϕk+1=ϕk-K1'[etotalk]+Λo

(4.22)

where K1'=ωG1,and letting W=ωoω and K1=WK1'. It is clear from (4.22) that the error have two parameters one of which is from the upper loop and the other from the lower loop and both of them have weighing factors *a* and *b*.

(a)

(b)

Figure 4. (a) DPD-TDTL linear model (b) Block diagram of the proposed system using arctan PD.

The proposed algorithm has three conditions as follows:

- a>b higher noise performance as in (4.20) with slow acquisition as described in (3.19) to (3.21).
- a<b lower noise performance as in (4.20) with fast acquisition as described in (3.19) to (3.21).
- To prevent oscillation the weighing factor should be a+b<1 .
- The DPD-TDTL system performance in Figure 4. tested by subjecting it to a sudden change in input signal frequency higher than the DCO free running frequency and its performance is compared to that of the original TDTL. The proposed system was also tested for phase noise performance and jitters. Due to the fact that this architecture is used for noise immunity application, only positive frequency step was conducted.
- The simulation was carried out with two schemes with different weighting factors
- Scheme1: a=0.6 and b=0.4.
- Scheme2: a=0.4 and b=0.6.
- For the above schemes, it will be shown from the following tests that as the weighting factor of the lower loop (i.e. *b*) increases, Figure 4., the noise immunity will improve at the expense of the acquisition time and the reverse is true for Scheme1.
- Figure 4. and Figure 4. illustrates the output response of the proposed schemes and of original TDTL for a frequency step test. It is shown from the figure that both Scheme1 and the original TDTL have almost similar acquisition time. This test shows that by increasing the weighting factor *a*, better acquisition time is achieved.
- The phase plane plots of both the DPD-TDTL schemes and the TDTL when they are in lock state are depicted in Figure 4.. Again, analysis of the plots shows that both Scheme2 and the original TDTL have almost similar acquisition time in comparison to a slight improvement shown with Scheme1.
-
  - (a)
-
- (b)
-
- (c)
- Figure 4. First-order response for positive frequency step 0.3 V (a) TDTL phase error response(b) Scheme1 phase error response (c) Scheme2 phase error response, K_1 =1 and ψ=п/2 (rad).
-
- (a)
-
- (b)
-
- (c)
- Figure 4. First-order response for negative input frequency step of -0.3 V (a) TDTL phase error response (b) Scheme1 phase error

response (c) Scheme2 phase error response, K_1 =1 and ψ=π/2 (rad).

-
-
- (a)
-
- (b)
-
- (c)
- Figure 4. First-order phase planes of (a) TDTL (b) Scheme1 (c) Scheme2 with a positive frequency step of 0.3 V, K_1 =1 and ψ=π/2 (rad).
- The effect of AWGN on the performance of both schemes and TDTL were tested for SNR=10 dB. Results achieved in Figure 4. shows an improvement was achieved by both Scheme1 and Scheme2 with a value of 0.6 and 1 in pdf scale respectively. It can be seen from the plots that both schemes have better noise performance compared with original TDTL. This is due to the fact that the proposed loop allows for at least 50% of the higher order ripple reductions [77]. The figure also shows a further improvement achieved with increasing the weighing factor *b* which improved the mechanism effect of the additional second (lower) PD.
- The impact of noise on the jitter performance of both schemes and original TDTL loop were tested and the results are shown in Figure 4.. As shown in the figure, the average jitter of both schemes is lower than the one produced by TDTL which is 0.08 second for Scheme1 and 0.13 seconds for Scheme2. This proves that the proposed modified PD is used to enhance the reduction in phase noise. In addition, it also shown that the system provides better jitter performance as the SNR decreases. Moreover, the figure also shows that there is further improvement with increasing the weighing factor *b* as in Scheme1.

- Figure 4. Proposed loop schemes and TDTL noise performance for SNR=10dB, frequency step 0.1 V.
-
- Figure 4. Proposed loop schemes and TDTL jitter performance for a range of SNR, frequency step 0.1 V.

TDTL with Acquisition Aided Circuits

- One of the main drawbacks of the original TDTL system relates to its stability when its acquisition is thrown outside its locking range. The system becomes unstable and steps must be taken to re-establish its stability. In general when the DPLL system automatically recovers and acquires a locking, the process is referred to as self-acquisition. On the other hand, if the system

recovery is assisted by auxiliary circuits, the process is called aided acquisition. Although the TDTL is an excellent tracking device, its acquisition performance requires some improvement.

- Acquisition aided circuits are commonly used in many different applications such as satellite communications and optical internet broadband [50, 78, 79, 80]. In this section, both feed-forward (FF) and feedback (FB) aided circuits schemes are employed to enhance the original TDTL locking range, hence the acquisition process for satellite application [81, 82]. Both schemes improve the locking range of the conventional TDTL by employing auxiliary circuits. The ultimate objective of the FB and FF techniques is to control the damping ratio so as to prevent overshooting, which can lead to oscillations. However, the FF topology, which uses an adaptive threshold as opposed to a fixed threshold in the FB scheme, provides better control and improved response.
- As those auxiliary circuits are used to prevent overshoot the usual tests used above don't suit those architectures. Therefore, there are two main scenarios that acquire acquisition from the loop; the first one is when the change of the incoming frequency is within the locking range, whilst the other is when the change is outside the locking range. These scenarios are described in the following sections.

TDTL Acquisition within the Locking Range

- When the incoming frequency is within the locking range but is changing rapidly, that produces cyclic-slipping which affects the initial condition fed to the free running DCO. This may result in throwing the system outside its locking range. This might send the system into oscillation and it will take some time before the system regains its stable conditions Figure 4..
-
- Figure 4. Cycle slipping due to rapid change in the input frequency, K_1 =1 and ψ=π/2 (rad).
- To overcome this problem, an acquisition system is proposed as shown in Figure 4.. The controller block diagram shown in Figure 4. consists of a FSM, attenuators and a multiplexer. The FSM is used to detect the rapid changes in frequency, and to control the multiplexer that will pass the original or an attenuated signal coming from the loop filter. The attenuator merely increases the damping ratio, i.e. holds an initial value to the DCO input that prevents was overshooting which can result in throwing the loop outside the locking range leading to cycle slipping and then to oscillations. The cycle slipping and oscillation usually results from a delay on reaching the zero crossing point, which was speeded up using the acquisition-aided circuits.
-
- Figure 4. TDTL with feedback aided acquisition circuit block diagram.
-

Figure 4. Feedback aided acquisition circuit block diagram.

-
-
- Figure 4. Effect of FB acquisition aided circuit to rapid changes in the input frequency, K_1 =1 and ψ=π/2 (rad).
- The improved behaviour of the TDTL with FB aided acquisition is shown in Figure 4. with around 6 seconds faster than the original TDTL.

TDTL Acquisition outside the Locking Range

- The second scenario refers to the case when the incoming frequency jumps outside the locking range of the system. Depending on the value of the input signal, and hence the severity of the unlocked condition, the loop may only need some time to get into lock with the new frequency. The feedback aided circuit used in the first scenario can also be used for this scenario with some additional modifications. A feedforward arm is used in order to enhance acquisition speed as depicted in Figure 4..
-
- Figure 4. TDTL with feedforward aided acquisition circuit block diagram.
- The block diagram of the FE is shown previously in Figure 4. which consists of a derivative function, gain block, envelope detector and subtractor [83]. Both derivative and gain blocks produce a signal that has an amplitude equal to the amplitude of the signal frequency which is shaped by the envelope detector. This produces the same error that is produced by the loop filter of the original TDTL system.
- The main difference between the feed-forward and feedback aided circuits is that the former supports the system with an adaptive value i.e. it has a memory mechanism to provide the last error value when the system was in lock. The two systems and the original TDTL system were simulated with the second scenario and the results are shown in Figure 4.. It is evident from these results that the FF system has better performance, whilst the other two systems were unsuccessful for the second scenario.
-
- (a)
-
- (b)
-
- (c)
- Figure 4. The second scenario test for (a) TDTL (b) FB and (c) FB acquisition aided circuit, K_1 =1 and ψ=π/2 (rad).

Simulation Results

- Both proposed systems and the original TDTL were simulated with different tests; FSK with large difference between its levels was

used. These tests demonstrated the performance of both FB and FF compared to the original TDTL for faster acquisition and reliable locking which is very important the satellite communications [84, 85].

- The FSK used in this test is binary FSK which basically uses two frequency levels. These levels are selected to be at both edges of the locking range as illustrated in Figure 4.. This is to provide consecutive large sudden changes in the incoming frequency. The results shown in Figure 4. illustrate that both systems with aided circuit outperform the original TDTL and the best performance was achieved with the FF aided circuit as shown in Figure 4.d.
-
- (a)
-
- (b)
-
- (c)
-
- (d)
- Figure 4. (a) FSK modulation input and the response for (b) TDTL (c) FB and (d) FF acquisition aided circuit, K_1 =1 and ψ=π/2 (rad).
- The main strength of both FB and FF aided system will be shown clearly in improving the TDTL system for Doppler and Total Harmonic Distortion (THD) in Chapter 8.

Optimum First-order Loop Design

- There are different architectures presented in the previous sections, which have different development target to improve the performance of the TDTL such as linearity, acquisition time, locking range and noise performance. The performance parameters have conflicting relation which means increasing the locking range causes the noise performance to decrease as depicted in Figure 4.. Therefore, by improving one parameter the other parameter will be adversely affected. As a result, the optimum architecture is to moderate all performance parameters, which is achieved simply by linearizing the PD of the TDTL as discussed previously. Figure 4. show that linearizing PD architectures take moderate level of all performance parameters which means that those are the optimum architectures. On the other hand, improving one of the performance parameter will result in getting the optimum design for the needed architecture for specific application which means that the optimum design is application oriented.
-
  - Figure 4. Performance triangle.
- Table 4.1 proves the concept of the performance triangle. This table shows measurable performance parameters. The moderate

level of all performance parameter can be achieved in both TDTL-LPD and pre-distortion TDTL architectures which are following the linearization enhancing method. To get the best noise performance the designer is recommended to follow the Scheme2 of the modified PD architectures. To have the best acquisition the Fast acquisition TDTL using adaptive filter is the best choice. For a specific application such as FSK demodulation, the Feedback rounding concept can be selected.

• **Architecture**	• **Li**	• **Ac**	• **Locking Range**	• **Noise performance (pdf)**	• **Ji**
• TDTL	• n	• 6	• Large (baseline)	• 1	• 0
• TDTL-LPD	• li	• 3	• Smaller than TDTL	• 1.4	• 0
• Pred-	• li	• 3	• Smaller th	• 1.5	• 0

istortion TDTL			an TDTL		
• Feedback rounding concept	• n	• 1	• Similar to TDTL	• 1.2	• 0
• AEC-TDTL	• n	• 2	• Larger than TDTL	• 0.55	• 0
• Fasta	• n	• 1	• Larger than	• 0.85	• 0

cquisition TDTL using adaptive filter			TDTL		
• DPD-TDTL Scheme1	• n	• 3	• Similar to TDTL	• 1.6	• 0
• D	•	•	• Si	• 2	•

PD-TDTL Scheme2	n	5	similar to TDTL		0
• TDTL with FB aided circuit	• n	• 6	• Larger than TDTL	• 1	• 0
• TDTL with FF	• n	• 6	• Larger than TDTL with FB aide	• 1	• 0

aided circuit			d circuit		

- **Table 4: Measurable loop performance parameters for different First-order arctan based architectures.**

1.1 Conclusions

- This chapter presented the modified first-order system architectures that overcome or mitigate different original system limitations using different aided circuits.
- The nonlinearity associated with the first- order TDTLs was overcome by introducing the modified TDTL architecture TDTL-LPD and the Pre-distortion TDTL scheme. Those changes in both methods results in improvement of the system acquisition time in addition to linearity and consequently expanding locking range.
- For improving the acquisition speed of first-order TDTL different architecture were proposed which are fast feedback concept using rounding, adaptive TDTL structures based on comparison AC-TDTL and fast acquisition of TDTL using adaptive filters.
- Two architectures were proposed for noise performance which is DPD-TDTL Scheme 1 and Scheme 2.
- Finally a TDTL with both FB and FF aided circuits are proposed which are mainly used to bring the system back to locking state and stable mode i.e. widening the locking range.
- Each one of the proposed architectures has different improvement objective. Therefore, the choice of the appropriate architecture will depend on the overall system requirements. The incorporation of the additional blocks to improve the performance of the original TDTL impacts the overall system complexity. Depending on the specific application requirements this additional complexity may be acceptable in order to meet the necessary performance objectives. The decision on the appropriate architecture will obviously rest with the system designer.
-

SECOND-ORDER TDTL WITH ENHANCED ARCHITECTURES

Introduction

- This chapter describes the various techniques used to eliminate or/minimize the effects of the limitations of the original second-order TDTL in order to improve its performance parameters; acquisition, locking range, noise performance and linearity. The chapter also presents a technique for optimising these performance parameters to suit a given set of applications requirements.

TDTL with a Linearized Phase Detector (TDTL-LPD)

- As mentioned in Chapter 4, to reduce the nonlinearity of the original second-order TDTL system, an improved TDTL architecture with a linearized phase detector (TDTL-LPD) has been introduced in which the fixed time delay was replaced by a variable time delay unit [60]. The architecture of the TDTL-LPD is shown in Figure 5., which shows that the system resembles the original TDTL in all of its components except for the two new blocks; the phase linearization controller and the variable 'adaptive' time delay block. In addition, note that the second-order system in Figure 5., differs from that first-order system of Figure 4. only by the connection from the output of the DCO to the digital filter.
- In the TDTL-LPD system, the phase linearization controller assesses the value of the error resulting from changes in the frequency of the input signal, while the loop is in locked state. This is used to compensate for the nonlinear variations in the phase by adjusting the adaptive time delay block so that y(t) and x(t) maintain their quadrature relationship.
-
- Figure 5. Block diagram of the second-order TDTL-LPD.
- The basic concept of the second-order TDTL-LPD follows similar concept for the first-order that is discussed in Chapter 4

therefore, the locking range for the second-order TDTL-LPD, which is derived from TDTL in details in Chapter 3, can be written as

- $0<K1< 41+r\ W\ \sin\pi 2$
  (5.1)

- which is simplified to:
  - $0<K1< 41+r\ W$
    (5.2)

- Figure 5. Locking range of the second-order TDTL-LPD with r=1.2, $K_1 = G_1\ \omega_o$, $W=\omega_o/\omega$ and $\psi=\pi/2$ (rad).
- The locking range for second-order TDTL-LPD with a fixed phase shift of $\pi 2$ (rad) is shown in Figure 5.. To control the size of the locking range of the TDTL-LPD system, the variable delay block can be set to a value other than $\pi 2$. Therefore, using (5.1) and (5.2) different locking range sizes can be achieved as shown in Figure 5. simply by replacing the $\pi 2$ in (5.1) with other values. This is achieved by setting the variable delay unit to provide different phase shifts other than $\pi 2$ (rad).
-
- Figure 5. Locking range of the second-order TDTL-LPD with r=1.2, $K_1 = G_1\ \omega_o$ and $W=\omega_o/\omega$ for different phase values of $\pi/2$, $\pi/4$ and $\pi/8$ (rad).
-
- Similar testing procedure outlined above for testing previous TDTL architectures was employed to assess the acquisition, the locking range, and the noise performances of the second-order TDTL-LPD.
- Figure 5. and Figure 5. illustrate the response of TDTL-LPD and the original TDTL system to positive frequency steps of 0.3 V and negative frequency steps of -0.3 V respectively. The phase plane plots of both the second-order TDTL-LPD and the original TDTL within the locking range are illustrated in Figure 5.(a) and Figure 5.(b) respectively. From previous figures (i.e. Figure 5., Figure 5. and Figure 5.) the TDTL-LPD shows a mark improvement compared with the TDTL in the acquisition time. The TDTL-LPD required 9 cycles compared with 20 cycles for the original TDTL to reach the steady state while for a positive step, shown in Figure 5. while for negative step the TDTL-LPD required 9 cycles compared with 15 cycles for original TDTL as shown in Figure 5.. Consequently, in both cases, it can be seen that TDTL-LPD requires less number of sample times to achieve locking state.
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- (a)
-
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- (b)

- Figure 5. Second-order response for positive input frequency step of 0.3 V (a) TDTL phase error response and (b) TDTL-LPD phase error response r =1.2, K_1 =1 and ψ=π/2 (rad).
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- (a)
-
- (b)
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- Figure 5. Second-order response for negative input frequency step of -0.3 V (a) TDTL phase error response and (b) TDTL-LPD phase error response r =1.2, K_1 =1 and ψ=π/2 (rad).
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- (a)
-
- (b)
- Figure 5. Second-order phase planes of (a) TDTL and (b) TDTL-LPD with a positive frequency step of 0.3 V, r =1.2, K_1 =1 and ψ=π/2 (rad).
- To assess the locking range performance of the TDTL-LPD in comparison with the TDTL, both systems were subjected to frequency step inputs. An example of such tests is shown in Figure 5. with a positive frequency step of 0.6 V. It can be seen from Figure 5.a that the TDTL goes out of lock while the TDTL-LPD, as shown in Figure 5.b, achieves the locking state.
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- (a)
-
- (b)
- Figure 5. Second-order response for positive input frequency step of 0.6 V (a) TDTL-LPD phase error response and (b) TDTL phase error response r =1.2, K_1 =1 and ψ=π/2 (rad).
- The noise performance test demonstrates the effect of the AWGN on the performance of the TDTL-LPD which is measured using the pdf with a frequency step of 0.1 V. The effect of the AWGN, with an input signal of SNR=10 dB, on the performance of both TDTL-LPD and TDTL was tested with a simulation results achieved as shown in Figure 5.. It is shown from the plots that the TDTL-LPD outperforms TDTL, by a 0.15 in pdf scale. This improvement over the original TDTL is attributed to its nonlinearity, which compounds the effects of noise. The impact of noise on the jitter performance of both TDTL-LPD and TDTL loops was tested and the results are shown in Figure 5.. As can be seen from the figure, the average jitter for TDTL-LPD is lower by 0.1 seconds on the best case than that produced by TDTL.

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- Figure 5. TDTL-LPD and TDTL noise performance for SNR=10dB and frequency step 0.1 V.

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- Figure 5. TDTL-LPD and TDTL jitter performance for a range of SNR, frequency step 0.1 V.

o TDTL with Pre-distortion Technique

- The same techniques used in Chapter 4 to linearize the PD characteristics were used to linearize the second-order TDTL. It consists of a feedforward pre-distortion function, usually a look-up table (LUT), in the loop channel which consists of the delay as depicted in Figure 5.. This figure shows the block diagram of the proposed architecture using a LUT.

- Figure 5. Architecture of the modified TDTL using a feedforward pre-distortion technique.

Following the same procedure as in Chapter 4 the locking range for the second-order pre-distortion TDTL can be written as

- $0<K1<41+r\ W\ \sin\pi 2\pm\delta$

(5.3)

- Where δ is a tolerance factor which decreases as the number of points stored in the LUT increases.
- The locking range for second-order pre-distortion TDTL is shown in Figure 5. using (5.3).

- Figure 5. Locking range of the second-order pre-distortion TDTL with r=1.2, K_1 =1, ψ=π/2 (rad) and δ=0.01.
- A similar set of tests was conducted to evaluate the response of the second-order with pre-distortion TDTL in comparison with the original second-order TDTL. Both Figure 5. and Figure 5. illustrate the response of pre-distortion TDTL and TDTL system to positive frequency step of 0.3 V and negative frequency step of -0.3 V respectively.
- In Figure 5. the pre-distortion TDTL required 10 cycles compared with 20 for the original TDTL to reach the steady state while for a positive step while for a negative step, Figure 5., the original TDTL required 15 cycles compared to 10 cycles for the pre-distortion TDTL. The phase plane plots are also a different way to evaluate the acquisition responses which are also shows the same results, when they are in lock, are depicted in Figure 5..

- (a)
- (b)

- Figure 5. Second-order response for positive input frequency step of 0.3 V (a) TDTL phase error response and (b) pre-distortion TDTL phase error response, r =1.2, K_1 =1 and ψ=π/2 (rad).
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- (a)
-
- (b)
- Figure 5. Second-order response for negative input frequency step of -0.3 V (a)TDTL phase error response and (b) Pre-distortion TDTL phase error response, r =1.2, K_1 =1 and ψ=π/2 (rad).
-
- (a)
-
- (b)
- Figure 5. First-order phase planes of (a) TDTL and (b) pre-distortion TDTL with a positive frequency step of 0.3 V, K_1 =1 and ψ=π/2 (rad).
- The effect of the AWGN, with an input signal pdf of SNR=10 dB and with a frequency step of 0.1 V, on the performance of both pre-distortion TDTL and TDTL was tested with a simulation results achieved shown in Figure 5.. It is shown from these results that the pre-distortion TDTL outperforms the original TDTL, by a value of 0.1 in pdf scale, the impact of noise on the jitter performance of both pre-distortion TDTL and TDTL loops was tested and the results are shown in Figure 5.. As can be seen from the figure, the average jitter for pre-distortion TDTL is lower by 0.035 second on average than the one produced by TDTL.
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- Figure 5. Pre-distortion TDTL and TDTL noise performance for SNR=10dB and frequency step 0.1 V.

- Figure 5. Pre-distortion TDTL and TDTL jitter performance for a range of SNR, frequency step 0.1 V.

○ Loop Filter Sampling Improvement Architecture

- As previously mentioned the phase error in the second-order TDTL takes relatively long time to reach its steady state value of zero, as depicted in Figure 3., Figure 3., Figure 5., Figure 5. and Figure 5.b due to the fact that the second-order loop is controlled by the samples produced by the DCO. This is due to the fact the accumulation process of the proportional plus accumulation loop filter to reach the steady state is directly work with the DCO samples. Therefore, without the DCO samples the filter won't be able to approach the steady state. The acquisition time can be enhanced by increasing the sampling rate for the accumulation path in the digital loop filter to speed up the process to reach the

zero steady state as proposed in the TDTL with wide locking range and fast acquisition (TDTL-WFA) architecture [60].

- Fast acquisition is obtained by modifying the DCO block as shown in Figure 5..
-
- Figure 5. Block diagram of the TDTL-WFA.
- This is done by increasing the DCO free running frequency by a factor M and using its output to speed up the loop digital filter response. The free running frequency is then divided by the same factor M in order to maintain the sampling rate of the loop. The remaining structure is similar to the original TDTL.
- An extensive set of tests has been carried out to compare the second-order TDTL with the improved second-order TDTL-WFA using M=2; that is doubling the free running oscillator frequency. The performance of the TDTL-WFA was evaluated in a similar way as previously discussed; by subjecting it to sudden changes in the input signal frequency and comparing its response with the TDTL under the same conditions. The results clearly show that the TDTL-WFA performs better than the TDTL-LPD as demonstrated below.
- Figure 5. and Figure 5. illustrate the response of the TDTL-WFA and the TDTL, which has better performance compared with TDTL depicted in Figure 5.b, to a positive frequency step of 0.3 V and a negative frequency step of -0.3 V respectively within the locking range. In both cases, it shown that TDTL-WFA requires much less number of samples to achieve locking state as it convergences to zero steady state error. Figure 5. shows an improvement of the TDTL-WFA, which reaches to 5 cycles compared with 20 cycles for the original TDTL and 10 cycles for the TDTL-LPD. For the negative step the TDTL-WFA is taking 6 cycles to reach steady state compared with 15 cycles for the original TDTL and 9 cycles for the TDTL-LPD.
- The phase plane plots of both the TDTL and the TDTL-WFA, when they are in lock state, are depicted in Figure 5.a and Figure 5.b respectively. Again, analysis of the plots shows that the TDTL-WFA settles to the zero-steady state error faster than the original TDTL. Further improvement of the acquisition speed can be achieved by increasing the value of the factor M that is used in the construction of the DCO in Figure 5.. It can be seen that increasing M from 2 to 4, as shown in Figure 5., enables the TDTL-WFA error to converge relatively faster for a frequency modulation (FM) input signal. This test is intentionally used due to rapid change phenomena of the FM signal. In fact, under the same input conditions, as in Figure 5., the peak of the error for the TDTL-WFA with an M=2 is nearly double that of the same system with an M=4.
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- (a)
-
- (b)

- Figure 5. Second-order response for positive input frequency step of 0.3 V (a) TDTL phase error response and (b) TDTL-WFA phase error response, r =1.2, K1=1 and ψ=π/2 (rad).
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- (a)
-
- (b)
- Figure 5. Second-order response for negative input frequency step of -0.3 V (a) TDTL phase error response and (b) TDTL-WFA phase error response, r =1.2, K_1=1 and ψ=π/2 (rad).
-
- (a)
-
- (b)
- Figure 5. Second-order phase planes of (a) TDTL and (b) TDTL-WFA with a positive frequency step of 0.3 V, r =1.2, K_1 =1 and ψ=π/2 (rad).
-
- Figure 5. phase error response of the effect of the factor M changing from 2 to 4 on TDTL-WFA response in frequency modulation FM input signal, r =1.2, K_1 =1 and ψ=π/2 (rad).
- The effect of AWGN, with an input signal pdf of SNR=10 dB and with a frequency step of 0.1 V, on the performance of both TDTL-WFA and TDTL was tested and the simulation results achieved are shown in Figure 5.. These plots show that the TDTL-WFA outperforms TDTL, by a value of 0.3 in pdf scale, due to the nonlinearity overhead produced by the original TDTL that adversely affects its noise performance. The impact of noise on the jitter performance of both TDTL-WFA and original TDTL loops was tested and the results are shown in Figure 5.. As can be seen from the figure, the average jitter for TDTL-WFA is lower by 0.075 second on average than the one produced by TDTL. This indicates the suitability of this loop for both good phase noise performance and fast acquisition.
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- Figure 5. TDTL-WFA and TDTL noise performance for SNR=10 dB and frequency step 0.1 V.

- Figure 5. TDTL-WFA and TDTL jitter performance for a range of SNR, frequency step 0.1 V.

○ Second-order TDTL with Initialization Technique

- Due to the accumulation nature of the loop filter used by the second-order TDTL, it is necessary that the transient response of the filter is relatively slow in order to enable it to reach the steady state. This obviously compromises its performance,

particularly for applications that require fast response. One way of improving the transient response of a digital filter is by initializing its internal memory with a value other than zero [86, 87, 88, 89]. This method is a well-known method in image processing and digital filters field which requires fast initialization process of the loop filter memory to calculate the steady state value from the incoming input signal. Therefore, this section proposes an improved TDTL system in which a feedforward loop is used to initialize the loop filter memory so as to enhance the acquisition speed of the system [86, 87, 88, 89]. The feedforward loop is used to estimate the value of the steady state frequency of the input signal which is subsequently loaded into the memory of the loop filter.

- The block diagram of the proposed system with initialization is shown in Figure 5..
-
- Figure 5. Architecture of the second-order TDTL with loop initialization.
- The Frequency Estimator (FE) block is used to generate an estimated value of the steady state frequency of the incoming input signal and then use this value to initialize the loop filter memory using a feedforward loop. The block diagram of the FE is shown previously in Figure 4.. It consists of a derivative function, gain block and envelope detector. The derivative block generates the frequency value of the input signal. For example, if the input signal is sinωt then the output signal of the derivative block is ωcosωt which is altered using the gain block to produce the frequency value Fi*cosωt, Figure 4.. The envelope detector then removes the high frequency component leaving the DC part Fi which is the steady state value used to initialize the loop filter memory instead of a zero value.
    - Initialization and loading the internal filter memories with steady state value other than zero is used to improve the transient performance of digital filters as stated earlier as reported in the literature [88, 87, 86]. Therefore, the improvement of the loop filter response improves the acquisition performance of the loop.
    - Using the initialization process in the digital loop filter will speed up the whole TDTL transient response by easing the calculation of the error in (3.35) as in (5.4). This is due to the fact that the steady state response of the loop filter is initialized using the feedforward mechanism, which helps the PD to calculate the steady state error faster compared with the original TDTL.
    - ess=-K1'(r+1)2
      (5.4)
    - The same performance test was conducted by applying rapid changes in the input signal frequency assess the effect of initialization on the performance of the original TDTL. The change is represented as positive and negative steps as previously done and its response compared with the original TDTL under the same conditions. As will be shown below, the response of the TDTL with initialization shows a considerable improvement compared to the original TDTL.

- For the second-order loops, Figure 5. and Figure 5., illustrate the response of the TDTL with initialization and without initialization to a positive of 0.3 V and negative of -0.3 V frequency steps respectively. In both cases, it can be seen that TDTL with initialization requires less number of samples to achieve locking state. It requires 3 cycles for the both positive and negative steps compared with 20 and 15 cycles respectively for the original second-order TDTL to approach the steady state. The phase plane plots of both loops, when they are in lock, are depicted in Figure 5..
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- (a)
-
- (b)
- Figure 5. Second-order response for positive input frequency step of 0.3 V (a) TDTL phase error response and (b) TDTL with initialization phase error response, r=1.2, K_1=1 and ψ=π/2 (rad).
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- (a)
-
- (b)
- Figure 5. Second-order response for negative input frequency step of -0.3 V (a) TDTL phase error response and (b) TDTL with initialization phase error response, r=1.2, K_1 =1 and ψ=π/2 (rad).
-
- (a)
-
- (b)
- Figure 5. Second-order phase planes of (a) TDTL and (b) TDTL with initialization phase error response with a positive frequency step of 0.3 V, r =1.2, K_1 =1 and ψ=π/2 (rad).
- The system was evaluated by subjecting it to an FSK signal with a frequency step shown in Figure 5.a, in comparison with the original TDTL. This test provides evidence that the TDTL with initialization system has better acquisition in compared with failure in original TDTL response as it is clearly shown in Figure 5.b and Figure 5.c.
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- (a)
-
- (b)
-
- (c)
- Figure 5. (a) FSK input signal (b) FSK demodulation using conventional TDTL (c) FSK demodulation using TDTL with initialization, r =1.2, K_1 =1 and ψ=π/2 (rad).
-
- The effect of AWGN, with an input signal pdf of SNR=10 dB and with a frequency step of 0.1 V, on the performance of both TDTL

with initialization and original TDTL was tested and the simulation results are shown in Figure 5.. It is shown from the plots that the original TDTL outperforms TDTL with initialization, by a value of 0.2 in pdf scale. The impact of noise on the jitter performance of both TDTL with initialization and original TDTL loops was tested and the results are shown in Figure 5.. As can be seen from this figure, the average jitter for TDTL with initialization is, on average, lower by 0.025 second than the one produced by TDTL. This proves that the loop is suited for fast acquisition.

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- Figure 5. TDTL with initialization and TDTL noise performance for SNR=10dB and frequency step 0.1 V.

- Figure 5. TDTL with initialization and TDTL jitter performance for a range of SNR, frequency step 0.1 V.

○ Frequency and Phase-locked Separation Architecture

- The section proposes a solution to overcome the limitation of a nonzero steady state phase error of the first-order TDTL. Although it is modified first-order architecture, it will be compared with the original second-order due to its capability to achieve near zero phase error in the steady state. It exhibits the architecture and performance of an adaptive TDTL with zero phase error (ATDTL-ZPE) [90]. The proposed architecture eliminates the nonzero phase error limitation of the original TDTL and extends its locking range.
- The block diagram of ATDTL-ZPE is shown in Figure 5.. The main difference between the original TDTL and the ATDTL-ZPE is the introduction of the frequency estimator (FE) and adder blocks. These blocks are used to initialize the loop DCO so as to produce a frequency that matches the incoming input signal frequency. Therefore, the DCO will sample the incoming input signal at a rate that is equal to its frequency but with a different phase. This phase difference between the incoming signal and the DCO produces an error at the arctan PD output.
- The introductions of the FE block frees the loop from frequency tracking and make it available for the prime purpose of phase tracking only. This process results in reducing the steady state phase error of the first-order loop to zero. It also leads to a wider locking range through a transparent translation or shift process of the TDTL locking range characteristics to the desired frequency range of the system depending on the DCO operating range.
- The block diagram of the FE is shown previously in Figure 4.. By initializing the DCO using the value produced by the FE block, as shown in Figure 4., the incoming input signal will be sampled at a rate that matches its frequency but with a difference in the zero crossing between the two, i.e. that is different in phase. Consequently, the error produced by the arctan phase detector is

only related to the phase difference between the DCO and the incoming input signal, which will be reduced by the loop.

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- Figure 5. Architecture of the ATDTL-ZPE.
- The locking range of the proposed system is similar to that of the first-order TDTL system as in [50] as shown in Figure 3.. The new system has the ability to quickly move the locking range to the specific frequency and hence the ATDTL-ZPE will always operate at W=1 while keeping K_1 at the initial design value of 1. However, K_1 should be kept within the limit $0 < K_1 < 2$ for the loop to stay in lock and to prevent the system from oscillation.
- By initializing the DCO, it samples the incoming input signal at a rate that matches its frequency but with a difference in the zero crossing between the two; that is different in phase. Consequently, the error produced by the PD is only related to the phase difference between the DCO and the incoming input signal, which will be reduced by the loop. As the loop is working at W=1 all the time consequently the loop is used only to reduce the phase error of the ATDTL-ZPE system. Therefore, (3.30) can be given as in (5.5) which add a constraint on the loop gain as shown in Figure 5.. This constraint is simply putting a restriction on the usable operating loop gain without oscillation.
- $0<K1<2\sin 2\alpha+\sin 2\alpha+\psi\sin 2\psi$ (5.5)

- Figure 5. Locking range of ATDTL-ZPE with $K_1=G_1\ \omega_o$ and $W=\omega_o/\omega$.
- The ATDTL-ZPE performance was evaluated in a similar way to the systems proposed earlier. Figure 5. illustrates the response of the ATDTL-ZPE and the original second-order TDTL to a positive input frequency step of 0.3 V. The Figure shows the phase error of both the ATDTL-ZPE and the original second-order TDTL. From these responses, it is clear that the ATDTL-ZPE achieves a zero steady state phase error with one cycle compared with 15 cycles for the original second-order TDTL. An example of the ATDTL-ZPE response to negative frequency step of -0.3 V is shown in Figure 5., which shows that it achieved the steady state in 5 cycles compared to 15 cycles for the original TDTL. The phase plane plots of both ATDTL-ZPE and the original first-order TDTL for positive frequency step are shown in Figure 5.. The test results of ATDTL-ZPE show faster acquisition time as compared with the original TDTL with a zero phase error, which is clearly shown in Figure 5. and Figure 5..
- As the TDTL is assisted by the FE block, the loop only kept for phase-locked process instead of doing both frequency and phase locking at the same time which will enhance the noise immunity performance as will be shown in the following tests.
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- (a)

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- (b)
- Figure 5. Phase response for positive input frequency step of 0.3 V (a) Second-order TDTL phase error response and (b) ATDTL-ZPE phase error response, K_1 =1 and ψ=π/2 (rad).
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- (a)
-
- (b)
- Figure 5. Phase response for negative input frequency step of -0.3 V (a) Second-order TDTL phase error response and (b) ATDTL-ZPE phase error response, K_1 =1 and ψ=π/2 (rad).
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- (a)
-
- (b)
- Figure 5. Phase planes of (a) Second-order TDTL and (b) ATDTL-ZPE phase error response with a positive frequency step of 0.3 V, K_1 =1 and ψ=π/2 (rad).
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- This test presents the effect of AWGN on the performance of the proposed loop architecture and the performances are measured using pdf and jitter. The effect of AWGN, with an input signal of SNR=10 dB, on the performance of both ATDTL-ZPE and TDTL was tested with a simulation results achieved as shown in Figure 5. and Figure 5.. It is shown from the plots that the ATDTL-ZPE outperforms TDTL by a value of 0.8 in pdf scale, due to the fact that the ATDTL-ZPE system is used only for phase synchronization with a help of the FE auxiliary circuit that provides the frequency value. The ATDTL-ZPE system is using FE to provide the frequency value to the loop that works only to synchronize the phase. The impact of noise on the jitter performance of both ATDTL-ZPE and TDTL loops was tested and the results are shown in Figure 5.. As can be seen from the figure, the average jitter for ATDTL-ZPE is much lower than the one produced by TDTL which reach to 0.2 second at most. In addition, it also indicates that the system provides better jitter performance as the SNR decreases. In the figure, it is shown that below 2 dB the ATDTL-ZPE performance starts to degrade. This is due to fact that the auxiliary circuit, i.e. the FE, starts failing , due to increase in the noise affect, to provide the correct required frequency value to the TDTL loop and consequently, this situation results in the worst noise performance at around 0.5 dB. Therefore, this topology depends on how good the FE is implemented which puts constraints on implementation against the requirements.
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- Figure 5. ATDTL-ZPE and TDTL noise performance for SNR=10dB and frequency step 0.1 V.

- Figure 5. ATDTL-ZPE and TDTL jitter performance for a range of SNR, frequency step 0.1 V.

1.1 Dual TDTL Loop with Improved Performance

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- The section presents a dual loop TDTL (D-TDTL) architecture that provides improved phase noise (jitter) performance [91]. The new architecture has dual stacked loops, referred to as the top and bottom loops, and connected in cascode topology to improve the overall system performance. The section highlights the design architecture of the proposed structure which is shown in Figure 5.. The top loop acts as a frequency lock loop (FLL) for the bottom PLL which is used only for overall system phase error enhancement. The FLL uses a second-order TDTL in order to prevent a non-zero phase shift that can be conveyed to the PLL circuit. As shown in Figure 5., the DCO1 output of the top loop is used as an input for the second loop to initialize its DCO2. The analysis of the D-TDTL follows a procedure similar to that given in [11, 50]. The top loop follows the second-order analysis while the bottom loop follows the first-order analysis which already explained in details in Chapter 3.
- As shown in Figure 5., the bottom loop uses the output of the top loop filter to initialize its DCO2 [50]. By initializing the DCO2, it samples the incoming input signal at a rate that appropriate to its frequency but with a difference in the zero crossing between the two; that is different in phase. Consequently, the error produced by the PD is only related to the phase difference between the DCO2 and the incoming input signal, which will be reduced by the loop. This means that the loop is working at W=1 at all times. As a result, the bottom loop is used only to enhance the phase error of the D-TDTL system. Consequently the bottom loop only adds constraints on the loop gain as in (5.5). The locking range of the D-TDTL is shown in Figure 5., which consists of FLL locking range that follow the second-order TDTL and PLL that follows the loop gain restriction as in (5.5).
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- Figure 5. Block diagram of the D-TDTL.
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- Figure 5. Locking range of D-TDTL with $K_1 = G_1\ \omega_o$ and $W = \omega_o / \omega$.
- A similar set of tests was conducted to evaluate the response of the D-TDTL in comparison with the original second-order TDTL. Both Figure 5. and Figure 5. illustrate the response of TDTL-LPD and TDTL system to positive frequency step of 0.3 V and negative frequency step of -0.3 V respectively.
- In Figure 5., both the D-TDTL and the original TDTL required about 20 cycles to reach the steady state for a positive step in while, as shown in Figure 5. for a negative frequency step input

the original TDTL required 15 cycles compared with 18 cycles for the D-TDTL. Consequently, in both cases, the original TDTL requires less number of samples to achieve locking state. The phase plane plots of both loops that proves the same, when they are in lock, are depicted in Figure 5..

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- (a)
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- (b)
- Figure 5. Second-order response for positive input frequency step of 0.3 V (a) TDTL phase error response and (b) D-TDTL phase error response, r =1.2, K_1 =1 and ψ=π/2 (rad).
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- (a)
-
- (b)
- Figure 5. Second-order response for negative input frequency step of -0.3 V (a)TDTL phase error response and (b) D-TDTL phase error response, r =1.2, K_1 =1 and ψ=π/2 (rad).
-
- (a)
-
- (b)
- Figure 5. First-order phase planes of (a) TDTL and (b) D-TDTL with a positive frequency step of 0.3 V, K_1 =1 and ψ=π/2 (rad).
- To assess the noise performance of the proposed system, the effect of AWGN, with an input signal of SNR=10 dB, on the performance of both D-TDTL and TDTL was tested with the simulation results shown in Figure 5.. Clearly, the D-TDTL system has better noise performance than the original TDTL by 2.45 in pdf scale. This is due to the fact that the bottom loop of the stacked dual loop is used for only phase error reduction. The impact of noise on the jitter performance of both D-TDTL and TDTL loops was tested and the results are shown in Figure 5.. The figure indicates that the average jitter for D-TDTL is lower than the one produced by TDTL by 0.125 seconds at most. This proves that the bottom loop is primarily used to reduce the phase noise. In addition, it also indicates that the system provides better jitter performance as the SNR decreases with a considerable improvement compared with the original TDTL system.

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- Figure 5. D-TDTL and TDTL noise performance for SNR=10dB and frequency step 0.1 V.
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- Figure 5. D-TDTL and TDTL jitter performance for a range of SNR, frequency step 0.1 V.

○ TDTL Loop with Adaptive Loop Filter Coefficients

- In a highly dynamic environment such as in wireless communication systems, the performance of conventional PLLs becomes restricted. This led researchers to focus on adapting the PLLs using auxiliary circuits to cope with dynamic environments in order to improve the levels of synchronization that can be achieved [7, 44, 92, 93].
- In addition, modern communication systems require PLLs with fast acquisition speeds, which consequently require wide loop bandwidth. However, wide bandwidth reduces the noise immunity of the system and increases the jitter effects. This increases the effects of the dynamic environment on the system and adversely affects its synchronization ability.
- These two conflicting requirements of wide bandwidth and good noise immunity can be resolved by using a PLL with an adaptive loop bandwidth. This can be achieved by modifying the loop filter coefficients using an auxiliary circuit such as an adaptive filter to improve the noise and jitter performance and thus synchronization as discussed in [2, 94, 95, 96, 97].
- In this section, the technique of adaptive loop bandwidth using an adaptive filter is applied to the second-order TDTL; henceforth it is called AS-TDTL [98]. The proposed architecture is simply a second-order TDTL with real-time adaptive calculation of the loop filter coefficients. An adaptive digital filter based on the recursive least squares (RLS) algorithm is used to generate the coefficients of the TDTL loop filter. This allows the filter coefficients to be continuously updated in real-time so as to optimise the noise immunity of the TDTL in a highly dynamic environment. This method has a very slight improvement in acquisition with a clearer improvement in the noise immunity. The effect of the dynamic environment especially Doppler effect will be explained in the Chapter 8; the applications chapter.
- The proposed architecture mathematical analysis follows the original second-order TDTL as explained earlier with addition of the adaptive filter mathematical analysis.
- The input to the adaptive filter is the timing offset between the zero crossing of the incoming signal and the signal that is locally generated oscillator. Let 1To and 1T1 denote the clock rates of the received and the transmitted signals, respectively. At the k^{th} zero crossing point, the time offset αk can be express as
- αk=t0+kT1-T0
  (5.6)
- where t0 is the initial timing offset.
- The variable gain sequences G1(k) and G2(k) can be obtained from the adaptive filter based on the following state space model [99].
- xk+1=Axk+wk
  (5.7)

- yk+1=αk'=Cxk+nk
  (5.8)
- Where wk is the filter coefficients matrix and αk' is the corrupted time offset with a mean white noise nk has zero and the initial timing offsets and the current state estimate given by xk=[αk βk]T; βk=T1-T0; A=1101 and C=10.
- Note that αk and βk represent the zero crossing time (carrier phase) and the period offset (carrier phase offset) estimated state variable as shown in Figure 5..
-
- Figure 5. Plot of the transmitted carrier states.
- The estimation of the states can be solved statistically due to the fact the signal is corrupted by a white noise. The adaptive filter based on the RLS with the following cost function is used [99].
- Jx= k=0N-1λN-1-k(yk-Cxk)
  (5.9)

- where N is the order of the adaptive filter and will be one for the second-order TDTL and λ is the forgetting factor. The optimal gains G1(k) and G2(k) minimizing the trace of the prediction error covariance matrix P(k+1|k) are given by the Gk=G1(k)G2(k), which is obtained by solving the recurrence relations in (5.10) and (5.11).

- Gk= P(k|k-1)1+CP(k|k-1)CT
  (5.10)
- Pk+1k= AI-GkCPkk-1ATλ
  (5.11)
- In the proposed system, the second-order TDTL is modified as shown in Figure 5. by the inclusion of the RLS adaptive filter, which is used to modify the coefficients of the first-order TDTL loop filter.
-
- Figure 5. Architecture of the adaptive second-order TDTL.
- The simulation was conducted using a sampling frequency of 100 Hz and the carrier frequency 1 Hz. The initial statistics P0|-1 required for the adaptive filtering isT021200T02300. The forgetting factor λ was set to 0.9 throughout the simulation. The value 0.9 was selected to prevent oscillation and improve the speed of achieving the required signal.
- Testing this architecture follows similar testing tools starting from acquisition performance test to show the affect response of AS-TDTL in comparison with the original TDTL. Both Figure 5. and Figure 5. illustrate the response of AS-TDTL and TDTL system to positive frequency steps of 0.3 V and negative frequency steps of -0.3 V respectively. The AS-TDTL required 14 cycles compared with 20 cycles for the original TDTL to reach the steady state for a positive step shown in Figure 5., and for negative step the AS-TDTL required 10 cycles compared with 15 cycles for original TDTL as shown in Figure 5. . Consequently, in both cases, it can be seen that AS-TDTL requires less number of samples to achieve

locking state. The phase plane plots of both the second-order AS-TDTL and TDTL within the locking range are illustrated in Figure 5.a and Figure 5.b respectively.

- (a)
- (b)
- Figure 5. Second-order response for positive input frequency step of 0.4 V (a) TDTL phase error response and (b) AS-TDTL phase error response r =1.2, K_1 =1 and ψ=π/2 (rad).
- (a)
- (b)
- Figure 5. Second-order response for negative input frequency step of -0.3 V (a) TDTL phase error response and (b) AS-TDTL phase error response r =1.2, K_1 =1 and ψ=π/2 (rad).
- (a)
- (b)
- Figure 5. Second-order phase planes of (a) TDTL and (b) AS-TDTL with a positive frequency step of 0.4 V, r =1.2, K_1 =1 and ψ=π/2 (rad).
- The effect of AWGN, with an input signal of SNR=10 dB, on the performance of both AS-TDTL and TDTL was tested and the simulation results are shown in Figure 5.. It is shown from the plots that the AS-TDTL system has better noise performance, by 0.9 in pdf scale, when compared with TDTL. This is due to the fact that the loop filter coefficients are calculated in a real time to compensate for the corrupted signal using the RLS algorithm. The impact of noise on the jitter performance of both AS-TDTL and TDTL loops was tested and the results are shown in Figure 5.. As can be seen from the figure, the average jitter for AS-TDTL is lower, by at most 0.1 second, than the one produced by TDTL. This architecture is best suited for the high dynamic environment such as Doppler affect as discussed in detail in Applications Chapter 8.

- Figure 5. AS-TDTL and TDTL noise performance for SNR=10dB and frequency step 0.1 V.
- Figure 5. AS-TDTL and TDTL jitter performance for a range of SNR, frequency step 0.1 V.

○ Optimum Second-order Loop Design

- Different TDTL based architectures have been discussed which use different approaches to enhance the performance of the original TDTL system. Since the performance parameters are conflicting for example, increasing the locking range causes the noise performance to degrade as depicted previously in Figure 4.. The optimum architecture is to moderate all parameters, which may be achieved by linearizing the PD of the TDTL as discussed previously in both TDTL-LPD and TDTL with pre-distortion. Therefore, this chapter is confirms the concept of linearizing the PD as discussed in Chapter 4 as shown in both TDTL-LPD and TDTL with pre-distortion. This figure shows that linearizing PD architectures moderates all performance parameters which means that those are the optimum architectures. Conversely, improving one of the performance parameter will result in getting the optimum design for the required architecture for specific application, which means that the optimum design is application driven.
- Table 5.1 proves the concept of the performance triangle shown in Chapter 4 in Figure 4.. This table shows measurable performance parameters. The moderate level of all performance parameter can be achieved in TDTL-LPD; Pre-distortion TDTL and TDTL-WFA architectures which are involve the linearization method. To get the best noise performance, the designer is recommended to follow the ATDTL-ZPE. To have the best acquisition the TDTL with initialization and D-TDTL are the best choice. For a specific application such as high dynamic system immunity, the AS-TDTL can be selected.
-

• Architecture	• Li	• Ac	• Locking Range	• Noise performance (pd	• Ji

				f)	
• TDTL	• n	• 20	• Small (baseline)	• 0.8	• 0
• TDTL-LPD	• Li	• 9	• Smaller than TDTL	• 0.95	• 0
• Pre-distortion TDTL	• Li	• 10	• Smaller than TDTL	• 0.9	• 0
• TDTL-WFA	• Li	• 6	• Similar to TDTL	• 1.1	• 0
• TDTL with	• n	• 3	• Similar to TDTL	• 0.6	• 0

initialization					
• ATDTL-ZPE	• n	• 5	• Larger than TDTL	• 1.6	• 0
• D-TDTL	• n	• 20	• Similar to TDTL	• 3.25	• 0
• AS-TDTL	• n	• 14	• Similar to TDTL	• 1.7	• 0

- **Table 5: Measurable loop performance parameters for different second-order arctan based architectures.**

1.1 Conclusion

- This chapter presented modified second-order system architectures that overcome or mitigate different limitations of the original TDTL using different auxiliary aided circuits.
- The nonlinearity associated with the second-order TDTLs was overcome by introducing the modified TDTL architectures; the TDTL-LPD, the TDTL with pre-distortion, and the TDTL-WFA. These

modified architectures result in improvement of the system acquisition time in addition to linearity and consequently expanding locking range especially for second-order loop. In addition, a wide locking range was achieved by introducing the adaptive TDTL with zero phase error (ATDTL-ZPE) due to the system ability to quickly shift the locking range to the specific frequency and hence maintain the loop operating at W=1.

- The limitation in the acquisition speed of second-order TDTL was alleviated by introducing the TDTL with wide locking range and fast acquisition (TDTL-WFA) topology.
- Finally, different architectures were proposed for noise immunity, namely the ATDTL-ZPE, D-TDTL and AS-TDTL systems.

- Each one of the proposed architectures has different improvement purpose. Therefore, the choice of the appropriate architecture will depend on the overall system requirements. The incorporation of the additional blocks to improve the performance of the original TDTL impacts the overall system complexity. Depending on the specific application requirements this additional complexity may be acceptable in order to meet the necessary performance objectives. The decision on the appropriate architecture will obviously rest with the system designer.

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• NO-DELAY DIGITAL TANLOCK LOOP

○ Introduction

- This chapter describes a new digital tanlock loop, which does not use any time delay block and eliminates the need for the auxiliary circuits discussed in chapter 4 and 5. The new novel no-delay architecture proposes a more efficient TDTL scheme that overcomes the nonlinearity problem, caused by the delay block of the original TDTL, by sampling the incoming signals using two samplers with a 90° phase shift between them. This process maintains a quadrature relationship between the two channels of the modified TDTL system. The mathematical analysis and testing results are presented in this chapter.
- The process of simplifying the tanlock loop design and implementation resulted in replacing the Hilbert Transform (HT) block with the fixed time delay unit. This led to degradation in the linearity of the locking range characteristic of the tanlock loop as discussed earlier [11, 52]. A number of possible solutions have been proposed in the literature to overcome this problem including the use of a variable time delay block as in [60, 66, 90] and by using a pre-distortion method as described in chapters 4 and 5. All previously discussed methods have various implementation difficulties which limit the performance of the method to achieve very linear PD characteristics. The new method in this chapter proposes a more efficient TDTL architecture that overcomes the nonlinearity problem through the elimination of the 90° phase shift block [100]. This new no-delay DTL (NDTL) architecture modifies the design of the DCO circuitry so that two sampling signals with 90° phase shift are generated in order to maintain the quadrature relationship between the two channels of the system.
- The architecture of the proposed NDTL system is shown in Figure 6.. The DCO centre frequency is set at twice the overall loop DCO (L-DCO) free-running frequency (f_0). The DCO signal is then used to drive the two counters whose outputs are used to sample the input signal xt. Since there is a phase shift of 90° between the outputs of the counters, the quadrature relationship between the two sampling signals is preserved without the need for a phase-shifter in one of the channel's arms.
-
- Figure 6. block diagram of NDTL.

o Mathematical Model and Analysis

- The NDTL system receives a continuous sinusoidal input signal xt with a frequency offset Δω=(ω-ωo), which is also translated as a phase shift, from the free running frequency ωo of DCO as follows
- xt=Asinωot+θt
  (6.1)
- where A is the amplitude of the input signal, ωo(rads) is the free running frequency of the DCO, and θt is the information bearing phase in radians. Following a similar analysis to that in [11, 36, 50] and to Chapter 3 with a difference of having two sampling intervals of the DCO between the sampling instants t(k+1) and t(k) which are given by
- T1k=To-ck-1
  (6.2) T2k=To-ck-1+π2ωo
  (6.3)
- where To=2πωo is the free-running period of the DCO, and ck-1 is the output of the digital filter at the previous sampling instant.
- The total times up to the k^{th} sampling instant for both sampling intervals can be defined as
- t1k=i=1kTi=kTo-i=0k-1ci
  (6.4)
- and

- t2k=i=1kTi=kTo-i=0k-1c(i)+π2ωo
  (6.5)
- The discretized signals generated by the samplers are
- x(k)=Asinωot1+θk
  (6.6)
- and
- yk=Asinωot2+θk
  6.7
- Substituting (6.4) and (6.5) in (6.6) and (6.7) respectively yields
- xk=Asinθk-ωoi=0k-1ci
  (6.8)
- yk=Asinθk-ωoi=0k-1ciπωo2ω=Acosθk-ωoi=0k-1ci
  (6.9)
- The phase error between the input signal and the DCO is given by
- ϕk=θk-ωoi=0k-1ci
  (6.10)
- Therefore, both (6.8) and (6.9) can be redefined as
- xk=Asinϕk
  (6.11) y(k)=Acos[ϕk]
  (6.12)
- When the signals x(k) and y(k) are applied to the PD, the generated error signal e(k) between the two arms of the loop is
- ek=ftan-1sinϕkcosϕk=ftan-1tan(ϕk=fϕk (6.13)

- where fγ=-π+γ+π mod 2π and ϕk is the phase error. Consequently, the degradation in the linearity of the TDTL system caused by the time delay unit is eliminated [11, 36, 52].
- Since ck=Dzek=K1'f[ϕ(k)], where Dz is the loop filter transfer function and K1' is the loop gain, two system difference equations can be derived from (6.4), (6.5) and (6.14) as follows
- ϕ1k+1=ϕk-ωDzek+Λo
  (6.14)
- ϕ2k+1=ϕk-ωDzek+Λo+Λo4
  (6.15)
- From (6.14) and (6.15) it can be shown that
- ϕ2k+1=ϕ1k+1+Λo4
- =ϕ1k+1+π2ω-ωoωo
  (6.16)
- ϕ2k+1=ϕ1k+1+π21-WW
  (6.17)

- where W=ωoω and Λo=2π(ω-ωoωo).
  - From (6.17), it is evident that apart from a phase shift of π2 (rad), (6.14) and (6.15) are similar. Therefore, the sampling signal given by (6.2) is used to follow the zero crossing of the incoming input signal, whilst the shifted sampling signal defined by (6.3) samples the input signal with a phase shift of 90°. This maintains the quadrature relationship between the two channels without the need for a phase shifter to achieve locking. Therefore the final difference equation is
  - ϕk+1=ϕk-ωck+Λo
    (6.18)
- For the first-order loop
  - ck=Dzek=K1'fϕk
    (6.19)
  - Using (6.1), (6.2) and (6.3) and following a similar analysis to that in [11, 36, 48, 49, 50, 101] which is also explained in details in Chapter 3, the difference equation and the locking range, depicted in Figure 6., for the NDTL first-order system, are given by (6.20) and (6.21) respectively. The locking range of the first-order TDTL is also included in Figure 6., for comparison purpose.
  - ϕk+1=ϕk-K1'fϕk +Λo
    (6.20) 21-W<K1<2W
    (6.21)
- where fγ=-π+γ+π mod 2π , ϕk is the phase error at the instant k, Λo=2πω-ωo/ωo , K1'=ωG1, G1 is loop filter coefficient, W=ωo/ω , and K1=WK1'.

•

- Figure 6. Locking range of first-order NDTL and TDTL, $K_1 = G_1$ ω_o and $W = \omega_o / \omega$.
- The convergence speed and after following the fixed-point analysis developed in [57, 58] , the steady state phase error is
- ϕss=η β1sinη≥0 fη+π, otherwise.
  (6.22)

- where fγ=-π+γ+π mod 2π, β1=tanη and η=Λo K1'. The characteristic function of the PD and its first derivative are continuously differentiable in the principal interval –π,π, hence fixed-point analysis is applicable to the NDTL. Following fixed-point analysis developed in [57, 58, 59] for the sinusoidal DPLL, the Lipschitz constant is given by
- L=maxgϕ-gϕss ϕ-ϕss
  (6.23)
- where gϕ can be expressed as
- gϕ=ϕ-K1'fϕ+Λo
  (6.24)
- The asymptotic estimate (upper bound) to the number of steps required for convergence of the phase error ϕk within a radius ϵ of the fixed-point ϕss is given by
- m=int lnϵϕ-ϕsslnL+1
  (6.25)
- where int . is the integer function.
- It can be shown that the time required to reach the fixed-point steady state ϕss is given by
- Tc=mToW+ϕm-θoω≈mToW
  (6.26)
- since ϕm-θoω≪mT0W
- As a result, (6.26) shows the effect of frequency on the acquisition time which means that the acquisition time is differ with a variation in the incoming frequency.
- Using (6.1) , (6.2) and (6.3) for the second-order loop analysis, which uses a first-order accumulation digital filter with transfer shown in (3.34), the loop difference equation are given by (6.27) which the locking range is in (6.28) which is depicted in Figure 6.. The derivation of the both difference equation and the locking range are explained in details in Chapter 3.
- ϕk+2=2ϕk+1-rK1'ek+1+K1'ek-ϕk
  (6.27)
- 0<K1<4W1+rand r>1
  (6.28)
- where r=1+G1G2, and G1and G2 are the filter coefficients.
-
- Figure 6. Locking range of both second-order NDTL and TDTL, r =1.2, $K_1 = G_1 \omega_o$ and $W=\omega_o / \omega$.
- The convergence of the second-order loop is directly controlled by the samples produced by the DCO, which is used to control the loop filter. Due to fact that the NDTL DCO centre frequency is set at twice compared with the conventional TDTL loop, consequently the overall convergence of the second-order loop is improved by a factor of two.

○ NDTL Loop Noise Analysis

- Assuming that the input signal is corrupted by an AWGN with a zero mean and two- sided power spectrum density of Gnwf=no/2,

the autocorrelation can be given by the inverse Fourier Transform of Gnwf as Rτ=noδ(τ)/2 [2, 63], where δτ represents the Dirac Delta function. As a result, Rτ=0 for τ≠0 so any two different samples of this kind of noise are uncorrelated and for this reason they are statistically independent [59, 102].

- Since the NDTL has a discrete nature, the Chapman-Kolmogorov equation is used to study the statistical analysis of the phase error process [11, 36, 50]. The noise samples η(k)s are mutually independent at any k instant. Therefore, the phase error process ϕk can be regarded as a first-order, discrete time, and continuously variable Markov process which is also governed by modulo2π. The variable Markov process states that the first-order Markov process depends only on the previous state. As a result with a given initial phase error ϕ0, the pdf of ϕk will satisfy the Chapman-Kolmogorov equation [11, 36, 50].
- Assuming that the sampled noise process {η(k)} is a sequence of independent and identical disturbance (i.i.d) Gaussian random variables with zero mean and a variance σn2 it follows that the phase shifted noise process {η'(k)} is also a sequence of i.i.d with the same mean and variance.
- Both inputs in (6.11) and (6.12) are independent Gaussian random variables with the following statistical characteristics [50]
- Exk=Asinϕk
  (6.29)
- Eyk=Acosϕk
  (6.30)
- **varx=vary=varn=varn'=σn2**
  (6.31)
- where **n'** is of the noise that is sampled at 90ophase shifts, E represents the expectation (mean) and var represents the variance. Following similar noise analysis in Chapter 3 therefore, the joint pdf g(x,y)of the Gaussian random variables x and y is given by
- gx,y=12πσn2exp-12σn2(x-Asin(ϕk)2+(y-Acos(ϕk)2
  (6.32)
- As AGWN has a disturbance effect on both amplitude and phase, both x and y can be re-defined as in (6.33) and (6.34) respectively, which is also explained in details in Chapter 3.
- xk=Rksinϵ
  (6.33)
- yk=Rkcosϵ
  (6.34)

- where both random variables Rk and ϵ have the following limits 0<Rk<∞ and -π<ϵ <π. The joint pdf of both random variables Rk and ϵ can be obtained from (6.32) and the pdf p[ϵ] can be computed by integrating over the range from zero to infinity with respect to Rk to get
  - pϵ=12πexp-α+fα,kexp[-α sin2ϵ-ϕk-∞fα,kexp(-ω22)]dω (6.35)
- where α=A2/2σn2 is the SNR and fα,k=2αcosϵ-ϕk.
  - It is obvious that the peak of pϵ occurs at ϵ=ϕk in the modulo 2π sense. ϵ is usually around fϵ in the presence of noise, and

therefore can be decomposed into the term fϵ and the random variable ηk as in (6.32).

- ϵ= fϵ+ηk
  (6.36)
- where ηk lies in the interval (-π-fϕk,π-fϕk).
- Using both (6.35) and (6.36), the pdf of the random phase error noise disturbance pηkcan be expressed from as
- pη=12π[exp-α+αcos(η)πexp-α sin2(η)12+erf2α cos(η)
  (6.37)

- where erfx=12π0xexp-ω22dω

Statistical Behaviour of the First-order NDTL in AGWN

-
- From (6.20) the difference characteristic equation in the presence of noise of the first-order NDTL can be expressed as follows with an addition of noise term.
- ϕk+1=ϕk-K1'fϕk+Λo+K1'ηk
  (6.38)
- where ϕk is the phase error at the input of the phase detector and hψϕk=e(k) is the phase error at the output of the PD. The noise samples η(k)s are mutually independent for different values of k. Therefore, the phase error process ϕk can be regarded as a first-order discrete time and continuously variable Markov process. The first-order Markov process depends only on the previous state, so with a given initial phase error ϕ0, the pdf of ϕk will satisfy the following Chapman-Kolmogorov equation [11, 36, 50] which means that it follows the same principle of the original TDTL explained in Chapter 3.
- pk+1ϕϕo=-∞∞qkϕupkuϕodu
  (6.39)

- where pk+1ϕϕois the pdf of ϕkgiven an initial condition ϕ0 and qkϕu is the transition pdf of ϕk+1 given ϕk=u, which is given in this case as
- qψ,kϕu=12πK1'expα
- +1K1'απcos(ϕ-vK1')exp-αsin2ϕ-vK1'×12+erf2αcosϕ-vK1'
(6.40)

- where all parameters are defined from (6.35), v=u-K1'hψu+Λo and the range of ϕ is the interval (u+Λo-K1'π,u+Λo+K1'π).
- If ϕk is limited to (-π,π), (6.38) can be given by
- ϕk+1=ϕk-K1'ϕk+Λo+K1'ηk
  (6.41)
- By squaring both sides of (6.41) and then taking the statistical expectation as in (6.35) and (6.37), the steady state variance can be obtained as follows [36, 59]
- Varϕss=K1'2-K1'Eη2=-π-Eϕssπ-Eϕssη2pηdη
  (6.42)

- Statistical Behaviour of the Second-order NDTL in AGWN

-
- In the presence of noise, the difference equation (6.20) of the second-order NDTL can be modified to
- ϕk+1=2ϕk+1-rK1'ek+1+K1'ek-ϕk-rK1'ηk+1+K1'ηk
  (6.43)
- Equation (6.43) consists of two first-order difference equations that describe two Markov processes, which can be solved in a manner similar to the first-order DTL [36].
- The mean and variance are given by (6.44) and (6.45) respectively.
- Eϕss=0
  (6.44)
- Varϕss=2r-1+K1'r+14-K1'r+1Eη2
  (6.45)

○ Simulation Results

- This section presents some of the extensive set of results used to compare NDTL and TDTL. The simulations were performed in both noisy and noise-free environments. The performances of the first- and second-order NDTL systems were evaluated in comparison with that of the respective first- and second-order TDTL systems. The evaluation process included applying various sudden frequency steps and FSK input signals. The sudden frequency changes, which are either less or higher than the DCO free running frequency are indicated by a negative or a positive step respectively. This test is usually used to evaluate the acquisition time required by the system to reach its steady state [11].
- Starting with frequency step test, in noise-free environment, Figure 6. and Figure 6. illustrate the response to positive frequency steps for both the NDTL and the TDTL first- and second-order loop respectively. Clearly, NDTL requires nearly one third of the time needed by the TDTL to achieve locking state. This is reflected in the much reduced number of samples that the NDTL requires to reach steady state. Another way to express the same results is to use phase plane plots which show the consecutive phase error samples ϕk and ϕk+1 of both the NDTL and TDTL. The phase plane plots, following the application of a positive step, for the first- and second-order NDTL and TDTL are depicted in Figure 6. and Figure 6. respectively. The improvement in the acquisition time is more profound with the second-order compared with the first-order topology. This is due to the fact that the loop filter of the second-order loop is triggered by doubling the loop DCO free running frequency which improves the climbing mechanism of the accumulation filter to reach the steady state in half the time required by the TDTL.

-
- (a)
-
- (b)
-
- (c)
- Figure 6. (a) Positive frequency step input 0.2 V (b) First-order NDTL and (c) TDTL phase error responses, K_1 =1 and ψ=π/2 (rad).
-
- (a)
-
- (b)
-
- (c)
- Figure 6. (a) Positive frequency step input 0.2 V (b) Second-order NDTL and (c) TDTL phase error responses, r=1.2, K_1 =1 and ψ=π/2 (rad).
-
- (a)
-
- (b)
- Figure 6. First-order phase planes of (a) NDTL (b) TDTL with a positive frequency step of 0.2 V, K_1 =1 and ψ=π/2 (rad).
-
- (a)
-
- (b)
- Figure 6. Second-order phase planes of (a) NDTL (b) TDTL with a positive frequency step of 0.2 V, r=1.2, K_1 =1 and ψ=π/2 (rad).
- The NDTL system was also tested with FSK input signal in noise-free environment. The results for FSK demodulation are shown in Figure 6. and Figure 6. for the first- and second-order loop of both the NDTL and the TDTL respectively. It is clear that the acquisition time of the NDTL is three times faster than that of the TDTL. This is attributed to the fact that the NDTL uses a DCO with double free running frequency compared with the original TDTL, i.e. shorter intervals between the zero crossing, which results on reducing both the phase error and acquisition time to reach the steady state.
-
- (a)
-
- (b)
-
- (c)
- Figure 6. (a) FSK input (b) First-order NDTL and (c) TDTL phase error responses, K_1 =1 and ψ=π/2 (rad).
-

- (a)
-
- (b)
-
- (c)
- Figure 6. (a) FSK input (b) Second-order NDTL and (c) TDTL phase error responses, r=1.2, K_1 =1 and ψ=π/2 (rad).
- Another performance test was carried out under AWGN where both the first- and second-order NDTL were evaluated and compared with TDTL of the same orders. Figure 6. shows the phase noise pdf for the first-order NDTL and TDTL for input SNR=7 dB. The figure shows the pdf for various input frequency steps. It is clear, from Figure 6. that the first-order NDTL has better performance than the TDTL when positive or negative frequency steps were applied. Furthermore, it is evident from Figure 6. that the NDTL margin of performance improvement increases with the increase in the input frequency step. This results from the additional phase error that the time delay block in the TDTL brings to the system as the input signal frequency increases. Figure 6. shows the phase noise pdf for the second-order NDTL and TDTL systems for an input of SNR=7 dB when applying various step inputs. It is clear that the NDTL system outperformed the TDTL especially for higher frequency steps.
- The final test is jitter performance evaluation. This parameter is calculated by comparing the difference in time of the zero crossing point between the original signal in noiseless environment and the NDTL output affected by the AWGN noise. Jitter values have a critical impact on many communication systems [1, 2, 3]. The impact of noise on the jitter performance was tested and the results are illustrated in Figure 6., which indicates that the NDTL outperforms the TDTL as the SNR ratio decreases. For the second-order, the NDTL is slightly better compared to the TDTL.
-
- Figure 6. Steady state pdf of phase error of first-order system for SNR=7dB, K_1 =1 for different frequency steps.
-
- Figure 6. Steady state pdf of phase error of second-order system SNR=7dB, r=1.2, K_1=1 for different frequency steps.
-
- (a)
-
- (b)
- Figure 6. Jitter performance for a range of SNR (a) First-order (b) Second-order ,for frequency step of 0.1 V and K_1 =1.

○ NDTL System Limitations

- Although the NDTL loop has many advantages compared with the original TDTL in terms of improving linearity which has direct effects on its overall performance. This system has couple of limitations, which impacts its performance especially in implementation. The main drawbacks are:
- The NDTL system is producing a square waves and with doubling the DCO free running frequency which will have an impact on designing of the DCO there will be possibility to lock to the harmonics i.e. false locking.
- Due to the use of two dividers with direct triggering edges in designing NDTL the skew affect will have a direct impact in the performance.

○ Conclusions

- A digital tanlock loop with no time delay unit (NDTL) has been presented. The system uses two sampling frequencies with a phase shift of $\pi 2$ (rad) to preserve the quadrature sampling relationship between the two loop channels. This enhances the linearity of the PD characteristics of the TDTL. The system was evaluated in the presence as well as in the absence of noise. The acquisition performance was assessed, in a noise-free environment, by subjecting it to frequency steps that cause sudden changes in the DCO free running frequency. In addition, the acquisition performance was also evaluated using FSK input signal. The NDTL system performance showed a clear improvement in the acquisition time compared with the TDTL. The improvements in the results are even more pronounced with the second-order NDTL. The acquisition is shown to be three times faster with the new loop compared to the TDTL system.
- By corrupting the input signal with AWGN, two performance evaluation tests were performed; the pdf and phase noise (jitter) tests. Both tests indicated that the NDTL system outperformed the TDTL. For the pdf test, the first-order NDTL has better performance than the TDTL when positive or negative frequency steps were applied. The margin of improvement increases with the increase of the input frequency step. In the case of the TDTL an increase in the input step frequency results in additional phase error (i.e. nonlinearity) due to the frequency dependence of the time delay block. For the second-order systems, the NDTL system outperformed the TDTL especially for higher frequency steps. The impact of noise on the jitter performance, both first- and second-order NDTL systems have better jitter compared with TDTL. In terms of hardware implementation complexity the NDTL modified DCO requires two additional flip-flops compared with the TDTL. This is an acceptable overhead in terms of gate count for a physical implementation that achieves the aforementioned

performance. The main overhead is using double the DCO free running frequency. However, this provides an improvement of the acquisition speed by twofold for the second-order.

- The drawback resulting from the doubling the DCO free running frequency may be compromised depending on the applications.
-

COMPOSITE PHASE DETECTOR DIGITAL PHASE-LOCKED LOOP

Introduction

- This chapter describes a new digital phase-locked loop that uses an arctan based composite phase detector [103, 104]. The main feature of this new system lies in its ability to tailor its performance according to the required application using an adaptive controller. The mathematical analysis and performance testing of the systems are presented.
- As mentioned earlier the sampling process of the analogue signals is one of the major processes in a DPLL. Accordingly, DPLLs are classified as uniform and non-uniform according to the nature of the sampling process. A uniform DPLL type uses a fixed clock sampling process, which limits the speed performance of the loop. Non-uniform DPLLs achieve better speed performance with less circuit complexity. [10, 105]. The ZC-DPLL, shown in Figure 2., is an architecture that uses the non-uniform sampling approach and is widely used due to its modelling and implementation simplicity. However, the ZC-DPLL is sensitive to variations in input signal power, which is a major drawback that leads to performance degradation. In addition, the ZC-DPLL inherent nonlinearity imposes limitation on its locking range [57, 58, 106, 107, 108].
- It was therefore necessary to explore ways of improving its performance. One approach was to consider improving the design of the phase-detector (PD). Many different PD designs are reported in the literature with the aim of improving the locking range, linearity and other performance parameters of DPLL [7, 92, 108]. In this work, a composite type phase detector (CPD) is used which is a combination of a sample and hold and an arctan blocks as shown in Figure 7. [103]. The arctan block is similar to the one used in the original TDTL. This new PD offers the advantage of higher linearity and hence wider locking range capability.
- Figure 7. CPD phase detector.
- An adaptive controller block was added to the proposed loop, as shown in Figure 7., to take care of the loop's sensitivity to variations in the power of the input signal. The output X of this adaptive controller can be adjusted in order to customize the performance of the loop to suit a particular application. With these modifications, the CPD-DPLL overcomes the two main limitations exhibited by the conventional ZC-DPLL; linearity and the system's sensitivity to the variations in the input signal power

[34, 44, 59] .The proposed DPLL, shown in Figure 7., consists of a CPD, digital filter, DCO and the adaptive controller. The CPD, shown in Figure 7., offers and tailors the required performance parameters using the adaptive controller through the adaptive controller for the required application.

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- (a)
-
- (b)
- Figure 7. CPD-DPLL block diagram (a) First-order loop (b) Second-order loop.
- An example of implementing the adaptive controller, shown in Figure 7., includes a lookup (LUT) table that can be adjusted for different applications, which will be elaborated on in the following sections. The adaptive controller consists of an envelope detector, Frequency Estimator (FE), Subtractor, FSM, and the adjustable LUT. This provides the required X values which depend on the input signal amplitude A and the input signal frequency for the desirable application as will be shown later. The Adaptive Controller uses the envelop detector and FE for sensing purposes and the FSM and the adjustable LUT for decision purposes for the required application.
-
- Figure 7. Adaptive controller suggested block diagram.

○ Mathematical Model, Analysis and Discussion

- In this section the mathematical model, analysis and discussion of both first- and second-order CPD-DPLL are discussed in details taking into consideration the effect of the adaptive controller output X on both acquisition and locking range.
-

□ First-order CPD-DPLL Loop

- In the analysis of the first-order CPD-DPLL system of Figure 7., it is assumed that the input to the loop is a continuous time dependent sinusoidal signal of the form given in (7.1). This is similar to the process followed in [11, 50, 44, 59].
- $yt=A\sin\omega ot+\theta t$
  (7.1)
- where A is the amplitude of the signal, ωo(rads) is the free running frequency of the DCO, and θt is the information bearing phase in radians. Assuming a frequency step at the input, the phase of the phase process is
- $\theta t=\omega-\omega ot+\theta o$
  (7.2)

- where ω (rads) is the angular frequency of the input signal and θo (rad) is a constant. The discretized signal generated by the sampler is
- yk=Asinωotk+θk
  (7.3)
- where tk is the elapsed time up to the k^{th} sampling instant. The sampling interval of the DCO between the sampling instants tk+1and tk is given by
- Tk=To-ck-1
  (7.4)
- where To=2πωo(s) is the free running period of the DCO, while ck-1 is the output of the digital filter at the previous sampling instant. The total time up to the k^{th} sampling instant may be expressed as
- tk=i=1kTi=kTo-i=0k-1ci
  (7.5)
- Using (3.9) and (7.5), (7.3) can be re-written as
- yk=Asinϕk
  (7.6)
- The digitized input signal y(k) and the output of the adaptive controller signal (X) are applied to the arctan phase detector producing the error signal ek
- ek=ftan-1AsinϕkX
  (7.7)

- where fγ=-π+[γ+πmod 2π]
  - The error signal ek will serve as an input to the digital filter whose transfer function is Dk and its output is the signal ck that drives the DCO. Therefore, the system difference equation can be derived from (7.5), (7.6) and (7.7) as follows which is also derived in details in Chapter 3.
  - ϕk+1=ϕk-ωck+Λo
    (7.8)
- where Λo=2π(ω-ωo)/ωo
  - The digital filter of the first-order loop consists of a single gain block whose gain is denoted as G1. Therefore, the system difference equation can be redefined as follows which is also derived in details in Chapter 3.
  - ϕk+1=ϕk-K1'hϕk+Λo
    (7.9)
  - ϕk+1=ϕk-K1'tan-1Asin ϕkX+Λo
    (7.10)
- where K1'=ωG1.
  - Defining K1=ωoG1 will result in K1'=K1W, where W=ωoω. Following the analysis in [50] and follows similar analysis in Chapter 3, the locking range of the first-order loop can be found by numerically solving the inequality
  - 21-W<K1<2WA2sin2α1+X2AXcosα1
    (7.11)
- where α1=asinβ1, β1=XA*tan(η) and η=Λo K1'
- The steady state phase error ϕss is

- ϕss=α1+jπ,j1,0,-1
  (7.12)
- Figure 7., plotted using (7.11); depicts changes in the locking range of the first-order CPD-DPLL as a function of both, the input signal amplitude (A) and the input controller (X). Figure 7.a shows the locking range behaviour of the CPD-DPLL for two different values of X with (A=1 V), whilst Figure 7.b illustrates the changes in the locking range for various input signal (A) values with (X=1 V).
- Figure 7.a and Figure 7.b, plotted using (7.11), depict changes in the locking range of the first-order CPD-DPLL as a function of both input signal amplitude (A) and the input controller (X) produced by the adaptive controller. Figure 7.a shows the behaviour of the CPD-DPLL for various values of X at (A=1 V). Figure 7.b illustrates the changes in the locking range for various input signal (A) values at (X=1 V). Figure 7.c shows the locking range of the conventional non-uniform ZC-DPLL and enables comparison with that of the CPD-DPLL. The plot in Figure 7.c is basically fixed and the system designer does not have much control on it.
- From the plots in Figure 7.a and Figure 7.b, and for an operating condition of $K_1=1$ and $W=1$, the locking range can be customized according to the particular application requirements. For example, for a $0.6 \leq X \leq 2$ the loop can operate under input signal variation in the range of $0 \leq A \leq 1.8$.
- The ability to control the major loop parameters through the choice of X, while A is within the range indicated above, can solve the conflicting requirements of the locking range and acquisition speed. This also affects the noise performance of the system which will be addressed in the following section. However, if the adaptive controller output X is used to follow A in the range above then a very fast acquisition system can be designed which will be discussed later. The following subsections present the analyses of the various performance parameters of the proposed loop.
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- (a)
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- (b)
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- (c)
- Figure 7. Locking range of the first-order (a) CPD-DPLL with fixing (A=1 V) and changing X (b) CPD-DPLL with fixing (X=1 V) and changing A (c) ZC-DPLL, $K_1=G_1\omega_o$ and $W=\omega_o/\omega$.

- Locking Range

- To gain the widest possible locking range the adaptive controller output X can be expressed as
- X=f1Asinωtk+θ0tanckG1
- = f1y(t)tanckG1
  (7.13)

- where f1γ=γ+πmod 2π, yt is the input signal, A is the amplitude of the signal, ω(rads) is the input signal frequency and θ0 is the initial phase in radians. From (7.13) it is obvious that the adaptive controller output X value has a nonlinear relationship with the amplitude and frequency of the input signal. Therefore, the performance in terms of acquisition and locking range can be controlled through the CPD-PD using the adaptive controller output X.
- From (7.13) it is evident that the adaptive controller output X is proportional to the input signal amplitude A with a nonlinear factor which is controlled by the incoming signal frequency, the output of the loop filter, and the initial phase. To reduce the loop sensitivity to the incoming signal amplitude, the adaptive controller output X value should be at least equal to A or higher. This ensures that any degradation in the performance of the loop is negligible as long as the amplitude of the input signal is less than the value of adaptive controller output X.
- Therefore, to obtain maximum linearity, the characteristic equation (7.10) can be modified using (7.13) to
- ϕk+1=ϕk-K1'tan-1Asinϕky(t)tanckG1+Λo
- ϕk+1=ϕk-K1'ckG1+Λo
- ϕk+1=ϕk-K1'ϕk+Λo
  7.14

- From (7.14) proper design of the adaptive controller can ensure linear characteristic equation.
- From (7.11) and (7.13) the locking range can be re-expressed as
-
  - 21-W<K1<2Wsin2α1+y(t)tanckG12Ay(t)tanckG1cosα1
    (7.15)
- where α1=asinβ1, β1=XA*tan(η) and η=Λo K1'
  - To set the locking range size to the desired value a proper selection of amplitude and frequency of the incoming signal and the filter output c(k) values should be made by using the adjustable LUT with the help of envelop detector, FE, subtractor and the FSM.

• Acquisition

- To show the effect of the adaptive controller output X values on the convergence speed and after following the fixed-point analysis developed in [57, 58, 109] and follows similar analysis in Chapter 3 the steady state phase error is
- ϕss=α1 β1sinη≥0 fα1+π otherwise.
  (7.16)
- where α1=asinβ1, β1=XA*tan(η) and η=Λo K1'
  - The characteristic function of the PD and its first derivative are continuously differentiable in the principal interval –π,π, hence fixed-point analysis is applicable to the CPD-DPLL. Following fixed-point analysis developed in [57, 58, 59] for the sinusoidal DPLL, the Lipschitz constant is given by

- L=maxgϕ-gϕss ϕ-ϕss
  (7.17)

- where gϕ can be expressed as
  - gϕ=ϕ-K1'tan-1AsinϕkX+Λo
    (7.18)
  - The asymptotic estimate (upper bound) to the number of steps required for convergence of the phase error ϕk within a radius ϵ of the fixed-point ϕss is given by
  - m=int lnϵϕ-ϕsslnL+1
    (7.19)
- where int . is the integer function.
  - It can be shown that the time required to reach the fixed-point steady state ϕss is given by
  - Tc=mToW+ϕm-θoω≈mToW
    (7.20)
  - where ϕm-θoω≪mT0W
  - As a result equation (7.20) shows the effect of both the input signal amplitude and frequency in the acquisition time performance.
  - From (7.13), (7.15) and (7.20) all performance parameters of locking range, input power sensitivity and the acquisition time can be controlled. These equations are the fundamental for designing the adaptive controller block in such a way that it meets the requirements of a particular application. The results in the simulation section demonstrate the effect of the adaptive controller block on the overall loop performance.

Second-order CPD-DPLL Loop

  - For the second-order loop, the digital loop filter utilizes a proportional-plus accumulation digital filter with a transfer function as shown in (3.34). Therefore, the system difference equation can be redefined as follows by following similar analysis in Chapter 3 and as in [110].
  - ϕk+2=2ϕk+1-ϕk-K1'ek +rK1'ek+1
    (7.21)
  - ϕk+2=2ϕk+1-ϕk+K1'tan-1AsinϕkX-rK1'tan-1AsinϕkX
  - (7.22)
- where ϕk is the phase error at the instant k, K1'=ωG1, and r=1+G1G2.
  - In the steady state ϕk+2=ϕk+1=ϕk=ϕss, as a result (7.22) becomes
  - K1'tan-1(AsinϕssX)+rK1'tan-1(AsinϕssX)=0⟹ϕss=0
    (7.23)
  - Thus, the second-order CPD-DPLL locks onto zero steady state error. Nevertheless, (7.23) has the general solution
  - ϕss=nπ n=0,±1, ±2
    (7.24)
  - From (7.24), it is clear that the steady state phase error ϕss is a multiple of πs (i.e. ϕss=nπ, where n is an integer). In view of the

fact that f[ϕss]≠±π, the f[ϕss] must equal zero, hence ϕss=2mπ (m is an integer). Following the fixed-point analysis given by [2, 7, 11] the locking condition that the Eigen values of matrix G using Jacobian for (7.22) is given as

- G=01-1+K1'XAcosϕssX2+A2sin2ϕss2-rK1'XAcosϕssX2+A2sin2ϕss (7.25)

- Consider the fixed-point ϕss=0,2mπ , then (7.25) will be
  - G=01-1+K1'AX2-rK1'AX (7.26)
- In order to have the eigenvalues less than 1, therefore we must have
  - 0<K1<Wβ24r+1, r>1 (7.27)
- where β2=XA
  - Figure 7.a and Figure 7.b, plotted using (7.27), depict changes in the locking range of the second-order CPD-DPLL as a function of both input signal amplitude (A) and the input controller (X) produced by the adaptive controller. Figure 7.a shows the behaviour of the CPD-DPLL for various values of X at (A=1 V). Figure 7.b illustrates the changes in the locking range for various input signal (A) values at (X=1 V). Figure 7.c shows the locking range of the conventional non-uniform ZC-DPLL. The plot in Figure 7.c is basically fixed and the system designer does not have much control on it.
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  -
  - (a)
  -
  - (b)
  -
  - (c)
  - Figure 7. Variations of the locking range the second-order (a) CPD-DPLL with fixing (A=1 V) and changing X (b) CPD-DPLL with fixing (X=1 V) and changing A (c) ZC-DPLL, r=1.2 and K_1 =1.

- Locking Range

  - To obtain maximum linearity, the characteristic equation (7.22) can be modified using (7.13) with direct substitution to
  - ϕk+2=2ϕk+1-ϕk+K1'tan-1Asinϕky(t)tanckG1-rK1'tan-1Asinϕky(t)tanckG1
  - ϕk+2=2ϕk+1-ϕk+K1'ϕk-rK1'ϕk 7.28
- From (7.28) proper design of the adaptive controller can ensure linear characteristic equation.
- From (7.28) and (7.13) and by following similar analysis explained in Chapter 3 therefore the locking range can be re-expressed as
  - 0<K1<Wy(t)tanckG1A4r+1 (7.29)
  - To set the locking range size to the desired value a proper selection of amplitude, frequency of the incoming signal and the

filter output c(k) values should be done by using the adjustable LUT with the help of envelop detector, FE, subtractor and FSM.

-
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- Acquisition

- As previously highlighted, the convergence of the second-order loop is directly controlled by the samples produced by the DCO which are used to control the loop filter. With the CPD-DPLL architecture, the number of DCO samples used to control the loop filter will not change but the flow speed of the phase error produced by the sample-and-hold block will be controlled by the arctan. This is due to fact that the arctan will act as a re-limiter which will have the effect on increasing/decreasing the speed flow of the produced phase error going to the loop filter for convergence purpose. Therefore the DCO samples intensity for that particular period will increase as the flow speed decreases which is directly controlled by the arctan. Consequently, changing the output X of the adaptive controller will have an effect on the acquisition time by increasing/decreasing the sampling process intensity [111].
- The CPD-DPLL has similar concept effect discussed in [41, 112, 113, 111] which depends on increasing the number of samples in the PD that is used in estimating the phase difference. The CPD-DPLL advantage over method discussed in [41, 112, 113, 111] is the design simplicity which only requires proper controlling of the X factor instead of changing the DCO sampling rate. This will not only have an effect on the convergence behaviour but also will improve the locking range without affecting the noise performance. This is due fact that the arctan will act as limiter that provide more sampling concentration without changing the DCO samples rate.

o CPD-DPLL Noise Analysis

- For the purpose of noise analysis, it is assumed that the incoming input signal is corrupted by an AWGN with zero mean and two sided power spectrum density of Gnwf=no/2. Therefore, the autocorrelation can be given by the inverse Fourier Transform of Gnwf as $R\tau=no\delta(\tau)/2$ [2, 7, 61]. Where $\delta\tau$ represents the Dirac Delta function. As a result, $R\tau=0$ for $\tau\neq0$ so any two different samples of this kind of noise are uncorrelated and for this reason it statistically independent [2, 63].
- Due to the discrete nature of the CPD-DPLL, the statistical analysis of the phase error process can be obtained by studying the Chapman Kolmogorov equation [10]. The noise samples $\eta(k)$s are mutually independent for different sample instants k i.e. i.i.d Gaussian random variables with zero mean and a variance $\sigma n2$. Therefore, the phase error process ϕk can be regarded as a first-

order, discrete time, and continuously variable Markov process which is also governed by modulo 2π. The variable Markov process states that the first-order Markov process depends only on the previous state. As a result with a given initial phase error ϕ0, the pdf of ϕk will satisfy the Chapman-Kolmogorov equation and stated as follows.

- pkϕϕo=-∞∞qkϕupkuϕodu
  (7.30)

- Where ϕo=ϕ(0) initial phase error value, pkϕϕo is the pdf of the ϕ(k+1) given ϕoand qkϕu is the pdf of ϕ(k+1) given k=u .

First-order CPD-DPLL Loop

- For first-order CPD-DPLL noise analysis, (7.10) can be rewritten as
  - ϕk+1=ϕk-K1'tan-1AsinϕkX+Kn'ηk+ Λo (7.31)
- where K1'=ωG1 which results in K1'=K1W, W=ωoω and Kn'=K1'A.
  - Since samples from ϕk is independent at any sampling instant k and is a continuously variable Markov process state, the transient response of the probability density function qkϕu can be described as
  - qkϕu=1σ2πexp[-ϕ-u-K1'tan-1AsinuX+Λo22σ2] (7.32)
- where ϕ=ϕk+1, u=ϕk and variance σ2=(Kn')2σn2 with Expectation mean as
  - Eϕk+1u=u-K1'tan-1AsinuX+Λo
    (7.33)
- which is independent of k due to use of modulo 2π process.
- To find the mean, expectation of both sides of (7.31) is taken which yields to
  - Eϕk+1=Eϕk-K1'Etan-1AsinϕkX+Λo (7.34)
- As the value of k approaches infinity, the stationary means is
  - Etan-1AsinϕX=ΛoK1'
    (7.35)
  - To linearize and simplify the equation for analysis purpose, the control signal should be selected so that X=A . Therefore, (7.32) can be further simplified to
  - Etan-1AsinϕX≈sinϕ1≈XAΛoK1'≈ΛoK1'
    (7.36)
  - To derive the variance of phase error σϕ2, equation (7.34) is squared and the Expectation is computed.
  - Eϕ2=Eϕ2+-K1'2Etan-1AsinϕX2+Kn'2σn2 +Λo-2K1'Etan-1AsinϕX-2K1'ΛoEtan-1AsinϕX+2ΛoEϕ
    (7.37)
  - When the first-order CPD-DPLL is in the tracking mode and assuming that X=A then tan-1AsinϕX≈AXϕ which results in
  - σϕ2=Eϕ2-ϕ12=XKn'2σn2 AK1'cosϕ12-cosϕ1
    7.38
  - Where ϕ1 is the locked state phase error.
  - This is a linearized variance of the phase error with a mean of ϕ1 results in a phase error pdf of

- pϕ=1σn2πexp-ϕ-ϕ122σn2
  7.39

Second-order CPD-DPLL loop

- For the second-order CPD-DPLL noise analysis, by adding a noise term and following similar analysis in explained in Chapter 3 therefore (7.22) can be rewritten as
- ϕk+2=2ϕk+1-ϕk+K1'tan-1AsinϕkX-rK1'tan-1Asinϕk+1X-rK1'ηk+1 + K1ηk
  (7.40)
- The phase error generated by this equation is not Markovian. Therefore, an auxiliary variable should be introduced to be able to use Markovian chain properties as follows:
- uk+1=2-1rϕk+1-ϕk+ukr
  (7.41)

- This allows equation (7.40) to be written as two equations
  - ϕk+1=-rK1'tan-1(AsinϕkX)+uk-rKnnk
    (7.42)
  - and
  - uk+1=-ϕk-2r-1K1'tan-1AsinϕkX+2uk-2r-1Knnk (7. 43)
  - In this format, the two vectors ϕk+1, uk+1 are Markovian, therefore Chapman-Kolmogorov equation can be applied
  - Pk+1ϕk+1=ϕ,uk+1=uϕo,uo=
  - -∞∞qk[ϕk+1=ϕ,uk+1=uϕk=X,uk=Y]
  - × Pkϕk=X,uk=Yϕo,uodXdY
    (7.44)
-
- The pdf can then be written as
  - Pk+1ϕk+1=ϕ,u k+1=u =1 σ r 2π-∞∞exp2xp K1'tan-1AsinϕkX22σ2
  - × Pkϕk=X,Uk=2r-1AXϕ+r(u+X) dX
    (7.45)
  - To derive linear approximation of pdf Expectation is taken for (7.42) at the steady state
  - Etan-1(AsinϕkX)=0
    (7.46)
  - Eϕ=Eu=0
    (7.47)
- This is the mean value, which is equal to zero. Squaring both sides of both equations (7.42) and (7.43) then taking the Expectation of each and letting k goes to infinity i.e. as the steady-state is approached, results in the following two equations:
  - Eϕ2=E-rK1'tan-1AsinϕX+u2+r2Kn2σn2
    (7.48)
  - Eu2=E-ϕ-2r-1K1'tan-1AsinϕX+2u2+(2r-1)2Kn2σn2 (7.49)
  - When the second-order CPD-DPLL is the in tracking mode and by choosing the control signal to be X=A, the tan-1AsinϕX≈ϕ which results in linearization of both (7.48) and (7.49) as:

- $E\phi 2=r2+12-K1'-2r(2-rK1')K1'(2-K1')2-(2-rK1')2Kn2\sigma n2$ (7.50)
- $Eu2=5r2-4r+12-K1'-2r(2r-1)(2-rK1')K1'(2-K1')2-(2-rK1')2Kn2\sigma n2$ (7.51)
- This result in a linearized variance of $E\phi 2$ with a zero mean $E\phi=0$, therefore the pdf is
- $p(\phi)=1\sigma n2\pi exp-\phi 22\sigma n2$ (7.52)

○ Simulation Results and Discussion

- The dynamic performance parameters of both first- and second-order CPD-DPLL systems in terms of the locking range, acquisition, and noise performance will be discussed in the next subsection. These parameters depend on customizing the adaptive controller to achieve the performance required by the particular application. The system performance features will be compared with those achieved by the conventional ZC-DPLL. A possible realization of the adaptive controller can be achieved by using an FE, envelope detector and a FSM. This provides the required adaptive controller output X values that depend on the input signal amplitude (A) and frequency for the desirable performance.

First-order CPD-DPLL Loop

- Performance of the first-order CPD-DPLL is evaluated by different tests. Starting with the evaluation of the locking range affected by both input signal amplitude A and the adaptive controller output X. Then applying a frequency input step to the loop to evaluate the acquisition time, and finally applying an AWGN to the loop to evaluate the noise performance.

• Locking Range

- The locking range (M) is defined here as the maximum tolerable deviation of the input signal frequency (ω) from the DCO free running frequency ωo at K1=1. Figure 7. illustrates the locking range as function of both adaptive controller output X and A as will be investigated below. As shown in Figure 7.a and Figure 7.b, variations in the adaptive controller output X values are affected by the changes in A. This has different effects on the system locking range M. The relation between the locking range M and A for different controller output X values is shown in Figure 7.. Therefore, to compensate for the input signal power variation, different values of the adaptive controller output X should be produced according to Figure 7. in order to provide the required locking range. This will result in fixing the looking range to the variation of the input signal power. For example, to set the locking range to 0.15 the adaptive controller should provide a

value of (X=2.5 V) for the input power range of $0 \leq A \leq 3$, which eliminates the problem associated with the conventional ZC-DPLL. It is to be noted that the values for M in Figure 7. represent the spread in the locking range around the frequency ratio W=1 and loop gain $K_1=1$.

- Figure 7. Variations in the locking range size (M) with A and X.

- Acquisition

- The acquisition time is the time required for the error signal ek to reach a steady state condition following a sudden change in the frequency of the input signal. Figure 7. shows the response of the first-order CPD-DPLL to a positive input frequency step of 0.2 V in comparison with the conventional ZC-DPLL. It can be seen from the transient response in Figure 7.b that the CPD-DPLL system acquired locking within one cycle compared with 10 cycles for the conventional ZC-DPLL. Similar results were obtained when a negative step was applied.
- The system acquisition time performance under different frequency steps with various values of A and the adaptive controller output X was investigated as shown in Figure 7.. The plots indicate that there is a minimum acquisition time for particular values of A and X for different frequency steps. Figure 7.c shows the acquisition time for particular values of the adaptive controller output X and with fixed value of (A=1 V) for different frequency steps. Therefore, the adaptive controller needs to re-map the changes in both the amplitude and frequency of the input signal with the appropriate values to achieve the required acquisition time using the LUT.

- (a)
- (b)
- (c)
- Figure 7. (a) Positive frequency step , (b) First-order CPD-DPLL transient response (c) First-order conventional ZC-DPLL transient response, for $K_1 =1$, (A=2 V), and (X=0.2 V).

- (a)
- (b)
- (c)
- Figure 7. Acquisition time as a function of X and A for different frequency steps.

- The adaptive controller block that monitors changes in the input signal amplitude and frequency will provide information to produce the adaptive controller output values to achieve the required goal. Figure 7. shows the effect of variations in A on the value of adaptive controller output X for various frequency steps to achieve fast acquisition. The plots in the figure are generated from Figure 7. for minimum acquisition time.
- For example, assuming that (A=1 V), (X=1 V), K1=1, and a negative frequency step of -0.1 V is applied, then the response of the CPD-DPLL is as shown in Figure 7.b which shows slowness in the acquisition time. However, when the same conditions are applied to the adaptive controller algorithm of the CPD-DPLL a new value for (X=0.6 V) is generated automatically to give a faster acquisition response as shown in Figure 7.c which shows a reduction by 6 cycles. These figures clearly show the improvement in the acquisition speed that can be achieved by the adaptive CPD-DPLL.
-
- Figure 7. Fast acquisition as a function of A, X, and frequency steps (S).
-
- (a)
-
- (b)
-
- (c)
- Figure 7. (a) Negative frequency step (b) Adaptive CPD-DPLL response with (X=1 V), (c) Adaptive CPD-DPLL response with (X=0.6 V), for K1 =1.

Noise Performance

- This section presents the effect of AWGN on the performance of the first-order CPD-DPLL. Some of the simulation results achieved are shown in Figure 7.. It can be seen from the plots that the system noise performance improves as the locking range decreases due to an increase in the adaptive controller output X value. However, as X decreases the locking range increases causing the noise performance of the system to degrade. It should be pointed out that decreasing the locking range leads to an increase in the system acquisition time and vice versa. Figure 7. shows that the conventional ZC-DPLL has similar performance compared with the CPD-DPLL when (X=0.94 V) is chosen. However, better performance can be achieved with a selection of (X=3 V) for a different input signal SNR.
-
- (a)
-
- (b)
-

- (c)
- Figure 7. Noise performance of CPD-DPLL and ZC-DPLL for (a) SNR=5dB (b) SNR=10dB (c) SNR=15dB, (A=1 V), K_1 =1 and frequency step 0.05 V.
- The preceding sections established that the value of X, which is controlled by the adaptive controller, has direct impact on the system locking range, acquisition speed, and noise performance. This interdependency enables optimization of the CPD-DPLL to meet the particular application requirements. For example some communication applications, such as global positioning systems require (GPS) [92, 114, 115, 116] fast acquisition with a wider locking range in the transition state whereas in a steady state a narrow locking range is required to have better jitter and noise performance.
- For example, in Figure 7.d, for (A=1 V), K1=1, (X=0.94 V), and when the system is subjected to a frequency step of 0.05 V the transient response in Figure 7.b shows that the system acquires locking in one cycle. Since the locking range is wide, fast acquisition achieved is at the expense of degradation in noise performance. However, under the same condition with a value of (X=3 V), i.e. narrower locking range, the system takes 14 cycles to achieve locking as illustrated in Figure 7.c but with much better noise performance. Hence, it is possible to design a system that has fast acquisition and improved noise performance by adaptively changing the value of adaptive controller output X. For all the above dynamic changes for the CPD-DPLL system the ZC-DPLL shows a fixed acquisition time similar to CPD-DPLL condition with a value of (X=0.94 V) and locking range as depicted in both Figure 7.d and Figure 7.c respectively.
- The impact of noise on the jitter performance of the CPD-DPLL compared with the conventional ZC-DPLL was evaluated and the results are shown in Figure 7.. It can be seen from the figure that the average jitter for the loop with wide locking range (X=0.94 V) is higher than that with narrow range (X=3 V). In addition, the figure shows that the jitter for (X=0.94 V) is around three times higher than when (X=3 V) is applied. Moreover, the figure shows that the conventional ZC-DPLL has similar performance of the CPD-DPLL condition with a value of (X=0.94 V).
-
- (a)
-
- (b)
-
- (c)
-
- (d)
-
- (e)
- Figure 7. (a) Positive frequency step (b) Transient response of the CPD-DPLL with (X=0.94 V) (c) Transient response of the CPD-DPLL with (X=3 V)

(d) Locking range, (A=1 V) and K_1 =1 (e) Transient response of the
ZC-DPLL, for K_1 =1.

- Figure 7. CPD-DPLL and ZC-DPLL jitter performance for a range of SNR, (A=1V), frequency step 0.05 V and K_1 =1.

Second-order CPD-DPLL Loop

- Performance of the second-order CPD-DPLL is evaluated by different tests as previously done. The detail will be discussed in the consecutive subsections.

Locking Range

- The locking range size (M), defined previously as the maximum deviation of ω going to higher or lower frequencies from the DCO free running frequency at specific K1. The variation of the controller X values for different input signal Amplitude (A) shows changes in the locking range (M) size as illustrated in Figure 7.a. Taking more points by changing the adaptive controller output X with measurement of the locking range size M provides a relation between then as shown in Figure 7..
- In addition, the variation in the input signal Amplitude (A) for different adaptive controller output X values shows a variation in the locking range (M) size as depicted previously in Figure 7.b. To plot a relation between the locking range sizes M with a variation in the input signal amplitude A for different X controller values more results of Figure 7. were measured which is shown in Figure 7..

- Figure 7. Locking range size (M) versus the adaptive controller output
(X) for different input signal amplitude (A).

- Figure 7. Locking range size (M) versus the input signal amplitude (A)
for different adaptive controller output (X).

Acquisition

- The acquisition is the time required for the loop to reach the steady state, which can be evaluated by subjecting the CPD-DPLL loop to a frequency step to shift the DCO free running frequency, either lower or higher and measure the required time for the loop to settle to the zero steady state. For the second-order loop, only one step frequency is required to accomplish this test. This is due to fact that the convergence of the second-order, as explained

earlier, has no direct relation with the size of frequency step away from the DCO.

- The system acquisition time performance under a frequency step with various values of A and the adaptive controller output X was investigated as shown in Figure 7.. The plots indicate that there is a minimum acquisition time for particular values of A and X for different frequency steps. Therefore, the adaptive controller needs to re-map the changes in both the amplitude and frequency of the input signal, using LUT, with the appropriate values to achieve the required acquisition time.

•

- (a)
-
- (b)
- Figure 7. Acquisition time as a function of X and A for a frequency

  step 0.05 V.
- Figure 7., Figure 7., Figure 7. and Figure 7. illustrate the responses behaviours of the second-order CPD-DPLL to positive and negative frequency inputs of 0.05 V away from the DCO free running frequency with a change in the input Amplitude (A) and the adaptive controller output (X). Figure 7. illustrates the acquisition responses the affected by changing in the adaptive controller output X value with fixing A value to 1 V. The same affect in the acquisition time can be achieved by a change in the input signal amplitude as shown by Figure 7.. Therefore, both figures show that the acquisition time is indirectly dependent on the ratio of the input signal amplitude A and the adaptive controller output X. The reason for that, as explained earlier, is the role of the arctan for re-scaling and controlling the intensity entering the loop filter which is controlled by samples produced by the DCO. Consequently, the loop filter is indirectly controlled by the ratio between the input Amplitude A and the adaptive controller output X. The effect of the negative frequency step input of 0.05 V (i.e.5 % of the DCO frequency) away from the DCO free running frequency is shown in both Figure 7. and Figure 7. which illustrates the change in the input Amplitude (A) and the adaptive controller output (X).

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- Figure 7. Effect of changing A and fixing (X=1 V) in the acquisition time
  for a positive frequency input of 0.05V away from the DCO free running
  frequency, r=1.2 and K_1 =1.
-
- Figure 7. Effect of changing X and fixing (A=1 V) in the acquisition time
  for a positive frequency input of 0.05V away from the DCO free running frequency, r=1.2 and K_1 =1.
-

- Figure 7. Effect of changing A and fixing (X=1 V) in the acquisition time for a negative frequency input of 0.05V away from the DCO free running frequency r=1.2 and K_1 =1.
-
- Figure 7. Effect of changing X and fixing (A=1 V) in the acquisition time for a negative frequency input of 0.05V away from the DCO free running frequency, r=1.2 and K_1 =1.

• Noise Performance

- This section presents the effect of AWGN on the performance of the second-order CPD-DPLL. Some of the simulation results achieved are shown in Figure 7.. It can be seen from the plots that the system noise performance improves as the locking range decreases due to an increase in the adaptive controller output X value. However, as X increases the locking range increases causing the noise performance of the system to improve which has opposite behaviour compared with the first-order. This is due to fact that the number of consecutive observation samples in the PD used in estimating the phase difference is increased. This has an effect on improving the noise performance in compensation with degradation in the acquisition time as also discussed in [111] and as explained earlier of the arctan role.
- Figure 7. shows that the conventional ZC-DPLL has similar performance compared with the CPD-DPLL when (X=1 V) is chosen. However, better performance can be achieved with a selection of (X=4 V) for a different input signal SNR.
-
- (a)
-
- (b)
-
- (c)
- Figure 7. Noise performance of CPD-DPLL and ZC-DPLL for (a) SNR=5dB (b) SNR=10dB (c) SNR=15dB, (A=1 V), K_1 =1 for frequency step of 0.05 V.
- The impact of noise on the jitter performance of the CPD-DPLL compared with the conventional ZC-DPLL was evaluated and the results are shown in Figure 7.. It can be seen from the figure that the average jitter for the loop with wide locking range (X=4 V) is higher than that with narrow range (X=1 V). In addition, the figure shows that the jitter for (X=1 V) is around five times higher than when (X=4 V) is applied. Moreover, the figure shows that the conventional ZC-DPLL has similar performance of the CPD-DPLL condition with a value of (X=1 V).

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- Figure 7. CPD-DPLL and ZC-DPLL jitter performance for a range of SNR, (A=1V), frequency step 0.05 V and K_1 =1.

Conclusions

- A non-uniform DPLL that uses a CPD and an adaptive controller is proposed in this chapter. The two main limitations exhibited by the conventional ZC-DPLL; the loop's nonlinearity and its sensitivity to input signal amplitude variation have been overcome in the proposed CPD-DPLL loop. The CPD which is composed of two blocks; a sample-and-hold and an arctan block, offers much improved linearity and hence improved locking range when compared to the ZC-DPLL.
- For first-order loop fast acquisition with wider locking range can be obtained by reducing the adaptive controller output X through a re-mapping process simply using a LUT. This, however, leads to degradation in the system SNR and jitter performance. On the other hand, for improved SNR and jitter performance, the value of X needs to be increased. This results in reducing the acquisition speed and narrowing the locking range. Through proper selection of the adaptive controller output values, the CPD-DPLL offers many improvements in system performance when compared with the conventional ZC-DPLL.
- For second-order loop, wide locking range can be obtained by increasing the value of the controller X. This however, leads to improvement in the system SNR and jitter performance. This is due to fact that the arctan will act as a moderator which will have the effect on increase/decrease speed flow of the produced phase error going to the loop filter for convergence purpose by only changing the X controlled output. Therefore, the DCO samples intensity for that particular period will increase as the flow speed decreases which is directly controlled by the arctan. This interdependency enables optimization of the second-order CPD-DPLL to meet the particular application requirements.

APPLICATIONS

Introduction

- The applications of DPLLs have grown to span a wide spectrum of systems including various communications, control, signal processing systems, clock extraction and generation, signal demodulation and frequency modulation threshold extension [7, 93, 92, 117, 118, 119, 120]. This chapter describes a variety of applications that may use the above proposed tanlock-based DPLL architectures. These applications include FSK demodulation, FM threshold extension, FM demodulation with improved THD, and Doppler effect improvement.

FSK Demodulation

- Frequency-shift-keying (FSK) is a well-known modulation scheme that is common in many communication systems, such as radio broadcasting and the Internet modem. Modems use multiple frequency-shift keying (MFSK) which is a variation of FSK that uses more than two frequencies. The most fundamental concept of the function of the modem is that it can convert the digital binary signal from the computer to a sinusoid signal with varying frequencies for transmission along the cable and back to binary signals to be input into the computer after it reaches its destination.
- The test shown in this section is performed by varying the noise level in the communication channel which sweeps the SNR from -5 to 20 dB and then demodulate the MFSK signal to produce the BER. This test, which used a four-level FSK signal, was carried out for different tanlock-based architectures which were developed during this work, and a comparison was drawn with the original TDTL and the theoretical graph as indicated in Figure 8.. The figure shows that the NDTL architecture has the best BER performance, while the CPD-DPLL has the worst performance, which however was enhanced by changing the value of the X controller from one to three. The feedback fast concept has better performance than the conventional TDTL while the NDTL has outperforms the TDTL-LPD.
- Figure 8. BER performance of different TDTL enhanced architectures
  for 4 levels FSK modulations.

CEOFDM Demodulation

- One of the most popular modulation techniques for wireless digital communications is the orthogonal frequency division

multiplexing (OFDM). There are two main drawbacks of the OFDM modulation [121]. The first one is its high sensitivity to time variations in the channel caused by high dynamic environment such as Doppler, carrier frequency offsets, and phase noise. The second drawback is that the OFDM waveform has a high amplitude fluctuation which is known as the peak-to-average power ratio (PAPR). As PAPR increases, the OFDM will have higher sensitivity to nonlinear distortion produced by the transmitter's power amplifier (PA). Lacking of a sufficient power back-off will have an effect of spectral broadening, intermodulation distortion, and consequently, performance degradation. A high level of back-off reduces the efficiency of the PA. A new PAPR improvement technique is presented using a constant envelope OFDM (CEOFDM) by transforming the high PAPR OFDM signal in to a constant envelope waveform [122]. Therefore, the constant envelope signal can be efficiently amplified with nonlinear power amplifiers thus achieving greater power efficiency. In this subsection, the tanlock-based architectures are used to demodulate the constant CEOFDM as shown in Figure 8.. This figure demonstrates the possibility to use the TDTL as a phase demodulator in the CEOFDM receiver which may make it possible to use nonlinear PA in the CEOFDM transmitter.

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- Figure 8. CEOFDM modulations and demodulation block diagrams.
- The performance of the system is evaluated using a CEOFDM with 8 PSK in the transmitter. The communication channel is also affected by 10% Doppler effect to show the effect of tanlock-based DPLLs performance. The BER of the received signal is measured for different architectures and the theoretical graph as shown in Figure 8.. The figure shows that the NDTL architecture has the best performance, while the CPD-DPLL has the worst performance which was enhanced using the adaptive controller by changing the value of its output X from one to three. The feedback fast concept has better performance by 20% compared with the original TDTL, while the TDTL-LPD has slightly reduced performance by 30%. The best performance can be achieved by the NDTL architecture which has an improvement of 90% compared with the original TDTL.

•

- Figure 8. BER performance of different TDTL enhanced architectures
  for CEOFDM modulations.

○ FM Threshold Extension for Satellite Applications

- By definition, the most common criteria of assessing the performance of an FM demodulator are based on the capability of the receiver to provide a linear relationship between the output SNR and input Carrier-to-Noise Ratio (CNR). However, the useful

operational range of all FM demodulators is restricted by the fact that this linear relationship, or transfer characteristics, becomes nonlinear below a certain value of the input CNR which is called the point of threshold for the demodulator as depicted in the Figure 8. for a typical demodulator [123, 124, 125].

- As it is difficult to specify the exact value of the input CNR that segregates the linear and nonlinear regions of the threshold curve, a reasonable principle for the determination of the threshold point must be defined. One of the most acceptable and popular definition of the FM threshold is based on the graphical determination of the specific input CNR value for which the corresponding output SNR occurs exactly 1 dB below an extension of the linear part of the linear region curve as depicted in Figure 8. [123, 125, 126].
- FM extension is one of the most important measurement tools for the FM demodulator. Therefore the research is after building an FM demodulator that will extend the FM threshold for a purpose of improving the communication system performance especially for remote applications such as satellites where an improvement of 1 dB matters [126, 127]. Threshold extension can be obtained in most FM systems by implementing DPLLs. Therefore, in this section different improvement architectures of the TDTL were tested for the FM threshold extension. The FM extension of a FM frequency is measured up to an input CNR of 30 dB as shown in Figure 8. for a modulation index of β=10. This figure shows that the threshold point of the conventional TDTL is 10dB where this threshold is extended to 8dB and 7 dB using both the TDTL-LPD and NDTL architecture respectively. A failure is shown for the CPD-DPLL when (X=1) and TDTL architectures which show a decrease of the threshold extension to 12 dB and 13 dB respectively.

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- Figure 8. Graphical determination of the FM threshold for a typical

  FM demodulator.

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- Figure 8. FM threshold extension for different TDTL improved architectures.

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- The threshold extension performance can be also tested for the 8-PSK CEOFDM using the setup shown in Figure 8. for β=10 with communication channel affected by 10% Doppler. The CEOFDM extension is measured also up to an input CNR of 30dB as shown in Figure 8.. This figure shows that the threshold point of the conventional TDTL is 10dB where this threshold is extended to 8 dB and 7dB using both the TDTL-LPD and NDTL architecture respectively. A failure is shown for the CPD-DPLL when (X=1) and TDTL architectures which shows a decrease of the threshold extension to 11.5 dB and 12.5 dB respectively.

- Figure 8. CEOFDM threshold extension for different TDTL improved
architectures.

FM Demodulation with Improved THD

- Due to the fact that FM signal varies rapidly, particularly for large frequency deviation, there is a challenge in the demodulation process especially in extracting a harmonic-free distortion signal. This section highlights the FM reception with the evaluation of the total harmonic distortion (THD) for TDTL with acquisition aided circuits, DPD-TDTL architectures, described in Chapter 4, in comparison with the original TDTL.
- The FM tests are divided into two; in the first test, the systems were tested with a large frequency deviation and the in the second test with a small frequency deviation and both with different modulation indices β. To clearly illustrate the performance, the THD was measured for the demodulated baseband signal produced by the systems. The results illustrate that Scheme 1 DPD-TDTL surpasses other systems while both TDTL and TDTL with feedback (FB) aided circuit has the worse THD.
- The THD measurements are shown in Figure 8.. These results demonstrate that as the modulation index β increases the THD decreases and Scheme 2 DPD-TDTL system is always better compared with other systems which can provide a reduction of the THD by 12% for large frequency deviation and 4% for the small frequency deviation. The second best architecture is the TDTL with Feedforward (FF) aided-circuit which shows 9% for large frequency deviation and 2.5% for the small frequency deviation. Scheme 1 DPD-TDTL shows a THD of 2% for large frequency deviation and 1.5% for the small frequency deviation. Finally both original TDTL and TDTL with FB aided-circuit have the same performance by providing 24% for large frequency deviation and 5.9% for the small frequency deviation.
- (a)
- (b)
- Figure 8. THD of (a) Large and (b) Small frequency deviation.

Doppler Effect Improvement

- In a mobile communication environment, the input signal experiences Doppler effect that results in loss of lock in DPLL systems which will degrade the overall communication system performance. In the following section performance test results

will be highlighted for the tanlock-based architectures that have Doppler effect improvement.

- In this simulation performance test, the channel is modelled as a Rayleigh fading channel with different Doppler shifts. Rayleigh fading is a statistical model used to provide an effect in a propagation environment on mobile communication channels, which vary randomly according to a Rayleigh distribution [128, 129].
- The test starts with a Doppler frequency effect on the incoming frequency, as shown in Figure 8., and the result is presented as a pdf of how often the phase error produced by the loop's PD stays in the steady state. Both Figure 8. and Figure 8. show the effect of the Rayleigh channel with a step frequency of 0.2V on original TDTL, both FF and FB aided circuits and AS-TDTL architectures for first- and second-order loops. Figure 8. shows the effect of a 10% Doppler shift on the first-order conventional TDTL loop compared with TDTL equipped with both FF and FB aided circuits while Figure 8. shows the effect of a 10 % Doppler shift on the second-order conventional TDTL compared with the AS-TDTL architecture. From Figure 8., it is shown that the performance strength of both aided circuit compared with the conventional loop with a best performance appears in the loop equip with FF aided circuit. Figure 8. shows a very successful achievement appears by using the AS-TDTL architecture compared with all architecture due to fact of using the RLS algorithm that are design for such applications to continuously adapt the loop filter coefficients.
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- Figure 8. Incoming signal affected by Doppler shift.
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- Figure 8. Phase error steady state pdf of a 10 percent Doppler shift for
  first-order loop for an input frequency step of 0.2 V, K_1 =1 and ψ=π/2 (rad).
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-
-
- Figure 8. Phase error steady state pdf of a 10 percent Doppler shift for
  second-order loop for an input frequency step of 0.2 V, r=1.2, K_1 =1 and
  ψ=π/2 (rad).

Conclusions

- There are different applications of digital phase-locked loops (DPLL) which has grown to span a wide spectrum of systems including various communications, control, signal processing systems, clock extraction and generation, signal demodulation and frequency modulation threshold extension which can be tackled. A selection different application of the tanlock-based

architectures was presented in this chapter for assessing the validity of the architectures designed in this work. These applications include frequency shift keying (FSK) demodulation, frequency modulation (FM) threshold extension, FM demodulation with improved total harmonic distortion (THD), and Doppler effect improvement. It is shown that the performance of the improved TDTL architectures outperformed the conventional TDTL.

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IMPLEMENTATIONS

Introduction

- This chapter discusses the implementation of some of the TDTL architectures developed in this work, on an FPGA (field programmable gate array) based system. The primary objective of the implementations is to prove that the concepts involved in the architectures are correct and realizable. Therefore, the optimization of the FPGA resources used as well as alternative form of implementations, such as an application specific integrated circuit (ASIC) are considered outside the scope of the research work in this thesis. The FPGA was preferred as the targeted technology due to the flexibility of reconfiguring it and the ability to provide a fast prototyping system [130, 131, 132, 133, 134, 135, 136]. Xtreme DSP development system from Xilinix/MATLAB-Simulink was used for the synthesis process [137, 138].
- The synthesis and subsequent implementation process required the conversion of TDTL blocks to hardware realizable circuitry. This chapter provides a general idea of the process of converting the TDTL MATLAB/Simulink models to FPGA implementation and the real-time results that were obtained. The FPGA implementation of the enhanced TDTL demonstrated its effectiveness in a real-time performance.
- To compile the TDTL blocks into a hardware description language (HDL) script, an initialization of the FPGA implementations process of the design requires a translation of the systems blocks, using MATLAB/Simulink, into hardware-mappable blocks that can be simulated on bit and cycle true basis.
- Xilinx System Generator includes the necessary blocks, which were used to modify the TDTL architectures into the reconfigurable models.
- For FPGA implementation as shown in Figure 9., the sample-and-hold can be substituted by a latch while the arctan PD block can be designed using CORDIC
  (COordinate Rotation DIgital Computer) algorithm. The latch will execute the same conceptual function as that of the sample-and-hold block; nevertheless it will have both of its ports (i.e. input and enable ports) operating in the digital mode. The function of the arctan is implemented using the CORDIC algorithm, which can translate trigonometric functions into digital circuits composed of address ,addition, subtractions and shift registers [137, 139, 140, 141]. The DAC (digital to analogue converter) block as in [11, 52] is used to propagate the phase error to the outside world, in order to study the performance of the loop.
- In the following subsections, the performance of several tanlock-based architectures is discussed. The additional required Virtex

FPGA modules resources are highlighted and the real transient response of the architectures is studied.

- **TDTL**

- The following subsections present the real-time results that were achieved following the FPGA conversion and implementation of the first- and second-order TDTL which has the main reconfigurable structure as shown in Figure 9..
•
- Figure 9. Structure of the Reconfigurable TDTL.

- First-order TDTL

- The original first-order TDTL is designed by multiplying the output of the PD with a loop filter coefficient G1 that is equal to $12\pi=0.1592$ as a result of selecting the loop gain K1 to be unity. In order to induce a nominal phase shift of $\pi 2$ in the input signal, the time delay unit should be equal to quarter the period of the DCO free running frequency, namely 0.65 microseconds. Since the smallest possible delay is equal to the period of the system clock (1/105 MHz), the number of required delay stages is the ratio between the time delay and the system period, which is approximately equal to 68 in this case. The implementation of the TDTL consumed a total of 54,751 gates out of the total capacity of the Virtex-4 [11] which is around 4 million system gates.
- The reconfigurable model is tested using a frequency step to investigate the behaviour of the phase error. The test starts with an initial input frequency of 350 kHz, and a step increase caused the input frequency to rise to 400 kHz as shown in the Figure 9. . As Figure 9. shows, the TDTL follows the change in frequency and settles rapidly. The presence of ripples, which may seem to contradict the theoretical simulations, is not an indication that the loop is out of lock. This is attributed to several reasons, such as the quantization noise, truncation and calculation of errors and the limited frequency resolution of the DCO [11, 101].
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- Figure 9. Real-time transient response of the first-order TDTL for a binary
FSK frequency steps from 350 kHz to 400 kHz.

- Second-order TDTL

- The original second-order TDTL has the same implementation structure except that the loop filter is implemented as a proportional accumulative filter as described in Chapter 3 and 5 with a loop gain of unity nnd with G1 that is equal to $12\pi=0.1592$ and G2 .is equal to $120\pi=0.01592$. The FPGA reconfigurable

model is tested using a frequency step function as depicted in Figure 9.. Due to the accumulator in the digital filter, it is expected that the truncation and calculation errors are also going to accumulate at each clock cycle, causing the performance to be very sensitive to frequency changes, and in most cases oscillatory [11, 101].

- Figure 9. Real-time transient response of the second-order TDTL for a
binary FSK frequency steps from 350 kHz to 400 kHz.

WFA-TDTL Architecture

- The TDTL-WFA architecture has the same implementation structure as that of the second-order TDTL except that the DCO has to produce double the free running frequency of the original TDTL which helps the accumulative process of the proportional accumulative loop filter to reach the required steady state more rapidly. A frequency divider is required to reduce the DCO frequency for the sampling process of the incoming signal as depicted Figure 9.. The test starts with an initial input frequency of 350 kHz, and a step increase causes the input frequency to rise to 400 kHz as shown in the Figure 9.. As Figure 9. shows, the WFA-TDTL follows the change in frequency and settles faster, by three folds, compared with the original TDTL as in Figure 9..
- Figure 9. Structure of the Reconfigurable TDTL-WFA.
- Figure 9. Real-time transient response of the WFA-TDTL for a binary FSK
frequency steps from 350 kHz to 400 kHz.

NDTL Architectures

- Both first- and second-order no-delay (NDTL) architectures have the same implementation structure of the first- and second-order TDTL as shown in Figure 9.. By comparing the NDTL and the original TDTL it is possible to see that the modified DCO of the NDTL only requires two additional flip-flops which is a very small cost in terms of the FPGA gate count. At the same time, the NDTL does not require the delay block which may need to be a true analogue block therefore can’t be digitally integrated. Optimized implementation of the NDTL, as well as other TDTL architectures, in a practical system will depend on the overall system specifications and the target technology. As in the previous cases

the performance test is used here with an initial input frequency of 350 kHz and a sudden rise to 400 kHz. The real phase error of both first- and second-order NDTL are shown in the Figure 9. and Figure 9. respectively. Figure 9. shows that the NDTL has similar performance compared with the first-order TDTL. However, Figure 9. shows a an improvement by three folds of the NDTL performance compared with the second-order TDTL due to the doubling of the DCO free running frequency.

- (a)
- (b)

- Figure 9. Structure of the reconfigurable NDTL (a) first-order (b) second-order.
- Figure 9. Real-time transient response of the first-order NDTL for a binary FSK frequency steps from 350 kHz to 400 kHz.
- Figure 9. Real-time transient response of the second-order NDTL for a binary FSK frequency steps from 350 kHz to 400 kHz.

ATDTL-ZPE Architecture

- The Adaptive TDTL with Zero Phase Error (ATDTL-ZPE) architecture has similar implementation structure of the first-order TDTL with an additional FE block as discussed in Chapter 5. The additional block used for frequency estimation was implemented using the central-difference differentiator, gain block and envelope detector. The differentiator is a tapped-delay line finite impulse response filter (FIR), followed by a simple gain and finally a low pass filter that acts as an envelope detector [83] as shown in Figure 9.. The performance of the proposed system implementation has been tested by injecting an FSK signal that is changing from 350 kHz to 400 kHz. Figure 9. shows successful demodulation of the FSK signal with better performance, by folds, compared with the second-order TDTL. This architecture is compared with the second-order due to its characteristics in achieving zero phase error.

- Figure 9. Frequency estimator and envelop detector in FPGA.

- Figure 9. Real-time transient response of the ATDTL-ZPE for a binary
  FSK frequency steps from 350 kHz to 400 kHz.

TDTL with Initialization Architecture

- TDTL with initialization architecture has a similar implementation structure of the second-order TDTL with an additional FE block, as discussed in Chapter 5 and shown in Figure 9.. The performance of the proposed architecture implementation compared with original TDTL has been tested by injecting it with FSK signal that changes from 330 to 550 kHz. With these sudden changes that approach the edge of the locking range, the responses of both systems are shown in Figure 9.. It can be clearly seen that the proposed system outperformed the original second-order TDTL.
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- Figure 9. Real-time transient response of the TDTL with initialization (bottom) compared with original TDTL (top) for a binary FSK frequency steps from
  330 kHz to 550 kHz.

CPD-DPLL Architectures

- Both first- and second-order Composite Phase Detector (CPD-DPLL) architectures do not require a time-delay block as shown in Figure 9.. They only use one channel and an adaptive controller block. A possible realization of the adaptive controller can be obtained by using an envelope detector, frequency estimator, a FSM and a lockup table which has similar blocks to those shown in Figure 9.. Therefore, by customizing the requirements to cope with changes in the input signal amplitude, the adaptive controller will provide a constant value to match the requirement. The performance of the proposed system implementation was tested by injecting an FSK signal that changes from 350 kHz to 400 kHz. Both Figure 9. and Figure 9. show successful demodulation of the FSK signal using the FPGA implementation of the CDP-DPLL. Figure 9. show that the second-order CPD-DPLL has a good performance compared of original second-order TDTL in term of a response which is free from glitches.
  -
  - (a)
  -
  - (b)
- Figure 9. Structure of the reconfigurable CPD-DPLL (a) first-order (b) second-order.
  -

- Figure 9. Real-time transient response of the first-order CPD-DPLL for a binary FSK frequency steps from 350 kHz to 400 kHz.
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- Figure 9. Real-time transient response of the second-order CPD-DPLL for
  a binary FSK frequency steps from 350 kHz to 400 kHz.

○ DPD-TDTL Architecture

- The implementation of the Dual Phase Detector TDTL (DPD-TDTL) architecture includes an additional arctan PD, an adder and two gain factors compared to that of the original first-order TDTL as shown in Figure 9. and discussed in Chapter 4. The performance of the DPD-TDTL implementation compared with the original first-order TDTL was also studied by injecting FSK signal that changes in frequency from 350 to 440 kHz as shown in Figure 9..
-
-
- Figure 9. Structure of the Reconfigurable DPD-DPLL.
- A THD of 80% with a signal-to-noise ratio of 10 dB were used to test the performance of two different schemes of the DPD-TDTL in comparison with original TDTL as discussed in Chapter 4. In Figure 9.b, Scheme 1 has better noise performance compared with the original TDTL whose response is in Figure 9.a, but Scheme 2 results in the best performance as shown in Figure 9.c. In terms of acquisition performance, Figure 9.c is the worst. These results show an obvious agreement between the practical results and simulations.
-
- (a)
-
- (b)
-
- (c)
- Figure 9. FSK response of the proposed system and the original TDTL
  for a frequency step from 350 to 440 kHz with THD of 80% and SNR=10dB (a) TDTL (b) Scheme 1 and (c) Scheme 2.

○ Conclusions

- This chapter presented an FPGA implementation of some of the TDTL architectures, which were developed in this work and compared their performance to that of the original TDTL. The FPGA implementations are based on the Xtreme DSP system, which enabled real-time results to be illustrated. Comparison of the real-time results with those obtained from MATLAB/Simulink simulations indicates that they are in good agreement. This

demonstrated the validity of the proposed system architectures through physical implementations. The performance of the various system architectural implementations can be improved through FPGA resource utilization optimization as well as targeting other more refined technologies such as ASIC.

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CONCLUSIONS AND FUTURE WORK

Conclusions

- In pursuit of achieving the objectives of the research presented in this thesis, the research work concentrated on designing new architectures to enhance the performance of a particular class of DPLLs that uses an arctan phase detector; the TDTL. The loop parameters, which were used to assess the performance enhancements produced by the proposed architectures, are: linearity, acquisition time, locking range, and noise.
- A major challenge to improve the aforementioned parameters is the fact that they conflict with one another. For example, increasing the locking range degrades the noise performance. Therefore, the challenge was to devise techniques to improve some of the loop performance parameters while keeping the other parameters either unchanged or keep the degradation to a minimum. Following identification of the limitations of both the first- and second-order TDTLs, the research focused on the development of new tanlock-based architectures that can be re-configured so that their performance parameters can be optimized to meet a given set of application requirements. In this work, two approaches were used to improve the performance parameters: the first involved using auxiliary circuits to aid the original TDTL architecture, whilst the other approach involved modifying the actual loop architecture.
- Nonlinearity of the first-order TDTLs was overcome by introducing the TDTL with linearized phase detector (TDTL-LPD) and the TDTL with pre-distortion architectures. These modified architectures resulted in improving the locking range and acquisition time. Compared to the original TDTL, the acquisition time of the modified architectures was improved by nearly 50%.
- The feedback with rounding and the adaptive TDTL structures were used to improve the acquisition speed. The limitation in the acquisition speed of second-order TDTL was also overcome by introducing the TDTL with wide locking range and fast acquisition TDTL-WFA with an improvement of fourfold.
- Architectures with different schemes were proposed for noise performance enhancement; the DPD-TDTL scheme1 and scheme2. These architectures provided an improvement in the pdf scale by at least a factor of two compared to the original TDTL. The TDTL with both feedback and feedforward aided-circuits were proposed. These were mainly used to help bring the system back into the locking range and stable mode following an oscillatory state. This effectively results in widening the locking range. The ATDTL-ZPE architecture, used for wide locking range and zero phase error for the first-order TDTL, is also effective for noise performance due to fact that the loop is only used to

provide phase locking, which produces better noise performance compared to the original TDTL giving an improvement of fifty per cent.

- The adaptive second-order TDTL (AS-TDTL) architecture, which is based on RLS algorithm that is used to generate the coefficients of the TDTL loop filter. The advantage of this architecture compared to other architectures lies in improving the loop performance related to the Doppler shift effect.
- The nonlinearity associated with the second-order TDTLs was overcome by introducing the TDTL with linearized phase detector, TDTL with Pre-distortion TDTL, and the TDTL with wide locking range and fast acquisition (TDTL-WFA) architectures. These architectures linearized the system and improved the acquisition time by fourfold.
- In addition, a wide frequency locking range was achieved by introducing the adaptive TDTL with zero phase error ATDTL-ZPE that enables the system to quickly shift the locking range to the specific frequency and hence widening its frequency locking range.
- The no-delay tanlock-based (NDTL) architecture enhances the linearity of the phase detector characteristics and consequently the acquisition and the noise performances. The main drawbacks of NDTL architecture are the need for doubling the DCO free running frequency, which has an impact on the complexity of the DCO and the possibility of false locking due to locking to harmonics.
- The new non-uniform DPLL that uses a composite phase detector (CPD) and an adaptive controller overcome the two main limitations of nonlinearity and sensitivity to variations in input signal amplitude exhibited by the conventional ZC-DPLL.
- The implementations of some of the tanlock-based architectures on an FPGA based system to get real-time results were presented. Comparison of the FPGA based real-time results with those obtained from MATLAB/Simulink simulations indicates that they are broadly in agreement. Depending on the application, the designer may opt for an application specific integrated circuit (ASIC) implementation to achieve an optimal overall system performance.

○ Recommendations for Future Work

- Further improvement in the performance of the proposed architectures is likely to be achieved using Application Specific Integrated Circuit (ASIC) implementation. It is also recommended to explore the performance of the proposed architectures by conducting practical experiments in physical systems such as communications, signal processing, and control systems. This will enable the evaluation of the performance of the proposed architectures in real and practical environments.

- An interesting area for further exploration is the design of a tanlock-based delay-locked loop (DLL) and comparison of its performance with those of DLLs reported in the literature. DLL is a negative feedback control system similar to DPLL, the main difference being the absence of an internal DCO, which is replaced by a delay line. DLL is mainly used to change the phase of the clock signal for clock recovery applications. Therefore, it has some limited application but it has less circuitry compared with PLLs.
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