Transport simulations of ZnO nanowires and semiconductor devices in the presence of scanning probes.

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Transport simulations of ZnO nanowires and semiconductor devices in the presence of scanning probes

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Summary

A simulation methodology to model contact and non-contact microscopy measurements has been developed within a 3-D finite element commercial device simulator by Silvaco. The tip-sample system is modelled self-consistently including tip-induced band bending and realistic tip shapes. When modelling scanning tunnelling microscopy, the resulting spectra from III–V semiconductors show good agreement with experimental results and a model based on the Bardeen tunnelling approach. We have found that the image force induced barrier lowering increases the tunnelling current by three orders of magnitude when tunnelling in to the sample valence band, and by six orders of magnitude when tunnelling in to the sample conduction band. We have shown that other models which use a single weighting factor to account for image force in the conduction and valence bands are likely to underestimate the valence band current by three orders of magnitude.

The role of probe shank oxide formed at the tip in air has been examined by carrying out contact and non-contact current-voltage simulations of GaAs when the probe oxide has been controllably reduced. For both contact and non-contact simulations, the contact resistance change due to oxide is dependent on polarity and as confirmed experimentally.

An electrostatic tip apex interaction with an In_2O_3 thin film transistor under operation is studied using a combination of experimental electrostatic force microscopy measurements and simulations. An error in the surface potential near the drain electrode is observed in simulations due to the tip induced band bending.

Two point probe measurements on ZnO nanowires and 3-D transport simulations reveal the change in the electrical behaviour of nanoscale contacts from Schottky-like to Ohmic-like when the size of Au catalyst particles is changed at the ends of free-standing ZnO nanowires in relation to the nanowire cross-section. In addition, a geometry dependent current crowding effect was analysed in the combination with self-heating calculations.

Finally, we have investigated carrier confinement at the ZnO/GaZnO interface due to band offset and polarization effects. We have found that this material system is a good candidate for polarization heterostructure field effect transistors.

Definitions or Acronyms

SPM	-	scanning probe microscopy
STM	-	scanning tunnelling microscopy
STS	-	scanning tunnelling spectroscopy
EFM	-	electronic force microscopy
4PP	-	four point probe
TEM	-	transmission electron microscopy
KPFM	-	Kelvin probe force microscopy
HFET	-	heterostructure field effect transistor
FET	-	field effect transistor
TFT	-	thin film transistor
HEMT	-	high electron mobility transistor
2DEG	-	two-dimensional electron gas
WKB	-	Wentzel-Kramers-Brillouin
DFT	-	density functional theory
TIBB	-	tip induced band bending
BL	-	barrier lowering
UST	-	universal Schottky tunnelling
GZO	-	GaZnO

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Chapter 1 Theory

Scanning probe microscopy (SPM) is a technique that can be used to make surface electronic, morphological, optical, chemical and magnetic measurements down to the atomic scale [1]. All scanning probe methods use a conducting probe to scan different surfaces and obtain with atomic resolution physical properties of these surfaces. The basic principles of some of the SPM methods used in this thesis like scanning tunnelling microscopy (STM), scanning tunnelling spectroscopy (STS), four point probe microscopy (4PP) and electrostatic force microscopy (EFM) are discussed in Chapter 1.1.

SPM allows characterisation of samples and devices with a nanoscale spatial resolution, including devices under operation [2]–[5]. In this thesis semiconductor devices in the presence of scanning probe are of interest and detailed explanation of the device principles for ZnO/MgZnO heterostructure field effect transistor (HFET) and In_2O_3 thin film transistor (TFT) are given in Chapter 1.2.

The main limitation of the method is that with all SPM techniques the probe can interact electrostatically and physically with the sample, changing the measured properties of the device under test [6]. Modelling the electrostatic probe interaction can be used to quantify the measurement error, to match experimental results to device properties, or potentially to remove the effects of probe interaction [7]–[11]. In this thesis, modelling of the semiconductor plain surfaces, heterostructures and devices is performed using the simulation tool *ATLAS* by Silvaco. In Chapter 1.3, an overview of the Silvaco toolbox is presented.

1.1 Scanning probe methods

1.1.1 Scanning tunnelling microscopy

The idea of scanning tunnelling microscopy (STM) was first introduced by G. Binnig, H. Rohrer, Ch. Gerber, and E. Weibel in 1981 by showing a successful tunnelling experiment with an externally and reproducibly adjustable vacuum gap which demonstrated the exponential dependence of the tunnelling current on the width of the gap [12], [13].

When a probe is brought to the sample on small distance z (smaller then few nanometres) and voltage V is applied on a probe, the electrons will tunnel through the vacuum barrier as seen in Figure 1.1.1. The tunnelling current I is then exponentially dependant on the barrier width (tip-sample separation):

$$I \propto Ve^{-kz},\ k = \sqrt{[\phi_t + \phi_s - eV]^{m_0}/\hbar^2} \tag{1.1}$$

where m_o is an effective mass, ϕ_t and ϕ_s are tip and sample Fermi levels.

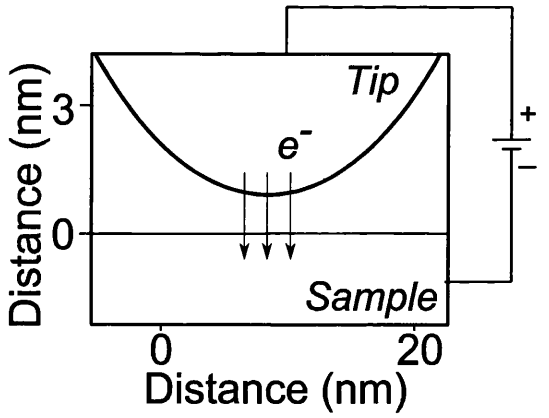

Figure 1.1.1. Schematic representation of the scanning tunnelling microscopy method when voltage is applied on a tip, electrons will tunnel through the vacuum barrier between the tip and sample.

There are two methods to obtain surface topography of the sample with atomic resolution: constant height mode measurements and constant current mode measurements. In constant current mode the current between tip and sample is kept constant while tip is mapping sample in *x-y* directions. Depending on a change of the surface topography a change in the tip lift height is recorded. In constant height mode a change in topography is obtained from the change in the recorded values of current. Because current is exponentially dependant on *z*, STM gives a good depth resolution.

The resulting topography image from STM is not only influenced by the sample's actual topography, but also it is influenced by the electronic structure of the sample surface because surface charge density is probed by this method [14]. That is why another application of STM is scanning tunnelling spectroscopy (STS) which directly measures surface density of states of the sample.

1.1.2 Scanning tunnelling spectroscopy

A detailed spectrum of the material surface can be obtained by STS. The spectrum contains information about conduction and valence band edges and various features of the surface states. The bulk bandgap can be obtained for the material like GaAs because dangling-bond states on the surface do not appear in the gap [17]. As well as in STM, the main limitation of this method is a systematic measurement error due to tip-induced band bending which can be small for highly doped samples [15], [16].

Like in STM, there are two STS measurement modes to obtain the spectra: using variable tip-sample separation and using constant tip-sample separation [18], [19]. In principle, identical results should be achieved using both methods. The variable separation method can be more preferable because with this method a conductance at the low voltages can be obtained with better accuracy [17]. As the voltage reduces, the separation is reduced in order to keep the current above the noise floor and maintain sufficient signal to noise ratio to measure within the band gap. Thus variable separation method will give a better quality data due to the better signal-to noise ratio than constant separation method.

Spectra analysis is performed in two steps. First the tip is held above the sample surface and current *I-V* is measured for the range of the applied biases. Measured data then needs to be transformed to the constant tip-sample separation using Eq. (1.1) if the variable separation mode was used. In the experiment values of k can be obtained by measuring current dependence on the separation and are estimated to be in the range 0.7-1.1 $Å^{-1}$ for III-V semiconductors [17]. The conductance *dI/dV* is then defined as a partial derivative of the current with respect to voltage for a fixed value of tip-sample separation. After measurement of current I and conductance *dI/dV*, the normalised differential conductance to the total conductance *(dI/dV)/(I/V)* is analysed on the linear scale to reveal features of the spectra.

1.1.3 Four point probe microscopy

The four point probe method of the scanning probe microscopy is generally used for measurements of surface conductivity (resistivity) and sheet resistance [20]–[22]. In Figure 1.1.2(a) current I is flowing through two current probes 1 and 4 and voltage drop V across the sample during the current flow is measured using two voltage probes 2 and 3. The first formulism for the collinear four point probe with an equal probe spacing s was introduced by Valdes [20] in 1954 and the equation for the resistivity ρ when probes are placed on a semi-infinite volume of semiconductor material is the following:

$$\rho = 2\pi s \cdot V/I \tag{1.2}$$

To obtain results for other probe geometrical configurations and spacing between probes correction factors are used [23]. The most common probe setup is the collinear mode as shown in Figure 1.1.2 [24]–[26] where probe 1 and 4 are current sensing probes and probe 2 and 3 are voltage sensing probes.

In the four point probe system shown in Figure 1.1.2, each probe has a probe resistance R_p, a contact resistance R_{cp} at the probe-sample contact, a spreading resistance R_{sp} due to the current flowing from the tip through sample, and semiconductor itself has a sheet resistance R_s which needs to be measured. Ideally, contact resistance, probe (lead) resistance, and

spreading resistance (R_{cp}, R_p, and R_{sp}) should not contribute to the measurement of the sheet resistance R_s measurements.

In the collinear four point probe (4PP) method, the inner two probes will drive negligible current due to high impedance of the voltmeter used in the measurements. This will result in a very low current through the inner voltage probes 2 and 3 making $I_2 \ll I_1$ and $I_3 \ll I_4$. That is why, unlike in a two point probe [22], the contact type (Schottky or Ohmic) of the voltage probes in 4PP does not play a significant role [20]. Due to negligible current I_2 and I_3, the voltage V measured by the voltmeter will correspond to the potential drop across sample V_s making: $V = V_s$. Also, when current on the voltage probes is negligible, current through the probes 1 and 4 becomes: $I_1 = I_s = I_4$ as seen in Figure 1.1.2(b). Then measured resistance in the four point probe would be:

$$R_s = {}^{V}/_{I_1} = {}^{V_s}/_{I_s} \tag{1.3}$$

Despite the wide use of 4PP methods, there exists disagreement in the literature about whether the contact type of the four probes is important. Many authors claim that the contact type of current probes (probes 1 and 4 in Figure 1.1.2(a)) does not influence 4PP measurements too, irrespective of whether the probe contacts are Ohmic or Schottky-type [25]–[28]. Some authors cite Smits work [23] from 1958 to confirm the assumption even though this work does not include a study of the probe contact type.

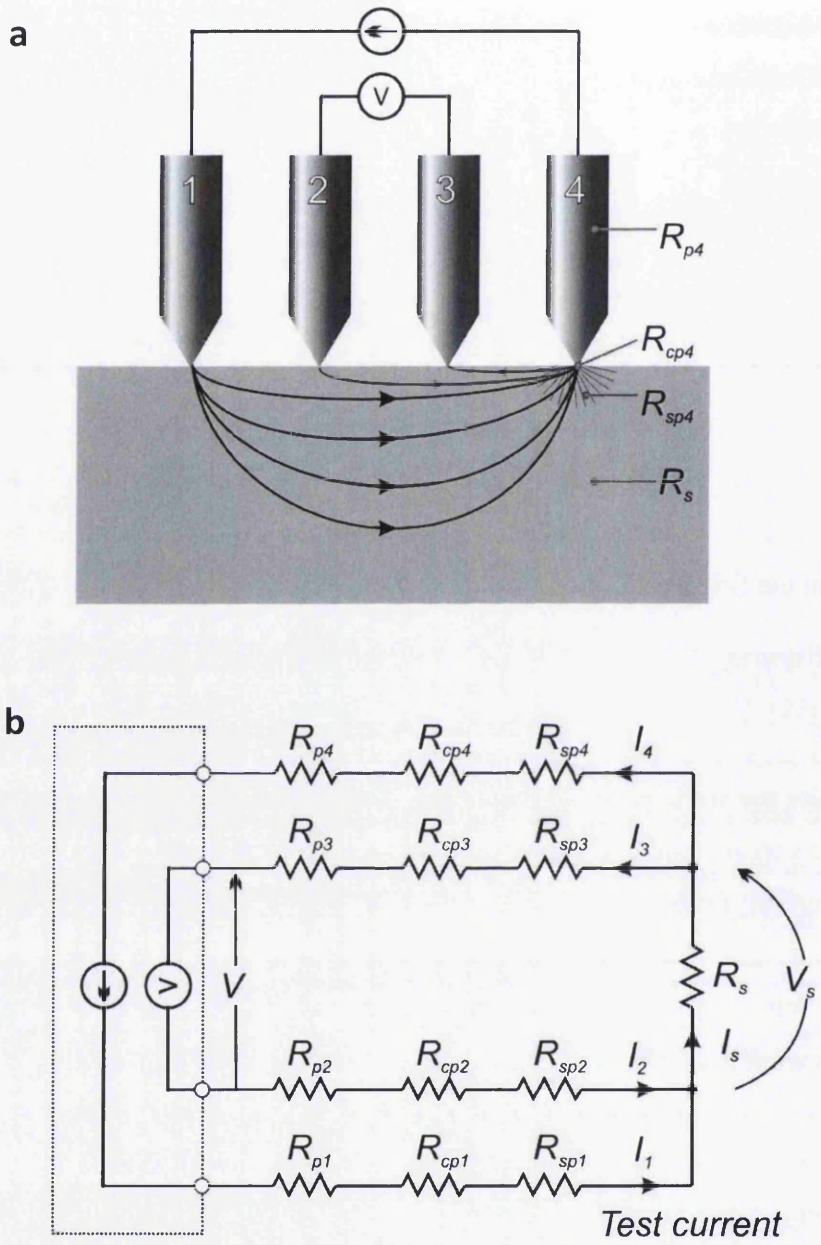

Figure 1.1.2. Four point probe measurements of semiconductor resistance. (a) The outer two probes 1 and 4 are used for current sensing and inner two probes 2 and 3 are used for voltage sensing. Each probe has a probe resistance R_p, at the probe-sample contact there is a contact resistance R_{cp}, spreading resistance R_{sp}, and semiconductor itself has a sheet resistance R_s. (b) Current from the voltage probes 2 and 3 is negligible when a voltmeter has high impedance: $I_2 << I_1$, $I_3 << I_4$, $I_1 = I_s = I_4$. .Then voltage sensed by voltmeter (V) will be equal to voltage drop across the sample: $V=V_s$. The measured resistance becomes: $R_s = {}^{V}/_{I_1} = {}^{V_s}/_{I_s}$.

The assumption of rectifying contacts used in 4PP was introduces earlier by Valdes [20] in 1954 to study the surface resistivity of germanium. Valdes derived the formulism to improve the existing measurements methods, the new four point probe method was claimed to account for the rectifying nature of the germanium semiconductor when a contact with metal is formed [20]. Excess concentrations of minority carriers were known to affect the potential of contacts and it was claimed to modulate the resistance of the material [20]. Nowadays it is widely accepted that resistance (resistivity) is the intrinsic property of the material independent from a measurement method [29] and it cannot be modulated by the properties of the contact, instead the contact resistance can introduce an error in measurements of semiconductor resistivity. The formulism did not account for the separate impact of contact resistance and material resistivity, and a semiconductor sample was considered to be a semi-infinite volume of uniform resistivity material [20].

Valdes in Ref. [20] is referencing work by Bardeen [30] which demonstrates non-linear current-voltage behaviour of the germanium point contacts. Nowadays it is known that in Schottky contacts there are five basic transport processes (Figure 1.1.3) [29], [31]–[33]: (1) emission of electrons over the potential barrier, (2) diffusion of electrons, (3) quantum-mechanical tunnelling through the barrier (important for heavily doped semiconductors), (4) recombination in the space-charge region, and (5) holes injected from the metal into the

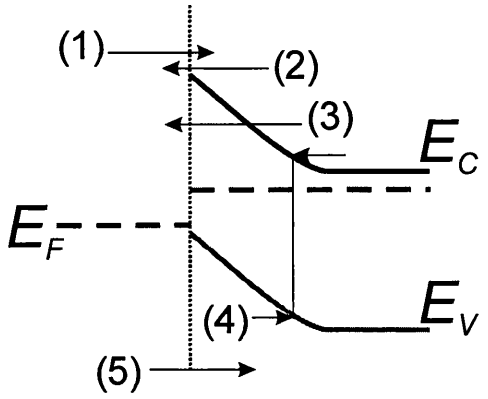

Figure 1.1.3 Schematic band diagram showing transport processes: (1) emission of electrons over the potential barrier, (2) diffusion of electrons, (3) quantum-mechanical tunnelling, (4) recombination, and (5) holes injected from the metal.

semiconductor. Current due to each transport process is taking place at different bias range and it is non-linearly dependant on the applied bias. This means that in Schottky contacts when Schottky diode behaviour is present at the metal-semiconductor interface the current in to the electrode and out of the electrode will have significantly different magnitude. If we consider that current probes 1 and 4 in Figure 1.1.2(a) have the same material parameters and both probes are forming Schottky contact with the sample, then for the current directions indicated in Figure 1.1.2(a) the forward bias current I_1 and corresponding reverse bias current I_4 are non-equal ($I_1 \neq I_4$) and form contact resistances: $R_{cp1} << R_{cp4}$. This would violate one of the main principles of 4PP theory: current-carrying electrodes carry currents of equal magnitude but in opposite directions [20]. A rise of the contact resistance R_{cp1} or R_{cp4} will result in non-negligible current through the voltage probes I_2 and I_3, measured voltage becomes $V \neq V_s$, which then results in the measurement errors as seen in 2PP.

Experimental data demonstrated by Chandra [21] indicated that for the wide band gap semiconductor SiC 4PP measurement are not suitable, even though it is routinely used for Si and other semiconductors. One probe measurement on the SiC surface revealed the non-linear current-voltage characteristic of SiC. Extremely high contact resistances between tip and sample of the probe–SiC contacts was estimated using 4PP [21]. This was due to the high currents through voltage probes (probe 2 and 3 Figure 1.1.2(a)) in comparison to currents at the current probes (probe 1 and 4 in Figure 1.1.2(a)) making four-point probe sheet resistance measurements on SIC surface with non-linear I-V characteristic fraught [21]. These measurements demonstrate that in case of non-linear Ohmic contacts a violation of one of principles of 4PP formalism is present: the current on the voltage probes become non-negligible in comparison to the current through current probes.

It is recommended by the 4PP production companies to make one probe measurements to test the contact linear current-voltage behaviour before the measurement including testing , and successful 4PP measurements demonstrated in literature were performed with Ohmic tip-sample contacts [22], [25], [34]–[39].

Oxide coatings can have an effect on the contact type formed, and so four point probe measurements should be taken with probes that are oxide free using methods such as direct

current annealing [36,69]. Li and Ba state that the probes used for four point probe measurement need to be regularly cleaned to avoid the effect of probe surface oxidation and/or contamination, but as of 2012 they report that no work has been done to examine the effects of probe oxide [24]. With the need for Ohmic contacts established, even for 4PP, in Chapter 3.8 we investigate whether oxide coatings on local probes can modify the contact behaviour using a combination of experimental and simulation techniques. The work presented in this section and in Chapter 3.8 was included in a submitted publication.

1.1.4 Electrostatic force microscopy

Electronic force microscopy (EFM) is one of the non-contact methods of atomic force microscopy that allows measurement of long-range electrostatic forces and capacitance with a resolution around 100 nm, first introduced by Martin in 1988 [40].

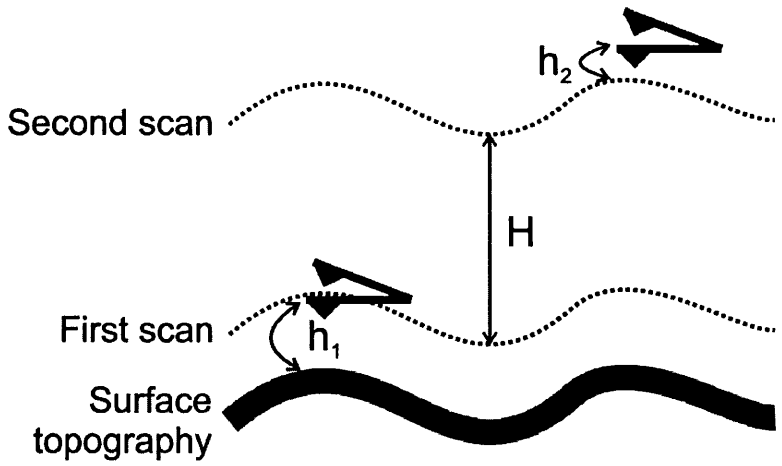

Figure 1.1.4 Schematic illustration of the electronic force microscopy double pass method. During the first scan topography of the sample is obtained in a "tapping mode" with a tip-sample separation h_1. During the second scan tip is lifted on the distance H above the sample and it is scanning with vibration the amplitude h_2. During the second scan a constant DC voltage is applied on the tip.

A double pass EFM method allows mapping the surface potential. It is performed in two stages and is shown in Figure 1.1.4. At the first scan a cantilever vibration amplitude h_1 is kept constant to obtain the morphology of the sample in a "tapping mode" [41]. To obtain the surface potential in the second scan the tip is retracted at the constant lift height H and it follows the topography obtained in the first scan with the amplitude h_2, where $h_2 < h_1$. During the second scan a constant voltage is applied to the tip and the electrostatic forces due to the tip-sample potential offset are measured [42], [43].

The frequency shift $\Delta f(\omega)$ in the cantilever vibration will be proportion to the gradient of the force:

$$\Delta f(\omega) \propto grad_{DC} F = -\frac{1}{2}\frac{\partial^2 C}{\partial z^2}(V_{DC} - V_{CPD})V_{AC}\sin(\omega t) \qquad (1.4)$$

where the force F depends on the applied voltages V_{DC} - DC potential applied between tip and sample, V_{AS} - AC potential on the cantilever, V_{CPD} - contact potential difference between tip and sample and capacitance C [44].

For the quantitative determination of the surface potential the correct tip-sample capacitance is needed. This involves determining the tip-sample separation and the exact geometry of the tip.

One of the drawbacks of the method is a contribution of the tip cone and cantilever which introduce an error in force gradient measurements due to the averaging of the contact potential over a large area [45], [46]. Error is present during the 'height measurement' at the first scan when sample topography is obtained, which then adds an error when the potential is measured in the second scan.

1.2 Semiconductor device theory

1.2.1 ZnO/MgZnO heterostructure field effect transistor

The operation of the high electron mobility transistor (HEMT) is based on the effect of the creation of two-dimensional electron gas (2DEG), first described by Khan *et al.* [47]. When the energy states in the triangular potential well are formed, no electron can be placed below the energy level corresponding to a half-wavelength of the electron (first energy sub band) [29]. Electrons at these states cannot move in the direction of the potential well formation but can freely move in the other two directions. These electrons that can move only in two dimensions are referred to as the 2DEG. The inability of electrons to move in one of three directions will eliminate scattering mechanisms in this direction, consequently increasing the electron mobility in the 2DEG channel. This makes HEMTs important for the high-frequency and low noise applications.

ZnO has good high-field transport properties and a high melting temperature of 2248 K which makes this material suitable for high-temperature device applications [48]. Resulting $Mg_xZn_{1-x}O$ semiconductor material has a wider bandgap then ZnO, and it has a Wurtzite structure for the Mg content up to x=0.5 [50]. This suggests a carrier confinement in the $ZnO/Mg_xZn_{1-x}O$ material system (Figure 1.2.1(a)) similar to GaAs/AlGaAs and GaN/AlGaN making $ZnO/Mg_xZn_{1-x}O$ a good candidate for HEMT applications [29], [47]. Similar to the case of GaN/AlGaN, crystallographic polarity along the c-axis direction is expected in $ZnO/Mg_xZn_{1-x}O$ due to non-centrosymmetric atomic arrangement in the Wurtzite structure. The undoped ZnO/MgZnO structure will have a 2DEG formed in the ZnO channel layer due to the interplay between spontaneous and piezoelectric polarizations in the heterostructure [48].

The sheet carrier density in the ZnO channel will depend on the electron density from the native donors and of accumulated electrons due to polarization-induced interface charges which depends on the Mg content in $Mg_xZn_{1-x}O$ layer. The spontaneous polarization increases with Mg content x in $Mg_xZn_{1-x}O$ due to the deviation of the material crystal structure from ideal Wurtzite: $P_{SP} = -(0.057 + 0.066x)$ C/m^2 [50]. Polarization charges

when the electron density is larger than 10^{11} cm^{-2} can also act as an additional source of scattering leading to the degradation of the mobility [51].

In the ZnO/MgZnO structures with thin well width less than 4.6 nm and low Mg composition x< 0.2 the cancellation of the sum of spontaneous and piezoelectric polarization is present which will result in a negligible internal field effect and 2DEG will not be formed [49], [52].

The first n-channel depletion mode ZnO/$Mg_{0.3}Zn_{0.7}O$ heterostructure field effect transistor (HFET) was suggested by Koike *et al.* in 2005 [53]. A typical HFET structure is

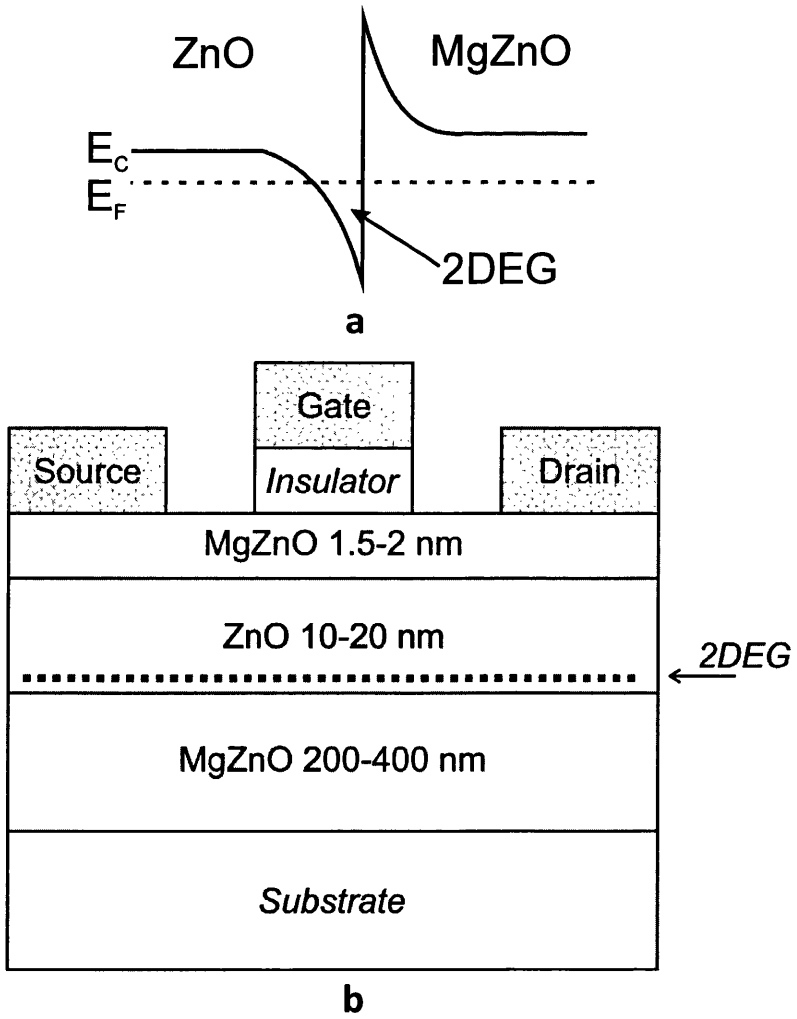

Figure 1.2.1. (a) Formation of the 2DEG at ZnO/MgZnO interface. (b) Schematic of ZnO/MgZnO HFET: an insulator layer of 50 nm can be formed using one of the following materials: MgO [53], Al2O3 [48] or HfO2 [54]–[56].

demonstrated in Figure 1.2.1(b). At the heterostructure interface band edge discontinuities were estimated to be ~0.7 eV for the conduction band and ~0.08 eV for the valence band suggesting the formation of a deep potential well for electrons and the creation of a 2DEG. The electron sheet density in a single quantum well was estimated to be $\sim 6 \cdot 10^{12}$ cm^{-2}, field-effect mobility 140 $cm^2/V \cdot s$. This very high mobility was nearly two orders of magnitude larger than in ZnO thin film transistors with polycristalline ZnO channel [53]. A maximum transconductance at V_{GS}=−4.6 V was estimated to be 0.7 mS/mm. Also the device showed light-sensitive properties, the source-drain current increase with the increase in the light power was observed.

The main problem of the first device was a leakage current through the bottom $Mg_{0.3}Zn_{0.7}O$ barrier which resulted in a low on/off ratio. To solve the problem of leakage current, Sasa *et al.* suggested a depletion mode ZnO/$Mg_{0.4}Zn_{0.6}O$ HFET structure with a thin 2 nm $Mg_{0.4}Zn_{0.6}O$ cap layer and 50 nm Al_2O_3 layer to form a gate dielectric [48]. This device showed FET operation with an effective mobility of 62 $cm^2/V \cdot s$, threshold voltage of −7.2 V and transconductance of 28 mS/mm. The estimated charge density was $2 \cdot 10^{12}$ cm^{-2}. As well as the previous HFET structure, this device showed light-sensitive behaviour which resulted in a shift of the output characteristic of −0.6 V to −0.7 V of gate bias. Due to the presence of the mobile charge in the dielectric layer an output characteristic of the device showed a hysteresis of about 2 V.

To significantly reduce hysteresis up to 0.1 V a new ZnO/$Mg_{0.3}Zn_{0.7}O$ device structure was suggested where Al_2O_3 dielectric was replaced with HfO_2 [54]. The estimated mobile charge density changed to $1.4 \cdot 10^{11}$ cm^{-2} and use of HfO_2 improved the stability and performance of the transistor.

A study of the high frequency performance of ZnO/$Mg_{0.3}Zn_{0.7}O$ HFET demonstrated a current gain cut-off frequency of 1.75 GHz and unilateral power gain of 2.45GHz demonstrating a high-speed capability of these transistors [55]. Also, radiation hardness was found to be better than in GaAs HEMTs demonstrating the good radiation-proof characteristics of new HFETS [56].

1.2.2 In_2O_3 thin film transistor

In_2O_3 is a wide bandgap material with a cubic crystal structure [57], [58]. When used in thin films it has a high transparency in the visible range (>90%), high electrical conductivity, large-area uniformity making In_2O_3 thin films important for the device application like liquid crystal displays and solar cells [59]–[61]. The excess indium atoms or oxygen vacancies serve as donors and make In_2O_3 an n-type semiconductor [60], [62]. The electron affinity was estimated from experimental data to be 3.7 eV (3.3-4.45 eV) [59], with a direct bandgap around 3.6 eV (2.93-4.0 eV) [58]–[60], [62] and an effective mass of 0.3m [58]. The electron mobility in In_2O_3 thin films was estimated to be 36-52 $cm^2/V{\cdot}s$ for n-type doping levels of $2.2{\cdot}10^{19}$-$7{\cdot}10^{19}$ cm^{-3} [59], [63] and 11-55 $cm^2/V{\cdot}s$ for n-type doping of $1.5{\cdot}10^{18}$-$7.5{\cdot}10^{18}$ cm^{-3} [60]. Additional doping of the film can increase the mobility up to ~130 $cm^2/V{\cdot}s$ [63]. It was demonstrated in the literature that conductivity of the In_2O_3 thin film is also dependant on the thickness of the film [62]. Experimental investigation of the high-quality single-crystalline thin films show accumulation of electrons on the (001) surface introducing surface band bending of ~0.4-0.5 eV resulting in the unoccupied donor surface states charge density of ~$1.3{\cdot}10^{13}$ cm^{-2} [58], [60].

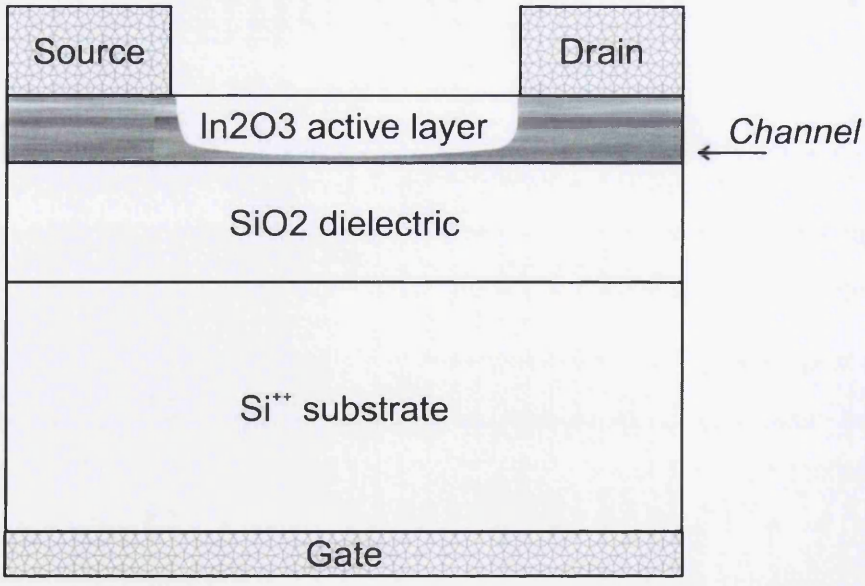

Figure 1.2.2 Typical structure of n-channel In_2O_3 TFT operating under Vg>0 and Vd>0.

In_2O_3 thin film transistor (TFT) structures were suggested for high resolution displays where it is preferable to have large on-currents to drive pixels and low off-currents for low power consumption. A typical structure of In_2O_3 TFT is demonstrated in Figure 1.2.2 [64]–[67]. In_2O_3 TFTs on SiO2/Si substrate demonstrated in the literature are typically bottom gate, normally-on n-channel transistors [68]. These devices show mobility of 0.44-23.03 $cm^2/V{\cdot}s$ and on-off ratios of $\sim 10^5$-10^6 are demonstrated [61], [68]. The increase in the mobility was related to the increase in the annealing temperature which resulted in different crystallisation of the In_2O_3 films [61]. It was also demonstrated that In_2O_3 TFTs show semiconducting behaviour for annealing temperatures only up to 300 ° [61].

In_2O_3 TFT devices show typical FET behaviour. In the on state a linear regime in the output characteristic indicates good Ohmic contact between the Al electrodes and the channel layer. The saturation regime is observed in the output characteristics indicating that the channel is depleted of free carriers. When the drain bias is further increased a decrease in the drain current is present due to the charge-trapping effects in the channel layer [68].

A good interface between the In_2O_3 channel and dielectric material is necessary to reduce scattering at the interface and enhance device performance. The maximum density of surface states at the insulator-channel was estimated to be 3.9×10^{11} cm^{-2} [68].

Typically an enhancement mode operation of FET is more preferable as no voltage needs to be applied to turn off the device. This can be achieved when amorphous In_2O_3 TFTs are used [68].

1.3 Silvaco device simulation toolbox

Physically-based simulations are becoming widely used because they can provide information which is difficult or impossible to measure. These simulations are often quicker and cheaper than performing experiments. The effective use of the physically-based device simulator is possible when all relevant physics models are incorporated in the simulator and effective numerical algorithms are used to obtain the solutions. More details on physical models and numerical algorithms will be given in Chapter 2.

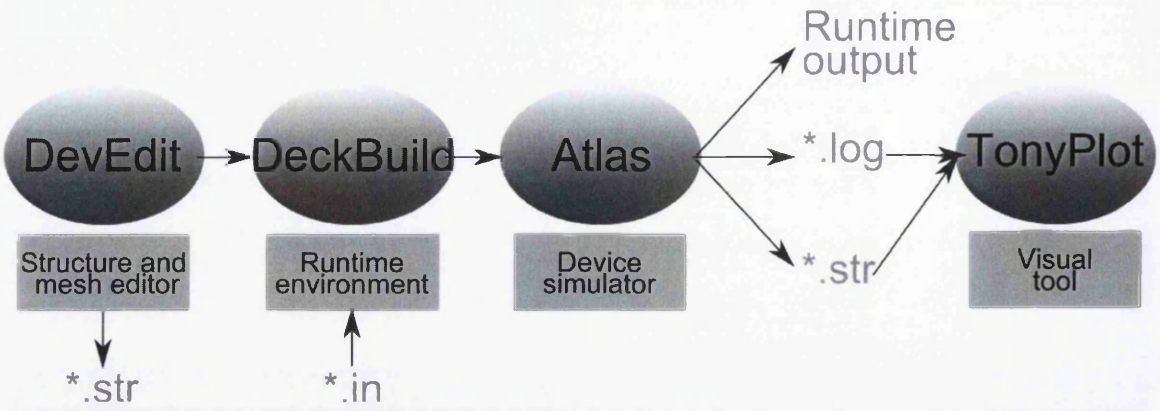

Figure 1.3.1. Simulation procedure, input and output setup using Silvaco interface tools Atlas, DeckBuild, Tonyplot and Devedit.

Silvaco software combines interface tools like Atlas, DeckBuild, Tonyplot, DevEdit for physically-based 2D and 3D simulations of the semiconductor devices (Figure 1.3.1). Atlas is a platform that combines a set of physical models for modelling electrical and thermal behaviour of semiconductor devices. When the problem is simulated in Atlas first the physical structure and mesh are defined, then the physical models and the bias conditions at which the physical models will be applied to the structure geometry are specified. The Atlas models are defined using commands and can run in the interactive run-time environment DeckBuild. The results of the run can be traced in the DeckBuild runtime output and graphically presented in Tonyplot. Tonyplot tool allows graphical visualisation of 2D and 3D structures and simulation data analysis. The Tonyplot package also provides the analytical tools for the inspection of the physical quantities calculated for the structure and allows multiple plots to be compared by overlay. The device structure and device mesh can also be defined in a structure and mesh editor called DevEdit. Structure created in DevEdit can be used in DeckBuild and Atlas physical models can be applied to simulate the structure behaviour.

The following three types of output provide information about the semiconductor structure analysis (Figure 1.3.1): runtime output gives the information about the code execution progress, possible errors and warning messages, ".log" files provide all electrode voltages and currents in the structure and ".str" provides 2D and 3D visualisation of the physical quantities on the device mesh at the selected bias point. More details about simulation setup and physical models used are given in Chapter 2.

1.4 Summary

The basic principles of some of the SPM methods used in this thesis like scanning tunnelling microscopy, scanning tunnelling spectroscopy, four point probe microscopy and electrostatic force microscopy are discussed in Chapter 1.1. STM is used to obtain surface topography of the sample with atomic resolution. The resulting topography image from STM is not only influenced by the sample's actual topography, but also it is influenced by the electronic structure of the sample surface because the surface charge density is probed by this method. STS directly measures surface density of states of the sample. An electrostatic interaction of probe with sample which results in a tip induced band bending. In Chapter 3 a simulation methodology to reproduce the STS and STM process will be shown and compared against experimental data and other models.

Collinear four point probe is used to measure nanoscale surface conductivity and employs two outer probes to pass a current through the sample while two inner high impedance sense probes measure the potential difference induced by the outer probes. The method relies on at least two current sensing of the probes forming the same barrier to the sample with low resistivity non-rectifying contacts. The presence of oxide on the shank of probes can change contact properties. Change in the conductivity due to presence of oxide on the probe will be investigated experimentally and in simulations in Chapter 3.8. Two point probe measurements of electrical properties of ZnO nanowires with metal contacts are considered in detail using simulations in Chapter 4.

Electrostatic force microscopy (EFM) is one of the non-contact methods of atomic force microscopy that allows measurement of long-range electrostatic forces and capacitance with a resolution around 100 nm. One of the drawbacks of the method is a contribution of the tip cone and cantilever which introduce an error in force gradient measurements due to the averaging of the contact potential over a large area. Error is present during the 'height measurement' at the first scan when sample topography is obtained, which then adds an error in the potential measurement during the second scan. EFM is widely used for surface potential measurements of devices in operation, for example, In_2O_3 thin film transistors.

In_2O_3 thin films are important for device applications including liquid crystal displays and solar cells. In_2O_3 TFTs on SiO2/Si substrate demonstrated in the literature are typically bottom gate, normally-on n-channel transistors. In Chapter 5.1, an error in the surface potential profiles obtained on the In_2O_3 TFTs under operation using the EFM method due to the tip induced band banding is analysed using a combination of experimental and simulation techniques.

Carrier confinement in the $ZnO/Mg_xZn_{1-x}O$ material system makes it a good candidate for HEMT applications. The undoped $ZnO/Mg_xZn_{1-x}O$ structure will have a 2DEG formed in the ZnO channel layer due to the interplay between spontaneous and piezoelectric polarizations in the heterostructure [48]. The first n-channel depletion mode $ZnO/Mg_{0.3}Zn_{0.7}O$ heterostructure field effect transistor (HFET) was suggested by Koike *et al.* in 2005 [53]. In Chapter 5.2, a concept of ZnO/GaZnO HFET similar to $ZnO/Mg_xZn_{1-x}O$ HFET will be presented.

All listed simulations in this thesis are performed using Silvaco Atlas. Silvaco Atlas is a physically-based device simulator with an effective numerical algorithms used to obtain the solutions. Silvaco allows electrostatic and transport simulations of metal-semiconductor structures and semiconductor devices. More details about simulation setup and physical models used will be seen in Chapter 2.

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Chapter 2 Simulation methodology

2.1 Device simulations using Silvaco

Silvaco software combines interface tools like Atlas, DeckBuild, Tonyplot, and Devedit for physically-based 2D and 3D simulations of semiconductor devices [1], as explained in Chapter 1. In this chapter the details of the device modelling using the Silvaco Toolbox are given.

Physical models for simulations of semiconductor devices can be presented as a system of discrete non-linear problems that only approximate the behaviour of the continuous model. This approximation is performed using a discretisation method. Therefore, any solution for a device system will be presented as a non-linear algebraic problem which consists of: 1) non-linear partial differential equations which will be solved on the 2) structure mesh using 3) a discretisation method.

The calculation of the discrete non-linear problem starts with the initial guess solution. The solution is then obtained iteratively. The iteration is finished when the convergence criteria are achieved: the corrections between iterations are smaller than the specified tolerance. In addition, a maximum number of iterations is often defined. If the convergence was not achieved in the maximum allowed number then a different numerical technique should be used or a structure mesh needs to be reconsidered. Corrections between the iterations are obtained by linearization of the problem. The convergence criteria are an important aspect as it defines if the solution will be obtained, the accuracy of the approximation in the solution, time needed to obtain the solution (efficiency), and if the method can be applied to the wide range of the solutions (robustness).

Atlas supports several boundary conditions: Ohmic contacts, Schottky contacts, insulated contacts, and Neumann (reflective) boundaries.

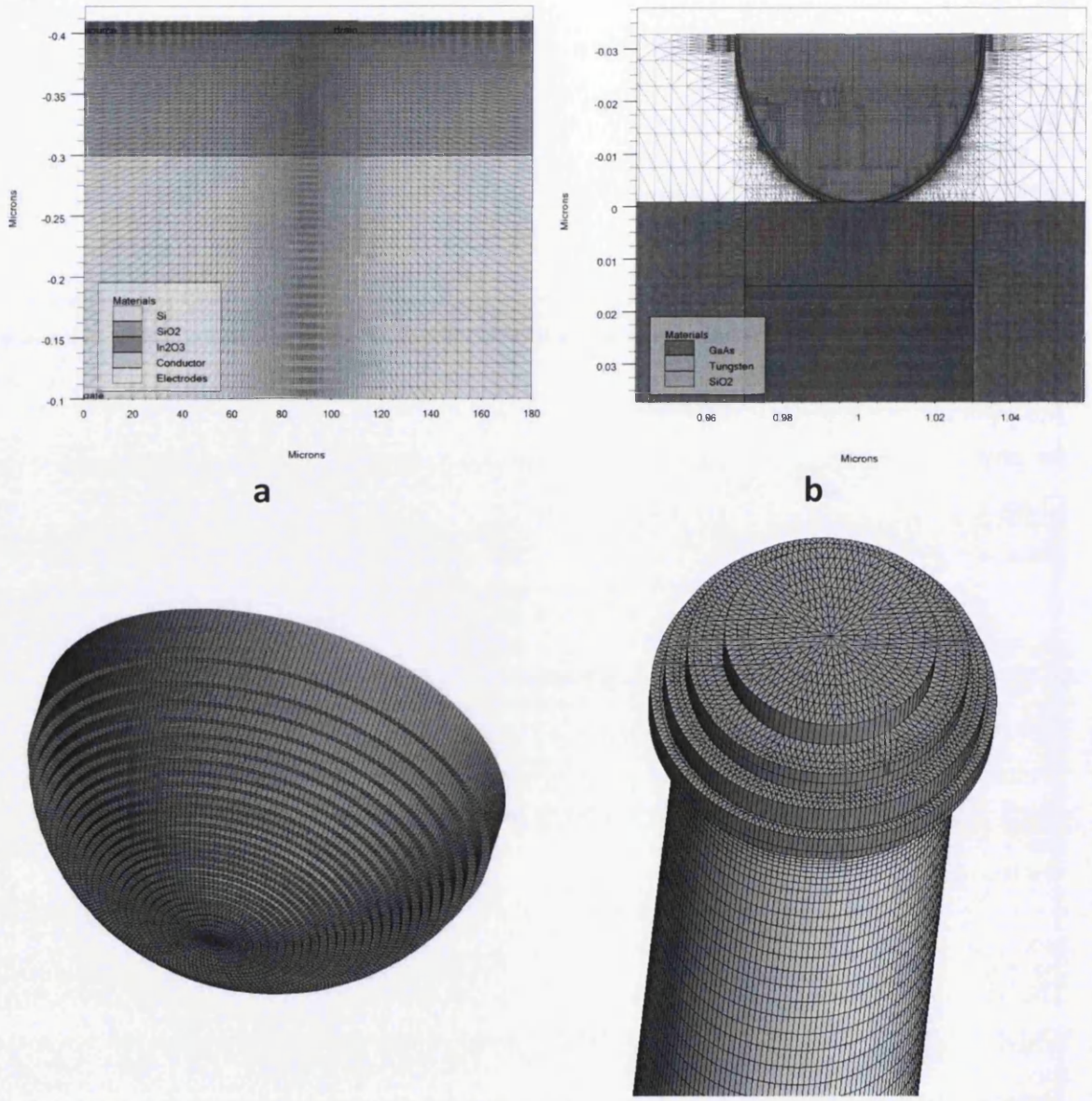


Figure 2.1.1. Example of 2D mesh for (a) rectangular structure of the In_2O_3 thin film transistor demonstrated in Chapter 5 created using Atlas commands, (b) arbitrary tip-sample structure shape used in Chapter 3.7 created using DevEdit command. Circular 3D mesh for the (c) tip structure in Chapter 3.3, (d) ZnO nanowire structure used in Chapter 4 created using Atlas commands.

2.1.1 Mesh considerations

For accurate modelling of the device geometry Atlas allows the specification of a rectangular triangular finite element mesh for 2D geometries (the structure is specified using X and Y coordinates) and 3D geometries (the structure is specified using X, Y and Z coordinates). Triangular mesh has two triangular elements in each rectangular pixel as seen in Figure 2.1.1(a) and (b). A circular mesh specification is also available. For the circular mesh, radial mesh spacing and angular mesh spacing should be defined as seen in Figure 2.1.1(d). For a 3D circular mesh, Z spacing should be specified additionally.

The CPU time required to obtain the solution for a mesh with N nodes is proportional to N^a, where values of a~2-3 [1]. Having a fine mesh in the structure is critical because it will affect the accuracy of the solution. The number of nodes used should not also be in excess as this might affect the numerical efficiency. That is why the mesh is normally optimised depending on the region importance and change in quantities in this region.

It is important to have a refined mesh in the following regions: at the electrode and channel junctions with the high electric field (as seen in Figure 2.1.1(a) for In_2O_3 thin film transistor channel), insulator layer through which tunnelling is allowed (as seen in Figure 2.1.1(b) for tip-sample structure), heterojunctions which form the channel in high electron mobility transistors (HEMTs) (as will be used for HEMT structure in Chapter 5.2). The number of obtuse triangles (long and thin triangles) should be minimised to avoid poor accuracy, convergence and robustness.

Figure 2.1.1 demonstrates different mesh types created using Atlas and the DevEdit toolbox. The rectangular triangular mesh is good for representation of the rectangular structures, and as seen in Figure 2.1.1 (a) for In_2O_3 thin film transistor there are no obtuse triangles in the structure (total grid points in the structure: 7979, obtuse triangles: 0 (0 %)). This structure of In_2O_3 thin film transistor in Figure 2.1.1 (a) will be used in Chapter 5.1. For an arbitrary structure shape the mesh should be created using the DevEdit environment. Figure 2.1.1(b) demonstrates the mesh for the tip covered in oxide in contact with the GaAs sample as will be seen in Chapter 3.7 created using the DevEdit toolbox. Due to the non-rectangular shape of this structure an approximation with a rectangular triangular mesh will

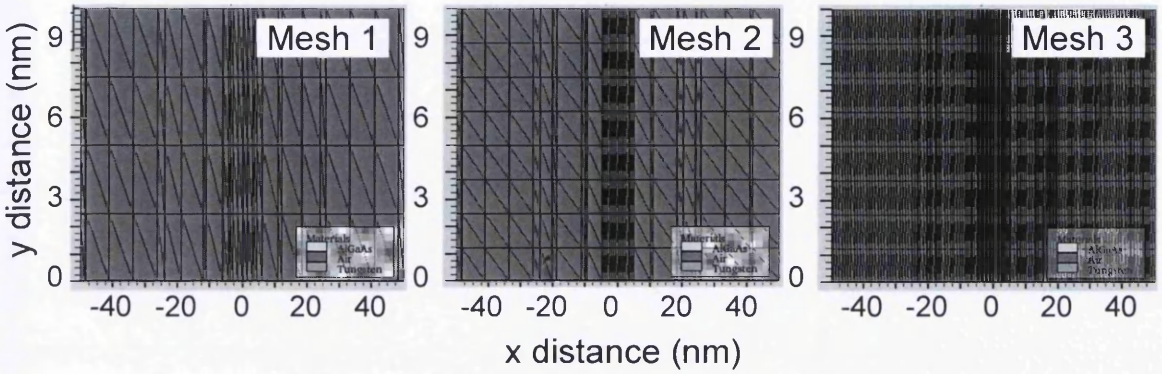
produce a small amount of the obtuse triangles (total number of grid points: 23596, number of obtuse triangles: 15 (0.0321523 %)). An example of the 3D circular mesh created using Atlas syntax is presented in Figure 2.1.1(c) (will be seen in Chapter 3.4) and Figure 2.1.1(d) (will be seen in Chapter 4). For the circular structures the mesh spacing is defined for the radial component and angular component.

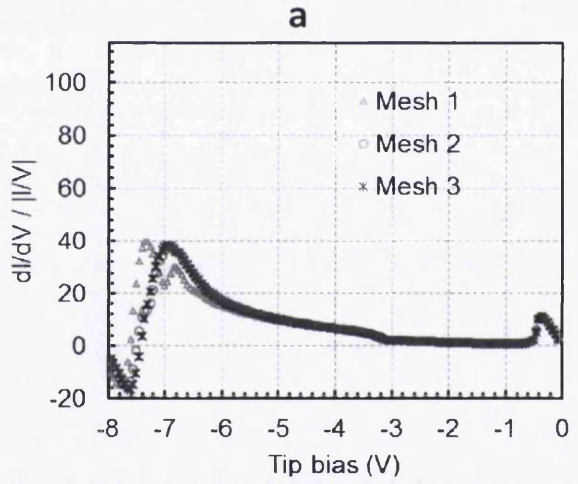
An example to demonstrate the mesh refinement effect on the final result of the calculations is shown in Figure 2.1.2. For circular tip structure as seen in Figure 2.1.1(b) and $Al_{0.3}Ga_{0.7}As$ sample with n-type doping concentration of $N_d=10^{18}$ cm^{-3} test simulations were performed for 1 nm tip-sample separation. Differential conductance (dI/dV)/|I/V| in Figure 2.1.2(b) was obtained for tree different mesh geometry shown in Figure 2.1.2(a). In Figure 2.1.2(a) the mesh was gradually refined at 10 nm around the tip apex for "Mesh 1" and "Mesh 2" because the tunnelling probability is the highest at this region. For "Mesh 3" the mesh density away from the tip apex was also increased. Results of the calculations of differential conductance (dI/dV)/|I/V| in Figure 2.1.2(b) shows that the mesh density of "Mesh 1" is not sufficient enough and result diverges from other more precise solutions with higher mesh densities. Calculation results for "Mesh 2" and "Mesh 3" are in good agreement that is why "Mesh 2" can be selected for further simulations because it requires a smaller computational time than "Mesh 3".

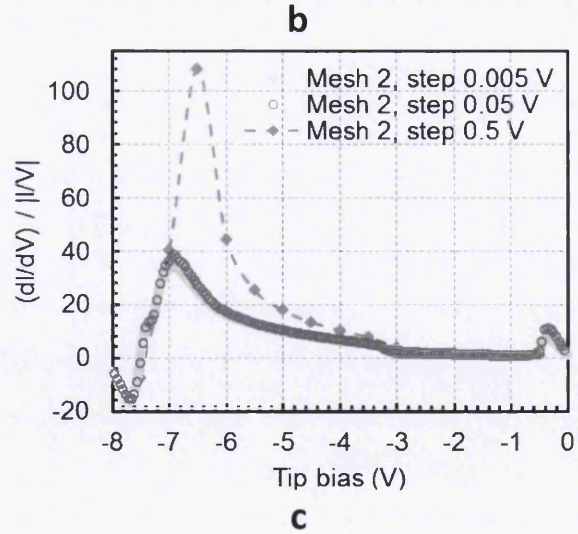
2.1.2 Numerical methods

When the regions are specified and the mesh is defined at every region of the device the structure will be created. The solution of the physical models can be found.

Discretisation processes will define variables at each mesh point. The error of the discretisation between two mesh points varies proportionally to the square of the separation between two nodes; the second order discretisation is used in Atlas. For the discretisation a box integration method is used [1]. The discretisation of the current densities and energy fluxes is performed using the Scharfetter and Gummel method [2].







c

Figure 2.1.2 (a) Example of the mesh geometry for the various mesh spacing. (b) Results of differential conductance calculation for various mesh spacing shown in (a) for n-type $Al_{0.3}Ga_{0.7}As$ sample. (c) Results of calculation for various bias step.

After discretisation of the problem on a mesh Atlas allows the following non-linear iteration solution methods: the Gummel decoupled method l, or the fully coupled Newton and Block method [1]. The choice of the non-linear iteration technique will define the iteration and convergence criteria.

The Newton algorithm [3] is default for most transport models including the drift-diffusion model. It solves a linearised complex problem for all variables making each iteration time-consuming. However, this method will have a quick convergence only with a good initial guess. The Gummel method [4] will divide a complex non-linear problem into a sequence of the linear sub-problems. The solution of a sub-problem will be found for the primary variable while other variables remain constant according to their recently computed values. Each step of the Gummel iteration is looking for the solution of each independent variable. This method will tolerate a poor initial guess but it requires more time to converge in comparison to Newton algorithm. The Gummel and Newton algorithms can be combined. Because Gummel method allows a poor initial guess, the initial guess can be refined using Gummel algorithm and the final result can be found with Newton algorithm which will give better convergence.

The Block algorithm is used when the lattice heating model is activated and also for the energy balance equation transport model (a hydrodynamic model). This method gives a solution for the sub-groups of equations. In Atlas this division of the complex problem into sub-groups was done based on the numerical experiments [1]. This method will not be used in this work because it is not available for 3D models and we consider self-heating only in 3D structures. In the present work a combination of Gummel and Newton algorithms is used.

If there are x variables in the problem and y mesh nodes then for the whole system there are $x \times y$ unknowns. Each Newton iteration solves a matrix with $(x \times y)^2$ elements and Gummel methods solves matrix with n^2 elements. The size of the problem will define the algorithm according to which linear sub-problems are solved. There are two methods for solving linear sub-problems available: the direct method and the iterative method [1]. For large linear systems, the iterative method will require less memory and time for calculations. The solution is found by making corrections to the initial guess. Atlas 2D uses the direct method to solve

sparse matrices in which variables at each node are connected only to the neighbouring nodes.

Stable convergence can be also achieved by reducing the calculation step. An example to demonstrate the effect of bias step on the final result of the calculations is shown in Figure 2.1.2(c). The differential conductance (dI/dV)/|I/V| was calculated with various bias steps: 0.5 V, 0.05 V and 0.005 V. Bias step of 0.5 V is not sufficient enough and result diverges from other more precise solutions with smaller calculation steps. Calculation results for bias steps of 0.05 V and 0.005 V are in good agreement that is why bias step of 0.05 V can be selected for further simulations because it requires a smaller computational time than bias step of 0.005 V.

Detailed explanations of the physical models that are solved on the structure mesh are found in the following chapters.

2.2 Modelling transport across metal-semiconductor junction

Metal-semiconductor contacts can be separated into two different types according their typical behaviour: Ohmic contacts with linear current-voltage characteristics and Schottky (rectifying) contacts which have asymmetric current-voltage characteristics. However, in reality, Ohmic contacts are just Schottky contacts with low resistivity [5]. The Schottky contact is formed when there is a potential barrier between carriers in the metal and carriers in the semiconductor - the Schottky potential barrier [6].

In this chapter the theory for the simulation of the Schottky metal-semiconductor contacts is presented in detail. The described in this Chapter models for metal-semiconductor contact including barrier lowering, thermionic emission and tunnelling current will be used to simulate metal probe in contact with sample surface in Chapter 3.8, ZnO nanowires with Au particle deposited on top or in contact with tungsten probe in Chapter 4, and device modelling in Chapter 5.

2.2.1 Formation of the Schottky contact

The first theory on the formation of the Schottky barrier was introduced by Walter Schottky [7] and also Sir Neville Mott [8], and was further corrected and developed by Hans Bethe [9].

When a metal and semiconductor are not in contact the vacuum level of both regions are aligned (Figure 2.2.1 (a)). The vacuum level represents the energy of the free electron in space. The metal work function ϕ_m represents the position of the Fermi level E_F with respect to the vacuum level. The semiconductor affinity χ expresses the position of the lowest conduction band energy with respect to the vacuum level. The metal work function represents the lowest energy needed to remove an electron from the metal. The semiconductor affinity represents the lowest energy needed to remove an electron from the bottom of the conduction band.

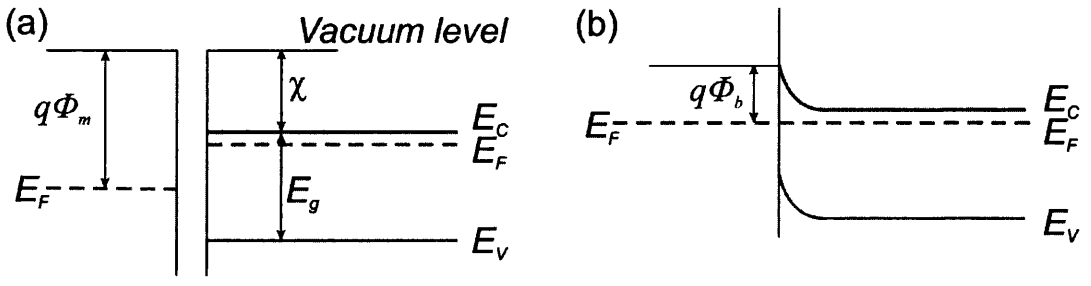


Figure 2.2.1 (a) n-type semiconductor and metal in separation. (b) n-type semiconductor and metal in contact.

When metal and semiconductor are brought in to intimate contact (Figure 2.2.1 (b)) the thermal equilibrium in a single system is established. This is due to the alignment of the Fermi levels in the semiconductor and metal which results in charge movement from the semiconductor to the metal. The negative electric charge will build up at the metal interface and an equal positive charge will build up at the semiconductor surface. Due to charge movement a depletion region of width W will be created at the semiconductor surface. The potential difference at the metal-semiconductor interface due to the energy band offset will be equal to the initial difference in the Fermi levels. For an n-type semiconductor a created barrier height ϕ_b will be calculated from the standard expression of the Schottky-Mott theory [6]:

$$q\phi_b = q(\phi_m - \chi) \tag{2.1}$$

The barrier height for the p-type semiconductor is given by:

$$q\phi_b = E_g - q(\phi_m - \chi) \tag{2.2}$$

The surface potential ψ_S changes with the applied voltage V as described by the expression:

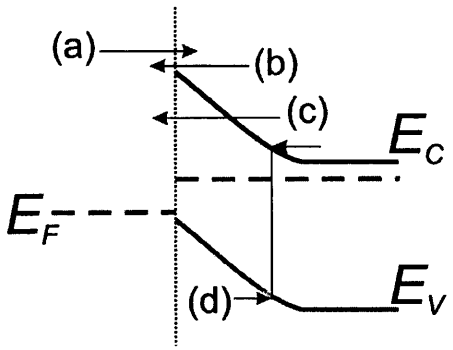


Figure 2.2.2 Schematic band diagram showing the carrier transport due to (a) thermionic emission, (b) carrier diffusion, (c) tunnelling and (d) recombination.

$$\psi_S = \frac{E_g}{2q} + \frac{kT}{2q} \cdot \ln\left(\frac{N_C}{N_V}\right) - \phi_m + \chi + V \tag{2.3}$$

where E_g is the band gap, T=300 K is the ambient temperature, and N_C, N_V are the conduction and valence band density of states, respectively.

As demonstrated in Figure 2.2.2, depending on the barrier shape (barrier height ϕ_b and barrier width W) carrier transport can be due to (a) thermionic emission of carriers from the metal to semiconductor over the potential barrier (see Chapter 2.2.3), (b) carrier diffusion from the semiconductor to the metal over the potential barrier, (c) carrier tunnelling through the potential barrier (see Chapter 2.2.4), and (d) recombination in the space-charge region.

2.2.2 Barrier lowering

The barrier height at the metal-semiconductor interface can be different from the ideal value described in Equations (2.1) and (2.2) due to the (a) presence of the interface states, (b) barrier lowering due to the image force, and (c) dipole effects [10].

Image force is a bias dependent effect which results in barrier lowering in the presence of an electric field [11]. At the metal-vacuum interface when the electric field is applied at the metal the electron will escape from the metal side. This electron will create a positive charge at the metal surface (a negative charge at the vacuum side). This positive charge at the metal side is called image charge. The image charge will induce the Coloumb attractive force called the image force, which tends to return the electron back to the metal side. When an electric field is applied the effect of the image force at the metal-vacuum interface will result in a lowering of the metal work function [12].

The effect of the image force barrier lowering is also observed at the metal-semiconductor interface even when no bias is applied due to the presence of the depletion region which will create a non-zero electric field (E) at the metal-semiconductor junction. The field dependent barrier lowering due to the image force $\Delta\phi_{im}$ is calculated as follows [11]:

$$\Delta\phi_{im} = \sqrt{\frac{qE}{4\pi\varepsilon_S}} \tag{2.4}$$

The image force effect at the metal-semiconductor interface is demonstrated in Figure 2.2.3. It is bias dependent, s due to image force barrier lowering $\Delta\phi_{im}$ being directly proportional to $E^{1/2}$. In Figure 2.2.3 (a) the electric field without barrier lowering has a maximum value close to $x=0$ and decreases to zero at $x=W$. This will result in a rounding off of the corners of the barrier only close to the metal-semiconductor interface and a reduction of the barrier height by the value of $\Delta\phi_{im}$ as seen in Figure 2.2.3 (b).

The barrier lowering due to dipole layer effects $\Delta\phi_d$ is calculated as follows [11]:

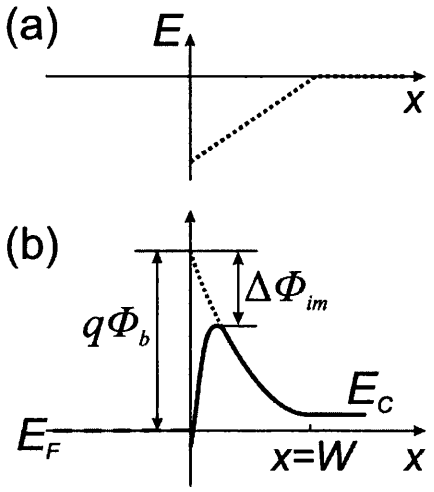


Figure 2.2.3 Schematic diagram showing the electic field (a) and image force barrier lowering (b) at the metal-semiconductor interface.

$$\Delta\phi_d = \alpha \cdot E \tag{2.5}$$

where E is an electric field, α is a linear coefficient [13].

2.2.3 Thermionic emission

Generally, the thermionic emission is the emission of electrons from a hot metal surface [11]. In the case of metal-semiconductor contacts the thermionic emission current flow from the semiconductor to the metal is defined as the concentration of electrons which have a minimum kinetic energy sufficient to overcome the potential barrier: $m^*\upsilon^2/2 \geq q\phi_b + E_{Fn}$, where m^* is the electron effective mass and υ is a carrier velocity. In general form the thermionic emission current can be written as follows:

$$J_{th} = \int_{q\phi_b + E_{Fn}}^{\infty} q\upsilon dn \tag{2.6}$$

The thermionic emission current depends solely on the barrier height at forward bias conditions. When incorporating the thermionic emission model, the surface thermal velocities for electrons V_{SN} and holes V_{SP} were calculated as follows [1]:

$$V_{SN} = \frac{A_{RN}T^2}{qN_C} \tag{2.7}$$

$$V_{SP} = \frac{A_{RP}T^2}{qN_V} \tag{2.8}$$

where A_{RN} and A_{RP} are effective Richardson constants for electrons and holes. Values A_{RN} and A_{RP} account for quantum mechanical reflection and tunnelling, respectively.

$$A_R = \frac{4\pi q m^* k^2}{h^3} \tag{2.9}$$

The electron J_{thN} and hole J_{thP} currents at the surface due to thermionic emission were calculated for every triangle of the mesh structure using the value of the electric field for each triangle, taking into account the barrier lowering terms $\Delta\phi_b = \phi_b - (\Delta\phi_{im} + \Delta\phi_d)$:[5]

$$J_{thN} = qV_{SN}(n_s - n)\exp(\Delta\phi_b / kT) \tag{2.10}$$

$$J_{thP} = qV_{SP}(p_s - p)\exp(\Delta\phi_b / kT) \tag{2.11}$$

where n_s and p_s are the surface concentration of electrons and holes.

The thermionic emission current will be calculated through the device structure geometry at every grid point of the mesh.

2.2.4 Universal Schottky tunnelling model

The wave-like nature of the electrons will allow carriers to penetrate through the potential barrier when the barrier width is smaller than the tail of the electron wave function [11]. This carrier movement is called the tunnelling current, and a probability of the electron to pass through the potential barrier is called tunnelling probability.

The universal Schottky tunnelling model [14], [15] is used to calculate the tunnelling current J_{tunn}between the semiconductor and metal as follows:

$$J_{tunn} = \frac{AT}{k}\int_0^\infty \Gamma(E)\ln\left(\frac{1+f_{ZnO}(E)}{1+f_{Au}(E)}\right)dE \tag{2.12}$$

where A is the effective Richardson's coefficient, $\Gamma(E)$ tunnelling probability, $f_{ZnO}(E)$ and $f_{Au}(E)$ are Maxwell-Boltzmann distribution functions in the ZnO semiconductor and Au.

The tunnelling probability is calculated using the Wentzel-Kramers-Brillouin (WKB) method [17] assuming a linear variation of the potential between two mesh points:

$$\Gamma(x) = \exp\left(\frac{-4x\sqrt{2m^*}}{\hbar}\sqrt{(-q\phi_m + q\phi_b - E_c(x))}\right) \tag{2.13}$$

The calculation of the tunnelling current is done for both electrons and holes. In the present simulations the tunnelling current model will allow current calculations at a fixed distance away from the metal-semiconductor interface (typically 0.01 μm).

2.3 Modelling transport across thin barrier

Tunnelling through an insulating layer was first investigated by Fowler and Nordheim [18], [19]. Comparison between experimental data and theoretical calculations using the Fowler-Nordheim model for ultra-thin insulators (below 3 nm) resulted in calculated currents which were far too low and a new concept of direct tunnelling model was suggested instead [22]–[25]. Because the theory in this Chapter will be applied to investigation of the scanning tunnelling microscopy (Chapter 3) in where typical values of the air/vacuum gap are below 2 nm [26]–[28] the direct quantum tunnelling model will be used in the calculations.

2.3.1 Direct tunnelling through ultrathin insulator

Tunnelling current calculations within the direct quantum tunnelling model [1] take place along parallel slices through the gap. The model is based on a formula for elastic tunnelling proposed by Tsu and Esaki [29], and further developed by Price and Radcliffe [30]. The current density J through a potential barrier is obtained according to the number of generated carriers using the following formula [23]:

$$J = \frac{qkT}{2\pi^2\hbar^3} m^* \int T(E) \times \ln\left[\frac{1+\exp(E_{Fsamp} - E)/kT}{1+\exp(E_{Flip} - E)/kT}\right] dE \tag{2.14}$$

where $T(E)$ is the transmission probability, E is the charge carrier energy, $m^* = \sqrt{m_x m_y}$ (where m_x and m_y are carrier effective masses in the lateral directions), $E_{F_{tip}}$ is the tip quasi-

Fermi level and $E_{F_{samp}}$ is the sample quasi-Fermi level. The integration term is determined with respect to the band edge position for every bias point. In equilibrium, $E_{F_{samp}} = E_{F_{tip}}$ and the term J is equal to zero.

The transmission probability $T(E)$, defined as the ratio of transmitted and incident currents, is calculated by solving Schrödinger's equation in the effective mass approximation [31]. It was demonstrated in the past that these approximations are very accurate to describe the sample-tip system in STS [32] because electrons do not tunnel in to or from one specific energy level, instead using a broad band of energies decaying away exponentially from the Fermi level. The transmission probability $T(E)$ is obtained using Gundlach formula [33]:

$$T(E) = \frac{2}{1+g(E)} \tag{2.15}$$

with

$$\begin{aligned} g(E) = {} & \frac{\pi^2}{2}\frac{m_s k_m}{m_m k_s}\left(Bi'_d Ai_0 - Ai'_d Bi_0\right)^2 + \frac{\pi^2}{2}\frac{m_m k_s}{m_s k_m}\left(Bi_d Ai'_0 - Ai_d Bi'_0\right)^2 + \\ & + \frac{\pi^2}{2}\frac{m_m m_s}{\lambda_0^2 m_i^2 k_s k_m}\left(Bi'_d Ai'_0 - Ai'_d Bi'_0\right)^2 + \frac{\pi^2}{2}\frac{\lambda_0^2 m_i^2 k_m k_s}{m_s m_m}\left(Bi_d Ai_0 - Ai_d Bi_0\right)^2 \end{aligned} \tag{2.16}$$

where m_m, m_s and m_i are effective electron masses in metal, semiconductor and insulator respectively, k_m and k_s are the wavevectors in metal and semiconductor, respectively, $\lambda_0 = \hbar\Theta_i/qF_i$, and A_i and B_i are the Airy functions defined as following:

$$Ai_0 \equiv Ai\left(\frac{\Phi_B - E}{\hbar\Theta_i}\right) \tag{2.17}$$

$$Ai_d \equiv Ai\left(\frac{\Phi_B + qE_i d - E}{\hbar\Theta_i}\right) \tag{2.18}$$

where $\hbar\Theta_i = \sqrt[3]{q^2\hbar^2 F_i^2/2m_i}$, Φ_B is the barrier height for electrons or holes, E_i is electric field in insulator, and d is the insulator thickness [1], [23]. This approach was found to be

more accurate than the commonly used WKB approximation for the case of thin barriers for all energies due to the rapid change in the potential in the transport direction in ultrathin dielectrics [23], [34].

The tip-sample system is described by a 2D model such that electrostatics and current continuity equations are solved fully in 2D real space. In self-consistent calculations, the current continuity equations including tunnelling process are solved iteratively until convergence is achieved to obtain the terminal currents. The tunnelling current can also be obtained non self-consistently (in a post processing) for comparison. In practice, the non-self-consistent solution for a bulk semiconductor will be very close to the self-consistent solution of the current continuity equations as shown later.

To match experimental data to the theoretical calculations using tunnelling model the following free parameters are typically used in the literature: tip-sample separation, tip apex

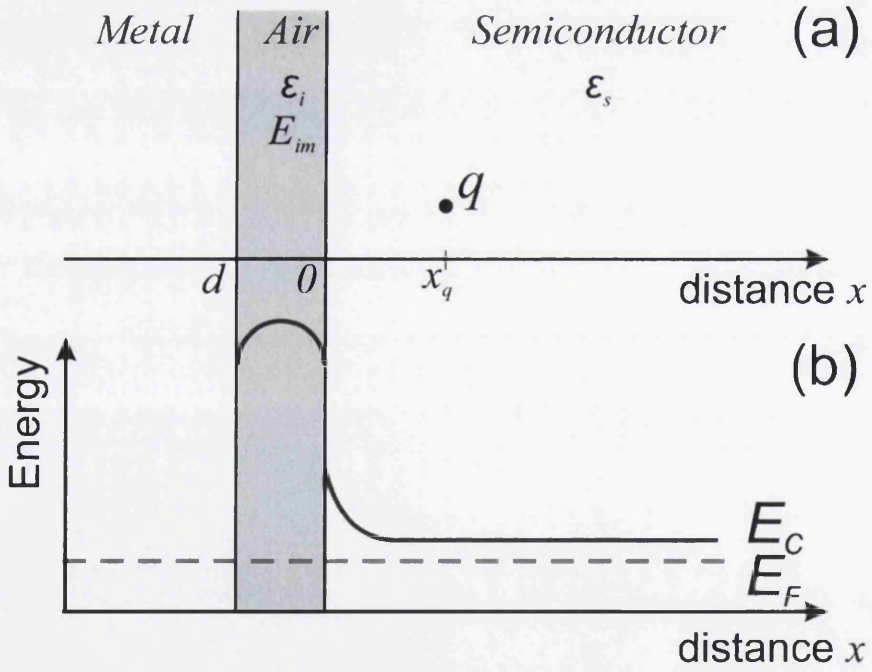


Figure 2.3.1 (a) Point charge q in the system of three media: metal, air/vacuum and semiconductor. (b) Rounding off the corners of the band profile in air/vacuum region in the presence of free charge carriers.

radius, tip work function, tunnelling area under the tip for 2D calculations, electron and hole effective tunnelling mass, 3 orders of magnitude correction to the current to account for the image force effect.

2.3.2 Image force barrier lowering model

The tunnelling model by Schenk for ultrathin insulator [23] layers accounts for the image force effects using a pseudobarrier method which calculates the transmission probability coefficient $T(E)$ (Equation (2.15)) of the modified trapezoidal potential barrier (Figure 2.3.1). To evaluate the effective barrier height (potential at the centre of the air/vacuum region in Figure 2.3.1(b)) as a function of electron incident energy, the image force potential is calculated according to the formula by Kleefstra and Herman [35]:

$$E_{im}(x) = \frac{q^2}{16\pi\varepsilon_i}\sum_{n=0}^{\infty}(k_1k_2)^n \times \left[\frac{k_m}{nd+x} + \frac{k_s}{d(n+1)-x} + \frac{2k_mk_s}{d(n+1)}\right] \quad (2.19)$$

where the reflection coefficients at metal and semiconductor regions are:

$$k_m = -1,\ k_s = \frac{\varepsilon_i - \varepsilon_s}{\varepsilon_i + \varepsilon_s} \quad (2.20)$$

and ε the relative dielectric permittivity of insulator (ε_i) and semiconductor (ε_s) regions, d is the insulator thickness, and x is the position through the barrier.

The image force potential is added to the trapezoidal barrier potential. The model assumes the simple parabolic approximation of the barrier shape due to the fact that for a very thin potential barrier the error is negligible [36]. The barrier height is evaluated at three different energy levels as follows [1]:

$$\Phi(E) = \Phi(E_1) + \frac{\Phi(E_3)-\Phi(E_1)}{(E_3-E_1)(E_2-E_3)}(E-E_1)(E_2-E) - \quad (2.21)$$

$$-\frac{\Phi(E_2)-\Phi(E_1)}{(E_2-E_1)(E_2-E_3)}(E-E_1)(E_3-E)$$

The Schenk tunnelling current model was implemented both self-consistently and in post processing calculations [1].

2.3.3 Material parameters of III-V semiconductors

The material parameters used in simulations can be found in Table 2.3.1 and Table 2.3.2, where m_c is an effective mass in the conduction band, $m_{hh}$is a heavy hole effective mass, m_{lh} is a light hole effective mass and E_g is a band gap.

Table 2.3.1 The material parameters used in simulations [1].

Material	m_c, [× m_o]	m_{hh}, [× m_o]	m_{lh}, [× m_o]	E_g, [eV]	Affinity, [eV]
GaAs	0.067	0.49	0.16	1.42	4.07
InP	0.0759	0.56	0.12	1.35	4.4
GaP	0.13	0.79	0.14	2.75	4.4
$Al_{0.3}Ga_{0.7}As$	0.092	0.571	0.157	1.8	3.75
$In_{0.53}Ga_{0.47}As$	0.045	0.532	0.088	0.734	4.67

Table 2.3.2 Band gap defaults used in simulations and in literature.

Material	Ref.	Eg(300), [eV]	Er, [eV]	El, [eV]	Ex, [eV]	Erl	Erx	Exl
InAs	[1]	0.35	0.417	1.133	1.433	0.716	1.016	0.3
	[38]	0.354	0.35	1.08	1.37	0.73	1.02	0.29
InSb	[1]	0.174	0.235	0.93	0.63	0.695	0.395	0.3
	[38]	0.17	0.17	0.68	1.0	0.51	0.83	0.32
InP	[1]	1.35	1.4236	2.014	2.3840	0.5904	0.9604	0.37
	[38]	1.344	1.34	1.93	2.19	0.59	0.85	0.26
GaAs	[1]	1.42	1.519	1.815	1.981	0.296	0.462	0.166
	[38]	1.424	1.42	1.71	1.90	0.29	0.48	0.19
GaSb	[1]	0.81	0.812	0.875	1.141	0.063	0.329	0.266
	[38]	0.726	0.726	0.81	1.03	0.084	0.31	0.22
GaN	[1]	3.42-3.507						
	[38]	3.2-3.503	3.2	4.8-5.1	4.6			

On the flat defect free (110) surface of III-V materials there are no surface state distributions centred in the bandgap and the surface can be modelled as bulk [37]. Nevertheless, the developed methodology allows a full treatment of surface states very straightforwardly and can be included in a wide range of ways from i) uniform distribution of defect states, via ii) realistic distribution either defined by iia) analytical functions (Gaussian, exponential) or even iib) a realistic distribution of surface states obtained experimentally, to introducing iii) interface traps.

2.4 Modelling thermal effects

In the present work, a thermal model considers carrier transport of electrons and holes self-consistently coupled with thermal flow [39]. Since the transport parameters depend on the lattice temperature, lattice heating and cooling due to the carrier generation and recombination, Joule heating and Peltier-Thomson effects are also included [39]. The thermal modelling considers temperature dependent thermal conductivity model [40] and heat capacity model [41] for ZnO.

The effective density of states for electrons and holes, mobility and electron and hole current densities (J_n, J_p) are calculated as a function of the local lattice temperature T_L [1], [39]:

$$J_n = -q\mu_n n(\nabla\phi_n - P_n\nabla T_L),\ J_p = -q\mu_p p(\nabla\phi_p + P_p\nabla T_L) \qquad (2.22)$$

where ϕ_n and ϕ_p are electron and hole quasi-Fermi levels, μ_n and μ_p electron and hole mobilities, n and p are the electron and hole concentrations, P_n and P_p are electron and hole thermionic powers. The thermopower is calculated based on the following components: temperature dependent Fermi potential, carrier scattering and phonon drag contribution (it is not significant for the high doped ZnO used in the present work).

The heat flow equation [39] is used in the simulation:

$$C\frac{\partial T_L}{\partial t} = \nabla(k\nabla T_L) + H \tag{2.23}$$

The heat generation rate H is calculated taking into account Joule heating H_J, generation and recombination heating, and cooling H_{GR} and Thompson-Peltier effects H_{TP} as follows:

$$H = H_J + H_{GR} + H_{TP} \tag{2.24}$$

where

$$H_J = \left|\vec{J}_n\right|^2 \Big/ q\mu_n n + \left|\vec{J}_p\right|^2 \Big/ q\mu_p p \tag{2.25}$$

$\vec{J}_n$ and $\vec{J}_p$ are the electron and hole current densities.

$$H_{GR} = q(R-G)\left((P_p - P_n)T_L + \phi_p - \phi_n\right) \tag{2.26}$$

G and R are the carrier generation and recombination rates, P_p and P_n are the thermoelectric powers of electrons and holes, ϕ_n and ϕ_p are the quasi-Fermi levels of electrons and holes. The Thompson-Peltier effects are given by the expression:

$$H_{TP} = -T_L\left(\vec{J}_n \nabla P_n + \vec{J}_p \nabla P_p\right) \tag{2.27}$$

In the numerical solution of the model an air region around structure and insulator layers are used as a heat sink layers to simplify the solution because no current continuity equations are solved in insulator regions. The bottom contact is defined as a thermal boundary condition and it is kept at the constant temperature T_c. The thermal boundary condition is defined as [1]:

$$\sigma\left(\vec{J}_{tot} \cdot \vec{s}\right) = (T_L - T_c) \Big/ R_{th} \tag{2.28}$$

where $\vec{J}_{tot}$ is a total energy flux, $\vec{s}$ is a unit normal to the boundary and σ is equal to 1 or 0. When $\sigma=0$ then $T_L=T_c$ and the Dirichlet boundary condition is specified.

The thermal boundary condition with the fixed temperature of 300 K is specified at the bottom contact of the structure, and the air region around the structure is used as a heat sink layer in the calculations.

2.4.1 ZnO thermal material parameters

In the model, the temperature dependent heat capacitance model is used. The heat capacitance C in $J/cm^3/K$ for ZnO was approximated from experimental data widely excepted in the literature [41] as a function of the lattice temperature as follows:

$$C = 3.22 + 4.68 \cdot 10^{-4} T_L - 1.31 \cdot 10^{-8} T_L^2 - 4.74 \cdot 10^4 T_L^{-2} \quad (2.29)$$

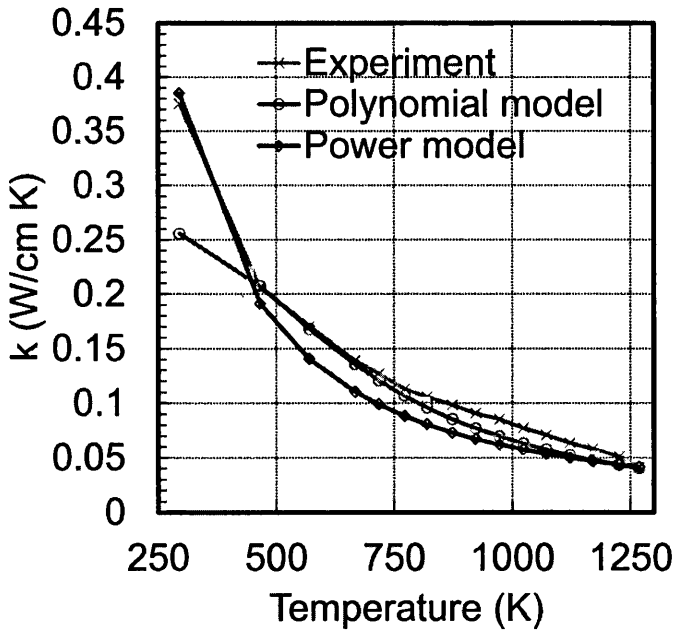


Figure 2.4.1 Comparison of the thermal conductivity models approximation with the experimental values of thermal conductivity for ZnO obtained by Olorunyolemi et al.[42]

The thermal conductivity k in $W/cm \cdot K$ for ZnO can be approximated from experimental data [42] using lattice temperature-dependent models. In Silvaco Atlas approximation using three following thermal conductivity models is available: i) simple model assuming $k(T_L)$ to be constant, ii) the power model:

$$k(T_L) = 0.37/(T_L/300)^{1.53} \tag{2.30}$$

and iii) the polynomial model:

$$k(T_L) = 1/(2 \cdot 10^{-5} T_L^2 - 9.9 \cdot 10^{-3} T_L + 5.0926) \tag{2.31}$$

The comparison between three models and the model agreement with the experimental data can be found in Figure 2.4.1.

Previous work on the thermal behaviour of ZnO nanowires under bias conditions [43], [44] used a constant value of the thermal conductivity. Figure 2.4.2 demonstrates the current and lattice temperature calculations for the different models of thermal conductivity: when

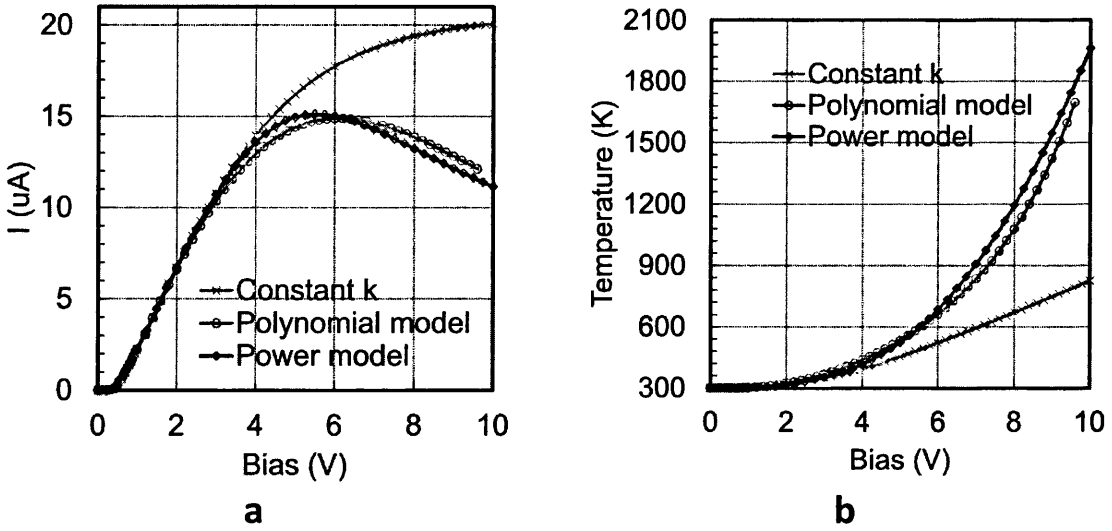


Figure 2.4.2. (a)Current calculations and (b) the highest lattice temperature value in the device for ZnO nanowire structure presented in detail in Chapter 4.

one uses a constant value of k=30 $W/cm \cdot K$ as in Refs. [43], [44], the polynomial model (Equation (2.8)) or the power model (Equation (2.7)). The data was generated for the 60 nm diameter ZnO nanowire and a full geometry of structure and simulation parameters can be found in Chapter 4.7. The polynomial and power models give relatively good agreement, but using a constant value of thermal conductivity would not model correctly the current degradation effect with temperature due to underestimating a lattice self-heating effect in the structure. For the simulations in this work a power thermal conductivity model was selected due to the better convergence at very high biases.

2.5 Modelling polarization effects in Wurtzite ZnO

For the present simulations a polarization model for Wurtzite materials was used, where the polarization effect is included as a fixed charge. The total polarization charge will be calculated as a sum of spontaneous P_{sp} and piezoelectric polarization P_{piezo} as:

$$P_{total} = P_{sp} + P_{piezo} \tag{2.32}$$

The spontaneous polarization in Wurtzite material is present at zero strain due to the lack of the lattice symmetry and deviation of the unit cells from the ideal Wurtzite geometry. Spontaneous polarisation P_{sp} is given in the polarization material parameters Table 2.5.1 for ZnO [40], [45].

Table 2.5.1 Polarization material parameters for ZnO

Parameter	Value	Units
Spontaneous polarization, P_{sp}	-0.057	C/m^2
Piezoelectric const. (Z), E_{33}	0.89	C/m^2
Piezoelectric const. (X,Y), E_{31}	-0.51	C/m^2

By default positive fixed charge will be placed at the top of the layer and negative fixed charge will be placed at the bottom of the layer. The model allows a scaling factor from -1 to 1 in order to modify the magnitude and a sign of the polarization charge.

The piezoelectric polarization is present when two materials are in contact due to the difference of the lattice constants. The piezoelectric polarization P_{piezo} will be calculated as follows:

$$P_{piezo} = 2\frac{a_s - a_0}{a_0}\left(E_{31} - \frac{C_{13}}{C_{33}}E_{33}\right) \tag{2.33}$$

where E_{31} and E_{33} are piezoelectric constants, C_{13} and C_{33} are the elastic constants, a_0 is a lattice constant, a_s is the average value of the lattice constant of the layer directly above and below.

Electronic band-structure parameters and lattice parameters for ZnO are provided in Table 2.5.2 [40], [45].

Table 2.5.2 Electronic band-structure parameters and lattice parameters for ZnO

Parameter	Value	Units
Electron effective mass (z)	0.23	m_0
Electron effective mass (t)	0.21	m_0
Hole effective mass param., A1	-3.78	
Hole effective mass param., A2	-0.44	
Hole effective mass param., A3	3.45	
Hole effective mass param., A4	-1.63	
Hole effective mass param., A5	1.68	
Hole effective mass param., A6	-2.23	
Direct band gap (300K)	3.37	eV
Spin-orbit split energy	0.016	eV
Crystal-field split energy	0.043	eV
Lattice constant, a_0	3.250	Å
Elastic constant, C_{33}	210.9	GPa
Elastic constant, C_{13}	105.1	GPa
Shear deform. potential, D1	3.9	eV
Shear deform. potential, D2	4.13	eV
Shear deform. potential, D3	1.15	eV
Shear deform. potential, D4	-1.22	eV

In the present work the spontaneous polarization ZnO-GaZnO (GZO) will be modelled. The material parameters for GZO used in the modelling [46], [47] are presented in Table 2.5.3.

Table 2.5.3 Electronic band-structure parameters for GZO

Parameter	Value	Units
Direct band gap (300K)	4.7	eV
Affinity	3.67	eV
Low field electron mobility	13	cm^2/Vs

The electron mobility in ZnO was modelled using Curve Fit Velocity Saturation Mobility Model. The model is based on Monte Carlo simulations of electron mobility change with the applied electric field and can be used in Silvaco Atlas using the following command: "ozgur.n". The model is based on the Monte Carlo mobility calculations for electrons in ZnO [40], [48], [1]. The mobility parameters used for the transport simulations in ZnO field effect transistors are presented in Table 2.5.4.

Table 2.5.4 Mobility model parameters for ZnO

Parameter	Value	Units	Reference
Low field electron mobility	155	cm^2/Vs	[40], [49]
Saturation velocity for electrons	1.9e7	cm/s	[1], [40],
Electric field	256e3	V/cm	[48]

2.6 Summary

Silvaco Atlas is a physically based device simulator that allows 2D and 3D analysis of electrical and thermal performance of the semiconductor based technologies. The material parameters and doping profiles are incorporated in the device structure created using the Atlas command language or the DevEdit toolbox. The simulator uses a rectangular triangular mesh. Accurate results and stable convergence are provided by the numerical methods of solving a non-linear algebraic problem and algorithm for the selection of the initial solution.

To model the transport across a metal-semiconductor interface the barrier height and potential distribution are calculated. The barrier lowering term due to the image force and dipole effects is included in the model. When calculating the thermionic emission current a surface thermal velocity is taken into account. The tunnelling current across the barrier is calculated using universal Schottky tunnelling model which is based on the calculation of the local tunnelling rates.

Transport across ultrathin insulator layer is accounted for using direct tunnelling model. The transmission probability of the tunnelling is calculated using Gundlach formula and the Schenk model for the image force barrier lowering term in the insulator layer. The image force potential is calculated based on the Kleefstra and Herman formula. The model assumes a parabolic approximation for the barrier as this approximation is accurate for ultrathin insulator layers.

Lattice self-heating effects can be included in the calculations. A thermal model considers carrier transport of electrons and holes self-consistently coupled with thermal flow. Since the transport parameters depend on the lattice temperature, lattice heating and cooling due to the carrier generation and recombination, Joule heating and Peltier-Thomson effects are also included. The thermal modelling considers temperature dependent thermal conductivity model and heat capacity model for ZnO because using a constant value of the thermal conductivity and thermal capacity will result in underestimation of the lattice temperature.

Finally, a polarization model for Wurtzite materials was used, where the polarization effect is included as a fixed charge. The total polarization charge will be calculated as a sum of spontaneous and piezoelectric polarization.

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Chapter 3 Results of scanning probe microscopy modelling

3.1 Introduction

As the active regions of electronic materials and devices reduce in size to the nanoscale, the analysis tools applied to them need to be able to characterise with a spatial resolution at the same length scale. Scanning probe microscopy (SPM) is one such technique and can be used to make surface electronic, morphological, optical, chemical and magnetic measurements down to the atomic scale [1]. Unlike most electron microscopy techniques, SPM can be applied to biased devices under operation [2]–[5]. The main limitation of the method is that with all SPM techniques the probe can interact electrostatically and physically with the sample, changing the measured properties of the device under test [6]. Modelling the electrostatic probe interaction can be used to quantify the measurement error, to match experimental results to device properties, or potentially to remove the effects of probe interaction [7]–[11].

In general, a number of approaches and computational techniques exists to estimate quantitatively the tip induced band bending on semiconductor surfaces by solving Poisson's equation in 1D [12]–[15], 2D [16] and 3D [17]. First-principles calculations such as density functional theory (DFT) [18]–[20] are often used to calculate band structure of the semiconductor surfaces, as measured using STS. However, DFT can be used to model only small system of atoms, and is therefore not suitable for tasks where the whole device structure needs to be included in the calculations. In addition to the limitation to a small number of atoms, the DFT is based on a single electron approximation [21], [22] and the assumption that there is a link between density and the exact ground state energy. Consequently, the calculation of excited states is cumbersome and computationally expensive

when a flexible basis is needed to simultaneously describe the ground and excited states. DFT can accurately model atomic scale band structure of single material but also has difficulty when considering two different types of materials like semiconductor and metal. Our approach, based on the 3-dimensional multi-physics device simulations, combing physical models of various complexities, is a more computationally suitable technique for the study of 10-100 nm scale systems of various materials (metals, semiconductors, dielectrics) as typical for studying device surfaces, where atomic level perturbations are self-averaged. For devices, long-rage Coulomb interactions at the surface (the electrostatics) have to be taken into account. Therefore, Coulomb interactions are included within a model of the whole device structure and with simultaneous tip-sample tunnelling [23], [24]. In addition, the effect of barrier lowering due to the image force is of the many body nature of the tip-sample structure. The effect can be included in DFT via an exchange-correlation potential [18], but only approximately at large computational costs. The computation of the tunnelling current is often based on the transfer-Hamiltonian formalism [25], [26] and is used for quantitative and qualitative tunnelling current evaluation [27]–[30].

In this chapter a simulation methodology to reproduce the scanning tunnelling spectroscopy (STS) and microscopy (STM) process using the simulation tool *ATLAS* by Silvaco [31] is presented. The developed methodology also allows realistic tip geometries as shown in Chapter 3.2. It allows correct modelling of the band gap for the variety of semiconductor materials as demonstrated in Chapter 3.3 and includes the effect of tip induced band bending (TIBB) as studied in Chapter 3.4. It can recover STM affected data enabling the study of a range of semiconductor devices including quantum well lasers [32], photovoltaic devices [33], resonant tunnelling diodes [34] and semiconductor sensors [35]. The simulation of the quantum tunnelling between the metal probe and the surface of the semiconductor is performed self-consistently, i.e., the electrostatic potential is obtained in an iterative process in which the solution of Poisson's equation follows the calculation of the tunnelling current until convergence is achieved.

The developed simulation methodology for modelling STS in this work uses a direct quantum tunnelling model based on Price and Radcliffe's formalism [36]. A detailed explanation of the model was given in Chapter 2. To estimate the validity of the results of the

2D finite element solution, Chapter 3.5 compares the computational results for *p*-GaAs with the experimental data and the model implemented by Feenstra [30]. Note that the model by Feenstra has a good agreement with experimental data and is widely accepted and used by other researchers [2], [37].

The methodology presented here also includes the effect of barrier lowering due to image force on the tunnelling of electrons and holes. The effect of the image force on the STS spectra is studied in Chapter 3.6. In the past, approximate approaches to compensate for the image force induced barrier lowering were applied equally to the conduction and valence band [30], [38], [39]. Following work by Schenk [40], we include a complete calculation of the image force effect in our model, which will later show that equal barrier height lowering in both the conduction and valence band is not appropriate and can miscalculate the tunnelling current by orders of magnitude.

The study in Chapter 3.7 also focuses on technologically relevant III-V materials including GaAs, InP, $Al_{0.3}Ga_{0.7}As$, $In_{0.53}Ga_{0.47}As$ and GaP.

The work presented in Chapters 3.2-3.7 has led to the following publication: O. Kryvchenkova, R. J. Cobley, and K. Kalna, "Self-consistent modelling of tunnelling spectroscopy on III–V semiconductors," *Appl. Surf. Sci.*, vol. 295, pp. 173–179, Mar. 2014. The work was also presented at the conference UK Semiconductors, July 2013, Sheffield UK, O. Kryvchenkova, K. Kalna, R. J. Cobley, "Modelling Scanning Probe Interactions using a Finite Element Device Simulator".

In Chapter 3.8, the effects of surface oxide layers on the probe-sample contact type is examined by taking contact and non-contact measurements with the probe oxide in place and then with the probe where the oxide is removed in a well-controlled way. The use of both contact and non-contact simulations allows an understanding of the modification of both tunnelling and thermionic emission due to contact type changes caused by the presence of oxide probe contamination, which both play a role in contact measurements.

For STS, previous experimental work [41] observed that leaving a metal tip to degrade in ultra-high vacuum changed the spectrum of a sample from Ohmic to Schottky suggesting

carbon or oxygen contamination of the tip [42]–[44]. In Chapter 3.8.1 a combination of experimental and simulations work gives a detailed explanation to the nature of changes in the STS spectra. Simulated structures were prepared and measured by other researchers.

A four-point probe (4PP) approach of SPM employs two outer probes to pass a current through the sample while two inner sense probes measure the potential difference of the sample [45]. Local probe methods can be used to measure nanoscale surface conductivity, but some techniques including nanoscale 4PP rely on at least two of the probes forming the same barrier to the sample with low resistivity non-rectifying contacts (see Chapter 1.1 for explanation). Schottky contacts, or non-equal contacts between the central voltage sense probes, would produce different contact resistances for the forward and reverse bias, which violate the assumptions made in the technique. Oxide coatings, which can occur on the surface of the 4PPs, can have an effect on the contact type formed, and so 4PP measurements should be taken with probes that are oxide free. In Chapter 3.8.2, the role of probe shank oxide has been examined by carrying out contact and non-contact current-voltage measurements on GaAs when the probe oxide has been controllable reduced, both experimentally and in simulation.

3.2 Probe shape

The tip-sample structure (including air surrounding the metal tip) is 2.5 μm wide with the bulk semiconductor layer 0.9 μm deep. An example of the 2D circular tip structure with a regular triangular mesh is given in Figure 1(e), where the projection of the cylindrical tip into 2D assumes that the tip is uniform in the z-direction. We have checked, by numerical experiments, that a sufficient number of grid points is used in the tip-sample separating region in the direction of the current flow. Homogeneous (reflecting) Neumann boundary conditions are used at all simulation cell boundaries except contacts where the Dirichlet boundary conditions are used. The metal tip is assumed to be a contact. An additional contact is added at the bottom of the semiconductor to allow for current to flow. The current flow from the semiconductor through the insulator/air is via a tunnelling process only.

To test the importance of the probe shape, several tip geometries were simulated, as shown in Figure 3.2.1. The discretised geometry of the finite element model allows any realistic tip shape. The triangular tip shape Figure 3.2.1 (b) results in a slow convergence of calculations of tunnelling current at high voltages for the low doped sample, while Figure 3.2.1 (c) and Figure 3.2.1 (d) give similar results, as seen in Figure 3.2.1 (f). The main difference in the results arises from the change in the electrostatic interaction of tip and sample. Due to the low doping of the sample a dopant screening effect will be low and tip induced band bending will be high for all tip shapes giving similar results of the conductivity calculation in Figure 3.2.1 (f). A circular tip shape (Figure 3.2.1 (c)) with a 70 nm tip radius, 1 nm tip-sample separation and a tip work function of 5 eV is used for the results presented here to reduce computational time.

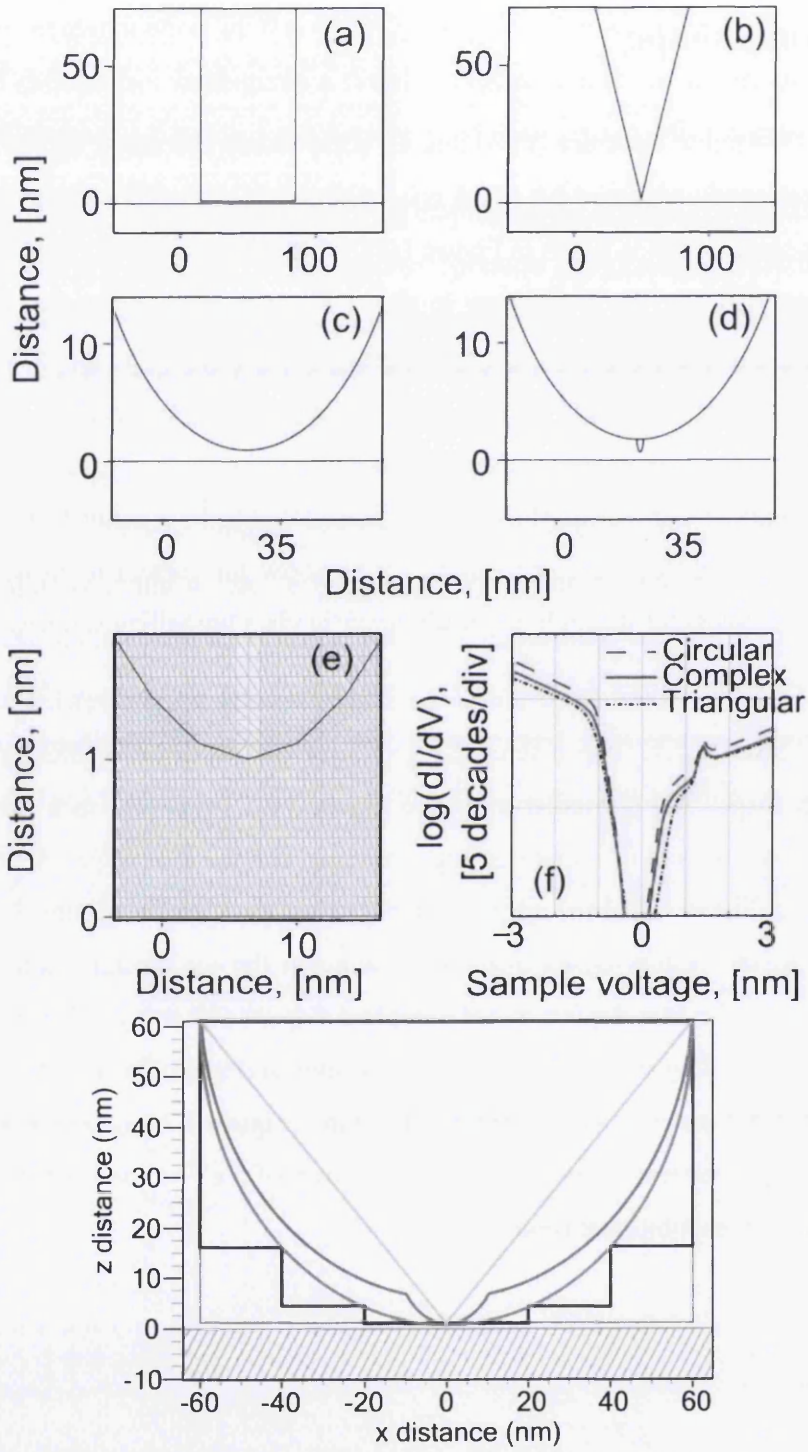

Figure 3.2.1 Probe tip in 2D of rectangular (a), triangular (b), circular (c) shapes, and realistic complex (d) shape with a large radius of 70 nm with a smaller tip on the top with a radius of 10 nm. (e) 2D circular tip structure with mesh. (f) Conductivity simulations for different tip shapes. (g) Overlay of different tip structures.

3.3 Band gap simulations for GaAs

Tunnelling spectra for *n*-type GaAs (*n*-GaAs) with a doping concentration of $N_D = 10^{18}$ cm^{-3} and $N_D = 10^{12}$ cm^{-3} are shown in Figure 3.3.2. For the *n*-GaAs with $N_D = 10^{12}$ cm^{-3}, the vertical solid lines at sample voltages of +1.5 V and -1.1 V indicate the onset of higher tunnelling outside of the band gap region. Similarly, for the *n*-GaAs with the $N_D = 10^{18}$ cm^{-3}, the lines at sample voltages of +0.65 V and -0.78 V indicate the band gap by the onset of larger tunnelling.

The change of the apparent band gap with doping concentration in Figure 3.3.2 demonstrates the effect of tip-induced band bending. For the higher doped case, the onset of

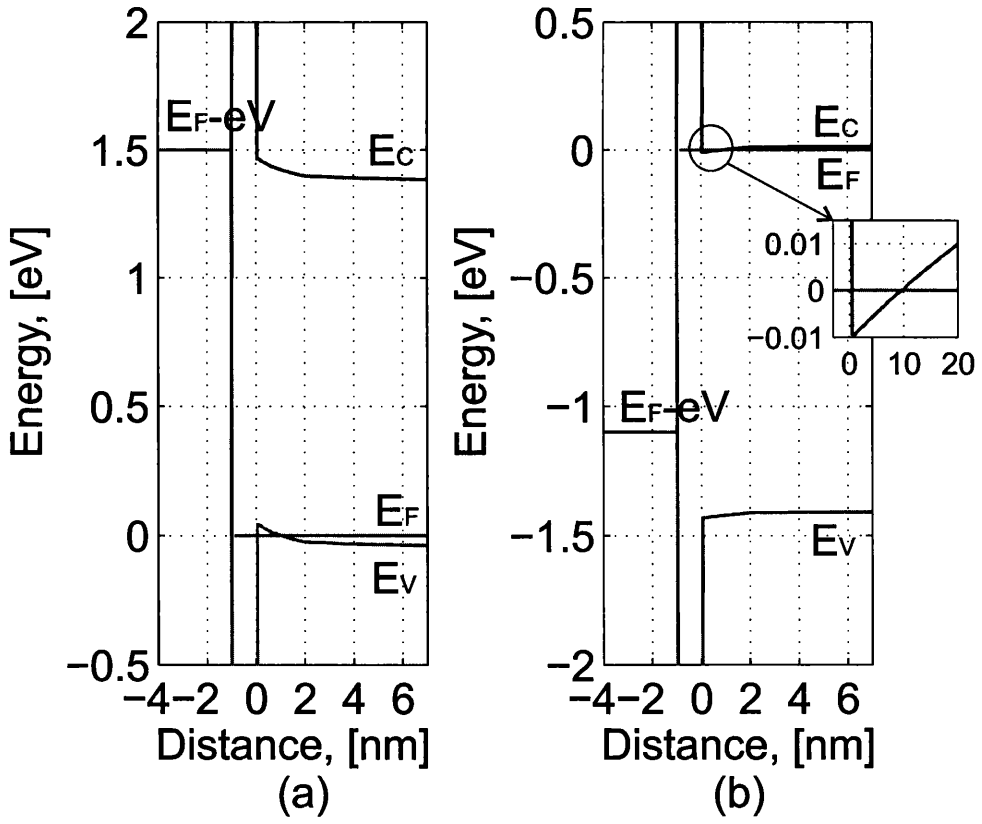

Figure 3.3.1 Energy band structure of the n-GaAs, $N_D = 10^{18}$ cm^{-3}, obtained at sample voltages of +1.5 V (a) and -1.1 V (b).

larger current corresponds to the tip crossing the valence and conduction band edges. In the case of low doping, the origin of the observed gap is not so straightforward. Therefore, the energy band alignment is shown in detail in Figure 3.3.1 for the onset voltages of +1.5 and -1.1 V. In Figure 3.3.1 (a), the applied tip voltage has induced depletion and inverted the surface to make it appear *p*-type. The tip applied bias has to be beyond +1.5 V before a significant tip-to-sample tunnelling can take place.

In Figure 3.3.1 (b), the sample surface is in accumulation appearing more *n*-type than the bulk. The induced surface accumulation region has filled states in the conduction band (see Figure 3.3.1 (b) inset) from which sample-to-tip tunnelling can take place before the tip crosses the valence band edge. This effect is described by Koenraad as Type I accumulation [13]. For $N_D = 10^{18}$ cm^{-3} *n*-GaAs, a band gap of 1.43 eV is obtained from simulations, 0.01 eV larger than the true band gap of 1.42 eV, which would be within the systematic error of experimental data [46]. The screening effect of the high doping reduces the amount of tip-

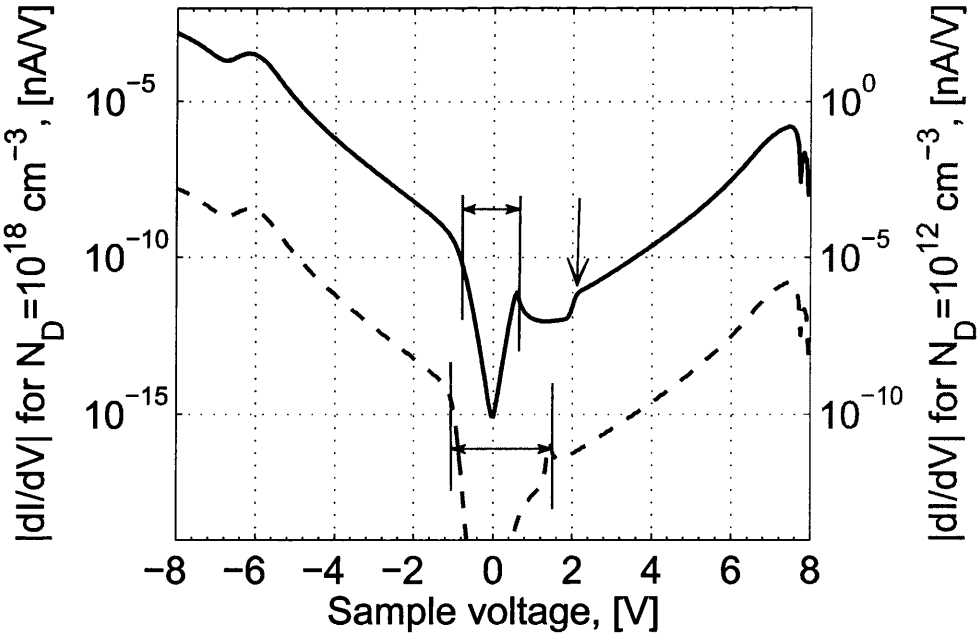

Figure 3.3.2 Tunnelling current spectra for the n-GaAs with a doping concentration of $N_D = 10^{18}$ cm-3 (blue solid line corresponds to the left scale) and $N_D = 10^{12}$ cm-3 (red dashed line corresponds to the right scale). The onsets of higher tunnelling in the CB and VB are marked with vertical lines.

induced band bending. For n-GaAs with a doping of $N_D = 10^{12}$ cm^{-3}, tip-induced band bending increases the observed band gap to 2.60 eV. An onset in the tunnelling current spectra is visible in the conduction band around +2 V in the highly doped n-type GaAs marked by an arrow in Figure 3.3.2.

Figure 3.3.3 shows the band edge in detail before and after the onset of the tunnelling current at +1.9 eV and +2.5 eV. At +2.5 eV, the surface inversion has bent the valence band above the sample Fermi level, allowing electrons to also tunnel from the tip to these empty inversion states. This is described by Koenraad as Type II inversion [13]. This induced depletion region is spatially localised under the tip. In Figure 3.3.3 (c) and (d), the tunnelling current contributions from the valence and conduction bands are shown as a function of distance, with the tip at the origin, for the corresponding case shown in Figure 3.3.2. At +2.5 V, the valence band tunnelling increases in magnitude beyond the conduction band tunnelling. In all cases, the tunnelling current is larger under the tip and reduces almost exponentially as a function of the tip-surface distance.

3.4 Tip induced band bending simulations

Tip-induced band bending (TIBB) is the effect which originates from the probe-sample interaction and will change the properties of the sample surface under study introducing a measurement error. The amount of a TIBB depends on the several factors: tip work function, tip-sample separation, tip radius and a doping level of the sample. While tip-sample separation, tip radius and a doping level of the sample change the observed amount of TIBB, a change in the tip work function shifts the voltage at which different regimes of TIBB occur.

To test the validity of the model, simulation of TIBB was performed for high doped and

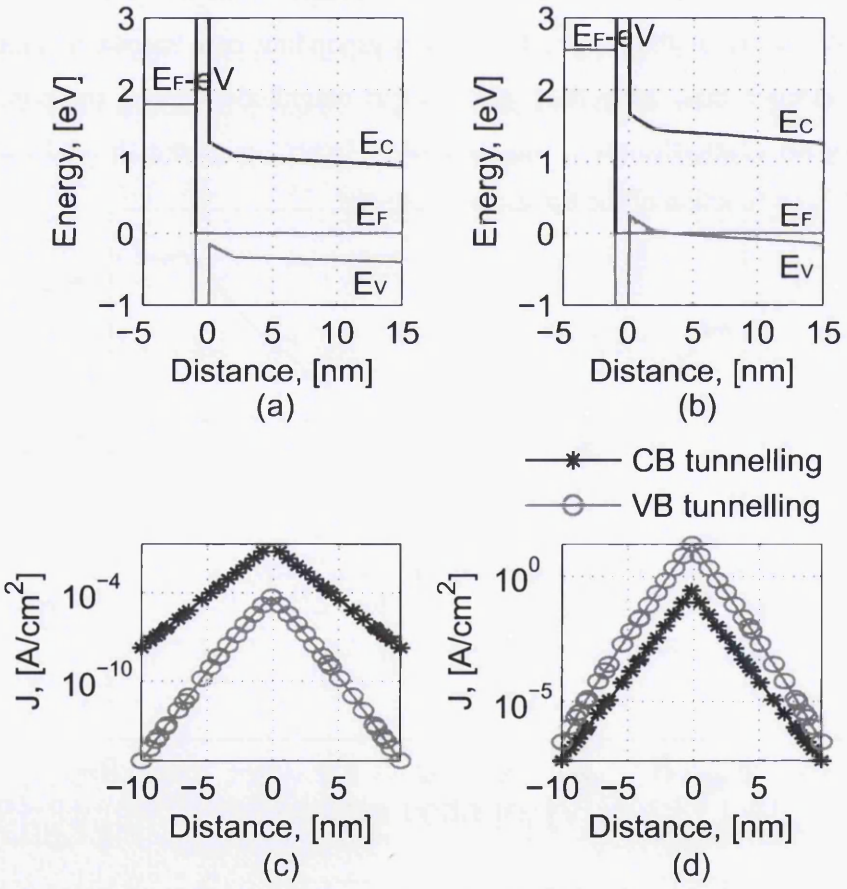

Figure 3.3.3 Energy band structure profiles at sample voltages of +1.9 V (a) and +2.5 V (b). Corresponding tunnelling current density from the conduction (blue stars) and valence (red open circles) bands at sample voltages of +1.9 V (c) and +2.5 V (d).

low doped semiconductors of *n*-type and *p*-type. In the simulation, a 3D approximation of the tip is used (Figure 3.4.1(a)). The tip was approximated using 30 sublayers. The coordinates of the tip structure were generated using *Matlab* code (see Appendix C) and the geometry simulation was performed using *Silvaco Atlas 3D*, where each coordinate (x_n, y_n) of the layer edge shown in Figure 3.4.1(b) was found as follows:

$$x_n(i) = i \cdot R/n \tag{3.1}$$

$$y_n(i) = \sqrt{R^2 - (iR/n)^2} \tag{3.2}$$

where R is the radius of the tip.

In the simulation, a 30 nm tip radius and 1 nm tip-sample separation were used. The calculation of TIBB was performed for different doping types and concentrations. High doped (10^{18} cm^{-3}) and low doped (10^{16} cm^{-3}) *p*-type and GaAs with a metal tip work function of 4.026 eV, and high doped (10^{18} cm^{-3}) and low doped (10^{16} cm^{-3}) *n*-type and GaAs with a tip work function of 4.3 eV.

Figure 3.3.3 demonstrates a bias-dependent effect of TIBB for different sample doping. In accumulation (positive bias for *p*-type GaAs, negative bias for *n*-type GaAs), the amount of the TIBB remains low. This is due to the doping screening effect. In the depletion and inversion regime, the TIBB is strongly dependant on the applied bias. For both samples of *p*-type and *n*-type, the decrease in the doping concentration will result in the increase of the TIBB at both negative and positive biases.

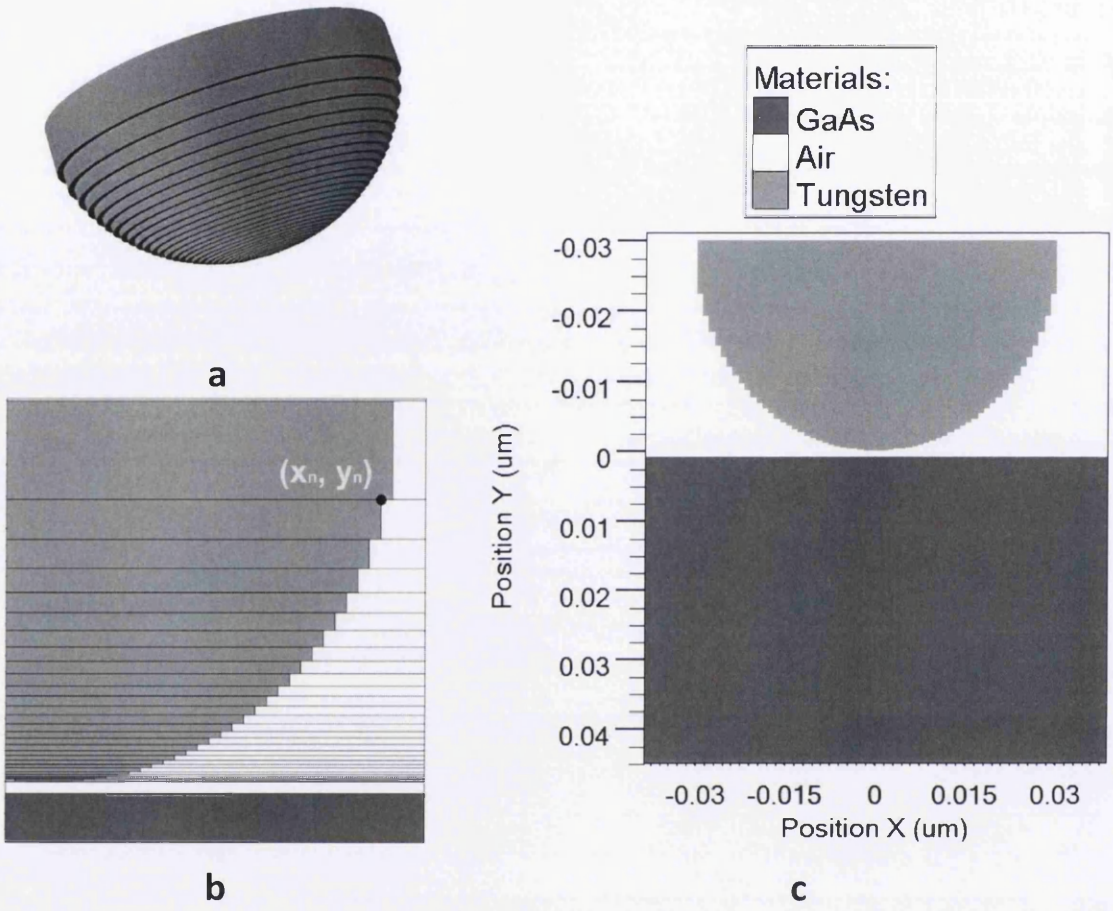

Figure 3.4.1. (a) 3D representation of the SPM tip. (b) Geometry approximation of the tip using 30 sublayers. (c) 2D cutline through the final structure of the tip-sample system.

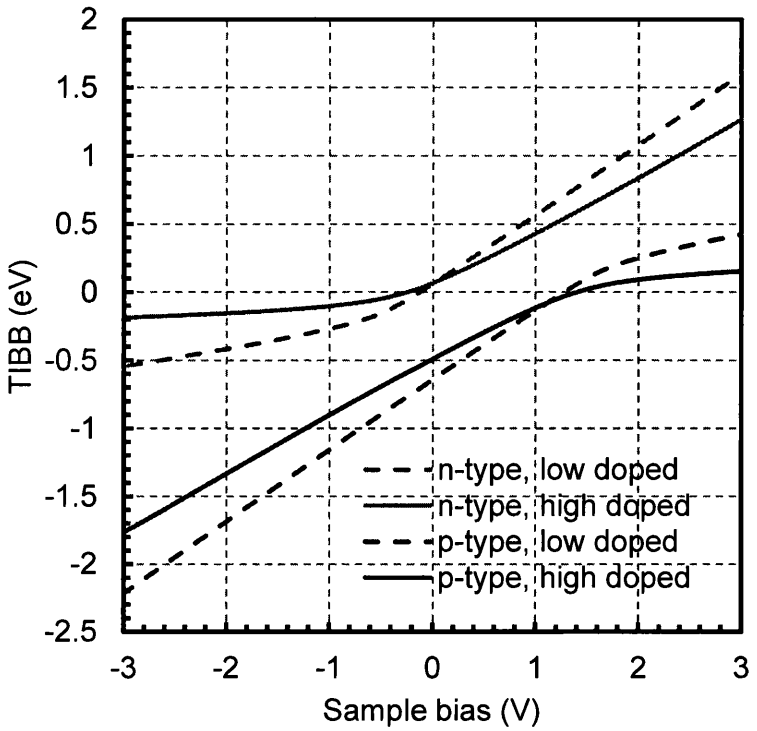

Figure 3.4.2. Tip induced band bending (TIBB) for low doped (10^{16} cm^{-3}) and high doped (10^{18} cm^{-3}) GaAs with 30 nm tip radius and 1 nm tip-sample separation.

3.5 Comparison with experimental data and other models

Figure 3.5.1 compares the experimental data obtained from the STM measurements performed on *p*-type GaAs [30] with the simulated results from our approach and from the latest version of software Semitip 6 [47]. The Semitip model [48] is based on the Bardeen formalism using the Tersoff and Hamann approximation [49]. The Bardeen model [25] assumes that the tunnelling current can be obtained from the difference in electron scattering rates of the tip and the semiconductor sample, which is equal to the number of sample or tip states weighted by their occupation probabilities, multiplied by their charge [50]. However, this model does not account for the effect of the image force, which is known to reduce the potential barrier for tunnelling and thus increase the current. Therefore, the tunnelling current obtained directly from the Semitip simulations was multiplied by three

orders of magnitude to obtain an agreement with the experiment [30], [38], [39]. We investigate the effect of image force on conduction and valence bands in detail in Section 3.6.

A comparison with experimental results has been carried out using the following parameters taken from the Ref. [30] in order to have the same conditions: a tip radius R=30 nm, a tip-sample separation s=0.9 nm, a contact potential $\Delta\varphi$=-1.4 eV, and 0.7 nm^2 area of the tunnel junction [30]. Figure 3.5.1 compares the current spectra as a function of applied tip bias for the latest version of Semitip 6 software and our model created

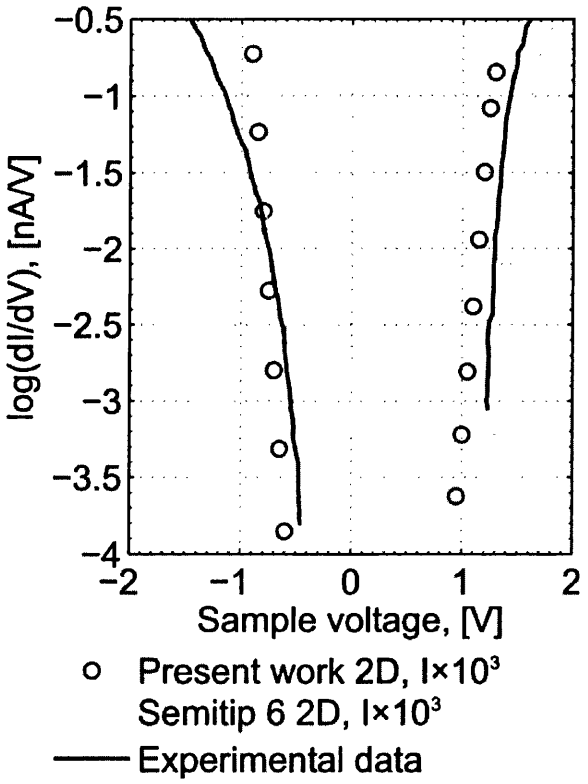

Figure 3.5.1 Simulation results from Semitip 6 model and present work compared against experimental spectra for p-GaAs with a doping concentration of $N_A = 10^{18}$ cm-3 [30]. Simulations were made with the same set of parameters to study the difference in the models. The current was increased by three orders of magnitude following procedure from Semitip 6 to account for the image charge induced barrier lowering. Both models can be fitted exactly to the experimental data with another set of the parameters for the of contact potential and tip-sample separation.

with the same set of free parameters to explain the differences in the models.

One of the differences between the 2D models arises in the calculation of the magnitude of the tip-induced band bending. The surface potential energy directly under the tip apex was compared with the potential energy far inside the semiconductor for voltages from -2 V to +2 V as illustrated in Figure 3.5.2 for both Semitip 6 and our model in 2D and 3D. Both reproduce a large tip-induced band bending when the semiconductor is in depletion (negative sample voltage for *p*-type material) and a small band bending due to the screening effect of the surface charge density when the semiconductor is in accumulation (positive sample voltage for *p*-type material). The difference in the potential computation for the valence band is one of the sources of the mismatch in the 2D models in Figure 3.5.1. This is due to the fact that a 2D model used by Atlas assumes that a 2D tip shape is extended in the 3rd direction, while Semitip 6 2D model uses an azimuthal symmetry in cylindrical coordinates. When a full 3D model is used than the tip-induced band bending agrees with that of Semitip 6 model calculations as shown in Figure 3.5.2.

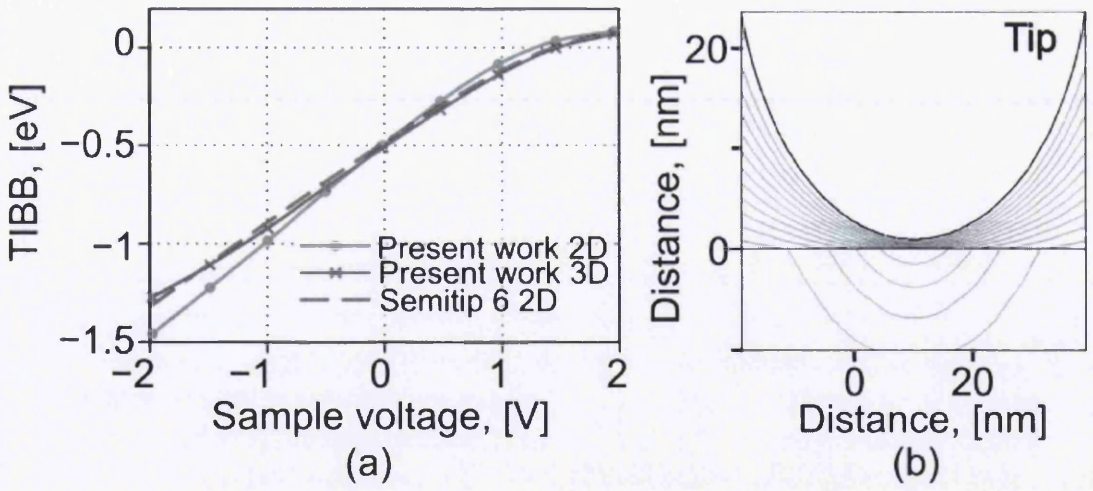

Figure 3.5.2 Comparison of tip-induced band bending models for present work and the Semitip 6 model. (b) Potential distribution directly under the tip apex when no bias voltage is applied, contours are displaced by 0.1 V.

The material parameters used in our simulations differ from those used by Feenstra. In Semitip 6, heavy hole effective mass m_{hh}=0.643m_o, light hole effective mass m_{lh}=0.081m_o, and split-off effective mass m_{so}=0.172m_o. The material parameters for GaAs used in the present work are summarized in Table 2.3.1. However, when the parameters from Table 2.3.1 were used in Semitip 6, we have found no significant difference in results for the TIBB.

3.6 Image force simulations

The image force alternates the shape and lowers an ideal trapezoidal tunnelling barrier

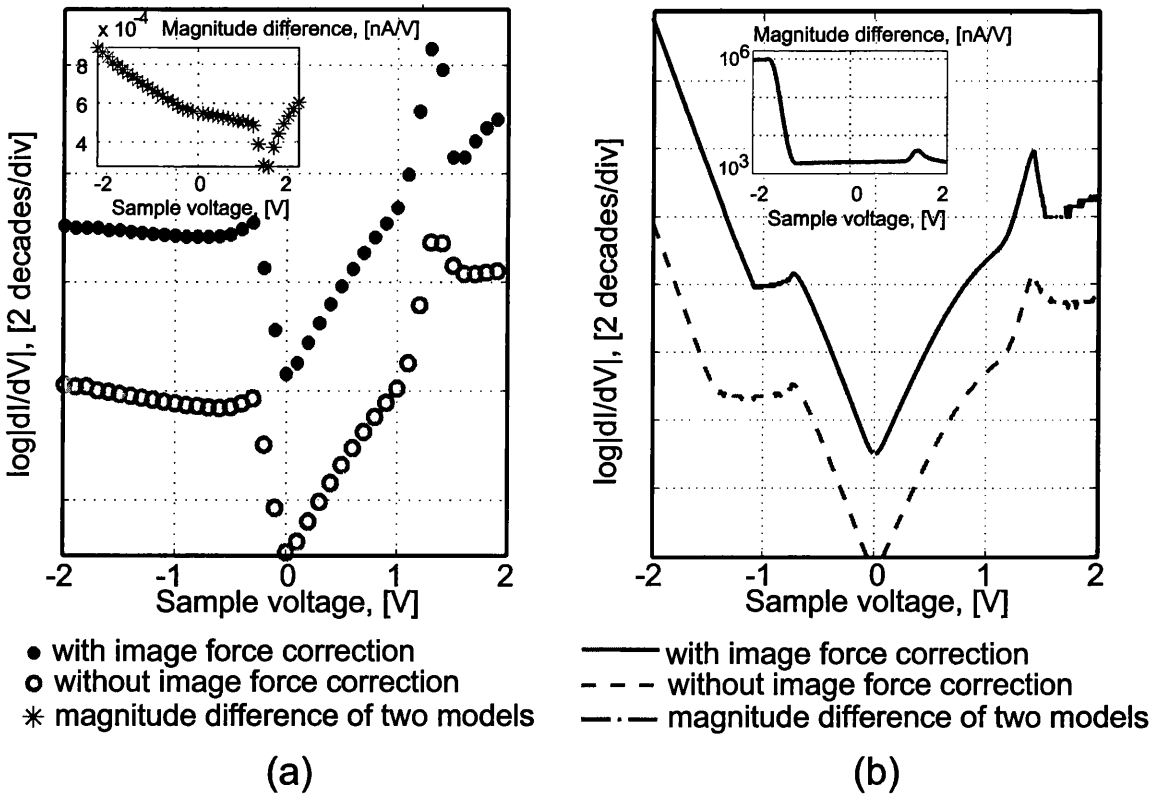

Figure 3.6.1. dI/dV spectra obtained when no image force correction is included in the model and when the image force correction is included for (a) rectangular tip shape and (b) circular tip shape. The insets show the difference in the currents when the image force correction is included or excluded.

and thus increases the tunnelling current. One approximation to avoid performing computations of this complex, image force affected barrier shape is to introduce a constant magnitude scaling factor for the tunnelling current which mimics the lowering of the height of triangular barrier, as it was used for Semitip 6 in previous section [30], [38], [39]. In case of the ultra-thin gate dielectrics in metal-oxide-semiconductor structures the common approximation of the image force [51], [52] brakes as shown by Schenk [40]. Because the distance between the tip and the semiconductor surface is less than 1 nanometre and vacuum/air can be considered as a special type of dielectric, we use the Schenk tunnelling model which includes image force in the case of STM in vacuum/air.

Figure 3.6.1 shows spectra with and without the image force correction for a rectangular tip shape, similar to Figure 3.2.1(a) but with a width of 0.7 nm. Figure 3.2.1(b) presents the same result but for simplified circular tip shape with a radius of 30 nm, similar to Figure 3.2.1 (c). In the both cases, the tip is separated by 0.9 nm from the *p*-GaAs surface with a doping concentration $N_A = 10^{18}$ cm^{-3}. There is a consistent four orders of magnitude increase in tunnelling current when the correction is included for the rectangular tip shape (see Figure 3.6.1 (a)). Alternation of the tunnelling current through the conduction band (CB) due to the effect of image force is well known [38] so the Semitip 6 model used a constant scaling factor for the tunnelling current considering the correction for CB only. We include the image force correction also for valence band (VB). This results in a very different impact on the CB and VB tunnelling currents for every bias point. With the same model applied to a circular tip, conduction band tunnelling current is found to be three orders of magnitude larger and the valence band tunnelling current six orders larger (see Figure 3.6.1 (b)). The magnitude difference will change with the different structure parameters, tip shape, and semiconductor materials. The difference observed in the image force correction for circular and rectangular tip shapes might have a serious implication on the tunnelling current magnitude for models where a circular tip shape is approximated by a staircase, which is commonly used in the modelling of atomic force microscopy and Kelvin probe microscopy measurements [7], [8].

3.7 Band gap simulations for InP, AlGaAs, InGaAs and GaP

The simulation methodology was applied to $Al_{0.3}Ga_{0.7}As$, $In_{0.53}Ga_{0.47}As$ and GaP, all with a doping concentration of $N_D = 10^{16}$ cm^{-3}. All material parameters used in the simulations can be found in Table 2.3.1 and 2.3.2. These simulations used a 70 nm tip radius, 1 nm tip-sample separation and a tip work function of 4.7 eV. For this intermediate *n*-type doping, Figure 3.7.1 shows that modelled band gaps are 2.6 eV for $Al_{0.3}Ga_{0.7}As$ compared to the experimental value of 1.8 eV, and 1.4 eV instead of 0.734 eV for $In_{0.53}Ga_{0.47}As$, both due to tip-induced band bending delaying the onset of increased current. For GaP, the apparent band gap was 1.7 eV instead of 2.75 eV due to Type I accumulation as seen earlier. A kink-like feature is also seen in the spectrum of GaP at +3 V, when Type II depletion shifts to Type II inversion [13], and tunnelling in to the valence band dominates over tunnelling in to the conduction band.

To demonstrate the modelling for a *p*-type material, *p*-type InP with a doping concentration of $N_A = 10^{12}$ cm^{-3} is shown in Figure 3.7.2 using the same tip-sample structure parameters and a tip work function of 5 eV. The observed band gap of 2.85 eV is larger than the experimental band gap of 1.42 eV due to a large amount of the tip-induced band bending in the low doped material, when the screening effect of the doping is weak.

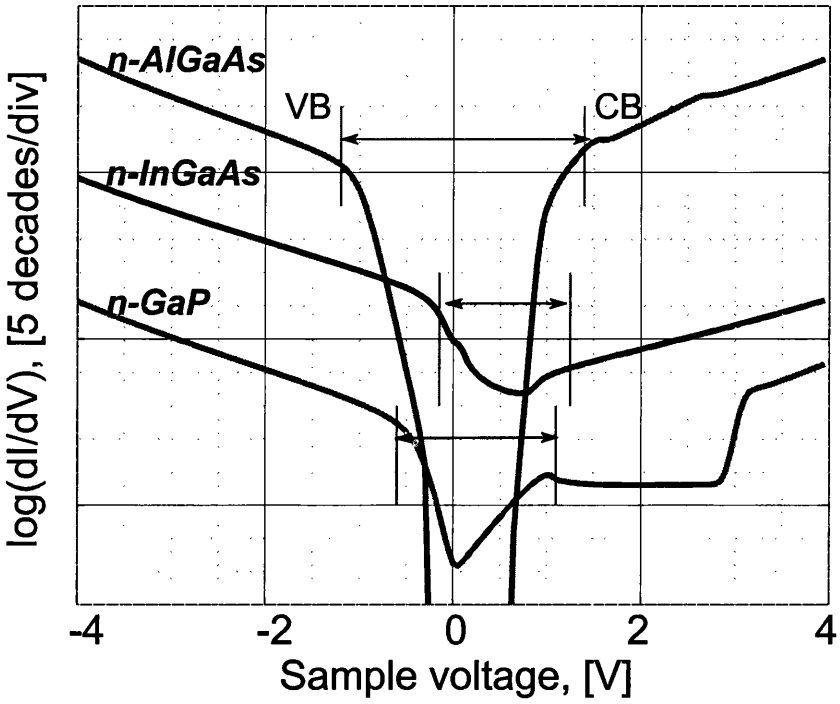

Figure 3.7.1 Tunnelling spectra of the $Al_{0.3}Ga_{0.7}As$, $In_{0.53}Ga_{0.47}As$ and GaP with $N_D = 10^{16}\ cm^{-3}$.

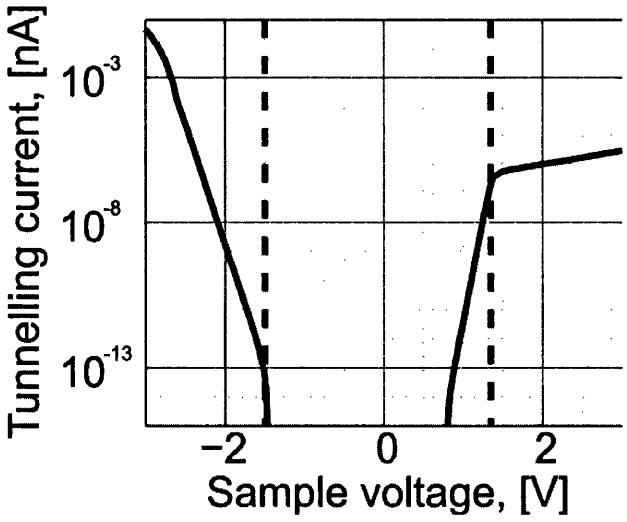

Figure 3.7.2 Simulated tunnelling spectra for p-InP. The vertical dashed lines correspond to the onsets of the larger tunnelling in the conduction and valence bands.

3.8 Role of the oxide in SPM measurements

Scanning probe microscopes offer sub-nanometre measurements and induce local modification of materials and devices. However, probe oxide coatings have been observed to modify the electrical interaction of the probe with the sample. To compare with the simulation results, contact and non-contact spectroscopic measurements of GaAs (110) were performed using scanning tunnelling microscopy. Here, the effects of surface oxide layers on the probe-sample contact type is examined by taking contact and non-contact simulations with the probe oxide in place and controllably changed. The use of both contact and non-contact simulations allows an understanding of the modification of both tunnelling and thermionic emission due to contact type changes caused by the presence of oxide probe

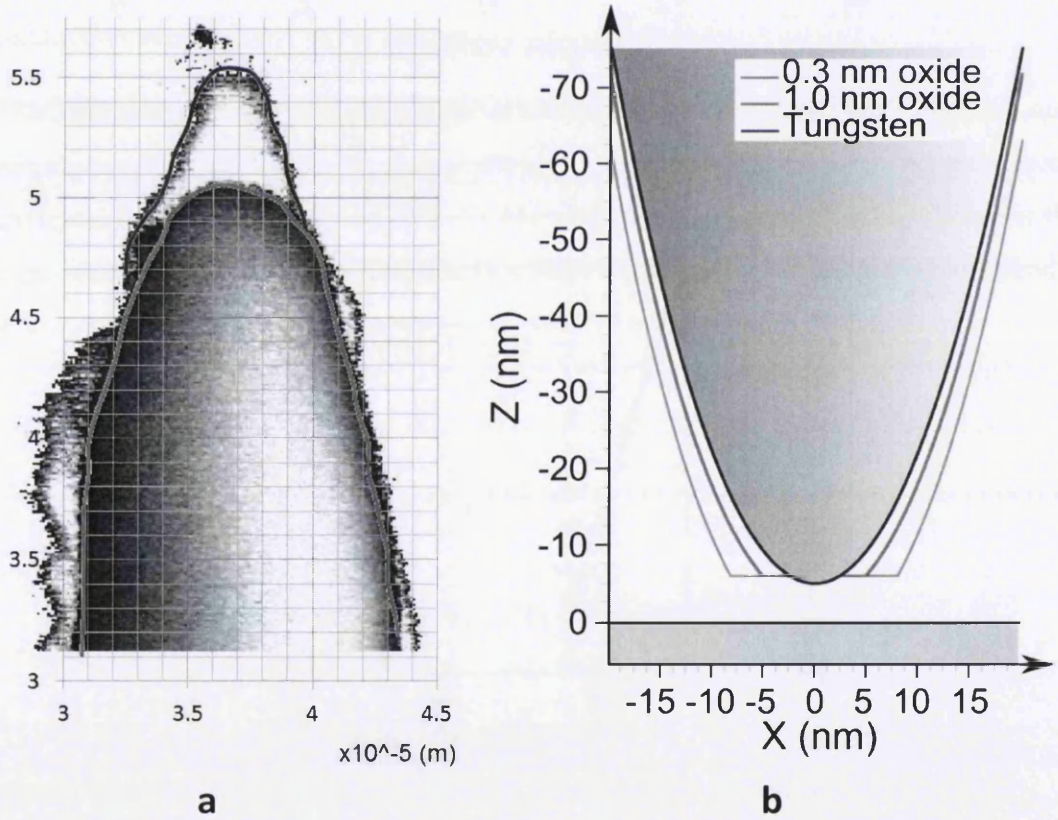

Figure 3.8.1. (a) Tip geometry approximation using an overlay of a scanning electron microscope image of clean tip and tip with oxide layer. (b) Physical model of the tip, with an exposed metal apex and oxide coated shaft.

contamination, which both play a role in contact measurements.

Simulated structures were prepared and measured by other researchers. Tips were electrochemically etched from 0.25 mm diameter polycrystalline W wire in 2M KOH in a method similar to Ibe [53]. The tungsten to oxygen ratio (W:O) was measured to verify the controllable reduction of surface oxide by calibrated direct current annealing using an Hitachi S-4800 field emission scanning electron microscope (SEM) with an Oxford Instruments X-Max 50 analyzer to carry out EDX [54]. N-type GaAs doped 9.2×10^{17} cm^{-3} with Zn were cleaved in UHV to expose an atomically flat (110) surface [2].

WO_3, the oxide layer formed on the tip, is a wide band gap semiconductor. For un-cleaned tips, if tunnelling was taking place through the oxide at the tip apex, the WO_3 band structure would convolve with the sample band structure to produce spectra with a much wider apparent band gap. This is the opposite of what we observe experimentally. The simulations show that the tip apex behaves predominantly as a metal. An overlay of SEM images of the tip before and after annealing illustrated in Figure 3.8.1(a) gives an estimate of 50 nm layer of the oxide at the tip apex. This would make the tunnelling process at the bias range of ±2 V impossible. Therefore, we find that during the initial tip approach the probe moves close enough to the sample surface to mechanically remove the oxide coating before tunnelling initiates through the exposed metal tip apex. The tip was cleaned of the WO_3 layer by using a direct current annealing at 1714 K which is high enough to sublimate the oxide and is low enough to prevent blunting of the tip. However, a residual oxide layer remains [54]. In line with this, and our SEM and EDX results, we construct a model of a 32 nm diameter tip with a 1 nm WO_3 layer around the shank of the probe. After annealing, the tip shaft oxide is reduced to 0.3 nm with the tip apex exposed for both. This structure used for all simulations is shown in Figure 3.8.1(b).

The effect of the different oxide geometry is demonstrated in Figure 3.8.2. In the simulation n-type GaAs sample with doping concentration of 10^{18} cm^{-3} is considered. Metal tip is kept above the sample surface at a constant height of 1.5 nm. Three different tip geometries were simulated: tip without oxide, tip with 1 nm oxide coated shaft and tip completely coated in 1 nm oxide including a tip apex (Figure 3.8.2(a)). The difference in the differential conductance in Figure 3.8.2(b) for the tip without oxide and with oxide coated

shaft will be explained in the later chapters. Tip with oxide coated apex will be more conductive because WO_3 wide band gap semiconductor layer around the apex of the probe allows an additional tunnelling current through the conducting layer. This will result in the change of simulated differential conductance of the tip with oxide coated apex in comparison to the tip with oxide coated shaft.

3.8.1 Role of the oxide on a probe in non-contact measurements

Results for non-contact measurements were found to be dependent on doping concentration. We used GaAs doped to 9.2×10^{17} cm^{-3} and 1.7×10^{16} cm^{-3} with Zn. For the high doped sample, measurement results in Figure 3.8.3 (a) demonstrate the shift of the conduction band profile at the positive gap voltages after probe shank oxide removal. The

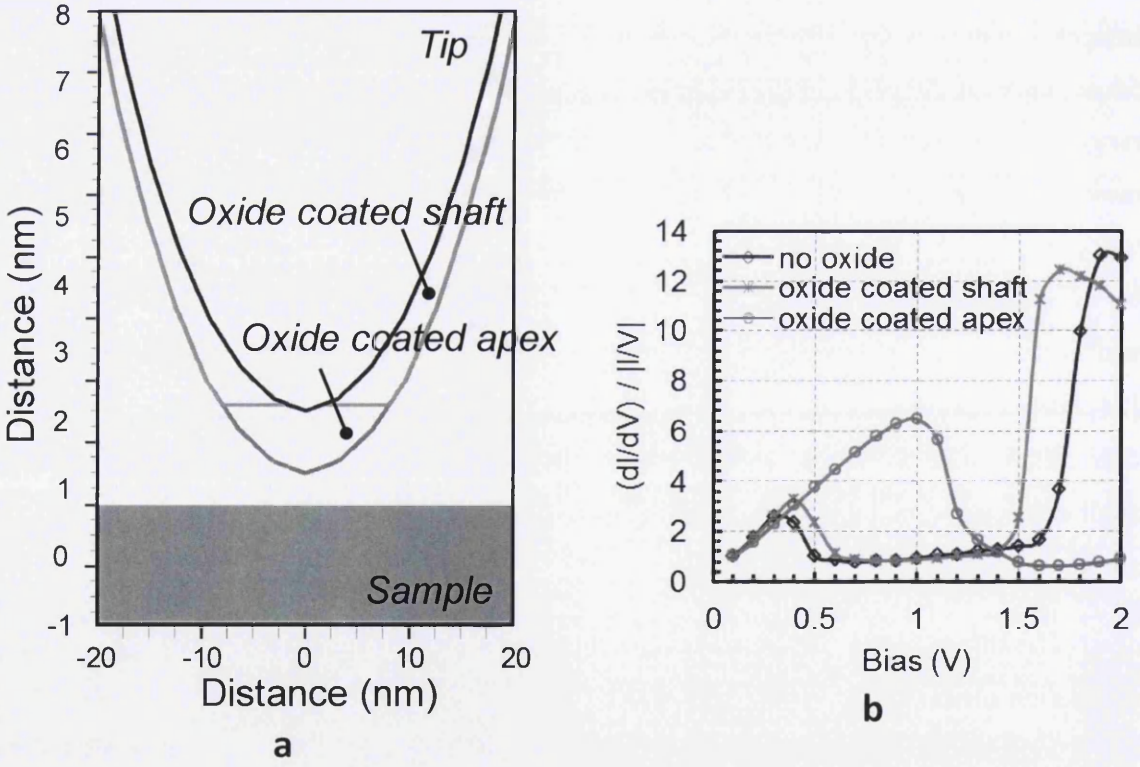

Figure 3.8.2 (a) Simulated tip geometries without oxide, with oxide coated tip shaft and when tip is completely coated in oxide including a tip apex. (b) Simulated differential conductance (dI/dV)/|I/V| for three tip structures.

same behaviour is observed in the simulations shown in Figure 3.8.3 (b). Note that no shift is observed in the valence band (negative gap voltages).

Band diagrams for the non-contact case are shown in Figure 3.8.4. Simulations find that the probe field is high enough to induce localised surface depletion (Figure 3.8.4 (a, b)) at high positive voltages. The tip Fermi level will not cross the conduction band profile up until 1.8 V (Figure 3.8.4(b)), but the significant amount of current is observed already at the voltages below 1.8 V. This is due to the transport of carriers through the valence band as seen in Figure 3.8.4(a), which becomes significant for both 1 nm oxide and 0.3 nm oxide structures at 1.4 V.

At the high positive gap voltages, a tip-induced quantum dot-like potential will be created with empty discrete states in the VB above the Fermi level. An example is shown in Figure 3.8.5, where at +1.8 V for the highly doped sample, localised band bending is larger with the thicker probe oxide before annealing. This leads to discrete states above the Fermi level for the thicker oxide seen in Figure 3.8.5 (b) although these states have not yet come in to play for tunnelling, see Figure 3.8.5 (c). As the gap voltage increases, the discrete states are used for tunnelling in the annealed probe but the onset of higher current has already occur for the thicker oxide at a lower gap voltage. The divergence in the formation of the quantum dot-like potential for the 1 nm oxide structure and the 0.3 nm oxide structure explains a shift of the normalised conductivity at the high positive voltages in Figure 3.8.3.

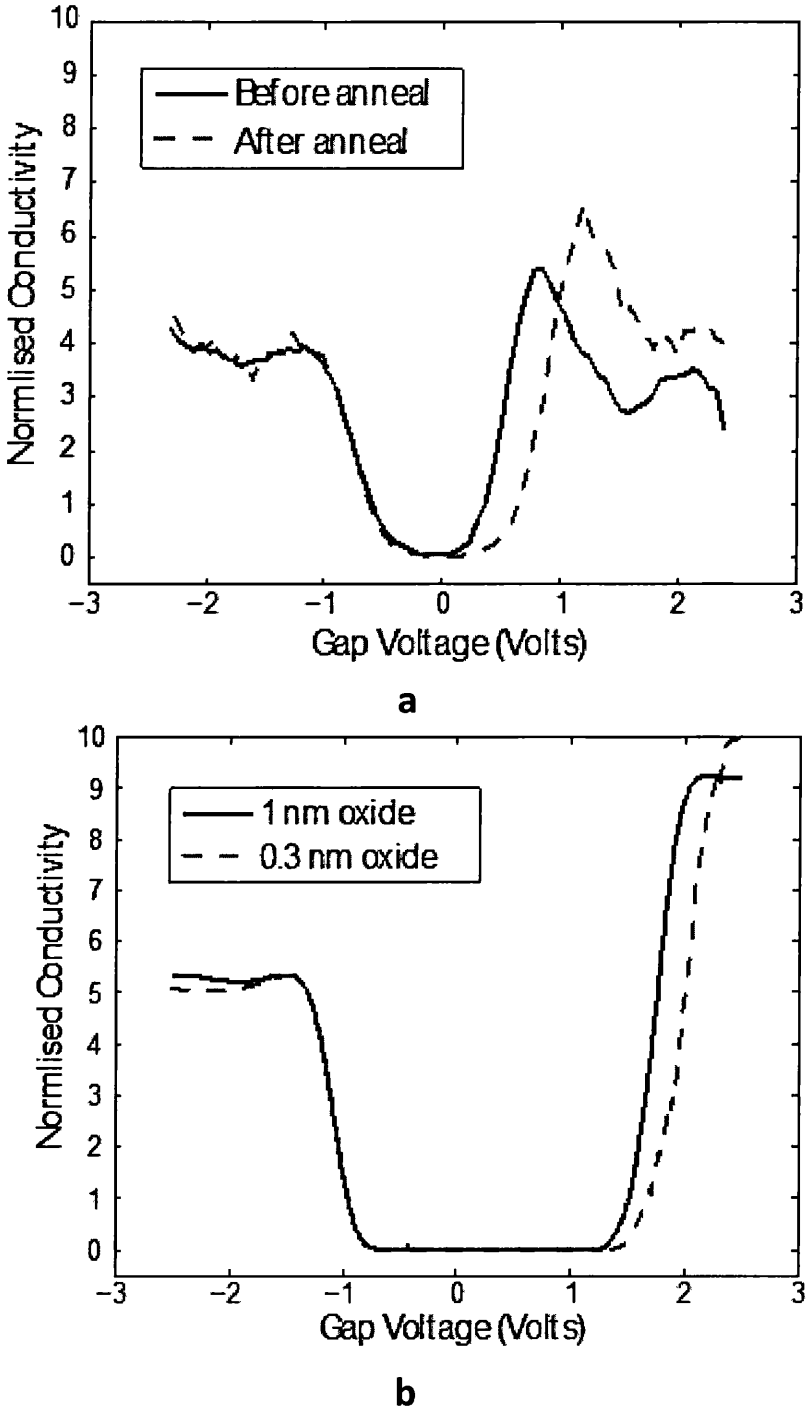

Figure 3.8.3 Normalized conductivity plots with a denominator offset constant c = 0.02 and a rolling average of six for non-contact measurements on highly doped GaAs comparing (a) experimental observations and (b) simulations.

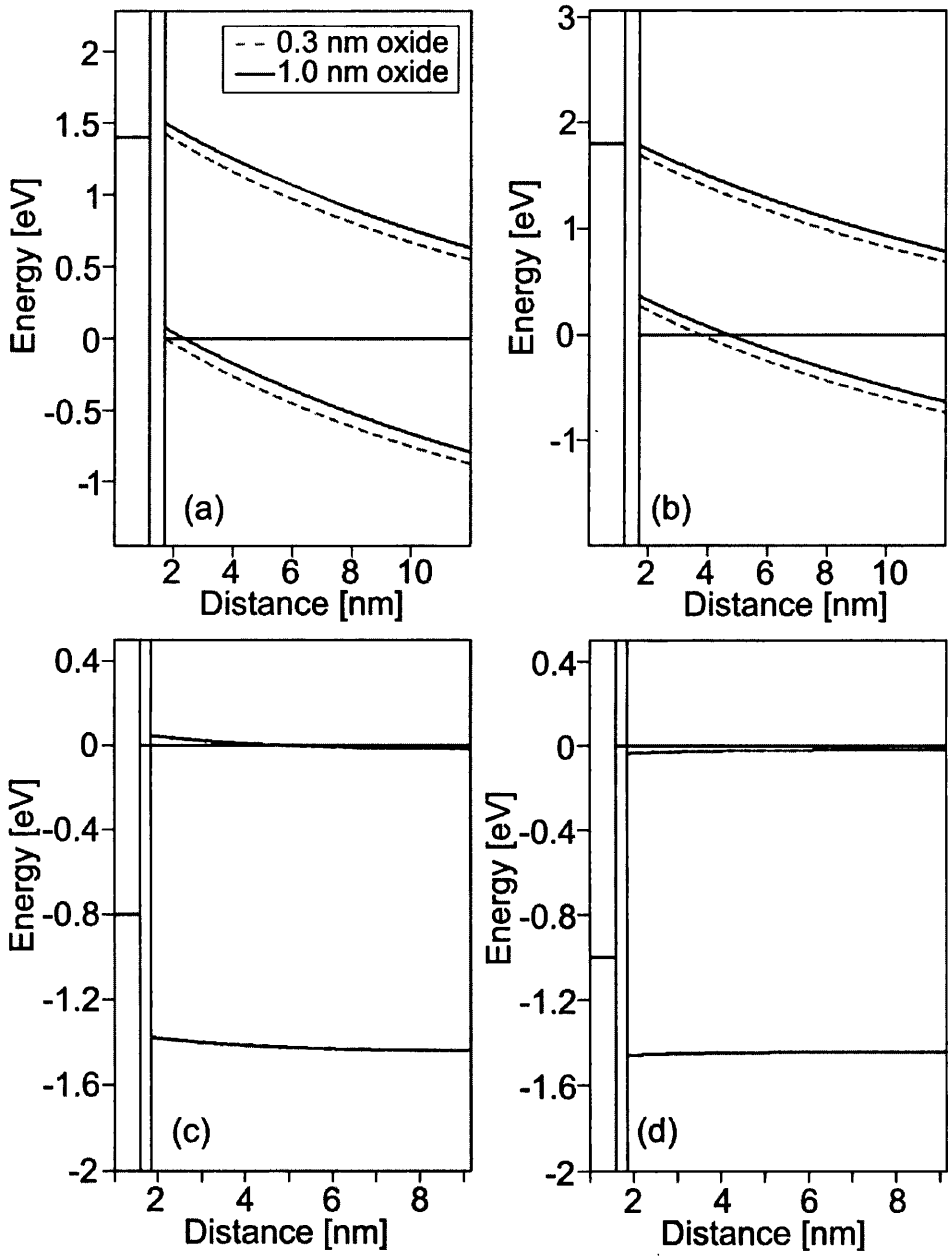

Figure 3.8.4. Band edge profiles of the tip and sample surface for applied gap voltages of a) 1.4 V, b) 1.8 V, c) –0.8 V and d) –1 V for the highly-doped sample.

Similar tip-induced quantum dot-like potential is also formed at negative gap voltages but the increase in conduction band states is not significant enough to introduce the difference in the tunnelling for both oxide structures.

The normalised conductivity in Figure 3.8.3 indicates the valence band edge at ~−0.9 V. The band diagram for the −0.8 V and −1 V in Figure 3.8.4(c) and (d) shows that this increase in the tunnelling current at ~−0.9 V is due to the allowed transport of electrons from the conduction band to the tip. The tip Fermi level will cross the valence band at the higher negative voltages.

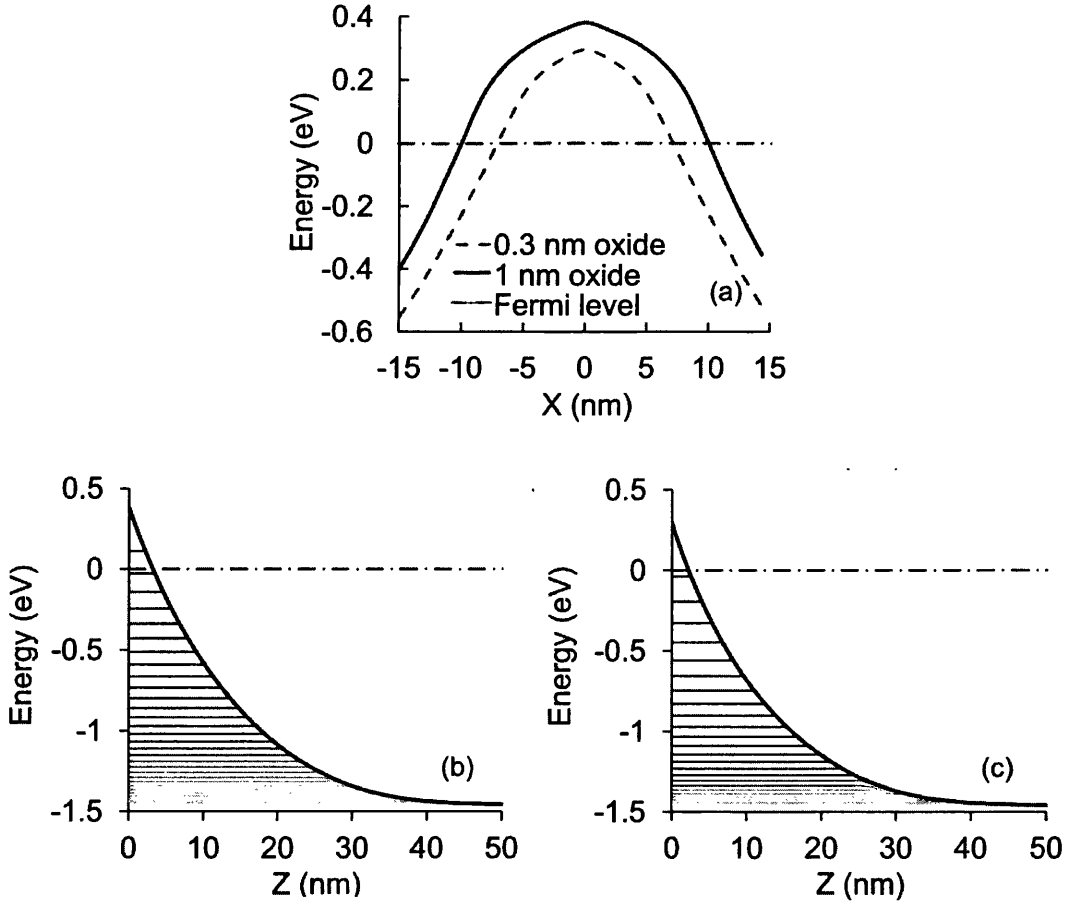

Figure 3.8.5 (a) VB profile under the tip before and after annealing obtained From simulations with the VB profile orthogonal to z-direction directly under the centre of the tip with discrete states for highly doped GaAs at a gap voltage of +1.8 V, (b) before tip annealing, and (c) after annealing.

With negative gap voltage, the sample is in accumulation and the screening effects of the dopants reduce the electrostatic tip-induced band bending. The band diagram in Figure 3.8.4(c) and (d) indicates no change in the accumulation layer with the change in the oxide thickness. This will result in no apparent shift in the tunnelling current at the negative gap voltages shown in normalised conductivity plot in Figure 3.8.3.

For low doped GaAs (Figure 3.8.6), there is a little difference between a tip that has been annealed and a tip that has been not. The reduction in screening in the low doped material gives rise to a long range electrostatic interaction and a high tip-induced band bending for all cases. The only exception is a shoulder centred around 1 V caused but the on-set of the quantum dot-like potential, which appears earlier when the tip oxide has not been reduced as shown in both experiment and simulations.

A shift in the spectra observed by Shen and Clemens may be due to a similar effect as that observed here [43], [44]. In their case, the oxide layer deposited on the InGaAs sample reduces the effect of the electric field and reduces the tip induced band bending which causes the CB edge to shift towards the Fermi level.

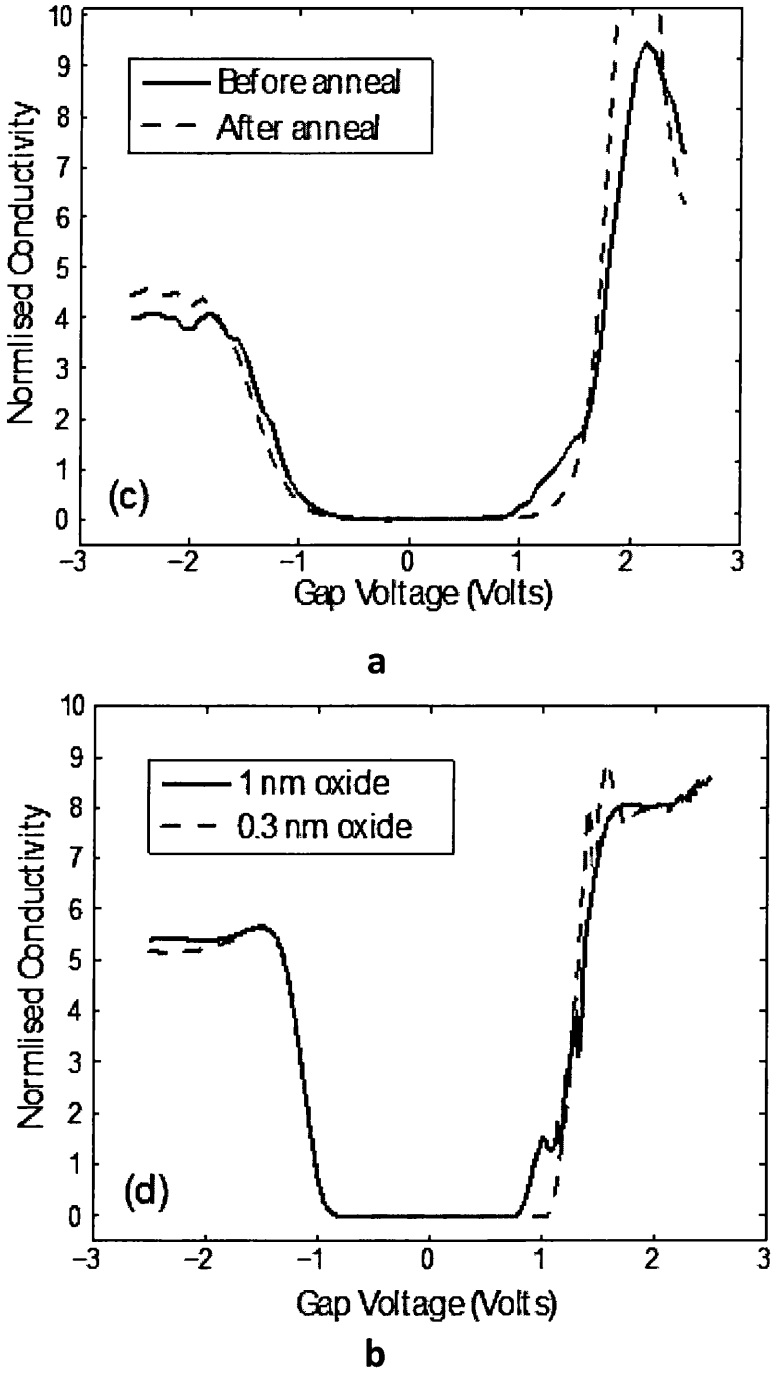

Figure 3.8.6 Normalized conductivity plots with a denominator offset constant c = 0.02 and a rolling average of six for non-contact measurements on low doped GaAs comparing s(a) experiment and (b) simulation.

3.8.2 Role of the oxide on a probe in contact measurements

For contact measurements, the feedback loop was disabled at the 0.5 nA set point and the probe approached incrementally by a distance of dz = 0.1 nm until the spectroscopy was observed to change from tunnelling dominated to contact dominated. This occurred at dz = −0.5 nm and was used for all contact measurements.

Normalized conductivity is an invariant quantity that indicates features of surface state distributions and is calculated using following equation [55]:

$$\frac{(dI/dV)}{(I/V)+c} = \frac{d(\log I)}{d(\log V)} \qquad (3.3)$$

where I is current, V is voltage and c is a small offset to prevent divergence as the denominator goes towards zero. Normalized conductivity results for both experimental and simulation are shown in Figure 3.8.7, where a denominator offset constant of 0.02 was used [55]. The conductivity, both the experimental and in the simulation, increases after the probe shank oxide is reduced. The shift in the conduction band is narrowing the apparent band gap when the oxide is removed and no change in the valence band is observed.

Simulations find that the creation of a near-intimate contact between the tip and the sample forms a Schottky contact with a fixed barrier height for both, as seen in Figure 3.8.8. However, the different oxide profile alters the electrostatic interaction with the sample, changing the shape and the width of the barrier, giving rise to the altered transport shown. At the positive gap voltage of +1 V, the barrier is narrowed when the oxide layer is reduced (Figure 3.8.8(b)). That is why a rapid increased in the tunnelling current for the 0.3 nm oxide structure at the forward bias in Figure 3.8.7 occurs due to the exponential dependence of the tunnelling current on the width of the potential barrier. At the negative gap voltage of −1 V ((Figure 3.8.8(a)), the band profiles for the 0.3 nm oxide and the 1 nm oxide will match due to the dopant screening effect, as seen for the non-contact case in Chapter 3.8.1. At the negative gap voltage, the dominant transport mechanism is electron diffusion from the semiconductor to the metal side, which will not be affected by the change in the oxide layer as seen in Figure 3.8.7. The change in the current behaviour in the forward and the reverse

biases, when tip is in contact with the semiconductor surface, confirms that the barrier for current through the centre two voltage probes in four point probe technique would be non-equally affected by the probe shank oxide.

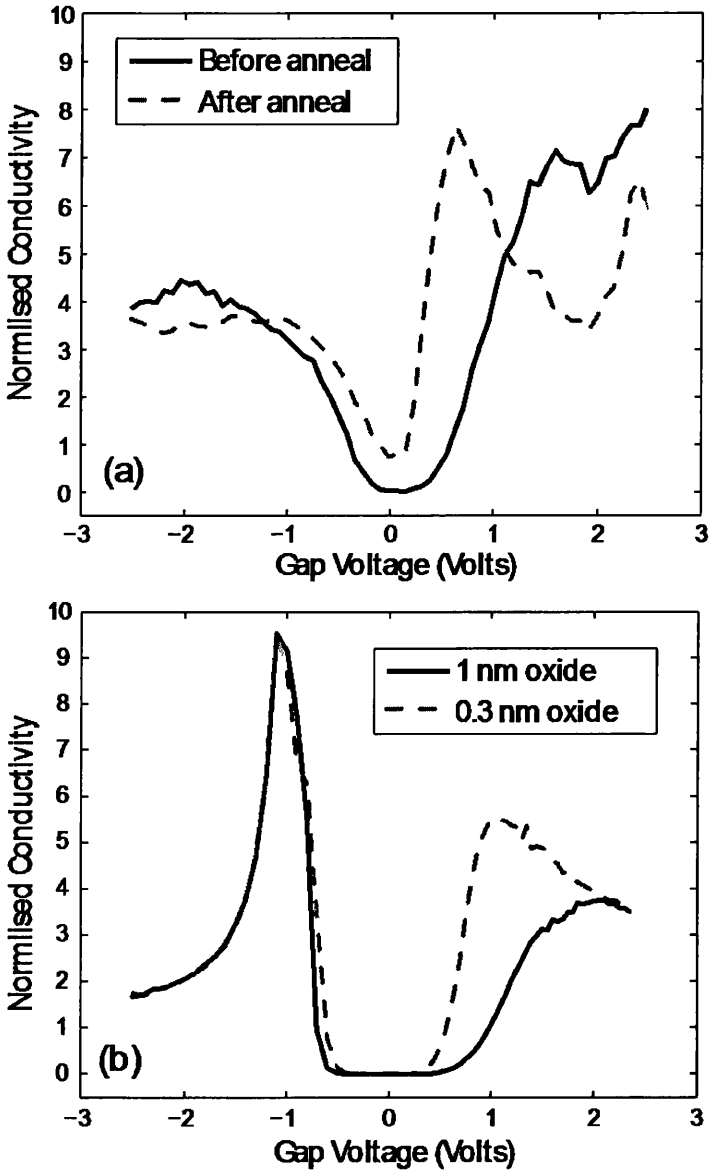

Figure 3.8.7 Normalised conductivity plots with a denominator offset constant c = 0.02 and a rolling average of six for contact measurements on GaAs comparing (a) experimental and (b) simulation results.

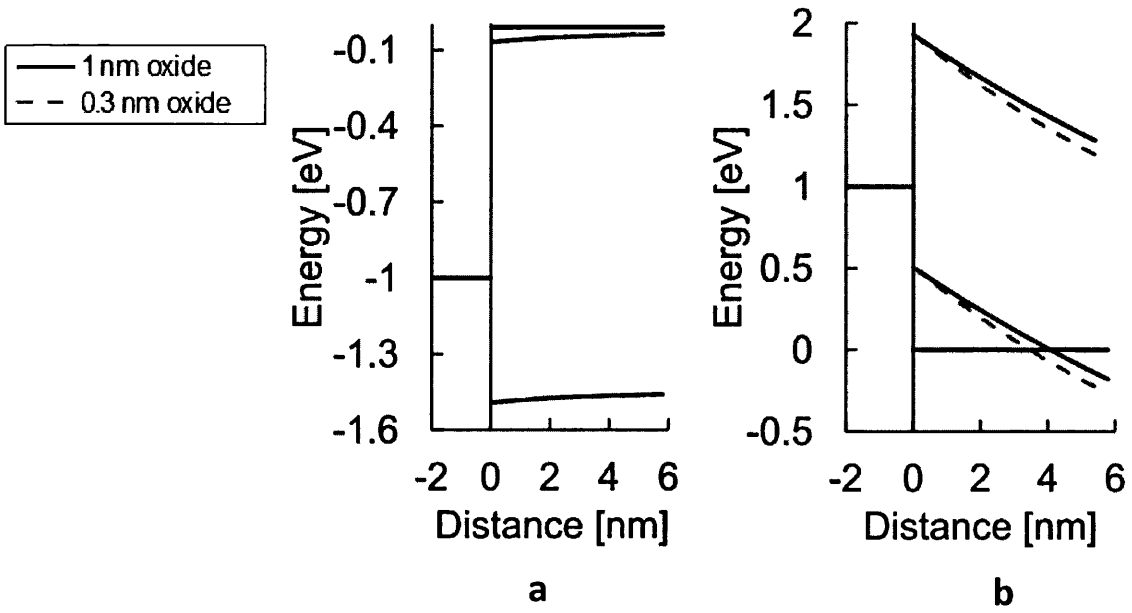

Figure 3.8.8. Band profile for the tip in contact in the sample surface at −1 V gap voltage (a) and +1 V gap voltage (b).

3.9 Summary

An STM and STS simulation methodology based on the Price and Radcliffe tunnelling formalism using image force correction has been developed using Silvaco *ATLAS*. This 2D finite element model was applied to several semiconductor materials to verify its accuracy, with the origin of features in the spectra examined in detail. The simulations confirmed that, at larger doping concentrations, the screening effect of the semiconductor reduces the tip-induced band bending. The tip induced band bending was also tested using a 3D tip geometry.

For *n*-type GaAs, the modelled spectra band gap deviates from the bulk value by only 0.1 eV or 0.7 % which is within the experimental systematic error [46]. At low *n*-type doping concentrations, the screening is weak, and tip-induced band bending causes the apparent band gap to either increase or reduce depending on the tunnelling mechanism. These phenomena well justify the need for STM and STS modelling to accompany the experimental measurements. Our 2D model, which uses a self-consistent Poisson-Schrödinger solution, predicts a larger tip-induced band bending when a sample is in depletion (resulting in a shift of the band onset in the spectra) than that from Semitip 6 2D model, and the same amount of tip-induced band bending when a full 3D model is used.

The image force correction gives a conduction band tunnelling current increase of three orders of magnitude and a valence band tunnelling current increase of six orders when compared to the 'artificial' uniform increase of three orders of magnitude used in Ref. [30]. However, the magnitude change is different for different tip shapes and sample materials.

The work presented in Chapters 3.2-3.7 has led to the following publication: O. Kryvchenkova, R. J. Cobley, and K. Kalna, "Self-consistent modelling of tunnelling spectroscopy on III–V semiconductors," *Appl. Surf. Sci.*, vol. 295, pp. 173–179, Mar. 2014. The work was also presented on the conference: UK Semiconductors, July 2013, Sheffield UK, O. Kryvchenkova, K. Kalna, R. J. Cobley, "Modelling Scanning Probe Interactions using a Finite Element Device Simulator".

The presence of the oxide on the shank of the probe alters the contact behaviour in contact and non-contact measurements. This has implications for all nanoscale surface probe measurements, and macroscopic 4PP, both in air and vacuum. The work presented in Chapter 3.8 is in preparation for a publication: C. J. Barnett, O. Kryvchenkova, L. S. J. Wilson, T. G. G. Maffeis, K. Kalna and R. J. Cobley, "The role of probe oxide in local surface conductivity measurements" aimed for *Physical Review B*.

Finally, our STM model developed within a commercial simulation tool offers several advantages over other STM models. These advantages include i) the ability to use any realistic tip shape, ii) to include full device transport models for SPM on devices, and iii) to model spectra from SPM on powered devices. The model can also account for surface states, and can readily be extended to other SPM techniques.

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Chapter 4 Results of modelling of ZnO nanowires

4.1 Introduction

In any metal-semiconductor contact, the electrical conductivity is determined by the intrinsic properties of the constituents and, more importantly, the interface they form [1]. At the micro-scale, the size of the contact (or interface area) has little effect on the transport mechanisms, whilst at the nanoscale, dipole-like electrostatic fields replace uniform parallel fields, leading to electrical behaviour that is poorly understood [2]. Indeed, some prototype devices such as lasers [3] and nanogenerators [4] have been demonstrated in laboratories, but selecting Ohmic- or Schottky-like behaviour is challenging for repetitive manufacture[5].

Some experimental evidence demonstrates a size-dependant Schottky- or Ohmic-like behaviour in the metal-semiconductor nanostructures [6]–[8]. Other works, extended to more challenging interfaces at the tips of free standing semiconductor nanowires, have shown promising results for different metal contacts deposited onto ZnO nanowires [9], [10] providing a range of rectifying and Ohmic behaviour. In addition, the contact formatted from Au catalyst particles, used to grow a range of nanowires, have demonstrated Ohmic behaviour [11] for InAs and InP nanowires, yet rectifying behaviour on Ge nanowires [12]. It is clear that a range of electrical behaviour is possible for nanoscale metal contacts. However, there is no generalized understanding of how to actively control the interface barrier and how the transport properties are related to the size of the metal or nanowire [8], [12]–[14]. In the present chapter this problem is analysed using a full 3D simulation and verified against the experimental results. The findings reveal a mechanism to control the conductivity of metal-nanowire interfaces.

The current-voltage (I-V) measurements in Chapter 4.2 reveal size dependent properties that can be used to create a spectrum of electrical behaviour from Schottky to Ohmic, without

the need of any sample processing, nanowire samples were prepared and measured by other researchers. To explain the change in the transport properties, full 3D numerical simulations were necessary to reveal the features of the depletion region that allowed enhanced current for the nanoscale contacts, as demonstrated in Chapter 4.3. In this Chapter the simulations demonstrate that neglecting one of the dimensions in calculations, like when using a 2D model, will give a different effect, while the contact phenomena cannot be studied using a 1D modelling. In Chapter 4.4 the complex geometry-dependant behaviour of ZnO nanowires is demonstrated. The important conclusion from the work is that the conductivity is not just determined by contact size as demonstrated in Chapter 4.5, but also by the size of the interface in relation to the nanowire diameter below a critical dimensional ratio as seen in Chapter 4.6. This study has implications for all nanodevices where the semiconductor width approaches the size of the metal interface. This work was prepared for the following publication: Alex M. Lord, Thierry G. Maffeis, Olga Kryvchenkova, Richard J. Cobley, Karol Kalna, Despoina M. Kepaptsoglou, Quentin M. Ramasse, Alex S. Walton, Michael B. Ward, Jürgen Köble, Steve P. Wilks, "Controlling the electrical transport properties of nanocontacts to nanowires" submitted to *Nano Letters*.

In Chapter 4.7 describes an essential role of current crowding in ZnO NWs which increases parasitic resistance at the edge of the downscaled contacts. The current crowding effect was reported earlier in side-bonded nanostructures like carbon nanotubes [15], [16], ZnO, GaN and Si nanowires [17], and graphene-metal contacts [18]. Current crowding is known to result in a local temperature rise at the metal-semiconductor interface which can lead to device failure [18],[19]. The work was presented at ANM 2014, Fifth International Conference on Advanced Nanomaterials, July 2014, Aveiro, Portugal and was accepted for the publication in the *Materials Today Proceedings* entitled O. Kryvchenkova, K. Kalna, R. J. Cobley, "The Current Crowding Effect in ZnO Nanowires with an End-Bonded Metal Contact". It was also presented on the UK Semiconductors 2014, July 2014, Sheffield UK entitled O. Kryvchenkova, K. Kalna, R. J. Cobley, "Modelling Current Crowding Effect in the ZnO Nanowires".

Using a 1D electrothermal model, LeBlanc *et al* [17] demonstrated that for ZnO NWs with side-bonded Ohmic contacts, the peak of the temperature rise will occur at the metal-

nanowire interface. Post-measurement images of the ZnO NW with side-bonded Ti/Ag contacts indicated melting of the metal electrode, limiting the operational range of these devices. Leonard *et al.* [20] reported the temperature distribution through the NW length with a fixed contact temperature. This simulation predicted heat loss to the environment due to the high surface to volume ratio of the NWs.

In Chapter 4.8, we study the effect of current crowding on the temperature profile along the nanowire and around the metal contact for the end-bonded ZnO NWs with Schottky contacts. A full 3D simulation model considers carrier transport of electrons and holes self-consistently coupled with thermal flow [21]. Since the transport parameters depend on the lattice temperature, lattice heating and cooling due to the carrier generation and recombination, Joule heating and Peltier-Thomson effects are also included [21]. Finally, unlike in previous works [17], [20], the thermal modelling considers temperature dependent thermal conductivity model [22] and heat capacity model [23] for ZnO. This work was presented on ASDAM 2014, The Tenth International Conference on Advanced Semiconductor Devices and Microsystems, October, 2014, Smolenice, Slovakia and accepted for the publication in the conference proceeding entitled Kryvchenkova, O., Kalna, K., Cobley, R.J., "Modelling heating effects due to current crowding in ZnO nanowires with end-bonded metal contacts," *Advanced Semiconductor Devices & Microsystems (ASDAM), 2014 10th International Conference on* , vol., no., pp.1,4, 20-22 Oct. 2014.

In Chapter 4.9 the effect of the surface charge on the electrical properties of ZnO nanowires was studied in detail. The measurement data was obtained from the hydrothermally grown ZnO nanowires [24], [25]. The electrical measurement performed using two metal probes demonstrated a change in the surface conductivity after the argon ion bombardment [26] of the surface was performed. The full 3D model of the tip on the nanowire surface is used to explain the change in the electrical behaviour due to the presence of the surface charge.

The work in this chapter was also presented by the author at an invited talk in the National Physical Laboratory, NPL, London, October 2014.

4.2 Experimental measurement of the current

ZnO nanowires of diameters ranging from 15 to 80 nm were fabricated by chemical vapour deposition using Au catalyst particles to initiate their vertical growth on α-Al_2O_3 substrate [27]. This particular fabrication method can lead to contamination of the nanowire by the catalyst atoms [28]–[30]. Such contamination can subsequently produce variability in electrical behaviour [1], [31]. However, this can be discounted as the Au catalysed growth of ZnO exhibits no such alloying due to the low solubility of the solid catalyst material in the nanowire during and after growth [32]–[34]. However, the structural and chemical integrity of the metal-nanowire interface are also known to play a key role in perturbing the resultant transport properties [1], [31], [35], [36].

Samples in this work were prepared and measured by other researchers. After growth, close inspection of the nanowires (Figure 4.2.1(a) and (b)) using scanning backscattered electron (BSE) imaging and transmission (TEM) electron microscopy showed that for similar size nanowires, a variation in metal particle size, and hence interface size, was evident. An interface image (Figure 4.2.1(c)) and corresponding line profile (Figure 4.2.1(d)) were recorded using an aberration-corrected Nion UltraSTEM microscope with a probe size of 0.8Å and high angle annular dark field (HAADF) detector. This revealed the period atomic columns and the abruptness of the junction as indicated by the clear discontinuity in contrast on either side of the junction. Importantly, no Au atoms were detected in the nanowire material near the interface. Hence, it can be stated that the Au-ZnO nanowire interface is clean, ordered and intimate, an ideal test bed for understanding the intrinsic electrical properties of particle-nanowire contacts.

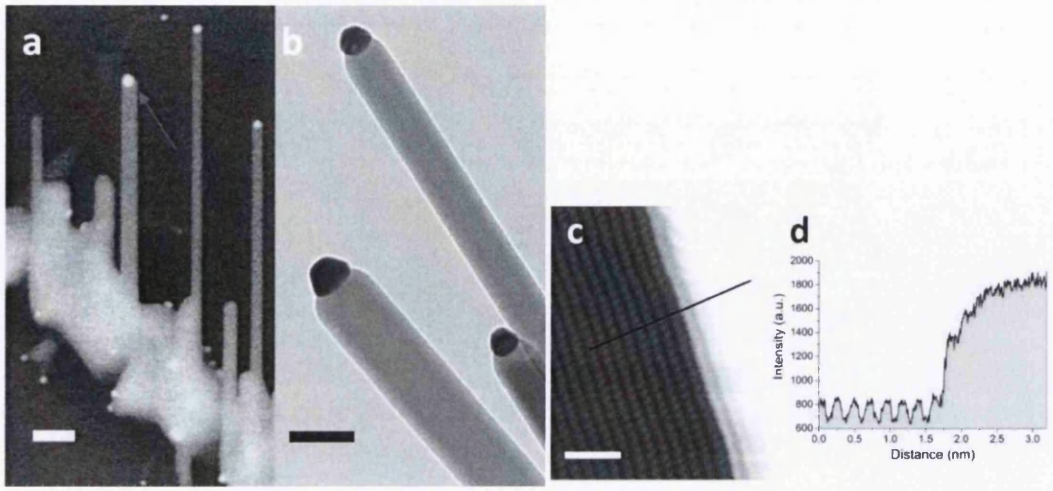

Figure 4.2.1. Electron microscopy images of ZnO nanowires with the Au catalyst particle interface. (a) Backscattered electron image showing as-grown nanowire with Au catalyst particle clearly visible at the nanowire tip, scale 200 nm. The red arrow indicates the 59 nm contact measured with the local multi-probe technique. (b) TEM image of several ZnO nanowires with a variation in Au catalyst particle size that is independent of nanowire diameter, scale 30 nm. (c) Unprocessed aberration-corrected HAADF image of the Au-ZnO nanowire interface with the beam aligned along the $[01\bar{1}0]$ *ZnO zone axis showing the abrupt interface, scale 1 nm. (d) Line profile of the interface, corresponding to the blue line in (c) showing the expected equal intensity of Zn columns with the sudden intensity increase indicating an abrupt interface and no interfacial layer. The first Au column appears less intense due to the Au particle curvature as presented in Ref. [10].*

Accurately measuring the electrical properties of contacts to individual nanowires requires the use of more than one probe [10], [37] overcoming the limitations of single probe techniques such as AFM and STM. Here the same technique is employed based on two scanning probes, one forming an Ohmic contact to the side of the nanowire whilst the other probe was placed in contact with the Au particle. This enabled a single Au-ZnO contact to be isolated in the as-grown configuration, providing a measurement of the metal-nanowire interface, free from any extraneous affects associated with the substrate or nanowire substrate junction which is essential to ensure accurate measurement [37].

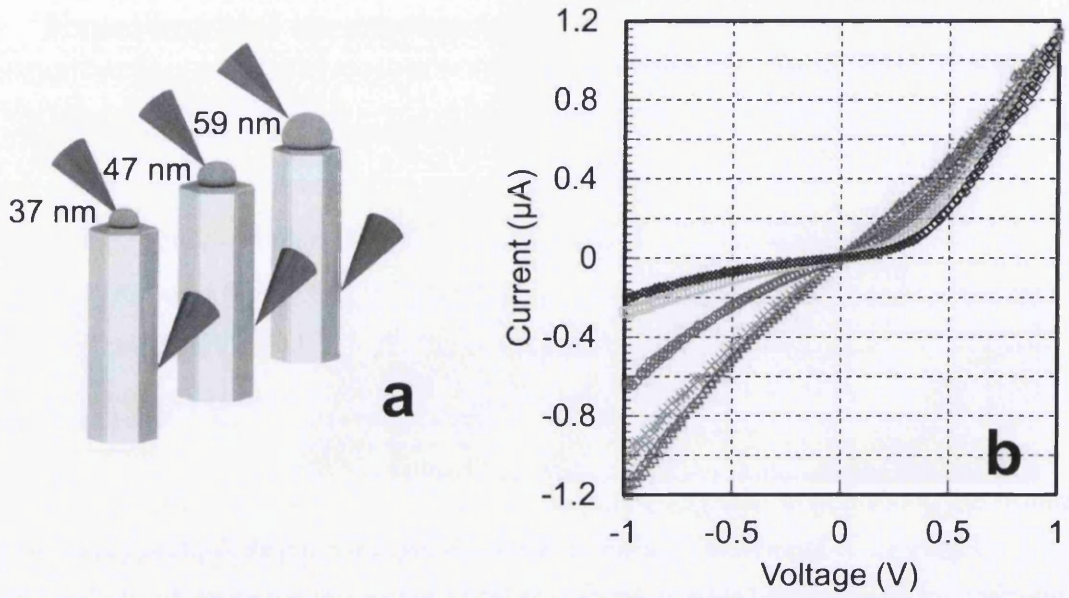

Figure 4.2.2 (a) A schematic diagram of the experimental setup for the two-probe I-V measurements of Au catalysed ZnO nanowires. The measurements (b) correspond to nanowires with a diameter of 72 nm (blue, ◊), 70 nm (yellow, □), 73 nm (red, ○), 73 nm (green, ×) and 79 nm (purple, △) with Au particles with a diameter of 59 nm, 50 nm, 47 nm, 40 nm and 36 nm, respectively. The measurement data is scaled to the value of current at +1 V for the nanowire with the 59 nm Au particle to account for the variation in series resistance and resistivity between nanowires.

I-V measurements were recorded for nanowires having a variety of contact sizes as depicted in Figure 4.2.2. The voltage triangulation, −1 V to 1 V and 1 V to −1 V, showed no hysteresis for each measurement indicating that the interfaces were stable and unaffected by the high current densities. The results clearly showed the transition from rectifying to Ohmic behaviour as the Au particle diameter decreases (59, 50, 47, 40 and 36 nm on wires with a diameter in the range of 70-79 nm). The measurement data is scaled to the value of the current at +1 V for the nanowire with the 59 nm Au particle to highlight the change in I-V shape as the particle size changes. The absolute current magnitude varies between different nanowires because the spatial separation between the two probes is different, leading to different series resistances. Additionally, it was shown previously that the apparent resistivity of similar size ZnO nanowires from the same growth batch can vary by as much as 2 orders of magnitude, depending on the surface coverage of ionized oxygen species [33].

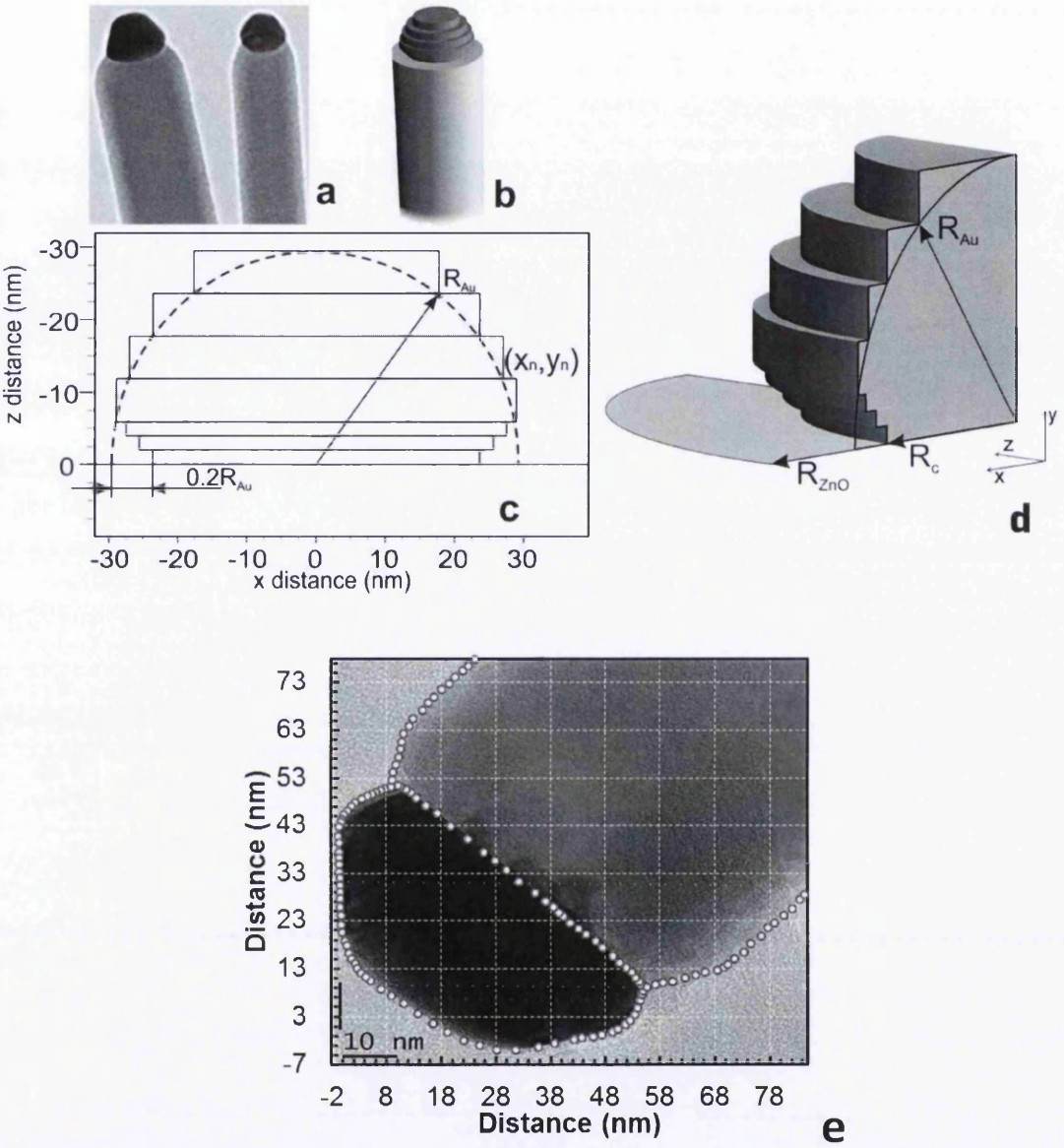

Figure 4.2.3. The Au contact shape approximated in the simulations. (a) TEM image of the ZnO nanowires aligned on the $[1\bar{2}10]$ *zone axis with a catalyst particle at the end. (b) 3D model structure of the nanowire and Au particle. (c) Schematic diagram of the geometry used to approximate the Au metal contact and interface geometry. (d) Cutline through the 3D model structure of Au particle. (e) Extraction of the nanowire geometry from TEM image.*

4.3 Geometry approximation

The Au catalyst particle at the nanowire tip had a distinct shape as shown in Figure 4.2.3(a) which was approximated by a hemisphere of radius R but with a high degree of curvature near the interface producing a small overhang as observed experimentally as in Figure 4.2.3(e) resulting in the full 3D structure in Figure 4.2.3 (b). As demonstrated in Figure 4.2.3(e), sever nanowire structures were analysed to extract the Au particle diameter, nanowire diameter and a curvature near the interface.

Using MATLAB (see Appendix A), the co-ordinates of the structure are generated according to the geometry approximation shown in Figure 4.5.2(c) for the DeckBuild and Atlas simulation tools. A gold contact particle radius R_c is approximated using N_l=4 large cylindrical layers. The height of each layer is R_c/N_l. The coordinates of the n_l large sub-layer (x_n,y_n) can be found as follows:

$$x_n = R_c\sqrt{1-\left(n_l/N_l\right)^2} \tag{4.1}$$

$$y_n = R_c\, n_l/N_l \tag{4.2}$$

For the complex gold shape near metal-semiconductor interface a change in the particle radius by Δ=80% at the base of the contact was approximated using N_s=3 cylindrical sub-layers. The coordinates of the n_s-th small sub-layer (x_n,y_n) can be found as follows:

$$x_n = R_c\left(1-n_s/N_s\,(1-\Delta)\right) \tag{4.3}$$

$$y_n = R_c\, n_s/N_sN_l \tag{4.4}$$

The height of each small sub-layer is R_c/N_lN_s.

An example of the 3D structure mesh of the obtained simulation geometry is shown in Figure 2.1.1(d). The mesh was defined using 3D cylindrical coordinates. The highest mesh

density was implemented directly at ZnO-Au interface to account for the high tunnelling rates in this region. Because the nanowire length of 900 nm is much higher than nanowire width of 73 nm the mesh density was reduced at the centre of the nanowire length to avoid high computational times.

The importance of the complex approximation of the gold particle is demonstrated in Figure 4.3.1. For the three geometries of the similar size (R_c=30 nm, R_{ZnO}=60 nm), 2D approximation with a simple rectangular presentation of gold particle (Figure 4.3.1(a)), complex 2D contact shape (Figure 4.3.1(b)) and a full 3D approximation (Figure 4.3.1(c)) was investigated. Current density with respect to the applied bias (J-V characteristics) in Figure 4.3.1(d) for all structures show the difference of two orders of magnitude at the reverse bias, and a smaller current change at the forward bias. This is due to the geometry-dependent current behaviour which will be discussed in details in the next chapter. A big difference in the current calculations indicates the importance of using a full 3D solution with a good approximation of the gold particle shape.

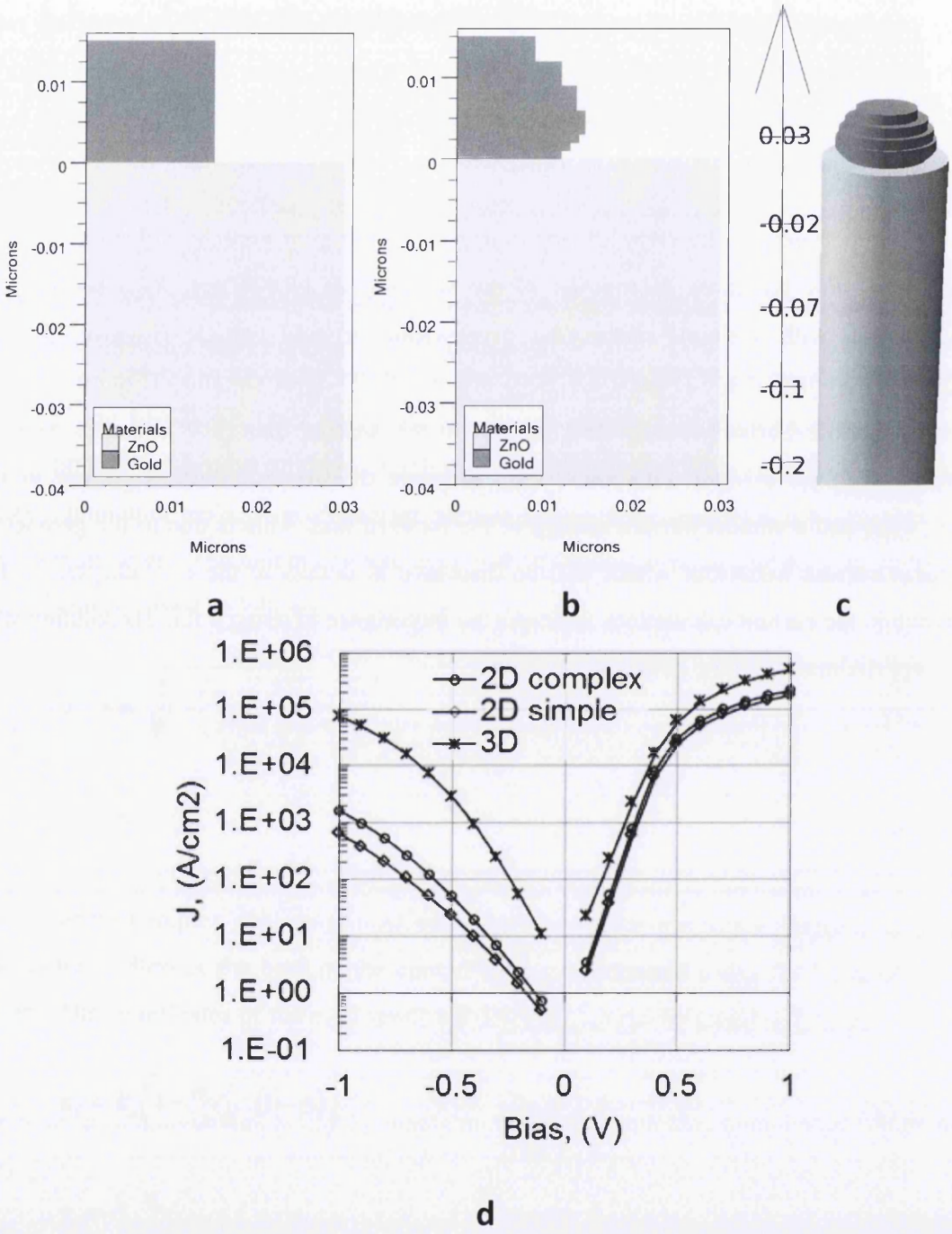

Figure 4.3.1 Comparison of the simple 2D solution (a), 2D solution with a complex particle approximation (b) and 3D geometry approximation. (d) Simulated current density versus applied bias (J-V) characteristics for 2D and 3D geometries in (a), (b) and (c).

4.4 Current mechanism

The model considers a ZnO nanowire of length 900nm, having an electron affinity of 4.5eV and *n*-type doping of 10^{18} cm^{-3}. At the end of the nanowire, Au contacts were considered with a work function of 5.1eV. In the simulation, the second contact, defined as Ohmic, was assumed to be at the base of the nanowire. Both thermionic emission and tunnelling across the Schottky barrier at the metal-nanowire interface were included in the simulation. The thermionic emission current was calculated taking into account the surface recombination velocity, static dipole effects, and a field dependent barrier lowering which originated from the image force. Tunnelling was considered for both electrons and holes, where localized tunnelling rates were calculated through the structure of the semiconductor close to the interface with the universal Schottky tunnelling model [38] (see Chapter 2 for the details on the model). The impact of each transport mechanism will be studied in detail in this chapter.

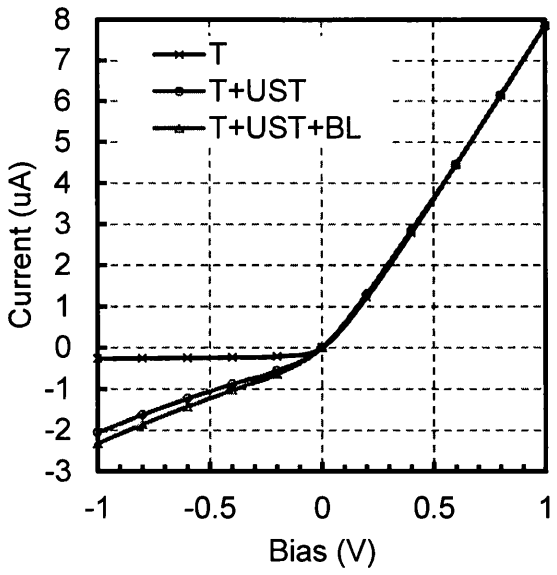

Figure 4.4.1. The transport current at the forward and reverse bias due to thermionic emission and electron diffusion (T), and including universal Schottky tunnelling (UST) and barrier lowering (BL).

The following material parameters were used for ZnO semiconductor: bandgap 3.37 eV, electron affinity 4.5 eV, conduction band density of states at temperature 300 K 2.2×10^{18} cm^{-3}, valence band density of states at temperature 300 K of 1.8×10^{19} cm^{-3}, effective Richardson constants for electrons and holes are 23.7 $A/cm^2/K^2$ and 96.3 $A/cm^2/K^2$ respectively [39]. Using a work function of 5.1 eV for the Au presents a potential barrier at the interface of 0.6 eV.

Figure 4.4.1 demonstrates different contributions from the

different current components: tunnelling of carriers through the potential barrier (UST) and thermionic emission or diffusion of carriers over the potential barrier (T). The additional current increase due to the barrier lowering (BL) is also presented in Figure 4.4.1.

At the forward biases up to 0.6 V, the tunnelling of electrons is a dominant carrier transport mechanism through the potential barrier. This is because at the low forward biases there is a depletion region at the interface introducing a potential barrier. As the bias is further increased, the depletion region at the interface will reduce allowing carrier diffusion from the ZnO NW to the Au contact. This can be seen in Figure 4.4.1, as the bias is reaching +1 V the current component from the carrier diffusion over the potential barrier becomes commensurable with the carrier tunnelling through the depletion region. At the reverse bias up to −1 V, the only carrier transport mechanism allowed is tunnelling. This is due to a very

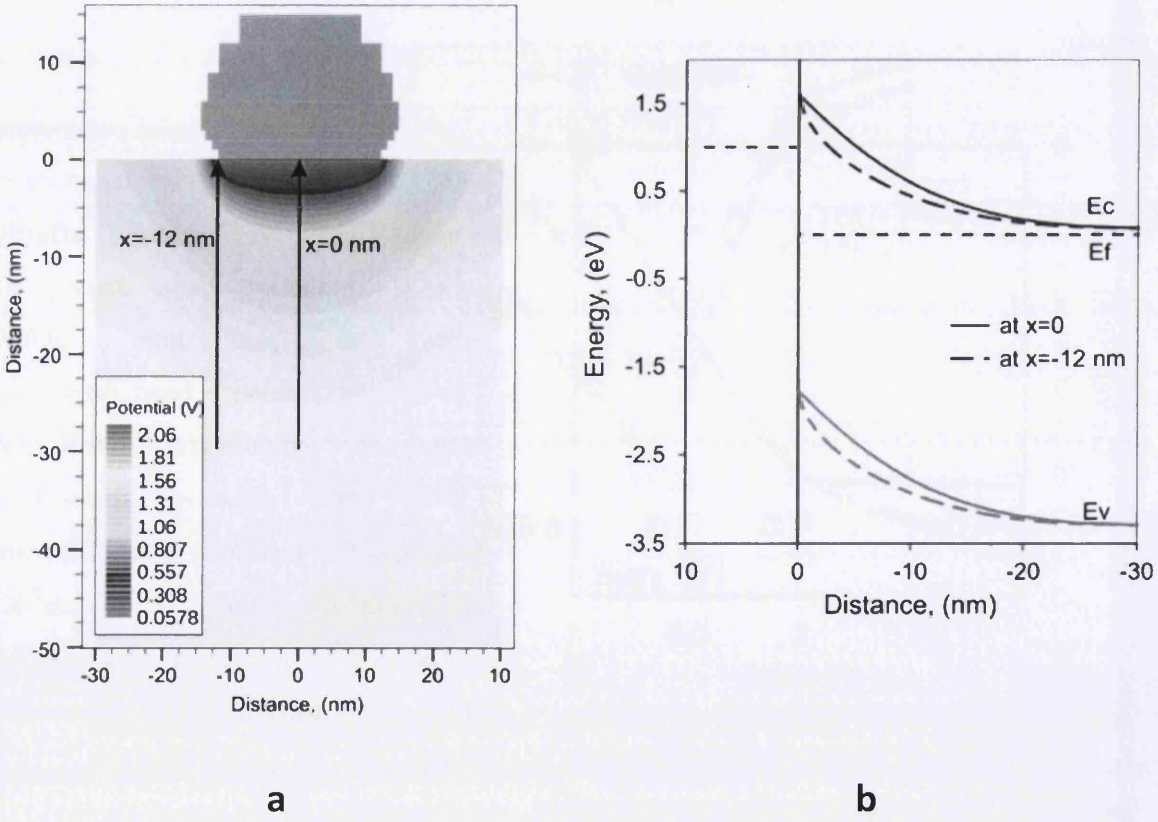

Figure 4.4.2. (a) Spatial distribution of the potential at −1 V bias. (b) Cutline through the centre and at the edge of the contact representing a band profile at a bias of −1 V.

high potential barrier at the interface, and the magnitude of the current at the reverse bias will depend solely on the barrier width. The potential distribution demonstrating depletion region depth and band diagram for −1 V are shown in Figure 4.4.2.

Including the barrier lowering term in the calculations will result in an additional increase of the current as seen in Figure 4.4.2. Preliminary work showed tunnelling through the air gap between the metal curvature and semiconductor surface is negligible (at least 8 orders of magnitude smaller of the total current) and it was neglected in the final simulation.

Unlike in micro-scale metal-semiconductor, the Au-ZnO nanowire nano-contact behaviour and distribution of the current density through the contact will be influenced by the geometry of the structure. Figure 4.4.2(a) demonstrates the spatial distribution of the potential at −1 V for the 60 nm nanowire diameter with a 30 nm gold particle diameter. Due to the

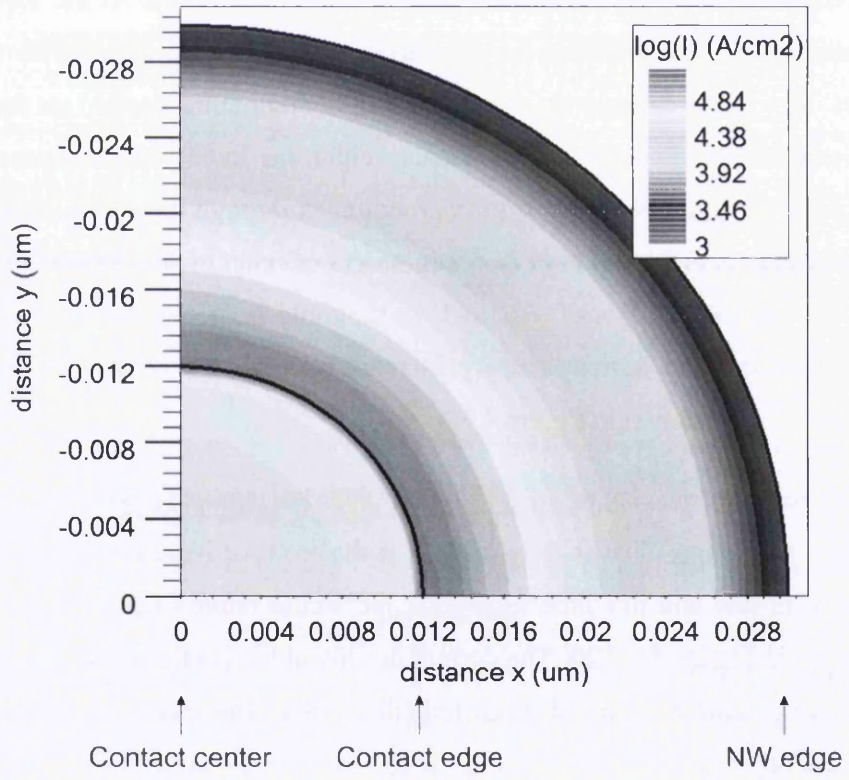

Figure 4.4.3 Current density distribution directly under the contact edge at +1 V for the structure described in Chapters 4.6 and 4.7.

complex shape of the metal particle, the local narrowing of the potential barrier near contacts edge is present. The depletion region is the biggest at the contact centre and it is narrowing to the edge of the contact. This effect can be confirmed using a band diagrams for the centre x=0 nm and edge x=−12 nm of the contact (Figure 4.4.2(b)). At the edge of the contact, the barrier is thinner which will result in the increased carrier tunnelling through the narrow region at contact edge at the reverse bias. The same effect takes place at the forward bias.

The current density plot in Figure 4.4.3 confirms the effect of the edge depletion region narrowing for the forward bias. The highest current density is concentrated around the contact edge (represented with red colour on the colour scale in Figure 4.4.3) and it reduces by roughly one order of magnitude to the contact centre. As expected, the lowest current density is observed away from the contact near the surface of the ZnO nanowire.

Figure 4.4.4 is a simplified representation of the distribution of the current density which allows analysis of the change though the whole bias range. At the forward bias, the barrier thinning and the reduction in the barrier height is significant with the increasing applied bias. Due to the exponential dependence of the tunnelling current on the barrier width and thermionic emission current on the barrier height, the increase in the current density for every bias point in Figure 4.4.4(a) is quite pronounced through the whole contact length and at the edge of the contact. A change in seven orders of magnitude is observed at the contact centre for the bias change from 0.1 V to 1 V. It should be noted that all profiles in Figure 4.4.4(a) demonstrate the current density increase around one order of magnitude at the contact edge as it was shown in Figure 4.4.3.

At the reverse bias up to −1 V, a major carrier transport mechanism is tunnelling though the contact edge. That is why, unlike at the forward bias, the current density at the contact centre is low and has little change at the whole range of the reverse biases −0.2 - −1 V as shown in Figure 4.4.4(b). The current density at the centre of the contact at +1 V and −1 V will have at least 8 orders of magnitude difference. The increase in the current density at the contact edge is observed at the both reverse and forward biases. The edge current density at the reverse bias will have a small bias dependence as seen in Figure 4.4.4(b).

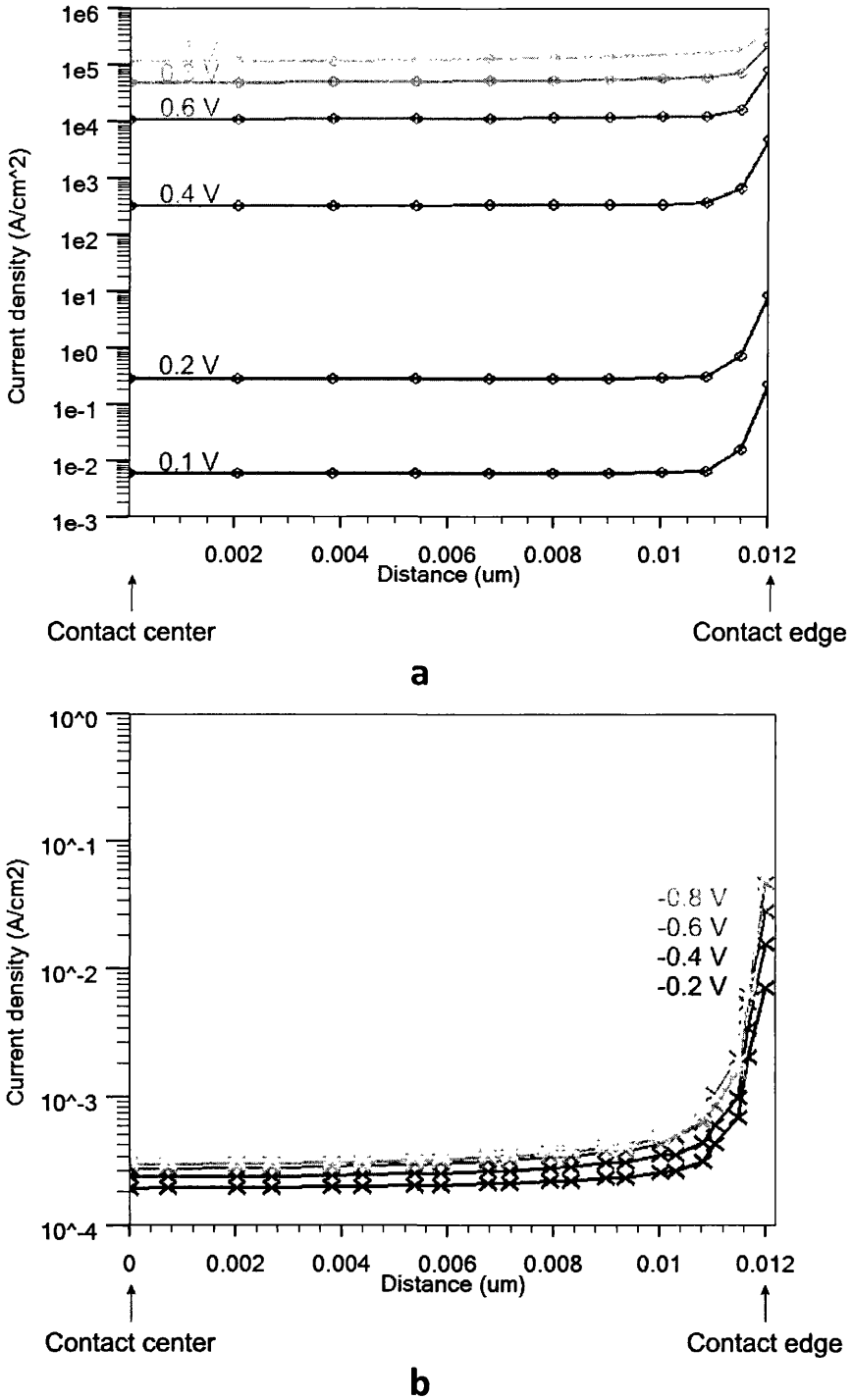

Figure 4.4.4. (a) Current density cutline from the centre of the contact to the contact edge at forward bias in the range of 0.1-1 V. (b) Current density cutline from the centre of the contact to the contact edge at the reverse bias in the range of −0.2- −1 V.

4.5 Effect of the contact size

To explain the experimental results in Chapter 4.2 where the transition from rectifying to Ohmic behaviour was observed as the Au particle diameter decreases, the following transport mechanisms are considered in the simulation: thermionic emission, tunnelling and recombination [1], [40]. The model considers a ZnO nanowire of a diameter 73 nm and a length of 900 nm, having an *n*-type doping concentration [41] of 10^{18} cm^{-3}. At the end of the nanowire, Au contacts with diameters of 59 nm, 47 nm and 37 nm were considered. In the model for this chapter, interface charge on the nanowire surface or at the contact junction was

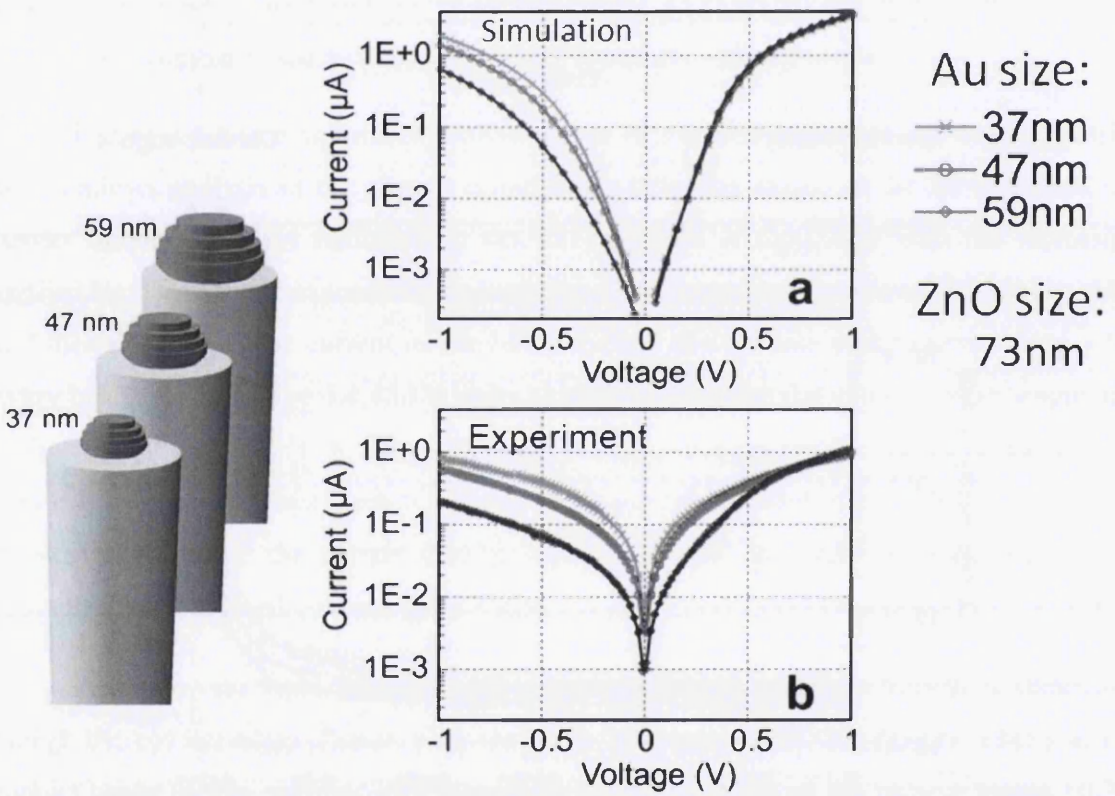

Figure 4.5.1 Comparison of the simulation results with the experimental measurements. (a) Simulated I-V characteristics for contacts with a diameter of 37 nm (green, ×), 47 nm (red, ○) and 59 nm (blue, ◊). (b) The experimental I-V characteristics for the same sized contacts on a 73 nm diameter nanowire (The experimental values of the current are scaled to the current value of the 59 nm diameter contact at +1 V to account for the external resistance).

neglected, in addition to series resistance effects.

A calculated current as a function of applied bias (I-V characteristics) at biases of ±1V, following the experimental regime, are displayed in Figure 4.5.1(a) for contact diameters of 59 nm, 47 nm and 37 nm. The figure illustrates the effect that the contact size has on the electrical properties. The simulated I-V characteristics showed that the reverse bias current density increases when the contact size is decreased changing contact behaviour from Schottky to more Ohmic-like. For comparison, the experimental results are shown in

Previously, Smit *et al.* [13] predicted that when a metal contact to a semiconductor is reduced in size, spanning the micro-scale to the nanoscale, a significant reduction in depletion width will be observed. The reduction in the Au particle size from 59 nm to 37 nm is not significant enough to bring about an appreciable change in the depletion width at the centre of the contact as shown by the simulation results in Figure 4.5.2(a). Figure 4.5.2(c) shows that nearly all of the current will be concentrated at the periphery of the interface area due to depletion region narrowing at the edge of the contact in comparison to the centre of the contact. Current transport occurs almost exclusively through a narrow region at the edge of the contact (refer to the Chapter 4.4). Importantly, the narrowing of the depletion region at the edge is more pronounced for nanowire contacts due to the complex curved shape of the Au particle near the interface. The diminishing size of the contact from 59 nm to 37 nm will produce a depletion region that will narrow near the contact edge as the contact size is reduced, as shown in Figure 4.5.2 (b). Although the difference in the reduction of depletion region width with reduction in the contacts size appears small, this has a profound effect on the tunnelling current due to exponential dependence on a barrier thickness. Increase in the tunnelling through the contact edge with decrease in the Au contact size can be confirmed by the I-V characteristics in Figure 4.5.1 showing an increased conductance at reverse bias for the 37 nm contact.

To confirm this characteristic, the simulation predicts that for a simple cylindrical metal contact covering the entire end of the nanowire, similar to those used by Smit *et al.*[13] and Leonard *et al.*[2], the barrier narrowing at the edge will not be significant. If the barrier narrowing is small, the large tunnelling current is limited leading to Schottky-like contact behaviour. It should be noted that 2D calculations do not capture the effect of shape as demonstrated in Chapter 4.3 thus overestimating the contact area and thermionic emission components, whilst underestimating the influence of the edge region on the tunnelling current. Therefore, the intricacies of the nanowire contact geometry and size provide a means

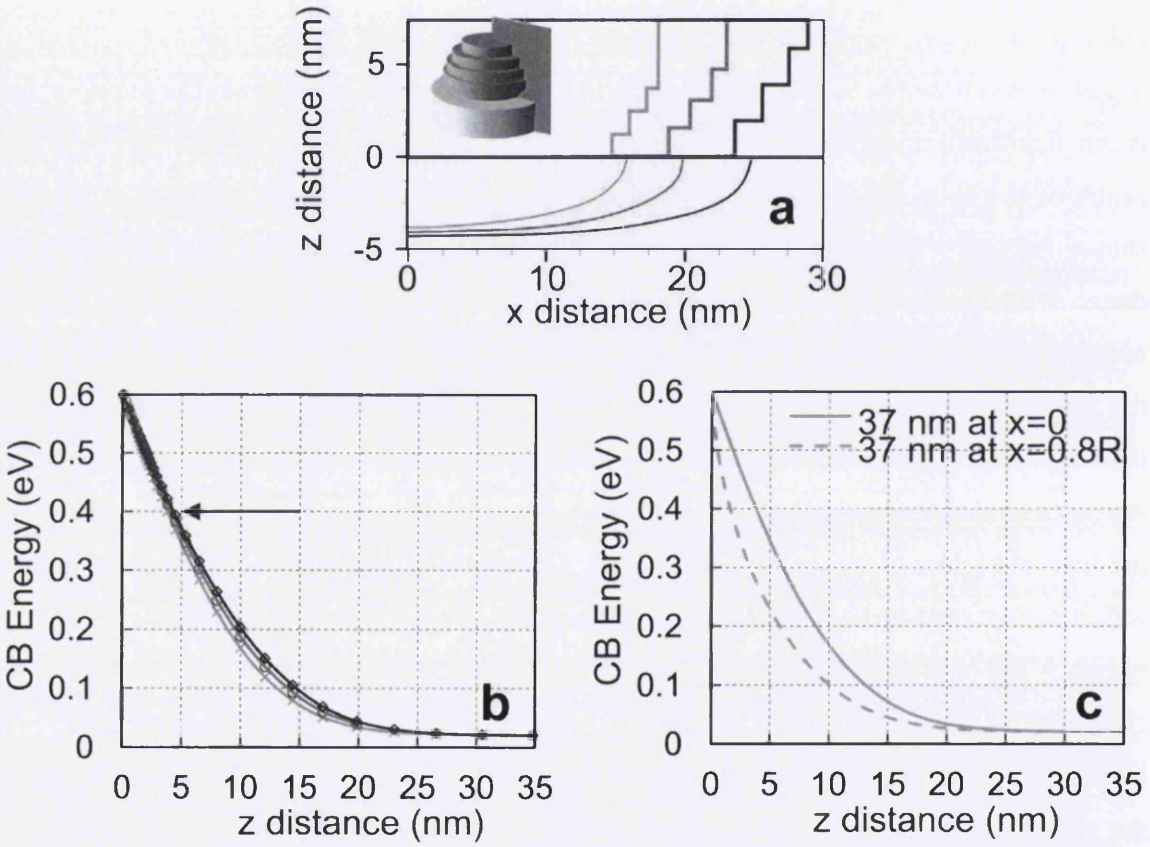

Figure 4.5.2 (a) The position of the constant 0.4 eV conduction band potential contour. The inset indicates the plane of the cross-section used. (b) Conduction band profile along the z-axis, down in to the nanowire at the contact edge for the 37 nm, 47 nm and 59 nm diameter contacts, an arrow indicates 0.4 eV conduction band potential shown in (a). (c) Conduction band profile along the z axis at the contact centre, x=0, and contact edge, x=0.8R.

through which quantum effects control the transport properties.

4.6 Effect of the nanowire diameter

The change in the electrical behaviour is investigated using the rectification ratio. The rectification ratio is defined as the ratio of the forward bias current to the reverse bias current. Figure 4.6.1 shows rectification ratio (ratio between current at +1 V and −1 V) as a function of the interface and nanowire diameter ratio for the experimental data. Experimental points marked with diamond symbols are for ZnO NW with no Au particle, in these measurements tungsten tip was used as a metal contact. The error bars account for the diameter variation of the hexagonal nanowire and for the ±2 nm measurement error of the Au diameter. Simulation

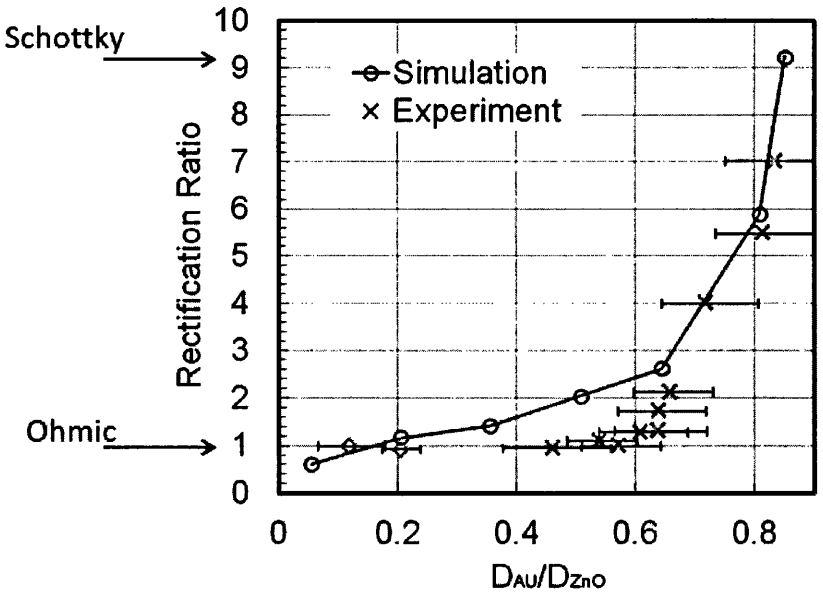

Figure 4.6.1. The rectification ratio at ±1 V as a function of the contact (D_{Au}) and nanowire (D_{ZnO}) diameter ratio (the error bars account for the diameter variation of the hexagonal nanowire and for the ±2 nm measurement error of the Au diameter) for the experimental data. Experimental points marked with diamond symbols are for ZnO NW with no Au particle, tungsten tip used as a metal contact. Simulation data was created for 37 nm Au particle diameter and a range of ZnO diameters.

data was obtained for 37 nm Au particle diameter and various ZnO diameters to create a range of D_{Au} / D_{ZnO} ratios. The agreement between the two curves is evident, showing correlating trends for rectification ratios measured at +/−1.

Figure 4.5.1 illustrate that the electrical behaviour of the contacts depends on the Au contact size. The rectification ratio decreases towards 1 (which defines pure Ohmic behaviour) when the ratio between the diameters of Au contact and ZnO NW (D_{Au}/D_{ZnO}) decreases towards 0.0. The qualitative change of the rectification ratio observed at about the D_{Au}/D_{ZnO} ratio of 0.6 for both the experimental and simulated data. Contacts with the D_{Au}/D_{ZnO} ratios above 0.6 become markedly more Schottky-like. This is because the size of the Au contact becomes so small in comparison with the size of the ZnO NW that it does not play a role in the transport across the interface. Instead, the effect of the nanowire diameter on the carrier transport through the metal-semiconductor interface becomes a dominant factor.

To explain the effect of the nanowire diameter on the electrical properties of the Au-ZnO contacts, two particular structures are studied. Figure 4.6.2 (c) and (d) illustrate such structures with different ZnO NW diameters for a fixed gold particle diameter of 30 nm. In the structure shown in Figure 4.6.2 (c), the ZnO NW diameter is equal to the metal-semiconductor interface diameter of 24 nm (R_{ZnO}=12 nm) and D_{Au}/D_{ZnO}=1.25. In the structure in Figure 4.6.2 (d), a ZnO NW has a diameter of 60 nm (R_{ZnO}=30 nm) and D_{Au}/D_{ZnO}=0.5. Here, the nanowire diameter is significantly larger than the metal-semiconductor interface area with the interface-to-nanowire diameter ratio is 0.5. The NW length of 900 nm was assumed in all the simulations.

The result of the current calculations is shown in Figure 4.6.2 (a). A geometrical effect of the change in the NW radius results in a transformation of Ohmic to Schottky behaviour in the current when the NW radius is reduced. At a high forward bias, the current originates predominantly from the thermionic emission. Due to a high doping of the NW, the metal Fermi level will go above the conduction band resulting in a significant increase in the current for both structure variations. At the reverse bias and small biases than 0.6 V, the current will be dominated by tunnelling as explained in Chapter 4.4.

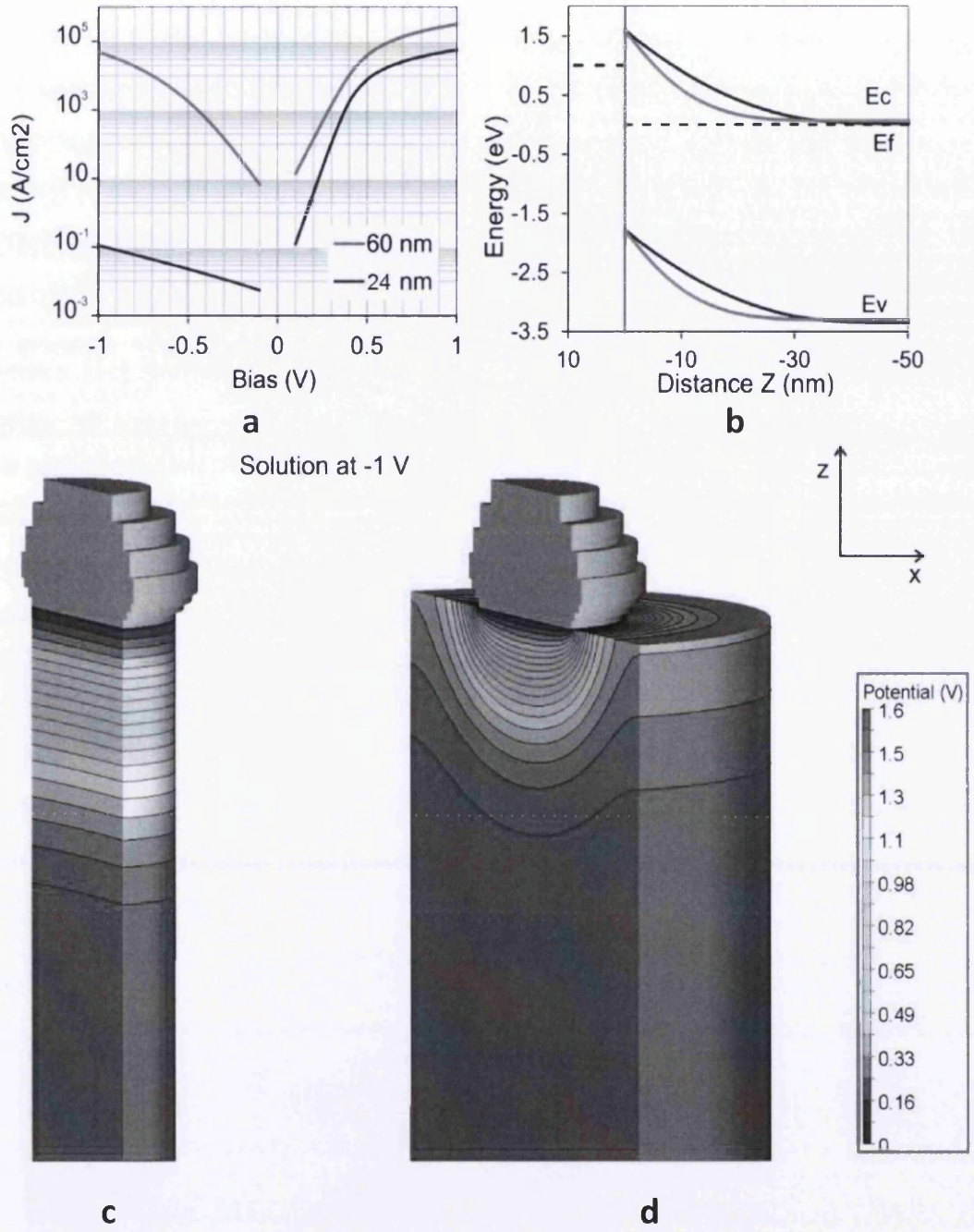

Figure 4.6.2 (a) Current density versus applied bias (J-V) characteristic for the ZnO nanowires with 24 nm(blue) and 60 nm (red) diameters. (b) Band diagram at -1 V for the nanowires with 24 nm(blue) and 60 nm (red) diameters. Potential distribution at −1 V in ZnO nanowires of (c) 24 nm diameter with D_{Au}/D_{ZnO}=1.25, and (d) 60 nm ZnO diameter with D_{Au}/D_{ZnO}=0.5. Gold particle diameter of 30 nm used in simulations.

The current density calculations in Figure 4.6.2 (a) demonstrates a difference in 6 orders of magnitude in reverse bias current when the nanowire diameter is increased from 24 nm to 60 nm (from R_{ZnO}=12 nm to R_{ZnO}=30 nm). This change can be explained using a band diagram at −1 V in Figure 4.6.2 (b). The band diagram shows an increase in the potential barrier width when the nanowire diameter is reduced. The increase in the barrier width will result in the reduced magnitude of the tunnelling current due to the exponential dependence of the tunnelling current on the barrier width.

The microscale contact scaling will result in a reduced depletion width [31]. Leonard *et al.* [12] have shown that in the case of nanocontacts with the contact covering the entire end of Ge NWs, the depletion region width will be increased as the NW radius is scaled down. The depth of the depletion region for the ZnO NW with a diameter of 24 nm is larger than in 60 nm NW (Figure 4.6.2 (c)), which confirms that nanoscale contacts will have a complex behaviour different from the behaviour of microscale contacts. The effect of the increase of depletion region width in NWs with contact covering the entire end of the NW will introduce a large potential barrier for the tunnelling current in the case of the structure in Figure 4.6.2 (c) and will result in 6 orders of magnitude difference in the tunnelling currents at reverse bias (Figure 4.6.2 (a)), making the contact with D_{Au}/D_{ZnO}=1.25 more Schottky in comparison to contact with D_{Au}/D_{ZnO}=0.5.

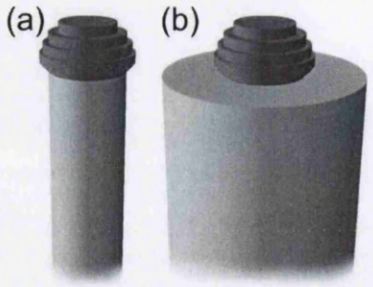

Figure 4.6.3 3D simulations of ZnO NWs with Au particle (R_{Au}=15 nm) deposited on the top and forming the contact radii R_c=12 nm with (a) R_{ZnO}=12 nm and (b) R_{ZnO}=30 radii of ZnO NWs. The top ~70 nm of the structure is shown here.

4.7 Effect of current crowding

The current crowding effect, which leads to the non-uniform distribution of the current density near the edge of the metal contact, was reported earlier for nanostructures like silicon MOSFETs [19], carbon-nanotubes with side contacts [16], graphene sheets [18], and other side-bonded contacts and structures lying flat on the substrate. In the present chapter, we focus on the size-dependent effect of current crowding in end-bonded contacts for the ZnO NW structure. We examine the effect for two geometry configurations demonstrated in in the previous chapter (see Figure 4.6.3).

In Figure 4.6.2 and Figure 4.7.2, the spatial current density distribution at the bias of −1 V and +1 V presents the regions of the highest current density.

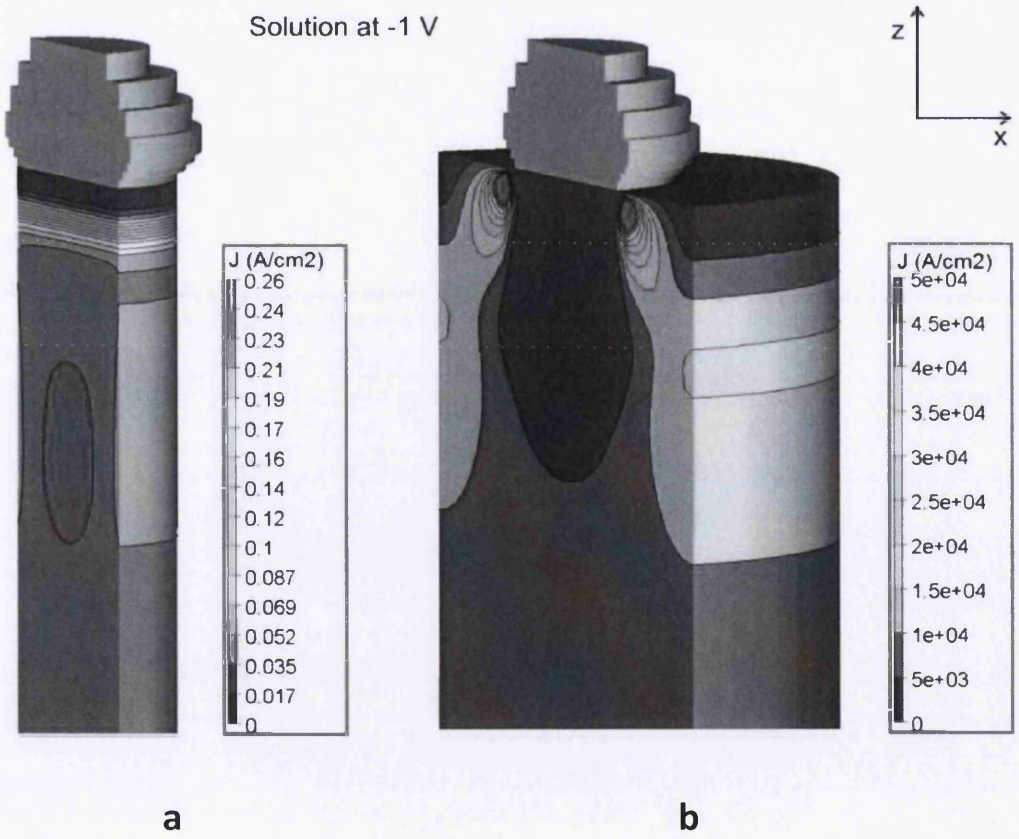

Figure 4.7.1. Current density distribution at −1 V for ZnO NWs with Au particle (R_{Au}=15 nm) deposited on the top of the ZnO NW (a) R_{ZnO}=R_c=12 nm and (b) R_{ZnO}=60 nm, R_c=12 nm.

When the NW is reverse biased at −1 V (Figure 4.7.1 (a) and (b)), the largest current density for the smaller NW radius of R_{ZnO}=12 nm is at least 5 orders of magnitude smaller than the largest current density for a radius of R_{ZnO}=30 nm. Local current crowding outside of the contact will occur when the area of the Au-ZnO interface is much smaller than the NW cross-sectional area. This area which is supplying electrons has electrons concentrated at the edge region to maintain a constant flux. The area of high density current (~10^5 A/cm^2) will not contribute to the current transport through the contact due to a large potential barrier in the depletion region as seen in Figure 4.6.2 (c) and (d). The current density at the metal-semiconductor interface will remain as low as ~10^{-4} A/cm^2 (Figure 4.4.4(b)) but the current density at the contact edge will be increased by 2 orders of magnitude to ~10^{-2} A/cm^2 due to the large tunnelling into the area of the local barrier thinning (see Chapter 4.4).

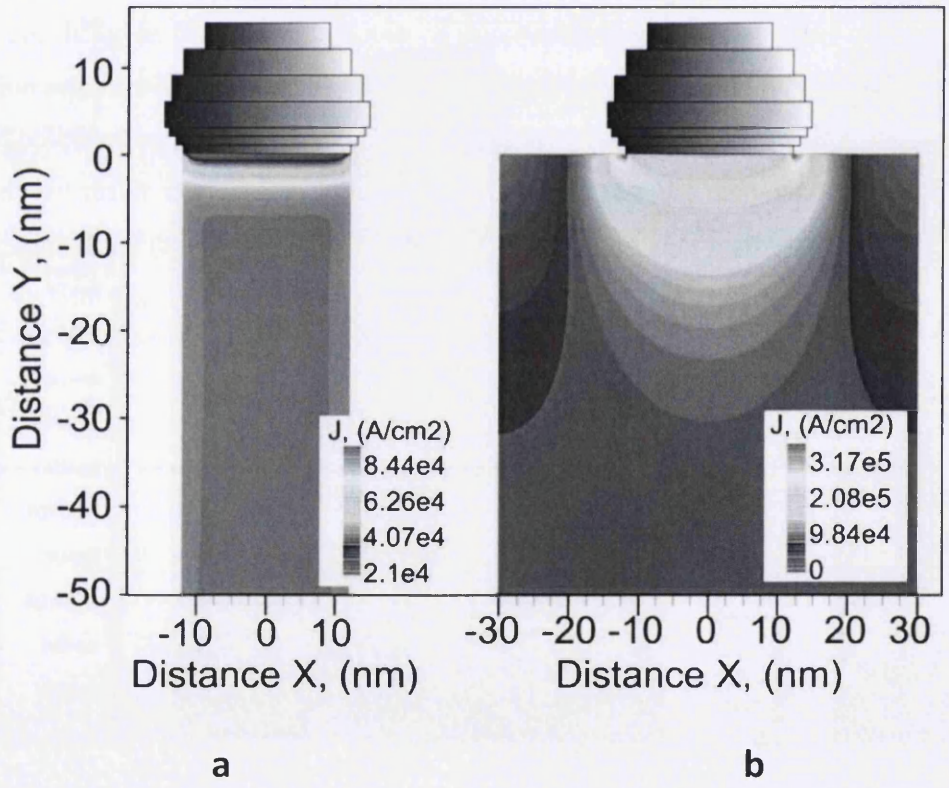

Figure 4.7.2 The spatial distribution of the current density for 1 V (a, b) indicates a size-dependent current crowding effect. Au particle (R_{Au}=15 nm) deposited on the top of the ZnO NW (a) R_{ZnO}=R_c=12 nm and (b) R_{ZnO}=60 nm, R_c=12 nm.

At the forward bias of +1 V, a completely different electrical behaviour is observed (Figure 4.7.2 (a) and (b)). At voltages higher than 0.6 V, the thermionic emission overtakes the tunnelling current (see Chapter 4.4). This results in a more uniform distribution of the current through the NW structure and under the interface. The current density plot under the interface in Figure 4.7.2 (b) indicates a relatively higher current at the edge of the metal-semiconductor contacts where a high electric field is present but the current density remains at the same order of magnitude through the rest of the interface. This effect is confirmed in Figure 4.4.4 (a).

The schematic plot of the current vectors indicates the direction of current at −1 V (Figure 4.7.3 (b)) and +1 V (Figure 4.7.3 (d)). The highest current density area is indicated with longer vectors. When a forward bias is applied, the highest current density will be passing directly through the contact (Figure 4.7.3 (c)). It can be seen from the plot that, in reverse bias, the current is crowding at ~3 nm away from the contact in the direction towards the contact but only a very small current is passing directly through the contacts (Figure 4.7.3 (a)). This current crowding effect may lead to Joule heating which is known to result in heating or cooling near the contact area depending on the direction of the current flow [18]. It has been demonstrated that a large NW surface-to-volume ratio will lead to heat lost due to Joule heating of the semiconductor [20]. This self-heating effect will be discussed in the next chapter.

For the small nanowire radius of 12 nm at −1 V bias, the total current vectors are shown in Figure 4.7.4 (c). It indicates that the dominant component of the current is *z*- component. The current density is reduced near-metal semiconductor interface where the depletion width and barrier width for the tunnelling current is the highest. This is observed in Figure 4.7.4 (c) as well showing that the current density at the interface is at least 3 orders of magnitude smaller than through the nanowire body. There is also *x*- and *y*- component of the current present. Figure 4.7.4(b) demonstrates the current density component in *x*- direction. A complex radial component of the current is present in a contacted ZnO nanowire with a radius of R_{ZnO}=12 nm, indicating a vortex behaviour [42] of the current in *x*- and *y*-directions at the forward and reverse biases. However, this radial current component will not

significantly contribute to the total current density due to its low density as shown in Figure 4.7.4 (d).

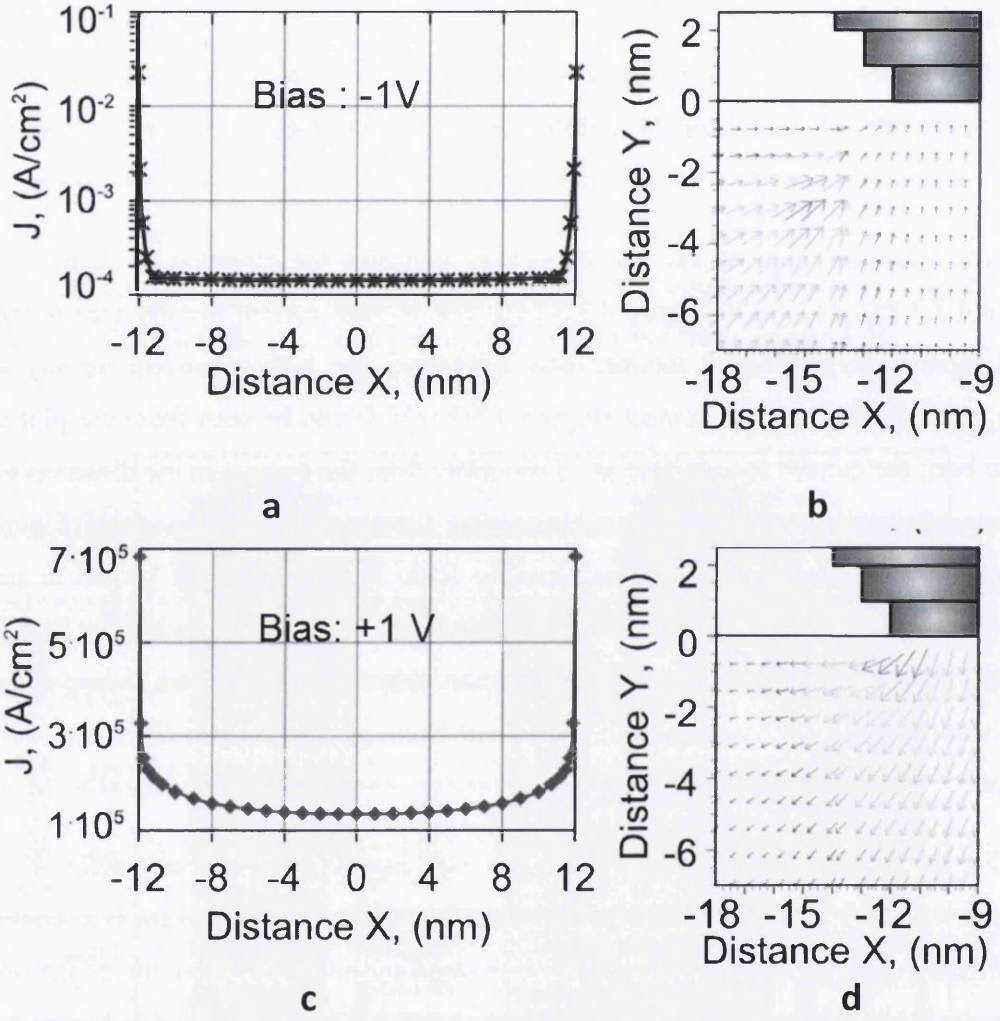

Figure 4.7.3 Current density distribution directly under the contact interface at −1 V on a logarithmic scale (a) and at +1 V on a linear scale (c). The direction of the current flow near the contact is marked using vectors for −1 V (b) and +1 V (d). The regions of a larger current density are marked with the longer arrows.

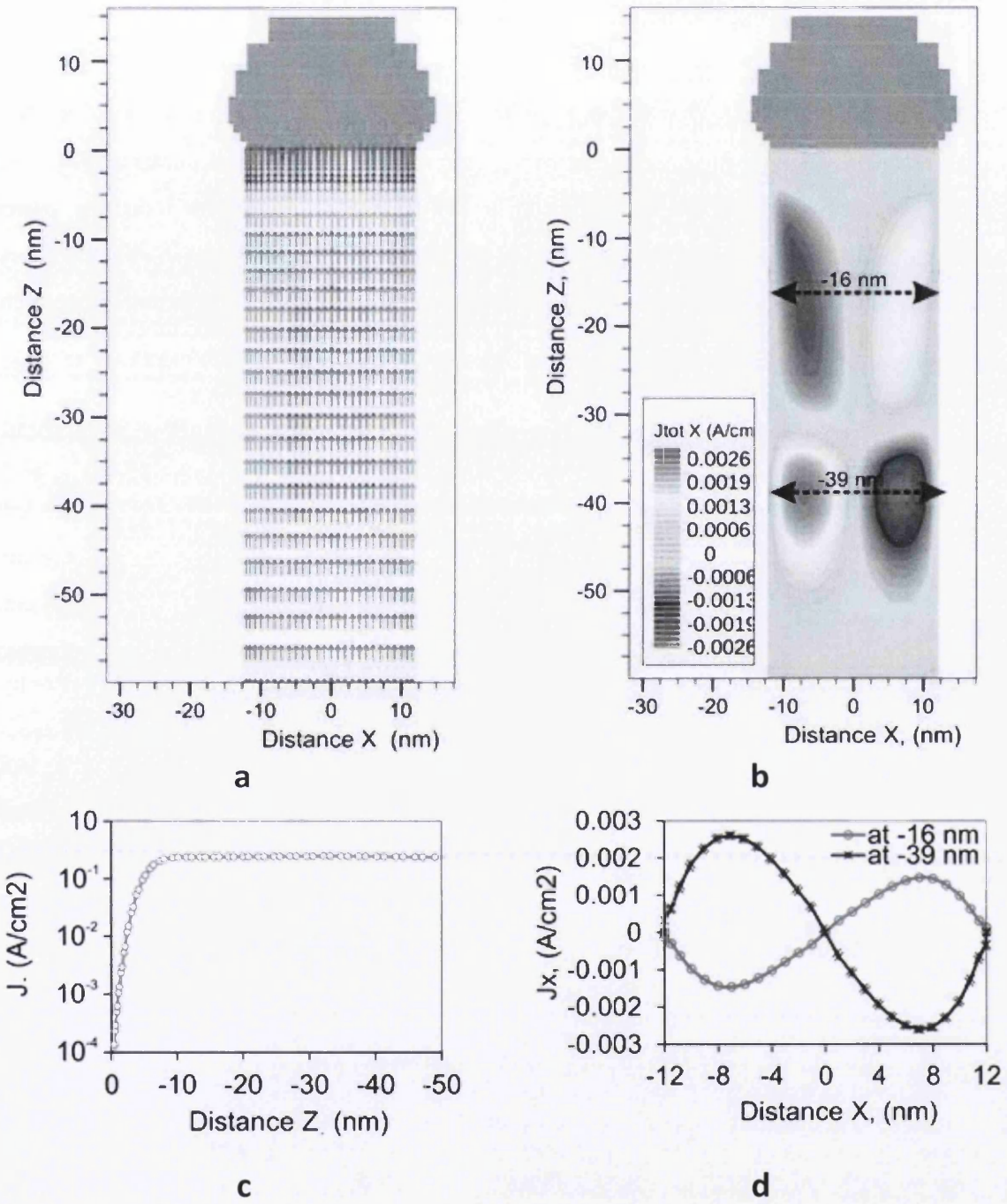

Figure 4.7.4 (a) The direction of the total current flow at −1 V indicating that dominant current component of the current is in z-direction. (b) Current density component in x-direction. (c) Total current density cutline through the body of the nanowire. (d) Current density cutline at −16 nm and −39 nm indicating the magnitude of the current density component in x-direction.

4.8 Heating effects

Thermal behaviour of metal contacts to nanostructures due to current flow has been investigated earlier in side-bonded nanostructures like graphene-metal contacts [18], ZnO, GaN [17] and SiGe [20] nanowires (NWs). These nanoscale contacts induce a current crowding effect [18] due to parasitic resistance at the edge of the downscaled contacts. Current crowding is known to result in a local temperature rise at the metal-semiconductor interface which can lead to device failure [18].

The thermal properties of the nanostructures during the current flow were studied earlier in the literature. Leonard *et al.* [20] reported the temperature distribution through the

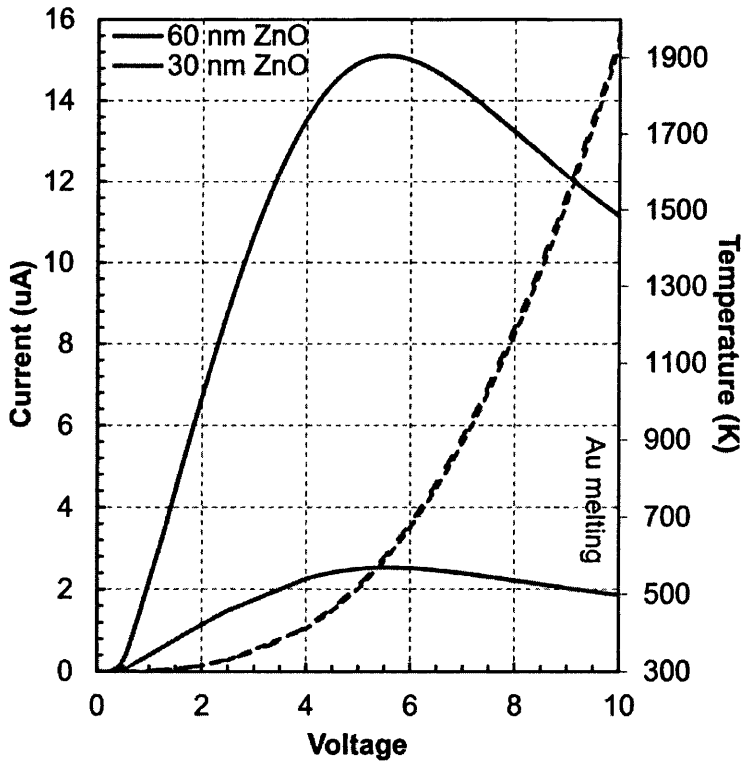

Figure 4.8.1 Simulated I-V characteristics (solid line) and a highest lattice temperature (dashed line) of the metal-semiconductor interface at the forward bias.

NW body with a fixed contact temperature. LeBlanc *et al.* [17] studied the heat generation along ZnO NWs and near electrical contacts using a 1D model for the Ohmic contacts for the side-bonded ZnO NWs.

In the present chapter, we study the effect of current crowding on the temperature profile along the nanowire and around the metal contact for the end-bonded ZnO NWs with Schottky contacts. A full 3D geometry, as seen in Chapters 4.6 and 4.7, is employed in order to accurately model the geometry at the nanoscale. This 3D model considers carrier transport of electrons and holes self-consistently coupled with thermal flow [21]. The carrier transport includes both thermionic emission and tunnelling current with static dipole effects and a field dependent barrier lowering due to image force [43]. Since the transport parameters depend on the lattice temperature, lattice heating and cooling due to the carrier generation and recombination, Joule heating and Peltier-Thomson effects are also included [21]. Finally, the thermal modelling considers temperature dependent thermal conductivity model [22] and heat capacity model [23] for ZnO (see Chapter 2).

The simulation results in Figure 4.8.1 demonstrate the current decrease at around 5 V due to a high generation of Joule heating near the contact. As the device temperature is further increased with the increase in voltage until ~8.5 V, the Au contact melting temperature is reached which can lead to device failure. At the forward bias, the effect is very similar for both nanowire geometries.

At the reverse bias (Figure 4.8.2), the difference in the Au-ZnO nanowire geometry will results in difference in the reverse bias current magnitude (see Chapter 4.7). For the 60 nm diameter nanowire, the current degradation due to the Joule heat will be observed at ~−7 V (Figure 4.8.2(a)). The self-heating of 60 nm structure will result in the device failure due to the Au contact melting at ~−8 V (Figure 4.8.2(b)). The smaller nanowire structure with 30 nm diameter will have a current breakdown at the much higher voltages. The observed effect demonstrates that in case of the nanoscale devices a change to the nanostructure geometry will substantially affect the electrical behaviour and reliability of the device without any change to the material parameters of the system.

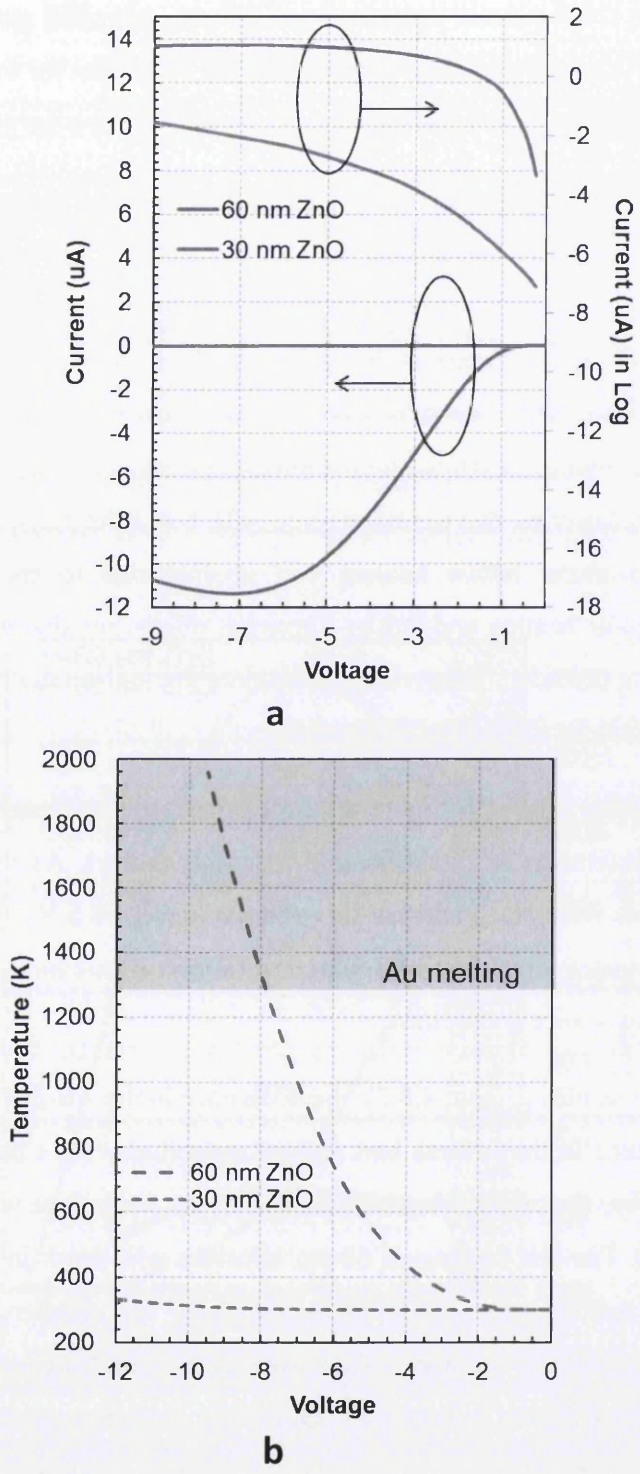

Figure 4.8.2 (a) Simulated I-V characteristics on the linear and logarithmic scales and (b) a highest lattice temperature of the metal-semiconductor interface at the reverse bias.

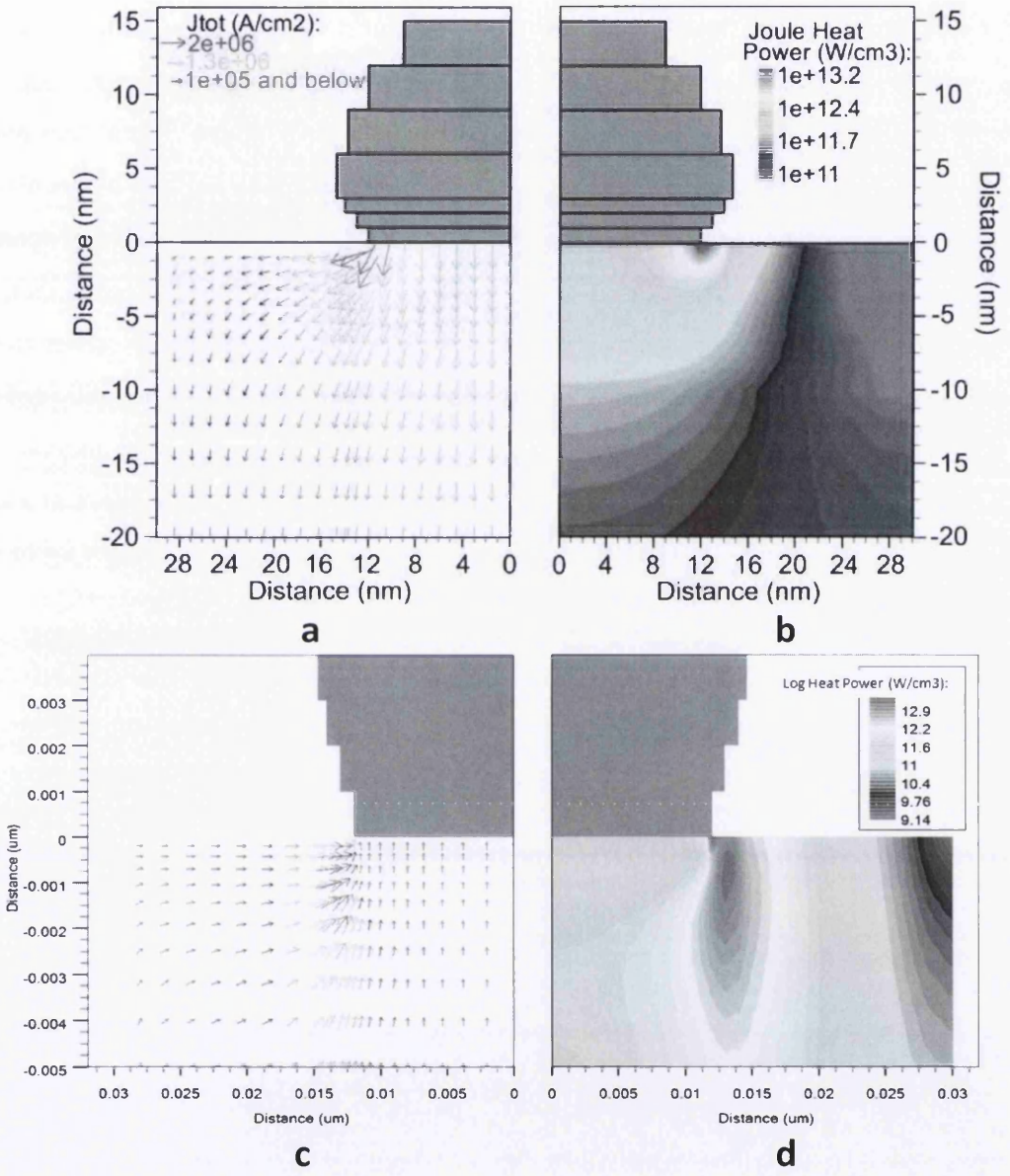

Figure 4.8.3. (a) Schematic plot of the current vectors near the contact edge at 8 V demonstrating the current crowding effect. (b) Spatial distribution of the Joule heating power at 8 V. (a) Schematic plot of the current vectors near the contact edge at −8 V demonstrating the current crowding effect. (b) Spatial distribution of the Joule heating power at −8 V.

The heating of the Au-ZnO nanowire structure will be highest directly at the metal-semiconductor interface. Figure 4.8.3(a) and (c) demonstrate the current vectors at the forward and reverse bias of 8 V and −8 V, respectively. The current vectors indicate the increased current density at the edge of the contact. Due to the local narrowing of the potential barrier at the corners of the Au contact (see Chapter 4.4), the current transport will mostly occur through the narrow region at the contact edge and will result in the local current crowding effect. The increased current density will lead to the high Joule heat generation at the edge of the contact as shown in Figure 4.8.3 (b) and (d). It should be noted that, at the reverse bias of −8 V, the high current density area does not contribute to the carrier transport through the metal-semiconductor interface as seen in Figure 4.8.3 (d). This will lead to the Joule heat generation at two locations: directly at the metal-semiconductor interface and a 1 nm away from the interface. As a result the spatial distribution of temperature at a bias of −8 V in Figure 4.8.4 indicates higher local temperature around the NW contact up to nearly 1330 K.

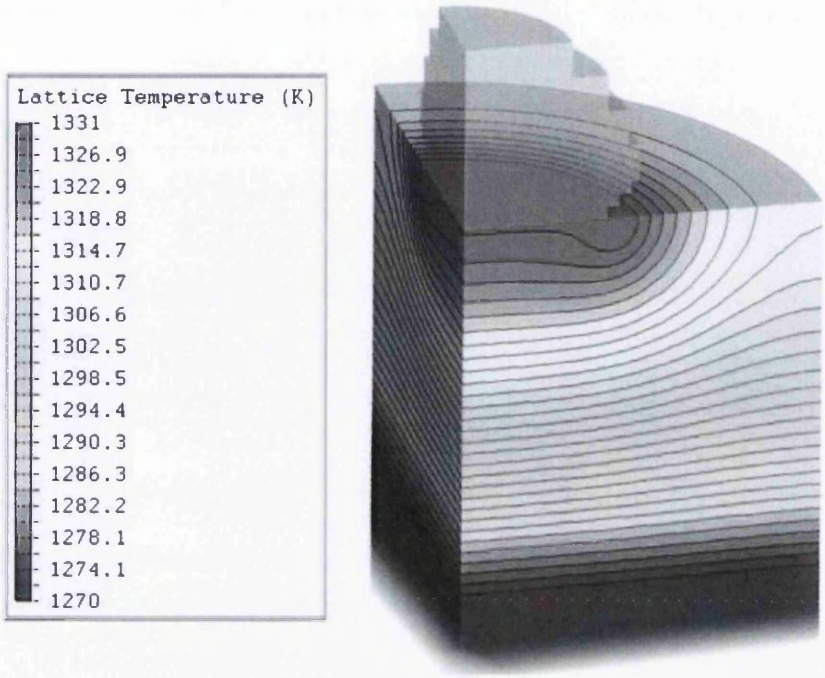

Figure 4.8.4 Spatial distribution of the lattice temperature at −8 V (only the top of ~40 nm of the nanowire length is shown).

4.9 Influence of surface charge on transport in ZnO nanowires

4.9.1 Surface charge in hydrothermally grown nanowires

To study the influence of surface charge on the electrical properties of ZnO NW, hydrothermally grown nanowires were used to experimentally confirm simulation results [24], [25]. These nanowires do not have metal contact deposited on the surface like in ZnO NW structure studied earlier in Chapter 4.1-4.7, instead metal probe placed on the nanowire surface is used to perform current measurements. The measured current before and after the argon ion bombardment in Figure 4.9.2 (a) and (b) demonstrate the reduction in the current magnitude and deviation from the linear shape of the I-V characteristic. This is due to the change in the surface properties of the nanowire. The measurement results demonstrate a

surface defect density of states of 10^{13} cm^{-2} which has a non-uniform nature decreasing to the centre of the nanowire.

In the simulation, a full 3D approximation of the tip-nanowire structure was used as shown in Figure 4.9.1. The nanowire has a 330 nm diameter; the tip structure is approximated using cylindrical shape with a 5 nm diameter. *n*-type doping with a concentration of $N_D=10^{17}$ cm^{-3} is assumed in the nanowire with a barrier height of $\varphi_B=0.27$ eV at the metal-nanowire interface.

Figure 4.9.2 (d) shows I-V simulation results without interface charge. When the surface charge of 10^{13} cm^{-2} is introduced in to the simulations (Figure 4.9.2(c)), the increase in the current magnitude and a change in the current slope to linear is observed.

Figure 4.9.3 (a) shows a charge distribution at the nanowire surface. It can be seen that the charge density at the metal-nanowire surface is not changing. When there is no charge at the nanowire surface, the bands at the nanowire-air interface will be flat as seen in Figure 4.9.3 (b). Presence of the positive charge at the surface (negative charge at the nanowire) will result in the band bending down and electron accumulation near the surface. The accumulation layer will be increased with the increase in the charge as expected. At the

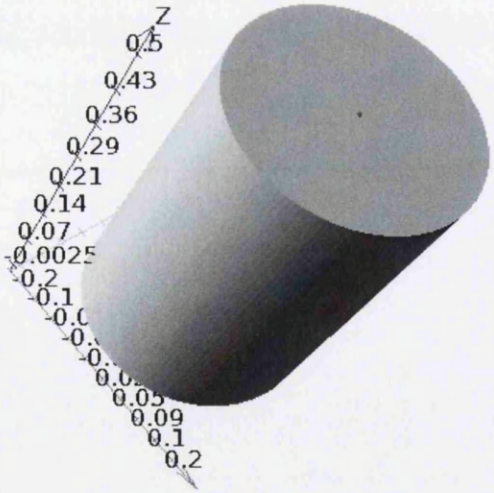

Figure 4.9.1. 3D approximation of the ZnO nanowire with a diameter of 330 nm (yellow) and a metal tip with a diameter of 5 nm (blue) at the top and at the bottom of the structure.

metal-nanowire interface, the barrier height will be determined by the work functions of the metal and nanowire and will be always fixed to 0.27 eV. The charge accumulation at the surface will alter the barrier width as seen in Figure 4.9.3 (c). The accumulation will act as the additional doping at the surface introducing the screening effect. As described in Chapter 4.4, the main current transport mechanism takes place through the narrow region at the contact edge. The additional barrier narrowing at the metal-nanowire interface will introduce the increase in tunnelling due to the exponential dependence of the tunnelling current on the barrier width. This will result in the change of the current magnitude and a slope of the I-V characteristic as seen in Figure 4.9.2.

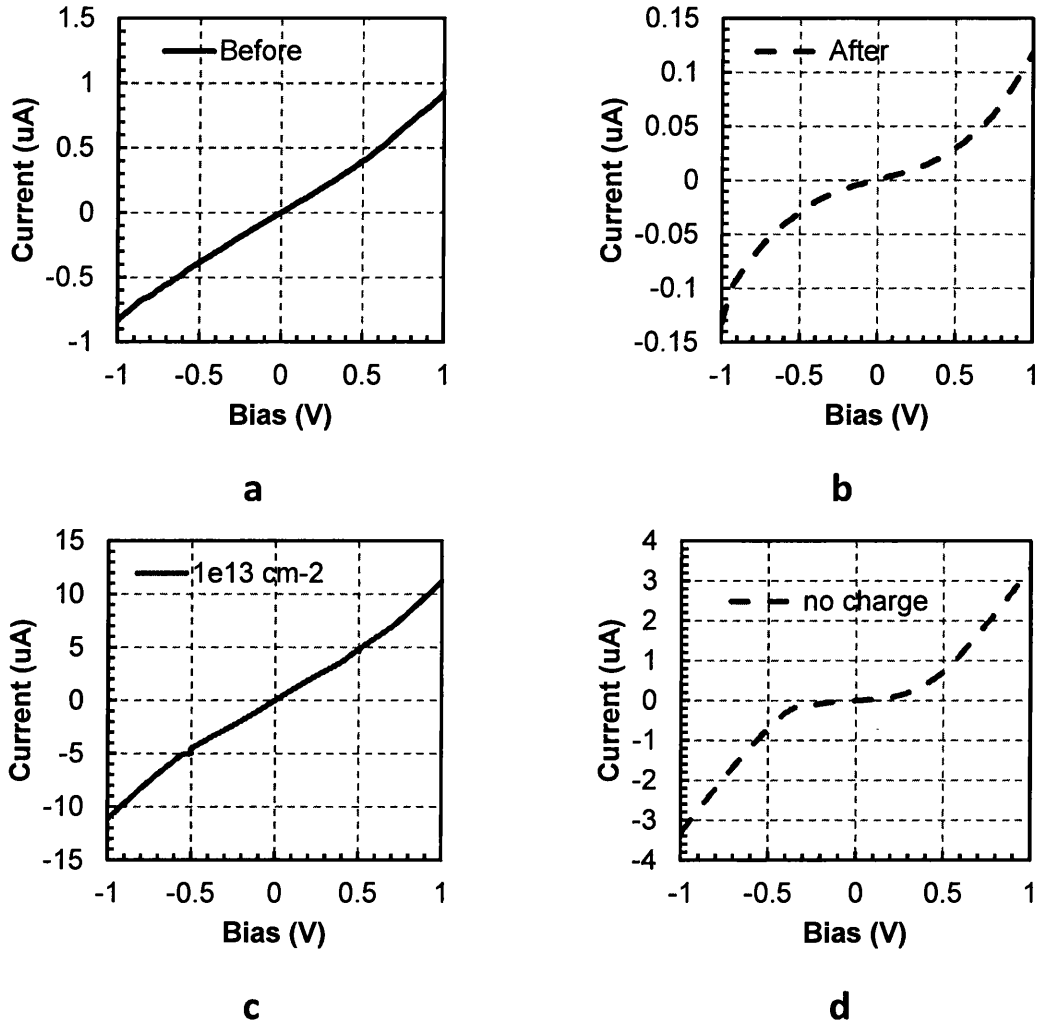

Figure 4.9.2. Measurement results on the hydrothermally grown ZnO nanowires using two probe methods: (a) before argon ion bombardment and (b) after argon ion bombardment. Simulation results using a 3D nanowire structure with metal tip when (c) the fixed charge of 10^{13} cm^{-2} is present at the surface and (d) without surface charge.

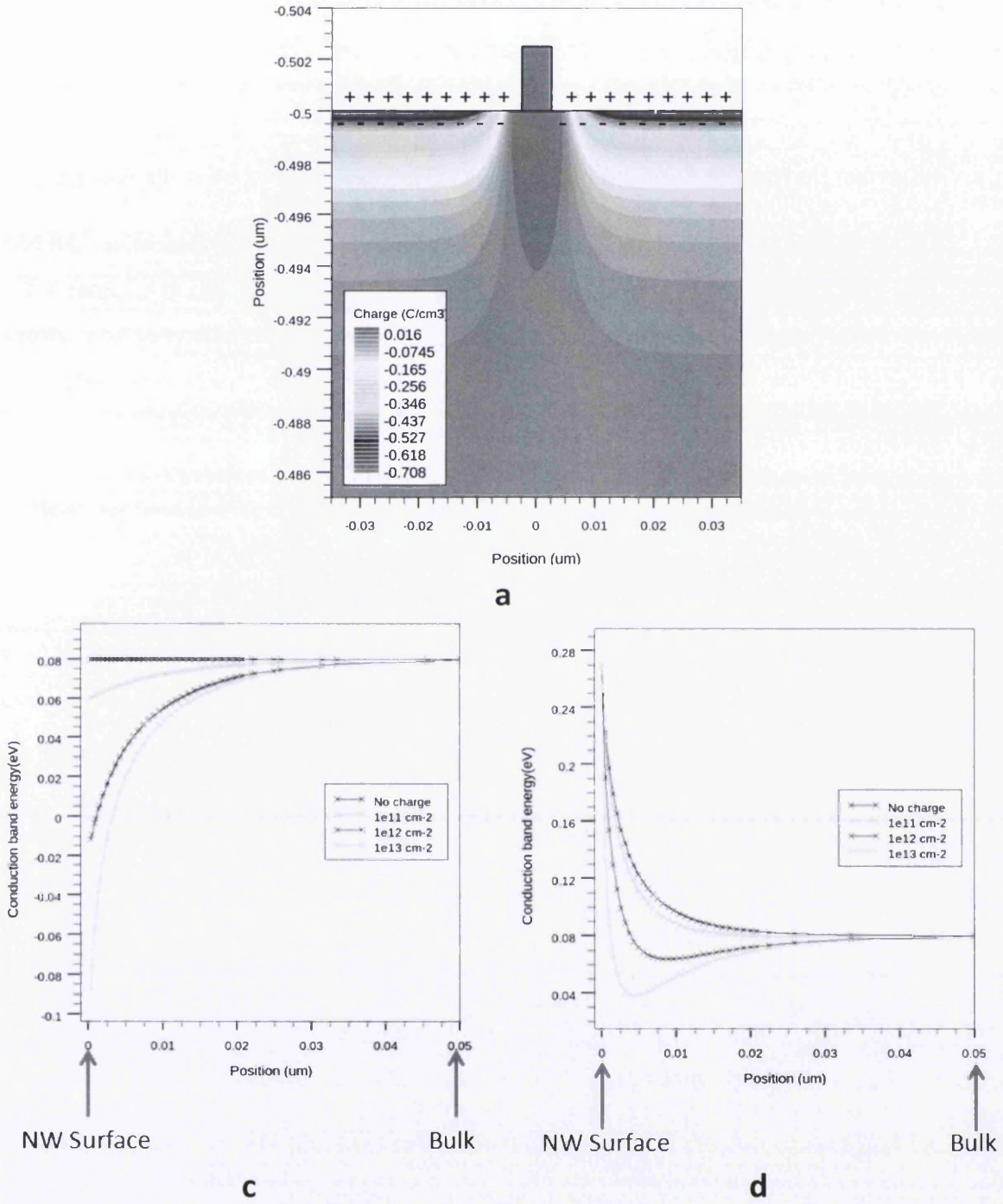

Figure 4.9.3 (a) Charge distribution at the surface of the ZnO nanowire with a surface charge concentration of 10^{13} cm^{-2}. (b) Conduction band profile at the nanowire-insulator interface. (c) Conduction band profile at the nanowire-metal interface at the edge of the tip.

4.9.2 Surface charge in end-bonded Au-ZnO nanowires

Vapour phase catalytic ZnO NWs are known to adsorb ions of O_2^- and OH^- hydroxyls on the surface when exposed to the air. Surface states will be induced on the surface of the NWs acting as electron traps and pushing electrons away from the surface to the bulk [33].

To investigate the effect of surface charge in end-bonded Au-ZnO nanowires the NW structure with 73 nm diameter and Au particle of 47 nm diameter as seen in Chapter 4.4 is used. A range of charge densities were included on the nanowire side: negative charge deficiency (acceptor type states), for negative charge abundance (donor type states), no charge was included on the top nanowire face.

Deficiency of the surface charge leads to a depletion layer while abundance leads to

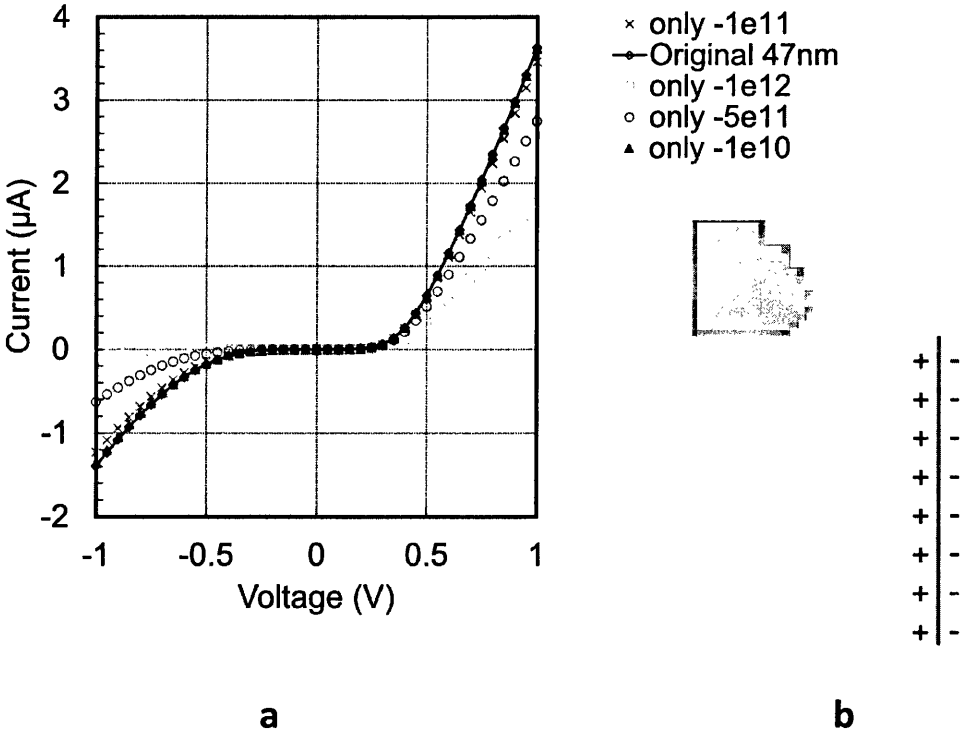

Figure 4.9.4 (a) The simulated I-V for ZnO NW diameter 73 nm, Au diameter 47 nm. The occupied acceptor type surface charge density is: no charge (blue ◊), 1×10^{10} cm^{-2} (purple Δ), 1×10^{11} cm^{-2} (green ×), 5×10^{11} cm^{-2} (orange □), 1×10^{12} cm^{-2} (red ○). (b) Schematic representation of the acceptor type surface charge on the NW side surface.

surface accumulation. Accumulation on the nanowire side faces has minimal effect over the case of no charge. Therefore, we examine only the depletion region formed at the nanowire side surface. Figure 4.9.4(a) shows the nanowire transport behaviour becomes more Schottky-like as the surface acceptor states (Figure 4.9.4(b))increase in density leading to a greater depletion of the nanowire side faces creating a narrow conduction channel. This effect is effectively the same as reducing the nanowire diameter as seen in Chapter 4.6. As a result the rectification ratio will be increased with the increase of NW diameter making contact more Schottky. As the acceptor charge density increases the size of the conducting channel is decreased resulting in decreased current magnitude at the forward bias.

The nanowire top face around the Au contact is the sloping with $\{1\bar{1}01\}$ faces that

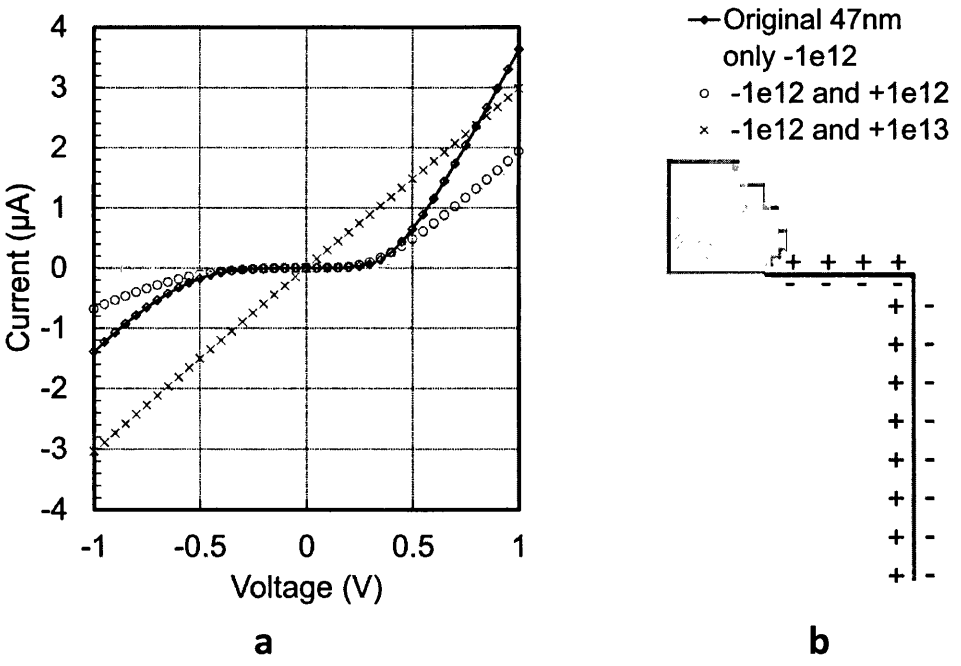

Figure 4.9.5 (a) The simulated I-V for ZnO NW diameter 73 nm, Au diameter 47 nm. Original I-V characteristic without surface charge is marked with blue (◊). All other simulation data was created for the occupied acceptor type charge density of 1×10^{12} cm^{-2} at the side of the NW surface. Occupied donor type surface charge density on the top face used in the simulation: no top charge (orange □), 1×10^{12} cm^{-2} (red ○), and 1×10^{13} cm^{-2} (green ×). (b) Schematic representation of the acceptor type surface charge on the NW side surface and donor type surface charge density on the top face of the NW.

extend from the nanowire $\{01\bar{1}0\}$ side facets to join the Au contact interface and (0001) nanowire top facet. The defective nature of the sloping faces $\{1\bar{1}01\}$ results in increased deep donor oxygen vacancies and shallow donor zinc interstitials which are expected to act in accumulation, although it is difficult to accurately estimate an accumulation density [45]. To study this further we examine accumulation charge densities (donor type states) on the nanowire top face around the contact with simulations.

Figure 4.9.5(b) schematically shows that in simulation charge accumulation is introduced around the contact edge at the top surface of the NW. On the side surface of the NW charge depletion is present. Charge accumulation will result in more pronounced edge tunnelling effect (as seen in Chapter 4.9.1) even when a depletion region is present on the nanowire side. Current-voltage characteristics in Figure 4.9.5(a) demonstrate a transition between Schottky to linear Ohmic behaviour.

4.10 Summary

The simulations of nano-contacts in this work extend beyond previous works necessitating a full 3D finite-element analysis and allowing quantifiable results to be calculated and complex geometries to be taken into account. The results here provide a fundamental understanding of the transport processes surrounding metal contacts to nanowires and also a practical method to fabricate Schottky or Ohmic contacts to nanowires where the interface is abrupt.

The work has demonstrated that the experimental transition between Ohmic and Schottky behaviour is related to the ratio of the interface area to the nanowire cross-sectional area using full 3D simulations. A clear transition occurs at a contact-to-nanowire area ratio of 0.6 that is heavily influenced by geometric effects and enhanced tunnelling at the contact periphery. When the contact-to-nanowire area ratio is smaller than 0.6 then the contact size will influence the electrical properties of the structure with the Schottky contacts forming for the bigger contact diameters and Ohmic contacts forming for the smaller contact diameters. The work in this Chapter has been included into publication: Alex M. Lord, Thierry G. Maffeis, Olga Kryvchenkova, Richard J. Cobley, Karol Kalna, Despoina M. Kepaptsoglou, Quentin M. Ramasse, Alex S. Walton, Michael B. Ward, Jürgen Köble, Steve P. Wilks, "Controlling the electrical transport properties of nanocontacts to nanowires" submitted to *Nano Letters*.

Simulation predicts that due to the complex geometry of the end-bonded ZnO NWs the effect of the current crowding will happen around the metal contact at the edge of the contact. For the Schottky contacts, the increase in the NW diameter will lead to a parasitic effect of current crowding at reverse bias occurring at the edge of the contact away from the contact interface. Current crowding at forward bias will occur directly at the metal-semiconductor interface. This explains experimentally observed phenomena of metal contact melting in side-bonded Ohmic contacts of ZnO nanowires [17]. The work was presented on ANM 2014, Fifth International Conference on Advanced Nanomaterials, July 2014, Aveiro, Portugal, and was accepted for the publication in the *Materials Today Proceedings* entitled O. Kryvchenkova, K. Kalna, R. J. Cobley, "The Current Crowding Effect in ZnO Nanowires

with an End-Bonded Metal Contact". It was also presented on the UK Semiconductors 2014, July 2014, Sheffield UK entitled O. Kryvchenkova, K. Kalna, R. J. Cobley, "Modelling Current Crowding Effect in the ZnO Nanowires".

The full 3D model was implemented for the thermal calculation of the free-standing ZnO nanowires with the end bonded contacts. The current crowding will lead to a significant heat generation with a rise of the local temperature up to 1337 K which will result in device failure due to the contact melting. This identifies the need to engineer the contacts to reduce the barrier narrowing near the contact edges or use a method to allow generated heat to flow away from the interface more efficiently. This work was presented at ASDAM 2014, The Tenth International Conference on Advanced Semiconductor Devices and Microsystems, October, 2014, Smolenice, Slovakia, and submitted for the publication in the conference proceeding entitled Kryvchenkova, O.; Kalna, K.; Cobley, R.J., "Modelling heating effects due to current crowding in ZnO nanowires with end-bonded metal contacts," *Advanced Semiconductor Devices & Microsystems (ASDAM), 2014 10th International Conference on* , vol., no., pp.1,4, 20-22 Oct. 2014

The combination of the measurement and simulation results demonstrates that the electrical properties of the ZnO nanowires with a metal contact can be manipulated by the surface charge. The positive charge density at the surface (donor type states) will result in electron accumulation in the nanowire near the surface. This will lead to the reduction in the barrier width at the metal-nanowire interface and increase in the tunnelling current making the contact Ohmic. The negative charge at the NW surface (acceptor type states) will result in the narrower conduction channel making the contact Schottky. This work is in the preparation for publication.

The work in this chapter was also presented as an invited talk in National Physical Laboratory, NPL, London, October 2014.

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Chapter 5 Results of semiconductor device modelling

5.1 In_2O_3 thin film transistor in the presence of scanning probe

Electrostatic force microscopy (EFM) and scanning Kelvin probe force microscopy (KPFM) are contactless methods which allow investigation of electronic properties of a material surface like work function of metals, band bending of semiconductors, and electrical polarization of surface due to presence of surface charge [1]. The obtained surface potential provides a map of local energy distributions and surface states [2]. Potential mapping of transistors under operation using EFM or KPFM can be performed with a resolution of about 100 nm [1]. The detailed explanation of EFM measurement procedure is given in Chapter 1.1.

Measurements of the surface potential on transistors under operation can be intricate because during device operation charges are continuously created and transported across the device [2]. Measurement result will include not only intrinsic electrical properties of the sample but also measurement artefacts due to presence of a tip: surface potential signal is averaged over a finite area of the sample surface and includes interaction with the tip. A measurement result was found to depend on the tip-sample distance and AC potential applied on the tip [2], tip apex radius [3], cone-pyramid lateral surface of the tip and cantilever shape [4].

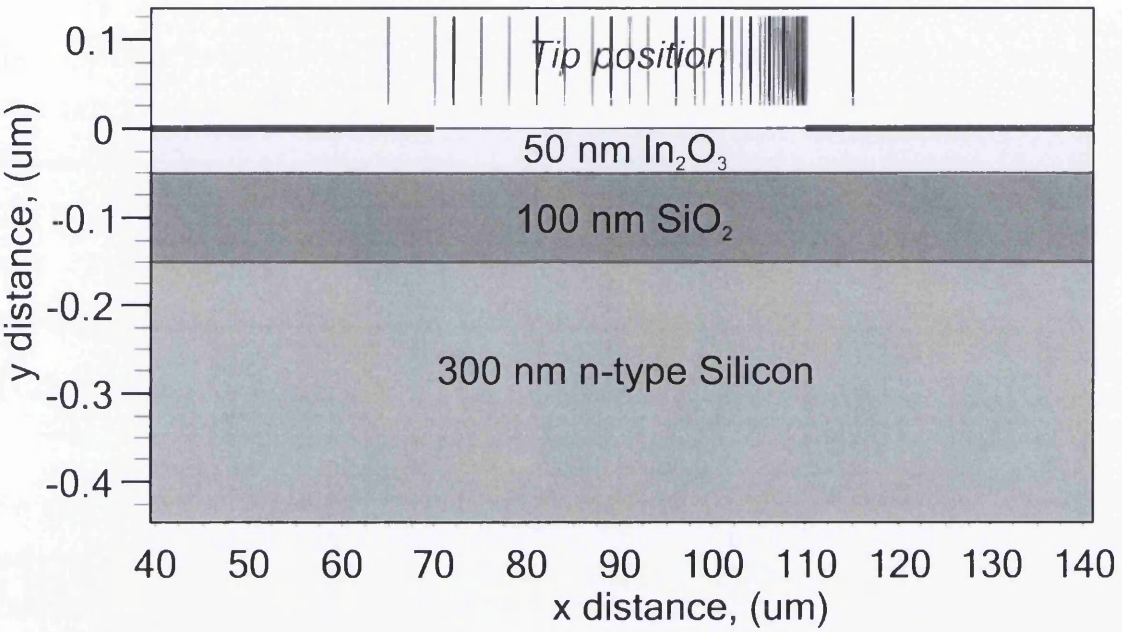
The force contribution of the tip apex at the various tip-sample separations was found to be the smallest and this contribution will further reduce as the tip-sample separation is increased. Cantilever shape has the largest force contribution which increases as the tip-sample separation is increased [4]. When measurements of the surface potential between

source and drain side of the transistor is performed, the measured potential was also found to depend on the tip orientation (parallel or orthogonal) relative to the channel [1]. As a result, the following measurement artefacts are typically found in the measured surface potential: (i) potential is not constant over metal electrode areas, (ii) the channel edge cannot be determined precisely because the highest curvature in the surface potential is not corresponding to the channel edge, (iii) full bias applied to the drain electrode is not visible [1], [5]–[8].

Uncoupled non-simultaneous simulations of KPFM surface potential profile obtained after scanning a semiconductor heterostructure was performed by Robin *et al.* [10] using Silvaco Atlas [9]. No tip structure was included in the simulation. The potential profiles were obtained as a convolution of simulated surface potential and measured tip transfer function [10], [11].

Simulations of EFM and KPFM surface potential profile with full tip and cantilever structure were demonstrated in the literature. In these simulations, the tip induced band banding was considered negligible [2], [6]. When investigating semiconductor surfaces, the electrostatic force between the tip and sample is nullified by setting the contact potential difference (V_{CPD}) between the tip and sample to be equal to the applied constant voltage (V_{DC}) on the tip. Also, when $V_{CPD}= V_{DC}$ tip induced band bending at the sample surface is zero [6]. This approach to nullify the electrostatic force between the tip and sample was shown to be valid for metal-metal infinite plates. However, it is not always valid for metal-semiconductor material system because when experiment is performed with n-type silicon tips or on semiconductor sample surface the charges are distributed inside the semiconductor over a distance near the surface and a charge distribution will depend on the tip-sample separation [1], [12].

In this Chapter, an electrostatic tip apex interaction with the In_2O_3 thin film transistor (TFT) under operation is considered using a combination of experimental technique and simulation in Silvaco Atlas 2D [9] for a different doping level of In_2O_3 channel layer.



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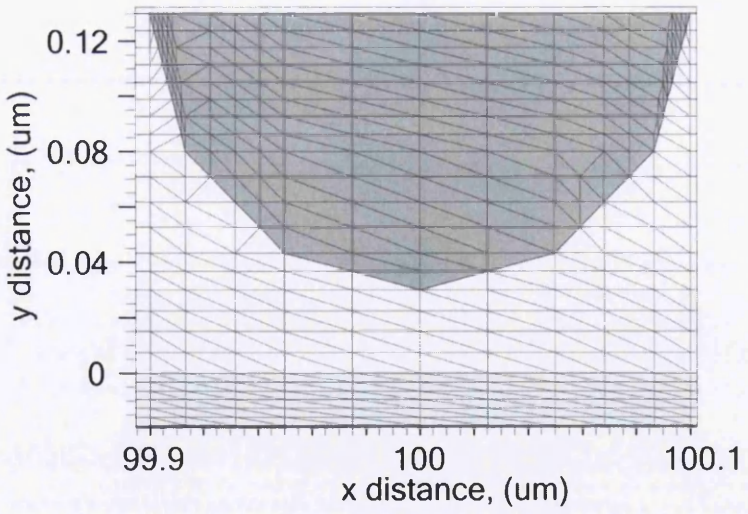


b

Figure 5.1.1 (a) Simulated In_2O_3 TFT structure with channel length L=40 μm. Only 100 μm of the structure length is shown. (b) Simulated tip structure with mesh for the tip radius of 100 nm. 30 nm tip-sample separation is used in the simulation.

5.1.1 Geometry approximation of In_2O_3 TFT and scanning tip

In_2O_3 TFT is a bottom gate transistor. The main principle of In_2O_3 TFT operation is described in Chapter 1. Experimental data was obtained for the number of transistors with channel length L of 30-40 μm and device width W of 200-1500 μm. Figure 5.1.1(a) shows In_2O_3 TFT structure used in the simulation. The structure was created in Silvaco Atlas [9]. For the simulation L=40 μm channel length was selected. The aluminium source and drain electrodes are 70 μm in length parallel to the channel as found in the fabricated In_2O_3 TFTs. In the simulation the following geometry used: 50 nm n-type In_2O_3 conducting channel layer with doping concentration of 3.5×10^{17} cm^{-3}, 100 nm SiO_2 insulator layer and 300 nm n-type Si substrate layer with doping concentration of 10^{18} cm^{-3} followed by the bottom Al gate.

To investigate the surface potential in the presence of a scanning tip apex, a Si tip with 100 nm radius was created using DevEdit toolbox and placed 30 nm above the transistor surface (Figure 5.1.1(b)). The tip was then moved above the surface with a changing step size with more positions considered at the drain side as seen in Figure 5.1.1(a). In total 33 different tip positions above the transistor structure are used in simulation but each simulation will be performed for a single tip position. To implement the tip movement 33 different DevEdit structures are needed. To make the process of creating an Atlas input script automated, a Matlab script (see Appendix) was created to vary the tip position and create a set of DevEdit coordinates for 33 structures. The tip radius, the tip-sample separation, the tip position and applied biases are used as free input parameters in the Matlab script.

Other material parameters used in the simulation are: In_2O_3 permittivity of 8.9 [13], bandgap of 4 eV, affinity of 4.45 eV [14], field-effect mobility 2 $cm^2/V\times s$, electron effective mass $0.3m_0$ (m_0 been the electron mass in vacuum) [15]. The tip work function was considered to be 4.6 eV. An Ohmic contact between Al source, drain and gate electrodes is assumed which are calibrated to give a negative threshold voltage of −3.8 V as seen in measurements.

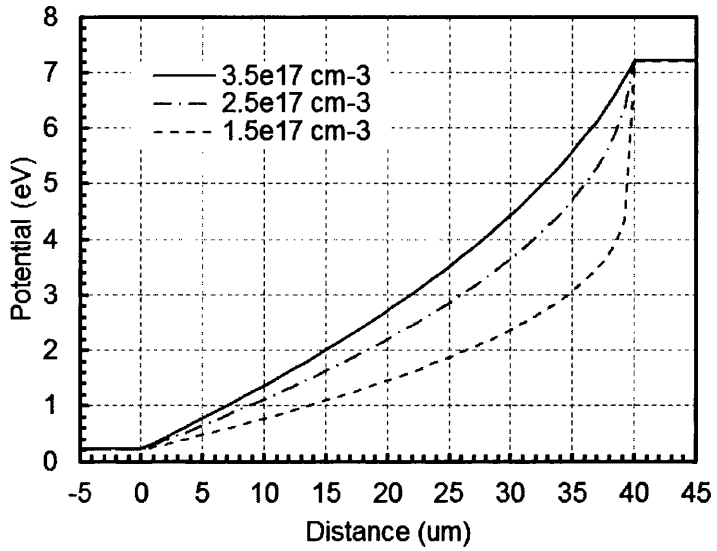


Figure 5.1.2 Simulated surface potential profiles at V_{GS}=0 V, V_{DS} =7 V for different doping concentrations of In_2O_3 channel layer: 1.5×10^{17} cm^{-3}, 2.5×10^{17} cm^{-3} and 3.5×10^{17} cm^{-3}.

5.1.2 Effect of doping concentration in In_2O_3 channel layer

The intrinsic doping level in solution-processed metal oxides like In_2O_3 is estimated to be in the range of 2×10^{17} to 6×10^{17} cm^{-3}.

Simulation results in Figure 5.1.2 shows surface potential profiles with no tip structure included in the simulation when doping concentration of In_2O_3 layer changes from 1.5×10^{17} cm^{-3} to 3.5×10^{17} cm^{-3}. For the higher doping levels, the profile is closer to linear. It was suggested earlier in the literature that for organic field-effect transistors a lower surface potential through the channel indicates lower mobility of the device [16].

Figure 5.1.3 demonstrates measured EFM surface potential profiles with grounded source and gate and varying drain bias (V_{DS}) between 0 and 8 V for In_2O_3 (double-spin) TFT width W = 200 μm and In_2O_3 (single-spin) TFT width W = 1500 μm, both transistors have channel length L = 40 μm. It can be seen from the profiles that a double-spin TFT in Figure 5.1.3(a) has a higher potential at the centre of the channel in comparison to single-spin TFT in Figure 5.1.3(b) indicating a higher mobility in double-spin device suggested earlier from the simulation. Indeed, there is 2 orders of magnitude difference in the drain current of two

devices in the saturation regime: the double-spin TFT has a drain current of 3.35×10^{-8} A/μm (Figure 5.1.3(c)) and the single-spin TFT has a drain current of 5.66×10^{-10} A/μm (Figure 5.1.3(d)) at V_{GS} =10 V and V_{DS} =16 V.

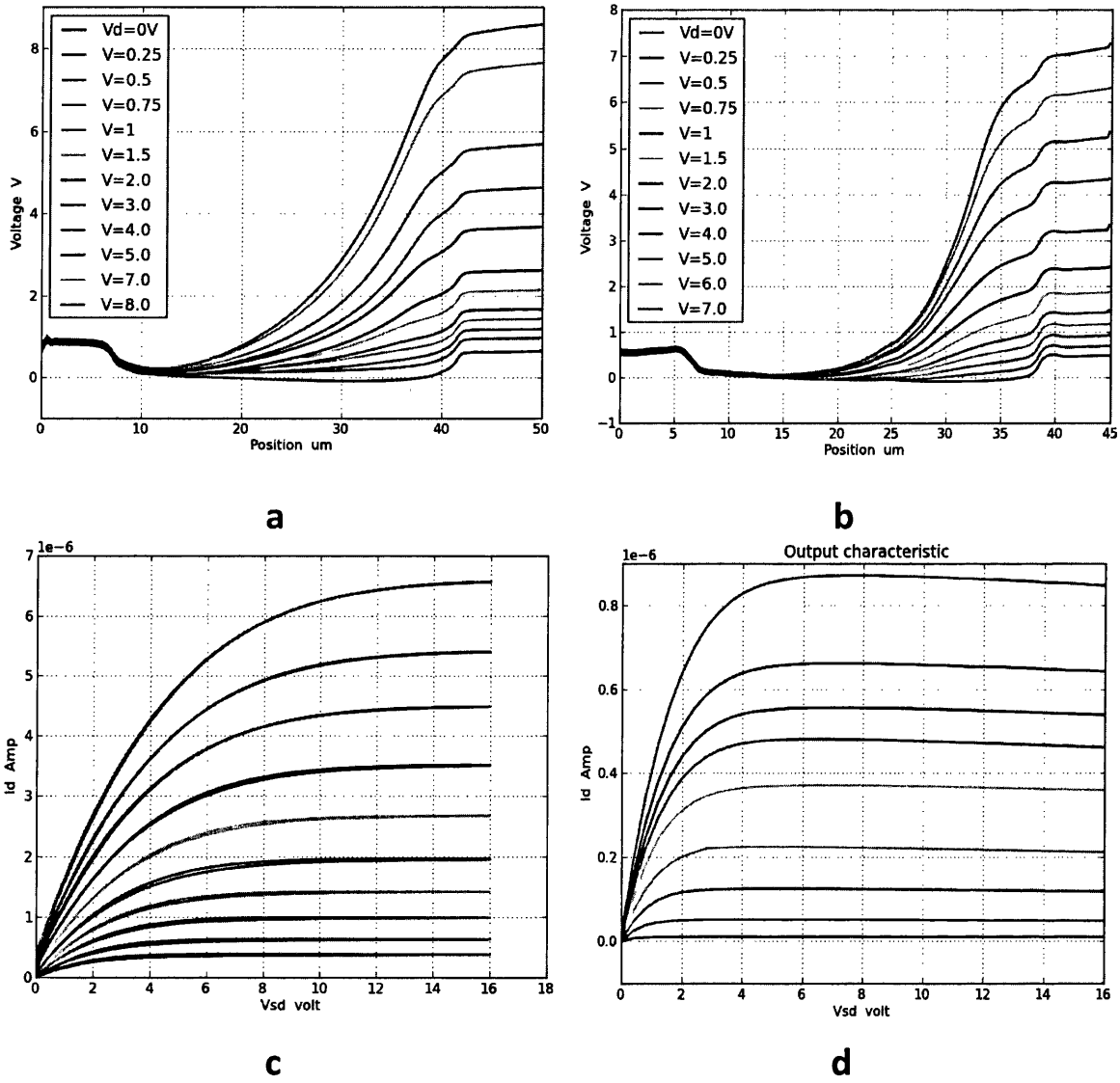


Figure 5.1.3 In (a) and (b) EFM profiles with grounded source and gate, varying V_{DS} between 0 and 8V. Profiles obtained for (a) In_2O_3 (double-spin) TFT, device width W = 200 μm and channel length L = 40 μm. Profiles obtained for (b) In_2O_3 (single-spin) TFT, device width W = 1500 μm and channel length L = 40 μm. (c) Output characteristic of the device in (a). (d) Output characteristic of the device in (b).

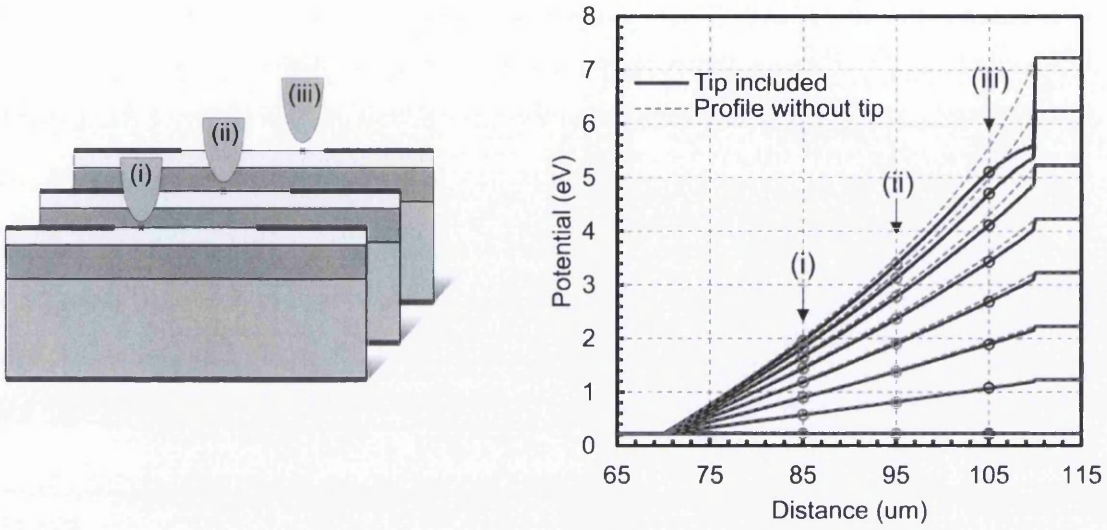


Figure 5.1.4 (a) Schematic of the simulated tip movement, 33 tip positions are used in total. Surface potential acquired at one point under tip apex for each tip position ((i), (ii) and (iii)) and used to reconstruct surface potential profile in (b). (b) Simulated surface potential for grounded source, gate and tip and varying drain bias from 0.1 V to 7 V. Profiles without tip (dashed line) and with tip of 100 nm radius and tip-sample separation of 30 nm (solid line).

Both experimental and simulation data demonstrate that in the In_2O_3 TFTs a surface potential through the length of the channel is increasing with the increasing doping.

Additional experimental data for L = 40 μm and L = 30 μm can be found in Appendix.

5.1.3 Surface potential in the presence of a tip apex

Potential profiles in Figure 5.1.3(a) and (b) have the following typical measurement artefacts: (i) potential is not constant over metal electrode areas and it is varying by ~0.3 V, (ii) for both devices with L=40 μm the channel edge cannot be determined precisely and the channel length appears as 35.85 μm in the double-spin device in Figure 5.1.3(a) and 28.6 μm in the single-spin device in Figure 5.1.3(b), indicating an error of 28.5% and 10.3%, respectively, in the measurement of the channel length. In the double-spin device with higher

mobility this error is lower due to a larger screening effect of dopants in the channel. (iii) Full bias applied to the drain electrode is not visible at the high drain biases: in Figure 5.1.3(a) a potential scan above the drain electrode when V_{DS} =8 V is applied measure the applied V_{DS} bias of 7.57-7.79 V.

All listed above errors are related to the known effects of the cantilever broadening discussed earlier in this chapter. The non-linearity at the drain side is present for both TFTs resulting in flattening of the potential at the drain side on the profiles in Figure 5.1.3(a) and (b). We relate this effect to the electrostatic interaction with the tip apex which will be demonstrated in this chapter.

To simulate the effect of the tip apex on the resulting potential profile, an In_2O_3 TFT with n-type channel layer and a doping concentration of 3.5×10^{17} cm^{-3} is used. When the tip structure is included in the simulation tip is considered at 33 different tip positions and every simulation is performed for a single selected tip position as explained earlier (Figure 5.1.1(a)). For each tip position, the value of the potential will be extracted at the point directly

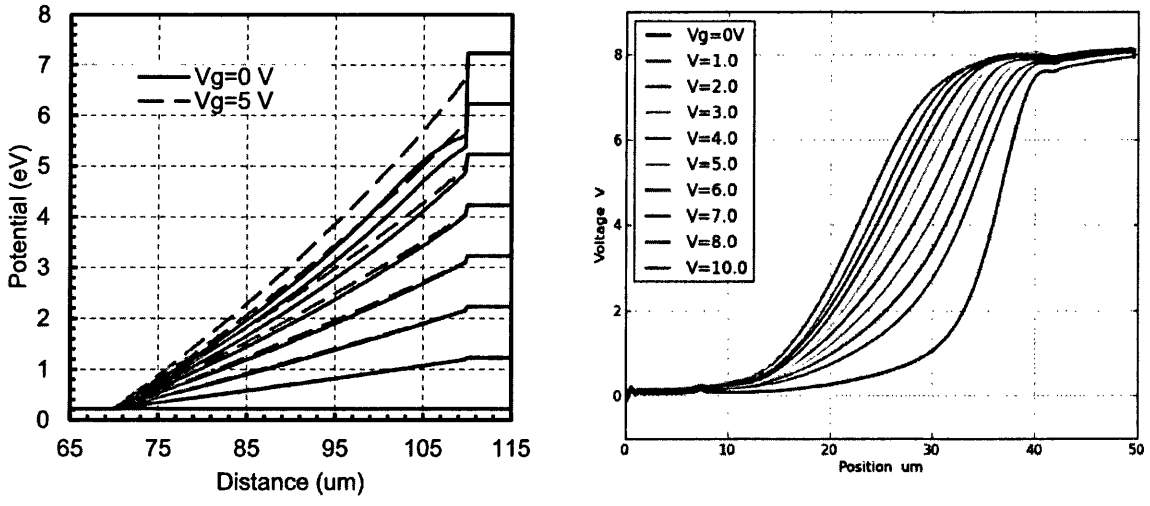


Figure 5.1.5 (a) Simulated surface potential for grounded source and tip and varying drain bias from 0.1 V to 7 V at gate biases of 0 V (solid line) and 5 V (dashed line) is applied. (b) Measured surface potential for the double-spin In_2O_3 TFT with grounded source, drain bias of 8 V and varying gate bias from 0 V to 10 V.

under the tip apex at a surface of the transistor for a range of applied drain, gate and tip biases (Figure 5.1.4(a)). Then, using Matlab script (see Appendix), values of surface potential from 33 tip positions is combined and a potential profile is reconstructed for each setup of the applied biases as shown in Figure 5.1.4(b).

Figure 5.1.4(b) shows simulated surface potential for a grounded source, gate and tip and varying drain bias from 0.1 V to 7 V without a tip and with a tip of a radius of 100 nm and a tip-sample separation of 30 nm. Just like in the measurement data in Figure 5.1.3(a) and (b), a deviation from the linear profile and flattening of the potential near a drain electrode is seen in the simulation. This effect is more pronounced at the higher drain biases. The flattening occurs due to the tip induced band banding which becomes higher at the drain side when the drain electrode is biased. The effect of the tip is depleting electrons from the transistor surface. Resulting measured potential is reduced by electrostatic interaction with a tip creating a flat region on the potential scan near the drain electrode. The simulation demonstrates that this error will be higher for lower doping levels due to the lower dopant screening effect.

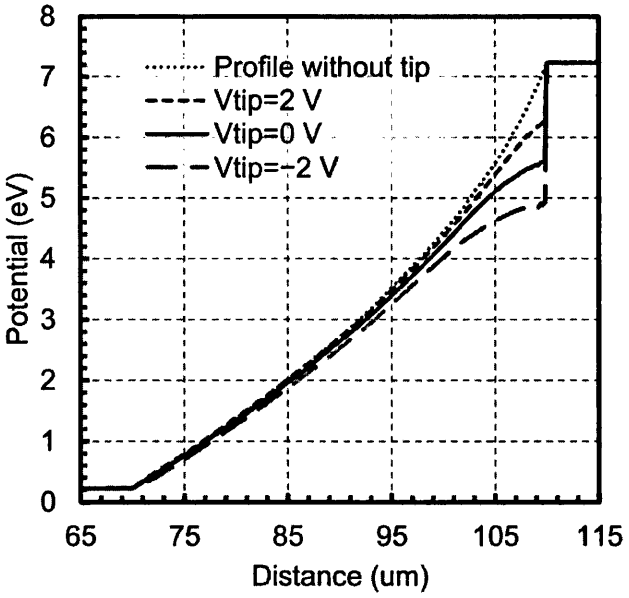


Figure 5.1.6 Simulated surface potential for grounded source and gate when drain bias of 7 V is applied for the different applied tip biases: −2 V, 0 V and 2 V. Simulated surface profile without tip is also given for the reference.

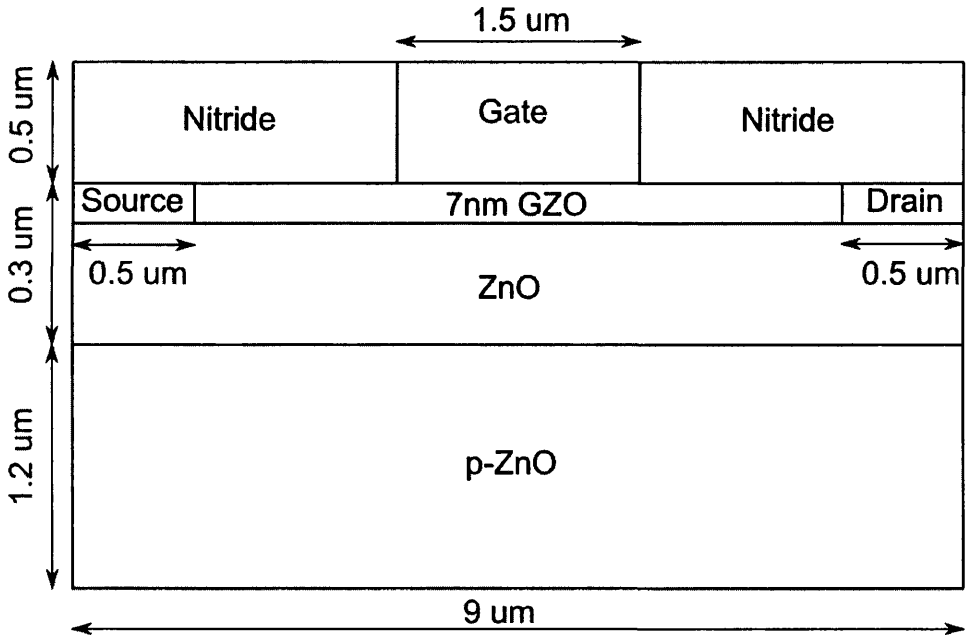
Figure 5.1.5(a) shows simulated surface potential for grounded source and tip and varying drain bias from 0.1 V to 7 V at gate biases of 0 V and 5 V. A high gate bias will increase a surface potential through the channel making the profile more linear. This is due to the increase in carrier concentration and mobility in the channel when a high gate bias is applied. Similar effect is observed in measured potential profiles in Figure 5.1.5(b) performed for the double-spin In_2O_3 TFT with grounded source, drain bias of 8 V and varying gate bias from 0 V to 10 V. Measured profiles become more linear and potential at the centre of the channel increases as a gate bias is increased.

Simulation in Figure 5.1.5(a) also demonstrates that a higher carrier concentration in the channel at the applied V_{GS} =5 V will also lead to a higher screening effect from the tip which results in a smaller deformation in the potential profile at the drain side. An error due to the electrostatic interaction with a tip apex can be reduced by applying gate bias which will increase the screening effect of electrons in the channel.

It is known that an amount of the tip induced band bending can be manipulated by the applied tip bias [6]. As seen in Figure 5.1.6, an applied tip bias of −2 V can further increase an error due to the potential profile flattening at the drain side and a tip bias of 2 V can reduce an error by reducing an electrostatic influence of the tip on the sample. A tip bias has to be further increased beyond 2 V to fully compensate the tip apex influence on the measured surface potential profiles in In_2O_3 TFTs.

5.2 ZnO/GZO polarization heterostructure field effect transistor

Field effect transistors with the operation based on the effect of the creation of two-dimensional electron gas (2DEG) [19] which provides a higher carrier mobility in the channel due to reduced scattering were demonstrated earlier in the literature for the materials like GaAs/AlGaAs and GaN/AlGaN [19], [20]. A carrier confinement in $ZnO/Mg_xZn_{1-x}O$ material system is similar to GaAs/AlGaAs and GaN/AlGaN material systems making $ZnO/Mg_xZn_{1-x}O$ a good candidate for transistor applications [19], [20]. The first structure of



Doping concentrations:	
n-type GZO	10^{19} cm^{-3}
n-type ZnO	10^{16} cm^{-3}
p-type ZnO	10^{17} cm^{-3}

Contact work functions:	
Gate	5.2 eV
Source	3.67 eV
Drain	3.67 eV

Figure 5.2.1. Geometry approximation, doping concentrations and contact work functions of simulated GaZnO/ZnO polarization HFET.

n-channel depletion mode ZnO/$Mg_{0.3}Zn_{0.7}O$ heterostructure field effect transistor (HFET) was suggested by Koike *et al.* in 2005 [21]. More details on the operation of ZnO/$Mg_{0.3}Zn_{0.7}O$ HFET are provided in Chapter 1.2.

Ga doped ZnO (GZO) thin films have polycrystalline nature [22]. GZO is an n-type material, and its doping concentration observed in the experiment varies from 5×10^{19} to 1.96×10^{21} cm^{-3} [17], [22], [23]. An increase in the carrier concentration in highly doped n-type materials due to Burstein-Moss effect will block the lowest states in the conduction band by excess electrons and enlarge the bandgap [22], [24]. Indeed, the band gap of GZO depends on the doping concentration and it was measured to be 3.16-4.9 eV [17], [22], [23]. In addition, there is a stress and strain in the as deposited GZO thin films due to a lattice disorder caused by defects and presence of Ga atoms [22]. That is why ZnO/GZO heterostructure will have a band gap shift and a formation of 2DEG at the ZnO/GZO interface is possible [25] due to polarization difference. This makes this material system a good candidate for HFET application [26]. In this chapter, a theoretical structure of ZnO/GZO HFET is suggested using 2D modelling in Silvaco Atlas [9].

The investigated ZnO polarisation field effect transistor (FET) is based on a GaZnO/ZnO heterostructure assuming a metal gate and the source/drain in direct contact with a channel at the heterointerface. Device structure is outlined in Figure 5.2.1. The simulated device has a gate length of 1.5 μm assuming a 0.5 μm source and drain width deposited in parallel to the 8 μm long channel. In the simulated HFET, the channel is formed between a 7 nm GZO layer and a 0.293 μm n-type ZnO layer. A 1.2 μm p-type ZnO layer is used as an insulating substrate. To increase the reliability of the device, a 0.5 μm thickness nitride layer is added at the surface of the device to passivate it. This layer will prevent possible chemical reactions between the GZO layer and air in order to reduce a degradation of the device. A ground contact is placed at the bottom of the device. The source and drain contacts have a work function of 3.67 eV and are assumed to form an Ohmic contact with GZO layer; gate has a work function of 5.2 eV.

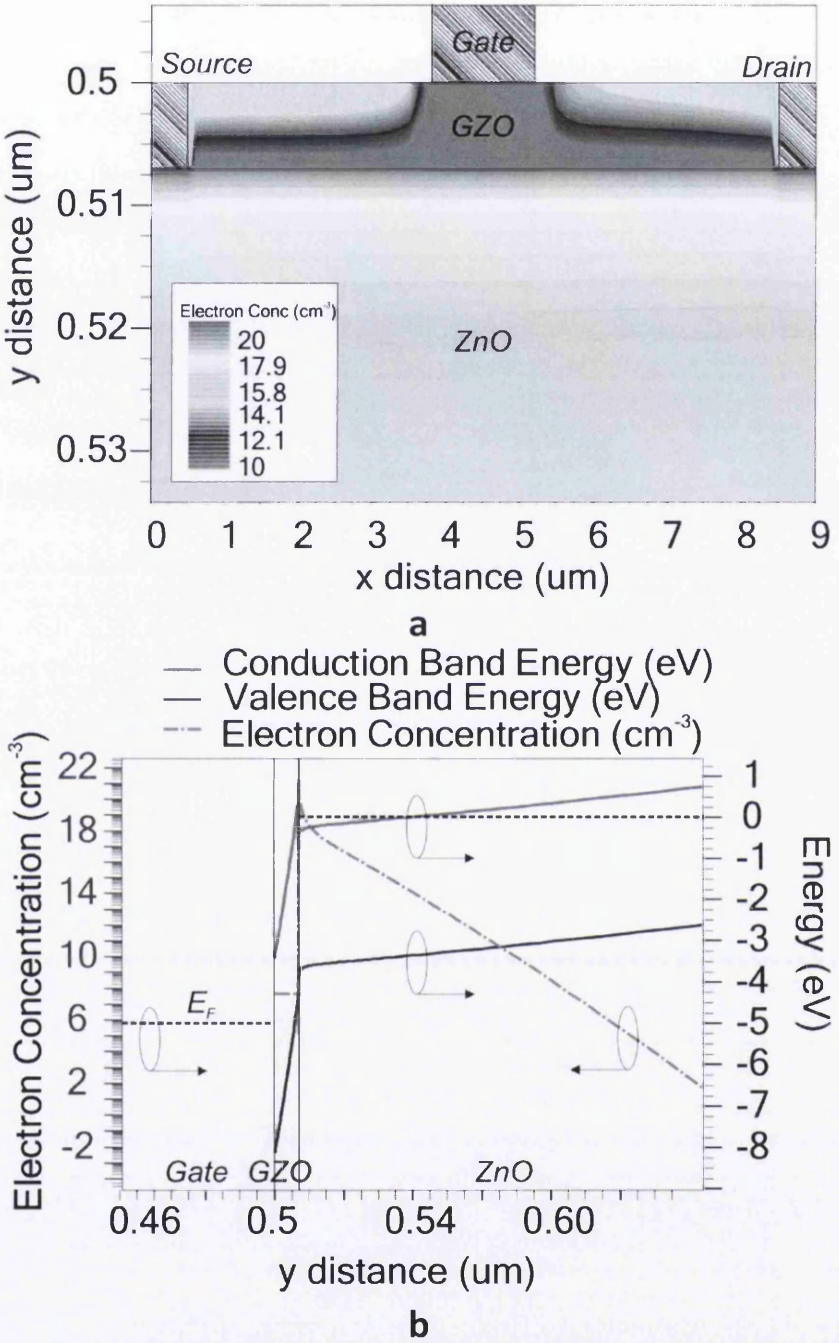


Figure 5.2.2 (a) Simulated electron concentration distribution at grounded source and applied gate bias of V_{GS} =5 V and drain bias of V_{DS} =3 V. The highest electron concentration is at the ZnO/GZO interface where the channel is formed. (b) Band profile and electron concentration at V_{GS}=5 V and V_{DS} =3 V plotted through the centre of the structure in y direction. Fermi level E_F is marked with a blue dashed line.

Due to the presence of the intrinsic defects ZnO is a naturally n-type material. The doping concentration of the n-type ZnO varies from 10^{16} to 10^{21} cm^{-3}. For the present simulations, we use a doping concentration of 10^{16} cm^{-3} [18]. We introduce a p-type ZnO layer with a doping concentration of 10^{17} cm^{-3} in the structure to confine electrons in the channel and to prevent a leakage current. In experiments, the p-type doping concentration of 5.0×10^{16} - 7.3×10^{17} cm^{-3} was achieved in ZnO by using nitrogen-ion implantation [27]. An n-type GZO layer has a doping concentration of 10^{19} cm^{-3}. However, a very high doping concentration in the GZO layer will lead to the formation of the additional channel inside the layer and make a device operation impossible. Other material parameters used for the GZO layer are: a bandgap of 4.5 eV, a mobility 13.51 $cm^2/V\times s$, [22], [28] an affinity of 4.5 eV. No traps or surface charge affecting the surface potential are considered in this work.

Polarization charge will be calculated at the ZnO/GZO interface as a sum of spontaneous and piezoelectric polarizations. The detailed explanation of the polarization model and polarization material parameters used in the simulation for ZnO is given in Chapter 2.5.

The result of calculation of the polarization charges observed at the ZnO/GZO interfaces is given in Table 5.2.1.

Table 5.2.1. Calculated polarization sheet charge per cm^2 at the ZnO/GZO interface.

Region	Spontaneous	Piezoelectric	Total
GZO	-1.098×10^{13} cm^{-2}	-1.120×10^{13} cm^{-2}	-2.219×10^{13} cm^{-2}
ZnO	-2.846×10^{13} cm^{-2}	0 cm^{-2}	-2.846×10^{13} cm^{-2}

Figure 5.2.2 (a) shows simulated spatial distribution of electron concentration when a gate bias of V_{GS}=5 V and a drain bias of V_{DS}=3 V are applied. The highest electron concentration is found at the ZnO/GZO interface where the channel is formed. This is due to the formation of a potential well at the ZnO/GZO interface as seen on a band diagram in Figure 5.2.2 (b) at a gate bias of V_{GS}=5 V and a drain bias of V_{DS}=3 V. In the formed

potential well, electrons cannot move in the direction of the potential well but can freely move in two other directions. The highest electron concentration in the structure is in the channel (Figure 5.2.2 (b)) and reaches 10^{21} cm^{-3}.

Transfer characteristic on a linear scale of the simulated device is shown in Figure 5.2.3 (a) at V_{DS}=0.5 V, 1.5 V and 3 V. The simulated ZnO/GZO is a depletion mode device like most of ZnO/$Mg_{0.4}Zn_{0.6}O$ HFET [48]. Device has a negative threshold voltage of V_{th}=−0.25 V which means that a negative gate bias needs to be applied to switch the device off. Sub-threshold behaviour of the device is shown in Figure 5.2.3 (b) using a transfer characteristics at indicated drain biases on a logarithmic scale. The leakage current is as small as 10^{-13}-10^{-14} A. Output characteristic on a linear scale is plotted in Figure 5.2.3 (c) for V_{GS}= 0 V, 2 V, 4 V and 6 V.

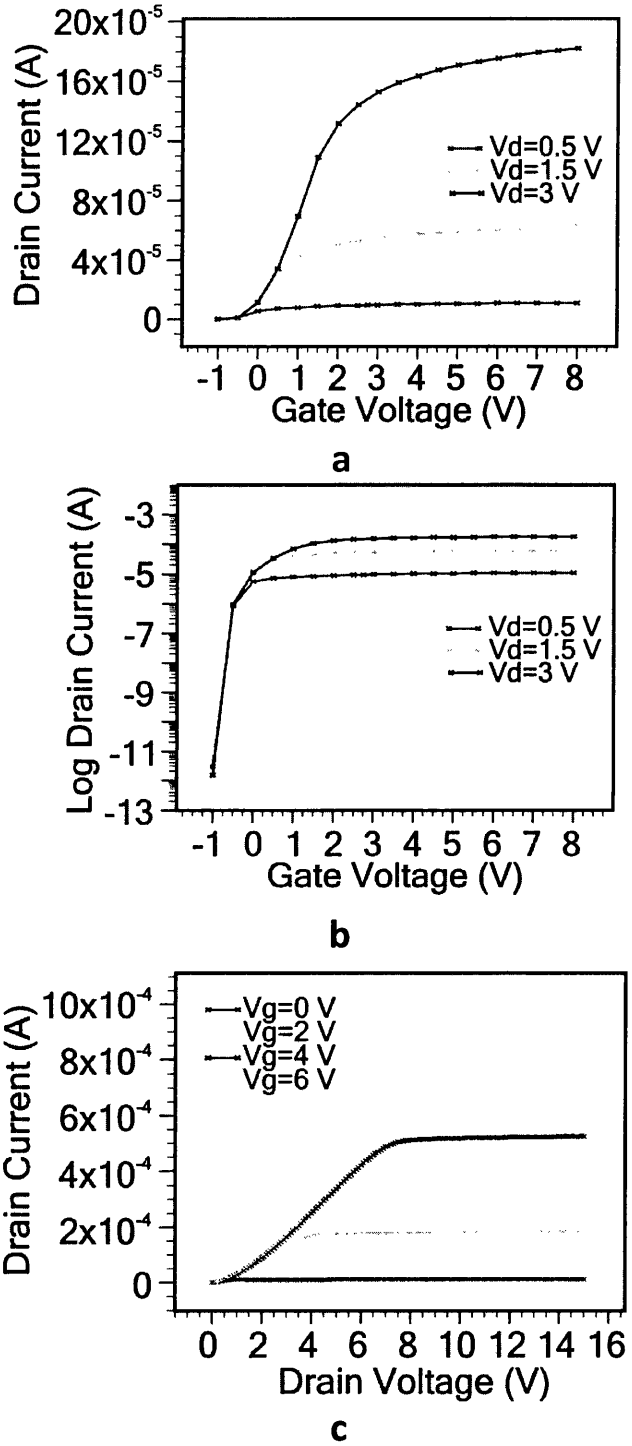


Figure 5.2.3 (a) Transfer characteristics at drain biases of 0.5 V, 1.5 V and 3 V on a linear scale for the drain current. (b) Transfer characteristics at drain biases of 0.5 V, 1.5 V and 3 V on a logarithmic scale for the drain current to see the sub-threshold behaviour. (c) Output characteristics on a linear scale for the drain current at gate biases of 0 V, 2 V, 4 V and 6 V.

5.3 Summary

Electrostatic tip apex interaction with the In_2O_3 thin film transistor (TFT) under operation was studied using a combination of experimental technique and simulation by Silvaco Atlas 2D [9] for a different doping concentration of In_2O_3 channel layer. A higher doping concentration of In_2O_3 channel layer leads to a linear surface potential profile and a higher surface potential through the channel indicates higher mobility of the device.

Experimental potential profiles of the In_2O_3 TFT obtained using EFM method contain the following typical measurement artefacts due to the cantilever broadening: (i) potential is not constant over metal electrode areas and it is varying by ~0.3 V, (ii) for both devices with L=40 μm, the channel edge cannot be determined precisely and the channel length appears as 35.85 μm in the double-spin device and as 28.6 μm in the single-spin device indicating an error of 28.5% and 10.3%, respectively, in the measurement of channel length. In the double-spin device, a higher surface potential indicates a higher doping concentration and as the result a smaller error of 10.3% due to a higher screening effect of dopants in the channel. (iii) Full bias applied to the drain electrode is not visible on the EFM surface potential profile: a potential scan above the drain electrode when V_{DS} =8 V is applied measure the applied V_{DS} bias of 7.57-7.79 V.

Experimental potential profiles of the In_2O_3 TFT contain non-linearity at the drain side resulting in flattening of the potential. Simulation demonstrates that this non-linearity is related to the effect of the tip apex and it is more pronounced at the higher drain biases. The effect of the tip apex is depleting electrons from the transistor surface. Resulting measured potential is reduced by the electrostatic interaction with the tip apex creating a flat region on the potential scan near the drain electrode. The simulation demonstrates that this error will be higher for lower doping levels due to the lower dopant screening effect.

The simulation also demonstrates that when a gate bias of 5 V is applied a carrier concentration in the In_2O_3 channel increases which leads to the higher screening effect from the tip. When the gate bias is applied, the deformation of the potential profile at the drain side is smaller.

An applied tip bias of −2 V can further increase an error due to electrostatic interaction with the tip apex at the drain side but the tip bias of 2 V can reduce an error by reducing an electrostatic influence of the tip on the sample. A tip bias has to be further increased beyond 2 V to fully compensate the tip apex influence on the measured surface potential profiles in In_2O_3 TFTs. The work on In_2O_3 TFT in the presence of scanning probe is currently under preparation for the publication.

A theoretical structure of the ZnO/GZO HFET is suggested using 2D modelling by Silvaco Atlas [9]. Total polarization charge at the ZnO/GZO were calculated to be -2.219×10^{13} cm^{-2} in the GZO layer and -2.846×10^{13} cm^{-2} in the ZnO layer. A band offset and a presence of the polarization charge at the ZnO/GZO interface results in a formation of the potential well and the creation of a 2DEG at the ZnO/GZO interface. That is why the highest electron concentration is at the ZnO/GZO interface where the channel is formed and 2DEG prevents leakage to the gate or ground electrodes. Simulated device has a negative threshold voltage of −0.25 V which means the device would be normally on (a depletion mode transistor). An n-type GZO layer with a doping concentration of 10^{19} cm^{-3} was used in the simulation. At higher doping concentrations of the GZO layer, an additional channel appears which would make the device operation impossible.

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Chapter 6 Summary

Chapter 3 demonstrates an STM and STS simulation methodology based on the Price and Radcliffe tunnelling formalism using image force correction which was developed using Silvaco *ATLAS*. Arbitrary tip shapes can be used in the simulations including a tip with the oxide, as seen in Chapter 3.2. A 2D finite element model was applied to several semiconductor materials to verify its accuracy, with the origin of features in the spectra examined in detail. The simulations confirmed that, at larger doping concentrations, the screening effect of the semiconductor reduces the tip-induced band bending.

Chapter 3.3 demonstrates that for *n*-type GaAs, the modelled spectra band gap deviates from the bulk value by only 0.1 eV or 0.7 % which is within the experimental systematic error. At low *n*-type doping concentrations, the screening is weak, and tip-induced band bending causes the apparent band gap to either increase or reduce depending on the tunnelling mechanism. These phenomena well justify the need for STM and STS modelling to accompany the experimental measurements. Our 2D model, which uses a self-consistent Poisson-Schrödinger solution, predicts a larger tip-induced band bending when a sample is in depletion (resulting in a shift of the band onset in the spectra) than that from Semitip 6 2D model, and the same amount of tip-induced band bending when a full 3D model is used (Chapter 3.4). As demonstrated in Chapter 3.5 and Chapter 3.7 the simulation model used in this thesis is in a good agreement with a model based on the Bardeen tunnelling approach and experimental data.

Chapter 3.6 demonstrates that the image force correction gives a conduction band tunnelling current increase of three orders of magnitude and a valence band tunnelling current increase of six orders when compared to the 'artificial' uniform increase of three orders of magnitude used in the literature. However, the magnitude change is different for different tip shapes and sample materials.

Chapter 3.8 demonstrates that the presence of the oxide on the shank of the probe alters the contact behaviour in contact and non-contact measurements. For contact measurements the presence of oxide on the shank of the probe alters the contact behaviour with the resulting current transport dependent on the voltage polarity. When injecting electrons into the sample, the presence of shank oxide causes a widening of the Schottky barrier compared to removing electrons from the sample. This results in non-equal resistivity in and out for the sample when carrying out contact measurements when the shank oxide is present. This also means that the increased size of the Schottky barrier increases the resistance of the contact when the probe oxide is present. Both of these results confirm that the assumption that contact type is irrelevant in 4pp measurements is violated. When in the non-contact regime, the main shifts in the spectra occur when the sample is in depletion, where a tip-induced quantum dot is created in the sample below the probe. The shape and size of the induced quantum dot is altered by the electrostatic field from the tip, which is governed by the oxide coating.

Finally, our STM model developed in Chapter 3 within a commercial simulation tool offers several advantages over other STM models. These advantages include i) the ability to use any realistic tip shape, ii) to include full device transport models for SPM on devices, and iii) to model spectra from SPM on powered devices. The model can also account for surface states, and can readily be extended to other SPM techniques.

Chapter 4 explains a geometry and size dependant electrical behaviour of ZnO nanowires with Au particle deposited on top or when the metal probe is forming a contact with the sample.

Experimental transition between Ohmic and Schottky behaviour (Chapter 4.2) was related to the ratio of the interface area to the nanowire cross-sectional area using full 3D simulations with a complex approximation of the metal contact geometry (Chapter 4.3). The main current transport in the structure is due to the enhanced tunnelling at the contact periphery (Chapter 4.4). When the contact-to-nanowire area ratio is smaller than 0.6 then the contact size will influence the electrical properties of the structure with the Schottky contacts forming for the bigger contact diameters and Ohmic contacts forming for the smaller contact

diameters (Chapter 4.5). When the contact-to-nanowire area ratio is larger than 0.6 the nanowire diameter will influence the electrical properties of the structure with the Schottky contacts forming nanowire diameter is approaching contact diameter (Chapter 4.6).

Simulations in Chapter 4.7 predict that due to the complex geometry of the end-bonded ZnO NWs the current crowding will occur around the metal contact at the edge of the contact. For Schottky contacts, the increase in the NW diameter will lead to a parasitic effect of current crowding at reverse bias occurring at the edge of the contact away from the contact interface. Current crowding at forward bias will occur directly at the metal-semiconductor interface. This explains the experimental phenomena observed by others of metal contact melting in side-bonded Ohmic contacts of ZnO nanowires (Ref. [17] in Chapter 4).

The full 3D model was implemented in Chapter 4.8 for the thermal calculation of the free-standing ZnO nanowires with the end bonded contacts. The thermal modelling considers temperature dependent thermal conductivity model and heat capacity model for ZnO because simulations in Cheater 2.4 show that using a constant value of the thermal conductivity and thermal capacity will result in underestimation of the lattice temperature. Current crowding will lead to significant heat generation with a rise of the local temperature up to 1337 K which predicts device failure due to the contact melting. This identifies the need to engineer the contacts to reduce the barrier narrowing near the contact edges or use a method to allow generated heat to flow away from the interface more efficiently.

In Chapter 4.9 the combination of the measurement and simulation results demonstrates that the electrical properties of the ZnO nanowires with a metal contact can be manipulated by the surface charge. The positive charge density at the surface (donor type states) will result in electron accumulation in the nanowire near the surface. This will lead to the reduction in the barrier width at the metal-nanowire interface and increase in the tunnelling current making the contact Ohmic. The negative charge at the NW surface (acceptor type states) will result in the narrower conduction channel making the contact Schottky.

In Chapter 5 results of semiconductor device modelling using Silvaco Atlas are presented including EFM probe interaction with the device under operation.

Electrostatic tip apex interaction with the In_2O_3 thin film transistor (TFT) under operation was studied using a combination of experimental technique and simulation by Silvaco Atlas 2D in Chapter 5.1 for a different doping concentration of In_2O_3 channel layer. A higher doping concentration of In_2O_3 channel layer leads to a linear surface potential profile and a higher surface potential through the channel indicates higher mobility of the device. Experimental potential profiles of the In_2O_3 TFT contain non-linearity at the drain side resulting in flattening of the potential. Simulation demonstrates that this non-linearity is related to the effect of the tip apex and it is more pronounced at the higher drain biases. The effect of the tip apex is depleting electrons from the transistor surface. Resulting measured potential is reduced by the electrostatic interaction with the tip apex creating a flat region on the potential scan near the drain electrode. The simulation demonstrates that this error will be higher for lower doping levels due to the lower dopant screening effect. The simulation also demonstrates that when the gate bias is applied, the deformation of the potential profile at the drain side is smaller.

An applied tip bias of −2 V can further increase an error due to electrostatic interaction with the tip apex at the drain side but the tip bias of 2 V can reduce an error by reducing an electrostatic influence of the tip on the sample.

In Chapter 5.2 a theoretical structure of the ZnO/GZO HFET is suggested using 2D modelling by Silvaco Atlas. A band offset and a presence of the polarization charge at the ZnO/GZO interface results in a formation of the potential well and the creation of a 2DEG at the ZnO/GZO interface. Total polarization charge at the ZnO/GZO were calculated to be -2.219×10^{13} cm^{-2} in the GZO layer and -2.846×10^{13} cm^{-2} in the ZnO layer. That is why the highest electron concentration is at the ZnO/GZO interface where the channel is formed and 2DEG prevents leakage to the gate or ground electrodes. Simulated device has a negative threshold voltage of −0.25 V which means the device would be normally on (a depletion mode transistor). An n-type GZO layer with a doping concentration of 10^{19} cm^{-3} was used in the simulation because at higher doping concentrations of the GZO layer an additional channel appears which makes the device operation impossible.

Chapter 7 List of publications and conference presentations

[1] O. Kryvchenkova, R. J. Cobley, and K. Kalna, "Self-consistent modelling of tunnelling spectroscopy on III–V semiconductors," *Appl. Surf. Sci.*, vol. 295, pp. 173–179, Mar. 2014.

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[3] O. Kryvchenkova, K. Kalna, and R. Cobley, The Current Crowding Effect in ZnO Nanowires with an End-Bonded Metal Contact, in Proceedings of 5th Int. Conf. on Advanced Nanomaterials (ANM 2014) (Aveiro, Portugal, 2-4 July 2014), accepted to *Materials Today: Proceedings* (2014).

[4] Alex M. Lord, Thierry G. Maffeis, Olga Kryvchenkova, Richard J. Cobley, Karol Kalna, Despoina M. Kepaptsoglou, Quentin M. Ramasse, Alex S. Walton, Michael B. Ward, Jürgen Köble, Steve P. Wilks, "Controlling the electrical transport properties of nanocontacts to nanowires" submitted to Nano Letters.

[5] C. J. Barnett, O. Kryvchenkova, L. S. J. Wilson, T. G. G. Maffeis, K. Kalna and R. J. Cobley "The role of probe oxide in local surface conductivity measurements" submitted to the Physical Review B

List of conferences and invited talk:

[1] Invited talk in the National Physical Laboratory, NPL, London, October 2014

[2] Presented on ASDAM 2014, The Tenth International Conference on Advanced Semiconductor Devices and Microsystems, October, 2014, Smolenice, Slovakia (will be published in proceedings)

[3] Presented on the UK Semiconductors 2014, July 2014, Sheffield UK

[4] Presented on ANM 2014, Fifth International Conference on Advanced Nanomaterials, July 2014, Aveiro, Portugal

[5] Presented on the UK Semiconductors 2013, July 2013, Sheffield UK

Publications prepared for submission:

[1] "Electrostatic force microscopy of In2O3 thin film transistor under operation" in collaboration with Cardiff University and Imperial College, London.

[2] "Surface defects in hydrothermally grown ZnO nanowires"

[3] "Electrothermal phenomena in zinc oxide nanowires with metal contacts"

Appendix A. Geometry approximation of Zno/Au structures

Matlab script allows automated creation of the Silvaco Atlas script with geometry approximation of free standing ZnO nanowires with Au particle deposited on top. Nanowire length, radius of Au particle, number of layer used to approximate Au particle shape, radius of the ZnO-Au interface are used as an input parameters.

```
clc
% #Wire depth:
 W_Depth=0.9;
% #Gold radius:
 G_R=0.015/2;
% #Nanowire radius:
 N_R=0.073/2;
 % Number of slices:
 Num=5;
% #Slice length relative to radius 0.2R=20%R:
 S_L=1/Num;
% #Radius of a gate bottom structure:
 B_R=0.2*G_R;
% Undoped surfce layer:
 Surf_L=0.002;
%Number of Bottom layers:
Bottom=6;
 disp('go atlas')
 disp(sprintf('#=====THIS IS A %2.1f NM STRUCTURE, bottom layer %2.0f percent====', G_R*2*1e3,
B_R*100/G_R))
disp('mesh cylindrical three.d')
%% RADIUS MESH
disp ('r.mesh l=0.0 spacing=0.001')
 disp('#gate region:')
 for l=(Num-1):-1:1
   l=sqrt(G_R^2-(l*S_L)^2*G_R^2);
   disp(sprintf('r.mesh l= %6.4f spacing=0.001', l))
end
 %%
disp('#bottom gate layer, x% smaller:')
 for i=Bottom:-1:1
  disp(sprintf('r.mesh l= %6.4f spacing=0.001', G_R-i*B_R/Bottom))
 end

%%
disp('#Undoped ZnO region:')
```

```
disp(sprintf('r.mesh l= %6.4f spacing=0.01', N_R-Surf_L))
 disp('#ZnO region:')
disp(sprintf('r.mesh l= %6.4f spacing=0.0001', N_R))
%%
disp('#=======')
disp('a.m  l=0   spac=45')
disp('a.m  l=360 spac=45')
%% Z COORDINATE MESH
disp('#======')
disp('#ZnO region:')
z1=-W_Depth;
disp(sprintf('z.mesh l=%6.4f spacing=0.0001', z1))
z2a=-W_Depth+0.001;
z2b=W_Depth/10;
disp(sprintf('z.mesh l=%6.4f spacing=%6.4f', z2a, z2b))
disp(sprintf('z.mesh l=-0.01 spacing=0.002'))
disp(sprintf('z.mesh l=-%6.4f spacing=0.0001', Surf_L))
disp(sprintf('z.mesh l=0 spacing=0.001'))
%%
disp('#Gate region 10% smaller:')
for i=1:Bottom
   disp(sprintf('z.mesh l=%6.4f spacing=0.001',i*S_L*G_R/Bottom))
end
 %%
 disp('#Gate region:')
for i=2:Num
   a=i*S_L*G_R;
   disp(sprintf('z.mesh l=%6.4f spacing=0.002',a))
end
%%
disp('#=======')
disp('#Region definition:')
 disp(sprintf('region num=1 material=ZnO  z.min=-%6.4f  z.max=0.0 r.max=%6.4f', W_Depth, N_R))
disp(' # Vacuum/air region around gate 10% smaller:')
 %%
for i=0:Bottom-1
disp(sprintf('region num=%1.0f  material=air  z.min=%6.4f  z.max=%6.4f r.min=%6.4f', i+2,
i*S_L*G_R/Bottom, (i+1)*S_L*G_R/Bottom, G_R-(Bottom-i)*B_R/Bottom))
end
%%
 disp(' # Vacuum/air region around gate:')
for p=2:Num
   zmin=(p-1)*S_L*G_R;
   zmax=p*S_L*G_R;
   rmin=sqrt(G_R^2-((p-1)*S_L)^2*G_R^2);
   disp(sprintf('region num=%g  material=air  z.min=%6.4f  z.max=%6.4f r.min=%6.4f',i+p+1, zmin, zmax,
rmin))
end
 %%
disp(' # Gate region 10% smaller:')
 for i=0:Bottom-1
disp(sprintf('electrode name=gate material=gold  z.min=%6.4f  z.max=%6.4f r.max=%6.4f',
i*S_L*G_R/Bottom, (i+1)*S_L*G_R/Bottom, G_R-(Bottom-i)*B_R/Bottom))
end
```

```
%%
disp(' # Gate region:')
for m=2:Num
   zmin=(m-1)*S_L*G_R;
   zmax=m*S_L*G_R;
   rmax=sqrt(G_R^2-((m-1)*S_L)^2*G_R^2);
   disp(sprintf('electrode name=gate material=gold z.min=%6.4f  z.max =%6.4f r.max=%6.4f', zmin, zmax,
rmax))
end
z.max=-W_Depth+0.0003;
disp(sprintf('electrode name=ground material=gold z.min=-%6.4f z.max=%6.4f r.max=%6.4f',W_Depth, z.max
,N_R))
 %%
disp(sprintf('DOPING uniform N.TYPE CONC=1.0e18 R.MAX=%6.4f z.min=-%6.4f z.max= %6.4f',N_R-
Surf_L, W_Depth, -Surf_L ))
disp(sprintf('DOPING uniform N.TYPE CONC=1.0e18 R.MAX=%6.4f z.min=%6.4f z.max=%6.4f', G_R-B_R, -
Surf_L, 0))
 disp(sprintf('method newton bicgst')
```

Appendix B. Geometry approximation of In_2O_3 TFT in presence of scanning probe

Matlab script allows automatically creates Silvaco Atlas script with In_2O_3 TFT structure and scanning probe approximation. To reconstruct the surface potential profile a multiple tip positions needed. Script uses tip position coordinates, tip radius, tip-sample separation, number of points for circular tip approximation and applied electrode biases as an input parameters.

```
clc
points=6;
alpha=180/points;
Radius=0.08;
Separat=0.075;
Y_cent=-(Radius+Separat);
Vg=1;
Tip_Move=[110; 100; 99.9; 99.5; 99; 98; 97; 96; 95; 93; 91; 89; 87; 84; 81; 78; 75; 72; 70; 65];
p=length(Tip_Move);
%=========================
%% Creating the Atlas code
for tm=1:p
  X_cent=Tip_Move(tm);
  for i = 1:points+1
    XY(i,:)=[(X_cent-(Radius*cosd(alpha*(i-1)))), (Y_cent+(Radius*sind(alpha*(i-1))))];
      X(i)=[(X_cent-(Radius*cosd(alpha*(i-1))))];
    Y(i)=[(Y_cent+(Radius*sind(alpha*(i-1))))];
  end
%X=X'
%Y=Y'
%XY
   display(sprintf('go DevEdit \n work.area x1=0 y1=0 x2=0 y2=0 \n region reg=1 mat=Air
color=0xfefefe pattern=0x10 \\'))
  % Writing a string with coordinates for the Air region
  display(sprintf(' \t polygon="170,%6.4f 170,0 0,0 0,%6.4f ',Y_cent, Y_cent))
    for i=1:points+1
      display( sprintf('\b %6.4f, %6.4f',X(i), Y(i)))
    end
  display(sprintf('\b"'))

  display(sprintf(' constr.mesh region=1 default \n \n region reg=2 name=emitter mat=Silicon
elec.id=4 work.func=0 color=0xfecb00 pattern=0x4 \\'))
  %  Writing a string with coordinates of Tip
  display(sprintf(' \t polygon='"'))
```

```
      for i=1:points+1
         display( sprintf('\b %6.4f, %6.4f',X(i), Y(i)))
      end
   display(sprintf('\b"'))
  type('transistor.in')
   %Different gate biases:
      for k=Vg
      display(sprintf(' method gummel  newton itlim=20 trap  maxtrap=6 vsatmod.inc=0.01
carriers=1 elect \n output con.band val.band '))
      display(sprintf(' solve vgate=%6.2f \n log outf=%g_vg=%6.2f.log', k, X_cent, k))
      display(sprintf('probe name=tip-P x=%d y=0 POTENTIAL',X_cent))
      type(',IdVd.in')
      display(sprintf('log off \n'))
      end
end
 %==================================
%% Process the result: Select Vg?
Vg=1;
for y=1:length(Tip_Move)
   X_cent=Tip_Move(y);
   LogFileID=sprintf('%g_vg=%g.log',X_cent,Vg); %introducing result file names to matlab
   A = importdata(LogFileID,' ',21);
   a=length(A.data);
      for k = 1:a
        Mat(k,:)=[A.data(k, 4), A.data(k, 7), A.data(k, 13), X_cent];
      end
   OutFileID=sprintf('%g_vg=%g_processed.csv',X_cent,Vg); %In this file values are: Vd Vg
Potential X(um)
   save(OutFileID,'Mat','-ascii')
   %type(OutFileID)
end
 %unites all data in one file for processing with excel later:
 FinalMat=[]   %introduce initial empty matrix to which all results will be added one by one
for j=1:length(Tip_Move)
     X_cent=Tip_Move(j);
   LogFileID2=sprintf('%g_vg=%g_processed.csv',X_cent,Vg)
   B = dlmread(LogFileID2);
   FinalMat=[FinalMat;B];
end
FinalMatSort=sortrows(FinalMat, 1)
save('FinalResult.txt','FinalMatSort','-ascii')
%ploting results: select Vd? 37 is number of gate biases used
hold off
for p=1:37
   PlotPotFinal=[];
   PlotPot=[];
   Vd=FinalMat(p,1)
   for t=1:length(FinalMatSort)
        if FinalMatSort(t, 1)==Vd
          PlotPot(t,:)=FinalMatSort(t, :);
```

```
        end
    end
    PlotPot
    PlotPotFinal=sortrows(PlotPot, 4)
  plot(PlotPotFinal(:,4), PlotPotFinal(:,3), '-',[65,70],[1.37, 1.37], 'r-*', [100,105],[9.37527,
9.37527], 'r-*')
xlabel('Distance (um)')
ylabel('Potential')
xlim([65 105])
ylim([1.37 10])
    hold on
end
%%
```

Content of 'transistor.in'

```
constr.mesh region=2 default
region reg=3 mat=ZnO color=0xcb9326 pattern=0x2 \
        polygon="0,0 70,0 100,0 170,0 170,0.05 0,0.05"
impurity id=1 region.id=3 imp=Donors \
        peak.value=3.5e+17 ref.value=1000000000000 comb.func=Multiply
constr.mesh region=3 default
region reg=4 mat=SiO2 color=0xfe pattern=0x2 \
        polygon="0,0.05 170,0.05 170,0.15 0,0.15"
constr.mesh region=4 default
region reg=5 mat=Silicon color=0xfecb00 pattern=0x4 \
        polygon="0,0.15 170,0.15 170,0.45 0,0.45"
impurity id=1 region.id=5 imp=Donors \
        peak.value=1e+18 ref.value=1000000000000 comb.func=Multiply
constr.mesh region=5 default
region reg=6 name=source mat=Aluminum elec.id=1 work.func=0 color=0xfec7c7 pattern=0x7 \
        line="70,0 0,0"
constr.mesh region=6 default
region reg=7 name=drain mat=Aluminum elec.id=2 work.func=0 color=0xfec7c7 pattern=0x7 \
        line="170,0 100,0"
constr.mesh region=7 default
region reg=8 name=gate mat=Aluminum elec.id=3 work.func=0 color=0xfec7c7 pattern=0x7 \
        line="170,0.45 0,0.45"
constr.mesh region=8 default
# Set Meshing Parameters
base.mesh height=0.02 width=7
bound.cond !apply max.slope=100 max.ratio=300 rnd.unit=0.0001 line.straightening=1 align.points
when=automatic
imp.refine min.spacing=0.02
constr.mesh max.angle=90 max.ratio=300 max.height=1000 \
        max.width=1000 min.height=0.0001 min.width=0.0001
constr.mesh type=Semiconductor default
constr.mesh type=Insulator default
constr.mesh type=Metal default
constr.mesh type=Other default
```

```
constr.mesh region=1 default
constr.mesh region=2 default
constr.mesh region=3 default
constr.mesh region=4 default
constr.mesh region=5 default
constr.mesh region=6 default
constr.mesh region=7 default
constr.mesh region=8 default
constr.mesh id=1 x1=69 y1=0 x2=101 y2=0.05 default max.height=0.002 max.width=1
constr.mesh id=2 x1=69 y1=-0.03 x2=101 y2=0 default max.height=0.002 max.width=1
Mesh Mode=MeshBuild
base.mesh height=0.02 width=7
bound.cond !apply max.slope=100 max.ratio=300 rnd.unit=0.0001 line.straightening=1 align.Points
when=automatic
#==================
go atlas
material material=ZnO permittivity=8.9 semiconduc eg300=3.6 affinity=3.3
contact name=emitter workfun=4.6
#contact name=source workfun=4
#contact name=drain workfun=4
model print
save outf=structure.str
model   fldmob srh
#
# SECTION 4: Id-Vd calculation
```

Content of 'IdVd.in'

```
solve vdrain=0.05
solve vdrain=0.10
solve vdrain=0.125
solve vdrain=0.15
solve vdrain=0.20
solve vdrain=0.30
#
method  newton trap itlim=35  maxtrap=6   carriers=1 elect
solve vdrain=0.50  vstep=0.25  name=drain vfinal=8
```

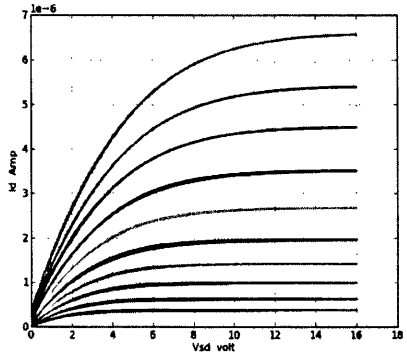
Appendix C. Results of In_2O_3 TFT measurements

Summary of electrical characteristics for In_2O_3 transistors

W/L	μ_{sat} $Cm^2/V.S$	V_{th} Volt	V_{on} Volt	I_{on}/I_{off}
200μm/40μm Double spin	0.845±0.11	-0.20V	-4.45V	10^5
1000μm/30 μm Double spin	1.143±0.13	-6.65V	-8.2V	10^4
1000μm/20 μm Double spin	1.25±0.081	-15.8V	> -19V	10^6
1000 μm/30μm Single spin	0.24±0.069	-0.5V	-1.85V	10^5
1000 μm /20 μm Single spin	0.215±0.07	-4.5V	-5.9V	10^5
1500 μm /40 μm Single spin	0.153±0.09	9.3V	8.6V	10^4

C-1 Sample 1: In_2O_3 double-spin TFT

Device has a width of W = 200 μm and a channel length of L = 40 μm.
Output and transfer characteristics:



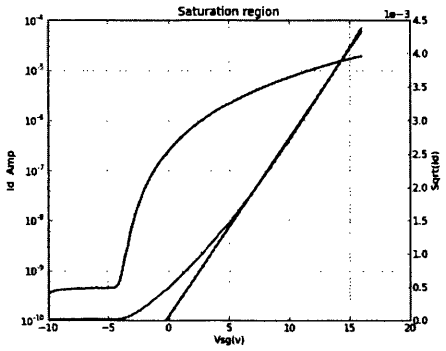


Figure 5.4.1: (a) Output characteristic at Vg=1, 2, ...10V with step 1V. (b) Transfer characteristics in saturation regime Vd=10V and sweeping gate bias between 0 and 16V. V_t= -0.20V, V_{on}= -4.45V, μ_{sat}= 0.845±0.11 Cm^2/Vs, I_{on}/I_{off} =10^5

Potential profiles as a function of source-drain voltage (source & gate grounded):

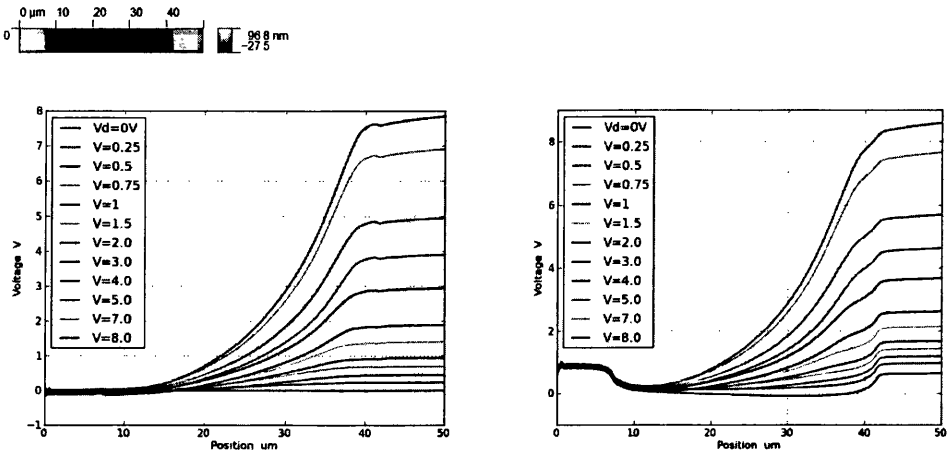


Figure 5.4.2: (a) EFM profile with grounded source and gate, varying V_{ds} between 0 and 8V. The lower measured potential in the channel between electrodes is the contact potential difference between In_2O_3 and Al. (b) The same profile after subtraction of the V_{ds} = 0 profile to correct for the CPD. There is a slight discontinuity at the electrode. (c) The AFM image of the electrodes and channel.

Potential profiles as a function of source-drain voltage at fixed gate voltage (+5V).

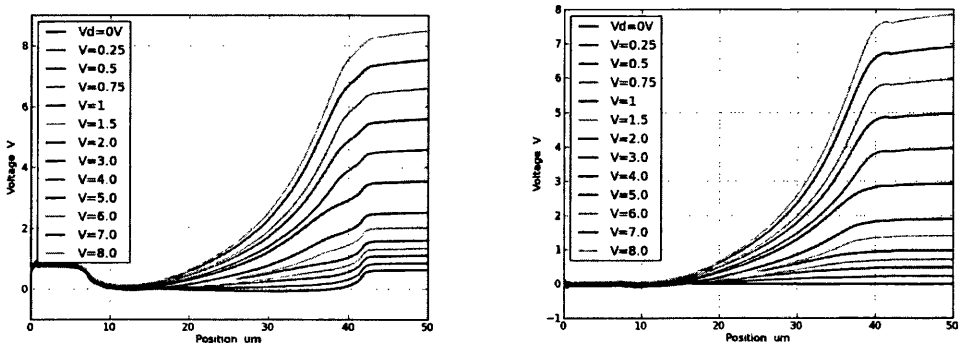


Figure 5.4.3: As for figure 2 with a fixed gate bias of V_g = +5 V. For low bias the potential is approximately linear. For V_{ds} in the range 2-5 V, approaching saturation, the potential profile shows curvature consistent with the carrier concentration decreasing gradually along the channel. For V_{ds} ≥ 6V, the profile close to the drain electrode is linear, consistent with a depletion region.

Potential profiles as a function of gate bias at fixed drain voltage (V_{ds} = +8V)

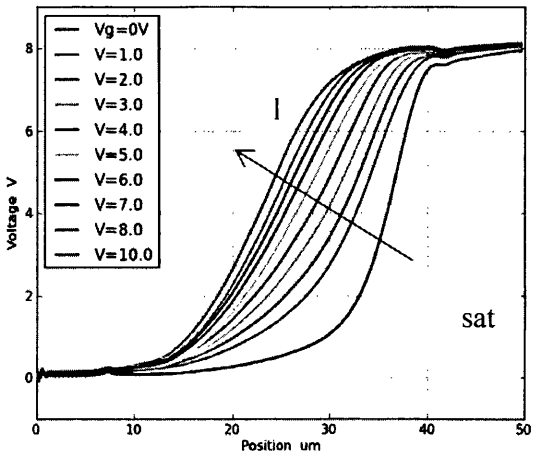


Figure 5.4.4: Effect of gate voltage for fixed V_d=8V. In the saturated regime, most of the potential is dropped across the depleted region as expected. In the linear regime, the profile is roughly symmetric as expected for a relatively uniform conducting channel. In the intermediate region, there is curvature as the channel becomes more resistive on approaching the drain electrode.

For this first sample, the behaviour is well-behaved and agrees broadly with what we would expect. However, it is the only sample out of seven samples we tested that behaves exactly this way. There is one other sample that shows some resemblance. Sample 2 is broadly typical of the remaining samples.

C-2 Sample 2: In_2O_3 single-spin

Device has the following geometry: W = 1000 μm; L = 30 μm.

This sample is typical of several. We have selected it for direct comparison with sample 1 since the threshold values are similar, easing comparison.

Output and transfer characteristics:

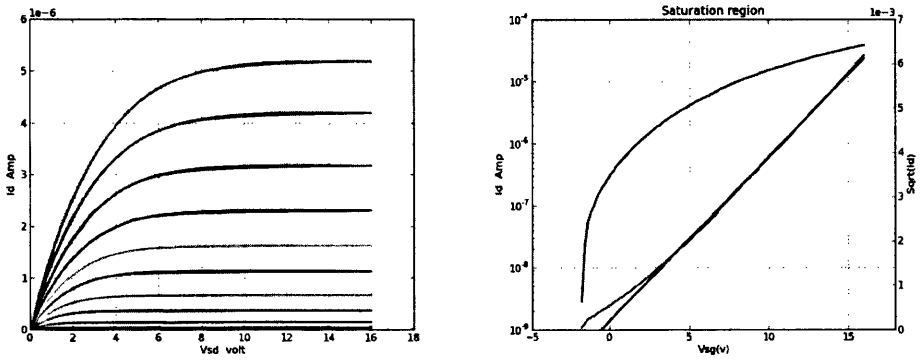


Figure 5.4.5: (a) Output characteristic at Vg=1, 2, ...10V with step 1V. (b) Transfer characteristics in saturation regime Vd=10V and sweeping gate bias between 0 and 16V.

Potential profiles as a function of source-drain voltage (source & gate grounded):

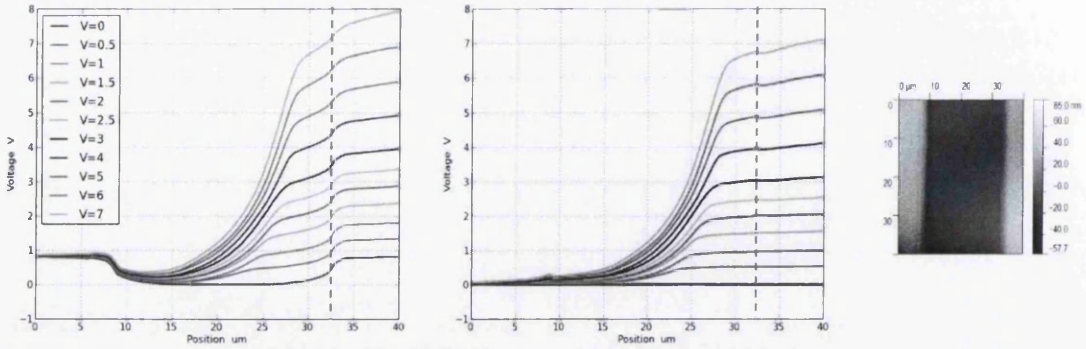


Figure 5.4.6: (a) EFM profile with grounded source and gate, varying V_{ds} between 0 and 8V. (b) The same profile after subtraction of the V_{ds} = 0 profile to correct for the CPD. (Corresponds directly to Figure 2). Dashed lines indicate drain electrode position.

Potential profiles as a function of source-drain voltage at fixed gate voltage (+5V).

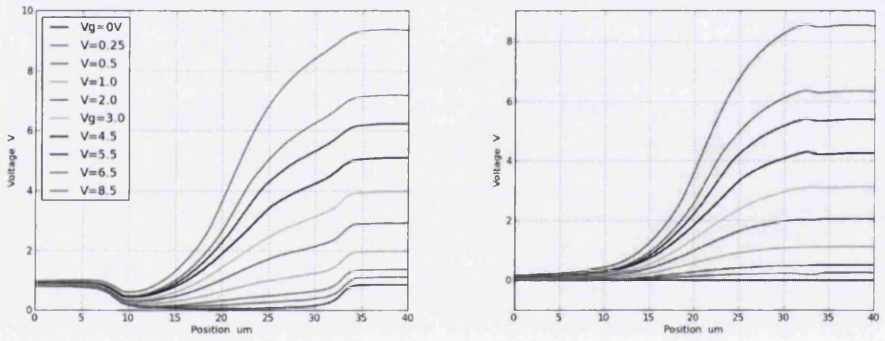


Figure 5.4.7: As for figure 5 with a fixed gate bias of V_g = +5 V (corresponds directly to Figure 3). For low bias the potential is approximately linear.

In both Figure 5.4.6 and Figure 5.4.7, a less steep gradient of the potential (i.e. apparently lower electric field) in the depletion region close to the drain electrode is observed. This appears to be inconsistent with the highly resistive nature of this region.

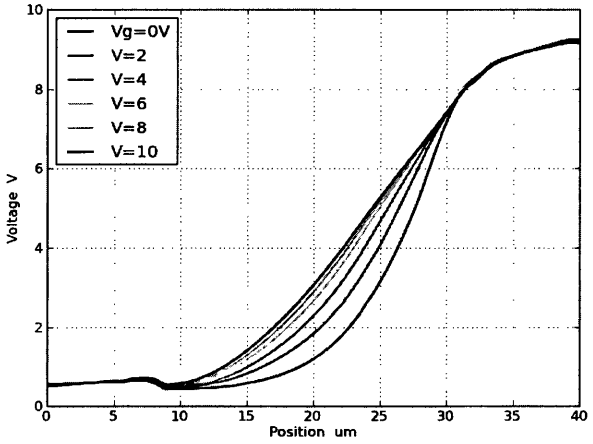


Figure 5.4.8: Effect of gate voltage for fixed V_d=9V.

C-3 Sample 3: In_2O_3 double-spin

Device has the following geometry: W = 1000 μm; L = 30 μm.

This sample has identical dimensions to Sample 2, except that it has been spin-coated twice. It is included as comparison of the effect of the second spin-coating.

Output and transfer characteristics:

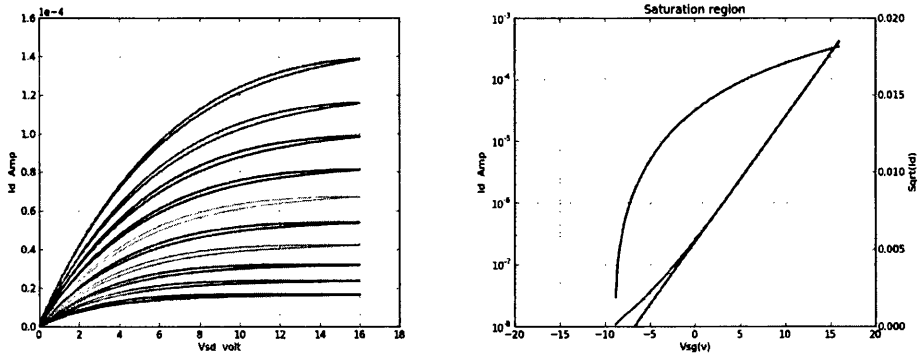


Figure 5.4.9: (a) Output characteristic at Vg=1, 2, ...10V with step 1V. (b) Transfer characteristics in saturation regime Vd=10V and sweeping gate bias between 0 and 16V.

The threshold voltage has shifted to a more negative bias with the second spin-coating.

Potential profiles as a function of source-drain voltage (source & gate grounded):

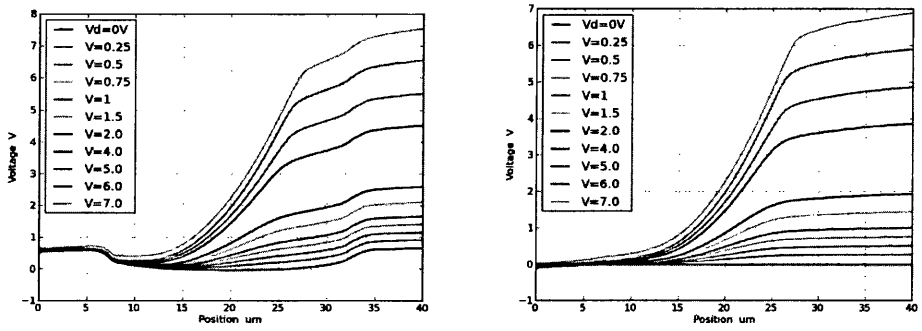


Figure 5.4.10: we observe this flat profile close to the electrode in the saturated regime.

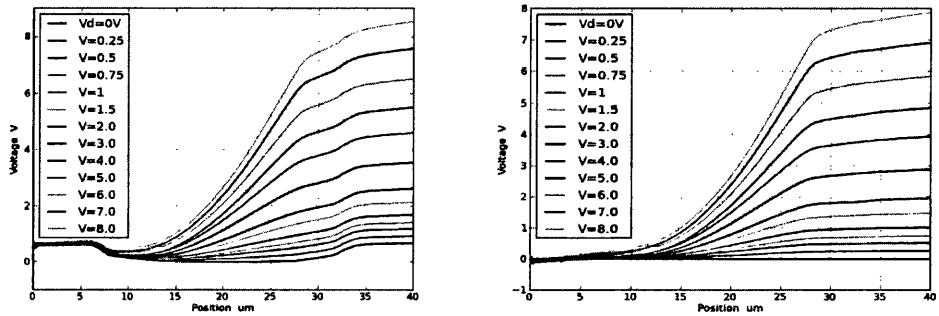


Figure 5.4.11: Potential profiles as a function of gate bias at fixed drain voltage (V_{ds} = +5V)

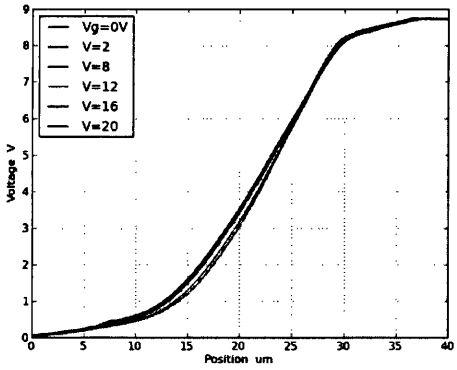


Figure 5.4.12: Potential profiles as a function of gate bias at fixed drain voltage (V_{ds} = +8V). There is very weak dependence on the gate bias, with no change in the region close to the drain electrode.

C-4 Sample 4: In_2O_3 single-spin

Device geometry: W = 1500 μm; L = 40 μm

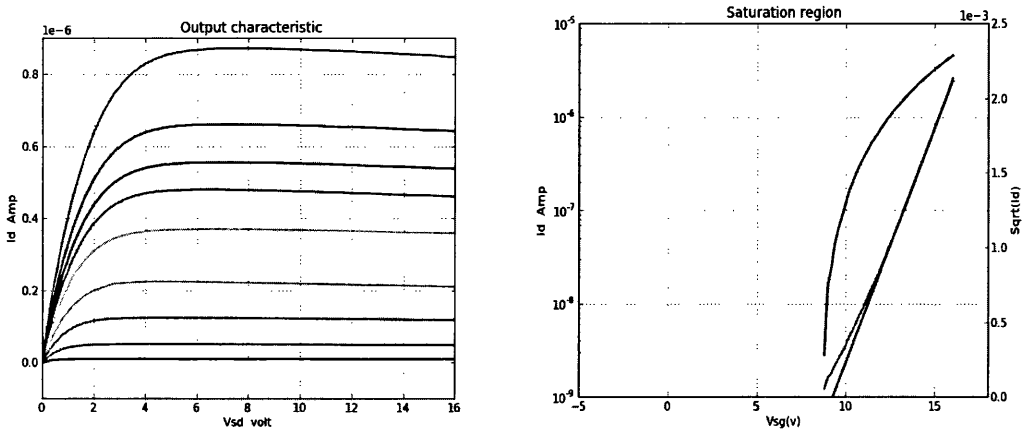


Figure 5.4.13: The output and transfer characteristic of Indium oxide transistor with dimension W/L= 1500μm/40μm. The output characteristic shows curves at Vg= 1, 2, 3,5,6,7,8,9,10V. The transfer characteristic is at saturation regime with Vd=10V. The output curves show some reduction of drain currents at high Vg and Vd. Saturation mobility μ_{sat}= 0.153±0.081 $Cm^2/V.s$, Vo=8.6V, Vt= 9.3V and $I_{on} / I_{off} = 10^4$ Note large threshold voltage

Potential profiles as a function of source-drain voltage (source & gate grounded):

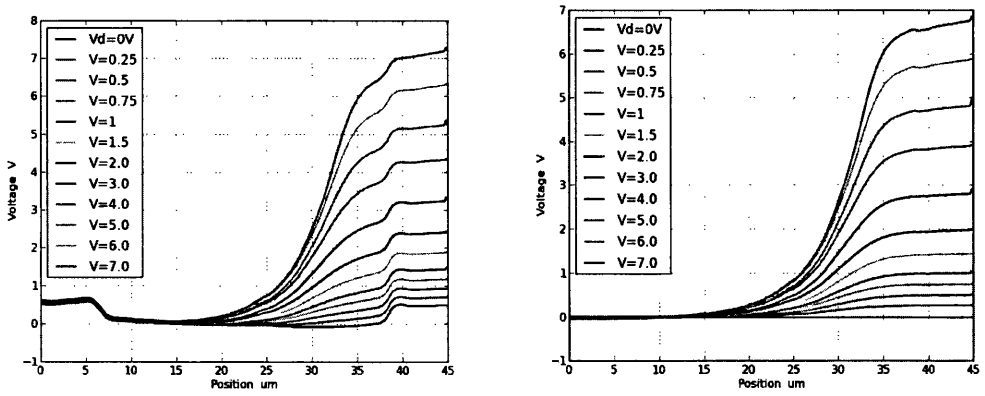


Figure 5.4.14: The potential profiles of transistor as a function of drain voltage after grounding both source and gate. The figure on right shows profiles after subtraction of Vd=0 V from all other profiles.

Potential profiles as a function of gate bias at fixed drain voltage

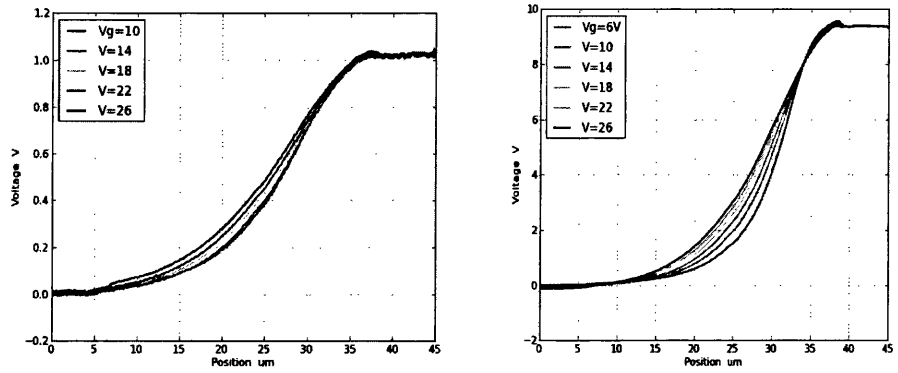


Figure 5.4.15: First graph indicates profiles of Vd=Vg=0 V in addition to profiles for Vd=9.5 V and Vg= 6 to 26 V with step 4 V. The second one presents profiles after subtraction of Vg=Vd=0 V.