Qucs Equation-Defined and Verilog-A RF device models for Harmonic Balance circuit simulation

Mike Brinson
Centre for Communications Technology
London Metropolitan University
UK
Email: mbrin72043@yahoo.co.uk

Vadim Kuznetsov
Bauman Moscow Technical University
Russia
Email: ra3xdh@gmail.com

Abstract—This paper is concerned with the development and evaluation of a number of modelling techniques which improve Qucs Harmonic Balance simulation performance of RF compact device models. Although Qucs supports conventional SPICE semiconductor device models, whose static current/voltage and dynamic charge characteristics exhibit second and higher order derivatives may not be continuous, there is no guarantee that these will function without Harmonic Balance simulation convergence problems. The same comment also applies to a number of legacy compact semiconductor device models. The modelling of semiconductor devices centered on non-linear Equation-Defined Devices and blocks of Verilog-A code, combined with linear components, is introduced. These form a class of compact macromodel that has improved Harmonic Balance simulation performance. To illustrate the presented modelling techniques RF diode and bipolar junction transistor macromodels are described and their Harmonic Balance performance simulated with Qucs and Xyce©.

Index Terms—Qucs, Xyce, Harmonic Balance RF simulation, compact semiconductor device modelling, equation-defined devices, macromodels.

I. Introduction

Since the adoption by the Qucs circuit simulation community of Equation-Defined Devices (EDD) [1] and Verilog-A analogue modules for compact device modelling [2] they have become amongst the most widely used forms of non-linear device model for established and emerging technologies [3]. The release of the open source General Public License (GPL) "Automatic Device Model Synthesizer" (ADMS) [4], has ensured that Verilog-A will remain one of the dominant compact modelling languages for the foreseeable future. Although ADMS only handles a sub-set of Verilog-A it includes a number of language statements which simplify compact semiconductor device model design [5]. Verilog-A modules and EDD models are now established as important Qucs modelling features. Qucs treats EDD models and Verilog-A modules as non-linear entities, including those with interface ports linked to internal model nodes via resistors implemented with EDD two terminal branches or Verilog-A code. This structure implies that only non-linear components are connected to internal model nodes. In general, such models function well in the DC, AC and Transient simulation domains without problems. However, the reverse is true with Harmonic Balance (HB) simulation, mainly due to problems occurring when circuits are partitioned into a frequency domain linear subcircuit and a time domain non-linear subcircuit or because of large changes in device bias points between circuit equation iterative solution steps [6]. Circuit nodes with only non-linear components connected can make partitioning difficult, often resulting in HB simulation non-convergence [6]. A revaluation of the role of EDD and Verilog-A modules suggests that reserving either for the non-linear sections of an HB model reduces partition failure, provided the remaining model components are linear and at least one linear component is connected to each macromodel node. Moreover, this structure naturally builds into a compact macromodel. Non-linear EDD and Verilog-A modules with current or charge characteristics that have discontinuous differential terms can also be a source of HB simulation non-convergence. This paper introduces EDD and Verilog-A macromodelling techniques which attempt to eliminate the problems found with Qucs HB circuit partitioning and device model discontinuities. Semiconductor diode and BJT Qucs HB models are described and their performance simulated with Qucs and Xyce©[7].

II. Modelling a diode non-linear static current-voltage characteristic

A basic compact device model for a semiconductor diode is shown in Fig. 1. To prevent HB floating point numerical overflow in the diode forward bias region of operation the Verilog-A function $limexp$ is often used to calculate diode current, rather than the standard exponential function exp. When computed diode voltages have a value such that $\delta \cdot Vd > 80$ function $limexp$ linearizes the diode current characteristic equation in an attempt to prevent numerical overflow. At the crossover point between the diode exponential and linear regions of operation the Id and dId/dVd curves are continuous. Qucs C++ code represents real numbers using IEEE binary 64 bit real numbers. These have a decimal range of roughly $\pm 2.23 \cdot 10^{-308}$ to $\pm 1.80 \cdot 10^{308}$. Writing the diode equation given in Fig. 1 in terms of a critical voltage $Vcrit$, which represents the value of Vd where Id changes from the exponential to the linear region of operation, yields equations 1 and 2 respectively.

$$Id = Is \cdot (exp(\delta \cdot Vd) - 1), \quad \forall (Vd <= Vcrit) \quad (1)$$

$$Id = Is \cdot exp(\delta \cdot Vcrit) \cdot [1 + \delta \cdot (Vd - Vcrit)], \forall (Vd > Vcrit) \tag{2}$$

where where $exp(\delta \cdot Vcrit) >> 1.0$ and $Vcrit = 308/\delta$ volts. For $N = 1$ and $T = 300$ Kelvin, $Vcrit(max) \approx 7.7$ volts. Hence with $N = 1$, adopting a value of $Vcrit$ near to, but below 7.7 volts, will ensure that values of Vd below $Vcrit$ do not cause floating point overflow when calculation Id [6]. In the exponential region of operation the first and higher order current derivatives are continuous which is ideal for HB simulation. However, in the linear region of operation ($Vd > Vcrit$) only the first order derivative is continuous. Figures 2 and 3 introduce a non-linear EDD model and a Verilog-A module which, when either are combined with linear resistors Rs and Rp, form a compact diode macromodel. Typical simulated DC data for a diode macromodel under test are given in Fig. 4. The test circuit has $Vcrit = 0.6$ volts. This value is set artificially low in order to demonstrate the change from the exponential to the linear region of operation in the diode Id characteristic. In Fig. 4 the plot of $\frac{d^2 Id}{dVd^2}$ against Vd clearly illustrates a discontinuity at $Vd = 0.6$ volts. A
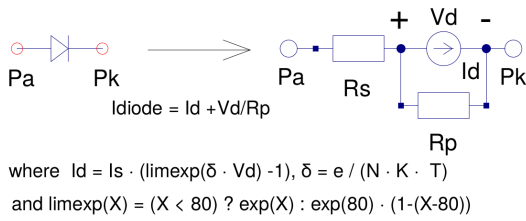

Fig. 1. A semiconductor diode static I/V model: N is the diode emission coefficient, e is the electron charge, K is the Boltzmann constant, T is the diode temperature in Kelvin, Rs is the series bulk and contact resistance and Rp a diode junction parallel leakage resistance.
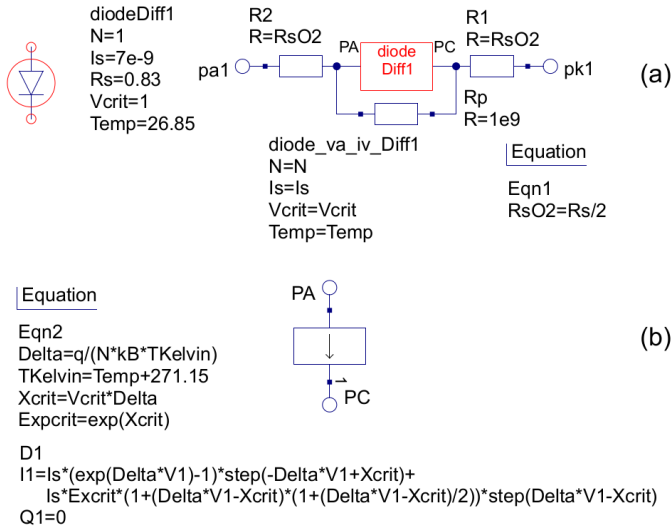

Fig. 2. A diode compact macromodel: (a) Qucs schematic symbol and macromodel circuit, (b) Qucs EDD diode current $I1$ selected with function $step()$. For clarity $I1$ is displayed on more than one line.

more general equation for the diode model current Id, when

$Vd > Vcrit$, is given by equation 3.

$$Id = Is \cdot exp(\delta \cdot Vcrit) \cdot \sum_{i=0}^{p} \frac{\delta^i}{i!} (Vd - Vcrit)^i \quad \forall (Vd > Vcrit) \tag{3}$$

where $0 \leq p \leq 5$. Illustrated in Fig. 5 are a typical set of DC simulation data obtained from the test circuit shown in Fig.4 and a diode model based on the extended macromodel defined by equation 3. In this example both $Diff1$ and $Diff2$ are continuous, making the model more suitable for HB simulation.

III. MODELLING DIODE NON-LINEAR DYNAMIC CHARGE CHARACTERISTICS

Semiconductor diode diffusion and depletion capacitance are given by equations 4, 5 and 6 [11].

$$Cdiff = \frac{dQdiff}{dVd} = Tt \cdot \frac{dId}{dVd} \tag{4}$$

where Tt is the diode transit time in seconds.

$$Cdep = \frac{dQdep}{dVd} = Cj0 \cdot \left[1 - \frac{Vd}{Vj}\right]^{-M} \forall \left(Vd < \frac{Vj}{2}\right) \tag{5}$$

$$Cdep = 2^M \cdot Cj0 \cdot [2 \cdot M \cdot \frac{Vd}{Vj} + (1 - M)] \quad \forall \left(Vd >= \frac{Vj}{2}\right) \tag{6}$$

where $Cj0$ is the zero bias junction capacitance in Farads, M is a pn junction grading coefficient, Vj is the junction potential voltage in Volts, and $Qdiff$ and $Qdep$ are stored diffusion and depletion charges in Coulombs respectively. To reduce the effect of the discontinuity in equation 5 at $Vd = Vj$ the depletion capacitance can be represented by equations 5 and 7.

$$Cdep = 2^M \cdot Cj0 \cdot \sum_{i=0}^{p} \frac{(Vd - Vmax)^i}{i!}, \forall \left(Vd >= \frac{Vj}{2}\right) \tag{7}$$

```
// Diode I/V HB model diode_va_iv_Diff1.va
`include "disciplines.vams"
`include "constants.vams"
module diode_va_iv_Diff1(pa,pk);
inout pa, pk;  electrical pa, pk;
parameter integer N = 1 from [1 : inf);
parameter real Is = 1e-14 from [1e-20 : inf);
parameter real Vcrit = 0.6 from (0.4 : 5);
parameter real Temp = 26.85 from [-100 : 200];
parameter real Tnom = 26.85 from [-100 : 200);
real TKelvin, Delta, Xcrit, Expcrit, X;
analog begin
 @(initial_model)
 begin
  TKelvin = Temp+271.15; Delta = `P_Q/(N*`P_K*TKelvin);
  Xcrit = Vcrit*Delta; Expcrit = exp(Xcrit);
 end
 X = Delta*V(pa, pk);
 I(pa,pk) <+ (X <= Xcrit) ? Is*(exp(X)-1) : Is*Expcrit*(1+(X-Xcrit) );
end
endmodule
```

Fig. 3. Qucs diode Verilog-A code: diode current $I(pa, pk)$ selected with ternary operator $x?y : z$.
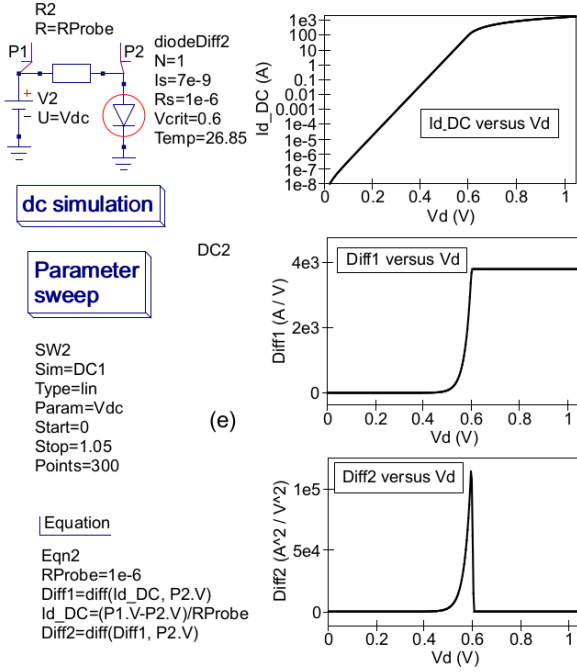
Fig. 4. Qucs compact diode macromodel test circuit and simulated DC current characteristics: $Id\_DC = Id$, $Diff1 = \frac{dId}{dVd}$, and $Diff2 = \frac{d^2Id}{dVd^2}$.
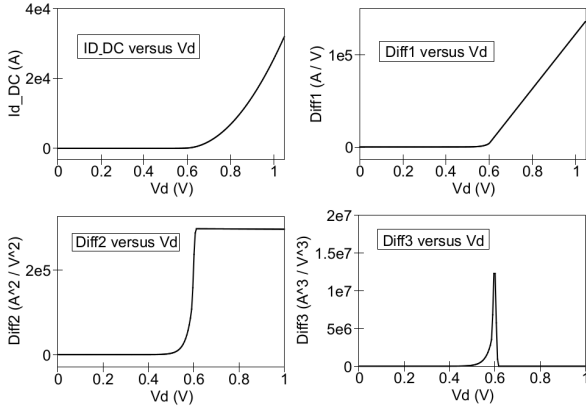

Fig. 5. Extended diode compact macromodel simulated DC current characteristics for $p = 2$, $Vcrit = 0.6\ V$, $Is = 7e-9\ A$, $Rs = 1e-6\ \Omega$ and $T = 300\ Kelvin$: $Id\_DC = Id$, $Diff1 = \frac{dId}{dVd}$, $Diff2 = \frac{d^2Id}{dVd^2}$ and $Diff3 = \frac{d^3Id}{dVd^3}$.

where $0 < p \le 5$. Although equation 7 gives an approximate value for $Cdep$ at $Vd > Vj/2$ it is normally acceptable because $Cdiff$ is the dominant capacitive component in this region of diode operation. Setting $p = 2$ and integrating equations 4, 5 and 7 gives

$$Qdiff = Tt \cdot Id \quad (8)$$

$$Qdep = Cj0 \cdot \left(\frac{Vj}{(1-M)}\right) \cdot \left[1 - \left(1 - \frac{Vd}{Vj}\right)^{1-M}\right],$$

$$\forall \left(Vd < \frac{Vj}{2}\right) (9)$$

$$Qdep = 2^M \cdot Cj0 \left[Vdiff + \frac{Vdiff^2}{2} + \frac{Vdiff^3}{6}\right],$$

$$\forall \left(Vd >= \frac{Vj}{2}\right) \quad (10)$$

where $Vdiff = Vd - Vmax$ and $Vmax = Vj/2$. A modified EDD macromodel which includes $Qdiff$ and $Qdep$ is shown in Fig. 6. The Verilog-A code for this model is similar to the module code listed in Fig. 3 with $I(Pa, Pk) <+ ddt(Q1)$ added, where $Q1 = Qdiff + Qdep$. Shown in Fig. 7 is a test circuit for extracting semiconductor diode capacitance from S parameter simulated data. In this circuit the diode under test has series resistance Rs set at $0.1\mu\Omega$ to ensure that Rs does not affect the accuracy of the extracted values of Cd. The diode under test has DC bias voltage Vdc swept over the range 0 to 0.8 volts and, at each bias point, $S[1,1]$ determined with Qucs S parameter simulation. Conversion of $S[1,1]$ to $y[1,1]$ allows diode capacitance values to be extracted from the imaginary component of the $y[1,1]$ data; $Cd = imag(y[1,1]/(2 \cdot \pi \cdot frequency)$. Diode parameter Vj is set at 0.6 volts to be able to observe any discontinuities in the diode capacitance characteristics. Fig. 7 presents plots of Cd, and its first two derivatives, with respect to diode bias voltage Vd. These suggest that the change in depletion capacitance given by equations 5 and 7 is smooth and does not introduce any significant discontinuities in the diode capacitance characteristic.

IV. HARMONIC BALANCE AND TRANSIENT SIMULATION OF AN RF DIODE DETECTOR

The diagram in Fig. 8 shows an unbiased RF diode detector circuit and a set of Qucs HB simulation output voltage and diode current spectral plots for a 915 MHz five volt peak AC input signal. The detector diode model parameters are similar to the AVAGO HSMS-2820 published SPICE parameters [8].
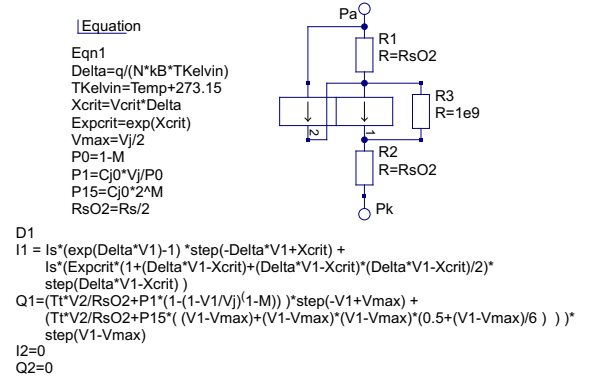

Fig. 6. A semiconductor diode EDD macromodel including dynamic charge characteristics. For clarity EDD $D1$ current $I1$ and charge $Q1$ are displayed on more than one line.
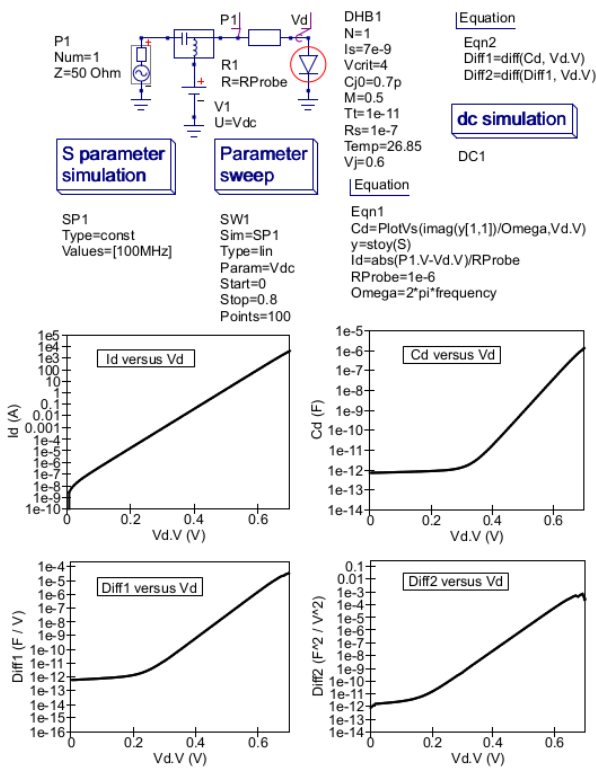
Fig. 7. Diode compact macromodel S parameter simulation: test circuit and *Equation* scripts for extracting diode capacitance from Qucs S parameter simulated values.

This particular circuit illustrates the performance of the diode HB compact macromodel and how effective HB simulation is in determining the AC steady state response of RF circuits, particularly when compared to number of AC input signal cycles needed before the transient simulation output voltage $Nout.Vt$ approaches a steady state response, see Fig.9.

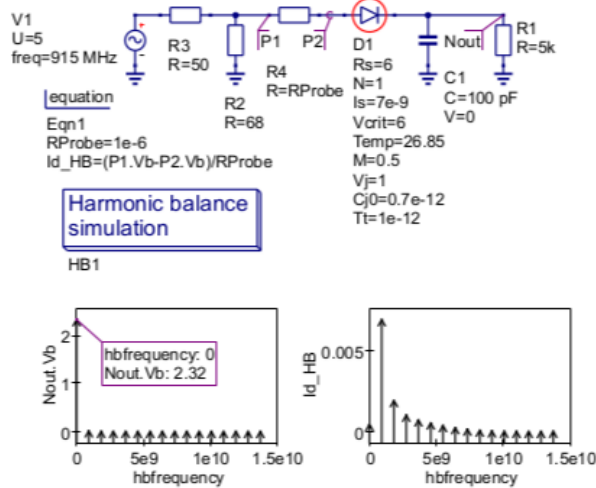**Fig. 8.** RF diode detector test set and HB simulation data plots: $Is = 7e-9A$, $N = 1$, $Vj = 1.0V$, $Rs = 6\Omega$, $Cj0 = 0.7pF$ and $Tt = 1e-12s$.
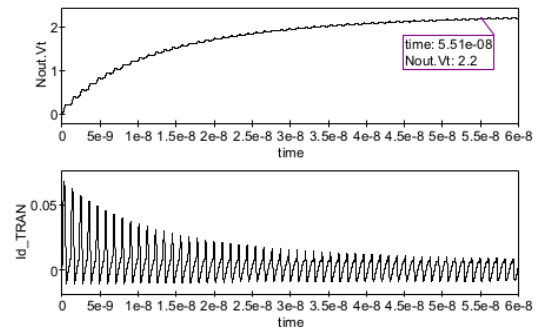
Fig. 9. RF diode detector transient simulation data plots: $Nout.Vt$ and Id_TRAN against time.

V. A BJT COMPACT MACROMODEL FOR HB SIMULATION

A Qucs compact macromodel for an npn BJT modelled by a large signal Ebers-Moll I/V characteristic and non-linear stored charge is given in Fig. 10. This macromodel is constructed from a nonlinear block called *npnBlock* and three linear resistors connecting port terminals $PC1$, $PB1$ and $PE1$ to *npnBlock*. Figures 11 and 12 present details of the npn BJT nonlinear static current and dynamic charge properties derived from the semiconductor diode model introduced previously. Figure 13 introduces a basic BJT test bench and a set of Qucs HB and transient simulation derived frequency domain spectral plots for the voltage at output node Pc. The latter being obtained with FFT techniques, see Qucs equation $Eqn5$ Fig. 13. DC voltage sources $V3$ and $VinDC$ were set at 15V and 0.65V to bias the BJT output node Pc at a quiescent DC voltage of approximately 10V at a collector current of 2mA. Comparison of the HB and transient voltage spectral data for node Pc, with $VinAC$ a single tone AC test signal of 1MHz frequency and 20mV peak amplitude, indicates good agreement between both sets of data. The latest development version of Qucs/spice4qucs [9] includes routines for generating Xyce netlists from Qucs schematics. A Xyce netlist for the $npnBlock$ macromodel is given in Fig. 14. This netlist has a similar structure to both the Qucs EDD $npnBlock$ model, Fig. 11, and the Verilog-A $npnBlock$ module, Fig. 12, introduced previously. However, some minor adjustments were required
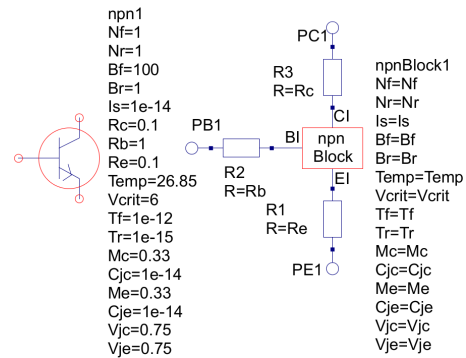
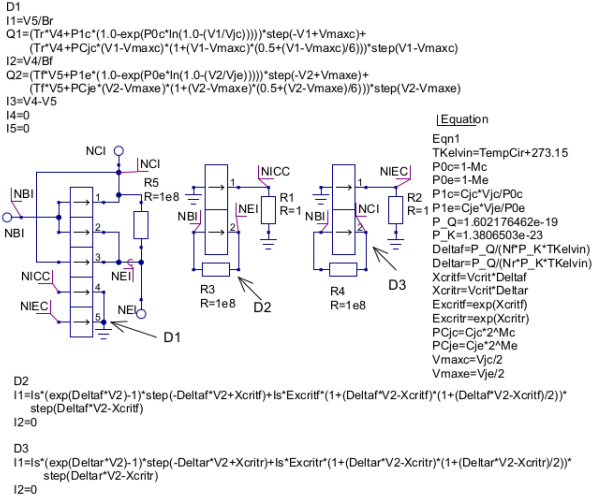**Fig. 10.** An npn BJT compact macromodel: symbol and circuit.

```
D1
I1=V5/Br
Q1=(Tr*V4+P1c*(1.0-exp(P0c*ln(1.0-(V1/Vjc)))))*step(-V1+Vmaxc)+
   (Tr*V4+PCjc*(V1-Vmaxc)*(1+(V1-Vmaxc)*(0.5+(V1-Vmaxc)/6)))*step(V1-Vmaxc)
I2=V4/Bf
Q2=(Tf*V5+P1e*(1.0-exp(P0e*ln(1.0-(V2/Vje)))))*step(-V2+Vmaxe)+
   (Tf*V5+PCje*(V2-Vmaxe)*(1+(V2-Vmaxe)*(0.5+(V2-Vmaxe)/6)))*step(V2-Vmaxe)
I3=V4-V5
I4=0
I5=0
```

```
Equation
Eqn1
TKelvin=TempCir+273.15
P0c=1-Mc
P0e=1-Me
P1c=Cjc*Vjc/P0c
P1e=Cje*Vje/P0e
P_Q=1.602176462e-19
P_K=1.3806503e-23
Deltaf=P_Q/(Nf*P_K*TKelvin)
Deltar=P_Q/(Nr*P_K*TKelvin)
Xcritf=Vcrit*Deltaf
Xcritr=Vcrit*Deltar
Excritf=exp(Xcritf)
Excritr=exp(Xcritr)
PCjc=Cjc*2*Mc
PCje=Cje*2*Me
Vmaxc=Vjc/2
Vmaxe=Vje/2
```

```
D2
I1=Is*(exp(Deltaf*V2)-1)*step(-Deltaf*V2+Xcritf)+Is*Excritf*(1+(Deltaf*V2-Xcritf)*(1+(Deltaf*V2-Xcritf)/2))*
   step(Deltaf*V2-Xcritf)
I2=0
```

```
D3
I1=Is*(exp(Deltar*V2)-1)*step(-Deltar*V2+Xcritr)+Is*Excritr*(1+(Deltar*V2-Xcritr)*(1+(Deltar*V2-Xcritr)/2))*
   step(Deltar*V2-Xcritr)
I2=0
```

Fig. 11. A Qucs npn BJT EDD macromodel block $npnBlock$: For clarity EDD $D2$ and $D3$ currents ($I1$) and charge $Q1$ are displayed on more than one line, BJT current and charge equations are selected with function $step()$.

```
`include "disciplines.vams"
`include "constants.vams"
//
module npnBlock(CI, BI, EI);
inout CI, BI, EI ;  electrical CI, BI, EI;
//
parameter integer Nf = 1 from [1 : inf];
parameter integer Nr = 1 from [1 : inf];
parameter real Is = 1e-14 from [1e-20 : inf];
parameter real Bf = 100 from [1 : inf];
parameter real Br = 1 from [0.1 : inf];
parameter real Vcrit = 6 from [0.5 : inf];
parameter real Tf = 1e-12 from [1e-20 : inf];
parameter real Tr = 1e-11 from [1e-20 : inf];
parameter real Mc = 0.33 from [0.05 : 5];
parameter real Cjc=1.0e-14 from [1.0e-20 : inf];
parameter real Vjc=0.75 from [0.1 : inf];
parameter real Me = 0.33 from [0.05 : 5];
parameter real Cje=1.0e-14 from [1.0e-20 : inf];
parameter real Vje=0.75 from [0.1 : inf];
parameter real Temp = 26.85 from [-100 : 200];
parameter real Tnom = 26.85 from [-100 : 200];
real TKelvin, Deltaf, Deltar, Xcritf, Xcritr, Expcritf;
real Expcritr, PCjc, PCje, Vmaxc, Vmaxe, ICC, IEC, Xr, Xf;
real Vdiffr,Qtc, P0c, P1c, Vdifff, Qte, P0e, P1e;
analog begin
 @(initial_model)
  begin
  TKelvin = Temp+271.15; Deltaf = `P_Q/(Nf*`P_K*TKelvin);
  Deltar = `P_Q/(Nr*`P_K*TKelvin); Xcritf = Vcrit*Deltaf;
  Xcritr = Vcrit*Deltar; Expcritf = exp(Xcritf);
  Expcritr = exp(Xcritr); PCjc = Cjc*exp(Mc*ln(2));
  PCje  = Cje*exp(Me*ln(2)); Vmaxc = Vjc/2; Vmaxe = Vje/2;
  P0c  = 1-Mc; P1c=Cjc*Vjc/P0c; P0e=1-Me; P1e=Cje*Vje/P0e;
  end
 Xr=Deltar*V(BI,CI);
 IEC=(Xr-Xcritr) ? Is*(exp(Xr)-1)
            : Is*Expcritr*(1+(Xr-Xcritr)*(1+(Xr-Xcritr)/2));
 I(BI, CI) <+ IEC/Br;  Vdiffr = V(BI, CI)-Vmaxc;
 Qtc = (V(BI, CI) < Vmaxc) ? Tr*ICC+P1c*(1.0-exp(P0c*ln(1.0-V(BI, CI)/Vjc)))
          : Tr*ICC+PCjc*(Vdiffr + Vdiffr*Vdiffr/2 + Vdiffr*Vdiffr*Vdiffr/6);
 I(BI, CI) <+ ddt(Qtc);  Xf=Deltaf*V(BI,EI);
 ICC=(Xf-Xcritf) ? Is*(exp(Xf)-1)
            : Is*Expcritf*(1+(Xf-Xcritf)*(1+(Xf-Xcritf)/2));
 I(BI, EI) <+ ICC/Bf;  Vdifff = V(BI, EI)-Vmaxe;
 Qte = (V(BI, EI) < Vmaxe) ? Tf*IEC+P1e*(1.0-exp(P0e*ln(1.0-V(BI, EI)/Vje)))
          : Tf*IEC+PCje*(Vdifff + Vdifff*Vdifff/2 + Vdifff*Vdifff*Vdifff/6);
 I(BI, EI) <+ ddt(Qte);  I(CI, EI) <+ ICC-IEC;
 end
endmodule
```

Fig. 12. A Qucs npn BJT Verilog-A code block $npnBlock$: BJT current and charge equations are selected with ternary operator $x?y : z$.
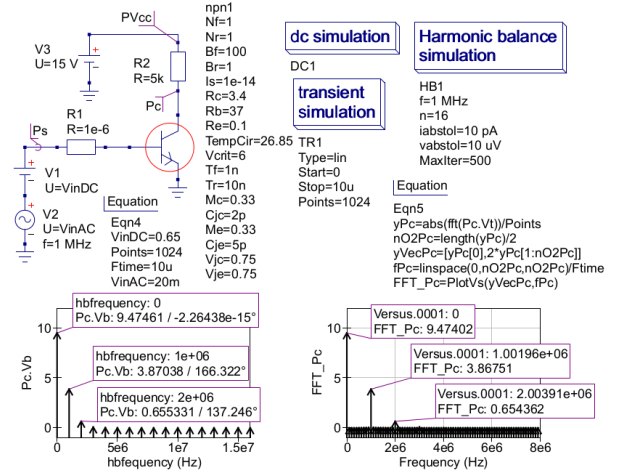

Fig. 13. A BJT HB and transient simulation test bench: Circuit, node Pc HB simulation data and frequency domain spectral plot of transient simulation data.

```
.SUBCKT npnBlock NCI NBI NEI Nf=1 Nr=1 Is=1e-14 Bf=100 Br=1 TempCir=26.85 Vcrit=6
+         Tf=1e-12 Tr=1e-11 Mc=0.33 Cjc=1e-12 Me=0.33 Cje=1e-12 Vjc=0.75
+         Vje=0.75 Rc=1e-3 Rb=1e-3 Re=1e-3
.PARAM TKelvin={TempCir+271.15}
.PARAM P0c={1-Mc}
.PARAM P0e={1-Me}
.PARAM P1c={Cjc*Vjc/P0c}
.PARAM P1e={Cje*Vje/P0e}
.PARAM P_Q=1.602176462e-19
.PARAM P_K=1.3806503e-23
.PARAM Deltaf={P_Q/(Nf*P_K*TKelvin)}
.PARAM Deltar={P_Q/(Nr*P_K*TKelvin)}
.PARAM Xcritf={Vcrit*Deltaf}
.PARAM Xcritr={Vcrit*Deltar}
.PARAM Excritf={exp(Xcritf)}
.PARAM Excritr={exp(Xcritr)}
.PARAM PCjc={Cjc*2**Mc}
.PARAM PCje={Cje*2**Me}
.PARAM Vmaxc={Vjc/2}
.PARAM Vmaxe={Vje/2}
R2 0 NEIC  1
R1 0 NICI  1
BD2I0 0 NICI I=Is*(exp(Deltaf*(V(NBI)-V(NEI)))-1)*stp(-Deltaf*(V(NBI)-V(NEI))+Xcritf)+
+         Is*Excritf*(1+(Deltaf*(V(NBI)-V(NEI))-Xcritf)*(1+(Deltaf*(V(NBI)-V(NEI))-Xcritf)/2))*
+         stp(Deltaf*(V(NBI)-V(NEI))-Xcritf)
BD2I1 NBI NEI I=0
BD3I0 0 NEIC I=Is*(exp(Deltar*(V(NBI)-V(NCI)))-1)*stp(-Deltar*(V(NBI)-V(NCI))+Xcritr)+
+         Is*Excritr*(1+(Deltar*(V(NBI)-V(NCI))-Xcritr)*(1+(Deltar*(V(NBI)-V(NCI))-Xcritr)/2))*
+         stp(Deltar*(V(NBI)-V(NCI))-Xcritr)
BD3I1 NBI NCI I=0
R3 NEI NBI  1E8
R4 NCI NBI  1E8
R5 NEI NCI  1E8
BD1I0 NBI NCI I=(V(NIEC)-V(0))/Br
GD1Q0 NBI NCI nD1Q0 NCI 1.0
LD1Q0 nD1Q0 NCI 1.0
BD1Q0 nD1Q0 NCI I=-((Tr*(V(NICC)-V(0))+P1c*(1.0-exp(P0c*ln(1.0-((V(NBI)-V(NCI))/Vjc)))))*
+         stp(-(V(NBI)-V(NCI))+Vmaxc)+
+         (Tr*(V(NICC)-V(0))+PCjc*((V(NBI)-V(NCI))-Vmaxc)*(1+((V(NBI)-V(NCI))-Vmaxc)*
+         (0.5+((V(NBI)-V(NCI))-Vmaxc)/6)))*stp((V(NBI)-V(NCI))-Vmaxc))
BD1I1 NBI NEI I=(V(NICC)-V(0))/Bf
GD1Q1 NBI NEI nD1Q1 NEI 1.0
LD1Q1 nD1Q1 NEI 1.0
BD1Q1 nD1Q1 NEI I=-((Tf*(V(NIEC)-V(0))+P1e*(1.0-exp(P0e*ln(1.0-((V(NBI)-V(NEI))/Vje)))))*
+         stp(-(V(NBI)-V(NEI))+Vmaxe)+
+         (Tf*(V(NIEC)-V(0))+PCje*((V(NBI)-V(NEI))-Vmaxe)*(1+((V(NBI)-V(NEI))-Vmaxe)*
+         (0.5+((V(NBI)-V(NEI))-Vmaxe)/6)))*stp((V(NBI)-V(NEI))-Vmaxe))
BD1I2 NCI NEI I=((V(NICC)-V(0))-(V(NIEC)-V(0)))
BD1I3 NICC 0 I=0
BD1I4 NIEC 0 I=0
.ENDS
```

Fig. 14. A Xyce npn BJT SPICE subcircuit $npnBlock$: BJT current and charge equations are selected with function $stp()$.

to the Xyce netlist due incompatibilities in some parameter and function names, for example Qucs $Temp$ is replaced by $TempCir$ and Qucs function $step()$ is replaced by Xyce function $stp()$. Shown in Fig. 15 is the Xyce HB simulation spectral data for the magnitude of the voltage at test circuit node Pc. The date illustrated in Fig. 15 confirms the values

VI. AC AND HARMONIC BALANCE SIMULATION OF A SINGLE STAGE RF BJT AMPLIFIER

The schematic for a single stage Rf BJT amplifier is illustrated in Fig. 16. This amplifier is designed to give a 20dB voltage gain at midband frequencies. The theoretical midband
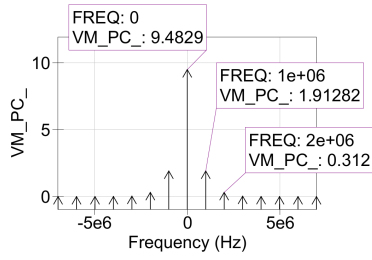
Fig. 15.   Xyce HB simulation data for the magnitude of node Pc voltage: Test configuration identical to Fig. 13.

magnitude of the amplifier voltage gain is given by equation 11 due to the negative feedback introduced by resistor $R9$. The Qucs plots of small signal AC and HB simulation data show very similar values for the output voltage at node $Nout$.

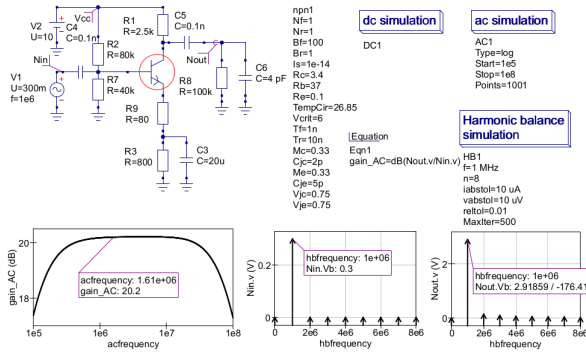$$V gain \approx 20 \cdot log(R1/R9) \qquad (11)$$

Fig. 16.   A 20dB single stage npn transistor RF amplifier: circuit, small signal AC voltage gain and HB simulation data obtained with $R9$ adjusted to give a gain of 20dB at 1MHz.

VII. Conclusions

Harmonic Balance simulation of RF circuits is rarely implemented in GPL circuit simulators derived from Berkeley SPICE 2g6 or 3f5 [10]. Currently, Qucs includes single tone HB simulation. This paper introduces a compact macromodelling approach to Qucs HB simulation which is suitable for simulating RF discrete and integrated circuit steady state AC performance The proposed modelling technique introduces a compact macromodelling structure which reduces HB linear and non-linear circuit partitioning problems and helps reduce the effects of discontinuities in model current and charge differential characteristics on HB solution convergence. Experience with the proposed Qucs HB compact macromodelling method has shown that it is suitable for any general purpose circuit simulator provided it implements HB simulation and can handle Equation-Defined Devices or Verilog-A analogue modules. HB simulation data for a semiconductor diode and an npn BJT are reported. This data was obtained from test simulations using both the Qucs and Xyce GPL simulators.

Good agreement was found between the steady state AC simulation results obtained from Qucs HB simulation and transient time domain simulation.

References

[1] S. Jahn, and M. Brinson, "Interactive Compact Modeling Using Qucs Equation-Defined Devices", Int. J. Numer. Model. 2008, vol 21, pp. 335-349.
[2] G. J. Coram, "How to (and How Not to) Write a Compact Model in Verilog-A", IEEE International Behavioural Modeling and Simulation Conference (BMAS), San José, Calfornia, pp. 97-106, October 2004.
[3] Toshi Lab. (Optical and RF-MEMS Lab), "MEMS DAIQ=MEMS Design and Analysis Interface to Qucs", 2011, http://toshi.iis.u-tokyo.ac.jp/toshilab/?DAIQ [accessed March 2015].
[4] L. Lemaitre, W. Grabinski and C. McAndrew, "Compact device modeling using Verilog-A and ADMS", Electron Technology Internet Journal, Vol. 35, pp. 1-5, 2003.
[5] L. Lemaitre, G. J. Coram, C. McAndrew and K. Kundert, "Extensions to Verilog-A to support compact device modeling", IEEE International Behavioral Modeling and Simulation Conference, BMAS-03, pp. 134-138. October 2003.
[6] S. A. Maas, "Nonlinear Microwave and RF Circuits", Second Edition, Artech House, Boston and London. 2003.
[7] Sandia National Laboratories, "Xyce Parallel electronic simulator: version 6.2", 2015, https://xyce.sandia.gov/ [accessed March 2015].
[8] Avago Technologies, "HSMS-282x Surface Mount RF Schottky Barrier Diodes data sheet, Av02-1320EN, May 28, 2009.
[9] V. Kuznetsov, "QEP: Qucs schematic simulation with ngspice", 2015, https://github.com/Qucs/qucs/wiki/QEP, (also at: https://github.com/ra3xdh/qucs/tree/spice4qucs) [accessed March 2015].
[10] A.R. Newton, D. O. Pederson, A. Sangiovanni-Vincentelli, "SPICE Version 2g User's Guide", Department of Electrical Engineering and Computer Sciences, University of California: Berkeley, CA. 1981, and B. Johnson, T. Quarles, A.R. Newton, D. O. Pederson, A. Sangiovanni-Vincentelli, "SPICE3 Version 3f User's Manual", Department of Electrical Engineering and Computer Sciences, University of California: Berkeley, CA. 1992.
[11] P. Anongnetti, and G. Massobrio (Editors), "Semiconductor Devise Modeling with SPICE", McGrew-Hill Inc., New York, 1988.