Low Power Signal Processing Techniques for Radiometric Partial Discharge Detection in Wireless Sensor Network.

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Abstract

High-voltage infrastructure condition monitoring and diagnostics is essential for the continuous and uninterrupted supply of electricity to the grid. A common metric for establishing HV plant equipment condition is the identification and subsequent monitoring of insulation faults known as partial discharge. Traditional techniques for this require physical connection of sensors to plant equipment to be monitored, leading to potentially high cost and system complexity. A non-invasive and significantly less costly approach is the use of wireless receivers to measure the electromagnetic waves produced by partial discharge faults. Hence, a large-scale monitoring network can be realized to monitor equipment within a substation compound at relatively low cost.

An issue with the use of commercially available wireless sensor technology, based around high-speed data conversion, is ensuring each node is low cost and low-power, whilst still being capable of detecting and measuring partial discharge faults within a reasonable distance. In order to reduce power consumption two signal processing techniques are proposed, a transistor-reset integrator and a gated high-speed analogue-to-digital converter, which provide a low power method of radiometric partial discharge measurement by avoiding continuous high-speed sampling.

The measured results show that the transistor-reset integrator based system is capable of measuring partial discharge over a distance of 10 m with an error within 1 m, and performing location estimation to within 0.1 m as compared to estimation

performed using high-speed sampling, at fraction of the power consumption. The folding ADC based system is able to sample a PD like signal, but requires additional development to improve performance and fully integrate it into a system. The overall results prove the operating principle of the partial discharge monitoring system, which has the potential to be developed into a viable solution.

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Acronyms

ADC	Analogue to Digital Converter
AGC	Automatic-Gain Control
AM	Amplitude Modulation
Balun	Balanced to Unbalanced
CMOS	Complementary Metal-Oxide Semiconductor
DAB	Digital Audio Broadcasting
DAC	Digital to Analogue Converter
DNL	Differential Non-Linearity
DSO	Digital Sampling Oscilloscope
DVM	Digital Volt Meter
FET	Field Effect Transistor
FFT	Fast-Fourier Transform
FM	Frequency Modulation
FPGA	Field Programmable Gate Array
GIS	Gas Insulated Switch-gear
GSM	Global System for Mobile communications
HFCT	High Frequency Current Transformer
HSa/P	High Samples-per-Pulse
HV	High Voltage
INL	Integral Non-Linearity
JFET	Junction Field Effect Transistor
LNA	Low-Noise Amplifier

LSa/P	Low Samples-per-Pulse
LSB	Least Significant Bit
MCU	Micro-Controller Unit
MSB	Most Significant Bit
NI	Non-Inverting
Op-Amp	Operational Amplifier
PD	Partial Discharge
RAM	Random Access Memory
RF	Radio Frequency
RMS	Root Mean Square
RSS	Received Signal Strength
SAR	Successive Approximation Register
SDR	Software Defined Radio
SFDR	Spurious Free Dynamic Range
S/H	Sample & Hold
SHA	Sample & Hold Amplifier
SHFA	Sample & Hold Folding Amplifier
SINAD	Signal-to-Noise-And-Distortion
SMD	Surface Mount Device
SNR	Signal-to-Noise Ratio
SPST	Single-Pole Single-Throw
TDOA	Time Difference of Arrival
TEV	Transient Earth Voltage

THD	Total Harmonic Distortion
TOA	Time of Arrival
TRI	Transistor-Reset Integrator
TV	Television
UART	Universal Asynchronous Receiver-Transmitter
UHF	Ultra-High Frequency
USB	Universal Serial Bus
VGA	Variable-Gain Amplifier
VHF	Very-High Frequency
WSN	Wireless Sensor Network

1 Introduction

1.1 Background

Sensors for pulse-based signals are required in applications such as high voltage (HV) plant condition assessment, portable ultrasound measurements and scintillation gamma and neutron radiation detection. Typically, sensors may be employed remotely which commonly require battery power. Since these applications typically involve the measurement of stochastic pulses, whose duration last from hundreds of nanoseconds to microseconds, continuous high-speed sampling above 10 MS/as is unsuitable, since above this sample-rate analogue-to-digital converters (ADCs) require substantial power for normal operation, which places demands on battery life, and therefore, the operational run-time of the sensor.

The power consumption of the sensor can be drastically reduced by activating the ADC only when a signal is present. This can be implemented using techniques such as gating of ADC clock signals, or utilizing power-down and stand-by modes. However, these techniques are limited, since suitably fast ADCs feature architectures that cannot be activated instantaneously, and therefore, have a time delay from stand-by to active which is typically above a microsecond; therefore, part or the entirety of the pulse requiring measurement is likely to be missed. This is illustrated in Figure 1-1, where a 1 μs pulse is sampled by a 20 MSa/s ADC that requires 500 ns to begin sampling from stand-by.

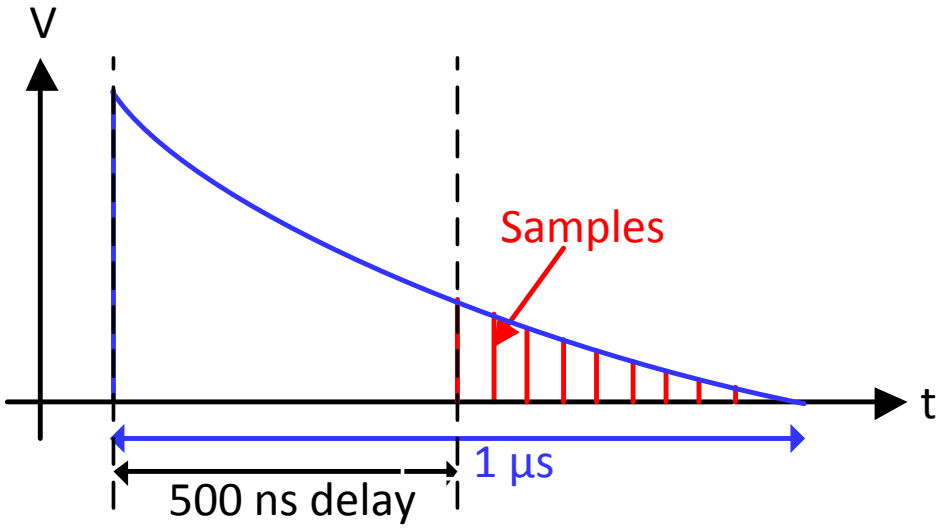


Figure 1-1: Illustration of a Pulse Sampled by an ADC Exiting Stand-By Mode

Additional analogue signal processing can be employed in order to avoid high-speed sampling in battery powered applications, such as peak detectors, integrators and other non-linear circuits, to perform functional operations which modify the signal in such a way that a reduced number of samples is required for each measured event. However, traditional implementations for these circuits have limited bandwidths, due to the requirement in many applications for non-linear components such as switching diodes, and inaccuracies making the speed, sensitivity and dynamic range of such circuits constrained.

Such techniques can be employed for the application of HV plant condition assessment, where monitoring and measuring faults with HV equipment requires low power. Each technique poses advantages and limitations, and therefore, varying

suitability depending on the particular monitoring approach used.

1.2 High Voltage Plant Condition Assessment

The condition of HV plant equipment plays an important role in maintaining the consistency and integrity of the national power grid system. Failures in HV equipment may result in widespread power outages, posing potential safety risks and fines levied against the power distributor. It is therefore vital that the condition of HV plant equipment is periodically assessed and maintained. The condition assessment of HV plant is traditionally employed utilizing hardwired or close-coupling techniques, which may require offline installation, where the HV equipment is de-energized, or fairly extensive implementation procedures for large-scale monitoring.

Online measurement techniques, where installation does not require de-energizing the plant, have been developed which rely on phenomena resulting from the existence of faults within plant, such as sound, light and RF electromagnetic signals, and provide an attractive non-invasive method of HV fault diagnostics. These techniques, however, typically utilize real-time processing in order to provide detailed information of the fault under measurement, placing high demands on signal processing, data conversion rates and data processing requirements; therefore, leading to high power consumption and cost, limiting these high-speed processing techniques to the monitoring of specific HV items or small areas of plant, where a

hard-wired computer based system can be implemented, or short term measurement over a period of a few hours or less using a portable, manually operated, battery powered device, such as a hand-held spectrum analyzer.

In order to provide a large scale solution for HV diagnostics cost and power consumption need to be minimized. This can be achieved by utilizing low power analogue signal conditioning to negate the requirement for high speed data conversion and processing, or by providing a low power method of data conversion. In this thesis two techniques for low power signal conditioning for HV plant diagnostics have been developed and tested. Both techniques are intended for application in battery powered sensors for a wireless sensor network (WSN) capable of large scale monitoring of HV plant equipment.

The failure of HV plant is typically caused by faults which include insulation degradation, loose connections, mechanical parts (such as relays, interrupters and tap changers) and bushings. Insulation degradation, which accounts for a large portion of faults within switch-gear and instrument transformers [1–3], can be assessed through the detection and monitoring of a widely used fault referred to as Partial Discharge (PD), which is discussed in the following section.

1.3 Partial Discharge

A widely used and very effective metric for assessing the condition of HV plant is Partial Discharge (PD). PD is an electrical fault that occurs within the insulating material of high voltage plant equipment, such as transformers, switch gear and transmission lines [4, 5]. It is caused by a decrease in permittivity, and therefore an increase in electric field strength, due to the presence of a void or defect within the dialectric, resulting in a discharge across the void that does not breach the conductors [6, 7], but can worsen over time due to prolonged electrical stresses increasing the physical size of the void. PD is defined by the IEC60270 standard as:

"a localized electrical discharge that only partially bridges the insulation between conductors and which can or cannot occur adjacent to a conductor. Partial discharges are in general a consequence of local electrical stress concentrations in the insulation or on the surface of the insulation. Generally, such discharges appear as pulses having a duration of much less than 1 microsecond" [8].

The frequency and intensity of these discharges may increase over time if the defect becomes physically larger, due to damage such as treeing (cracking to the insulation surrounding the void) caused by prelonged arcing across the void, eventually leading to catastrophic failure when the void is so large that the potential is able to breach the inner and outer conductors (referred to as flashover) [9]. PD faults are more likely to occur in aged HV plant, where long term exposure to constant changes in environmental conditions may accelerate deterioration of the insulating

material, such as thermal expansion and retraction.

An example of a typical PD fault is a gas-filled void within the insulation of a HV transmission line, represented by the Gemant and Phillippoff model [10] shown in Figure 1-2.

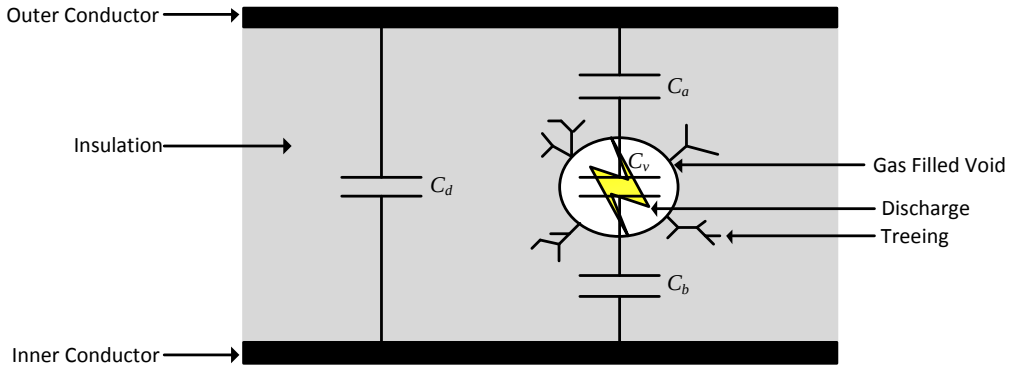


Figure 1-2: Gemant and Phillippoff gas-filled void PD model

C_d is the capacitance of the insulation, C_v is the capacitance of the gas-filled void, and C_a and C_b are the dielectric capacitances in series with the void. As stated earlier, the permittivity of the void is lower than that of the surrounding insulation since the void tends towards the permittivity of air which is lower than that of the insulation; therefore, the electric-field strength within the void is increased and arcing may occur as the AC potential is increased across the conductors. The resulting arcing can weaken the surrounding insulation causing treeing, eventually leading to an increase in the size of the void and a greater risk of catastrophic failure. Figure 1-3 shows an example of a PD current pulse discharged across an

insulation void as a result of the increased field strength within the void [11], where the strength of the PD is quantified by the total charge within it. Typically, the current pulse lasts between 1 ns to 1000 ns [11, 12].

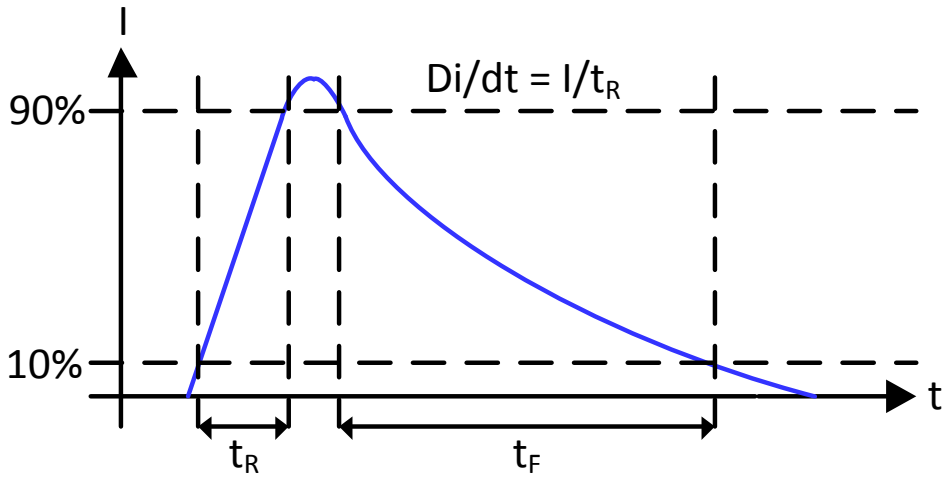


Figure 1-3: A PD Current Pulse across a HV Insulation Void

Detecting and monitoring PD can give an indication of the current condition of fault, and allows for any changes in the condition to be critically assessed over time. Indication that a fault is worsening allows for action to be taken before total failure occurs. Traditional techniques for detecting partial discharge, which include galvanic contact devices, high frequency current transformer (HFCTs) and transient earth voltage (TEV) sensors [13, 14], provide highly accurate and detailed information on any PD activity within the equipment under observation, due to the close coupling of the sensor to the piece of plant, such as a transformer or switchgear. This information includes apparent charge and spectra, giving

indication to the type of PD fault, as well as any fault progression over time.

Due to this requirement of close coupling to each piece of plant to be observed, however, each sensor is only capable of monitoring the equipment it is coupled to, requiring separate sensors for each item of plant to be monitored. Therefore, extensive monitoring of HV equipment within a large-scale substation would be difficult using these techniques, due to the extensive wiring harnessing required, along with the complexity of the data acquisition system needed. Also, reconfiguration of the system, if required, would be difficult, and likely costly, due to the amount of manual labour required to physically reconnect sensors, along with the design and cost of a replacement wiring harness.

Various alternative techniques have been suggested and developed for PD detection, monitoring and measurement, these include optical measurement [15], acoustic techniques [16] and radiometric techniques that utilize the far-field electromagnetic wave propagated from a PD source due to the current discharged over the void. Optical PD measurement involves using fibre optic sensors and probes to detect ionization in oil and gas dielectrics [17] by detecting the light emitted during the ionization process. The benefits of optical PD measurement techniques include immunity to electromagnetic interference, as well as isolation from the HV equipment, due to the use of light coupling. However, a disadvantage is the requirement each sensor to be physically connected to the plant under test.

Acoustic techniques involve capturing localized acoustic emissions from source of PD via audio sensors [18]. Captured acoustic emissions can be cross correlated with know PD transient acoustic patterns in order to assess if the acquired signal is of PD origin [19]. As with optical detection, acoustic techniques have the advantage of immunity to electromagnetic interference. A difficulty with this type of measurement is susceptibility to local ambient noise. Additionally acoustic measurements suffer due to the unpredictability of propagation paths and attenuation, limiting the maximum dielectric thickness that can be measured [20].

Radiometric PD measurement, which is the focus of this thesis, utilizes the electromagnetic signal that is propagated from a source of PD due to the current across the void. This radiometric signal is measured using a radio-receiver placed at a certain distance from the PD source. Figure 1-4 shows the process of receiving a radiometric signal from a source of PD.

The 1-1000 ns current pulse discharged across the void transmits an electromagnetic wave, which has a frequency range of approximately 50-3000 MHz, depending on the type of defect and structure of the void [21]. However, due to the low-pass effect of the band-limiting propagation environment [22], the frequency range is limited to a range of approximately 50-800 MHz [3]. This radiometric signal is then received and measured via a radio receiver. Radiometric PD detection has various advantages, such as ease of installation, comparatively low cost and potential scale-ability. Various disadvantages include susceptibility to electromagnetic

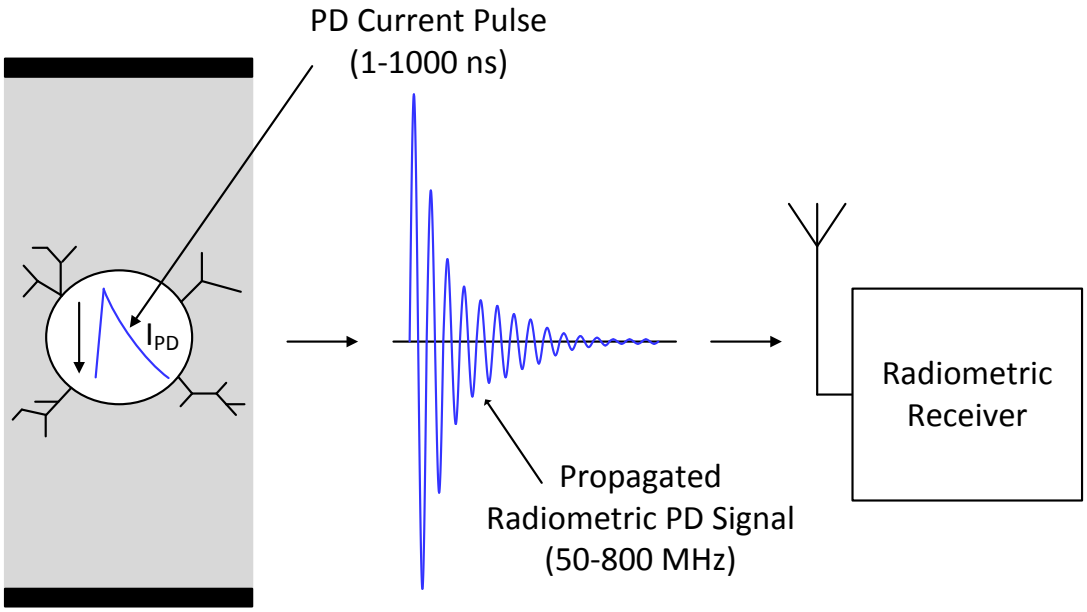


Figure 1-4: Radiometric PD Propagation and Reception using a Radio Receiver

interference, including locally transmitted radio signals, and limited range due to sensor sensitivity and the propagation environment. These effects will be discussed in more detail in the following chapter.

1.4 Aims and Objectives

The main objective of this work is to identify, develop and evaluate low power signal processing techniques suitable for battery powered sensors in a large scale WSN for PD monitoring. The sensors must be capable of monitoring PD over distance whilst lasting at least 12 months from a single battery source, placing strict design guidelines on the circuit implementation.

The main aims and objectives are as follows:

- **To implement techniques to receive and process radiometric signals propagated from a PD source**

The sensors must be capable of receiving a signal from a source of PD over a distance of at least 10 m, and therefore a sensor spacing of 10 m, in order for a radiometric PD monitoring WSN to be plausible.

- **To ensure the sensor nodes are as low power as possible**

Since an operating time of 12 months or greater is required from a single battery source, the circuitry must consume limited power when in operation. Therefore, traditional high-speed data conversion techniques and data processing are unsuitable for long term PD monitoring.

- **To ensure the output of the sensors is a usable quantity**

The sensors should ideally produce an output that can be related to the charge conducted within the PD source, such as the energy of the propagated radiometric signal. As well as being capable of detecting and locating a source of PD, the WSN should potentially be able to provide some useful diagnostic information for a given PD fault.

- **Each sensor node should be as low-cost as possible**

For a large-scale network to be feasible, each sensor should cost as little as possible to ensure that the overall network cost is still a viable option. A total cost of less than £100 is deemed acceptable.

1.5 Original Work

The work presented in this thesis is original and has led to the following original contributions:

- Design and development of two transistor-reset integrators (TRI)s for integration of radiometric PD signals. One is based on precision high-speed components and one is designed using composite amplifier techniques to achieve high-speed and precision at a lower power consumption.

- A technique of using composite amplifiers for high-speed low power field effect transistor (FET) input precision amplifiers and TRIs. The technique combines a very low-power precision op-amp, a low-power high-speed bipolar op-amp and a discrete FET for performance that is not obtainable from a single commercial op-amp.

- Design and development of a high-speed sample-and-hold based folding ADC circuit. The circuit combines a folding amplifier along with a sample-and-hold amplifier (SHA), removing the requirement for two separate circuit sections, and therefore, lowering power consumption and circuit complexity.

- Development of a folding ADC structure optimized for pulsed signal

acquisition. The proposed folding ADC is designed so that sampling only occurs when a signal is present at the input, therefore; power consumption is minimized for most of the sensor operation.

1.6 Document Structure

This thesis is structures as follows:

- The 2^{nd} chapter presents an overview of data acquisition techniques for pulsed signals. Various ADC architectures are then presented with their advantages and disadvantages for pulse signal acquisition, with folding ADCs discussed in further detail to the other architectures. RF power measurement techniques are discussed with focus on the application of pulsed RF signals. Finally, previously proposed techniques for radiometric PD detection are presented along with a critical analysis of each technique.

- The 3^{rd} chapter presents an overview of the radiometric PD WSN, and details the two proposed PD sensors at a system level, with detailed overview of the purpose of each section.

- The 4^{th} chapter details the two proposed techniques at circuit level. The basic and composite TRI designs are presented with a detailed discussion of their operation. The folding ADC is detailed at a system level. The sample-and-hold folding ADC circuit is then presented along with detailed operation and analysis.

- The 5^{th} chapter presents analysis of the performance of the TRI and folding

ADC based systems.

- The 6^{th} chapter presents the results taken from the TRI and folding ADC based systems. Results were recorded for both incremental distance tests and location tests.

- The 7^{th} chapter discusses the results presented in chapter 6.

- Finally, the presented work is concluded with an outline of the main achievements made, along with some suggestions for further work and development.

2 Literature Review

This chapter details the design requirements for processing pulsed signals compared to traditional data acquisition techniques for continuous signals, as well as methods used for processing pulsed signal sources. Suitable ADC architectures are detailed and critically evaluated for pulsed signal processing. Suitable RF power measurement techniques are presented for pulse signal processing. Finally, existing techniques for radiometric PD measurement using wireless and RF technologies are presented and discussed.

2.1 Data Acquisition Techniques for Pulsed Signals

Most data acquisition applications are designed for processing continuous signals, where the received signal is always present, and therefore, continuous sampling can be used to digitize and measure the signal of interest. The two main acquisition techniques for continuous sampling are oversampling and undersampling. Whilst the higher number of samples per cycle can give better measurement accuracy, undersampling is becoming much more common for RF communication systems, such as software-defined radio (SDR), due to the lower sample-rates required, and therefore, lower power requirements and cost.

Oversampling is defined as a sample-rate greater than twice the maximum frequency component of the signal being sampled, whilst undersampling is defined as sampling below twice the maximum frequency component of the signal [23]. Figure 2-1 shows

an example of oversampling verses undersampling.

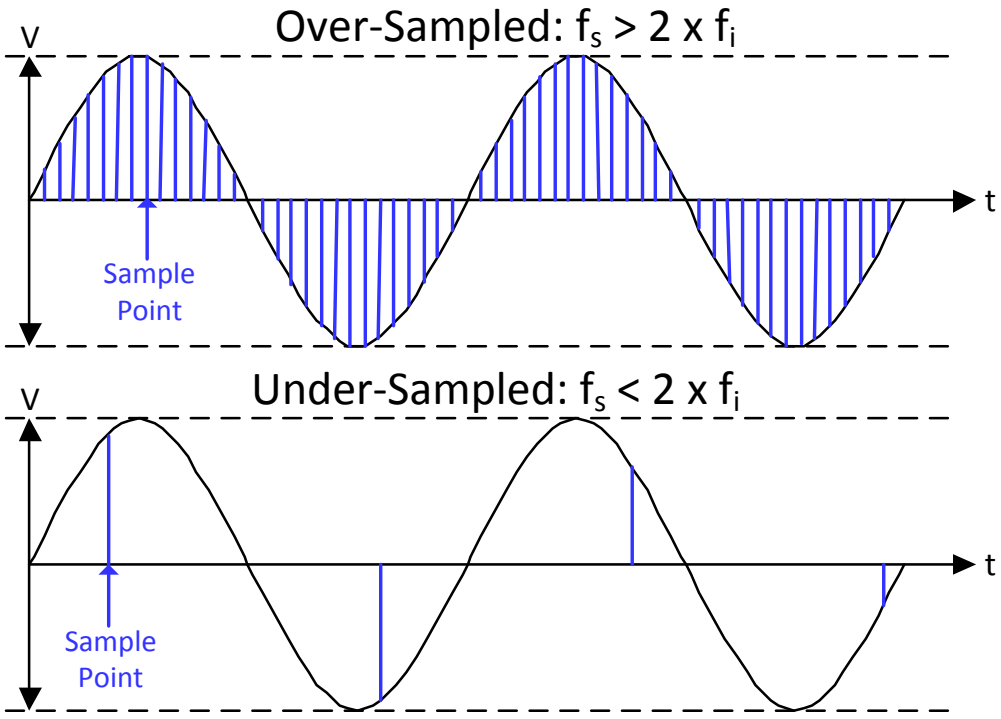


Figure 2-1: Example of OverSampling and UnderSampling

Typically, oversampling is used in systems where measurement is performed within a large bandwidth, such as digital sampling oscilloscopes (DSO) [24], which usually feature sampling-rates that are at least four times greater than the -3 dB bandwidth of the DSO. Oversampling is also used in systems where high accuracy measurement is required, and therefore, high resolution, thus averaging is performed to reduce the noise present and increase the number of bits obtainable [25]. Therefore, the signal must be sampled at a much higher rate in order for averaging to be effective.

For pulsed signals the term oversampling is not applicable, since pulsed signals are time-limited, and therefore, have infinite bandwidth [26]. High sample-rates still yield high accuracy for pulsed signals, since the higher harmonics are usually a significantly lower amplitude than those below the sampling frequency. Therefore, the terms high samples-per-pulse (HSa/P) or low samples-per-pulse (LSa/P) will be used in place of oversampling and undersampling, where HSa/P is defined as at least 10 samples-per-pulse. Data acquisition of fast pulsed analogue signals may place limitations on the performance parameters when using either HSa/P or LSa/P. Whilst HSa/P provides a high measurement accuracy, it requires high power consumption and potentially high cost. Since samples are being continuously taken at a high data rate, most of the samples are redundant due to the time pulses are present to the that of the total measurement time being minor. Figure 2-2 shows an example of a 310 ns duration pulse being sampled at a rate of 100 MSa/s.

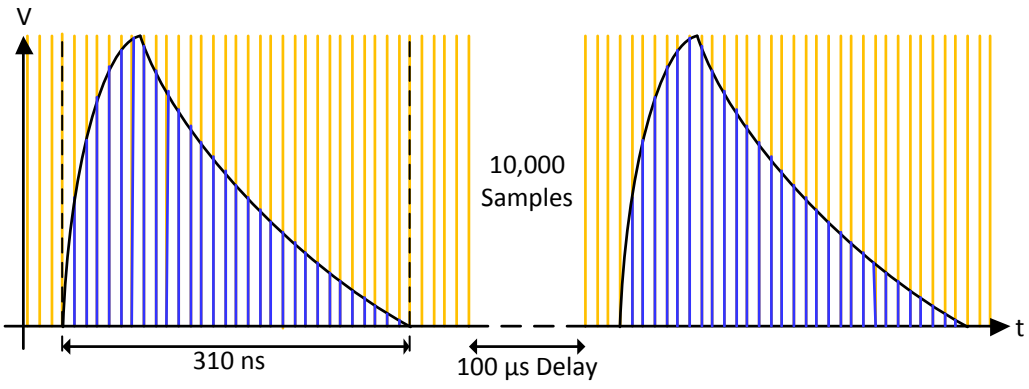


Figure 2-2: HSa/P of a 310 ns Duration Pulse at 100MSa/s

In this example, the pulse is sampled a total of 31 times, which should provide

enough information for different measurements, such as the peak height, pulse rise and fall times, the integral, and pulse shape. However, the time between pulsed events is 100 μs; therefore, 10,000 samples are acquired that contain no signal information. Even though these samples can be ignored using digital logic, they still make the system inefficient, considering the power consumption required for 100 MSa/s.

Using LSa/P for the acquisition of high-speed pulsed signals has contrasting difficulties in comparison to HSa/P, with the power consumption being much less significant, whilst measurement accuracy is much more of an issue. Figure 2-3 shows an example of a 350 ns pulse sampled at rates of 10, 5 and 2.5 MSa/s.

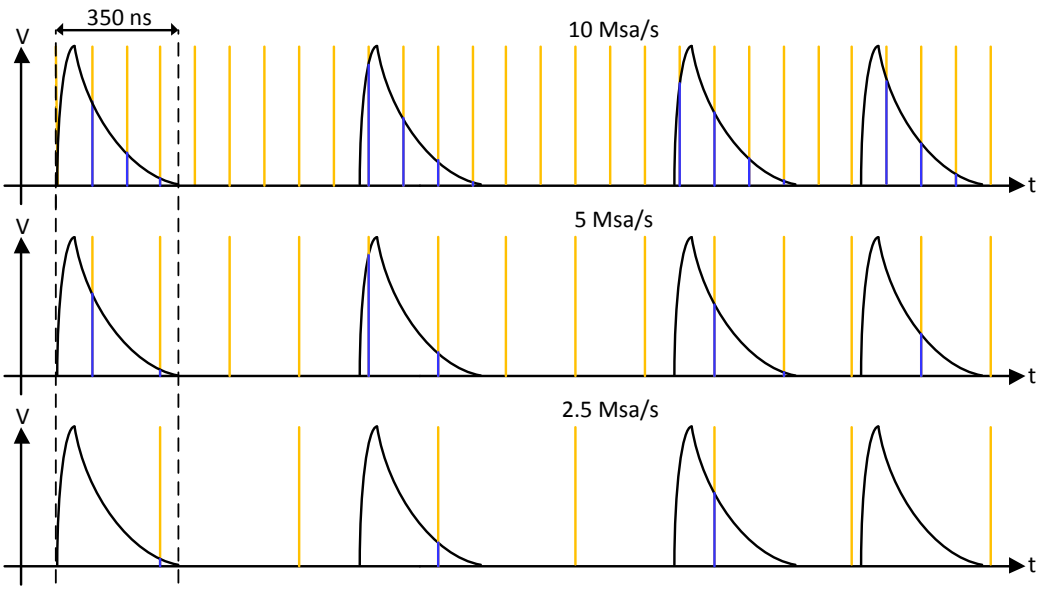


Figure 2-3: LSa/P of a 350 ns Duration Pulse at 10, 5 and 2.5 MSa/s

At a sample rate of 10 MSa/s 3 samples are acquired for each pulse on average. Whilst this will not provide accuracy comparable with HSa/P, it may be adequate for an approximate estimation of various characteristics of the measured pulse. At a sample-rate of 5 MSa/s the average number of acquired sampled per pulse drops to 1, with some pulses being intermittently sampled twice. Dropping this sample-rate further still to 2.5 MSa/s results in only one sample per pulse, and a chance of missing the pulse entirely. Reducing the sample-rate further still would increase the probability of this. Therefore, acquisition via HSa/P is a much more attractive option for high-speed pulsed analogue signals due to the increased measurement accuracy.

In many applications HSa/P is used for pulsed signal acquisition, generally where power consumption and efficiency are not critical. However, if high efficiency is required, the system must be capable of digitizing only when a signal is present. This may involve including some analogue signal processing prior to digitization, as well as activating the ADC when a received signal is detected. This is limited, depending on the sample-rate required and activation time, due to the architecture of the ADC, as well as the design of the analogue pre-processing.

2.2 Comparison of ADC Architectures

There are various well established architectures for ADCs which are, generally speaking, specific to applications, depending on resolution, sample-rate and linearity.

The main architectures available are sigma-delta, successive approximation registers (SARs), pipelined, slope and dual slope integrating, folding, folding and interpolating, and flash. Sigma-delta ADCs are generally constrained to low sampling rates, due to the use of oversampling to achieve high resolutions [27]. Therefore, Sigma-Delta ADCs are typically only used in high quality audio and high accuracy, low-speed, sensor applications [28, 29].

Single and dual slope integrating ADCs can provide high resolution and good noise performance [30]. The integrating ADC utilizes a precision integrator and reference voltage to generate a slope voltage equal to that of the input, a counter is then used to determine the input voltage [31]. The requirement for a counter makes integrating ADCs only suitable for low to medium sample rates, typically 500 times lower than that of the SAR architecture [32]. The accuracy of single slope integrating ADCs is also limited by component tolerances, whilst dual slope types are designed to eliminate this dependence [33].

The folding and interpolating architecture uses a subranging scheme similar to the pipelined architecture; however, they use a parallel structure with a course and fine flash ADC to achieve higher resolutions [34]. They are typically used in commercial devices for sample-rates beyond 1 GSa/s, and typically dissipate power in excess of 1 W, and therefore, are not suitable for low-power radiometric PD acquisition. Pipelined, flash and folding architectures are all capable of achieving sample rates greater than 10 MSa/s, whilst SAR ADCs are limited below this speed. In the

following sections each of these architectures is detailed, along with the advantages and disadvantages in general, as well as specifically to pulsed signal processing.

2.2.1 Successive Approximation Register ADC

The SAR ADC, shown in Figure 2-4 [35], is one of the most widely used architectures. The SAR contains a front-end sample-hold amplifier (SHA), a comparator, a digital-to-analogue converter (DAC), along with control and timing logic.

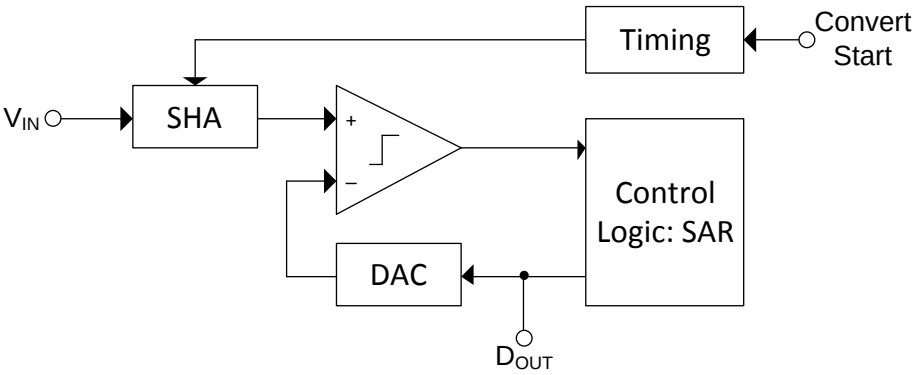


Figure 2-4: SAR ADC Block Diagram

An input voltage is applied to a SHA, which is captured and held, and applied to the input of a comparator when a logic high is applied to the convert start input. The second comparator input is connected to the output of a DAC, which has a resolution equal to that of the ADC. The DAC outputs a voltage equal to half

the input range, causing the output of the comparator to give the most significant bit (MSB), which is loaded into the SAR on the first clock cycle. The DAC then outputs a voltage equal to either 1/4 or 3/4 the input range, depending on whether the MSB was low or high respectively. This process is repeated for each successive bit down to the least significant bit (LSB) on each clock cycle. Figure 2-5 shows the operation of a 4-bit SAR ADC.

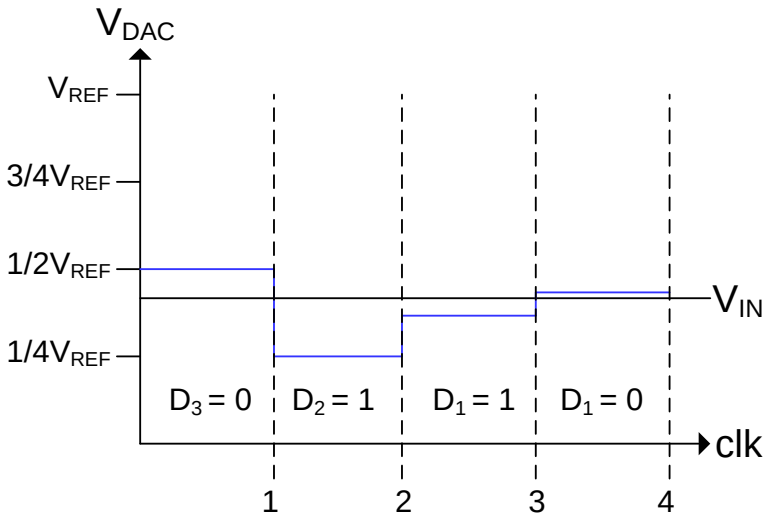


Figure 2-5: 4-bit SAR ADC Operation

Since each bit is generated on a successive clock cycle, the conversion time is dependent on the clock speed as well as the resolution of the ADC, for example; a 10-bit 1 MSps SAR ADC will require a 10 MHz clock for correct conversion.

The SAR has the benefit of a simple architecture, which can be implemented with little space onto silicon with minimal cost. Due to this, SARs are generally used for internal ADCs in micro-controllers along with other system on a chip (SoC) devices [36]. A benefit of the SAR is that sampling can be performed instantaneously as soon as a logic high is applied to the convert start input [37]. However, the sample rate of the SAR is limited due to the clock per bit conversion process [38, 39], meaning that the SAR has historically been used only in low speed low power applications, although in recent years, with the advancements in CMOS, SAR designs have been reported with sample rates in the region of 1 GSa/s [40]. However, no commercial SARs are available featuring sample rates above 20 MSa/s.

2.2.2 Flash ADC

Flash ADCs are the fastest and simplest architecture for low resolution data conversion [41]. A flash ADC comprises 2^{n-1} comparators in parallel, where n is the number of bits for the converter. A 3-bit flash ADC is shown in Figure 2-6.

Referring to Figure 2-6, the input voltage is applied to each parallel connected comparator, whilst the second input of each comparator is connected to a resistive reference voltage string. Each section of the resistive string sets the threshold level of each comparator to a voltage equal to a resolution step. The comparator outputs are then applied to a priority encoder to convert the signals to a 3-bit parallel binary word. Due to the parallel operation, the flash architecture features

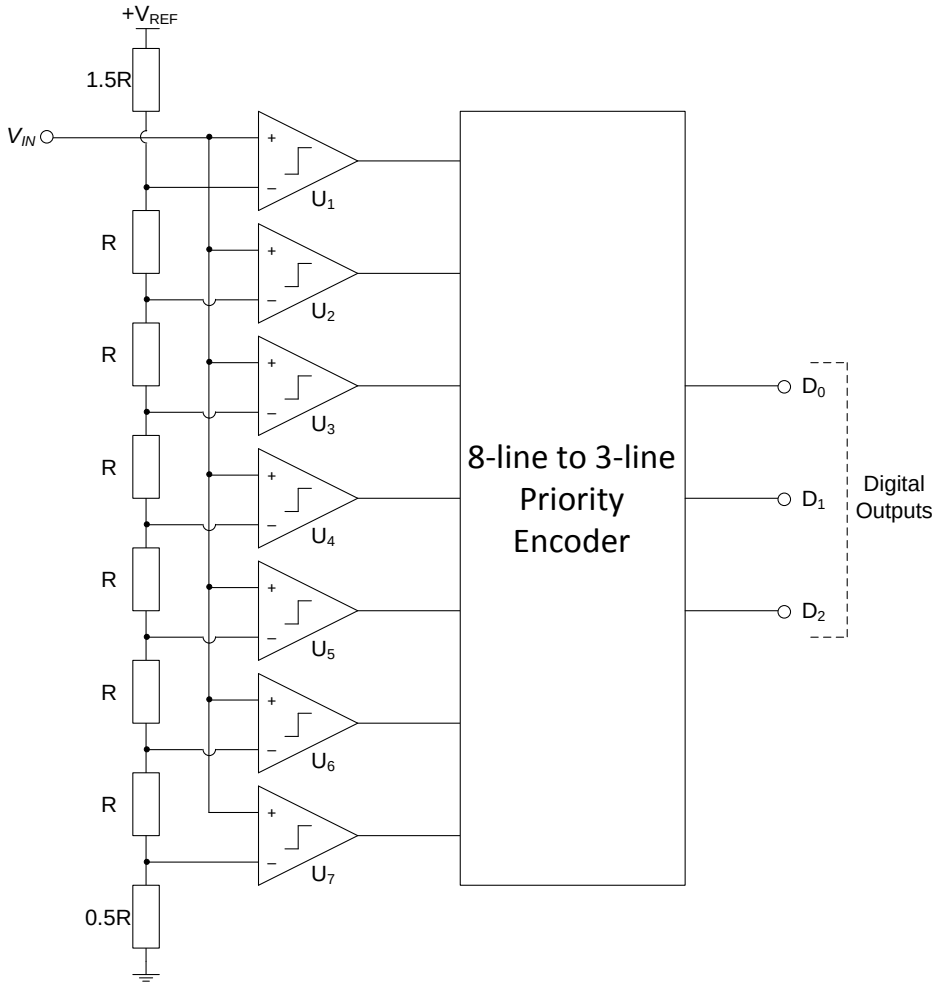


Figure 2-6: 3-bit Flash ADC Circuit Diagram

the fastest conversion speed [42].

The flash architecture has several limitations that constrain its use to specific applications, where typically only low resolutions (8-bit or less) are required, since the number of comparators required doubles per bit [43], meaning an 8-bit ADC would require 255 comparators. The requirement for 2^{n-1} effectively

doubles the size of the IC as well as the power consumption with every additional bit of resolution [44]. Along with these restraints on complexity and power consumption, bandwidth is severely hindered since the parasitic input capacitance of the comparators are paralleled, increasing the overall input capacitance of the ADC [45, 46].

2.2.3 Pipeline ADC

The pipeline ADC can be viewed as a compromise between flash and SAR architectures. The pipeline ADC utilizes multiple flash ADCs for conversion; however, the resolution of the flash is limited to 3 or 4 bit to reduce the required amount of comparators [47]. A 16-bit pipelined ADC is shown in Figure 2-7.

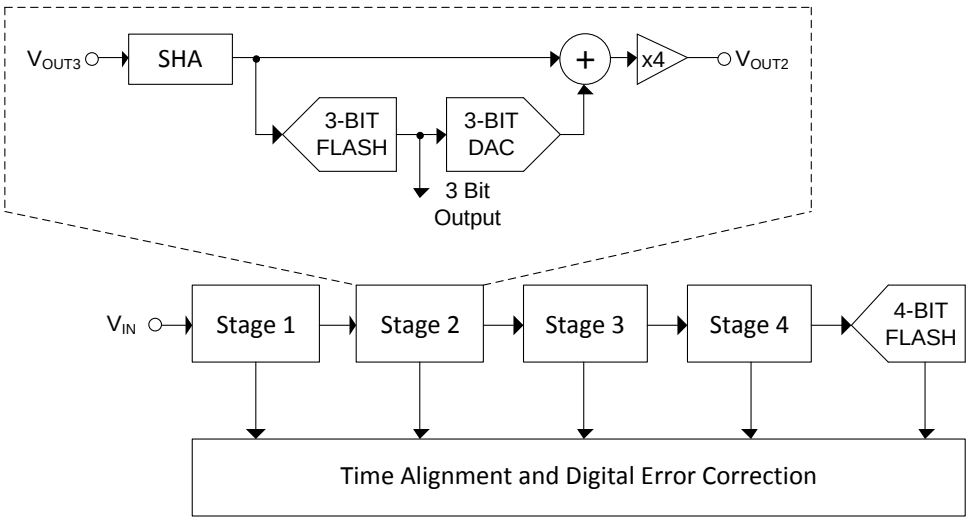


Figure 2-7: 16-bit Pipelined ADC Block Diagram

The pipelined ADC in 2-7 consists of a number of series connected identical stages. Stage 1 samples the input and applies it to a 3-bit flash ADC, which provides the 3 MSBs of data. The flash output is then converted back to an analogue voltage via a 3-bit DAC and subtracted from the original input voltage to produce a residue voltage. The residue voltage is then amplified by a factor of 2^{n-1} (4 for a 3-bit ADC), to scale it to the full input voltage range, and applied to stage 2. Each following stage produces the next 3 MSBs, with the final 4 LSBs produced by a 4-bit flash [48].

Due to the series structure of this architecture, there is a latency from input to output in the pipelined ADC due to the serial propagation through each stage [49]. Whilst there is a latency due to the number of pipelined stages, the throughput is still a sample per clock, as with flash ADCs, since multiple conversions are in serial at each stage [50]. The main source of errors in the pipelined architecture are comparator offset voltage, op-amp finite open-loop gain and switched-capacitor mismatch [51, 52]; therefore, typically additional redundant bits are taken in order to perform error correction to the converted digital codes [53], increasing the complexity of the ADC. A further difficulty for acquisition of pulsed signals is that sampling cannot be triggered instantaneously due to time delays required for the internal circuitry circuitry to stabilize, which is typically greater than 1 μs; therefore, sampling must be done continuously in between received pulsed signal at a greater cost in power consumption.

2.3 The Folding ADC Structure

The folding ADC takes in name from the non-linear response it uses for data conversion. The folding ADC is comprised of stages which produce a non-linear 'folding' output to a linear input signal, as shown in Figure 2-8.

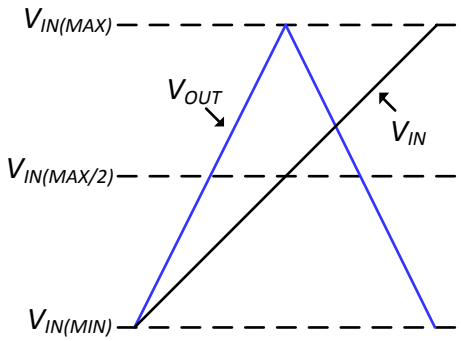


Figure 2-8: Folding Stage Input/Output Response

The output increases linearly with the input signal up to half the input range, after which the output folds and begins to tend back to $V_{IN(MIN)}$. The transfer function of the folding stage is given by Equation 1.

$$V_{OUT} = \begin{cases} A_V V_{IN} & \text{if } V_{IN} \leq V_{REF} \\ A_V(2V_{REF} - V_{IN}) & \text{if } V_{IN} > V_{REF} \end{cases} \quad (1)$$

where A_V and V_{REF} are the stage voltage gain and half the input range reference voltage. Folding ADCs are a relatively old architecture, first reported in 1956 [54]. The folding ADC uses an analogue to Gray code conversion scheme, and provides

1-bit of resolution per stage. The basic folding ADC architecture is shown in Figure 2-9 [35].

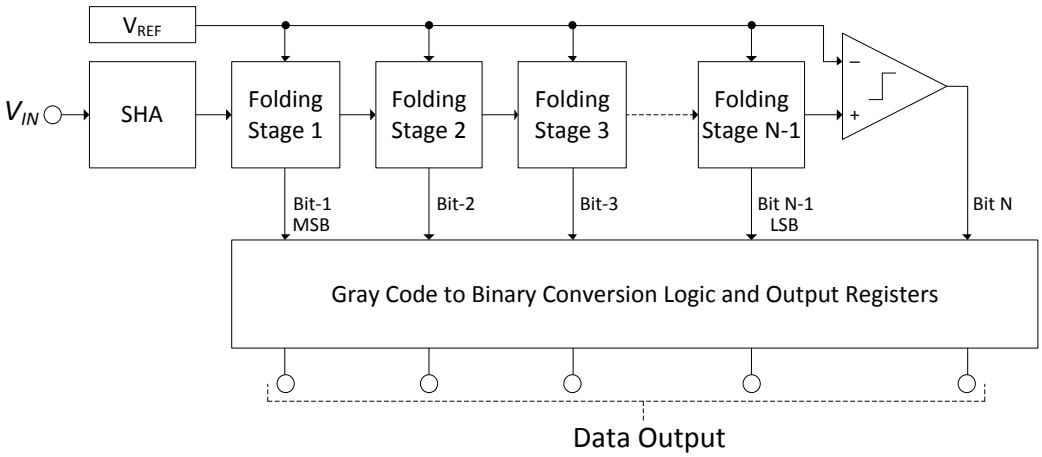


Figure 2-9: Folding ADC Block Diagram

The analogue input signal is applied to a SHA, which then applies the sampled signal to the first folding stage. Within the folding stage is a comparator with a reference voltage equal to half the input range. The comparator produces the MSB of the Gray-coded data word. The folded output of the first stage is then applied to the second stage which provides the next significant bit and folds the signal once again. This process is repeated through each stage until the N-1 bit, where a single comparator is used to acquire the LSB. Figure 2-10 shows the principle operation of the folding ADC for 4 stages.

The folding architecture has not been popular in recent years and has been overshadowed by the pipelined ADC. However, the folding ADC has the benefit

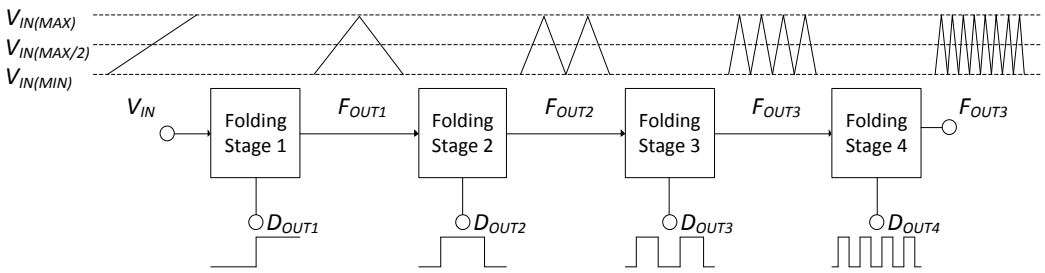


Figure 2-10: Folding ADC Principle Operation [55]

of producing a bit of resolution per stage, meaning the circuitry required for the folding ADC is much less, and therefore, the power consumption is reduced. Numerous folding circuits have been developed, with various advantages and disadvantages.

The MagAMP$^{\mathrm{TM}}$ [56], developed at Analog Devices during the 1990's, is a simple circuit that produces signal folding. The circuit is shown in Figure 2-11.

The MagAMP$^{\mathrm{TM}}$ is built around a Gilbert cell, which is commonly used for analogue multiplication and RF mixer applications, as well as phase detectors in phase-locked loops (PLLs) [57–59]. Here, the arrangement is used as a current-steering folding stage. The input signal is applied to the lower emitter degenerated differential pair, which are biased by identical current sources I, along with a high-speed, fully differential, comparator. The collector currents of the lower differential pair are switched between half of each of the upper pairs, depending on the polarity of the input signal.

With no difference between the inputs, the differential tail currents are conducted

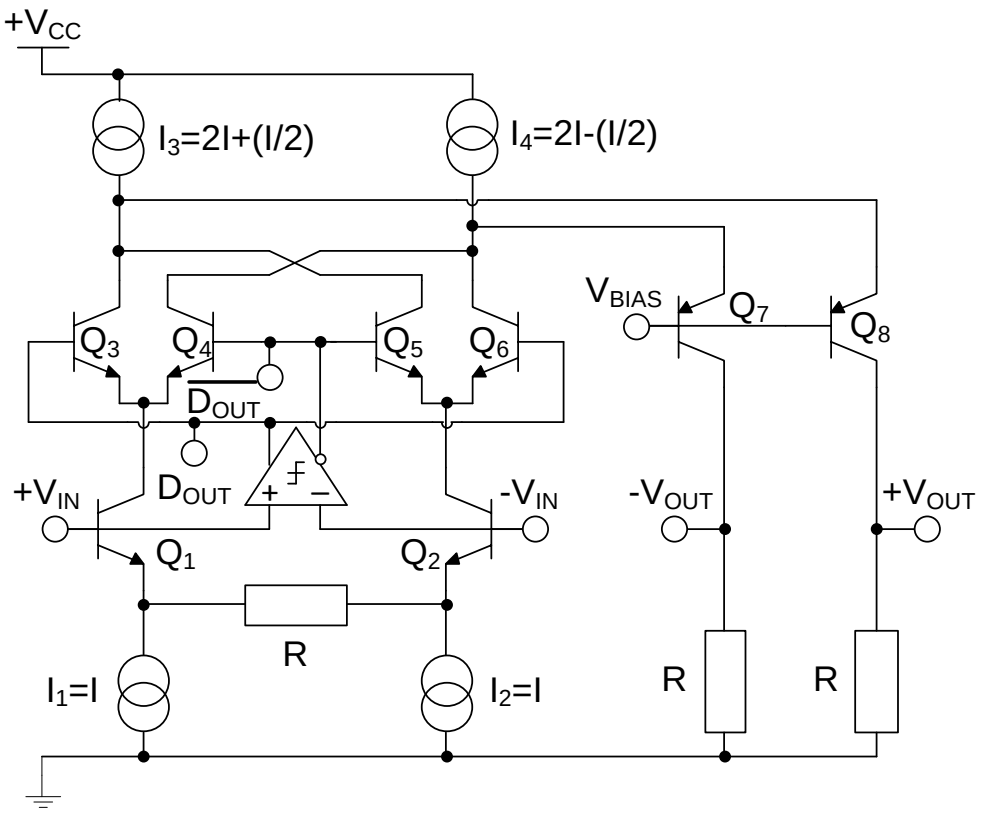


Figure 2-11: MagAMP Circuit Diagram

equally through the upper differential pairs, causing equal currents to flow through commom-base amplifier output transistors Q_7 and Q_8, with the difference between the outputs at the maximum level. If $+V_{IN}$ is greater than $-V_{IN}$ then transistors Q_3 and Q_6 are turned on, and transistors Q_4 and Q_5 are turned off; therefore, an increased amount of the differential tail currents I_1 and I_2 are conducted through Q_1, and a decreased current flows through Q_2. Therefore, the differential voltage at the outputs decreases from the maximum level, with the minimum level reached at max V_{IN}.

If $+V_{IN}$ is driven less than $-V_{IN}$ then transistors Q_3 and Q_6 are turned off, and transistors Q_4 and Q_5 are turned on, causing a decreased tail current to flow through Q_4 and an increased tail current to flow through Q_5. Since the collectors of Q_3 and Q_5 are connected, along with the collectors of Q_4 and Q_6, the polarity of the output is identical to a positive input change, with the differential output decreasing from the maximum level towards the minimum. The midpoint output level is maintained to the same value by adding I/2 to I_3 and subtracting I/2 from I_4.

The MagAMP^{TM} is fully differential; therefore reducing switching and common-mode noise, along with removing the requirement for precision voltage references. The basic structure of the MagAMP^{TM} ADC was a converter utilizing 5 MagAMP^{TM} stages and a 3-bit to obtain 8-bit resolution [60], and was used in the AD8054A commercial 8-bit ADC [61]. The MagAMP^{TM} based ADC has the disadvantage that the structure is designed so that the S/H input signal is required to propagate through all stages simultaneously; therefore, the bias currents must be relatively high to ensure the bandwidth of each stage is wide enough, since transistor current gain over frequency is proportional to current it is biased at [62], to minimize the total cumulative propagation time through the stages. Higher resolution was added by using a structure similar to that of a pipelined ADC [63,64] using FA-based ADCs instead of flash, as shown in Figure 2-12. This structure was used for the 105 MSa/s AD6645 ADC [65].

Here, the input is applied to a 5-bit ADC that is a cascaded series of 5 FAs. As with

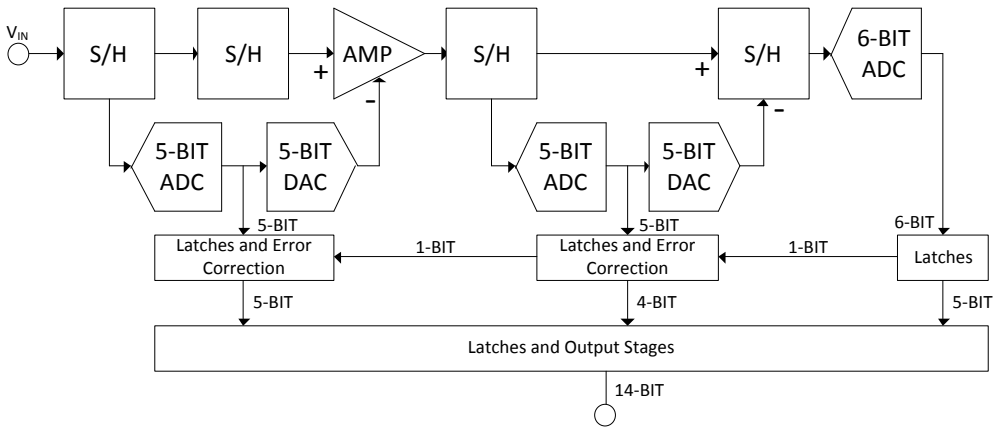


Figure 2-12: Simplified 14-Bit Pipelined Folding ADC Block Diagram

the pipelined architecture, a 5-bit DAC is used to convert the digitized word back to an analog voltage. This is then subtracted from the input signal, and the result is then amplified by 16. The amplified residue is then applied to another FA-based 5-bit ADC via a S/H. In a similar fashion to the first pipelined stage, the output of the 5-bit ADC is converted back to an analogue signal via a 5-bit DAC and is then subtracted from the first residue. The result is then applied to a final 6-bit ADC, which has a gain of 16 MagAMP$^{\mathrm{TM}}$ as the first stage to amplify the residue. The outputs of the second and third ADCs provide 1-bit of error correction to the previous ADCs, making 2-bits of the 16-bit conversion redundant, and therefore, a total conversion of 14-bit per sample.

Whilst the resolution is greatly increased from the 8-bit serial structure to 14-bit, the circuit complexity is higher, since additional DACs and redundancy is required for high-speed operation. Therefore, power consumption is increased as well as die

area, resulting in lower yield and higher cost [66]. A further disadvantage is that whilst high precision is not required for the 5-bit folding ADCs, since digital error correction is used, it is required for the two DACs. This is due to the dependence on accuracy during the subtraction process, which is amplified in both DACs by a factor of 16; therefore, any error due to non-linearity in the DAC response is amplified, causing a greater error to the overall linearity of the ADC. Therefore, the first DAC requires precision to within 14-bits, and the second precision to within 10-bits [64].

2.4 RF Power Measurement Techniques

The measurement of power signals is an important factor in the design of RF and microwave systems to ensure correct operation and optimal performance. Whilst at low frequencies (below 10 MHz) voltage and current measurements are accurate, at higher frequencies they become difficult due to reflections, standing waves and impedance mismatch as the wavelength of the signal decreases to that of the conductor it is traveling through [67]. Typically, RF power measurements are performed in receiver and transmitter systems, to ensure adequate amplification is applied to a received signal for optimal SNR for example, or to monitor the strength of a transmitted signal to ensure transmission covers a specific area. Power detection can be divided into two main categories, consumer level devices such as radios, mobile phones and television, and high level bench equipment for design, test and manufacturing.

The cost and performance of consumer level power detection is much less than that of professional bench type measurement equipment, with bench power meter and sensors providing the most accurate measurements. Consumer level devices can be grouped into three types, rms-responding, logarithmic and Schottky-peak detectors, the simplest and least expensive of these being Schottky-peak detectors. Schottky-peak detectors can be passive or active, where the simplest form is a single Schottky diode, a resistor and a capacitor, know as a zero-bias detector [68], shown in Figure 2-13.

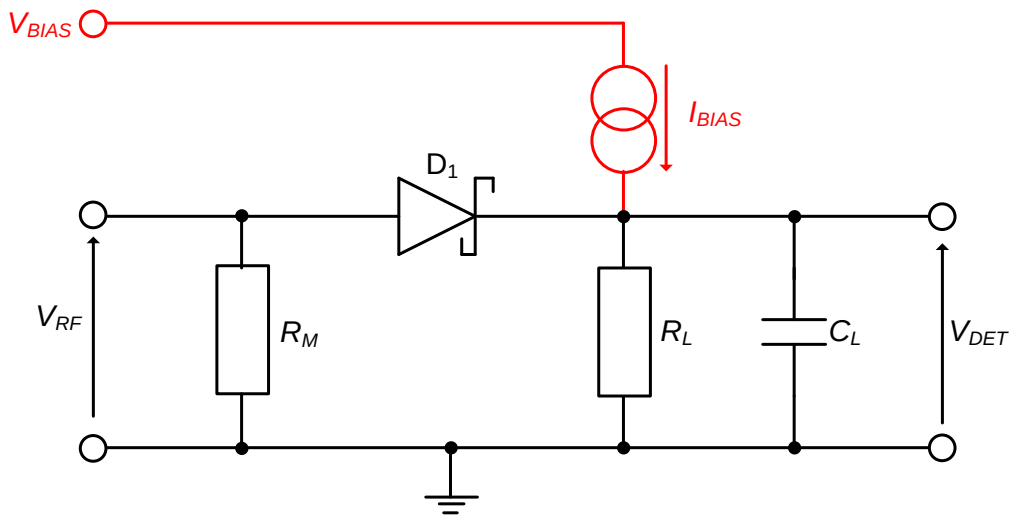


Figure 2-13: Schottky Diode Zero Bias Peak Detector

The zero bias detector uses the exponential response of the diode, below the turn-on voltage, to produce an output voltage that is an approximate square of the input, and therefore, an output voltage that is an approximation of the input power [69, 70]. This behavior is typically limited to input powers below -20 dBm,

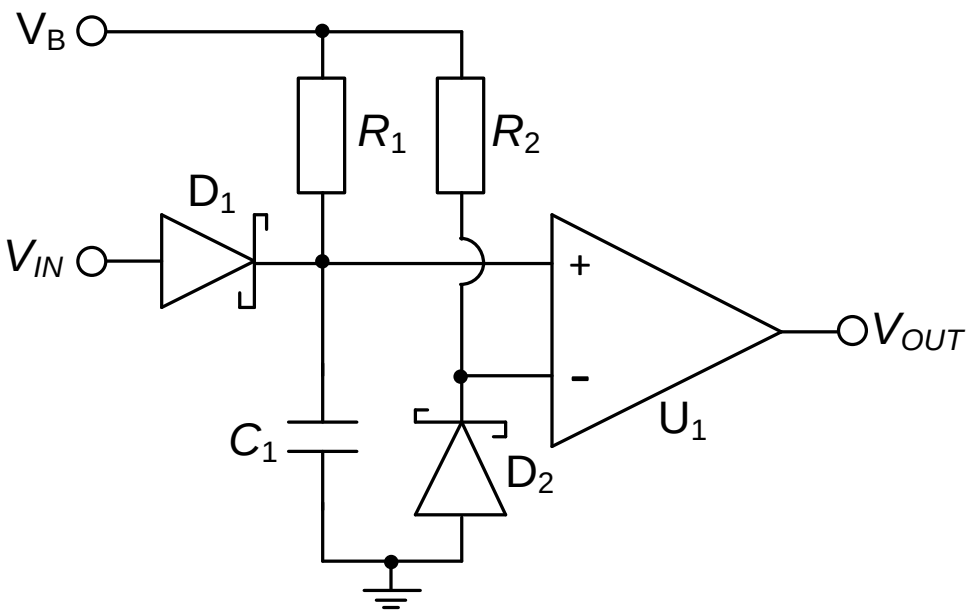


Figure 2-14: Differential Zero Bias Detector

depending on the diode used. Above this value the detector starts to deviate towards a linear response as the input power is increased. The low bulk resistance of the diode allows capacitor C_L to charge rapidly, and to discharge at a slower rate through resistor R_L, careful selection of component values ensures that the output follows the envelope of the input signal. The detector sensitivity can be increased in some cases using a bias network, shown in red, by turning the diode on by a few milli-volts to tens of milli-volts.

Active diode detectors can provide higher sensitivity and better temperature stability when using a differential configuration [71]. A basic differential zero-bias detector is shown in Figure 2-14.

U_1 is a differential amplifier. Diode D_1 and capacitor C_1 form a Schottky detector

on the non-inverting input of the differential amplifier, which is biased through R_1 via V_B. Diode D_2 is applied to the non-inverting input of the amplifier and is biased through resistor R_2 which is equal to R_1, and provides temperature compensation by matching variations to the forward voltage of D_1 so that any effects are canceled at the output of the differential amplifier. Ideally, D_1 and D_2 are matched on a single silicon substrate for close thermal tracking. An issue with this type of detector is that sensitivity is decreased due to the diode biasing.

Logarithmic detectors use a cascade of fixed gain amplifiers to compress the input voltage to a logarithmic response. A typical logarithmic detector architecture is shown in Figure 2-15 [72].

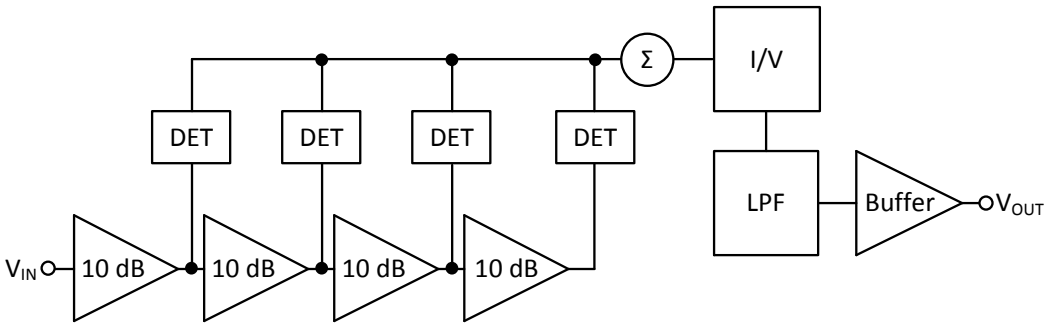


Figure 2-15: Logarithmic Responding Detector

The output of each amplifier is rectified using a current-mode full-wave or half-wave detector. The rectified signals are then summed together and applied to a trans-conductance amplifier to convert the signal back to a voltage. This voltage is then applied to a low-pass filter with a -3 dB frequency in the video-bandwidth range (usually between 10-40 MHz) to remove the high frequency content, leaving

only the envelope of the signal. the filtered signal is then buffered to the output. Since the output voltage is the logarithm of the input voltage, it can be related to the input power in dBm by determining the slope of the output voltage for two input powers.

Logarithmic detectors have a sensitivity below -50 dBm, and usually feature very high dynamic range (typically in excess of 70 dB). However, most logarithmic amplifiers are limited by their response times, which can be as high as micro-seconds, making them incapable of tracking the fast transient response of a radiometric PD signal and only suitable for continuous signals.

RMS-responding detectors, also known as tru-RMS detectors, give an output voltage that is an accurate representation of the true RMS signal power. The simplified architecture of the AD8362 RMS-responding detector is shown in Figure 2-16 [73].

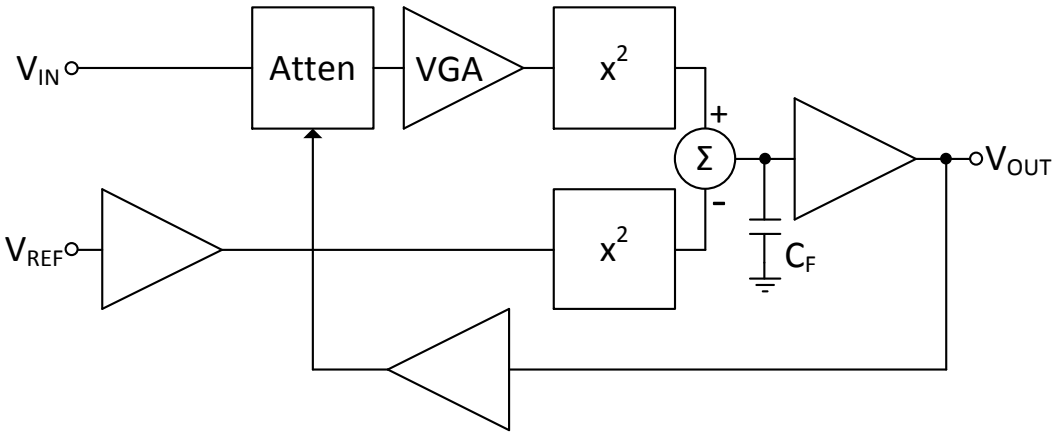


Figure 2-16: RMS−Responding Power Detector

The input voltage is applied to a resistive attenuator to adjust the range of the

received signal, and then to a variable-gain amplifier (VGA), which produces a linear-in-dB output response, that is, an output that is a set amount of mV per dB. The output of the VGA is applied to an RMS-to-DC converter, which produces an output that is the RMS of the VGA output. A precision voltage reference is applied to V_{REF} and is also applied to an RMS-to-DC converter, and the two RMS values are fed into an error amplifier. The error signal is then used to control the gain of the VGA, with a higher error signal causing a higher reduction in gain. This operation is similar to automatic-gain control (AGC), with the output increasing or decreasing the gain of the VGA until the error signal is nulled, increasing the overall dynamic range of the detector.

RMS-responding detectors produce an output voltage that is independent of the waveform shape, and are therefore typically used for transmit and receive signal strength where high accuracy is required. The accuracy of RMS-responding detectors is with 1 dB, with good temerature stability and linearity. However, they typically require higher power consumption due to the additional circuit complexity. They also typically feature slower output response times as compared to peak and logarithmic detectors, due to the use of AGC.

2.5 Techniques for Radiometric Partial Discharge Measurement

Radiometric PD measurement has seen many developments over the past 20 years, due to the ease of installation and reconfiguration compared to alternative PD measurement techniques. Radiometric PD detection utilizes broadband radio receivers to detect and measure the electromagnetically radiated UHF signal propagated from a PD source [74–76]. Generally, multiple radiometric sensors, separated by a spacing of at least several meters, can be used to detect and locate a source of PD [77]. Radiometric PD detection allows for easy, non-intrusive installation, and is simple to reconfigure if required [75]. It provides an alternative that has several advantages over traditional PD measurement techniques since it does not require galvanic or physical contact with the item of plant under observation; therefore, a single radiometric sensor is capable of monitoring multiple items of HV equipment simultaneously.

Some wireless approaches for locating and monitoring PD utilize the received signal strength (RSS) of the electromagnetic energy propagated from a PD source, whilst more advanced techniques locate PD using the received time differences for a set of measurement sensors, such as time-of-arrival (TOA) and time-difference-of-arrival (TDOA). Each technique has advantages and limitations, in relation to cost, complexity, accuracy and efficiency.

2.5.1 Characteristics of Radiometric PD

As previously stated in Section 1.3, the charge displaced in an insulation fault results in an electromagnetic signal propagated away from the discharge source. Whilst the actual current discharged in the fault is a pulse with a fall time in the order of 1 to 1000 ns, the resulting radiometric signal bears similarities to a classical decaying oscillation [78], with a frequency range in the order of 50-3000 MHz [79]. The frequency of the radiometric signal is dependent on the resonant structure of the insulation defect, resulting in a narrow-band band-pass response [80]. The propagation environment effectively low-pas filters this frequency range to 50-800 MHz, with the majority of the frequency content residing below 300 MHz.

A variety of radio receivers are capable of detecting and measuring the transmitted PD signal; however, a difficulty of radiometric PD monitoring is susceptibility to any electromagnetic interference. This includes locally transmitted signals within the VHF and UHF bands, such as FM, private mobile radio, digital audio broadcasting (DAB) and digital TV. Figure 2-17 shows the typical spectrum of broadcast frequencies within the VHF and UHF bands.

FM occupies the 87.7-107.9 MHz band, whilst DAB is typically broadcast within 174-239.2 MHz. Digital TV is broadcast from 470-606 MHz and 614-790 MHz. 2G GSM is broadcast at 880-915 MHz and 925-960 MHz; however, this is out of the band of interest. There are also sources of interference transmitted locally, such as fluorescent lamp ignition [81], unlicensed portable radios, such as PMR446, and

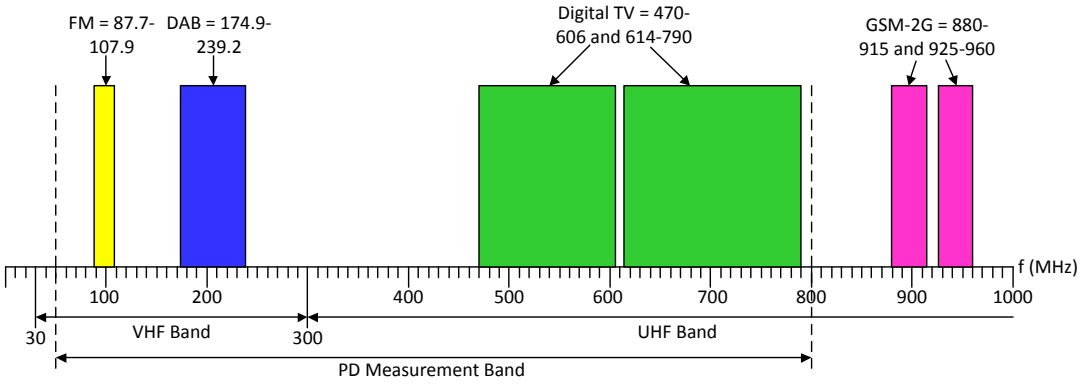


Figure 2-17: VHF/UHF Electromagnetic Spectrum with Typical Wide Range Transmission Signals

licensed portable and amateur radio. Fluorescent lamp ignitions should only be a possible issue in indoor environments, in which additional filtering may have to be employed to remove the interference if it is problematic.

Amateur radio, which is transmitted within bands of 50-52 MHz, 70-70.5 MHz, 144-146 MHz and 430-440 MHz [82], requires a license for broadcasting. They are also restricted to a maximum transmission power of 10 dBW, 17 dBW and 26 dBW for foundation, intermediate and full license types [83], corresponding to theoretical distances of 10 km, 22 km and 63 km respectively for a receiver sensitivity down to -40 dBm. However, in reality these distances would be reduced due to the complexity of the propagation path, and it is unlikely that most radio amateurs would transmit at the maximum power allowed. The radiation pattern of the antenna used will also decrease the likelihood of amateur transmission causing interference to radiometric PD detection.

License free PMR446 radio is broadcast in a narrow-band of 446.0-446.2 MHz, and has a maximum transmission power limit of -3 dBW [84], corresponding to a distance of approximately 2 km. Whilst it is unlikely that these transmissions outside of a radiometric PD monitoring area would be received, there is a possibility that personnel within, or visiting, a HV site may operate personal radios operating in this band. Such transmissions would not be a significant issue, since these types of transmissions would only be temporary, and could be easily discriminated from a source of PD. Interference of this type from outside of the monitoring area would also be easily discriminated when localization was applied, positioning it outside of the HV area.

Ensuring these locally transmitted signal do not interfere with the radiometric PD measurement requires some knowledge of the typical frequency content of various types of radiometric PD signals, such as those that propagate from insulation faults within transformers, switch-gear and transmission lines. Measured spectra for a variety of simulated defects has been presented in publications for purposes including propagation effects on UHF PD, antenna comparisons for reception, and similarities between galvanic and radiometric PD signals.

Data presented in [85] measures the frequency response of radiometric PD within gas-insulated switch-gear (GIS) using sulphur-hexaflouride (SF_6). The measurements were made using a biconical antenna and a log-periodic antenna, with bandwidths of 30-300 MHz and 80-1000 MHz respectively, at a distance

of 2 m from the source of PD. The reported spectra was between 30-820 MHz, with the majority of the energy from 30-75 MHz. In [86] radiometric PD spectra was measured for an air-blast circuit breaker, with a focus on the change in spectra due to the propagation environment. Three sensor positions were used, two of which were fixed at a distance of 12 m from the PD source, and one which was varied between 12 m and 18 m. The mean spectra measured at each position fluctuated by over 50 MHz between the three sensor positions; however, the majority of the frequency content was still between 50-400 MHz at each position.

In [87] and [88] a PD fault was emulated using a sandwich of transformer paper submerged in transformer oil. Five sheets were used in [87] in between two electrodes paper, whilst eleven sheets were used in [88] with the five inner most sheets pierced with a 1 mm hole to produce an air-filled void. The radiometric PD signal produced was then measured using four different antennas, a 5 cm and 10 cm monopole, a log-periodic and a zig-zag antenna. Cumulative power was measured with and without the PD source in bands of 0-300 MHz and 1300 to 1900 MHz, with the ratio of the two cumulative quantities provided; therefore, allowing for the difference in received power to be determined between background broadcast interference and PD within these bands, along with the power level in each band .

The reported results in [87] show that the majority of the received power is within the 0-300 MHz band, with the exception of the 5 cm monopole antenna, where the majority of received power was in the 1300-1900 MHz band. However, the

reason for this is that the lower bandwidth of such an antenna is restricted due to its physical size, since a monopole antenna should be half the wavelength of the received signal frequency [89].

The results shown in [88] divide the measured spectrum into 250 MHz bands for each antenna, from DC to 2.5 GHz, with the log-periodic taken as the absolute measurement due to its flat frequency response across the specified range. The antennas were placed at a distance of 45 cm from the PD source, with the exception of the log-periodic antenna, which was placed at a distance of 90 cm to ensure the antenna was in the far field. Approximately 75% of the received power was measured in the 0-250 MHz band, along with 17% in the 250-500 MHz band. The remaining energy was between 1.4% and 0.26% in each consecutive frequency band.

The spectra of three simulated PD faults within a HV transformer were measured in [90], an internal void PD fault, a surface PD fault and a insulator bushing PD fault. The internal PD fault was simulated with a dielectric oil-filled glass vessel placed inside a transformer tank which contained eleven layers of insulation, with a 1 mm hole perforated through the three inner most layers to produce an air-filled void. Two electrodes are connected to each side of the vessel to attach a HV source, the air was removed using a vacuum in order to ensure a lower permittivity within the void than in the insulating layers.

The surface PD fault was created using a twisted-pair of HV, resin polymide-imide

insulation, enameled wire placed within the tank, which has an additional layer of polyester trishydroxyethyl isoyanurate over the insulation. Finally, the bushing fault was generated using a porcelain bushing insulator whose surface was covered with a saline solution, which was allowed to dry in order to obtain a salt polluted surface to generate PD. The emulated PD faults were measured using two 10 cm monopole antennas, one placed inside the tank and one outside at a distance of 30 cm from the fault under test. The spectra was measured within three bands, a lower band of 0-300 MHz, a middle band of 300-1200 MHz, and an upper band of 1200-2500 MHz.

The cumulative power within each band was measured, with and without the PD fault, to determine the contribution of locally transmitted interfering transmissions. For the internal PD fault the percentage of power measured by the inner antenna were 0.3%, 94.3% and 5.4% for lower, middle and upper bands respectively, whilst the percentages were 61.9%, 35.8% and 2.1% in the lower, middle and upper bands for the outer antenna. For the surface PD fault the measured powers in each band were 0.1%, 99.1% and 0.8%, and 89.2%, 10.7% and 0.1%, in the lower, middle and upper bands for the inner and outer antennas respectively.

The cumulative energies for the bushing PD fault in the lower, middle and upper bands were 69.3%, 27.4% and 3.3% for the inner antenna, and 40.3%, 58.1% and 1.6% for the outer antenna. For the two internal fault types the majority of the cumulative power measured by the internal antenna was in the middle band, whilst

fir the external antenna the majority of power was in the lower band. The inverse of this is the case for the bushing fault, where the majority of the power was in the middle band. The reason for this was due to the transformer tank causing low-pass filtering to the radiometric signal. However, the higher frequency content of the measurements made where the tank was not an obstruction were closely coupled. A measurement made at a distance greater than 3 m would likely have incurred attenuation to the higher frequency content.

In [91] the spectra of an emulated HV floating electrode PD fault, which is a common fault in switch-gear [92], was obtained and compared using both galvanic and radiometric measurements. A floating electrode PD test cell was energized to 6.2 kV using a HV DC supply. The measured energy was divided into bands of 50-290 MHz, 290-470 MHz and 470-800 MHz. For the contact and radiometric measurements the percentages of energy in each band were 62.8% and 78.3% in the 50-290 MHz band, 0.76% and 4.33% in the 290-470 MHz band, and 0.56% and 1.59% in the 470-800 MHz band respectively, the remaining energy was below 50 MHz. In both cases, the majority of the measured energy was within the 50-290 MHz band.

In [93] and [3] spectra were taken for a further two emulated PD faults using galvanic and radiometric measurements. Both PD cells emulated defects within solid insulation. One consisted of an acrylic tube containing two electrodes at each end, between the electrodes a sandwich of three circular pieces of 1.5 mm thick FR4 insulation are placed, in which the middle piece has a 1 mm hole drilled in

the centre to create a higher electric field within it, and therefore, a discharge. The second consisted of a sandwich of three sheets of 2.4 mm thick epoxy glass dielectric between two electrodes, with a 1 mm diameter hole, again, drilled in the centre of the middle sheet.

The acrylic tube PD source was filled with transformer oil in order to suppress any discharges occurring at the edges of the electrodes. However, measurements were taken with and without the presence of oil. The acrylic tube emulator was energized to 20 kV AC, both with and without oil, to generate PD, whilst the epoxy glass dielectric emulator was energized to 18 kV AC. Even though the frequency response of the acrylic tube emulator was higher with the presence of oil, almost the entire energy is in the 50-800 MHz band for all three measurements of the two emulators, with the majority of the energy below 300 MHz.

2.5.2 Time Difference of Arrival PD Measurement

TOA and TDOA techniques, traditionally used for radio positioning systems, use the times that signals are received at specific receivers to determine the distance, using the speed of light to convert time to distance, of a transmitting signal from each receiver, and therefore, the location of the transmitting source [94]. TOA relies on the time at which the transmitted signal was sent along with the reception time for each receiver, whereas TDOA only requires the latter, and is therefore more versatile [95]. Figure 2-18 shows an example of TDOA positioning.

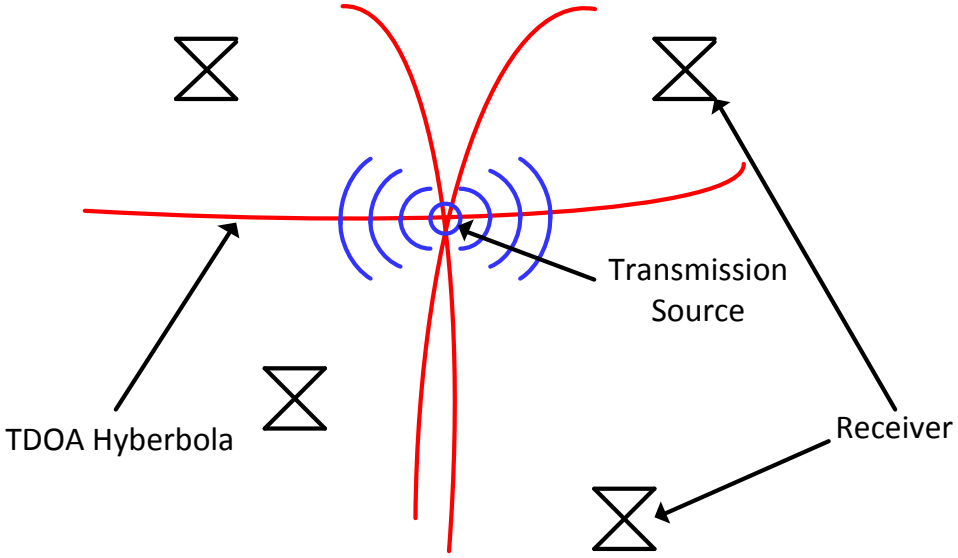


Figure 2-18: TDOA Location of a Wireless Transmission via Multilateration [95]

In this example, four receivers are positioned around a transmitting signal which is the target for location. The distance of the source from each receiver is calculated by determining the precise time difference of received signals between sensors. This is then converted to distance using the speed of light. The resulting distances are used to plot hyperbolic lines via non-linear regression, at which the intersecting point of the lines is the estimation for the transmission [96]. TDOA has been used in many schemes for PD location, and can provide accuracy within 5 cm [97].

TDOA techniques have been employed for the detection of PD using multiple techniques, such as cross-correlation, cumulative energy and the amplitude of the first received peak [98, 99], that is, by comparing received PD patterns, or by using the integral of the received signal or the amplitude of the first received peak.

TDOA location provides a high level of estimation accuracy, and has been used to successfully detect and locate sources of PD in live HV environments [100–104].

Although TDOA techniques provide an accurate and non-invasive solution to PD detection and location, there are various constraints that impact the feasibility of large-scale deployment using this technology. The sample-rate required to discern the differences has to be as high as possible, since the time between samples equates to the resolution in distance [105]. Since the transmitted signal is a radioemtric electromagnetic wave, the resolution in distance is proportional to the speed of light divided by the sample-rate. For example, a sample-rate of 1 GSa/s has a resolution distance of 30 cm, whereas a sample-rate of 5 GSa/s has a distance resolution of 6 cm [106]. Whilst techniques such as interpolation can be used to increase the distance resolution at reduced sample-rates [107, 108], rates in excess of 1 GSa/s are still necessary.

The requirement for high sample-rates makes this technology impractical for a large-scale battery powered WSN, since the power requirements of such a high-speed data processing system would not be capable of sustained operation from a single battery source over a reasonable period of time, and would also have considerable costs. Furthermore, the complexity of scaling a coherent TDOA system on a large-scale would be difficult, due to requirement for synchronization between nodes to accurately determine the time difference of signal reception.

2.5.3 Received Signal Strength PD Measurement

A simpler method to TOA and TDOA techniques is RSS only localization, which is based on the classical radiometric propagation model, given by Equation 2.

$$R_i = R_0 - 10n \log_{10} d_i \tag{2}$$

where R_r and R_0, n, and d_i are the ith sensor received power and source transmitted power in dBm, path-loss index, and distance from the source respectively. In free space n is typically 2 at short distances from the transmitting source. It increases to approximately 4 when ground reflections occur, and it increases further still if the propagation environment contains obstructions, or produces multi-path propagation.

The main benefit of an RSS-based system is the use of incoherent receivers, and therefore, no requirement for synchronization between nodes. This allows for a network that is far more flexible than coherent based detection, and can be easily scaled for a given monitoring area of HV plant [109]. This versatility comes at the cost of decreased accuracy compared to TOA and TDOA techniques, due to the complexity of the propagation environment [110]; however, this can be alleviated through calibration, by transmitting an artificial PD source of known strength from a single node within the WSN to each other node. The received signal at each node can then be adjusted to account for the propagation environment for

a given transmission path [111]. A further challenge is the limited signal-to-noise ratio (SNR), due to the use of incoherent detectors with a wide bandwidth, and therefore a limited dynamic range.

A typical technique used in some proposed implementations [112–114] is to measure the energy of the received PD signal, since experimental data has been reported that links the total RF energy propagated from a PD source to the apparent charge conducted across the void [115, 116], suggesting that the two quantities have a linear relationship; therefore, the integral of the received PD power may contain useful diagnostic information.

Methods of RSS PD localization have been proposed which directly sample the received PD signal [117–120]. Whilst these techniques eliminate the need for synchronization, they still employ sample-rates above 1 GSa/s. Although direct sampling of the received PD signal obtains detailed information of the PD signal, which allows for frequency analysis via fast-fourrier transform, along with pattern recognition and better noise immunity [119, 121], it still requires excessive power consumption.

To reduce the required sample-rate, various techniques have been proposed which utilize envelope detection to remove the VHF/UHF frequency components, thus leaving only the envelope of the received PD signal [122], allowing for sample-rates down to a minimum of approximately 20 MSa/s at a reduced measurement

accuracy. Data published in [123] states an error of 0.54 % at a sample-rate of 100 MSa/s, with 20 samples per pulse for a 200 ns radiometric PD signal, compared to a sample-rate of 10 GSa/s and 20,000 samples per pulse. This accuracy drops to 8.68 % at 10 MSa/s, with only 2 samples per pulse. Whilst this does not seem a significant error, due to the stochastic nature of the PD, it is likely that in some cases only 1 sample will be obtained for a received signal; therefore, reducing the accuracy of the measurement.

A technique utilizing envelope detection, along with basic frequency measurement, was proposed in [124] and [112]. The proposed system, shown in Figure 2-19 used three parallel filtered channels to obtain basic spectra of the received PD signal.

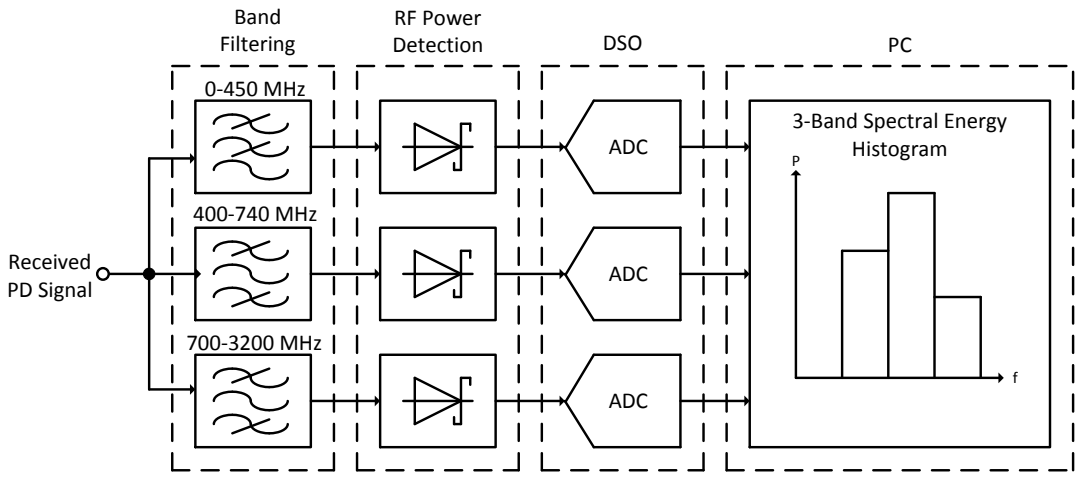


Figure 2-19: A Frequency-based RF PD Sensor [112]

The received RF signal is applied to 3 separate parallel filters, a 450 MHz cutoff low-pass filter, and 400-750 MHz and 700-3200 MHz band-pass filters. The filtered

signals are each applied to a Schottky diode power detector with bandwidths of 5 MHz, which remove the UHF components from the received PD signal. The detected signals are then sampled at a rate of 1 GSa/s by a DSO. The sampled data is then processed via a PC to calculate the energy of received PD signals in each frequency band. This is then used to plot a histogram of the received pulses for a given energy band.

Whilst this system is only a prototype, it is limited for large-scale use due to various factors. The 1 GSa/s sample-rate would make the cost per sensor too high for a WSN to be a viable option for PD monitoring. Along with this, three ADCs are required to digitize each frequency band, increasing the cost and power consumption 3 fold. ADCs with a sample-rate at least a factor of ten lower could be used to reduce this limitation. However, the data processing requirements would still require significant power consumption to perform, particularly if the sampled data was transmitted back to the central HUB before any processing was performed. Furthermore, the parallel connection of the RF front-end would result in the received signal power being split between each channel due to the 50 Ω matching, reducing the signal strength, and therefore, the sensitivity of the sensor.

A single channel sensor using envelope detection was proposed in [109], shown in Figure 2-20, which utilizes the internal ADC of a micro-controller unit (MCU) to digitize the received PD.

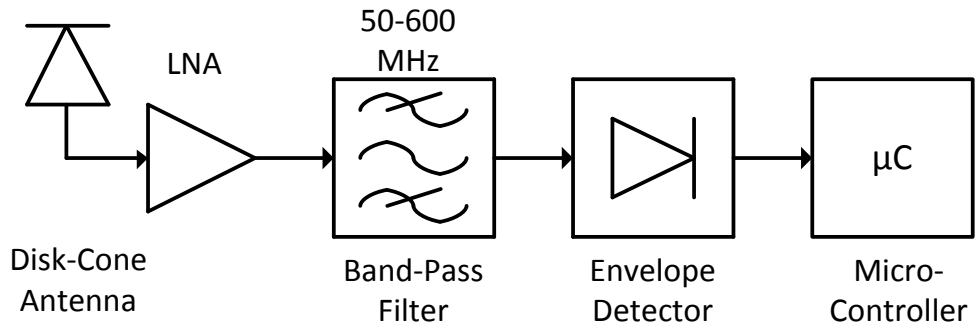


Figure 2-20: Single Channel PD Sensor from [109]

The sensor is composed of a wide-band receiving disk-cone antenna, low-noise amplifier (LNA), band-pass filter, envelope detector and MCU. The disk-cone antenna is used to receive the radiometric PD signal. This is applied to an LNA to provide some amplification, increasing the sensitivity of the sensor. The amplified signal is band-limited to a bandwidth of 50-600 MHz via the band-pass filter, before being applied to the envelope detector, which removes the high frequency content from the PD signal. The envelope of the received PD is then sampled by the internal ADC of the MCU.

This arrangement alleviates the requirement for high-speed sampling, and thus, provides a low-power technique for radiometric PD monitoring. The envelope detector is a square responding device; therefore, each sample acquired by the MCU ADC is proportional to the power at a given point of the envelope of the received PD signal. The MCU can therefore process these samples to obtain the total received energy of the envelope. A disadvantage to this technique is the

low sampling-rate of the ADC, which decreases the accuracy of the measured PD signal, as well as no way to discern between received PD and other interfering signals.

Further developments were made to the previous sensor, which were proposed in [125]. The sensor, shown in Figure 2-21, is designed around the single channel version with the addition of calibration circuitry and a communications module for transmission of received data.

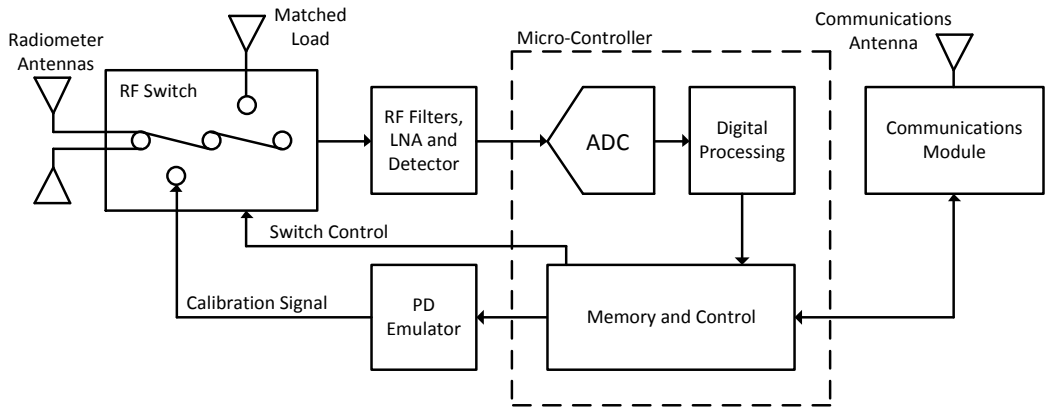


Figure 2-21: Advanced Single Channel PD Sensor from [125]

The receiving radiometer antenna is, again, a disk-cone type. Here, the radiometer antenna is connected to an RF switch, which configures the sensor as a receiver or transmitter. The signal processing section is nearly identical to that of Figure 2-20, with the exception that a logarithmic detector is used in place of the square-law detector; therefore, providing higher sensor sensitivity and dynamic range. The main addition is the PD emulation circuitry, which is activated by the micro-controller in order to transmit a known PD-like signal to the other

sensor nodes within the WSN. This allows for the propagation environment to be calibrated between nodes, increasing the accuracy of the radiometric localization. A further modification is the addition of a Zigbee communications module to transmit received data to a data collection point.

Low power techniques using an active peak-hold detector is proposed in [126]. This technique removes the requirement for multiple samples per pulse by capturing and holding the maximum peak of the received PD signal, Figure 2-22 shows the proposed system.

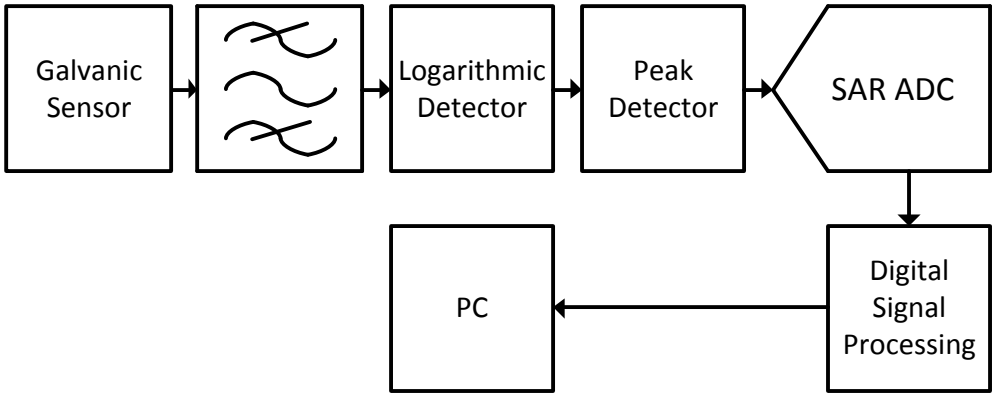


Figure 2-22: Peak Detector-based PD Signal Processing

Whilst this technique is described for galvanic measurement of PD, it has potential for use in radiometric-based PD sensor. The sensor output is band-limited via the band-pass filter, the output of which is applied to a logarithmic detector. The logarithmic detector compresses the received signal, effectively increasing the dynamic measurement range. The output of the detector is then applied

to an active peak detector, which captures and holds the maximum voltage of the detector output. This is then sampled by a 12-bit SAR ADC, which is internal to an ADuC814 data acquisition IC. Some digital signal processing is then applied to the digitized signal, and the result is transmitted to a PC via RS232.

The benefit of this technique is that only a single sample is required per received PD event, drastically reducing the required sample-rate, and therefore, power consumption and cost. A difficulty is that high-speed active peak hold circuits, capable of capturing peaks of less than 10 ns associated with radiometric PD signals, are difficult to implement. This is due in part to the requirement for rectifying diodes, which add non-linearity to the dynamic range of the detector. Further difficulties are caused by the requirement for high-speed field effect transistor (FET) input components, to ensure fast response and minimal hold droop, increasing the power consumption of the circuit. Furthermore, whilst the peak power of the received signal can be used for localization, it does not have a direct relationship to the apparent charge in the PD source [114]; therefore, diagnostic analysis using this technique is difficult.

2.6 Conclusion

This chapter has outlined the techniques for acquisition of short duration analogue pulses, along with the advantages and limitations of each technique. The basic operation of relevant ADCs was discussed, with the suitability for analogue pulse

acquisition, and in particular radiometric PD, assessed. The type and functionality of typical RF envelope tracking detectors were described and evaluated. The typical frequency spectra for various radiometric PD faults were detailed, along with the frequency spectrum of locally transmitted signal that would likely be detected within the range of radiometric PD. Finally, techniques for radiometric partial discharge measurement were presented and discussed, with a focus on the suitability for their deployment in a large-scale PD monitoring WSN. The main points taken from this literature review are as follows:

- Whilst undersampling acquisition allows for a lower power ADC to be used, the lower sample-rate limits the accuracy of the measurement. Conversely, oversampling provides a high level of measurement accuracy, but is limited by the requirement for higher power consumption.

- The SAR ADC architecture is capable of sampling almost instantaneously on command. However, it is limited to sample-rates below 10 MSa/s due to the clock-per-bit operation of the ADC.

- The flash ADC features a fast conversion time, but an adequate resolution for PD acquisition would require a level of complexity unsuitable for low-power operation due to the power consumption required. Furthermore, the increased input capacitance would hinder high-speed operation.

- The pipelined ADC solves the complexity issues of the flash, but still requires power consumption that is beyond what is ideal for long term sensor operation from a single battery source.

- The folding ADC architecture provides a simple bit-per-stage conversion process. However, previous implemented ADCs using this technique require high power consumption due to the high propagation speed required for each series connected folding stage in order to achieve high speed.

- Schottky diode based RF power detectors can provide an accurate measurement of received power, at no or low power consumption, and can track the fast envelope of a received PD signal. However, their dynamic range is limited due to the requirement for them to operate in the square-law region of the diode.

- Logarithmic and RMS-responding power detectors have high dynamic ranges, typically greater that 70 dB, and have sensitivities typically below -50 dBm. This comes at the cost of increased circuit complexity, and therefore, increased power consumption. Furthermore, they are limited by a response time in the range of hundreds of nanoseconds to microseconds.

- Various reported measurements have shown that the typical frequency spectra of many radiometric PD faults is within the 50-800 MHz band. Within this band are various transmitted signals that may cause interference to radiometric PD measurement.

- TOA and TDOA radiometric PD detection provides a high level of location accuracy, yet due to the requirement for high-speed sampling, in excess of 1 GSa/s,and the requirement for synchronization between sensors, it is not suitable for large-scale monitoring of HV plant.

- RSS PD measurement techniques can alleviate the dependence on excessive conversion rates when used in conjunction with envelope detection. Furthermore, implementation of a large-scale WSN utilizing this technique is simpler, since incoherent sensors can be used. However, existing sensors using RSS still require sample-rates beyond 10 MSa/s.

The next chapter will present an overview of the proposed radiometric PD sensors, suitable for low power operation within a large-scale WSN. The design of which has been developed with focus on the above points.

3 Proposed Wireless PD Measurement Systems

This chapter details the design and operation of the proposed signal processing circuitry for wireless PD processing, as well as an overview of the sensor nodes and the large-scale WSN for PD monitoring and measurement. The two techniques detailed rely on both analogue and digital processing; however, one type of processing is predominant in each of the proposed techniques, the first being based around a TRI to remove the requirement for high-speed sampling, and the second being based around a high-converter that only consumes significant power when a signal is present.

3.1 Wireless PD Sensor Network Overview

The PD monitoring WSN, shown in Figure 3-1 is composed of sensor nodes which communicates via a central HUB using wirelessHART. The sensor nodes are arranged in a grid array, spaced approximately 20 to 30 m apart. WirelessHART may transmit data via intermediate nodes to the central HUB in order to ensure no data is lost by using the shortest transmission path available, and therefore, minimizing the possibility of a transmitted signal being below the receiver range of the central HUB due to attenuation over a long distance. The electromagnetically radiated PD signal is received by sensor nodes in the immediate vicinity of the source. The nodes measure the power of the PD with relation to the simple propagation model given by Equation 2. The average power measured at each sensor node is transmitted to the central HUB, where an RSS-based location

algorithm can be used to estimate to location of the PD source, by triangulating the source based on the average power strengths received at each node.

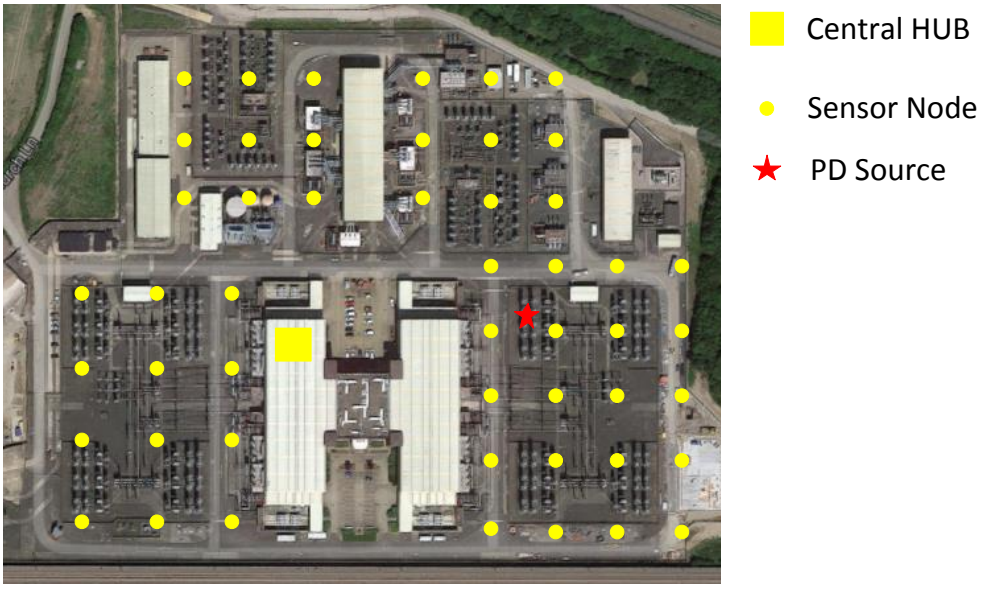


Figure 3-1: Conceptual PD WSN Layout [127]

The WSN should be easy to install, along with being as low power as possible; therefore, it must operate over a significant amount of time from a battery source without modification. The sensor nodes should also be portable, so they can be easily arranged within the monitoring environment. The sensor nodes have been developed with these requirements in mind. However, the nodes need to be capable of processing and measuring PD signals down to a range of at least -30 dBm, whilst also providing immunity to interfering broadcast signal; therefore, an front end RF section is included to provide pre-amplification and filtering, shown in Figure 3-2.

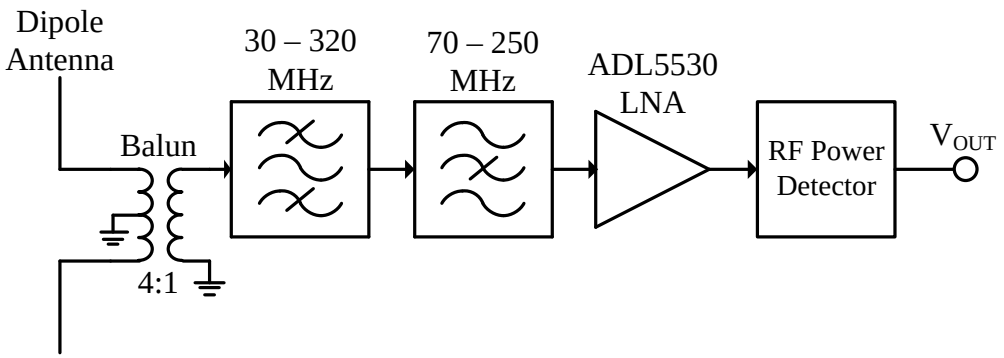


Figure 3-2: RF Front-End Electronics

The radiometric PD signal is received via a dipole antenna, connected via a 4:1 balun to provide a wider antenna bandwidth by providing a closer impedance match to the following section over a broader band. A dipole antenna is used as an omni-directional response is required. The signal is then applied to the filters and LNA. The band-pass filter removes interference and noise outside the 30-320 MHz band of measurement interest. The band-stop filter removes FM, DAB and digital TV signals in the region of 70-250 MHz, the LNA then provides a fixed gain of 16.5 dB. The resulting transfer function results in two pass-bands from 30-75 MHz and from 250-330 MHz, with a gain between 11.7-14.4 dB in the mid-band, and a measured noise figure between 5-7 dB [128]. The frequency response of the RF front-end is shown in Figure 3-3.

The output signal from the RF electronics is applied to an RF envelope detector, which removes the frequency components and produces an output voltage proportional to the linear or logarithmic power of the received PD signal envelope,

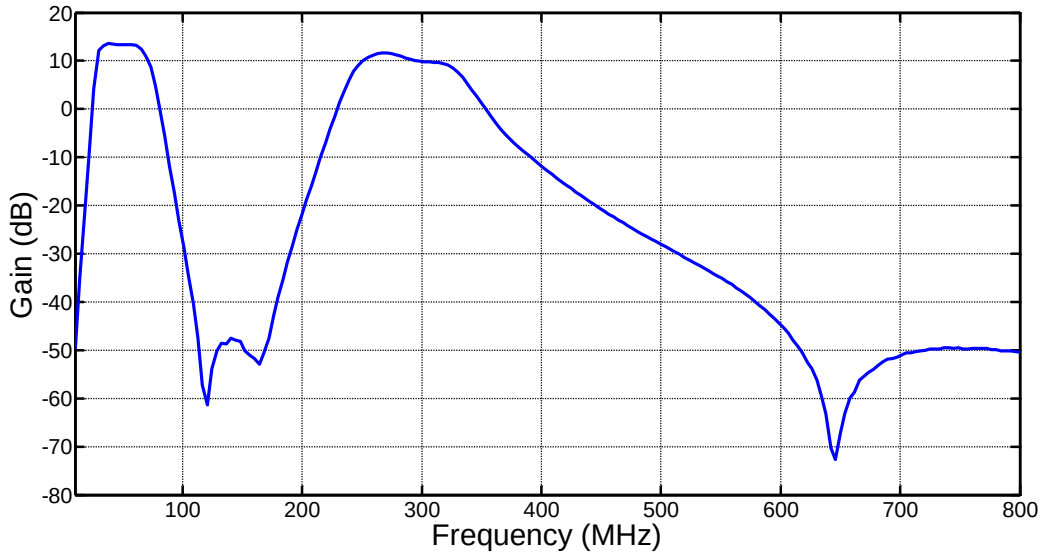


Figure 3-3: RF front-end frequency response

depending on the type of detector used. Figure 3-4 shows the structure of the sensor nodes.

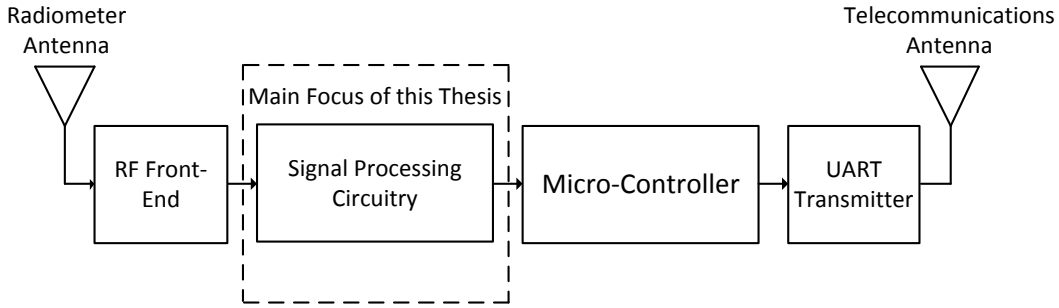


Figure 3-4: Wireless PD Sensor Node Block Diagram

The envelope detected PD signal is applied to one of the proposed signal processing sections, which are the main focus of this thesis and are detailed in the following sections. The output of the signal processing section is inputted into an MCU,

which calculates the energy of the received radiometric PD signal, and provides a count of the total number of PD events received over a predefined measurement period. The average of the received energy is then calculated by the MCU, and the mean received energy and count are transmitted back to the central HUB via a wirelessHART transmitter. Since only two values are transmitted per measurement period, the requirement for data processing and memory are kept to a minimum, and therefore, power consumption is reduced.

3.2 Transistor-Reset Integrator

The first technique, shown in 3-5, utilizes a TRI to reduce the envelope detected signal to a DC voltage level, avoiding the requirement for high data conversion rates [129].

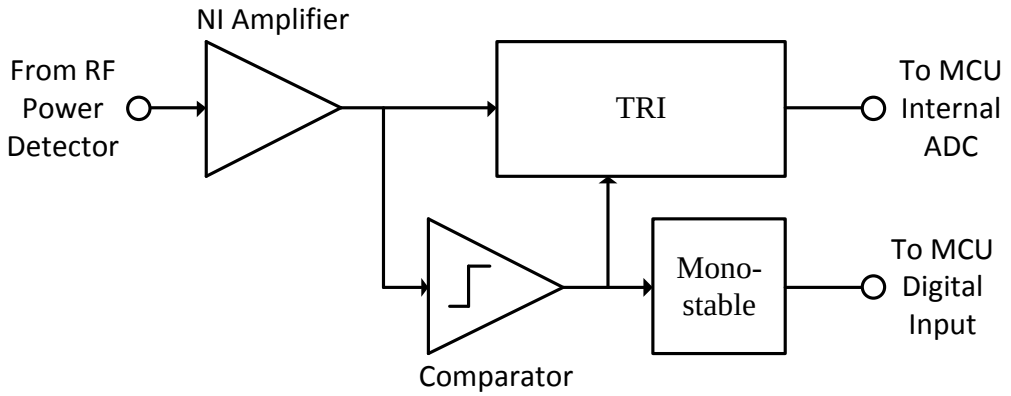


Figure 3-5: TRI Signal Processing Section

The envelope detected PD signal is amplified by a high speed non-inverting (NI)

amplifier to increase the amplitude of the signal, ensuring that the full supply range is used. The output of the NI amplifier is then applied to a high-speed comparator and the TRI. The high-speed comparator activates the TRI when the NI amplifier output is above the comparator threshold level. The comparator also activates a mono-stable circuit, which provides a pulse to the MCU to acknowledge that a PD pulse has been received, triggering sampling. The MCU also uses the mono-stable for a count of the received PD events.

The envelope detected signal is integrated by the TRI to a DC voltage level. Once the NI amplifier output drops below the threshold level the TRI is deactivated and its output is held at the current level until another pulse is received. Since the TRI output is a DC level it requires only one sample per received pulse, drastically reducing the sample-rate required. This sampling is done by the internal 10-bit SAR ADC of the MCU, since it has adequate resolution and can be triggered when required with minimal delay. When the TRI output level reaches the supply rail voltage it is reset back to 0 V to ensure it does not saturate to the supply rail.

A Schottky-diode based square law RF power detector is used for the TRI based system. Since the output of such a detector is proportional to the instantaneous power of the received signal, the resulting output voltage of the TRI is therefore proportional to the energy of the received signal, and these values can be directly inputted into a linear power-based RSS location algorithm.

3.3 High Speed Folding ADC Based System

The second technique relies on high-speed sampling of the received PD signal. This method, shown in Figure 3-6, utilizes an ADC that has been designed to only consume significant power, above 100 mW, when a PD signal is present, with the digital clock circuitry only active during the acquisition of a received pulse, thereby reducing power due to transient switching currents in the digital section [55].

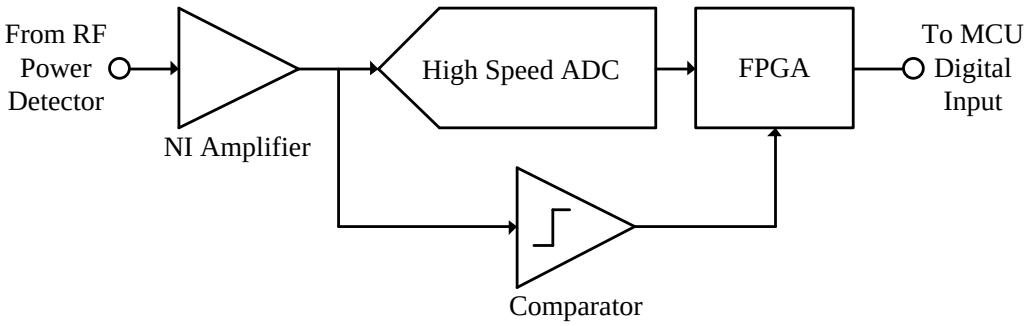


Figure 3-6: High Speed Sampling Based System

A logarithmic power detector is used for this signal processing system to increase the dynamic range and sensitivity of the sensor. The detected signal is amplified by an NI amplifier to increase the signal to the full input range of the ADC. The amplified signal is then sampled by the high-speed folding ADC, where acquisition is triggered by a high-speed low-power comparator. The logarithmic detector alleviates the requirement for the comparator threshold to be set as near as possible to 0 V, since the detector effectively compresses the dynamic range at the input making a small input change large at the detector output. Therefore, the comparator threshold voltage is set far above the noise floor. This is illustrated in

Figure 3-7.

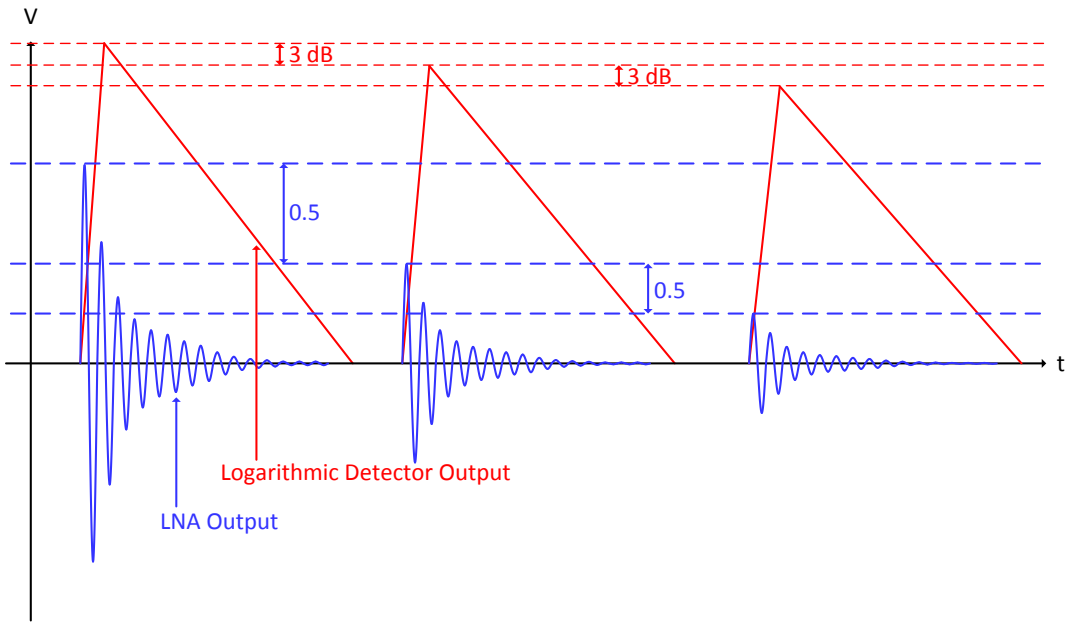


Figure 3-7: Logarithmic Detector Compression of the LNA Output

As shown by Figure 3-7, reducing the LNA output by one half would result in a decrease of 3 dB to the detector output. Another reduction of a half to the LNA output decreases the detector output by a further 3 dB. Typically, the slope of a logarithmic detector is between 25-50 mV/dB for a device with a wide dynamic range; therefore, whilst the LNA output, and therefore the received PD signal, are reduced by a total of 0.25, the detector output only decreases by a total of 150-300 mV due to the logarithmic response. A further point that can be observed from Figure 3-7 is the logarithmic response of the detector alters the shape of the received PD envelope, from an exponentially decay to a linear decay.

When the comparator threshold is reached a logic high signal is outputted to the FPGA, which then begins to clock the folding ADC with a complementary dual non-overlapping 25 MHz signal. The FPGA also increments a 'count' variable for the number of received pulses when the comparator outputs a logic high. The acquired samples are transferred to the MCU once acquisition is complete, where they are converted from logarithmic power in dBm to linear power in mW. The samples are then summed to gain the integral of the received PD event. Each received event is then averaged using the 'count' variable to gain the mean of the received radiometric PD energy. The count and mean energy values are then transmitted to the central HUB via the WirelessHART node once the predefined measurement period is over.

3.4 Conclusion

This chapter presented a system level overview of the proposed radiometric PD signal processing techniques. The basic function of each section of the two main techniques presented were defined, and the fundamental operation was discussed. The main principles of each techniques are as follows:

1. The first signal processing system is based around a TRI which features:
    - a precision op-amp based integrator to reduce the detected signal to a DC voltage level, which requires only one sample per received PD signal in order to measure the signal.
    - a self-resetting transistor-based feedback system, which automatically

resets the integrator when its output reaches a predetermined threshold level; therefore, no monitoring is required from the MCU to determine when a reset is required.

- an output that is proportional to the energy of the received PD signal since the RF detector output is proportional to the power in the envelope of the PD event. The energy may provide some diagnostic information and can be directly inputted to an RSS based location algorithm.

2. The second signal processing system is based around a high-speed folding ADC which:

   - only samples when a received PD signal is present; therefore, reducing the power consumption of the system by the limiting the transient switching currents used when sampling.
   - utilizes a high-speed logarithmic detector for an increased dynamic range and sensitivity.
   - converts the logarithmic power to linear values via the MCU to allow for a lower processing rate, and therefore, a reduced power consumption.

The following chapter will present the circuit implementations of the two proposed signal processing techniques for low-power radiometric PD measurement.

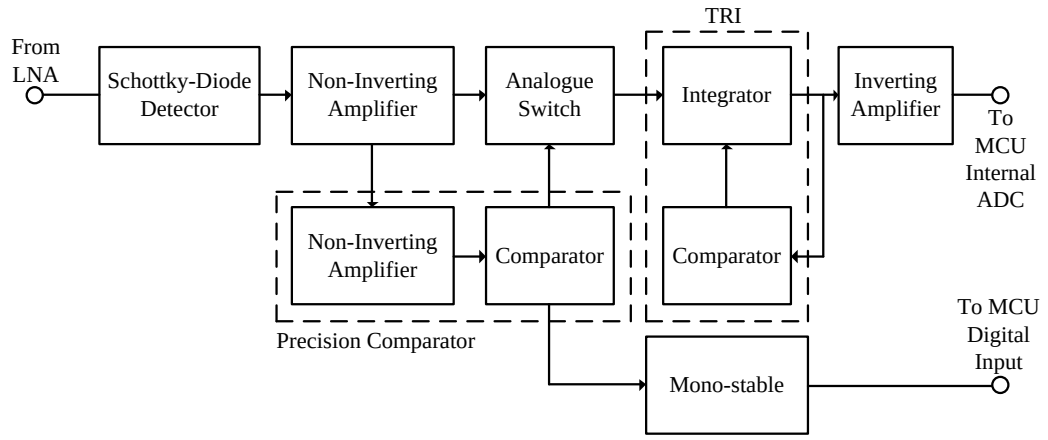
4 Circuit Implementation of the Signal processing Techniques

This chapter details the circuit design and implementation of the TRI and high-speed folding ADC based systems described in Chapter 3. Each circuit section is described in detail, along with circuit analysis and critical justifications for the designs implemented. Two versions of the TRI were developed, one based around a 17 MHz bandwidth precision FET input op-amp and one based around a composite amplifier design, in which multiple amplifiers are used to create a circuit with higher performance than any single op-amp based amplifier is capable of. The precision op-amp type will be referred to as the standard TRI, whilst the composite type will be referred to as the composite TRI. The power supply circuitry for each system can be found in Appendix C

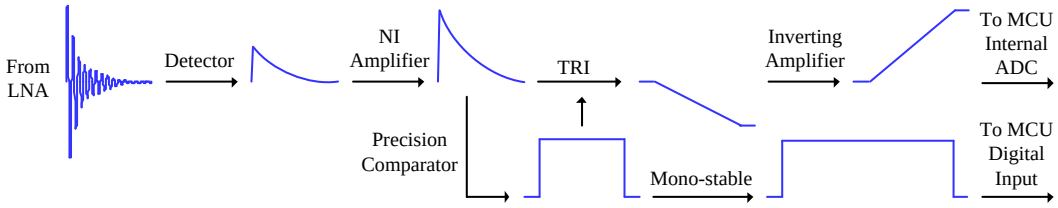
4.1 Transistor-Reset Integrator Circuit Design

A detailed block diagram of the TRI is shown in Figure 4-1. The circuit is an expansion of that shown in Figure 3-5, and shows the additional sections of the circuit, primarily the precision comparator and the TRI.

The output signal from the LNA is applied to an RF envelope square law detector, which removes the high frequency components and produces an output voltage proportional to the instantaneous input power. The detected signal is then amplified



(a)



(b)

Figure 4-1: TRI, (a) Block Diagram, and (b) Signals

by a high-speed NI amplifier to increase the amplitude of the signal to span the supply rail, which is then applied to the precision comparator and the TRI. The precision comparator is composed of a NI amplifier and a high-speed comparator, the NI amplifier increases the signal in order for the comparator threshold to be set to a voltage that is at least 40 mV the noise floor, therefore ensuring that no oscillation occurs at the output of the comparator due to false triggering.

When the output of the NI amplifier exceeds the threshold level the comparator triggers high, activating the analogue switch and producing a pulse at the output

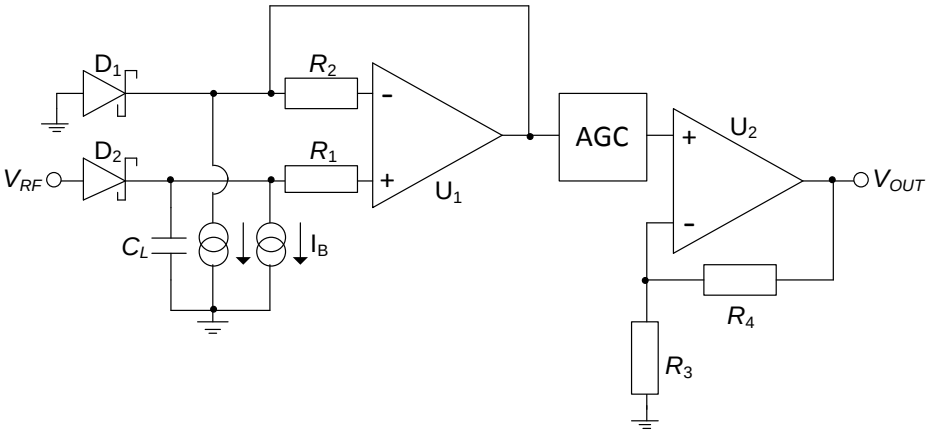
of the mono-stable circuit for a pulse count. The analogue switch activates the TRI which integrates the received PD signal to a DC level. The TRI comprises a precision inverting integrator, a transistor and a comparator. Each received PD signal causes a DC step change to the output of the integrator, proportional to the integral of the instantaneous power of the received pulse. Once the output voltage of the integrator reaches a predetermined level the TRI comparator resets the TRI and the process is then repeated. The output of the TRI is then applied to an inverting amplifier to obtain a positive signal which is then sampled by the internal SAR ADC of the MCU.

The standard and composite TRI implementations are detailed in the following sections.

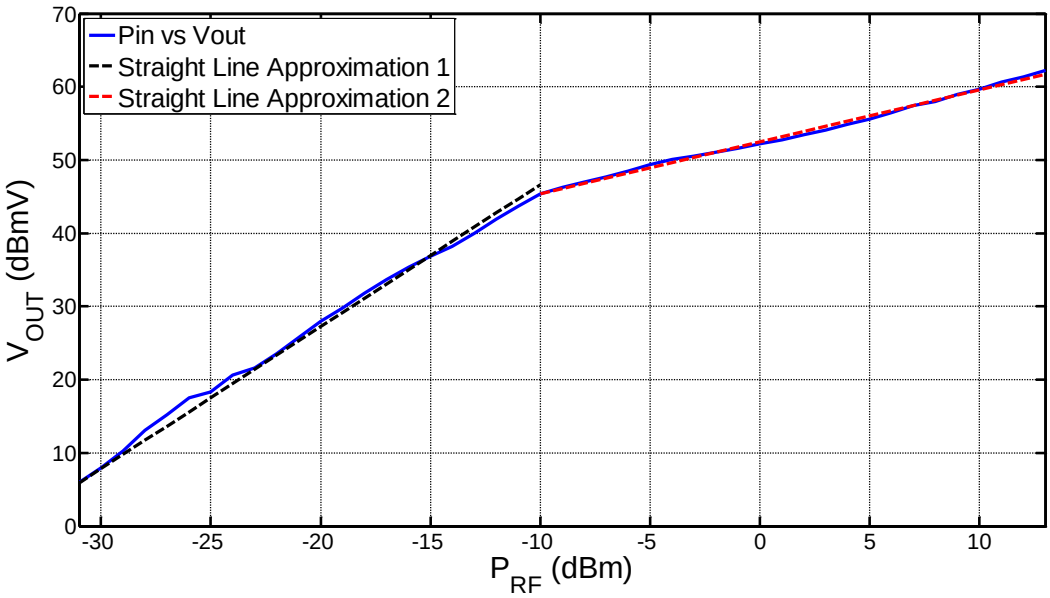
4.1.1 Standard TRI

The standard TRI design is based around precision and high-speed CMOS and FET input op-amps. The detector used is an LTC5507 temperature compensated active schottky diode detector, similar to that shown in Figure 2-14. Figure 4-2 shows the simplified circuit diagram of the LTC5507 along with the transfer curve of the detector.

Op-amp U_1 is setup as a temperature compensated active Schottky diode detector. The output of the detector is applied to a non-inverting amplifier, through an AGC circuit. The AGC circuit effectively adds gain compression depending on the size



(a)



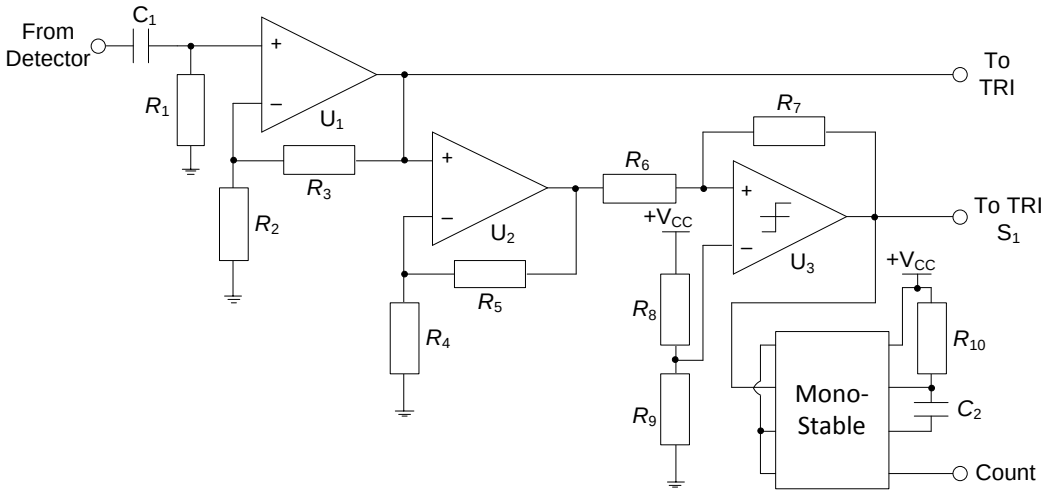
(b)

Figure 4-2: LTC5507 Active Schottky Diode Detector, (a) Simplified Circuit Diagram, and (b) Transfer Curve

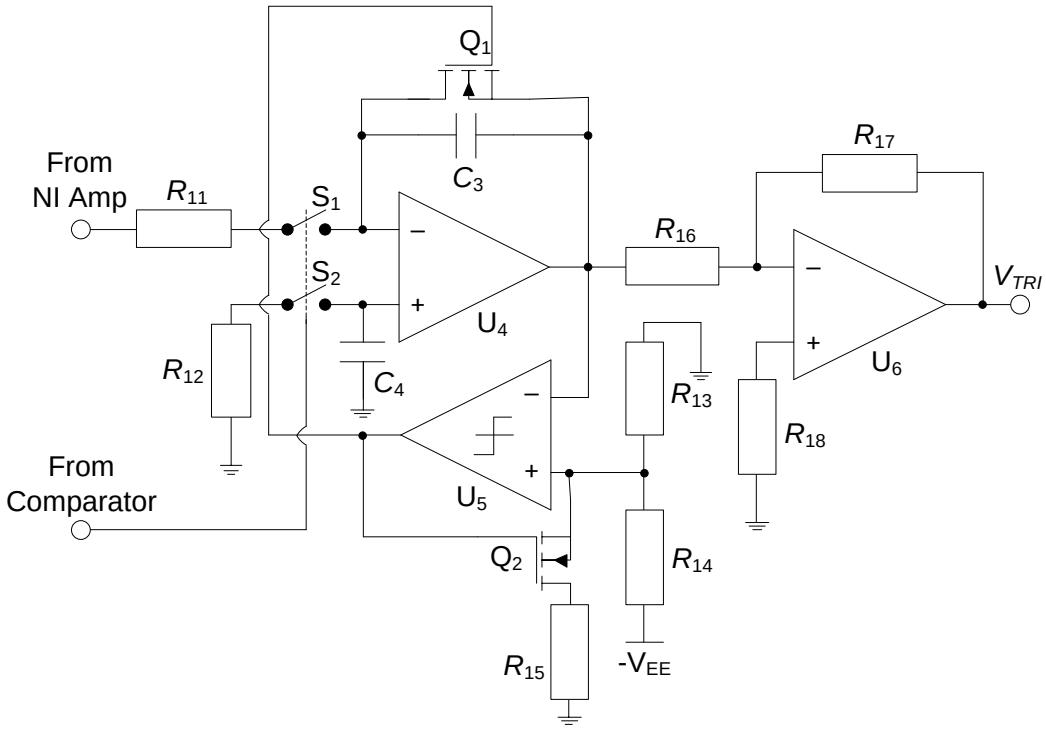
of the input signal [130]. The gain is set to 4 for input voltages below 60 mV, and to 0.75 for input voltages above 140 mV; therefore, the dynamic range of the detector is increased. This can be seen from the transfer curve shown in Figure 4-3b. Below an input -10 dBm the gain of the detector sets the transfer to a slope of 934.6 mV/mW. Beyond -10 dBm the slope is drastically reduced to 51.1 mV/mW. This gives the detector an extended range of -30 dBm to +14 dBm. The output of the LTC5507 is then applied to the standard TRI, shown in Figure 4-3 [127] (component values are given in Table B-1 in Appendix B).

The output of the power detector is AC-coupled through high-pass filter C_1 and R_1, and then applied to gain of three amplifier U_1. The amplified signal is then applied to both the precision comparator, composed of NI amplifier U_2 and high-speed comparator U_3, and the precision TRI, integrator U_4 and comparator U_5. U_4 is an 18 MHz bandwidth FET input op-amp with a typical DC offset error of 7 μV, ensuring minimal drift to the output of the TRI between received events.

The TRI is switched between two modes, integration and hold, via switches S_1 and S_2. The high-speed precision comparator, which is set to a threshold level of 4 mV, controls these modes. When a signal above approximately 1.3 mV is at the output of the detector the comparator drives the TRI into integration mode by actuating S_1. S_2, which should be closely matched to S_1 if a dual SPST analogue switch is used, is also actuated to compensate for the charge injection of S_1 onto the feedback capacitor [131]. Signals below the comparator threshold, such as noise at



(a)



(b)

Figure 4-3: Standard TRI Circuit Diagram, (a) NI Amplifier, Precision Comparator and Mono-stable, and (b) TRI and Inverting Amplifier

the detector output, do not cause any change to the output of the TRI. The ideal transfer function of the integrator is given by Equation 3.

$$V_{TRI} = \frac{1}{R_{11}C_3}\int_0^t V_{IN}\mathrm{d}t \tag{3}$$

In practice, various parasitic parameters introduce errors to the integrator output. Primarily, the open loop gain, bandwidth and input impedance. The input impedance can be ignored since the integrator op-amp features a JFET input, and therefore, a high input impedance. The finite open-loop gain and bandwidth errors can be derived in the frequency domain, given by Equation 4. Replacing $j\omega$ for s, and simplifying assuming that $A_{OL} >> 1$, yields Equation 5.

$$\frac{V_{TRI}}{V_{IN}} = \frac{-1}{j\omega R_{11}C_3}\left(\frac{1}{1+\left(\frac{1+\frac{\omega}{\omega_C}}{A_{OL}}\right)\left(1+\frac{1}{j\omega R_{11}C_3}\right)}\right) \tag{4}$$

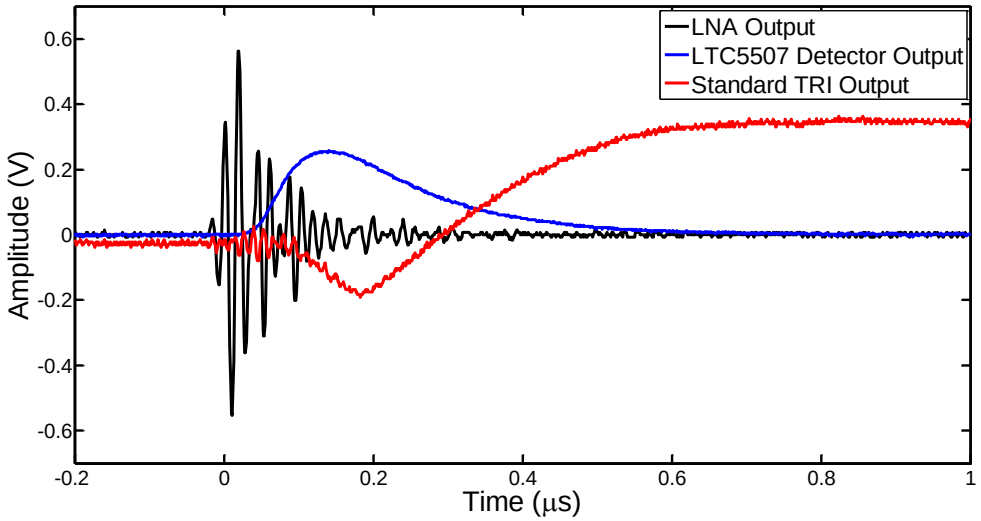
$$\frac{V_{TRI}}{V_{IN}} = \frac{-1}{sR_{11}C_3}\left(\frac{1}{1+\frac{s}{A_{OL}\omega_C}+\frac{1}{A_{OL}sR_{11}C_3}}\right) \tag{5}$$

where ω_C and A_{OL} are the -3 dB open-loop gain cutoff frequency and the DC open-loop gain respectively. A logic high 'count' signal is also sent to the MCU via the mono-stable, activated by the comparator, providing a total count of received PD events. The mono-stable is set to a time of 5 μs to ensure enough time for the

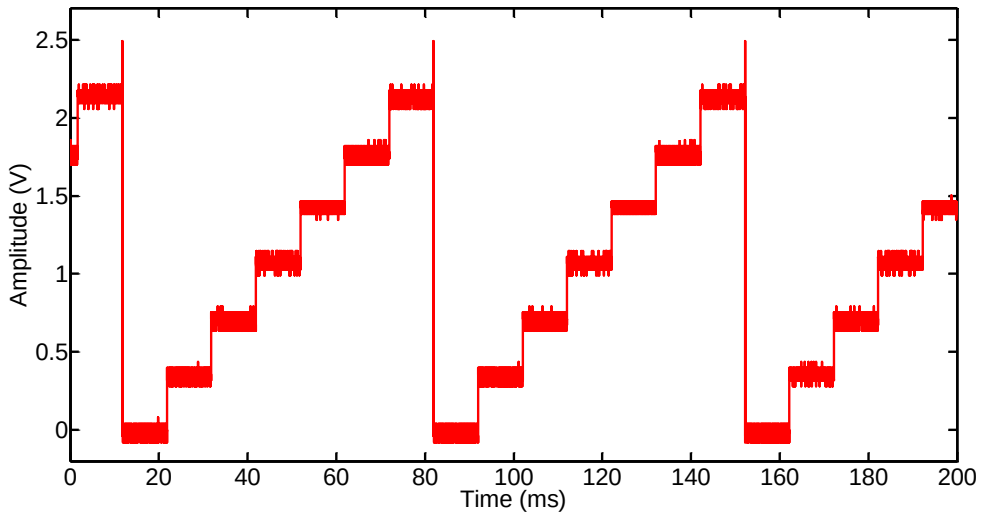
MCU to acknowledge the signal. The amplified detector output is integrated onto the TRI feedback capacitor, C_3, via R_4, setting the TRI time-constant to 1 μs. Once the detector output drops below the threshold the comparator switches the TRI back to hold mode, holding the TRI output at a constant level until the next received event.

The reset function of the TRI is performed via comparator U_5, and transistors Q_1 and Q_2. When the output of U_3 drops below -1.5 V the output of U_5 is driven positive, activating Q_1, which discharges feedback capacitor C_3 resetting the TRI, and Q_2 which adjusts the threshold voltage of U_5 to approximately 0 V, ensuring C_2 is fully discharged and the TRI is reset to zero. The gain of two inverting amplifier, U_6, inverts the negative going output signal of the TRI to a positive voltage and scales it to the 3 V power supply range, ensuring that the full resolution of the ADC is utilized. Figure 4-4a shows the detector and TRI outputs for a single emulated PD event, whilst Figure 4-4b shows the TRI output for multiple PD events produced by a PD calibrator set to a repetition rate of 10 ms.

The TRI reduces the envelope detected signal to a DC level, and therefore, a staircase signal at the output of the TRI for multiple received PD events. Each step at the output of the TRI is sampled by the internal SAR ADC of the MCU when a 'count' signal is received from the mono-stable. The integral of each received PD pulse is then determined by taking the difference of current and previous samples, and the samples are averaged by the MCU, before transmission back to the central



(a)



(b)

Figure 4-4: (a) LNA, LTC5507 Detector and Standard TRI Outputs for a Single Received PD Event, and (b) Standard TRI Output for Multiple Received PD Events

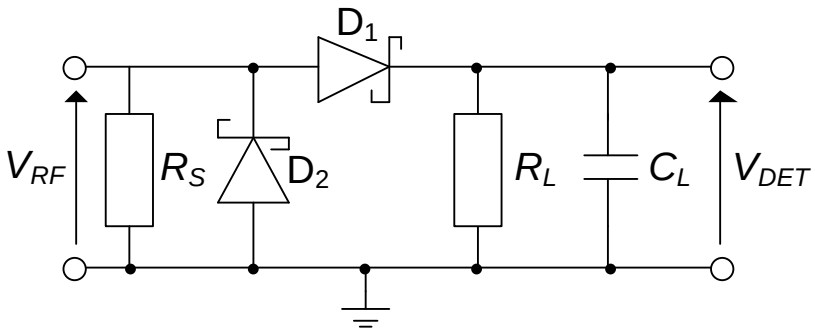
HUB via the wirelessHART mote.

4.1.2 Composite TRI

A second implementation of the TRI was developed to improve speed and precision, and reduce power consumption as compared to that of the standard TRI [132]. The implementation was designed utilizing composite amplifier techniques, in which multiple amplifiers are used to obtain enhanced performance beyond the capabilities of any single commercial op-amp [133, 134]. The circuit was based on the system level design shown in Figure 4-1. The detector used for the composite TRI, shown in Figure 4-5a (component values are given in Table B-2 in Appendix B), is a discrete voltage doubler zero bias detector [135], which uses an additional detector diode to increase the output voltage, and therefore sensitivity, of the detector.

The zero-bias Schottky diode detector is used as the time-constant can be set to closely follow the true envelope of the received PD signal; therefore, reducing any error caused due to inadequate bandwidth, rendering the detector incapable of tracking the true envelope of the received PD signal. The circuit diagram of the composite NI amplifier is shown in Figure 4-6 (component values are given in Table B-3 in Appendix B).

The circuit is a composite amplifier built around a discrete high speed JFET and a high speed bipolar op-amp, whilst maintaining DC precision over temperature by incorporating a very low offset amplifier for DC stability. This is important to ensure



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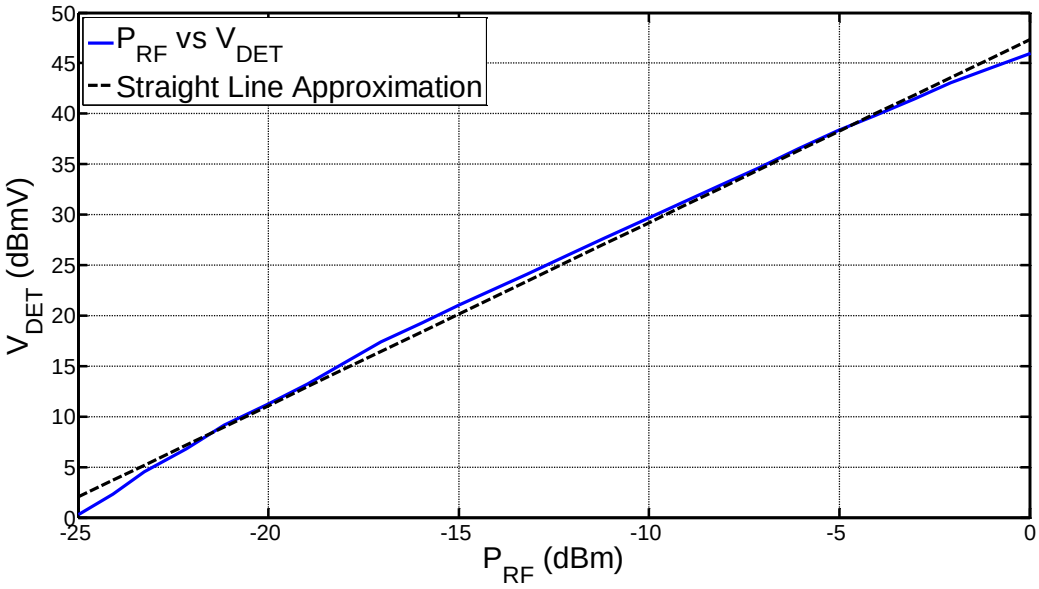


(b)

Figure 4-5: HSMS-2850 Schottky Diode Zero-bias detector [132], (a) Circuit Diagram, and (b) Transfer Curve

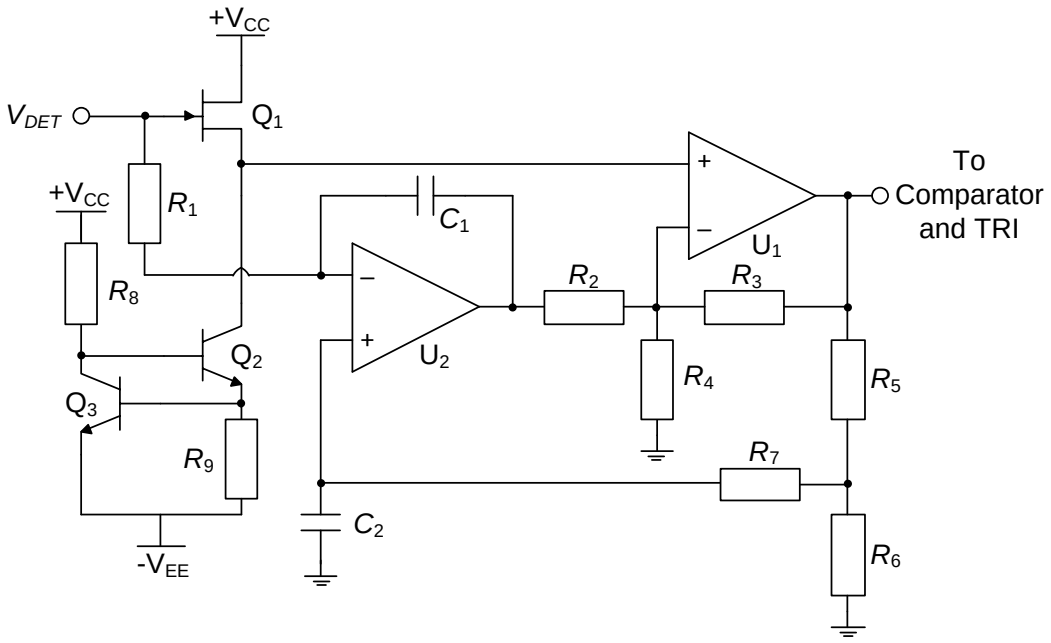


Figure 4-6: Composite Non-Inverting Amplifier [132]

correct operation as the sensor nodes will operate in an out door environment where temperature can range from -10 to +40 C. The detector output signal is applied to a discrete FET source follower buffer, biased at 0.5 mA via the V_{BE} current source composed of Q_2, Q_3, R_8 and R_9 [136]. U_1, R_3 and R_4 form a standard NI amplifier using a high speed low power bipolar type op amp, where the transfer function is given by Equation 6, which includes errors for the FET soure follower attenuation and the op-amp finite open-loop gain.

$$A_V = \Big(\frac{g_m R_{OCS}}{1 + g_m R_{OCS}}\Big)\Big(1 + \frac{R_3}{R_4}\Big)\Bigg(\frac{1}{1 + (\frac{1+\frac{\omega}{\omega_C}}{A_{OL1}})(1 + \frac{R_3}{R_4})}\Bigg) \tag{6}$$

where g_m and R_{OCS} are the trans-conductance of FET Q_1 and the V_{BE} current

source output resistance respectively, and ω, ω_c and A_{OL1} are the input frequency, gain -3 dB point and U_1 open loop gain respectively. R_5 and R_6 form a replica of the NI amplifier feedback network, which is monitored by the DC stabilization integrator, U_2, R_2 and C_2, through low-pass filter R_7 and C_3, which has a time constant of 330 ms. The DC voltage at the replica network is compared to the DC input voltage of amplifier U_1 and the output of U_2 adjusts the feedback network DC level to ensure the DC output voltage is close to the DC input voltage, with the offset error only contributed by U_2 multiplied by the gain of the NI amplifier. A low power auto-zeroing amplifier is used for the DC stabilizing amplifier, with an offset of 5 µV max, and a drift of 0.05 μV/°C. The mathematical expression for the DC stabilization is given by Equation 7.

$$V_{ADJ(NI)} = \left(\frac{R_4}{R_2 + R_4}\right) \frac{1}{RC} \int_0^t \left(V_O \left(\frac{R_6}{R_5 + R_6}\right) - V_{DET}\right) \mathrm{d}t \qquad (7)$$

where $V_{ADJ(NI)}$ is the DC voltage at the summing node of U_1 which is adjusted by the DC stabilization to minimize the offset error to that of U_2, multiplied by the gain of U_1, and V_O is the output voltage of U_1. The finite open-loop gain error term is not included in Equation 7 since the time-constant is so low that the open-loop gain of U_2 will be near its DC value, which is approximately 130 dB; therefore, the error due to finite open-loop gain will be negligible. V_{ADJ} is mainly dominated by the V_{GS} of Q_1, with the actual DC offset voltage of U_1 causing only a slight change in V_{ADJ} due to the large values of C_1 and C_2.

The precision comparator, shown in Figure 4-7 (component values are given in Table B-4 in Appendix B), is composed of a high speed NI amplifier and a high speed comparator. A high speed low power bipolar type op-amp is again used for the non-inverting amplifier, the comparator is also a high speed low power device.

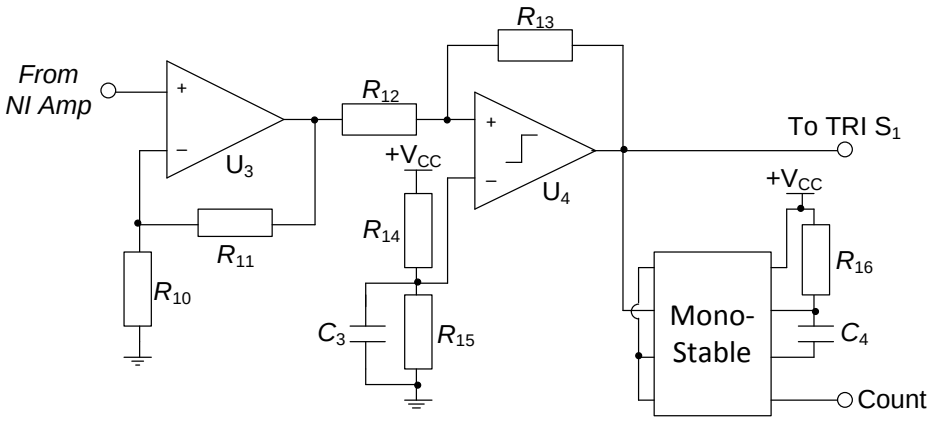


Figure 4-7: Precision Comparator and Mono-stable Circuit [132]

The high speed NI amplifier is a standard design, set to a gain of 11. The Comparator is set in a non-inverting configuration, with 35 mV of hysteresis added through R_{12} and R_{13}. The threshold voltage, set by voltage divider R_{14} and R_{15}, is 96.77 mV. The trigger high and low levels are therefore 98.5 mV and 59 mV respectively. DC drift is not an issue since the trigger levels are set to a level that is beyond the maximum offset of the devices and components. The NI amplifier allows for the comparator threshold to be set to a voltage way above the noise floor of the system, since setting the threshold to a low level would result in false

triggering on the output of the comparator.

The TRI, shown in Figure 4-8 (component values are given in Table B-5 in Appendix B), is designed again using composite techniques. The TRI requires a precision high-speed low-power integrator, which places high demands on the requirements for a single op-amp.

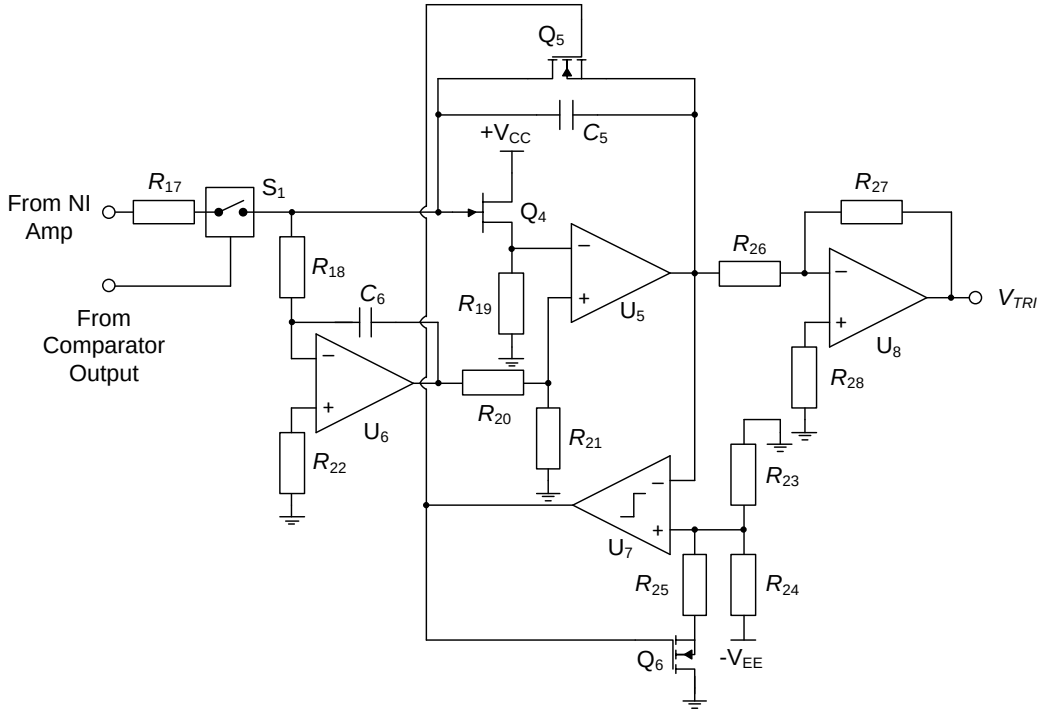


Figure 4-8: Composite TRI Circuit Diagram [132]

The precision integrator utilizes an 80 MHz 0.9 mA quiescent current bipolar op-amp, U_5, with the inverting input driven by a source follower connected N-type JFET, Q_4, providing a high input impedance. Normally this type of arrangement would require a large offset voltage to be set manually at the non-inverting input of

U_5 due to the bias voltage required for Q_4 to operate in the linear region; however, this is compensated for by the DC stabilizing amplifier, Q_6. The DC stabilization performs two functions, it ensures that the DC offset voltage of the integrator is kept to that of U_6 and it automatically forces Q_4 in to the required self-biased operating region. This is done by monitoring the summing point through a 330 ms time-constant, set by R_{18} and C_6, and comparing it to ground. The output of U_6 then adjusts the non-inverting input of U_5 through voltage divider, R_{20} and R_{21}, until the summing point is at zero, plus the minor DC offset of U_6. R_{22} compensates for the very minor offset voltage caused by the bias current of U_6 across R_{18}. The mathematical expression for the DC stabilization is given by Equation 8.

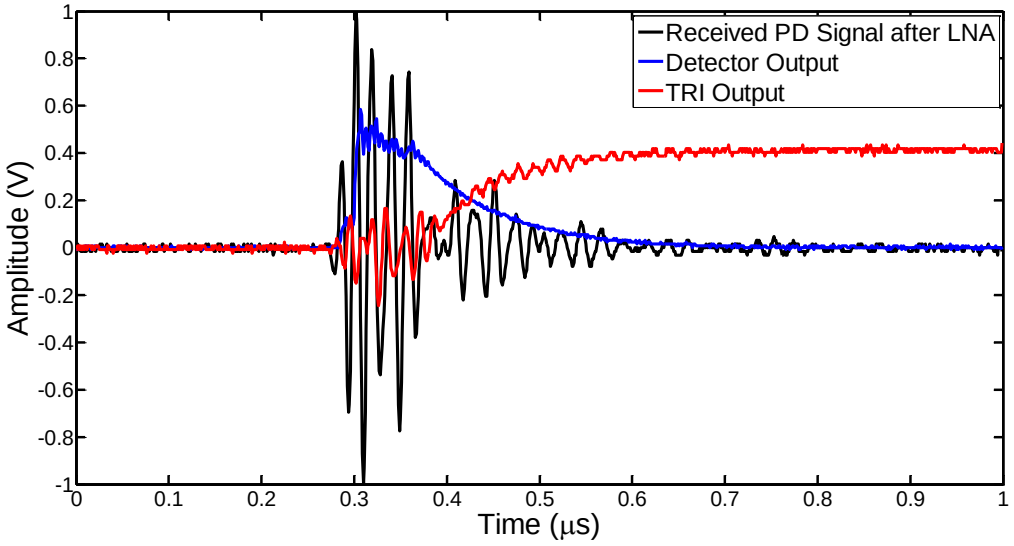
$$V_{ADJ(TRI)} = -\frac{R_{21}}{R_{18}C_6\left(R_{20}+R21\right)}\int_0^t V_{SN}\mathrm{d}t \tag{8}$$

where $V_{ADJ(TRI)}$ is the non-inverting input of U_5, and V_{SN} is the summing node of the composite integrator. Again, the finite open-loop gain of U_6 is not included since the time-constant is so close to DC, and therefore, any error is negligible. The feedback capacitor, C_5, and reset transistor, Q_5, are fed back from the output of the op-amp to the gate of Q_4, closing the feedback loop around the integrator. When a signal is received the precision comparator activates analogue switch S_1, the output of Figure 4-6 is then integrated to a DC level due to the charge accumulated on C_5. The integrator is reset by comparator U_7, with a threshold set at half the voltage range of the negative supply. Once the output voltage of the integrator reaches this level the comparator activates, turning on transistors Q_5 and Q_6. Q_5 discharges

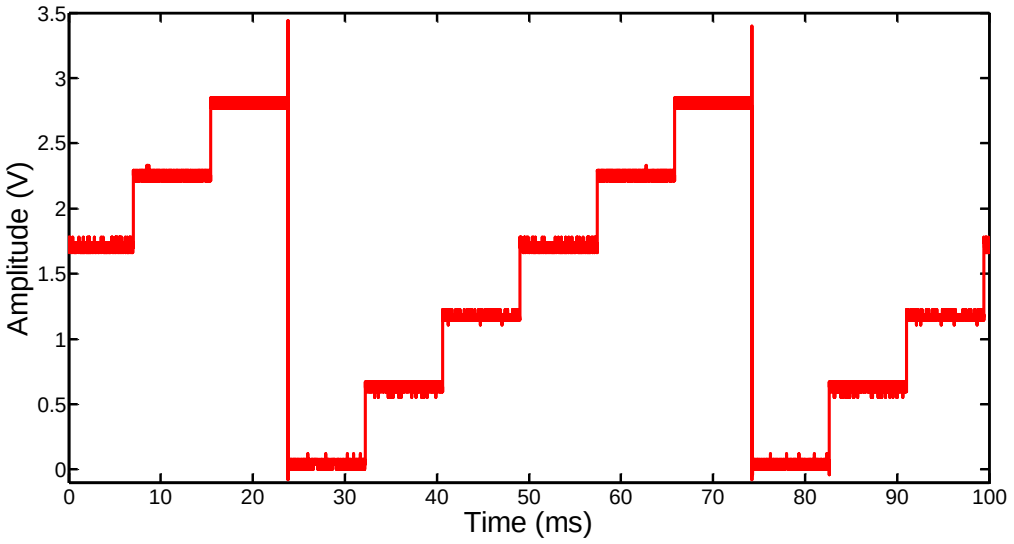
feedback capacitor C_5, whilst Q_6 adjusts the comparator threshold voltage to near zero, to ensure that the feedback capacitor is fully discharged, and the integrator is completely reset. The transfer function of the composite TRI is given by Equation 9.

$$\frac{V_{TRI}}{V_{IN}} = \frac{-1}{j\omega R_{18} C_5} \left(\frac{1}{1 + \left(\frac{1+\frac{\omega}{\omega_c}}{A_{OL}} \right) \left(\frac{1+gm_4 R_{19}}{gm_4 R_{19}} \right) \left(1 + \frac{1}{j\omega R_{18} C_5} \right)} \right) \tag{9}$$

where gm_4 is the trans-conductance of Q_4. Equation 9 is identical to Equation 4 with the addition of a decrease in op-loop gain, caused by the attenuation through the common-drain connected JFET input. The output of the integrator is then applied to the inverting amplifier, composed of U_8, R_{26}, R_{27} and R_{28}, which inverts the signal to a positive going voltage and amplifies it by a factor of two to the full supply range. Figure 4-9a shows a received radiometric PD signal at the output of the LNA, the zero-bias detector output and the composite TRI output, whilst Figure 4-9b shows the composite TRI output for multiple received emulated PD events.



(a)



(b)

Figure 4-9: (a) Composite TRI Output for A Single PD Event, and (b) Composite TRI Output for Multiple PD Events [132]

4.2 Folding ADC Design

The folding ADC based PD sensor node, shown in Figure 4-10, contains a logarithmic detector, a 159 Hz high-pass filter, a high-speed non-inverting amplifier, a high-speed comparator, an 8-bit folding ADC and a field programmable gate array (FPGA).

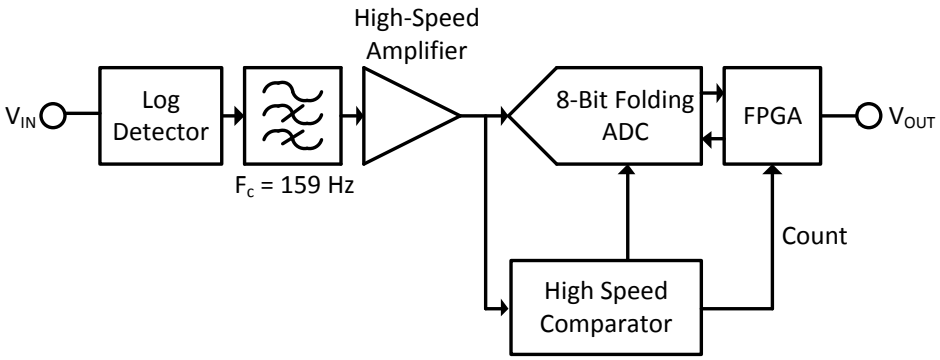


Figure 4-10: Folding ADC based PD Sensor Block Diagram

The received signal is applied to the logarithmic detector, which removes the high frequency components of the signal, leaving only the envelope, and produces an output voltage proportional to the input power in dBm. The chosen detector is capable of tracking the envelope of the received PD signal, has a sensitivity of approximately -75 dBm, a dynamic range of approximately 95 dB, and a bandwidth that extends from DC to 440 MHz.

The output of the detector is AC-coupled through the high-pass filter, which has a -3 dB cut-off frequency far below the pulse bandwidth, to remove the DC offset of the detector and ensure the ADC power consumption is minimized when no pulse is present. The signal is then scaled to the input range of the ADC via the

high-speed amplifier, which also provides a high input impedance so no loading is caused by the ADC input to the detector output.

The signal is then applied to the ADC and high-speed comparator. The comparator outputs a logic high signal which triggers the FPGA to initiate ADC sampling, and thus acquisition of the received signal. An internal mono-stable circuit within the FPGA controls the sampling duration once a received pulse is detected, this duration is set to 1 μs to ensure long received events are fully acquired. Inside the FPGA an internal synchronized mono-stable is also triggered, which ensures that the entire received PD pulse is acquired, and that any oscillation or instability to the output of the comparator does not affect the acquisition. Any additional samples that are taken after the received PD event have very little effect on the measurement of the pulse as they are near the noise floor and are equivalent to less than micro-Watts in power.

The proposed folding ADC, shown in Figure 4-11, is composed of a front end sample and hold amplifier (SHA), one sample and hold folding amplifier (SHFA) per bit, a complimentary non-overlapping clock, and data alignment and Gray code to Binary conversion logic.

The applied input signal is sampled by the front end SHA which passes the sampled signal to the first SHFA, which is clocked by the complement to the front end SHA clock. Each subsequent SHFA is clocked by the previous stages compliment;

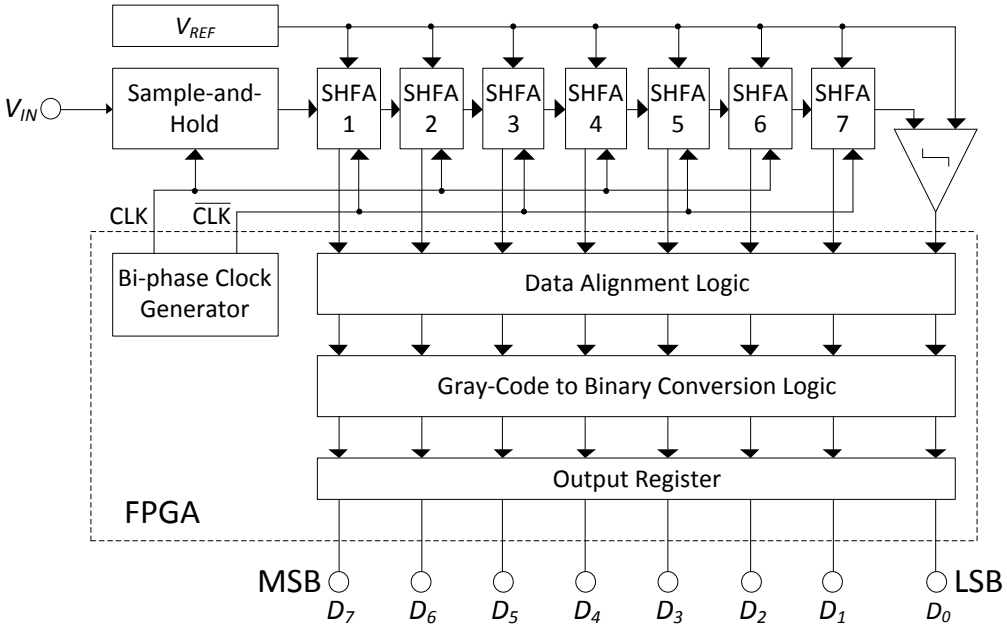


Figure 4-11: Folding ADC system diagram

therefore,the sampled signal is propagated through the SHFAs in a similar fashion to a bucket brigade.The SHFAs comparator output provide an offset Gray-coded output which is applied to the alignment logic, realigning each data bit into a corrected word. The realigned Gray code is then applied to the Gray code to binary conversion logic to provide each binary output word.

The front end SHA, shown in Figure 4-12 (component values are given in Table B-6 in Appendix B), uses an inverting architecture to reduce the constraints on common-mode performance for the amplifiers. U_1 is a simple unity gain inverting amplifier with the output offset by half the input range, 1.5 V. U_2 is an inverting SHA with an identical DC bias point to that of U_1, utilising a differential switching arrangement to compensate for charge injection from the switches,

as well as reducing the droop rate by ensuring the hold capacitor discharge is only dependent on the input offset current of U_2 and not the input bias current [137].

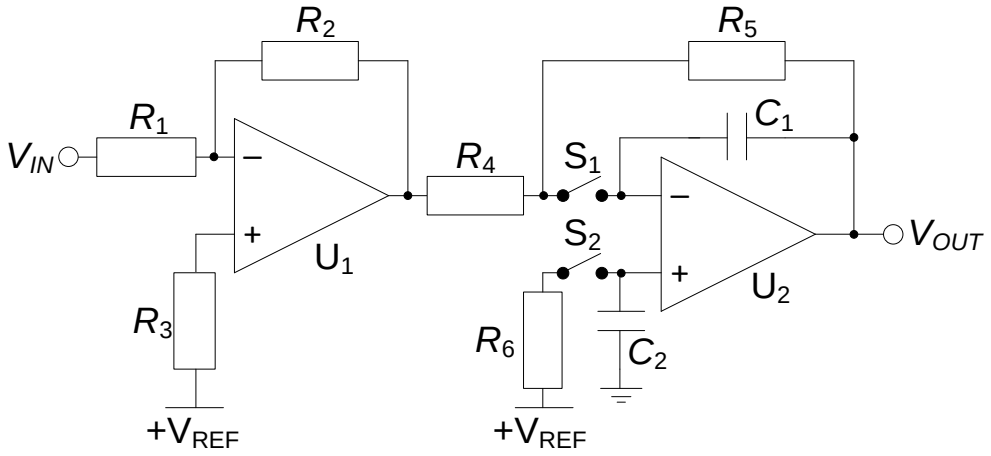


Figure 4-12: High Speed Sample-and-Hold Folding Amplifier Circuit

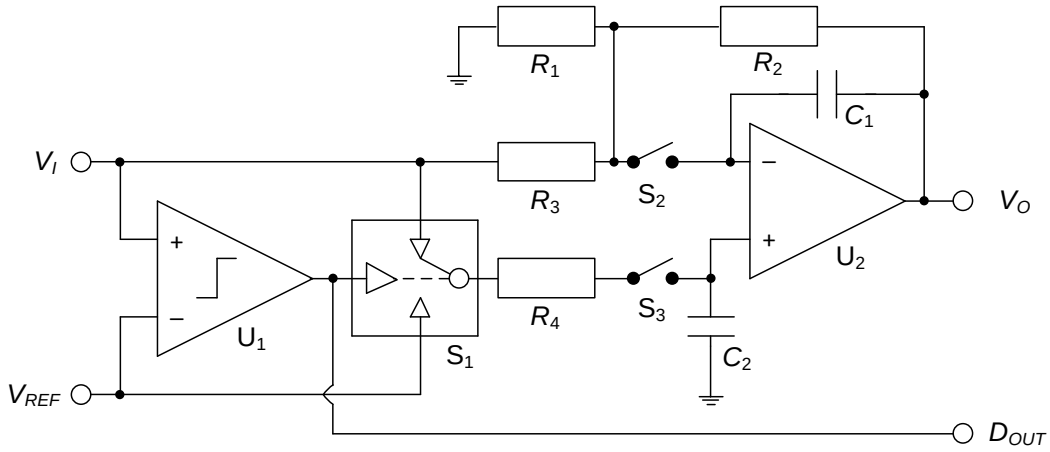


Figure 4-13: High Speed Sample-and-Hold Folding Amplifier Circuit

The SHFA, shown in Figure 4-13 (component values are given in Table B-7 in Appendix B), comprises comparator U_1 and op-amp U_2. The op-amp is

switched between non-inverting and offset-inverting modes by switch S_1. The sample-and-hold operation is performed by switches S_2 and S_3, and capacitors C_1 and C_2. U_2 is again configured in a differential arrangement in order to compensate for charge injection from the sample-and-hold switches, and the op-amp input bias current, this also ensures that sample-and-hold operation is performed in either mode. The circuit operates as follows, for input voltages from zero to V_{REF}, set at half the input range, the comparator outputs a logic low and the circuit is configured as a non-inverting amplifier. Only an insignificant current flows though R_3 in this arrangement. When the input voltage exceeds V_{REF} the comparator output is driven to a logic high level, activating S_1 and re-configuring the op-amp to an offset inverting amplifier. The non-inverting and offset inverting amplifier ideal transfer functions are shown in Equation 10. R_4 reduces the voltage offset caused by the input bias current of op-amp U_2 when it is configured in offset inverting mode.

$$V_{OUT} = \begin{cases} \left(1 + \frac{R_2}{R_1}\right) V_{IN} & \text{if } V_{IN} \leq V_{REF} \\ \left(1 + \frac{R_2}{R_1}\right) V_{REF} - \frac{R_2}{R_3}(V_{IN} - V_{REF}) & \text{if } V_{IN} > V_{REF} \end{cases} \tag{10}$$

For $R_1 = R_2 = 1/2R3$ 10 becomes 11

$$V_{OUT} = \begin{cases} 2V_{IN} & \text{if } V_{IN} \leq V_{REF} \\ 2(2V_{REF} - V_{IN}) & \text{if } V_{IN} > V_{REF} \end{cases} \tag{11}$$

In practice numerous parasitic elements reduce the gain from the ideal transfer function given by Equation 11. These include component tolerance, voltage offsets, and finite op-amp open-loop gain and bandwidth, along with the low-pass filtering caused by hold capacitors, C_1 and C_2. Including the finite open-loop gain, bandwidth and hold capacitors in the transfer function produces Equation 12, where Equations13 and 14 are the non-inverting and offset inverting errors due to finite open-loop gain respectively, given by Equations 13 and 14.

$$V_{OUT} = \begin{cases} V_{IN}\left(1 + \dfrac{R_2}{(1+j\omega R_2 C_1)R_1}\right)\varepsilon_{NI} & \text{if } V_{IN} \leq V_{REF} \\ \left(\begin{array}{c} V_{REF}\left(1 + \dfrac{R_2}{(1+j\omega R_2 C_1)R_1}\right) \\ -\dfrac{R_2}{(1+j\omega R_2 C_1)R_3}(V_{IN} - V_{REF}) \end{array}\right)\varepsilon_{OI} & \text{if } V_{IN} > V_{REF} \end{cases} \tag{12}$$

$$\varepsilon_{NI} = \frac{1}{(1+j\omega R_4 C_2)\left(1 + \dfrac{1+\frac{\omega}{\omega_C}}{A_{OL}}\left(1 + \dfrac{R_2}{(1+j\omega R_2 C_1)R_1}\right)\right)} \tag{13}$$

$$\varepsilon_{NI} = \frac{1}{(1+j\omega R_2 C_1)\left(1 + \dfrac{1+\frac{\omega}{\omega_C}}{A_{OL}}\left(1 + \dfrac{R_1R_2+R_2R_3}{(1+j\omega R_2 C_1)R_1R_3}\right)\right)} \tag{14}$$

where ω and ω_C are the input frequency and -3 dB frequency of the op-amp open loop gain in rads/s, and A_{OL} is the open-loop gain at at frequencies below ω_C. It is clear from Equation 12 that hold capacitors C_1 and C_2 form poles in the transfer

functions in conjunction with the gain setting resistors R_2 and R_4; therefore, the values of these components are set as low as possible to ensure the -3 dB bandwidth is way beyond the sampling frequency of the ADC.

4.3 Conclusion

This first section of this chapter detailed the circuit structures for the two proposed TRI based signal processing systems, whilst the second section detailed the high-speed ADC based system, as well as the Folding ADC architecture. Circuit level diagrams were given, along with detailed descriptions of circuit operation. Transfer functions were also detailed to provide better insight into the circuit functionality, along with highlighting the main sources of potential errors.

Each circuit was developed using components selected to achieve high performance and ensure efficient, high-speed and low-power operation; however, various trade-offs in performance and complexity exist between each system due to the different component specifications required for correct system operation and reliability.

The next chapter will demonstrate the performance of each circuit implementation, and assess the accuracy of the main parameters of importance for radiometric PD detection and location.

5 Performance of the PD Signal Processing Methods

In this chapter the performance of the three systems is evaluated and demonstrated. There are various parameters that each system much meet to ensure correct operation. For the TRIs this includes DC offset error and drift, response time and integration accuracy. DC offset error and drift is critical for the NI amplifier as if it is high enough it will cause false triggering of the integrator, drift with temperature will have the same effect. For the TRI, any offset error will be integrated, causing a ramp signal at the output of the integrator. It is impossible to completely remove the offset; however, it can be minimized.

The input bias current of the integrator has the same effect as DC offset, causing a continuous ramp signal at the output due to the constant current being integrated onto the feedback capacitor. Therefore, a high input impedance and low bias current is required to minimize this error. A JFET or CMOS transistor input stage is therefore required. The gain of the NI amplifier, and the time-constant of the integrator, should ideally be constant and close to the calculated ideal, in order for the measured integral of the received PD signal to be quantified within a reasonable accuracy.

The ADC was tested separately from the system. The main parameters for the ADC are with respect to linearity, noise and frequency response, with the most

importance placed on the linear response of the ADC transfer function. Frequency response, in terms of added distortion products, is not critical as no frequency information is obtained from the received PD. Various tests are detailed in this section, along with results, to ascertain the accuracy and associated errors for these parameters.

5.1 Performance of the Standard TRI

The standard TRI uses a high-speed rail-to-rail input-output CMOS op-amp for the NI amplifier. Whilst this op-amp features a high bandwidth and slew-rate, it has a DC offset error specified at ± 2 mV typically, and a drift of 4 μV/°C. The DC offset drift with temperature from 25 °C is theoretically only +60/140 μV, the main DC offset is large, and could potentially cause false triggering to the comparator output, since the comparator threshold voltage is set to only 4 mV. Therefore, the decoupled input to the NI amplifier is biased at -3 mV to ensure false triggering does not occur.

The gain of the NI amplifier and the time-constant of the integrator, which essentially sets the gain of the TRI, are important to ensure that the integral of the received signal can be determined with minimal error, so that any calculations performed on the sampled TRI output are accurate across the amplitude range. The gain of the precision TRI were measured using the test configuration in Figure 5-1.

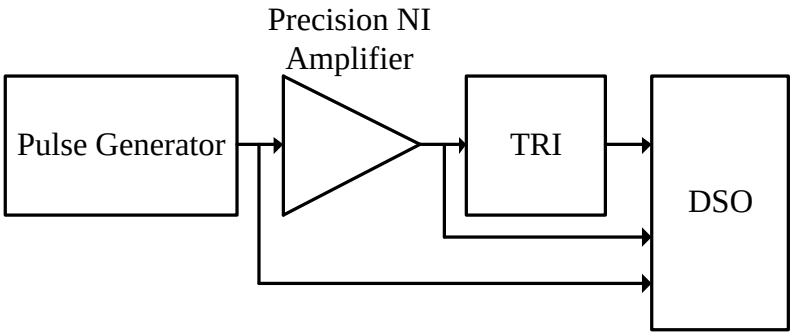


Figure 5-1: TRI Time-Constant Test Configuration

A pulse generator was used to provide an input signal to the NI amplifier. The amplitude of the pulse generator was adjusted from 25 mV to 500 mV in increments of 25 mV. The outputs of the pulse generator, NI amplifier and standard TRI were then measured using a DSO for each incremental change in input amplitude. The gain of the NI amplifier was set using ±1% ceramic SMD chip resistors to ensure accuracy. The standard TRI time-constant was measured for each incremental increase in input amplitude. The NI amplifier and standard TRI outputs as a function of input voltage are shown in Figure 5-2, along with the error between the ideal and actual integrals.

The error between the NI amplifier and standard TRI was between +5.00/-11.27%, with the error becoming larger as the amplitude of the input signal increased. The positive error at low input amplitudes of 25 mV and 50 mV are due to noise being integrated along with the NI amplifier output when the TRI is active. The actual error starts from 0 and increases exponentially. The increasing error is due to the

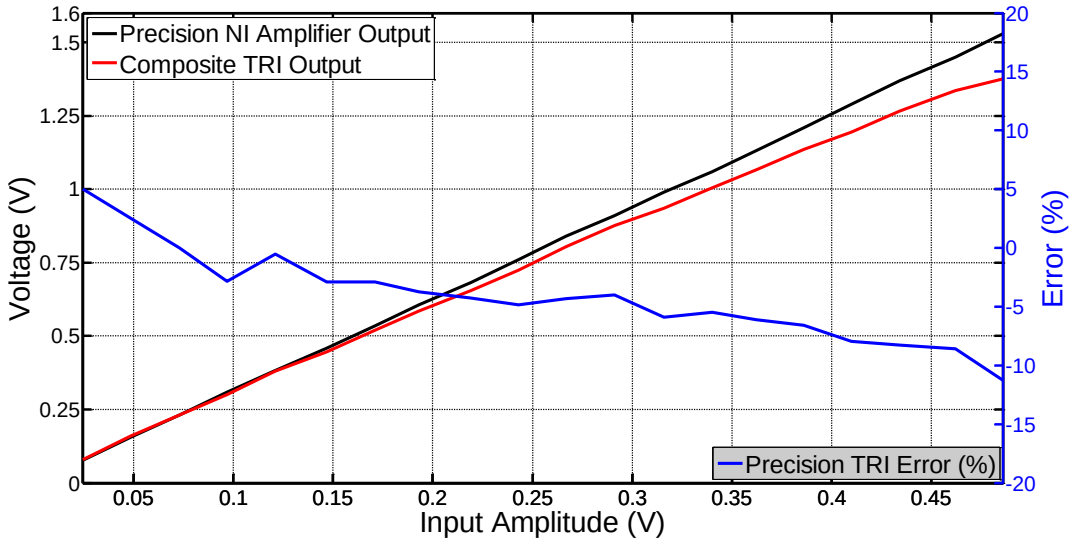


Figure 5-2: NI Amplifier and TRI Outputs vs Input, and TRI Error vs Input

finite open-loop gain of the precision op-amp used, as discussed in Section 4.1.1.

5.2 Performance of the Composite TRI

5.2.1 Composite Precision High-Speed NI Amplifier Performance

There are various requirements for the composite precision high-speed amplifier, for correct and accurate operation of the signal conditioning circuitry. The DC offset error must be minimal, and should not drift excessively over temperature, as this may cause the comparator to trigger in the absence of a pulse and even stay activated for the duration of the measurement period. The accuracy of the energy calculated from the integral of the received PD event also relies on various performance factors of the amplifier. The accuracy of the gain is important to calculate the received energy with reasonable accuracy, this is achieved by using

a large bandwidth op-amp for the main amplifier, and at least 1% tolerance resistors.

The rise time of the amplifier is also an important factor, as if the amplifier cannot respond quickly enough it cannot track the output of the RF power detector, which will cause errors in the integral of the signal. The main limiting factor here is the slew-rate of the main op-amp used, which is 225 V/μs; and therefore, 225 mV/ns. The precision high-speed comparator also requires a fast response time to ensure the TRI is activated with minimum delay when a PD event is received. A comparator with a 8 ns response time was selected. Figure 5-3 shows an emulated received PD event versus the response of the detector output, composite precision high-speed NI amplifier output and comparator output.

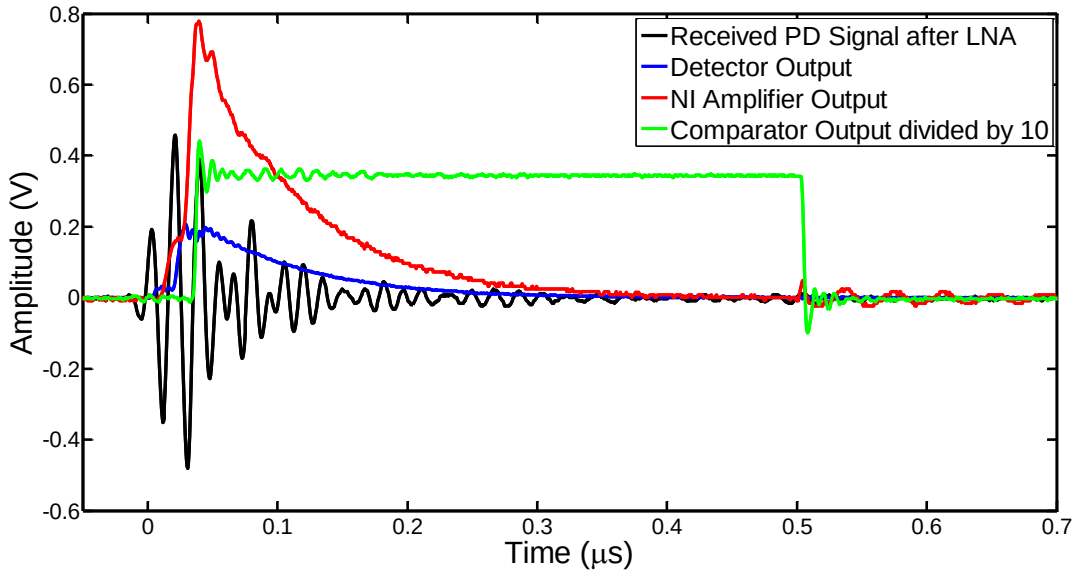


Figure 5-3: Received PD Pulse, Detector Output, Precision NI Amplifier Output and Comparator Output

To determine the response time of the composite precision high-speed NI amplifier for various signal amplitudes, the circuit was tested by applying a step input to it and measuring the output response time, using the test configuration shown in Figure 5-4.

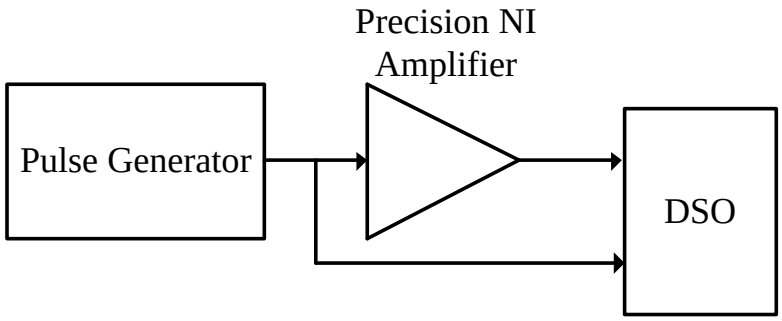


Figure 5-4: Composite Precision NI Amplifier Response Time Test Configuration

A Keysite 33600A series 120 MHz waveform generator was used to produce a pulse signal of 1 μs, with a rise time of 3 ns. The signal was applied to the input of the composite precision high-speed NI amplifier, and the amplitude of the pulse was increased from 50 mV to 1 V in 50 mV increments. The input rise time and precision NI amplifier output rise time were then measured using an Agilent MSO7054A 500 MHz 4 GSa/s DSO for each incremental increase in amplitude. The input of the precision NI amplifier was connected directly to the DSO, and the cable connecting the waveform generator and precision NI amplifier was kept as short as possible, in order to ensure that no additional rise time delay was added by the LC parasitics of additional coaxial cable. Figure 5-5 shows the results of the test.

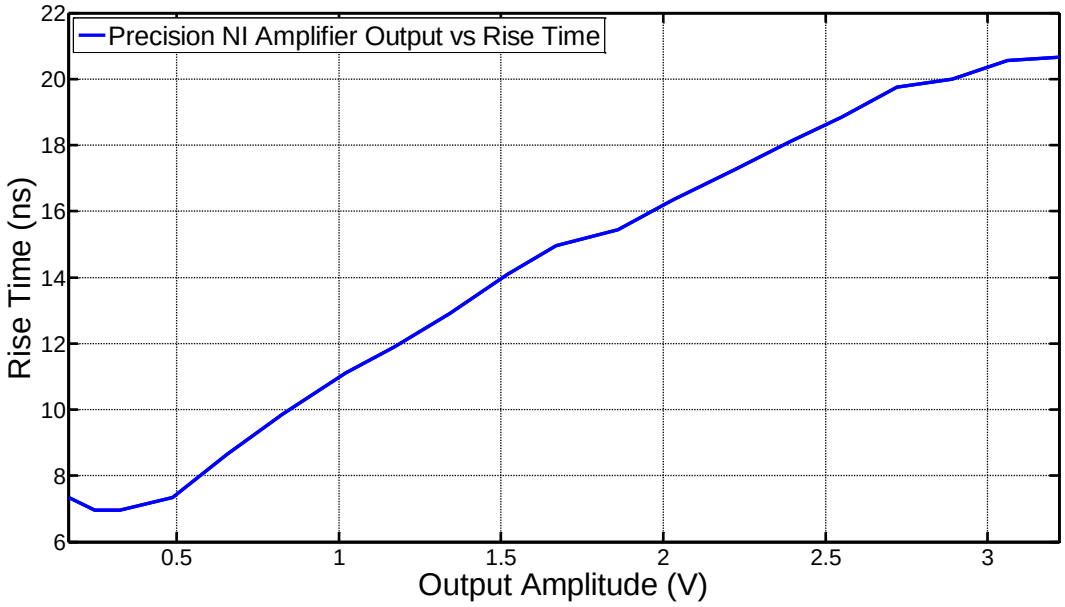


Figure 5-5: Precision NI Amplifier Output vs Rise Time

The measured rise time of the waveform generator was from 3.65 ns to 4.05 ns, with an average of 3.79 ns. The composite precision NI amplifier output rise time was between 6.95 ns and 7.35 ns for output voltages below 500 mV, rising linearly to a maximum of 20.65 ns for an output voltage of 3.22 V. This rise time is minor and should pose minimal error to the accuracy of the calculated energy, since the envelope of the received PD signal is not significantly dispersed.

The DC offset error was evaluated by connecting the input to 0 V (GND) and cycling the composite precision NI amplifier across a temperature range of -20 °C to +40 °C using a computer-controlled temperature chamber, whilst monitoring the output with a DVM. Figure 5-6 shows the test configuration for the DC offset measurement.

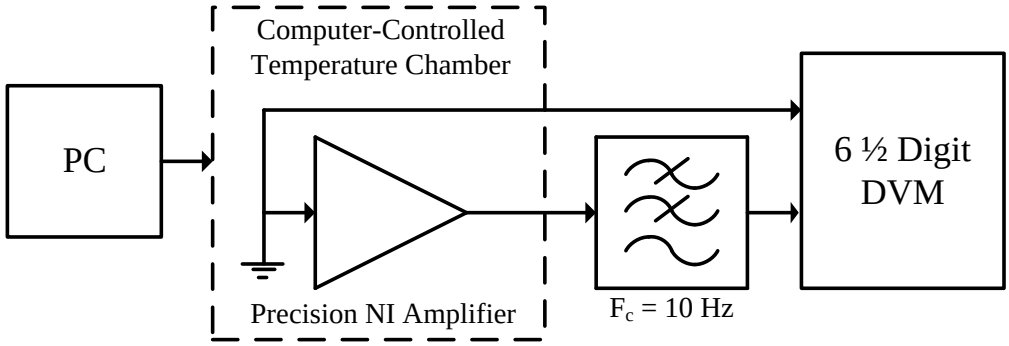


Figure 5-6: Precision NI Amplifier DC Offset Test Configuration

The input and output voltage of the composite precision NI amplifier were monitored by a 6 1/2 digit DVM, whilst the computer-controlled temperature chamber was swept across the temperature range at a rate of 1 °C/40minute. The output was monitored via a 10 Hz low-pass filter to reduce the output noise for better DC measurement accuracy. The input and output voltages were remotely recorded every 10 minutes, along with the temperature at that point. The results are shown in Figure 5-7.

The average offset voltage is -6.31 μV, with the offset increasing and decreasing with temperature between approximately ± 2 μV within a temperature range of -20 ∘C to +30 ∘C. Beyond +30 ∘C the voltage offset begins to increase up to a range of +2 μV to -14 μV, although the average offset is still approximately 6 μV. The main reason for this increase in offset range is due to the solder joints on the prototype circuit forming thermocouples, which exhibit a very small change in voltage over temperature [138], as well as the quantization noise of the DSO front-end ADC.

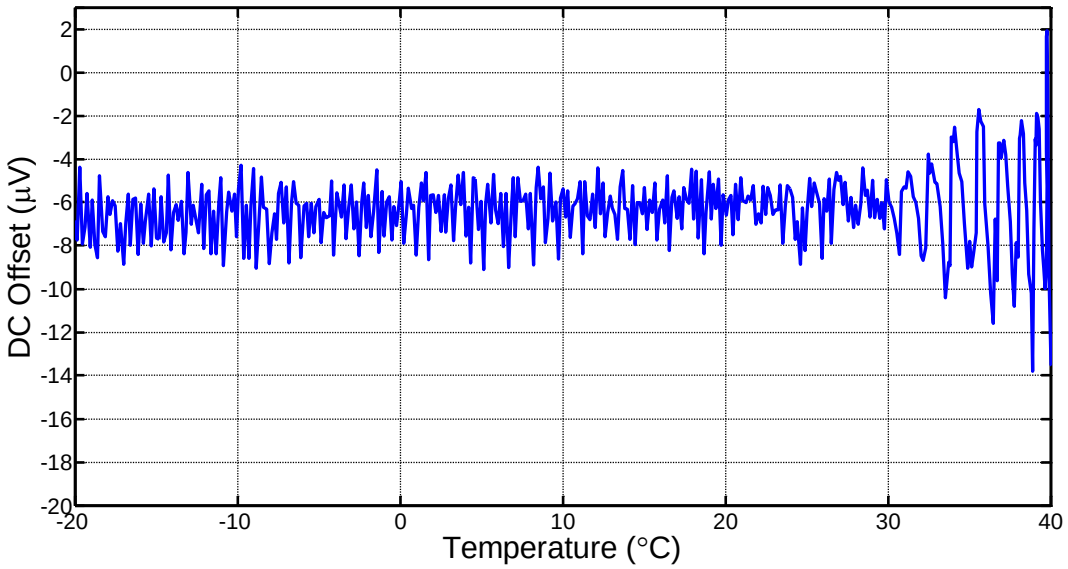


Figure 5-7: Composite NI Amplifier DC Offset Voltage vs Temperature

However, the offset voltage of the composite NI amplifier is still at least a factor of two thousand below the comparator threshold voltage at the maximum offset voltage.

5.2.2 Composite TRI Performance

The time-constant of the integrator effectively determines the gain of the circuit, and is set to 1 μs. The time-constant was tested by inputting a pulse with a 1 μs duration, and a repetition rate of 10 kHz, into the TRI. Figure 5-8 shows the response of the precision NI amplifier and the composite TRI to a 350 mV input pulse.

The amplitude of the input was adjusted from 20 mV to 1 V in increments of 50

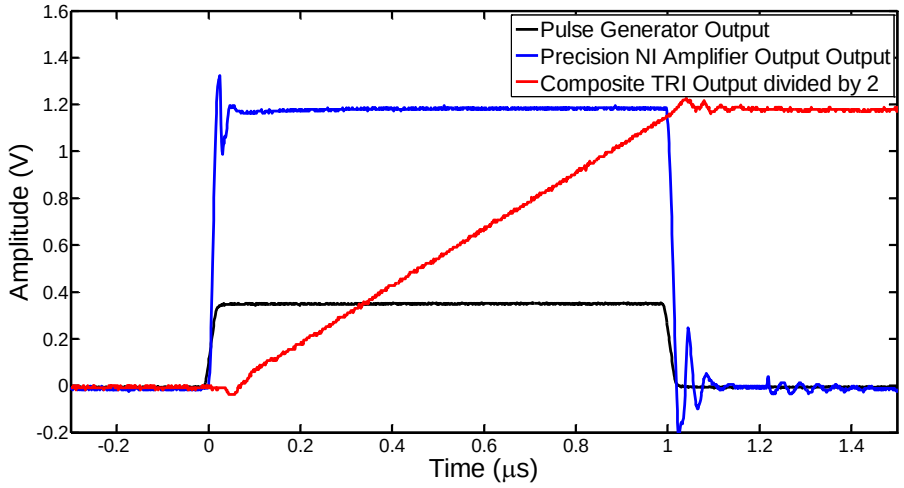


Figure 5-8: Precision NI Amplifier and Composite TRI Output Response to an Input Pulse

mV, and the outputs of the pulse generator, precision NI amplifier and TRI were recorded. The pulse generator signal was monitored to ensure the precision NI amplifier was working correctly. The test configuration was identical to that shown in Figure 5-1. Figure 5-9 shows the response of the precision NI amplifier and composite TRI outputs to the input, as well as the composite TRI time-constant error.

Since the pulse width duration of the input signal is close to that of the TRI time-constant, the step output voltage of the TRI should be identical to the amplitude of the precision NI amplifier output multiplied by the gain of the inverting amplifier, set to two. Therefore, the TRI output was divided by two in order to plot the values on the same voltage scale. From Figure 5-9, it is clear that the precision NI amplifier and composite TRI output traces are similar, identical

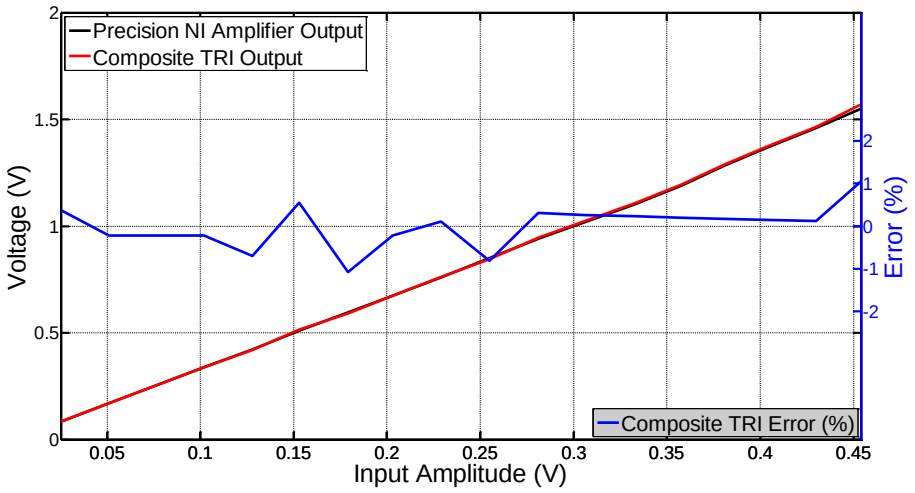


Figure 5-9: TRI Time-Constant Test Configuration

at some points, showing a high integration accuracy. The calculated error was within $\pm 1\%$, and the variation is due to inaccuracies in the measurements caused by the resolution of the DSO ADC, particularly at mid-range voltages where the NI amplifier and TRI are measured in milli-volts compared to volts.

5.3 Performance of the ADC

In practice, a real ADC diverges from the ideal due to parasitic effects such as gain error, offset error, noise, bandwidth and non-linearity. ADCs are tested to assess their performance in terms of these parameters. These tests can be divided into two categories, static performance tests and dynamic performance tests. Static performance tests are used to determine the gain and offset errors, whilst dynamic performance tests calculate the noise, non-linearity and bandwidth.

5.3.1 Static Performance

In order to determine the effects of gain and offset error on the ADC transfer function, differential non-linearity (DNL) and integral non-linearity (INL) are calculated for the device. DNL is used to calculate the difference between an actual step for a given code compared to the ideal, and therefore, what the bin-width of each code is for each step in resolution [139]. INL shows the total linearity of the ADCs response is across the input range. DNL and INL were calculated using histogram testing, using the test setup shown in 5-10.

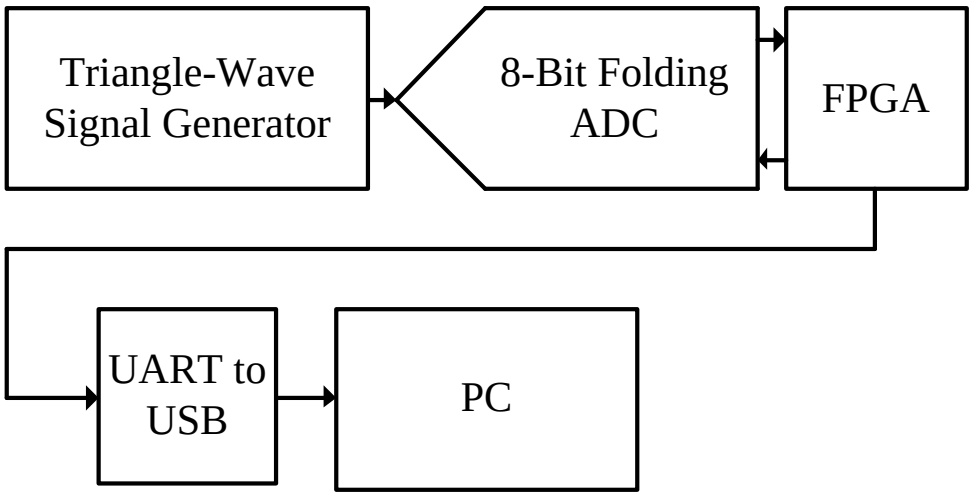


Figure 5-10: Test Configuration for the Histogram

A 0.01% linear triangle-wave was used as an input signal, with an amplitude that extended 5% above and below the maximum and minimum input levels. The ADC was continuously clocked and the output codes of the ADC were stored in RAM within the FPGA, and then transmitted at a lower speed of 1 M/baud to a PC

via a UART to USB converter. The recorded samples were then checked to ensure continuity, with any random glitches or UART restarts removed. a total of number of codes in excess of 80,000 were used to calculate the DNL and INL. The DNL and INL were then calculated using Equations 15 and 16 [140].

$$\mathrm{DNL}(i) = \frac{h(i)}{h(avg)} - 1 \tag{15}$$

$$\mathrm{INL}(n) = \sum_{i=0}^{n} \mathrm{DNL}(i) \tag{16}$$

where DNL(i), H(i) and H(avg) are the DNL at code i, bin-width at code i and average bin-width, and INL(i) is the INL at point n. The range of i is from 0 to $2^n - 1$ and a measured bin-width of 1 LSB corresponds to a missing code. The measured DNL and INL are shown in Figures 5-11 and 5-12 (see Appendix A for the MATLAB code).

Referring to Figure 5-11, the measured DNL and INL are +0.82/-0.65 LSB and +0.77/-0.82 LSB respectively, with no missing codes, with the main fluctuations in code bin-widths are at approximately 1/2, 1/4 and 1/8 of the input range. It is clear from Figures 5-11 and 5-12 that the main non-linearity is at 1/2 the input range. These fluctuations are due to the finite-gain errors of the MSB SHFAs, as well as instability in the comparator outputs at these points, where the

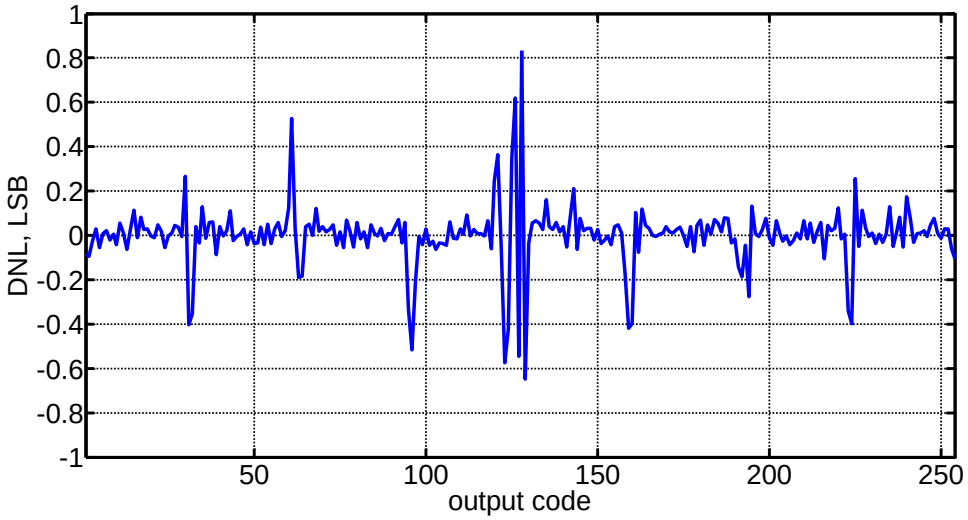


Figure 5-11: DNL for the High-Speed Folding ADC

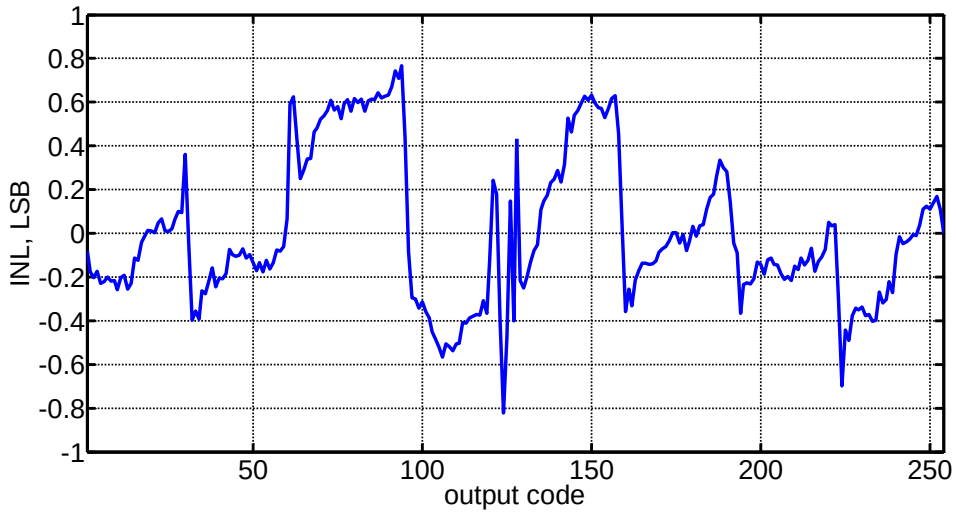


Figure 5-12: INL for the High-Speed Folding ADC

analogue signals are close to the comparator threshold level. However, the measured DNL shows that in between these points the bin-widths are within ± 0.02 LSB, which is a comparable linearity to commercial 8-bit ADCs with similar sample-rates.

Input referred noise is a measure of the noise generated internally within the ADC,

and determines how stable the transition between two codes is for certain DC input voltages [141]. Input referred noise is generally measured by grounding the input or applying a filtered DC signal for a number of different codes. A large number of samples are then recorded for a specific DC input voltage, and a histogram is plotted for the measured codes, as shown in Figure 5-13.

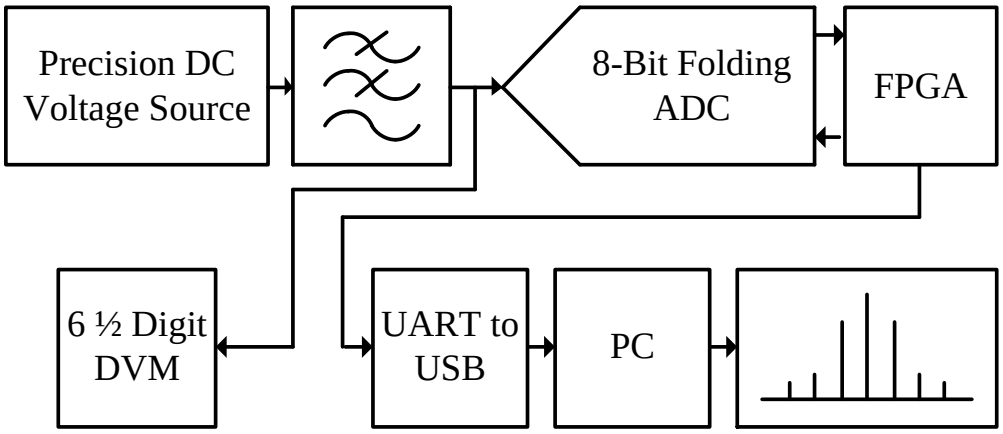


Figure 5-13: Input Referred Noise Test Configuration

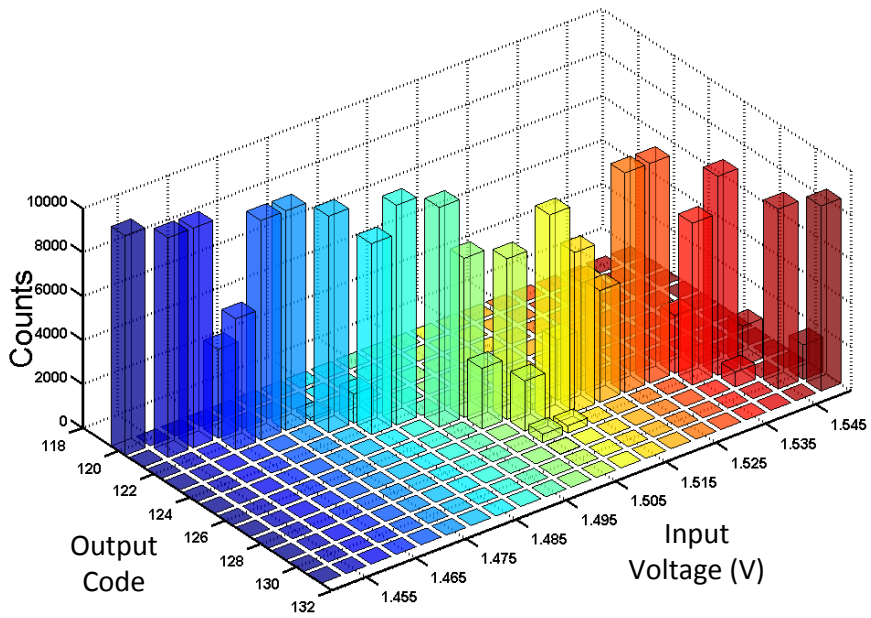
The output of a Krohn-Hite Model 511 precision DC voltage source was applied to the ADC via a low-pass filter with a cutoff frequency of 10 Hz. The input voltage was monitored using an Agilent 34401A 6 1/2 digit multi-meter to ensure the voltage level was correct. Since the ADC is only 8-bit the theoretical bin-width is 11.8 mV for a 3 V input range. Therefore, measuring the input referred noise at most DC points yielded only one code at the output even for large data records. Figures 5-11 and 5-12 show that most irregular bin-widths occur at half the input range. To test the DC noise performance, and DC stability at the center range,

a range of DC levels were applied to the ADC, from 1.45 V to 1.55 V, in 5 mV increments. The RMS noise measured at the input of the ADC was approximately 3 mV RMS. Figures 5-14a and 5-14b shows the measured results (see Appendix A for the MATLAB code).

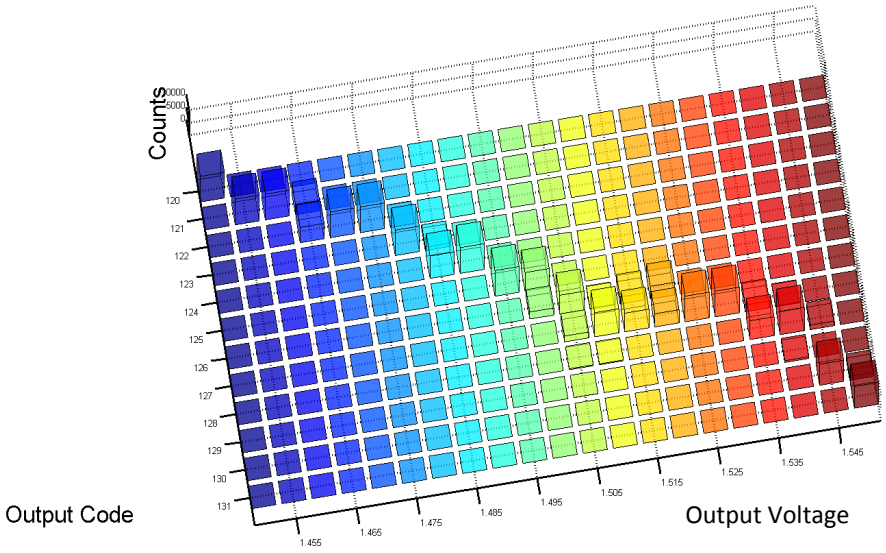
The output codes for a given input voltage are stable across the measurement range of 1.45 V to 1.55 V, with 125 being the output code measured for an input of 1.5 V. At certain input voltages, recorded codes fell into two bins, such as 1.465 V, 1.500 V and 1.535 V, and 3 codes were recorded an 1.505 V, which is likely due to the noise on the input signal. At the higher end of the measurement range the bin-width is reduced compared to the codes at the lower end of the measurement. Particularly at 1.540 V and 1.545 V where code 129 has very few counts compared to codes 128 and 130, showing a drastically narrower bin-width at that input position. However, figures 5-14a and 5-14b do show a reasonably linear response across the measurement band at the middle of the ADC input range.

5.3.2 Dynamic Performance

Dynamic testing of ADCs is done to determine the overall noise and linearity performance over a given bandwidth, usually half the sample-rate used. Various parameters were calculated from recorded data for a given input frequency. Specifically, signal-to-noise ratio (SNR) spurious free dynamic range (SFDR), total harmonic distortion (THD) and signal-to-noise-and-distortion (SINAD) were measured. SNR is the ratio of the maximum input signal range to the noise floor



(a)



(b)

Figure 5-14: Input Referred Noise 3D Graph, (a) Side View, and (b) Top View

of the ADC, SFDR is the difference between the maximum input signal range and the highest harmonic, THD is the sum of the first 5 harmonics, excluding the fundamental, and SINAD is the ratio of the maximum input signal to the sum of the noise and THD. Each parameter was calculated by performing a Fast-Fourier Transform (FFT) on data measured using the test configuration shown in Figure 5-15.

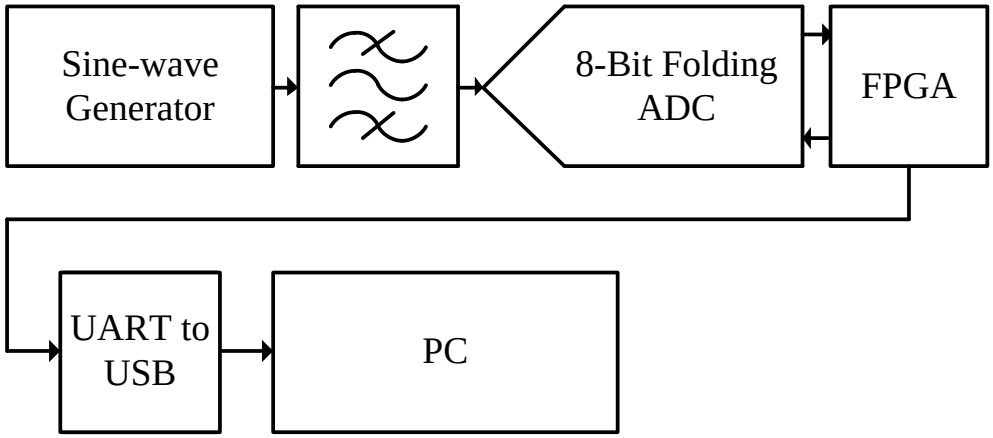


Figure 5-15: FFT Test Configuration

A sine-wave signal was applied to the input of the ADC through a 6^{th} order band-pass filter, with an identical center frequency. The amplitude of the signal was set just below the maximum input range of the ADC to ensure no distortion was produced from clipping, and the DC offset level was set to half the input range. Frequencies at approximately 207 kHz, 500 kHz, and 2 MHz were used for the FFT testing to determine the effects of increased input frequency on non-linearity . To ensure minimal spectral leakage, each frequency was calculated using Equation 17,

and Hanning windowing was applied to the FFT data.

$$\frac{f_{IN}}{f_S} = \frac{M}{N} \tag{17}$$

where f_{IN}, f_S, M and N are the input signal frequency, the ADC sampling, the number of integer input signal cycles and the number of data points respectively. M must ideally be a prime integer value, and N must be to the power of two for the FFT to function properly [142]. The spectrum of the 207 kHz input signal is shown in Figure 5-16 (see Appendix A for the MATLAB code).

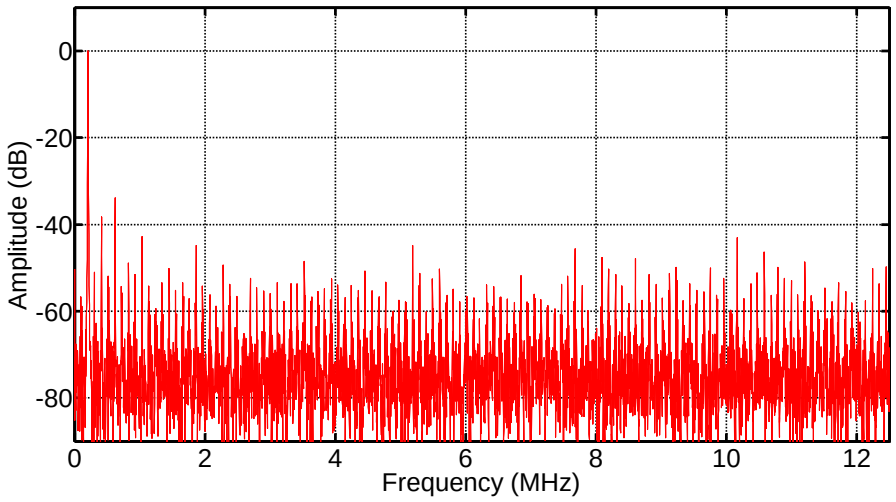


Figure 5-16: FFT for a 207 kHz Input Signal

At 207 kHz, the measured SNR, SFDR and THD were 31.89 dB, 37.36 dBc and -32.68 dBc respectively. This dropped to 22.16 dB, 28.98 dB and -23.89 for SNR, SFDR and THD respectively at a frequency of 845 kHz. At 1.5 MHz, the measured

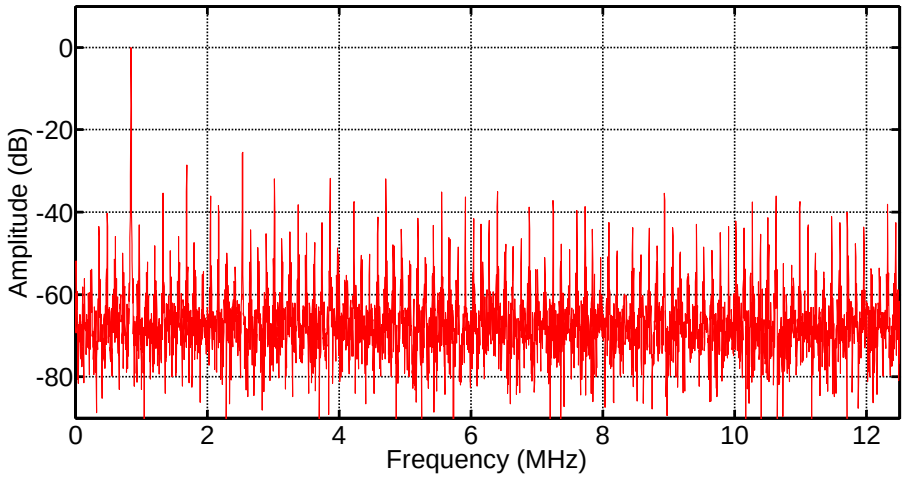


Figure 5-17: FFT for an 845 kHz Input Signal

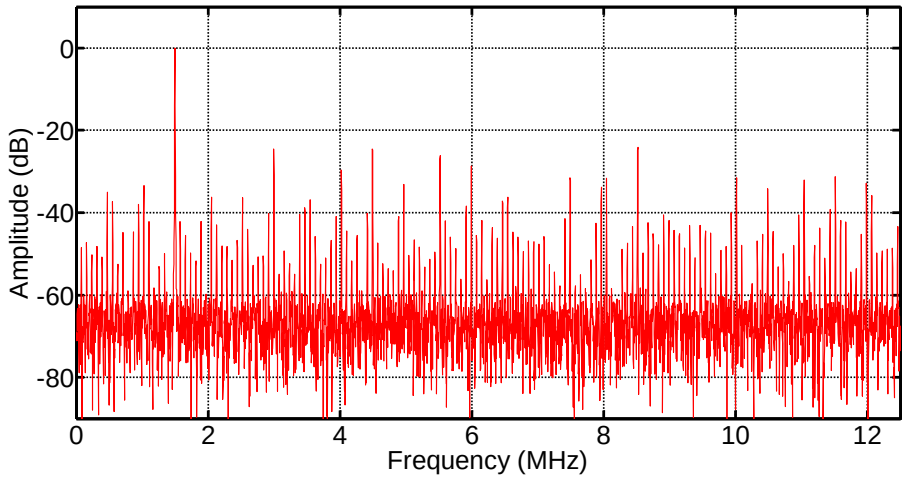


Figure 5-18: FFT for a 1500 kHz Input Signal

SNR, SFDR and THD further decreased to 18.27 dB, 27.69 dB and -21.17 dBc respectively. The SINAD was 28.9 dBc, 19.69 dBc and 16.32 dBc for 207 kHz, 845 kHz and 1.5 MHz respectively. From Figures 5-16, 5-17 and 5-18 it is clear that there are non-integer frequency spurs across the band, at an approximate frequency of 100 kHz. However, the reason for these spurs is unclear, but is possibly due to any non-linearity in the SHFAs.

Whilst the dynamic performance of the ADC is far below that which would be acceptable as a commercial device, the non-linear products generated by the ADC are only an issue if they significantly change the value of a sampled data point so that it contains a large error when converted to linear power. Furthermore, the frequency content of the received PD is removed by the detector; therefore, no useful frequency information is present that could be measured.

The low SNR would be significant in many applications; however, the logarithmic response of the detector alleviate any requirement to measure low values, as the received PD signal is compressed so that low-level signals are in the range of at least a few hundred mV. Therefore,

5.4 Conclusion

This chapter has demonstrated the performance of the main important parameters of each system for efficient and effective radiometric PD signal processing. The standard and composite TRIs both produce an integral of the input signal within an acceptable accuracy of +5%/-11% for the standard TRI and ±1% for the composite TRI. The composite NI amplifier has a response time between 6.95 ns and 20.65 ns, which should cause minimal lag, and therefore error, to the envelope detected PD signal.

The measured linearity of the proposed high-speed folding ADC is adequate for PD

measurement, with a DNL of +0.82/-0.65 LSB and an INL of +77/-0.82 LSB. The measured dynamic performance of the ADC was far below that of a commercial type, with a SNR, SFDR and THD of 18.27 dB, 27.69 dB and -21.17 dBc at an input frequency of approximately 1.5 MHz. However, the ADC is not used to measure or calculate any frequency content from the received PD signal, since the RF power detector removes any spectra and leaves only the envelope. Therefore, these parameters are not critical unless they cause significant error to the measured power in each received PD pulse.

The performance of the signal processing systems for radiometric PD detection and location are presented and detailed in the next chapter.

6 Results

This section will present the measurement results for the three radiometric signal processing systems proposed, along with analysis and comparisons of the results.

6.1 Attenuation and Distance Measurements

Distance measurements were performed for both the TRI and folding ADC based systems, and compared to data obtained from high-speed sampling (in excess of 1 GS/as), to ensure the sampled data had minimal error. The distance tests were initially simulated in a laboratory using attenuators, which ensures that reflections do not impair the measurement since any reflections occurred will the identical for each, and then in an outdoor environment. The laboratory-based distance tests, the setup of which is shown in Figure 6-1, were carried out by placing the sensors approximately 2 m away from an artificial source of PD to ensure the sensor was outside of the nearfield of the source.

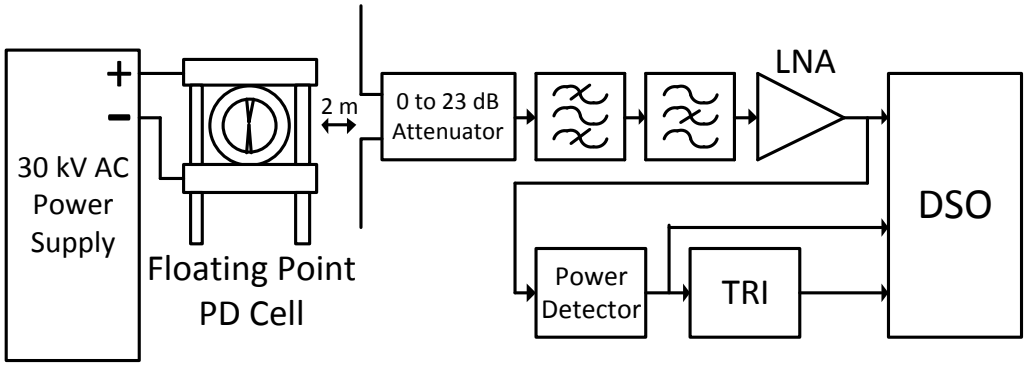


Figure 6-1: Laboratory distance test setup for the TRI [132]

The received signal was attenuated via -3, -6, -10 and -20 dB RF pads, simulating increasing distance with increasing attenuation. The amplified PD signal, detector output and TRI output were sampled at 2 GS/as using a DSO. The source was generated using a floating electrode PD emulation cell energized at 10 kV AC via a Bicotest P123 power supply, shown in Figure 6-2. The radiometric signal propagated from the PD cell was received via a dipole antenna, and applied to the sensor under test.

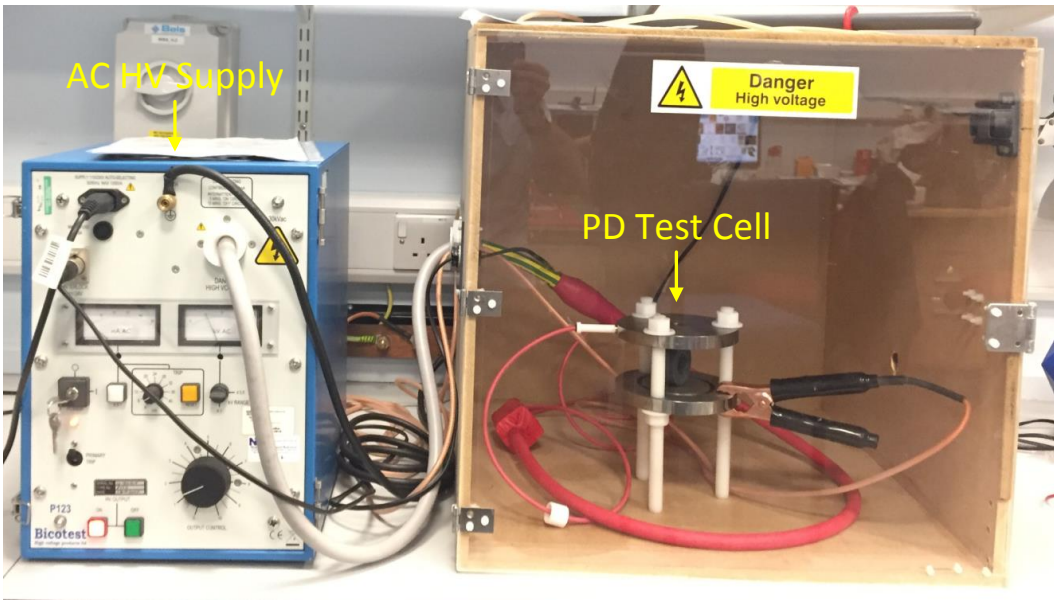


Figure 6-2: Floating electrode PD emulation cell and Bicotest P123 30 kV AC power supply [132]

The received energies for the LNA output and detector output were calculated by integrating digitally, whilst the energy for each TRI was calculated using a step voltage change to the output. The energy for each output was calculated using

Equations 18, 19 and 20.

$$E_{LNA} = \Delta T \sum_{i=n}^{n} \frac{Vi_{LNA}^2}{R} \tag{18}$$

$$E_{DET} = \Delta T \sum_{i=n}^{n} \frac{Vi_{DET}}{K} \tag{19}$$

$$E_{TRI} = \frac{\Delta V_{TRI} \tau_{TRI}}{K A_{NI} A_{IN}} \tag{20}$$

where E_{LNA}, E_{DET} and E_{TRI} are the energies calculated from the LNA output, detector output and TRI output, V_{LNA}, V_{DET} and V_{TRI} are the LNA, detector and TRI output voltages, and T, n, R, K, τ_{TRI}, A_{NI} and A_{IN} are the time between samples, number of samples, LNA output load, detector constant, TRI time constant, NI amplifier gain and inverting amplifier gain respectively. The NI amplifier gain was 3.0 for the standard TRI and 3.2 for the composite TRI, whilst the inverting amplifier gain was 2.0 for both TRIs.

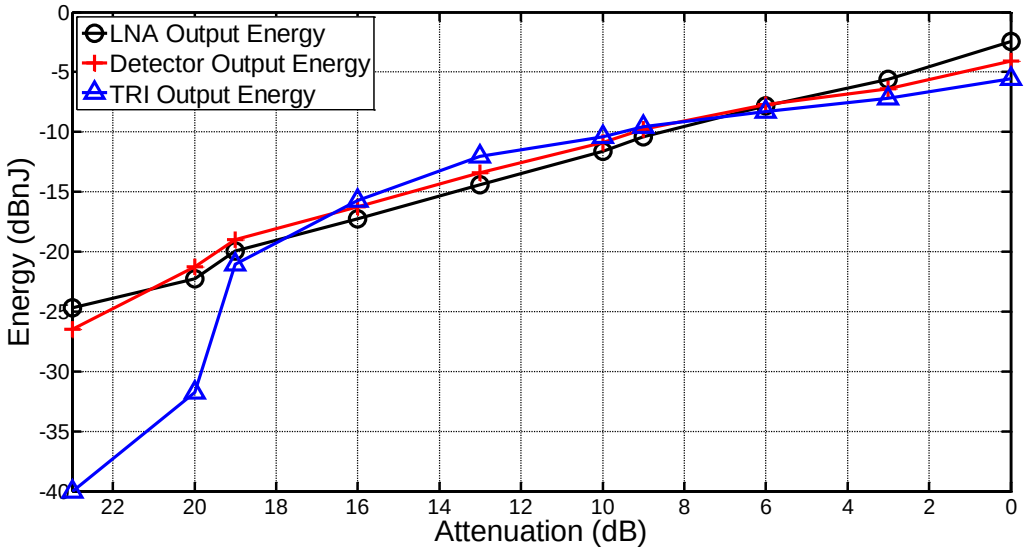
6.1.1 Standard TRI

The standard TRI was tested with both the HSMS-2850 based zero-bias detector and the LTC5507 detector. The reason for this being that whilst the LTC5507

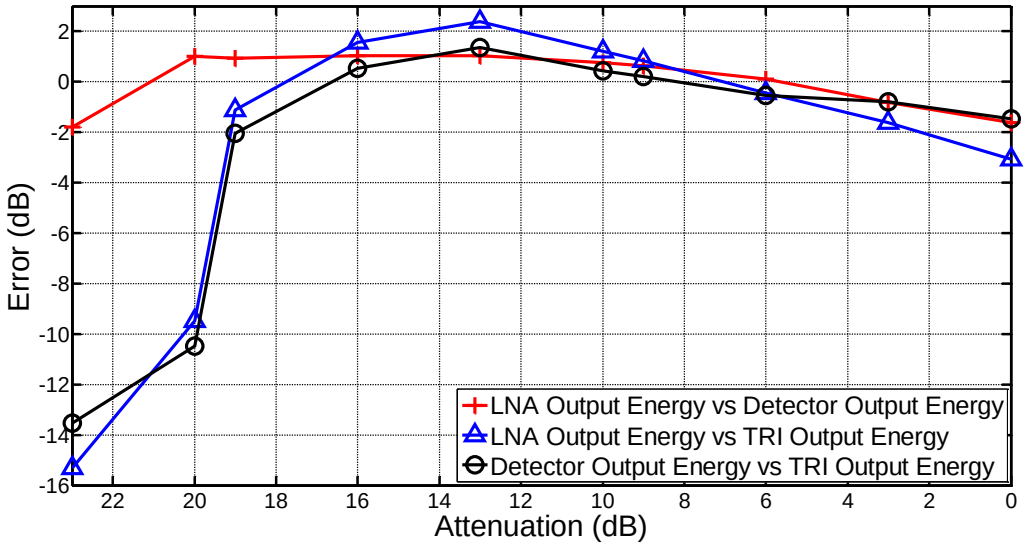
detector provides higher sensitivity and dynamic range over the HSMS-2850 based detector, it is incapable of following the true envelope of the radiometric PD signal; therefore, the accuracy of the LTC5507 is limited since the output envelope shape is dependent on the detector time-constant. Figure 6-3a and 6-3b show the energies calculated from the LNA, detector and standard TRI outputs for values of attenuation between 0 dB and 23 dB, and the error between the LNA, detector and standard TRI outputs (see Appendix A for the MATLAB code to calculate the energies for each measurement).

The error between the LNA and detector output energies is between -1.79 dB and +1.04 dB, with the highest deviation at an attenuation of 0 dB and 23 dB. The errors between the LNA and TRI output, and between the detector and TRI outputs, are much greater, with maximum and minimum deviations of +2.39 dB and -15.31 dB between LNA and TRI, and +1.03 dB and -13.52 dB between the detector and TRI. The main source of error at large attenuation values, at and beyond 19 dB, is due to the propagation time before the integration is started, which limits the amount of the received PD pulse that is integrated. The error between the TRI and detector energies at low values of attenuation, below 6 dB, is due to the large signal response of the TRI as shown in Figure 5-1 in the previous chapter.

The same test was performed with the standard TRI using the LTC5507 detector. The energies for the LNA, LTC5507 detector and TRI outputs were calculated using Equations 18, 19 and 20, as with the HSMS-2850 based detector. However,



(a)



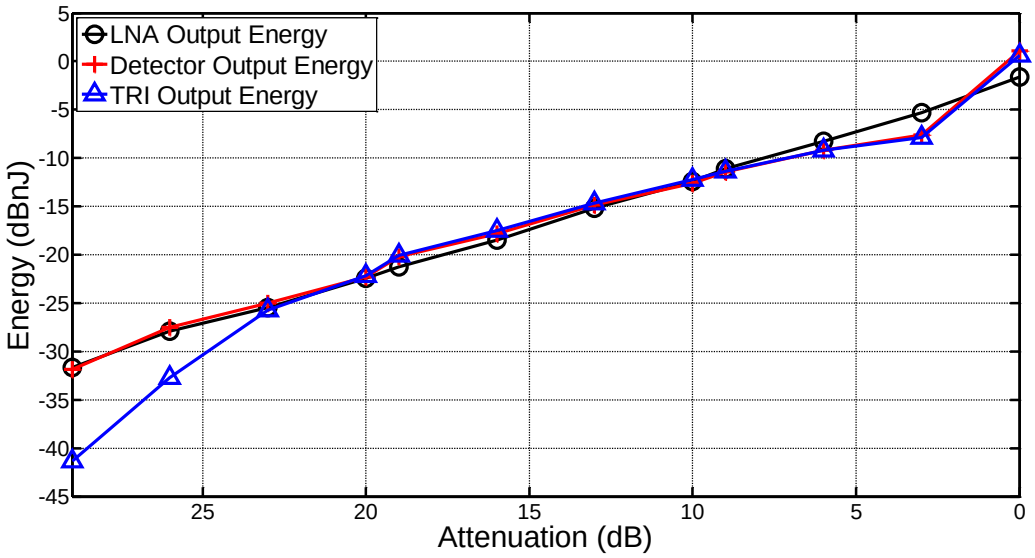
(b)

Figure 6-3: LNA, HSMS-2850 Based Detector and Standard TRI output, (a) Energies versus Attenuation, and (b) Error versus Attenuation

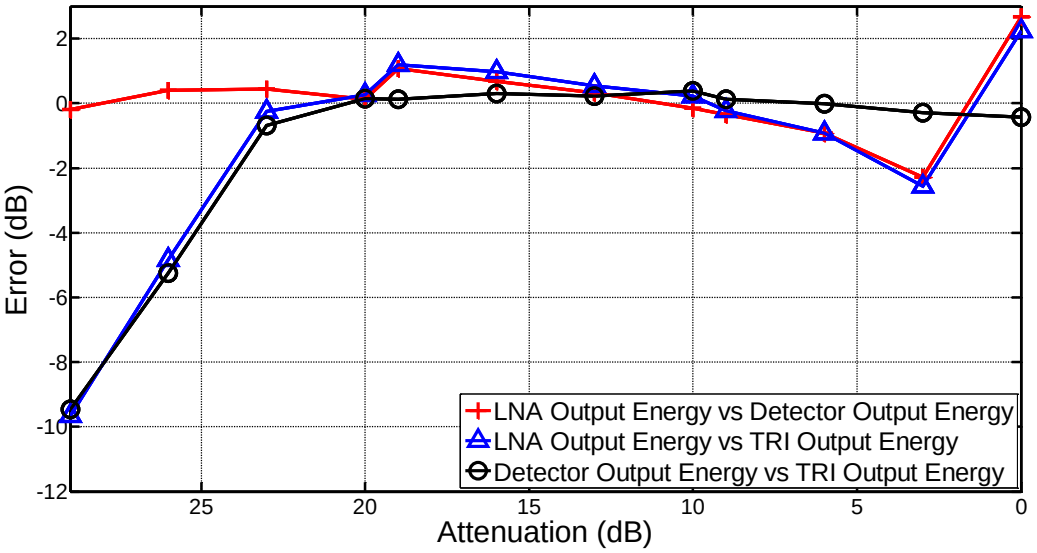
since the transfer function of the LTC5507 has two slopes, two values were used for the detector constant, k, which were 99 and 541 for detector output voltages above and below 481 mV respectively. Figure 6-4a and 6-4b show the calculated energy for the LNA, detector and TRI outputs at each attenuation setting, and the error between the LNA and detector outputs, LNA and TRI outputs and detector and TRI outputs.

The measurement taken at an attenuation of 0 dB required a detector constant of 99, all other measurements used 541. The error between the detector and TRI was within 1 dB at and below an attenuation of 23 dB, Beyond which the error increases to a maximum of -9.47 dB due to the amplitude of the detector output falling below the threshold of the comparator; therefore, causing the integrator to remain inactive for the majority of the detected pulse. This error is further increased by the propagation speed of the TRI, which includes the slew-rate of the front-end NI amplifier, the precision comparator NI amplifier, the high-speed comparator itself and the analogue switches.

The error between the LNA and detector outputs is between -0.92 dB and +1.08 dB for attenuations at 6 dB and above, below this the error is -2.28 dB and +2.67 dB at attenuations of 3 dB and 0 dB respectively, which is primarily due to the LNA output being near the threshold for the internal AGC of the LTC5507 detector, causing it to switch between the two slopes, and therefore, to change the gain whilst processing a received pulse. This issue causes the detector



(a)



(b)

Figure 6-4: LNA, LTC5507 Detector and Standard TRI output, (a) Energies versus Attenuation, and (b) Error versus Attenuation

constant to become ambiguous, and an accurate value of k to be difficult to realize. The error between the detector and TRI outputs is -0.69 dB to +0.39 dB at and below attenuations of 23 dB, and closely follows the error between the LNA and detector outputs up until an attenuation of 20 dB. As with the the difference between the LNA and TRI outputs, at attnuations of 26 dB and 29 dB the error increased to -5.25 dB and -9.47 dB respectively. The reason for this larger error is exactly the same as with the error between the LNA and TRI outputs.

Whilst the results in Figure 6-4 look reasonably accurate, it should be noted that the LTC5507 detector is incapable of tracking the true envelope of the signal; therefore, whilst the calculated detector energy is close to the LNA output energy, this would likely change if the pulse duration and height of the received PD pulse were to change, since the output pulse of the LTC5507 is influenced by the bandwidth of the detector. A further issue is that whilst the detector has a higher dynamic range than that of the HSMS-2850 detector, this is diminished when receiving fast duration pulses as the envelope of the pulse is stretched by the response of the detector, and therefore, the peak height is reduced. This causes the pulse to drop below the comparator threshold level at low PD signal amplitudes, which limits the range at which a source of PD can be measured by the TRI. Figure 6-5 shows the response times of the LTC5507 and the HSMS-2850 detector.

Since the composite TRI has various benefits over the standard TRI, such as lower power consumption, greater speed and higher accuracy, no outdoor tested was

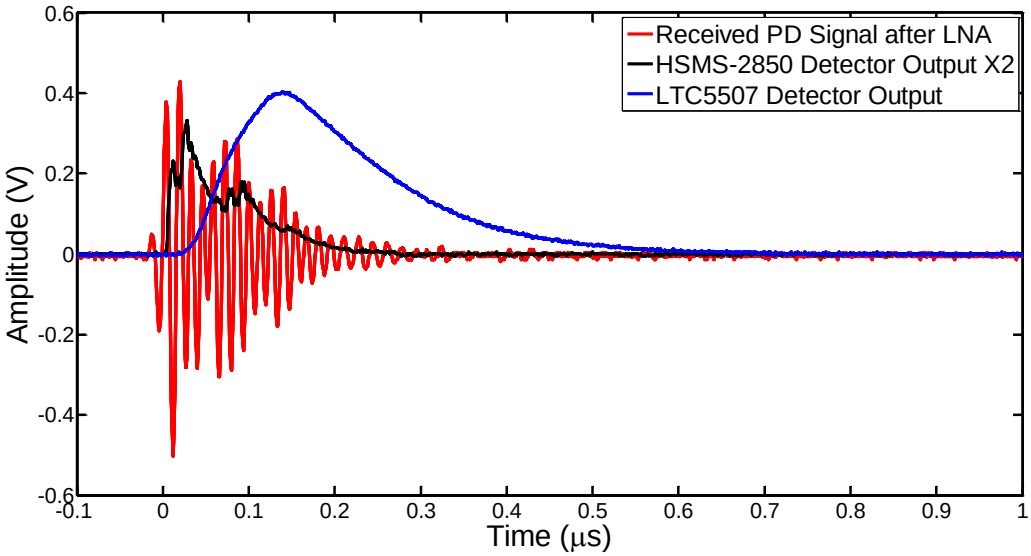


Figure 6-5: LNA Output, and HSMS-2850 and LTC5507 Detector Outputs

performed on the standard TRI since the results would likely be below the accuracy of the composite TRI. The composite TRI was only tested with the HSMS-2850 based zero bias detector, due to the higher accuracy and bandwidth of the detector. The results of the composite TRI are shown in the next section.

6.1.2 Composite TRI

The composite TRI was tested using the HSMS-2850 based detector only, since it features a much higher bandwidth than the standard TRI, and therefore, would likely feature higher accuracy. A comparison of the LNA, detector and TRI output energies is shown in Figure 6-6.

The time delay between the LNA and detector energies is due to the response of the

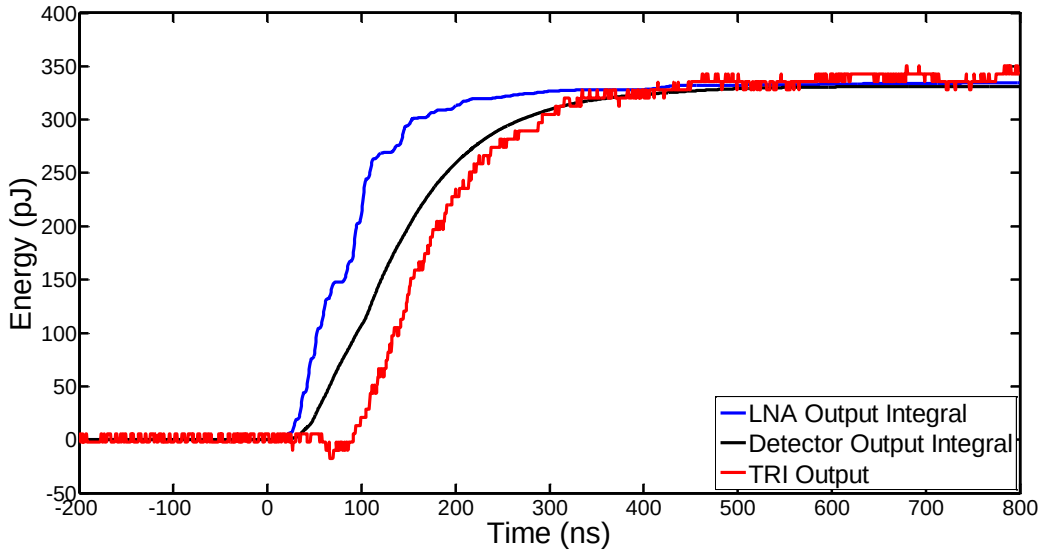
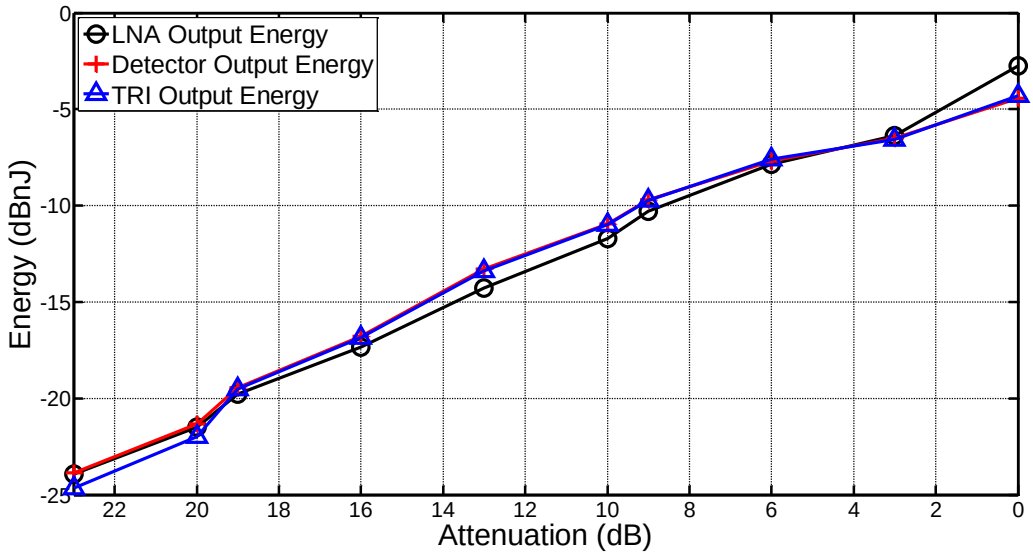


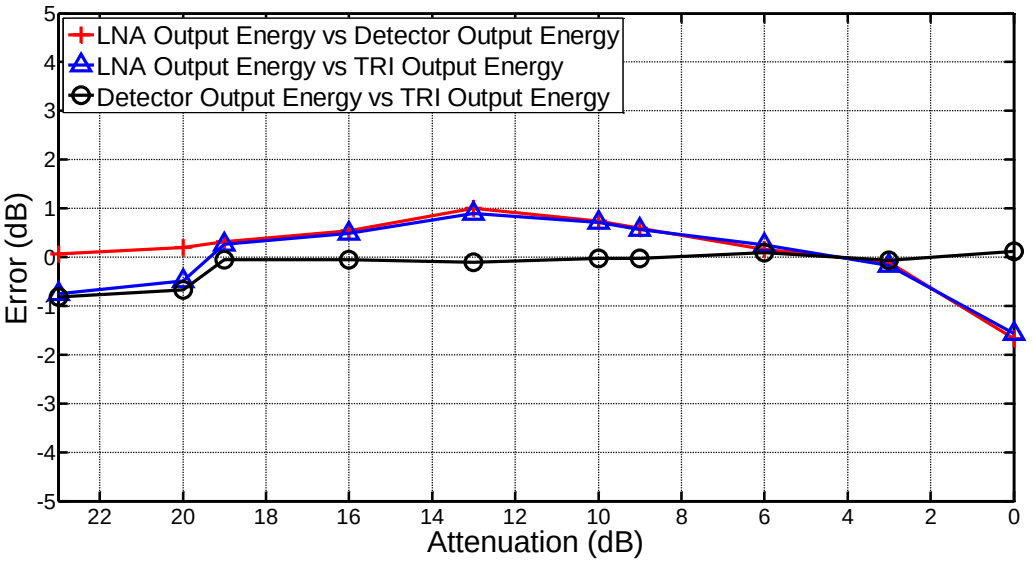
Figure 6-6: Integrated energies for the LNA, detector and TRI outputs [132]

detector causing a minor expansion to the pulse envelope. The further delay to the TRI response is due to the transient response times of the high-speed comparator and analog switch S1, along with propagation delays through interconnecting transmission lines and adapters. However, although delays are present between each integral, they still converge to approximately the same value. The energies were calculated for each step increase in attenuation, from 0 to -23 dB, for all three outputs. The results are shown in 6-7a, whilst the error between each output is shown in 6-7b.

The energy calculated using Equation 18 from the DSO measurement of the LNA output signal is assumed to have the highest accuracy. The accuracy of the detector output (with respect to the LNA output) is +1.0/-1.7 dB. The accuracy of the TRI is +0.9/-1.6 dB. The difference between the detector and TRI outputs is



(a)



(b)

Figure 6-7: LNA, HSMS-2850 Based Detector and Composite TRI output [132], (a) Energies versus Attenuation, and (b) Error versus Attenuation

+0.1/-0.8 dB suggesting that the error is principally due to non-linearity of the detector response, especially at high signal levels. The accuracy of the energy inferred from the composite TRI output has been shown to be sufficient for RSS location of PD sources to within about 1 m. Figure 6-7b shows that the error between the composite TRI and zero-bias detector is insignificant as compared to the error between the standard TRI and zero-bias detector, as shown in Figure 6-8.

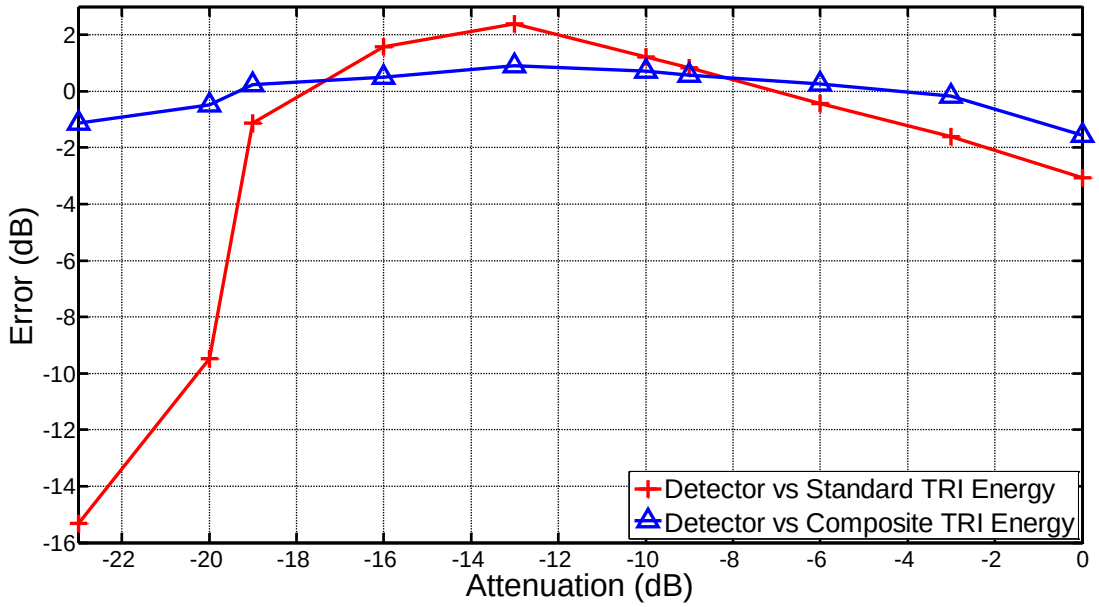


Figure 6-8: Standard and Composite TRI Error vs Attenuation using the HSMS-2850 Detector

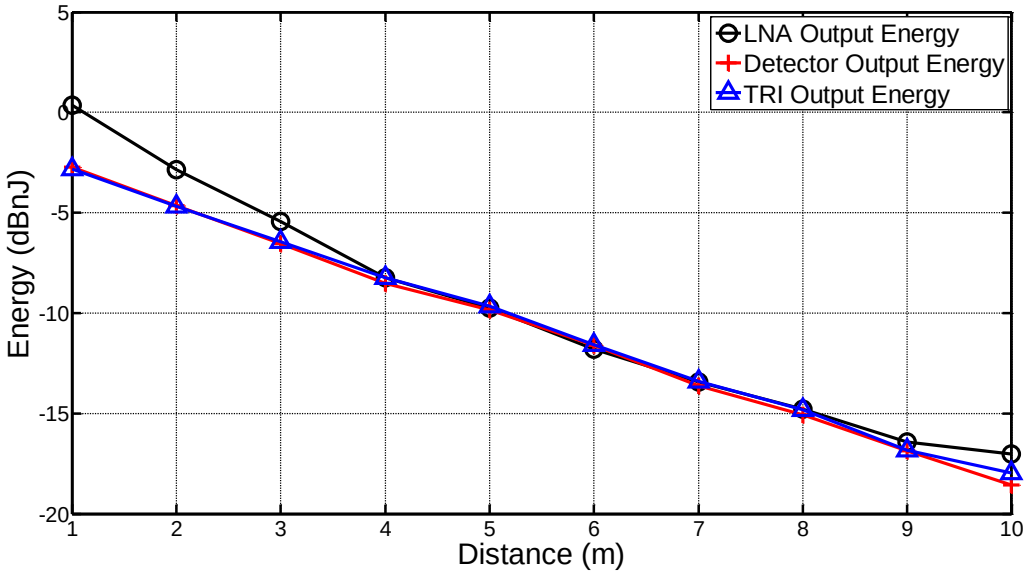
The outdoor distance test was performed by positioning the sensor 1 m away from the PD calibrator, set to 10 nC. Measurements were then taken for the sampled LNA output, sampled detector output and TRI output. The calibrator was then moved away from the sensor by increments of 1 m and measurements were made for each incremental step up to 10 m. Figure 6-9a shows the results for sampled LNA

and detector outputs, and the TRI output, whilst Figure 6-9b shows the errors between sampled LNA, sampled detector and TRI outputs.

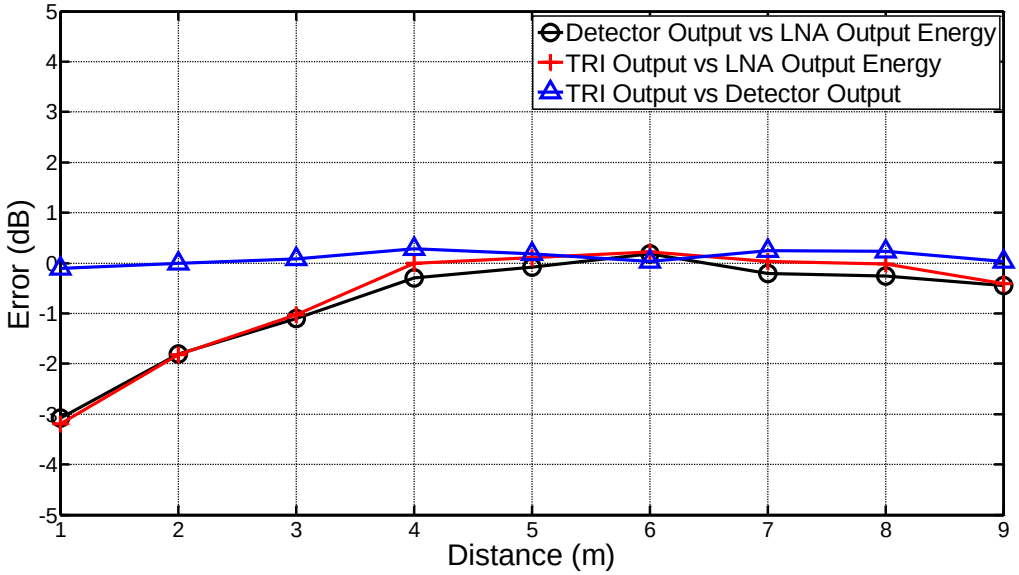
The error between TRI and detector energies is between -0.1 and +0.3 dB. The error between the detector output and LNA output energies is between -0.4 and +0.2 dB beyond a distance of 4 m, whilst the error between the LNA Output energy and the TRI is between -0.4 and +0.2 dB beyond 4 m. At distances below 4 m the error increases, with an error of -3.1 and -3.2 dB at 1 m for the detector output and TRI output energies respectively, corresponding to an error in distance of approximately 1 m. The error below 4 m is primarily due to the zero-bias detector entering the transition between the square and linear responding regions, above a signal level of approximately 0 dBm.

The distance test was repeated with a stronger PD source to determine the increase in non-linearity to the detector output compared to distance. The PD calibrator was set to 100 nC and the experiment was repeated, with the sampled LNA output, sampled detector output and TRI output measured from 1 to 10 m in 1 m increments. Figures 6-10a and 6-10b show the results and errors for sampled LNA, sampled detector and TRI outputs respectively.

It is clear that with the increased PD source strength the error is more severe; however, the error between the sampled LNA and TRI energies is still within 1 dB at 4 m and beyond. Below 4 m, the error increases to maximum of 5.1 dB at a

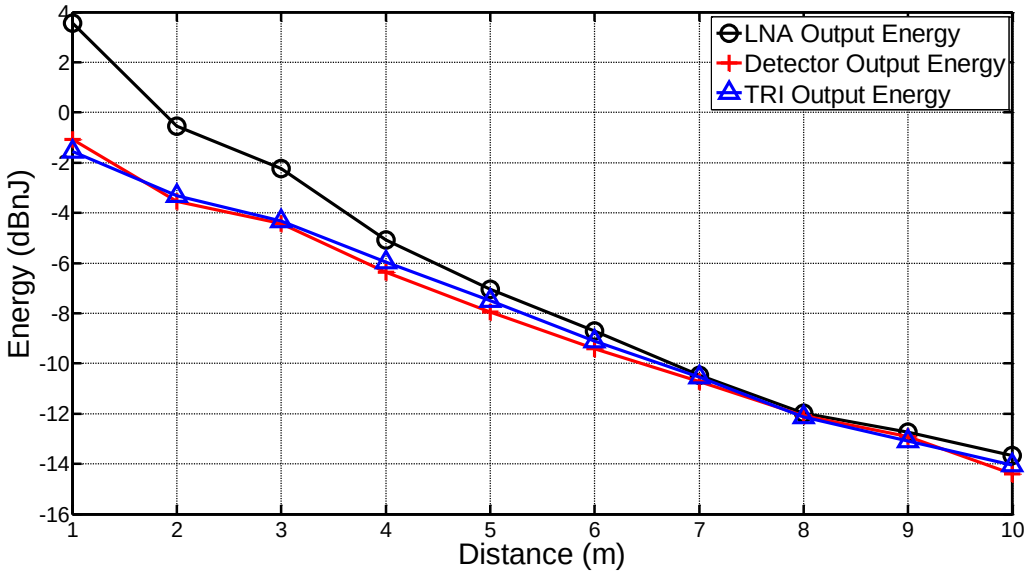


(a)

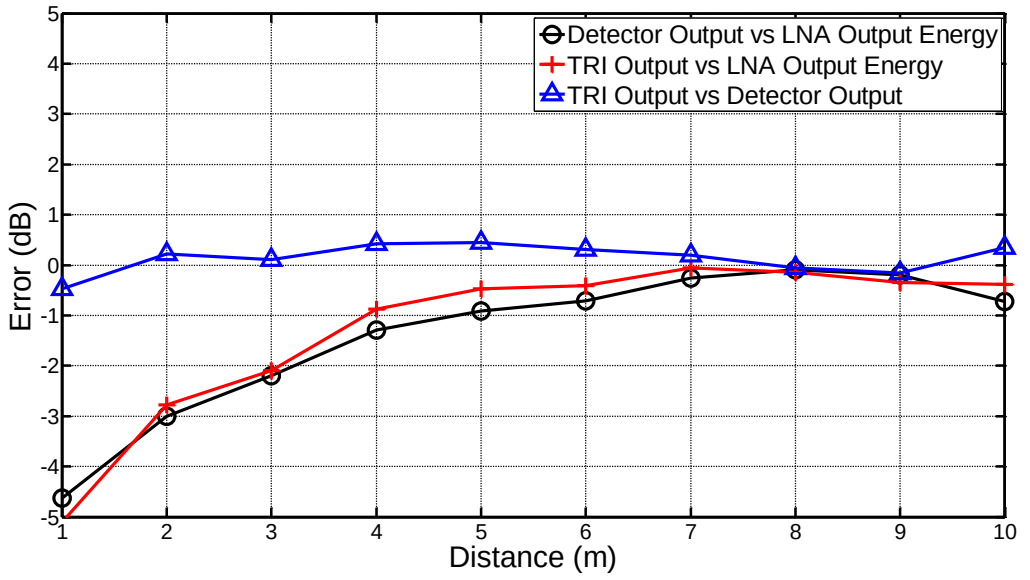


(b)

Figure 6-9: Composite TRI Measurements from a 10 nC PD Source [132], (a) at distances of 1 to 10 m, and (b) Errors between sampled, detector and TRI energies



(a)



(b)

Figure 6-10: Composite TRI Measurements from a 100 nC PD Source, (a) at distances of 1 to 10 m, and (b) Errors between sampled, detector and TRI energies

distance of 1 m.

6.2 Location Estimation Measurements for the Composite TRI

To ascertain the accuracy of the composite TRI-based signal processing systems for location estimating based on RSS, the data acquired for the system was again compared to a system utilizing high-speed sampling to obtain a measure of the received energy. The output of the LNA, detector and composite TRI were all sampled via the 2 GS/as ADC of a DSO, and the received energies were calculated in the same manner as those in 6.1.2, using equations 18, 19 and 20.

The calculated energies were then entered into a simple location algorithm. The algorithm is based upon the ratio of received power for sensor node pairs [97], since the transmitted PD power is unknown. The algorithm uses the simple propagation model given in Equation 2 from Section 2.5.3, and the ratio of received sensor powers shown in Equation 21.

$$\frac{d_i}{d_1} = \left(\frac{P_1}{P_i}\right)^{\frac{1}{n}} \tag{21}$$

where P_i is the ith sensor received power in mW, and P_1 and d_1 are the 1^{st} sensor received power in mW and distance. Since d_i can be expressed in x and y coordinates

using 22, this can be substituted into 21 to obtain 23.

$$d_i = \left(\left(x_i - x\right)^2 + \left(y_i - y\right)^2\right)^{1/2} \tag{22}$$

$$\left(\frac{P_1}{P_i}\right)^{\frac{1}{n}} = \left(\frac{\left(x_1 - x\right)^2 + \left(y_1 - y\right)^2}{\left(x_i - x\right)^2 + \left(y_i - y\right)^2}\right)^{1/2} \tag{23}$$

where x_1 and textity$_1$ are the 1^{st} sensor coordinates, x_i and textity$_i$ are the ith sensor coordinates, and x and y are the source coordinates. Rearranging 23, and making $S = x^2 + y^2$ results in 24.

$$\begin{aligned} 2\left(P_1^{2/n}x_1 - P_i^{2/n}x_i\right)x + 2\left(P_1^{2/n}y_1 - P_i^{2/n}y_i\right)y + S\left(P_i^{2/n} - P_1^{2/n}\right) \\ = P_1^{2/n}\left(x_1^2 + y_1^2 big\right) - P_i^{2/n}\left(x_i^2 + y_i^2\right) \end{aligned} \tag{24}$$

Equation 24 is in the form of a classical linear system, $A\theta = b$, and can therefore be resolved, using Equations 25, 26 and 27, to obtain values for x and y.

$$A = \begin{bmatrix} 2\left(P_1^{2/n}x_1 - P_2^{2/n}x_2\right) & 2\left(P_1^{2/n}y_2 - P_2^{2/n}y_i\right) & P_2^{2/n} - P_1^{2/n} \\ \cdots & \cdots & \cdots \\ 2\left(P_1^{2/n}x_1 - P_i^{2/n}x_i\right) & 2\left(P_1^{2/n}y_1 - P_i^{2/n}y_i\right) & P_i^{2/n} - P_1^{2/n} \end{bmatrix} \tag{25}$$

$$\theta = \begin{bmatrix} x \\ y \\ S \end{bmatrix} \tag{26}$$

$$b = \begin{bmatrix} P_1^{2/n}\left(x_1^2 + y_1^2 big\right) - P_2^{2/n}\left(x_2^2 + y_2^2\right) \\ \cdots \\ P_1^{2/n}\left(x_1^2 + y_1^2 big\right) - P_i^{2/n}\left(x_i^2 + y_i^2\right) \end{bmatrix} \tag{27}$$

where P_2, x_2 and y_2 are the 2^{nd} sensor received power in mW and coordinates. It should be noted that no additional processing was performed to compensate for the propagation environment; and therefore, improve the location estimation accuracy. This was to ensure any difference between the difference measurement techniques was not corrected; and therefore, any error was evident. In an actual deployed PD system, the propagation environment would be compensated for by using a more advanced location algorithm [143–145]. The location estimation test for the TRI was performed by forming a 6 position 5 m by 5 m grid of sensor positions, shown in Figure 6-11, with Node 1 being set as the origin.

The HVPD calibrator was set to 10 nC and placed at coordinates of approximately 3.15 m and 1.79 m. The output of the LNA, detector and TRI were then sampled at a rate of 2 GS/as using a DSO. The energies for each measurement were then calculated as done previously, using Equations 18, 19 and 20. A MATLAB script

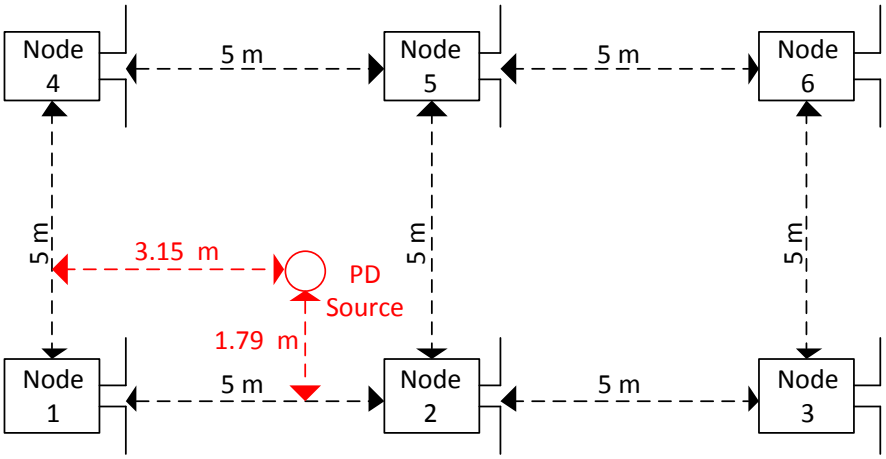
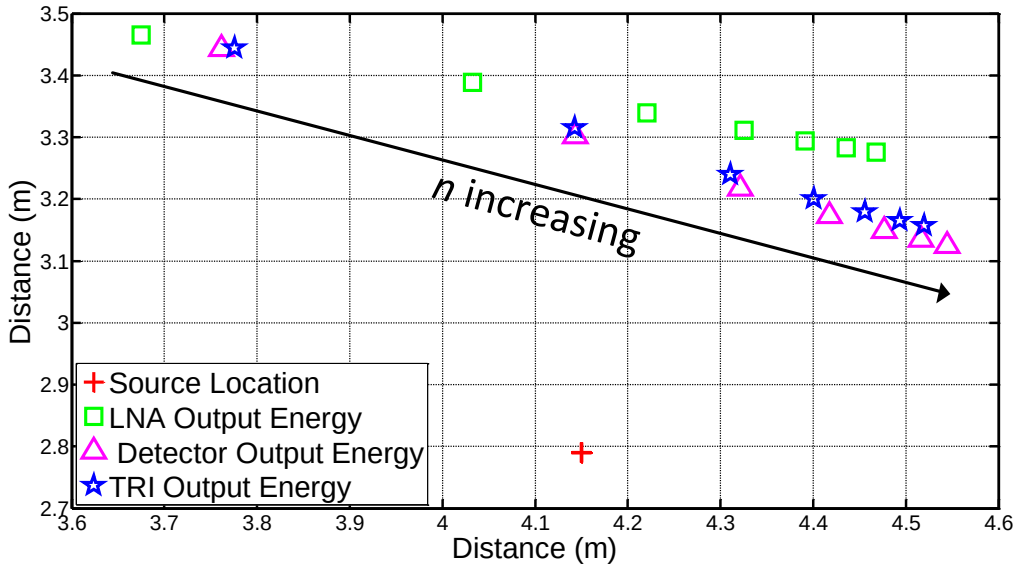


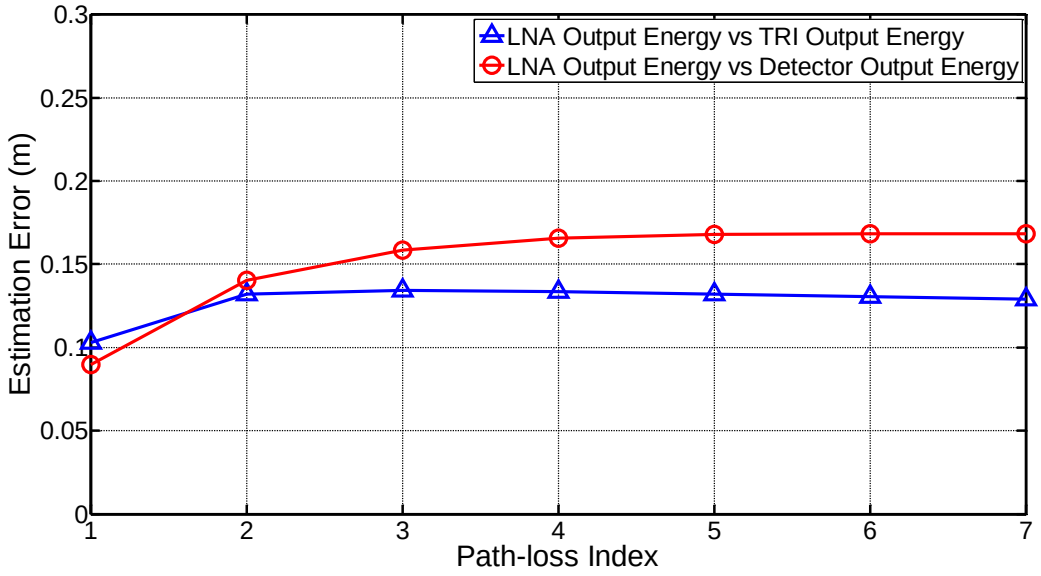
Figure 6-11: Outdoor PD Localization Test Sensor Layout [132]

was created, based around Equations 25, 26 and 27, to perform the location estimation. Since the received energy is the integral of the received power, the calculated energies were directly inputted into the location algorithm.

The path-loss index was adjusted from 1 to 7 and location estimation was calculated for each value of n. The PD calibrator was then increased to 100 nC and the test was repeated. Figure 6-12a shows the calculated localization for the 10 nC source, and Figure 6-13a shows the calculated localization for the 100 nC source (see Appendix A for the MATLAB code). The error between the sampled LNA output, sampled detector output and TRI localization estimations are shown in Figures 6-12b and 6-13b for 10 nC and 100 nC results respectively

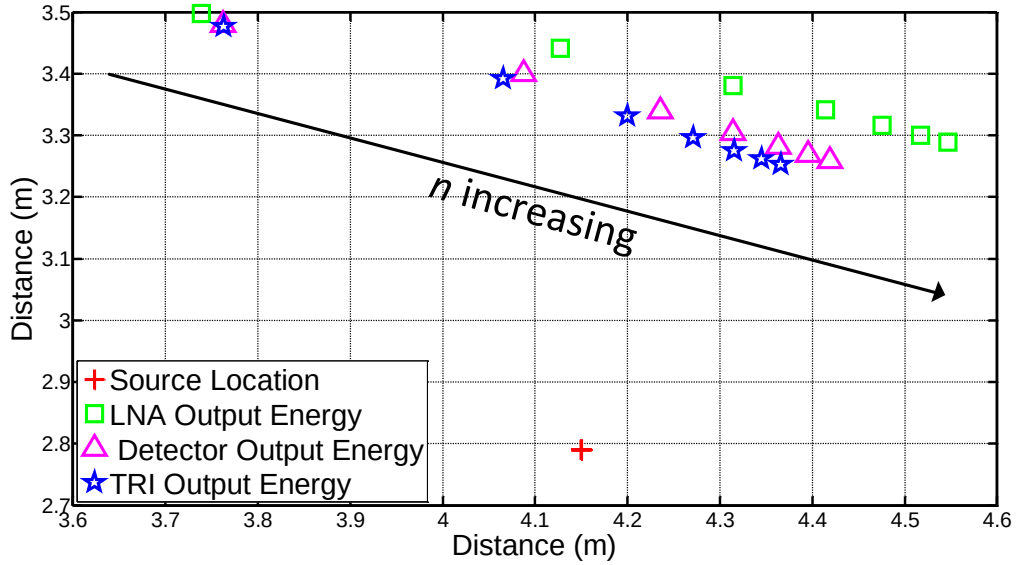


(a)

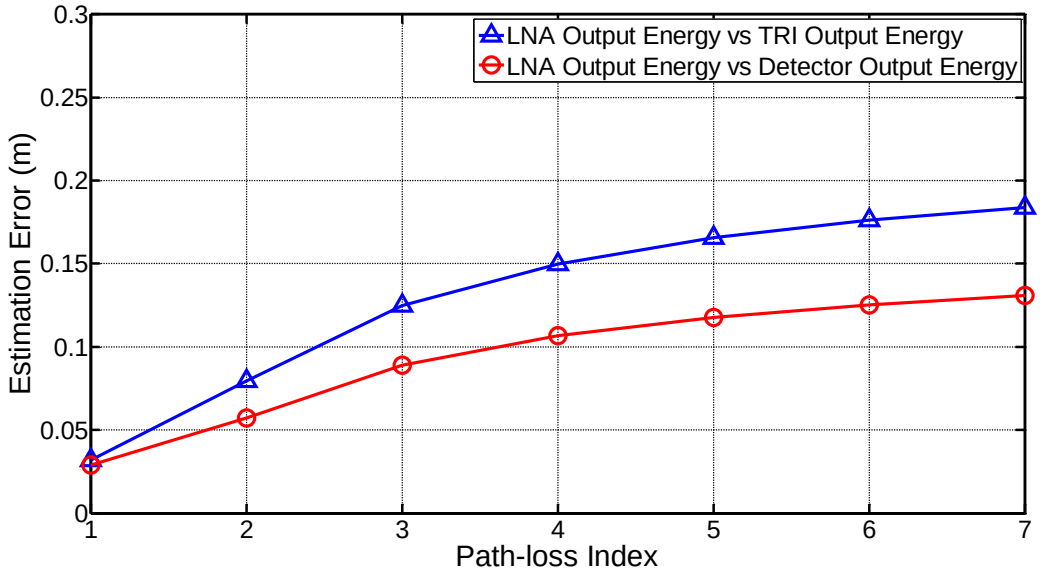


(b)

Figure 6-12: PD Localization for the 10 nC source [132], (a) Location Estimation, and (b) error vs path-loss index



(a)



(b)

Figure 6-13: PD Localization for the 100 nC source, (a) Location Estimation, and (b) error vs path-loss index

Referring to Figures 6-12a and 6-12b, the estimation error is 55 to 83 cm, 46 to 76 cm and 48 to 75 cm between the sampled LNA output, sampled detector output and TRI output respectively, and the actual PD source location. However, the error in distance between the sampled LNA output energy and the TRI energy is between only 10 and 13 cm, whilst the error between the sampled LNA output energy and the sampled detector output energy is between 9 and 17 cm. With a path-loss index of 2 the sampled LNA energy, and the TRI and sampled detector energies is 13 and 14 cm respectively. These errors are minimal in contrast to the errors between each measurement technique and the PD source location.

For the 100 nC location estimation, shown in Figures 6-13a and 6-13b, the estimation error is 61 to 82 cm, 54 to 79 cm and 51 to 79 cm between the sampled LNA output enery, sampled detector output energy and the TRI energy respectively, and the PD source location. Whilst the relative error between sampled LNA output energy, and sampled detector and TRI energies are between 3 to 13 cm and 3 and 18 cm respectively, with errors of 6 and 8 cm for the sampled detector and TRI energies when the path-loss index was set to 2.

6.3 Plausibility of the Folding ADC based System for Radiometric PD Measurement

The folding ADC-based PD monitoring system could not be directly tested for radiometric PD in the same manner as the TRI-based systems owing to a

combination of several factors. Firstly, due to time and resource constraints the folding ADC could not be incorporated into a complete system, therefore, the MCU and wirelessHART sections were not included. Secondly, whilst the logarithmic detector chosen for the system provided greater sensitivity and dynamic range, the increased sensitivity caused the sensor to receive transmitted interference, as well as noise, within the selected measurement bandwidth, even with the inclusion of the band-pass and band-stop filters. Figure 6-14 shows a PD pulse, transmitted from the HVPD calibrator through a 10 dB attenuator, along with the noise present at the output of the AD8310 detector measured within a well shielded laboratory.

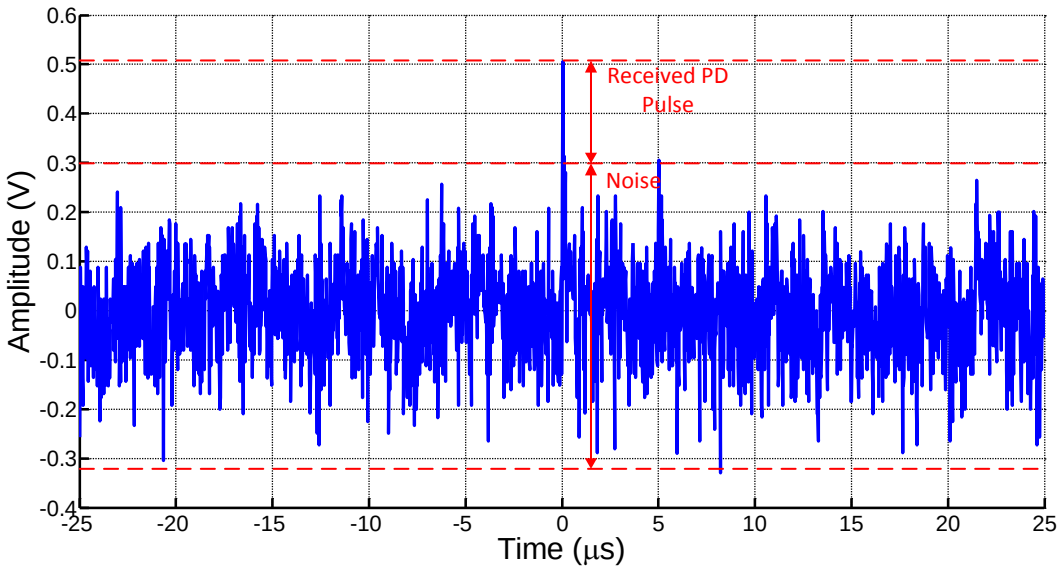


Figure 6-14: Single PD Pulse and Noise at the Output of the AD8310 Logarithmic

The measured noise in Figure 6-14 was 312.75 mVp, with the received PD measured at 516.34 mVp. Therefore, the received PD is only 203.59 mV above the noise. Whilst this could still be received if the comparator threshold voltage was set

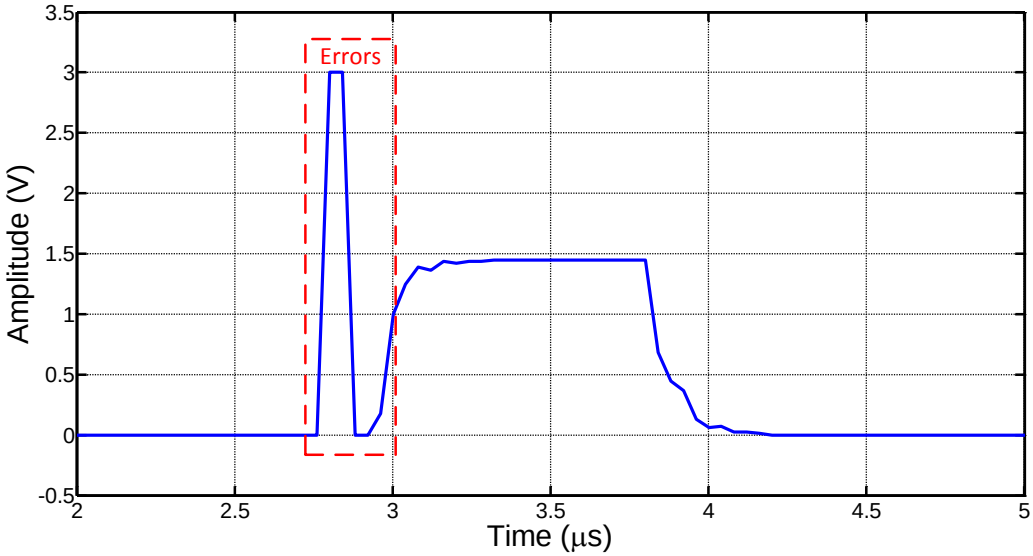


Figure 6-15: Folding ADC Comparator Activated Error

above this noise, any further reduction in the size of the PD signal may cause the received PD signal to be masked by the noise floor of the sensor. Furthermore, in an outdoor environment transmitted interference would likely cause issues also, as even though the RF filters provide attenuation to these signals they may appear at the detector output due to the high sensitivity of the detector.

A further issue is that the comparator activated sample control did not operate as accurately as intended, causing multiple false samples at the output of the ADC when sampling was triggered. Figure 6-15 shows an example of this error from a digitized square-wave pulse input.

The error occurs at the start of the pulse, with multiple full-scale and zero codes being outputted before correct data. These codes cannot just be ignored, as they

are not additional to the correct codes, but have actually replaced the first five or more correct codes. The reason for this error is unclear, but is likely due to the synchronization of the internal digital logic registers. Although efforts were made to correct this problem, the further development required are beyond the time scales available.

This problem could not be avoided by triggering continuously, due to the repetition rate of the HVPD calibrator source and the available PD emulation cells. The repetition rate of the HVPD calibrator was 400 Hz max, meaning one pulse every 2.5 ms. Since the folding ADC was set to a sample-rate of 25 MSa/s, this resulted in 62,500 samples between each received PD signal.

This causes further issues due to the limitations of the method used to store data within the FPGA before transmitting to the PC via USB. The memory buffer-size that stores data before transmitting it over the TTL-to-USB converter connection is limited to 30,000; therefore, there is a probability that the buffer memory will reset before a received PD signal is sampled, resulting in the ADC missing the PD event. This causes even more difficulty when coupled with the interference present within the selected measurement band, since discerning a received PD pulse from within 30,000 recorded data points is problematic.

Whilst these issues lead to difficulties measuring radiometric PD signals directly, it is still possible to measure PD signals emulated using alternative methods, such as

a function generator or RF burst generator, in order to prove the method is valid for PD detection and measurement. As stated in Section 2.5.1, the radiometric signal propagated from a source of PD bears striking similarities to a classical decaying oscillation, with the function given by Equation 28.

$$V_{PD}(t) = V_{pk} \mathrm{e}^{\frac{-t}{\tau}} \cos \omega t \tag{28}$$

where $V_{PD}(t)$, t and τ are the voltage at time t and time constant of the radiometric PD signal. Envelope detecting this signal removes the frequency content, resulting in Equation 29, and since the detector used is a logarithmic responding type, the output becomes the linear function given by Equation 30.

$$V_{DET}(t) = V_{pk} \mathrm{e}^{\frac{-t}{\tau}} \tag{29}$$

$$V_{LOG}(t) = -\frac{V_{pk} t}{\tau} \tag{30}$$

Equation 30 shows that the output of the detector for an exponentially decaying input function is a linear decaying signal. This is confirmed by the measured PD pulse shown in Figure 6-16, which shows a received radiometric PD signal and the output of the AD8310 logarithmic detector.

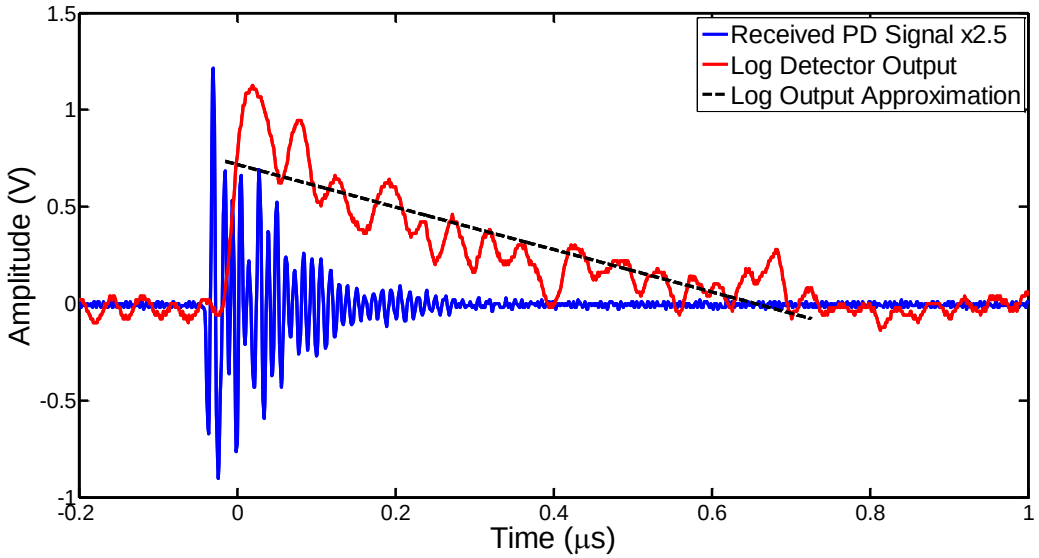


Figure 6-16: Logarithmic Detector Output for a Received PD Signal

Whilst the output of the detector is not a ideal linear decaying ramp, it can be approximated as a straight line, as shown by the black trace in Figure 6-16, and therefore, a linear decay. A further observation that can be taken from Figure 6-16 is that whilst the received PD signal has a time duration of approximately 250 ns, the pulse at the output of the logarithmic detector has a time duration of approximately 800 ns. The reason for this is the extended dynamic range of the detector, which amplifies the low amplitude segment of the signal, as described in Section 3.3. However, since the detector has a sensitivity of approximately 75 dBm any signal below this has no effect on the output; therefore, the received pulse begins to descend into the noise floor of the detector as distance, or attenuation, is increased. This leads to the time duration of the pulse decreasing, along with the number of samples per pulse, as attenuation increases. Figure 6-17 shows the time

duration of an emulated 10 nC radiometric PD pulse, transmitted at a distance of 2 m from the receiver, versus attenuation.

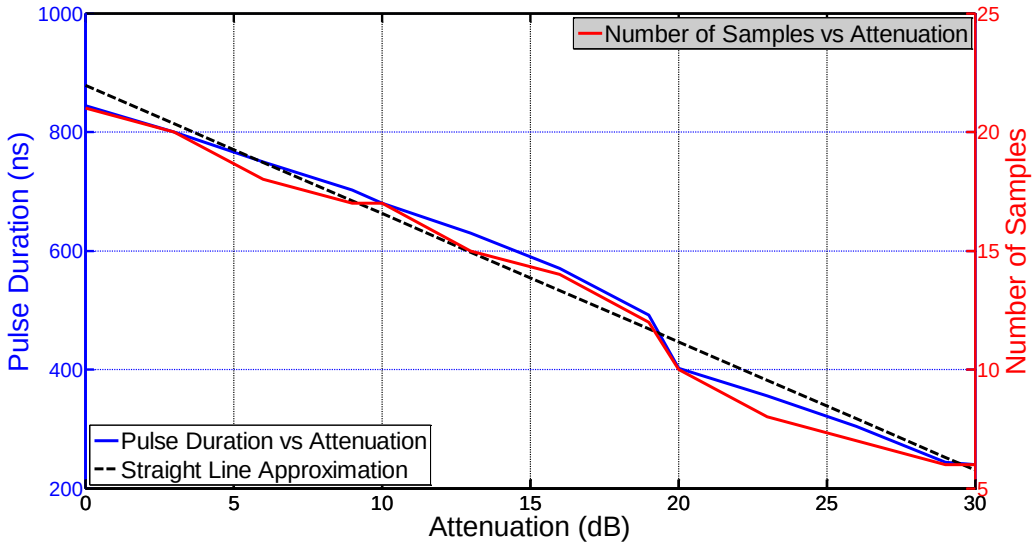


Figure 6-17: AD8310 Detector Pulse Width and Number of Samples versus Received PD Attenuation

The blue trace in Figure 6-17 shows the decrease in pulse duration as attenuation is increased, and is approximately linear with a decrease of 21.6 ns/dB, as shown by the dashed black straight line approximation. The pulse duration at 0 dB is 844 ns, which drops to 240 ns at an attenuation of 30 dB. The number of samples per pulse is based on the sample-rate of 25 MSa/s, and follows a similarly linear decreasing trend as attenuation increases to that of the pulse duration. The number of samples at 0 dB is 21, which should allow for a reasonable accurate measurement of the detected PD pulse. This drops by approximately 1.5 sample per 3 dB to 6 samples at an attenuation of 30 dB. Therefore, the accuracy of the measurement is reduced

as attenuation, or distance, is increased between the radiometric PD source and receiving sensor.

Based on the fact that the logarithmic detected PD pulse can be approximated using a linear decaying pulse, the AD8310 output can be simulated using a similar signal generated via a function generator. Although this signal is not identical to that shown in Figure 6-16, it should provide a good indication of the performance of the folding ADC, along with any errors that are produced by the conversion process. The logarithmic power in dBm of the AD8310 can be obtained through Equation 31.

$$Pi(dBm) = \frac{V_{DET}}{V_{SLOPE}} + P_{INTERCEPT} \tag{31}$$

where V_{DET}, V_{SLOPE} and $P_{INTERCEPT}$ are the detector output voltage, detector transfer slope and intercept power in dBm respectively. V_{SLOPE} is stated as 24 mV/dB typically on the datasheet, although the average value was measured at 21.73 mV/dB experimentally. Using the measured value $P_{INTERCEPT}$ can be calculated from Equation 32.

$$P_{INTERCEPT} = P_{I(MID)} - \frac{V_{O(MID)}}{V_{SLOPE}} \tag{32}$$

where $P_{I(MID)}$ and $V_{O(MID)}$ are the midpoint input power in dBm and the midpoint output voltage. With a midpoint input power and output voltage of -40.16

dBm and 1.1422 V, $V_{INTERCEPT}$ was calculated to be -92.72 dBm. Using these values, the power of each sample point and the total energy can be obtained using Equations 33 and 34.

$$P_{S(i)} = \frac{\left(\frac{V_{DET}}{A_{V(NI)}} + V_{DET(OFFSET)}\right)}{V_{SLOPE}} + P_{INTERCEPT} \tag{33}$$

$$E_{S(i)} = E_{S(i-1)} + \Delta T \sum_{i=1}^{n} 10^{\frac{P_{S(i)}}{10}} \tag{34}$$

where $P_{s(i)}$, $A_{V(NI)}$ and $V_{DET(OFFSET)}$ are the power in dBm at sample point i, the NI amplifier gain respectively, and $E_{S(i)}$, $ES(i-1)$ and n are the total energy at sample point i, total energy at the previous sample and the total number of samples respectively. $V_{DET(OFFSET)}$ is approximately 0.5 V and $A_{V(NI)}$ was set to a value of 1.6 in order to scale the output of the detector to the full input range of the folding AD. The maximum power value was set to 0 dBm, corresponding to a V_{DET} value of 2.3 V, which is 1.8 V when DC decoupled as $V_{DET(OFFSET)}$ is subtracted from it. The simulated logarithmic detector acquisition was performed using the test configuration in Figure 6-18.

A function generator was set to produce a linear decaying ramp, with a starting peak height of 2.88 V, representing a 1.8 V peak (0 dBm) signal before the NI amplifier, and a starting time duration of 810 ns. The peak voltage of the function

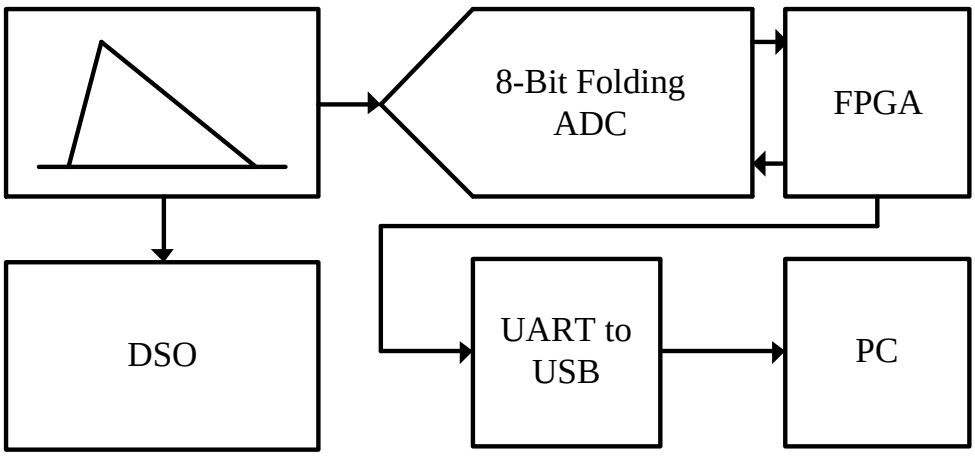
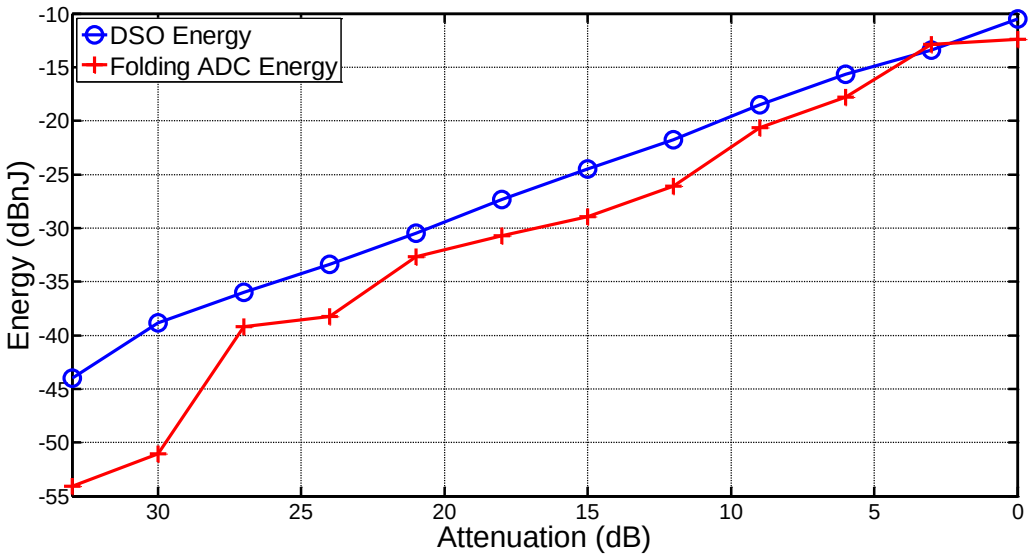


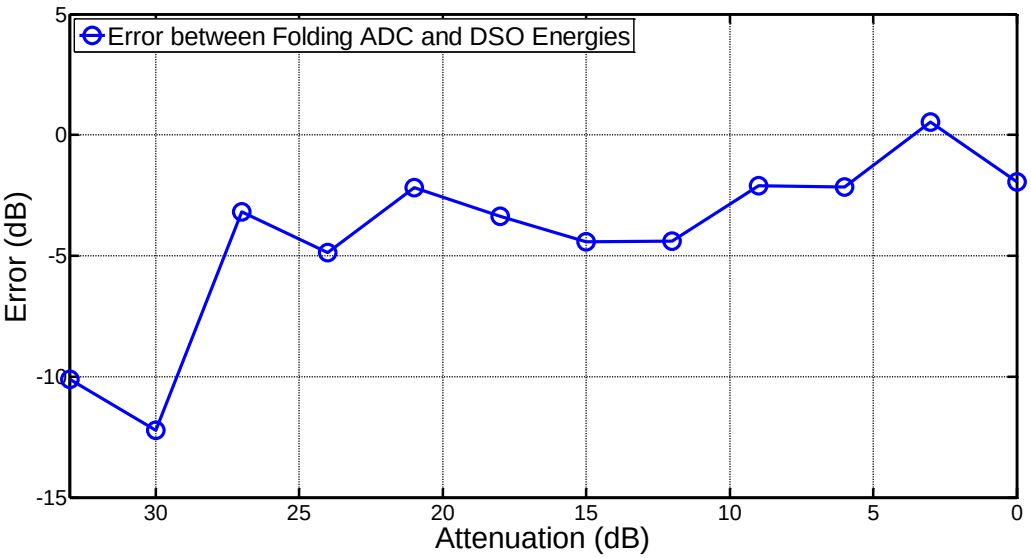
Figure 6-18: Simulated Logarithmic Detector Folding ADC Data Acquisition Test Configuration

generator was decreased in increments of 104.31 mV to emulated a decrease of 3 dB at the input of the detector. Furthermore, the pulse duration was decreased by increments of 64.8 ns between each measurement to reproduce the effect of attenuation to the width of the AD8310 output. The function generator output was sampled by the folding ADC, along with a DSO at a rate of 2 GSa/s to ensure a very high accuracy. Equations 33 and 34 were used to calculate the energy of the signals acquired by the DSO and folding ADC. Figure 6-19a shows the calculated energy of the DSO and folding ADC measurements (see Appendix A for the MATLAB code), whilst 6-19b shows the error between the two calculated energies.

Referring to Figure 6-19b, the error between the energy calculated from the DSO and folding ADC is within 2.2 dB from attenuations of 0 to 9 dB, beyond this the



(a)



(b)

Figure 6-19: DSO and Folding ADC Measurements for a Simulated AD8310 Source, (a) at Attenuations of 0 to 33 dB, and (b) Errors between DSO and Folding ADC energies

error begins to increase, but is within 5 dB up until an attenuation of 30 dB, where the error drastically increases to 12.22 dB. The error then reduces to 10.11 dB at an attenuation of 33 dB. The main source of the error is the reduced number of samples as the pulse duration is decreased with an increase in attenuation, with the pulse width starting at 810 ns and ending at 97.2 ns at an attenuation of 33 dB. Therefore, the number of samples decreases from approximately 20 at 0 dB to 2 at 33 dB.

Even though the error is greater than that of the TRIs presented in the previous sections, it is still an encouraging result, showing that samples obtained by the folding ADC can be used to process the logarithmic detected received PD signal with an error that remains moderately consistent over the attenuation range. Even though the accuracy of the folding ADC is hindered by the sample-rate limit, the theoretical peak voltage of the AD8310 detector output would extend to attenuations that are at least a factor of two greater than 33 dB, with the peak value at 33 dB being only 1.73 V. Therefore, this extended dynamic range would allow greater sensitivity and measurement distances, although higher sample-rates would be required to ensure the ADC was capably of measuring this increased sensitivity with reasonable accuracy.

6.4 Conclusion

The results presented in this chapter demonstrate that each of the three proposed radiometric PD signal conditioning techniques are capable of receiving and processing radiometric PD signal with the following properties:

- The standard TRI can process radiometric PD with an accuracy within ±2 dB. Using the HSMS-2850 based zero-bias detector the standard TRI can measure a radiometric PD source of approximately -2.5 dBnJ strength up to an attenuation of 19 dB. Using the LTC5507 detector this is extended to an attenuation of 23 dB, although the accuracy of the LTC5507 detector would vary greatly depending on the bandwidth of the received PD envelope.

- The composite TRI was able to process the same PD source up to an attenuation of 23 dB with an error within ±1 dB. The composite TRI was able to measure a 10 nC and 100 nC emulated source of PD over a distance of 10 m. The error between the composite TRI output energy and that obtained through high speed sampling were within 1 dB beyond a distance of 4 m for the 10 nC source, but increased as the source became closer to the sensor node. This error increased slightly with the 100 nC source, with a maximum error of 5.1 dB. However, this error was due to the zero-bias detector deviating from a square-law to a linear response. The composite TRI was used to locate an emulated source of PD within a 6 node network, with location estimations for PD strengths of both 10 nC and 100 nC sources within 17 cm and 13 cm respectively of the estimation performed using high-speed sampling.

- Whilst the folding ADC based system was not completed, nor was it tested using emulated PD sources due to technical and time restrictions, the ADC was tested with a simulation approximating the output of a logarithmic detector for a received radiometric PD signal. The results of which indicated potential for the use as a radiometric PD sensor, with an error within 5 dB up to an attenuation of 27 dB, increasing to 12.22 dB at an attenuation of 33 dB. The main source of error is due to the decreasing number of samples per pulse as the pulse duration decreases with attenuation. However, this error can be reduced with an increased sample-rate.

- The standard TRI and the folding ADC based systems feature similar power consumption, at 97.5 mW and 101.1 mW respectively, whilst the the composite TRI is considerably lower at 27.1 mW. However, the folding ADC provides higher sensitivity since a logarithmic detector is used. Although a logarithmic detector could be used with the TRIs the resulting output would not easily be related to the energy of the received PD signal making potential diagnostics difficult. The TRIs are complete systems and are easily implemented, whilst the folding ADC requires further development to incorporate it into a fully functioning PD detection system. Even after further development the folding ADC is likely to consume significantly more power than the composite TRI.

The following chapter will discuss and compare the obtained results for each signal processing technique.

7 Discussion

The three measurement systems proposed have been specifically designed to detect and measure radiometric PD, with each technique providing advantages and limitations in comparison to the other systems. The main differences being concerned with power consumption, sensitivity, dynamic range and accuracy, the latter with respect to absolute measurement and location estimation. The two TRI implementations are based on the same principle, to avoid the requirement for high-speed data acquisition, and therefore, high power consumption and data processing, whilst the folding ADC based system is designed to sample only when a signal is received.

The two variants of the TRI are almost identical in operation and system level design. However, the circuit level design of the composite TRI has been developed to overcome many of the limitations of the standard TRI, such as power consumption, speed and accuracy. The standard TRI utilizes high-speed precision components, which provides reasonable accuracy and speed, but requires higher levels of power consumption than are ideal. Most of this power is consumed by the high-speed components required, including the NI amplifier and precision high-speed comparator. The NI amplifier is based around a 250 MHz bandwidth CMOS device, which consumes a maximum of 7.5 mA of quiescent current. This specific op-amp is not a precision type; therefore, it may produce an offset error up to ± 8 mV max, with a typical offset of ± 2 mV. Whilst the offset voltage drift is only typically ± 4 μV/$\circ$C, the main offset voltage requires care to ensure

that the offset does not cause the comparator to trigger, enabling the TRI when no signal is present. Therefore, a -3 mV DC bias voltage is applied to the input of the NI amplifier to ensure the offset is below the comparator threshold level.

This requirement for a DC bias reduces the minimum signal amplitude that can be processed by the TRI, and therefore, the sensitivity of the sensor. The LTC5507 detector provides an increase of approximately 4 dB in sensitivity compared to the HSMS-2850 based zero-bias detector, but is limited by a bandwidth and slew-rate below that of the received PD signal envelope, causing potential errors to the measurement of the received energy. The TRI itself is based around a precision op-amp, with an offset error of of 7 μV typically 25 μV max, a bandwidth of 18 MHz and a quiescent current 1.1 mA max. Although this op-amp ensures minimal drift to the output of the TRI between pulses, it is limited by the 18 MHz bandwidth, which causes further errors, although minor, particularly at larger input signal.

The composite TRI alleviates many of these problems, particularly the power consumption and speed. The use of multiple amplifier elements allows for the composite NI amplifier to obtain DC accuracy of approximately -6 μV over a temperature range of -20 $\circ$C to +40 $\circ$C, which is more than adequate for correct operation in an outdoor environment. Since the DC accuracy of the NI amplifier is controlled to within $\pm$20 μV, it will never cause false triggering of the comparator; therefore, no bias voltage is required and the sensitivity of the TRI is increased, which can be noted from Figure 6-8, where the accuracy of the composite TRI

extends to an attenuation of 23 dB with an error within -2 dB, compared to an error of approximately -15 dB for the standard TRI.

The outdoor distance tests conducted with the composite TRI for the 10 nC emulated PD source gave measurements well within a dB between a distance of 4 to 10 m, with an increased error up to approximately 3 dB below 4 m. This error increased for the 100 nC source, with the maximum error increased to approximately 5 dB. This error is due to the HSMS-2850 zero-bias detector diverging from a square-law to a linear response, and increases with an increase in received power. The error, therefore, is not a result of a design flaw with the TRI, and can be improved by selecting a detector with a higher dynamic range and square-law response. A difficulty with acquiring such a detector is that they are predominantly designed for continuous AC signals, and do not feature bandwidths capable of accurately following the true envelope of a radiometric PD signal. Therefore, a custom implementation may have to be realized to provide the extended dynamic range along with the bandwidth required.

The maximum distance the composite TRI was able to measure the 10 nC PD source was also limited by the HSMS-2850 zero-bias detector, to a distance of approximately 10 m. Whilst this distance only allows for the minimum requirement of a 10 m spacing between nodes, the reduced cost of the node due to the Schottky diode based detector and composite circuit design alleviate the requirement for wider spacing between nodes, since the main purpose of this requirement is to

minimize the overall cost of the sensor network. The location estimation tests performed using the composite TRI-based sensor were close to those obtained through direct high-speed sampling, with a maximum error of 13 cm for 18 cm for the 10 nC and 100 nC PD sources respectively. Whilst the error between the location estimations and the actual PD location were up to 83 cm, the main cause of this error is not due to the TRI, but to the propagation environment in which the measurements were taken, along with the accuracy of the location algorithm utilized.

The folding ADC based system should allow for a radiometric PD source to be measured over a greater distance than the TRI based systems, since a logarithmic detector is utilized in place of the square-law types. Although the folding ADC based system could not be used to detect and measure radiometric PD signals directly, the results provided by simulating the response of an AD8310 detector to a typical PD signal provide a good indication that the system will be capable of radiometric PD measurement, with errors between 2 dB and 5 dB below an attenuation of 27 dB. The inaccuracies in the simulated measurements are primarily due to the pulse duration of the detected PD signal decreasing as attenuation increases. Since the sample-rate of the detector is fixed at 25 MSa/s the number of samples per pulse decreases by approximately 1.5 for every 3 dB in attenuation. The accuracy and dynamic range could be extended by increasing the sample-rate of the folding ADC, which would require modifications to the architecture for wider bandwidth and slew-rate.

8 Conclusion and Further Work

8.1 Conclusion

The main conclusions taken from this thesis are as follows:

1. Two main low power signal processing techniques have been investigated which alleviate the power requirements necessary with traditional high-speed data acquisition systems, and therefore, ensure that the sensors can operate for an extended duration without replacing the power source.

2. A TRI-based system has been proposed that completely removes the requirement for high-speed sampling to be used; therefore, removing the need for high power consumption and large data processing. Each received PD signal is integrated to a DC level requiring only one sample per event, reducing the required sample-rate well below 100 kSa/s.

3. A folding ADC-based system has been proposed which is designed to only sample when a signal is present; therefore, reducing the required power consumption in between received PD events to the total static quiescent current of the internal devices, significantly lowering the power dissipation compared to that used when sampling. Furthermore, the system allows for a logarithmic detector to be incorporated, increasing the sensitivity and dynamic range of the sensor.

4. Composite amplifier techniques have been implemented to allow for circuitry which features specifications of low DC offset voltage error, low

power consumption, high-input impedance and high-speed, which a single commercially available amplifier would not be capable of matching.

5. Two TRI variants have been developed, of which the composite TRI provides many benefits over the standard version, Including power consumption a factor of 3.9 lower and a bandwidth approximately 4 times higher, along with a higher sensitivity when receiving radiometric PD.

6. The composite TRI has demonstrated an acceptable accuracy when measuring radiometric PD over a distance of 10 m, with the majority of errors incurred due to the zero-bias detector used. However, the distance was acceptable considering the reduced cost of the sensor when using composite circuit design compared to precision high-speed components.

7. The location estimation obtained using the composite TRI have an accuracy within 1 m to the original PD source location. However, the error between the location estimation calculated using the TRI output energy and the energy derived from high-speed sampling is negligible, at a value below 20 cm.

8. The folding ADC-based system shows potential as a low power technique for radiometric PD detection and measurement, with an accuracy between 2 dB and 5 dB when measuring a simulated logarithmic detected PD source. Although much further work is required, the folding ADC provides a simple data conversion technique that allows for a faster enable time compared to traditional commercially available ADCs, providing an ideal data acquisition technique for radiometric PD.

8.2 Further Work

The following is a list of suggestions to improve the techniques presented in this thesis:

- The potential interference within the selected measurement band poses several problems for distinguishing PD faults from other transmission sources. Therefore, a technique for discerning frequency spectra of the measurement band would allow the ability to distinguish between these signals, as well as providing potential diagnostic information for the PD fault. A traditional swept heterodyne receiver, such as those used in spectrum analyzers, is not ideal since radiometric PD only has a duration of hundreds of nanoseconds to microseconds. Therefore, a stepped heterodyne receiver would provide a more flexible solution, where the receiver could be set at a specific frequency for as long a duration as required, and bands containing interference could be bypassed.

- The TRI-based systems are limited by the dynamic range of the HSMS-2850 detector, whilst the LTC5507 detector has insufficient bandwidth to accurately track the true envelope of the PD signal, leading to potential errors in measurement. Therefore, a bespoke detector designed specifically for radiometric PD would provide higher dynamic range along with higher bandwidth. Ideally, the detector would include AGC controlled pre-amplification in order to limit the signal amplitude to the square-law range of the detector. With multiple switchable gains the dynamic range of the detector could be significantly extended.

- The performance of the folding ADC could be significantly improved if integrated onto monolithic silicon. A simpler, transistor-based, configuration would provide lower power consumption, higher bandwidth and potentially higher resolution. A fully differential implementation should significantly reduce the noise, as well as improving the linearity of the converter. Furthermore, digital correction logic could be included to improve the linearity of the converter.

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Appendices

A MATLAB Codes

Code for calculating the DNL and INL of the folding ADC:

```
N = 254;
binranges = 1:254;
bin = linspace(1,254,254);

Dout = zeros(87164,1);
DNL = zeros(N,1);

FileName = ['8BITHIST'];
sheet = 6;
Dout = xlsread(FileName,sheet,'B1:B87164');
H = histc(Dout,binranges);
Davg = mean(H);

for i=1:N

    DNL(i) = (H(i)/Davg)-1;

end

INL = cumsum(DNL);
plot(bin,DNL,'linewidth',5) %Change DNL to INL for
                            %Integral Non-Linearity

grid on

set(gca, 'box', 'on')
set(gca,'FontSize',35,'LineWidth',4)
xlim([1,254])

xlabel('output code','FontSize',35);
ylabel('DNL, LSB','FontSize',35);
```

Code for generating the Folding ADC 3D Input Noise Graphs:

```
Dout = zeros(100000,21);


FileName = ['Grounded_Histograms'];
sheet = 7;
Dout = xlsread(FileName,sheet,'B3:V10003');

xbins = [120:1:131];
h = hist(Dout,xbins,2);

grid on

```

```
b = bar3(xbins,h)

set(b,'FaceAlpha',0.5)

% set(b,'FaceAlpha',0.15,'FaceColor',[1 1 1]*0.9)
set(gca,'fontsize',10,'linewidth',2.5);
xlabel('Input Voltage (V)','FontSize',25);
ylabel('Output Code','FontSize',25);
zlabel('Counts','Fontsize',25);
```

Code for performing an FFT function on the folding ADC digital output:

```
Ts = 4E-008;
Fs = 1 / Ts;
N = 8192;
count = 0;

Bin = Fs/N;
x = zeros(N,1);
vout1 = zeros(N,1);
Dout1 = zeros(N,1);

FileName = ['FFT_845kHz_25MSps_NF'];
sheet = 5;
Dout1 = xlsread(FileName,sheet,'B1:B8192');

for i=1:N-1

    x(i+1,1) = x(i,1)+Bin;
    vout1(i,1) = (3/((2^8)-1))*Dout1(i,1);

end

voff = mean(vout1);

for i=1:N

    vo1(i,1) = vout1(i,1)-voff;

end

X1 = zeros(N,1)

for k=1:N-1
    for n=1:N-1
        X1(k+1) = X1(k+1)+vo1(n+1)*exp(-j*2*pi*n*k/N);
    end
end

maxmag1 = max(X1);
Dout_dB1 = 20*log10(abs(X1/maxmag1));

plot(x,Dout_dB1,'linewidth',3);
maxdB = max(Dout_dB1(1:N/2))

grid on

```

```
xlabel('Frequency (MHz)','FontSize',35);
ylabel('Amplitude (dB)','FontSize',35);

set(gca, 'box', 'on')
set(gca,'FontSize',35,'LineWidth',4)
```

Code to calculate the LNA output, detector output and TRI otuput energies:

```
format long

R = 100;
C = 10E-009;
K = 1/184.6;

T = 0.5E-009;
n = 1999;

Vrf = zeros(n,1);
Vdet = zeros(n,1);
Vint = zeros(n,1);
VintOfst = zeros(296,1);

Prf = zeros(n,1);
Pint = zeros(n,1);
Vdetint = zeros(n,1);
t = zeros(n,1);

FileName = ['PD_23dB.csv']
t = xlsread(FileName,'A4:A2002');
Vrf = xlsread(FileName,'B4:B2002');
Vdet = xlsread(FileName,'C4:C2002');
Vint = xlsread(FileName,'D4:D2002');
VintOfst = xlsread(FileName,'D4:D200');

Voffset = mean(VintOfst);
Vrfmag = abs(Vrf);
Vint(1) = (K*R*C*(Vint(1)-Voffset))/6.4;

for i=1:n-1


    Prf(i) = (Vrfmag(i)^2)/50;
    Pint(i+1) = (Pint(i) + T*Prf(i));

    if Vdet(i) >= 0.0008
        Vdetint(i+1) = (Vdetint(i) + ((K*T*Vdet(i))));
    else
        Vdetint(i+1) = Vdetint(i);
    end

    Vint(i+1) = (K*R*C*(Vint(i+1)-Voffset))/6.4;

end

Pi = max(Pint)-min(Pint)
Vdi = max(Vdetint)-min(Vdetint)
```

```
Vi = max(Vint)
Vif = max(VintF)

hold on

plot(t,Pint,'b','Linewidth',4)
plot(t,Vdetint,'k','Linewidth',4)
plot(t,Vint,'r','Linewidth',4)

xlabel('Time (\mus)','FontSize',35);
ylabel('Energy (pJ)','FontSize',35);
set(gca,'box','on');
set(gca,'FontSize',25,'linewidth',3);

Leg = legend('LNA Output Integral','Detector
 Output Integral','TRI Output','Location','Southeast')
set(Leg,'FontSize',35);
```

Code to perform and plot the basic location algorithm:

```
X = [1,1; 6,1; 11,1; 1,6; 6,6; 11,6];
index=7;
n=size(X,1);

R = zeros(n,1);
Rdet = zeros(n,1);
Rint = zeros(n,1);

FileName = ['Loc_4_Energies']
R = xlsread(FileName,'A3:A9');
Rdet = xlsread(FileName,'B3:B9');
Rint = xlsread(FileName,'C3:C9');


for i= 1:n
    P(i,1) = 10^(R(i)/10);
    Pdet(i,1) = 10^(Rdet(i)/10);
    Pint(i,1) = 10^(Rint(i)/10);
end

for i = 1:n-1

A(i,1) = 2 * ( P(i)^(2/index)*X(i,1) -
                                  P(n)^(2/index)*X(n,1) );
A(i,2) = 2 * ( P(i)^(2/index)*X(i,2) -
                                  P(n)^(2/index)*X(n,2) );
A(i,3) = P(n)^(2/index) - P(i)^(2/index);
b(i,1) = P(i)^(2/index)*( X(i,1)^2 + X(i,2)^2 ) -
P(n)^(2/index)*( X(n,1)^2 + X(n,2)^2 );
end

for i = 1:n-1

Adet(i,1) = 2 * ( Pdet(i)^(2/index)*X(i,1) -
        Pdet(n)^(2/index)*X(n,1) );
Adet(i,2) = 2 * ( Pdet(i)^(2/index)*X(i,2) -
```

```
                    Pdet(n)^(2/index)*X(n,2) );
Adet(i,3) = Pdet(n)^(2/index) -
                    Pdet(i)^(2/index);
bdet(i,1) = Pdet(i)^(2/index)*( X(i,1)^2 + X(i,2)^2 ) -
                    Pdet(n)^(2/index)*( X(n,1)^2 + X(n,2)^2 );
end

for i = 1:n-1

Aint(i,1) = 2 * ( Pint(i)^(2/index)*X(i,1) -
                    Pint(n)^(2/index)*X(n,1) );
Aint(i,2) = 2 * ( Pint(i)^(2/index)*X(i,2) -
                    Pint(n)^(2/index)*X(n,2) );
Aint(i,3) = Pint(n)^(2/index) - Pint(i)^(2/index);
bint(i,1) = Pint(i)^(2/index)*( X(i,1)^2 + X(i,2)^2 ) -
                    Pint(n)^(2/index)*( X(n,1)^2 + X(n,2)^2 );
end

    Y = A\b;
    Ydet = Adet\bdet;
    Yint = Aint\bint;


x = 4.15;
y = 2.79;

de = sqrt((x-Y(1,1))^2+(y-Y(2,1))^2)
dedet = sqrt((x-Ydet(1,1))^2+(y-Ydet(2,1))^2)
deint = sqrt((x-Yint(1,1))^2+(y-Yint(2,1))^2)

plot(x,y,'r+','markers',25,'linewidth',4)

hold on
grid on

plot(Y(1,1),Y(2,1),'gs','markers',25,'linewidth',4)
plot(Ydet(1,1),Ydet(2,1),'m^','markers',25,'linewidth',4)
plot(Yint(1,1),Yint(2,1),'bp','markers',25,'linewidth',4)

xlabel('Distance (m)','FontSize',35);
ylabel('Distance (m)','FontSize',35);

set(gca,'FontSize',25,'linewidth',3);
Leg = legend('Source Location','LNA Output Energy',
'Detector Output Energy','TRI Output Energy',
'Location','Southwest');
set(Leg,'FontSize',35);
```

Code to calculate the high-speed sampled emulated logarithmic detector output and the folding ADC output:

```
format long

t2 = 0;
T1 = 40E-009;
```

```
T2 = 0.5E-009;
n = 1999;
Edso = zeros(n,1);

FileName = ['DSO_SIM_27dB.csv']
t = xlsread(FileName,'A4:A2002');
Vdso = xlsread(FileName,'B4:B2002');

VOS = 0.5;
AV = 1.6;
Vslope = 0.024;
Vintercept = -92.72;

for i=1:n-1

    PdBm(i+1) = (((Vdso(i)/AV)+VOS)/Vslope) + Vintercept;

    Edso(i+1) = Edso(i) + T2*(10^((PdBm(i)-30)/10));

end

Pmax = max(PdBm)
Edsomax = max(Edso)


FileName2 = ['FADC_Simulated_Log_Det_Test']
ADC = xlsread(FileName2,2,'K4:K28');

m = 25;
Eadc = zeros(m,1);

for i=1:m-1

    Vadc(i) = ADC(i)*(3/255);

    PdBm2(i) = (((Vadc(i)/AV)+VOS)/Vslope) + Vintercept;

    Eadc(i+1) = Eadc(i) + T1*(10^((PdBm2(i)-30)/10));

    t2(i+1) = t2(i) + T1;

end

Eadcmax = max(Eadc)

hold on

grid on

plot(t2,Eadc,'b','Linewidth',4)

plot(t,Edso,'r','linewidth',4)

xlabel('Time (\mus)','FontSize',35);
ylabel('Energy (pJ)','FontSize',35);
set(gca,'box','on');
set(gca,'FontSize',25,'linewidth',3);
```

B Bill of Materials for Circuit Designs

Components for each circuit design in Chapter 4 are listed below.

Part ID	**Part Type**	**Part Value**
R_1	Resistor	1kΩ
R_2	Resistor	1kΩ
R_3	Resistor	2kΩ
R_4	Resistor	1kΩ
R_5	Resistor	9kΩ
R_6	Resistor	1kΩ
R_7	Resistor	51kΩ
R_8	Resistor	30kΩ
R_9	Resistor	1kΩ
R_{10}	Resistor	1kΩ
R_{11}	Resistor	100Ω
R_{12}	Resistor	100Ω
R_{13}	Resistor	10kΩ
R_{14}	Resistor	10kΩ
R_{15}	Resistor	10Ω
R_{16}	Resistor	10kΩ
R_{17}	Resistor	20kΩ
R_{18}	Resistor	6.67kΩ
C_1	Capacitor	100 nF

C_2	Capacitor	4.7 nF
C_3	Capacitor	10 nF
C_4	Capacitor	10 nF
Q_1	Transistor	2N7000
Q_2	Transistor	2N7000
U_1	Op-Amp	OPA357
U_2	Op-Amp	LMH6618
U_3	Comparator	LT1719
U_4	Op-Amp	OPA381
U_5	Comparator	LT1716
U_6	Op-Amp	TLV2460

Table B-1: BoM for Figure 4-3

Part ID	**Part Type**	**Part Value**
R_S	Resistor	50Ω
R_L	Resistor	2.7kΩ
C_L	Capacitor	6.8 pF
D_1	Schottky Diode	HSMS-2850
D_2	Schottky Diode	HSMS-2850

Table B-2: BoM for Figure 4-5

Part ID	**Part Type**	**Part Value**

R_1	Resistor	1MΩ
R_2	Resistor	4.7kΩ
R_3	Resistor	2kΩ
R_4	Resistor	1kΩ
R_5	Resistor	2kΩ
R_6	Resistor	1kΩ
R_7	Resistor	1MΩ
R_8	Resistor	1.4kΩ
C_1	Capacitor	330 nF
C_2	Capacitor	300 nF
Q_1	Transistor	BF862
Q_2	Transistor	1/2 DMMT-5551
Q_2	Transistor	1/2 DMMT-5551
U_1	Op-Amp	ADA4807
U_2	Op-Amp	OPA333

Table B-3: BoM for Figure 4-6

Part ID	**Part Type**	**Part Value**
R_{10}	Resistor	1kΩ
R_{11}	Resistor	9kΩ
R_{12}	Resistor	1kΩ
R_{13}	Resistor	51kΩ

R_{14}	Resistor	30kΩ
R_{15}	Resistor	1kΩ
R_{16}	Resistor	1kΩ
C_3	Capacitor	100 nF
C_4	Capacitor	4.7 nF
U_3	Op-Amp	ADA4807
U_4	Comparator	TS3011

Table B-4: BoM for Figure 4-7

Part ID	**Part Type**	**Part Value**
R_{17}	Resistor	100Ω
R_{18}	Resistor	1MΩ
R_{20}	Resistor	10kΩ
R_{21}	Resistor	10kΩ
R_{22}	Resistor	1MΩ
R_{23}	Resistor	10kΩ
R_{24}	Resistor	10kΩ
R_{25}	Resistor	33Ω
R_{26}	Resistor	10kΩ
R_{27}	Resistor	20kΩ
R_{28}	Resistor	6.67kΩ
C_5	Capacitor	10 nF

C_6	Capacitor	330 nF
Q_4	Transistor	BF862
Q_5	Transistor	2N7000
Q_6	Transistor	2N7000
U_5	Op-Amp	AD8031
U_6	Op-Amp	OPA333
U_7	Comparator	TS3011
U_8	Op-Amp	OPA835

Table B-5: BoM for Figure 4-8

Part ID	**Part Type**	**Part Value**
R_1	Resistor	1kΩ
R_2	Resistor	1kΩ
R_3	Resistor	500Ω
R_4	Resistor	500Ω
R_5	Resistor	500Ω
R_6	Resistor	250Ω
C_1	Capacitor	5 pF
C_2	Capacitor	5 pF
S_1	Analogue Switch	1/2 TS5A2066
S_2	Analogue Switch	1/2 TS5A2066
U_1	Op-Amp	ADA4807

U_2	Op-Amp	ADA4807

Table B-6: BoM for Figure 4-12

Part ID	**Part Type**	**Part Value**
R_1	Resistor	470kΩ
R_2	Resistor	470kΩ
R_3	Resistor	235Ω
R_4	Resistor	235Ω
C_1	Capacitor	5 pF
C_2	Capacitor	5 pF
S_1	Analogue Switch	TS5A63157
S_2	Analogue Switch	1/2 TS5A2066
S_3	Analogue Switch	1/2 TS5A2066
U_1	Op-Amp	MAX4412
U_2	Comparator	TS3011

Table B-7: BoM for Figure 4-13

C Diagrams of the Power Supply Circuitry

Power supply circuitry for the standard TRI, all ICs are powered from $+V_{CC}$ = +3 V and $-V_{EE}$ = -3 V, except for the mono-stable which is supplied from $+V_{CC}$ only:

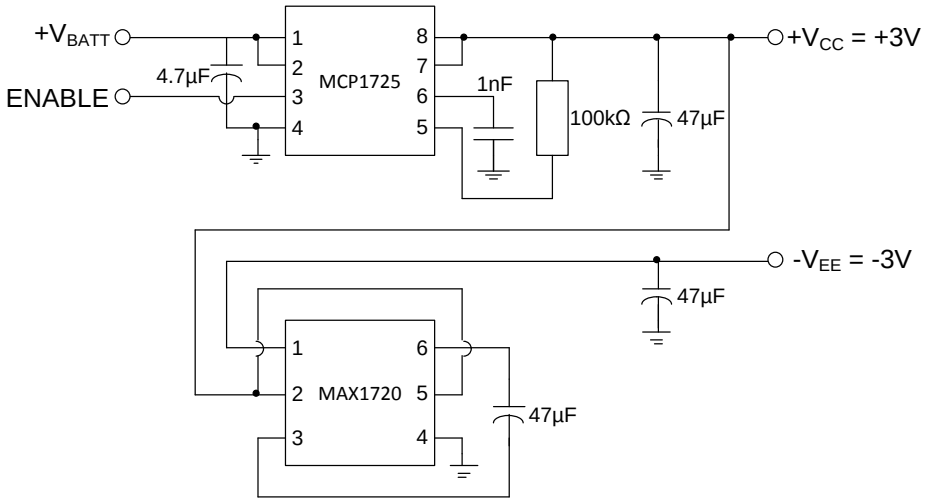

Figure C-1: Standard TRI Power Supply Circuitry

Power supply circuitry for the Composite TRI, ICs U_1, U_2, U_3 and U_8 are power from $+V_{CC}$ to $-V_{SS}$, U_4 is powered from $+V_{CC}$ to ground, U_5 and U_6 are powered from $+V_{DD}$ to $-V_{EE}$, and U_7 is powered from ground to $-V_{SS}$:

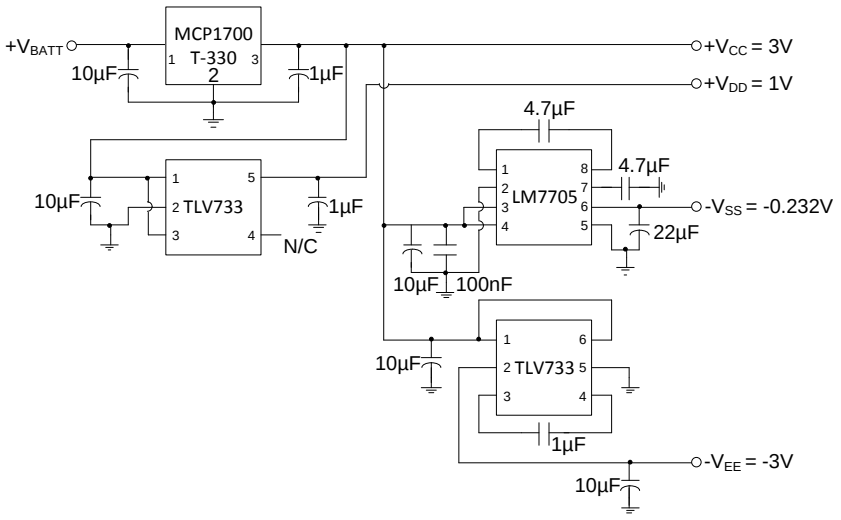

Figure C-2: Composite TRI Power Supply Circuitry

Power supply and reference circuitry for the folding ADC:

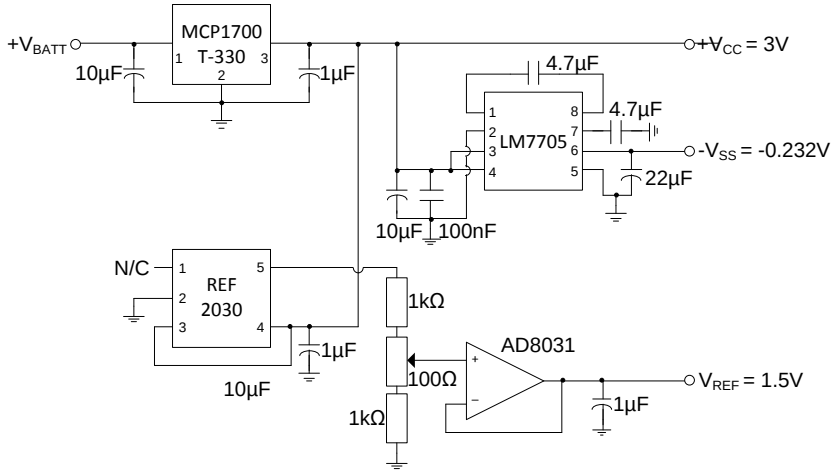

Figure C-3: Folding ADC Power Supply and Reference Circuitry

D List of Publications

Listed below are the manuscripts published during this work. Publications are listed in order of earliest to latest.

- Upton, D. W., Haigh, R. P., Saeed, B. I., Khan, U., Mohamed, H., Mistry, K., Mather, P. J., Lazaridis, P., Torres-Filho, F., Tachtatzis, C., Atkinson, R. C., Judd, M. D. and Glover, I. (2018) Low Power High-Speed Folding ADC based Partial Discharge Sensor for Wireless Fault Detection in Substations, *In: 2nd URSI Atlantic Radio Science Meeting (AT-RASC)*, pp. 1-4.

- Upton, D. W., Saeed, B. I., Mather, P. J., Sibley, M. J. N., Lazaridis, P., Mistry, K. K., Glover, I. A., Filho, F. T., Tachtatzis, C., Atkinson, R. C. and Judd, M. D. (2018) Low Power Radiometric Partial Discharge Sensor using Composite Transistor-Reset Integrator, *IEEE Transactions on Dielectrics and Electrical Insulation*, 25 (3), pp. 1001-1009.

- Upton, D. W., Saeed, B. I., Mather, P. J., Lazaridis, P., Vieira, M. F. Q., Atkinson, R. C., Tachtatzis, C., Garcia, M. S., Judd, M. D. and Glover, I. (2018) Wireless Sensor Network for Radiometric Detection and Assessment of Partial Discharge in High-Voltage Equipment, *Radio Science*, 53 (3), pp. 357-364.

- Haigh, R. P., Upton, D. W., Saeed, Mather, P. J. and Sibley, M. J. N. (2017) Low Power Embedded Processing of Scintillation Events with Silicon Photo Multipliers, *In: 32nd URSI General Assembley and Scientific Symposium (GASS)*, pp. 1-3.

- Upton, D. W., Saeed, B. I., Khan, U., Jaber, A., Mohamed, H., Mistry, K., Mather, P. J., Lazaridis, P., Vieira, M. F. Q., Atkinson, R., Tachtatzis, C., Iorkyase, E., Judd, M. D. and Glover, I. (2017) Wireless Sensor Network for Radiometric Detection and Assessment of Partial Discharge in High-Voltage Equipment, *In: 32nd URSI General Assembley and Scientific Symposium (GASS)*, pp. 1-4.

- Zhang, Y., Upton, D., Jaber, A., Ahmed, H., Khanzada, U., Saeed, B., Mather, P., Lazaridis, P., Atkinson, R., Vieira, M. and Glover, I. (2015) Multiple Source Localization for Partial Discharge Monitoring in Electrical Substation. *In: Loughborough Antennas & Propagation Conference*, 2nd - 3rd November 2015, Loughborough, UK, pp. 1-4.

- Zhang, Y., Neto, J., Upton, D., Khanzada, U., Saeed, B., Ahmed, H., Mather, P., Atkinson, R., Lazaridis, P., Vieira, M. and Glover, I. (2015) Radiometer Monitoring System for Partial Discharge Detection in Substation. *In: International Union of Radio Science Atlantic Radio Science Conference*, 18th - 22nd May 2015, Las Palmas, Gran Canaria, pp. 1-1

- Zhang, Y., Upton, D., Jaber, A., Ahmed, H., Saeed, B., Mather, P., Lazaridis, P., Mopty, A., Tachtatzis, C., Atkinson, R., Judd, M., Vieira, M. and Glover, I. A. (2015) Radiometric Wireless Sensor Network Monitoring of Partial Discharge Sources in Electrical Substations *International Journal of Distributed Sensor Networks*, 2015 (438302), pp. 1-9. ISSN 1550-1329

- Upton, D. W., Mather, P. J., Zhang, Y., Jaber, A., Ahmed, H., Khan, U.,

Saeed, B., Vieira, M. F. Q., Atkinson, R. and Glover, I. A. (2014) 'Signal Conditioning Electronics for UHF Partial Discharge Detection and Location System', *In: UK Festival of Radio Science 2014*, pp. 1-1.