Macromodel Extraction for Drivers in High-Speed Communications Channels

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Electronic Engineering Department

Licentiate Thesis

by

Jonathan Cedeño-Chaves

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Supervisor:

Dr.-Ing. Renato Rimolo-Donadio.

Reader:

1. Ing. William Marín-Moreno.

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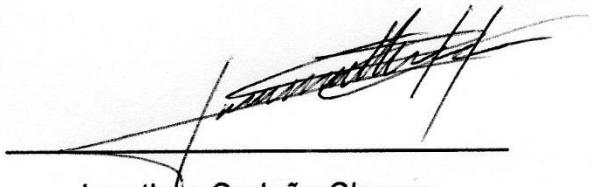

Jonathan Cedeño Chaves.

Cédula: 3-0455-0409.

Cartago, Noviembre 2015.

Abstract

This thesis describes the process performed for extracting a descriptive macromodel for a generic transmitter block at IC level for high-speed channels applications. The work has been focused on a first approach to establish at methodology to extract a macromodel considering both the signal and power domains.

Macromodels are required to perform accurate and numerically efficient simulations, in order to verify and validate behavior performances of communication links without having to consider the full driver model and potential IP sensitive information related to it.

In this work, different approaches for macromodeling generation are reviewed and a methodology based on the IBIS specification is explored. A driver specific topology had been chosen in order to exercise the methodology for macromodel generation. An important feature of the methodology is the possibility to include the effects concerning signal integrity and power integrity simultaneously, which was carried out by including controlled sources on the output of the driver.

Author key-words: Signal Integrity, Power Integrity, Transmitter, Macromodel, IBIS Models, Simultaneous Switching Noise (SSN).

A Dios y mis padres, por la gloria de hacerme vivir…

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Contents

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1. Introduction

Models for high-speed channels are usually highly complex due to the system density in modern electronics. For this reason, it is important to reduce the order of the models and to use efficient alternatives for models creation. In this way, the macromodels are often used to describe the different parts of the communication links. This is very important because it simplifies the analysis and the computational effort to generate simulation results.

Furthermore, it is possible to predict the signal and power integrity effects in the structures to simulate [1]. The Institute of Electromagnetic Theory, Hamburg-Harburg University of Technology (TUHH) [2] has been working in recent years in developing efficient models for interconnections of these channels and simulation tools in the time domain and frequency predict the performance of the channel and the degraded effects on the communications [3]. This work intends to contribute to this field by exploring alternatives macromodeling methodologies for high-speed drivers.

Among the principal effects concern to the high-speed links, the signal and power integrity are the main aspects to consider because of them depends the reliability of the transmission of information. The degradation effects are produced in the different physical structure parts of the link. As shown in Figure 1 an example of the typical scheme of the serial high-speed transmission link.

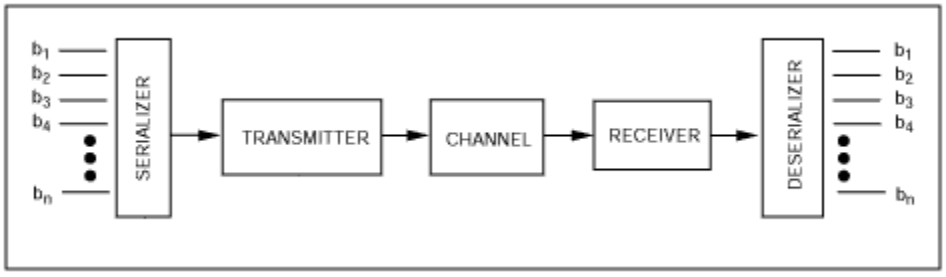


Figure 1. Scheme of high-speed communication link.

The main objective of this work is to develop a methodology for extraction of macromodels from generic transmitter designs at IC level using a standard format, which can consider power and signal effects and can be used in statistical and time domain high-speed channel simulations.

It is necessary to define a transmitter topology at IC level (SPICE framework) which contains relevant features for high-speed systems. In this work a differential driver was been chosen to build the macromodel.

Later, design a test circuit at IC level for characterizing the generic transmitter selected is necessary to define the driver behavior. Then, when the driver behavior defined, to develop a methodology for extracting the macromodel based on a standard description format (e.g. IBIS). The IBIS models methodology was used to macromodel the differential driver.

In order to build the macromodel, the driver variables extraction will be necessary. The macromodeling approaches use this information for the model construction. This extraction was performed on a SPICE-based framework.

Furthermore, the evaluation of the macromodel against circuit-level simulations will be the parameter to validate the reliability of the macromodel. This validation will be perform on high-speed link environment in ADS framework.

An important topic of this work is to take consideration the SPI effects in the macromodel. The Figure 2 shows the first approximation of the methodology scheme for this work.

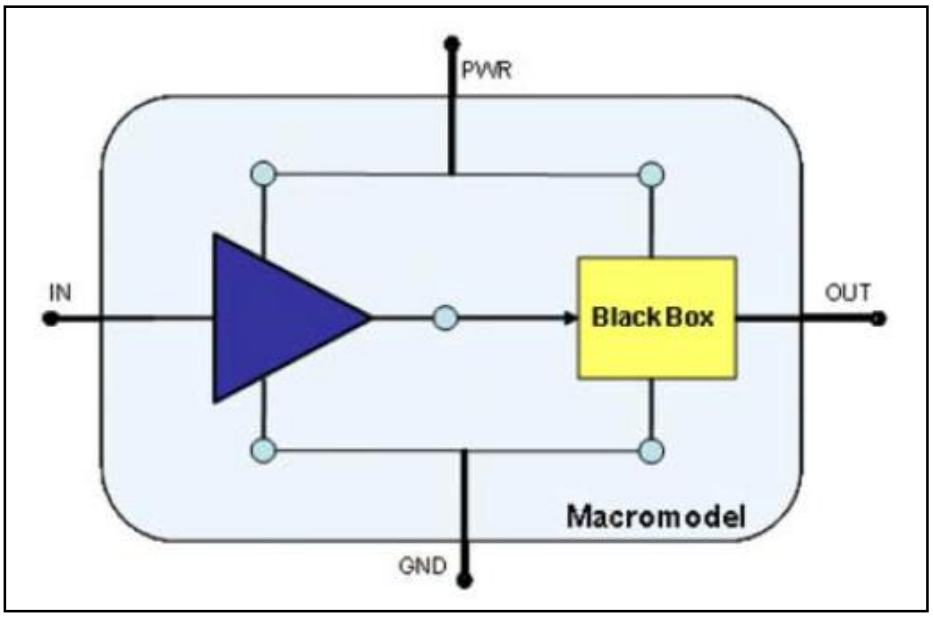


Figure 2. Improved IBIS model - Power Integrity issue [4].

2. High-Speed Serial Communication Channels

As in most communications (electric or otherwise), the elements or steps relating to the transmission and reception are needed. In this case, the control signals are basically essential for proper synchronization of the elements. Figure 3 shows a typical diagram of a high-speed link.

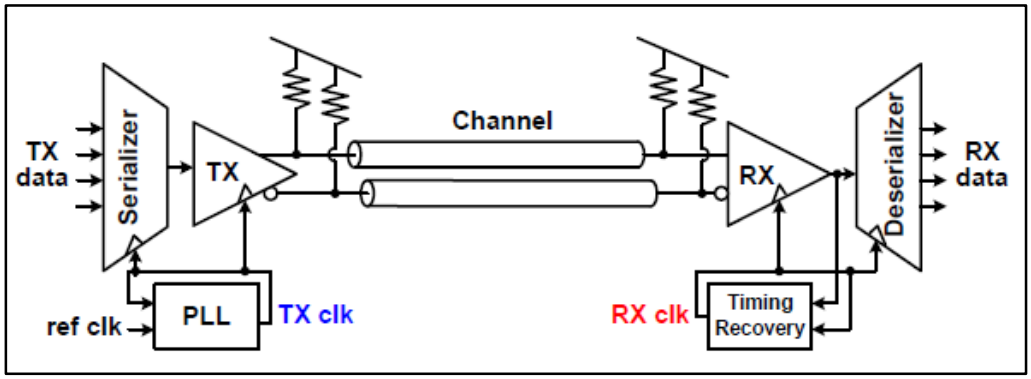


Figure 3. High-speed link diagram [5].

It is possible to observe how communication is performed in serially way due to the limitation that exists in the number of input and output terminals that the package or printed board has. For this reason, accurate synchronization of the elements directed to a correct transmission of information through the units. This synchronization is performed by the unit called PLL (Phase-Locked Loop) in the transmitter while the receiver is sampled according to the data flow entering the Timing Recovery [5].

Electrical inter-chip communication bandwidth is predominantly limited by high-frequency loss of electrical traces, reflections caused from impedance discontinuities, and adjacent signal crosstalk.

The relative magnitudes of these channel characteristics depend on the length and quality of the electrical channel which is a function of the application.

2.1 Passive Channel Model

The channel is the stage of the serial link where the information are transmitted. Several effects are present in the transmission and are produced in the communication channel. Inherent of it, the channel frequency response tends to mitigate the high frequency components, similar to a low-pass filter. In this way, the signal and power integrity take more important when a high-speed link is designed. The degraded effects are produced by the different stages of the channel.

Signal Integrity

In the electrical communications, transmitters and receivers are responsible for sharing information across different sectors and levels of a circuit. In high-speed communications, some effects produces degradation and low quality of the signal.

The degradation of the frequency components to transmit the information has inherent with the integrity of the same. Figure 5 shows how the different components of the link are responsible to mitigate the critical effects in terms of reliability of communication (Tx/Rx).

It is important to know the consequences that these effects can produce. Some of them are:

- Crosstalk.
- Impedance mismatches.
- Simultaneous Switching Noise (SSN).
- Reflections.

This thesis will focus on the macromodeling of the transmission driver in high-speed links.

Power Integrity

The noise induced by the power distribution network is produced for the parasitic effects in the interconnects and have to be in consideration when some information is transmitted.

Simultaneous Switching Noise is the main effect that affects the power grid. When many elements change state at the same time, a transient is generated at the voltage level required by the current. Such transient, in its most primitive form, can be approximated to an inductance of interconnections. This voltage can be described as:

$$v_{ind}(t) = L_{con}\frac{di(t)}{dt} \tag{1}$$

This phenomenon can be mitigated in several ways. One of them is the use of decoupling capacitors [6].

There are several methods to model the channel components in real backplane structure. Vias, Transmission Lines, cavities, connectors, etc., had been modeled with different types of modeling, such as analytical models, semi-analytical models, etc. The Figure 4 shows the typical channel components to model in real chip-to-chip links.

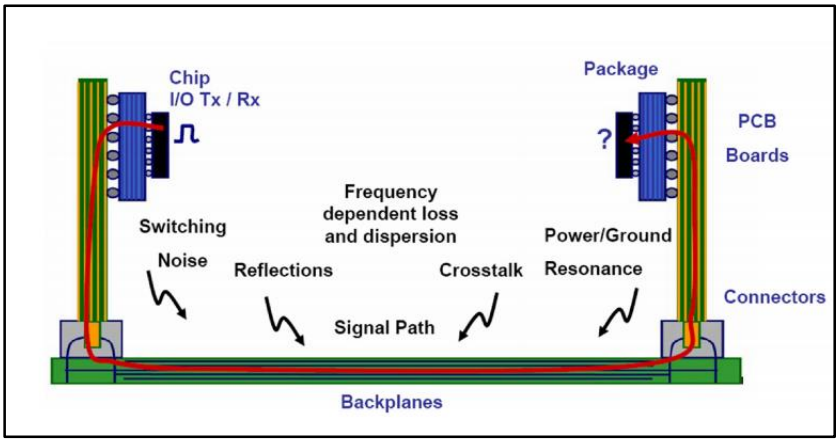


Figure 4. Typical Chip-to-Chip Link Diagram [8].

The Figure 5 and Figure 6 show different parts of a real channel for chip-to-chip links and are considered the real effects in high-speed simulations.

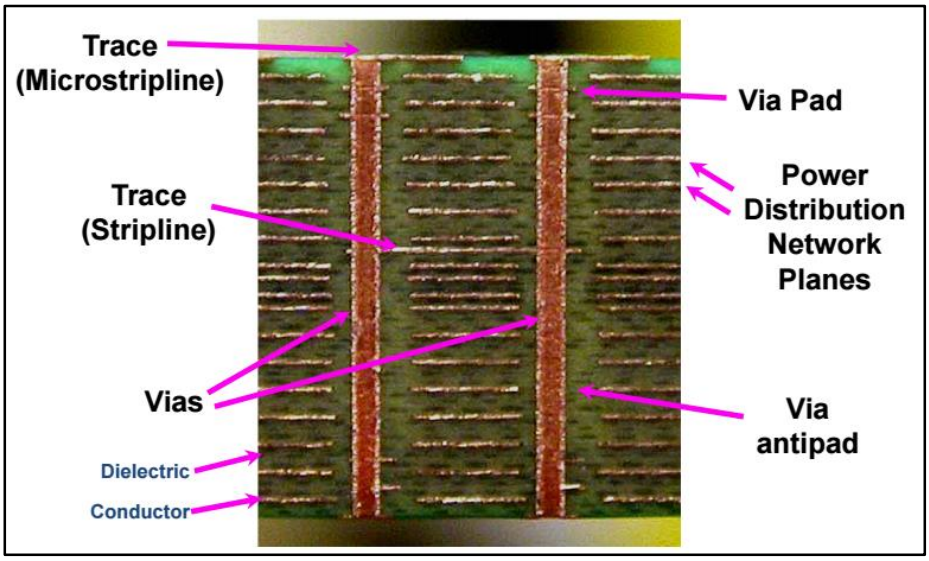


Figure 5. Printed Circuit Board (PCB) Cross Section [7].

The Institute of Electromagnetic Theory of the Technical University of Hamburg-Harburg has been working in recent years to develop efficient models for interconnections of these channels and simulation tools in the time domain and frequency predict the performance of the channel.

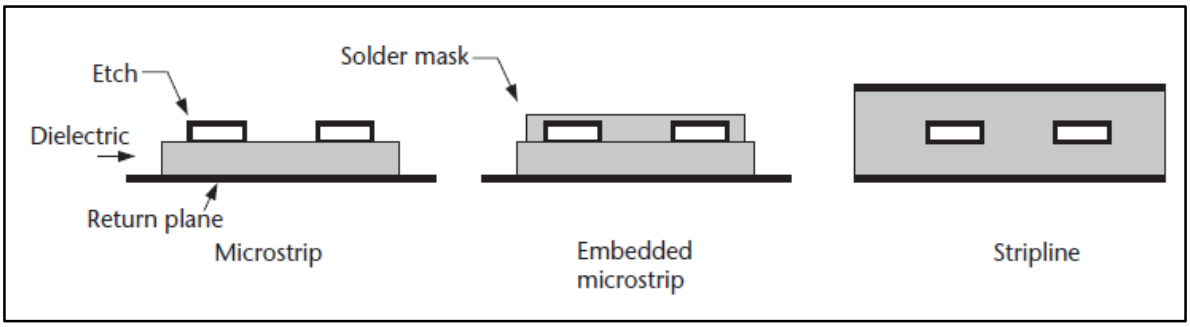


Figure 6. Microstrip and Stripline defined [1].

2.2 Power Distribution Network

The power supplying of an integrated circuits affects directly in its performance, cost, size and other characteristics. This system is comprised of interconnect networks with decoupling capacitors on a printed circuit board, an integrated circuit package, and a circuit die [8]. The Figure 7 shows the PDN scheme on a backplane system.

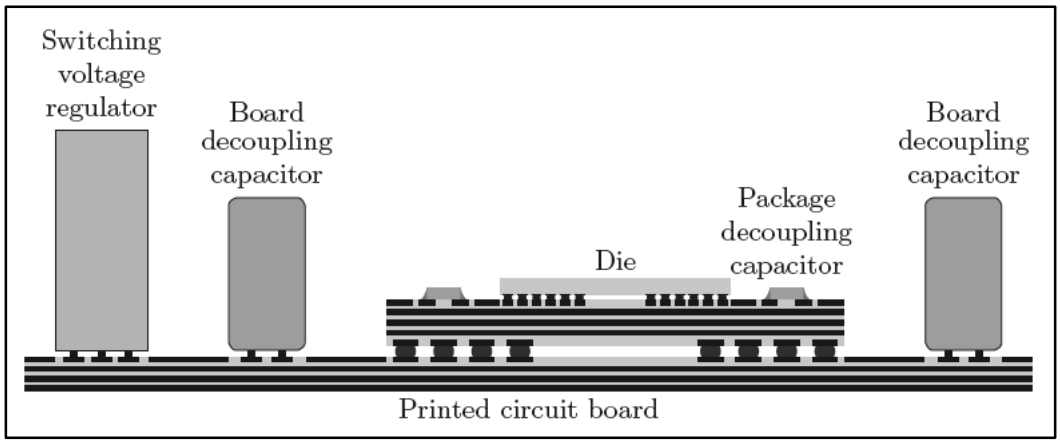


Figure 7. Power Distribution Network. Cross-Sectional View [8].

The physical structure of PDN is hierarchical. This hierarchical structures allows the desired impedance characteristics to be obtained in a cost effective manner. Each tier of the power distribution system typically corresponds to a tier of packaging hierarchy and consists of a power distribution network and associated decoupling capacitors.

Power distribution noise adversely affects the operation of an integrated circuit through several mechanisms. Some mechanism are: PDN noise produces variations in the delay of the clock and data signals, increases the uncertainty of the timing reference signals generated on-chip, lowering the clock frequency of the circuit, reduction of noise margins and power supply variations diminish the maximum supply voltage of the circuit, degrading the circuit frequency of operation. Specifically, some of the PDN noise affects are:

- Signal Delay uncertainty.
- On-chip clock jitter.
- Noise margin degradation.
- Degradation of gate oxide reliability.

2.3 Transmitter – Receiver

The transmitter in high-speed links is the unit responsible for stimulating the channel with a suitable voltage or current that allows the move of information between itself and the receiver. Also, the transmitter has the features that allow the improvement of the reliability of the communication, such as equalization. In practice, there are two main stages or types of drivers [9]. Those are shown in the Figure 8.

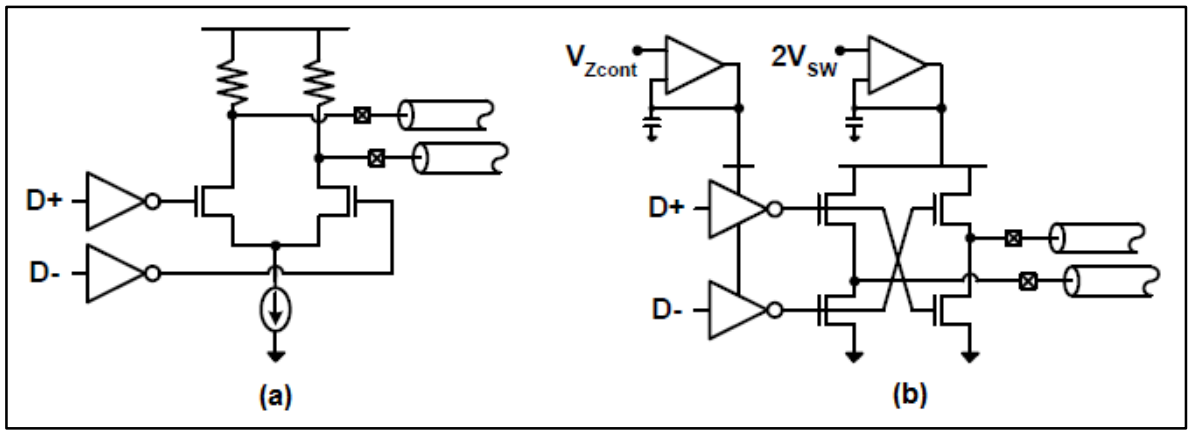


Figure 8. Transmitter stages (a) Current-mode (b) Voltage-mode [10].

There are some advantages in each one of those types of driver. In Figure 8 (a) we can see the schematic diagram of the driver CML (Current-Mode Logic) and Figure 3 (b), the schematic diagram of the driver VML (Voltage-Mode Logic) type. The first configuration is widely used in high-performance serial links. This configuration presents a low voltage consumption compared to other existing configurations [9].

Basically, the receiver needs to focus in two aspect when it is receiving information from the transmitter. The receiver has to synchronize with the transmitted signal. The transmitter and receiver are designed in concert, both use the same value for the bit interval time. Once synchronized and data bits are transmitted, the receiver must then determine every T seconds what bit was transmitted during the previous bit interval [10].

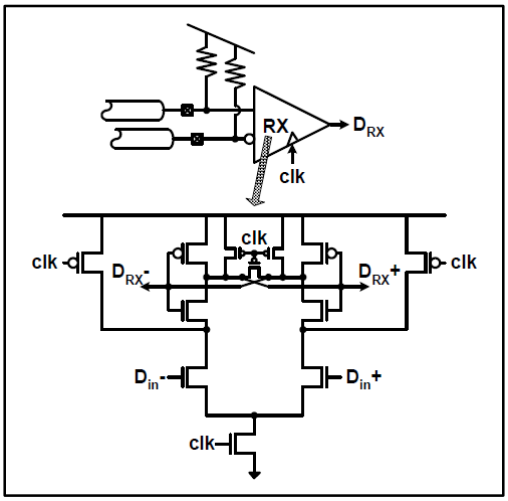


Figure 9. Receiver Input Stage [11].

The Figure 9 shows a high-speed receiver which compares the incoming data to a threshold and amplifies the signal to a CMOS value.

Transmitter Equalization – Pre-Emphasis

The methodology for development of this equalization is based on the difference of a signal with itself delayed. The Figure 10 is the time diagram which shows how this equalization is developed.

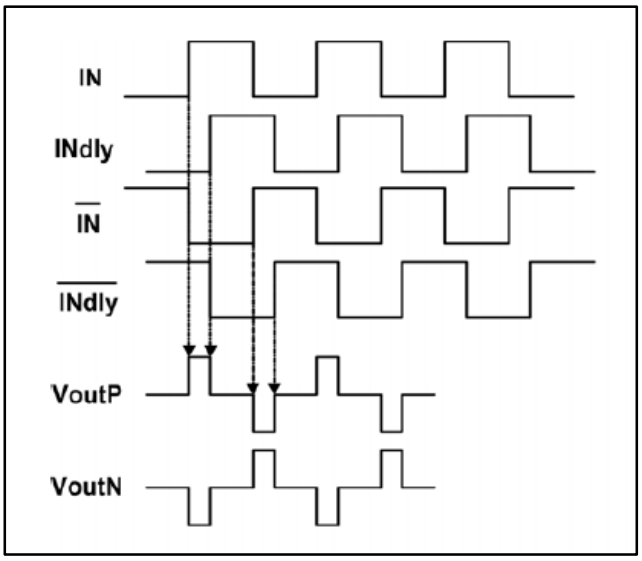


Figure 10. Pre-Emphasis Time Diagram [12].

It is possible to deduce that, after a train of two or more identical logic states are given, the first state or first bit train “emphasizes”. This equalization follows the following equation:

$$y[n] = x[n] - \alpha * x[n-1] \quad (2)$$

The equation (2) suggest, with the respective analysis data, the subtraction removes the part of samples that did not change in relation to its adjacent samples and for that reason, just remains the part of the signal that changes rapidly, the high-frequency components. In case, the pre-emphasis stage works that high-pass filter.

The schematic circuit in the Figure 11 shows the complete configuration of the transmitter (Driver + Equalization). In this way, it is possible to implement the transmitter in a framework environment to simulate the performance [11].

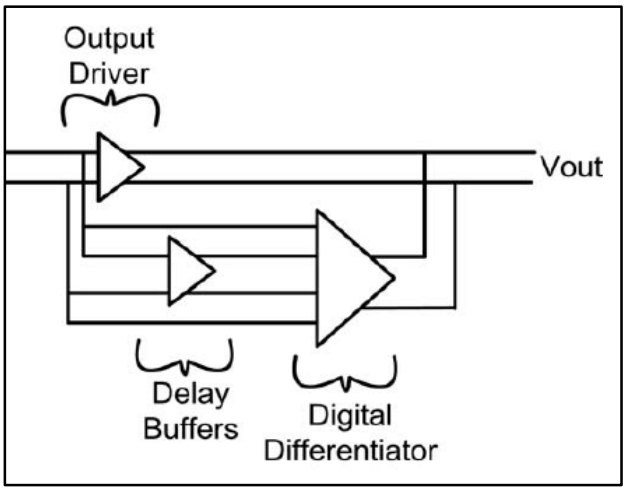


Figure 11. Equalized Transmitter Block Diagram [12].

The schematic circuit diagram of the pre-emphasis stage is based to the differential amplifier. With this configuration, the signal differences are easy to achieve. The simulation was performed based on it.

3. Macromodeling Approaches

The high-speed simulations are computationally exhaustive, in terms of CPU performance and memory required. For that reason, macromodels approaches are very useful in order to develop faster simulations with the plus of reduce the simulation time. Some approaches are analyzed in this chapter.

3.1 Radial Basis Function Based Modeling

This approach consist in a technique to model non-linear behaviors. The technique is based on a relation of the current and voltage output. That relation is described as follows:

$$i_o(k) = w_1(k)\, f_1\big(\Theta_1, x(k)\big) + \; w_2(k)\, f_2\big(\Theta_2, x(k)\big) \tag{3}$$

$$f_n(\Theta_n, x(k)) = \sum_{j=1}^{M} \Theta_{nj} \Phi(|x - cnj|, \beta), n = 1,2, \ldots \quad (4)$$

The last equations described the output current in function of the functions that describes the driver output current to the output voltage for driver input high and low.

The transition from one logic state to another is done with the help of weighting functions *w1* and *w2*. The time-varying weighting functions act as switches between the sub-models *f1* and *f2*. Sub-models *f1* and *f2* are expressed as a summation of radial basis functions, as shown in the second equation, where *M* is the number of basis functions needed for *f1* or *f2* to accurately model the digital driver. Gaussian, Multi-quadric, and thin-plate spline are some of the radial basis functions as shown in Figure 12. The centers of the basis functions are defined by *cj* [12].

The regressor vector x in the second equation collects the past *r* samples of the driver output voltage and the driver output current along with the present sample of the driver output voltage. The parameter *r* has been called the dynamic order of the model.

$$x^T(k) = \begin{Bmatrix} i_0(k-1), i_0(k-2), \ldots\ldots, i_0(k-r) \\ v_0(k-1), v_0(k-2), \ldots\ldots, v_0(k-r) \end{Bmatrix} \quad (5)$$

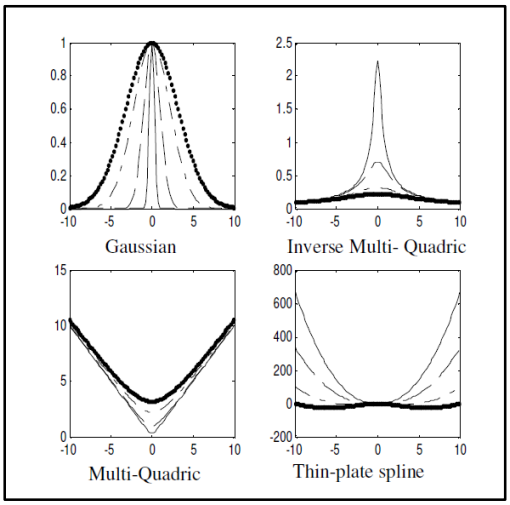


Figure 12. Different Radial Basis Functions [12].

3.2 Spline Function with Finite Time Difference (SFWFTD) Modeling

SFWFTD method can accurately model moderately nonlinear driver circuits. This modeling approach is simple and efficient compared to RBF modeling approach where macromodels have numerical convergence problems with SPICE.

For moderately nonlinear driver circuits, the dynamic characteristics start to dominate the static characteristics and therefore, static characteristic models cannot accurately capture the nonlinearity. It can be observe in the Figure 13 [12].

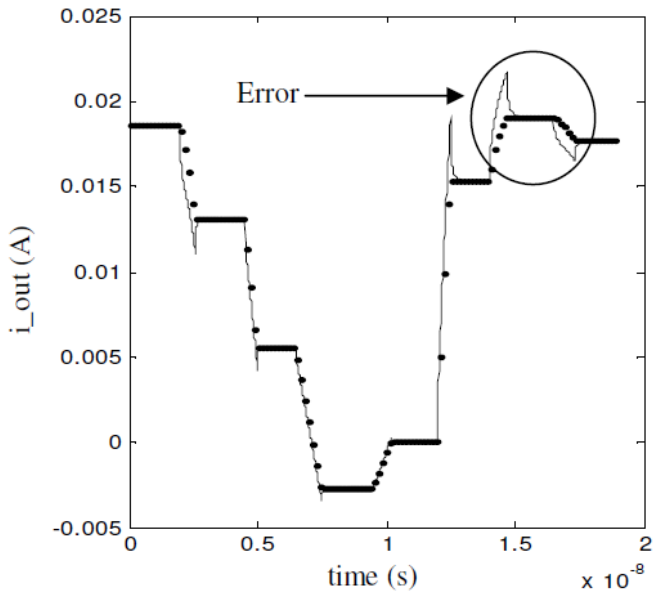


Figure 13. Transistor Level Response (Straight Line) and Static Characteristic Model (Dotted Line) [12].

A SPICE equivalent circuit of SFWFTD model is similar to the static characteristic model spice netlist. The Figure 14 shows an example of SPICE netlist representation for SFWFTD approximation.

```
.subcircuit     driver_output          gnd

V_w1            w1          gnd        PWL ....

V_w2            w2          gnd        PWL ....


E_f1            x1          gnd        VOL = ' ... '
R_f1            x1          x2         1
C_f1            x2          gnd        C

E_f2            y1          gnd        VOL = ' ... '
R_f2            y1          y2         1
C_f2            y2          gnd        C


G_out           gnd         driver_output   CUR = 'V(w1)*( ... ) + V(w2)*( ... )'

.ENDS
```

Figure 14. SPICE Netlist representation for SFWFTD model [12].

3.3 Recurrent Neural Network Modeling

Recurrent Neural Networks models systems with memory or feedback effect accurately. A Recurrent Neural Networks has the capability of learning and then representing dynamic system behavior [12].

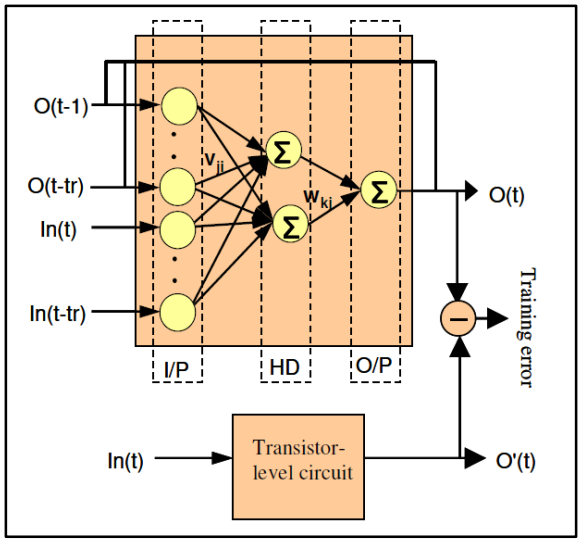


Figure 15. Schematic of Recurrent Neural Networks Model [12].

Recurrent neural networks (like ANNs) typically have three layers: the input layer, the hidden layer and the output layer. The inputs are fed into the input layer that is connected to the hidden layer through weights *vij*. The number of hidden layers and neurons can be increased or decreased depending on the complexity of the system being modeled.

3.4 IBIS Modeling

This technique is based on extracting the DC, AC and transient behavior of the driver to macromodel and such information can be tabulated in an ASCII file compatible for some simulators. The Figure 16 shows the design flow to create an IBIS macromodel.

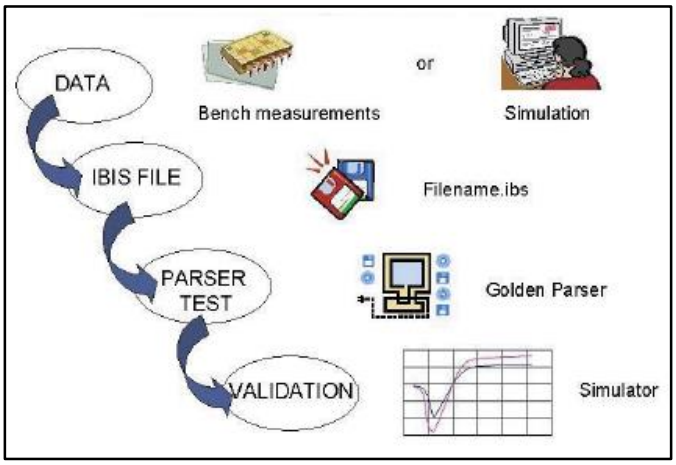


Figure 16. IBIS Extraction Flow [13].

In this work, the information has been extracted from simulations, developed in the Synopsys framework HSPICE.

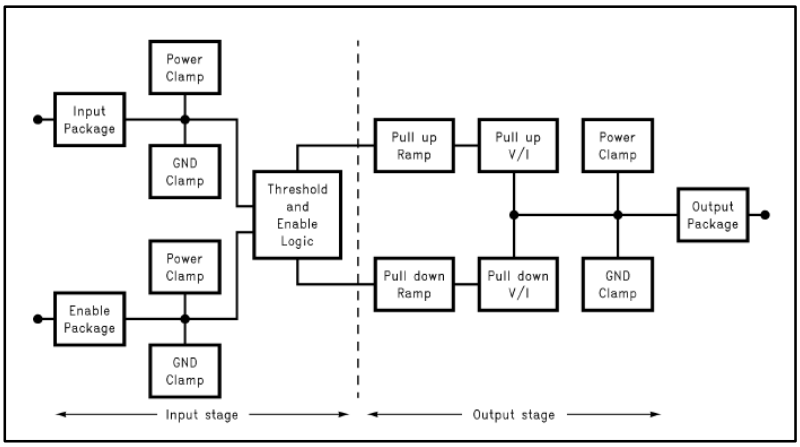


Figure 17. General IBIS Block Diagram [13].

The Figure 17 describes the general scheme of the IBIS stages, input model or output model. In the output case, the first stage called “Pull-up/down Ramp” shows the transient behavior of a buffer to model, it can show how each edge of an output stream which it is a function of time (curve VT). The second stage, “Pull-up/down V/I” shows de DC behavior, the output voltage according to the respective associated current. If tri-state buffer is modeling, stages “Power/GND Clamp” show the output values of the buffer in tri-state. As a last stage, the “Output Package” has the values according to the technology used.

The following schematic circuits show the equivalent of each IBIS type model.

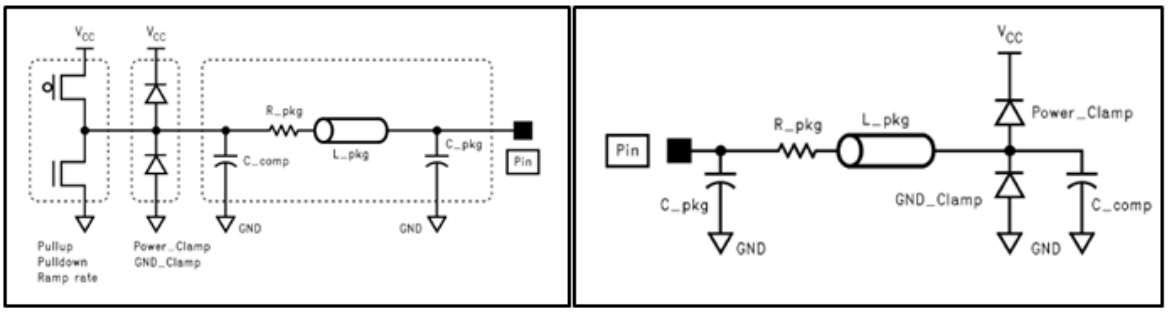


Figure 18. IBIS Stages Models (a) Output (b) Input [14].

The schematic configurations above are very general approaches of the behavior of each IBIS buffer, separate stages to extract.

This information is obtained by forcing the output driver pins to a value and extracting from it a current or voltage values and then, should be tabulated in an ASCII file, with a format defined by the methodology. Many simulators are compatible with such files, as its main advantage is that they show only the electrical behavior of the buffer and its internal composition design.

4. Macromodeling Methodology

The main goal of the research is to extract a descriptive macromodel of a transmitter to use in high-speed link simulations. In order to achieve the project solution proposal requirements, the next methodologies are proposed to perform the macromodel, such as:

- Mpilog Methodology
- Custom Methodology
- IBIS Methodology

It is important to note how all the above methodologies need to be extended in order to map the power noise at the output which is one of the main objectives of the research too.

Mpilog is a tool designed for the interactive generation of macromodels. Macromodels are mathematical relations approximating the port electrical behavior of devices, thus completely hiding the internal structure of devices and preserving the proprietary information of vendors. They are obtained from a set of port voltage and current responses carrying the information of port behavior that can be obtained either via direct measurements or via circuit simulation by driving the port with

suitable stimulus. The mathematical expressions in order to model the driver increases the construction of the macromodel.

The next option, the custom methodology presents more complex to perform the macromodel. The last methodologies present higher complex than the third option. In the chapter number 3 IBIS methodology had been analyzed. Its principal scheme does not present high complex and in fact, was chosen such the principal approximation. Following the methodology, it is necessary to characterize a generic driver.

There are different types of drivers used in high-speed communications. These drivers in general, differ in the type of control signal or the scheme of modulation/demodulation. There are two main types of drivers: current-mode and voltage-mode.

The principal differences among the topologies are the ease of generation and the noise coupling. This means that is easier to generate a small current than a small voltage.

LVDS Driver

Such configurations in the Figure 19 belong to a driver family called LVDS (Low-Voltage Differential Signaling), which are widely used by low power and speed in performance. The typical usages are:

- Ultra-Low Power Applications.
- Differential Operations.
- High performance serial links.

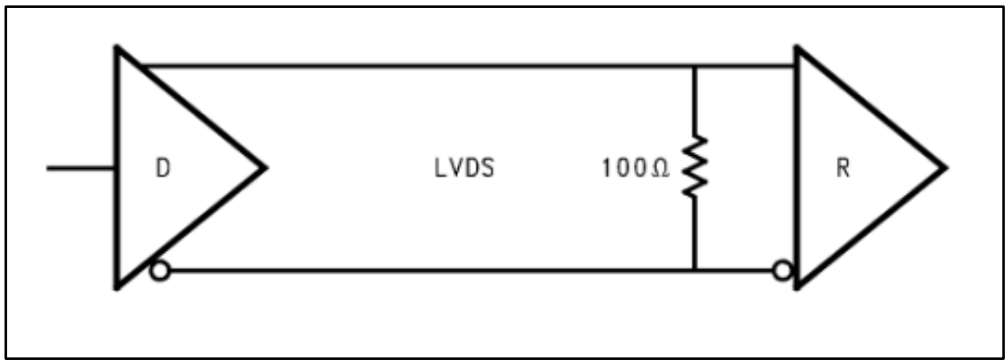


Figure 19. Typical Link Configuration – LVDS Drivers [15].

This technology uses differential transmission data. For that reason, the LVDS drivers are less susceptible to common mode noise. Furthermore, as the name implies, LVDS operates a low voltage swing compared to other data transmission standards. Typically, the voltage swing is around to 150 mVpp – 400 mVpp. The Figure 20 presents the schematic diagram of one of these transmitters.

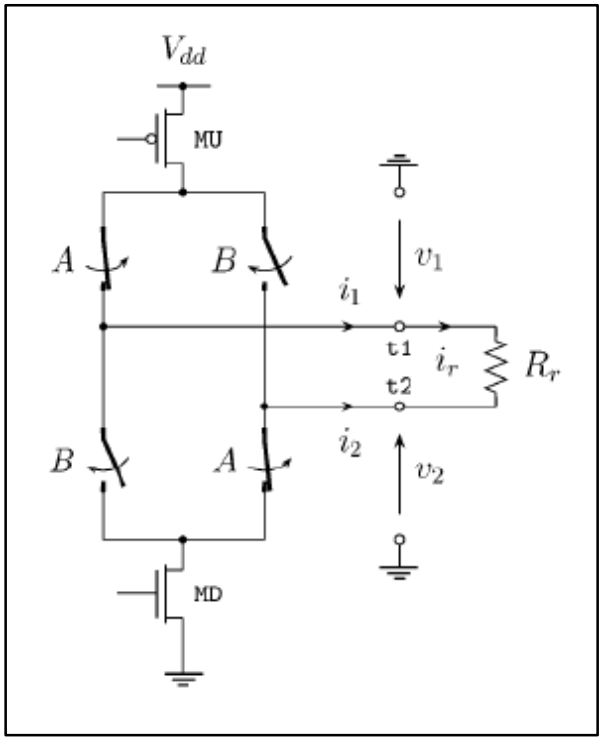


Figure 20. LVDS Configuration Driver [16].

Generally, in this type of transmitters, the modulation used depends on the polarity of the electric current on the load. As a following diagram, the current changes the direction flow when the transmitter is switching.

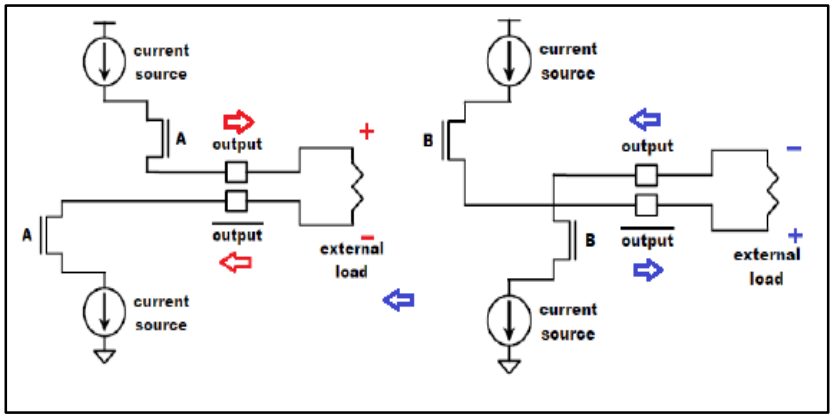


Figure 21. LVDS Driver Switching Behavior [17].

A resistor at the receiver allows the signal modulation, which the Figure 20 shows. The following figure shows the modulation used, NRZ (No-Return Zero).

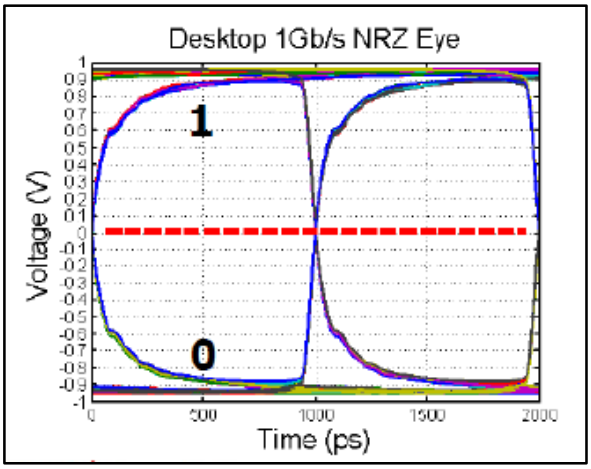


Figure 22. NRZ Modulation Scheme [9].

The Figure 22 shows the NRZ modulation scheme waveform. It is clearly to see that the signal does not take zero values among adjacent states.

This modulation allows a better immunity to a noise.

For the differential driver extraction, the IBIS methodology has some keywords that allow high accuracy models. These incorporate the common and differential modes of the driver. The Figure 23 shows the general diagram of the differential macromodel in IBIS, shown as functional blocks.

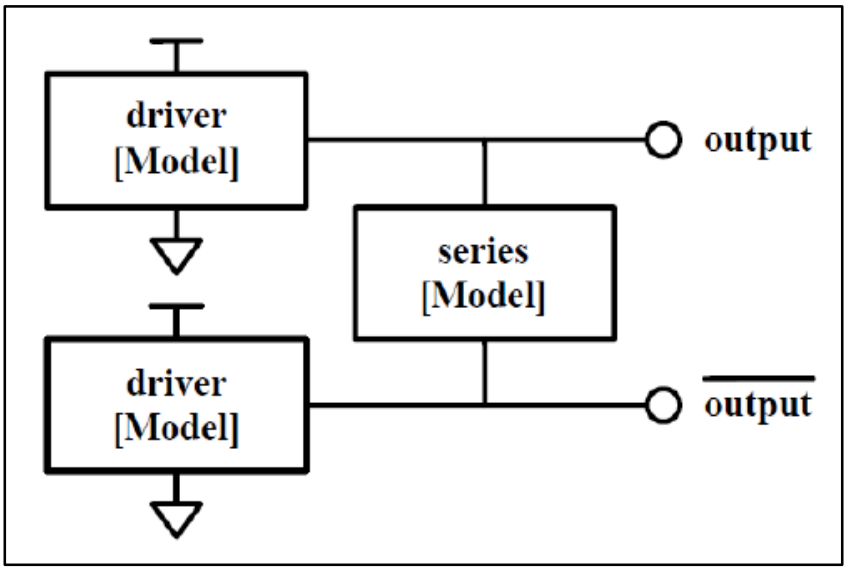


Figure 23. Full-Differential Driver Model Block Diagram in IBIS [17].

To the differential driver extraction, it is necessary to make a differential and common mode separation. The methodology defines two keywords for it:

- Common-mode: [Diff Pin] → Combines two different models as a differential pair.
- Differential-mode: Series [Diff Pin] → Modeling elements between terminals.

In the Figure 24, it is possible to identify each element in the modeling to IBIS differential drivers.

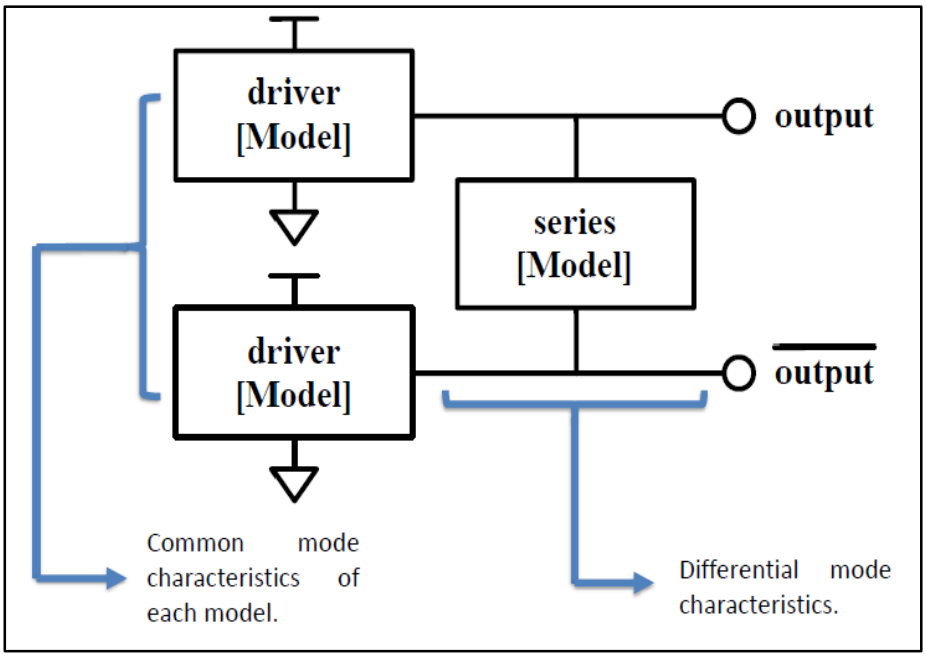
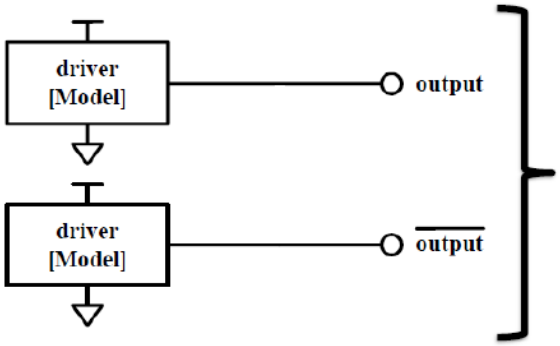


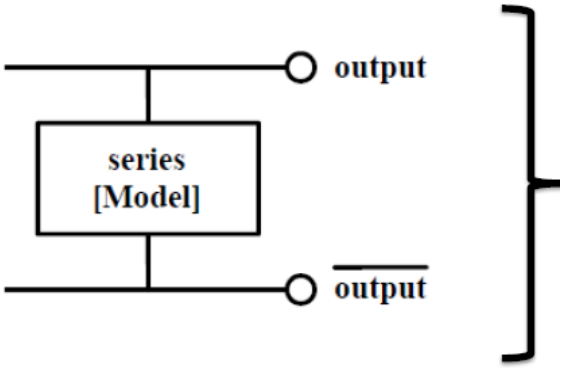
Figure 24. IBIS Differential Model Parts [17].

In each model blocks it is necessary to define the driver behavior. Due to this, the extraction and separation of each typical response part is fundamental in time to modeling the driver.



For the common-mode behavior, the outputs have to be modeling as a single-ended type (in separate models in case to not be symmetrical). Each output has its own common-mode behavior.

Figure 25. Common-mode Block Part [17].



In the differential behavior case, the outputs have to be related after the common-mode extraction. The Series [Model] block contains the differential behavior. This block is located between the both output terminals and will contain the current dependence information.

Figure 26. Differential-mode Block Part [17].

Results in HSPICE – Synopsys Framework

To validate the correct operation of the transmitter in Synopsys is necessary to define the technology to be used. According to the available tools, xh018-0.18um was used by XFAB. Such schematic test was developed and simulated in HSPICE tool.

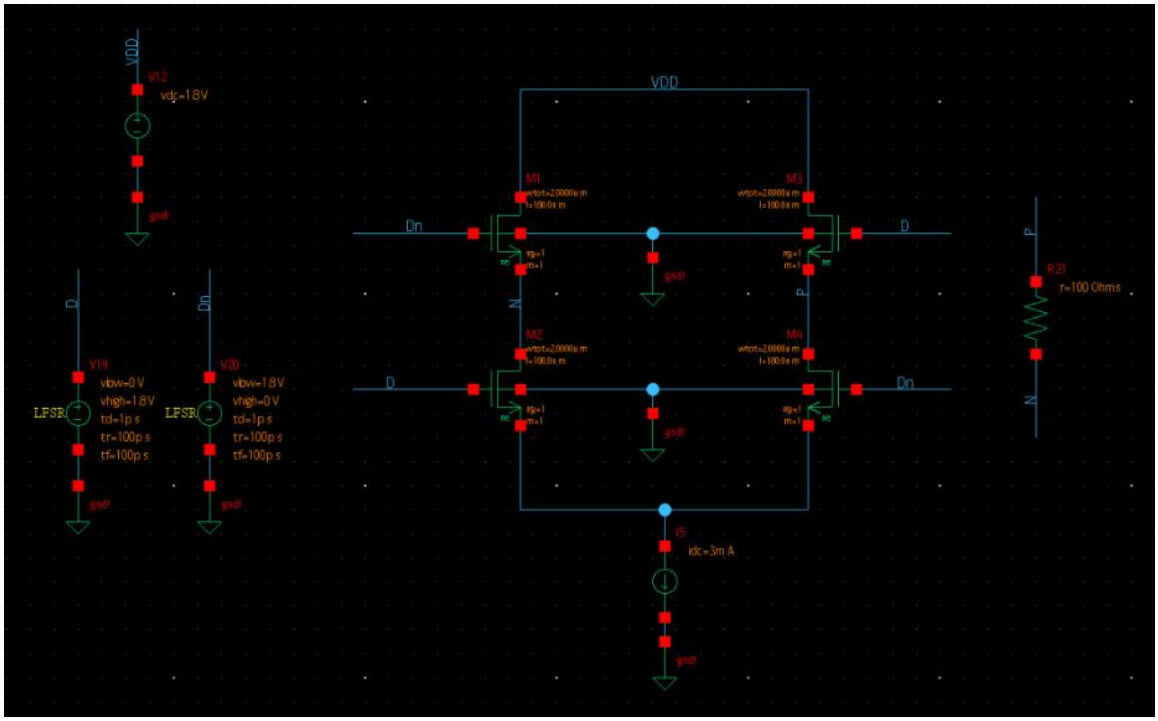


Figure 27. LVDS Driver implemented in Synopsys Framework

This test was developed with a 3 mA current vias, with a width (W) dimension in PMOS transistor is 2 um and NMOS transistor, 0.42 um. The length (L) dimension, by the used technology, is 0.18 um. With a 3 Gbps PRBS, 100 ps for rising and falling waveform, the transmitter was tested. The input and output waveform are shown in the Figure 28.

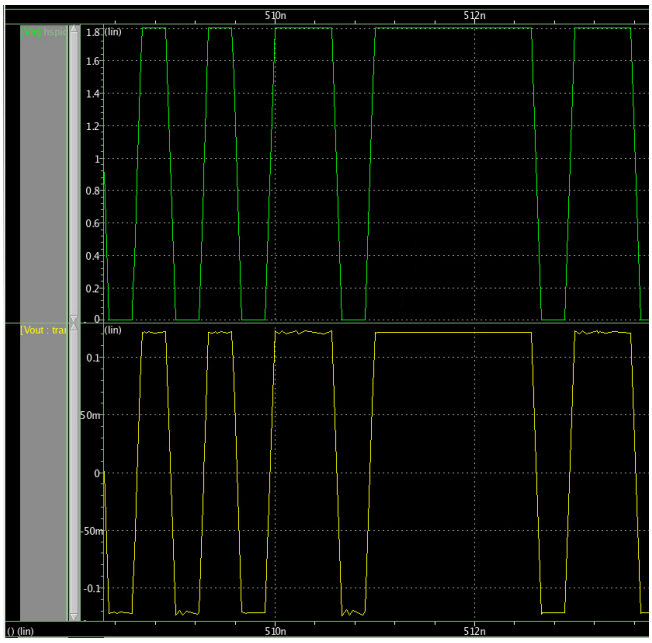


Figure 28. HSPICE Simulation – Input, Output.

The green signal represents the input of the driver and the yellow signal, the output. The output waveform has the typical LVDS output behavior. At the above figure, it is possible to see a noise at the output, due to the technology is not as quick to follow the input signal.

The output signal is a combination of two independent signals. As a following figure, it shows the waveforms of each output signals called *Vp* and *Vn*, that generate the differential output voltage following the next equation:

$$V_{diff} = V_p - V_n \tag{6}$$

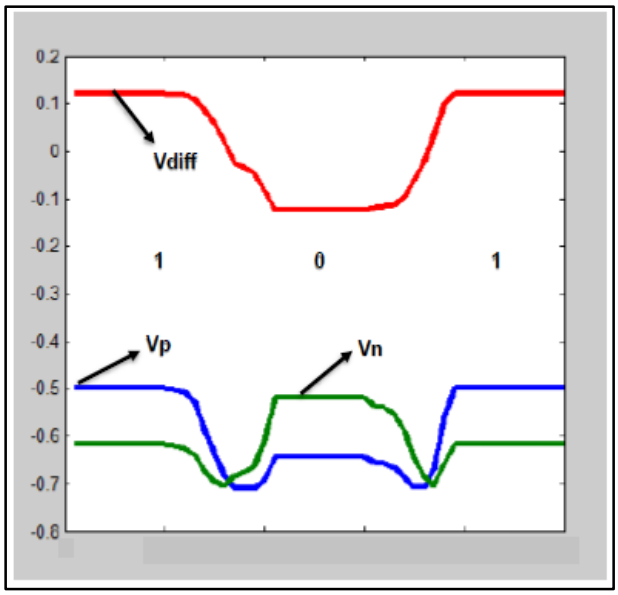


Figure 29. Differential Output Signals.

From the differential output signal, it is possible to analyze the maximum and minimum values to know the common-mode voltage. Exporting the output signal to MATLAB:

$$V_{max} = +0.11979\ V \qquad V_{min} = -0.12517\ V$$

$$V_{CM} = \frac{V_{max} + V_{min}}{2} = -2.69\ mV$$

This common-mode voltage is very short, but it is very important to take in consideration in the IBIS differential extraction.

The following Figure 30 the pre-emphasis schematic diagram.

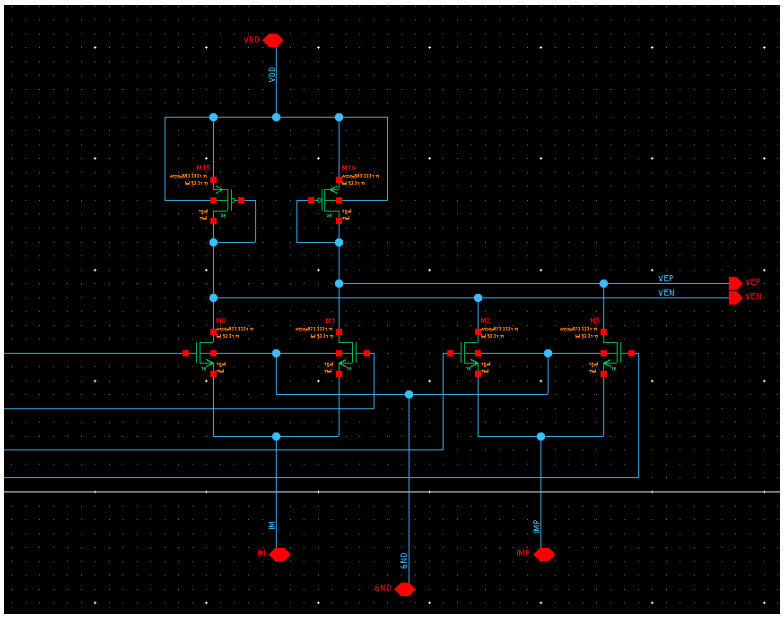


Figure 30. Pre-Emphasis Stage implemented in Synopsys Framework.

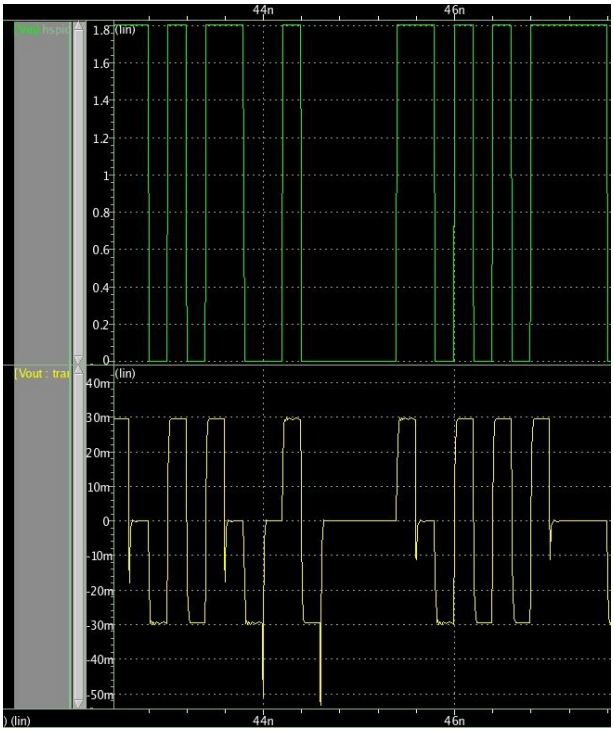


Figure 31. HSPICE Pre-Emphasis Simulation – Input, Output.

The above transient behavior shows that the signal is not clearly. The HSPICE simulation was developed with a 5 Gbps PRBS. It confirms that the used technology can not follow the input quickly.

IBIS Differential Driver Extraction

The IBIS methodology requires extracting and the tabulation of the voltage and output current data. This information contains the DC behavior of the driver. For differential drivers, the methodology is defined as follows:

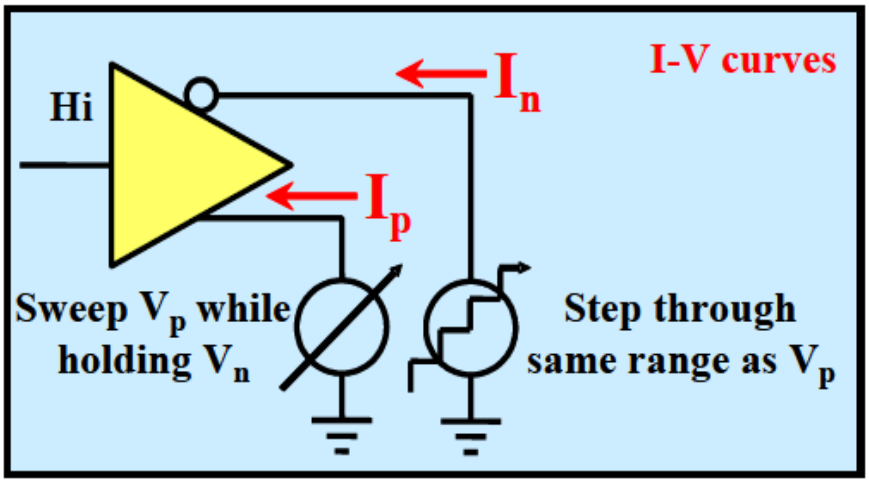


Figure 32. I-V Table Extraction for Differential Drivers [17].

An important feature of this kind of driver is the dependence that the output current has with the both output voltages. This dependence is defined:

$$i_{diff} \quad \rightarrow \quad i(v_p, v_n) \tag{7}$$

For this reason, it is necessary to extract the output current of each terminal for each voltage combinations. Thus, in one terminal is to set a fixed voltage value and the other terminal, a voltage sweep. With this procedure, the common and differential

modes have been extracted together. It means that the information extracted is not adequate or accurate typing on the IBIS model file.

For the driver to modeling:

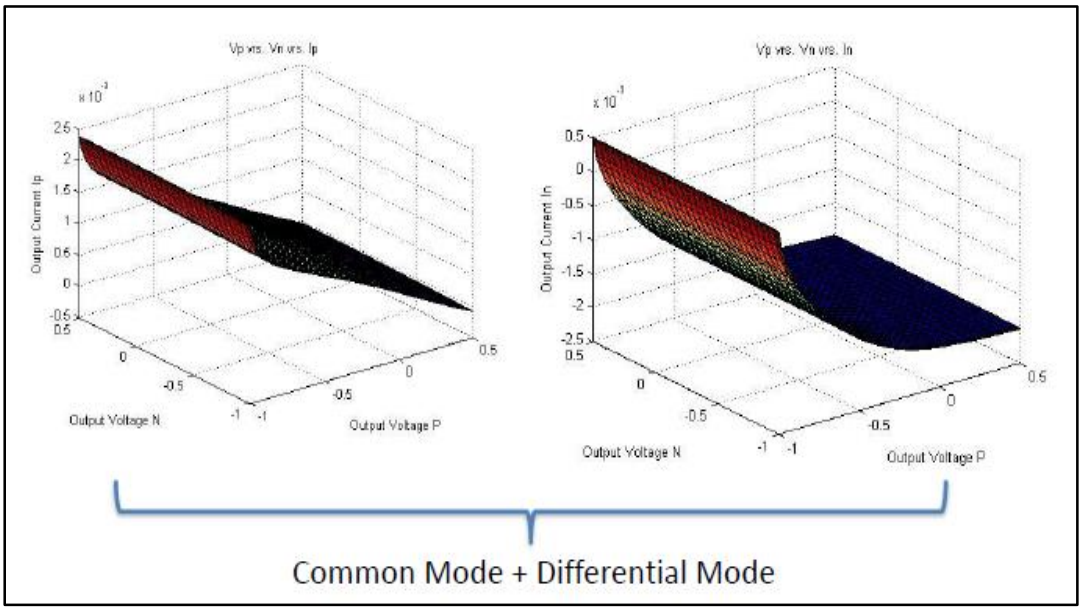


Figure 33. Surface Plots - V-I Data Extraction.

To separate the both behaviors, it is necessary to analyze the current value when the differential voltage output is zero. In the each terminal current matrix, it happens at the equipotential diagonal.

$$I_{p,n} = \begin{bmatrix} I_{11} & \cdots & I_{1N} \\ \vdots & \ddots & \vdots \\ I_{P1} & \cdots & I_{PN} \end{bmatrix}$$

When the both output voltages have the same value, ideally, the differential current has to be zero. Summary, the common-mode behavior can be obtained:

$$V_p = V_N \quad \rightarrow \quad I_{diff} = 0$$

At the current matrix, it possible to see that assumption is missing. For that reason, this equipotential diagonal represents the common-mode behavior of each terminal, in function of one voltage (*Vp* = *Vn*). To obtain the differential element of the driver, it is necessary to extract the common-mode values to set into the IBIS file. With the rest values, subtracting each row their respective value of common-mode current and the remaining information represents only the differential driver behavior.

The following Figures 34 and 35 show the common-mode current at each terminal and the surface of the differential current.

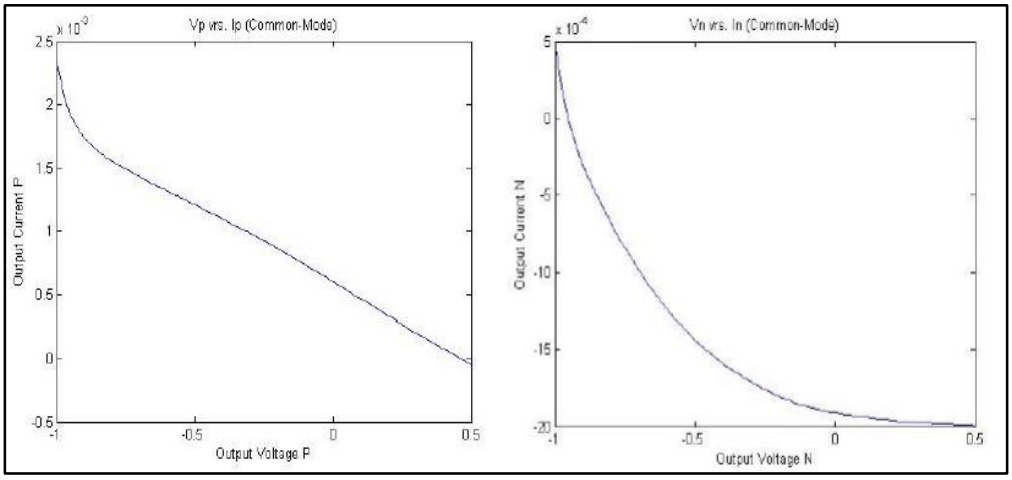


Figure 34. Common-mode V-I Curves.

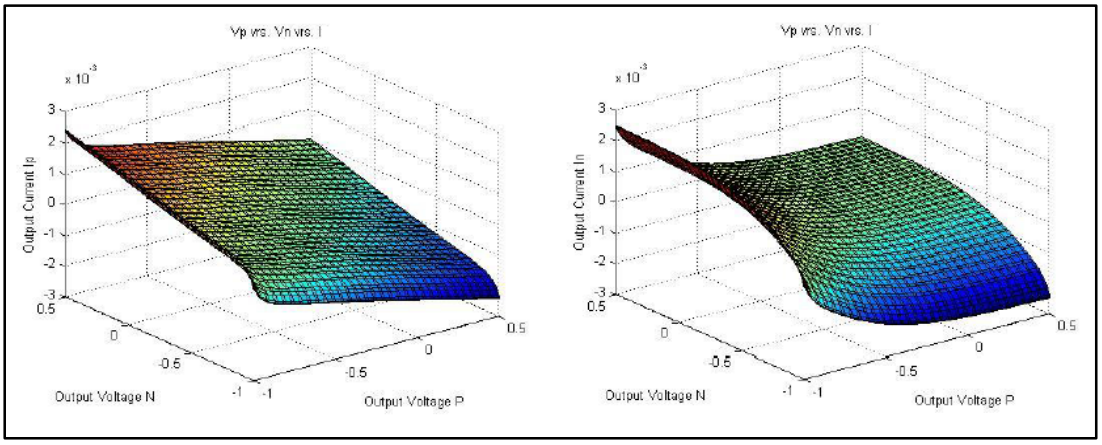


Figure 35. Differential Current Plots.

With the two last elements, the DC behavior of the IBIS model can be build.

Rising and Falling Waveforms

In the transient behavior case, the extraction of the V-T table data follows the usual techniques applied to single-ended buffers. The output has to be connected to a characteristic R_fixture and V_fixture on the load and produce an output state logic transition (low to high and high to low). In this way, it is possible to obtain the rising and walling waveforms.

Typically, the R_fixture is set to a matched transmission line impedance value. In the voltage case, the V_fixture is defined with the typical state logic values. The following Figure 36 shows the typical waveform and falling waveforms extraction.

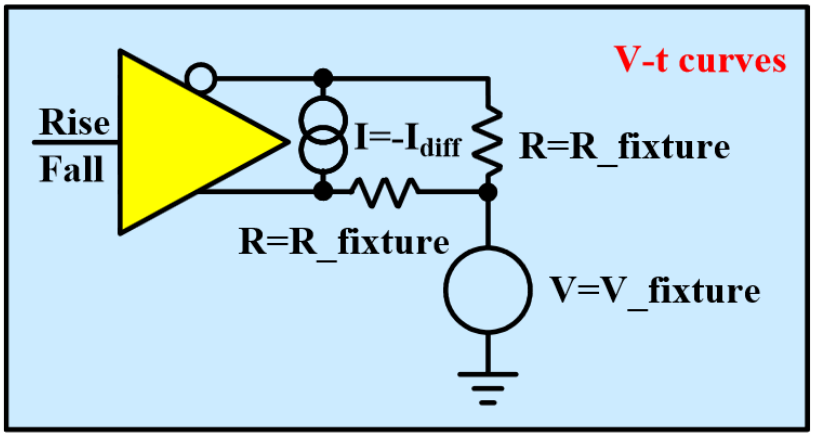


Figure 36.V-T Table Extraction for Differential Drivers [17].

An important topic about the above configuration is the necessity to extract the differential component of the output signal. It is because the relationship with the DC behavior is given with the common-mode component. Without this separation, the data values of the both waveforms and the DC behavior will present mismatches.

Respect to the macromodel extraction, the used methodology had followed the modeling drivers based on IBIS. Still, certain problems in the convergence model in the ADS framework tool are present.

Among the main problems that occurred were in high-speed simulations the methodology did not converge properly or as intended, and the proposal currently on the principle of having an overview of the behavior of a commercial module in order to offer it to pre-purchase simulations principally. For that reason, the coupling block in the IBIS simulation tool with a channel network parameters block is not enough robust to perform simulations under real conditions of a communication in high-speed channel. That is the main reason why the methodology fails for the research purposes. Also, the extraction steps became in high-complex steps. In this way, the macromodel convergence was an often problem in the development of the research. The technical support did not helpful with the progress of the work.

About all these topics, the way to follow in the research work was important. In this way, the decision was to substitute the macromodel behavior based on IBIS by its equivalent in waveform signal. The waveform extracted is defined in the Figure 37.

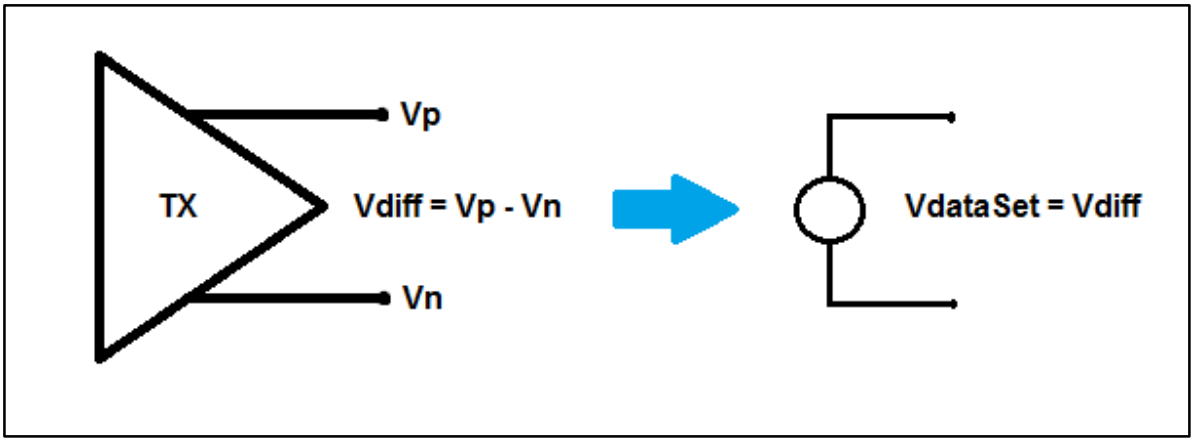


Figure 37. Differential driver waveform exported.

This waveform will use to apply the power noise mapping, described as follows.

Power Distribution Network Noise Mapping

The IBIS methodology versions before to 5.0 presented deficient when it take in consideration the effects in power delivery network (PDN). The principal effect to map is the simultaneous switching noise (SNN) that is very common to find in a high-speed links. Several works had been developed to correct or improve the model accuracy and its effects.

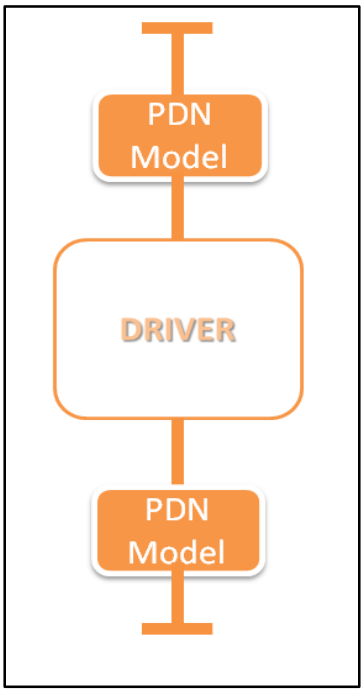


Figure 38. Transmitter with PDN Models.

For fortune, next to the version 5.0 is possible to map this noise effect in the PDN. In order to make it, the PDN model has to be definided. The Figure 38 shows the general block diagram of a driver with its PDN component to model in IBIS.

At the IBIS ASCII file, the way to set the effect is shows in the Figure 39.

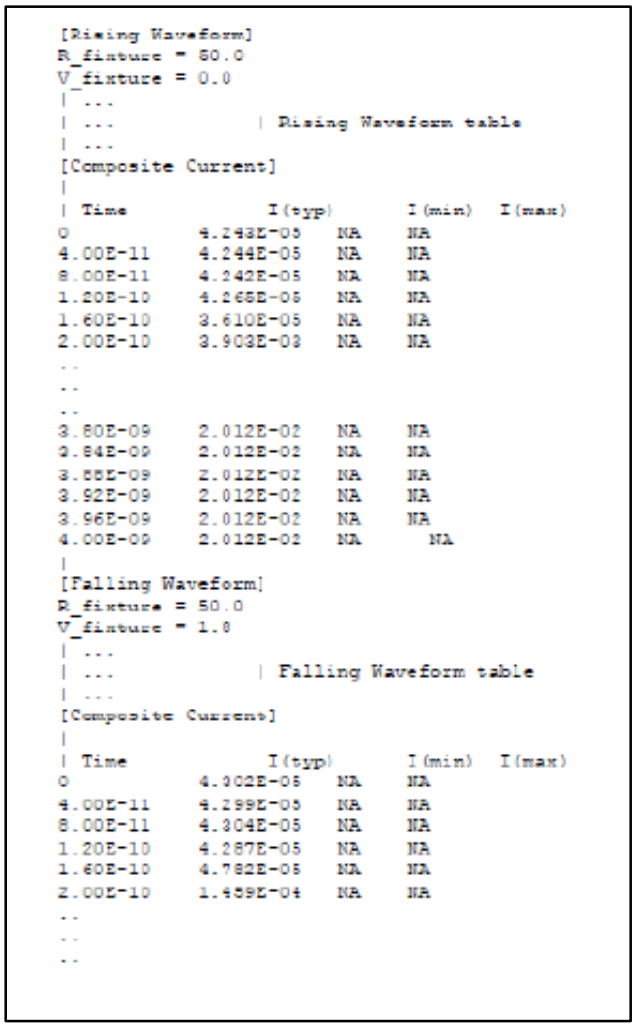


Figure 39. [Composite Current] IBIS keyword.

Under each voltage tabulated waveform, the I-T has to be tabulated also. With it, the output is on relationship with the power network. In fact, the both tabulated information have to be synchronized, with the same time scale. In the Figure 40 is possible to visualize what current will be map on the Composite Current keyword.

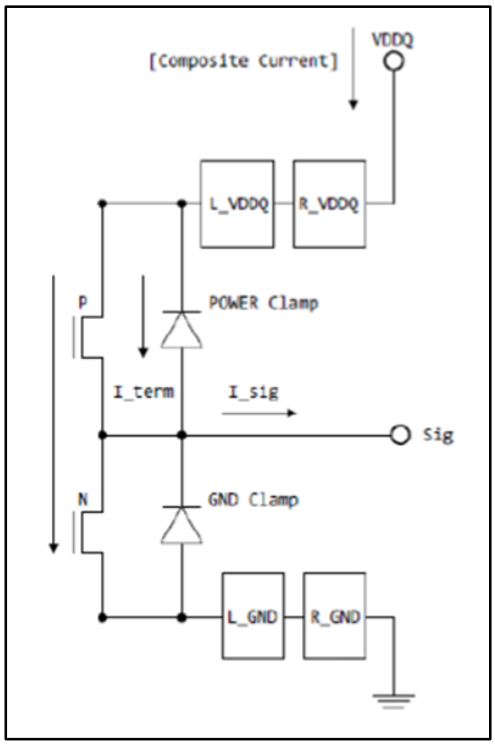


Figure 40. Composite Current – IBIS [17].

This case is to show the voltage noise at the power terminals but IBIS does not allow to parametrize the power noise at the output for a generic transmitter. For that reason, the model has to be improve.

It is necessary to define a PDN model to use in the extraction scheme. The PDN model was extracted from [8]. With the lumped elements, the circuit model is one-dimensional, where each level the packaging hierarchy is modeled by a pair of power and ground conductors and a decoupling capacitor across these conductors [8]. The Figure 41 shows the schematic lumped elements circuit.

The conductors are represented by the parasitic resistive and inductive impedances and the decaps by a series RLC circuit. The model represents the levels of regulator, board, package and on-chip conductors.

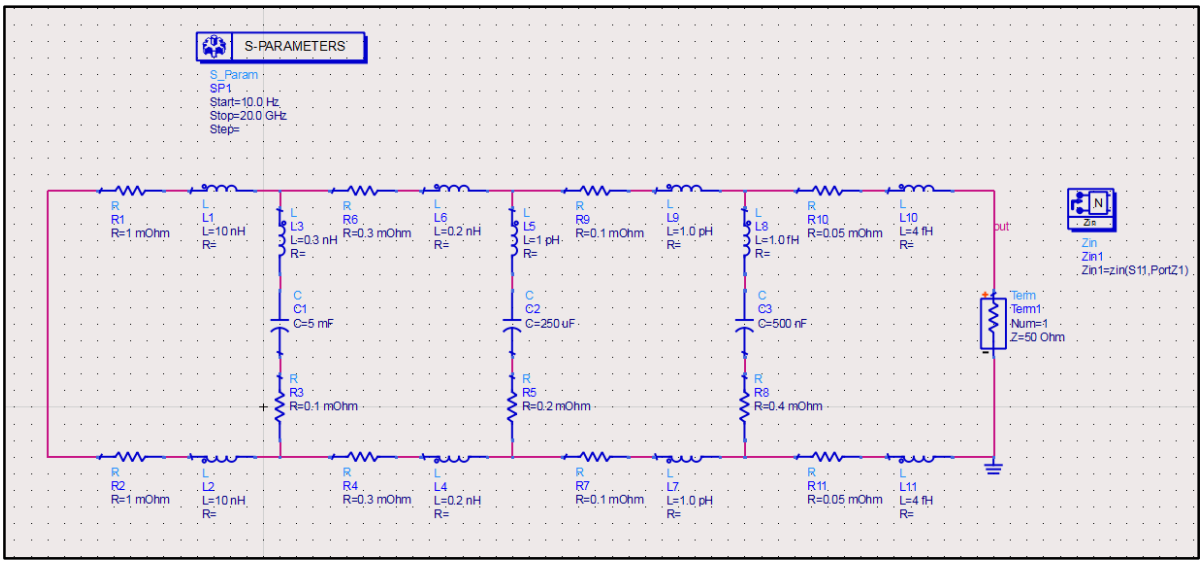


Figure 41. Power Delivery Network Model.

The Figure 2 allows to observe an approach developed [4] and consists in to perform the model with an extended block. The block functionality is based on introduce the function to describe the power noise effect at the output.

On the Synopsys framework, it is possible to extract the output waveform transient with power noise influence and without it. Both waveforms will use to find the effect of power noise in polynomial terms. However, because the way of the driver's behavior (waveform) is extracted is not possible to map according to the pull-up or pull-down electricals reference, because does not exist access to it. By this way, it was established finding the mapping function relating the output signal without induced power noise ("clean") and outputs affected by this effect ("dirty"). This correlation is performed by simulating the waveforms for different numbers of drivers in transition.

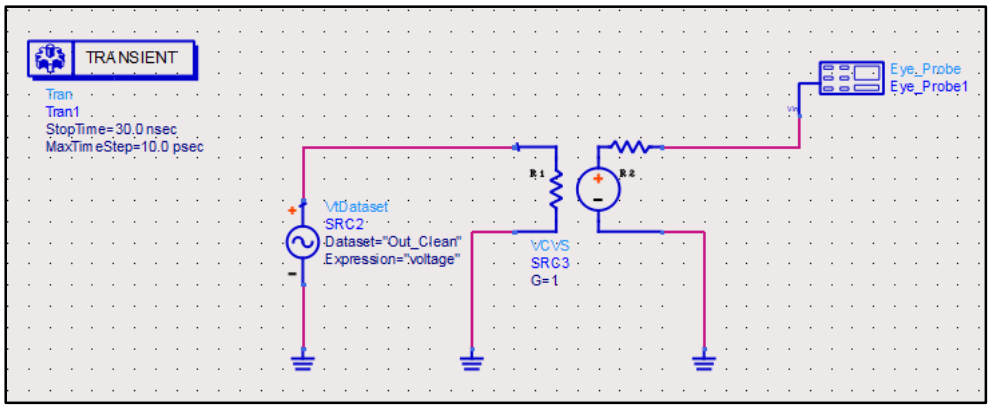


Figure 42. Testbench Correction to Map the PDN Noise Influence.

Thus, to map the power noise effect, it extracted from Synopsys framework each waveform "dirty" and relate it to the output signal "clean" which just contains the noise transmitter default. Thus, for a complete cycle of each stage it was interpolated between the two signals and the coefficients belonging to the characteristic function it is found. Thus, it is possible to vary the signal "clean" by a voltage controlled voltage source (VCVS) as shown in the Figure 42.

According to the interpolation, the characteristic equation that describes the mapping of the PDN noise to the output for **one** driver switching is as follows:

$$f(x) = 6 \times 10^{-7}x^2 + x - 1 \times 10^{-7} \quad (8)$$

where:

$$x: Output\ Voltage\ Driver\ without\ PDN\ Noise\ Influence$$

$$f(x): Output\ Voltage\ WITH\ PDN\ Noise\ Influence$$

Also, the characteristic equation that describes the mapping of the PDN noise to the output for a **five** driver switching is as follows:

$$f(x) = 6 \times 10^{-6}x^2 + x - 9 \times 10^{-7} \quad (9)$$

where:

$$x: Output\ Voltage\ Driver\ without\ PDN\ Noise\ Influence$$

$$f(x): Output\ Voltage\ WITH\ PDN\ Noise\ Influence$$

5. Validation of the Extraction Methodology

Respect to the validation of the macromodel, an environment of simulation has to be defined. This environment has to include: the driver macromodel, the PDN effect, a channel model and a termination as a receiver. Therefore, the macromodel results developed in SPICE have been the base to perform the voltage mapping for a generic driver, under the PDN model conditions. For that reason, comparing the mapping results with the Synopsys Framework results will be the base of the validation.

In this way, following to build a simulation environment for the macromodel, this chapter is focus in each environment stage, to present results and simulations of them.

5.1 Macromodel Extraction

Defined a basic environment of high-speed simulation, it is possible to validate the driver output waveform. The output waveform is described by polinomial function implemented with voltage controlled sources. These sources modifies the output voltage with the noise influence. The testbench in ADS framework to validate the power noise mapping is possible to observe in the Figure 42.

The Figure 43 shows the zoom output signal "clean" from transmitter. It simply to see that signal has equalization, so the noise effect occurs not only in the rising and falling edge of the output of the driver, but in all segments where the output signal has an abrupt change.

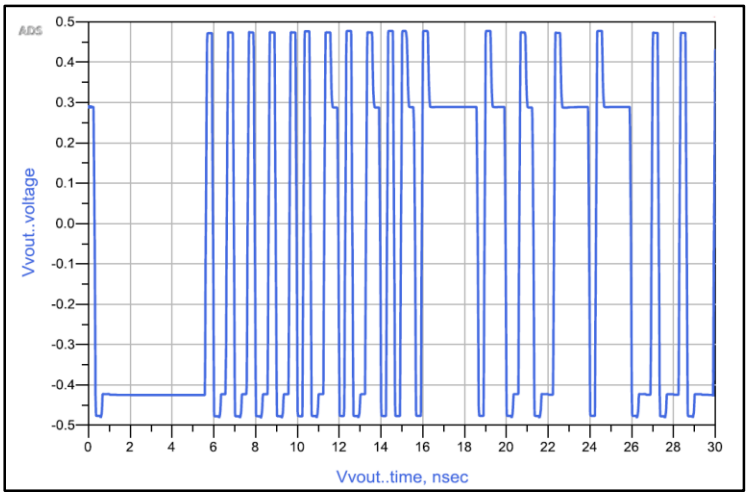


Figure 43. Voltage Output without PDN Noise Influence.

Also, the Figure 44 shows the transients with the power noise effect induced at the output driver when just one driver is switching. This waveform is performed following the schematic shown in the Figure 42.

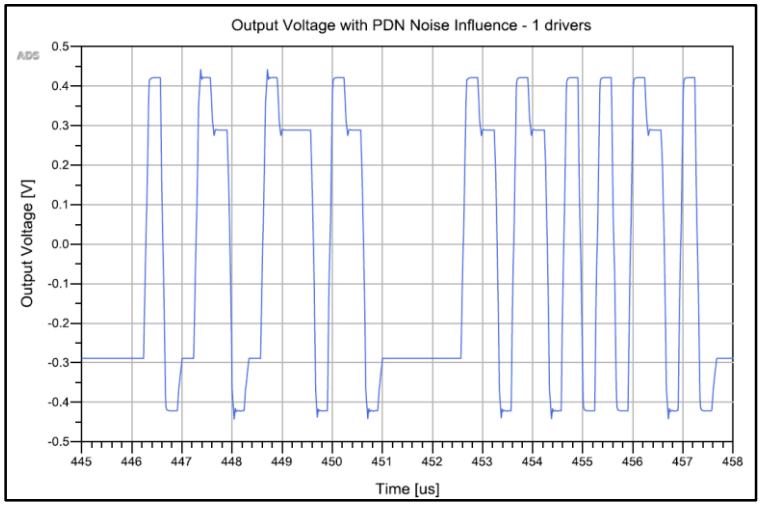


Figure 44. Output Voltage with PDN Noise Influence - 1 Driver (Zoom View).

Furthermore, a part of the transient with 5 drivers switching on the same time is shown in the Figure 45. Also, this output waveform is produced by the testbench in the Figure 42, with the corresponding polynomic effect.

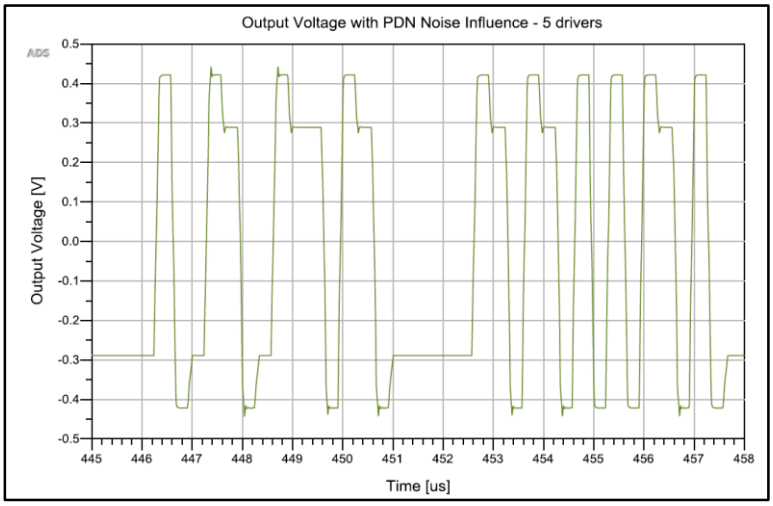


Figure 45. Output Voltage with PDN Noise Influence - 5 Drivers (Zoom View).

Then, the ADS waveform is extracted to compare with the SPICE waveform to validate the approximation. Figures 46 and 47 show the both waveform plotted in MATLAB to validate the behaviors.

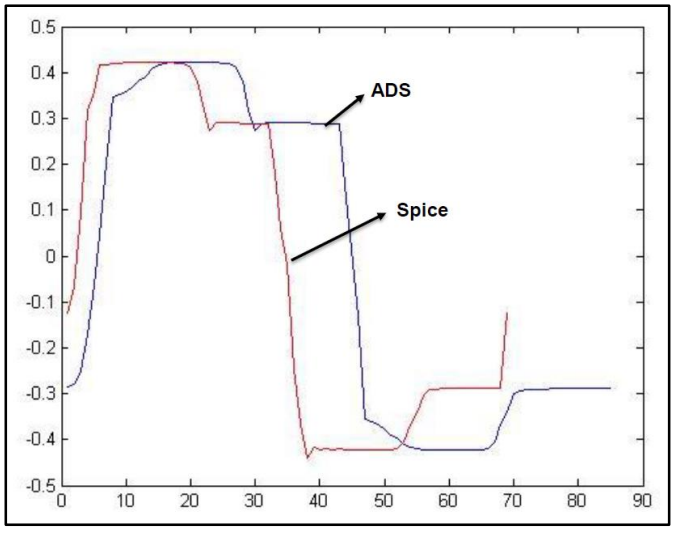


Figure 46. Validation with SPICE Model - 1 Driver.

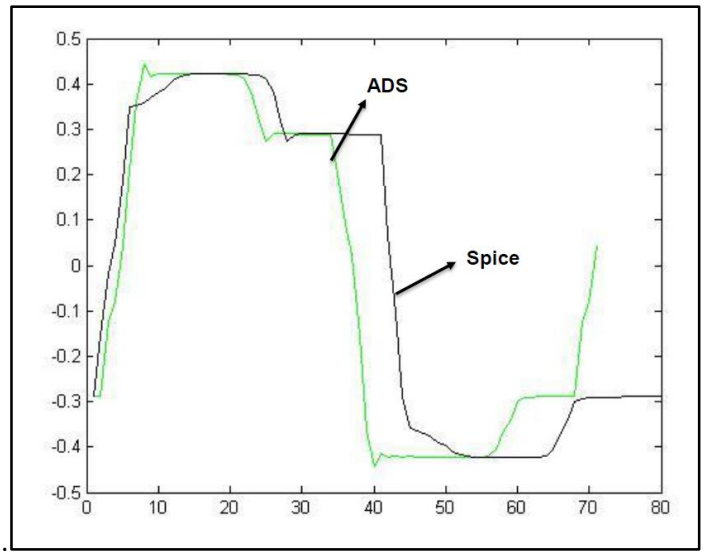


Figure 47. Validation with SPICE Model - 5 Drivers.

It is important to define that the signal of ADS is the corresponding model to compare with the original signal in SPICE. This generic model allows to map the influence of power noise for other drivers under the same simulation conditions.

5.2 Power Delivery Model Frequency Response

There is a variation at the source and reference terminals when the driver is switching in the transmission of information. This variation is also shown at the output driver terminal. The Figure 48 shows that voltage drop in function of the switching drivers in the same time.

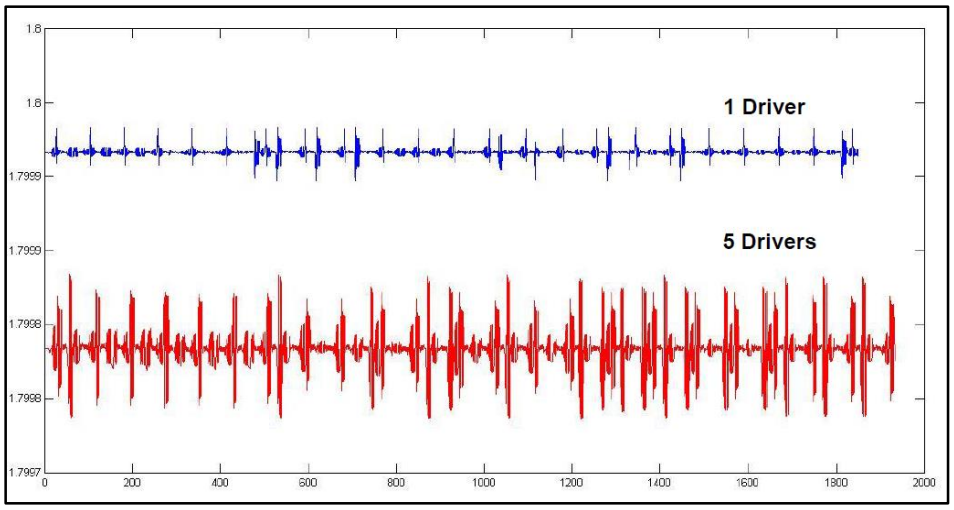


Figure 48. PDN Noise for 1 and 5 Drivers Switching.

Following the main goal of the research, the validation was performed in order to check the model accuracy and to test the result macromodel in a simulation environment.

In the Figure 48 it is possible to observe how the amplitude and points amount increase. It is because the exigency of current causes a higher voltage drop, taking the fundamental inductor laws analogy. For that, it is possible to conclude that the way to map the power noise effect at the output would be different in function of the number of drivers to simulate.

Also, the impedance magnitude of the PDN model is dependent of the frequency which the driver switch. The Figure 49 shown the frequency response for the model showed in the Figure 41.

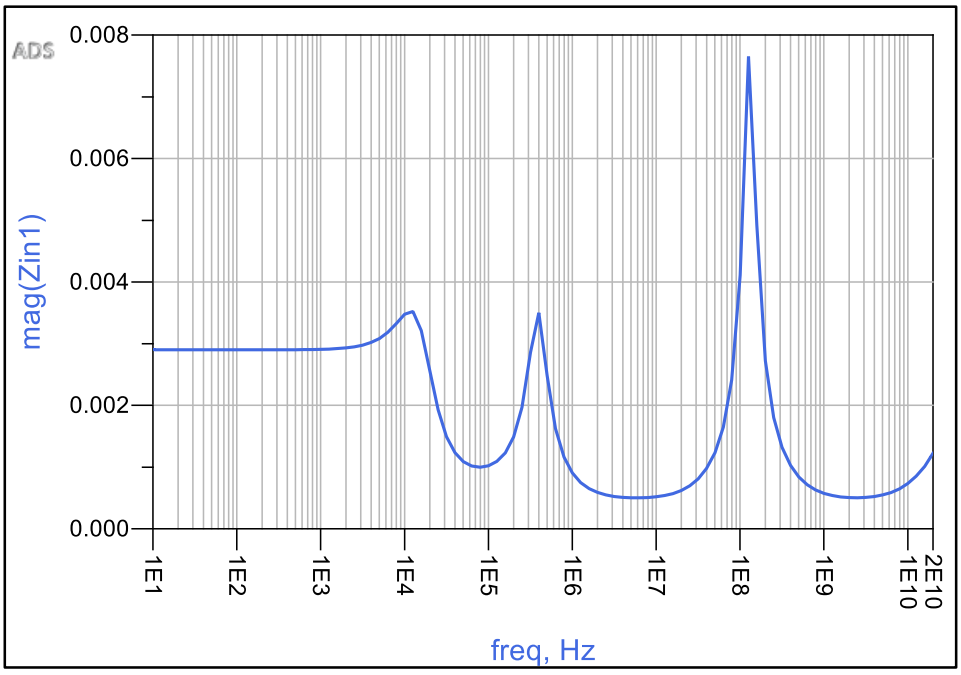


Figure 49. Frequency Impedance Response of PDN model.

This variation in the impedance magnitude refers directly to the voltage drop present in the PDN network. In this way, a channel model has to be defined to achieve the next stage of the environment simulation for the macromodel. Multilayer Substrate Simulator (MLSS), available at TET, TUHH; is a tool to perform a schemes of a PCB structure to build the channel as S-parameter blocks.

5.3 Channel Model

Referent to the channel model, two schemes of simulation had been performed with the tool available at TET, TUHH; ranging from full wave methods up to semi-analytical models. The tool allows the building of the interconnect structures and extract the S-parameter file which describes the transmission and reflection coefficients in function of the frequency, depending the ports. Some approaches will be described. In this work, two simplified structures had been extracted in order to use as S-parameters blocks to validate the macromodel.

MLSS Models

The multilayer substrate simulations allow a better prediction of channel responses in high-speed communications. At the Institute of Electromagnetic Theory was developed a channel response prediction algorithm for multilayer substrates simulations. The following simulations have been developed with the MLSS (Multilayer Substrate Simulator) software.

Several cases had been developed with the purpose to look the different effects due to physical design variations, such as traces geometry, traces length, dielectric losses etc. The used method let to ignore the boundary reflections.

1. **First Simulation Structure**

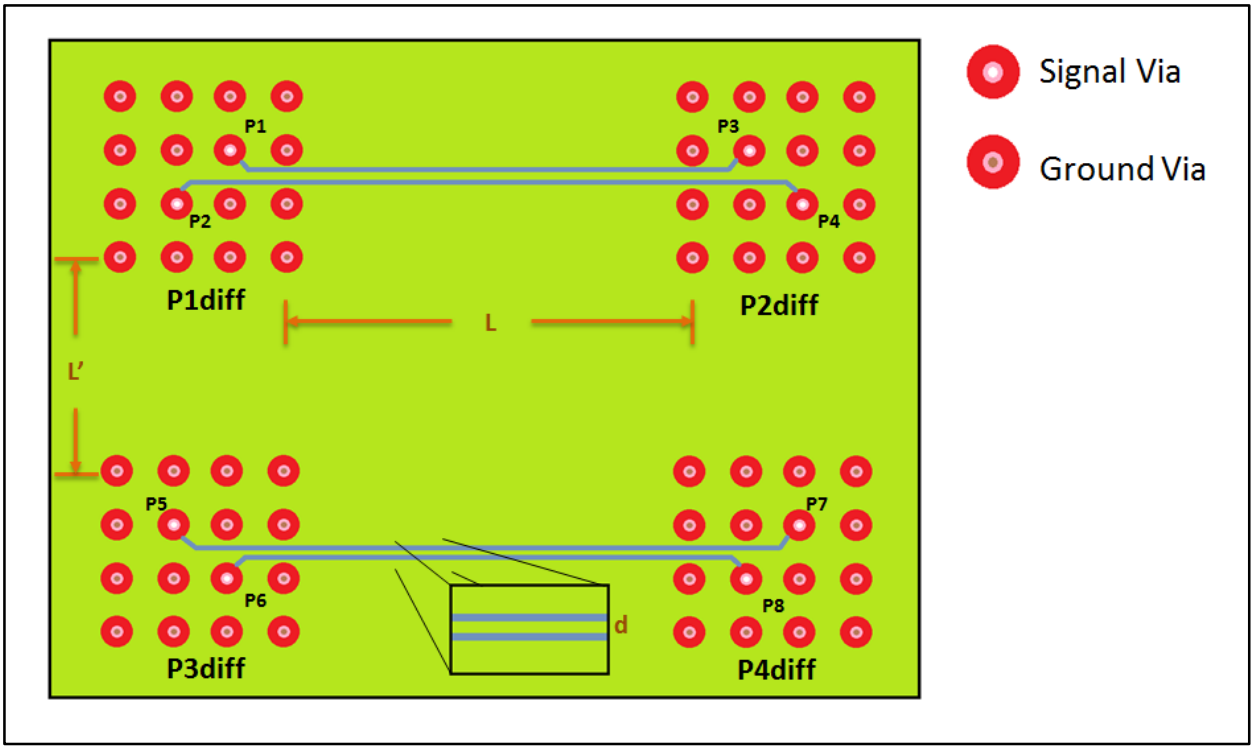
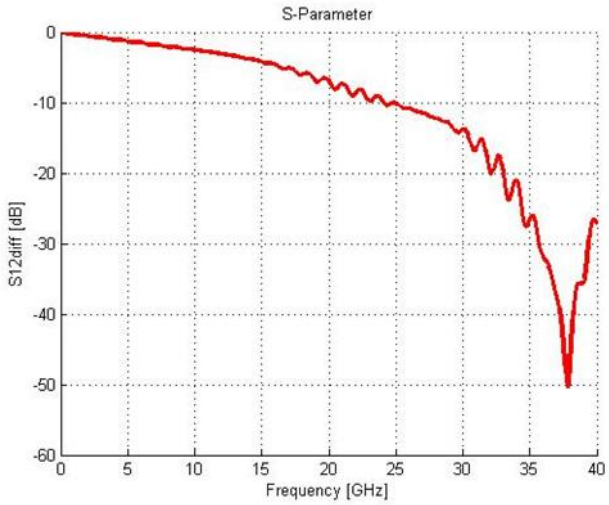


Figure 50. MLSS Model [1].

Features:

- *Via radius: 5 mil*
- *Via Pitch: 40 mil*
- *Antipad radius: 15 mil*
- *Cavity Thickness: 12 mil*
- *tanδ: 0.01*
- *ε_r: 3.8*
- *σ_{cooper}: 5.8e7*
- *8 cavities*
- *Method Zpp: pml_cim*
- *Traces position: 8 cavity*
- *L: 5 cm*
- *L': 500 mil*
- *d: 20 mil*

- S12diff [dB]:



- S34diff [dB]:

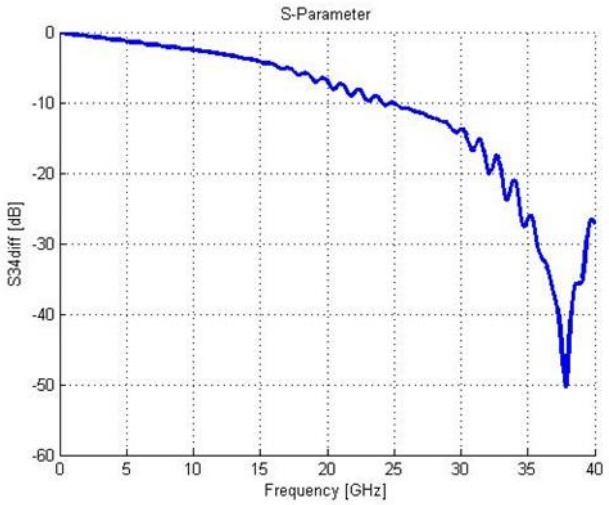


Figure 51. Model (1) Simulations [a].

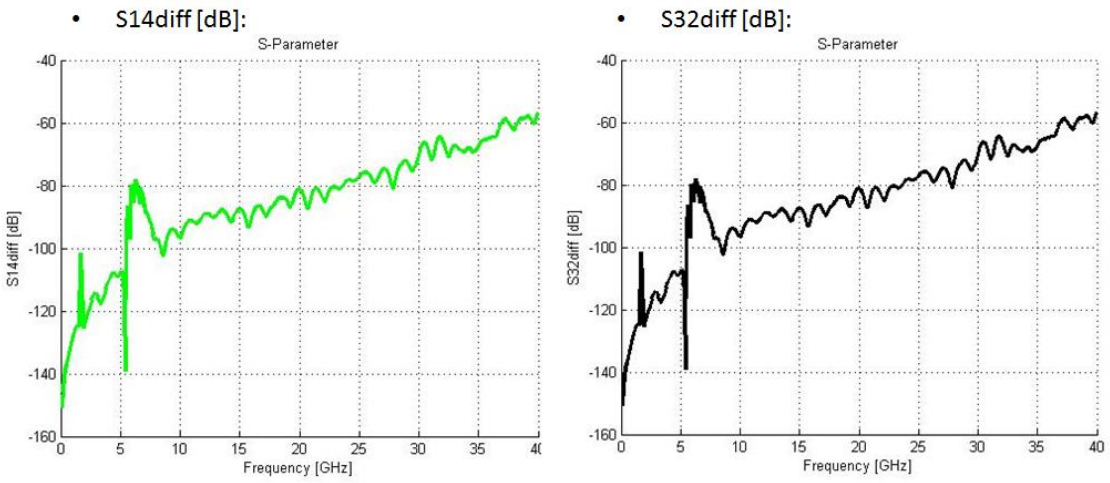


Figure 52. Model (1) Simulations [b].

The Figure 51 shows how the value of transmission coefficient decreases when the frequency increases. Therefore, the parasitic effects are directly involved in the reliability of the channel response. The Figure 52 and 53 denotes crosstalk among traces.

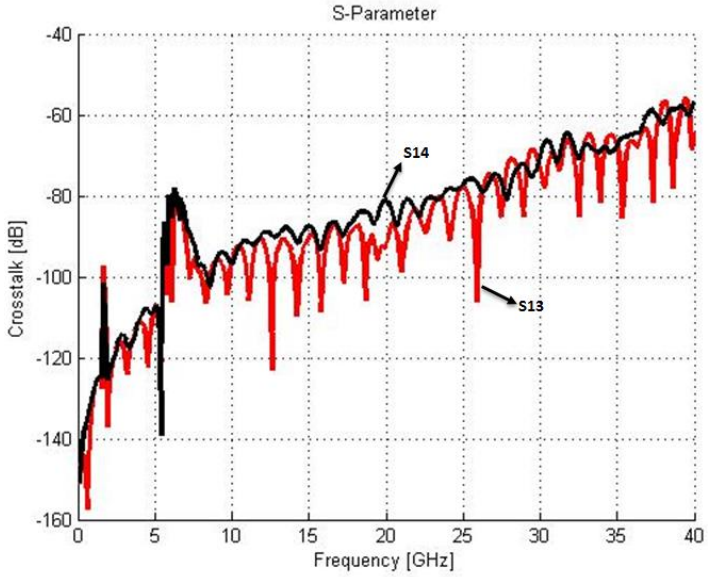


Figure 53. Model (1) Simulations [c].

2. Second Simulation Structure

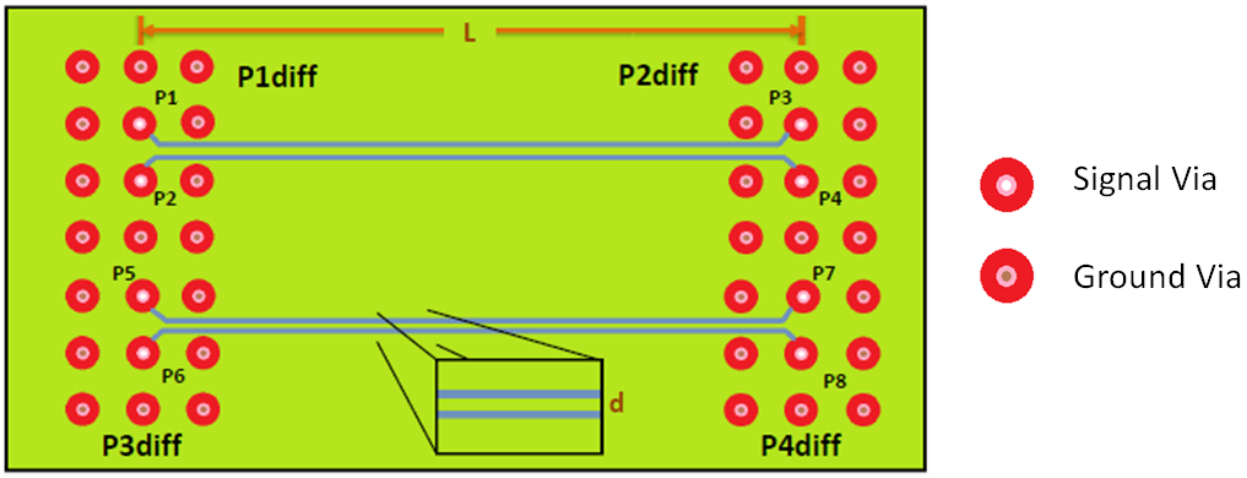


Figure 54. MLSS Model [2].

Features:

- *Via radius: 5 mil*
- *Via Pitch: 40 mil*
- *Antipad radius: 15 mil*
- *Cavity Thickness: 12 mil*
- *tanδ: 0.02*
- *ε_r: 3.8*
- *σ_{cooper}: 5.8e7*
- *8 cavities*
- *Method Zpp: pml_cim*
- *Traces position: 5 cavity*
- *L: 5 inch*
- *d: 6 mil*
- *Blind Vias: avoid Stub Length Resonances*

- Single-ended behavior:

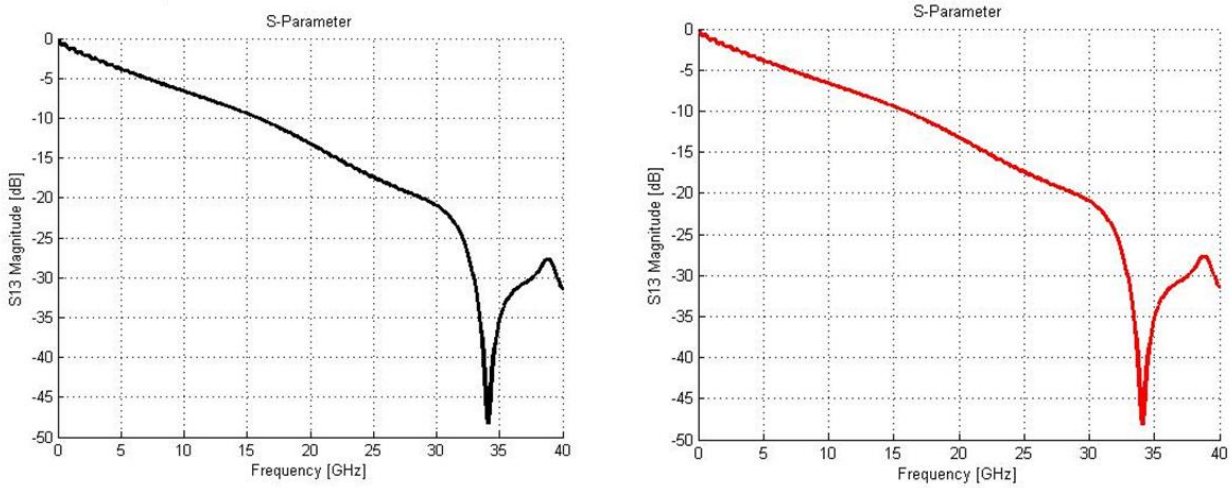


Figure 55. Model (2) Simulations [a].

- Single-ended behavior:

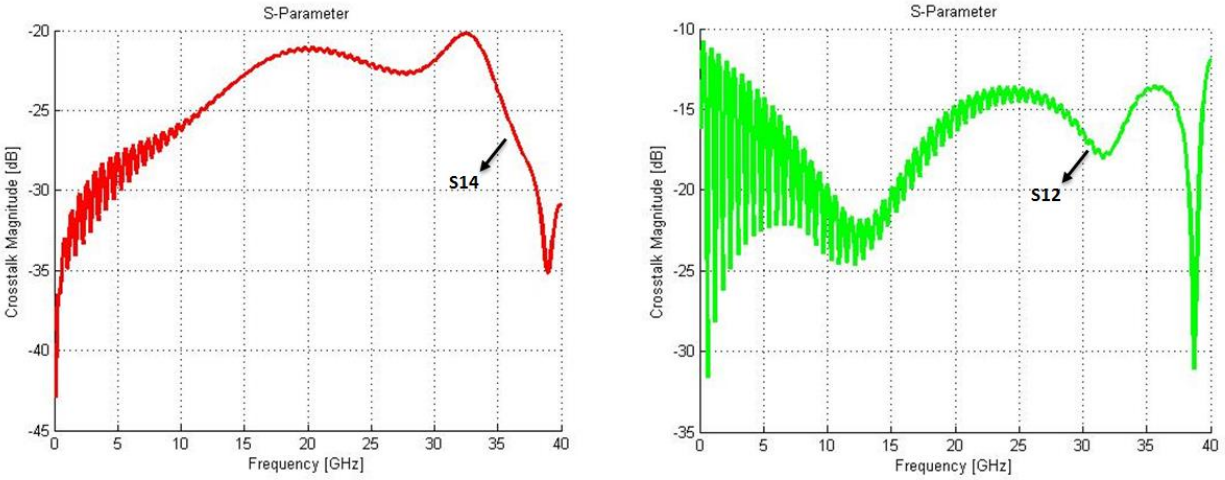


Figure 56. Model (2) Simulations [b].

- Differential behavior:

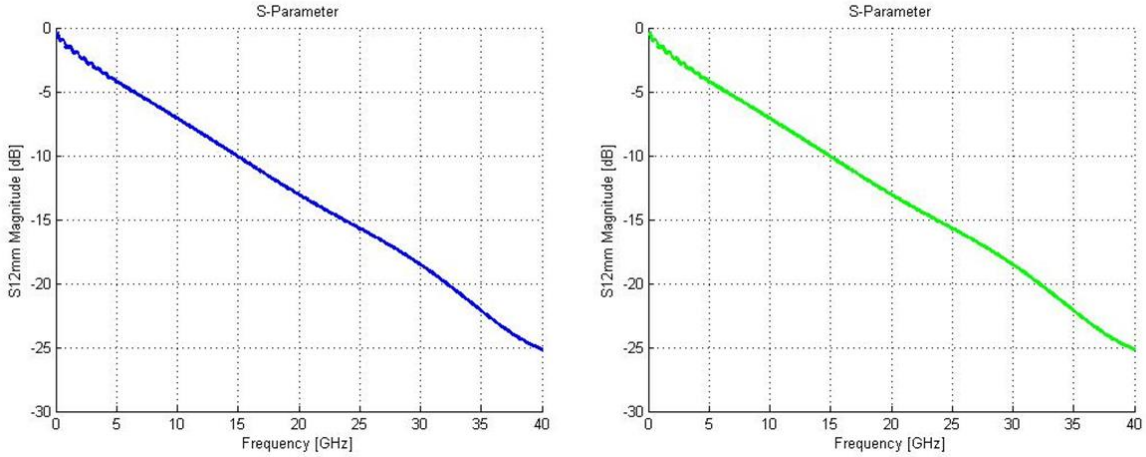


Figure 57. Model (2) Simulations [c].

- Crosstalk - Differential behavior:

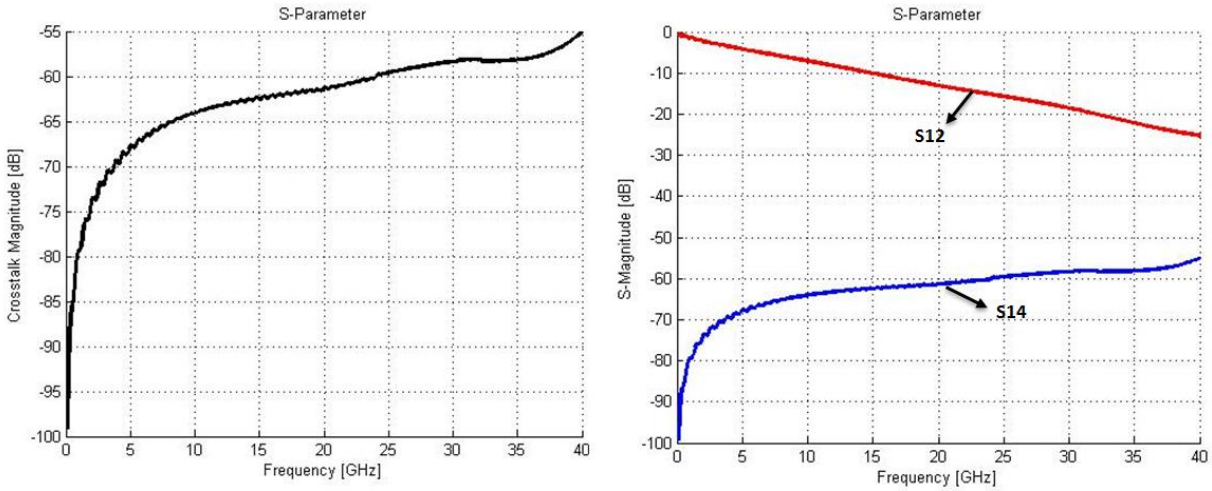


Figure 58. Model (2) Simulations [d].

5.4 Simplified Link Simulation

The simulation environment for a simplified high-speed channel is shown in Figure 59. MLSS simulation models have been used to create the channel model for the time domain. The signal at the net “out_rx” is show in the Figure 59 and represents the scope as a receiver input using the extracted macromodel from chapter 4.

Regarding of the simulation is important to declare the different parts of the channel, presented in the previous sections. The “VtDataset” represents the macromodel or the output driver waveform. The way of the extraction refer how the output waveform is not depend of a pull-up/down reference. For that reason to include the complete PDN model block between the output and the reference on the testbench is not possible at this point. The PDN model influence is considered in the voltage controlled sources.

For the channel model, the ADS framework allows to use S-parameter blocks. Instancing the 8-ports S-parameter component is possible to import the touchstone file concerning with simulated the channel model.

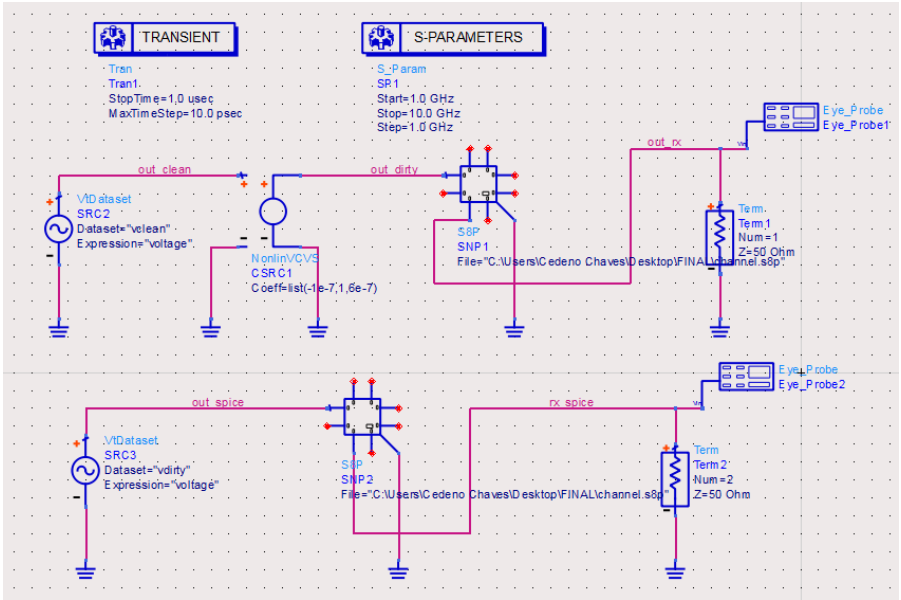


Figure 59. Simplified circuits describing the basic structures of a communication link, including: driver model, channel, PDN noise effect.

Figure 59 presents the macromodel scheme of simulation (top circuit) and its equivalent with the waveforms imported directly from the Synopsys SPICE simulator (bottom circuit). The Synopsys circuit does not present the VCVS element because the power noise is inherent on the waveform in the corresponding VtDataSet (the traditional time domain simulation approach without macromodeling). The results of the simulations can be found in the next Figures (62-63).

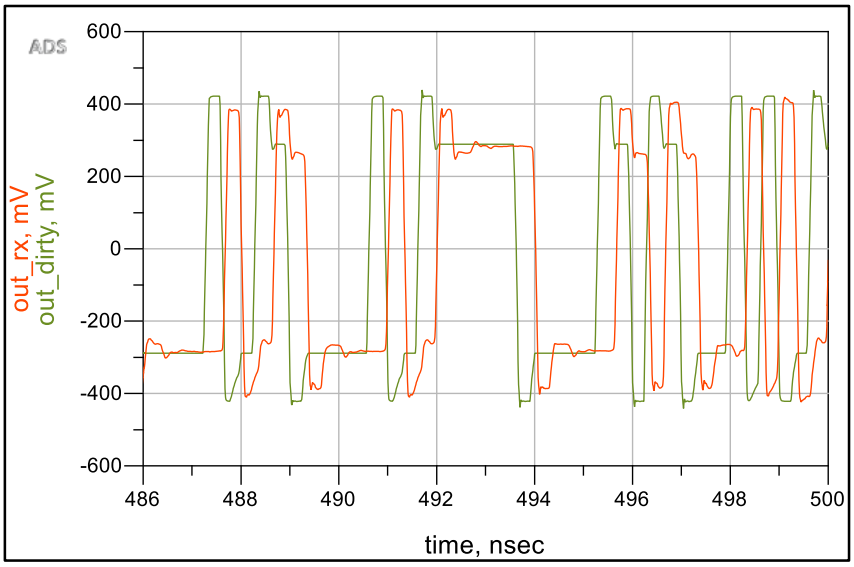


Figure 60. Macromodel voltage waveforms. Channel Structure 1.

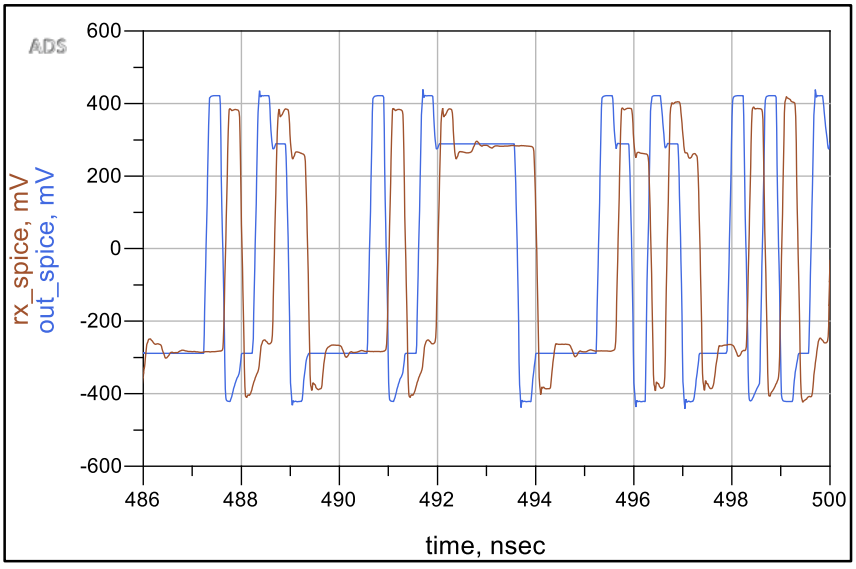


Figure 61. Synopsys voltage waveforms. Channel Structure 1.

The transient waveforms were extracted with a data rate of 3Gpbs. A 1us waveform allows to export approximated 3000 bits to use in the simulation. With the Figures above it is possible to conclude that the methodology proposed in this work indicates how the method conduces a good approximation to perform high-speed communication simulations described by its waveform similitudes.

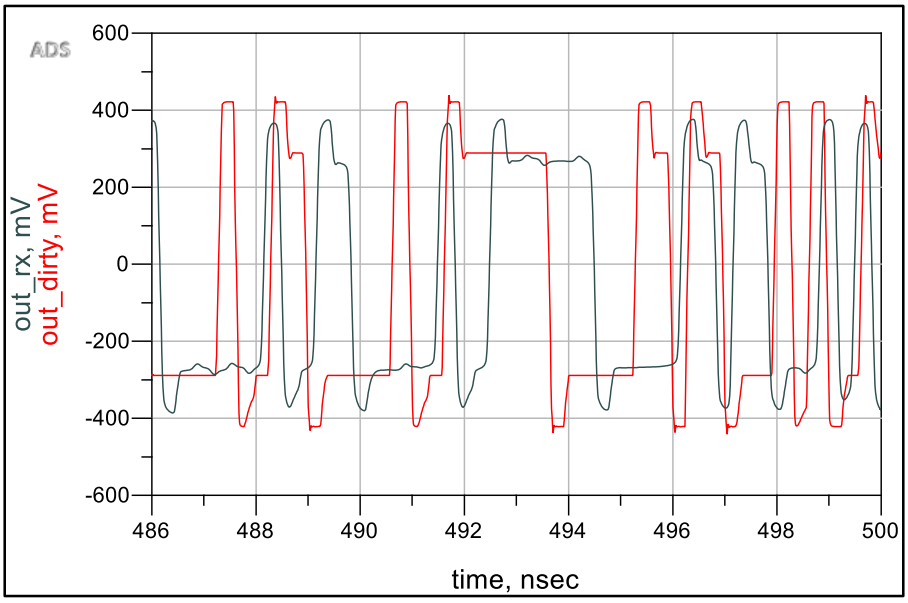


Figure 62. Macromodel voltage waveforms. Channel Structure 2.

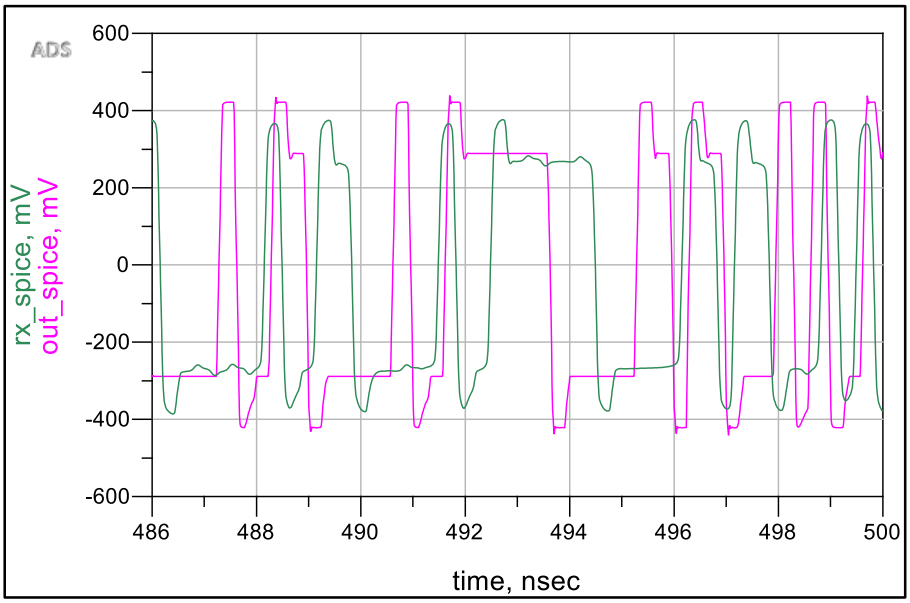


Figure 63. Synopsys voltage waveforms. Channel Structure 2.

According with the validation, the waveforms from ADS framework (Power Noise Mapping) and HSPICE tool of Synopsys framework have been simulated under the same simulation environment. The Figure 60 shows the waveform before to pass through the channel structure 1 and the signal at the receiver, represented by the termination of 50 ohms. The Figure 61 refers to the HSPICE output waveform with the PDN noise influence under the same simulation conditions than the Figure 60. In the Figures 60 and 61 it is possible to see how the correlation between them is very similar and indicates that the extraction approach could be useful for more complex scenarios.

Also, the same conditions are present in the Figures 62 and 63 with the difference that the simulation environment, the case was the different channel model, in this case the channel structure 2. As shown the Figures 62 and 63, the signal responses present a high degree of similarity.

6. Conclusions and Recommendations

The proposed methodology to extract the driver macromodel was useful to perform basic simulations resembling simplified high-speed channels with basic interconnect structure models. The methodology is potential to handle the power noise.

The LVDS drivers are a very common configuration for high-speed communications. For that reason, it was chosen to be the driver topology to inspect in this work. The driver was implemented and validated at schematic level with the XFAB 0.18 CMOS process using the Synopsys Custom Design Flow.

For this work, the macromodeling generation methodology was based on the IBIS Specification, an industrial standard widely adopted for signal integrity applications. The methodology was extended based on [4]. It approach to map the effect of power noise at the output for single-ended drivers. Due to issue with the stability of the IBIS commercial simulator available, the methodology was validated with a SPICE-like simulator by setting up a simple channel simulation.

The parameterization of the power noise model at the output to simulate generic transmitters is not straightforward achieved in the methodology at this point. Therefore, it is recommended to find out a more convenient driver modeling approach. For mapping the power noise, IBIS methodology could not be a very flexible approach because the necessity to extend the macromodel. The differential Modeling based on IBIS methodology becomes complicated when the model flow has to separate and tabulate the common-mode and differential behavior information. This separation has to follow the intrinsic IBIS formats, and depends to the driver.

In order to validate the macromodeling extraction methodology, a test for representative high-speed link was proposed, where two simple channels models for the signal path and the power distribution network was generated.

As a recommendations, the Power Distribution Network models are based on the different stages, from the principal distribution energy block to the on-chip terminals. The models are complex, frequency operations dependents. Thus, it is possible to improve the PDN Model with a more accurate model.

Despite to the problems with the IBIS simulator, a system level simulations had been performed which indicates the methodology can be useful to build the extraction. A way to improve the future works related to macromodel extraction is to evaluate other alternatives more adequate to map the power noise. Also, the macromodel validation would be more accurate with more realistic models with equalization.

7. References

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8. Appendix

8.1 Stripline Structure build in CST Microwave Studio

For an introduction to the multilayer substrate simulations, a Stripline was developed and according with it to analyze and extract the channel response as S-Parameters blocks.

The following simulations were performed in CST Microwave Studio, available at TET, TUHH. A stripline was built to extract the S-Parameters response. The exercise followed as a guide the document: "*Exercise: FIT Time Domain Simulation*", developed at TET, TUHH [7].

The construction flow is shown in the next figures.

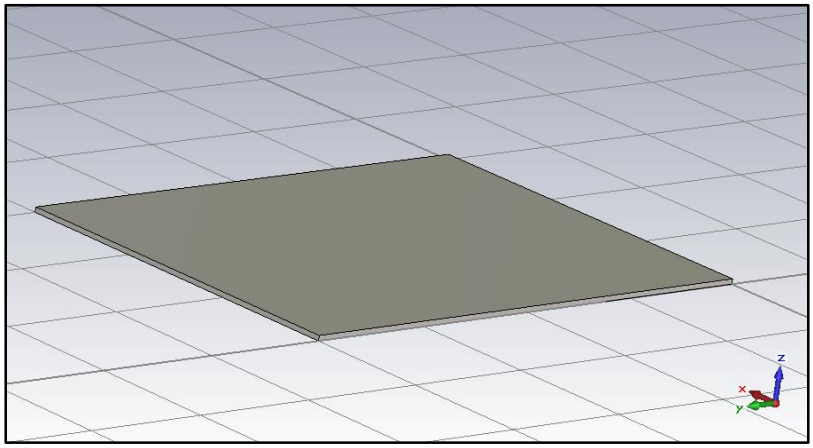

Figure 64. Stripline Construction Flow (1).

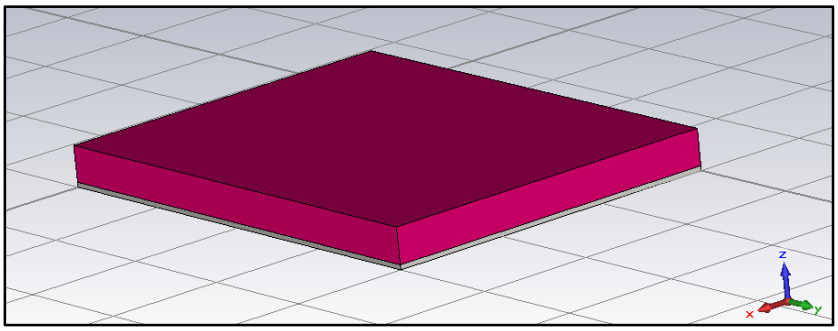

Figure 65. Stripline Construction Flow (2).

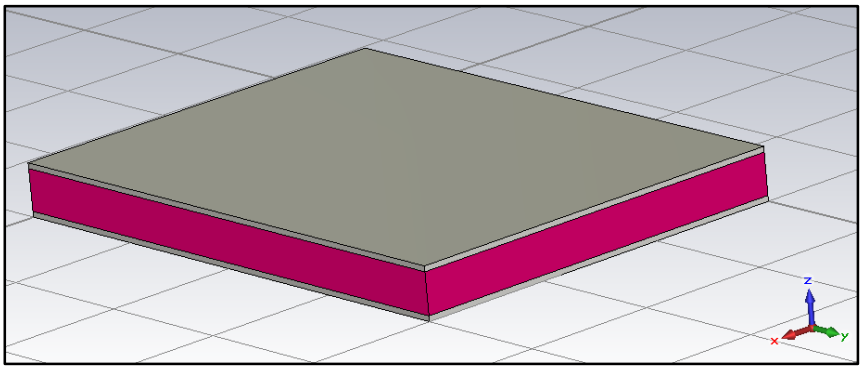

Figure 66. Stripline Construction Flow (3).

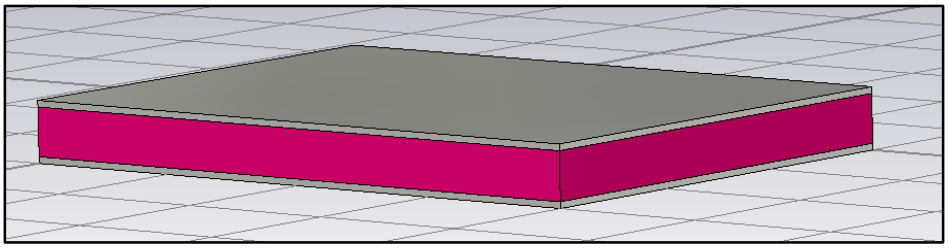

Figure 67. Stripline Construction Flow (4).

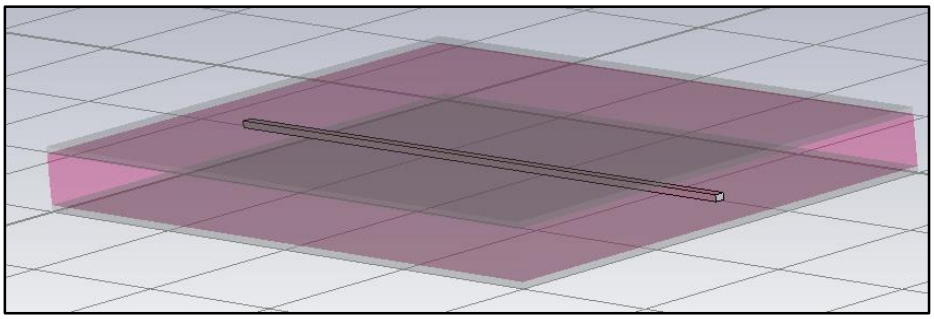

Figure 68. Stripline Construction Flow (5).

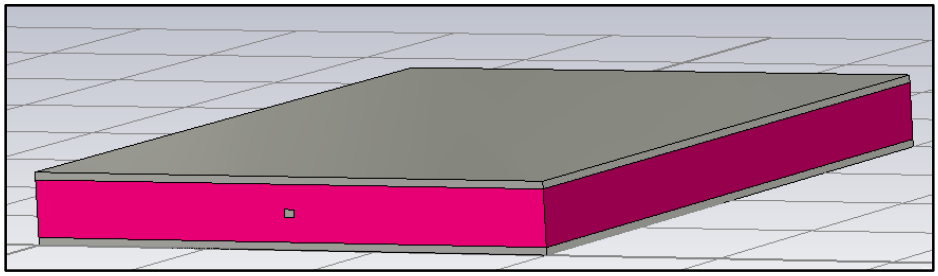

Figure 69. Stripline Construction Flow (6).

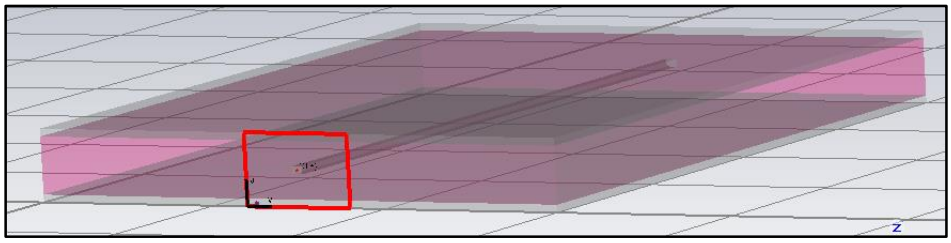

Figure 70. Stripline Construction Flow (7).

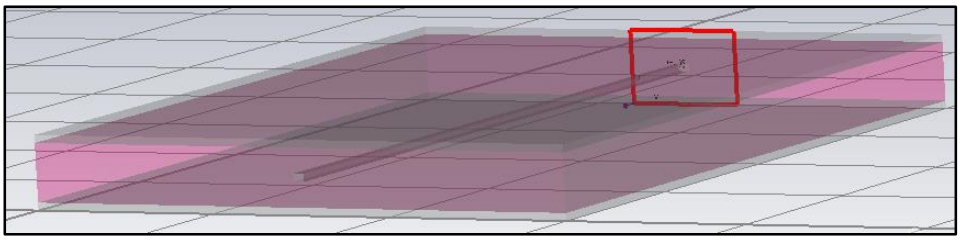

Figure 71. Stripline Construction Flow (8).

Regarding to the channel responses, the following figures show the transmission and reflection coefficients in function with the frequency. The structure was excited with a waveguide ports.

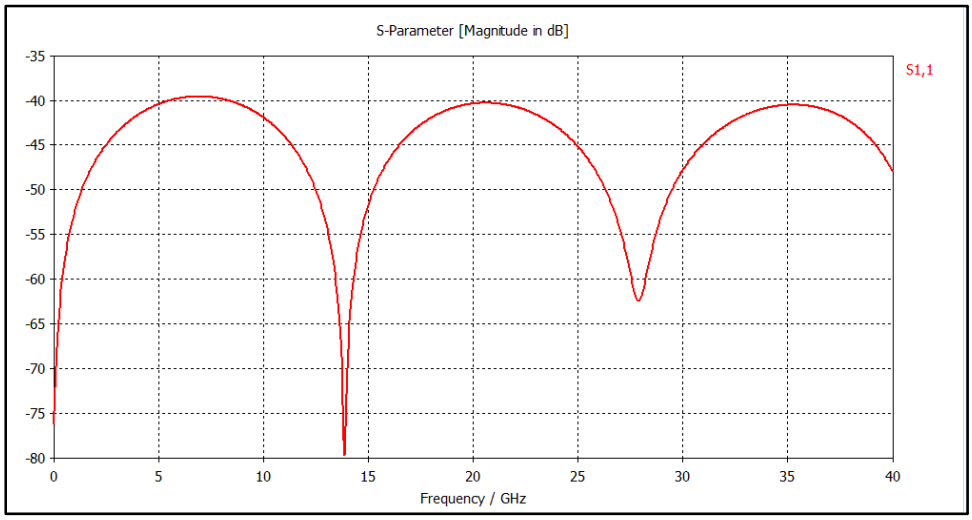

Figure 72. Reflection Coefficient - Port 1.

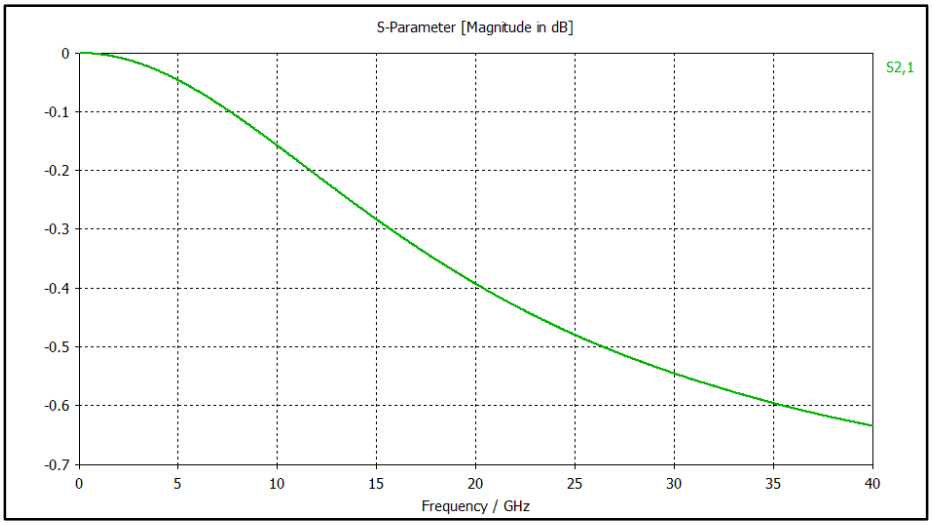

Figure 73. Reflection Coefficient - Ports 2,1.

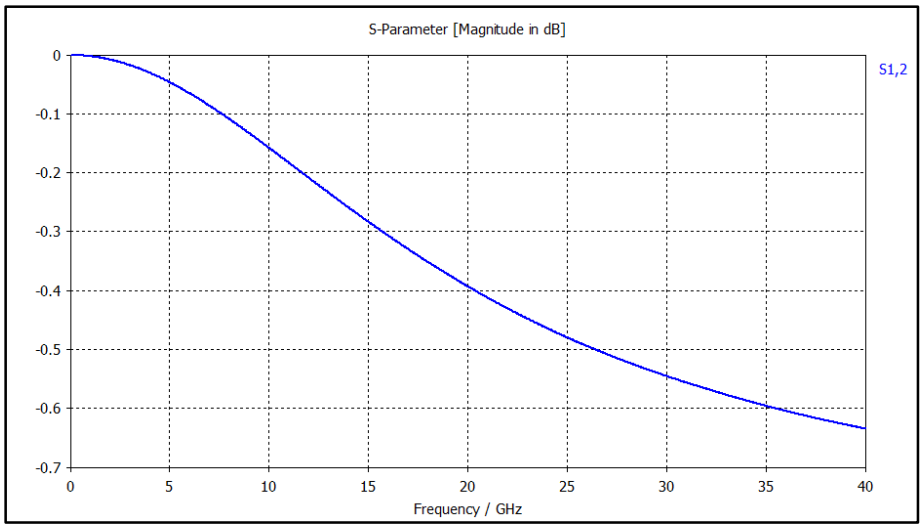

Figure 74. Transmission Coefficient - Ports 1,2.

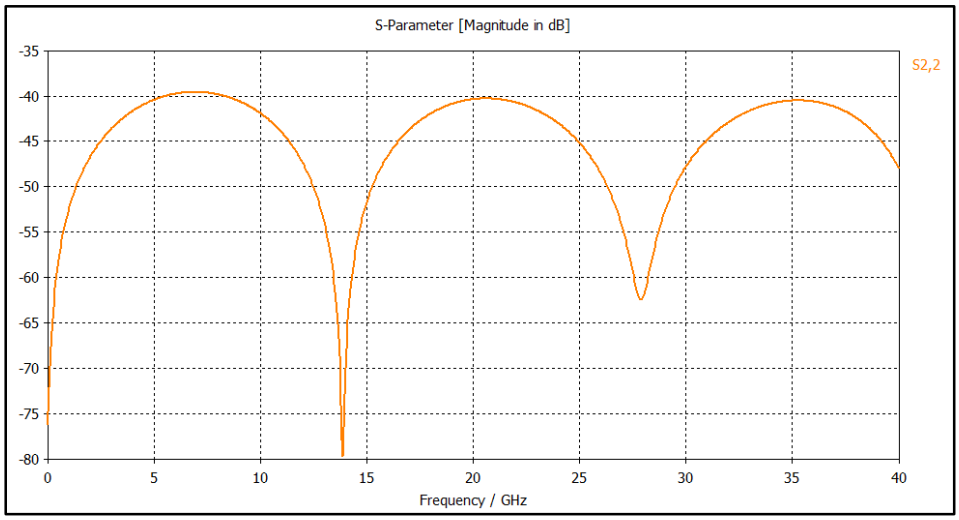

Figure 75. Reflection Coefficient - Port 2.

The resonances frequencies can be calculated following the next equation:

$$\lambda = \frac{c}{\sqrt{\varepsilon_r} f_n}$$

This is possible because the first minimum value of the reflection coefficient is located in lambda half distance. The *l* value is 200 mil ≈ 5.08 mm.

$$f_1 = \frac{c}{2 * l * \sqrt{\varepsilon_r}} \approx 13.34\ GHz$$

The second value is located in lambda distance. Then:

$$f_2 = \frac{c}{l * \sqrt{\varepsilon_r}} \approx 26.68\ GHz$$