Effect of Clock Jitter Error on the Performance Degradation of Multi-bit Continuous-Time ΣΔ Modulators With NRZ DAC

R. Tortosa, J.M. de la Rosa, A. Rodríguez-Vázquez and F.V. Fernández

Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC),
Ed. CNM-CICA, Av. Reina Mercedes s/n, 41012 Sevilla, SPAIN.
Phone: +34955056666, Fax: +34955056686, E-mail: {tortosa|jrosa|angel|pacov}@imse.cnm.es

***Abstract*– This paper analyses the effect of the clock jitter error in multi-bit continuous-time ΣΔ modulators with non-return-to-zero feedback waveform. Derived expressions show that the jitter-induced noise power can be separated into two main components: one that depends on the modulator loop filter transfer function and the other one due to the input signal parameters, i.e amplitude and frequency. The latter component, not considered in previous approaches, allows us to accurately predict the resolution loss caused by jitter, showing effects not taken into account up to now in literature which are specially critical in broadband telecom applications. Moreover, the use of state-space formulation makes the analysis quite general and applicable to either cascade or single-loop architectures. Time-domain simulations of several modulator topologies intended for VDSL application are given to validate the presented analysis.†**

I. INTRODUCTION

Continuous-Time (CT) Sigma-Delta Modulators (ΣΔMs) are good candidates for the implementation of Analog-to-Digital Converters (ADCs) in broadband communication systems. In addition to offer an intrinsic antialiasing filtering, these modulators provide potentially higher sampling rates with lower power consumption than their Discrete-Time (DT) counterparts [1][2]. However, CT ΣΔMs are more sensitive than DT ΣΔMs to several circuit non idealities. One of their major degrading factors, especially in high-speed applications, is due to uncertainties in the clock-signal edges, commonly referred to as clock jitter [1].

As sampling rates increase, clock jitter is becoming an ever-important consideration for the design of CT ΣΔMs. In fact, this error has been object of several studies reported in open literature [1][3]-[7]. Most of them were carried out considering ΣΔM architectures with an internal single-bit quantizer and a Return-to-Zero (RZ) DAC. However, multi-bit quantization has been used in most silicon prototypes achieving medium-high resolutions (11-14 bit) within high signal bandwidths (1-15 MHz) [8]-[10]. The combined used of high-order (3rd-4th order) single-loop architectures with multi-bit (3-6 bit) quantization allows to reduce the oversampling ratio (normally < 12) while guaranteeing stability and robustness with respect to circuit parameter tolerances – the latter being a very critical error in CT ΣΔMs [1][2]. In addition to improve resolution, multi-bit quantization can reduce the sensitivity of CT ΣΔMs to clock jitter if a Non-Return-to-Zero (NRZ) feedback waveform is used in the DAC [9]. Therefore, its study is needed in order to optimize the modulator performance in terms of sensitivity to jitter error.

The analysis of clock jitter in CT ΣΔMs considering a NRZ feedback waveform is mathematically more complex than using a RZ pulse shaping. This is the reason why, in most cases, designers resort to semi-empirical estimations based on simulation results and consider a white-noise model for the jitter error [1][5][9]. To the best of the authors' knowledge, only the work in [7] takes into account the effect of the modulator loop filter transfer function on the in-band jitter noise power of CT ΣΔMs with NRZ DAC. However, the analysis in [7] does not consider the effect of input signal for the sake of simplicity.

This paper analyzes the effect of signal-dependent clock jitter in multi-bit CT ΣΔMs with NRZ embedded DAC. State-space formulation [11] is used to derive closed-form relations among jitter error, sampling frequency, modulator specifications (resolution and signal bandwidth), circuit topology (loop filter transfer function and number of bits of the internal quantizer) and input signal parameters (amplitude and frequency). The results of this study show effects not considered in previous approaches which might become critical in medium- and high-frequency applications. In addition, the use of the state-space formulation allows for the generalization of the analysis, being applicable to any kind of CT ΣΔMs considering either cascade or single-loop architectures. As an illustration several modulators using either single-loop or cascaded topologies, designed for VDSL, are simulated to demonstrate the theoretical predictions.

†. This work has been supported by the Spanish Ministry of Science and Education (with support from the European Regional Development Fund) under contracts TEC2004-01752/MIC and TIC2003-02355.

II. MODELING THE CLOCK JITTER ERROR IN NRZ CT ΣΔMs

Fig.1 shows the conceptual block diagram of a single-loop CT ΣΔM. The loop filter is CT and the sampling operation is realized before quantization instead of at the modulator input as done in the case of DT ΣΔMs. Thus, the output signal, $y(n)$ [††], is DT, the input signal, $x(t)$, is CT and a DT-to-CT transformation is implemented by the DAC to create the CT feedback signal, $y(t)$. Therefore, there are two clocked building blocks subject to jitter error: the sampler and the DAC. The error introduced through the sampling process is reduced by the loop gain and shaped in the same way as the quantization noise and hence, its effect can be neglected. On the contrary, the jitter error associated to the DAC directly adds with the input signal, thus increasing the in-band noise power and degrading the modulator performance.

Traditionally, RZ feedback DACs have been used in CT ΣΔMs in order to overcome inter-symbol interference due to unequal rising and falling edges of the feedback DAC waveform. However, a multi-bit RZ DAC is more sensitive to clock jitter than a multi-bit NRZ DAC [9]. This is illustrated in Fig.2 by showing the arbitrary output feedback waveform[†††] of a multi-bit DAC considering both a NRZ and a RZ pulse shaping with a 0.5 duty cycle. Note that, as the output

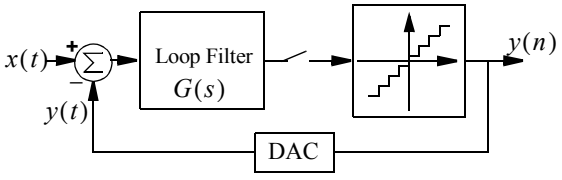

Fig. 1: Conceptual block diagram of a single-loop CT ΣΔM.

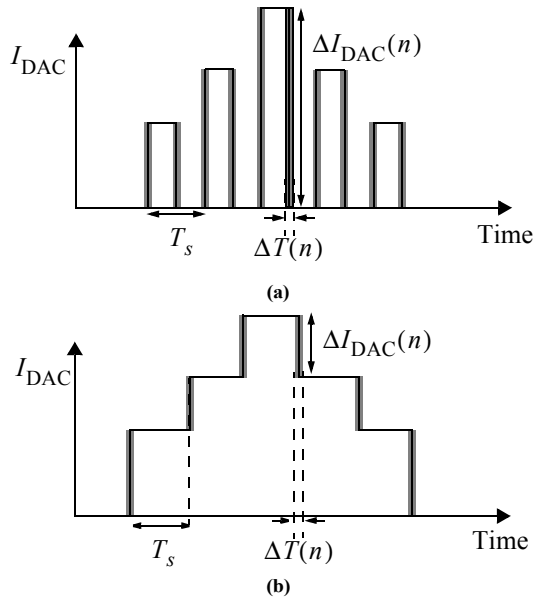

Fig. 2: Feedback DAC pulse shaping. (a) RZ DAC. (b) NRZ DAC.

signal (I_{DAC}) of RZ DAC goes back to zero at each clock cycle, signal transitions ($\Delta I_{\mathrm{DAC}}(n) \equiv I_{\mathrm{DAC}}(n)$) will be larger than in the case of NRZ DACs ($\Delta I_{\mathrm{DAC}}(n) \equiv I_{\mathrm{DAC}}(n) - I_{\mathrm{DAC}}(n-1)$). Furthermore, increasing the number of bits of the quantizer and DAC reduces significantly the signal transitions in the case of NRZ DAC and hence, lower amounts of charge ($\Delta Q(n) \cong \Delta I_{\mathrm{DAC}}(n) \cdot \Delta T(n)$) are loss during clock transitions as a consequence of the time uncertainty, $\Delta T(n)$. However, in a RZ DAC this reduction is practically non-existent.

Note from Fig.2 that the DAC output waveform with jitter can be seen as the sum of an unjittered output waveform and a stream of pulses with amplitude $\Delta I_{\mathrm{DAC}}(n)$ and width $\Delta T(n)$ – often referred to as *jitter error sequence* [1]. In the case of a NRZ DAC, the jitter error sequence can be related to the modulator output signal using the following relationship [12]:

$$\varepsilon(n) = (y(n) - y(n-1))\frac{\Delta T(n)}{T_s} \tag{1}$$

where T_s is the sampling period.

Assuming that the input signal and the quantization error are uncorrelated and that $\Delta T(n)$ is a Gaussian random process with zero mean and standard deviation $\sigma_{\Delta T}$, the power of the jitter error signal can be written as:

$$P_{\varepsilon} = E\{\varepsilon(n)^2\} = \frac{\sigma^2_{\Delta T}}{T_s^2} E\{[y(n) - y(n-1)]^2\} \cong$$
$$\cong \frac{\sigma^2_{\Delta T}}{T_s^2}(E\{(\Delta x_n)^2\} + E\{(q(n) - q(n-1))^2\}) \tag{2}$$

where $\Delta x_n \equiv [x(n) - x(n-1)]$, $E\{.\}$ stands for the mathematical expectation [13] and $q(n)$ is the shaped quantization noise, given by:

$$q(z) = N_{TF}(z)e(z) \tag{3}$$

where $N_{TF}(z)$ represents the quantization Noise Transfer Function and $e(z)$ is the quantization error – assumed to be a white noise source.

Considering a sinewave input signal of amplitude A and angular frequency $\omega_i = 2\pi f_i$, Δx_n can be simplified as:

$$\Delta x_n \cong \frac{d}{dt}x(t)\Big|_{t = nT_s} \cdot T_s = A\omega_i T_s \cos(\omega_i(n-1)T_s) \tag{4}$$

and hence,

$$E\left\{(\Delta x_n)^2\right\} =$$
$$= T_s^2 A^2 \omega_i^2 E\left\{(\cos(\omega_i(n-1)T_s))^2\right\} = \frac{T_s^2 A^2 \omega_i^2}{2} \tag{5}$$

The expectation value of $\Delta q_n \equiv [q(n) - q(n-1)]$ can be derived from (3) giving:

---

††. In order to simplify the notation, $y(nT_s)$ is written as $y(n)$ with T_s being the sampling period.

†††. A current-mode DAC is assumed in this example.

$$E\left\{(\Delta q_n)^2\right\} = E\left\{(Z^{-1}[(1-z^{-1})N_{TF}(z)e(z)])^2\right\} = \quad (6)$$
$$= \frac{X_{FS}^2}{12\pi(2^B-1)^2}\int_0^{\pi}\left|(1-e^{-j\omega})N_{TF}(e^{-j\omega})\right|^2 d\omega$$

where X_{FS} and B are the full-scale and the internal number of bits of the quantizer, respectively.

From (2), (5) and (6), we obtain:

$$P_{\varepsilon} \cong \left(\frac{\sigma_{\Delta T}}{T_s}\right)^2 \cdot \left(\frac{A^2\omega_i^2}{2f_s^2} + \right. \quad (7)$$
$$\left. + \frac{X_{FS}^2}{12\pi(2^B-1)^2}\int_0^{\pi}\left|(1-e^{-j\omega})N_{TF}(e^{-j\omega})\right|^2 d\omega\right)$$

where $f_s \equiv 1/T_s$ is the sampling frequency.

In some modulator topologies, the integration in (7) may become mathematically too complex, thus requiring the use of numerical solving methods. This can be simplified if the state-space formulation is used to derive $E[(\Delta q_n)^2]$ as shown in next section.

III. STATE-SPACE FORMULATION

Fig.3 shows the state-space representation of $N_{TF}(z)$, which can be described by the following finite difference equations [13]:

$$\overline{v(n+1)_0} = \bar{F}_0 \cdot \overline{v(n)_0} + \bar{p}_0 \cdot e(n)$$
$$q(n) = \bar{g}_0^T \cdot \overline{v(n)_0} + e(n) \quad (8)$$

where $\bar{F}_0$ is the state matrix, $\overline{v(n)_0}$ is the $L \times 1$ state vector, $\bar{p}_0$ and $\bar{g}_0$ are $L \times 1$ vectors and L is the order of N_{TF}.

Equation system (8) can be solved recursively to find the relation between the initial state ($\overline{v(n_0)_0}$), previous input ($e(k)$), present input ($e(n)$) and output ($q(n)$) of the system [13]. This gives:

$$q(n) = \bar{g}_0^T \cdot \bar{F}_0^{n-n_0} \cdot \overline{v(n_0)_0} +$$
$$+ \sum_{k=0}^{n-1} \bar{g}_0^T \cdot \bar{F}_0^{n-1-k} \cdot \bar{p}_0 \cdot e(k) + e(n) \quad (9)$$

Considering that $E\{e(k)e(j)\} = 0$ for $k \neq j$, and assuming $\overline{v(n_0)_0} = 0$, it can be shown from (9) that:

$$E\{q^2(n)\} = E\{e^2(n)\}(1 +$$
$$+ \sum_{k=0}^{n-1} [\bar{g}_0^T \cdot \bar{F}_0^{n-1-k} \cdot \bar{p}_0]^2) \quad (10)$$

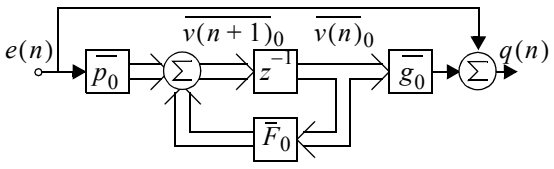

Fig. 3: State-space representation of $N_{TF}(z)$.

Diagonalizing $\bar{F}_0$ and considering that the system in Fig.3 is stable, the expression in (10) can be re-written as:

$$E\{q(n)^2\} = E\{e(n)^2\}(1 -$$
$$- \sum_{k=1}^{L}\sum_{j=1}^{L} g_k p_k g_j p_j \frac{\lambda_k^{-1}\lambda_j^{-1}}{1-\lambda_k^{-1}\lambda_j^{-1}}) \quad (11)$$

where λ_i are the eigenvalues of $\bar{F}_0$ and g_i and p_i are respectively the elements of $\bar{g}^T = \bar{g}_0^T \cdot \bar{T}$ and $\bar{p} = \overline{T^{-1}} \cdot \bar{p}_0$, with $\bar{T}$ being the matrix of the eigenvectors of $\bar{F}_0$.

Using a similar procedure, it can be shown that: $E\{q(n)q(n-1)\} =$

$$= E\{e(n)^2\}\left(\bar{g}^T \cdot \bar{p} - \sum_{k=1}^{L}\sum_{j=1}^{L} g_k p_k g_j p_j \frac{\lambda_k^{-1}}{1-\lambda_k^{-1}\lambda_j^{-1}}\right) \quad (12)$$

Taking into account that $E\{e(n)^2\} =$ $= X_{FS}^2/[12 \cdot (2^B-1)^2]$, and that $E\{(q(n))^2\} =$ $= E\{(q(n-1))^2\}$, the value of $E[(\Delta q_n)^2]$ can be derived from (11) and (12) as:

$$E\left\{(\Delta q_n)^2\right\} = 2[E\{(q(n))^2\} - (E\{q(n)q(n-1)\})]$$
$$= \frac{X_{FS}^2}{6(2^B-1)^2} \cdot \psi(\bar{g}, \bar{p}, \bar{\lambda}, L) \quad (13)$$

where

$$\psi(\bar{g}, \bar{p}, \bar{\lambda}, L) = 1 - \bar{g}^T \cdot \bar{p} +$$
$$+ \sum_{k=1}^{L}\sum_{j=1}^{L} g_k p_k g_j p_j \frac{\lambda_k^{-1} - \lambda_k^{-1}\lambda_j^{-1}}{1-\lambda_k^{-1}\lambda_j^{-1}} \quad (14)$$

Replacing (6) with (13) in (7) and assuming that the jitter noise is an additive noise source at the input of the modulator, the Signal-to-Noise Ratio (*SNR*) dominated by jitter can be written as:

$$SNR_j = \frac{A^2/2}{B_w \cdot (\sigma_{\Delta T})^2 \cdot \left[\frac{A^2\omega_i^2}{f_s} + \frac{X_{FS}^2 \cdot f_s}{3(2^B-1)^2}\psi(\bar{g}, \bar{p}, \bar{\lambda}, L)\right]} \quad (15)$$

where B_w is the signal bandwidth.

Assuming that the jitter noise and the quantization noise are not correlated, their powers can be added and the total *SNR*, considering both noise sources is:

$$SNR = \frac{A^2/2}{P_{\varepsilon b} + P_{Qb}} \tag{16}$$

where $P_{\varepsilon b}$ and P_{Qb} are the jitter and quantization in-band noise powers, respectively given by:

$$P_{\varepsilon b} = 2B_w(\sigma_{\Delta T})^2\left[\frac{A^2\omega_{in}^2}{2f_s} + \frac{X_{FS}^2 f_s}{6(2^B-1)^2}\cdot\psi(\bar{g},\bar{p},\bar{\lambda},L)\right]$$

$$P_{Qb} = \frac{X_{FS}^2}{6f_s(2^B-1)^2}\int_0^{B_w}|N_{TF}(f)|^2 df \tag{17}$$

Note that $(\sigma_{\Delta T})^2$ in $P_{\varepsilon b}$ is multiplied by a factor that is the sum of two terms: one depending on the input signal parameters (A and ω_i) and the other one which is a function of the modulator topology parameters (B, X_{FS}, $\psi(g, p, \lambda, L)$). The first term decreases with f_s while the second term increases with f_s. This is illustrated in Fig.4 where the two terms in brackets in (17) are plotted versus f_s for a 5-bit 3rd-order single-loop CT ΣΔM with $f_i = B_w = 20\text{MHz}$. Note that there is an optimum value of f_s, $f_{s\text{op}} = 170\text{MHz}$, that minimizes the in-band jitter noise power and hence, maximizes SNR ††††. Thus, using (17) as a figure of merit in multi-bit CT ΣΔMs with NRZ DAC in which jitter is the main limiting factor, the modulator performance can be optimized for given specifications in terms of loop filter parameters, sampling frequency and the number of bits of the internal quantizer.

IV. COMPARISON WITH PREVIOUS APPROACHES

The analysis in this paper presents a new way of quantifying the amplification effect of the loop filter through the calculation of $E[(\Delta q_n)^2]$ instead of using integration as in previous approaches. Using (15) as a figure of merit, the resolution of those modulators limited by clock jitter can be improved by modifying the noise shaping characteristics in order to reduce the in-band jitter noise power. Another important part of the analysis described in this paper is the inclusion of the influence that the input signal has on the jitter sensitivity of the modulator. This has not been considered in any previous analysis of CT ΣΔMs, even though it may become the dominant factor as it will be shown in Section V. Implications of the latter aspect are further explored next.

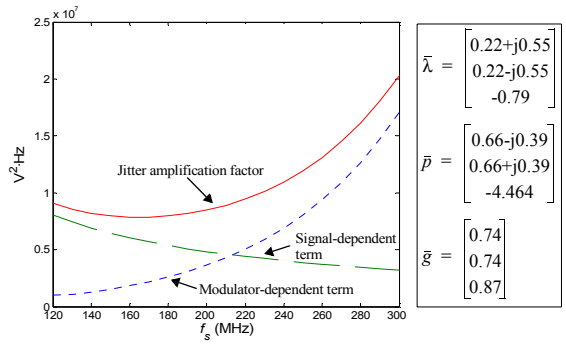

Fig. 4: Jitter components vs. f_s for a 5-bit 3rd order CT ΣΔM

††††. The values of g_i, p_i and λ_i for $f_s = f_{s\text{op}} = 170\text{MHz}$ are shown in Fig.4.

Assuming that SNR_j is dominated by the signal-dependent term, and that $f_i = B_w$, the maximum achievable resolution in a CT ΣΔM with clock jitter can be derived from (15), giving:

$$SNR_{\text{MAX}} = 10\log\left(\frac{M}{4\pi^2\sigma_{\Delta T}^2 B_w^2}\right) \tag{18}$$

where $M \equiv f_s/(2B_w)$ is the oversampling ratio.

Note that (18) is the same relation as that one obtained in DT ΣΔMs [14]. What is expressed in this relation is a simple idea: any converter (not only those based in ΣΔ modulation) clocked with an imperfect signal cannot be better than an ideal sampler clocked with the same signal. In DT ΣΔMs, this fact manifests itself through the input sampler, whereas in CT ΣΔMs it is introduced by the feedback DAC.

The fundamental limit shown in (18) is valid for either single loop or cascade modulators, since jitter-induced noise introduced in the first stage is not affected by latter stages which only process quantization error. This is also valid for any type of loop filter, since (18) is independent of the particular loop filter. Note that in those cases where the dominant factor in (15) is the modulator dependent term, the maximum achievable SNR is lower than the value given by (18). That is generally the case in those modulators that use single bit quantization, where, due to the much larger quantization step Δ, $E[(\Delta q_n)^2]$ is the dominant factor. To illustrate this point, let us consider the single-bit 2nd-order CT ΣΔM shown in Fig.5, with an input signal with frequency, $f_i = B_w$, and an amplitude of 80% of the reference level, with $f_s = 40\text{MHz}$ and $M = 64$. In this case, the modulator dependent term is more than one thousand times higher than the signal-dependent term. In other words, jitter sensitivity in this modulator is completely dominated by $E[(\Delta q_n)^2]$, making jitter-induced noise power practically independent of the input signal. Under these conditions, the general equations derived in this paper provide similar predictions to those given by other expressions reported in literature, obtained for single

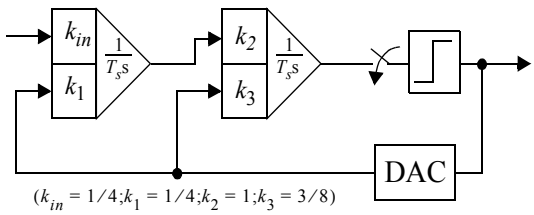

Fig. 5: Block diagram of a single-bit 2nd-order CT ΣΔM.

bit quantization [3]:

$$SNR_{\text{jitter}} = 10\log\left(\frac{1}{16M\sigma_{\Delta T}^2 B_w^2}\right) \qquad (19)$$

As an illustration, Fig.6 compares (15), (16) and (19) with simulation results of the modulator in Fig.5. Predictions of equations (15) and (19) are indeed very similar and, in the area where jitter dominates the resolution, close to the simulated values. The fundamental limit imposed by (18) is also shown in Fig.6, and it is clear that, in this case, it is not a limiting factor.

However, considering the more general case of multi-bit CT ΣΔMs which are not dominated by either the modulator-dependent term or the signal-dependent term, expressions derived in this paper should be used instead of (18) and (19). In case that the modulator-dependent term dominates the signal-dependent term, predictions given by (15) and (16) will approach those given in [7]. However the work in [7] does not take into account the impact of signal-dependent jitter term, which can be very critical in broadband applications as demonstrated in the next section.

V. SIMULATION RESULTS: APPLICATION TO VDSL

The presented study has been validated through time-domain behavioural simulation using SIMSIDES, a SIMULINK-based simulator for ΣΔMs [15]. Fig.7 shows the multi-bit NRZ CT ΣΔMs under study. Fig.7(a) is a 3rd-order single-loop and Fig.7(b) is a cascaded 2-1 topology. In both architectures, feed-forward stabilization is used and a feedback coefficient k_r is used to move one of the poles to an optimum position [16]. The modulators were synthesized to handle signals within $B_w = 20\text{MHz}$ for VDSL application. Three different cases are considered:

- CT ΣΔM1: Fig.7(a), $f_s = 400\text{MHz}$ and $B = 2$
- CT ΣΔM2: Fig.7(a), $f_s = 160\text{MHz}$ and $B = 5$
- CTΣΔM3: Fig.7(b), $f_s = 160\text{MHz}$ and $B_1 = B_2 = 5$

where B_1 and B_2 are respectively the number of bits of the internal quantizer in the first- and second- stage

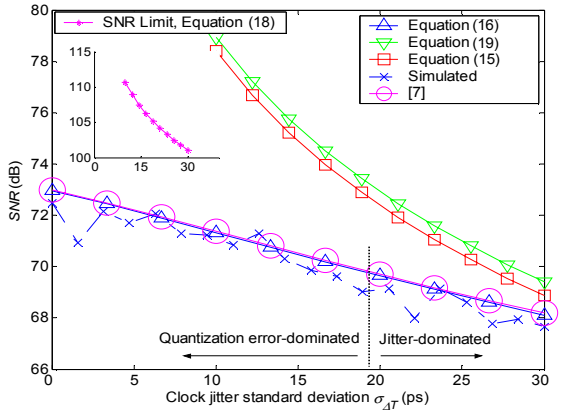

Fig. 6: Comparison of theory and simulations for the modulator of Fig.5.

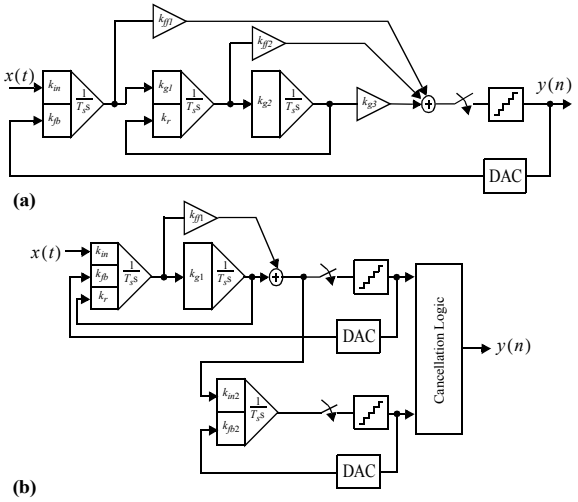

Fig. 7: Multi-bit NRZ CT ΣΔMs under study. (a) 3rd-order single-loop architecture. (b) Cascaded 2-1 architecture.

in Fig.7(b). Table 1 shows the values of the loop-filter coefficients (k_i) as well as the position of the poles and Table 2 shows the values of g_i, p_i and λ_i for the three cases mentioned above.

Fig.8 shows several simulated output spectra of cases CT ΣΔM1 (Fig.8(a)) and CT ΣΔM2 (Fig.8(b)) corresponding to different values of f_i and $\sigma_{\Delta T} = 25$ ps. Note that in Fig.8(a), the in-band noise power does not depend on f_i as predicted by [7]. However, as B increases from $B = 2$ to $B = 5$, the modulator-dependent term in (15) decreases and hence, the in-band noise is dominated by the signal-dependent term as illustrated in Fig.8(b). This effect is better shown in Fig.9, where the SNR-peak of the modula-

TABLE 1. Loop-filter coefficients of CT ΣΔMs in Fig.7

	CT ΣΔM1	CT ΣΔM2	CT ΣΔM3
k_{in}	1.5	2	1.6
k_{fb}	-1.5	-2	-1.6
k_{g1}	1	1	1.6
k_r	-0.1	-0.37	-0.24
k_{g2}	0.6	1	–
k_{g3}	0.5	1.2	–
k_{ff1}	1	1	1
k_{ff2}	0.5	1	–
k_{in2}	–	–	1
k_{fb2}	–	–	-1
Poles	$\omega_1 = 0$	$\omega_2 = \sqrt{3/5}\cdot 2\pi\cdot B_w$	

TABLE 2. Values of g_i, p_i and λ_i for the CT ΣΔMs in Fig.7

	CT ΣΔM1	CT ΣΔM2	CT ΣΔM3
$\bar{\lambda}$	[-0.328 0.664-j0.438 0.664-j0.438]	[0.122+j0.39 0.122-j0.39 -0.667]	[-0.543+j0.64 -0.543-j0.64]
$\bar{g}$	[-0.56 0.853 0.853]	[0.81 0.81 0.959]	[0.766 0.766]
$\bar{p}$	[3.503 0.016-j0.184 0.016+j0.184]	[1.476+j1.722E-3 1.476-j1.722E-3 -5.69]	[-1.78-j1.81 -1.78+j1.81]

tors in Fig.7 is plotted vs. $\sigma_{\Delta T}$ for several values of f_i, showing simulation results and theoretical predictions. For comparison purposes, predictions given by [7] are also included. Note that, simulated and theoretical data matched very well when the combined effect of signal- and modulator-dependent jitter noise is taken into account as shown in this work.

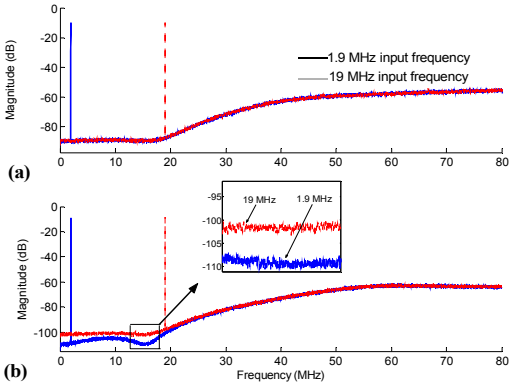

Fig. 8: Effect of jitter error on the output spectra of (a) CT ΣΔM1 and (b) CT ΣΔM2.

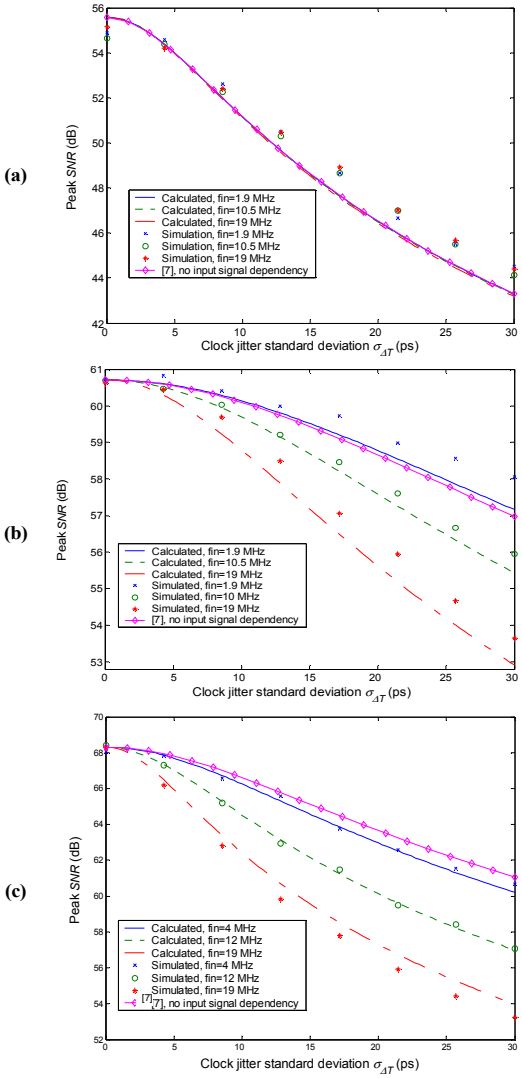

Fig. 9: SNR vs. $\sigma_{\Delta T}$ for different values of f_i : (a) CT ΣΔM1. (b) CT ΣΔM2. (c) CT ΣΔM3.

CONCLUSIONS

The effect of clock jitter on multi-bit CT ΣΔMs with NRZ DAC has been analyzed. Based on the use of state-space formulation, easy-to-compute closed-form expressions have been derived for the noise power and signal-to-noise ratio. It has been demonstrated that the jitter-induced noise has two components: one depending on signal parameters and the other one depending on the modulator loop filter. Their combined effect, not predicted by previous approaches, has been confirmed by time-domain simulations of several CT ΣΔMs intended for VDSL application.

REFERENCES

[1] J.A. Cherry and W.M. Snelgrove: *Continuous-Time Delta-Sigma Modulators for High-Speed A/D Conversion*. Kluwer, 2000.

[2] L. Breems and J.H. Huijsing: *Continuous-Time Sigma-Delta Modulation for A/D Conversion in Radio Receivers*. Kluwer, 2001.

[3] E. J. van der Zwan: "A 0.2-mW CMOS ΣΔ Modulator for Speech Coding with 80 dB Dynamic Range", *IEEE Journal of Solid-State Circuits*, Vol. 31, pp. 1873-1880, December 1996.

[4] O. Oliaei, H. Aboushady: "Jitter Effects in Continuous-Time ΣΔ Modulators with Delayed Return-to-Zero Feedback", *Proc. of the 1998 IEEE International Conference on Electronics, Circuits and Systems*, Vol.1, pp. 351-354.

[5] H. Tao, L. Toth, J. M. Khoury: "Analysis of Timing Jitter in Bandpass Sigma-Delta Modulators", *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, Vol 46, pp. 991-1001, August 1999.

[6] O. Oliaei, H. Aboushady: "State-Space Analysis of Clock Jitter in Continuous-Time Oversampling Data Converters", *IEEE Transactions on Circuits and Systems-II: Analog Digital Signal Processing*, Vol. 50, pp. 31-37, January 2003.

[7] L. Hernández, A. Wiesbauer, S. Patón and A. Di Giandomenico: "Modelling and Optimization of Low-Pass Continuous-Time Sigma-Delta Modulators for Clock Jitter Noise Reduction", *Proc. of the 2004 International Symposium on Circuits and Systems*, Vol. 1, pp. 1072-1075.

[8] M. Moyal, M. Groepl, H. Werker, G. Mitteregger, J. Schambacher: "A 700/900mW/Channel CMOS Dual Analog Front-End IC for VDSL with Integrated 11.5/14.5dBm Line Drivers". *Proc. of the 2003 IEEE Int. Solid-State Circuits Conf.*, pp. 416-417.

[9] S. Yan, E. Sánchez-Sinencio: "A Continuous-Time ΣΔ Modulator With 88-dB Dynamic Range and 1.1-MHz Signal Bandwidth", *IEEE Journal of Solid-State Circuits*, Vol. 39, pp. 75-86, January 2004.

[10] S. Patón, A. Di Giandoménico, L. Hernández, A. Wiesbauer, T. Pötscher and M. Clara: "A 70-mW 300-MHz CMOS Continuous-Time ΣΔ ADC With 15-MHz Bandwidth and 11 Bits of Resolution", *IEEE Journal of Solid-State Circuits*, Vol. 39, pp. 1056-1063, July 2004.

[11] R. Scherier and B. Zhang: "ΔΣ Modulators Employing Continuous-Time Circuitry", *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, Vol 43, pp. 324-332, April 1996.

[12] L. Risbo: *ΣΔ Modulators - Stability and Design Optimization.* PhD dissertation, Technical University of Denmark, 1994.

[13] J. G. Proakis, D. G. Manolakis: *Digital Signal Processing. Principles, Algorithms and Appications.* Prentice Hall, 1998.

[14] B. E. Boser and B. A. Wooley, "The Design of Sigma-Delta Modulation Analog-to-Digital Converters". *IEEE Journal of Solid-State Circuits*, Vol. 23, pp. 1298-1308, December 1988.

[15] J. Ruiz-Amaya, J.M. de la Rosa, F. Medeiro, F.V. Fernández, R. del Río, B. Pérez-Verdú and A. Rodríguez-Vázquez: "An Optimization-based Tool for the High-Level Synthesis of Discrete-time and Continuous-Time ΣΔ Modulators in the MATLAB/SIMULINK Environment". *Proc. IEEE Int. Symp. Circuits and Systems*, Vol V., pp. 97-100, 2004.

[16] R. Schreier, "An Empirical Study of High-Order Single-Bit Delta-Sigma Modulators". *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, Vol 40, August 1993.