OWLS: A MIXED-SIGNAL ASIC FOR OPTICAL WIRE-LESS LINKS IN SPACE INSTRUMENTS

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INTRODUCTION

This paper describes the design of a mixed-signal ASIC for space application and the techniques employed for radiation hardening and temperature effects compensation. The work is part of a planned long-term effort and collaboration between "Instituto de Microelectrónica de Sevilla (IMSE)", "Universidad de Sevilla (US)", and "Instituto Nacional de Técnica Aeroespacial (INTA)" aimed to consolidate a group of experienced mixed-signal space-ASIC designers. The initiative is partially funded by the Spanish National Research Program.

The ASIC performs the function of an optical digital transceiver for diffuse-light intra-satellite optical communications. It has been designed in a 0.35μm CMOS technology from austriamicrosystems (ams).

The chip has been manufactured and verified from a functional perspective. Radiation characterization is planned for the third quarter of 2012. Power- and temperature-stress tests, as well as life-tests are also planned for this next quarter, and will be carried out by Alter Technology TÜV Nord S.A.U.

Given the previous characterization of the technology [1] and the hardening techniques employed in the design and layout, radiation is not expected to be a problem. The specified environmental limits are a pedestal hard limit of 50KRads with the goal of maximizing TID tolerance, SEU and SET LET-thresholds above 70MeV/(mg/cm^2), and latch-up free behavior up to the same LET limit. Concerning temperature, the specified operation range is from -90 to +125ºC, while the non-operating temperature range is from -135 to +150ºC.

SYSTEM DESCRIPTION

The ASIC has been conceived to replace -with the associated advantages in volume and weight, and some significant increases in performance and versatility- the discrete electronics in use in several systems developed at INTA for diffuse-light intra-satellite asynchronous optical communication [2]. In particular, the ASIC, code-named OWLS, performs the function of an optical digital transceiver, using baseband transmissions and subcarrier modulation.

The system contains three main modules: receiver, driver (emitter), and digital interface. Each module has an independent power supply pin and can be independently biased within a wide range of supply voltages: [2.7, 5.5V]. This responds to several objectives. Specifications included the possibility of using very different single-supply voltage

levels, as well as the capacity of the system to reject low and medium frequency ripples of up to 100mV in the supply voltages. In addition, the voltage swing of the external digital signals was required to be independent, established by a dedicated power-pin, in order to support any logic family in that range. For the transmit and receive sections, the chip includes independent internal voltage regulators and a band-gap circuit as a reference. This provides a core-supply voltage of 2.4V, independent of the external supply level. Regulator and band-gap circuits employ thick oxide transistors (withstanding 5.5V), while the core circuitry employs thin-oxide devices for better TID tolerance. An additional regulator is used to bias the analog filters, as will be described latter. Each regulated voltage is externally accessible, with a 10μF (or higher) capacitor being required for stability and supply filtering.

Temperature- and process-independent bias currents are generated with a feedback loop involving an external low temperature coefficient (LTC) resistor and a band-gap referred voltage.

Fig.1 shows a simplified block diagram of the complete system. The receiver section includes a transimpedance amplifier (TIA), two filter banks, and a decision stage. The first filter bank is also used in some transmission modes. It can be configured in seven different bands, as described in Table 1, allowing band-base and digital amplitude shift-keying modulated communications.
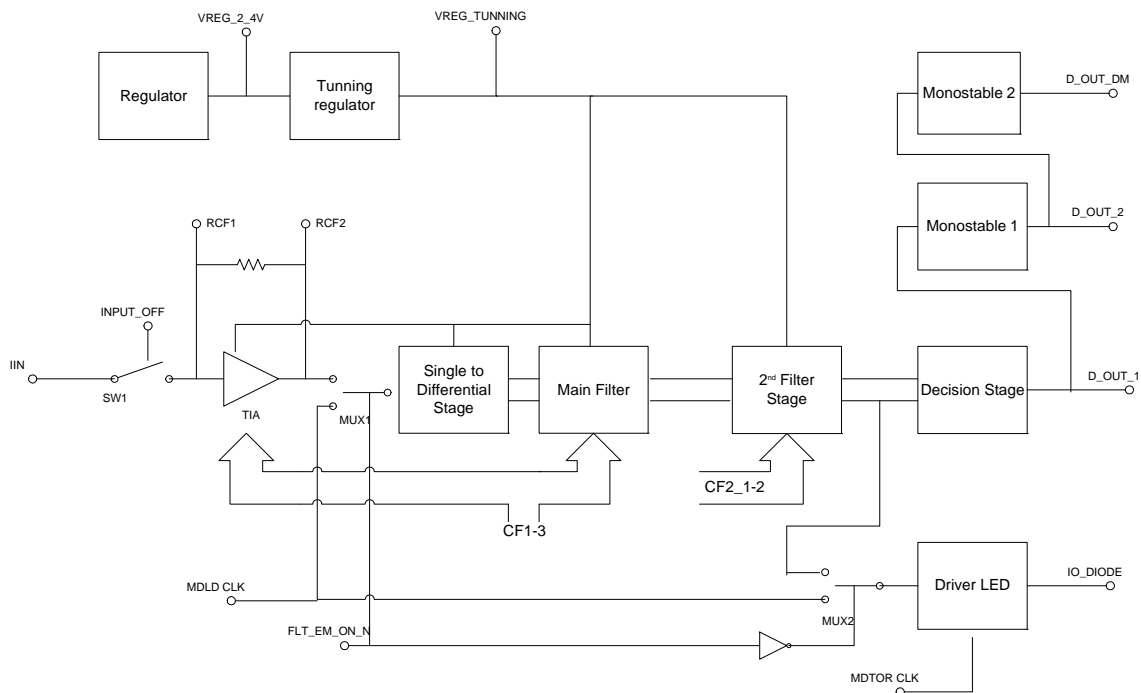

Fig. 1. OWLS block diagram.

Table 1. Configuration pins and corresponding band selection
of main filter stage. (*) For test purpose.

CFG3	CFG2	CFG1	Type	Band
0	0	0	Low-pass	DC-1MHz
0	0	1	Low-pass	DC-8MHz
0	1	0	Low-pass	DC-20MHz
0	1	1	-	Short (*)
1	0	0	Band-pass	Fc=500kHz, BW=210kHz
1	0	1	Band-pass	Fc=1.65MHz, BW=500kHz
1	1	0	Band-pass	Fc=5.4Mhz, BW=1.5MHz
1	1	1	Band-pass	Fc=18.2MHz,BW=3.3MHz

An external signal is used to set the chip in either reception or transmission mode. While in transmission, the input of the TIA is internally disconnected to avoid receiver saturation due to its own emission. Also while in transmission, the first filter bank can be used to generate a sinusoidal carrier from its digital version. A simple mixer and light emitting diode (LED) driver able to deliver 200mA at 20MHz complete the transmitter section. Emission power can be configured by means of an external resistor.

An external photodiode (or several of them in parallel, aimed to different directions for a wider solid-angle of reception) with a pull-up biasing resistor, must be connected at the TIA input pin using a capacitive coupling network in order to reject DC components, including some degree of background illumination. The maximum diode capacitance at the TIA input pin is of 500pF.

The photo-generated AC current is transformed into voltage by the TIA, with a maximum bandwidth of 20MHz. A configurable capacitive and resistive TIA feedback network is controlled by the same signals used to configure the first filter bank. The amplifier transconductance is also configured accordingly. The TIA output voltage signal is then filtered by the filters in the first bank. The several configurable bands and operation modes allow several of these systems to operate simultaneously within the satellite, without interferences.

The filters use gm-C techniques, and have been implemented using Bourdel Transconductors [3], a slight modification of Nauta Transconductor [4]. These transconductors are fully-differential, achieving high input voltage-ranges under low supply voltage conditions. A corresponding single-to differential conversion stage is therefore required at the main filter-bank input.

A second filter bank, also reconfigurable, is low-pass and is intended to reduce noise before the comparison done by the decision stage. Table 2 lists the allowed bands of the second filter-bank.

The accuracy of the corner and central frequencies, as well as their stability against temperature variations, is ensured by a gm-tuning feedback loop. Bourdel and Nauta transconductors are tuned using their supply voltage. A specific regulator is therefore used to generate their power supply level. The reference level of the regulator is obtained from the feedback loop, which comprises the current generated by an additional external LTC resistor driven by a fixed voltage difference, and the current generated by a reference transconductor with a fixed differential input voltage. The loop ensures that the gm of the reference transconductor is proportional to the inverse of the external resistor. Transconductance invariance with temperature and process is therefore guarantied. The effects of process variations of the capacitors in the associated time-constants are compensated by a proper trimming of the external LTC resistor value (and therefore, of the transconductance). Capacitance (double poly) variations with temperature are acceptable for the system specifications. Transconductors power supply levels change around its nominal 2.2V levels by about 100mV within the prescribed temperature range and process corners.

The two signals (the differential signal) at the output of the second filter-bank can be observed at specific pins for characterization purpose. The associated output buffers are powered-down during normal operation.

Fig.2 provides a simplified schematic of the decision stage. Several strategies are possible in setting the threshold of the comparison, including an externally-set invariant threshold level, a self-extracted signal average, or a combination (addition) of both. The same circuit used to set the invariant external component of the threshold level serves for offset compensation when required. The average signal level is obtained using a rough first-order low-pass filter, defined by a relatively large external capacitor (~10nF) and the transconductance of the last internal transconductor.

Table 2. Configuration pins and bandwidths
of second filter-bank.

CFG2_2	CFG2_1	Band
0	0	2MHz
0	1	10MHz
1	0	20MHz
1	1	Disabled

Fig. 2. Decision stage schematic.

Because of the bursting nature of the communication (by pulse packages) and the AC coupling at the TIA input pin, the pulses recovered at the comparator output have variable duration at the beginning of each bit stream package. A couple of configurable mono-stable sections are finally used to equalize recovered pulses duration in case of return-to-zero (RZ) modulation, and to demodulate the bit stream in amplitude-shift-keying (ASK) transmissions. Pulses-duration at the output of each mono-stable can be configured using external resistors. The two output signals of the mono-stables can be inverted by enabling a specific control signal, in order to obtain negative logic when required.

In emission mode, the current through the LED can be controlled by a base-band or by an amplitude shift-keying modulated signal. For the former option, the base-band signal is introduced trough a specific digital input pin. For the latter case, a pulsed carrier must be introduced at this pin, while the base-band signal to be modulated is introduced at a different digital input pin. In any case, either the base-band signal (in base-band transmission) or the pulsed carrier can optionally be filtered by the first filter-bank, reducing the emission of out-of-band harmonics.

Fig.3 shows a simplified schematic of the driver stage in the transmission section. The LED is driven by the current mirror, whose output current is modulated by transistor Mdrive acting either as a switch or as a source follower driving the current mirror output transistor into the triode region.

In ASK modulation mode, Mdrive gate is switched between the (optionally filtered) carrier signal and GND using a multiplexor controlled by the ASK base-band signal, thus ensuring very low output current during the emission of logic 0s. The ASK base-band input is set to logic 1 in base-band transmission modes.

The maximum output current is controlled by an external resistor. In order to reduce ground bounces, a dedicated pin has been used to drain the high current of the diode. Three parallel bonding wires have been used at this GND node and at the output of the LED driver.
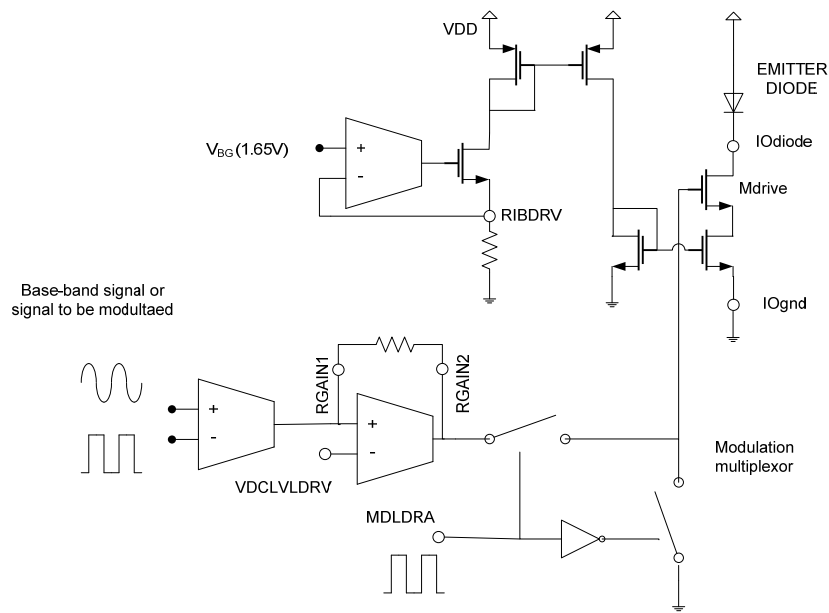
Fig. 3. Driver schematic.

SPACE-SPECIFIC MEASURES

Space-specific measures concern radiation, temperature, and packaging. Radiation effects on the 0.35μm CMOS process from austriamicrosystems (ams) being used have been characterized in its most relevant aspects in previous efforts [1]. The main conclusions of that undergoing characterization are that all MOS devices (thick and thin oxide, nmos and pmos) exhibit a correct behavior with minor threshold voltage shifts and slight increase in leakage currents, up to 300KRads of TID. The requirement for this design was a minimum tolerance of 50Krad, with a strong emphasis in maximizing the TID limit. Since area specifications were not severe, we decided to use ringed-source nmos transistors in every case, with standard layout for the pmos devices. Concerning single-event effects, these are basically restricted to latch-up, since the system does not include a significant digital section in this version. Single event transients are possible, but are considered acceptable for the function of the system: sporadic communication errors can be detected and recovered with low effects on the performance of the hosting system. Concerning latch-up, and again under the

loose area restrictions, we have used complete ward-rings around every nmos and pmos device. The previous characterization of the technology forecast a latch-up free behavior up to at least $68\text{MeV}/(\text{mg/cm}^2)$. The actual limit is probably much higher since the bound corresponds to the maximum LET in the ion cocktail available for characterization at the time, for which no latch-up was observed. On this premises, the expected latch-up behavior is clearly acceptable for our design specification of $70\text{MeV}/(\text{mg/cm}^2)$. Radiation validation is planned for this coming third quarter of 2012.

Concerning design and design verification issues, layout styles like ringed-source and others aimed to reduce leakage currents along the edge of the bird's beak oxide represent an additional difficulty in the conventional design flow, specially at the simulation, layout-extraction, and layout-versus-schematic (LVS) verification. Some amendments have been introduced in the standard design kit, including additional symbols for radiation-hardened (RH) nmos transistors that translate into an equivalent-with standard nmos for electrical simulation, and the necessary modification in the extraction and LVS scripts, as well as some additional layout norms and layers, for the proper verification of the layout, and an additional p-cell for the automatic generation of the layout of the ringed-source nmos.

Temperature effects do not differ qualitatively from the typical design tasks in terrestrial applications, except in the extended temperature range. The main difficulty is that the device models provided by the foundry, including temperature effects, are not guaranteed beyond the typical automotive or military ranges. However, again from the results of the previous characterization of the technology [1], it has been confirmed that the direct use of the foundry models up to our temperature limits provided reasonable results, with good agreement to experimental measurements of the critical device parameters. Therefore, our space-specific measures concerning the extended temperature range has been to verify, using electrical simulation with the foundry-provided models, that the system behavior is correct.

PACKAGING

Packaging is another critical topic in space applications. The adhesive used to attach the die to the package is critical in many aspects, specially under the extreme specifications in temperature range (operation and non-operation), thermal cycles, vibration, and impacts (acceleration) associated with most space missions. Cavity sealing must be and remain hermetic, and the atmosphere within the cavity must fulfill specific requirements of cleanliness and humidity. Dry-nitrogen atmosphere is a common approach.

Fig.3 shows a photograph of the 3.5mm x 3.5mm die. It has been packaged in a KYOCERA JLCC44 (PB_F86079) ceramic package. Fig.4 and Fig.5 show the corresponding bonding diagram and external pins connections respectively.

We have performed thermal cycles as prescribed by the specifications, and then the corresponding die shear tests, without observing any problems. Given the low mass of the die, impact (acceleration) issues are not expected to be a problem. Nevertheless, specific tests at INTA facilities have been programmed for the near future. Other tests, like those related to confirming the hermetic properties of the package after sufficient stress conditions, have been programmed and will be carried out by subcontractors.
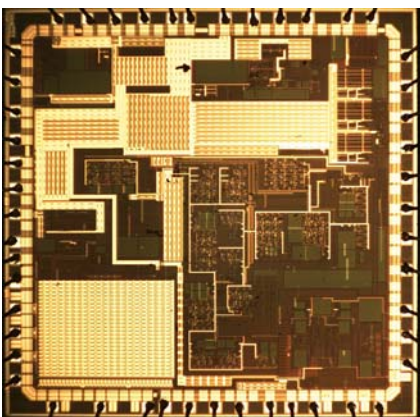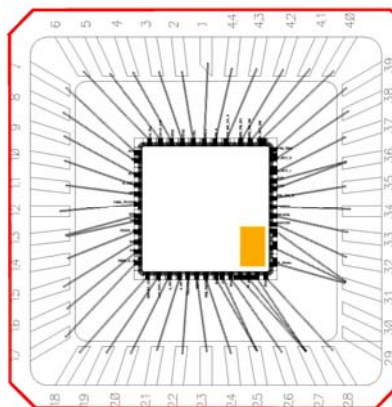

Fig. 3. Die photograph.
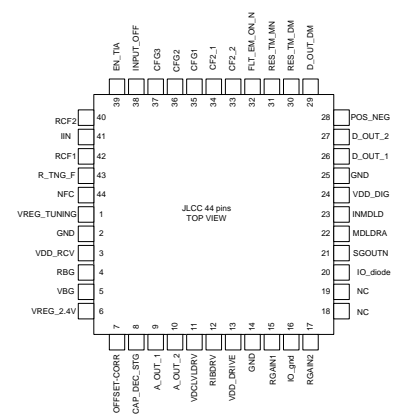

Fig. 4. Bonding diagram.

Fig. 5. Pin Connections.

EXPERIMENTAL RESULTS

The chip has been functionally verified. Its behavior is correct in general, but its stability against temperature is not as good as expected. The source of the deviation has been tracked to be related to a low performance of the band-gap. The ultimate cause, related to the modifications done in the bipolar devices in an attempt to achieve better radiation tolerance, has been diagnosed and will be corrected in a future version of the device. This future version is planned to incorporate the required digital section, reducing the number of pins, increasing the functionality, and simplifying the external interface so as to make the overall system more compact. Still, this first version is operative and can be used according to specifications.

The variety of tests and experimental results is too high to be reported exhaustively in this context. Some examples are given in the following figures.

Fig.6 and Fig.7 show the variation of the band-gap reference voltage with the power supply level and with temperature, respectively. Note that the band-gap reference circuit is biased by the unregulated power supply, and therefore subject to the effects of its changes. This was necessary as the regulated internal power supply uses a reference level derived from the band-gap itself. Note also the relatively large variation with temperature, as noted previously, to be corrected in a next iteration. The temperature range is that achievable in IMSE facilities. This variation is the underlying source of other dependencies with temperature described next. It is therefore expected that, once the reference level is made more stable versus temperature, several other characteristic will be improved as well.

Fig.8 through Fig.15 show the experimental Bode-magnitude plots at different temperatures and for different options of the first filter bank corresponding to low-pass and band-pass cases, together with the associated band-width or central frequency versus temperature for different samples. The observed pass-band gain variations with temperature is unexpected and was not observed in simulations. It is presently under analysis, and is most likely due to calibration variations in the spectrum analyzer during measurements. The variation in the corner and central frequencies, although much larger than expected, are still within specs. These larger variations are attributed to the relative large variations of the band-gap reference voltage, which makes the gm adaptive loop inefficient. They are expected to be solved in the next run.

Fig.16 shows the variation of the filters power supply versus temperature for different samples. As described earlier, this power supply is generated by its specific regulator, driven in turn by the gm adaptive loop, which is shown to be working properly (although fooled by the variation of the band-gap reference). Finally, Fig.17 shows the variation of the mono-stable output pulse-width with the associated control resistor.

SUMMARY AND FUTURE WORK

The design of a mixed signal ASIC for optical wire-less link intra-satellite communications has been described, together with space-specific measures used in the design and the obtained experimental results and undergoing qualification works. Although the ASIC fulfills the required specifications, some minor deviations have been observed, mainly related to the band-gap reference stability with temperature, which are expected to be solved in an upcoming iteration. The new version will incorporate a larger digital section, reducing the number of pins, increasing the functionality, and simplifying the external interface so as to make the overall system more compact.

ACKNOWLEDGEMENTS

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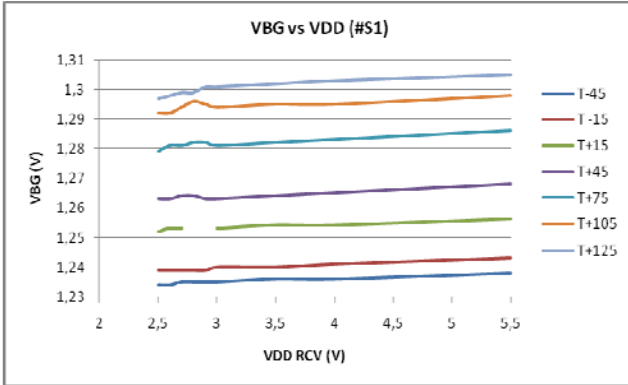
Fig. 6. Band-gap voltage versus VDD supply voltage for several temperatures. Sample 01.
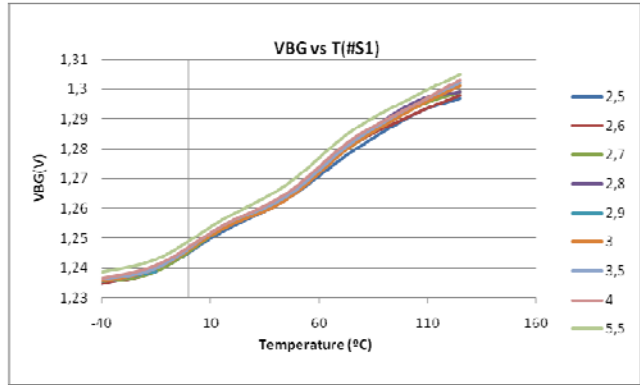
Fig. 7. Band-gap voltage versus temperature for several VDD supply voltages. Sample 01.
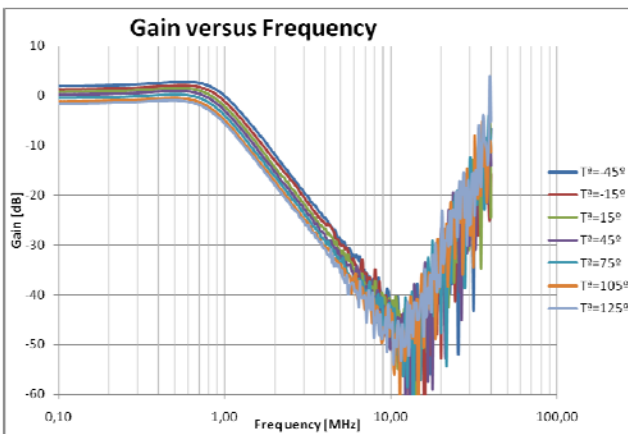
Fig. 8. Main filters. CFG=000. Gain versus Frequency at different temperatures. Sample 04. VDD=5V.
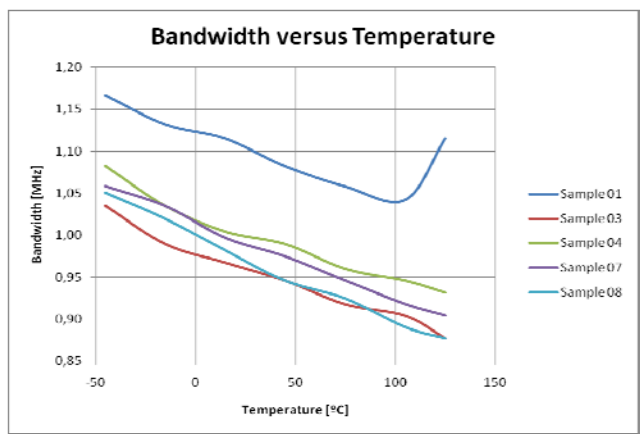
Fig. 9. Main filters. CFG=000. Bandwidth versus Temperature for different samples. VDD=5V.
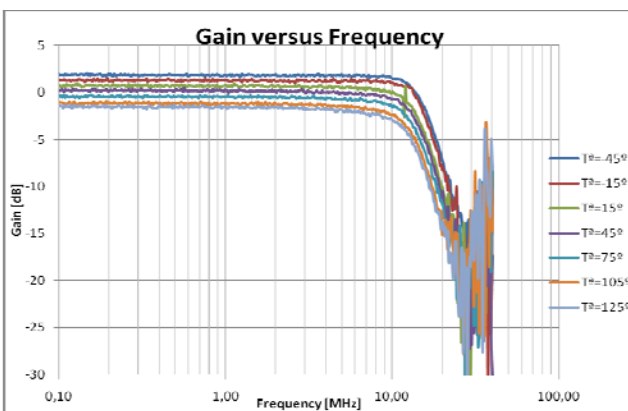
Fig. 10. Main filters. CFG=010. Gain versus Frequency at different temperatures. Sample 04. VDD=5V.
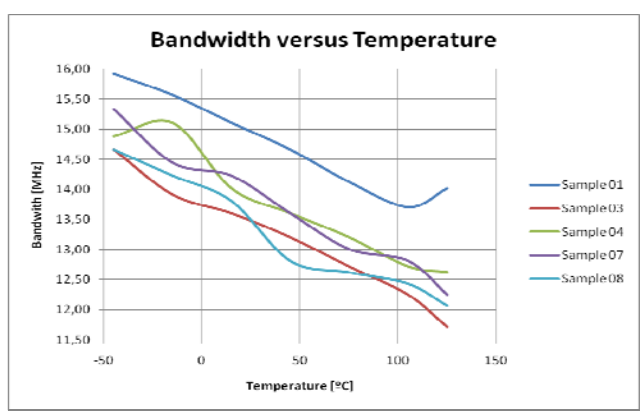
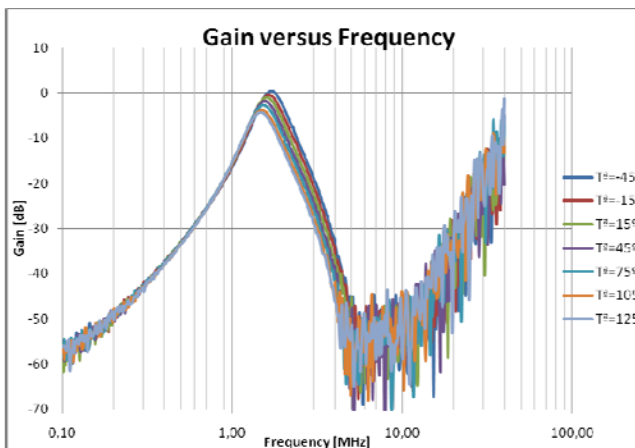Fig. 11. Main filters. CFG=010. Bandwidth versus Temperature for different samples. VDD=5V.

Fig. 12. Main filters. CFG=101. Gain versus Frequency at different temperatures. Sample 04. VDD=5V.
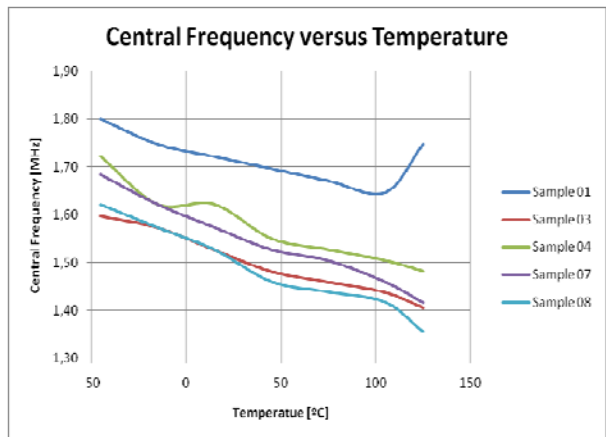

Fig. 13. Main filters. CFG=101. Central Frequency versus Temperature for different samples. VDD=5V.
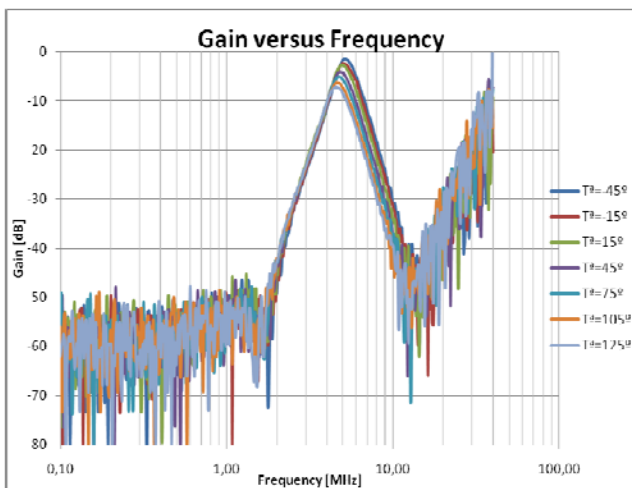

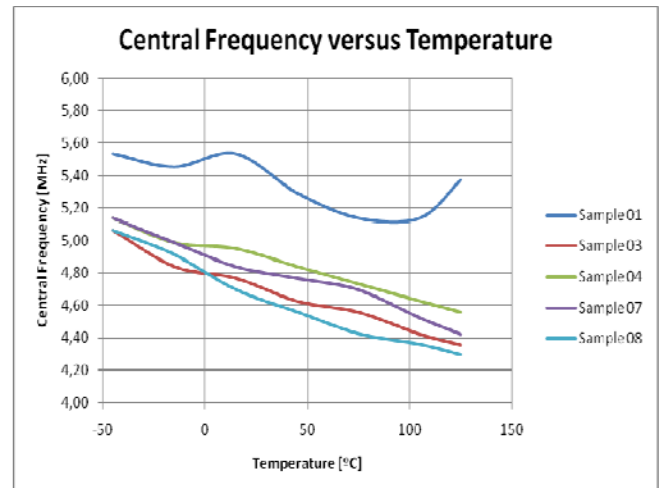Fig. 14. Main filters. CFG=110. Gain versus Frequency at different temperatures. Sample 04. VDD=5V.

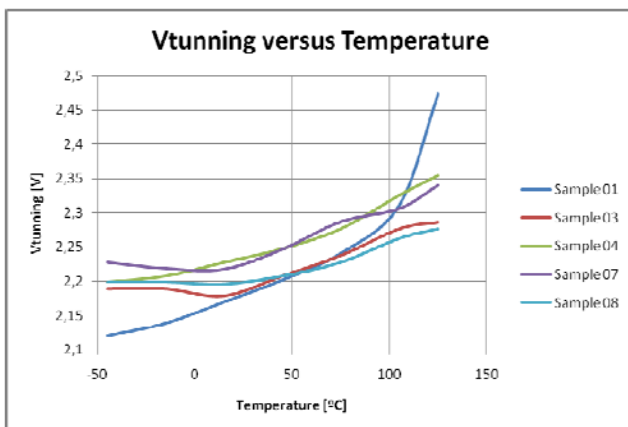Fig. 15. Main filters. CFG=110. Central Frequency versus Temperature for different samples. VDD=5V.

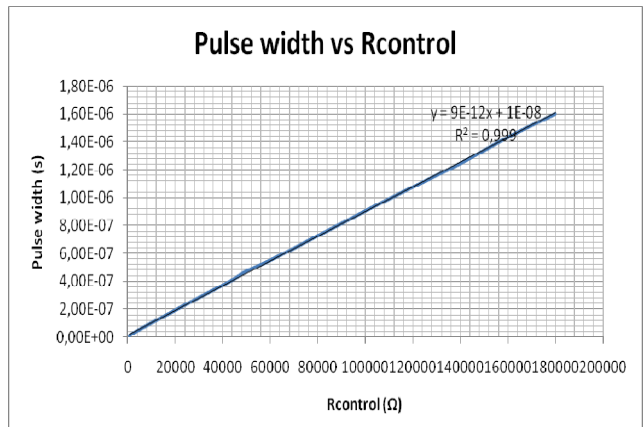Fig. 16. Tuning voltage versus Temperature for different samples.

Fig. 17. Pulse width versus control resistor. VDD=5V. T=25ºC