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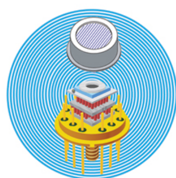

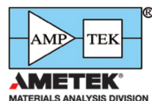

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JOURNAL OF APPLIED PHYSICS **122**, 155305 (2017)

Low temperature synthesis of highly oriented p-type $Si_{1-x}Ge_x$ (x: 0–1) on an insulator by Al-induced layer exchange

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A composition tunable $Si_{1-x}Ge_x$ alloy has a wide range of applications, including in electronic and photonic devices. We investigate the Al-induced layer exchange (ALILE) growth of amorphous $Si_{1-x}Ge_x$ on an insulator. The ALILE allowed $Si_{1-x}Ge_x$ to be large grained (> 50 μm) and highly (111)-oriented (> 95%) over the whole composition range by controlling the growth temperature (≤ 400 °C). From a comparison with conventional solid-phase crystallization, we determined that such characteristics of the ALILE arose from the low activation energy of nucleation and the high frequency factor of lateral growth. The $Si_{1-x}Ge_x$ layers were highly p-type doped, whereas the process temperatures were low, thanks to the electrically activated Al atoms with the amount of solid solubility limit. The electrical conductivities approached those of bulk single crystals within one order of magnitude. The resulting $Si_{1-x}Ge_x$ layer on an insulator is useful not only for advanced SiGe-based devices but also for virtual substrates, allowing other materials to be integrated on three-dimensional integrated circuits, glass, and even a plastic substrate. *Published by AIP Publishing.*
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I. INTRODUCTION

$Si_{1-x}Ge_x$ alloys are all-proportional solid solutions which exhibit a bandgap and lattice constant between those of Si and Ge.[1] The tuning of the SiGe composition enables a higher carrier mobility than Si[2,3] and a large light absorption coefficient at an arbitrary wavelength.[4,5] SiGe-on-insulator (SGOI) structures have been widely investigated for use in thin-film transistors,[6,7] thin-film solar cells,[5,8] and on-chip optical interconnects.[9,10] A (111)-oriented SGOI is of particular interest because it works as a virtual substrate for III-V compound semiconductors[11,12] and silicide materials.[13–15]

For incorporating SGOI structures in inexpensive glass substrates or three-dimensional large-scale integrated circuits (LSIs), the entire process from crystallization to device fabrication, including impurity doping, must be done at low temperature (<500 °C) to avoid damage.[16–19] Metal-induced layer exchange (MILE) was developed for elemental Si[20–29] and Ge,[30–35] which allowed for large-grained, orientation-controlled layers on insulators at low temperature. For optoelectronic device applications, the MILE using Al has been actively investigated for fabricating highly doped p-type layers, also working as seed layers for light absorption layers.[21,22,34] Several attempts have been made to fabricate high-quality SiGe alloys through MILE.[36–41] Large-grained (∼10 μm), preferentially (111)-oriented SGOIs were achieved when the Si or Ge compositions were low (≤ 20%); however, the grain size and (111)-orientation fraction deteriorated as SiGe approached intermediate compositions.[38,40] Very recently, we fabricated highly (111)-oriented $Si_{0.4}Ge_{0.6}$ using Al-induced layer exchange (ALILE) by tuning the growth conditions, that is, growth temperature, thicknesses of Al and SiGe layers, and interlayer thickness between SiGe and Al.[42]

In this study, we demonstrate highly (111)-oriented, large-grained $Si_{1-x}Ge_x$ over the whole composition range. The origin of the large grain growth is discussed by comparing the growth properties of ALILE with those of conventional solid-phase crystallization (SPC).

II. EXPERIMENT

Figure 1(a) presents a schematic of the sample preparation process. Preparation of the Al and amorphous (a-) $Si_{1-x}Ge_x$ layers (each 50 nm thick) on a SiO_2 glass substrate

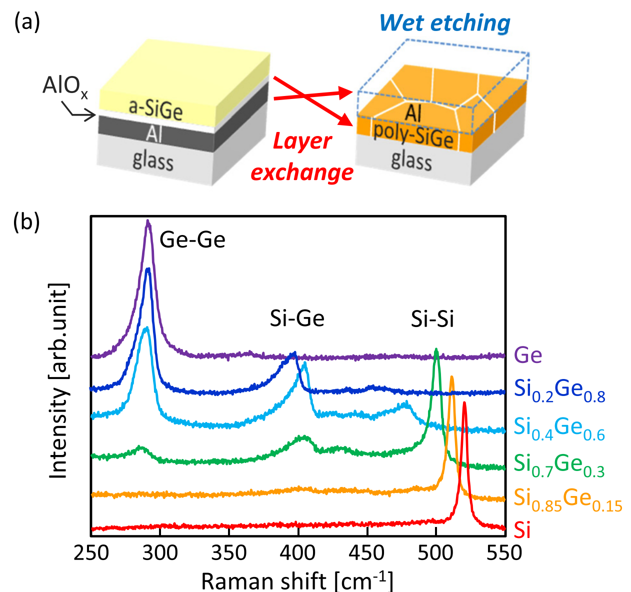

FIG. 1. (a) Schematic image of the sample preparation procedure. (b) Raman scattering spectra of the $Si_{1-x}Ge_x$ (x: 0, 0.15, 0.3, 0.6, 0.8, and 1) samples after annealing for 100 h. The annealing temperatures are 400 °C for Si, 375 °C for $Si_{0.85}Ge_{0.15}$ and $Si_{0.7}Ge_{0.3}$, 350 °C for $Si_{0.4}Ge_{0.6}$, and 340 °C for $Si_{0.2}Ge_{0.8}$ and Ge.

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was performed at room temperature using radio frequency (RF) magnetron sputtering (base pressure: 3.0×10^{-4} Pa) with Ar plasma. The RF power was set to 50 W for all the $Si_{1-x}Ge_x$ targets. The Ge composition x in the prepared a-$Si_{1-x}Ge_x$ layers was determined to be 0, 0.15, 0.3, 0.6, 0.8, and 1 by Rutherford backscattering spectrometry (RBS). Between the two deposition cycles, the Al film was exposed to air for 30 min to form a native Al oxide layer as a diffusion-limiting layer.[23,31] The samples were then annealed at 340–450 °C in a N_2 ambient chamber (Linkam 10042 D) using an *in-situ* optical microscopy observation system (Keyence VH-5500) until the layer exchange was finished. The Al and AlO_x layers were then etched away with HF solution (HF: 1.5%) for 1 min. The crystal quality of the samples was evaluated using Raman scattering spectroscopy (Nanophoton RAMANplus, spot size 1 μm, wavelength 532 nm) and electron backscatter diffraction (EBSD) analysis (TSL OIM Analysis). The Hall effect measurement (Bio-Rad HL5500PC) with the Van der Pauw method was performed for $1 \times 1\ cm^2$ square samples.

III. RESULTS AND DISCUSSION

The layers remaining on the substrates were evaluated using microprobe Raman scattering spectroscopy. Figure 1(b) shows Raman peaks corresponding to Si-Si, Si-Ge, or Ge-Ge vibration modes. These results indicate that the crystalline $Si_{1-x}Ge_x$ layers are formed on the substrates by layer exchange. The SiGe compositions, calculated from the Raman spectra using the equation proposed by Mooney *et al.*,[43] were the same as those of the as-prepared a-$Si_{1-x}Ge_x$ layers. The SiGe composition was uniform in the plane for each sample, which is proposed to arise from the diffusion coefficients of Si and Ge in Al being almost equal.[41,42]

Figures 2(a)–2(i) show the typical growth evolution of ALILE, observed using *in-situ* optical microscopy during annealing. These micrographs show the back surface of the samples observed through the transparent SiO_2 substrates. The dark-colored area indicates the semiconductors, and the bright-colored area indicates Al. The micrographs indicate that, during annealing, the semiconductor atoms diffuse to the back surface and then cover the entire surface of the substrate. This means that nucleation occurs and then the domain grows laterally with the increasing annealing time. The domain size saturates when the domains collide with each other. We note that dendrite patterns are present in each domain of Si and $Si_{0.4}Ge_{0.6}$ [Figs. 2(c) and 2(f)]. The dendrite patterns correspond to island layers formed on the front surfaces.[20,34] Although Ge also has island layers on the front surface, these are not visible from the backside [Fig. 2(i)]. This is likely because the transparency of SiGe layers decreases with the increasing Ge fraction. Thus, there is no actual difference in the growth morphology among the samples. These phenomena were quantitatively evaluated: Figures 2(j) and 2(k) show that the nucleus density and domain size increase with increasing annealing temperature. The lower growth temperature facilitates a lower nucleation rate and eventual nuclei density [Fig. 2(j)]. The lower growth temperature also enables a lower lateral growth velocity and a larger eventual domain size [Fig. 2(k)], reflecting the nuclei density. The growth temperature dependence of the nuclei density and domain size was the same among all $Si_{1-x}Ge_x$ samples prepared in this study. The eventual domain size was over 100 μm over the entire range of $Si_{1-x}Ge_x$ compositions.

The nucleation rate n and lateral growth velocity v_g of the samples were calculated from the slopes of the time dependent nuclei density and domain size, with typical examples shown in Figs. 2(j) and 2(k). Figure 3(a) shows that there is no clear dependence of the Ge fraction on n. This result suggests that n is determined using the diffusion-limiting AlO_x layer whose thickness strongly depends on the humidity during Al air exposure. Figure 3(b) shows that

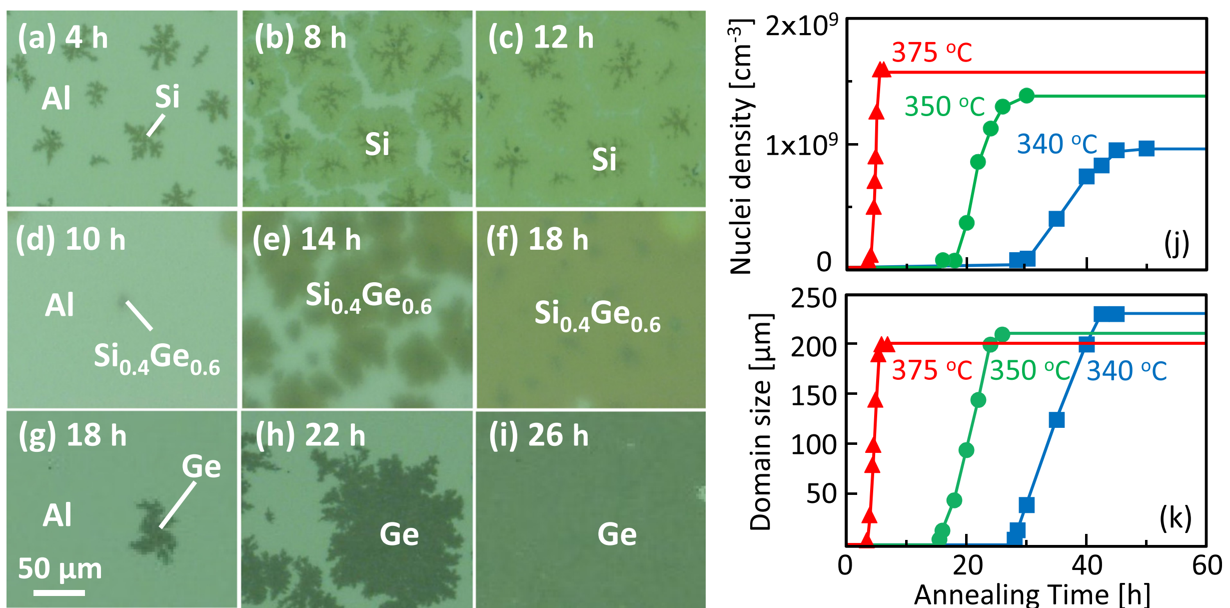

FIG. 2. *In situ* observation of the ALILE growth. Optical micrographs of (a)–(c) Si annealed at 400 °C, (d)–(f) $Si_{0.4}Ge_{0.6}$ annealed at 375 °C, and (g)–(i) Ge annealed at 350 °C. Here, back surfaces are observed through the transparent SiO_2 substrate. Annealing time dependence of the (j) nuclei density and (k) domain size for Ge derived from the micrographs.

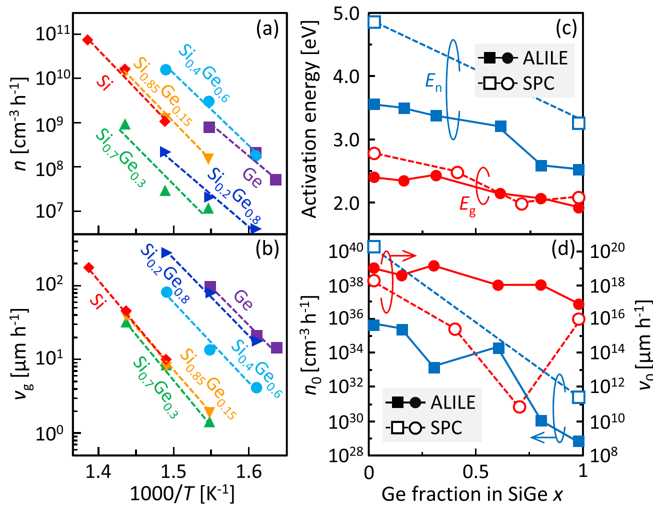

FIG. 3. Growth properties of the $Si_{1-x}Ge_x$ (x: 0, 0.15, 0.3, 0.6, 0.8, and 1) samples. Arrhenius plots of the (a) nucleation rate n and (b) lateral growth velocity v_g. (c) Ge fraction dependence of the activation energies of nucleation E_n and lateral growth E_g. (d) Ge fraction dependence of the frequency factors of nucleation n_0 and lateral growth v_0. For comparison, the data of SPC regarding the nucleation of Si[41] and Ge[42] and the lateral growth of SiGe[18] are shown in (c) and (d).

v_g increases with the increasing Ge fraction, which is the same behavior as the crystallization of the a-$Si_{1-x}Ge_x$ layers.[16,18] We note that the ALILE provides v_g two orders of magnitude higher than that of the SPC of a-$Si_{1-x}Ge_x$,[18] which leads to large domain growth.

From the Arrhenius equation and the results in Figs. 3(a) and 3(b), we determined the activation energies of nucleation E_n and lateral growth E_g and the frequency factors of nucleation n_0 and lateral growth v_0. Figures 3(c) and 3(d) show that both the activation energies and the frequency factors decrease with increasing Ge fraction x, respectively. These facts indicate that the lowering of the growth temperature with increasing x arises from the reduction of the activation energies. Therefore, we compared the growth characteristics between ALILE and SPC as follows. Figure 3(c) shows that ALILE exhibits a lower E_n than SPC.[44,45] This is because, with ALILE, SiGe nucleates in the Al grain boundaries at a lower interfacial energy compared to SPC, where SiGe nucleates in the amorphous SiGe layer.[26] Figure 3(c) also shows that E_g is almost the same between ALILE and SPC.[18] This is reasonable considering that E_g corresponds to the energy required for SiGe atoms to adhere to crystalline SiGe. Figure 3(d) shows that ALILE exhibits a lower n_0 than SPC.[44,45] This can be explained by the density of SiGe atoms being lower in Al for ALILE than amorphous SiGe for SPC. Figure 3(d) also shows that ALILE exhibits a higher v_0 than SPC.[18] A metal layer in contact with semiconductors weakens the covalent bonds between the semiconductor atoms at the interface due to electronic interactions.[46] This phenomenon allows for the high mobility of the interfacial semiconductor atoms and thus the high v_0 for ALILE.[41] The above discussion accounts for why ALILE can provide larger SiGe grains at lower temperature compared to SPC.

The crystal orientation and actual grain size of the $Si_{1-x}Ge_x$ layers formed by low temperature annealing (≤400 °C) for 100 h were evaluated using EBSD. Figures 4(a)–4(f) show that the $Si_{1-x}Ge_x$ layers are highly (111)-oriented over the entire SiGe composition range. The (111) orientation can be explained from the perspective of the appearance of the energetically stable plane.[24,31] Figures 4(g)–4(l) show that the $Si_{1-x}Ge_x$ layers have grains with diameters of several tens of μm. These actual grain sizes are smaller than the domain size observed from optical microscopy because the domains are divided into several grains.[32–35] Figure 4(m) shows that the (111) fraction and grain size do not depend on the SiGe composition but correlate roughly with the growth rate. In ALILE, the thicker interlayer between the semiconductor and Al layers provides the slower growth rate.[31,32] The slow growth rate and the large grain size for $Si_{0.7}Ge_{0.3}$ are likely attributed to the fact that the humidity of the air was relatively high (≥90%) during the sample preparation for $Si_{0.7}Ge_{0.3}$. Therefore, regardless of the composition, slow (longtime) annealing is a key to fabricate a highly oriented, large-grained SiGe layer. For the real industrial application, the annealing time can be shortened to less than one hundredth by initially doping SiGe in Al and by modulating the interlayer between SiGe and Al.[32] Thus, we have demonstrated SiGe layers on an insulator with a (111) orientation fraction of over 95% and a grain size over 50 μm over the entire SiGe composition range. These values are the highest among the low temperature synthesized SGOIs.[16–19,36–41]

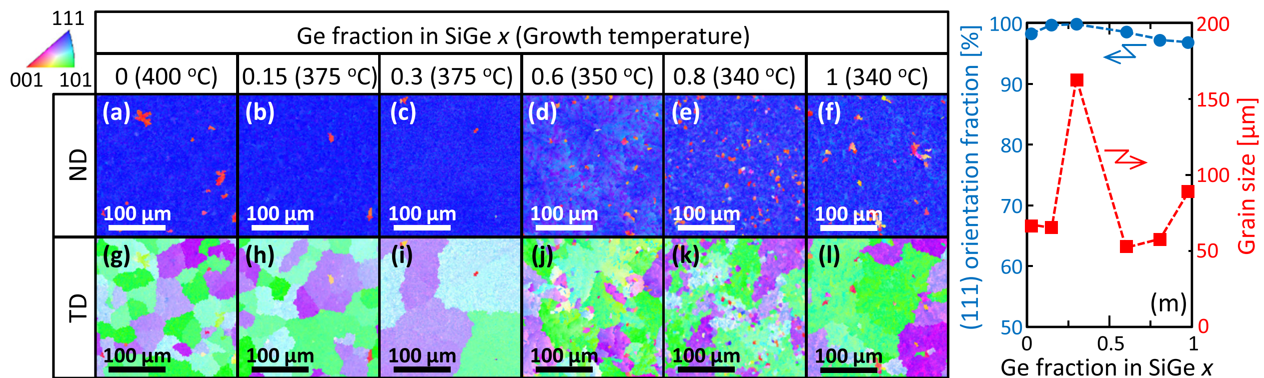

FIG. 4. EBSD analyses of the grown $Si_{1-x}Ge_x$ (x: 0, 0.15, 0.3, 0.6, 0.8, and 1) samples. EBSD images taken from the same region in the (a)–(f) normal direction (ND) and (g)–(l) transverse direction (TD) relative to the sample substrates. The coloration indicates the crystal orientation. (m) (111) orientation fraction and grain size as a function of Ge fraction. By definition, the (111) fraction included planes with tilts of up to 15° from the exact (111) plane; a grain was considered to be an area surrounded by random grain boundaries.

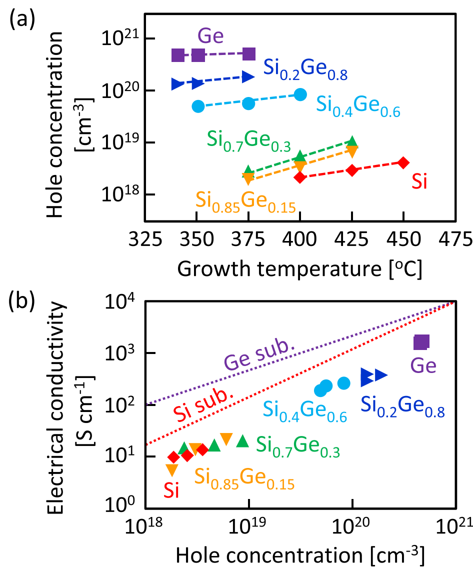

FIG. 5. Electrical properties of the grown $Si_{1-x}Ge_x$ (x: 0, 0.15, 0.3, 0.6, 0.8, and 1) samples. (a) Hole concentration as a function of growth temperature. (b) Relationship between the electrical conductivity and the hole concentration. The data of single crystal Si and Ge wafers are shown by dotted lines.

The electrical properties of the $Si_{1-x}Ge_x$ layers were evaluated using Hall measurements with the Van der Pauw method. The sample of each composition was formed at three annealing temperatures. The annealing times were 100 h for low temperature, 50 h for middle temperature, and 25 h for high temperature. According to the *in situ* observation, these times are enough to saturate the crystal growth of the samples. All samples exhibited p-type conduction, which is consistent with the fact that Al works as a p-type impurity for Si and Ge. Figure 5(a) shows that the hole concentration increases with the increasing Ge fraction and growth temperature. Secondary ion mass spectrometry determined that the Al concentrations in the grown layers are $2 \times 10^{18}\,cm^{-3}$ for Si formed at 400 °C and $4 \times 10^{20}\,cm^{-3}$ for Ge formed at 340 °C. These values are almost equal to each hole concentration [Fig. 5(a)], indicating that the Al atoms in Si and Ge are fully activated. In addition, the amounts of Al atoms in Si and Ge are equal to each solubility limit.[47] These results suggest that the hole concentration in the $Si_{1-x}Ge_x$ layers is determined by the solubility limit of Al in $Si_{1-x}Ge_x$. Because solubility limits increase with increasing temperature, this model accounts for the growth temperature dependence of the hole concentration in the $Si_{1-x}Ge_x$ layers [Fig. 5(a)]. Figure 5(b) shows that the electrical conductivities of the Si and Ge layers approach those of bulk single crystals within one order of magnitude despite the fact that these layers are polycrystalline. Such high conductivities are likely owing to the large grains, i.e., few grain boundaries, in the ALILE grown layers. Thus, ALILE enables the self-organization of p-type SiGe layers with high conductivity at low temperature.

IV. CONCLUSION

We have achieved ALILE growth of a-$Si_{1-x}Ge_x$ on insulators at low temperatures (≤ 400 °C) over the entire composition range. The ALILE provided a low nucleation frequency and high lateral growth velocity, resulting in large $Si_{1-x}Ge_x$ grains with diameters of not less than 50 μm. The area fractions of the (111) orientation were more than 95%. The SGOI fabricated in this study is useful as a virtual substrate, allowing advanced materials to be integrated on three-dimensional LSIs, glass, and even a plastic substrate.

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