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Testbeam results of irradiated ams H18 HV-CMOS pixel sensor prototypes

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ABSTRACT: HV-CMOS pixel sensors are a promising option for the tracker upgrade of the ATLAS experiment at the LHC, as well as for other future tracking applications in which large areas are to be instrumented with radiation-tolerant silicon pixel sensors. We present results of testbeam characterisations of the 4th generation of Capacitively Coupled Pixel Detectors (CCPDv4) produced with the ams H18 HV-CMOS process that have been irradiated with different particles (reactor neutrons and 18 MeV protons) to fluences between 1×10^{14} and 5×10^{15} 1-MeV- n_{eq}/cm^2. The sensors were glued to ATLAS FE-I4 pixel readout chips and measured at the CERN SPS H8 beamline using the FE-I4 beam telescope. Results for all fluences are very encouraging with all hit efficiencies being better than 97% for bias voltages of 85 V. The sample irradiated to a fluence of 1×10^{15} n_{eq}/cm^2 — a relevant value for a large volume of the upgraded tracker — exhibited 99.7% average hit efficiency. The results give strong evidence for the radiation tolerance of HV-CMOS sensors and their suitability as sensors for the experimental HL-LHC upgrades and future large-area silicon-based tracking detectors in high-radiation environments.

Contents

1 Introduction

To extend the physics reach of the Large Hadron Collider (LHC), upgrades are planned to increase its luminosity allowing for up to $3000\,\mathrm{fb}^{-1}$ of data to be collected by ATLAS and CMS. The increase in radiation damage associated with this also requires upgrades to the experiments, in particular the replacement of the Inner Trackers, which requires very large areas of extremely radiation-tolerant silicon detectors [1, 2].

Due to the large areas to be instrumented, special care has to be taken to investigate cost-efficient, but still very radiation-tolerant sensor options. Thanks to their large production output, CMOS foundries are capable of producing large areas of silicon at — compared to bespoke hybrid pixel detectors — affordable cost. Some CMOS processes developed for the automotive industry (HV-CMOS[1]) or imaging applications (HR-CMOS[2]) are promising candidates for sensor production, thanks to their tolerance to high bulk bias voltages which are necessary for fast charge collection (see e.g. [3]). In this work, the radiation tolerance of a test chip produced with the ams H18[3] High-Voltages CMOS process [4] was investigated after irradiation with mixed spectrum reactor neutrons at the TRIGA reactor [5] of the JSI, Ljubljana, Slovenia, and with 18 MeV protons at the Bern Cyclotron Laboratory [6], Switzerland.

An important feature of processes suitable for sensor production is the existence of a so-called deep n-well (DNW) in a moderately p-doped bulk, which is necessary to insulate the circuits from high voltages (see figure 1a). The depth of the DNW is a few µm, preventing the depletion region

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[1]High-Voltage CMOS.

[2]High-Resistivity CMOS.

[3]ams **H18** is an **H**V-CMOS process with **18**0 nm feature size by ams/IBM.
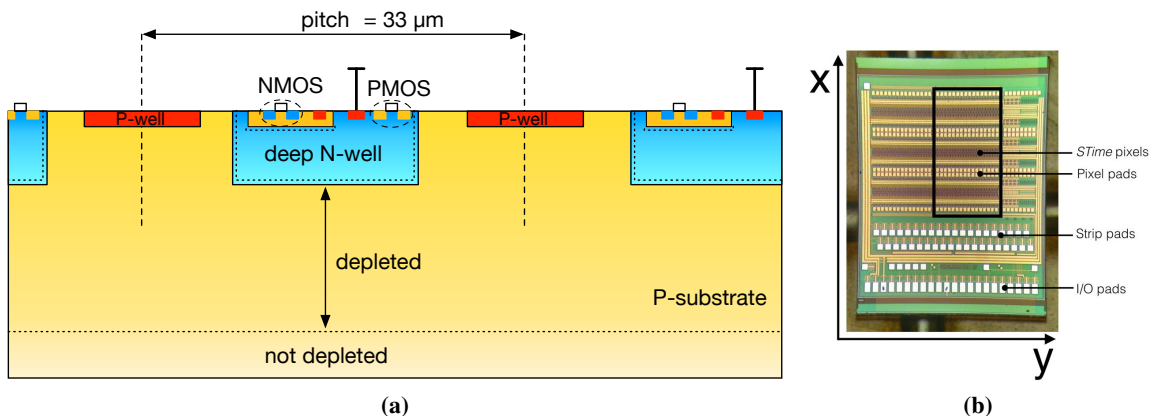
Figure 1. (a) Schematic cross section of an HV-CMOS sensor: the deep n-well is the charge-collecting electrode and also contains additional CMOS circuits such as a preamplifier. (b) Photograph of the CCDPv4 sensor used in this study with the sub-matrix of STime-type pixels marked.

inside the n-well from reaching the in-pixel CMOS FETs, which would cause their behaviour to change. The DNW itself must also have a suitable doping profile that avoids too high electric fields at its edges which would cause impact ionisation and thus breakdown.

In its most simple form, a matrix of DNWs could be used as a classical planar n^+-in-p pixel detector. However, the nominal resistivity of the standard base material is only $10–20\,\Omega \cdot cm$, leading to a calculated depletion depth of only about $10–15\,\mu m$ for bias voltages of $80–150$ Volts. Such thin layers of depleted silicon would yield a most probable charge of only about $600–900$ electron-hole-pairs for a vertically penetrating minimum ionising particle (MIP), clearly a very challenging value for classical pixel readout chips with usual threshold settings of 1500 electrons or above.

However, the CMOS production process allows for an in-pixel amplification stage. If combined with small pixels that yield low capacitance values, such in-pixel circuits can be used to amplify the signal to a suitable amplitude for a discriminator or directly for a readout chip. Examples for monolithic HV-CMOS sensors produced in the ams H18 process are the MuPix family of sensor prototypes [7], conceived for the Mu3e experiment at PSI. Sensors relying on dedicated readout chips are e.g. the HV2FEI4/CCPD (*HV-CMOS-to-FE-I4* or alternatively *Capacitively Coupled Pixel Detector*) prototypes [8] intended for use in the upgraded ATLAS detector at the HL-LHC. A schematic cross section of an HV-CMOS sensor is depicted in figure 1.

CCPD sensors are designed to be coupled to a pixel readout chip. As suggested by the name, this can be done by capacitive coupling using non-conductive glue since the amplifier and discriminator output signal is large and fast enough to not be affected by the glue-filled gap in the signal path. For comparison, the classical bump-bonding process is also possible. For R&D purposes, the sensor can also be operated standalone, and pixel outputs from the matrix can be investigated by configuring internal multiplexers. In this way, however, only individual pixels can be observed. In addition, several test structures and circuits have been added to the prototypes. For this study, ATLAS FE-I4 [9] IBL[4] [10] readout chips were glued to CCPDv4 HV-CMOS sensors,

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[4]Insertable b-layer, the new innermost 4th pixel layer of ATLAS at a radius of only 3.3 cm.

which was the latest generation of capacitively coupled HV-CMOS sensors available at the time of the beam test.

2 HV-CMOS devices under test

2.1 CCPDv4

CCPDv4[5] sensors — the 4th generation of test sensors produced in the ams H18 process using regularly scheduled multi-project wafer productions — were produced on a nominal $10\,\Omega \cdot \text{cm}$ substrate; details about the creation of the samples can be found in [11], therefore only a brief summary will be presented here. The design rule set specifies a minimum breakdown voltage of $60\,\text{V}$, the experimental breakdown voltage was found to be at $93\,\text{V}$. However, the noise gradually increases already at bias voltages above $80\,\text{V}$. The CCPDv4 contains a pixel matrix matching the FE-I4 with several different pixel flavours, out of which this study focused on the performance of the so-called *STime*-type pixels (see figure 1b). Each *STime* pixel on the HV-CMOS sensor features a size of only $33\,\mu\text{m}$ by $125\,\mu\text{m}$ and contains an amplifier and a discriminator together with a 4-bit in-pixel Tune-DAC, allowing a per-pixel threshold tuning. To match the FE-I4 pixel size of $50\,\mu\text{m}$ by $250\,\mu\text{m}$, the HV-CMOS pixels are grouped together in gangs of three, forming *two* $100\,\mu\text{m}$ by $125\,\mu\text{m}$ large macro-pixels for each *two* neighbouring $50\,\mu\text{m}$ by $250\,\mu\text{m}$ pixels (see figure 2a). While the chip allows the encoding of the hit pixel's coordinate, this feature was not used during this study and testbeam reconstruction was performed on the macro-pixel level. However, the threshold tuning of the HV-CMOS matrix was performed on the pixel level. The CCPDv4 sensors were glued to FE-I4 readout chips (see figure 2b) using Araldite 2011 non-conductive epoxy glue on a SET Accµra 100 flip-chip bonder at the University of Geneva with a typical glue thickness of less than $1\,\mu\text{m}$. The calibration factor between deposited charge and threshold voltage of $\sim 8.6\,\text{e}^-/\text{mV}$ from [11] can also be applied to this work, however, as it has not been re-measured, the thresholds are given in mV throughout this work.

2.2 Irradiated samples

In this paper, fluences are given in 1-MeV-Neutron equivalents per area, abbreviated to $\text{n}_{\text{eq}}/\text{cm}^2$.

The relevant fluences for the application in the upgraded ATLAS Inner Tracker (ITk) at HL-LHC (target integrated luminosity of $3000\,\text{fb}^{-1}$) range between *about* 2×10^{14} (outer strip layers), 1×10^{15} (outermost pixel layer), 4×10^{15} (pixel layer 1, assuming exchange after $1500\,\text{fb}^{-1}$) and $1 \times 10^{16}\,\text{n}_{\text{eq}}/\text{cm}^2$ (pixel layer 0, assuming exchange after $1500\,\text{fb}^{-1}$) [12]. The most relevant range for the ATLAS HV-CMOS pixel demonstrator project is in the region of the outermost pixel layer, i.e. around $1 \times 10^{15}\,\text{n}_{\text{eq}}/\text{cm}^2$, where the area to be instrumented is comparatively large.

Earlier measurements [13, 14] suggested that the fluence region with the worst collected charge/hit efficiency is at few $10^{14}\,\text{n}_{\text{eq}}/\text{cm}^2$. This is attributed to the set-in of trapping, causing the loss of diffusion. The performance recovers at about $1 \times 10^{15}\,\text{n}_{\text{eq}}/\text{cm}^2$ due to an increase of the depletion zone outweighing the reduced diffusion. The latter effect is attributed to a suspected acceptor removal effect. In view of these findings, this work focussed on the fluence region around the recovery point.

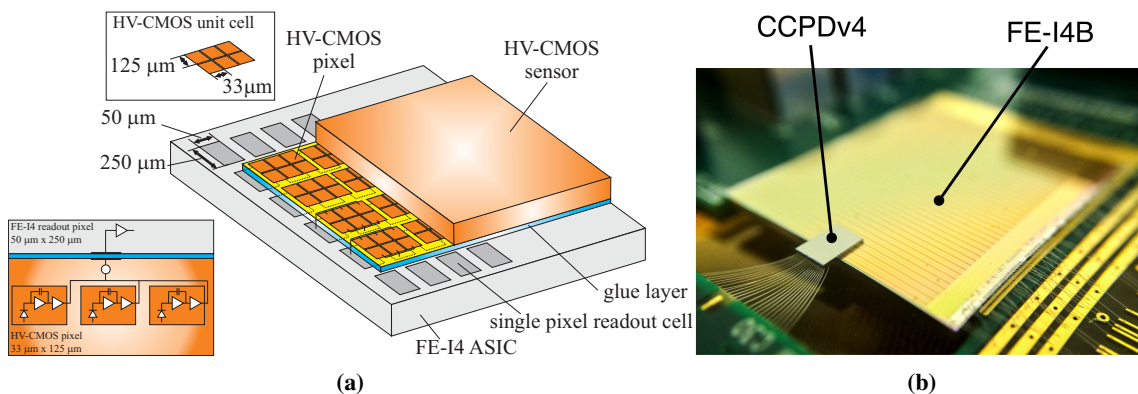[5]Sometimes also referred to as **AMS180v4**.

Figure 2. (a) Schematic representation (not in scale) of the HV-CMOS to FE-I4 connections. The bottom-left inset shows how three HV-CMOS pixels (forming a so-called *macro-pixel*) are capacitively coupled to a single FE-I4 readout pixel. (b) Final assembly of a FE-I4 pixel readout chip to a HV-CMOS CCPDv4 sensor via capacitive coupling. [11].

While it is very difficult to irradiate samples mounted on a PCB in a reactor, this is possible for irradiation with 18 MeV protons at the Bern Cyclotron [6]. Therefore, one sample was subsequently irradiated to 1.3×10^{14} n_{eq}/cm^2 and 5×10^{14} n_{eq}/cm^2 at Bern, while two individual samples were irradiated to 1×10^{15} n_{eq}/cm^2 and one to 5×10^{15} n_{eq}/cm^2 with reactor neutrons at the TRIGA reactor of the JSI in Ljubljana [5].

3   Testbeam experimental setup

The main part of the experimental beam test setup has already been described in earlier publications on the FE-I4 telescope itself [15] and also in a paper about testbeam results with an unirradiated CCPDv4 sample [11].

For this study, cooling of the irradiated devices under test (DUTs) had to be provided to reduce the radiation-induced leakage current. To this end, a dedicated cold box has been implemented (see figure 3). It consists of a cooled base plate housed inside an enclosure of a rugged insulating foam. The copper base plate contains a regular array of threaded holes (M5, 1 cm pitch) to be able to conveniently fix samples inside. Unlike earlier approaches, such as the DOBox [16, p. 49 ff.], the base plate is not cooled by dry ice, but by a Huber Unistat chiller, which circulates a silicon oil coolant (that can be used to cool down to $-75°C$) through a copper tube that is glued into in a milled semi-circular groove around the edge of the base plate. On top of the plate, a pipe is attached to the cooled plate to pre-cool the nitrogen used for flushing the box to avoid condensation; this pre-cooling is essential to reach low sample temperatures. The targeted on-sensor temperature for the ITk Pixel Detector — and therefore also for our cold box to be as realistic as possible — is $-25°C$.

The final setup can be seen in figure 3. During the commissioning of the box, the temperature of the CCPD DUT and FE-I4 readout chip reached $-28.6°C$ and $-26.9°C$, respectively, with a nitrogen temperature of $-28°C$. Both CCPD and FE-I4 were powered on. The temperature measurements were done with an uncertainty of $2°C$, the measured relative humidity typically is 5–7%.
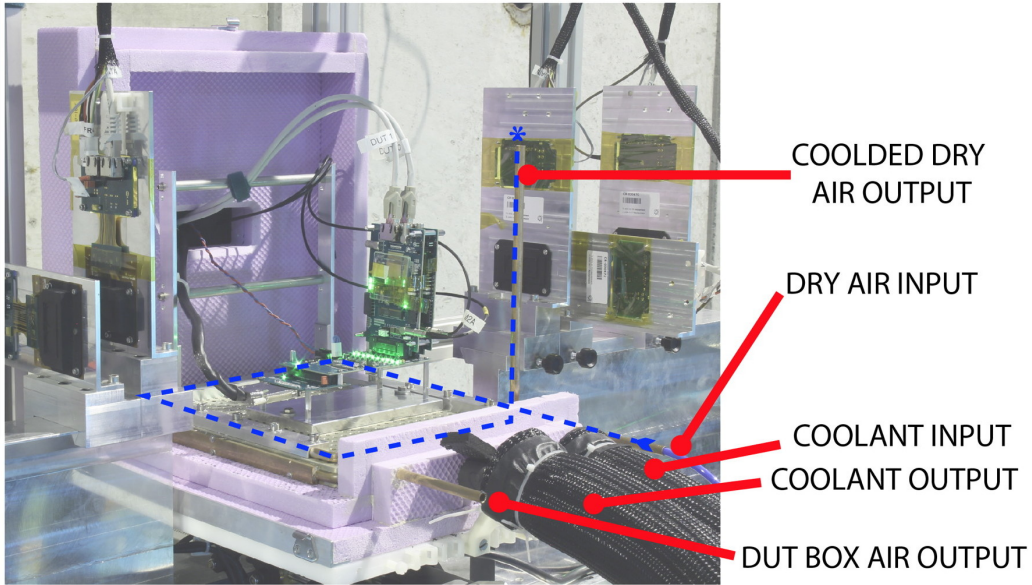
Figure 3. Photograph of the opened cooling box. The insulating foam of the remaining side wall containing the feedthrough for the DUT connection cables can be seen in violet. To the left and right, FE-I4 telescope planes are visible. The coolant and nitrogen inputs/outputs as well as the exhaust pipe are highlighted.

4 Results

4.1 Hit efficiencies

The hit efficiency is calculated as the ratio between the number of clusters in the DUT that match reconstructed tracks from the beam telescope and the number of the good reconstructed tracks that are predicted to penetrate the DUT within its active area. The search area for tracks is an ellipse with the major and minor radii being 1.5 macro-pixel pitches in x and y coordinates around the center of the cluster, i.e. 150 μm and 187.5 μm respectively (see also figure 4a). Compared to the residuals of the neutron-irradiated CCPDv4 sample (1×10^{15} n_{eq}/cm^2, figure 4b and 4c), the size of the search area encompasses virtually the complete residual distributions.
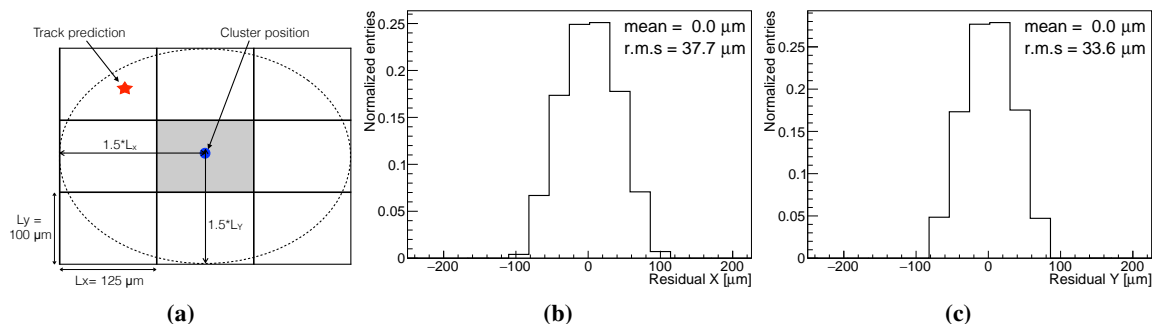

Figure 4. (a) Graphical depiction of the search area used to compute the hit efficiency, taken from [11]. Normalised residual distributions of the 1×10^{15} n_{eq}/cm^2 DUT along the x (b) and y (c) directions.

To avoid the excessive use of figures, the general properties will be introduced for one DUT (1×10^{15} n_{eq}/cm^2, neutron-irradiated) and then comparison plots will be used to assess the radiation effects for different fluences. The hit efficiency for the STime pixels in this sample at a bias voltage of 85 V and using a threshold of 80 mV is shown in figure 5a.

To avoid edge effects, the last 20 μm at the edge of the outermost pixels have been excluded as this is where the telescope resolution ($1\sigma \approx 10$ μm, see [15]) leads to tracks being mis-reconstructed to be within the sensor active area while in reality the particle did not penetrate it. It can be seen that a very homogeneous and high efficiency of 99.7% is reached across the whole matrix. By plotting the hit efficiency with sub-pixel resolution, it was found that there is no significant loss of hit efficiency in any region of the pixel (see figure 5b).
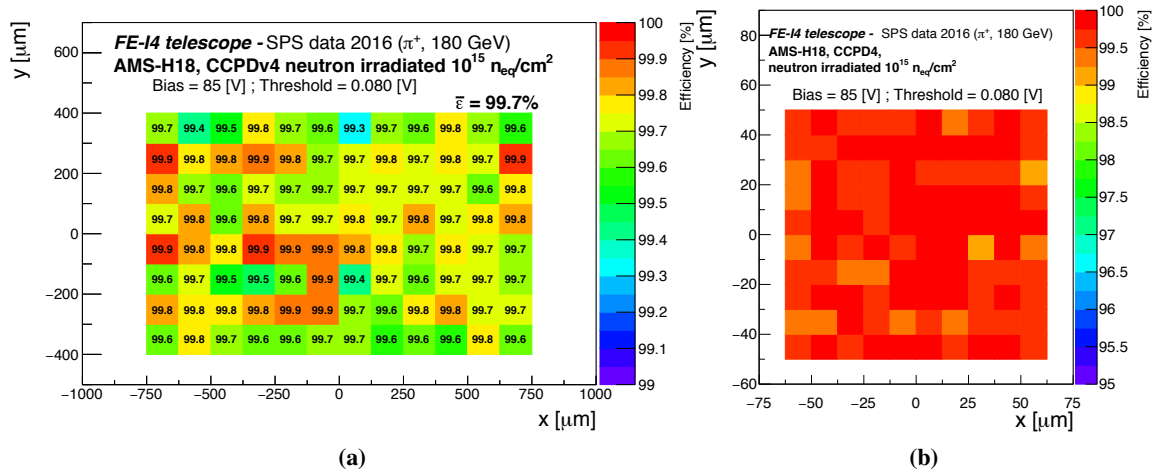

(a)   **(b)**

Figure 5. a) Hit efficiency map for CCPDv4 neutron-irradiated with 1×10^{15} n_{eq}/cm^2; the colour scale is only ranging from 99% to 100%. b) Sub-pixel hit efficiency map overlaid from all central pixels. No significant efficiency loss is visible in any region of the pixel. The threshold of 80 mV is assumed to be equivalent to $690\,e^-$ according to [11].

A more effective representation of the pixel hit efficiency distribution is by means of histograms, which allow to better judge outliers, for example due to defective sub-pixels. Figure 6 depicts hit efficiency histograms for samples irradiated with fluences of 1.3×10^{14}, 5×10^{14}, 1×10^{15} and 5×10^{15} n_{eq}/cm^2, which yield average hit efficiencies of 98.1%, 99.7%, 99.7% and 97.6%, respectively. These values are excellent and on a par with hit efficiencies of planar pixel sensors [17] — for comparison, detector specs often require hit efficiencies of $> 97\%$ after irradiation. For the highest fluence, it can be seen that there are several outlier pixels, most probably originating from individual deteriorated circuits due to the rather high fluence of 5×10^{15} n_{eq}/cm^2. It is possible that in future improved designs, these could be recovered by extending the operating point of internal DACs, but in any case this would require further detailed studies at circuitery level. It should be noted that for the 5×10^{14} n_{eq}/cm^2 sample, a working point at a bias voltage of only 60 V was chosen because at HV= 80 V the sample showed a slightly higher noise occupancy, with the consequence of having a slightly decreased hit efficiency at 80 V.

Bias-voltage and threshold scans were conducted to study their dependencies on the hit efficiency. The results are depicted in figure 7 and 8. It can be seen that for the bias voltage, a plateau
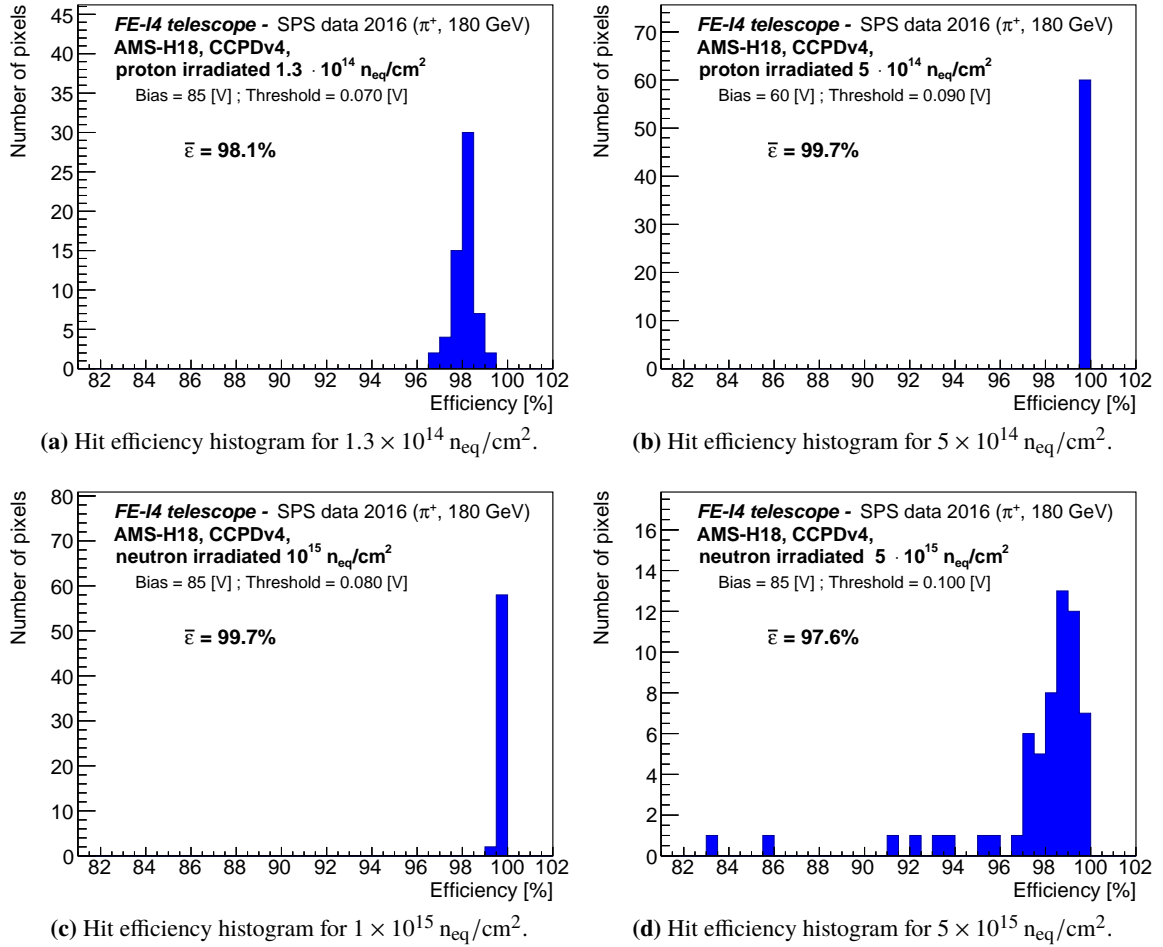
(a) Hit efficiency histogram for 1.3×10^{14} n_{eq}/cm^2.

(b) Hit efficiency histogram for 5×10^{14} n_{eq}/cm^2.

(c) Hit efficiency histogram for 1×10^{15} n_{eq}/cm^2.

(d) Hit efficiency histogram for 5×10^{15} n_{eq}/cm^2.

Figure 6. Hit efficiency histograms for different fluences of protons (upper row) and neutrons (lower row).The thresholds of 70, 80, 90 and 100 mV are assumed to be equivalent to 600, 690, 770 and 860 e^-, respectively, according to [11].

is reached after about 40 V, but in particular the very low and very high fluences profit from going to the highest possible bias voltages before the onset of breakdown, i.e. about 85 V for this design. This is probably due to the fact that the depletion zone is thin compared to that of passive hybrid pixel sensors and its increase with bias voltage contributes significantly to the hit efficiency. For the middle fluences, the extension is already large enough thanks to the acceptor removal effect to not require the highest possible bias voltages. There are indications from other ams H18-based sensors that at high bias voltages, charge multiplication effects may increase the detectable charge [18, p. 57 ff.], [19, p. 64 ff.]; this would be in line with the generally increased hit efficiency at bias voltages just below the breakdown.

In highly irradiated (above 10^{15} n_{eq}/cm^2) planar and 3D pixel sensors, it has been demonstrated that the high electric field combined with trapping due to radiation damage can lead to charge multiplication due to impact ionisation when sufficient high voltage is applied to the sensors [20]. This fact generates an increase of the signal associated to the passage of a particle, which is correlated to the increase in noise and leakage current in the device. For the 5×10^{15} n_{eq}/cm^2
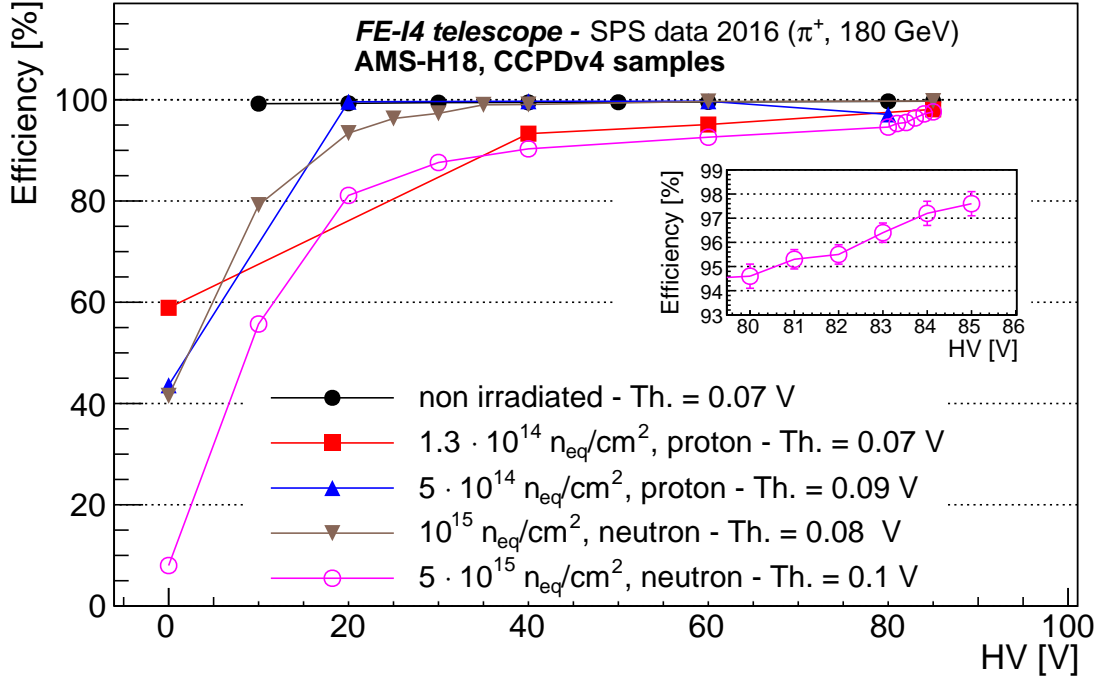
Figure 7. Average hit efficiency as a function of applied bias voltage. The inset shows the sudden increase in efficiency between 80 and 85 V, which could be attributed to charge multiplication. The thresholds of 70, 80, 90 and 100 mV are assumed to be equivalent to 600, 690, 770 and 860 e^-, respectively, according to [11].

CCPD sample, a sudden increase in detection efficiency is observed between 80 and 85 V, as shown in the insert of figure 7. This measurement is correlated with a similar increase in leakage current of the device. Such a behavior was not expected and was not observed for the other devices irradiated with lower fluences and can be interpreted as evidence for the existence of the charge multiplication process in HV-CMOS devices, as previously observed in planar and 3D pixel sensors.

From figure 8, three regions can be identified:

1. for very high thresholds there is a loss of events, and thus hit efficiency, due to low charge signals not being detected

2. for low threshold settings, the discriminators trigger on noise events and the dead time associated induces the measured inefficiency

3. in between there is a stable plateau, which is widest for the intermediate fluences, while for 1.3×10^{14} and 5×10^{15} n_{eq}/cm^2 the lack of signal due to small depletion depth or increased trapping, respectively, reduces the span of the plateau region, i.e. of the operation point

This is in line with earlier measurements [21] that saw an initial reduction in collected charge due to the loss of diffusing charge following the onset of trapping (at $\sim 10^{14}$ n_{eq}/cm^2). This is followed by a strong increase in collected charge thanks to the increase of the depletion depth, which is the result of acceptor removal (at $\sim 10^{15}$ n_{eq}/cm^2). At even higher fluences ($> 5 \times 10^{15}$ n_{eq}/cm^2), the increasing trapping leads to reduction in collected charge again.
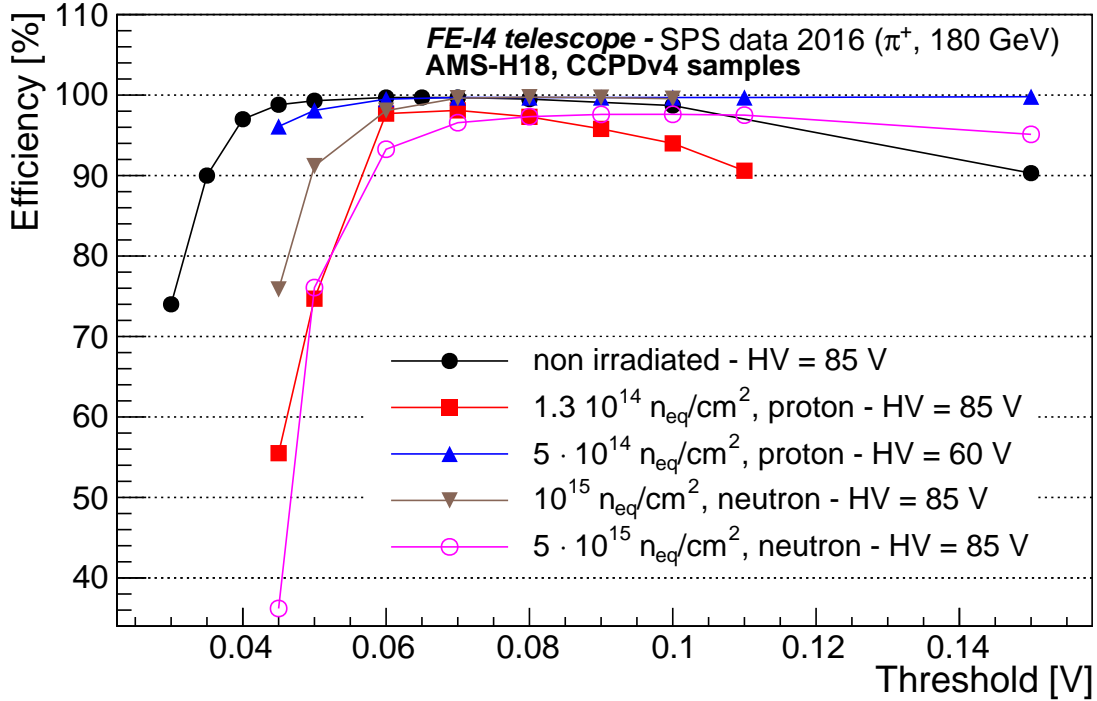
Figure 8. Average hit efficiency as a function of threshold voltage. For orientation: a thresholds of 60 mV is assumed to be equivalent to $520\,e^-$ according to [11].

4.2 Time resolution

For the HL-LHC ATLAS tracker, which will live in an environment with up to 200 pile-up events every 25 ns, it is essential to be able to assign the different tracks to the correct bunch crossing (BC) time window. This requirement imposes the utilisation of fast shaping and fast readout, making classical MAPS[6] readout schemes, like rolling shutter, impossible.

In the CCPDv4 architecture, the trigger handling is done by the FE-I4 readout chip that samples the preamplifier signal every clock cycle of 25 ns, which defines its time binning. However, due to time-walk of the FE-I4 preamplifier, particles depositing a small charge can sometimes be detected during the sampling interval next to the one of their arrival. During operation in the ATLAS Detector, the FE-I4 clock is synchronised to the bunch crossings of the LHC beams, meaning that particles arrive in a narrow time window with respect to the rising edge of the FE clock. By tuning the phase of the FE clock in a way that particles are detected mostly in one sampling interval, time-walk effects can be mostly mitigated in the LHC environment.

The SPS H8 beam, however, has no pronounced timing structure over the ~7 s long spill. Therefore, there is in general no coincidence of the time of arrival (ToA) of the particle and the FE clock, leading to an artificial smearing of the timing distribution. In order to mitigate this effect, a Clock-Phase Veto (CPV) as shown in figure 9a was implemented. Here, only particles that are detected in a tunable interval of 6.4 ns of the FE clock-phase can issue a trigger. The effect of the veto for a telescope plane is depicted in figure 9b. All timing results in this paper were taken with

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[6]Monolithic Active Pixel Sensors.

the CPV; remaining timing delays are likely to be caused by either slow charge collection, e.g. in regions with low electric field strength, by slow rise time of the amplifiers in the CCPD circuits, or by time walk effect on the CCPD's discriminators.
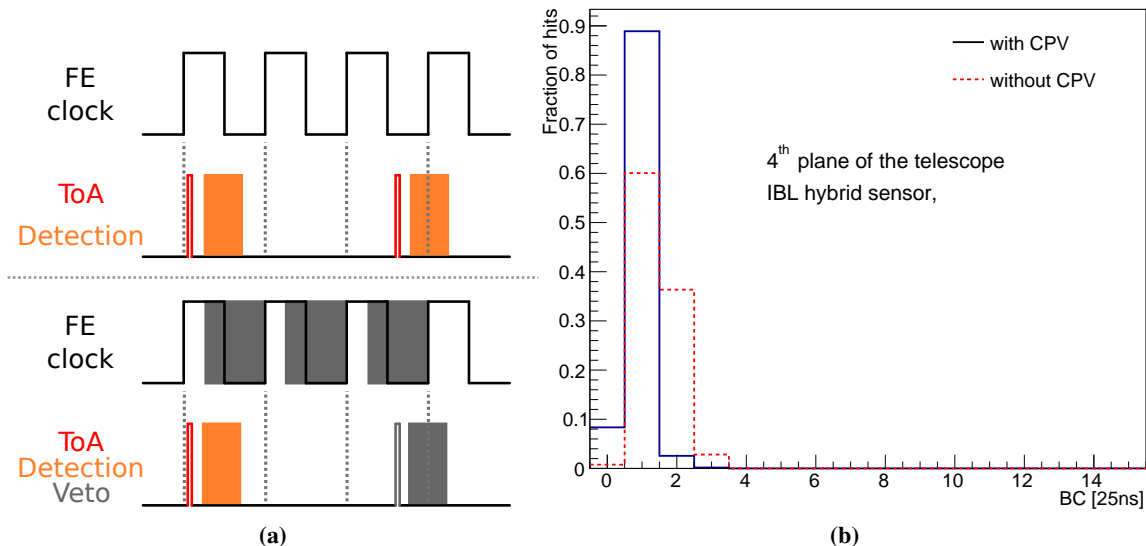

Figure 9. a) Schematic of the Clock-Phase Veto. Triggers from particles arriving late in the FE-I4 clock cycle are discarded, emulating a bunched particle beam. b) Timing distribution of a planar sensor of the *telescope plane* with and without Clock-Phase Veto.

Figure 10 shows the timing distributions of the four irradiated samples. Clearly, most events are collected within one timing bin. It appears that a cumulative in-time efficiency of better than 95% is achievable in 3 BCs for all fluences that have been investigated. This is comparable to the timing resolution of the FE-I4 telescope planes using passive 200 μm thin n-in-n sensors (see figure 9b), that have the same timing resolution as the baseline at least for the Pixel Endcap regions of the HL-LHC ATLAS Pixel Detector.

Some more insight can be gained when looking at the timing distribution for different applied bias voltages (figure 11a) and at the average timing of an event depending on the track's in-pixel position (figure 11b). As expected, the events still registered without any applied bias voltage are slow and very broad in their timing. The time resolution gradually increases with the increasing electric field causing faster collection. The in-pixel mean timing map indicates that central events — below or near the DNW — are collected faster, while events at the edges of the pixel are on average slower. The CCPDv4 sensors are biased from the front side as there is no backside contact. TCAD simulations carried out for this study indicate that this may lead to regions of low electric field strength, supporting our measurements. Future tests to include a backside contact are planned.

4.3 Cluster sizes

Due to the small depletion depth, elimination of diffusion due to trapping and almost perpendicular beam incidence, very little charge diffusion is expected. Table 1 shows this to be true, with the fraction of 2-hit clusters being reduced to the few % level. This actually is an advantage, as average
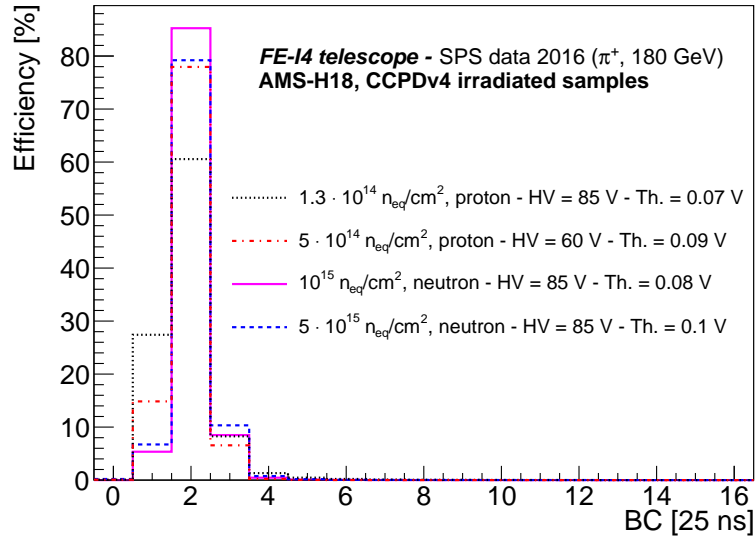
Figure 10. Timing distributions for the four irradiated CCPDv4 samples at the operational bias voltages. The thresholds of 70, 80, 90 and 100 mV are assumed to be equivalent to 600, 690, 770 and 860 e⁻, respectively, according to [11].
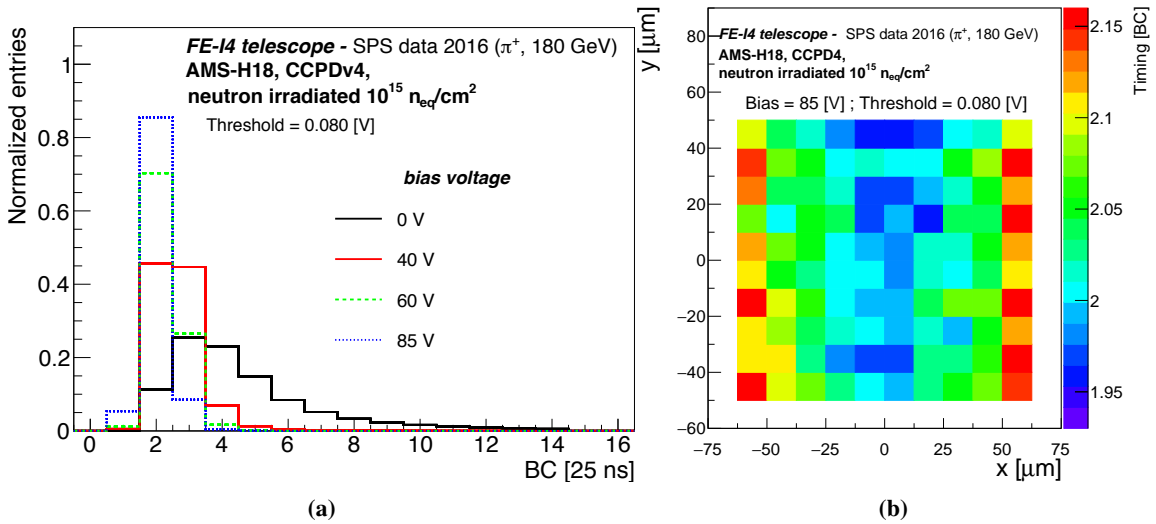

(a)   **(b)**

Figure 11. a) Timing for a CCPDv4 sensor for four values of the bias voltage. b) In-pixel timing map showing the mean timing of the event as depending on the track position inside the pixel. The threshold of 80 mV is assumed to be equivalent to 690 e⁻ according to [11].

cluster sizes of 2 — which are preferred thanks to their ability to yield better track resolution — can be created by tilting the sensors with respect to the expected track direction.

5 Conclusions and outlook

Hybrid CCPDv4 prototype sensors produced in the ams H18 HV-CMOS process were glued to FE-I4 readout chips, irradiated up to 5×10^{15} n_{eq}/cm^2 with reactor neutrons and 18 MeV protons

Table 1. Cluster size fractions for different fluences.

Fluence [n_{eq}/cm^2]	0	1.3×10^{14}	5×10^{14}	1×10^{15}	5×10^{15}
CS = 1	0.783	0.970	0.958	0.978	0.961
CS = 2	0.196	0.028	0.038	0.020	0.034
CS $\geq$ 3	0.020	0.002	0.004	0.002	0.004

and finally investigated in a testbeam experiment with high-energy pions at the SPS at CERN. Hit efficiencies up to 99.7% at 1×10^{15} n_{eq}/cm^2 were measured. Compared to unirradiated CCPD samples, they exhibit faster timing and less diffusion-based charge sharing. The improvement is attributed mainly to the increase in depletion depth as a consequence of reduced effective dopant concentration thanks to an acceptor removal effect in the low-resistivity ($10\,\Omega \cdot$ cm) p-type bulk.

The performance parameters after irradiation are impressive and close to being on a par with planar passive n-in-p pixel sensors. Further improvements can be expected by moderately increasing the base material resistivity. First sensors on such substrates (20, 80, 200 and 1000 $\Omega \cdot$ cm) have already been produced in the ams H35 process. In addition to the hybrid CCPD approach, the small feature size of the H18 process allows the pursuit of fully monolithic designs, which would be an even larger benefit for the instrumentation of large areas. The first such prototypes are the MuPix8 and ATLASPix designs, which use the new aH18 process.

Acknowledgments

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