Ternary full adder using multi-threshold voltage graphene barristors

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***Abstract*—Ternary logic circuit has been studied for several decades because it can provide simpler circuits and subsequently lower power consumption via succinct interconnects. We demonstrated a ternary full adder exhibiting a low power-delay-product of ~10^{-16} J, which is comparable with the binary equivalent circuit. The ternary full adder was modeled using device parameters extracted from the experimentally demonstrated multi-V_{th} ternary graphene barristors.**

***Index Terms*—Graphene barristor, Ternary full adder, Multi threshold voltage ternary graphene barristor, Ternary logic.**

I. Introduction

The demand for more functionality at lower power consumption has been driving the limit of complementary metal-oxide-semiconductor (CMOS) technology [1]. Multi-valued logic (MVL) has been pursued for several decades because it can provide significant advantages to reduce the complexity of interconnects and the arithmetic operations [2]-[11]. Various types of single or composite devices exhibiting multiple states have been investigated for this purpose. The single electron transistor, resonant tunneling diode, and ferroelectric field effect transistor (FET) are the only representatives of the long list investigated for MVL applications. Unfortunately, none of these devices has been implemented yet owing to practical limitations such as current drivability, operation temperature, and state stability.

Recently, various MVL architectures using carbon nanotube field effect transistors (CNTFET) have been studied because they can provide an ideal step wise I–V curve if three single-wall CNT FETs with different diameters (i.e., different V_{th}) can be used in one device [2]-[6]. Kim et al. proposed a static gate design methodology for ternary logic using the CNTFET with multi-threshold voltages [6]. These studies are more close to a theoretical approach because the nanoscale placement and alignment of CNTs with different diameters is not practically feasible. On the other hands, Karmakar et al. proposed quantum dot gate field effect transistors (QDGFETs) that produce three states by controlling the charge state of the quantum dots in the gate dielectric [7]-[9]. Even though this device is compatible with a top-down process, the scalability of device is limited by the diameter of quantum dot; further, the charging and discharging sequence limits the speed of the device operation.

Even with these progresses, replacing a binary logic with a ternary logic is a formidable challenge. Thus, a partial replacement for the noncritical circuit, which can be monolithically integrated with a binary backbone circuit, would be a more reasonable approach for MVL implementation. Thus, several MVL devices that can be fabricated with a low process temperature have been studied recently. Shim et al. demonstrated a ternary inverter using the graphene/WSe_2 heterojunction, which showed light-induced negative differential transconductance (NDR) characteristics [10]. Kim et al. demonstrated a complementary ternary logic device using graphene FET with npn and pnp channel profiles [11]. These devices showed the feasibility of the ternary logic device function with a low thermal budget integration process; however, their performances are not competitive to silicon devices yet. Hence, we suggest that the graphene barristor (GB) can be a promising candidate for MVL applications because of its low process temperature, high on-off ratio over 10^5, and reasonable device performance [12]-[16]. Furthermore, unlike many transition metal dichalcogenide (TMD) material based devices whose threshold voltage (V_{th}) is difficult to control, the V_{th} of the GB can be modulated by controlling the Schottky barrier height (SBH) [15], [16].

To provide the proof for this claim, we demonstrated n-type and p-type graphene barristors using a facile V_{th} control process, and developed a device model for a multi-threshold voltage graphene barristor (MTGB) using the experimental data. Subsequently, the performances of the ternary full adder (TFA) designed with MTGBs are compared with those of theoretical MVL devices using CNTFETs. The MTGB demonstrated power-delay product (PDP) of ~3.6×10^{-16} J, which is slightly higher than the ideal case using CNTFETs, but still very competitive.

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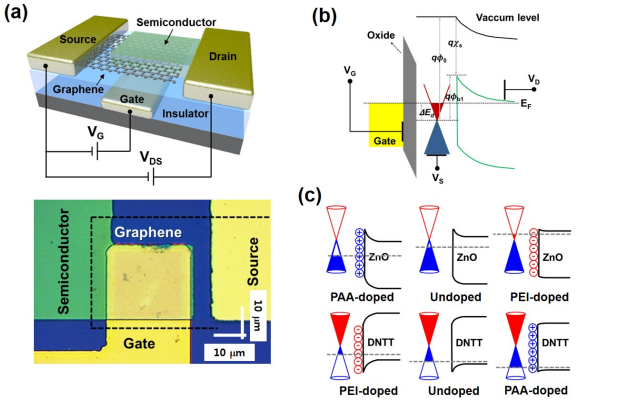

Fig. 1. (a) Schematic illustration of the graphene barristor and the optical image of the fabricated device. (b) Band diagram of gate metal/oxide/graphene/semiconductor vertical structure in the graphene barristor. (c) Band alignment between PAA or PEI doped graphene and semiconductor materials (ZnO and DNTT).

II. Experiments and Device Model

The schematic of the GB and the optical image of the fabricated device are shown in Fig. 1(a). The Schottky barrier height of the graphene /semiconductor junction is modulated by a buried gate, as shown in the band diagram in Fig. 1(b). The V_{th} of the GB can be controlled by modulating the Fermi level of graphene. The Fermi level of graphene is modulated by dipping the graphene channel in a polymer solution [17]-[19]. Here, 0.2 wt% poly-ethylene imine (PEI) was used for n-type doping [18], and 0.2 wt% polyacrylic acid (PAA) was used for p-type doping [19]. More details of the doping process can be found in reference [16]. An n-type semiconductor, ZnO, was deposited on the graphene using atomic layer deposition (ALD) and patterned to form an n-type GB. Similarly, dinaphtho [2,3-b:2',3'-f] thieno [3,2-b] thiophene (DNTT) was deposited using e-beam evaporation and the shadow mask process was used to form the p-type GB. The initial position of the Fermi level of graphene is modulated by the doping, as graphically shown in Fig. 1(c).

Fig. 2(a) and (b) shows the representative I_d–V_g and I_d–V_{ds} curves of the n-type graphene–ZnO barristor before and after the doping. The symbols represent the experimental data. In the graphene–ZnO barristor, both the n-type and p-type doping resulted in a consistent shift in the I–V curve according to the barrier height change. It is noteworthy that the barrier height changes affected both V_{th} and current level simultaneously. Meanwhile, for the graphene–DNTT barristor shown in Fig. 2(b), the range of current modulation was much smaller for the p-type doped because the Fermi level of graphene is typically in the hole branch and the doped Fermi level is shifted too close to the valence band edge.

Using these data, we have previously developed a device model for graphene barristor [20], [21]. The key parameters used for the device model includes the Fermi level of graphene ($q\phi_0$), the dopant-induced shift of the graphene Fermi level (ΔE_d), and the initial SBH ($q\phi_{b1}$), as shown in Fig. 1(b). The drive current of the graphene barristor is modeled using a modified diode equation:

$$I_{ds(p-type,n-type)} = \pm A_{eff} A^* T^2 \exp\left(\frac{-q\phi_b}{k_B T}\right)\left[\exp\left(\frac{\pm qV_{ds}}{\eta k_B T}\right) - 1\right] \quad (1)$$

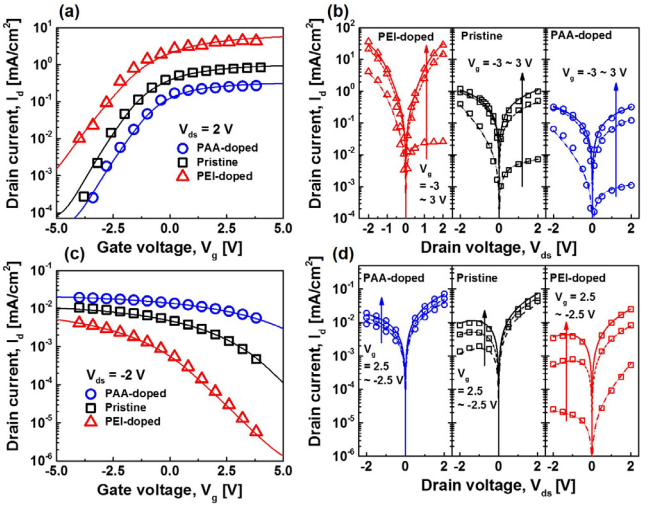

Fig. 2. Experiemental I_d–V_g, and I_d–V_{ds} characteristics of (a), (b) graphene/ZnO barristor and (c), (d) graphene/DNTT barristor with dopant molecules based the tuning of graphene Fermi level at a 10 nm Al_2O_3 gate dielectric and $|V_{ds}| = 2$ V. The solid line shows the simulated I_d–V_g curves using our semi-empirical barristor model.

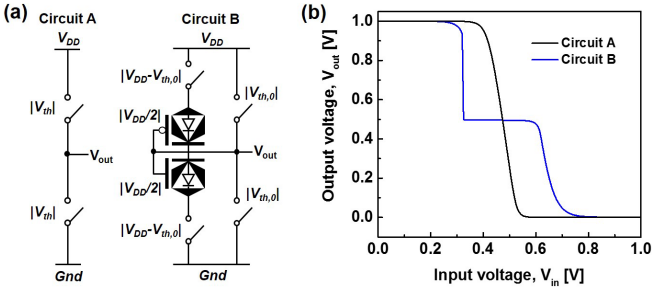

Fig. 3. (a) Switching-symbol-based stick diagram of complementary binary/ternary inverter circuit. Circuit A, and B are the binary and the ternary inverter without/with series diode connector, respectively. (b) Voltage transfer characteristics (VTC) of circuit A and B.

where A_{eff} is the effective area of the Schottky junction, A^* is the effective Richardson constant, q is the elementary charge, k_B is the Boltzmann constant, η is the ideal factor, and T is the temperature. At a given gate and drain bias, ϕ_b is determined by the charge conservation between the dielectric, graphene, and semiconductor.

$$Q_M + Q_{Graphene} + Q_S = 0 \quad (2)$$

where Q_M, $Q_{Graphene}$, and Q_S are the gate contact metal charge, the graphene layer charge of quantum capacitance containing the Dirac voltage shift ($|\Delta V_{Dirac}|=(1/\alpha\pi)(\Delta E_d/\hbar v_F)^2$), and the semiconductor charge, respectively [11], [22]. The solid lines in Fig. 2 are obtained using the Fermi level of graphene as a fitting parameter. From the best fitting result, the range of Fermi level modulation by the doping is found to be ~±130 meV (ΔE_d).

III. Ternary Full Adder Design

Using the theoretical device model, the ternary full adder (TFA) using the MTGB was designed to examine the feasibility of the GB as a ternary logic device. The multi-threshold-based basic ternary logic gate is designed with six GBs with three different V_{th} values, $|V_{th,0}|$, $|V_{DD}/2|$, and $|V_{DD}- V_{th,0}|$ [6]. Two different circuits shown in Fig. 3(a) and their voltage transfer characteristics (VTC) shown in Fig. 3(b) explain why six

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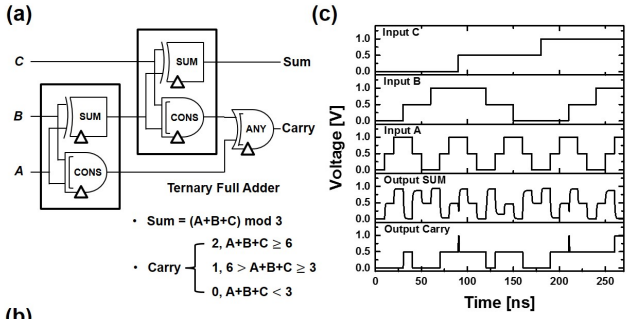

SUM	0	1	2
0	0	1	2
1	1	2	0
2	2	0	1

CONS	0	1	2
0	0	0	0
1	0	0	1
2	0	1	1

ANY	0	1	2
0	0	1	1
1	1	2	2
2	1	2	2

Fig. 4. (a) Gate-level schematic of the ternary full adder (TFA). (b) Ternary truth table of SUM, CONS, and ANY gates. (c) Transient responses of MTGB-based ternary full adder (TFA).

Table 1 Power and delay of various ternary and binary full adder (Monte-Carlo variation analysis)

		# of the device	Delay [ps] (±3σ)	Power [μW] (±3σ)	PDP [aJ] (±3σ)	
1 trit Ternary	CNTFET [23] (L = 100 nm)	110	181 (±50.1)	1.09 (±0.19)	199 (±67.8)	This work
	GB (L, W = 100 nm)	110	2250 (±201.6)	0.16 (±0.08)	360 (±180)	This work
		110	198 (±75.6)	0.15 (±0.05)	30.6 (±17.4)	Ideal
2 bits Binary	45 nm CMOS (PTM [24])	56	75.8 (±9.06)	0.74 (±0.22)	56.2 (±10.4)	This work

MTGBs are used to generate a stable ternary switch. The circuit A is a well-known binary inverter. Unlike the conventional inverter structure, circuit B consists of devices with $V_{th} = |V_{th,0}|$ for the pull-up/down network, and $V_{th} = |V_{DD}-V_{th,0}|$ to generating half V_{DD}. And two series-connected devices with $V_{th}=|V_{DD}/2|$ are used to make the stable noise immunity of a half V_{DD} using a negative feedback. Consequently, a stable ternary switch characteristic can be obtained.

Using circuit B as a unit ternary switch, a TFA is designed. For the design, MTGBs with three $|V_{th}|$ values (0.15 V, 0.5 V, and 0.85 V at V_{DD} = 1 V), 1-nm gate dielectric, and channel area of 10^{-2} μm^{-2}, were used to design a TFA consisting of SUM, CONS, and ANY gates [6], as shown in Fig. 4(a) and (b). The operation and performance of the TFA were verified using HSPICE contained Monte-Carlo variation analysis with the number of 100 iterations (standard deviation of V_{th} : 10 %), as shown in Fig. 4(c). To simulate the transient response of the TFA, V_{DD}, V_{SS}, and the transient time are set to 1 V, 0 V, and 0.1 *ns*, respectively. The voltage levels 1 V (V_{DD}), 0.5 V (half V_{DD}), and 0 V (V_{SS}) shown in Fig. 4 are equivalent to the logic values "2," "1," and "0," respectively. With three different input patterns (A, B, C), the SUM and Carry operations of the TFA are successfully verified. Because the parasitic components such as the internal resistance are not symmetrical owing to the differences in the n- and p-type GB devices and materials, a few glitches were generated from the timing difference of the input signals in the cascaded logic gates. Because this is the first demonstration of the MTGB-based ternary logic circuit, further optimization of the device characteristics can easily solve this problem.

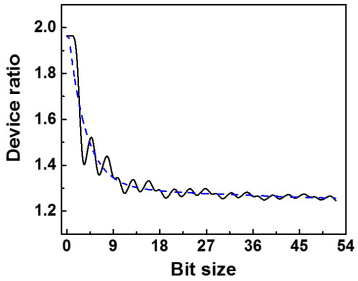

Fig. 5. Device ratio between binary and ternary full adder (TFA) as a function of bit size.

Moreover, the performance of the MTGB-based TFA is compared with CNTFET with different diameter (i.e., different V_{th}) based TFA, as shown in Table 1. For a fair comparison using the same circuit design, the energy efficiency of the TFA are simulated for two different devices: GB and CNTFET [2], [3], assuming the worst case delay and average power for all input patterns. The CNTFET showed better power consumption and shorter delay than the GB, primarily because the experimentally obtained parasitic resistance of the GB of ~50 kΩ was higher than ~1 kΩ of the CNTFET [20]. When the parasitic resistance is reduced to 1 kΩ, the delay in the MTGB-based TFA decreased to 200 ps, and the PDP was reduced to about ~10^{17}. Therefore, the more studies for GB optimization can further improve the PDP of the MTGB-based TFA.

The comparison between the ternary circuit and binary circuit is not straightforward. The PDP value of one trit MTGB-based TFA is similar to that of a two-bit binary full adder (BFA) designed with 45-nm silicon MOSFET technology, as shown in Table 1. However, the number of transistors used to design the MTGB-based TFA is approximately two times higher than that of the BFA because six devices were used for one ternary switch. The ratio of devices between ternary and binary rapidly decreases when the bit size increases. As shown in Fig. 5, the ratio converges to ~1.3. This result means that the area of the TFA can be 30% larger than the area of the BFA. Since the MTGB-based TFA can be fabricated on the backend of the line structure with a maximum temperature lower than 200 °C, the area penalty may not be a significant problem. Yet, the advantage of TFA in terms of device count and area will become more evident if a single device performing ternary switching function is developed because the device count will decrease to one sixth.

IV. Conclusion

We have demonstrated that the PDP of MTGB-based ternary full adder ~10^{-16} J is comparable to other ternary circuits as well as other binary full adders. Because the MTGB circuits can be implemented in the BEOL structure with a low thermal budget, the ternary logic circuit with MTGB devices is a reasonable option for monolithic three-dimensional integrated circuits.

REFERENCES

[1] T. Shibata and T. Ohmi, "A functional MOS transistor featuring gate-level weighted sum and threshold operations," *IEEE Trans. Electron Devices*, vol. 39, no. 6, pp. 1444–1455, Jun. 1992, DOI: 10.1109/16.137325.

[2] A. Raychowdhury and K. Roy, "Carbon-nanotube-based voltage-mode multiple-valued logic design," *IEEE Trans. Nanotechnol.*, vol. 4, no. 2, pp. 168–179, Mar. 2005, DOI: 10.1109/TNANO.2004.842068.

[3] P. Keshavarzian and R. Sarikhani, "A Novel CNTFET-based Ternary Full Adder," *Circuits Syst. Signal Process.*, vol. 33, no. 3, pp. 665–679, Mar. 2014, DOI: 10.1007/s00034-013-9672-6.

[4] M. H. Moaiyeri, R. F. Mirzaee, K. Navi, and O. Hashemipour, "Efficient CNTFET-based Ternary Full Adder Cells for Nanoelectronics," *Nano-Micro Lett.*, vol. 3, no. 1, pp. 43–50, Mar. 2011, DOI: 10.1007/BF03353650.

[5] S. Lin, Y. B. Kim, and F. Lombardi, "CNTFET-Based Design of Ternary Logic Gates and Arithmetic Circuits," *IEEE Trans. Nanotechnol.*, vol. 10, no. 2, pp. 217–225, Mar. 2011, DOI: 10.1109/TNANO.2009.2036845.

[6] S. Kim, T. Lim, and S. Kang, "An optimal gate design for the synthesis of ternary logic circuits," in *2018 23rd Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 476–481, Feb. 2018, DOI: 10.1109/ASPDAC.2018.8297369.

[7] S. Karmakar, J. A. Chandy, and F. C. Jain, "Design of Ternary Logic Combinational Circuits Based on Quantum Dot Gate FETs," *IEEE Trans. Very Large Scale Integr. VLSI Syst.*, vol. 21, no. 5, pp. 793–806, May. 2013, DOI: 10.1109/TVLSI.2012.2198248.

[8] F. C. Jain, E. Heller, S. Karmakar, and J. Chandy, "Device and circuit modeling using novel 3-state quantum dot gate FETs," in *2007 International Semiconductor Device Research Symposium*, 2007, pp. 1–2, DOI: 10.1109/ISDRS.2007.4422254.

[9] S. Karmakar, M. Gogna, E. Suarez, and F. C. Jain, "Three-state quantum dot gate field-effect transistor in silicon-on-insulator," *IET Circuits Devices Syst.*, vol. 9, no. 2, pp. 111–118, 2015, DOI: 10.1049/iet-cds.2014.0202.

[10] J. Shim, S.-H. Jo, M. Kim, Y. J. Song, J. Kim, and J.-H. Park, "Light-Triggered Ternary Device and Inverter Based on Heterojunction of van der Waals Materials," *ACS Nano*, vol. 11, no. 6, pp. 6319–6327, Jun. 2017, DOI: 10.1021/acsnano.7b02635.

[11] Y. J. Kim, S. Y. Kim, J. Noh, C. H. Shim, U. J. Jung, S. K. Lee, K. E. Chang, C. Cho, B. H. Lee, "Demonstration of Complementary Ternary Graphene Field-Effect Transistors," *Sci. Rep.*, vol. 6, p. 39353, Dec. 2016, DOI: 10.1038/SREP39353.

[12] H. J. Hwang, K. E. Chang, W. B. Yoo, C. H. Shim, S. K. Lee, J. H. S. Y. Kim, Y. S. Lee, C. Cho, and B. H. Lee, "A graphene barristor using nitrogen profile controlled ZnO Schottky contacts," *Nanoscale*, vol. 9, no. 7, pp. 2442–2448, 2017, DOI: 10.1039/c6nr08829e.

[13] M. G. Lemaitre, E. P. Donoghue, M. A. Mcarthy, B. Liu, S. Tongay, B. Gila, P. Kumar, R. K. Singh, B. R. Appleton, and A. G. Rinzler, "Improved Transfer of Graphene for Gated Schottky-Junction, Vertical, Organic, Field-Effect Transistors," *ACS Nano*, vol. 6, no. 10, pp. 9095–9102, Oct. 2012, DOI: 10.1021/nn303848k.

[14] H. Yang, J. Heo, S. Park, H. J. Song, D. H. Seo, K. E. Byun, P. Kim, I. Yoo, H. J. Chung, K. Kim, "Graphene Barristor, a Triode Device with a Gate-Controlled Schottky Barrier," *Science*, vol. 336, no. 6085, pp. 1140–1143, Jun. 2012, DOI: 10.1126/science.1220527.

[15] J. S. Kim, B. J. Kim, Y. J. Choi, M. H. Lee, M. S. Kang, and J. H. Cho, "An Organic Vertical Field-Effect Transistor with Underside-Doped Graphene Electrodes," *Adv. Mater.*, vol. 28, no. 24, pp. 4803–4810, Jun. 2016, DOI: 10.1002/adma.201505378.

[16] S. Y. Kim, J. W. Hwang, Y. J. Kim, H. J. Hwang, M. W. Son, N. Revannath, M. H. Han, K. J. Cho, and B. H. Lee, "Threshold voltage modulation of graphene-ZnO barristor using polymer doping process," Submitted to nanoscale.

[17] H. Liu, Y. Liu, and D. Zhu, "Chemical doping of graphene," *J. Mater. Chem.*, vol. 21, no. 10, pp. 3335–3345, 2011, DOI: 10.1039/C0JM02922J.

[18] I. Jo, Y. S. Kim, J. H. Moon, S. B. Park, J. S. Moon, W. B. Park, J. S. Lee, B. H. Hong, "Stable n-type doping of graphene via high-molecular-weight ethylene amines," *Phys. Chem. Chem. Phys.*, vol. 17, no. 44, pp. 29492–29495, 2015, DOI: 10.1039/C5CP03196F.

[19] M. Shimatani, S. Ogawa, D. Fujisawa, S. Okuda, Y. Kanai, T. Ono, and Z. Matsumoto, "Photocurrent enhancement of graphene phototransistors using p–n junction formed by conventional photolithography process," *Jpn. J. Appl. Phys.*, vol. 55, no. 11, p. 110307, Oct. 2016, DOI: 10.7567/JJAP.55.110307.

[20] S. Heo, Y. J. Kim, C. H. Kim, S. K. Lee, H. J. Lee, H. J. Hwang, J. Noh, B. H. Lee, "Graphene-ZnO:N Schottky junction based thin film transistor," in *2017 Silicon Nanoelectronics Workshop (SNW)*, pp. 131–132, 2017, DOI: 10.23919/SNW.2017.8242332.

[21] C. H. Shim, S. Heo, J. Noh, Y. J. Kim, S. Y. Kim, A. K. Khan, and B. H. Lee, "Design of Ratioless Ternary Inverter Using Graphene Barristor," in *2016 IEEE 46th International Symposium on Multiple-Valued Logic (ISMVL)*, 2016, pp. 23–30, DOI: 10.1109/ISMVL.2016.51.

[22] Y.-J. Yu, Y. Zhao, S. Ryu, L. E. Brus, K. S. Kim, and P. Kim, "Tuning the Graphene Work Function by Electric Field Effect," *Nano Lett.*, vol. 9, no. 10, pp. 3430–3434, Oct. 2009, DOI: 10.1021/nl901572a.

[23] Stanford University CNTFET Model website [Online]. Available: https://nano.stanford.edu/stanford-cnfet-model.

[24] Predictive Technology Model (PTM) website [Online]. Available: http://ptm.asu.edu/.