Analysis and Simulation of HV-CMOS Assemblies for the CLIC Vertex Detector

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Abstract. One of the design concepts currently under study for the vertex detector at the proposed Compact Linear Collider is a High-Voltage CMOS sensor, fabricated in a commercial 180 nm technology, capacitively coupled to a hybrid readout chip. Tests of the assemblies were carried out at the CERN SPS using 120 GeV/c pions, covering incident angles ranging from 0° to 80°. The measurements have shown an excellent tracking performance with an efficiency above 99.7 % and a spatial resolution of 5 µm to 7 µm over the tested angular range. These results were then compared to TCAD simulations carried out using simulations, showing a good agreement for the current-voltage, breakdown and charge collection properties. The simulations have also been used to optimise future sensor design.

Keywords: CLIC, vertex detector, HV-CMOS, capacitively coupled pixel detectors, testbeam, simulation, TCAD

1 Introduction

The Compact Linear Collider (CLIC) [1] is a proposed electron-positron collider at CERN with centre of mass energies up to 3 TeV [2]. The physics programme for CLIC includes measurements of the properties of the Higgs boson and the top-quark, as well as direct and indirect searches for physics beyond the standard model. The clean environment of an e^+e^- collider allows the physics programme to be studied with a high precision but limitations arise from the rate and timing of the beam as well as beam induced backgrounds. Taking the physics and environmental conditions into account, stringent requirements are set for the vertex detector design. These are: a 3 µm point resolution, in order to accurately reconstruct secondary vertices to achieve b- and c- flavour tagging; a low material budget of $0.2\,\% \, X_0$ per layer, to minimise scattering resulting in the need for thin sensors and cooling to be carried out by forced air flow; a low power consumption of below $50\,\mathrm{mW\,cm^{-2}}$, enabling air cooling and achievable by power pulsing of the front-end electronics; a time stamping of 10 ns to reduce backgrounds, giving the need for fast signal generation and processing; and trigger-less readout with data transfer in 20 ms gaps between consecutive bunch trains.

High-Voltage CMOS (HV-CMOS) sensors capacitively coupled to the readout electronics [3] are one of the proposals for the vertex detector technology. To gauge the validity of such devices for the CLIC vertex detector, prototypes have been produced and initial tests have been performed [4].

The HV-CMOS sensor embeds the pixel circuitry inside a deep n-well to isolate it from the substrate. This shielding allows a high bias voltage to be applied to the p-type substrate resulting in a large depletion region. The deep n-well also acts as the collection diode for the sensor. A dedicated HV-CMOS chip was created for CLIC, the CCPDv3, for use as a capacitively coupled sensor. It consists of a 64x64 pixel matrix with a pitch of 25 µm and a two-stage amplifier in each pixel which is required to avoid bump bonding. Instead the sensor is capacitively coupled to the readout ASIC, whose pixel footprint matches that of the CCPDv3, via a thin glue layer of around a few microns thick. The readout chip is the CLICpix which contains both a 4-bit time over threshold (ToT) counter and a 4-bit time of arrival (ToA) counter. Beam tests of such assemblies have been carried out at the CERN SPS with 120 GeV/c pions, covering incident angles ranging from 0° to 80°, results of which are described in Sec. 2. To better understand features of the measurements, simulations have been carried out and compared to the results from the testbeam, see Sec. 3. These simulations have also been used to improve future sensor design.

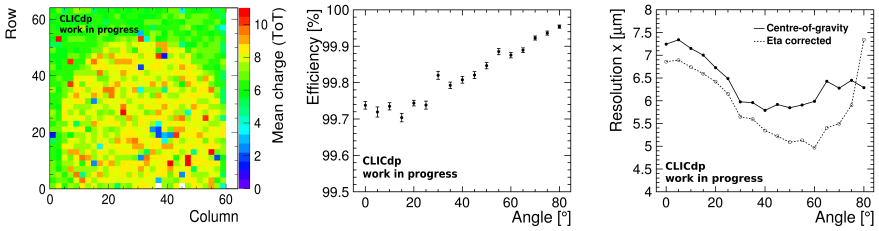
2 Performance Measurements

To gauge the performance of the assemblies, testbeam measurements have been carried out. At a perpendicular incidence (0°), the mean charge, in ToT, shows some non-uniformity across the chip, with a disc of higher ToT around the centre, as shown in Fig. 1a. This arises from a stronger capacitive coupling in this region due to the limited extent in which the glue spot spreads across the assembly. This is an artefact of the glueing process and is not seen in all assemblies. The efficiency of the whole assembly is very high reaching values above 99.7 % of the considered angular range, as shown in Fig. 1b.

Due to charge sharing, there are larger clusters at higher angles, Fig. 2c, resulting in a better spatial resolution, as shown in Fig. 1c. The best resolution obtained is worse than that required for CLIC. It can be improved for multi-pixel clusters by applying the so called eta correction, correcting the centre of gravity position for effects of the non-linear charge sharing between pixels. In this case the best resolution obtained is around 5 µm. The largest impact on the resolution comes from the small cluster sizes which are due to the limited charge diffusion in the sensor.

3 TCAD Simulations

In order to interpret the results, simulations were used to replicate the measurements and to gauge the prospects for improved performance. The simulation package used in this study was TCAD [6]. Using the design file (gds) of the



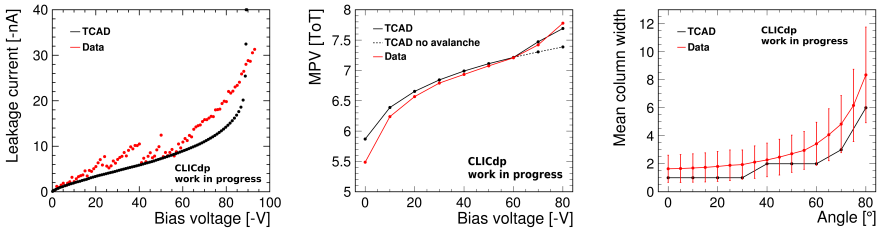
(a) (b) (c)

Fig. 1: (a) The mean charge, in ToT, per pixel averaged over a 4x4 square. (b) Single hit efficiency of the DUT at different angles. (c) x-resolution at different angles, found by fitting the global x residual for all clusters with a Gaussian [7].

chip, a simplified pixel structure was produced in TCAD [5]. This was done by extracting the relevant implant layers and using these to create masks for the simulations. From this a 2D structure was then implemented with a thickness of 250 µm.

From the current-voltage characteristics, Fig. 2a, it can be seen that both the leakage current and breakdown voltage are reproduced well in the simulations, with breakdown occurring at −93 V for data and −88 V for simulation. The source of the breakdown was found in the simulations to be a thin channel, through which current can flow, forming at the surface of the silicon, allowing the HV contact to short the deep n-well. To compare the TCAD charge collection to data, measurements with a radioactive source of known energy were used. The response of the amplifier on the HV-CMOS side was compared to the response of the injected charge on the CLICpix side, producing a curve which was parameterised and used to convert the TCAD output to ToT. A bias scan at perpendicular incidence shows that the simulations match well with data, even replicating the increase in gradient seen at −70 V and −80 V due to avalanche multiplication, shown in Fig. 2b. Angular data is also replicated well as shown, in Fig. 2c, by the mean column width as a function of angle, which agrees within the uncertainty of the measurement. While all the TCAD simulations and data agree within 10 %, small discrepancies arise due to several effects, in particular: no Landau deposition of charge is considered in the simulations, pixel-to-pixel variations in the calibration and the limitations of a 2D simulation when comparing to 3D data.

One possible way to improve the performance would be to use a higher resistivity substrate, producing a larger electric field and depletion region. Another way would be to bias from the backside by implantation of a p+ implant. Comparing the simulated performance of the topside to the backside biasing, there is no difference in depletion depth at 10 Ω cm but as resistivity increases so does the difference; at 1 kΩ cm the depth is 25 µm for topside and 79 µm for backside. Higher resistivities also produce: larger breakdown voltages, resulting in higher operating biases; a smaller deep n-well to bulk capacitance, resulting in less noise; and a larger and faster charge collection, resulting in an improved



(a) (b) (c)

Fig. 2: Three plots comparing data to TCAD showing: (a) the current as a function of bias voltage, (b) the most probable value of the ToT distribution for single pixel clusters as a function of bias voltage and (c) the mean column width as a function of angle [7].

timing performance. However, for the final sensor at a thickness of 50 µm, if the bulk is fully depleted the only collection method will be drift hence the signal will be fast but there will be less charge diffusion. This means there may be a trade off between timing and spatial resolution in the final sensor.

4 Summary

Measurements of HV-CMOS assemblies for the CLIC vertex detector have shown excellent tracking efficiency and spatial resolution across the full detector acceptance, although the CLIC target resolution of 3 µm has still not been met. TCAD simulations have been used to simulate the sensor properties and the results compare well to measurements. The simulations have also shown that using a higher substrate resistivity should lead to larger breakdown voltages, a smaller capacitance and faster charge collection. Even greater improvements are expected for backside biasing in the current-voltage and capacitance-voltage characteristics as well as producing larger depletion regions.

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