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Challenges and Progress on Carbon Nanotube Integration for BEOL Interconnects

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Abstract— Here, we review and present current challenges and progress on Carbon Nanotube Integration for BEOL Interconnects as well as our recent results. Amongst all the research on carbon nanotube interconnects, those discussed here cover 1) improvement of the variability of SWCNTs for local interconnects 2) process & growth of carbon nanotube interconnects compatible with BEOL integration and formation of CNT-copper-composites, 3) modeling and simulation from atomistic to circuit-level benchmarking and performance prediction, and 4) characterization and electrical measurements. The aim is to evaluate the use of CNT-based materials for future metallization, both in regards to manufacturability, i.e. CMOS compatibility and wafer-scale integration as well as realistic performance expectations, i.e. variability and defectivity.

I. INTRODUCTION

Carbon nanotubes (CNTs) have sparked a lot of interest in their applicability as future VLSI interconnects because of their extremely desirable properties of high mechanical and thermal stability, high thermal conductivity and large current carrying capacity [1] [2] [3]. Due to strong sp² bonding between carbon atoms, CNTs are much less susceptible to electromigration (EM) problems than copper interconnects and can carry high current densities [1]. Ballistic electronic transport can go over long nanotube lengths (> 1 μm), enabling CNTs to carry very high currents with virtually no heating due to nearly 1D electronic structure. Metallic single-walled CNT bundles have been shown to be able to carry extremely high current densities of the order of 10⁹ A/cm² [4]. In contrast, EM limits the current carrying capacity of Cu interconnects to 10⁶ A/cm² [5]. Copper interconnects with a cross-section of 100 nm x 50 nm can carry currents up to 50 μA, whereas a 1 nm diameter CNT can carry up to 20-25 μA current [6]. Hence, from a reliability perspective, a few CNTs are enough to match the current carrying capacity of a typical Cu interconnect. In this paper, we overview the recent advancements of carbon nanotubes as interconnect material for nanoelectronics.

II. CNT GROWTH & PROCESS

Using CNTs as interconnect material in semiconductor manufacturing is a huge paradigm shift. For this, a lot of challenges have to be addressed. We need reliable and reproducible integration approaches for manufacturing, more importantly CMOS compatibility has to be targeted, both in terms of materials and process temperature. Additionally, defectivity of CNTs has to be under control for performance and variability reasons and contacting the CNTs reliably is an

issue as well [7]. To target different requirements, two approaches have been the subject of research and are presented in this paper. First, local interconnects are to be replaced by single CNTs modified by doping to tackle variability and increase conductivity. Second, global interconnects of composite Cu-CNT material is studied to improve ampacity and help with integration. Fig. 1 illustrates this as a demonstrator scheme.

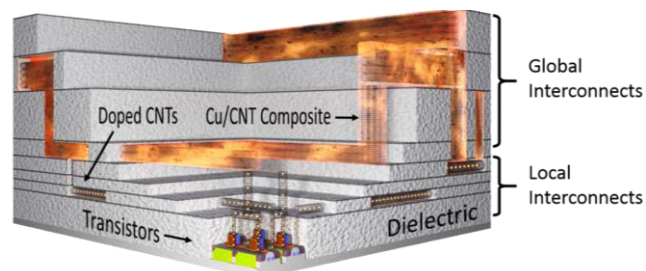


Figure 1: Schematic of using doped CNTs for local interconnects and CNT-Cu-composite material for global interconnects.

Doped CNTs as local interconnects

The parallel fabrication of single CNT horizontal interconnects with controlled placement was achieved by catalytic chemical vapor deposition (CVD) of CNT on catalyst nanoparticle localized in pre-patterned nanometric via holes. Single MWCNTs with 4 or 5 walls and diameter around 7.5 nm were synthesized from a 1 nm thick catalyst film deposited at the bottom of a 30 nm via hole (Fe catalyst on aluminosilicate support). CNTs were then aligned on the sample surface before patterning of Pd/Au electrodes to electrically contact the CNTs. Electrical measurements were performed to extract the line resistance vs line length dependence. External doping of the CNT lines by PtCl₄ solution was applied to tackle variability and defectivity problems, the results can be seen in Figure 2. High resolution TEM measurements were performed to check the Pt concentration inside the individual CNTs, see Figure 3.

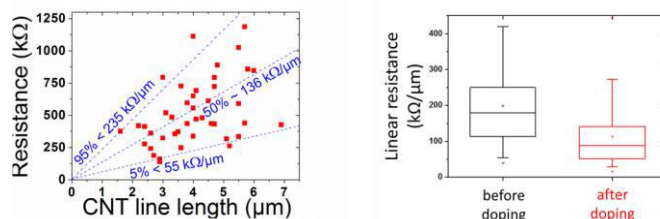


Figure 2: Variability of CNT line resistance vs line length and improvement by doping with Pt.

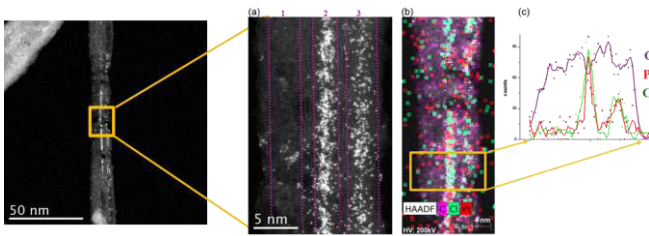


Figure 3: HRTEM measurements and elemental analysis of Pt concentration inside CNTs.

CMOS compatible CNT growth

To ensure compatibility with state of the art semiconductor manufacturing process flows, the growth of CNTs has to be adapted in terms of catalyst material and process temperature. For this we developed a catalyst based on cobalt (Co), which is a material commonly used in CMOS BEOL flows. Additionally, the CNT growth temperature has to be lowered to < 400 °C. Several experiments were done at Aixtron and the resulting CNT layers were characterized by SEM and Raman spectroscopy. First results indicate that good CNT growth on Co catalyst at lower temperatures is possible, enabling future integration paths (see Figure 4).

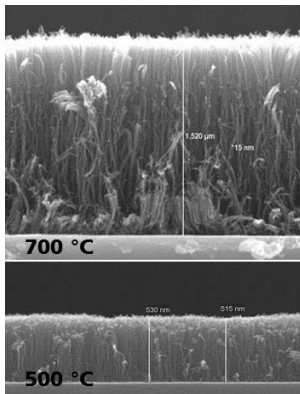


Figure 4: SEM results of CNTs grown with Co catalyst at different temperatures.

To be an actual alternative for leading edge semiconductor manufacturing, CNT integration has to be scaled up from a lab to a fab scale. This means reliable processes on 300 mm wafer size have to be demonstrated. This could be shown with a good starting uniformity and full 300 mm wafer CNT-growth.

Cu-CNT composite formation

To embed CNTs in a copper matrix presents several advantages. Void-free filling, CMP or patterning becomes possible, variability can be decreased and an efficient trade-off between resistivity and ampacity can be realized. Using galvanic electrodeposition several approaches of impregnating bundles of CNTs with copper were investigated.

In principal there are two ways, electroless deposition (ELD) [9] [10] [11] [12] and electrochemical deposition (ECD) [13]. The former needs lower technical effort, but often involves a multitude of chemicals. While the latter, ECD, is more common, has a lot of control knobs but needs a conductive substrate. Both methods were extensively investigated for both, vertically (VA) and horizontally aligned (HA) MW-CNTs. Figure 5 shows cross-section SEM views of HACNTs after successful ELD and ECD copper impregnation. Near

void-less fill could be achieved. Further process improvements need to work on copper overfill and selectivity.

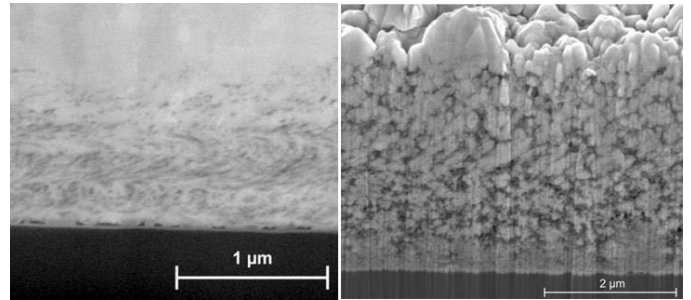


Figure 5: SEM results of HACNTs filled with Cu via ECD (left) and ELD (right).

III. ATOMISTIC TO CIRCUIT-LEVEL MODELLING

First, we performed the Density Functional Theory (DFT) calculations to provide the physical properties of CNT interconnects such as the ballistic conductivity of CNTs and the contact resistance between CNTs and relevant metals for the circuit-level simulations. The mean free path approximation is adopted to describe the phonon scattering effects in CNT interconnects. Using DFT results, a finite-difference approach was adopted to solve the Laplace equations for macroscopic resistance and capacitance (RC) extraction in complex interconnect structures: $\Delta\epsilon\Delta\psi = 0$ for an insulator and $\Delta\kappa\Delta\psi = 0$ for a metal, where ϵ , κ , and ψ are permittivity, conductivity, and potential, respectively.

Figure 6 shows the 3D TCAD simulation output for a 14nm CMOS inverter highlighting the cross-talk between lines up to the M2 interconnect level. Advanced models for conductivity and capacitance of both Cu and CNT were implemented using ab-initio results. Extracted RC netlists can be provided in a SPICE-like format for circuit-level simulation.

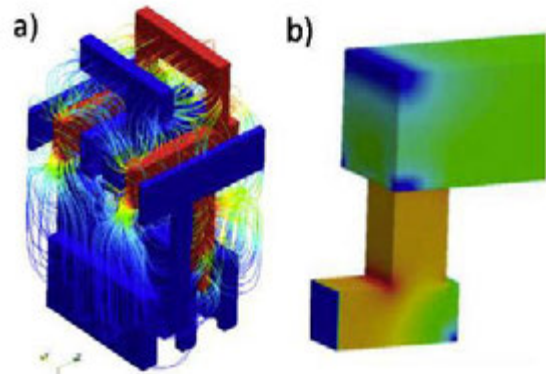


Figure 6:(a) 3D TCAD capacitance, where the electric field streamlines highlight the cross-talk between interconnects. (b) Resistance simulation detail, where the current density flow highlights the interconnect hot-spots.

IV. CHARACTERIZATION & MEASUREMENTS

The resistance of a CNT line always consists of two parts, the contact resistance and the resistance of the CNT itself. For obtaining the contact resistance and CNT resistance per unit length, the transmission line measurement technique can be used [14]. MWCNTs of different lengths were contacted and the resistance of the resulting structure was measured. By correlating line length with total resistance, contact resistance

and CNT resistance per unit length can be extracted. A major advantage of CNT interconnects is their high thermal conductivity, which holds the potential to alleviate thermal design constraints in advanced integrated circuits. To fully benefit from this advantage, a good understanding of their thermal properties is needed. Because MWCNTs have diameters in the order of 10 nm, only a few techniques for thermal conductivity and self-heating studies can be considered [15]. Scanning thermal microscopy with resistively heated probes holds the potential to perform temperature mapping of MWCNT interconnects under operation, hence we can study their self-heating and extract thermal conductivity data [16]. Figure 7 shows a combined temperature and topography image of a nanowire sample as measured using scanning thermal microscopy. The nanowire was located on a dielectric substrate and contacted with metal electrodes on the left and right of the image. Local heating at the metal contacts and at a defective region in the center of the wire was resolved. Using this technique, typically a resolution of below 10 nm is obtained.

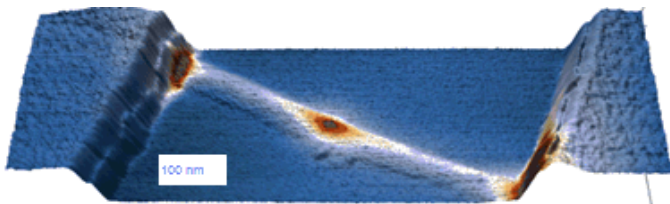


Figure 7: Temperature and topography image of a self-heated nanowire. The hot-spots at the contacts and around a defect region are clearly visible. From the temperature distribution one can also conclude back on thermal conductivity [15].

V. CONCLUSION

Carbon nanotubes present viable solutions to overcome the upcoming challenges with copper interconnect technology, nevertheless, many issues still remain. On the processing side, continued efforts are needed on the CVD growth of CNTs not only to produce high-quality CNTs at a reasonable temperature, but also to reduce the CNT tortuosity and increase their packing density in interconnects. For BEOL fabrication processes, challenges arise from high planarity CMP processes, temperature budget (i.e. 400 °C) and contamination management. Stable doping of CNTs at the operating temperature of circuits still needs to be developed and integrated into BEOL processing. The fabrication of aligned CNT-Cu composite material requires specific developments, and the corresponding electrical conduction mechanism needs to be carefully studied. On characterization, there is a need for structural and morphological CNT-level electrical and thermal characterization. Research efforts related to physical modeling, physical design, design space exploration, CNT processing and characterization are gaining momentum and will provide a clearer picture of the costs and benefits of integrating CNTs as on-chip interconnects. With respect to modeling, electro-thermal modeling and simulation tools are needed to evaluate the performance, reliability and variability of CNTs and composite Cu-CNT interconnects. It can also help to assess the impact of CNT-metal contacts. In this context, a multi-scale physics-based simulation platform (from ab-initio material simulation to circuit-level) that

considers all aspects of VLSI interconnects (i.e. performance, power, and reliability) is desirable to explore and evaluate the potential of CNT technology. In summary, there are a lot of research efforts ongoing and also required from the community into enabling CNTs for BEOL interconnects.

VI. ACKNOWLEDGEMENTS

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