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Random Discrete Dopant Induced Variability in Negative Capacitance Transistors

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***Abstract*—In this work we investigate the impact of random discrete dopants (RDD) induced statistical variability in ferroelectric negative capacitance field effect transistors (NCFETs). We couple the 3D 'atomistic' statistical device simulator GARAND with the Landau - Khalatnikov equation of the ferroelectric for this study. We find that the negative capacitance effect provided by the ferroelectric layer can lead to suppression of the RDD induced variability in the threshold voltage (V_t), OFF-current (I_{OFF}), and ON-current (I_{ON}). This immunity to RDD induced variability is found to increase with increase in the ferroelectric thickness.**

Keywords*—Negative capacitance, MOSFET, Ferroelectric, statistical variability, Random Discrete Dopants

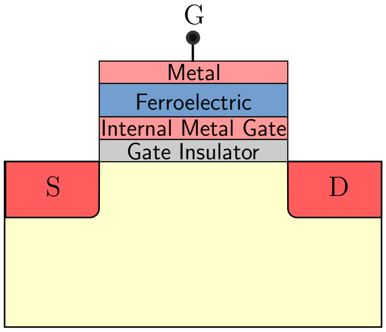


Fig. 1. Cross-sectional schematic of an NCFET. The ferroelectric is sandwiched between the internal and external metal gates.

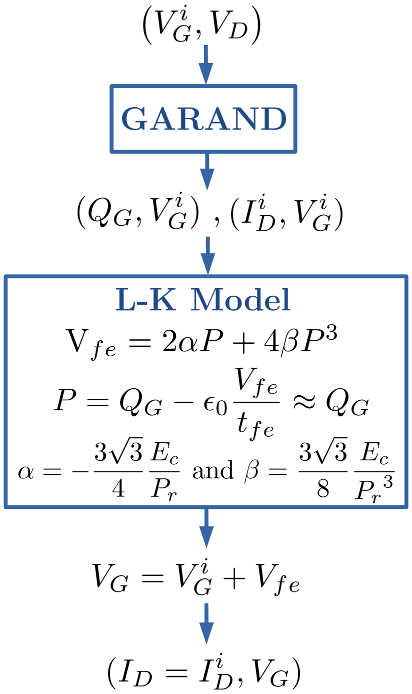


Fig. 2. NCFET simulation flow: V_G^i is the internal gate voltage, V_{fe} is the voltage drop across the ferroelectric, P is the polarization, Q_G is the gate charge density, α and β are the ferroelectric parameters which can be expressed in terms of the coercive field, E_c and remnant polarization, P_r. t_{fe} is the ferroelectric thickness. I_D and V_G denote the drain current and post-processed gate voltage for the NCFET.

I. INTRODUCTION

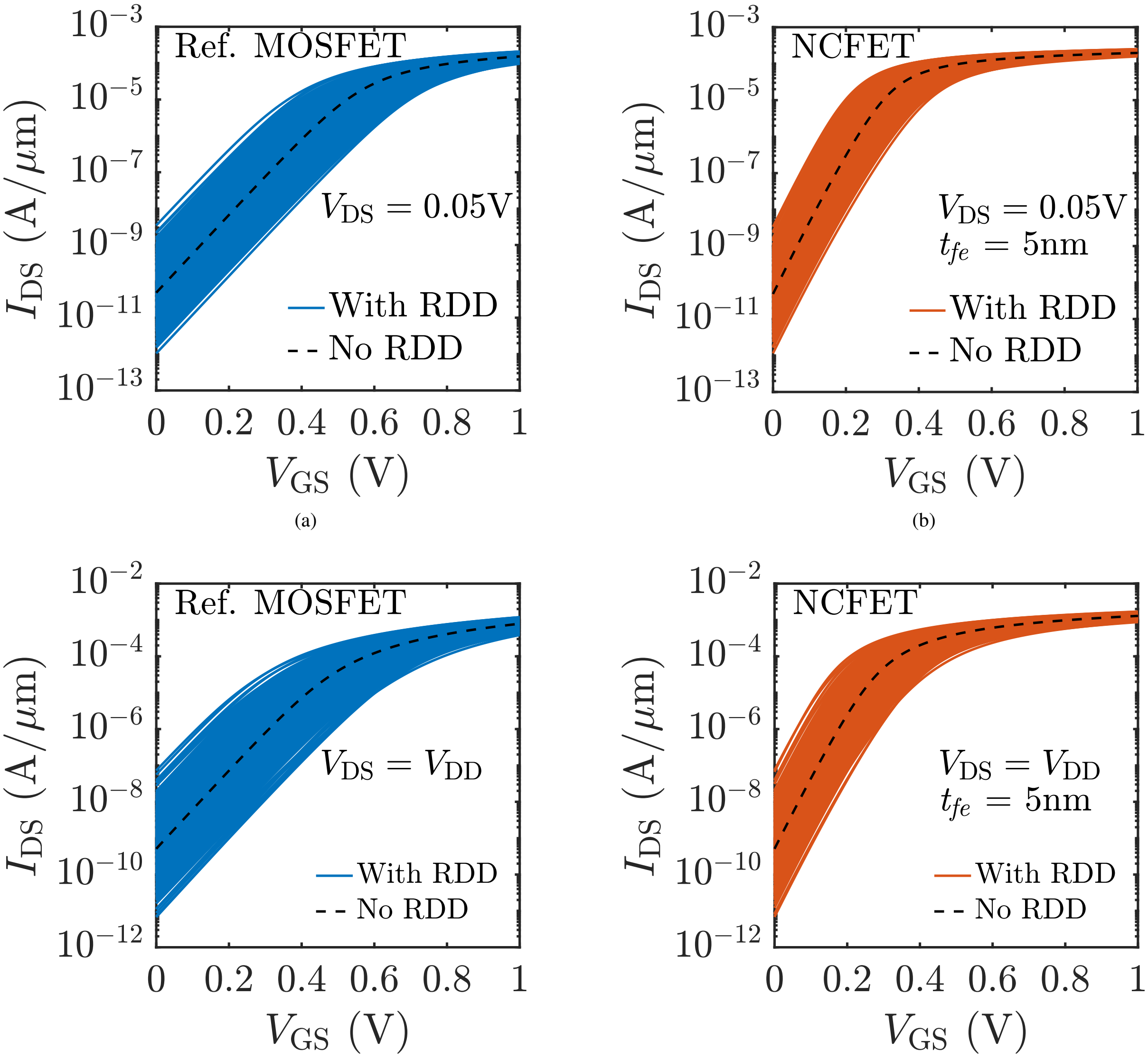
NCFETs are constructed by introducing into the gate stack a layer of a ferroelectric material that acts as a conditionally negative capacitor. Such devices have been demonstrated to achieve a sub-60 mV/dec subthreshold swing [1], [2] and consequently they are being pursued as a means to scale down supply voltage without loss of performance [3], [4].

Variability induced due to intrinsic statistical nature of random discrete dopants in the semiconductor channel of MOSFETs has been an important source of variability, and its role in limiting the performance of existing CMOS technologies has been well studied [5], [6]. In this work we compare the impact of RDD in conventional MOSFETs and ferroelectric based negative capacitance transistors combining 3D TCAD with the steady state Landau - Khalatnikov (L-K) model of ferroelectrics.

II. SIMULATION METHODOLOGY

We examine bulk NCFETs with the MFMIS (Metal–Ferroelectric–Metal–Insulator–Semiconductor) structure which essentially consist of a conventional MOSFET with a ferroelectric layer in between the gate of the conventional MOSFET and an external metal gate as shown in Fig. 1.

We use the 3-D device simulator GARAND [7] to obtain the charge-voltge and current-voltage characteristics of the reference MOS transistor. We then calculate the potential drop across the ferroelectric using the steady-state Landau-Khalatnikov equation [8], [9]. Finally we map the internal gate bias to the actual (external) gate bias using voltage balance, thus obtaining the terminal characteristics of the NCFET. The simulation flow and assumptions therein have been illustrated in Fig. 2. We have performed 1000 simulations



(a) (b)

(c) (d)

Fig. 3. $I_{\mathrm{DS}} - V_{\mathrm{GS}}$ curves for the reference MOSFET and NCFET (t_{fe} = 5 nm) obtained from statistical simulation (solid lines) and continuous doping profiles with no RDD (dashed lines). (a) - (b): at V_{DS} = 0.05V. (c) - (d): at V_{DS} = V_{DD}. The nominal NCFET curves are shifted to have the same I_{OFF} as the reference MOSFET, and the same amount of shift is applied to the statistical data for NCFETs.

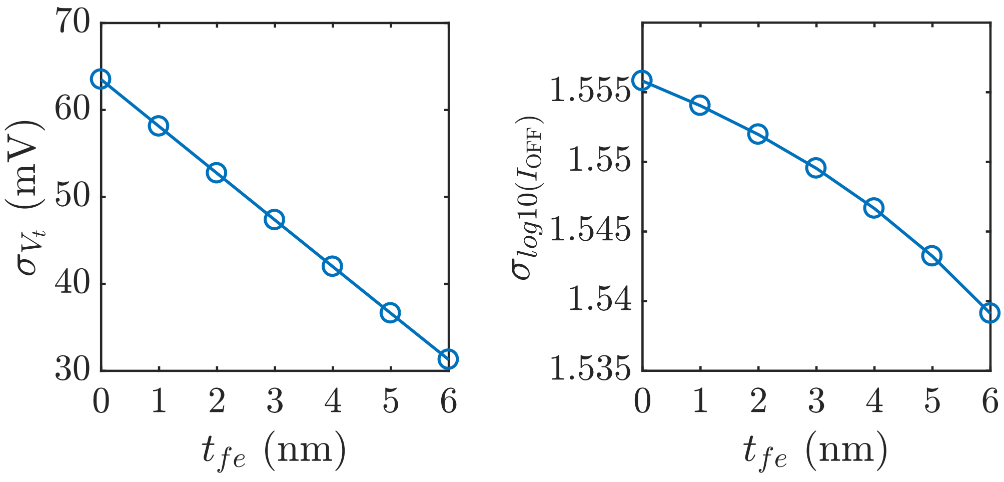
each with a random distribution of dopants and one simulation assuming continuous doping without any dopant fluctuation. Drift-diffusion transport model with density gradient quantum correction is employed in the simulations. We have not included the tunneling leakage mechanisms in this study.

We use a CMOS process compatible metal doped HfO_2 ferroelectric having a coercive field, E_c = 1 MV/cm and remnant polarization, P_r = 5 μC/cm^2 [10]. We have set each nominal NCFET device to be hysteresis-free (this limits the maximum t_{fe} to ~7nm). The operation of NCFETs based on capacitance matching, their typical characteristics and dependence on ferroelectric thickness and matarial parameters have been described elsewhere (e.g. see [8], [9], [11], [12]) and will not be discussed here. Also, note that the variability in the ferroelectric layer itself is not considered here, as the focus is to isolate the impact of the NC effect on RDD induced variability.

III. RESULTS AND DISCUSSION

For a reasonable comparison, the OFF-current of the RDD-free nominal NC device (assuming continuous doping) at each t_{fe} is set to that of the reference MOSFET. The $I_{\mathrm{DS}} - V_{\mathrm{GS}}$ curves of the reference MOSFETs and NCFETs with atomistic RDD are evaluated including the same offset. Fig. 3 shows the transfer characteristics of the reference MOSFETs and NCFETs (with t_{fe} = 5nm) at low and high drain biases. The improvement in the subthreshold slope and the ON-current are evident as is typical with NCFETs.

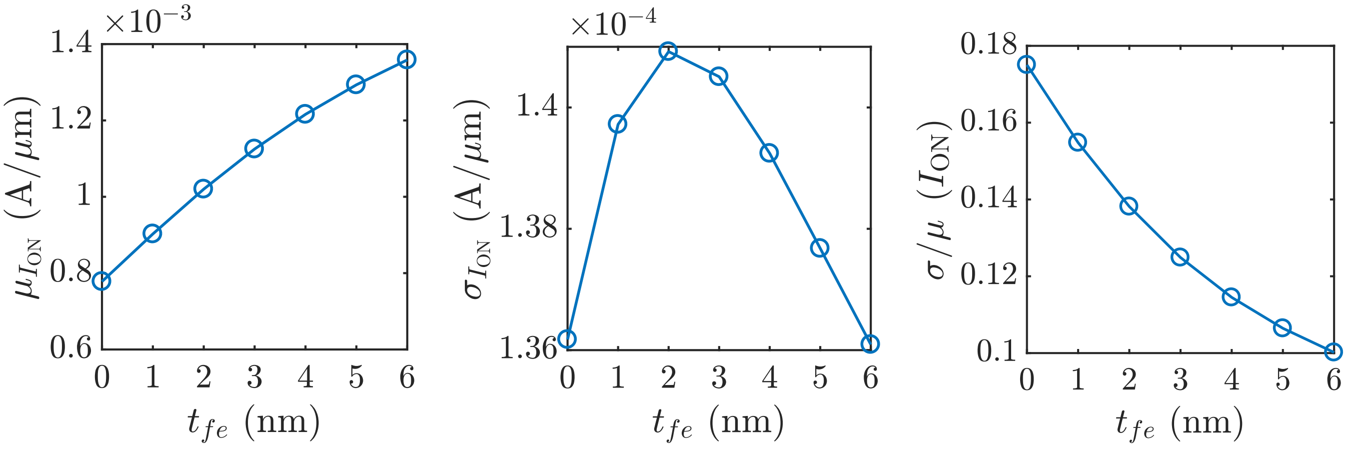
We examine the impact of RDD on the variability in the main device figures of merit V_t, I_{OFF}, and I_{ON} as a function of the ferroelectric thickness. σ_{V_t} linearly reduces



(a)

(b)

Fig. 4. Reduced (a) V_t, and (b) I_{OFF} variability in NCFETs with t_{fe}.

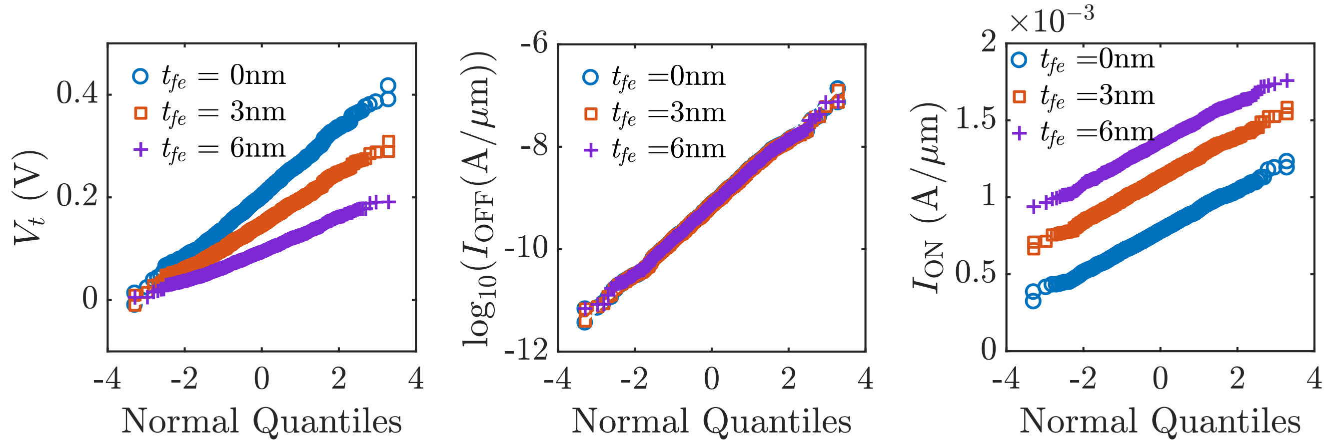


(a)

(b)

(c)

Fig. 5. Variation of (a) Mean, (b) standard deviation, and (c) relative standard deviation (σ/μ) of I_{ON} with t_{fe}.



(a)

(b)

(c)

Fig. 6. Q-Q plots for (a) V_t, (b) I_{OFF} and (c) I_{ON} for the reference MOSFET (t_{fe} = 0 nm), and NCFETs with t_{fe} = 3 nm and 6 nm.

with increased ferroelectric thickness, as shown in Fig. 4(a). NCFETs with ferroelectric thickness of 6 nm show more than 50% reduction in V_t variability. As the OFF-current follows a log-normal distribution, we calculate the standard deviation of the logarithm of the OFF-current, $\sigma log_{10}(I_{\mathrm{OFF}})$. We find that it is not affected much by t_{fe} and shows slight reduction with increasing t_{fe} (Fig. 4(b)).

Fig. 5(a) shows the increase in I_{ON} with t_{fe} on account of better capacitance matching and higher internal voltage amplification. But the standard deviation of the ON-current, $\sigma_{I_{\mathrm{ON}}}$ shows a non-monotonic behavior with increase in t_{fe}. As I_{ON} in NCFETs is significantly higher than the reference bulk MOSFET, instead of comparing the absolute standard deviations, it is more insightful to compare the relative standard deviation (σ/μ). It is clearly seen to improve with increased t_{fe}.

Quantile-quantile plots for these figures of merit which corroborate these observations are shown in Fig. 6 for the reference device and NCFETs with different ferroelectric thicknesses. Threshold voltage, logarithm of the OFF-current, and the ON-current distributions remain Gaussian in nature in the NCFETs. Similar results were reported in a recent study on geometrical process variations in negative capacitance based FinFETs using a compact modeling approach [13].

IV. CONCLUSION

We have shown that the negative capacitance effect of the ferroelectric in an NCFET can result in higher immunity to statistical variability induced by random discrete dopants in the transistor channel. In particular, NCFETs show reduced RDD induced V_t and I_{OFF} variability with the immunity increasing with increase in the ferroelectric thickness. For the ON-state current, although the absolute variability is not a monotonic function of the ferroelectric thickness, the variability relative to the mean value is suppressed with increase in the ferroelectric thickness.

V. ACKNOWLEDGMENT

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REFERENCES

[1] K.-S. Li, P.-G. Chen, T.-Y. Lai, C.-H. Lin, C.-C. Cheng, C.-C. Chen, Y.-J. Wei, Y.-F. Hou, M.-H. Liao, M.-H. Lee, M.-C. Chen, J.-M. Sheih, W.-K. Yeh, F.-L. Yang, S. Salahuddin, and C. Hu, "Sub-60mV-swing negative-capacitance FinFET without hysteresis," in *IEEE International Electron Devices Meeting (IEDM)*, Dec 2015, pp. 22.6.1–22.6.4.

[2] H. Lee, P.-G. Chen, S.-T. Fan, Y.-C. Chou, C.-Y. Kuo, C.-H. Tang, H.-H. Chen, S.-S. Gu, R.-C. Hong, Z.-Y. Wang, S.-Y. Chen, C.-Y. Liao, K.-T. Chen, S. T. Chang, M.-H. Liao, K.-S. Li, and C. W. Liu, "Ferroelectric Al:HfO2 negative capacitance FETs," in *IEEE International Electron Devices Meeting (IEDM)*, 2017.

[3] T. Dutta, G. Pahwa, A. R. Trivedi, S. Sinha, A. Agarwal, and Y. S. Chauhan, "Performance evaluation of 7-nm node negative capacitance FinFET-based SRAM," *IEEE Electron Device Letters*, vol. 38, no. 8, pp. 1161–1164, Aug 2017.

[4] Z. Krivokapic, U. Rana, R. Galatage, A. Razavieh, A. Aziz, J.Liu, J.Shi, H. Kim, R. Sporer, C. Serrao, A.Busquet, P. Polakowski, J. Müller, W. Kleemeier, A. Jacob, D. Brown, A. Knorr, R. Carter, and S. Banna, "14nm ferroelectric FinFET technology with steep subthreshold slope for ultra low power applications," in *IEEE International Electron Devices Meeting (IEDM)*, 2017.

[5] A. Asenov, "Random Dopant Induced Threshold Voltage Lowering and Fluctuations in Sub-0.1 μm MOSFET's: A 3-D "Atomistic" Simulation Study," *IEEE Trans. Electron Devices*, vol. 45, no. 12, pp. 2505–2513, Dec 1998.

[6] A. Asenov, G. Slavcheva, A. R. Brown, J. H. Davies, and S. Saini, "Increase in the random dopant induced threshold fluctuations and lowering in sub-100 nm MOSFETs due to quantum effects: a 3-D density-gradient simulation study," *IEEE Transactions on Electron Devices*, vol. 48, no. 4, pp. 722–729, Apr 2001.

[7] "GARAND Statistical 3D TCAD Simulator," *Synopsys, Inc. Mountain view, CA, USA*.

[8] G. Pahwa, T. Dutta, A. Agarwal, S. Khandelwal, S. Salahuddin, C. Hu, and Y. S. Chauhan, "Analysis and compact modeling of negative capacitance transistor with high ON-current and negative output differential resistance – Part I: Model description," *IEEE Transactions on Electron Devices*, vol. 63, no. 12, pp. 4981–4985, December 2016.

[9] G. Pahwa, T. Dutta, A. Agarwal, and Y. S. Chauhan, "Designing energy efficient and hysteresis free negative capacitance FinFET with negative DIBL and 3.5X I_{ON} using compact modeling approach," in *IEEE European Solid-State Device Research Conference (ESSDERC)*, Sept 2016, pp. 41–46.

[10] S. Mueller, J. Mueller, A. Singh, S. Riedel, J. Sundqvist, U. Schroeder, and T. Mikolajick, "Incipient ferroelectricity in Al-doped $\mathrm{HfO_2}$ thin films," *Advanced Functional Materials*, vol. 22, no. 11, pp. 2412–2417, 2012.

[11] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano Letters*, vol. 8, no. 2, pp. 405–410, 2008.

[12] G. Pahwa, T. Dutta, A. Agarwal, S. Khandelwal, S. Salahuddin, C. Hu, and Y. S. Chauhan, "Analysis and compact modeling of negative capacitance transistor with high ON-current and negative output differential resistance – Part II: Model validation," *IEEE Transactions on Electron Devices*, vol. 63, no. 12, pp. 4986–4992, December 2016.

[13] T. Dutta, G. Pahwa, A. Agarwal, and Y. S. Chauhan, "Impact of process variations on negative capacitance FinFET devices and circuits," *IEEE Electron Device Letters*, vol. 39, no. 1, pp. 147–150, Jan 2018.