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Compact J-band Oscillators With 1 mW RF Output Power and Over 110 GHz Modulation Bandwidth

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Abstract—We report a compact resonant tunneling diode (RTD) oscillator with 1 mW output power at 260 GHz and a modulation bandwidth of over 110 GHz. The oscillator employs an RTD device size of $4 \times 4 \mu\text{m}^2$ resonating with an 88 μm long microstrip inductor. The total chip size is $470 \times 530 \mu\text{m}^2$. All fabrication was done using the low cost photolithography technique.

I. INTRODUCTION

Resonant tunneling diodes (RTDs) offer a competitive resolution compared to the state of the art photonics-based uni-travelling carrier photodiode (UTC-PD) and CMOS technologies for high bandwidth wireless links as they are the fastest electronic device that is compact, cost effective and operates at room temperature, with highest reported frequency of 1.98 THz [1]. Few demonstrations of wireless links using RTDs have already been done with data rates of 34 Gbps using single channel on-off keying [2] and 56 Gbps using 2-channel frequency- and phase-division multiplexing schemes [3]. However, the bandwidth can be improved further by reducing circuit parasitics and increasing the output power [4]. Using higher output power in the milli-Watt range together with high gain antennas can enable practical wireless communication links over 100's of meters.

In this paper, we demonstrate an RTD source technology with a J-band (220 GHz- 325 GHz) oscillator exhibiting 1 mW output power and over 110 GHz of measured modulation bandwidth. We also report data rates of up to 13 Gbps (limited by available equipment) using these devices.

II. DEVICE STRUCTURE

The layer structure of the RTD wafer which was used in the oscillator reported here is illustrated in Fig. 1. It was grown by molecular beam epitaxy (MBE) by IQE Ltd on a semi-insulating InP substrate. It employs a 4.5 nm $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ quantum well sandwiched between two 1.4 nm AlAs barriers and 25 nm spacers. This double barrier quantum well (DBQW) design offers a current density J_p of $\sim 3 \text{ mA}/\mu\text{m}^2$ and a peak-to-valley current ratio (PVCR) of 3. The collector and emitter layers are made of highly Si doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ material ($3 \times 10^{19} \text{ cm}^{-3}$). The fabricated RTD has a mesa size of $4 \times 4 \mu\text{m}^2$. Chemical wet etching ($\text{H}_3\text{PO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}=1:1:38$) was used to define the RTD mesa. This recipe has an etch rate of 100 nm/min. Polyimide PI-2545 was used for device passivation and isolation. The devices exhibited a peak-valley bias voltage difference (ΔV) of 0.7 V and peak-valley current difference (ΔI) of 25 mA. The measured IV characteristics are shown in Fig. 1(b). Fig. 1(c) shows a scanning electron microscope (SEM) image of a fabricated device. Fig. 2(a) shows the layout of the RTD oscillator circuit. The RTD oscillator design approach presented here employs a single RTD device as shown in Fig.

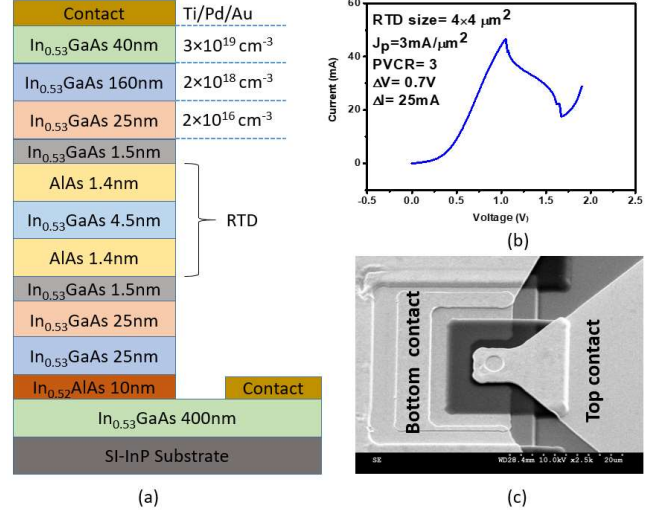


Fig. 1. (a) Epitaxial RTD structure, (b), IV characteristics of the RTD device, (c) SEM of the fabricated RTD device.

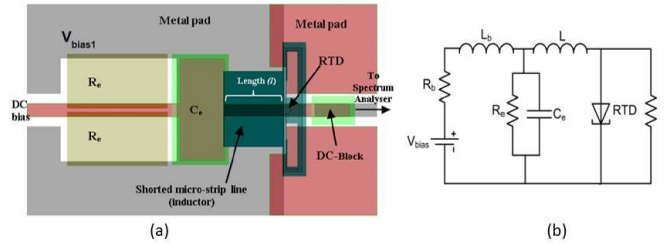


Fig. 2. (a) Layout of the RTD oscillator circuit, (b), equivalent RTD oscillator circuit

2(b). The shunt resistor R_e is used to suppress the low frequency bias oscillations and the bypass capacitor C_e is used to ground the RF signal. Inductance L is designed to resonate with the RTD self-capacitance to obtain the desired frequency. L_b is the biasing cable inductance. R_L is the load resistance. The RTD is modelled by its lumped equivalent circuit model; a negative differential conductance $-G_n$ in parallel with the self-capacitance C_n . A thin film NiCr resistor (33nm thick, with a sheet resistance of $50 \Omega/\square$) was used to realize R_e , while a SiN_x metal-insulator-metal (MIM) capacitor to realize C_e . The thin dielectric layer SiN_x (75 nm) was deposited by inductively coupled plasma (ICP) chemical vapor deposition (CVD). The inductance L was realized by a microstrip transmission line short stub. It consisted of a 20 μm wide signal line on top of a 1.2 μm thick polyimide. With this configuration, the characteristic impedance of the microstrip line is 10.4Ω . The short-circuit termination was provided by the capacitor C_e . R_L was introduced by the input impedance of the spectrum analyzer or power meter which is usually 50Ω .

III. EXPERIMENTAL RESULTS

Two oscillator circuits were fabricated and characterized, one from our first generation of J-band oscillators with a capacitor C_c value of 8 pF (called Generation 1 here), and the other from present devices with a reduced C_c value of 0.1 pF (called Generation 2 here). Fig. 3 shows the measured modulation bandwidth (S_{21}). Generation 1 oscillators exhibited a limited 3 dB bandwidth of 7 GHz, while Generation 2 oscillators exhibited a large 3 dB bandwidth of over 110 GHz due to its reduced C_c . The oscillation frequency was measured on-wafer using Keysight's N9040B UXA signal analyzer. The oscillator was biased using a GSG Cascade probe through the DC port, while the RF output signal was connected to the measurement equipment (spectrum analyzer or power meter) through, a WR-3 GSG Picoprobe. For measuring the oscillation frequency, the output signal was mixed down using a J-band harmonic mixer from Farran Technology (WHMB-03). The spectrum analyzer and mixer were connected through a diplexer which is used to separate the local oscillator (LO) and intermediate frequencies (IF). With the built-in signal identification function of the spectrum analyzer, an oscillation frequency of 260 GHz was measured. The output power was measured by the Erikson PM5 power meter. The measured oscillator power was 0.5 mW before calibrating for waveguide taper and probes losses of 3 dB to be 1 mW.

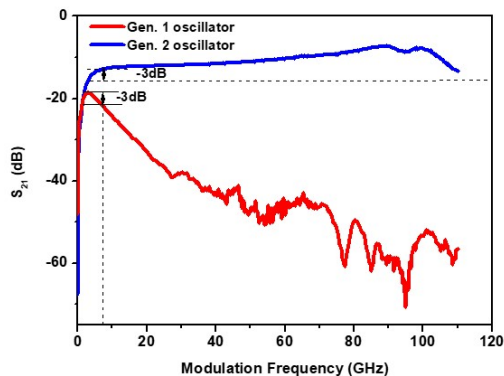


Fig. 3. Measured modulation bandwidth of Gen. 1 and Gen. 2 oscillators.

A schematic of the wireless experimental setup is illustrated in Fig. 4. A pseudorandom binary sequence (PRBS) data generator (Agilent N4903B) with maximum data rate capability of 13 Gbps was used and clocked using an internal clock. A bias-T connected to a 67 GHz probe was used to relay both the DC bias and the data from the PRBS to the DC port of the oscillator. The oscillator output (RF port) was connected via a GSG probe (including waveguide transition) to a 300 GHz VDI

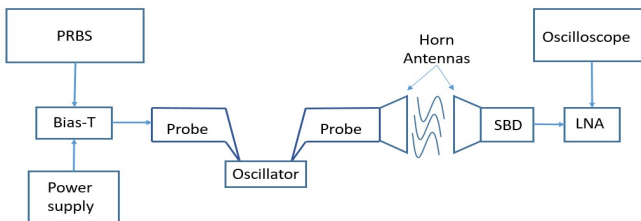


Fig. 4. Schematic diagram of the wireless measurement setup.

horn antenna to transmit the output signal (carrier + data) which was then received by another 300 GHz horn antenna that was connected to a Schottky barrier diode (SBD) detector, the WR3.4ZBD from VDI. The SBD was connected to a low noise amplifier from VDI with 20 GHz bandwidth, which feeds the data into a digital communications analyzer (Agilent 86100C). It uses the same clock that was used to clock the PRBS and data from the SBD to generate the eye diagrams.

In the experiment, the bias voltage and current were 1.24 V and 160 mA, respectively. A 200 mVp-p data signal was applied from the PRBS into the bias-T. The wireless transmission range was 1 cm. Clear eye diagrams were observed on the oscilloscope. The data rates were increased from 650 Mbps up to 13 Gbps (limit for our PRBS).

Fig. 5 (a) shows the eye diagrams of generation 1 oscillators with data rate of 7 Gbps. Beyond 7 Gbps the eye closes showing a bandwidth limitation matching the bandwidth measurement in Fig. 3. Fig 5(b) shows the eye diagram of generation 2 oscillators with data rate of 13 Gbps. The 13 Gbps is the limit for the existing data generator and optimizing the setup with a higher bandwidth data generator is expected to result in achieving higher data rates.

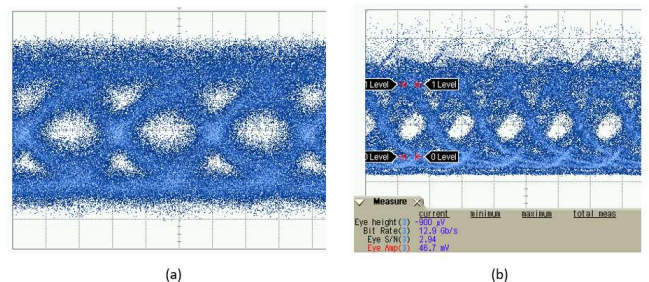


Fig. 5. (a) eye diagrams of Gen. 1 oscillators with data rate of 7 Gbps, (b). eye diagrams of Gen. 2 oscillators with data rate of 13 Gbps.

IV. CONCLUSION

We have demonstrated J-band RTD based oscillators with high output power of 1 mW and over 110 GHz modulation bandwidth. These offer a competitive advantage in terms of circuit simplicity and manufacturing requirements, and output power as well as modulation bandwidth over competing technologies that are more complex, less efficient or require cooling. The reported devices are expected to support wireless data rates of over 110 Gbps with a range of 10s of meters.

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