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Design, Simulation, Fabrication and Characterisation of 4H-SiC Trench MOSFETs

By

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Declaration

This thesis is submitted to the University of Warwick in support of the application for the degree of Doctor of Philosophy. It has not been submitted in part, or in whole, for a degree or other qualification at any other University. Parts of this thesis are published by the author in peer-reviewed research papers listed. Apart from commonly understood and accepted ideas, or where reference is made to the work of others, the work described in this thesis is carried out by the author in School of Engineering of the University of Warwick.

Zohreh Mohammadi

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To Mum, Dad, Zahra and Hamid

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Publications List

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2. T. X. Dai, Z. Mohammadi, S. A.O. Russell, C. A. Fisher, M. R. Jennings, P. A. Mawby, "4H-SiC Trench Structure Fabrication with Al_2O_3 Etching Mask", Materials Science Forum, Vol. 897, pp. 371-374, 2017

3. Rong, H., Z. Mohammadi, Sharma, Y., Li, F., Jennings, M. and Mawby, P. (2014). 4H-SiC Diode Avalanche Breakdown Voltage Estimation by Simulation and Junction Termination Extension Analysis. *Materials Science Forum*, 778-780, pp.824-827.

Abstract

For solid-state power devices, there exists need for a material with a higher band gap which will result in a higher critical electric field, improved power efficiency and thermal performance. This has resulted in the use of Silicon Carbide (SiC) as a serious alternative to Silicon for power devices. SiC trench MOSFETs have attracted major attention in recent years because of 1) lower on resistance by eliminating the JFET effect which exists in lateral MOSFETs, 2) higher channel density which lowers the threshold voltage and 3) reduction of the required surface area because of the vertical channel. These advantages allow faster switching speeds and the potential for a higher density of devices leading to more compact modules.

This work was focused on fabrication of the first generation of 4H-SiC trench MOSFETs in Warwick University. Two main goals were achieved in this work: a comprehensive understanding of fabrication of trenches in 4H-SiC and fabrication of first generation of 4H-SiC trench MOSFET with mobility as high as 35 $cm^2/V.s$.

A detailed study of fabrication of trenches in 4H-SiC showed that both masking method and the etching recipe affect the smoothness, the shape and the angle of the sidewalls. The biggest challenges in etching trenches in SiC were found to be roughness of sidewalls and microtrenches. Microtrenches are small trenches in the corner of the sidewall that results in lower breakdown voltages. The results showed that while Nickel (Ni) is the best mask to eliminate microtrenches, Silicone dioxide (SiO_2) results in the smoothest and cleanest sidewall hence lowest leakage current. SiO_2 was used as the etching mask and a sidewall shadow was created by optimizing the etching RF power that helped to protect the trench sidewall and hence successfully eliminate microtrenches.

The trench MOSFET fabrication results showed that without any post etch or oxidation treatments the mobility can be as low as $5cm^2/V.s$. Post etch treatment using hydrogen (H_2) annealing resulted in the highest mobility as high as 35 $cm^2/V.s$ while post oxidation H_2 annealing or phosphorus activation resulted in higher mobility close to 15 $cm^2/V.s$. The downside of post etch treatments is slightly higher leakage current than the post oxidation treatment.

List of Abbreviations

SiC	Silicon Carbide
MOSFET	Metal Oxide Semiconductor Field Effect Transistors
MOS	Metal Oxide Semiconductor
IGBT	Insulated Gate Bipolar Transistor
SEM	scanning electron microscope
AFM	atomic force microscopy
ICP-RIE	Inductively coupled plasma- Reactive Ion Etcher
HF	Hydrogen fluoride
N_2	Nitrogen
N	Nitrogen atom
H_2	Hydrogen
POB	post exposure bake
Al	Aluminium
Ti	Titanium
Ni	Nickel
SiO_2	Silicon dioxide
Ar	Argon
O_2	Oxygen
Cl_2	Chlorine
RTA	Rapid Thermal Annealing
N_2O	Nitrous oxide

N_2	Nitrogen
NO	Nitric oxide
POA	Post Oxidation Annealing
P	Phosphorus
NF_3	Nitrogen trifluoride
SF_6	Sulfur hexafluoride

List of Symbols

A Active die area (cm^2)

E Electric field (Vcm^{-1})

V_{GS} Gate source voltage (V)

I_D Drain current (A)

V_{DS} Drain source voltage (V)

V_{Th} Threshold voltage (A)

I_D Drain current (A)

μ_{FE} Field Effect Mobility($cm^2/V.s$)

g_m gate transconductance

I_{D/cm^2} Current Density (A/cm2)

$R_{DS(on)}$ Drain to Source On State Resistance (Ω)

R_s Source resistance (Ω)

R_{ch} Channel resistance (Ω)

R_{epi} Epi layer resistance (Ω)

R_{subs} Substrates resistance (Ω)

V_{br} Breakdown Voltage (V)

$\boldsymbol{I_{gss}}$ Gate source leakage current (A)

$\boldsymbol{I_{dss}}$ drain-source leakage current (A)

N_D Drift region doping (cm^{-3})

BV_{pp} parallel plane breakdown voltage(V)

W_{pp} parallel plane depletion width(μ)

N_A	doping concentration of the P-body (cm^{-3})
C_{ox}	the specific capacitance of the gate oxide
k_B	Boltzmann's constant
T	absolute temperature
ε_S	semiconductor dielectric constant
n_i	intrinsic carrier concentration
N_c	effective density of state of the conduction band
N_v	the effective density of state of the valance band
E_g	energy gap
ε_{OX}	oxide dielectric constant
N_{bulk}	bulk doping of the semiconductor
m_{SC}	the effective mass in semiconductor
h	Planck's constant
m_{OX}	the effective mass in the oxide
Φ_B	the barrier height of the oxide/semiconductor interface
E_{OX}	electric field across oxide

Chapter

1 Introduction to 4H-SiC Trench MOSFETs

1 Introduction

During recent years, it has been widely recognized that power switching devices in Silicon (Si) are approaching their theoretical limits and there is a need for another material with higher band gap, higher critical electric field, improved power efficiency and thermal performance. Silicon Carbide (SiC)

devices have been suggested as a suitable replacement to Si because of many advantages associated with this material.

Power semiconductors such as Schottky barrier diodes, MOSFETs are the heart of the power electronics. SiC Power semiconductors offer faster switching, less power loss and can be used in higher voltage and temperature applications. These advantages make SiC devices great candidate for applications such as convertors for renewable sources, electrical cars and trains. Using SiC devices results in higher energy efficiency and can also improve the size of passive components and weight by 50% [1].

SiC devices are widely used in power convertors such as AC/DC power convertors for renewable energy sources, PFC, UPS and power convertors for industrial applications such as air-conditioning. The main advantage that makes SiC suitable for this application is the higher energy efficiency compared to the SiC devices.

The other application of SiC power devices is in electrical distribution systems. The electricity grid is moving toward distributed energy resources in the recent years by addition of many distributed and renewable resources such as combined heat and power (CHP) plants, solar and wind farms. This results in more losses in the system as energy needs to be transmitted over long distance from these distributed resources. Also these resources degrade the frequency instability of the grid because of their low inertia and also volatile energy

generation. The grid should operate at frequency of 50Hz (in the UK) to avoid any damage to the connected electrical assets. At any time the consumption and generation of electricity should be equal to keep the frequency at 50 Hz and the volatile nature of renewable resources means that control of frequency is more difficult. The other main challenge with the renewable resources is their contribution to reduction in grid inertia. This is mainly due to the fact that inverter connected solar and wind farms do not provide rotational inertia. Low inertia results in faster frequency changes in the grid [1]. Currently National Grid uses assets with response times as fast as 1 seconds to balance the frequency during the consumption/generation imbalance to restore the frequency back to 50Hz but it is predicted that there will be need for assets with sub second response time. SiC Power systems offer high speed control of supplies and motors and also enables high voltage, high frequency power conversion that is necessary to add large scale renewables to the grid. This means that using such systems not only offer higher energy efficiency but also offer high speed of control during any electricity imbalance [2].

Other applications of SiC devices include aerospace and military where there is a need for stable power devices in extreme temperature since SiC can operate at temperate as high as 250 °C.

1.1 Wide Band Gap Material

4H-SiC material has a bandgap three times higher than Si (Table 1.1) which is a key benefit in term of power devices. Higher band gap results in a higher intrinsic temperature, at which the intrinsic carrier concentration becomes comparable to the doping concentration, resulting in a sudden current increase and hence failure of the device.

The intrinsic carrier concentration (n_i) of a semiconductor is given by equation 1.1, where N_c is the effective density of state of the conduction band, N_v is the effective density of state of the valance band, E_g is the band gap energy, k_B is the Boltzmann constant and T is the absolute temperature.

$$n_i = \sqrt{N_c N_v}.\exp(-\frac{E_g}{2.k_B.T}) \qquad \text{Equation (1.1)}$$

As can be seen, the intrinsic concentration depends on the energy band gap and the temperature. Hence due to the narrow band gap of Silicon (Si), the intrinsic carrier concentration of Si increases rapidly with the increase in the temperature and hence Si devices fail in lower temperature compared to SiC device. This high intrinsic temperature of SiC allow the device to reach temperature as high as 700°C before it fails.

1.1.1 High Avalanche Breakdown Electric Field

With a breakdown electric field 10 times higher than Si for the same voltage rating, 4H-SiC devices can be designed with thinner, more highly doped drift regions, which results in less specific-on resistance. This leads to higher power efficiency and decreasing power loss with respect to 4H-SiC.

Property	**Si**	**3C-SiC**	**6H-SiC**	**4H-SiC**
Bandgap(eV)	1.12	2.35	3.08	3.28
Breakdown field (MV/cm)	0.3	1.5	2.2	2.3
Intrinsic carrier concentration (cm^{-3})	1x10^{10}	1.5x10^{-1}	1.6x10^{-6}	5x10^{-9}
Electron mobility (cm^2/Vs)	1350	900	370	800
Hole mobility (cm^2/Vs)	480	40	80	120
Saturated electron velocity ($10^7 cm/s$)	1	2	2	2
Thermal conductivity (W/cmK)	1.5	4.9	4.9	4.9
Dielectric constant	11.8	9.6	9.7	9.7
Electron affinity (eV)	4.05	3.8	3.3	3.1

Table 1-1: Comparison of Si with different SiC polytypes

1.1.2 High Electron Saturation Velocity

An electron saturation velocity twice that of Si, enables faster switching frequencies. A higher electron saturation velocity also results in shorter

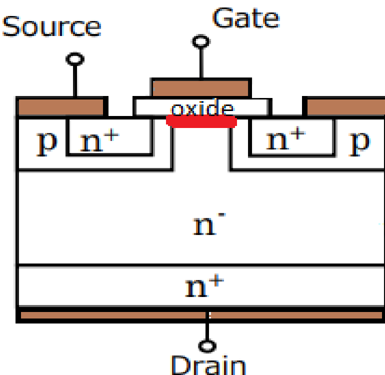
reverse recovery time as charge stored in the depletion region can be removed faster.

Other advantages such as the thermal conductivity being three times that of Si devices results in a higher thermal stability making 4H-SiC material perfect thermal conductors with further reduction in cooling requirements. 4H-SiC is the most favorable SiC polytype due to higher carrier mobility and a higher degree of isotropy.

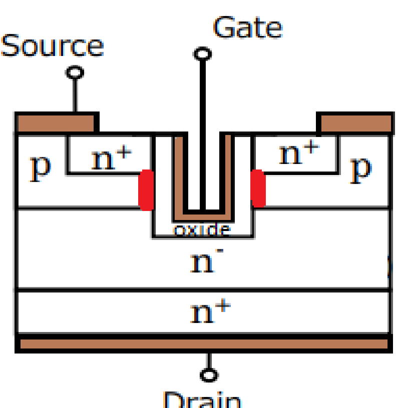
1.2 Metal Oxide Field Effect Transistor (MOSFET) Structures

Metal Oxide Field Effect Transistor (MOSFET) structure can be designed so that the channel region is lateral or vertical. The first SiC MOSFETs introduced were mostly based on lateral channels (Figure 1.1A). The recent attempts to block voltages higher voltages, resulted in the introduction of the double diffused MOSFET (DMOSFET), where a drift layer is included on top of the drain region to support high voltages, the channel is formed laterally when voltage is applied to the gate. As can be seen in Figure 1.1, there still exist a JFET region in this type of MOSFET like lateral MOSFETs. Also the lateral

channel imposes limitation on the cell pitch and requires a large surface area to accommodate the lateral channel.



(A): N-channel DMOSFET, the current channels (shown in red) are horizontal under the gate oxide.



(B): N-channel trench MOSFET, the current channels (show in red) are vertical on the trench sidewalls

Figure 1.1: Structure of (A) planar MOSFET (B) trench MOSFET

The attempts to reduce the specific-on resistance resulted in introducing trench MOSFETs. Trench MOSFET includes a vertical structure where the source and drain are on the opposite side of the wafer to support higher voltages. The gate is located in a trench and the channel is created on the vertical wall of the trench (Figure 1.1B). The trench is extended to the drift region and hence the parasitic JFET effect that exists in the lateral channel MOSFET is eliminated and therefore the specific on resistance is improved significantly. Since the current channels are vertical, using trench technology offers a higher channel density and helps to minimize the required surface area, since the channels exist on the side walls.

1.2.1 On State

Figure 1.2 shows the current flow in a trench MOSFET during the on state when the device is conducting current. The gate metal/insulator/P-body region create a MOS capacitor and hence applying voltage to the gate metal that is higher than a minimum voltage, called threshold voltage (V_{Th}), creates a current channel on the trench side wall in the P-body region. This will create a current path from the N+ source to the drain.

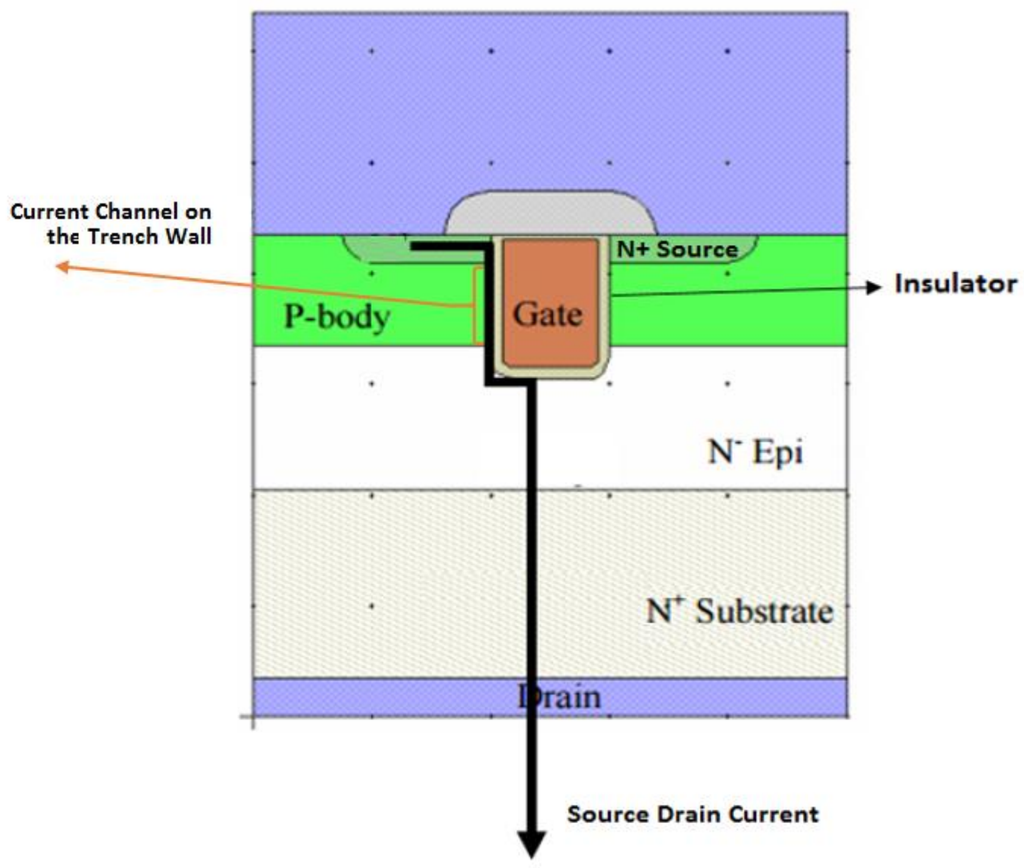


Figure 1.2: Current flow in trench MOSFET [3]

The amount of the source drain current depends on the gate voltage and the on-resistance between the drain and source. The current-voltage (I-V) curve of a MOSFET is shown in Figure 1.3. As can be seen, during the on state the I-V curve is divided into two regions: linear (ohmic) and saturation (pinch-off) regions. For low drain voltage (V_D), the I-V characteristics have a linear form, this area is called ohmic region. When the drain voltages is increased the drain current saturate at a maximum level (pinch off or saturation region). The transition between the ohmic region and the pinch off region is called quasi saturation.

As can be seen, the higher the gate voltage is, the higher the drain current would be. If the drain voltage is increased to more than the breakdown voltage rating of the device, avalanche breakdown happens, and the amount of current passing between the source and the drain increases rapidly and suddenly. The avalanche breakdown is due to the increase of electric field to more than the critical electric field of the semiconductor material. Though as would be discussed in this work, basic SiC trench MOSFET structure such as the one shown in Figure 1.2 enters breakdown because of breakdown of the insulator layer not the semiconductor material.

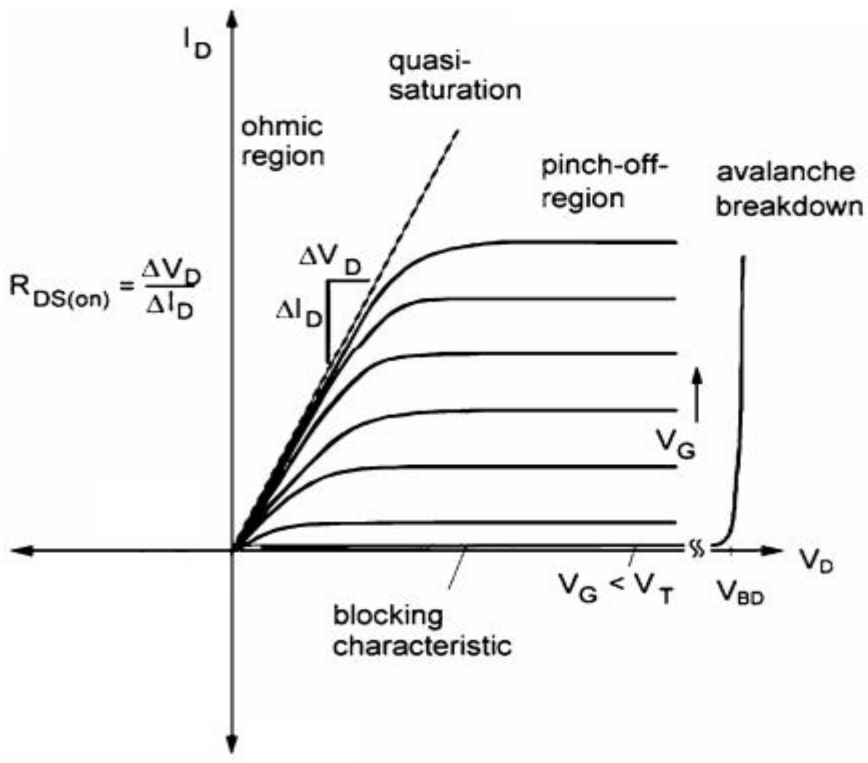


Figure 1.3 : Current-Voltage characteristics of a MOSFET [4]

The other factor that affect the I-V characteristics, is the on resistance between the source and drain (R_{DSON}). The amount of current that can pass through source to drain when the voltage is increased, depends on R_{DSON}. The slope of the curve on the ohmic region is representative of R_{DSON}, lower slope means higher R_{DSON}. Higher on resistance, results in higher energy loss, lower switching speed and lower channel mobility and should be minimized.

1.2.2 Off State

Off state refers to the state where there is no voltage applied to the gate contact (or if the gate voltage is less than the threshold voltage). During the off state, the current channel does not exist on hence there is no current flow between the N+ source and the drain region except for very little leakage current. The drain voltage in this state is supported by the depletion region that is created by the P-body/N- drift junction. The effect of the N+ source/P- body/N- drift bipolar transistor is suppressed by shorting the P-body and N+ source [5]. It is very important to choose the right thickness and doping for the P-body region, otherwise the depletion region in the P-body will reach to N+ source that will result in a large leakage current. The reach through design can result in premature breakdown of the device.

Figure 1.4 shows the creation of depletion region across P/N junction. The depletion region is created when the device is in reverse biased operation mode when a positive voltage is applied to the N- doped (drift) region. Majority

carriers in the N- doped region (free electrons) are attracted to the positive terminal, leaving immobile positive ions near the P/N junction. The positive ions near the junction on the N- doped region, will start to repel the holes on the P- doped side. The holes will leave immobile negative ions near the P/N junction. This will create a depletion region near the P/N junction of immobile ions that will block the current (Figure 1.4). The ions near the junction create a strong electric field that will block the voltage.

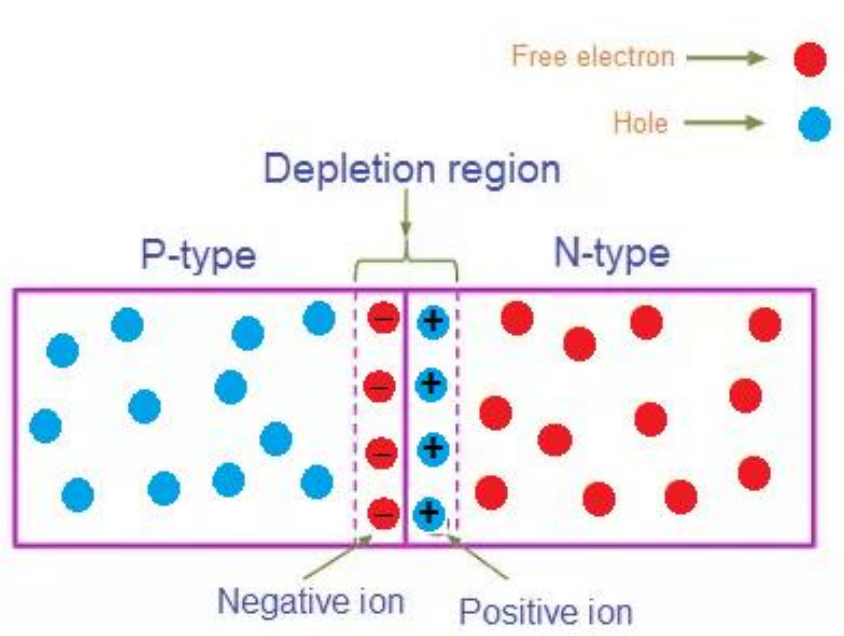


Figure 1.4: Depletion region created in a PN junction.

Higher drain voltages, result in higher electric field in the P/N junction. When this electric field reaches the critical electric field of SiC material, an

abrupt leakage current is observed. This maximum drain voltage is called breakdown voltage. The blocking capacity of the trench MOSFET is determined by the N^- drift region thickness and doping. This will be discussed in more details in the Chapter 3.

1.3 MOS Capacitor

MOS capacitors are the foundation of every MOSFET including trench MOSFETs, therefore it is necessary to understand MOS capacitors. In this section, the operations modes of a MOS capacitors are explained. As will be discussed in the Chapter 2, the quality of MOS capacitors in the trench MOSFETs is the main problem with SiC MOSFETs that needs to be improved hence the common defects and problem with MOS capacitor such as oxide and interface defects and leakage current are also discussed.

1.3.1 Characteristics of an Ideal MOS Capacitors

A MOS capacitor is made of two electrodes, separated be an insulation layer (Figure 1.5).

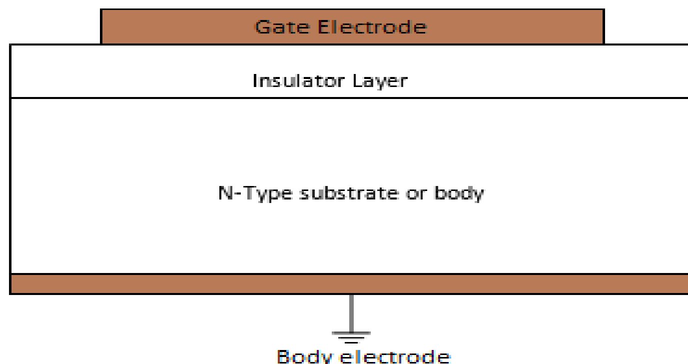
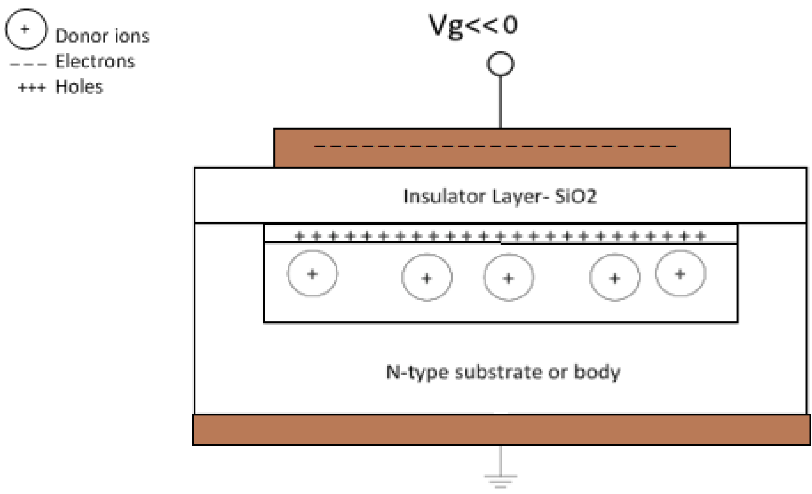
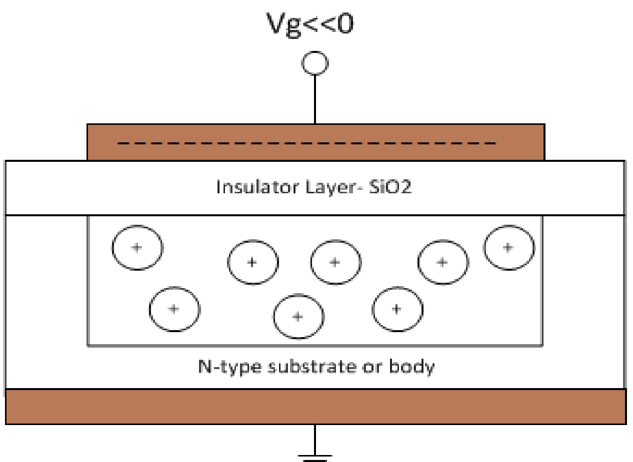


Figure 1.5: Structure of a MOS capacitor

A low resistivity metal (gate) at the top of the insulating layer acts as the first electrode and the N-type (or P- type) substrate act as the second electrode. When voltage is applied to the gate one of the cases shown below (Figure 1.6) takes place in the substrate.



(A) Inversion in Si MOS capacitor



(B) Deep depletion in a SiC MOS capacitors

Figure 1.6: Applying a large negative voltage to the gate results in two different behavior in Si and SiC MOS capacitors, while inversion is observed in Si MOS capacitor (A), a deep depletion is created in a SiC MOS capacitor

1.3.2 Inversion or Deep Depletion ($V_g \ll 0$)

When a large negative gate voltage is applied, it repels the electrons from the surface. In silicon substrate electrons leave the surface and the minorities of opposite charge (holes) are attracted to the surface right beneath the interface. This creates a channel of minority carriers (holes) in an N- type substrate where majority carriers are electrons (Figure 1.6A). This mode is called inversion where the surface of the substrate is inverted to the opposite polarity.

In SiC MOS capacitors, because of the long generation time for minorities, inversion mode is not observed and instead the SiC MOS structure turns to the

deep depletion mode. The very low concentration of the minorities in SiC is the reason behind the long generation time for minorities [6]. In this mode the negative voltage of the gate repels the electrons from the surface, and electron leave immobile accepter ions behind (Figure 1.6B). The capacitance is reduced to the minimum value at this mode and its value of capacitance in this mode is proportional to the doping concentration of the material.

1.3.3 Depletion ($V_g < 0$)

When the gate voltage is still negative but closer to zero, it still repulse the electrons in smaller number from the surface and they leave positively charged ions. This means in the area closer to the interface, the number of majority carriers (electron) is less than the value in the original substrate. That is the reason that this mode is called depletion.

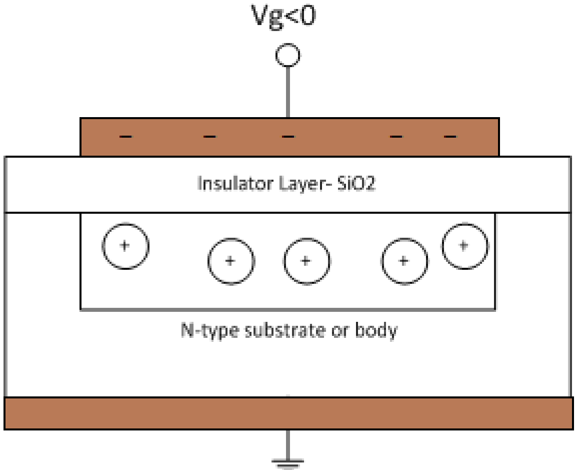


Figure 1.7: Depletion mode in SiC MOS structure

1.3.4 Accumulation Region ($V_g > V_{Th}$)

When the voltage is increased to more than a certain value, called threshold voltage (V_{Th}), the gate metal attracts a large amount of negative charges to a surface very close to the interface. In this case a high density of majority carriers (electron) are presented in the shallow layer just beneath the interface and therefor the MOS capacitor is operating in accumulation region. At this mode, the capacitor reaches the maximum level of capacitance that defines the oxide capacitance.

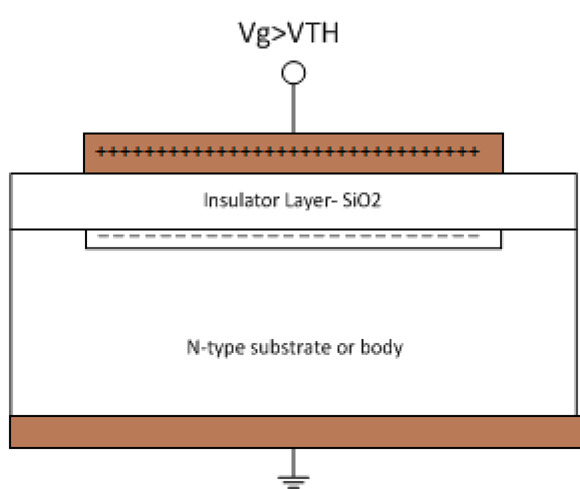


Figure 1.8: Accumulation mode in MOS structure

1.3.5 Electrical Properties of a MOS Capacitor

An ideal MOS capacitor has the following properties [7]:

1) The difference between work-function of metal (ϕ_M) and semiconductor (ϕ_{SiC}) is zero. This means the Fermi level of metal ($E_{F\,M}$) and SiC substrate ($E_{F\,SiC}$) is flat and is aligned. There is no flow of charge in this condition

2) Only charges in semiconductor and the opposite charge in the gate can exist under any biasing condition

3) There are no traps in the interface of SiC/SiO_2 and the oxide is free from defects and impurities.

4) There is no flow of carriers through the insulator layer.

Figure 1.9 shows the energy band model in accumulation, deep depletion and flatland mode of an ideal SiC MOS capacitor.

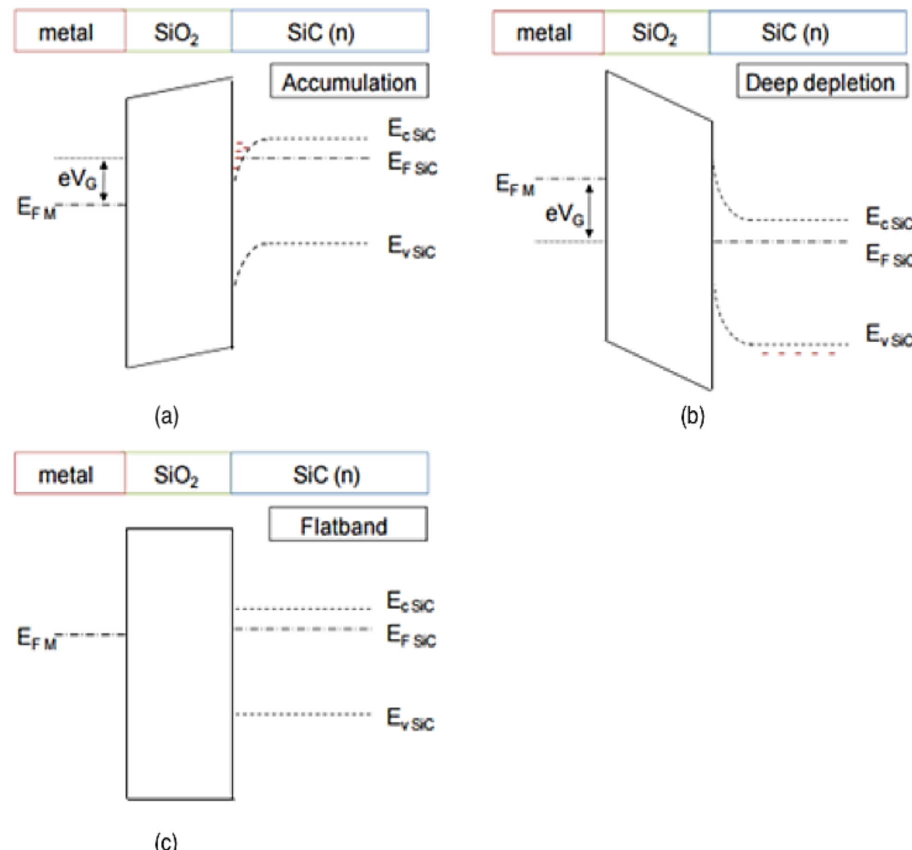


Figure 1.9: The energy band models a n- type SiC MOS capacitor assuming no defects exist [8]

Flat band mode is the state where there is no voltage applied to the gate and hence the conduction and valence bands are flat (Figure 1.9C). Fermi level is the highest energy state occupied by electrons in a material at absolute zero temperature. The distance between the metal and substrate Fermi levels in the ideal MOS capacitor is equal to the applied gate voltage (eV_G). If the MOS structure is in the flatband mode, this difference is called flatband voltage (V_{FB}), which is equal to zero for an ideal MOS capacitor.

$$V_{FB} = \Phi_M - \Phi_{SiC} \qquad \text{Equation (1.2)}$$

Applying bias will result in separation between Fermi levels of metal gate and the semiconductors and therefor flatband voltage is not zero anymore. When bias is applied to the gate, no bending will occur in the metal as it is an equipotential region (only the energy bands move up or down) but due to the imbalance of the charges in the semiconductors, there will be bending of the energy band near the interface where there is build up charge as well as moving up or down the energy band.

In accumulation region, positive voltage is applied to the gate. The resulting charges in gate and substrate moves the gate energy bands lower relative to the substrate and therefor bend the valence (E_v) and conduction (E_c) band downward near the interface in the semiconductor. This bend represents higher electric field that exist due to the crowding of electrons near the interface in accumulation.

As the negative bias is applied to the gate, the gate energy bands start to move higher relative to the n-type SiC substrate where electrons are repelled from the surface and the electric field is reduced [8].

In reality there are a number of issues that challenge the performance of a MOS capacitor specially SiC MOS structure. The oxide that is thermally grown on SiC substrate has defect and there exist different charges in addition to substrate and metal charges, like oxide trapped charges, fixed charges in oxide.

In the next section defects such as charges and leakage current of a non-ideal MOS capacitor are introduced.

1.3.6 Charges

In a real MOS device, there are charges in the oxide and the interface of SiC/SiO_2. There are at least four type of charges associated with SiC MOS capacitor. These charges are: fixed oxide traps, mobile ionic charges, oxide trapped charges and near interface trapped charges [9].

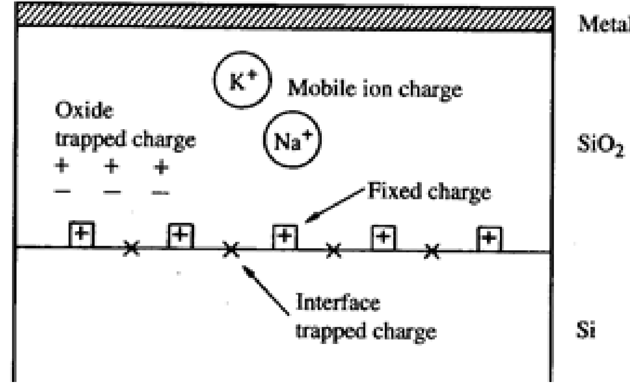


Figure 1.10: Oxide charges in SiC MOS structures [10]

1.3.6.1 Oxide trapped charges (Q_{tox})

These are high-energy positive or negative charges that exist in the oxide (not the interface) due to the existence of holes or electrons that are trapped in the defects in the oxide [11] during FN tunneling, avalanche breakdown and similar processes [10]. Density of these trapped charges varies and any kind of leakage current through the oxide can increase the number of trapped charges.

$Q_{tox} = -V_{FB}.C_{ox}$ Equation (1.3)

1.3.6.2 Mobile oxide charges ($\boldsymbol{Q_m}$)

These lightly charged ions are caused by the process and can move if voltage is applied to the device. It is suggested that ionic impurities inserted into the oxide film during oxidation may be the main cause of this issue [10]. These charges could be improved by surface conditioning before growing oxide or by passivation after oxidation. These charges could be calculated using the following equation in high temperature:

$Q_m = -\Delta V_{FB}.C_{ox}$ Equation (1.4)

1.3.6.3 Interface trap density ($\boldsymbol{D_{it}}$)

Interface trapped charges are one of the main challenges in growing high quality oxide on SiC. The origin of this issue is not clear but it is suggested that existence of carbon clusters and dimmers and oxygen vacancies very close to the interface can cause higher trap density [12].

These charges can be charged through the SiC surface potential. They can trap electron and holes and act as a scattering center.

These traps can be charged positively or negatively depending on the potential in the surface. Accepter traps are charged negatively, while donor traps are charged positively if filled.

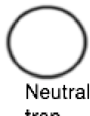


Figure 1.11: Different type of trap charges [12]

1.3.6.4 Near interface fixed charges (Q_f)

These are charges located near the interface inside the oxide. The density of fixed charges relates to oxidation process such as: gases, temperature and ramping down condition and could be reduced by optimizing process or annealing post oxidation [13].

The presence of fixed oxide charges shifts the flatband voltage of the MOS structure toward the positive range if the traps are positively charged and toward the negative range if the charges are negative. The value of fixed oxide charges could therefore be measured by following equation:

$$Q_f = (\phi_{ms} - V_{FB})C_{ox} \qquad \text{Equation (1.6)}$$

Where $\phi_{ms} = \phi_M - \phi_{SiC}$.

Figure 1.12 shows the capacitance-voltage graph of an ideal SiC MOS capacitor. As can be seen the maximum capacitance takes place when the capacitor is in accumulation and the capacitance decreases due to the depletion until it reaches deep depletion.

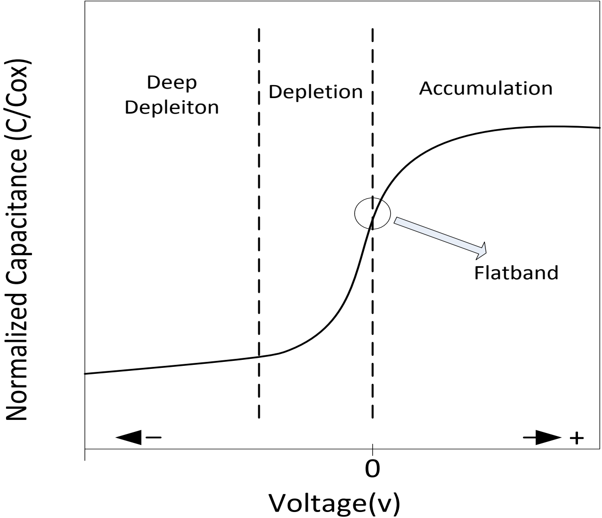


Figure 1.12: C-V characteristic of an ideal n-type SiC MOS capacitor

In a real MOS capacitor structure, the oxide and interface charges discussed earlier will change the electrical behavior of the device. As it is shown in the Figure 1.13, oxide trapped charges shift the flatband voltage positive or negative if it is charged positively and negatively (respectively). Near interface traps only create hysteresis [13].

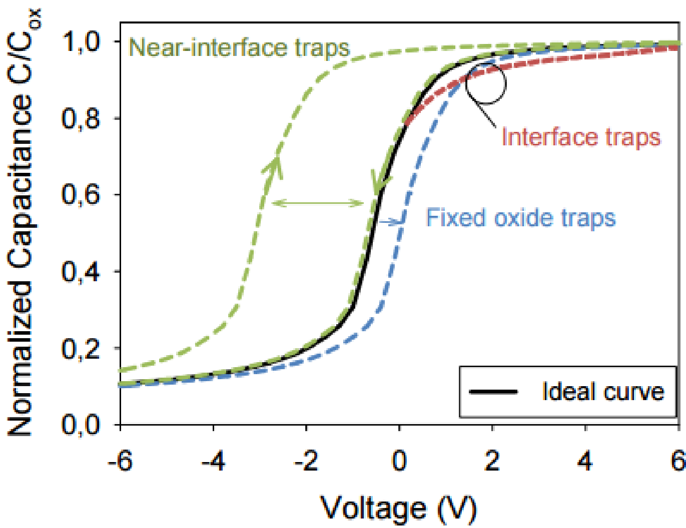


Figure 1.13: changes in C-V graph induced by oxide and interface charges [13]

Interface traps stretch out the C-V curve near the accumulation region. As mentioned previously in accumulation region, a large of number of electrons are attracted toward a thin layer very close to the interface in SiC bulk. Since interface traps can act as columbic scattering energy, they will scatter electrons away from the interface and therefor it takes a longer time to create the accumulation layer.

The most common way to characterize the defect in SiO_2/SiC interface is using the C-V measurement. High-low frequency method is used in this project to measureD_{it}.

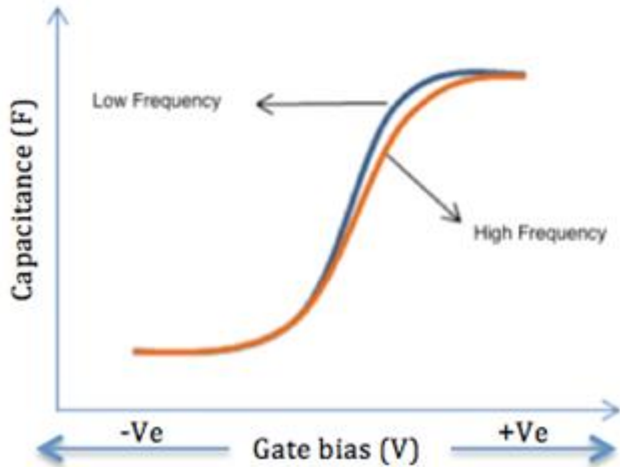


Figure 1.14: High-low frequency measurement technique

In the high-low method, capacitance in measured at two different frequencies. At very low frequency, all the interface charges can respond to the signal and at the high frequency, the interface trap life time is not short enough to respond to the signal. The equivalent circuits are shown in Figure 1.15, where C_{ox} is oxide layer capacitance, C_D is depletion layer capacitance and C_{it} is the interface trap capacitance.

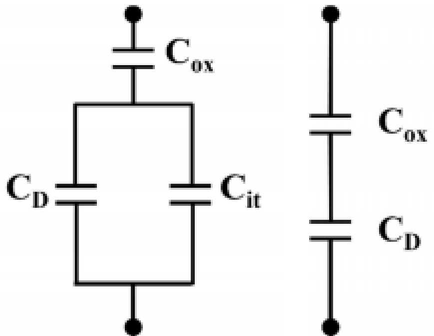


Figure 1.15: The equivalent circuits of capacitance in MOS capacitor under (A) low and (B) high frequency measurement

Capacity is defined as

$$C = \frac{\Delta Q}{\Delta V} \qquad \text{Equation (1.7)}$$

Where ΔQ is the change in charge corresponding to the change in the voltage, ΔV. Based on the models shown in Figure 1.15, the low frequency capacitance (C_{LF}) is defined by:

$$C_{LF} = \frac{1}{C_{OX}{}^{-1} + (C_{it} + C_D)^{-1}} \qquad \text{Equation (1.8)}$$

Since trap density (D_{it}) is defined as C_{it}/q, using equation 1.8, the trap density is given by

$$D_{it} = \left[\frac{C_{ox}.C_{LF}}{C_{ox} - C_{LF}} - C_D\right].\frac{1}{q} \qquad \text{Equation (1.9)}$$

Also the high capacitance (C_{HF}) is given by

$$C_{HF} = \frac{C_{ox} C_D}{C_{ox} + C_D} \qquad \text{Equation (1.10)}$$

Using equation 1.10 to solve for C_D, equation 1.9 could be rewritten as

$$D_{it} = \left[\frac{C_{ox} C_{LF}}{C_{ox} - C_{LF}} - \frac{C_{ox} C_{HF}}{C_{ox} - C_{HF}}\right].\frac{1}{q} \qquad \text{Equation (1.11)}$$

Since the value of traps can be different across the interface, the trap density is plotted against the energy band gap position ($E - E_V[eV]$) [9]. The position of the Fermi level with respect to the majority carrier band edge at the surface of the semiconductor is given by

$$E - E_V = \frac{E_g}{2} - KTIn(\frac{N_{bulk}}{n_i}) + \Phi_S \qquad \text{Equation (1.12)}$$

Where kT is the thermal energy at room temperature and Φ_S is the surface potential given by

$$\Phi_S = \frac{qN_{bulk}{W_{dep}}^2}{2\mathcal{E}_S\mathcal{E}_{OX}} \qquad \text{Equation (1.13)}$$

N_{bulk} is the bulk doping of the semiconductor, $\mathcal{E}_{OX}$ is the oxide dielectric constant, $\mathcal{E}_S$ is the dielectric constant of the semiconductor, W_{dep} is the depletion width.

1.3.7 Leakage currents

The other main challenge in achieving a high quality oxide is gate leakage current; there are two main sources of leakage current in MOS devices that are described in this section.

1.3.7.1 Direct tunnelling

When electrons move from a small band gap material (e.g.: metal) to a medium band gap material (e.g.: oxide), they encounter a potential barrier. According to quantum theory, electrons can pass this barrier and move inside the other material in some cases. This is called direct tunneling [14].

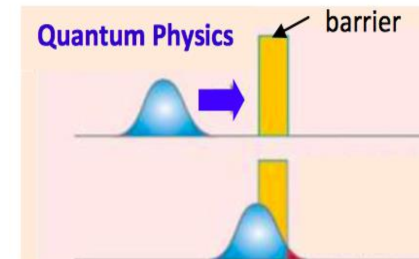


Figure 1.16: Quantum physics theory: Electron (blue in the picture) can pass the potential barrier and move from one medium to another medium [14]

As the width of the potential barrier decreases, the probability of direct tunneling increases exponentially [10]. When gate voltage is applied. At lower gate voltages electron can move from gate through oxide to 4H-SiC through the trapezoidal potential. This phenomenon happens mostly in oxide thinner than 5nm and therefor is not a main concern for this work where the oxide thickness is between 70-100 nm.

At higher gate voltages FN tunneling is responsible for the leakage current that is explained in the next section.

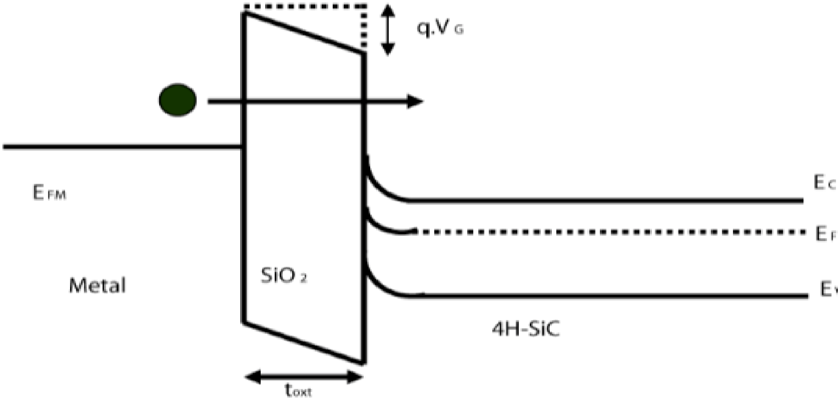


Figure 1.17: Direct tunneling in a MOS capacitor [10]

1.3.7.2 Fowler-Nordheim (FN) tunnelling

F-N tunneling refers to the phenomenon where the charges start to cross through the oxide to SiC substrate when voltage is applied to MOS structure. At higher gate voltages, the resulting electric field pulls down the barrier of the SiO_2 layer. The higher the electric field, the barriers is pulled down more and eventually the triangular potential barriers results in tunneling of the carriers from metal Fermi level into the oxide. Once the carriers are inside the dielectric layer, they can move to valence or conduction band of the dielectric material and if they move to the conduction bands they are free to move inside and through the oxide. This results in a leakage current across the gate.

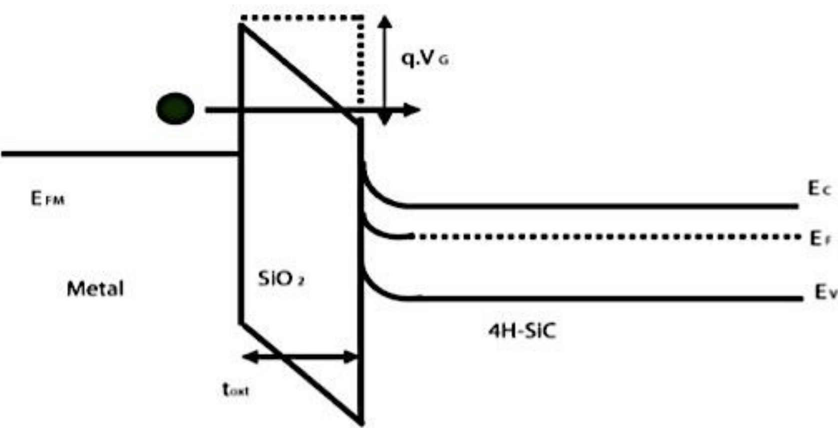


Figure 1.18: FN tunneling in MOS device [10]

The FN tunneling current, J_{FN}, is given by [10]

$$J_{FN} = \frac{q^3 m_{sc}}{8\pi h m_{ox} \Phi_B} E_{OX}{}^2 exp\left[-\frac{4\sqrt{2m_{ox}\Phi_B{}^3}}{3qhE_{ox}}\right] \qquad \text{Equation (1.14)}$$

Where h is Planck's constant, m_{SC} is the effective mass in semiconductor, m_{OX} is the effective mass in the oxide, Φ_B is the barrier height of the oxide/semiconductor interface and E_{OX} is the electric field across the oxide and is defined as

$$E_{OX} = \frac{V_g V_{FB}}{d} \qquad \text{Equation (1.15)}$$

Where V_g is the gate voltage, V_{FB} is the flatband voltage and is the oxide thickness.

The theoretical barrier height for FN tunneling is calculated as the difference between the dielectric conduction band and the semiconductor Fermi level. The conduction band offset between SiO_2 and 4H-SiC is 2.7 eV which is smaller compared to conduction band offset of 3.2eV between of SiO2 and Si. This results in higher leakage current in SiC devices (Figure 1.19). FN tunneling is one of the main concern in 4H-SiC MOS devices and can affect the lifetime of the device. FN tunneling gives rise to the gate current and can increase the threshold voltage, which results in power dissipation. FN tunneling is reported to happen in oxide with thickness less than 50nm [10].

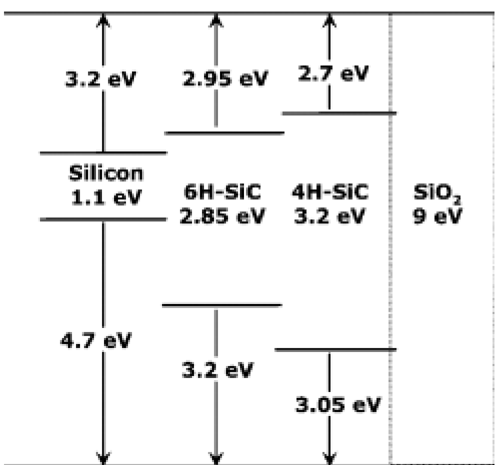


Figure 1.19: Conduction(top) and valence band(bottom) offsets of different semiconductors with respect to SiO_2

1.3.7.3 Trap Assisted Tunnelling

Trap assisted tunneling results in leakage current due to presence of traps density. This leakage current exists in low bias voltages as well. The amount of this leakage current depends on the traps density, though it is believed electric field stress can increase the number of traps and hence increases the leakage current. This current is called stressed induced leakage current (SILC) [10] [15].

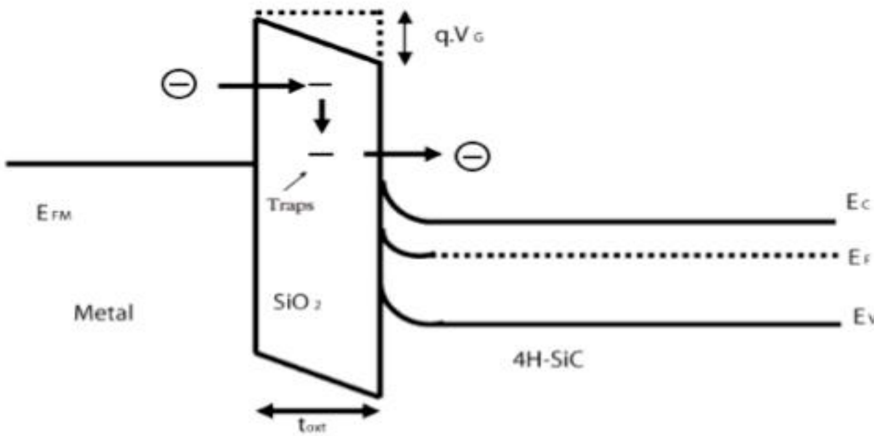


Figure 1.20: Trap assisted tunneling [10]

1.3.8 Electrical Characteristics of Trench MOS Capacitors

As MOS capacitor acts as the heart of a MOSFET, it is important to optimise this structure to reduce trap density and leakage current to have a functional trench MOSFET. One of the main questions in this project was if a trench MOS capacitor exhibits the same characteristics as a planar MOS capacitor. As there were not many resources available, the first step was to fabricate a trench MOS capacitor to confirm that the electrical characteristics such as the C-V curves are same as the planar MOS capacitors.

The process of fabricating trench MOS capacitor is shown in the Figure 1.21. 4H-SiC wafer was cleaned in solvent in ultrasonic bath to make sure there were not any large contaminations on the wafer (a), then a thick layer (2 μm) of TEOS oxide was deposited on the wafer to act as the mask layer (b). The next

step was to pattern the trench structures on the SiO_2 layer (c). Shipley S1818 has been used as the photoresist in this step.

Corial 200IL ICP-RIE etcher was used to etch the trenches in the SiO_2 layer (d) then photoresist layer is removed, and using SiO_2 as the mask, trenches were etched in the SiC layer (e) using ICP power of 1000 W, RF power of 55 W, gas flow of SF_6 and Ar with flow rate of 50 SCCM and 40 SCCM (respectively) and pressure of 10 mTorr. The sample carrier was made of quartz and graphite. After removing the oxide layer with HF (f) the samples were cleaned properly using the process described in the Chapter 5, to prepare the samples for growing thermal oxide in the furnace. A layers of sacrificial SiO_2 layer was thermally grown on the SiC layer in N_2O atmosphere at 1300°C for 4 hours (g). After removing the sacrificial oxide layer in HF (h), gate oxide layer was thermally grown on SiC wafer (i). A layer of Titanium and Nickel (Ti/Ni) was then deposited at the back substrate to act as the substrate electrode. This layer was activated by annealing at 1200°C in Argon (Ar) for 2 minutes. The last step was to deposit Aluminum (Al) on the front side as the gate metal electrode.

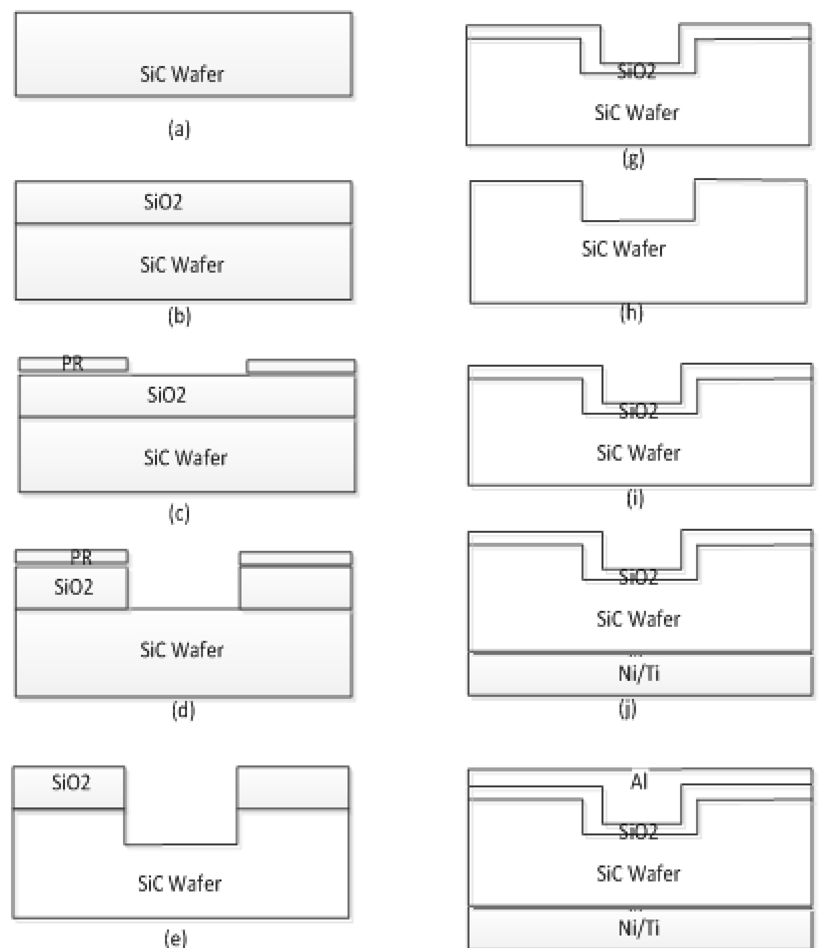


Figure 1.21: Fabrication process of a trench MOS capacitor

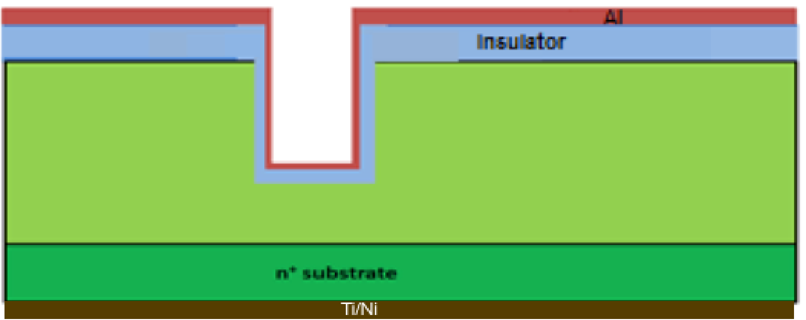


Figure 1.22: Structure of trench MOS capacitor

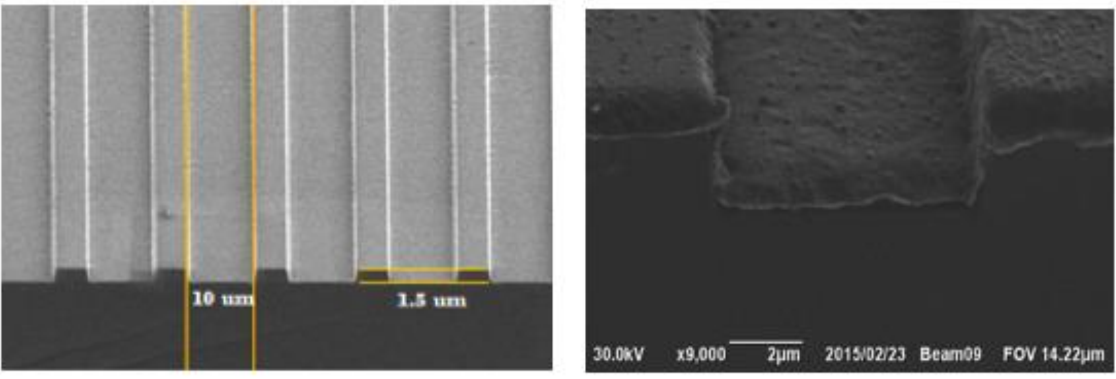


Figure 1.23: 4H-SiC trench MOS capacitor (A) after etch (B) after gate metal deposition

Table 1.2 lists the structure of different fabricated capacitors and the resulting capacitance from calculation and capacitance. The measured capacitance is from the accumulation region, where the capacitance is at its maximum. In previous section, the calculated capacitance is explained. All measurements were done in low frequency (100Hz) to make sure the effect of traps densities is taken into consideration.

No.	No. of trenches	Trench width (µm)	Trench depth (µm)	Surface width (µm)	Trench length (µm)	Calculated capacitance (F)	Measured Capacitance (F)
1	40	4	1.5	4	1000	1.23×1^{-10}	1.18×1^{-10}
2	40 (45°)	4	1.5	4	1000	1.23×1^{-10}	1.14×1^{-10}
3	30	4	1.5	4	1000	9.23×1^{-11}	9×1^{-11}
4	50	4	1.5	4	1000	1.55×1^{-10}	1.38×1^{-10}
5	40	7	1.5	4	1000	1.57×1^{-10}	1.58×1^{-10}
6	40	10	1.5	4	1000	1.91×1^{-10}	1.9×1^{-10}
7	40	4	1.5	6	1000	1.45×1^{-10}	1.5×1^{-10}
8	40	4	1.5	8	1000	1.68×1^{-10}	1.65×1^{-10}
9	Planar					1.35×1^{-10}	1.5×1^{-10}

Table 1-2: Comparison of capacitance measurement and calculation for 4H-SiC trench MOS capacitors with different structure. The oxidation was done in O_2 for 1.5 hour at 1400°C, this was followed by 3 hours of N_2O annealing at 1300°C. The resulting oxide thickness was 0.112 µm. All trenches are located on $11\bar{2}0$ wall except number 2, which is on °45 from $11\bar{2}0$ wall.

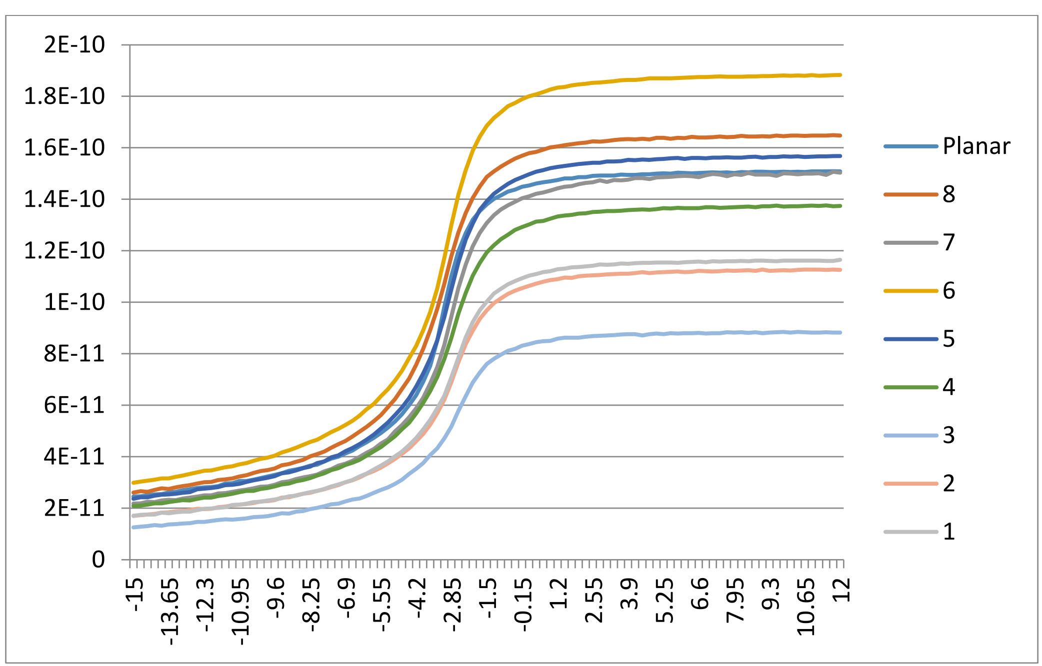


Figure 1.24: C-V measurement of fabricated 4H-SiC trench MOS capacitors from table 2

When calculating the capacitance, the circumstances such as crowding of the electric field in the corners of trenches and its effects on capacitance were ignored. As can be seen in Figure 1.25, the values of measured capacitance and calculated capacitance are very close. The lower values of measured capacitance can be explained by existence of leakage current through the oxide.

Capacitors number 1 and number 2 have same area, but trenches' wall are allocated on $11\bar{2}0$ plane in capacitor number 1, and 45° toward $1\bar{1}00$ orientation in capacitor number 2. It is seen that orientation of sidewall has resulted in a very small difference between these two capacitors.

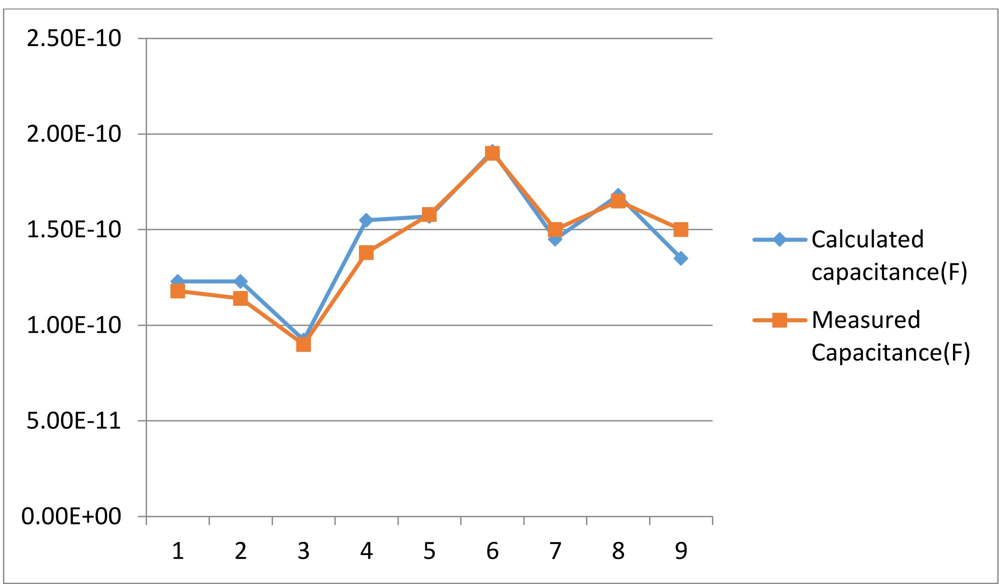


Figure 1.25: Comparison of capacitance from measurement of the fabricated capacitors and ideal value(calculation). The numbers on x-axis refer to the Table 1.2

When trench sidewalls were very rough, the C-V measurement usually showed very high leakage current. As can be seen in the Figure 1.26(B), lower frequencies in this case resulted in the lower capacitance, this is because the longer the voltage is applied on MOS structure, the more leakage current is resulted and therefor the capacitance is decreased.

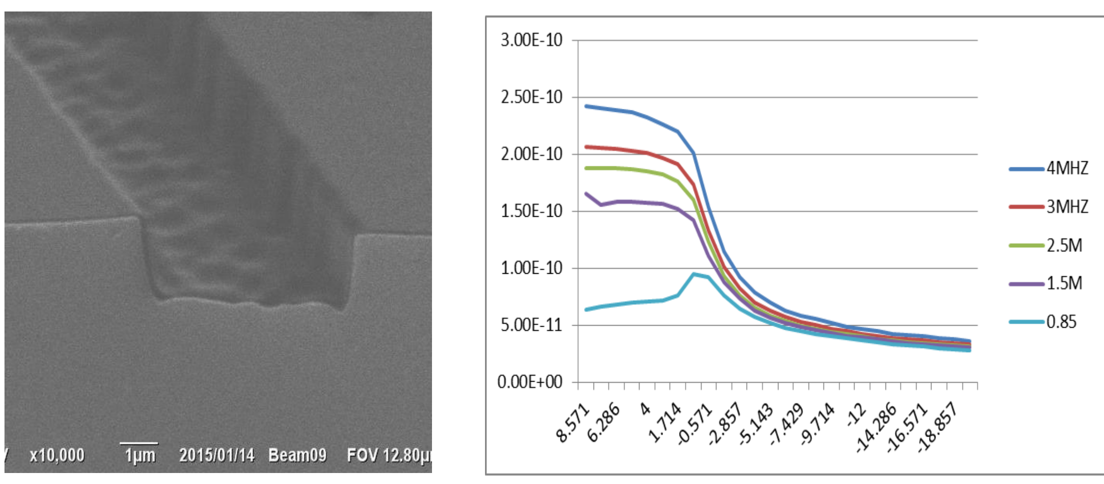


Figure 1.26: 4H-SiC trench MOS capacitor with rough sidewalls (a) and its resulting C-V measurement

1.4 Conclusion

This chapter gives an overview of characteristics of MOS capacitors and trench MOSFETs. In the last section, the common issues with gate oxide such as charges and leakage current were also introduced. This basic information will be used across this work and in different chapters.

In the next chapter, a literature review of the current status of 4H-SiC trench MOSFETs and the common issues and suggested solution will be discussed. The literature review was a necessary step to understand the areas that need to be improved in 4H-SiC trench MOSFET.

Chapter 2, reviews the studies on 4H-SiC trench MOSFETs. This was an important step before starting this work, as the results provided a clear overview of the current status of these devices, and the issue and obstacles that need to be solved. The literature review showed that the main issue with SiC trench MOSFETs, is the quality of the oxide and the interface between SiC and oxide. Hence the gate oxide was chosen as the focus of this project, instead of achieving high breakdown voltages.

In chapter 3, a brief overview of design and simulation of 4H-SiC trench MOSFETs is provided. The results show that without a gate protection, the breakdown always happens in the oxide layer in the bottom of the trench corners.

Chapter 4 is entirely focused on etching trenches in of 4H-SiC. The very first experiments proved that the etching process is a very challenging steps that usually results in very rough surface or microtrenches at the corners of the trenches. Since there were no experience of fabrication of trench structures in our group, the author concluded that a very clear understanding of etching process is necessary to be able to minimise roughness and microtrenches. The results of this chapter is that with combination of optimised photolithography process, mask and etching process, these issues could be minimised.

In chapter 5, the focus is to understand the processes that are commonly used to fabricate gate oxide. During the literature review, it became clear that except mobility and breakdown voltage, there are limited information on how different gate oxidation method can affect the electrical parameters of the device such as leakage current, threshold voltage. The results of this chapter provide a clear overview of effect of gate oxidation methods on the electrical measurements of the fabricated devices. This result could be used to determine which method should be used, or how the processes should be combined to achieve a reliable device when fabricating the second generation MOSFETs.

Chapter 6 provide some recommendations on how to fabricate a 1.2kV 4H-SiC trench MOSFET with higher current density and more reliable gate oxide.

1.5 References

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Chapter 2 Literature Review of 4H-SiC Trench MOSFETs

2 Introduction

SiC is a very attractive material for high voltage, low on-resistance rated devices due to its superior material properties; high critical electric field strength, low intrinsic carrier concentration and high thermal conductivity. Table 2.1 gives a history of some of the first SiC MOSFETs produced and their corresponding specific on resistances [1]. At present, optically triggered SiC thyristor technology has been demonstrated up to blocking voltages of 12 kV /

100 A [2, 3] and commercially available 6.5 kV / 80A (GeneSiC Semiconductors) [4]. Highly novel termination structures based on junction termination extension (JTE) accompanied by guard rings have been optimized for these structures.

These SiC devices can currently operate at temperatures of 150 °C, displaying superior switching characteristics to their Si counterparts and lowest in-class on resistance for a given voltage and current rating. BJT technology offers a potential alternative for high voltage application. 4 kV BJTs have been realized [5] as early as 2005 with recent work being aimed at higher voltages. These devices demonstrated low currents with a specific on-resistance of 56 mΩ-cm² and a current gain of 9.

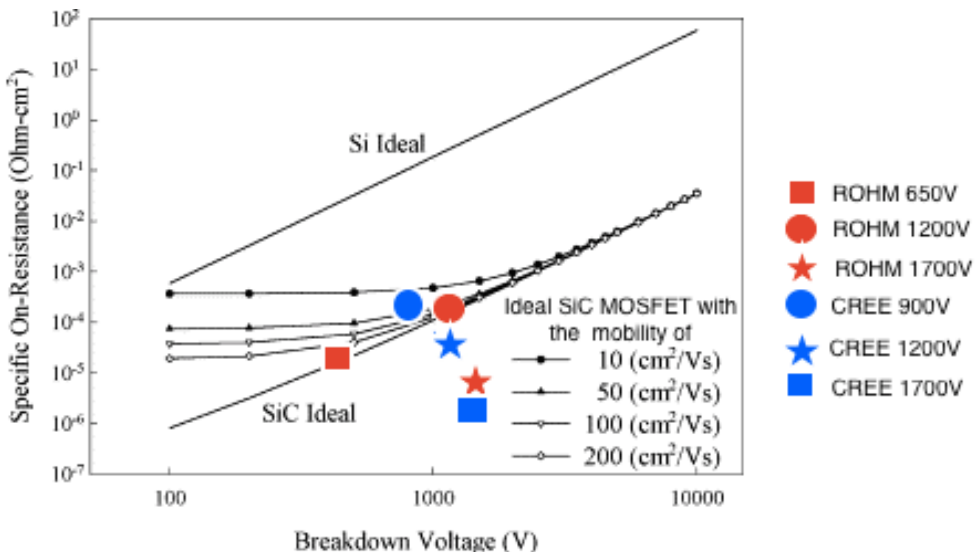

Figure 2.1: Specific on-resistance vs. breakdown voltage of modern SiC power devices

The current state of the art for BJT technology has been developed by TranSiC, now owned by Fairchild Semiconductor. These are up to 4 kV devices and can operate within the temperature range of -80 – 250 °C. For higher switching frequency application, the SiC metal oxide field effect transistor (MOSFET) offers huge potential, especially when one considers its ease of voltage control (gate drive). CREE inc. commercialized the SiC MOSFET in 2011 with their 1.2 kV / 24A / 160 mΩ range of devices. The SiC MOSFET has evolved from these initial 1.2 kV devices to 4kV/150A, right through to their latest research phase devices that have been demonstrated at 10 kV / 10 A. However, the specific on-resistance for these structures is extremely large measured [6] at 236 mΩ-cm2. This presents an opportunity for SiC trench MOSFETs to potentially enter the market. Trench MOSFETs can be realised with a lower specific on-resistance due to the elimination of the junction-FET (JFET) resistance. ROHM has commercialised SiC trench MOSFETs in the recent years with voltages as high as 1.2 kV, Current of 72A with on-resistance as low as 39 mΩ. These devices can operate at temperature as high as 175°C. The first question that needed to be answered before starting this work was: what are the problems with 4H-SiC trench MOSFETs that we might encounter? And what are the solutions that other studies have used. It is important to understand the common issues that the researchers and industry is facing and their suggested solution, to be able to find the areas in this field that needs improvement.

The main goal of this chapter is to look at studies on trench MOSFETs to provide an overview of main issues in design and fabrication of 4H-SiC trench MOSFETs. From the very first days of research on SiC MOSFETs, it became apparent that the main issue is the quality of oxide and interface of SiC/ SiO_2 and how it affects the operation and reliability of the devices.

2-1 Oxide Reliability

During the off state, the drain voltage is supported by a depletion region formed in the p-base and n-drift region. The depletion layer results in a high electric field in both sides of the depletion layer. This is illustrated in Figure 2.2, where the classis reverse biased p-n junction is shown.

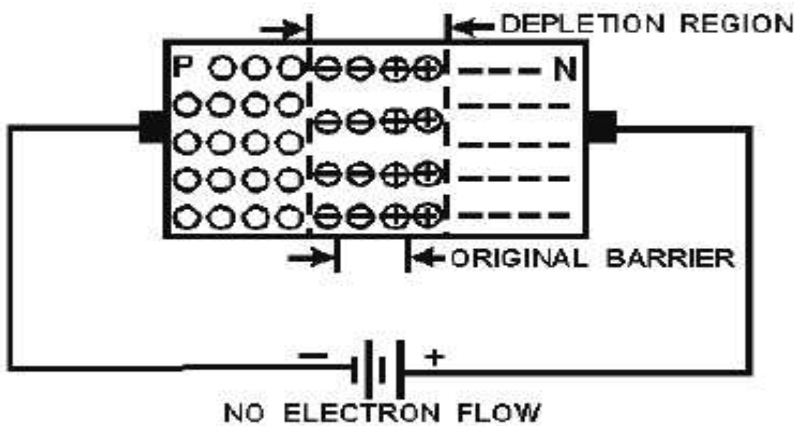

Figure 2.2: Formation of a p-n junction showing charge, electric field and potential distribution

The trenches in a trench MOSFET are extended downwards into the n-drift region to eliminate the effect of the parasitic JFET transistor, which exists in lateral channel MOSFETs. Therefore the gate oxide is exposed to the high electric field in the n-drift region. The electric field on the gate oxide in the off state could be determined from Gauss law:

$$E_{ox} = \left[\frac{\varepsilon_{SiC}}{\varepsilon_{ox}}\right] . E_{SiC} \qquad (2.1)$$

Moreover, since $\frac{\varepsilon_{SiC}}{\varepsilon_{ox}} = 2.5$, the electric field in the gate oxide is much higher than the adjacent high electric field in the drift region. Therefore the device reaches the critical electric field of the gate oxide before reaching the avalanche breakdown field of the SiC material or in other word the device operation is limited by the gate oxide properties not the SiC material. The oxide electric field is higher in the corner of the trench (field crowding) which limits the operation of the device even further [7]. The other limitation imposed by this issue is that there is a need for cooling which is usually not required in other high junction temperature devices [7].

The other origin of problem with SiC trench MOSFETs is the high electric field of SiC material. This high electric field results in a higher surface electric field up to 10 times greater than Si devices [8]. However the barrier for electrons in the conduction band between SiO_2 and SiC is only about 2.7eV [9,10] compared to a barrier height of around 3.15eV between SiO_2 and Si, therefore the probability of Fowler Nordheim(FN) Tunnelling of electron from SiC to oxide is higher in SiC especially at elevated temperatures. Flow of FN current into oxide and the trapping of electrons into oxide causes higher threshold voltage [12, 13]. This also means that because of elevated leakage current, the critical electric field in SiO_2 is reached before avalanche breakdown in the SiC bulk.

Although reducing the doping of the n-drift region can reduce the high electric field on the gate oxide, this results in a higher on-state resistance.

Many studies [7,14] have suggested keeping the oxide electric field under 1-2 MV/cm and the temperature below 150°C. This issue must be carefully studied and there is a need for an appropriate solution since the low critical electric field of the oxide imposes a limitation on the gate drive voltage under the on state condition and the p-doping of the base region must be optimized in order to minimize the threshold voltage [7].Various studies from the literature have suggested many approaches to minimize the oxide electric field in on and off states. Some believe the change in oxide material is the solution [7,14,16] while others seek solutions in utilizing alternative structures [17,18,19,20,21]. The results from all the studies agree that without the proper solution the operation of trench MOSFETs at elevated temperature for the long term might not be possible.

2.1.1 Optimization of Electric Field

The optimization of the electric field effect in SiC devices has been the focus of many studies since the start of research on 4H-SiC MOSFETs. To improve the high electric field distribution on the gate oxide, there have been many suggestions, which include:

- Electric Field Optimization through alternative structures.
- High permittivity insulators.

As mentioned before, the electric field on the SiO_2 is around 2.5 times higher than the adjacent SiC. This electric field is higher in the corner due to two-dimensional field crowding. The simplest solution to decrease the electric field at the trench corner is to

curve the corner [17,18,19,11]. One study [17] shows that the rounded corner results in around 2MV/cm less electric field on the oxide. It also indicates that wider trench width help to decrease the oxide electric field further. This study indicates that increasing the thickness of the oxide is another factor that can help to decrease the oxide electric field.

Trench width(μm)	4	6	8
Oxide electric field($\times 10^6$V/cm) rectangular corner	8.76	8.45	7.02
Oxide electric field($\times 10^6$V/cm) rounded corner	6.5	6.3	5.4

Table 2.1: Oxide electric field taking into account the trench width and rounded corners [17].

Another very popular design to decrease the oxide electric field at the bottom of the trench is to deploy a shielding technique with a P+ implanted region (gate shield) underneath the gate [18, 19, 11]. This structure is shown in Figure 2.3B and it can be inferred that this results in the creation of a JFET transistor between shielded regions within the structure.

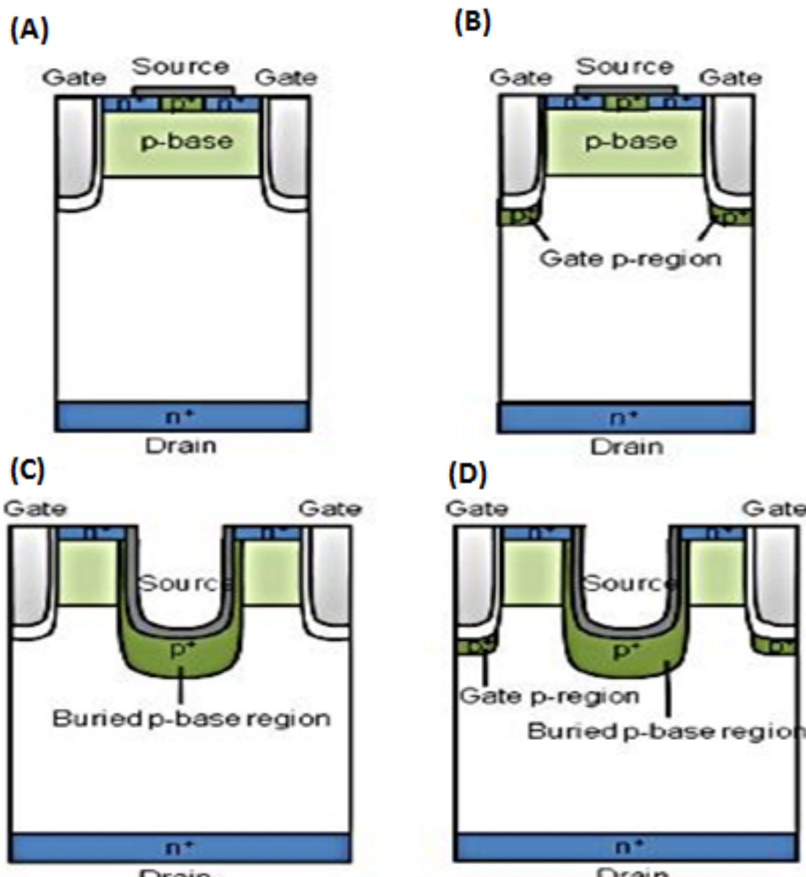

Figure 2.3: (A) conventional trench MOSFET (B) trench MOSFET with gate p-region c) buried p-region d) gate p-region and buried p-region[18]

Therefore the JFET resistance is added to the module, which degrades the on resistance. Studies [18,20] suggest that increasing the cell pitch can reduce the on resistance. However, it can be seen that the breakdown voltage and gate oxide electric field are also cell pitch dependent [18]. Increasing the cell pitch, increases the gate oxide electric field, with or without the gate shield, and also decreases the blocking voltage. Therefore there is always a trade-off between on resistance, electric field and breakdown voltage (Figure 2.4). Also it has

been suggested [18] that there is a critical cell pitch, with or without gate shield, which if exceeded, will result in punch through of the device. Therefore the effect of cell pitch must be carefully studied when designing a device.

Other suggested structures are source trenches that are deeper than the gate trenches (Figure 2.3C)[18]. Deeper trenches attract the electric field and hence protect the shallower gate trenches. There are no oxide in the deeper trenches and hence the device will not break down due to the high electric field on the oxide. A gate shield was added to both source and gate trenches in the study that increases the breakdown voltage but also the on resistance.

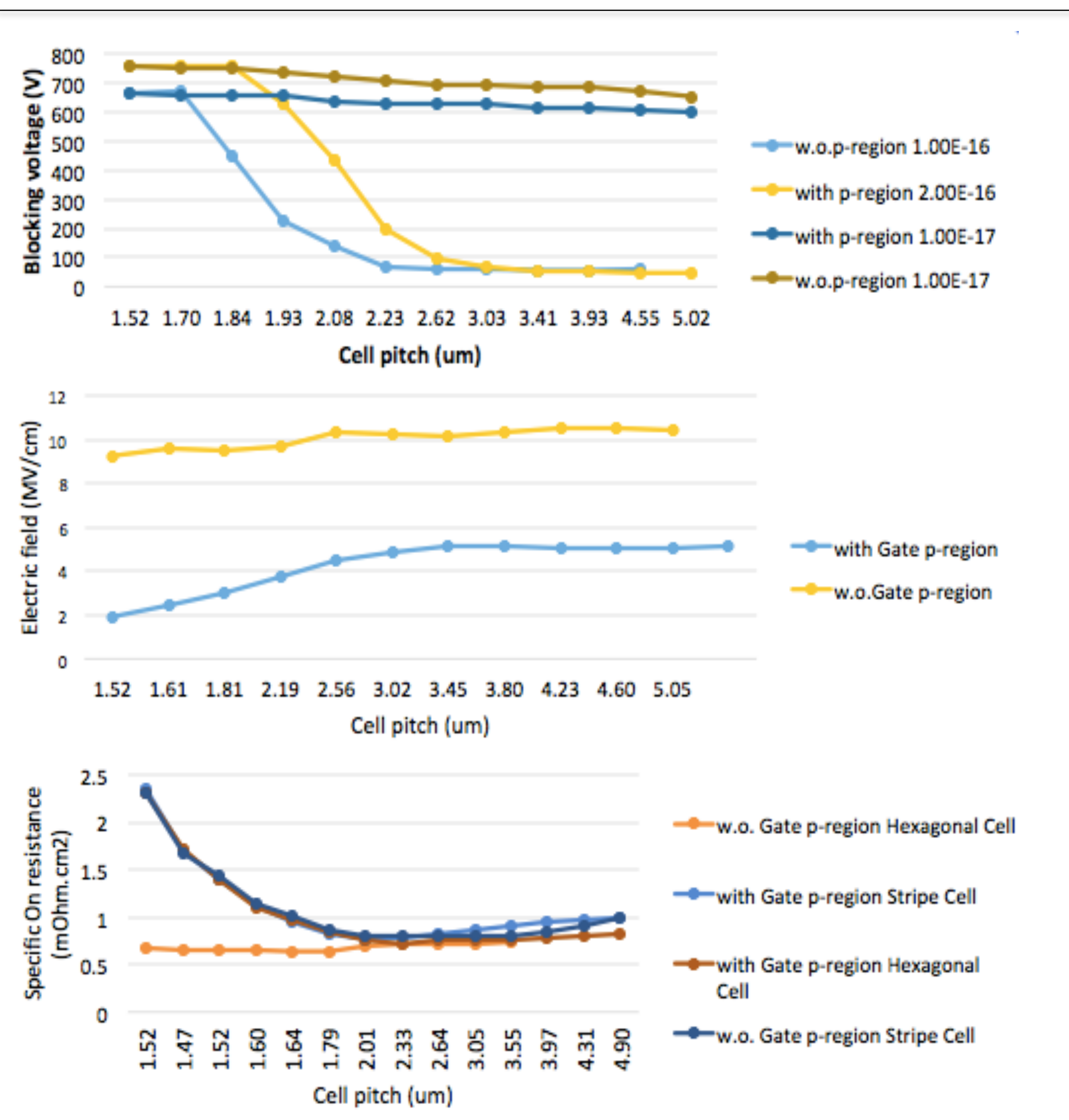

Figure 2.4: Cell pitch dependence of (a) blocking voltage with different p-base concentration (b) gate oxide electric field at the breakdown and (c) specific on-resistance of the UMOSFET structure with Gate p-region and without gate p-region[18]

Other alternative solution include shifting the high electric field from the gate trench to either another implanted p-region (Figure 2.5) [21] , to a trench p-base [18] or to a pillar under the p-base (super junction design) (Figure 2.6) [18,22].

[18] Has achieved gate oxide electric field of less than 3 MV/cm with on resistance of less than 6.8 mΩcm^2 using buried p-base regions for the breakdown voltage of 3300 V (Simulation results) which demonstrates a very promising trade-off between critical gate oxide electric field and the on resistance(Figure 2.6) but this structures are very difficult to fabricate.

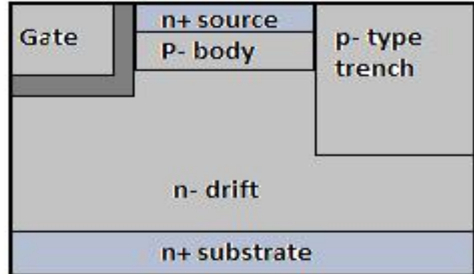

Figure 2.5: Trench MOSFET with implanted p-region shield

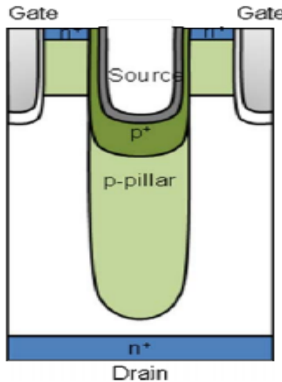

Figure 2.6: Trench MOSFET with Polysilicon trench [21]

Using a high permittivity insulator is another solution. Looking at equation 2.1, it can be seen that if a dielectric with higher permittivity is used, the oxide electric field will be reduced. The idea is to achieve a critical electric field of the insulator as close as possible to the SiC material to be able to take advantage of the SiC material properties to have a more reliable operation [14,16].[14] has considered dielectric such as TiO_2 and Ta_2O_5 and report successful results with low traps density(the value is not disclosed). Though this is a new method and there are not many study on reliability of this insulator layer in trench MOSFETs.

2-2 Channel Mobility

One main issue with SiC MOSFETs is the trapped interface charges. The source of trapped interface charges is not very clear in this moment, but it has been suggested that carbon clusters type defects situated near-interface sub-oxide is responsible [27]. Carbon dimmers in SiC or oxygen vacancies in the oxide near the interface can be the source of the trapped interface charge. A more detailed discussion on the origin of traps density will be presented in chapter 5. Interface traps create localized energy levels which rise exponentially toward the conduction band in the upper half of the band gap [27][28]. The value of the interface state density reaches above $10^{13} eV^{-1} cm^{-2}$ near the band edge in SiC MOS devices [27][29] and since the interface traps near the conduction band have the most influence on the mobility in n-channel

MOSFET[30], This high value of interface state density results in issues such as poor mobility in channel which is one of the main problem with SiC trench MOSFETS in low voltages [32]. A high density of interface traps causes the induced electrons at the interface to be trapped and no more available for conduction. Also this trapped charge acts as a columbic force which scatter the rest of the mobile electrons causing a lower channel mobility in SiC MOSFETs [28][34][7]. The channel mobility also needs to be improved to achieve a low threshold voltage.

Post oxidation annealing in Nitrogen, Phosphorus and Hydrogen have been the most effective solution to increase the mobility. Nitric oxide (NO) annealing is the most promising solution to date. In recent years there have been attempts to improve the mobility of the inversion channel by reducing the interface trap density. Successful studies suggest high temperature post oxidation annealing in nitric oxide [37][35][36][38] which has been reported to be useful in improving the channel mobility [39,40,20] and have reduced the interface state density near the conduction band of 4H-SiC to the value similar to 6H-SiC [37]. This has resulted in an increase of channel mobility to approximately 30-35 $cm^2/V.s$ and recently a peak field effect mobility of 150 cm^2/V has been reported by oxidation in presence of alumina [41]. Though in recent years Phosphorus annealing has become very popular as it can increase the mobility to more than 80 $cm^2/V.s$[42]. This has been linked to lower traps

density that resulting with Phosphorus passivation. The detailed discussion on these methods will be presented in chapter 5.

2-3 Time Dependent Dielectric Breakdown

The high electric field on oxide in addition to temperature results in another issue that has been coined: Time dependent dielectric breakdown (TDDB) in SiC devices.

[44] studies TDDB measurement at various temperatures and electric fields and suggest a lifetime of 10 years at 375°C if the oxide electric field is kept below 4.6 MV/cm. Bernstein [45] suggests that the existence of different failure mechanism under low and high electric field and studies the lifetime in the range of high and low field electric field condition, taking into account temperature acceleration, area and failure rate in a SiC MOS device, and concludes that the TDDB breakdown SiC/SiO_2 interface is only limited by the quality of oxide interface not the intrinsic properties of the SiC. A life time of 10 years is suggested for gate electric field less than 4.6 MV/cm for a temperature of 150 °C. For temperatures around 250 °C, maximum electric field strength of 2.9 MV/cm is suggested for a 10 years lifetime.

[46] measured the constant voltage TDDB for different 4H-SiC MOS capacitors and suggest lifetimes of 10^{10} hours at 3 MV/cm at the temperatures of 175°C. [47] has suggested lifetime of 10 years for oxide electric fields of 3 MV/cm at a temperature of 170 °C for a constant gate voltage of 20V.

2-4 Threshold Voltage Shift

High temperature gate bias (HTGB) stress test on SiC MOS devices [48] shows that when a device is heated up to the maximum allowable temperature for long period , even though the gate survive the test but there is an increase in threshold voltage of the device. Also the results from high temperature gate switching, similar to a real situation, shows that there is a shift in threshold voltage with time. The results of a 1200V MOSFET shows that the threshold voltage shift of about o.25 V in 800 hours.

Some researchers [49][50][51] suggest that the cause of this voltage shift is attributed to the channel electron trapped at the interface. Interface trap charges, oxide trap charges and fixed charges reduce the mobility and in consequence increase the threshold voltage and therefore they all need to be improved to achieve threshold voltage stability [49]. Solution such as NO annealing can improve the threshold voltage shift up to three times [25] as well as the channel mobility.

2-5 Conclusion

The common problems in designing and fabrication of 4H-SiC trench MOSFETs were issued. From the results in this chapter, it was decided that the work on the first generation of trench MOSFETs in Warwick University should be to focus on the quality of the interface and not improving the breakdown voltage. Quality of oxide and the interface in trench MOSFETs is the main issue in designing reliable SiC trench MOSFETs.

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Chapter

3 Design and Simulation of 4H-SiC trench MOSFET

3 Introduction

The ultimate goal of this project is to contribute to fabrication of 10kV 4H-SiC trench MOSFET, therefore in the first section (2.1), design and simulation of 10kV trench MOSFET is presented. In the next section (2.2) simulation of 1.2kV 4H-SiC trench MOSFET that is fabricated during this work could be found. All simulations have been done in Silvaco software [1].

3.1 Design of a10 kV Trench MOSFET Ideal Structure

All the equations used to design the structure of 10kV and 1.2 kV trench MOSFETs, are based on Baliga's theories [2].

3.1.1 Drift region Design

Doping and thickness of the structure is calculated based on Baliga's equations where doping (N_D) and thickness of drift region is chosen based on the following equations:

$$BV_{pp}(4H-SiC) = 3x10^{15}{N_D}^{-3/4} \quad \text{(Equation 3.1)}$$

$$W_{pp}(4H-SiC) = 1.82x10^{11}{N_D}^{-7/8} \quad \text{(Equation 3.2)}$$

The doping is chosen based on the parallel plane breakdown voltage (BV_{pp}), and the thickness is the corresponding maximum parallel plane depletion width (W_{pp}) given in equation 2. The resulting electric field (E_c) is calculated based on equation 3:

$$E_c(4H-SiC) = 3.3x10^{4}{N_D}^{1/8} \quad \text{(Equation 3.3)}$$

Figure 3.1 and 3.2 show the doping and thickness based on parallel plane junction breakdown voltage. There is a 20% added to the breakdown voltage value in this project. This is due to the fact that the value of breakdown voltage calculated based using Baliga's equations can result in 20% smaller value in

comparison to Fulop's power law [2]. Therefore, to add a safety margin we have added 20% to the required breakdown voltage and targeted breakdown voltage of 12.5 KV in our calculations. Using this equations doping of $1.5\text{x}10^{15} cm^{-3}$

And thickness of 100 µm is chosen for 10kV 4H-SiC trench MOSFET.

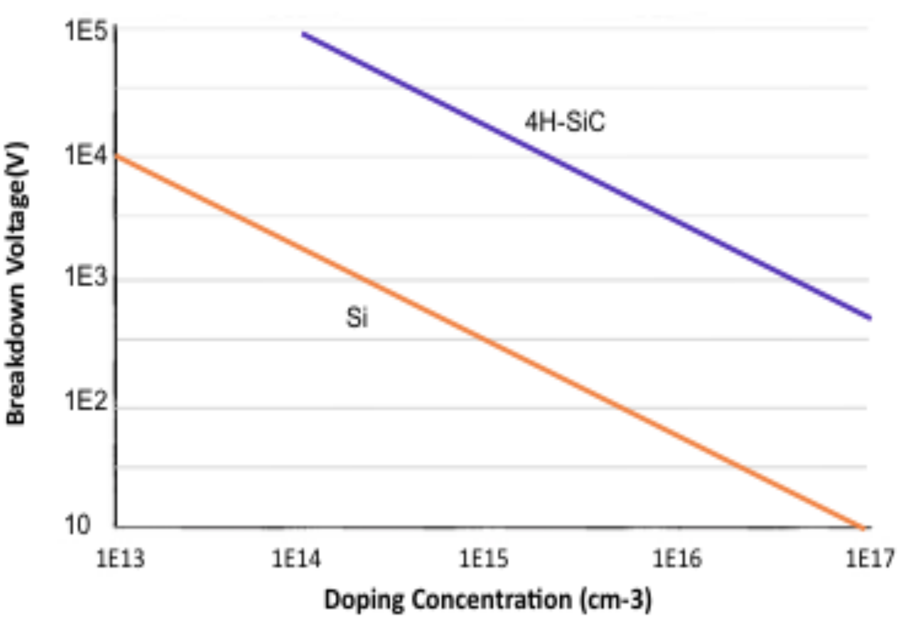


Figure 3.1: Breakdown voltage for Abrupt Parallel Plane Junction [2]

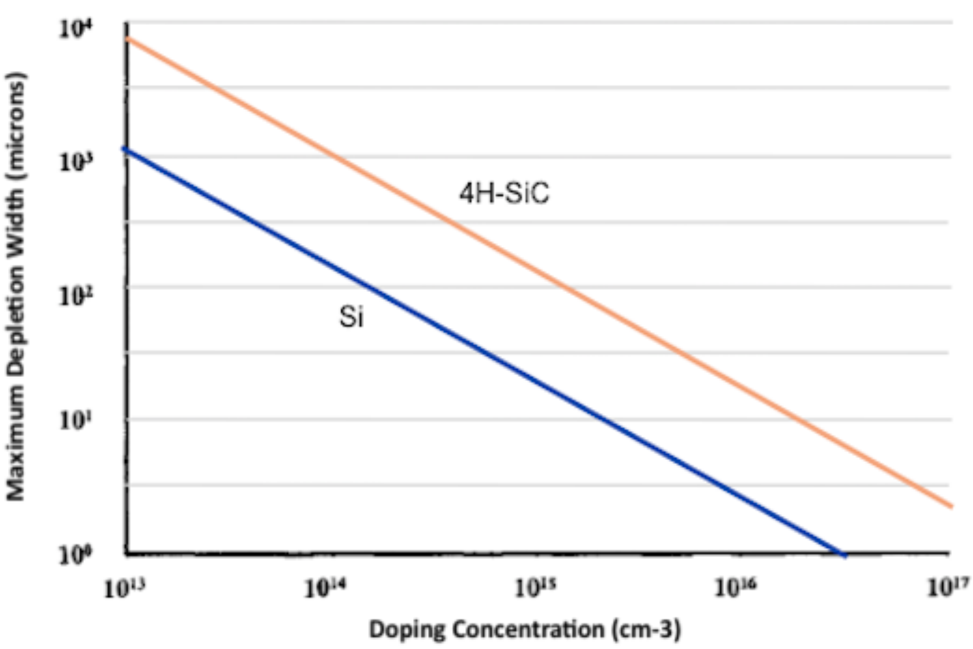


Figure 3.2: Maximum Depletion Width at Breakdown in Si and SiC[2]

3.1.2 P-body Design

The doping and thickness of the P-body region should be carefully chosen. The doping of the P-body affects the threshold voltage significantly. The results of the simulation is listed in Table 3.1. It is important to achieve low threshold voltage and hence lower doping is recommended.

P-body doping	1x$10^{17} cm^{-3}$	3x$10^{17} cm^{-3}$	5x$10^{17} cm^{-3}$
Threshold Voltage	7.619 V	12.932 V	14.186 V

Table 3.1: Effect of the P-doping on the threshold voltage

The P-body thickness was kept to minimum to reduce the channel length and hence the on-resistance [2]. Though it is very important to make sure the thickness is chosen carefully to avoid reduction in breakdown voltage. During the blocking mode, the electric field is extended into the P-body region due to the creation of depletion region. If the thickness of this region was less than the depletion region width in the P-body, the depletion region will reach the N+ source and hence the N+ source and P-body will be short circuited. This will results in lower breakdown voltage.

The depletion width in P-body for different P-body doping is shown in Figure 3.3. As can be see the depletion width in the P-body depend on the doping in both P-body and the N- drift region. For the calculated drift region doping of 1.5x$10^{15} cm^{-3}$ and P-body doping of 1x$10^{17} cm^{-3}$, the resulting depletion width of 1.7 µm is achieved. A 0.2 µm safety margin was added to to the P-body thickness in the simulations in this work.

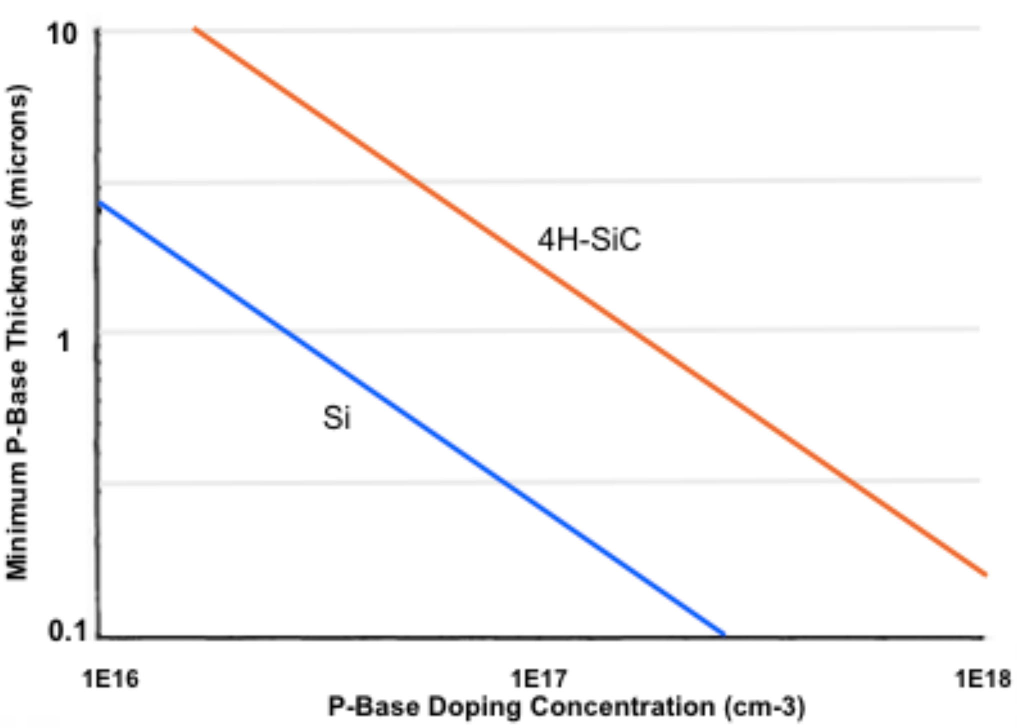


Figure 3.3: Depletion layer width inside the P-body region in Si and 4H-SiC [2]

3.1.3 Other Parameters

To design the ideal trench MOSFET, we need to achieve low threshold voltage. Threshold voltage could be calculated using the following equation:

$$V_{Th} = \frac{\sqrt{4\varepsilon_S kTN_A In(N_A/n_i)}}{C_{ox}} + \frac{2kT}{q} In(\frac{N_A}{n_i}) \qquad \text{(Equation 3.4)}$$

Where N_A is the doping concentration of the P-body, k is Boltzmann's constant, T is the absolute temperature, C_{ox} is the specific capacitance of the gate oxide, ε_S is the dielectric constant of the semiconductor, N_A is the doping concentration in the P- body region.

This equation results in the Figure 3.4, for an oxide layer with thickness of 0.05 μm. Based on this equation we can expect the threshold voltage of around 8V for a 10kV trench MOSFET.

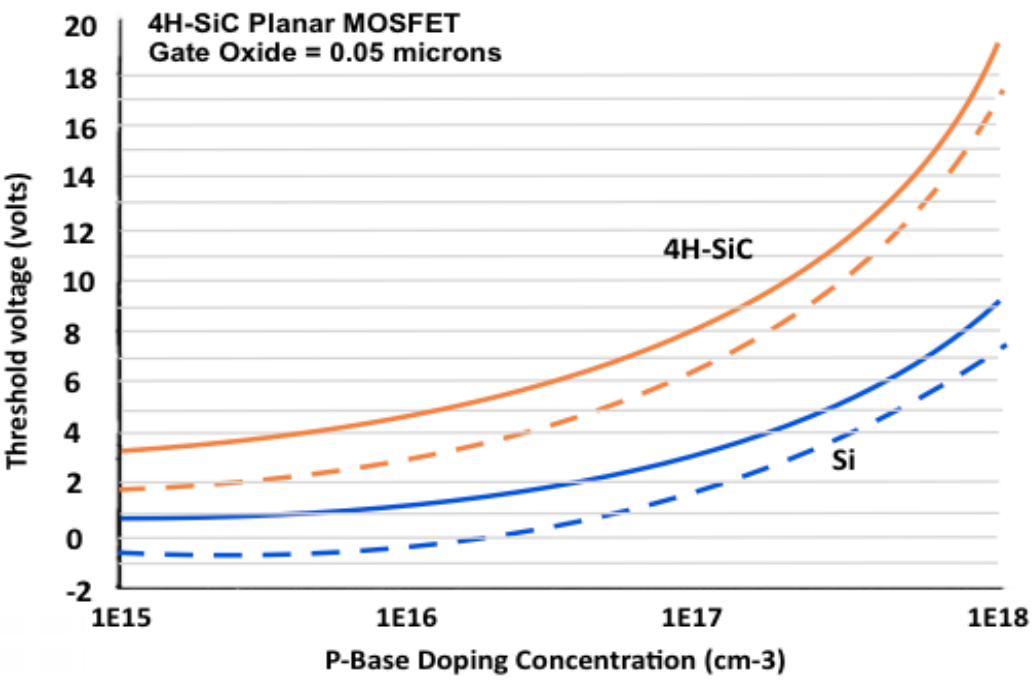


Figure 3.4: Threshold voltage of 4H-SiC MOSFETs (dashed lines represent the use N+ polysilicon gate and an oxide fixed charge of 2x$10^{11} cm^{-2}$)[2]

3.1.4 Ideal Structure of 10kV, 4H-SiC Trench MOSFET

The dopings of different regions of the 10kV trench MOSFET are listed in the Table 3.2. The thickness are shown in the Figure 3.5. The doping and thickness of the source and substrate(drain) are chosen following the industry standards[2]. These parameters were used to simulate the first model. A fixed

value of traps density($9 \times 10^{11} cm^{-2} eV^{-1}$) was used in all these simulation which is close to the best results achieved in the literature review.

Region	N+ source	P- body	N- Drift	N+ substrate (drain)
Doping	$1x10^{19} cm^{-3}$	$1x10^{17} cm^{-3}$	$1.5x10^{15} cm^{-3}$	$1x10^{19} cm^{-3}$

Table 3.2: Regional doping concentration of ideal 10kV SiC trench MOSFET

The ideal structure of 10kV, 4H-SiC trench MOSFET is shown in Figure 3.5. This structure contains a lightly doped drift region with 100 µm thickness, a substrate (drain) with 1 µm thickness and P-body of 1.9 µm.

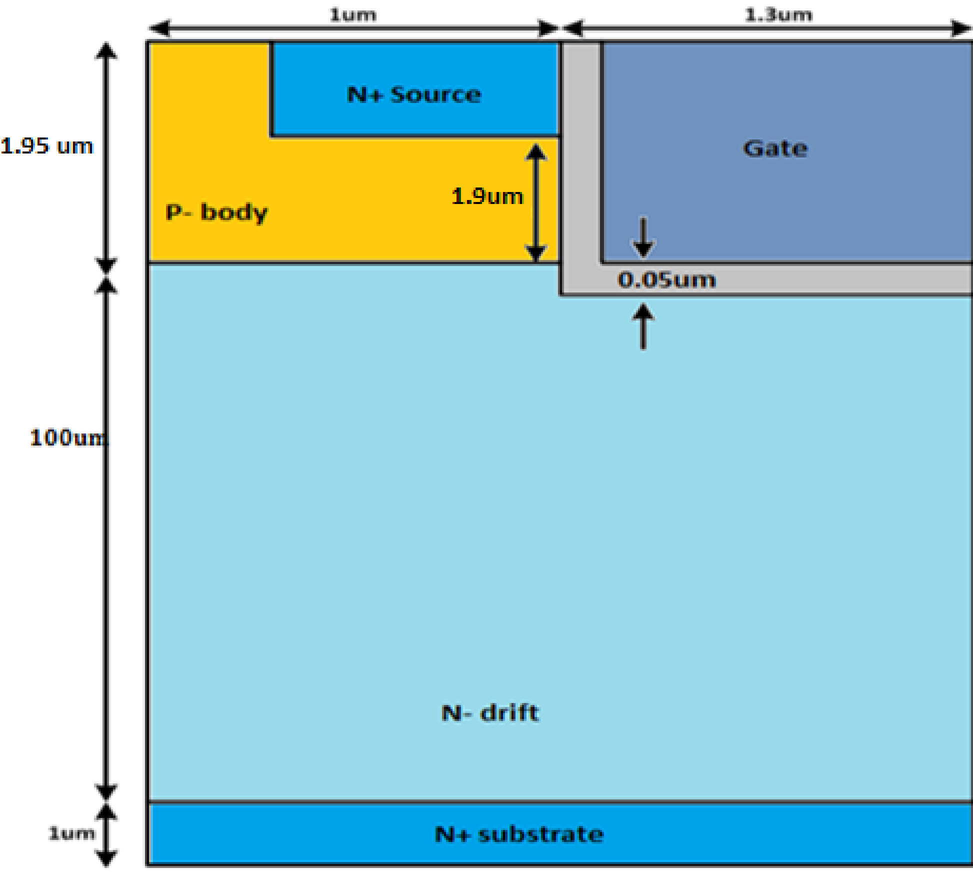


Figure 3.5: Ideal structure of 4H-SC 10kV trench MOSFET (um=μm)

Simulation results of this structure have demonstrated a breakdown voltage of 4.5 kV without any junction termination. Since in the off-state, no voltage is applied to the gate, the electric field in the insulator increases to a value more than in the on-state. Since the electric field across the insulator is about 2.5 times the SiC electric field, therefore it is important to minimize the oxide electric field so that it is less than the critical value. Figure 3.6 shows that the value of the maximum electric field in the SiC drift region and on the oxide layer.

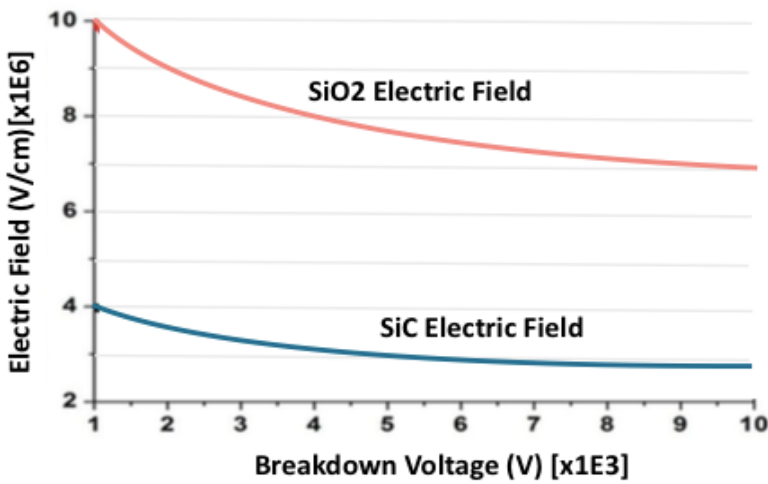


Figure 3.6: Electric field on gate oxide and SiC drift region as a function of breakdown voltage for fixed drift thickness and different doping concentration of drift region

As discussed in the previous chapter, in an ideal structure without gate protection, the performance of the structure is limited by the oxide breakdown and hence the breakdown occurs at 4.5 kV, when the electric field in the insulator bottom and corner has increased to a value more than the critical electric field of SiO_2.This is shown in Figure 3.7, where the potential inside the insulator layer has increased to more than zero. As can be seen the breakdown point is the corner of the trench. Therefore the 10KV trench MOSFET structure would be limited to about 4.5 KV because of the gate oxide breakdown.

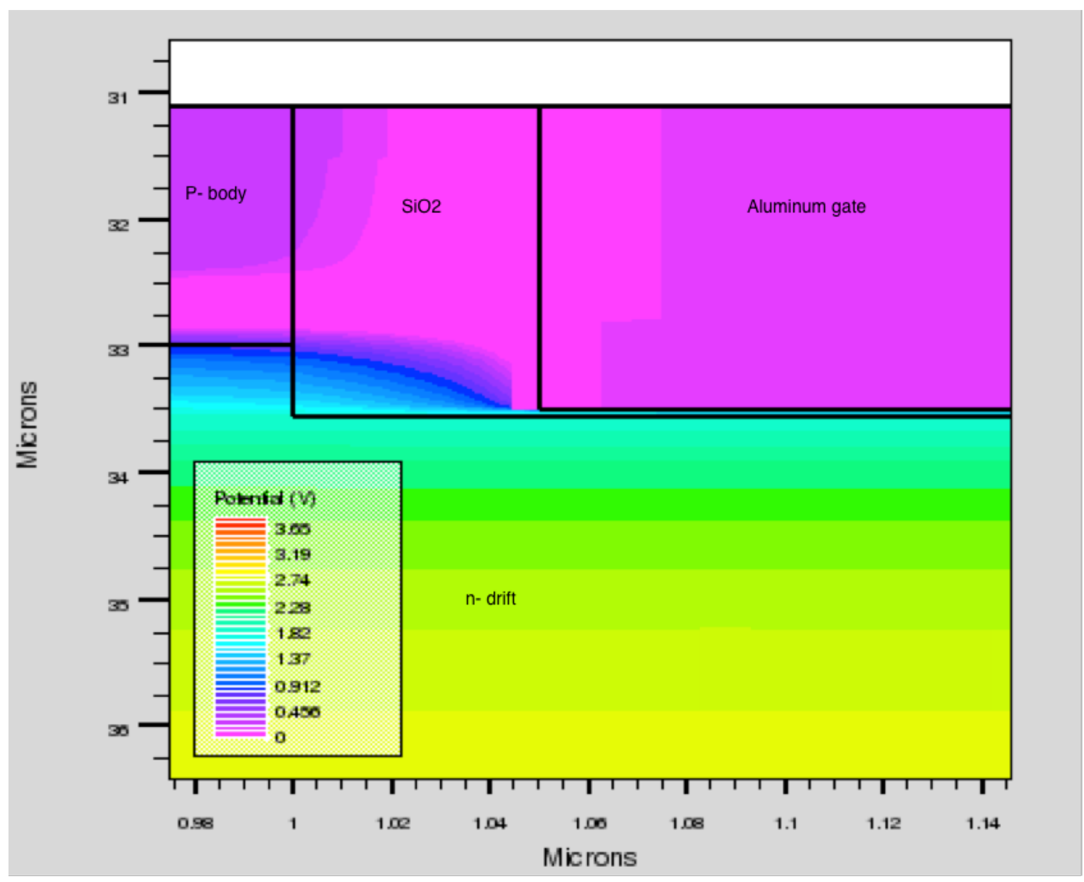


Figure 3.7: The potential distribution at breakdown for 100 µm drift region and doping of $1.5x10^{15} cm^{-3}$, the structure shows the potential across insulator has increased to a value more than zero.

The results clearly show that a solution is needed that prevent the breakdown in the oxide, so that the point of breakdown shifts the SiC. Next section present simulation of gate protection that is widely used in industry to avoid breakdown of oxide layers in SiC trench MOSFETs.

3.1.5 Gate Protection

In the previous section, it was demonstrated that careful consideration should be taken to avoid dielectric breakdown when designing a trench

MOSFET. The most common solution is to protect the gate insulator with a P+ shield instead of decreasing the drift region doping.

Figure 3.8 shows the potential and electric field distribution across the same structure with a gate protection. The gate shield has doping of $1x10^{19}cm^{-3}$. As can be seen there is zero potential across the gate and the maximum electric field has been shifted to the interface of shield/SiC.

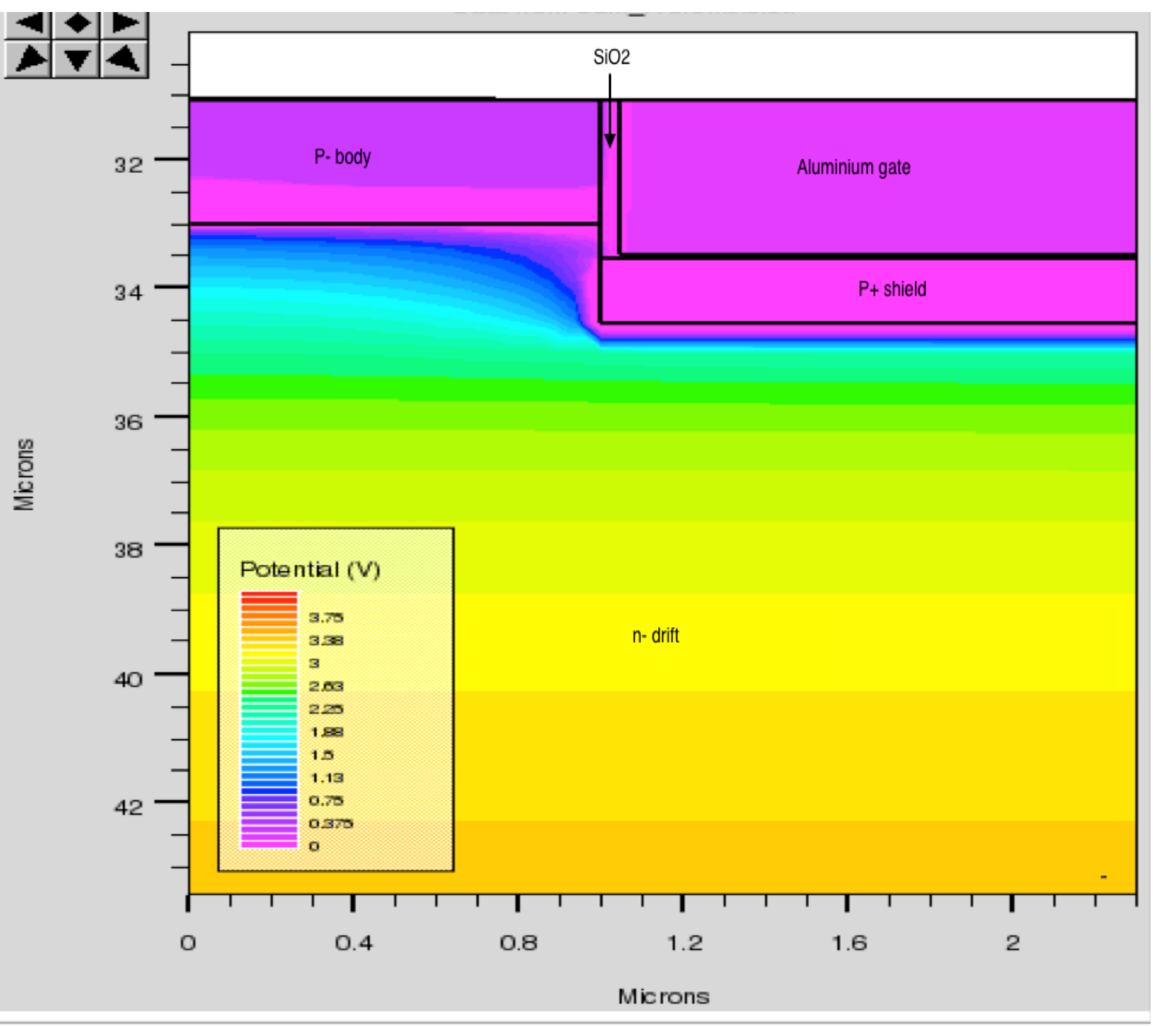


Figure 3.8: Potential distribution of shielded trench MOSFET with no gate voltage applied at 10KV for doping of $1.5\text{x}10^{15}cm^{-3}$ and thickness of 100 μm

The other advantage of P+ gate shield is that it prevents the punch through in the base region. In the conventional silicon carbide power MOSFET structure, the minimum P-base thickness and doping concentration are constrained by the reach-through limitation [2]. This does not occur in the silicon carbide shielded power MOSFET structure due to shielding of the P-base region from the drain potential by the P+ shielding region. This allows reducing the channel length to less than 1 μm. In addition, the doping concentration of the P-base region can

be reduced to achieve a desired threshold voltage without reach-through-induced breakdown. The smaller channel length and threshold voltage reduce the channel resistance.

The current-voltage characteristic of this trench MOSFET is shown in Figure 3.9. The breakdown voltage of this shielded trench MOSFET is 10.2 kV.

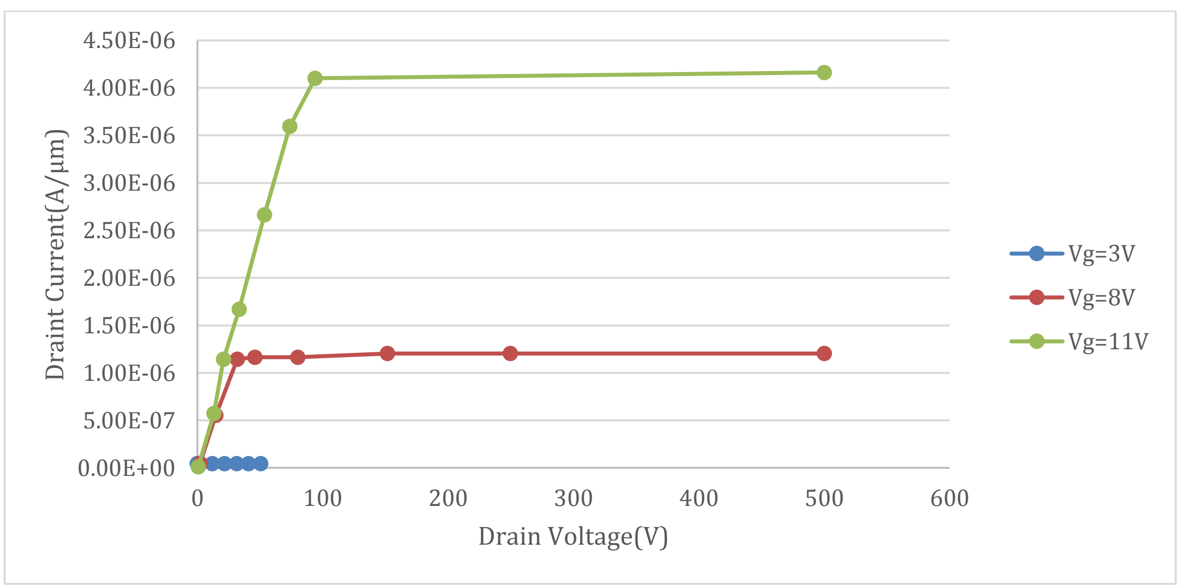


Figure 3.9: Forward Characteristics of 10kV trench MOSFET with gate shield

3.1.6 Threshold Voltage

Threshold voltage of a trench MOSFET is determined by the P-body doping and channel mobility, although the result of simulation listed in table 3.4 demonstrated that the gate thickness also slightly affects the value of threshold

voltage. To achieve low threshold voltage, P-body doping and oxide thickness needs to be kept to minimum. From the results listed in tables 3.3 and 3.4, the P- body doping of $1 \times 10^{17}\ cm^{-3}$ and gate oxide thickness of 0.05 µm was chosen for the first generation trench MOSFET.

P-body doping (cm^{-3})	1×10^{17}	3×10^{17}	5×10^{17}
Threshold Voltage(V)	7.619	12.932	14.186

Table 3.3: Effect of P-doping achieved from simulation of 4H-SiC trench MOSFET

Gate Oxide Thickness	0.05 µm	0.07 µm	1 µm
Threshold Voltage	7.619V	9.56V	12.1V

Table 3.4: Effect of gate dielectric thickness for P-body doping of $1 \times 10^{17} cm^{-3}$ achieved from simulation of 4H-SiC trench MOSFET

3.2 1.2 kV Trench MOSFET

A lower voltage trench MOSFET was fabricated in this project. The main reason for this decision was that all the experiments and results achieved using

a lower voltage trench MOSFET could be applied to a 10kV MOSFET without paying the high cost for a 4H-SiC wafer with 100-µm thicknesses.

The doping and thickness of this MOSFET are listed in Table 3.5. The goal was to design and fabricate a 1.2 kV trench MOSFET.

		Specification	**Unit**
Layer 1: n+ substrate (Drain)	Doping	$1.0x10^{19}$	cm^{-3}
n-type	Thickness	0.5	µm
Layer 2: n- drift	Doping	$9.42\ x10^{15}$	cm^{-3}
n- type	Thickness	15	µm
Layer 3: P- body	Doping	$1.0\ x10^{17}$	cm^{-3}
P- type	Thickness	2.1	µm

Table 3.5: Properties of 1.2 kV MOSFET

Since this was the first attempt of making any trench device in our research group, instead of creating an ideal device (smaller device with higher number of trenches to reduce on-resistance and increase current density), the focus was on fabricating trenches and then proving that the trenches can be used in a trench device. One other reason that prevented us from fabricating an ideal device was the limitation imposed by the machinery, mainly the resolution of photolithography mask aligner. Patterns and distance between patterns that were less than 4 µm were not clear using the microscope on the mask aligner

and hence the masks have to be re-ordered to make sure the boarders of the patterns are at least 4 μm from each other to avoid any error in fabrication that can be caused by high resolutions (example is short-circuiting source and gate contacts). The focus was of this work was on fabricating the first generation of trench devices that are working properly and improve on them in future.

The structure of trench MOSFETs that were fabricated during this work is shown in Figure 3.10.

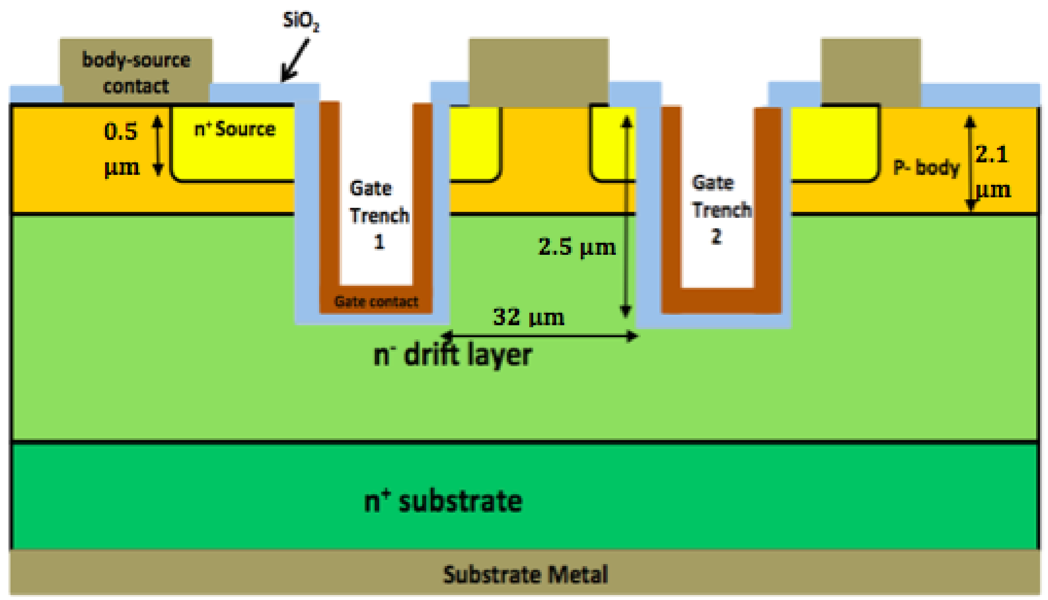


Figure 3.10: Structure of 1.2 kV trench MOSFET (without junction termination) that was fabricated in this project

The simulation results show that this 4H-SiC trench MOSFET has breakdown voltage of around 350-400 V (depending on the resolution of the simulation) without any gate protection or junction termination.

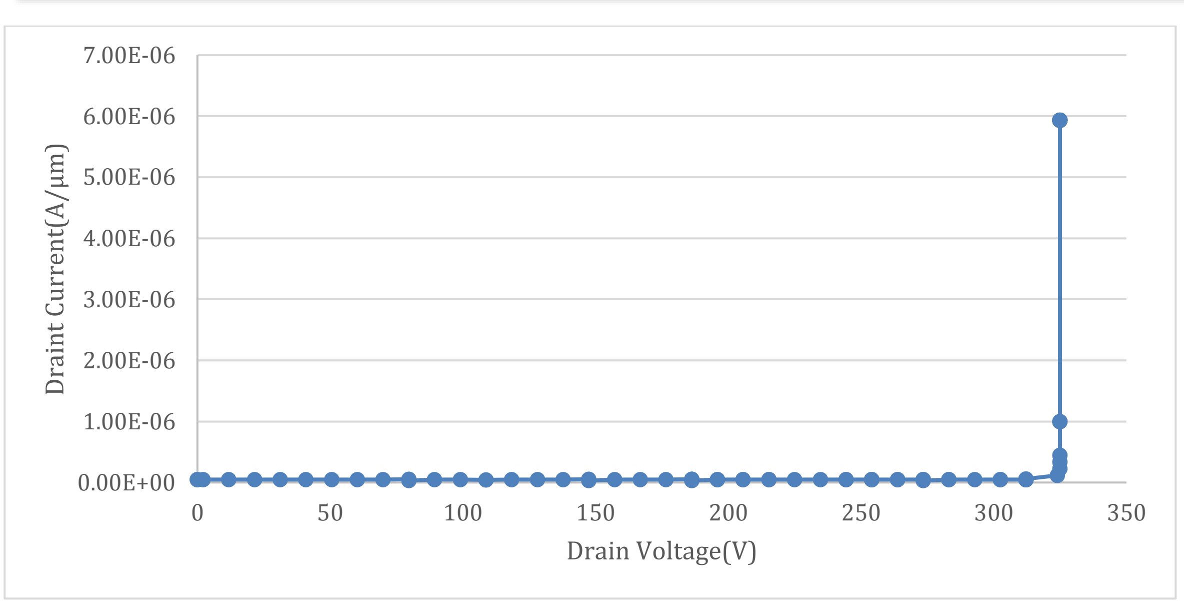


Figure 3.11: Simulation results of the breakdown voltage of 1.2 KV trench MOSFET fabricated in this project.

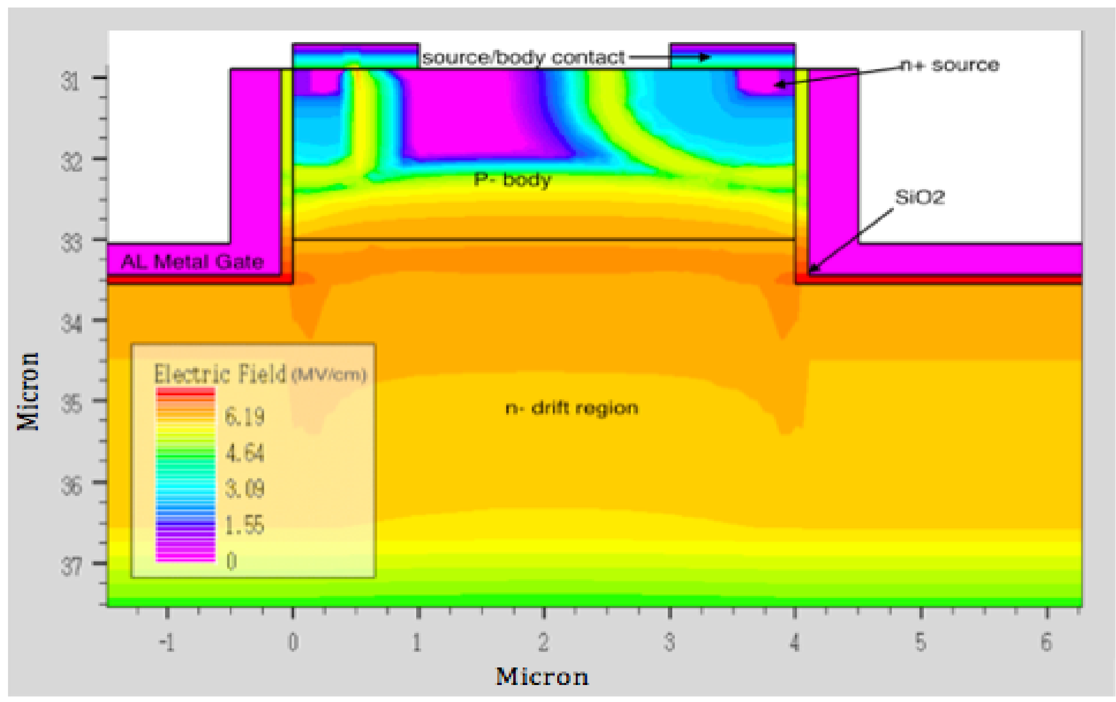


Figure 3.12: Breakdown happens in the oxide layer at the corner of trenches in devices without gate protection

As this is the first generation of trench MOSFETs in science city group, we have not focused on increasing breakdown voltage. The focus is rather on achieving a functional device with acceptable electrical measurements such as current, voltage, mobility and leakage current. In the last chapter (recommendation), alternative structures are introduced that can be used to increase the breakdown voltage of 1.2 kV trench MOSFETs. These suggestions could be used to improve the first generations MOSFET and achieve higher voltages in future.

3.3Double Trench Edge Termination

As it is shown in Figure 3.12, the trench corners seem to act as a point of attraction for the electric field. This behavior is similar to the P^- ring used as junction termination. This raises a question, "can trenches be used for the purpose of junction termination?" If this could be proved, trench junction termination could be used instead of implanted ring around the device. This will eliminate the need for implantation and high temperature activation of P^- rings.

For simplification, this theory is tested on a 4H-SiC Schottky diode first. This diode has an ideal breakdown voltage of 1.2 kV.

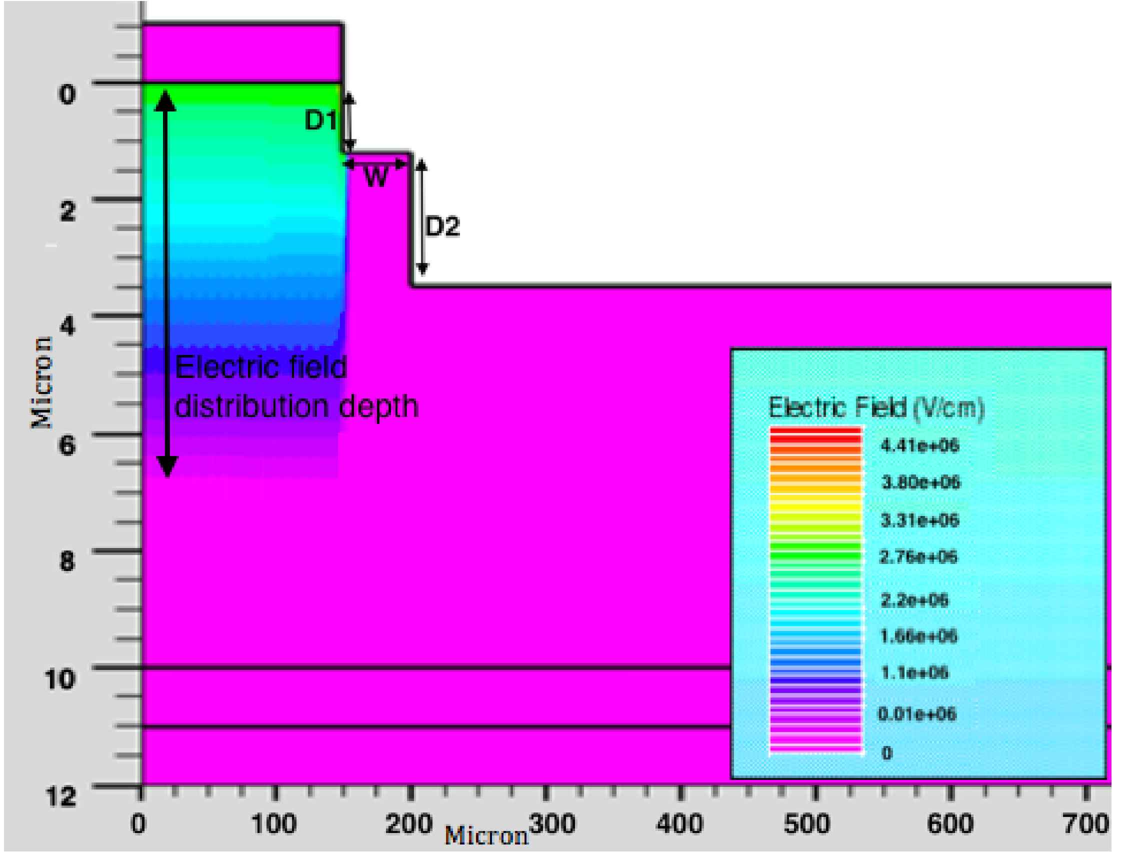


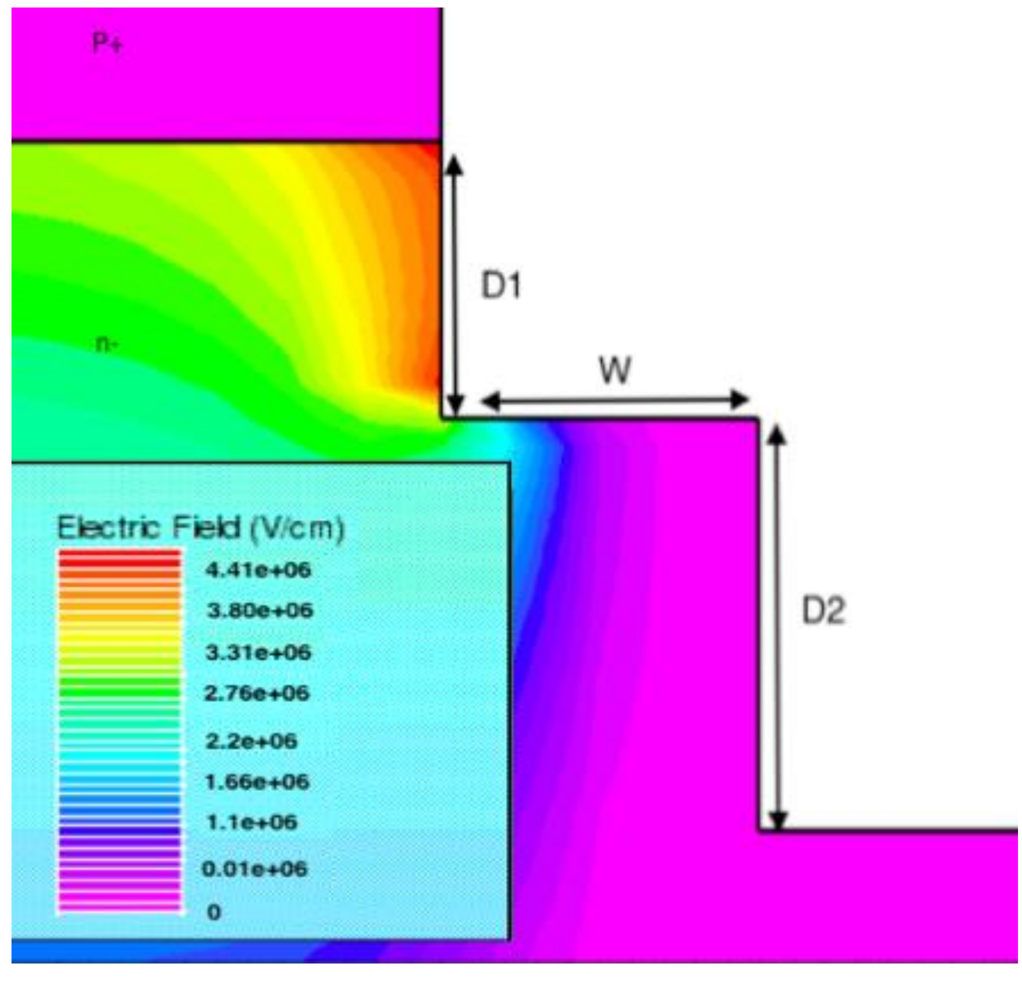
Figure 3.13: Schottky diode with double trench junction termination

From simulation results it can be seen unlike P-ring junction termination, where the electric field spreads horizontally, double trenches junction termination spreads the electrical field distribution mostly in Y-direction (Figure 3.13) and hence increases the breakdown voltage. The depth (D1, D2) and width of trenches (W) (shown in Figure 3.13) has to be carefully designed to achieve the highest breakdown voltage.

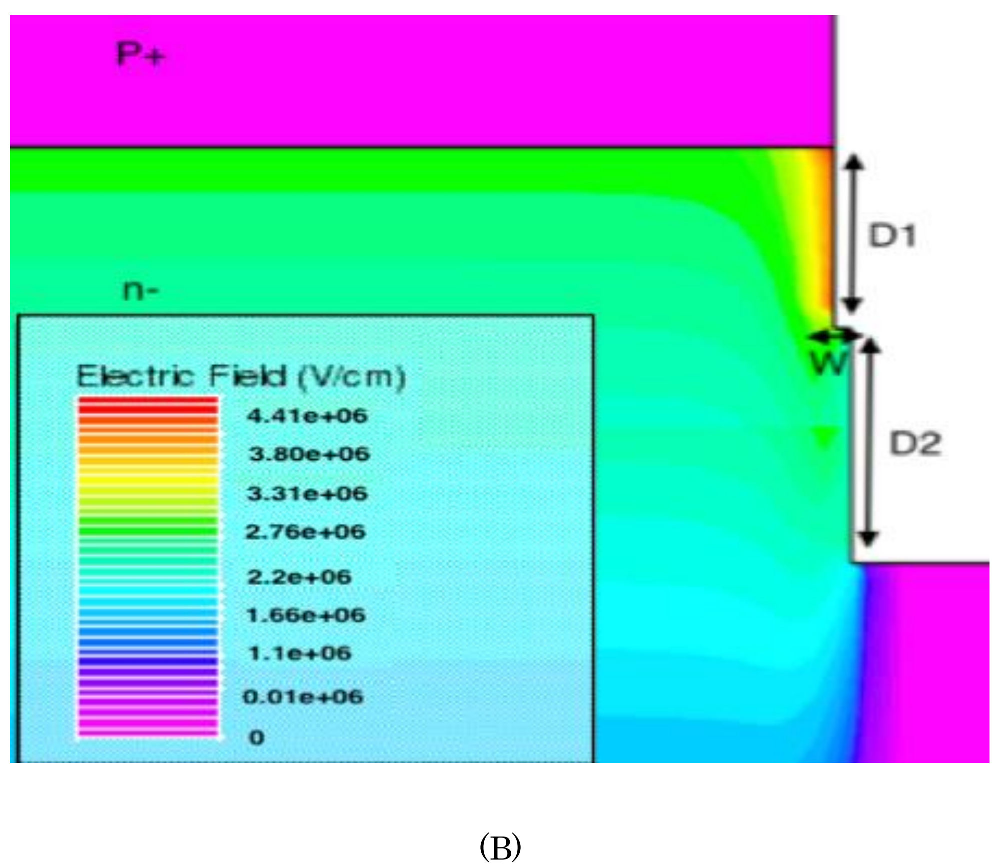
As can be seen in Figure 3.14A, when the width, W is more than 2.5 µm, the electrical field doesn't spread in the X-direction and does not reach the

second trench, but the second trench still helps to spread the electrical field in Y-direction.

Changing width, while D1 and D2 are constant shows that, smaller W results in higher breakdown voltage by spreading the electrical field further downward (Figure 3.14B).



(A)



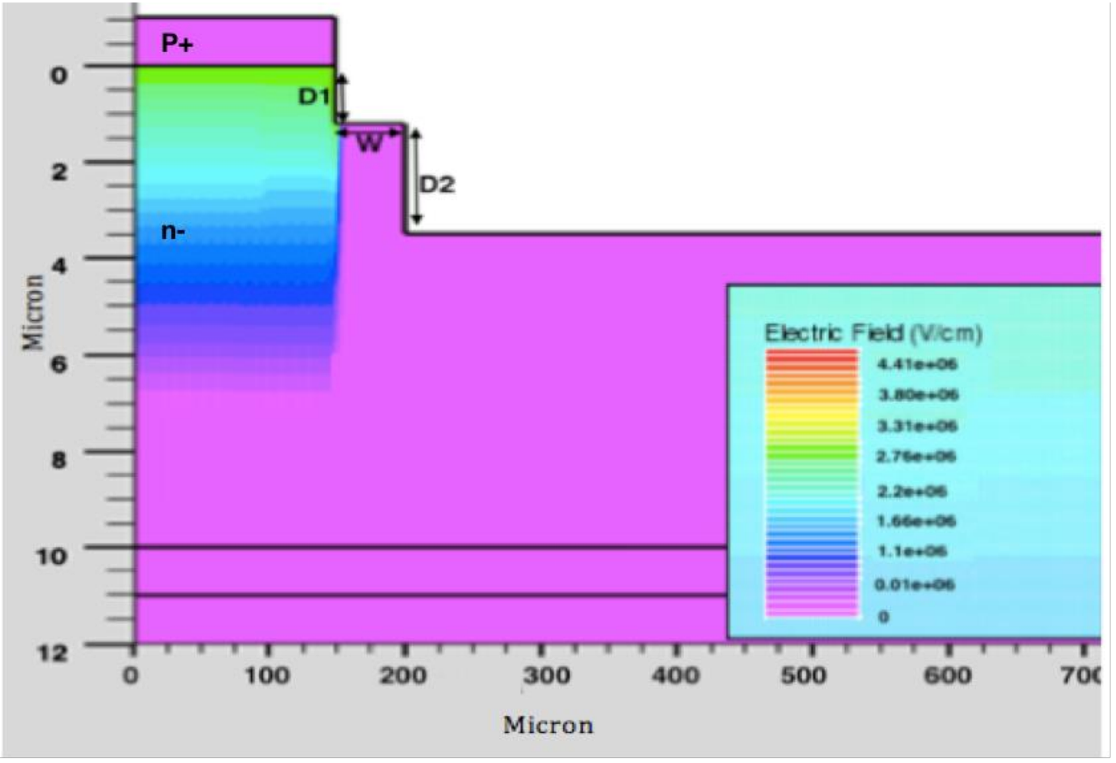
(B)

Figure 3.14: Effect of Width on the electrical field distribution D1=1.4 μm and D2=3.5 μm are kept constant (a) W=5μm (b) W=2.5 μm

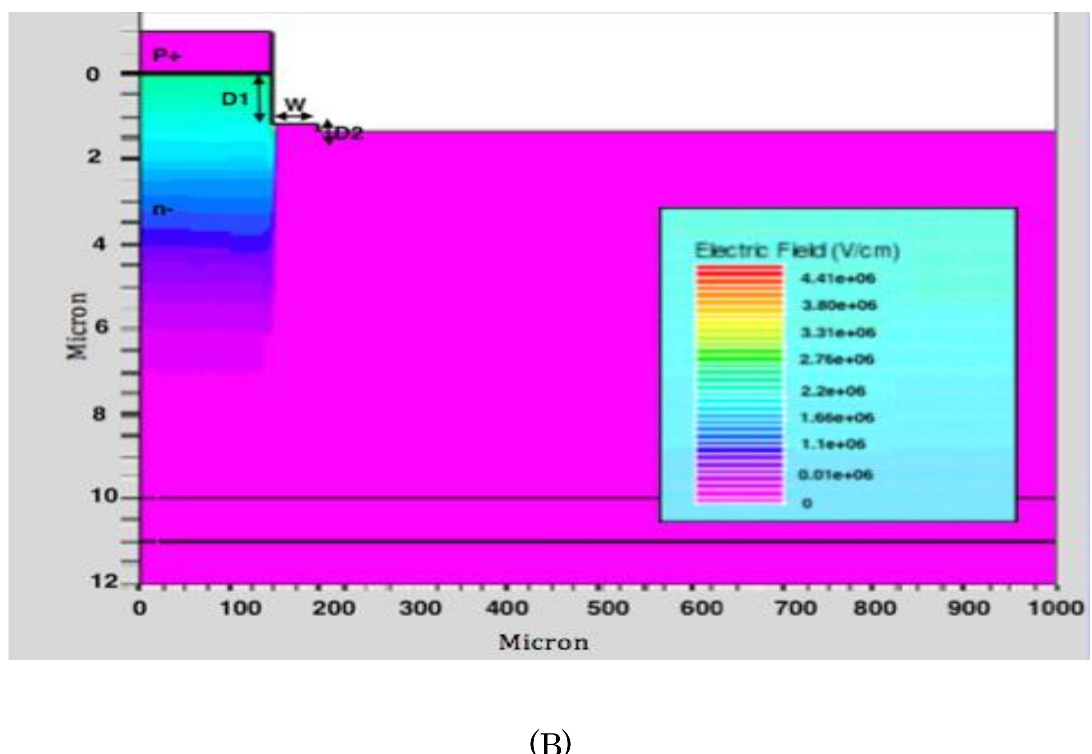
This can be explained by the fact that when width is smaller the second trench can affect the distribution of electric field more. In fact in best breakdown voltage (1000V) is achieved for the case where W is so small the electrical field has expanded to the second trench as well (Figure 3.14B), and hence the electric field distribution is both horizontally and vertically.

This also proves that to make sure the electric field is distributed between trenches we need to etch them at least 2.5 μm from each other. This result can be used in future to design the second generation of trench MOSFETs in science city group.

The results of simulation also show that when the width is 50μm, at which the electrical field doesn't spread to the second trench wall, and depth of the first trench, D1 is kept constant, by changing the depth of the second trench, D2, the breakdown voltage changes. Increasing D2 from 1.35 μm to 3.5 μm while keeping D1 at 1um and W at 50 um, the breakdown voltage changes from 700V to 850V by spreading the electrical field further in Y-direction.



(A)



(B)

Figure 3.15: Effect of changing depth of second trench, D2, on electrical field distribution while keeping W and D1 constant, D1=1 µm, W=50 µm, (a) D2=3.5 µm (b) D2=1.35 µm

This means that the second trench can help to spread the electric field in the Y-direction regardless of if the electrical field reaches the second trench wall in X-direction or not (Figure 3.15).

The point of breakdown in all cases is the wall of the first trench. There seems to be an optimum depth for D1 and D2, if they are increased or decreased after this point the break down voltage decreases. The best value of D1 for this device seems to be 2.5 µm and for D2 is 3.5 µm.

D1 (µm)	D2 (µm)	W1 (µm)	Breakdown voltage (V)	Electric Field Depth (µm)
0.5	*3.5*	*2*	867	5.2
1.4	*3.5*	*2*	867	5.2
2.5	*3.5*	*2*	1000	5.98
3	*3.5*	*2*	983	5.9
1.4	*2.5*	*2*	840	5.15
1.4	*1.35*	*2*	700	4.8
1.4	*0.35*	*2*	480	3.1
2.5	*3.5*	*50*	750	4.91
2.5	*4.5*	*2*	960	5.94
2.5	*1.5*	*2*	710	4.81

Table 3.6: Breakdown voltages achieved for different double trench junction termination on a Schottky diode with ideal breakdown voltage of 1.2 kV.

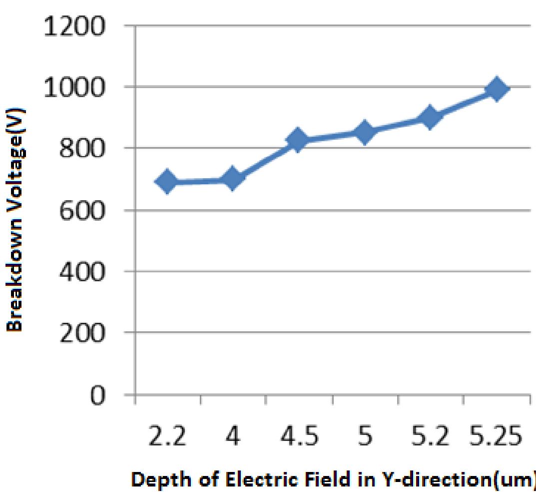


Figure 3.16: Breakdown voltage vs. the electric field distribution depth in Y-direction using double trench junction termination.

The maximum breakdown voltage of 1.0 kV was achieved using double trench junction termination. This is 80% of the ideal breakdown voltage.

The most common method of junction termination in power industry is mesa junction termination by ion implantation around the edge of device. This region can be a single implantation ring (Figure 3.17a) or more than one ring that is called space modulated junction termination extension(SMJTE) (Figure 3.17b). The implementation dosage, annealing temperature used to activate the implement and the distance between the rings (in case of Figure 3.17b) are the main factor that affect the breakdown voltage. There are other more complicated methods such as space modulated two zone junction termination (Figure 3.17d) that uses the same design as SMJTE but with two different implantation dosage(shown with light blue and dark blue color in Figure 3.17d) that is

reported to increase the breakdown voltage more than a single SMJTE design if the ratio of the JTE 1 and JTE 2 are kept to 3:2 [4][5]. The idea behind using implantation is that these regions become completely depleted close to the surface at voltages close to breakdown voltage and hence reduce the crowding of electric field in the edge. This process is highly dependent on the dosage and activation of the implanted region. A further study was carried out during this work with collaboration with another researcher from Warwick University to investigate the most efficient junction termination method for SiC power device [3]. In this study different methods of junction termination including single zone implant, SMJTE and space modulated two zone JTE were compared to two steps mesa JTE.

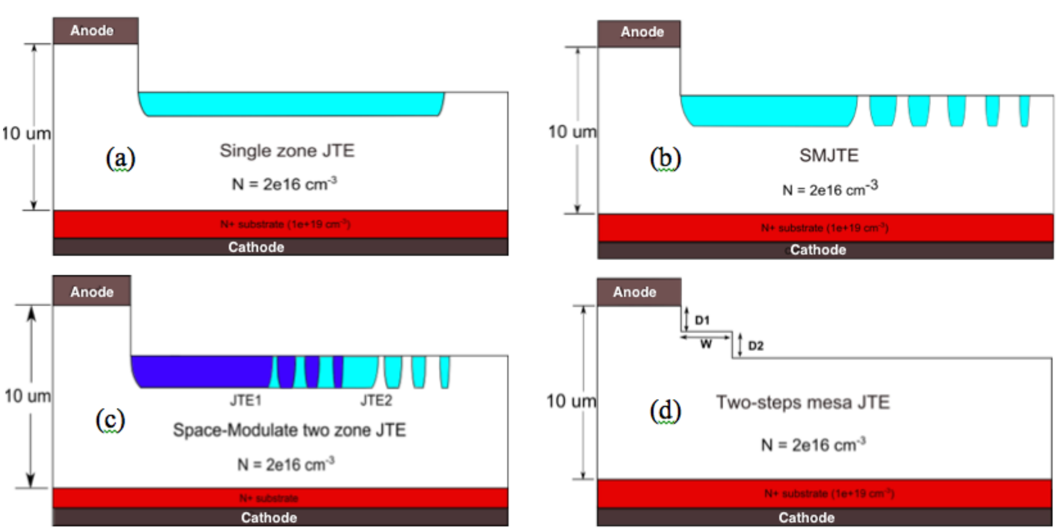


Figure 3.17: Schematics of different edge termination structures on Schottky diode [3]

The simulation results showed that two steps mesa JTE results in around 99% of the ideal breakdown voltage without the need for any implantation and

higher than the other methods shown in Figure 3.17. Combination of implantation and two steps mesa JTE did not improve the breakdown voltage any further, hence two steps mesa JTE method is suggested as the JTE solution for the next phase of this project. Further details on this JTE methods and results were published and could be found in the relative resource [3]. The fabrication process of trenches with high resolutions are discussed in this thesis in chapter 4 and the fabrication process and the optimised dosage of the implanted space modulated JTE(SMJTE) could be found in another project from Warwick University [4]. Simulation of two steps mesa JTE on a 1.2kV 4H-SiC MOSFET was carried out at the end of this project to find the optimised structure using this type of JTE. The results are presented in the last chapter of this thesis.

3.4 Conclusion

The results show that without a gate protection the breakdown voltage is limited by breakdown in oxide at the trench bottom. The results of simulation shows that without a gate protection and junction termination, a breakdown voltage of 350-400V is expected. The results also confirm that using the same structure and adding the gate shield will results in a 1.2kV trench MOSFET and hence the second generation MOSFET can use the same structure.

3.5References

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Chapter

4

Etching of 4H-Silicon Carbide (SiC) by Inductively Coupled Plasma Reactive Ion Etcher

4 Introduction

Due to the strength of the covalent bonds between silicon and carbon in Silicon Carbide (SiC), etching of SiC is a challenging process in the fabrication of trench MOSFETs. There are variety of etching techniques that can be exploited. However, wet etching is unsuitable for SiC as it is both slow and isotropic by nature (Figure 4.1A). In contrast, plasma dry etching is more applicable for the etching of SiC due to the high etch rate and anisotropic behaviour (Figure 4.1B).

Figure 4.1: Difference between (A) isotropic and (B) anisotropic etch

High-density plasma etcher including inductively coupled plasma (ICP), is the most common method used to etch SiC, because of its ease of tuning, fast etch rate and cost efficiency. This technique includes (a) generating ions (b) directing the ions toward the sample. The ions can etch the sample by chemical or physical reactions.

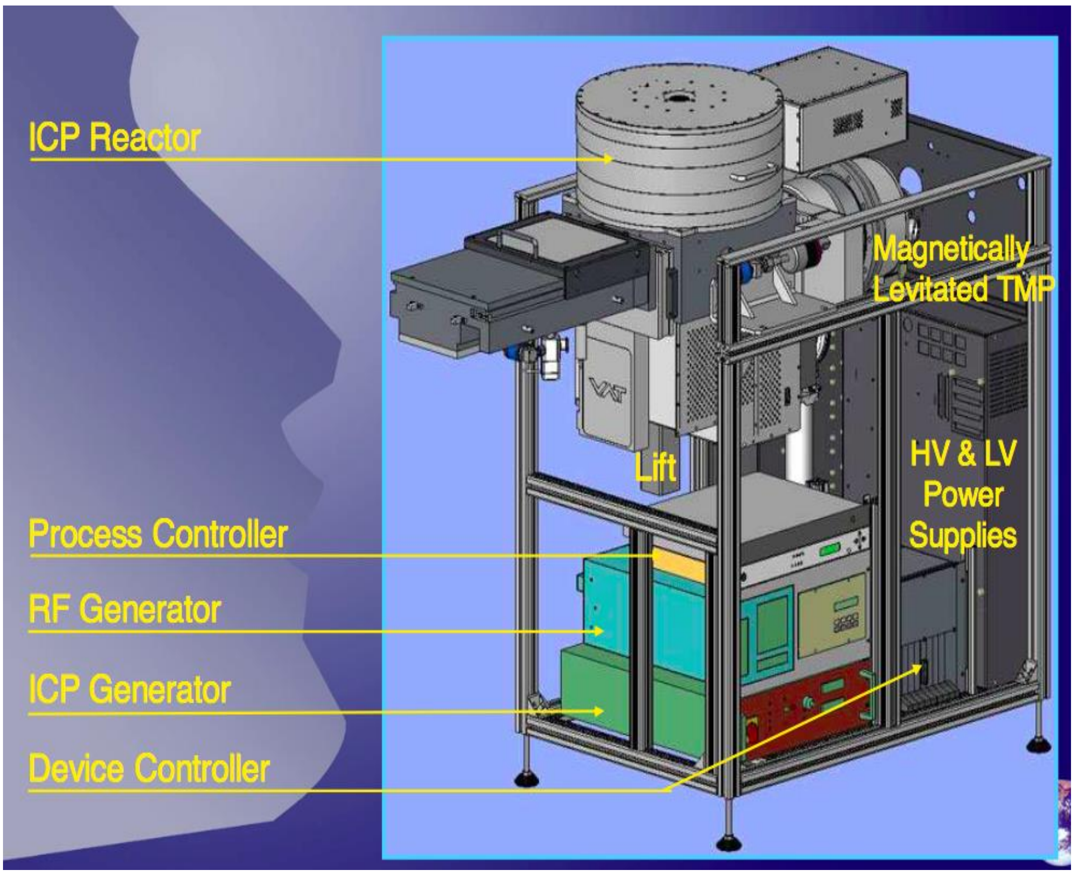


Figure 4.2: Illustration of Corial ICP-RIE etcher instrument [1]

A simple ICP-RIE etcher schematic is shown in Figure 4.2 and 4.3. To generate ions a time varying radio frequency voltage is applied to the coil (ICP generator).

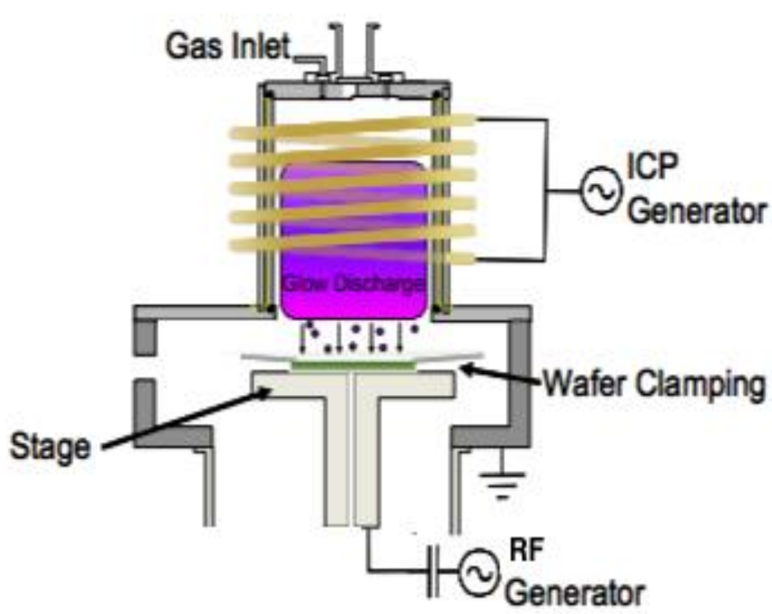


Figure 4.3: Inside ICP reactor in ICP-RIE etcher [2]

This coil is wrapped around the RIE discharge region called the glow discharge region (Figure 4.3). This results in a current that induces a magnetic field. The changing magnetic field induces an electric field equal to the Maxwell-Faraday equation. Maxwell-Faraday equation states that a time varying magnetic field will always accompany electric field and vice versa.

$$\nabla \times E = -\frac{\partial B}{\partial t}$$

Where E is the electric field and B is the magnetic field. The induced time varying electric field acts as a source of energy and helps to ionize the injected gas(es). The ionized gas is called plasma, which is combination of positive ions and free electrons. The initial ionized atoms and electrons are accelerated in this electric field and collide with the injected gas, hence further ions and electrons are generated.

As electrons are accelerated, they hit the chamber walls and wafer platter (shown in green color in Figure 4.3). Chamber walls are dielectric and feed the electrons to the ground. The electrons that are deposited on the wafer platter build up charge, which result in a negative voltage (RF DC bias voltage). The combination of this bias voltage and the other radio frequency source (RF generator) that is connected to the substrate stage build up a negative charge that attracts the positive ions toward the sample. These positive ions react with the material on the surface mainly through chemical reactions, although physical reactions can also occur through sputtering. This is commonly referred to as the milling effect.

Increasing the RF power connected to the substrate, increases the bias voltage and therefore the ions that hit the sample are more energetic. This can result in increasing milling aspect of the etching and if physical etching of a

sample is a high percentage, then increasing RF power can increase the etch rate noticeably.

The ICP power on the other hand controls plasma density. Raising the ICP power increases the induced electromagnetic field, which subsequently increases the ion density through amplifying the number of electron-gas collision. The degree of chemical etching is proportional to the number of ions reaching the sample. Due to the neutral charge of the plasma, the bias voltage remains unaffected by additional ions.

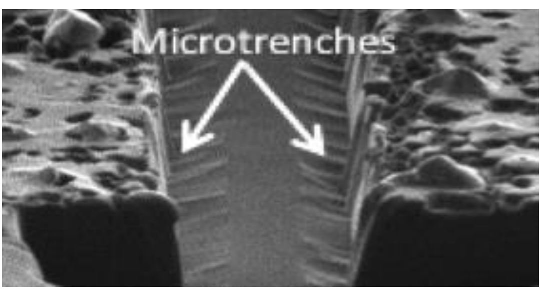
The presence of individual RF and ICP generators creates an efficient etching technique as it provides complete control over both ion density and ion incident energy. Moreover, an additional advantage of separate generators is the reduced milling effect due to the option to increase the ions densities that are less energetic.

The Corial 200IL Inductively Coupled Plasma (ICP) Reactive Ion Etching (RIE) instrument was used in this project.

4.1 Challenges in Fabricating Trenches in SiC

There are numerous challenges associated with dry etching of SiC including but not limited to microtrenches (Figure 4.4A), sidewall striation (Figure 4.4B) and roughness. Microtrenches or sharp corners induce the

crowding of electric field in the corner of trenches, thereby reducing the breakdown field. Striation in sidewall increases the leakage current through the gate oxide.



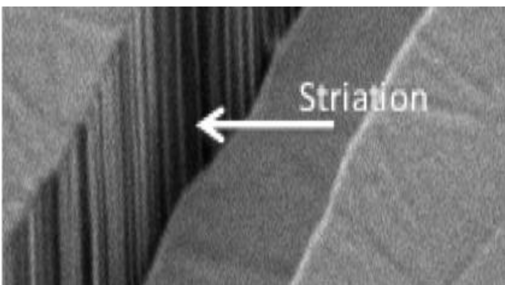


Figure 4.4: Common challenges in fabricating trenches in SiC: SEM images of (A) microtrenches: small trenches at the corner of the main trench, this can result in crowding the electric field and hence lower breakdown (B) striation is roughness of sidewall which can increase the leakage current

Our first attempts to etch trenches using literature studies [3][4], resulted in the same etching rate but different physical characteristics, such as existence of microtrenches and/or striation. Hence it was important to understand the origin of these two issues to be able to solve them.

4.1.1 Origin of Microtrenches

Microtrenches are small trenches that are formed in the corner of trenches (Figure 4.4A). The exact formation mechanism of microtrenches remains unclear but has been linked to ion reflection from the trench wall [5] and differential charging [5][6]. Figure 4.5 shows the mechanism of ion reflection from the sloped sidewall: ions that are closer to the sidewall are deflected when they reach the sloped sidewall.

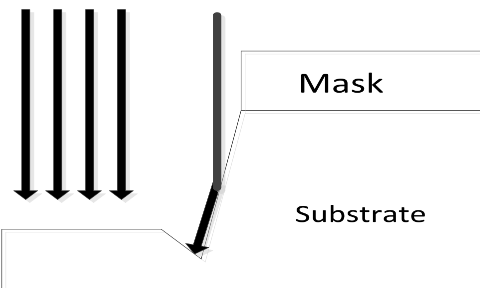


Figure 4.5: Schematic of first suggested cause of microtrenches: ion deflection due to sloped sidewall

On the other hand differential charging theory links the microtrenches to the difference in electrons and ions angular distribution. As electrons move isotropically, they tend to build up at the top opening corners of trenches, therefore even though ions move vertically; they are affected by the charge that is built up at the top corners and are deflected toward the sidewalls (Figure 4.6).

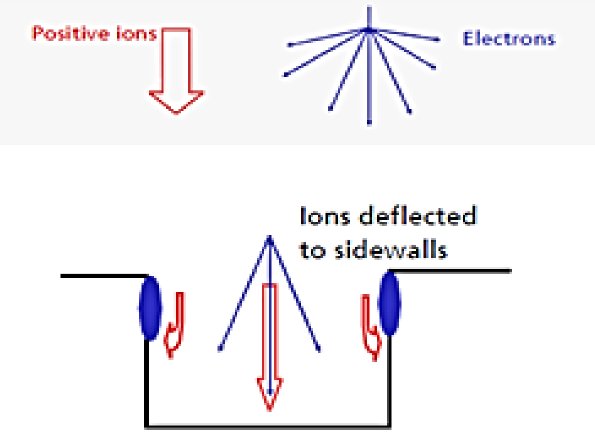


Figure 4.6: Schematic of microtrenches formation via differential charging effect based mechanism

To examine the source of microtrenches, SiC was etched using only Ar ions in metal beam evaporator in science city research group. This was to ensure the process was free from electrons charge. The result shown in Figure 4.7, confirms that in the absence of electron, there will be no microtrenches.

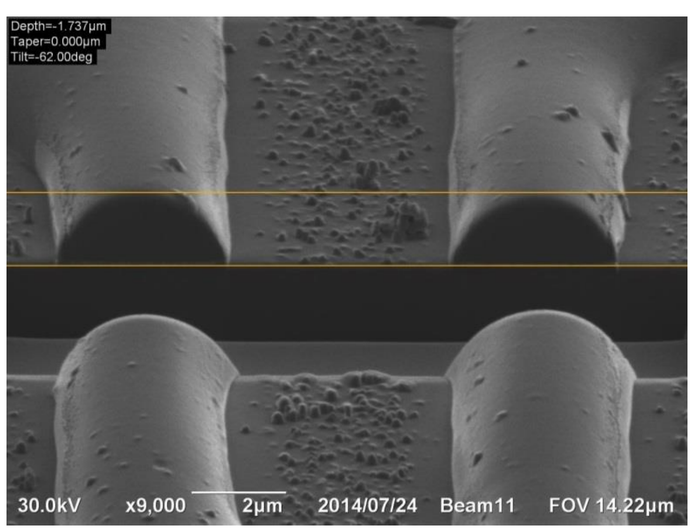


Figure 4.7: SEM image of Ar ion etching of SiC. This result confirms that in the absence of electron there will be no microtrenches.

This means that (a) the existence of electrons is the source of microtrenches, though if the exact reason behind creation of microtrenches is due to differential charging theory or not, could not be confirmed by this experiment (b) ion deflection from the sloped sidewall or ions scattering cannot cause microtrenches. As it is clear the sidewalls are almost 65°. So if ions deflection from sidewall was the cause of microtrenches, the results should have shown sever microtrenches. Also as there is no RF power in the metal evaporator to direct the ions toward the wafer holder in the metal beam evaporator, we expect more ions scattering. As can be seen this has caused much slopped

sidewall but there is no sign of microtrenches. This result also suggest that ions scattering might be the source of slopped trench sidewalls, but does not affect microtrenches.

During the first rounds of experiments, ICP-RIE etching of SiC using masks with different trench width (Figure 4.8), it was also evident that the lateral force on the ions that is directing them toward the trench corner, can only affect the ions in a very close distance to the sidewall.

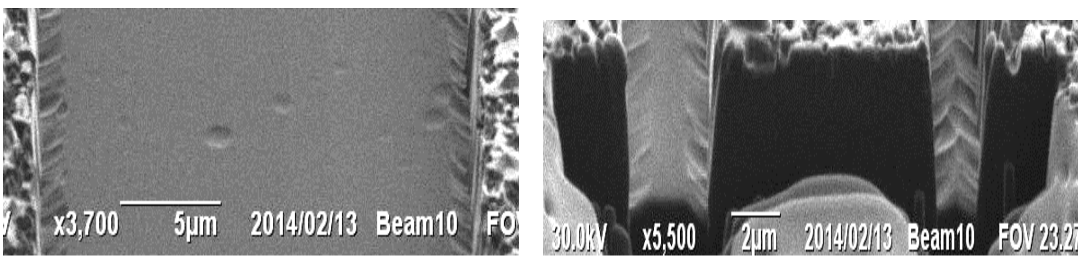


Figure 4.8: The results show that microtrenches sizes are equivalent for different trench width (SEM image)

Therefore, one way of removing the microtrenches can be to reduce the ions near the sidewalls. In this project, sidewall protection shadow was created to test this theory. The process and results are presented later in this chapter and the results prove that by creating side wall shadow, microtrenches could be completely eliminated.

Different mask materials including Ni and SiO_2 were also studied and the results show microtrenches do not depend on the mask material. This was done to make sure that charging of metal masks does not affect or cause

microtrenches. As will be presented in this chapter, even when SiO_2 was used as a mask, microtrenches were observed.

4.1.2 Origin of Striation

Striation or line edge roughness (LER) is the waviness on the trench sidewall as shown in Figure 4.9. During photolithography, the patterns on the mask are transferred to the photoresist layer. The solubility of photoresist changes depending on whether it is exposed to the UV light or not. This is the stage that striation was first observed on the photoresist patterns (Figure 4.9A). Striation was transferred to the etching mask and to SiC in the following steps (Figure 4.9B).

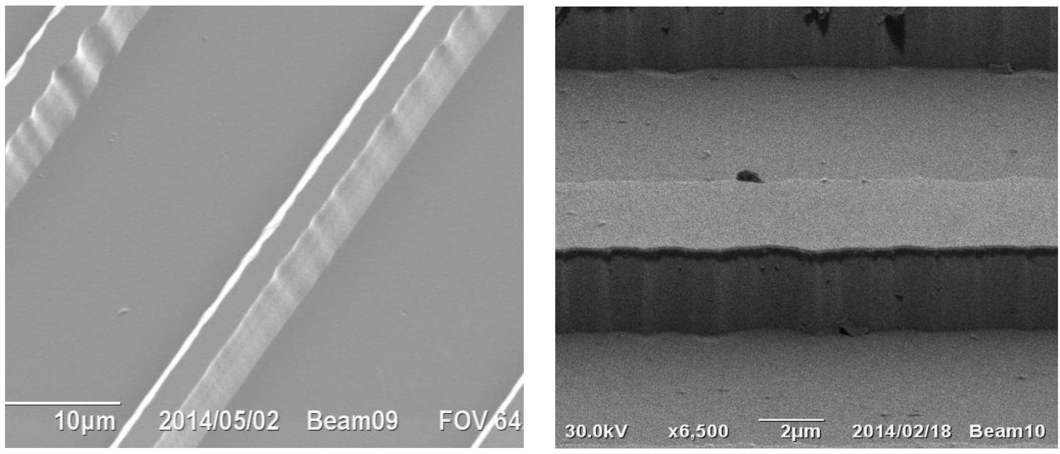


Figure 4.9: SEM images of (A) striation in photoresist before etching metal mask and SiC (B) after etching SiC, before removing metal mask (photoresist mask is removed)

There are different suggestions for the cause of striation in photoresist. Generally they are divided to two categories (1) photoresist quality (2) photolithography instrument and process.

Two factors that can affect striations in the photoresist, are thickness and sensitivity of the photoresist [7][8]. Higher sensitivity of photoresist corresponds to more photo-acid generator. Photo-acid generators are used for chemical amplification of photoresist. By amplification of photoresist, they will be more sensitive to the UV light exposure [9].

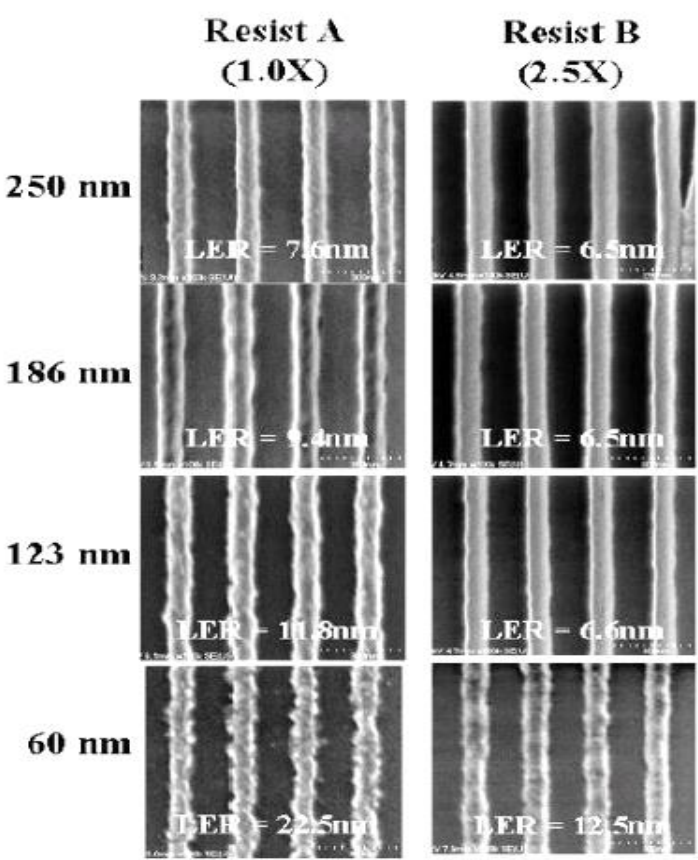


Figure 4.10: Effect of photoresist thickness and sensitivity on LER. Photoresist B is 2.5 times more sensitive [10]

Other source of striation that can be linked to photoresist is intrinsic non-uniformities in photoresist. Different sizes in the polymer chains of photoresist

can results in developing/under-developing along the edge of the photoresist [11].

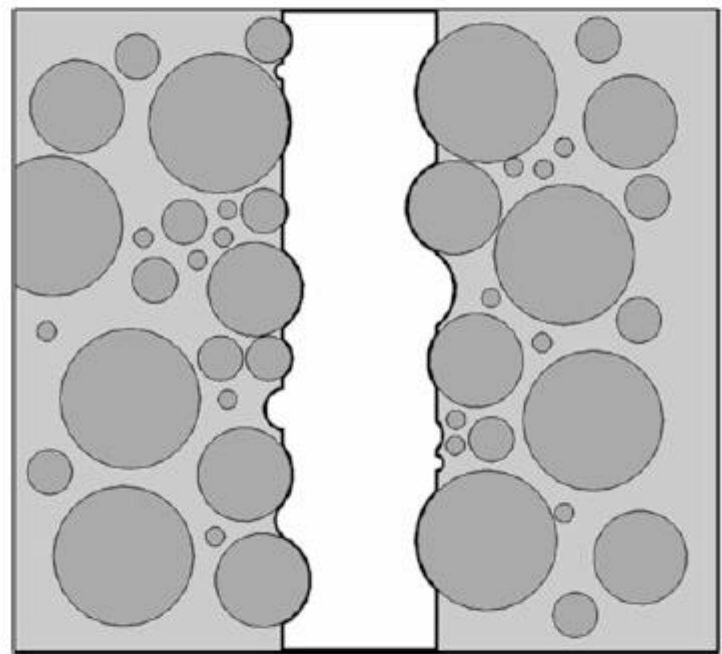


Figure 4.11: Intrinsic non-uniformities in photoresist can cause striation along the edge [11]

The third origin of striation is linked to the photolithography instruments and is suggested to be variation in the light exposure dose [11]. In an ideal photolithography process, the light that passes through the mask and reaches the photoresist has a step shape, hence unprotected photoresist is exposed to even dosage of light everywhere. In the real scenario though, the light dosage at the pattern edges are different and look like Figure 4.12. The light intensity is less on the edge of the patterns. If the intensity of light is less than a threshold value, then the photoresist will not receive enough UV exposure and hence will not be developed well. The exposure light fluctuation (due to variation in the

laser's output, optical system, movement in the wafer stage, or fluctuation in the light due to light quantization [11]) has therefore more effect on the edge of patterns. Can we solve this problem by increase the light dosage to much higher than the threshold value? This chapter will focus on studying all the photolithography process parameters to analyse the effect on striation.

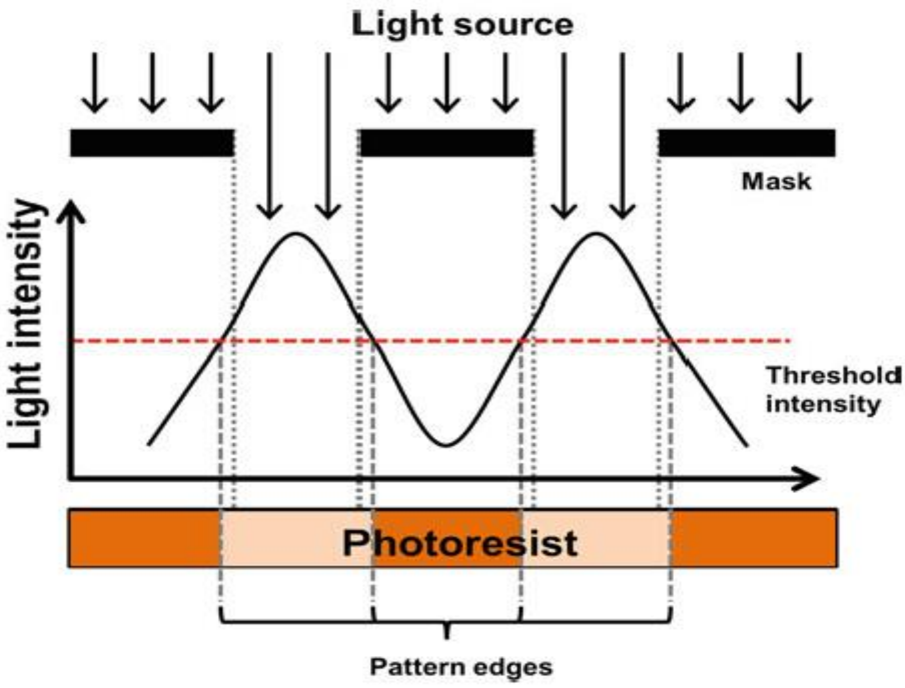


Figure 4.12: The light intensity that reaches the unprotected photoresist is not step shaped[11]

There are other factors such as the photolithography mask. In this work, high-resolution mask were used and the comparison of striation in mask and photoresist proved that the mask cannot be the origin of striation. The striation on the mask was non-existent under microscope, while the striation in the photoresist was clear to eyes.

There are alternative studies that suggest that reflections of UV light from a reflective mask layer can also affect striation and hence using non-reflective surface or post photoresist patterning bake can reduce striation [12][13]. Striation generated because of reflective masks seems to be along Y- direction. Though in this work, striation was only observed in X-direction and the first experiments showed that using non-reflective masks cannot eliminate or reduce striation hence this was not considered in this study.

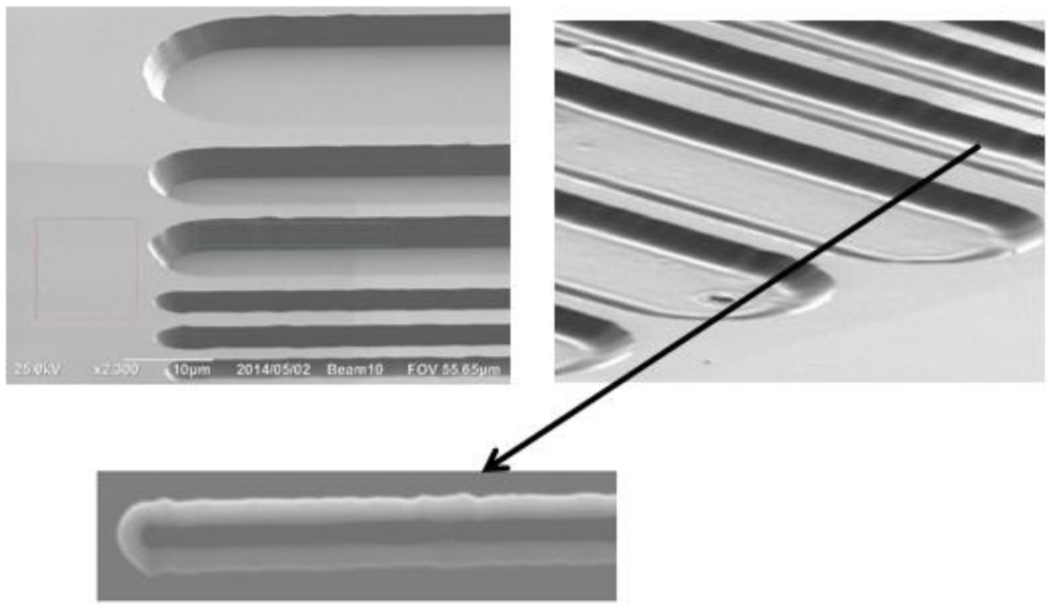


Figure 4.13:SEM images of photoresist after (A) post bake only (B) with TEOS as non-reflective surface and post-bake. None of these methods helps to improve the vertical striation.

Another important observation that will be discussed in this chapter was that the magnitude of the striation can increase when transferred to the underlying layers. Hence to minimise striation we must (1) minimize the

creation of striation during photolithography process (2) minimise the effect of mask and SiC etching process on striation.

As can be seen the two main challenges in fabricating trench structure, starts in the photolithography process not the etching. Hence it is important to understand every step of creating trench structure including (a) photolithography (b) etching mask (c) SiC etching parameters to be able to minimize striation and microtrenches. In the next section these three stages of fabricating trenches will be discussed and analyzed in detail. The ultimate goal of this chapter is to (a) understand how every parameters in the above three stage affect trench structure (b) minimize striation and microtrenches and create a smooth and clean trench structures.

As this was the first generation of trench devices in science city research group, there was no previous knowledge of any of these processes and hence the first part of this project was focused on understanding every process with the current material (photoresist, mask materials, etc.). We hope that the results of this chapter can be used as a reference point in identifying the source of problem in SiC etch process.

4.2 Overview of Dry Etching Process

An example of etching process of SiC is summarised in Figure 4.14. The photolithography process starts with cleaning the sample and then deposition of the mask material (metal in this example) on the SiC wafer. Then a layer of

photoresist is applied to the wafer. The photoresist is then baked before being exposed in the mask aligner. This is called soft baking and this process can be done in different temperature and duration. After soft bake, using a mask aligner, patterns on a chrome masks are transferred to the photoresist. The mask aligner can be set to use different exposure dosage, wavelength and times (duration). After exposing the photoresist to UV light using the aligner, some photoresist including AZ ECI 2000 will require additional round of baking, called post exposure bake (POB). This is not necessary for S1818 series (or most positive resist). Afterwards, the sample is put into a development solvent that develops the pattern on the photoresist. If a positive resist (S1818) is used, all areas that was exposed to UV light will be developed and hence will be removed. In the case of a negative resist, exposed areas will remain unaffected and unexposed area to UV light will be removed.

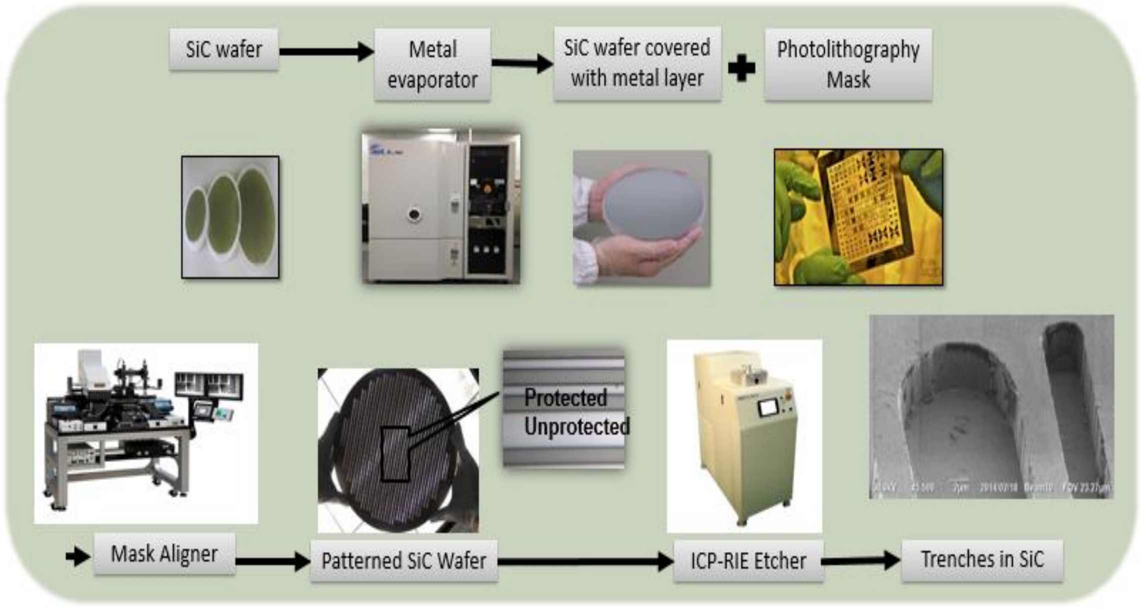


Figure 4.14:Photolithography process

The process is divided into four main stages:

1) Preparing the samples and masks
2) Photolithography process of photoresist and mask layer patterning
3) Etching of SiC

In the next section, every stage is studied in details to optimise the trench structures.

4.3 Step one: Sample and Mask Preparation

One important challenge in defining small patterns with fine straight boarders, is the requirement that the mask be in direct contact with the wafer through the entire wafer. With the test grade wafers problem such as what can be seen in following picture (uneven surface) can prevent this direct contact. Therefore, a prime grade wafer was used for this work.

Figure 4.15: Sample default on the surface of test grade material: This can prevent through contact with mask (miscroscopic image)

The second problem arises from contamination, therefore cleaning the wafer, mask and also the wafer chuck at each stage of fabrication is an important part of the experiment. Contamination is induced during fabrication, or from handling and wafer dicing.

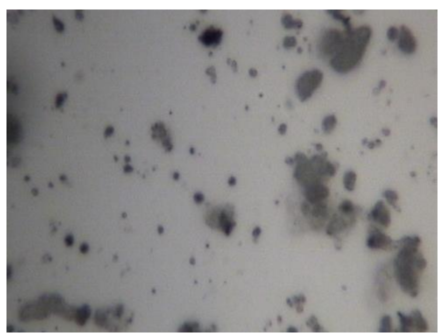


Figure 4.16: Microscopic images of SiC wafer (A) before cleaning (B) after cleaning

Figure 4.17 shows a clean wafer but the laser cut process has damaged the edges of the samples and can induce problems. It is possible to minimise the damage by lowering the laser cut power. At higher power, the damaged edge keep breaking up and the dust is deposited back on the sample during fabrication processes, even after cleaning the samples with solvent after every step.

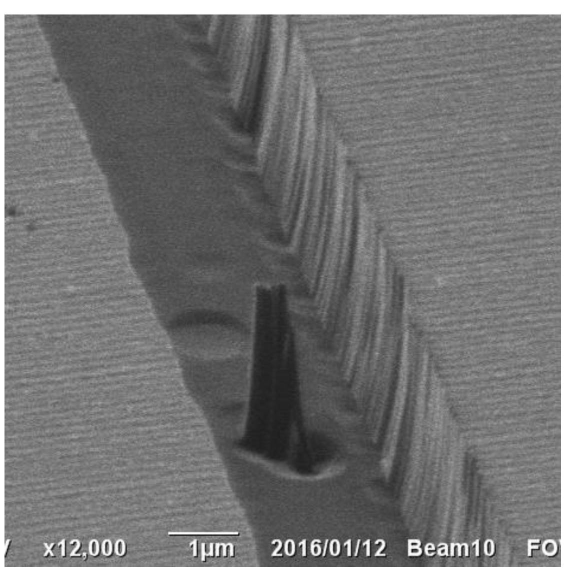
Figure 4.17: Microscopic image of effect of laser cutting on the edge of sample

Once laser cutting is complete, the wafer is subjected to the following procedures (1) blow drying with N_2 to get rid of the cutting dust; (2) cleaning the samples with both cotton and acetone; (3) soaking the sample in solvent for 10 min and (4) followed by ultrasonic for 4 minutes. Piranha cleaning for 15 minutes, followed by HF bath for one minute. At the end water bath the sample for five minutes and blow dry with N_2 again.

Sample preparation has a significant effect on the results. It is important to make sure there are no particles on the sample, especially cotton particles after removing the backside photoresist. Therefore, nitrogen blow dry before placing the sample in the aligner is suggested.

Another factor that can affect the trench structures is preparation of photolithography masks. To achieve straight boarders and grass-free trenches, cleaning the photolithography mask has to be done. Photoresist that remains on the mask during process builds up primarily around the boarders of the patterns on the mask, this results in striation of boarded as can be seen in Figure 4.18B.

Also the photoresist that remains in middle of the patterns results in the grass effect as can be shown in Figure 4.18A.



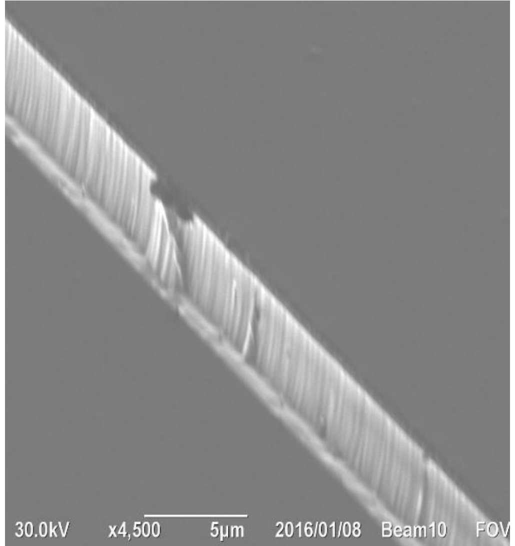


Figure 4.18: SEM images of (A) grass effect (B) striation caused by photoresist left on the photolithography mask

To avoid this problem, as mentioned before, masks have to be cleaned with acetone after every use but piranha cleaning(less frequently, depends on the photoresist) is essential. This is helpful in removing photoresist particles that cannot be removed by acetone. The exact time of piranha cleaning depends on photoresist.

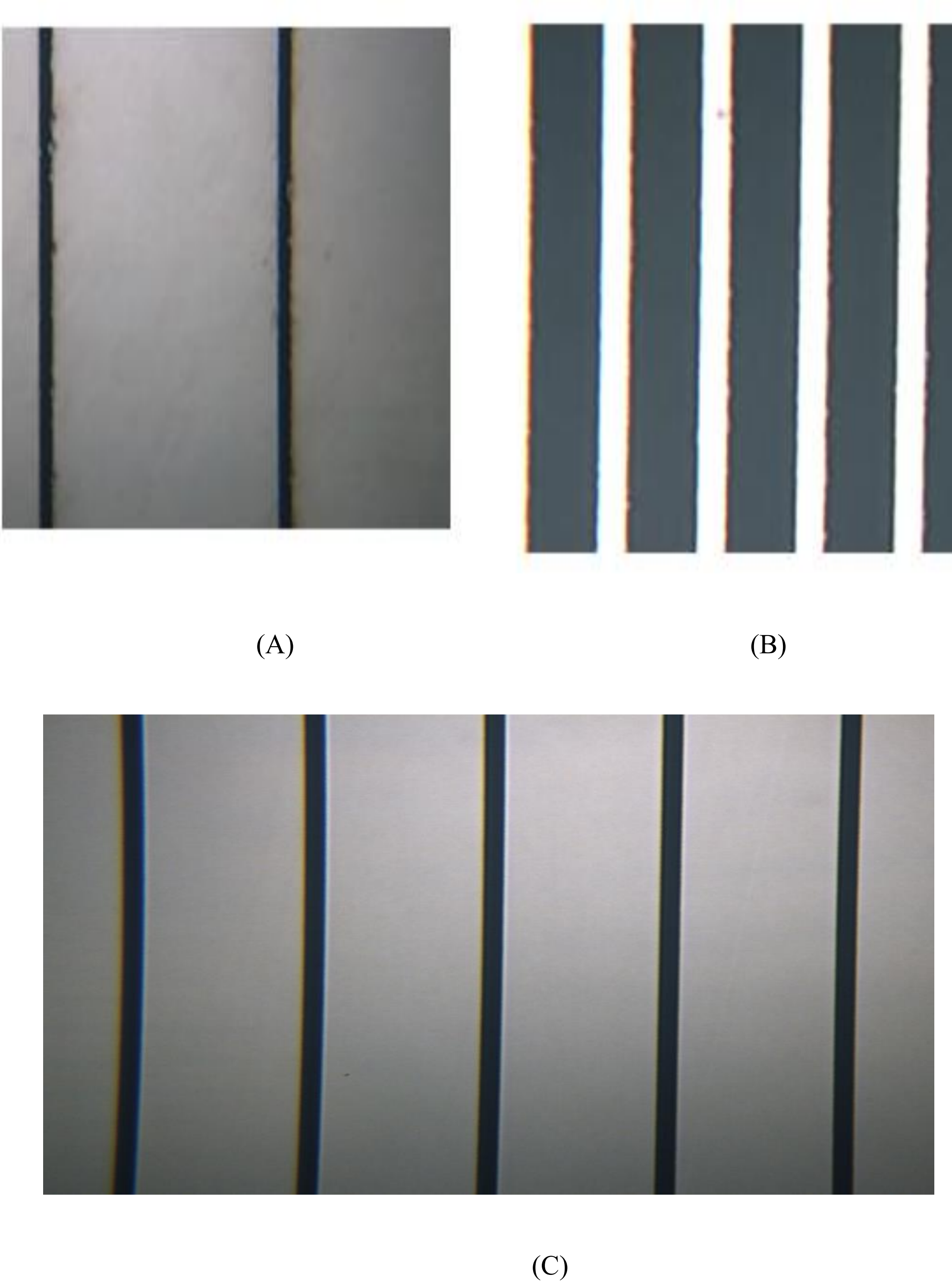


Figure 4.19:Microscopic images of photolithography chrome mask (A) before Cleaning Mask, (B) after 2 min Piranha cleaning(C) after 6 min Piranha clean

4.4 Step two: Photolithography process

Different parameters of the photolithography process have been investigated in this study including wavelength, soft bake temperature and time, exposure dosage, post exposure bake (POB) temperature and time (for AZ ECI 3012 photoresist) and development time. Two different positive resists (S1818 and AZ ECI 3012) photoresists and one negative resist (AZ 5214) have been used to fabricate trench MOSFET, hence the result in this chapter covers these three photoresist

In section 4.5.1 the experimental details are introduced, this includes experimental process of applying different masks. In section 4.5.2 the results are presented and effect of different photolithography parameters (including masking methods) on trench structure are discussed.

4.4.1 Experiments Setup

The experiment starts with cleaning the wafer as explained in section 4.4. The process of photolithography is different for each masking methods and will be described separately in section 4.5.1.2. Depending on the masking method, the photoresist is applied either on the SiC wafer (lift off method) or on the etch mask material (all the other methods). Photoresist is applied using Laurell WS-650Mz auto dispense spin coater. The photoresist is then baked (soft baked) using a hot plate. Suss Microtec MA/BA8 mask aligner is used to pattern the photoresist. The exposed photoresist is then immersed in developer liquid that

will dissolve the exposed photoresist. If a negative resist is used, another round of baking and exposure (flood exposure of the whole area of photoresist without a mask) is needed before developing the photoresist. Using negative resist the unexposed areas will be dissolved in the developer.

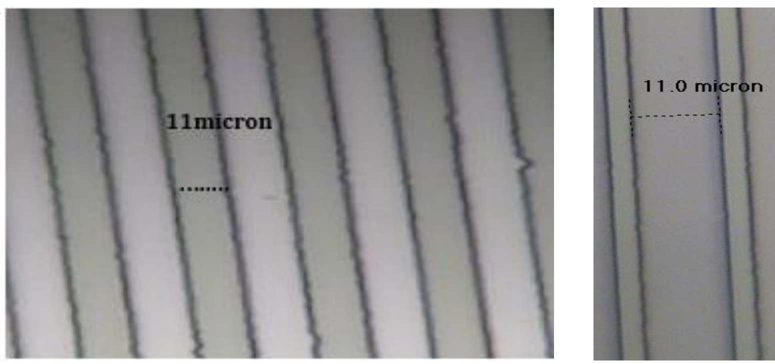
In the first round of experiments, we could not achieve any straight boarders. When high resolution microscope was used, uneven layer of photoresist was observed around the corners of the samples. This is called edge bead. After removing edge bead the striation of the patterns improved significantly. Next sections discuss the experimental details of removing edge bead and masking methods before the results are presented.

4.4.1.1 Removing Edge Bead

During spin coating of photoresist on the samples, a bead is created at the outer edge of the samples. This bead can be minimised by optimising the process but cannot be eliminated. Edge bead removal is done by exposing the edge of the sample to UV light while the rest of sample is protected using a photolithography mask. The sample is then placed in the photoresist developer that removes the edge bead.

Edge bead removing can help to achieve higher resolutions. During this step it is essential to ensure that there is zero distance between the mask and the sample during exposure. While it was possible to achieve 1 µm trenches with 1 µm distance from each other after removing edge bead, without doing so, it was only possible to achieve trenches with width bigger than 2 µm with distance

more than 2 µm. Also for sample size as small as 1 cm x 1 cm, it was impossible to get straight lines without removing edge bead, though this problem does not exist for quarter wafer samples.



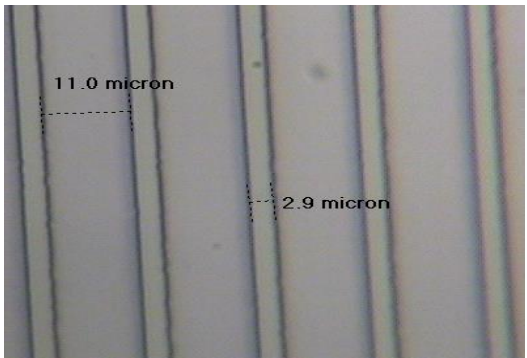


Figure 4.20: Microscopic images of pattern on photoresist (A) without edge bead removal (B) with edge bead removal

4.4.1.2 Masking Methods

Three different masking methods have been investigated in this work. This was done to investigate (A) effect of masking material on microtrenches (B) effect of masking material and process on striation.

- Method 1: Wet etching metal with positive resist using Nickel (Ni) as the mask
- Method 2: Lift off technique using negative resist using Aluminium (Al) as the mask layer
- Method 3: Dry etching using positive resist using Titanium (Ti) and Silicon dioxide (SiO_2) as the mask layer

4.4.1.2.1 Method 1: Wet etching of etch mask using Ni Mask

A Ni mask is deposited on the SiC wafer using SVS 8 pocket electron beam evaporator. Photoresist is applied on the Ni mask and is patterned using S1818 photoresist, and then the photoresist is used as a mask to etch Ni using the following wet etch recipe:

- Nitric acid (5ml)/Acetic acid (5ml)/Sulphuric acid (2ml)/Water (10ml).

All these percentage were studied carefully in 38 different test rounds to be able to achieve a percentage for each liquid that results in the best pattern with straight edge. Using different percentage of these liquids results in decreasing or increasing the development time which resulted in much distorted boarder on the Ni mask.

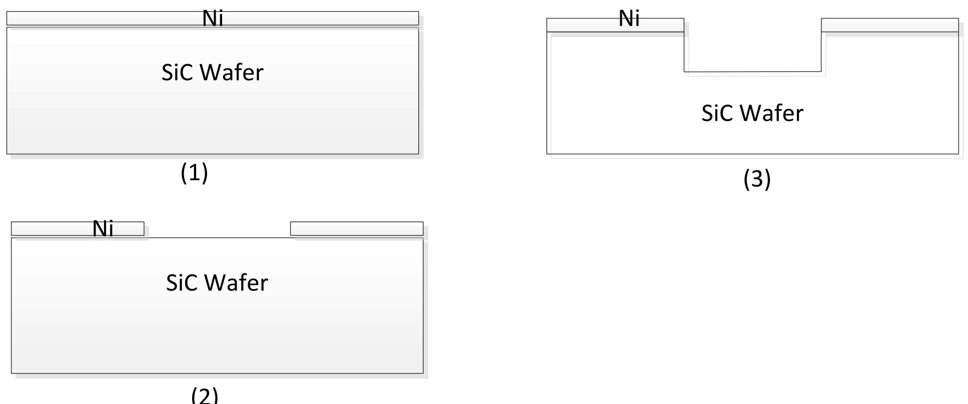
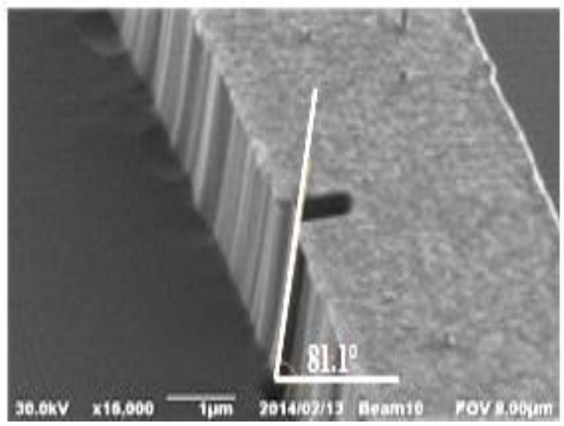


Figure 4.21:Etching SiC procedure using metal mask:1) deposit a 0.15 um thick layer of Ni, 2) pattern the photoresist on top on of the Ni mask layer and then etch Ni layer, etch Ni 3) etch SiC

A Ni mask has a very interesting characteristic that makes it very efficient as the etching mask for SiC. As mentioned in literature review, there is a requirement to exploit the use of a high-power ICP-etching system to achieve high etching rate of SiC. All mask materials studied in this work, have higher etching rate in high ICP etch. Experiments in this work show that in contrast to other materials, higher ICP power results in lower etch rate of Ni. Hence higher selectivity of Ni mask over SiC is achieved at high ICP power.

Dry etching of SiC is an anisotropic process and the best results achieved in this work show sidewalls with 80°-82° angle. Ni is etched very slowly at high powers and so creates a shadow masking at high ICP powers (Figure 4.22). As described in section 4.2.1 the results of this work show that the only the ions near sidewalls are affected by differential charging. Hence it can be assumed that if we can decrease the numbers of ions near sidewall, microtrenches can be minimised or eliminated. To test this theory, we have used high selectivity of Ni mask at high power to etch SiC while Ni mask creates a shadow protection around the edges. The results shown in figure 4.22 confirm our theory: that sidewall protection can eliminate microtrenches. This is especially important because the only other method is to reduce the ICP power which in turn reduces the etch rate.



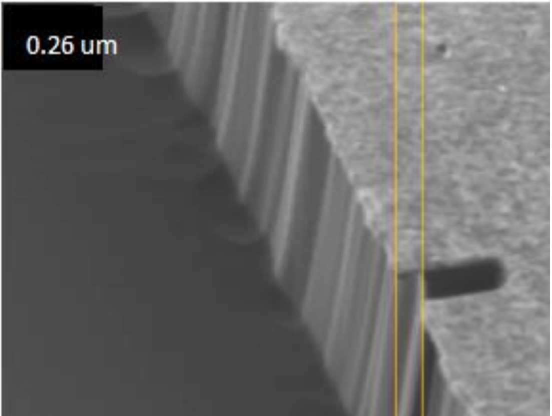


Figure 4.22: SEM images of overshadow protection of sidewall created when using Ni mask. This size of this overshadow protection is bigger in higher ICP powers.

As can be seen in Figure 4.22, the downside of using Ni mask is that striation of sidewall seems to be worse than what was observed on the photoresist mask. To minimise this, Ni wet etch process needs to be optimised even further. The most promising results achieved in these experiments gave average peak-to-peak striation of 0.16 μm with Ni mask.

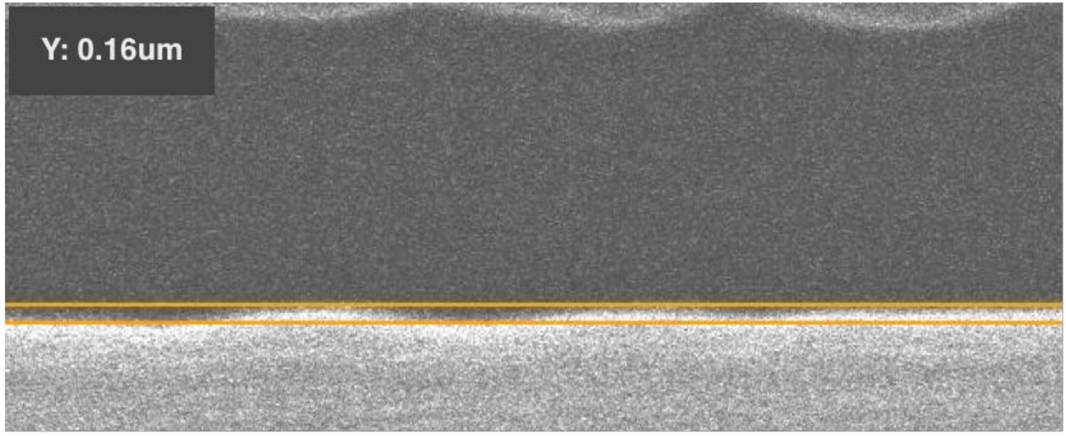


Figure 4.23: SEM picture illustrate the peak to peak measurement of striation for Ni mask

4.4.1.2.2 Method 2: Lift-off Technique - Al Mask

The lift off technique is an alternative method that has been explored. Figure 4.24 shows the complete process of life off.

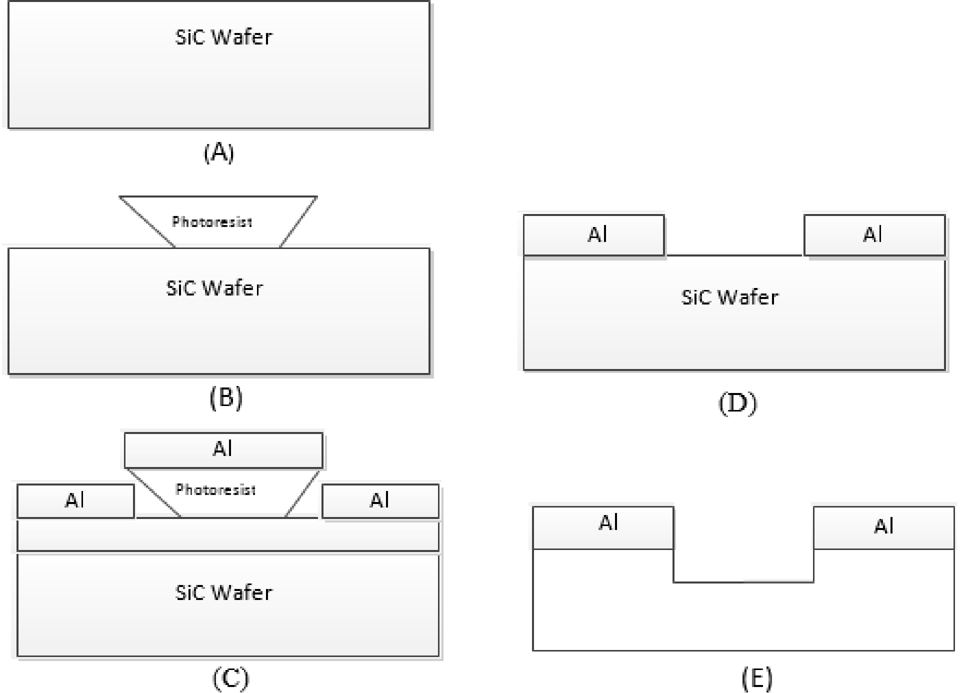


Figure 4.24:Lift off process using Al (A) clean SiC sample surface (B) pattern the photoresist on the SiC wafer (C) deposit Al on top of the photoresist (D) put the sample in ultrasonic acetone bath, this will remove the photoresist and the Al on top of it (E) the unprotected SiC parts will be etched.

An advantage of using this technique is that photoresist patterns are developed directly on SiC surface, which is a great deal easier than developing a pattern on deposited metal. In this process we usually use a negative photoresist (AZ 5214 in this project). This is because softening temperature of

positive resist are lower and hence the patterns become easily rounded, in such cases the mask layer usually covers everywhere on the photoresist including the sidewall of patterns and hence it is very difficult to remove the underlying photoresist with acetone bath. Negative resist on the other hand usually achieve under cut that make it more suitable for lift off (Figure 4.24B) [14].

Photoresist patterns on SiC surface generally possess straight borders and are well developed. This may be due to the non-reflective nature of SiC wafer and also the uniformity of the wafer. Moreover, the lift-off method is less sensitive to time. After depositing Al on top of the patterned photoresist, even if the sample is left in the ultrasonic bath longer than the required development time, the borders will not be distorted. An additional advantage of the lift off method is that only the photolithography process needs to be optimized we do not need to etch the metal layer in this process.

Table 4.1 shows the step by step process of etching SiC using lift-off achieved using AZ 5214 photoresist. Bake 1 and Exposure 1 refer to the soft bake of photoresist, which is done after photoresist spinning on the wafer. Unlike positive resist, negative resist will need another round of bake and exposure (Bake 2 and Exposure 2) to reverse their polarity (from positive to negative) before they are developed. The results show that the patterns are in average 0.4 μm bigger than the original pattern on the photolithography mask. Further study is needed to investigate the source of this problem.

The best peak-to-peak striation achieved by this process was around 0.25 µm using Al mask.

Experiment	**1**
Mask material	Al
Soft Bake 1	115 °C, 1 min
Exposure 1	90 mJ/cm²,3 s
Bake 2	120 °C, 2 min
Exposure 2	120 mJ/cm²,3 s
Photoresist development time: 35 s	

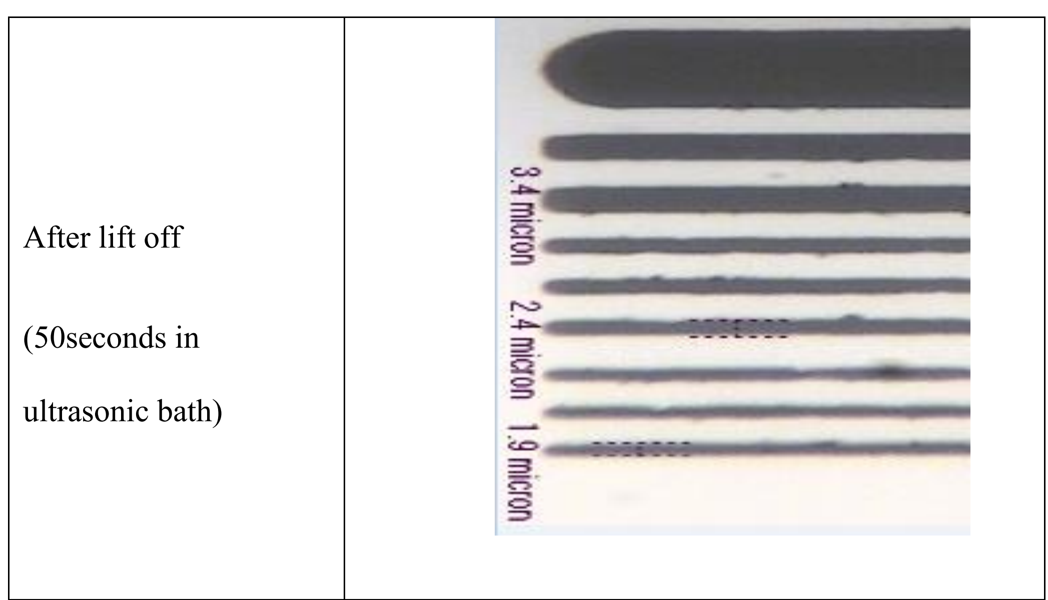
After lift off (50seconds in ultrasonic bath)	

Table 4.1: Lift off technique processes using AZ 5214 negative resist and Al mask

4.4.1.2.3 Method 3: Dry Etching of Etch Mask Using Titanium (Ti) Mask and SiO_2 Mask

A Ti layer was deposited on SiC wafer using metal evaporator. In the next step photoresist on top of Ti layer was patterned using S1818, and was dry etched using RIE etcher. This study was carried out to study if dry etching the mask can be useful to minimise the transfer of striation from photoresist to the mask layer.

Figure 4.25: Microscopic pictures of trench pattern (1) after photolithography, (2) after etching of Ti mask, (3) after etching SiC

A primary disadvantage of this technique is that SiC etch recipe simultaneously etches Ti, thereby reducing the selectivity of Ti on SiC. Consequently, very thick Ti should be used. Moreover, overshadowing of Ti was not as efficient as Ni despite the average peak-to-peak striation being similar to that of wet etching of Ni. The recipe used to etch Ti is shown in the Table 4.2.

Gas 1 - (sccm)	**Gas 2 - (sccm)**	**Chamber pressure(mT)**	**RF Forward Power (W)**	**Peak Voltage (V)**
Ar -5	SF6 - 10	7	150	850

Table 4.2: Etch recipe for RIE etch of Ti

Since Ti did not seem to solve striation problem, it was replaced by SiO_2 mask as shown in Figure 4.26. SiO_2 was etched using RIE etcher.

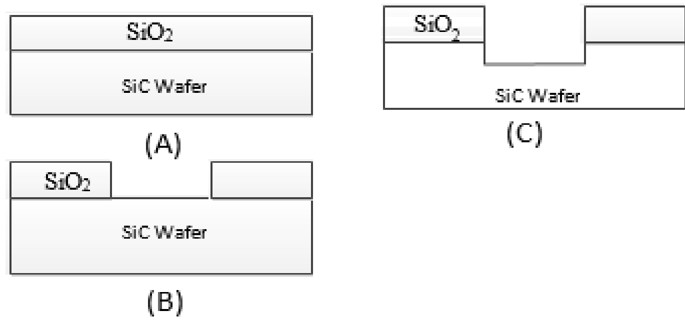


Figure 4.26: Etching SiC procedure using SiO_2 mask (A) deposit SiO_2 layer on SiC (B) pattern SiO_2 using dry RIE etch and S1818 photoresist and the mask layer (C) etch SiC using ICP-RIE etcher

One problem associated with the SiO_2 mask is the low densification, which results in etching SiC surface through the micro-holes in the SiO_2 layer. This problem was eliminated by densification of SiO_2 in Ar gas at 1000 °C for 1 hour.

Figure 4.27: SEM image of micro-etch problem due to low densification of SiO_2 mask layer.

As the selectivity of SiO2 masks is not very high at increased ICP power, the overshadowing is minimal. However, the minimum overshadowing is created and can still protect the sidewall (Figure 4.28). By further optimisation of the etching process, we can increase the width of overshadow and support the corners from micro trench as will be discussed in next section.

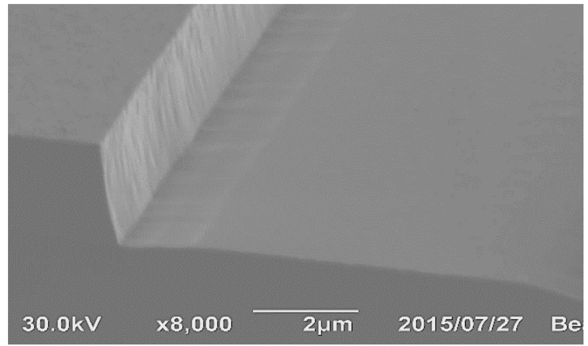


Figure 4.28: SEM image of microtrench effect in SiC using SiO_2 mask

Table 4.3 compared the selectivity of the mask layers. Mask selectivity is defined as the ratio of the SiC etch rate to the mask etch rate. Ni mask has the highest selectivity. Also Ni is the only material that showed higher selectivity by increasing ICP power.

Metal mask	Selectivity
Evaporated Ti	0.6
Evaporated Ni	68
Evaporated Al	16.25
SiO_2	1.93

Table 4.3: Comparison of mask selectivity

4.4.2 Results:

The detailed study of photolithography process and different masking method presented in previous sections shows that striation is affected by every step from cleaning, photolithography to etching SiC. On the other hand microtrenches seem to be only affected by the mask material (and the SiC etch process that will be discussed in the next section). In this section the effect of photolithography and masking method on striation and microtrenches are

represented. The goal was to find the best parameter and process that can help to minimise both challenges.

4.4.2.1 Striation

The results show that different parameters during photolithography process can affect striation. These parameters include: (1) softback time and temperature (2) exposure wavelength and dosage (3) development time (4) masking material

4.4.2.1.1 Photoresist Development Parameters

Two main factor seemed to affect striation the most when patterns are developed on photoresist: (1) Soft bake time and temperature (2) Development time of photoresist.

The process of soft bake is both temperature and time specific. If performed at a low temperature or the baking duration is insufficient, results in distorted boarders. This is due to the high dark erosion rate. Additionally, if performed at a high temperature or longer bake times, the development time would increase which also increase the dark erosion rate (Figure 4.29B). Therefor both time and temperature should be optimised for the soft bake time.

Figure 4.29: Soft bake of a S1818 photoresist at (A) 100°C and (B) 125°C. When soft bake is done at higher temperature like 125°C, the development time increased to more than 10 minutes and the trenches that were closer than 1µm to each other were over developed (microscopic images)

The other factor in the photoresist development process that can affect the striation is development time after the resist is exposed to UV light. It is essential to optimise the development time for vertical devices, as even an additional couple of seconds can lead to severely distorted boarders. The exposed resists need enough time in the developer liquid to dissolve, if the time is not enough, the small patterns will not be developed clearly, but if the duration is even a few more seconds that the necessary duration, then the boarders will be distorted severely.

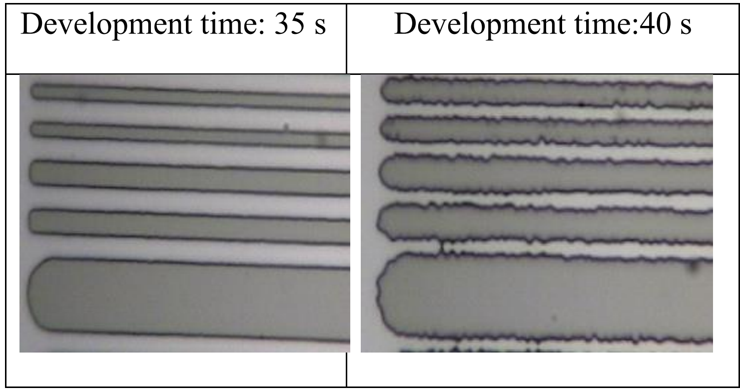
Development time: 35 s	Development time:40 s
	

Table 4.4: Lift off technique using AZ 5214 negative resist and Al mask: 5 more seconds of development time resulted in severe striation

4.4.2.1.2 Exposure Wavelength and Dosage

Apart from the photoresist, the parameters chosen when using mask aligner also affect the striation, but have no effect on microtrenches. The wavelength and dosage of mask aligner are the two parameters that must be optimised to minimise the striation in photoresist pattern. Suss Microtec MA/BA8 mask aligner has been used in this work and there are only two wavelengths available in the settings of this aligner: 365nm and 435nm.

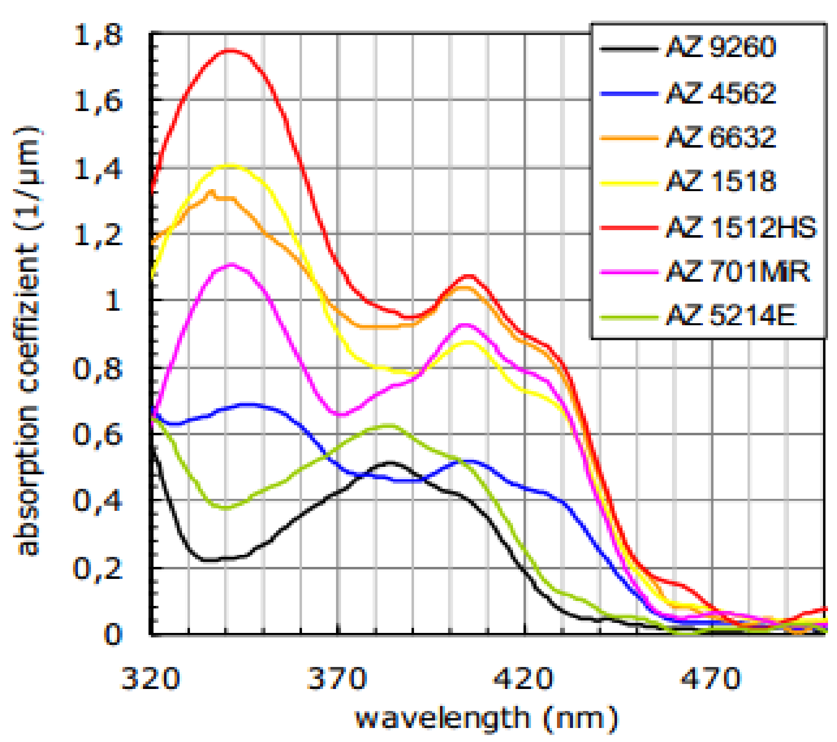


Figure 4.30: Absorption coefficient vs. wavelength for AZ series photoresist [15]

Using shorter wavelength (365 nm) decreases the development time significantly; this is due to the fact that the absorption increases at this wavelength as can be seen in Figure 4.30 (This can be different for different photoresist, AZ series and S1818 both show similar pattern in shorter wavelength). At higher wavelength the absorption coefficient decreases and the problem that is caused by this is that more time is needed to develop the photoresist. For example if 435 nm wavelength is used, a higher dosage (almost three times) is needed to develop the photoresist as can be seen in the Table 4.5. Long development time increases dark erosion and hence cause striation in photoresist, therefor it's important to use a wavelength that increase the absorption coefficient. In this work 365 nm has been used for AZ and S1818 photoresists.

Soft bake time & temperature	**Dosage**	**Wavelength**	**POB time and temperature**	**Development time**
90 °C for 1 min	75 mJ/cm^2	365 nm	110 °C for 1 min	55 s
90 °C for 1 min	75 mJ/cm^2	435 nm	110 °C for 1 min	3 min 10 s

Table 4.5: Development time vs. wavelength for AZ ECT 3000 resistance

Another parameter that should be chosen carefully is the dosage of exposure. High dosages are not recommended because they result in distorted boarders (Table 4.6). This is due to the increase of the scattered and diffracted

lights. Very low dosage can also result in distorted patterns as bad as high dosage because of the increase in dark erosion, mainly because of increase in the pattern development time. This means that there is an optimum dosage for every photoresist that should be used to minimise the striation. This optimum dosage value is different at different wavelength.

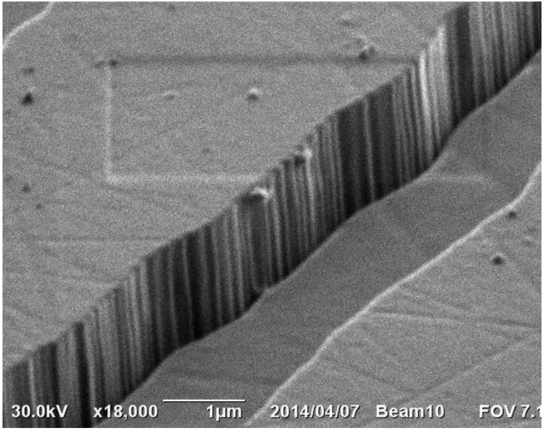
Exposure dosage mJ/cm^2	**Striation**
150	
130	
95	

Table 4.6: Effect of exposure dosage on the patterns: very high and low dosage increase the striation; a balanced dosage should be used.

4.4.2.1.3 Masking Material and Method

The third factor that affect striation is the etch mask material and method. Using the same recipe to etch SiC with the different masking methods that were introduced in the experimental setup (section 4.5.1.2), it was clear that the etch mask could degrade the striation in patterns. Using metal masks results in worse striation in comparison to SiO_2, regardless of what type of photolithography process has been used. All metal masks and methods including: Al (using lift-off), Ni (using wet etch of Ni) and Ti (ICP-RIE etching of the mask) have resulted in higher striation in comparison to SiO_2.

Figure 4.31 shows the comparison between the etching results using metal mask and SiO_2 mask. Between metals, Ni results in less striation. SiO_2 mask was further improved when photolithography was done on a quarter wafer instead of small samples.



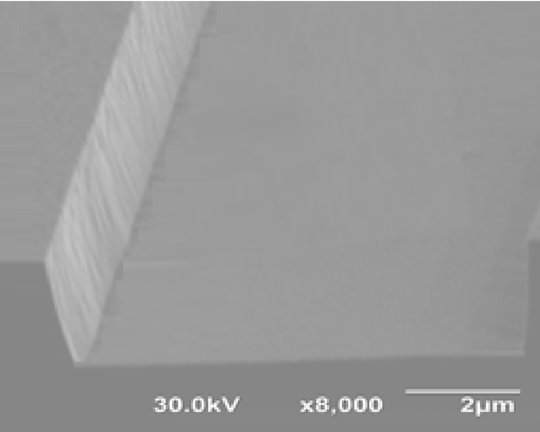


Figure 4.31: SEM images of striation in SiC trench using (A) Ni mask (B) SiO_2 mask

While the striation of metal could be measured peak to peak to be min around 0.16 μ for Ni and 0.25 μm for Al, the striation in SiO_2 is in much smaller scale. The striation was only observed by setting the contrast to maximum (Figure 4.31B) but even by using SEM, the striation in SiO_2 were too small (almost non-existent) from the top view to be measured. From the results of this section, we conclude that SiO_2 mask is the best choice to reduce striation. In the next section, the effects of photolithography and masking method on microtrenches are presented.

4.4.2.2 Microtrenches

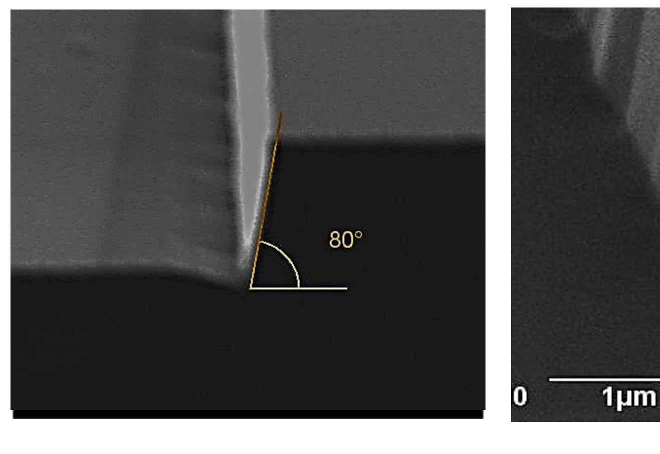
While the masking material does not directly affect the microtrenches, they result in different microtrench size since the undercut that is created using different material has different size. The Ni mask is the most efficient at eliminating microtrenches as it creates the biggest overshadow support at high ICP powers (Figure 4.32B).

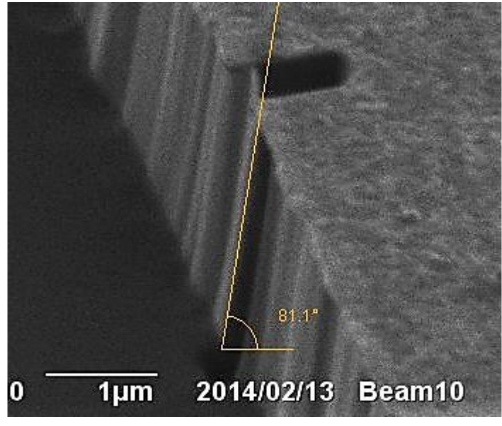
Using Al and Ti at high ICP power results in almost non-existent overshadow protection and hence the microtrench size is maximised (Figure 4.32C). SiO_2 mask create a smaller undercut that minimise the microtrenches but did not eliminate them (when the same recipe was used to etch using Ni mask, the microtrenches were completely eliminated) (Figure 4.32A and 4.32B).

One must notice that the sidewall angles are the same when different masks are used (80° in all cases). This proves that (1) anisotropic aspect of SiC etch is not related to metal mask (2) the difference in the size of undercut

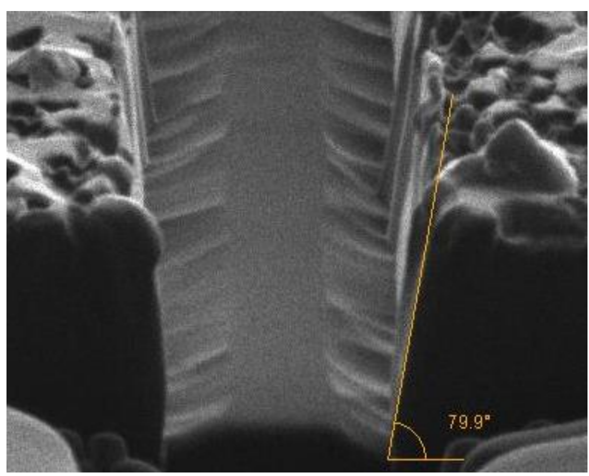
(overshadow protection) created by different mask material is not because of etch of SiC material in X-direction (anisotropic etching).

The reason for different undercut size is because all the masks used in this work, are also etched during SiC dry etch. Ni mask and SiO_2 mask seems to show minimum etch in the X-direction and when the SiC sidewall is etched from 90° to 80°, the mask material is not etched in the same rate in the X direction. This will create an undercut that is used as overshadow protection of sidewalls during ICP-RIE etching of SiC. Experiments in this work show that the bigger the overshadow is, the smaller is the microtrenches, and overshadow with width bigger than 0.1 μm can eliminate microtrenches are ICP power of 1000W.





(A) (B)



(C)

Figure 4.32: SEM image of various masks using equivalent etching recipe (A) SiO_2 (B) Ni and (C) Al.

This results also show that the origins of microtrenches and non-vertical sidewall angles, are different. Reducing ions density near sidewall has improved the microtrenches but sidewall angles remain unaffected. In the next section, it is shown that sidewall angles are only dependent on the ICP-RIE etch parameters.

There are other issues that also were factored in choosing SiO_2 mask including (1) Removing etching mask (2) Achievable resolution.

Removing a mask can be a challenging step in fabrication of semiconductor. It is important to choose a mask that can be completely removed from the surface of the semiconductor after etching SiC as impurities on the surface can degrade the performance of the device.

If a mask is dry etched (e.g. SiO_2 or Ti), the patterned photoresist on top can become carbonated which renders it extremely difficult to remove, as depicted in Figure 4.33. Moreover, in such cases there is increased difficulty in removing photoresist with acetone (even in an ultra-sonic bath). Although this problem has been rectified using dry RIE etching of photoresist.

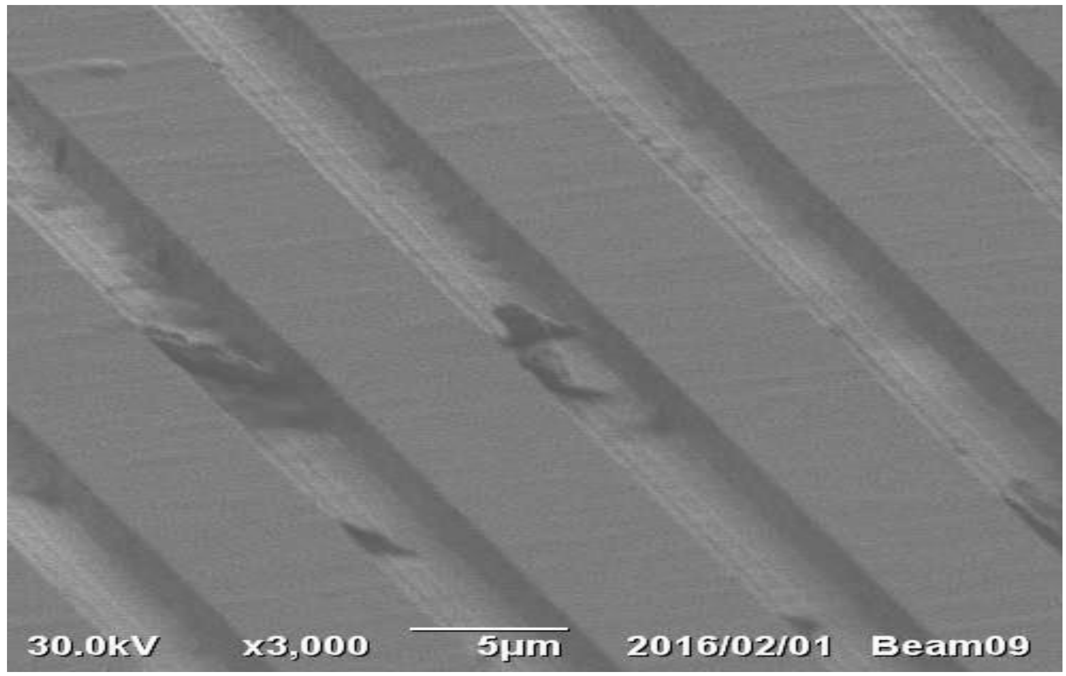


Figure 4.33: SEM image illustrating the presence of carbonated photoresist remaining in SiC trenches

A similar issue can occur whilst using a Ni mask. After removal of the Ni mask, even after cleaning with several different recipes, micro amounts of metals remain on the SiC, which could not be removed (Figure 4.34). Therefore, using metal mask on top of SiC is not recommended or the alternative is to use a thin layer of SiO_2 between the metal mask and SiC surface.

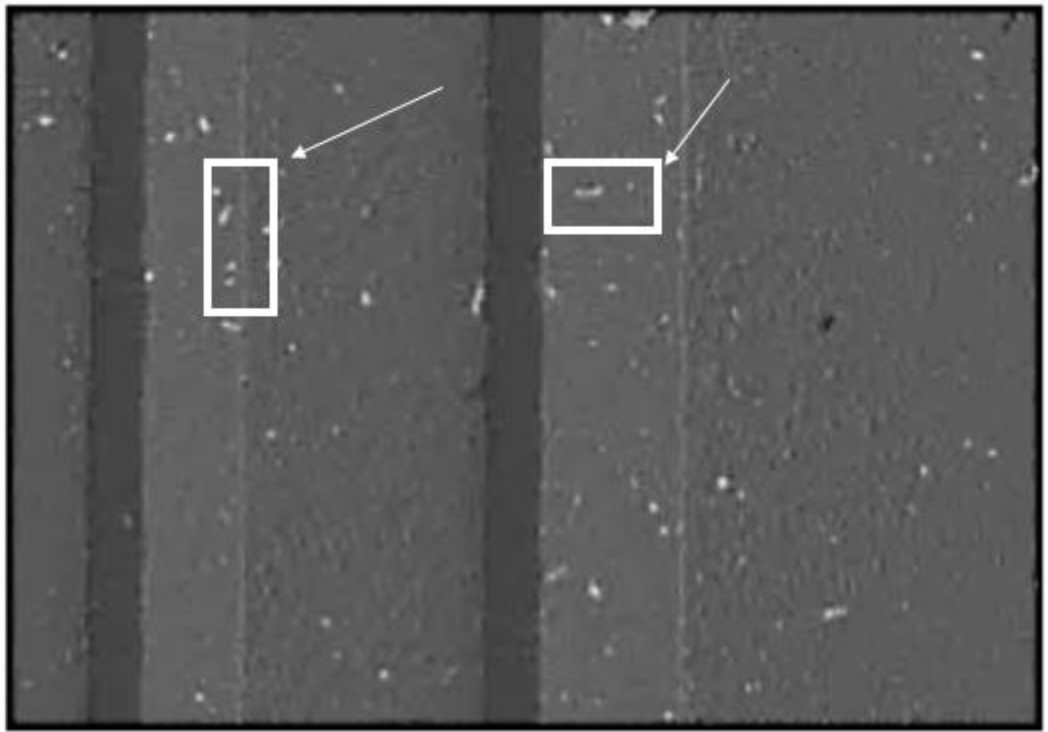
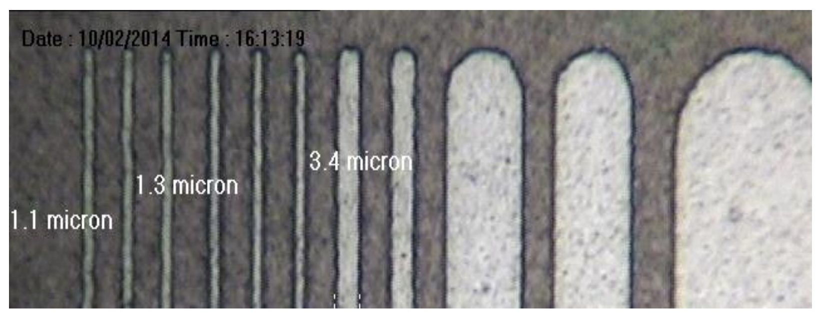


Figure 4.34: SEM images of remainder of micro metals after Ni removal

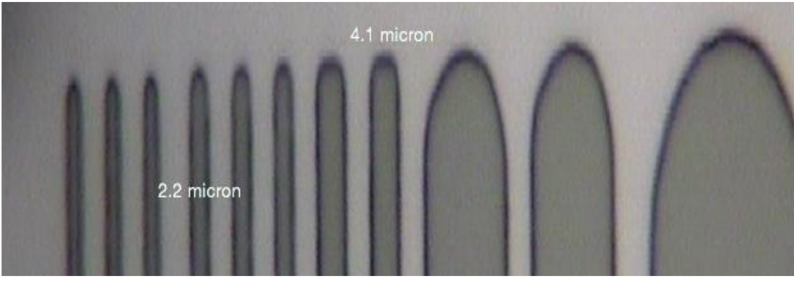
Achievable resolution is another important factor in concluding to use SiO_2 mask. Patterns as small as 2 µm are easily achievable using positive resist on Ti, SiO_2 and Ni masks. The resolution also depend on the instrument used in the cleanroom, the resolution of machinery in science city research group is 1 µm. 1 µm resolution was achievable with all these masks, although the etch process must be optimized in the case of Ni as otherwise the 1 µm trenches will not develop thoroughly.

Equivalent process and photolithography masks using the lift off method results in larger pattern. 1 µm trench pattern results in at 0.5-1 µm bigger

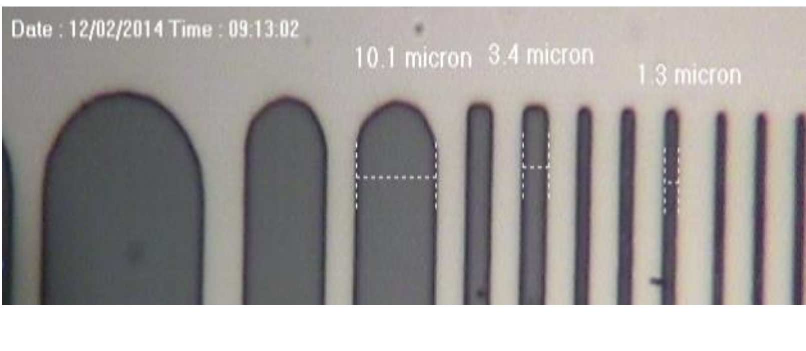
patterns in such cases (Figure 4.35B) and therefore would be more difficult to achieve high resolution device with lift off.



(A)



(B)



(C)

Figure 4.35: After etching the same pattern on SiC using (A) Ti mask (B)Lift off using Al (C) Ni mask. The results show that bigger pattern are achieved when using lift off technique (microscopic images)

Even though Ni is the most desirable and simplest method to eliminate microtrenches, SiO_2 mask comes in the second priority and since it resulted in the minimum striation, it was decided to use SiO_2 as mask layer. The minimum size microtrenches resulted using SiO_2 mask layer were eliminated by optimising ICP-RIE etch recipe. This was done by reducing the trench sidewall angles to less than 80° so that the mask overshadow is increased. The alternative is decreasing the ICP power to minimise the microtrenches effect. In the next section we discuss how ICP-RIE etch parameters could be optimised to eliminate microtrenches and striations.

SiO_2 is also the optimum choice as it results in the cleanest surface. Moreover, as it is dry etched using RIE etcher, very high resolutions can be obtained without over complicating the process.

In the next section, the effect of SiC etching parameters on trench structures will be discussed.

4.5 Step three: ICP-RIE etching of trenches in SiC

In this section, the effects of SiC etching parameters such as RF power, ICP power and pressure have been studied. The results demonstrate that both ICP power and pressure heavily affect sidewall striation and microtrenches. Even though striation is not generated during the ICP-RIE etch, it can be enhanced during the ICP-RIE etch of SiC if the etching parameters are not optimized. On the other hand microtrenches are created in this step. In the previous section, minimizing the microtrenches using masks were introduced. In this section we study the etch process to determine which parameters affect the microtrenches. As mentioned previously only Ni mask can completely eliminate microtrenches because of the wide undercut that it provide and hence protect the sidewalls. The results of this section could be used to eliminate microtrenches if any mask other than Ni is used. The main focus of this section is to understand how every parameters can affect different aspect of trench structure such as roughness, sidewall striation, side wall angles, microtrenches and etc. At the end the best recipes to etch SiC using Ni mask and SiO_2 mask is presented.

4.5.1 Experimental setup:

Corial 200IL ICP-RIE etcher was used to study the effects of varying etching parameters on the structure of 4H-SiC samples. ICP power in the range of 200 W-1000 W, RF power in the range of 20W-80W and pressure in the range

of 6-10 mTorr were used and the effects on microtrenches, striation, sidewall angles and bias voltage were analyzed. Different Sulfur hexafluoride (SF_6) combination with (Oxygen) O_2 and Argon (Ar) have been used to etch the SiC. The flow rate of SF_6 and Ar were kept constant at 50 SCCM and 40 SCCM respectively. The sample carrier (shuttle) is made of quartz and graphite

4.5.2 Choice of Etching Gas

There have been attempts to use different gases to etch SiC, SF_6 and NF_3 are reported to result in very high etch rate up to 600 nm/min for SF_6 and up to 900 nm/min for NF_3 at high ICP power, while NF_3 results in lower surface damage usually less than 1 nm in the wide range of low to high ICP power [16][17].

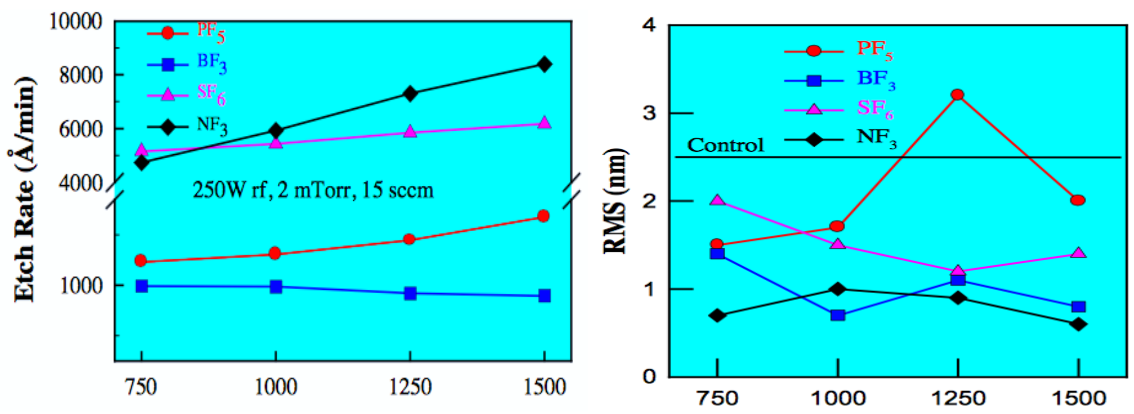


Figure 4.36: Effect of ICP power on etch rate and roughness (RMS) [17]

Choi [16] has studied NF_3 in a wide range of ICP and bias(RF) power, pressure and distance(sample to coil) (Figure 4.37) and the results show that

roughness is always below 1 nm, and for ICP powers less than 800W the samples show no microtrenches while the side wall angle is around 80°.

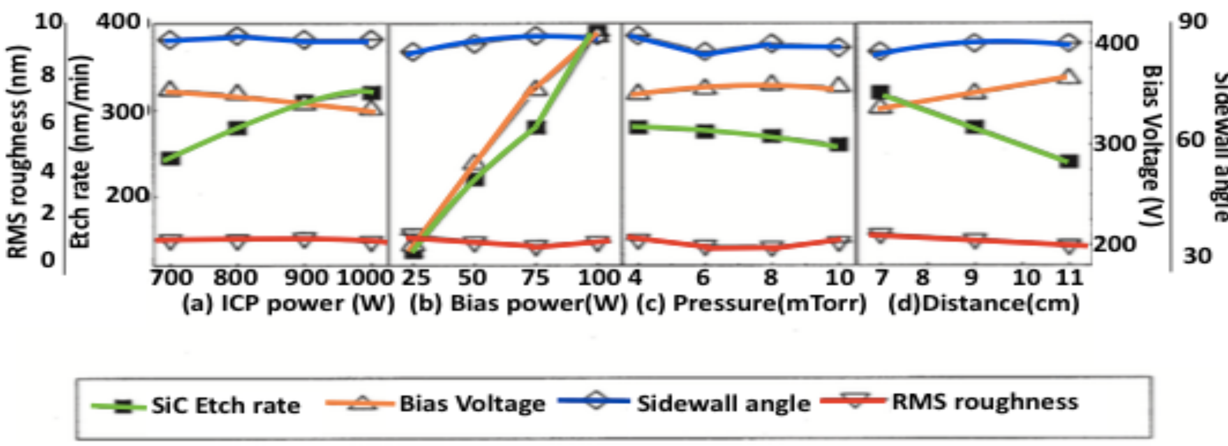


Figure 4.37:Effect of ICP-RIE etch parameters etch results using NF_3 gas[16]

SF_6 based gases has been used in majority of studies. Different studies report on the roughness to be 0.2-0.5 nm[3], 0.5-1 nm[18] or 1-2 nm[17] depending on the pressure, ICP power or RF power. There have been no success at eliminating roughness at high etch and roughness is still a problem with SF_6 etch [19][20][21]. Studies show that using 100% SF_6, at high ICP power (900 W) and pressure (10 mTorr), etch rate of 360 nm/minutes could be achieved that results in a roughness of 0.8 nm [18] and sidewall angles with an average of 80°.

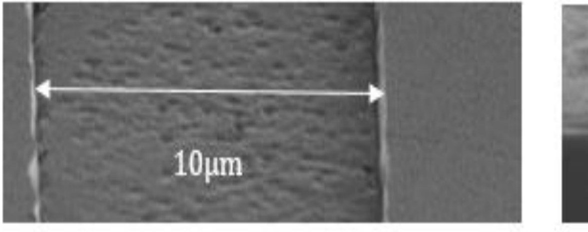
There have been attempts to increase the etch rate and decrease the roughness by adding Oxygen (O_2) [3][20][21] or Argon (Ar) [4][22] to SF_6. All studies agree that while O_2 can increase the etch rate to even more 1000nm/min [3][4], it degrades the roughness. On the other hand Ar has been reported to

reduce the roughness significantly [22] and hence it is recommended to use Ar with SF_6 plasma etch. The highest achievable etch rate using this combination has been reported to be around 1000 nm/min [4] at high bias voltage, though the roughness is not reported for this study.

Khan [4] has compared Cl_2 based plasma etch to SF_6 etch. The results show that the etch rate of Cl_2 based plasma is much lower, around 200 nm/min. The interesting point is that even though Cl_2 plasma results in slightly higher roughness, the results from electrical measurement such as barrier height (eV) or leakage current show that Cl_2 plasma etch can have better electrical performance. These results are important reminder that improving physical characteristics does not always results in better electrical.

The choice of gases in science city research group are Cl_2 or SF_6 based gases. Using Cl_2 results in low etch rate, and also a deep cleaning of the ICP-RIE etcher is needed after every use. From the literature review, it is clear that SF_6 offers very high etch rate and also low roughness and hence is a great choice for the first generation of trench device. SF_6 based gases are used in this work to etch trenches. Oxygen (O_2) and Argon (Ar) are the gases that were available as well and were used to study the effect of adding a noble gas and a highly chemically reactive gas to the etching process. Ar was used to study the effects of noble gas in etching. Noble gases are a group of gases that have very low chemical reactivity. O_2 was used to study the effect of a highly reactive gas in addition to SF_6 .

Adding O_2 to SF_6 increases the roughness of both the sidewall and bottom of the trenches (Figure 4.38A). As it can be seen, in Figure 4.38A, the milling (physical etch) effects is clear on the bottom of trench and seem O_2 increases the physical aspect of the etching. This is undesirable as milling effect usually results in increased roughness. Overall striation of side wall also becomes worse upon the addition of O_2 to the gas (Figure 4.38B). At higher powers with the addition of O_2 the striation and roughness becomes so severe and additional steps in the sidewall profile are seen (Figure 4.38B).



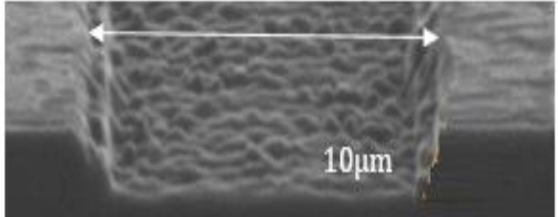


Figure 4.38: SEM images of (A) roughness increase due to addition of O_2 to SF_6 at ICP power of 200 W (B) striation becomes severe due to the addition of O_2 at an ICP power of 1000 W.

Adding 20% O_2 to SF_6 decreased the sidewall angle from ca. 80° to 68° but increased the etch rate from 0.58 μm/min to 0.64 μm/min (at fixed ICP power of 500 W). Increasing the percentage of O_2 to SF_6 did not enhance the etch rate any further, and interestingly led to a decrease (Figure 4.39). From these results it is clear that the addition of O_2 leads to an increase in the milling effect, roughness and striation and hence it was concluded that for roughness sensitive structures such as gate trench, O_2 should not be added to SF_6.

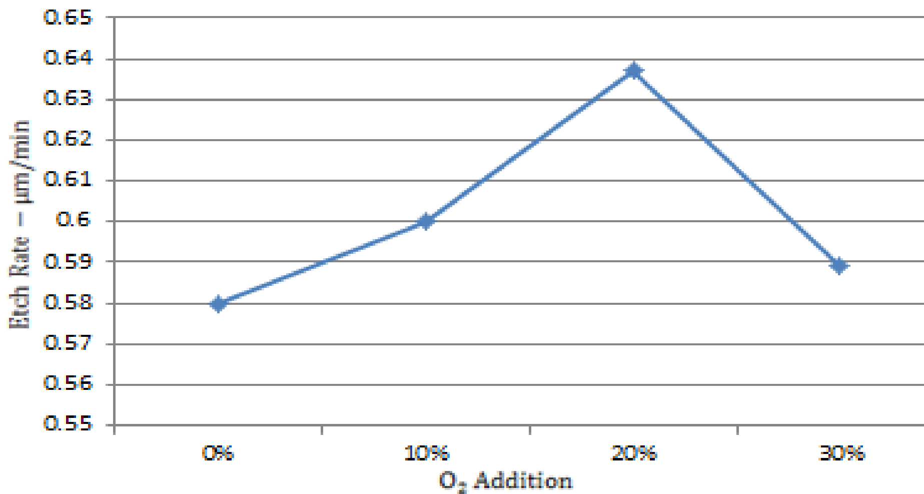


Figure 4.39: Effect of O_2 on the etch rate (ICP power = 500 W, RF power = 60 W, pressures = 10 mTorr)

The other available option that was Ar, a noble gas, was also studied. They possess low chemical reactivity and it was anticipated that the addition of Ar to SF_6 would render the etchant to become less reactive and thereby exposing less chemical damage on SiC. The results obtained demonstrated that the addition of Ar to SF_6/O_2 (Figure 4.40A) or SF_6 (Figure 4.40B) resulted in the smoothest surface across all power ranges without increase the sidewall angles or microtrenches effect. As a result, Ar/SF_6 gas combination was used in this project to etch trenches.

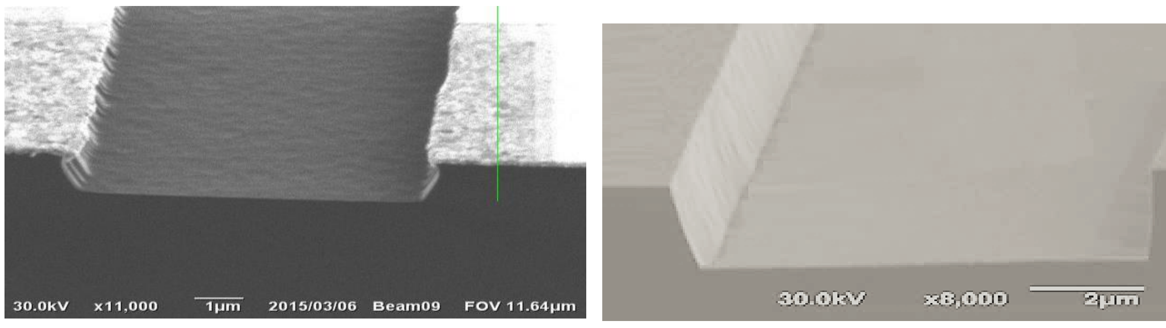


Figure 4.40: SEM images of etch results using (A) Ar/SF_6/ O_2 (1/4/1) (B) Ar/SF_6(1/4)

During this work, it was confirmed that the results are strongly linked to status of the etcher. The ICP-RIE etcher needs to be regularly checked to make sure different part such as ICP power generator, RF power generator, coil and etc. are working properly.

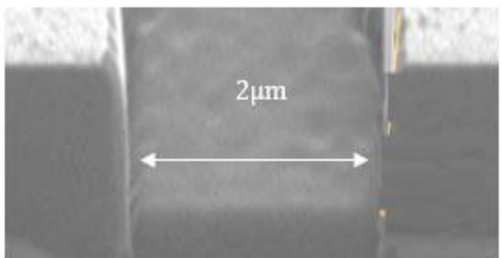
During the three years of experiments, using the same recipe resulted in very different results every six months (on average). The only option was to understand every parameter, study how they affect the trench structure (especially sidewall striation, roughness, microtrenches and sidewall angles), then when any of this issues are observed during etch process, the source could be easily identified and eliminated.

4.5.3 Results:

4.5.3.1 ICP and RF Power

To study the effect of ICP power, the RF power and pressure were kept constant at 60 W and 10 mTorr respectively.

Decreasing the ICP power results in reduced microtrenches size (Figure 4.41) while no clear effect on striation was observed. This agrees with our previous theory that the microtrenches depends on the ions density and by reducing the ions density, the microtrenching effect should be reduced. Increasing the ICP power increases the magnetic field through the ICP-RIE etcher, which results in more collisions in the plasma, between electron and gas ions. This increases the ions density, which subsequently increases the etch rate, while the energy of ions remains unchanged.



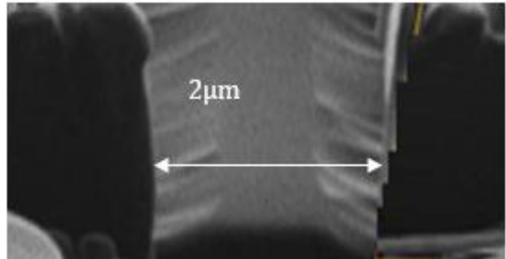


Figure 4.41: SEM images illustrating increase in microtrenches by increasing the ICP power, (a) 200 W and (b) 500 W both at constant working pressure of 10 mTorr and RF power of 60 W

A profound result elucidated was that when ions density is increased (by increasing ICP power), the sidewall angle remains at ca. 80° for ICP power in the range of 200 - 1000 W. This suggests that while microtrenches are linked to

the ions density, the sidewall angles is linked to the ions energy that is controlled by RF power.

The one question that arise from the results is from Figure 4.42D: The bias voltage decreases when ICP power in increased. Further investigation is needed to confirm why this behavior is seen and if the bias voltage is in fact increased, why the sidewall angles were unaffected?

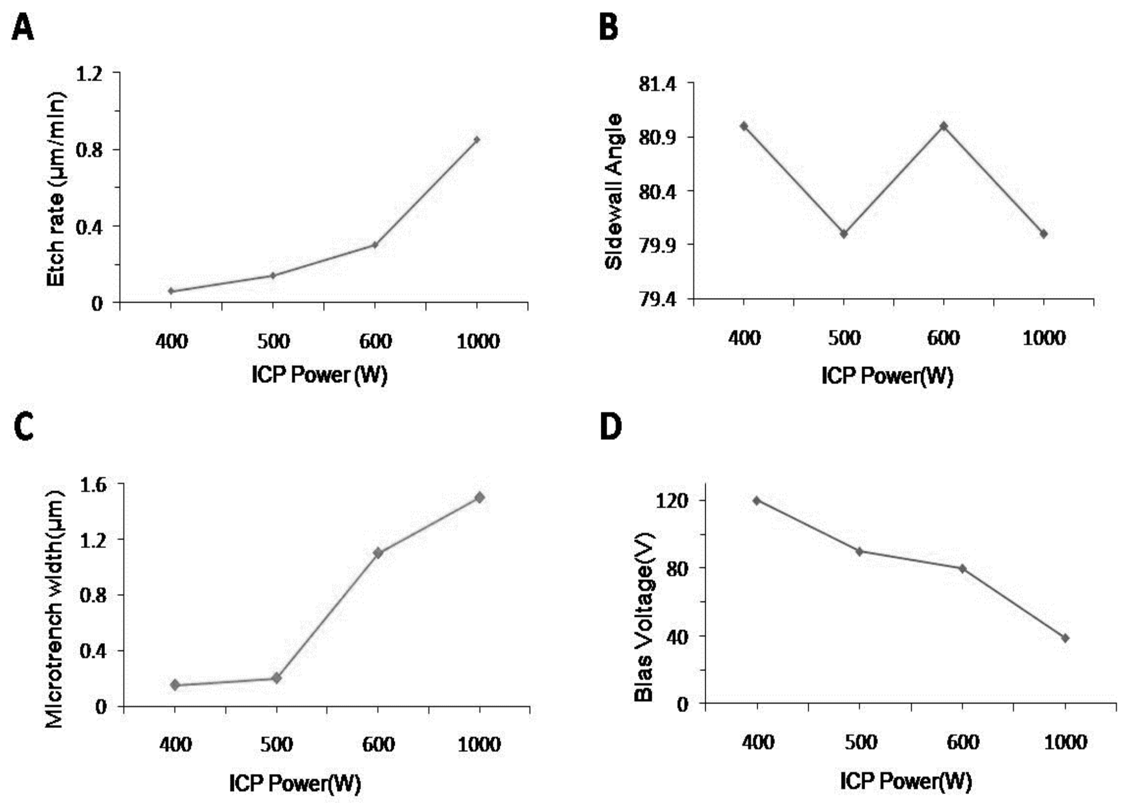


Figure 4.42:Effect of ICP power on (**A**) etch rate (**B**) sidewall angles (**C**) microtrenches width and (**D**) bias voltage (constant working pressure of 10 mTorr and RF power of 60 W)

To confirm the theory that RF power controls the ions density and hence controls the sidewall angles, RF power was studied in the range of 20-80 W. During this experiment ICP power was kept constant at 900 W and the pressure was 10 mTorr.

As expected RF power controls the sidewall angles and DC bias and has no direct effect on microtrenches or striation. The sidewalls are closer to 80° at higher RF power.

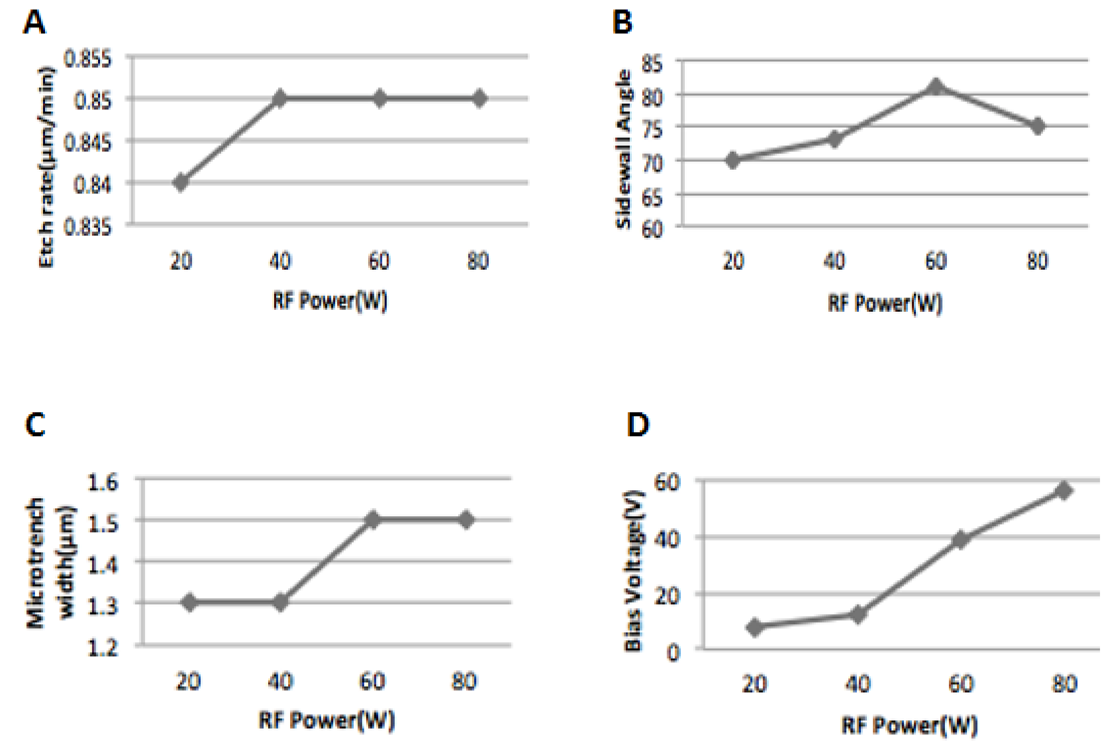


Figure 4.43: Effect of different etch RF power on (A) etch rate (B) sidewall angles (C) microtrenches width and (D) bias voltage (at constant working pressure of 10 mTorr and ICP power of 900 W)

One can conclude that as increasing the RF power, increase the bias voltage connected to the wafer stage, higher RF power creates stronger force to pull the ions toward the wafer. This lateral force can avoid the ions from

spreading and hence limit the ions angular distribution (IAD). Ions angular distribution refers to the spread of ions in X-direction as they move down the etcher [23].

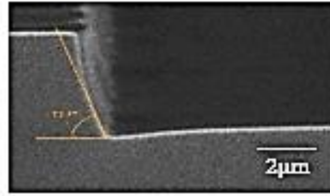
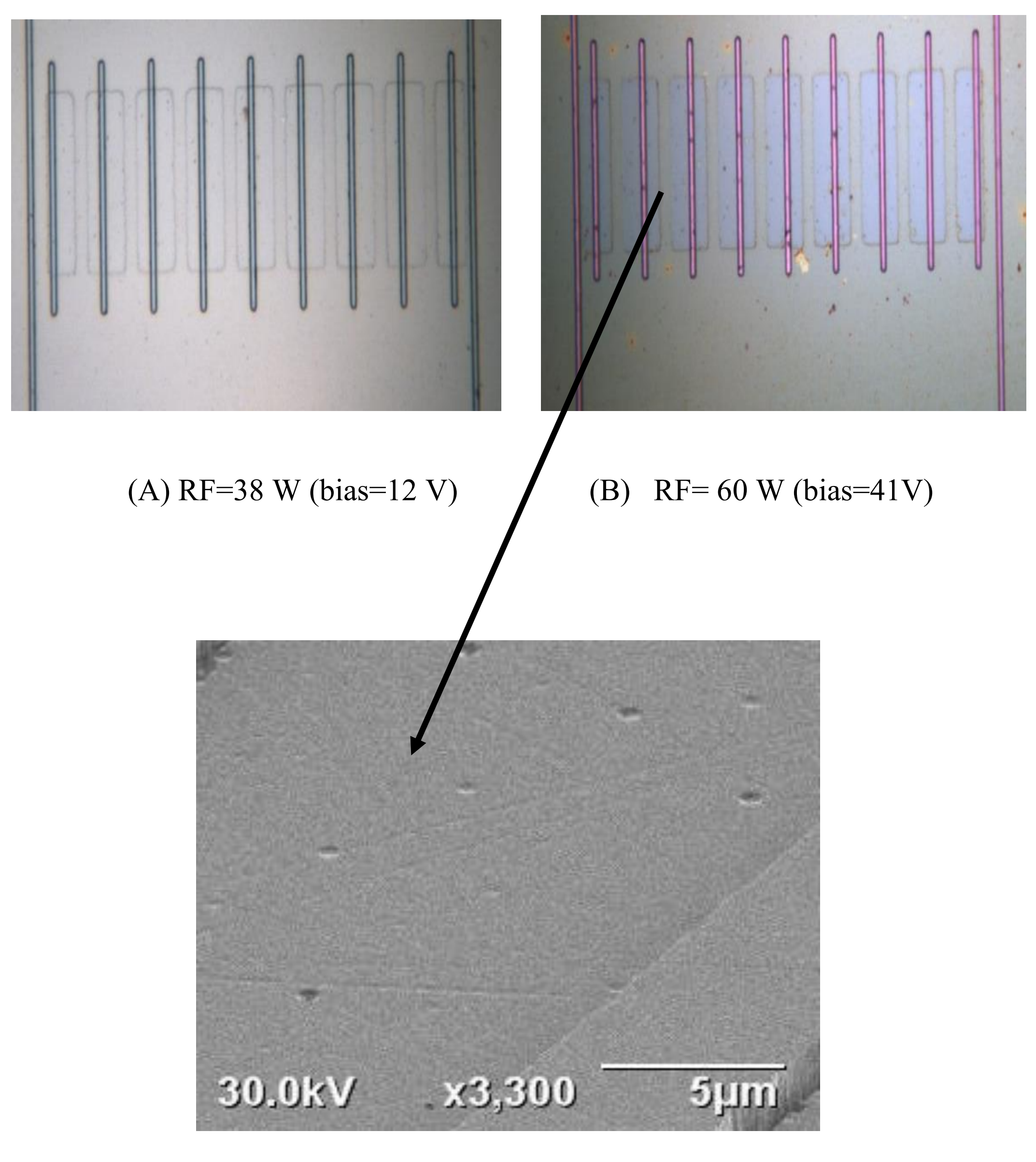


Figure 4.44: SEM images illustrating the effect of RF power on sidewall angles (1) RF=38 W (bias=12 V), (2) RF= 50 W (bias=25V), (3) RF= 60 W (bias=41V) at constant working pressure of 10 mTorr and ICP power of 900 W

Interestingly, increasing the RF power does not induce any effects on either the microtrenches or striation of the sidewalls, this again agrees with the theory that only ions density affect microtrenches regardless of their energy. It can be concluded that microtrenches are the result of chemical etch not physical etch (milling), otherwise if ions with higher energy reach the corners, microtrenching effect should increase.

This theory was further encouraged when milling effects where observed at higher RF power on the trench bottom (Figure 4.45), while the microtrenches size were unaffected.

Milling effects can be due to the fact that at higher RF power, ions possess higher energy, thereby the milling (physical etch) effect of ions increases.

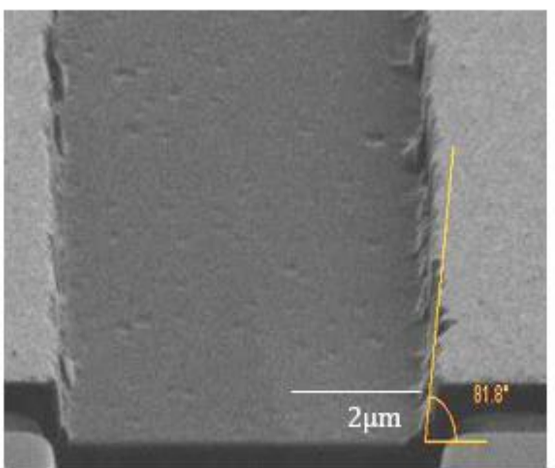


(C) RF= 60 W (bias=41V)

Figure 4.45: Microscopic images illustrating obvious milling effect at higher RF power (B and C) while microtrenches were unaffected. This suggest that microtrenches are not caused by physical etch (milling).

4.5.3.2 Effect of Chamber Pressure

This study has demonstrated that lowering the pressure leads to the elimination of microtrenches. However, this can degrade the striation to an unacceptable level (Figure 4.46A).



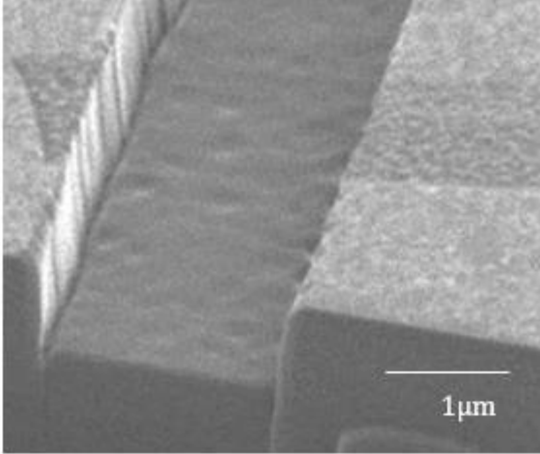


Figure 4.46: SEM images illustrating elimination of microtrenches by decreasing pressure. Sidewall striation is degraded severely. ICP power, RF power are 200W, 60W respectively, with a SF_6/Ar gas combination. Working pressure is (A) 7 mTorr and (B) 10 mTorr.

As the roughness of the bottom of trench is left primarily unchanged (Figure 4.46A), hence the change in ions energy due to pressure does not seem to be the original of very rough sidewall. Furthermore the bias voltage change also confirm that the bias voltage decreases (slightly) at lower pressure (Figure 4.47D) and hence the ions are expected to be less energetic.

As decreasing chamber pressure results in decrease in the concentration of reactive elements [24], it is expected that the etch rate should be decreased this is confirmed by the results in Figure 4.47A.

This agrees with our assumption that in ICP-RIE etch process, which is low ion energy process, the main factor in deciding the etch rate is ions density. We have previously discussed that the ions are attracted to the trench corners in the ICP-RIE etch process. However, from the results it appears as if the pressured is reduced to less the optimum value, the number of ions reaching the trench corners reduces significantly and the trench corner is under-etched.

Figure 4.46A shows that the corners are rounder when the pressure has been decreased. This however cannot explain the very rough sidewall at lower pressure and further study is needed to investigate this.

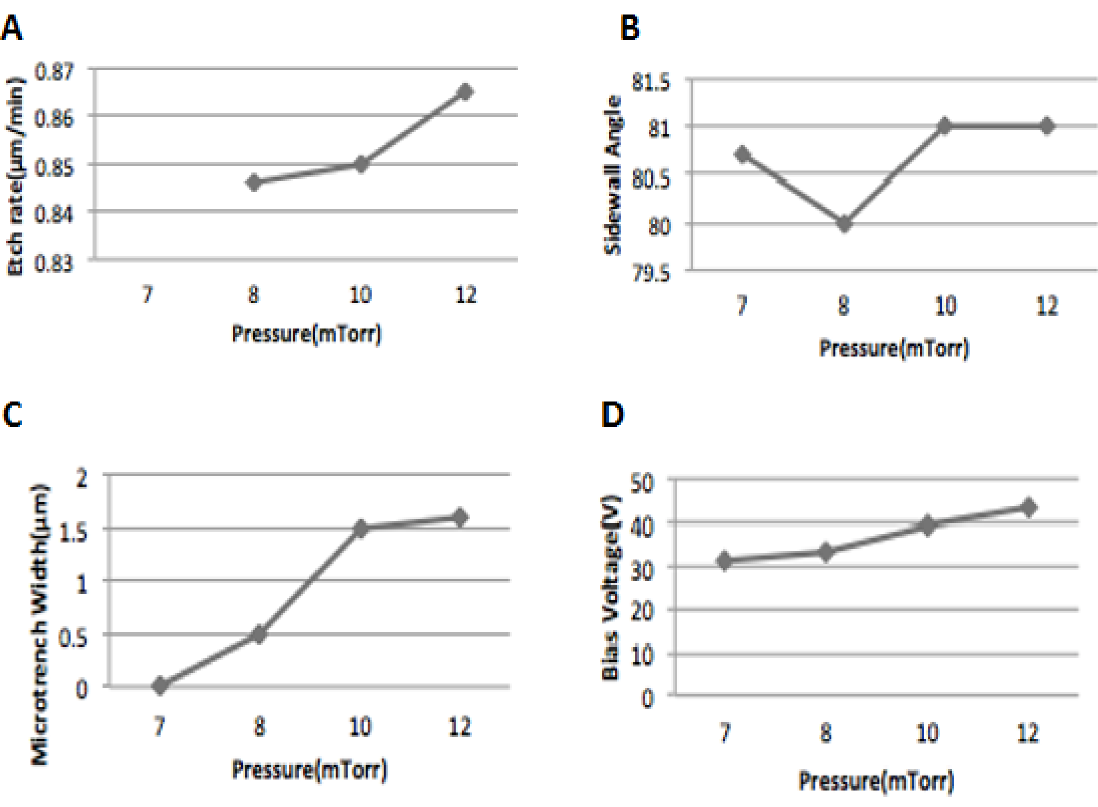
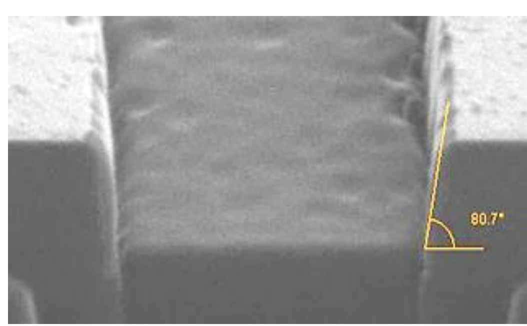


Figure 4.47:Effect of different etch pressure on (A) etch rate (B) sidewall angles (C) microtrenches width and (D) bias voltage

The results also demonstrate that sidewall angles are unchanged by the change of pressure and are all in the range of 80°-81° for the pressure between the ranges of 6-15 mTorr (Figure 4.47B, Figure 4.48).



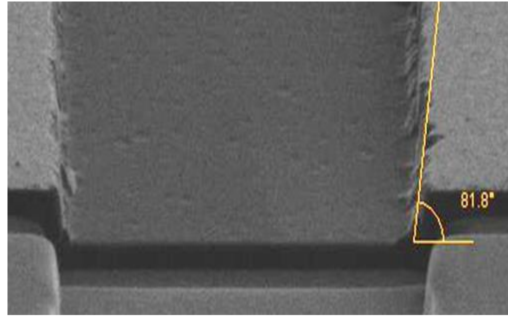
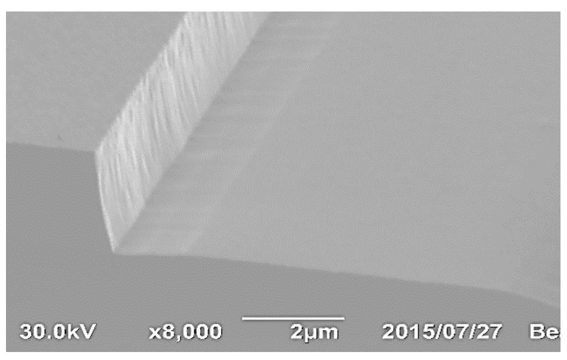


Figure 4.48: SEM images illustrating that sidewall angles are unaffected by the pressure. ICP Power is 200 W, with a SF_6/Ar gas combination. Working pressure is (A) 10 mTorr and (B) 7 mTorr

For the purpose of this work, it was decided not to use reduction in pressure as a mean to eliminate microtrenches and simply optimize microtrenches through the choice of mask and ICP power as described before and hence pressure of 10 mTorr was used to fabricate trench structures in this work.

From the results achieved in this section it is concluded that there is an optimum ICP and RF power that needs to be chosen carefully to achieve straight sidewalls, with smooth trenches, free of microtrenches. At pressure of 10 mTorr using SF_6 and Ar (50 SCCM and 40 SCCM respectively), RF power of 60 W and ICP power of 900 W results in the best trench structure using Ni mask. The same recipe, using SiO_2 mask results in Figure 4.49A.



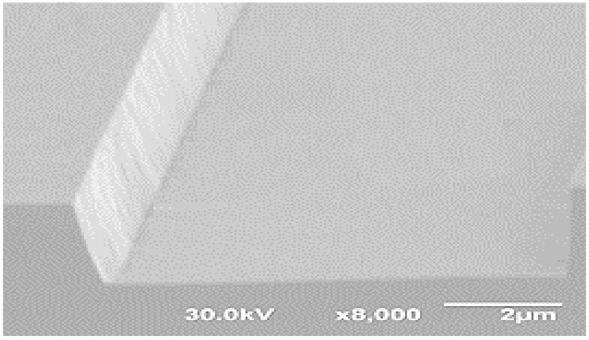


Figure 4.49: SEM images illustrating microtrench effect in SiC using SiO_2 mask (B) after optimising etch recipie to achive bigger overshadow and hence minimise microtrench effect

To eliminate the microtrenches completely, the RF power was reduced to 55 W that decreased the sidewall angles to 78° and provides an enhanced protection of the sidewalls, hence the microtrenches were eliminated as can be seen in Figure 4.49B. At this RF power no milling effect was observed. The etch rate is around 830 nm/min. This recipe has been used to create trenches in trench MOSFETs in this work.

4.6 Conclusion

To conclude, the results in this chapter demonstrate that both ICP power and pressure directly affect microtrenches. Additional factors such as gas combination can also slightly degrade microtrenches. Microtrenches is best optimized by a combination of mask material and etch recipe. An accurate recipe can provide overshadow on the sidewall. This is essential as other alternative use low ICP powers which result in very low etch rates.

Striation is primarily caused by photolithography process and the only parameters that can degrade striation, after photolithography, were determined to be (1) mask material and (2) pressure. This study demonstrated that SiO_2 is the best mask material that minimizes striation. It was demonstrated that the etch rate was dependent on ICP power above other parameters. Whereas, sidewall angles were dependent on the RF power.

4.7 References

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Chapter

5

Fabrication and Characterisation of 4H-SiC trench MOSFETs

5 Introduction

The main focus of this chapter is not to achieve best parameters such as mobility or breakdown voltage. Instead the author has tried to understand the effects of different oxidation and treatments methods that are commonly used on the electrical parameters. During the literature review, it became clear that most researches have focused on mobility and breakdown voltage and have ignored other aspects of a functional and reliable trench MOSFETS. A trench MOSFET with very high mobility is not functional if the leakage current is high. There are not many resources to find the effect of oxidation process on all the

electrical parameters. Hence the main focus of this chapter was to understand how electrical parameters such as current density, breakdown voltage, mobility, gate leakage current, source leakage current are affected by the oxidation process.

This chapter is divided into three sections. In the first section, characterisation techniques used in this chapter to characterise trench MOSFETs are introduced. In section 5.2, the fabrication process of 4H-SiC trench MOSFETs is explained in details and in the last section, 5.3, electrical measurement results on the fabricated devices are presented.

5.1 Characterisation techniques

Characterisation techniques are used to extract information about properties of semiconductors. In this work, various techniques have been used to compare different fabrication processes with each other, with the aim to select the best process. Characterisation techniques provide two types of information about semiconductors: physical properties and electrical properties.

Techniques such as scanning electron microscope (SEM) have been used to evaluate the physical properties of the trench such as the trench depth. Other physical techniques such as atomic force microscopy (AFM) can be used to measure surface roughness, though since the channel is formed on the trench sidewall, instead of spending the time correlating measurement using AFM, we

have used SEM to calculate average peak to peak striation for different samples to study the effects of fabrication process on roughness. Then the best results were chosen and electrical measurement were used to compare the results without studying the effects of roughness.

Electrical characterisation techniques such as current-voltage measurements, threshold voltage, leakage current, mobility and other measurements were the main focus of this section and these techniques have mainly been used to evaluate performance of the trench MOSFETs. This is simply because physical properties such as roughness should be further studied by electrical measurement to decide the nature of their effects on the device performance.

This chapter has used experimental method. The focus is to use experiments and measurements to find the recipe to fabricate MOSFETs with the lowest leakage current and highest mobility and breakdown voltage.

5.1.1 Scanning electron microscope (SEM)

SEM is used to visualise Nano-scale and Micro-scale devices. SEM uses electrons instead of light to form an image. SEM has much higher resolution (up to nm) compared to the conventional microscope and hence can be used to magnify very small specimen in Nano and Micro-level. SEM has been used to

measure the trench depth, width and other physical properties such as the shape of trench corners. Also using SEM, we have measured the peak-to-peak striation of trench sidewalls that were presented in Chapter 4.

Figure 5.1shows a picture of a typical SEM arrangement. Zeiss Supra 55-VP FEG-SEM has been used in this work to capture images of trench structures.

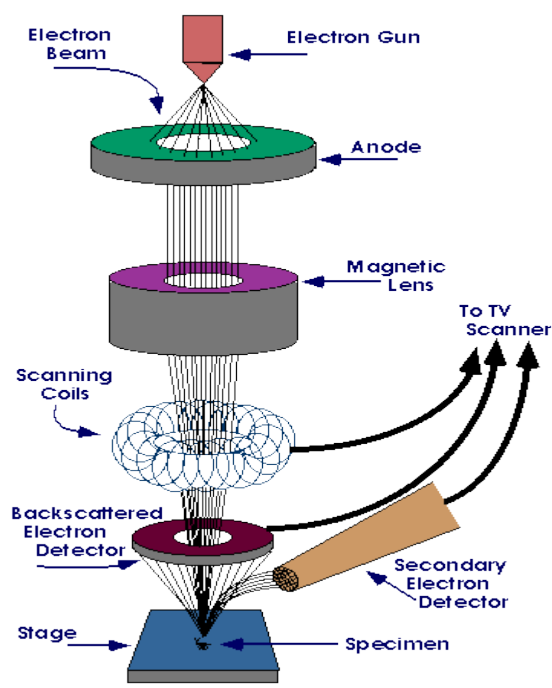


Figure 5.1: Components of an SEM (Courtesy of Iowa State University)

SEM scans a sample by using a focused beam of electrons. The electron gun at the top of SEM produces a beam of electrons. The electron beam is accelerated in a vertical path (in a vacuum) due to a high voltage which is applied at the anode. A series of magnetic lenses in the SEM focus the electrons beam toward the sample as it moves down the column. The focused electrons beam then

reaches the scanning coil. The scanning coil deflects the beam so that it can scan the surface in the X and Y direction. The specimen is located on a vacuumed stage that is equipped with tilt and rotation. This is important as without tilting the samples, pictures of trenches could only be 2-dimentional and hence information such as the depth of the trench could not be determined. When the beam reaches the specimen, ejected electrons and X-rays (Figure 5.2) are collected by the SEM detectors and converted to a signal readable by the screen [1].

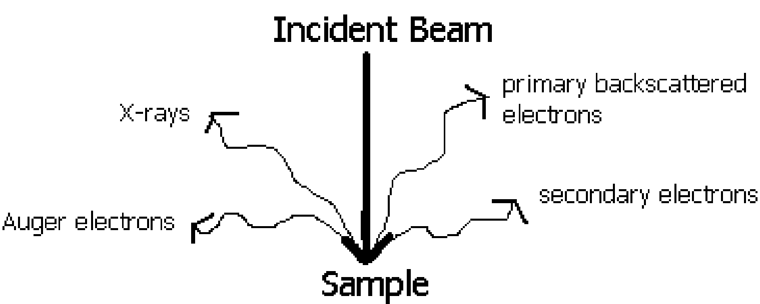


Figure 5.2: Ejected electrons X-rays from the samples after beam incident [1]

The main two types of electrons used for imaging are: (1) primary backscattered electrons and (2) secondary electrons. Primary electrons are high energy electrons that are backscattered by the sample's atoms [2]. The amount and direction of backscattered electrons depends on the specimen and hence compositional information could be concluded. These electrons are usually collected using semiconductors or scintillators detectors. The downside of

backscattered electron detector is that the quality of the image depends on the material.

On the other hand, a secondary electrons detector offers resolution independent of the material. Secondary electrons are low energy electrons that are ejected from the k-shell of atoms of the specimen in response to the inelastic scattering interactions with the beam. Everhard-Thornley detectors are usually used to collect secondary electrons. A Faraday cage is used to accelerate the electrons toward a scintillator. This results in a current that is amplified using photomultiplier. The amplified electrons can be viewed on an analogue video display.

SEM can cause sample charging and therefore it is recommended to make electrical measurement before using SEM. Alternatively the sample could be coated by a conductive material such as metal, to avoid sample charging. Sample charging results in blurry pictures.

5.1.2 Current-Voltage Measurement

Current-Voltage (I-V) measurement is a key technique in evaluating MOSFET electrical characteristics. I-V measurements are used to calculate different semiconductors' parameters such as current density and on resistance. The I-V curve is measured by applying voltage between the gate contact and source contact (V_{GS}), while sweeping the voltage between drain and source (V_{DS}) and measuring the drain current ((I_D). In an ideal MOSFET, if V_{GS} is less than a

voltage that is called threshold voltage (V_{Th}), the drain current will be zero. By increasing V_{GS} the drain current will increase.

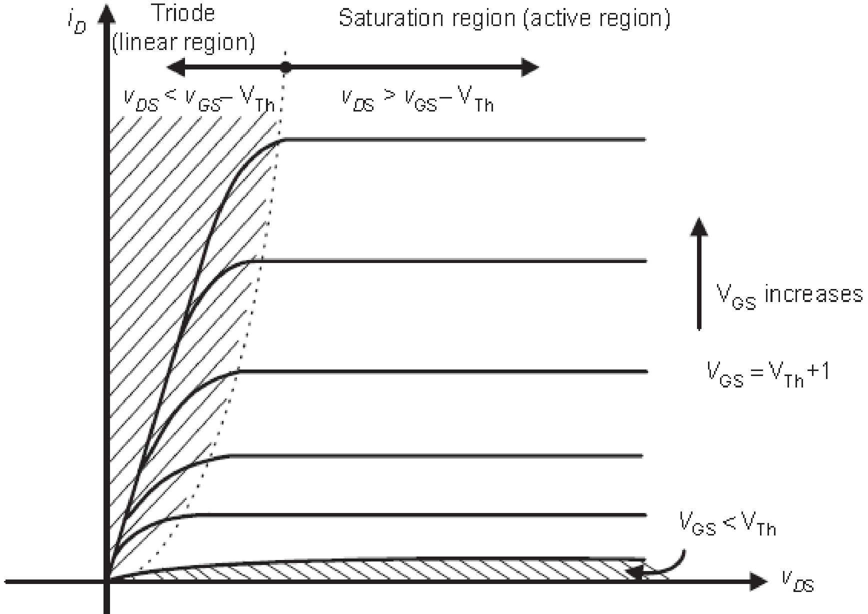


Figure 5.3: Typical I-V characteristics of MOSFET

In the cut-off region, the applied gate voltage is less than threshold voltage (V_{GS}<V_{Th}) and the device is off and there is no current conduction between source and drain. In reality there is small leakage current that is called subthreshold leakage current. The current in this region depends on the threshold voltage and hence any process that affects the threshold voltage value can affect the value of leakage current.

In the linear region V_{GS}> V_{Th} , but the applied drain voltage is very small (V_{DS}< $V_{GS} - V_{Th}$). The device is turned on and the current channel is created and

therefor there is a current flow between source and drain, though as can be seen the current is dependent on V_{DS} in this region.

In the saturation region, gate voltage is more than the threshold voltage (V_{GS}>V_{Th}) and also the drain voltage is comparable to the gate voltage (V_{DS}>$V_{GS} - V_{Th}$). As the gate voltage is higher than the threshold voltage, the channel has been created and there is a flow of current between source and drain. As can be seen in the Figure 5.3, the drain current in this region is primarily controlled by gate voltage and increases as the square of the gate voltage.

5.1.3 Threshold voltage measurement (V_{Th})

Threshold voltage is important to determine the on and off state of the device. Linear extrapolation method has been used to measure the threshold voltage. In this technique, drain voltage was kept constant at a very low value (50 mV) and the drain current is measured as a function of gate voltage. Low drain current ensures that the MOSFET is operating in the linear region.

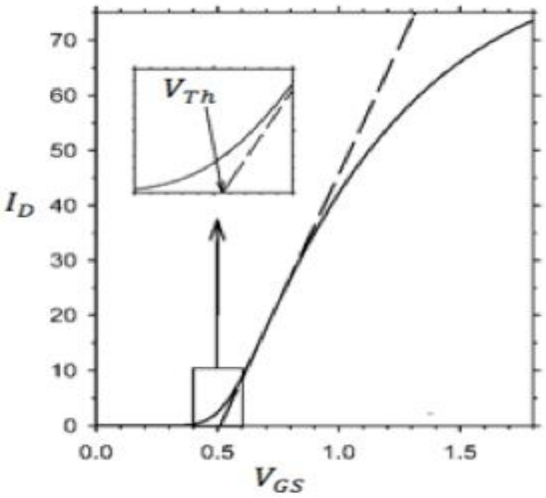


Figure 5.4: Threshold voltage measurement using $I_D - V_{GS}$ graph

As shown in Figure 5.4, the drain current versus gate voltage is extrapolated to I_D =0 and the threshold voltage is determined from the extrapolated point on V_{GS} axis. The exact value is $V_{Th} = V_{GSi} - V_{DS}/2$, where V_{GSi} is the extrapolated point. V_{DS} is ignored since the value of is very small.

In reality the I_D-V_{GS} curve is not straight, due to leakage current and degraded resistance and mobility above threshold voltage. Therefor a straight line is fitted to the I_D-V_{GS} and used for extrapolation. The threshold voltage can be measured in both linear and saturation regions. In saturation region, the current is given by

$$I_D = \frac{\mu_n C_{OX}}{2} \frac{W}{L} (V_{GS} - V_{Th})^2 \qquad \text{Equation (5.1)}$$

I_D is directly related to V_{Th}^2, therefor the square root of I_D is plotted against V_{GS} and the curve is extrapolated to I_D=0. The advantage of using this equation is that the I_D-V_{GS} curve is usually much more straight and hence easier to fit a straight line to it. In this project threshold voltage is calculated from $\sqrt{I_D}$-V_{GS} graph.

5.1.4 Field Effect Mobility ($\boldsymbol{\mu_{FE}}$)

One of the main challenges with 4H-SiC power semiconductors is the low channel mobility. Therefore one of the primary focuses of this work was to improve the field-effect mobility (μ_{FE}) of the device. μ_{FE} is derived from gate transconductance,g_m, defined by

$$g_m = \frac{\partial I_D}{\partial V_{GS}}|_{V_{DS}} \qquad \text{Equation (5.2)}$$

The drain current is the total of drift current and diffusion current. Mobility is measured at very low V_{DS}(50mV in this study), where the diffusion is minimum; therefore we can ignore diffusion current and assume the drain current to be

$$I_D = \frac{W}{L}\mu_{FE}C_{OX}(V_{GS} - V_{Th})V_{DS} \qquad \text{Equation (5.3)}$$

This results in

$$g_m = \frac{W}{L}\mu_{FE}C_{OX}V_{DS} \qquad \text{Equation (5.4)}$$

And therefore μ_{FE} could be calculated from the following equation:

$$\mu_{FE} = \frac{g_m L}{W C_{OX} V_{DS}}$$ Equation (5.5)

Where W is the channel width and L is the channel length. As mentioned in the literature review the value of drift resistance is quite high in voltages close to 1000V. The calculation described in this section does not exclude the drift resistance and hence the value of motilities achieved will be lower as they are also affected by the drift resistance. Though as the structure is kept constant and all MOSFETs were fabricated on the same wafer, during all the experiment, the drift resistance is constant and hence the difference in the motilities is a reflection of the channel mobility. This method has been used to compare different recipes to achieve the best oxidation recipe. Though it is recommended that the accurate value of mobility should be measured when junction termination is added to the device. The method to measure the accurate mobility is described in Chapter 6, recommendation.

5.1.5 Current Density

Current density is defined as the current flowing per unit area of MOSFET and is defined as:

$$I_{D/cm^2} = \frac{I_D}{A}$$ Equation (5.6)

Current density is an important factor in designing electrical circuits. Current density depends on the device area and hence it is important to achieve a higher current density as it means higher number of devices can be fabricated in smaller area.

5.1.6 Drain to Source On State Resistance ($R_{DS(on)}$)

On resistance is the resistance of the device in the on state. On resistance of a trench MOSFET is the sum of substrates resistance (R_{subs}), N- epi layer resistance (R_{epi}), P-N accumulation region resistance (R_{acc}), channel resistance (R_{ch}) and n+ source resistance (R_{s}) as can be seen in Figure 5.5.

$$R_{DSON} = R_{subs} + R_{epi} + R_{acc} + R_{ch} + R_s \qquad \text{Equation (5.7)}$$

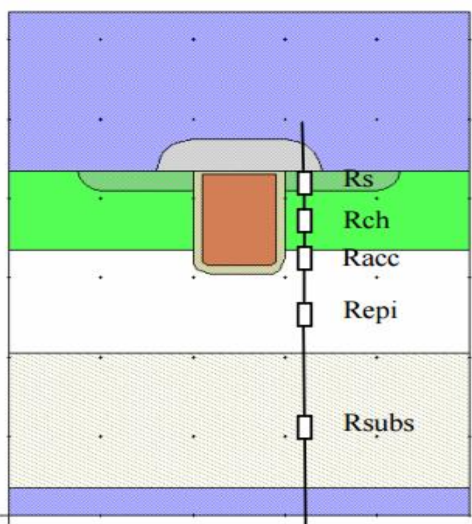


Figure 5.5: Drain source on resistance components on a trench MOSFET [3]

Channel resistance is given by [4]

$$R_{ch} = \frac{LW}{2\mu_{inv}C_{ox}(V_G - V_{TH})} \qquad \text{Equation (5.8)}$$

where L is the channel length, W is the channel width, and μ_{inv} is the inversion layer mobility. The resistance contributed by accumulation region is given by

$$R_{acc} = K_A \frac{L_A W_{cell}}{2\mu_{acc}C_{OX}(V_G - V_{TH})} \qquad \text{Equation (5.9)}$$

where K_A is accumulation region coefficient that accounts for the current spreading from this layer to drift region[4], which is usually around 0.6 in trench MOSFET, L_A is the accumulation layer path and μ_{acc} is the accumulation layer mobility. The epi-layer (drift region) resistance is given by

$$R_{epi} = \frac{\rho_D W_{cell}}{2} ln\left[\frac{W_T + W_M}{W_T}\right] + \rho_D\left(t + x_{JP} - t_T - \frac{W_M}{2}\right) \qquad \text{Equation (5.10)}$$

Where W_T is the trench width, W_M is the distance between two trenches, t is the drift region thickness, t_T us the trench depth, x_{JP} is the P-base junction depth and ρ_D is the resistivity of the drift region. The other types of resistance are smaller compared channel, accumulation and drift region resistance and can be ignored in the calculation [4].

Figure 5.6 represents the specific on resistance versus breakdown voltage for SiC trench MOSFETs in comparison with planar SiC MOSFET and Si MOSFETs [4]. As can be seen, as we move to higher voltages, the specific on resistance becomes closer to the theoretical (ideal) value. At voltages higher than 5000V, the drift region rather than the channel dominates the total

resistance of the trench MOSFET. This bodes well in that high power trench MOSFET devices in SiC have the potential to achieve ideal on resistances that are 100 times lower than their equivalent Si counterparts.

At voltages less than 1000V, the channel resistance is the dominant resistance of the device and since channel resistance is highly dependent upon the inversion channel mobility at the SiO_2/SiC interface (Equation 5.8), the inversion mobility plays an important role in the optimising the resistance of the device [4].

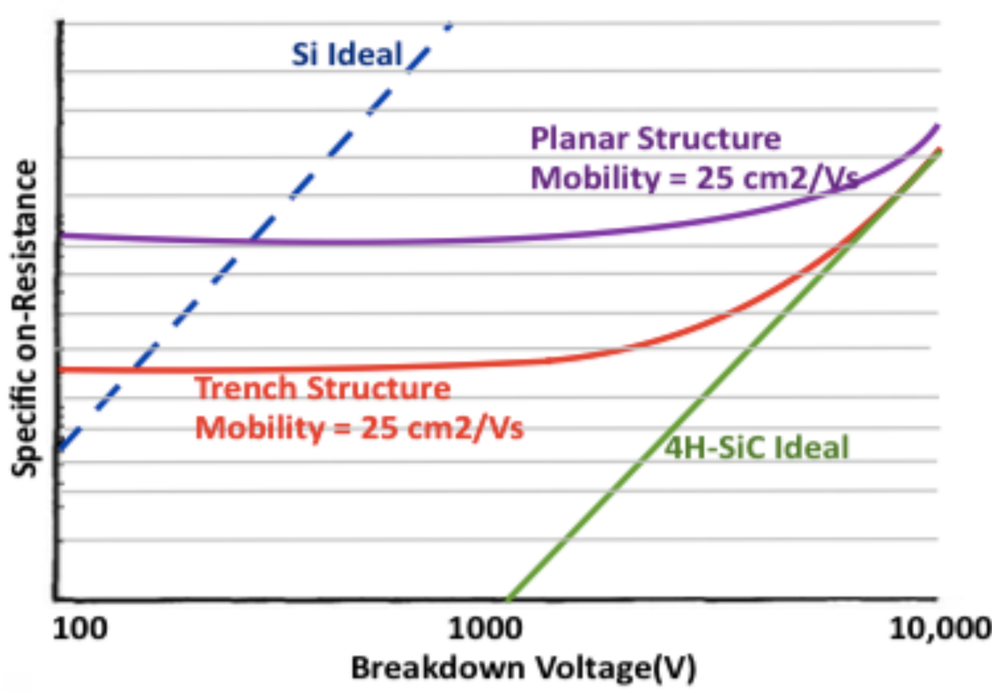


Figure 5.6: Trench MOSFET specific on-resistance vs. breakdown voltage for varying channel mobility[4]

The lower the resistance (in addition to higher field effect mobility) results in higher switching speed. $R_{DS(on)}$ is calculated in linear mode of operation and is given by:

$$R_{DS(on)} = \frac{V_{DS}}{I_D} \qquad \text{Equation (5.11)}$$

Which is the inverse slope in the linear region, so the steeper the I-V graph is in the linear region, the smaller is the on resistance.

5.1.7 Leakage currents

Zero gate drain current ($\boldsymbol{I_{dss}}$) is the drain source leakage current during the off state (when V_{GS} is zero). This measurement is made at a specified drain voltage. This current increases with temperature. This is an important factor as it contributes to leakage power loss. Leakage power loss is calculated as I_{dss} times V_{DS} and is usually negligible.

Gate source leakage current (I_{gss}) is the leakage current that flows through the gate. I_{gss} is measured by shorting the drain and source contacts and increasing the gate voltage to it is maximum. This current is independent of the temperature. The leakage current through the gates depends on the quality of the oxide. The sources of leakage current were discussed in Chapter 1.

5.1.8 Breakdown Voltage (V_{br})

Breakdown voltage is the V_{DS} of a MOSFET that causes the device to enter into breakdown region. At this region the drain current increases drastically. The breakdown curve of a MOSFET is shown in Figure 5.7.

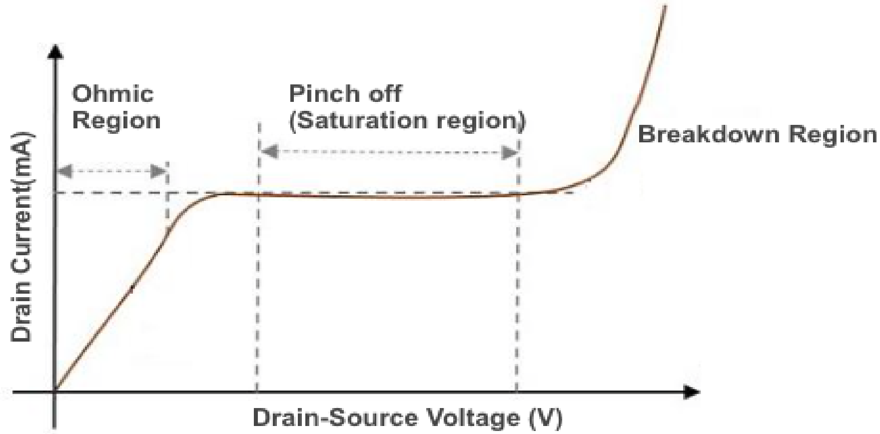


Figure 5.7: Breakdown characteristic of a MOSFET

5.2 Fabrication Process of 4H-SiC Trench MOSFET

A prime grade wafer was bought from Norstel with the following parameters listed in the Table 5.1. The original SiC wafer was bought from Norstel with Si-face surface, and the experiments were done with the trenches fabricated on a-face, $11\bar{2}0$ plane, as it's been reported to result in the highest mobility in different studies [5]. $11\bar{2}0$ plane can be found in respect to the major flat of the wafer. In case of the wafer order from Norstel, this plane was the perpendicular plane to the major flat (Figure 5.8). This information could be found the data sheet provided by the manufacturer.

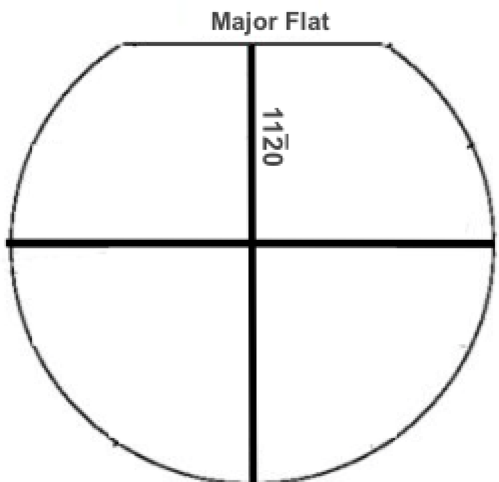


Figure 5.8: The major flat is used to identify the $11\bar{2}0$ plane on the wafer

As mentioned, we expect a breakdown voltage of 350V without any junction termination using this wafer (as presented in chapter 2).

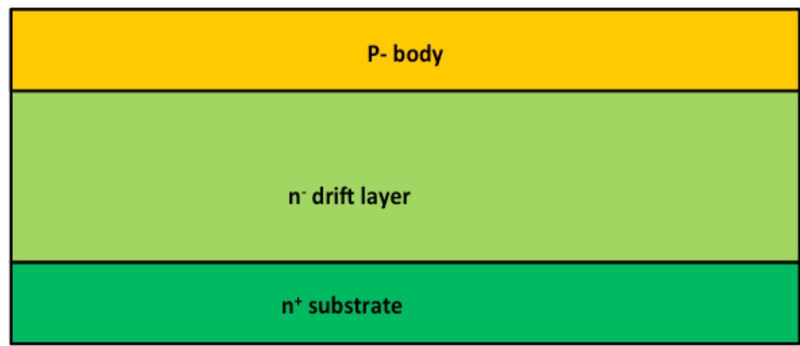
Layer	Properties	Value	Unit
Layer 1: n+ drain (n+ substrate)	Doping	1×10^{19}	cm^{-3}
	Thickness	0.5	µm
Layer 2: N- drift	Doping	9.42×10^{15}	cm^{-3}
	Thickness	15	µm
Layer 3: P- body	Doping	1×10^{17}	cm^{-3}
	Thickness	2.1	µm

Table 5.1: Properties of the SiC wafer

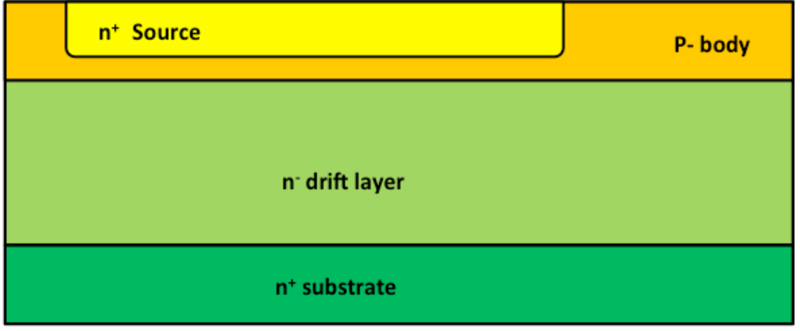
The fabrication process of trench MOSFET began with a simple sample preparation and cleaning, and then the alignment marks were etched on the sample surface (Figure 5.9A). The n^{+} source was implanted in the next step (Figure 5.9B). In the next step (Figure 5.9C) a layer of TEOS oxide was deposited on the surface to act as the mask for gate trench etching. Gate trench was then etched in the sample (Figure 5.9D) using oxide as the mask layer.

In step E (Figure 5.9E) a layer of sacrificial thermal oxidation was grown on the sample and was removed, this step is necessary to smooth the surface and round the trench corners. Gate oxide was thermally grown in the next step

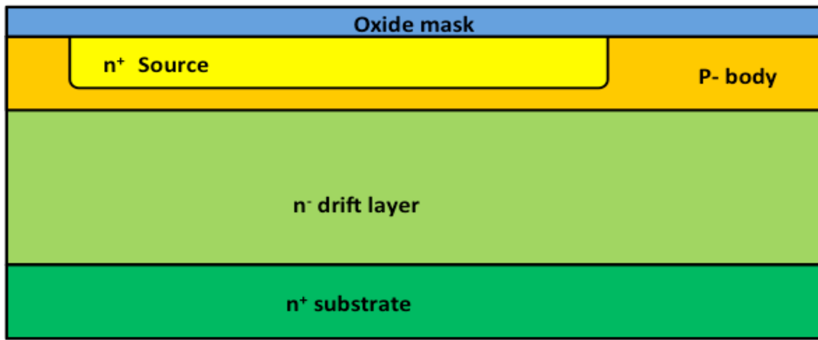
(Figure 5.9F). After that, the gate oxide was patterned to open space for source/body and substrate (drain) contacts (Figure 5.9G). The source/body and substrate (drain) contacts are deposited on the sample in the next step (Figure 5.9H) and the sample was annealed to activate the contacts. In the last step (Figure 5.9I) gate metal was deposited on the gate oxide.



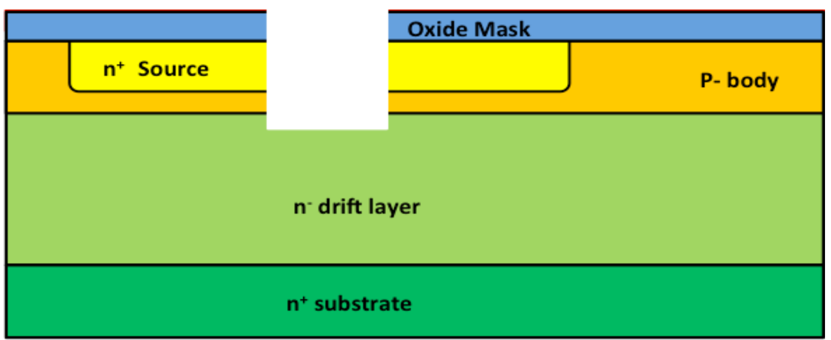
5.9(A): First step is sample preparation and cleaning, and then the alignment marks are etched on the sample surface (P- body)



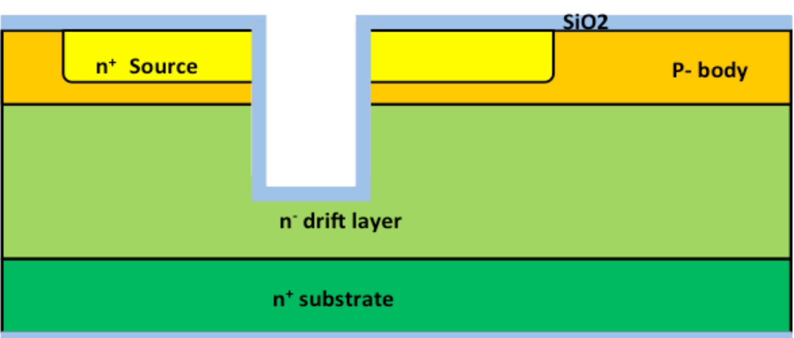
5.9(B): The n^+ source is implanted



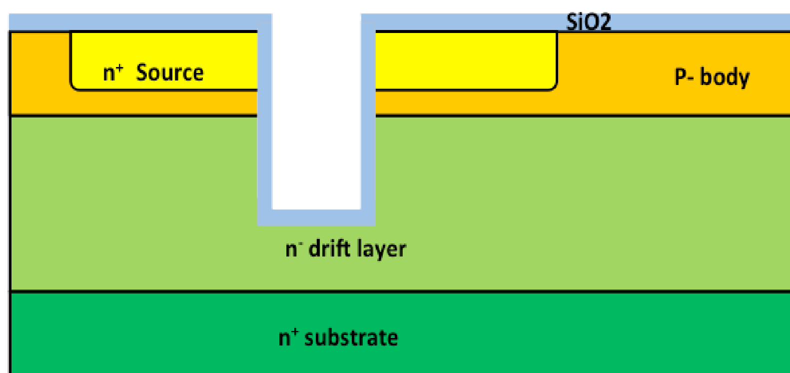
5.9(C): A layer of TEOS oxide is deposited on the surface to act as the etching mask



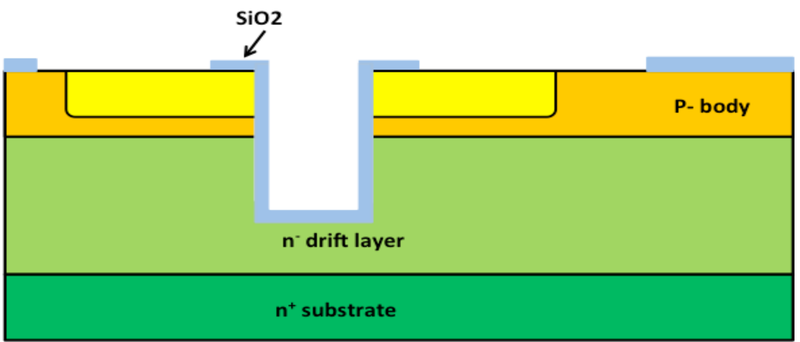
5.9(D): Gate trench is etched



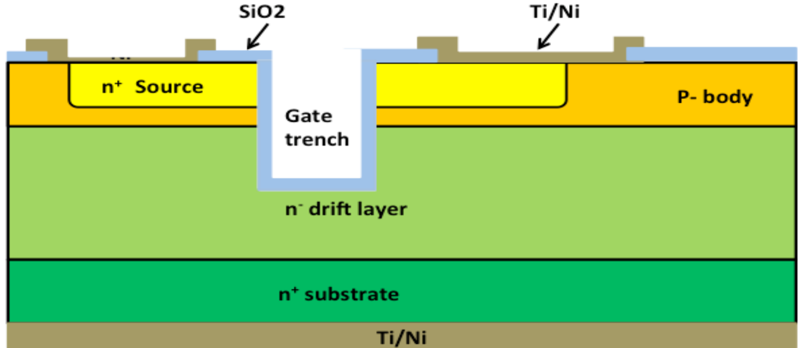
5.9(E): A layer of sacrificial thermal oxidation is grown on the sample and is removed. This steps help to round the corners



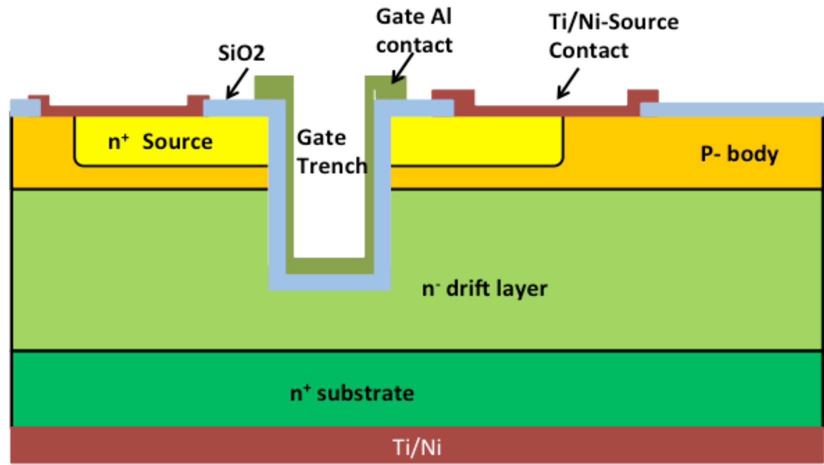
5.9(F): Gate oxide is thermally grown in high temperature furnace



5.9(G): The gate oxide is patterned to open space for source/body and substrate (drain) contacts



5.9(H): The source/body and substrate (drain) contacts (Ti/Ni) are deposited on the sample and annealed to activate the contacts

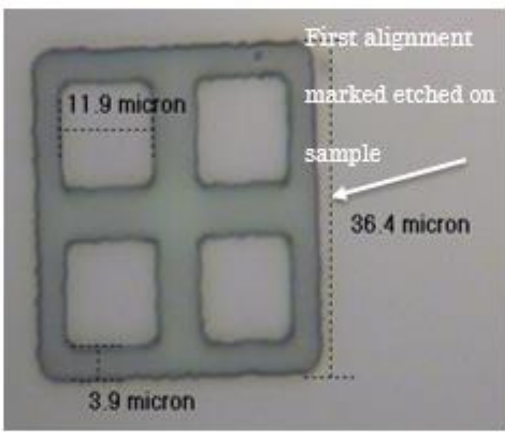


5.9(I): Al Gate metal is deposited on the gate oxide

Figure 5.9: Step by step overview of fabrication process of 4H-SiC trench MOSFET

5.2.1 Alignment marks

Alignment marks are used to align the patterning mask on the sample during photolithography process. Every photolithography mask has alignment marks on them that will be aligned to the previous marks. Figure 5.10A shows the first alignment mark on the sample and 5.10B is the same alignment mark at the end of the process. The silver rectangle shows the gate metal alignment marks that are aligned to the opposite windows on the original mark.



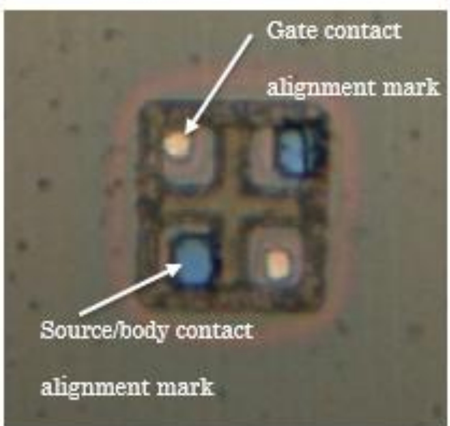


Figure 5.10: Microscopic image of (A) First alignment mark (B) alignment marks at the end of the process

Alignment marks must be carefully designed for the trench MOSFETs. This is due to the fact that as can be seen in Figure 5.9I the source and gate contacts are located very close to each other. To achieve a trench MOSFET with high current and breakdown voltage, the trenches are usually located 1 µm apart. This high resolution is more problematic especially if finger design (where source and gate contacts are strip such as Figure 5.9 is used. This is due to the fact that the metals contacts are very close to each other and any misalignment can result in shorting the gate and the source contacts and hence the device will not function properly.

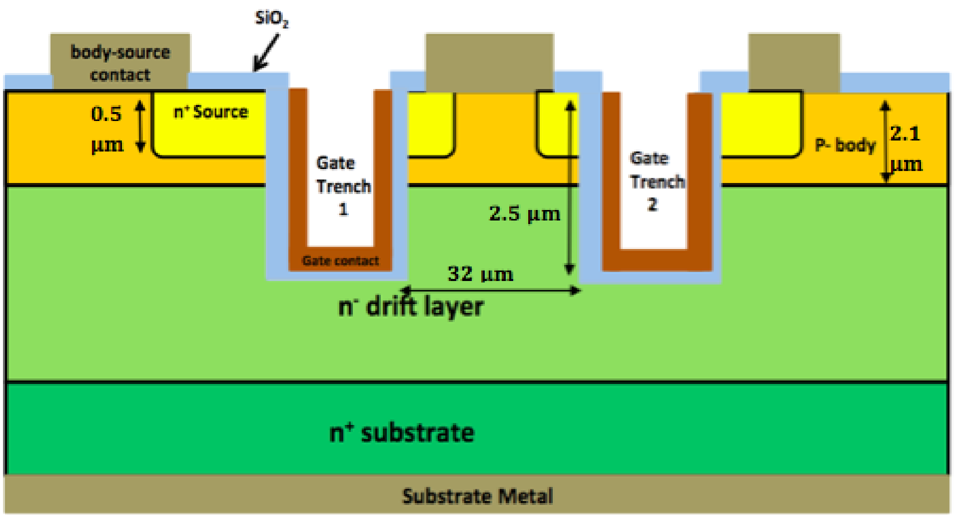


Figure 5.11: Structure of 1.2Kv trench MOSFET fabricated in this work

When alignment marks with a large distance between alignments marks are used (Figure 5.12A), misalignment is harder to inspect because of visual judgement error. Both 5.12A and 5.12B are misaligned toward the left and the bottom by the same distance, though this is more obvious in case of 5.12B.

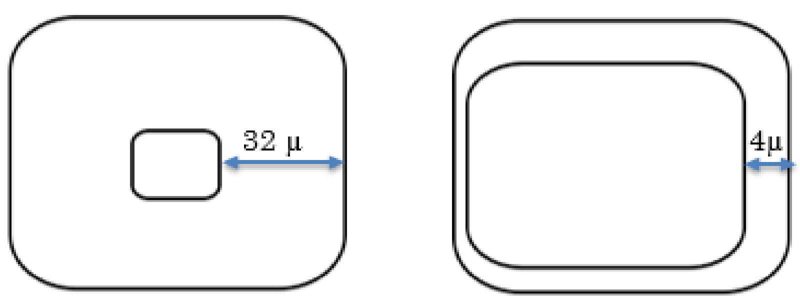


Figure 5.12: Comparison of two different sizes of alignment marks, the inner rectangle in both (A) and (B) is misaligned toward the left and the bottom by the same distance, but misalignment is more obvious in case (B)

Without the correct alignment marks, it is impossible to achieve high resolution. This is due to the fact that when gates are only 1-2 μm apart, there is no place for misalignment error. In such devices, even if the gate contact is misaligned toward left or right for 0.5 μm, it can create a short circuit between the gate and the source contacts. Therefore it is extremely important to design corrects alignment marks for such devices. Based on the results from this work, alignment marks with maximum distance of 4 μm from each other is suggested in Warwick University cleanroom (Figure 5.12B). The resolution is limited by the microscope on the mask aligner.

5.2.2 Source Implantation

The next step is the n^+ source implantation. The mask used for source implantation was (Tetraethyl orthosilicate) TEOS oxide. TEOS was deposited using Tetreon (Thermco) LPCVD system that is used to deposit high quality oxide film. The oxide was annealed in Argon (Ar) at 1000 °C for 1 hour as described in the previous chapter to increase the density and make sure there are no micro size holes in the TEOS.

There are three steps in source implantation: (1) simulation, (2) implantation, and (3) activation. The implantation was first simulated using SUSPRE software [6]. This software is used to simulate how far the ions can reach in the material when implanted. Nitrogen was used to create the n^+

source. It is important to achieve high density of ions concentration in the SiC surface as it helps to make better ohmic contacts.

The concentration in SiO_2 layer is also simulated to make sure the thickness of SiO_2 mask layer is enough to block the ions from the areas that are not supposed to be implanted. Multiple implantations has been used to achieve a box shaped profile for the n+ sources. The energy and dosage of each implantation are listed in Table 5.2. The resulting nitrogen ion profile, in both SiC and SiO_2 based on simulation are shown in Figure 5.13 and 5.14. Based on the simulation results, it can be concluded that TEOS with a thickness of 1.5 μm should be used as the implantation mask.

N2 implantation			
Energy	**Dosage**	**Range in SiC**	**Range in SiO2**
250 Kev	15e14	3613 A	6067 A
150	10e14	2312 A	3868 A
100	6e14	1602 A	2639 A
50	5.8e14	859 A	1365 A

Table 5.2: Ni implantations energy and dosage used to implant n+ source in trench MOSFETs in this work. The resulting profile in both SiC and TEOS is shown in Figure 5.12 and Figure 5.13

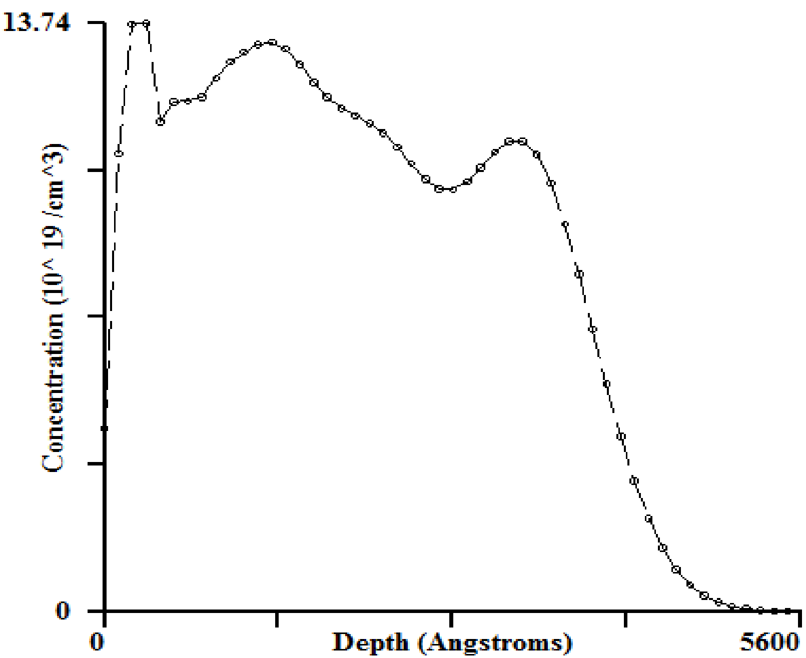


Figure 5.13: Simulation of Nitrogen ion implant range in SiC

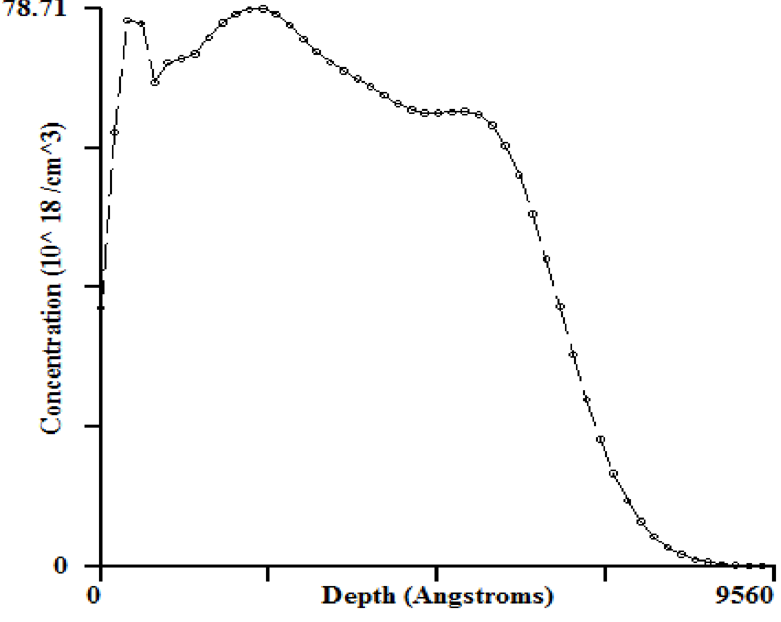


Figure 5.14: Simulation of Nitrogen ion implant range in SiO_2

Activation of ions was carried out in 1650 °C for 1 hour. The study on implant activation time and duration was performed by Dr. Hua Rong, a previous PhD student in the Warwick Science City research group [7]. The results showed that activation at 1650°C for 1 hour results in highest mobility. Argon was used during the annealing step and nitrogen was used for both ramp up and ramp down processes. The result is shown in Figure 5.15. Most of the implanted areas are visible to eyes, though this is not true for all parts.

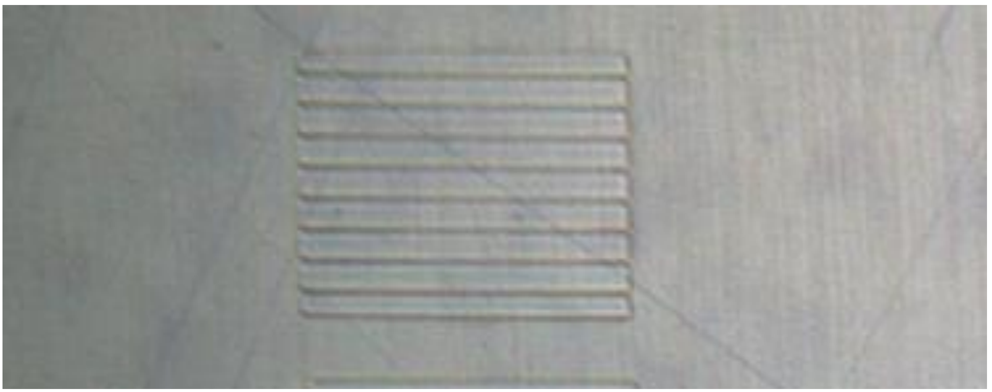


Figure 5.15: Microscopic image of SiC surface after source implantation and removing the oxide mask

5.2.3 Etching Trenches

A layer of TEOS SiO_2 was deposited on the SiC surface using LPCVD system (Thermco system) and was patterned to act as the etching mask. Densification of SiO_2 layer was carried out in Ar gas at 1000°C for 1 hour. This helps to ensure there are no micro holes in the mask layer (as discussed in Chapter 4). Trenches were etched using ICP power of 1000 W, RF power of 55

W, gas flow of SF_6 and Ar with flow rate of 50 SCCM and 40 SCCM and pressure of 10 mTorr. The picture below shows the etched sample after oxide mask was removed (Figure 5.16). A Corial 200IL ICP-RIE etcher was used to etch trenches in this work. The SiO_2 layer was removed by placing the samples in Hydrofluoric acid (HF 10%) acid for 15 minutes.

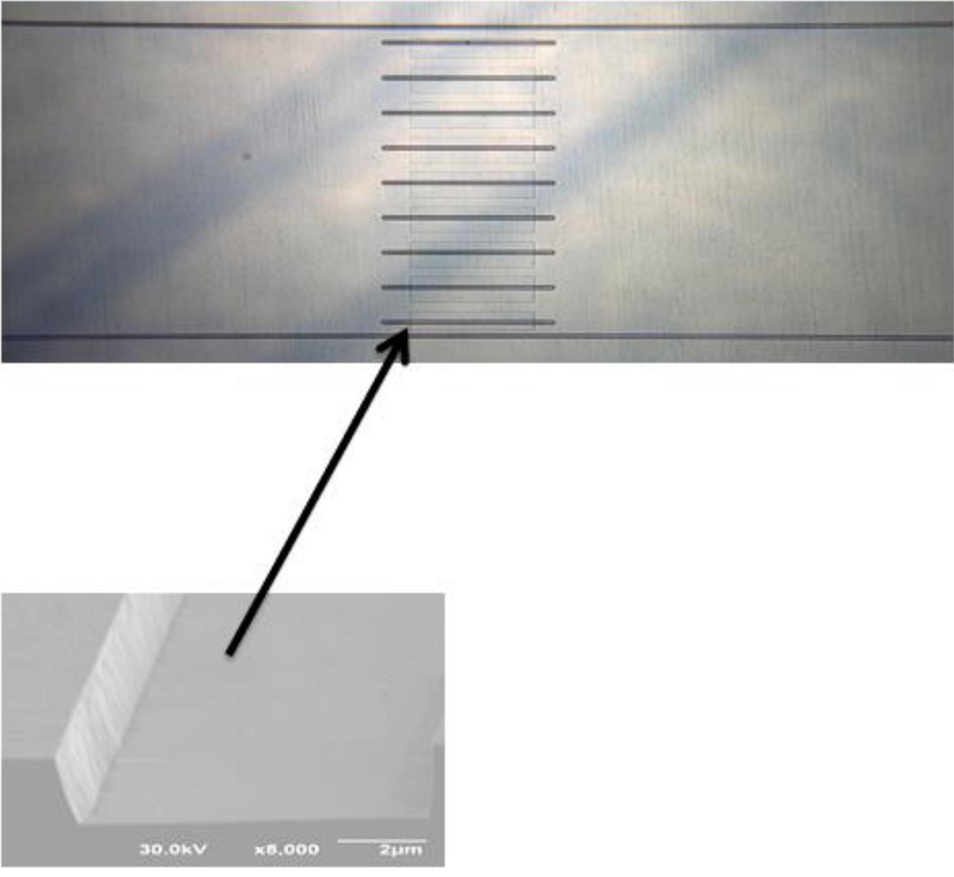


Figure 5.16: SEM images of the samples after etching trenches and removing the mask

5.2.4 Cleaning Process

The cleaning process is an important step in fabrication of thermally grown oxide. The main purpose of cleaning is to minimise (1) contaminating the oxide furnace and (2) contamination of the SiC/SiO_2 interface.

After removing the SiO_2 layer. The samples were first cleaned in solvents. They were first immersed into acetone for 15 minutes (in the ultrasonic bath) followed by methanol bath for 15 minutes. This process was repeated once more. The solvent cleaning helps to remove oil and organic residues, though they leave their own residues and hence two solvent methods are used.

The samples were then immersed in HF for one minute to remove any native silicon oxide. Then piranha cleaning was applied to the samples. The piranha includes hydrogen peroxide (50 ml) and sulphuric acid (150 ml). Piranha clean can help to remove any organics and hydroxylates. The samples were left in piranha for 15 minutes.

The last step was RCA cleaning procedure. The process is useful to remove organics and metallic contamination. The samples were first put in HF bath for another 1 minute. The RCA cleaning consists of the following two steps:

Step 1: 30ml ammonium hydroxide is added to 150 ml DI water (that is heat to 80°C), then 30 ml hydrogen peroxide is added. The samples are immersed in SC1 bath for 15 min while the temperature is kept at 80°C. This

process is finished by DI water bath for 1 minute and DI wash for another 5 minutes. Then another HF bath (2%) in used to remove the native oxide for 1 minute.

Step 2: 30ml Hydrochloric acid in added to 150ml DI water heated to 80°C, then 30 ml Hydrogen peroxide is added and then samples are cleaned in this bath for another 15 minutes. At the end the same process of DI water bath for 1 minute and 5 minutes of DI wash is applied. The samples were immersed in HF bath (2%) for another 1 minute and were washed in DI water for 5 minutes at the end and blown dry by nitrogen.

5.2.5 Gate Oxide

The thermal oxidation process was carried out immediately after the cleaning process. Warwick University's high temperature tech furnace was used to grow the oxide. The samples are loaded into the furnace at 600°C and the temperature was ramped up to 1400°C at the rate of 5°C per minute. The oxide is grown at 1300°C-1400°C using different gas combinations that will be discussed in the result section. At the end the temperature was ramped down at the same rate of 5°C per minute. During both ramp up and ramp down argon atmosphere was applied.

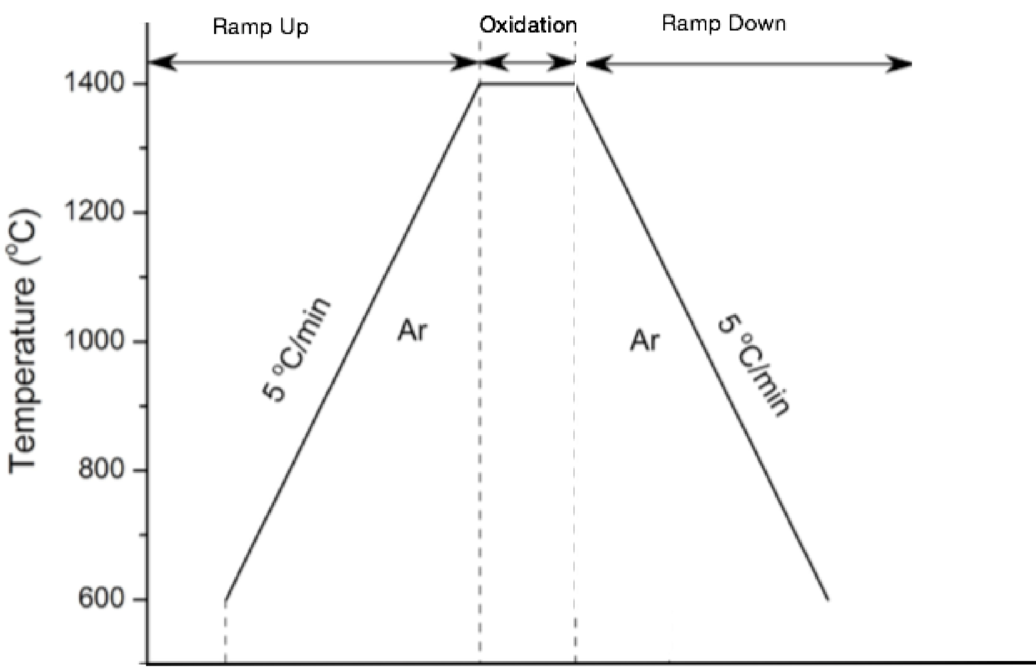


Figure 5.17: Thermal oxidation process of gate oxide

5.2.6 Opening Source and Drain Contacts

During thermal oxidation the backside of the samples were not protected. This was done to make sure no contamination exist. The backside oxide was removed using RIE etcher. The front side was patterned using S1818 photoresist. Unprotected areas were etched using RIE etcher to remove the thermal oxide to open space for source contacts. The photoresist is not removed and is used for lift off technique in next step.

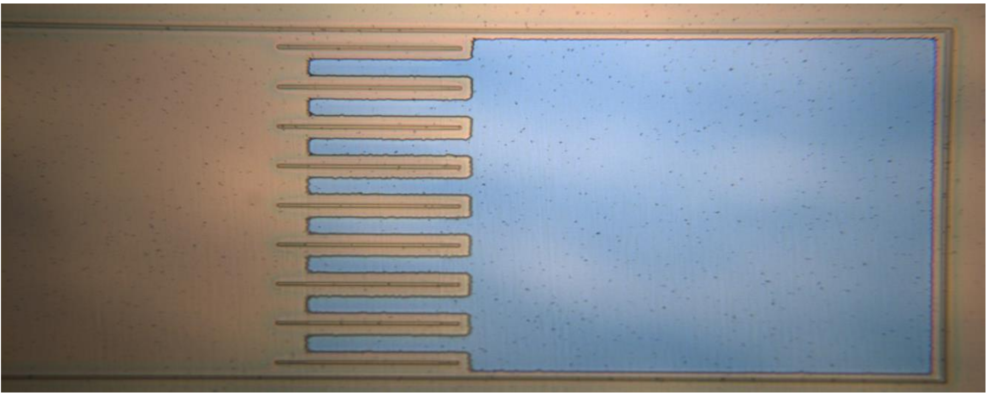


Figure 5.18: Samples surface after removing oxide from source/body contacts

5.2.7 Source and Drain Metal Contacts

10 nm Titanium (Ti) and 100 nm Nickel (Ni) were deposited on the patterned photoresist as the source/body contact using electron beam evaporator deposition system at the base pressure of 2×10^{-7} mBar. The unwanted metal was then removed using the lift off technique in acetone in an ultrasonic bath. The same metals were deposited at the back of the samples as the drain contacts.

Figure 5.19: After depositing source/body contacts (silver colour) before RTA annealing

Figure 5.20: Electron beam evaporator deposition system in Warwick University

The samples were then annealed in a Rapid Thermal Annealing (RTA) furnace at 1000°C for 2 minutes to activate the ohmic contacts. The contacts and activation process were studied in other work at Warwick University[7][8] and results in specific contact resistance in order of $10^{-6}\ \Omega.cm^2$ on the n- type SiC and $10^{-3}\ \Omega.cm^2$ on p- type SiC. The source and body contacts are short-circuited to supress the N+/P/N bipolar transistor effect when the transistor is in blocking mode.

5.2.8 Gate Metal Contact

500 nm Aluminium (Al) gate metal contacts were deposited on the gate using lift off technique. Electron beam evaporator deposition system was used to deposit Al as well. The experiments in this work shows that to achieve an acceptable cover in the gate trenches the photoresist thickness should be minimised. Otherwise the metal does not cover the top of the gate trenches very well.

Figure 5.21: Trench MOSFET after depositing gate metal

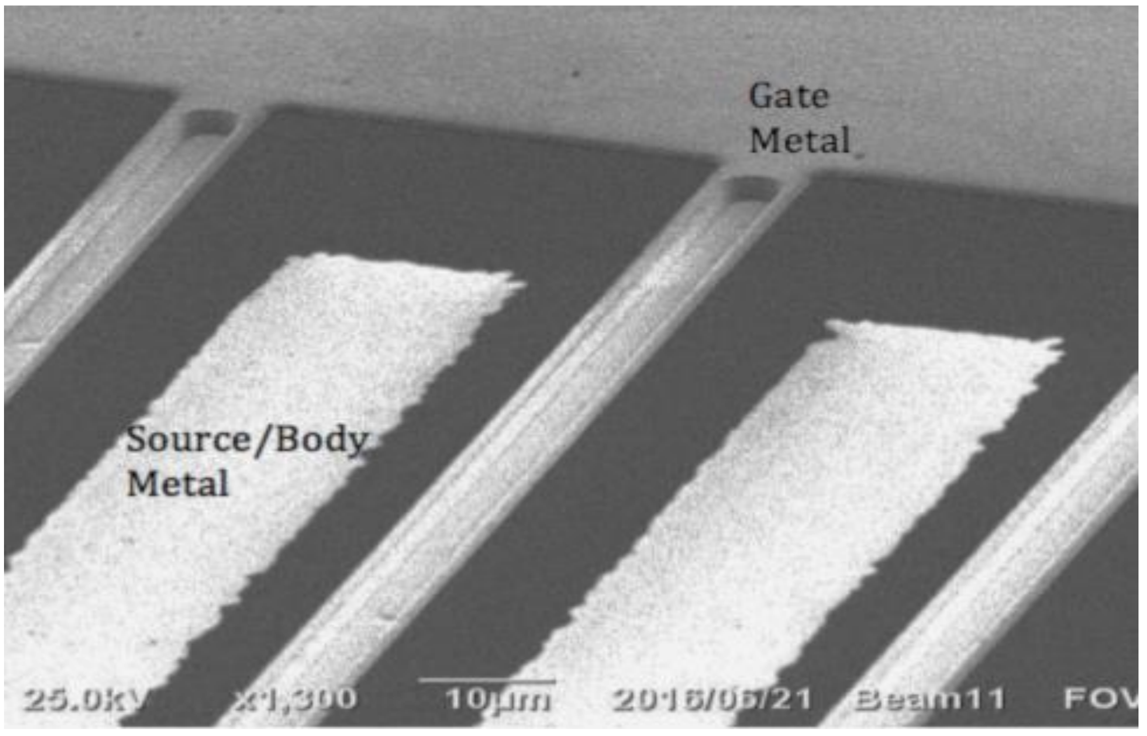


Figure 5.22: Trench MOSFET gate metal

The focus on this project is not increasing the current density, as this requires high-resolution photolithography process to etch trenches 1µm from each other. The distance between trenches in this project is 32µm. Though distance minimised to 4µm with trenches as wide as 4µm are achievable in the science city lab in Warwick University. Smaller features are not clearly visible by the microscope attached to the mask aligner and even 4 µm features are blurry. Hence it was decided to leave at least 4µm space between all features and not focus on achieving high-resolution devices in this project as it was the first attempt of making any trench device in our group.

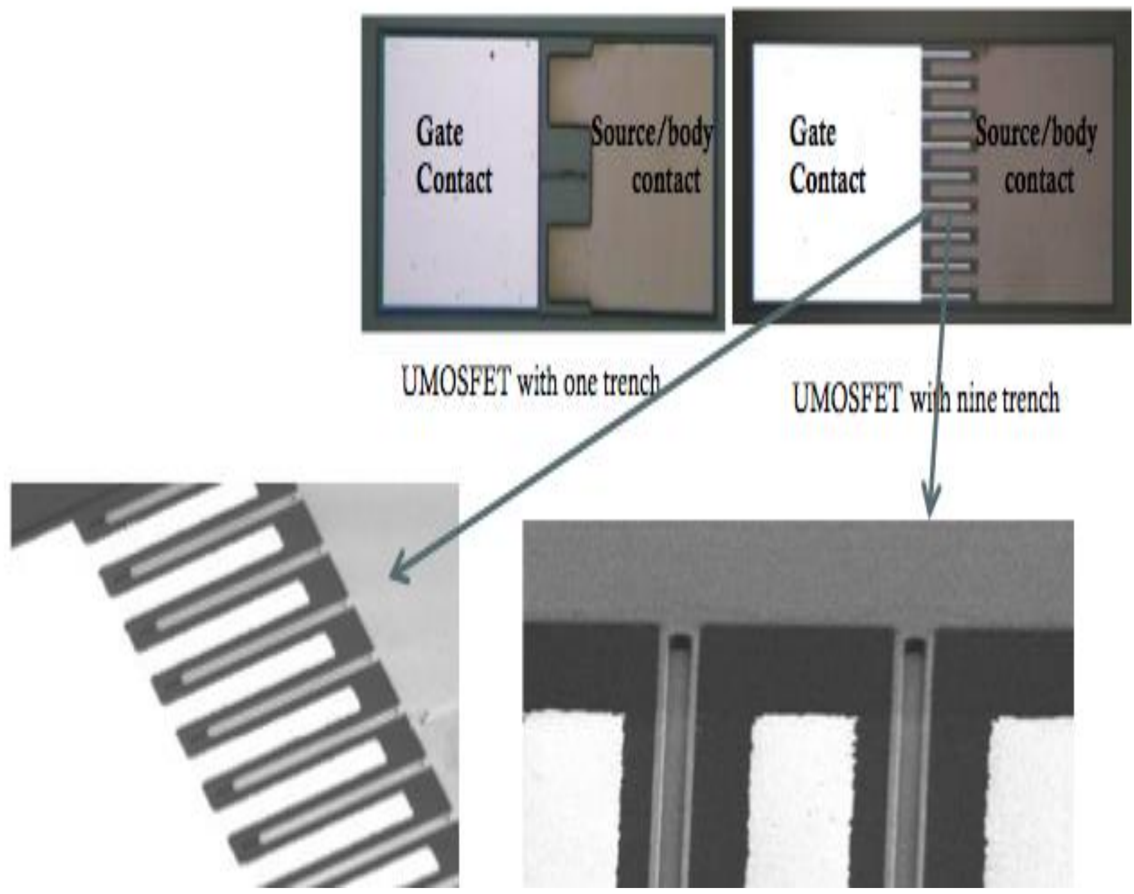


Figure 5.23: Trench MOSFET Structure

5.3 Results

The following section present the results achieved by different oxidation methods. These processes are listed in Table 5.3. The results are compared to the commercialised device by ROHM listed in the relevant reference [9].

No.	Post Etch Treatment	Gate Oxidation	Post Oxidation annealing (POA)	Thickness
1		1 hour direct O_2 thermal dry oxidation at 1300°C		50nm
2		1 hour direct O_2 thermal dry oxidation at 1300°C	3 hours N2O annealing	58nm
3		1.5 hours direct N_2O thermal dry oxidation at 1500°C		140nm
4		4 hours direct N_2O thermal dry oxidation at 1300°C		70
5		4 hours direct N_2O thermal dry oxidation at 1300°C	2 hours Phosphorus POA at 1000C, 5 lit/min	72
6	Sacrificial oxidation (4 hours direct N_2O thermal	4 hours direct N_2O thermal dry oxidation at 1300°C		75

	dry oxidation at 1300°C)			
7	1 hour H_2 post etch annealing at 1000°C, 2 lit/min	4 hours direct N_2O thermal dry oxidation at 1300°C		**68**
8		4 hours direct N_2O thermal dry oxidation at 1300°C	1 hour H_2 POA at 1000°C, 2 lit/min	**79**

Table 5.3: List of recipes used and the resulting gate oxide thickness

First we discuss why N_2O direct growth was chosen as the oxidation method. The post oxidation annealing and its effects will be discussed in details in the next section. Then the effect of post etch treatments are discussed. At the end of this chapter we compare effect of post etching treatments and post oxidation treatments.

5.3.1 Choice of the Gate Oxidation Method: Direct Nitrous Oxide (N_2O) Oxidation Growth

There are two choices of thermal oxidation gases in Science City lab in Warwick University: O_2 and N_2O. N_2O can be used for both direct thermal oxidation and/or N_2O post oxidation annealing (POA). Both of these methods are suggested to improve the mobility by increasing the nitrogen atoms at the interface and replacing the carbon atoms in comparison with O_2 direct thermal

oxidation [10].

Three different recipes were tested in this section: (1) direct O_2 thermal oxidation (2) direct N_2Othermal oxidation and (3) O_2 thermal oxidation followed by N_2O post oxidation annealing were performed in clean furnace to make sure there is no contamination. The goal of these experiments was to determine the ideal gas and temperature to create the thermal gate oxide layer.

The results show that direct growth in N_2O increases the mobility to about 8.7 $cm^2/V.s$ in a-face 4H-SiC trench MOSFETs, which is more than the results from direct O_2 oxidation with N_2O POA annealing. Also high temperature (1500°C) oxidation results in lower mobility. This is the first report of using temperature higher than 1400°C for a-face 4H-SiC trench MOSFETs based on the best of the authors knowledge.

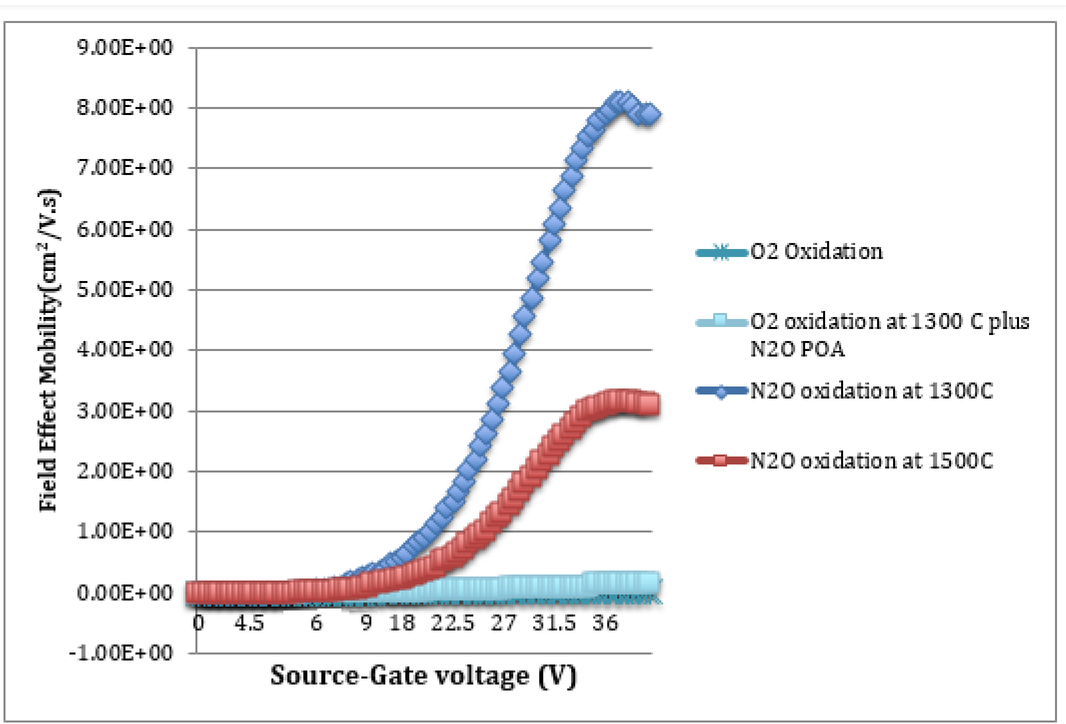


Figure 5.24: Comparison of field effect motilities

Direct oxide growth in O_2 results in the lowest mobility with or without N_2O annealing. The values of traps density calculated from trench MOS capacitors using the same recipes are listed in Table 5.4. The comparison of traps density and mobility shows that for the traps densities close to 10^{13} $\mathrm{cm}^{-2}\mathrm{eV}^{-1}$ and higher the mobility is very small and the devices are not functional. Using direct N_2O oxidation drops the traps density and increase the mobility dramatically. Any temperature less than 1300 °C using N_2O results in less mobility and very low oxidation rate, this agrees with the results achieved on the planar MOSFET[7][10].

Gate Oxide Recipe	**Traps density ($cm^{-2}eV^{-1}$) at $E_c = 0.2\ eV$**	**Mobility**($cm^2/V.s$)
O_2 at 1300°C (1 h)	1×10^{14}	3.3×10^{-2}
O_2 at 1300°C (1 h) plus N_2O POA(3 h)	8.1×10^{12}	1.35×10^{-1}
N_2O at 1300°C (4h)	8.5×10^{11}	8.07
N_2O at 1400°C (3h)	1.8×10^{12}	5.1
N_2O at 1500°C (1.5h)	2.1×10^{12}	3.17

Table 5.4: Comparison of traps density and mobility for different gate oxidation recipes

The very low mobility with direct O_2 growth could be linked to the high traps density in SiC/SiO_2 interface. The origin of this high interface traps densities are linked to different sources. The first source is the intrinsic defect in SiC. At the surface of SiC some atoms might be missing and this creates Si or C dangling bonds at the interface (Figure 5.25A) [11]. Every Silicon atoms has four valence electrons and can bond four carbon atoms and hence unpaired valence electrons (resulted from dangling bonds) form electrically active interface traps.

The second source of traps density has been linked to the carbon clusters as the main reason behind the high interface traps density [12]. The carbon

cluster model links the carbons on the surface and carbons generated during oxidation to be the main contributors to the high traps density. During oxidation of SiC, carbon atoms form Si-O-C-Si, Si-C-Si and C-C clusters [13][14][15][16].

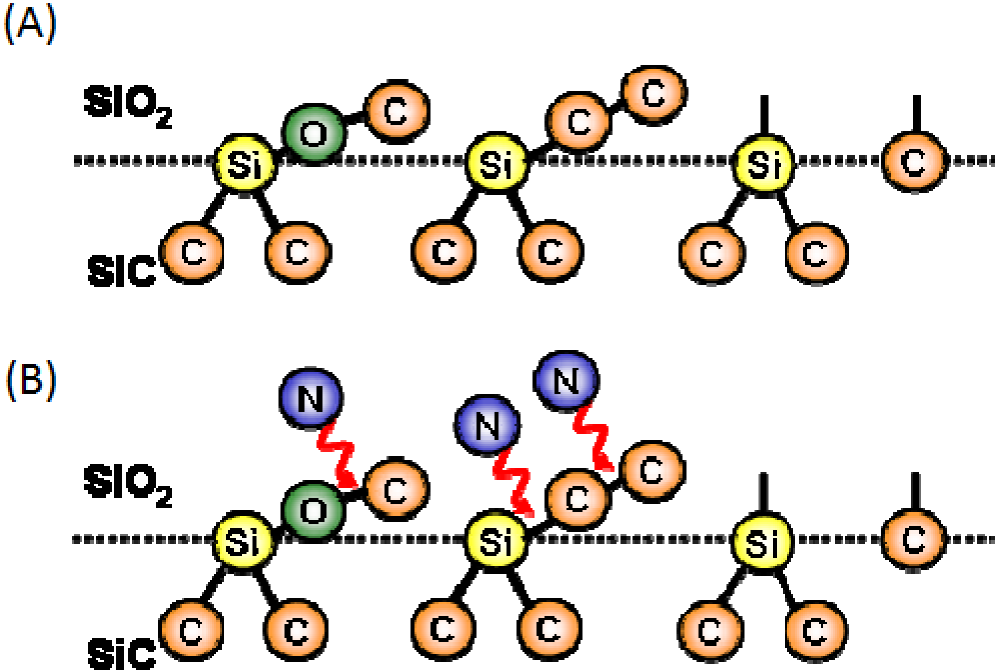


Figure 5.25: Illustration of SiC/SiO_2 interface: (A) intrinsic defects (B) Breaking Si-C bond by Nitrogen annealing (C) termination of dangling bond by Hydrogen [15]

The theory that high traps density is related to carbons at/near the interface has been confirmed by many other researchers [17][18][19][20]. The carbon cluster model can explain why N_2O annealing or direct N_2O growth results in lower traps density. It has been proved that both these methods results in less carbon compounds in the SiC/SiO_2 interface and also strong Si-N

bonds in the interface [21]. H. Watanabe [15] argues that annealing in nitrogen can break Si-O-C and C-C bonds by forming strong C-N bonads. D.P. Ettisserry [22] argues that when these carbon bonds are broken, some of these Nitrogen atoms actually incorporate in the SiO_2 lattice. This theory has been confirmed by other researchers [23]. One example of how nitrogen annealing (NO in this case) can remove the carbon from Si-C-Si defect and incorporate Nitrogen in the SiO_2 lattice is shown in Figure 5.26.

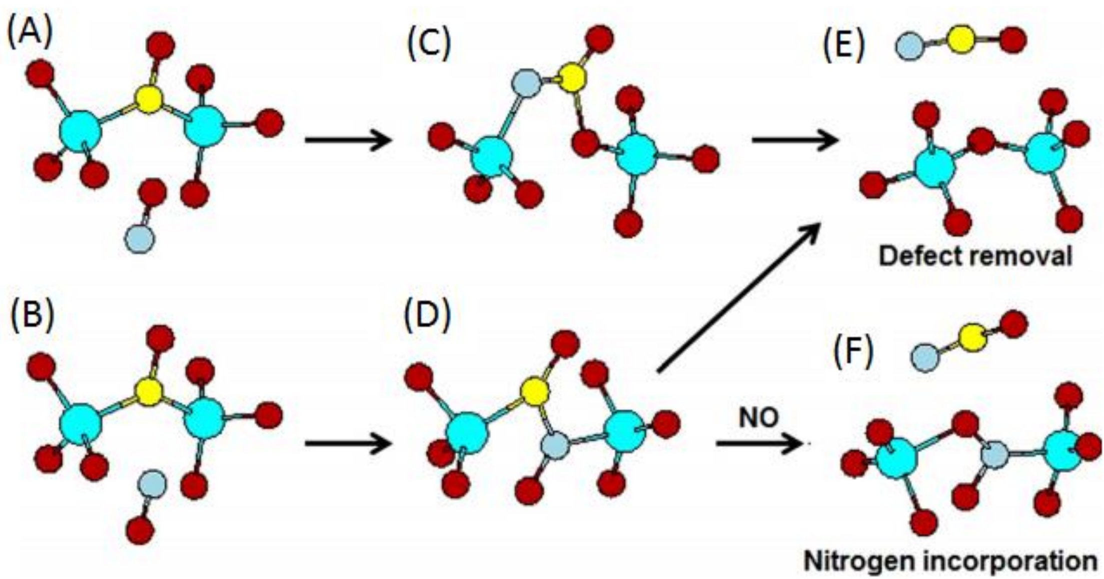


Figure 5.26: Effect of NO passivation on Si-C-Si defect. Either A-C-E or B-D-E will take place. If another NO is present, then Nitrogen incorporation in SiO_2 lattice (from D to F) will happen. In all cases defect is released as NCO molecule. Silicon-blue, Carbon-yellow, Oxygen-red, Nitrogen-Grey [22]

Using direct N_2O growth results in less carbon compounds in comparison with direct O_2 and N_2O annealing and hence this might be the reason why better motilities with less traps density are observed. Using direct N_2O growth, more nitrogen are incorporated at the interface [24] in comparison with direct O_2 growth with N_2O annealing. P. Jamet [21] propose that this is due to the initial condition of oxidation. Using direct growth method, the removal of carbons start from the beginning of the process, carbon clusters seeds are removed from the original surface and this continues throughout the process, whereas in the case of N_2O treatment after O_2 direct growth, first carbons are accumulated in the interface during oxidation and N_2O treatment has to remove the additional clusters as well. The author confirms that NO direct growth is the best solution that results in even higher mobility and less traps density than N_2O . NO was not available in Warwick University during this work. Hence direct N_2O oxidation was chosen as the gate oxidation recipe.

V. V. Afanas'ev [25] suggest that using UV ozone cleaning before oxidation car reduce the number of carbons on the surface before oxidation process. This step has not been performed in this work but could be used in the future improvement of trench MOSFET in Science City research group.

5.3.2 Post Oxidation Annealing (POA)

Common solutions to increase mobility are: hydrogen or phosphorus post oxidation annealing. There are other types of annealing such as sodium

passivation. Sodium passivation is carried out by incorporating sodium into oxide using carrier boats made of sintered alumina during oxidation. Even though sodium passivation is reported to increase the mobility but it is not a recommended procedure as it increases the mobile ions and results in unstable threshold voltage[26][27] and hence was not studied in this project. The following section first introduces these methods and then presents and compares the results of these treatments.

5.3.2.1 Hydrogen ($\boldsymbol{H_2}$) Post Oxidation Annealing

Hydrogen post oxidation annealing has been used in Si industry to terminate the dangling bonds, this techniques has been effective in reducing the traps density from 10^{14} $\mathrm{cm^{-2}eV^{-1}}$ to 10^{10} $\mathrm{cm^{-2}eV^{-1}}$ [28]. In the recent year, hydrogen post oxidation annealing has been reported to increase the mobility of SiC MOSFETs [29] to 110 $cm^2/V.s$ when it is done in temperature higher than 800 °C. The increased mobility has been linked to reduced traps density in the interface as well [30].

The hydrogen post etch annealing was carried out at 1000°C with flow rate of 2 litre/minutes for 30 minutes. Since $\mathrm{H_2}$ is a flammable gas and is dangerous to use it in high temperature, mostly NH_3 and NH_2 are used instead. We have used a mixture of nitrogen (N) and hydrogen (H_2) in this project.

5.3.2.2 Phosphorus Passivation

Phosphorus passivation has been reported to increase the mobility to around 80-90 $cm^2/V.s$ [31], which makes it more effective than the conventional NO or N_2O that can increase the mobility to average of 20 $cm^2/V.s$ [10][7].

In this technique, SiP_2O_7 phosphorus planar diffusion source (PDS) was used for the purpose of post oxidation annealing. The treatment was done at the temperature of 1000°C for 2 hours with nitrogen flow rate of 5 litres/minutes. The exact process of phosphorus passivation can be found in the relevant source [7]. Science city group has previously reported that by using phosphorus passivation the mobility of Si-face planar MOSFEET can increase to 60-80 $cm^2/V.s$ [7].

5.3.3 Results: Comparison of Post Oxidation Annealing Methods

Post oxidation annealing in hydrogen (forming gas) and phosphorus have improved the mobility to around twice of the reference sample (direct N_2O oxide growth). The results of direct N_2O oxide can be used as representative of N_2O post oxidation annealing and be compared to hydrogen and phosphorus annealing results.

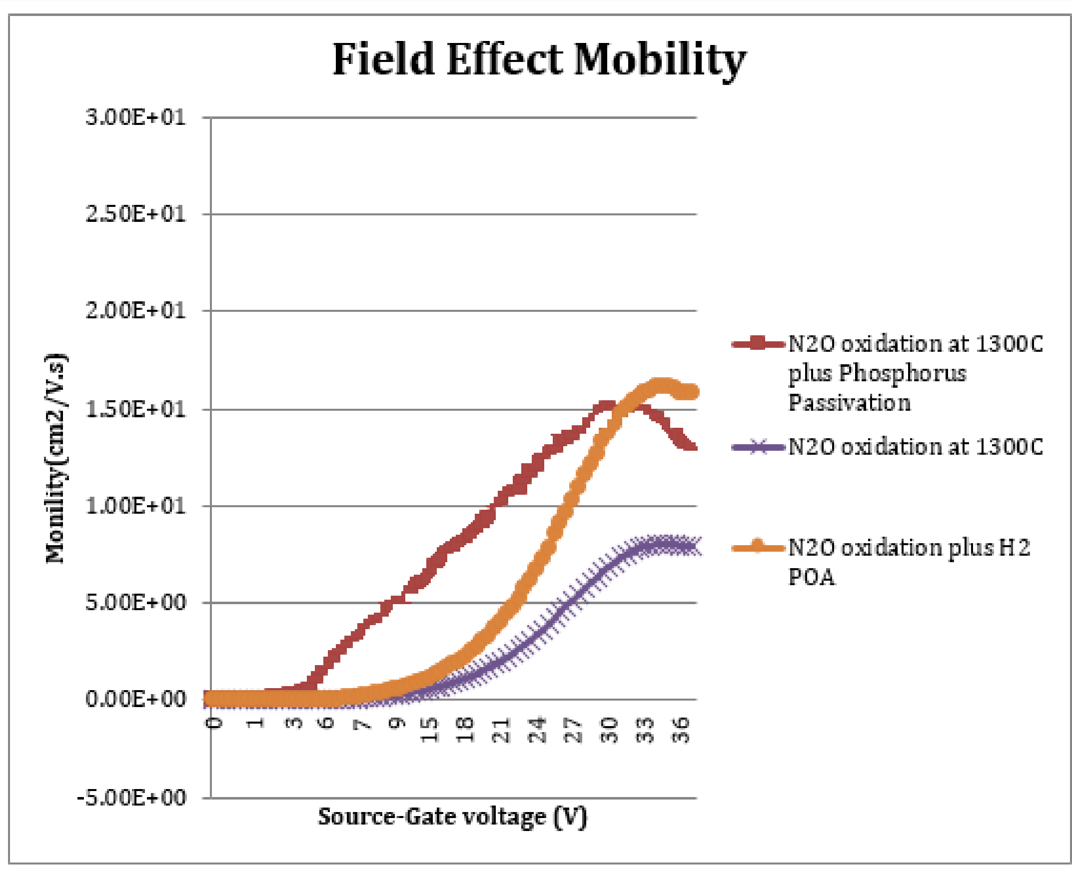


Figure 5.27: Comparison of motilities for trench MOSFETs with different post etch and post oxidation treatments

The limiting factors of mobility were discussed previously. The main questions to be answered is: how these treatments are helping? And why one treatment is more efficient that the other?

[32] and [33] have compared the traps density and mobility using the same fabrication process on both a-face and Si-face. The results show that even though a-face can show higher traps density than Si-face, it always show higher mobility. This suggests that the coulomb scattering effects of traps density is not

the main contributor to limiting the mobility on a-face. This theory has been confirmed for nitrogen annealed a-face trench MOSFETS. G. Liu [10] has studied the temperature dependencies of a-face after NO annealing and reports that mobility decreases at higher temperatures (Figure 5.28). Negative dependency on temperature suggests that phonon scattering might be the limiting factor of mobility of trench MOSFETs that are annealed in Nitrogen (NO or N_2O) [10] [34]. A reliable source of temperature dependencies information of phosphorus and hydrogen annealed trench MOSFET does not exist and it is strongly recommended to be carried out as part of further work of second generation trench MOSFETs in Warwick University. The important point to remember is that the annealing process, might have different effects on different surfaces.

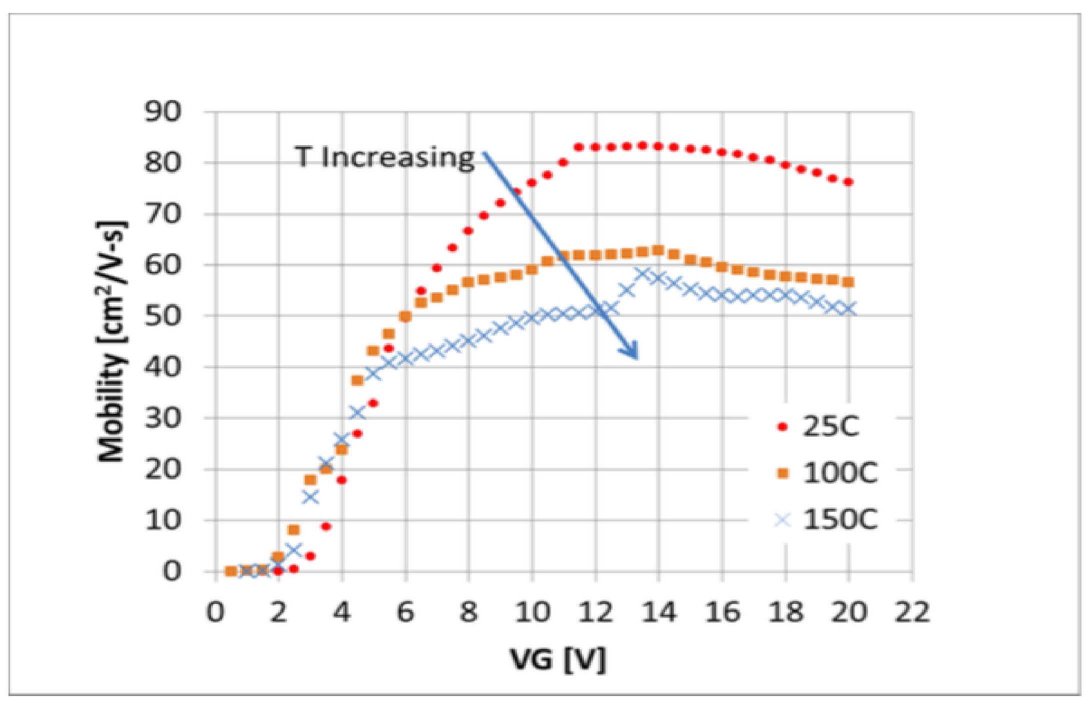


Figure 5.28: Negative temperature dependencies of mobility on the a-face SiC[10]

An important discovery was that defect passivation is not the only reason that mobility is improved with nitrogen or phosphorus passivation [35]. They are both n-type donor and studies suggest that they can insert in SiC and change a thin layer of p-body from p-type to n-type [36][37]. Surface of SiC was measured [37] after both nitrogen and phosphorus passivation and the results shows that the density of phosphorus and Nitrogen was much higher especially on the a-face (Table 5.5). This can explain why the mobility increase on a-face is more than Si-face using post oxidation annealing. In the previous section the mechanism of incorporation of nitrogen in SiO_2 lattice was discussed.

Species	a-face	Si-face
P	1.6×10^{14} cm^{-2}	1.8×10^{14} cm^{-2}
N	9.1×10^{14} cm^{-2}	5.5×10^{14} cm^{-2}

Table 5.5 : Density of nitrogen and phosphorus after NO and phosphorus passivation. The oxide is removed to make this measurement [37]

In another study [37], measurement of the surface resistance after removing oxide shows that phosphorus passivation results in less resistance compared to N_2O . Some studies [10][37] recommend this is due to the fact that phosphorus passivation results in higher n-doping in p-body and hence reduces the resistivity. This can explain why phosphorus passivation results in higher mobility as can be seen in Figure 5.27. This phenomenon is called counter doping. Counter doping and reduction in traps density result in higher mobility and less threshold voltage [38].

Hydrogen post oxidation annealing has also increased the mobility (Figure 5.27). Measurement of the a-face MOS capacitors after hydrogen post oxidation annealing shows reduction on traps density on both a-face [29] and Si-face [30]. W. Yiyu [39] studied the effect of H_2 POA annealing at low temperature (450ºC) and proves that there is no change in traps density or mobility. However when H_2 POA at low temperature is carried out after NO passivation, there is an improvement to the traps density in comparison with NO passivation only. The study suggests that the reason is that NO dissolves the carbon clusters and

hydrogen terminated the resulting dangling bonds (Figure 5.25). O.K. Fukuda [30] proves that Hydrogen POA can be efficient in decreasing traps density without the need for any other passivation if the annealing temperature is higher than 700°C. This study also proves that the decrease of traps density is due to increase of hydrogen concentration in the surface and suggests that the hydrogen atoms have terminated the dangling bonds of Si and/or C.

The results of this work also show that even though with phosphorus POA and hydrogen POA the mobility has increased to a similar value of 15 $cm^2/V.s$. The current density graphs were also similar for both methods..

Though there were three important differences observed between these two processes:

(1) The threshold voltage has not improved (decreased) by hydrogen annealing (Table 5.6). These results clearly shows that the mechanism of improving mobility using these annealing methods are different.

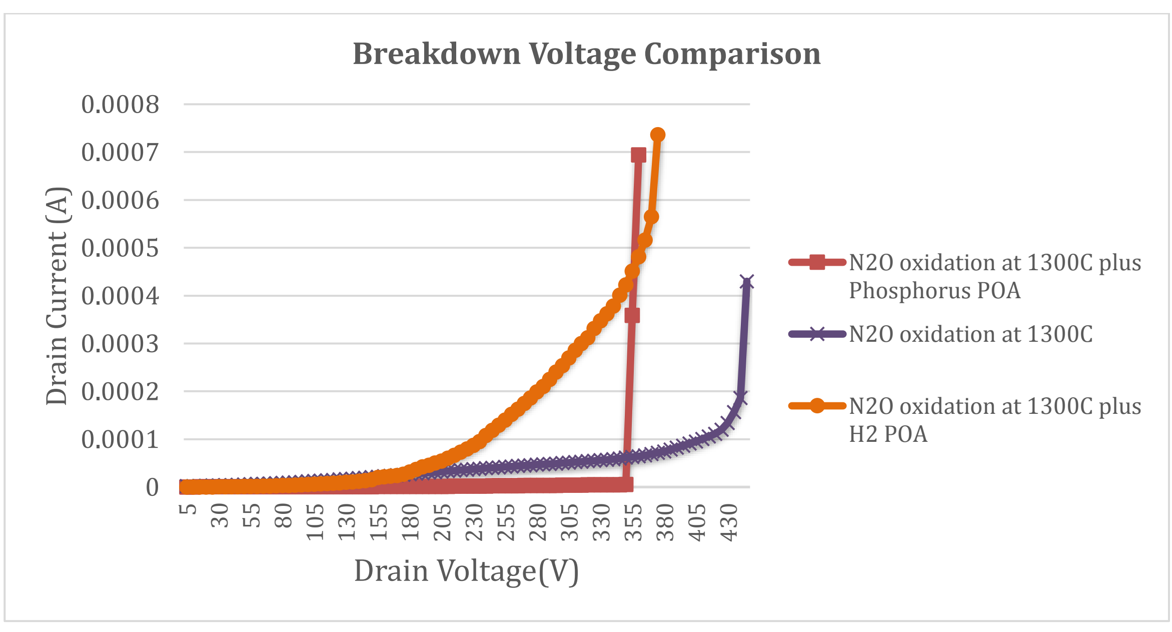
(2) The other important difference between phosphorus POA and hydrogen POA is the leakage currents. Phosphorus POA results in the lowest drain to source leakage current and hydrogen POA results in the lowest gate to source leakage current.

Gate oxide recipe	Vbr Vg= 0 V I_{DS}=0.01mA	Threshold voltage (V)	Mobility $cm^2/V.s$
1 hour O2 plus 3 hours N2O annealing	435	7.5	1.35×10^{-1}
4 hour N2O oxidation plus phosphorus POA at 1000C	354	0.1	15
4 hours N2O oxidation plus 4 hours sacrificial oxidation in N2O	195	16	22
4 hours N2O oxidation at 1300C	410	16	8
4 hours N2O oxidation plus 1 hour H2 post etch treatment	205	7	33
4 hours N2O oxidation plus 1 hour H2 POA	363	11	16

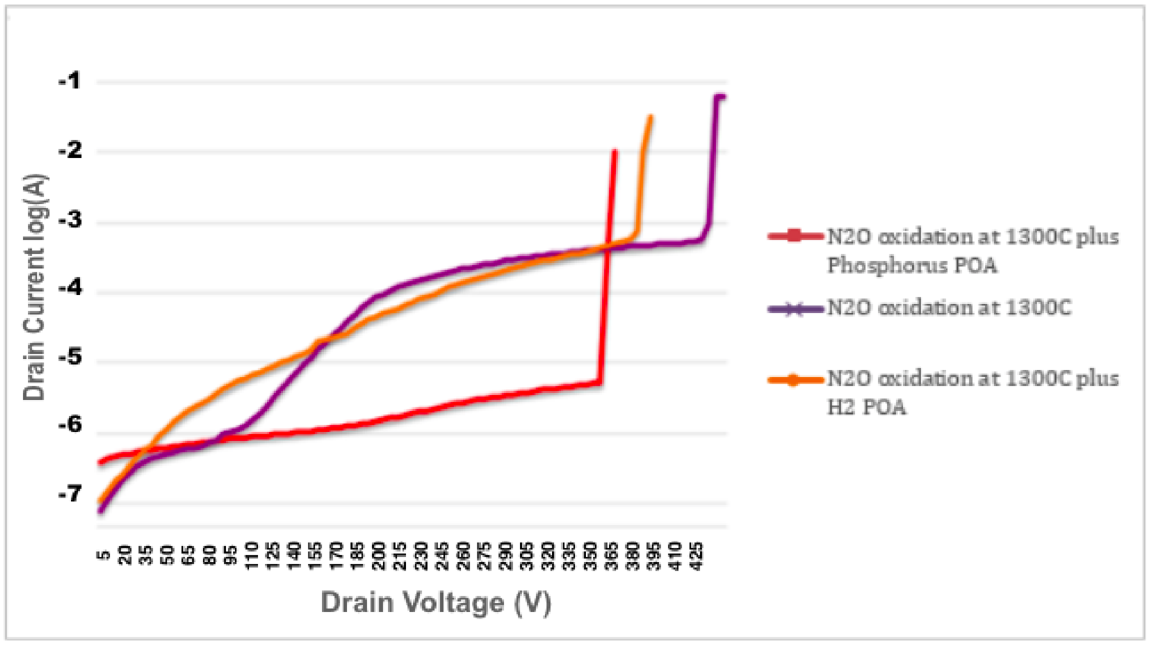
Table 5.6: Comparison of electrical parameters measured from trench MOSFETs with different post etch and post oxidation treatments

The value of drain to source leakage current (I_{dss}) is usually in range of average of 10 to 20 µA to maximum 500 µA for commercialised MOSFETs. I_{dss} for all trench MOSFETs were measured before their breakdown. All devices resulted in I_{dss} of less than 5-80 µA right before the breakdown and phosphorus POA results in the lowest I_{dss} **of** 5 µA just before breakdown. The point of breakdown for these trench MOSFETs with the area of 0.146mm^2 is defined to be when the devices reached the drain source current of 0.01mA. Based on this assumption, hydrogen POA results in breakdown voltage of 240V and I_{dss} of 10

μA (Figure 5.29). Phosphorus POA on the other hand results in breakdown voltage of 354 V with I_{dss} of 5 μA. If the hard breakdown is considered(instant rapid increase in the current), then both devices have reached breakdown at around 350V, though phosphorus POA results in I_{dss} of 5 μA and hydrogen POA results in I_{dss} of 500 μA which is similar to the maximum value of I_{dss} achieved in industry but far from the average value of 10 μA. Unfortunately the graph if I_{dss} is usually not available on datasheet and hence we can only compare the value of I_{dss} at the breakdown point.



(A) Drain current vs. drain voltage

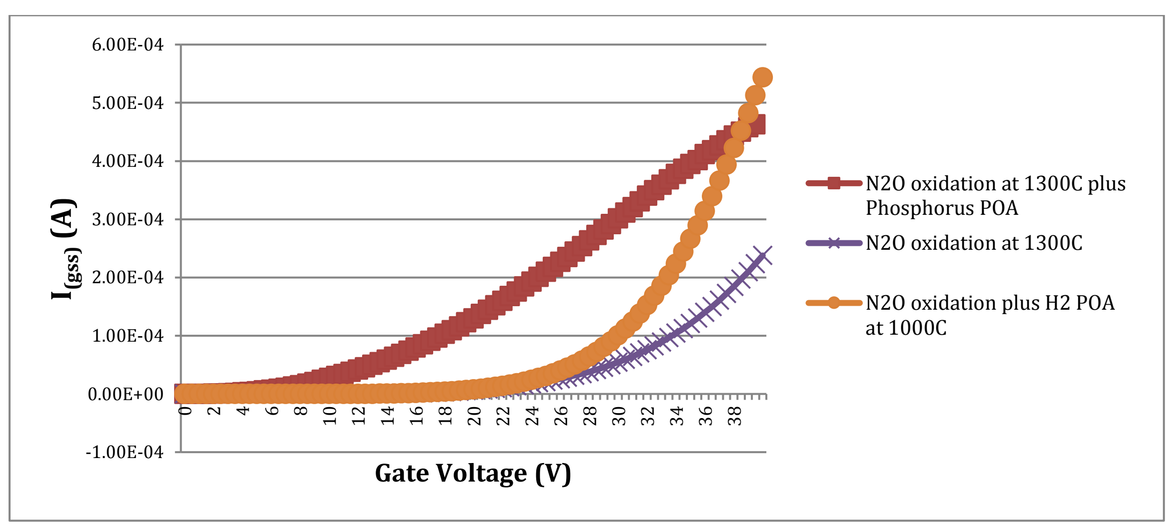


(B)Log of drain currents vs. drain voltage

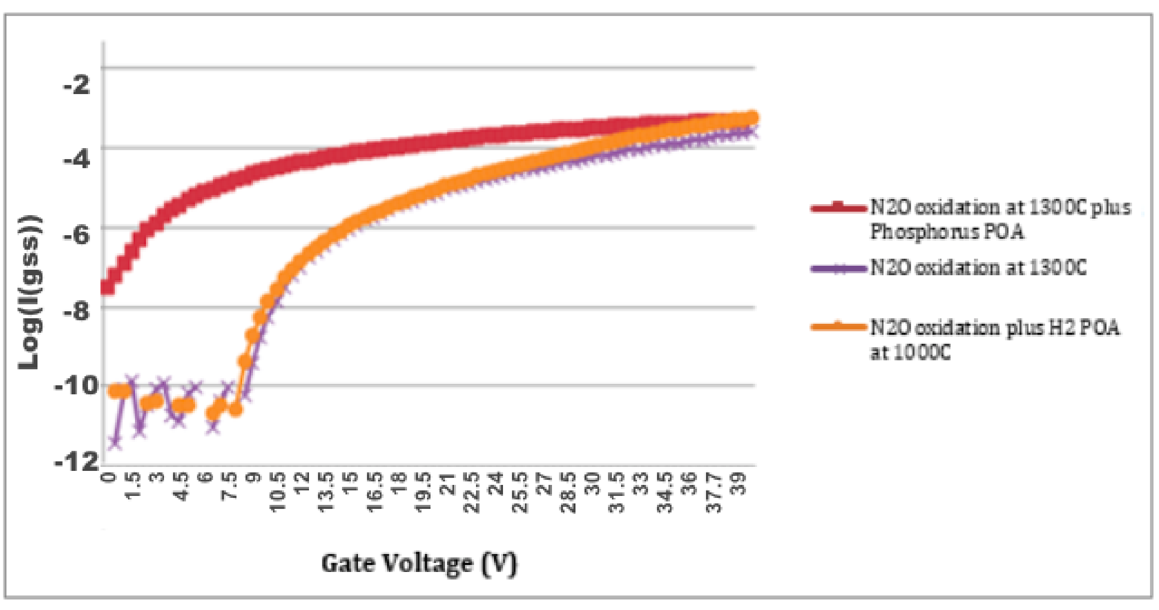
Figure 5.29: Comparison of breakdown voltages of trench MOSFETs with different post etch and post oxidation treatments

(3) The third important difference is seen in the gate source leakage current I_{gss}. The gate source leakage current is a representative of oxide and interface quality and hence it is important parameter. Hydrogen passivation and N_2O direct growth (that is a representative of Nitrogen annealing) results in the lowest I_{gss}, while the maximum I_{gss} at high gate voltage(more than 27V) seems to be similar, in lower voltage, Hydrogen annealing results in much lower I_{gss} in range of µA till 20 V. The commercial 1.2 kV devices have I_{gss} of maximum 100nA at gate-source voltage of 22V. The I_{gss} of phosphorus annealed devices

are 154 μA at the same voltage and hydrogen and nitrogen annealed device results in I_{gss} of 18 μA.



(A) Gate source leakage current



(B) Log of gate source leakage current

Figure 5.30: Gate source leakage current (I_{gss}) of trench MOSFETs with different post oxidation treatments

As can be seen in Figure 5.29 and 5.30, phosphorus annealing results in a better drain source leakage current but worse gate source leakage current in comparison to hydrogen post oxidation annealing. So which method is more suitable? As mentioned gate source leakage current measures the quality of oxide and interface around the channel area on the trench sidewalls, on the other hand the drain source leakage current in trench MOSFETs (without gate shield) is a representative of the structure (P-N Junction between the body and drift) and also the oxide quality at the bottom and corners of the trenches(Figure 5.31).

The drain source leakage current is calculated before the point of breakdown and during the reverse bias. In a simple P-N junction, during the reverse bias, there is very little current flow (leakage current) until the point of breakdown where the electric field reaches beyond the point of breakdown of the material. This leakage current depends on the structure (doping and thickness). In a trench MOSFET without a shield, the breakdown happens in the oxide at the corners of the trench bottom (as was discussed in the simulation chapter), before the P-N junction reaches the breakdown point. Hence the drain source leakage current can be the current that passes through the gate oxide bottom. Since the trench structure were the same in all the samples and they were all etched in the same batch, the difference in the results of drain source leakage current represent the difference in the oxide quality at the trench bottom specially at the corners(Figure 5.31).

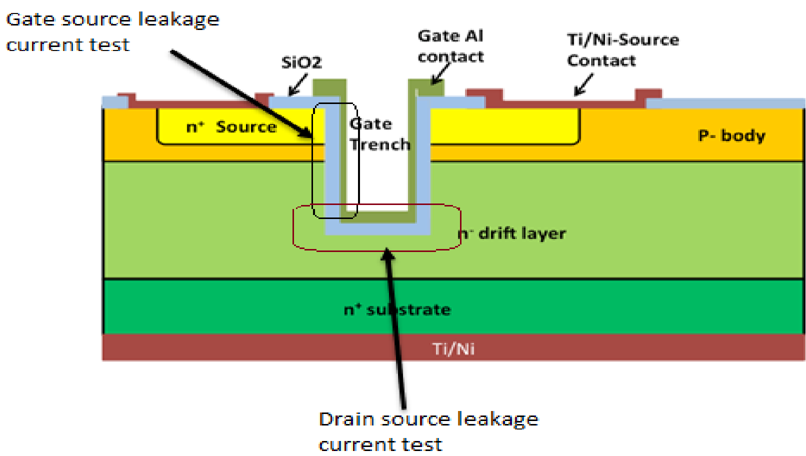


Figure 5.31: Areas of measurement using different leakage tests in a trench MOSFET without gate shield

Therefore it can be concluded that hydrogen annealing results in better oxide and interface quality on the a-face (where the trench walls are located) and hence improved gate source leakage current is observed. As it was discussed before both methods reduce traps density and hence result in reduction in traps assisted leakage current. Further investigation is needed to confirm the origin of superior quality of oxide resulting from hydrogen annealing, but the possibility is that the lowest traps density and hence lower leakage current is achieved using hydrogen. It must be noted that phosphorus annealed devices have slightly higher mobility but higher gate leakage current. If traps density was the origin of both low mobility and leakage current, we would have expected to see better mobility and reduce leakage current on the same samples.

The lowest source drain leakage current using phosphorus annealing can be because of (1) better quality of oxide in the Si-face (the trench bottom) using phosphorus annealing. Annealing on different planes can have different results and hence it is possible that phosphorus results in better quality oxide on the Si-face (2) randomness in the oxidation thickness which was observed during the experiments. The origin of this varying thickness is not clear but to minimise this, different batch of MOSFETs were fabricated (2 batch, 2 samples in each batch, 30 trench MOSFETs on each) and the results look similar (even though the value of leakage current were different).

Why is the drain source leakage current very different from the commercial devices while other parameters are similar? The commercial trench MOSFETs have gate shield protections (or other methods) to make sure the high electric field is not located on the trench oxide and hence the breakdown happens in the SiC region (as was shown in the simulation chapter). Therefor the leakage current is limited to the reverse bias leakage current. To be able to compare the source drain leakage current to the commercial devices, gate protection should be added to the second generation of the devices. Adding the gate protection (or other methods that will be presented in the recommendation chapter), will minimise the effect of trench bottom oxide on the drain source leakage current. We assume the source drain leakage current achieved from both hydrogen and phosphorus annealed devices will be similar to the commercial devices when gate protection is added.

5.3.4 Post Etch Treatments

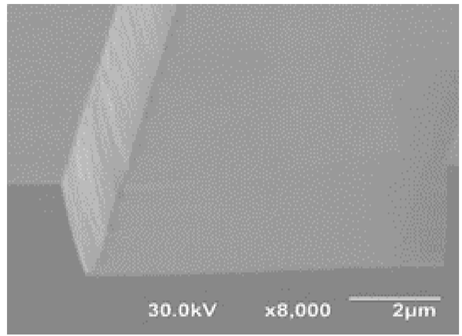
Two post etch treatments have been studied in this work: sacrificial oxidation and hydrogen post etch annealing. Both treatments have been proven successful in rounding the corners of trenches [40][41]. Rounding the trench corners can reduce the crowding of electric field on the corners and hence increase the breakdown voltage. Though the simulation results only show increase in breakdown voltage to be on average 35V. As presented in Chapter 3, a 1.2kV trench MOSFET, can enter breakdown in much lower voltages as low as 350V due to the breakdown in the gate oxide.

The fact is that rounding the corner cannot avoid the premature breakdown of the oxide. The best practice in industry to increase breakdown voltage is to implants a P^+ shield at the bottom of trench [42] or sacrificial trenches [43]. Increasing breakdown voltage is out of scope of first generation trench MOSFETs in Warwick University but will be introduced in the recommendation chapter in this work. Though looking at the recommended sources of low mobility and high traps density that were mentioned earlier, it is obvious that there is a need to eliminate the dangling bonds and carbon cluster to improve the traps density. One of the questions that has not been answered clearly is if improving the surface after etch and before oxidation can also increase the mobility. In the next section two methods of post etch treatments are discussed. As a matter of fact these two process were first examined to round

the corners of trenches, but the resulting trench MOSFETs exhibited very different electrical characteristics. The next sections present these results.

5.3.4.1 Sacrificial Oxidation

Sacrificial oxidation is the process of thermally growing oxide and then removing it before the growth of the main gate oxide layer. It is suggested that this process can help rounding the trench corner and hence increasing the breakdown voltage. Sacrificial oxidation was carried out in N_2O atmosphere at 1300°C for 4 hours as well. This was done to make sure the amount of carbons and dangling bonds on the surface is minimised before the actual gate oxidation growth. Sacrificial oxidation is very effective in eliminating microtrenches and rounding the corners as can be seen in Figure 5.32.



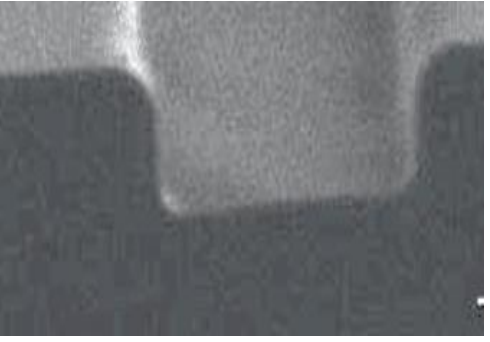


Figure 5.32: SEM images of (A)trenches before sacrificial oxidation, (B)trenches after sacrificial oxidation: the corners are rounded

Sacrificial oxidation helped to increase mobility and current density of trench MOSFETs as can be seen in Figure 5.33 and 5.35.

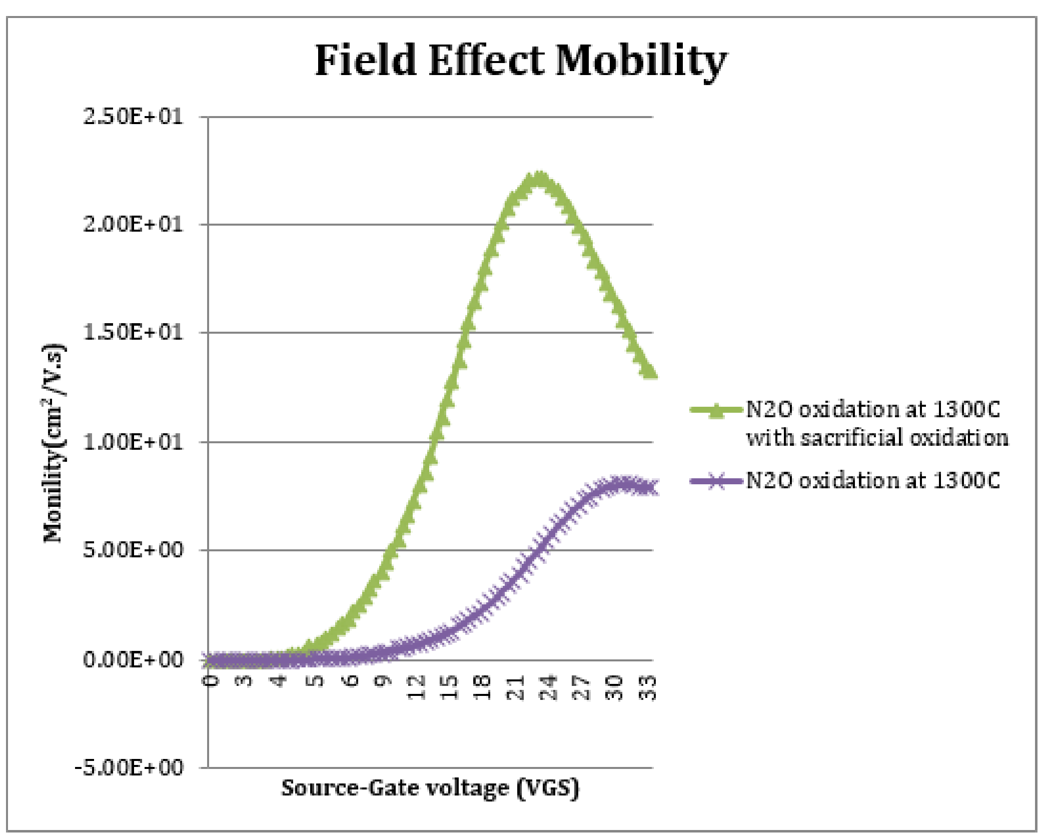
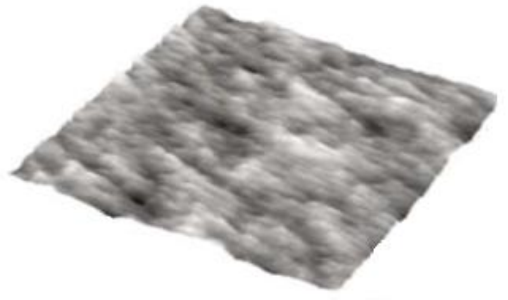


Figure 5.33: Comparison of motilities with and without gate sacrificial oxidation

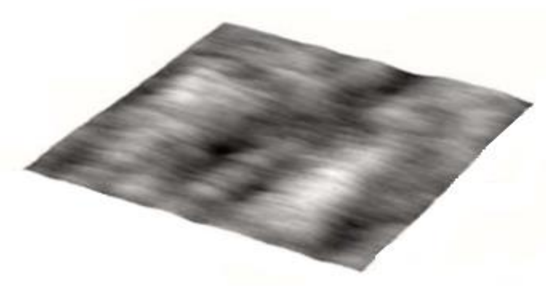
Figure 5.35 shows that the gate source leakage current for the device with sacrificial oxidation (1) increases rapidly even at low gate voltages (2) to a much higher value compared to the device without sacrificial oxidation. Gate source leakage current (I_{gss}) is the current that travels through the gate when gate-source voltage is applied and drain voltage is kept at minimum (0.5 V). I_{gss} increases due to poor oxide quality and it is dependent on the device size[44].

Thermal oxidation can results in surface roughness, K. Y. Cheong [45] has studied the SiC surface after oxidation and confirmed the roughness caused by

thermal oxidation. He has compared the roughness of the surface using direct O_2 growth with NO annealing and direct NO annealing and as can be seen in Figure 5.34, direct O_2 growth results in higher roughness. The study links the roughness to carbon removal as well. Carbone removal reduces the carbon cluster at the interface and hence might have been the reason for less roughness.



(A) SiC surface after direct O_2 + NO annealing



(B) SiC surface after direct NO growth

Figure 5.34: Topography images from AFM: SiC surface after removing the gate oxide grown in (A) direct O_2 + NO annealing (B) direct NO growth. The root mean square roughness is (A)0.193 and (B) 0.132 nm [45]

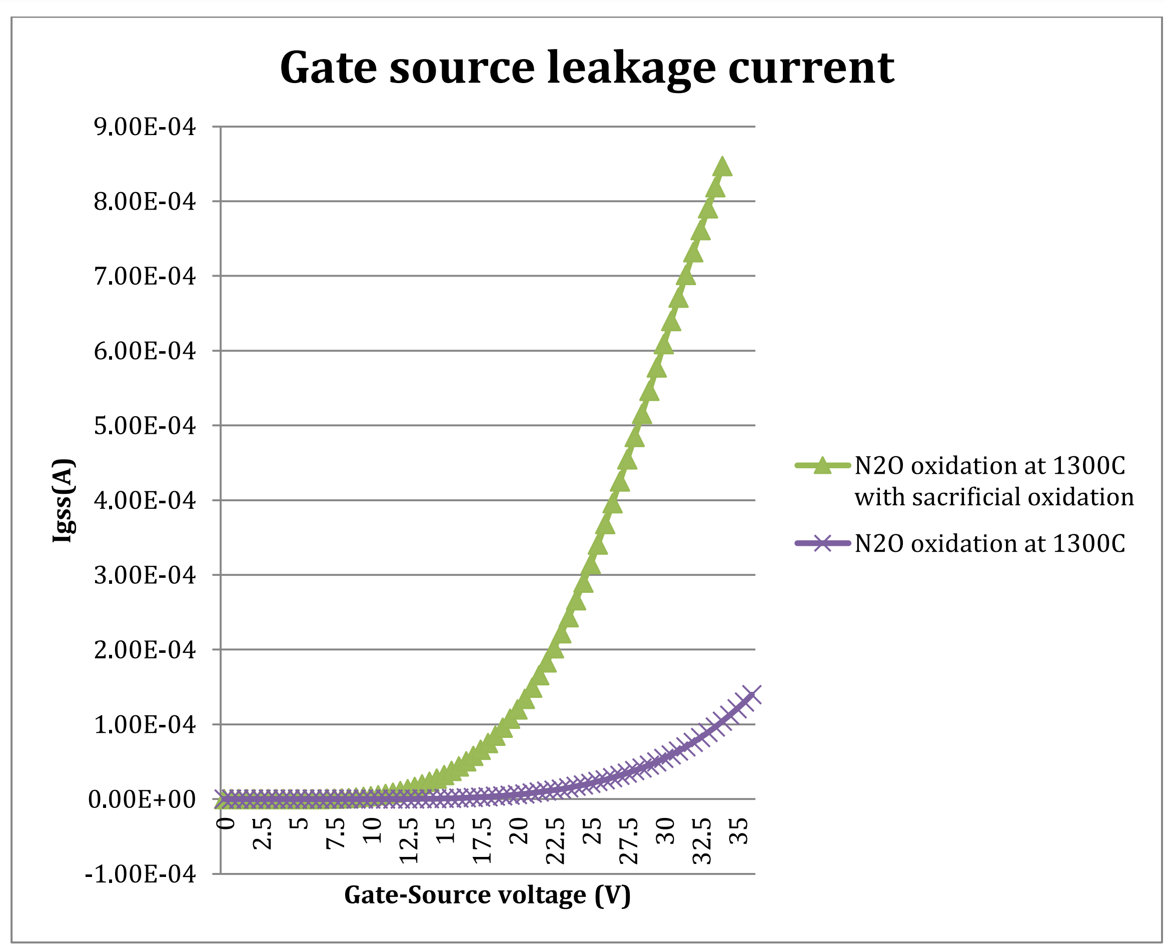
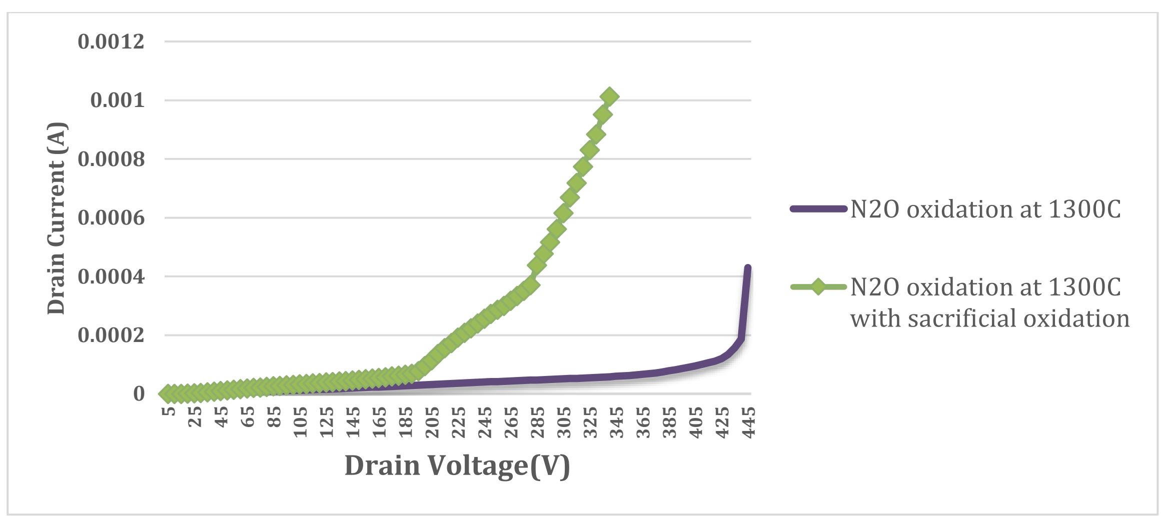


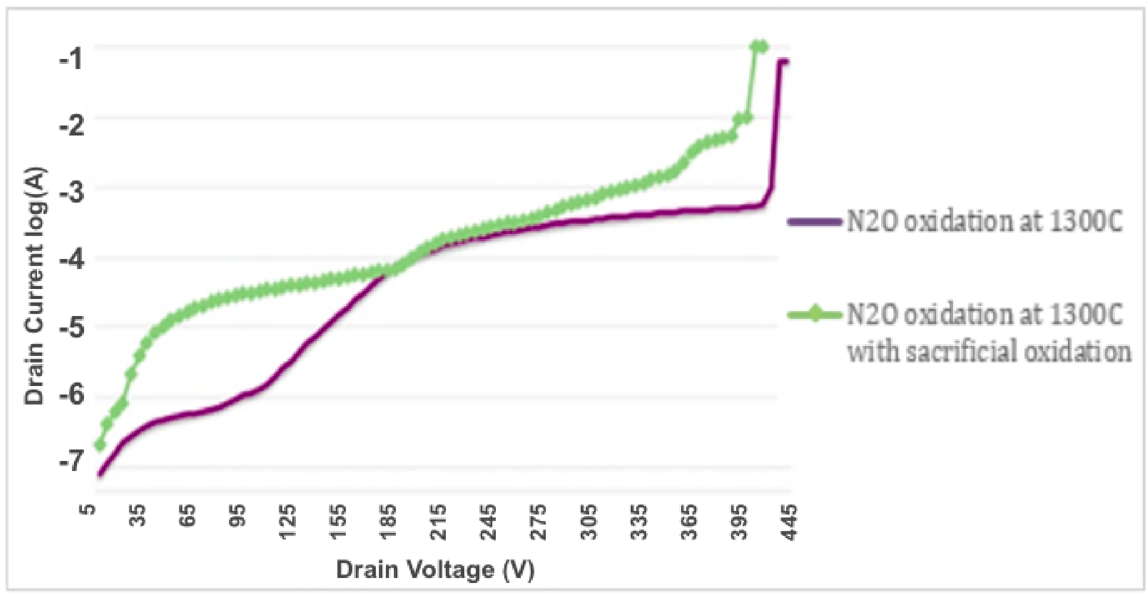
Figure 5.35: Comparison of leakage current with and without gate sacrificial oxidation

Also from simulation results, it is expected that if the gate oxide quality remains the same after sacrificial oxidation, the rounded corner should help to increase the breakdown voltage by an average of 30-40V. This is due to the less crowding of electric field at the corner of trenches. The results achieved in this work do not agree with the simulation (Figure 5.36). This means that the oxide or SiC surface quality was degraded because of sacrificial oxidation. As can be seen in Figure 5.36, the source drain leakage current is very high before the breakdown for the trench MOSFET with sacrificial oxidation and the low quality of the

oxide at the trench bottom results in the premature breakdown of the oxide. Other researchers have also reported that sacrificial oxidation can result in degraded gate and unreliable gate oxide [24][46].



(A) Breakdown voltage comparison (showing drain current)



(B)Breakdown voltage comparison (showing log of drain current)

Figure 5.36: Comparison of breakdown voltages with and without sacrificial oxidation

The value of traps density measured from the device with sacrificial oxidation was $3.4 \times 10^{12}\ \boldsymbol{cm^{-2}eV^{-1}}$. The Comparison of this value and the traps density of the device without sacrificial oxidation (listed in Table 5.4) shows that the improvement in mobility is not due to the decrease in traps density.

Though sacrificial oxidation does not really degrade the traps density and hence increased leakage current is not due to the traps density. S. Miyahara [46] reports higher roughness, leakage current and failure rate after sacrificial oxidation. The photo-emission analysis done in that work, suggests that the spot with higher roughness results in local electric field concentration and higher leakage current. Similar behaviour was seen with trench MOS capacitors in this work: most trench MOS capacitors with long time (4 hours) sacrificial oxidation were unreliable. They had very high leakage current and entered breakdown at very low voltages. Other method of oxidation were tested as part of recommendation for second generation trench MOSFET that will be introduced in recommendation chapter.

5.3.4.2 Hydrogen ($\boldsymbol{H_2}$) Post Etch Annealing

Post etch hydrogen annealing has been used to round the corners of trenches. Hydrogen annealing must be done in high temperature (more than 1400°C) to achieve rounding of corners, the suggested duration of annealing in temperature of higher than 1400°C is reported to be less than 10 minutes and only 2-3 minutes in higher temperature (1500°C) [40][41].

The temperature and time were studied carefully in the range of 500°C - 1550°C. Even though other studies have reported successful results in the range of 1400°C -1600°C, our results were not satisfactory and were similar to Figure 5.37. Etching at any temperature higher than 1000°C resulted in etching of the material. And in higher temperature (example: 1400°C) even 2 minutes annealing resulted in etched surface. As can be seen in Figure 5.37, annealing the etched surface resulted in a very rough surface.

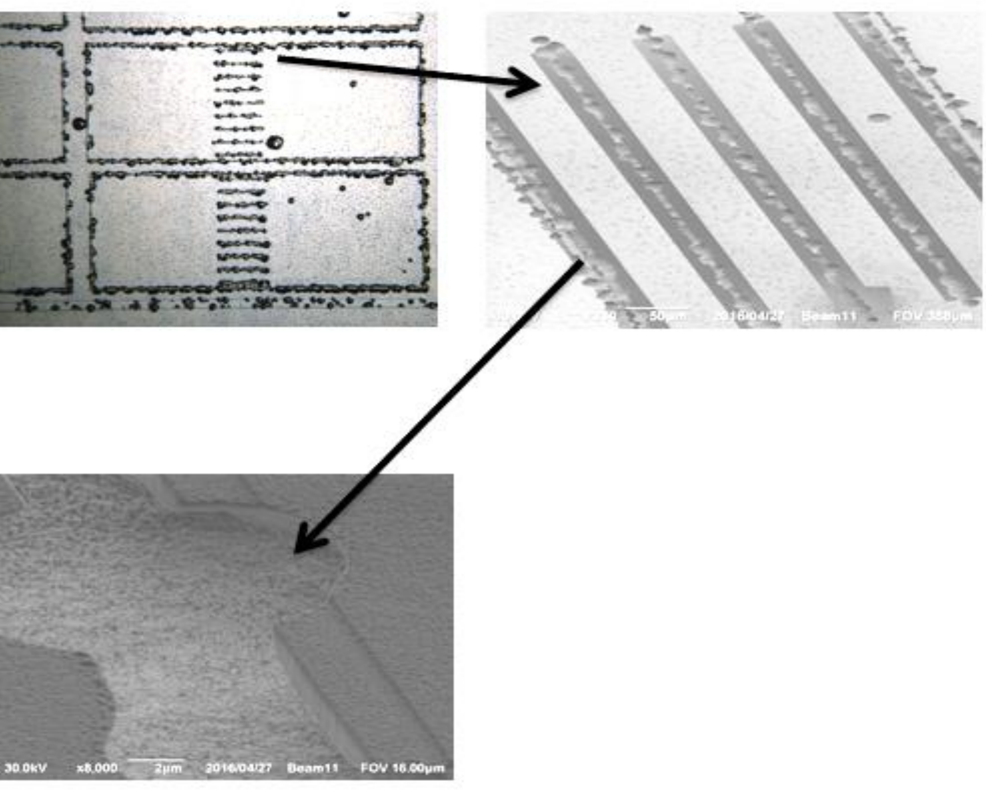


Figure 5.37: SEM pictures of the results of post trench etch annealing at 1550°C in H_2 for 15 min 2it/min

The type of the furnace that was used can cause this; the furnace has to evacuate the H_2 gas out of the furnace very fast at a very short time to make sure the duration of annealing is limited to 2-3 minutes; even one more minutes can cause surface distortion similar (but not as severe) as Figure 5.37. This capacity doesn't exist in the furnace in Science City lab. The highest temperature that we could achieve without etching the material was 1000°C. This is mainly due to the lack of fast vacuum in the furnace.

At this temperature there are no apparent effect on the corners or surface, but the effect of hydrogen post etch treatment on the electrical performance of the device was not clear and hence a device was fabricated using post etch hydrogen treatment at 1000°C with flow rate of 2 litre/minutes for 30 minutes.

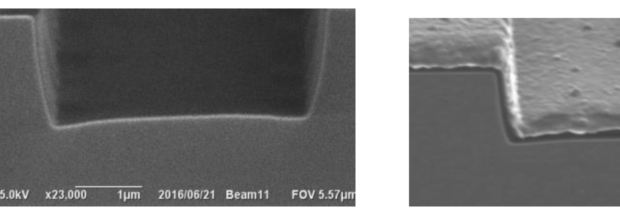


Figure 5.38: SEM images of trench structures (A)without annealing, (B)after H_2 post etch treatment at 1000°C for 30 min (Picture is taken after gate oxidation and gate metal deposition)

The results are similar to sacrificial treatments, higher mobility is achieved using hydrogen post etch treatment as can be seen in Figure 5.39. Though as can be seen in figure 5.40, the gate source leakage current has

increased. Since the mobility is higher, we assume the traps density has improved, and the leakage current seems to be due to the roughness caused by etching of surface. As discussed previously, hydrogen can terminate the dangling bonds on the surface and that can results in higher mobility. From the sever roughness in Figure 5.37, it can be concluded even at lower temperature the roughness is resulted from the hydrogen etching and hence results in higher leakage current.

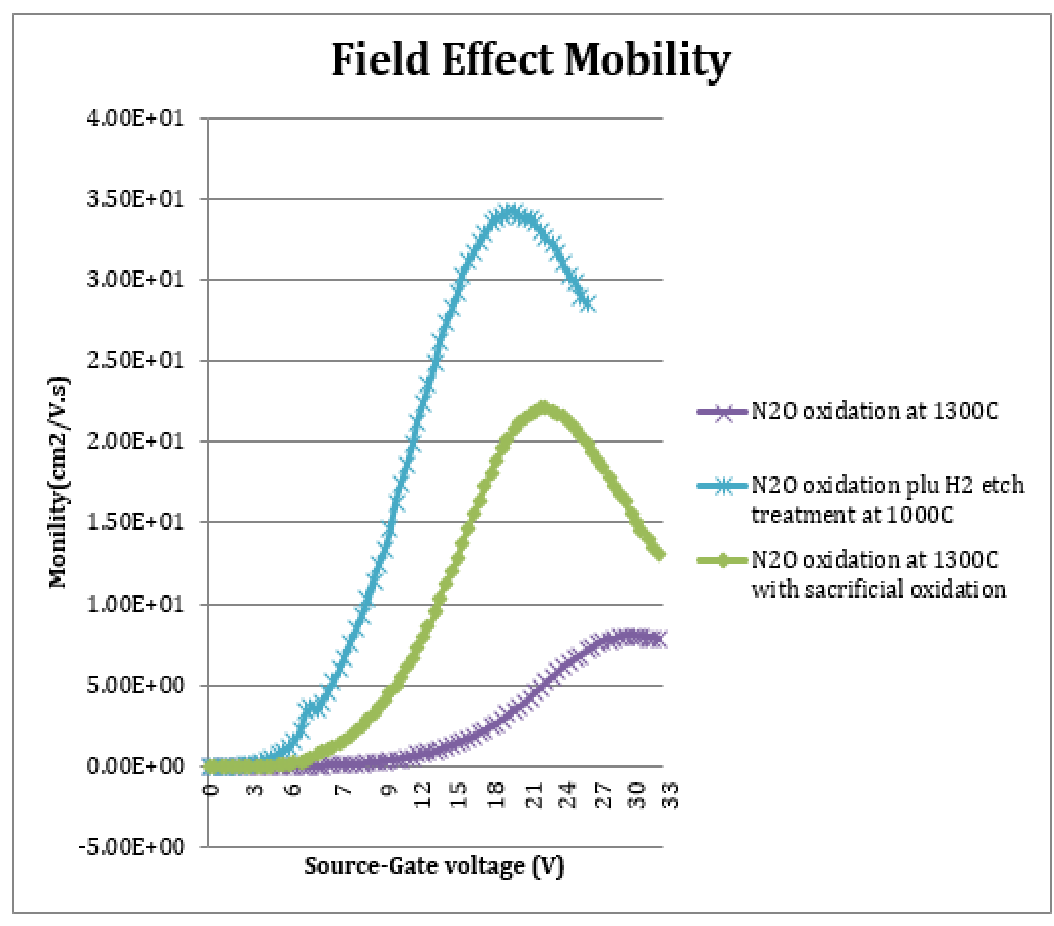


Figure 5.39: Comparison of motilities using post etch treatments

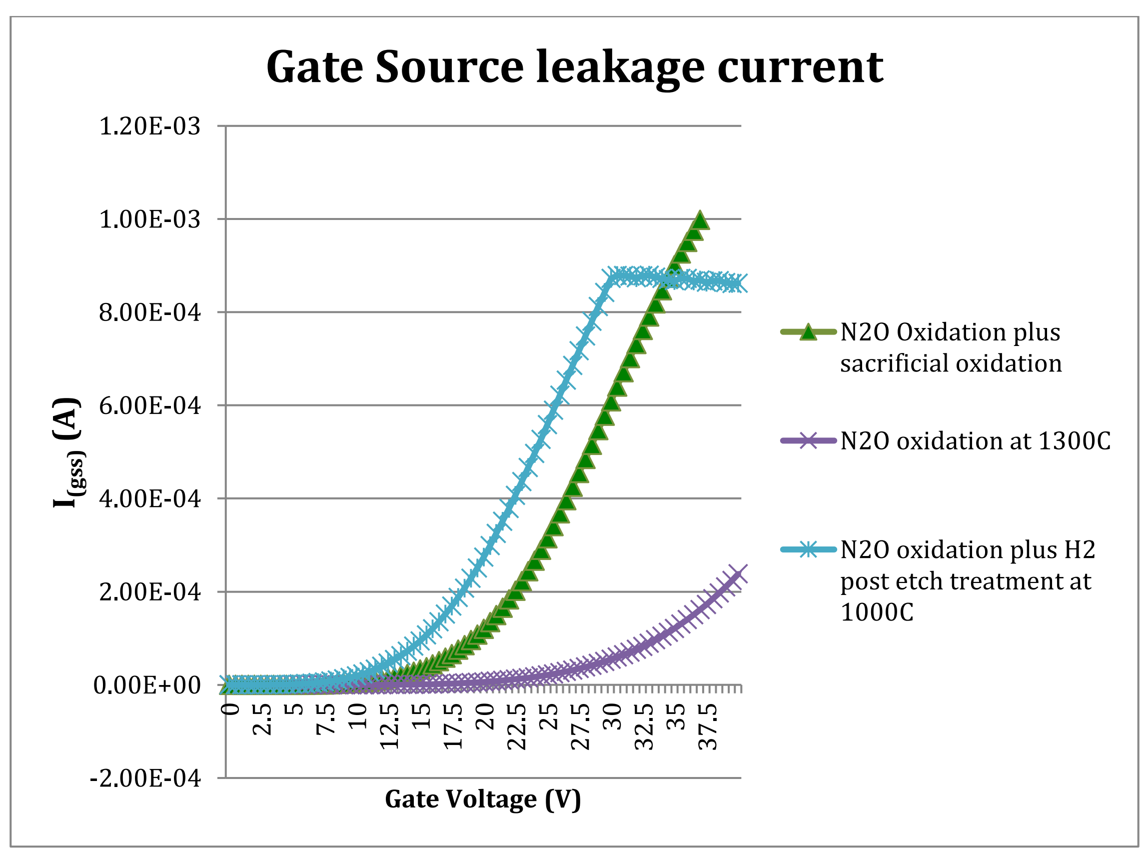


Figure 5.40: Comparison of gate source leakage current using post etch treatments

5.3.5 Comparison of all treatments types

Current density is measured from the devices with 9 trenches of width of 4 µm, trench distance of 32µm and trench length of 500 µm (total area of 0.146mm^2). Figure 5.41 shows the measured current densities of all the trench MOSFETs.

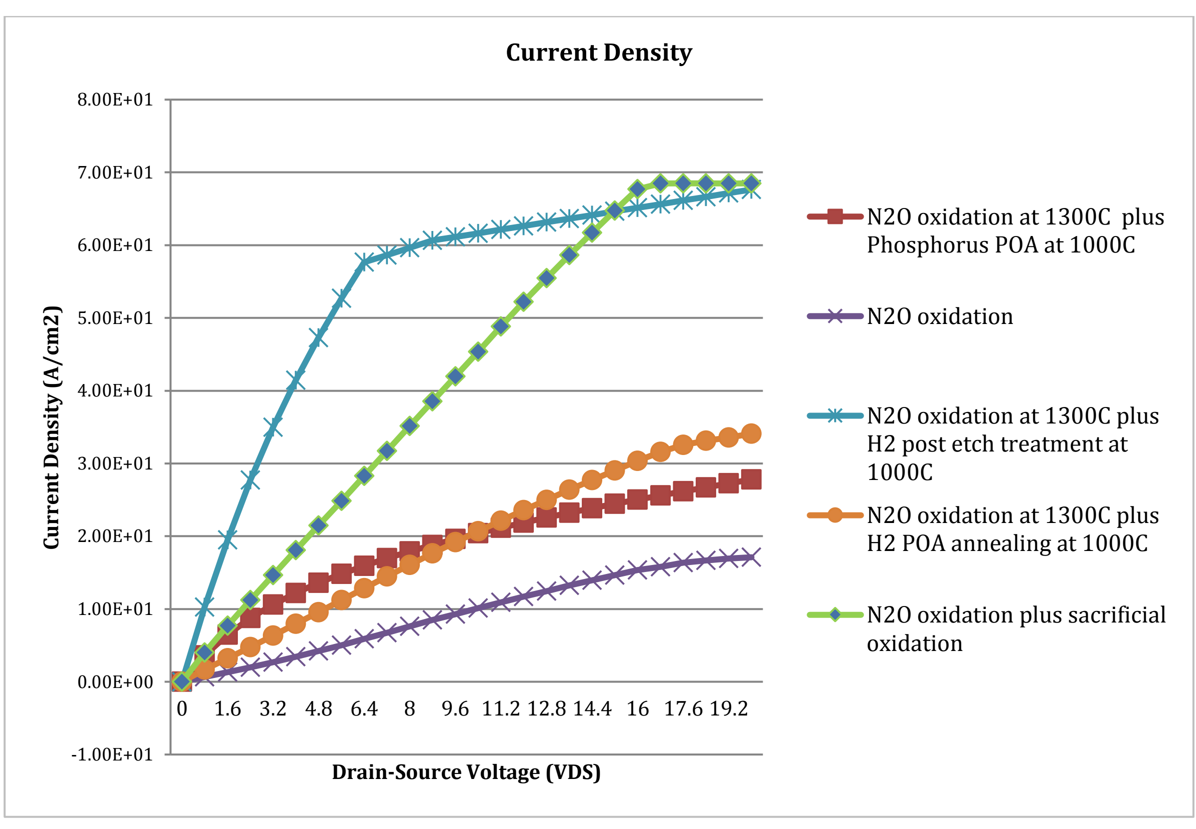
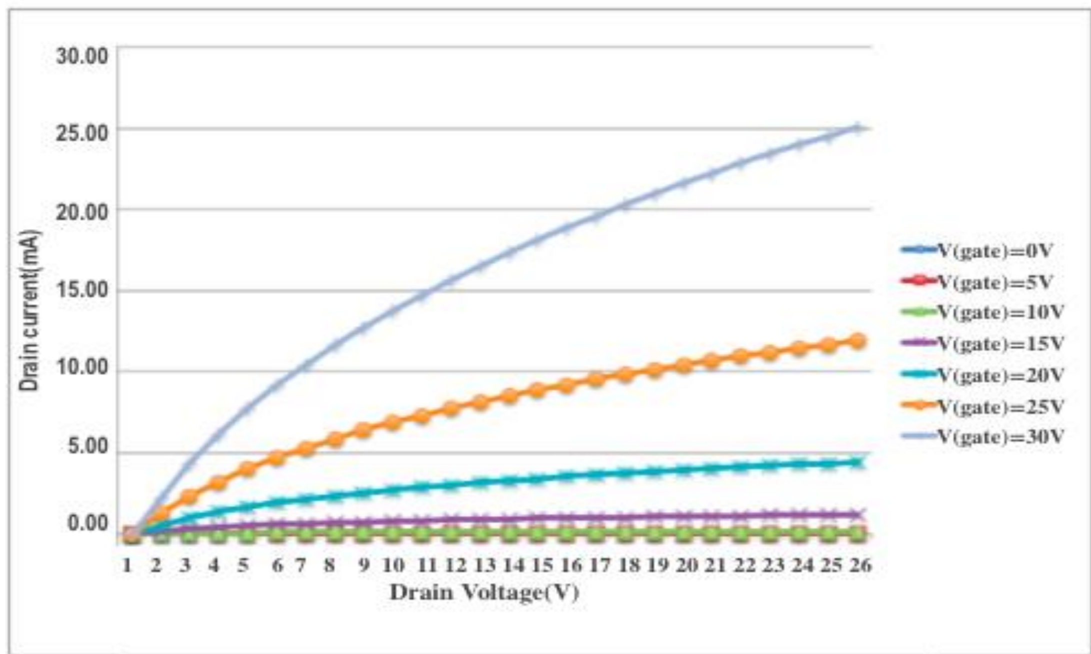
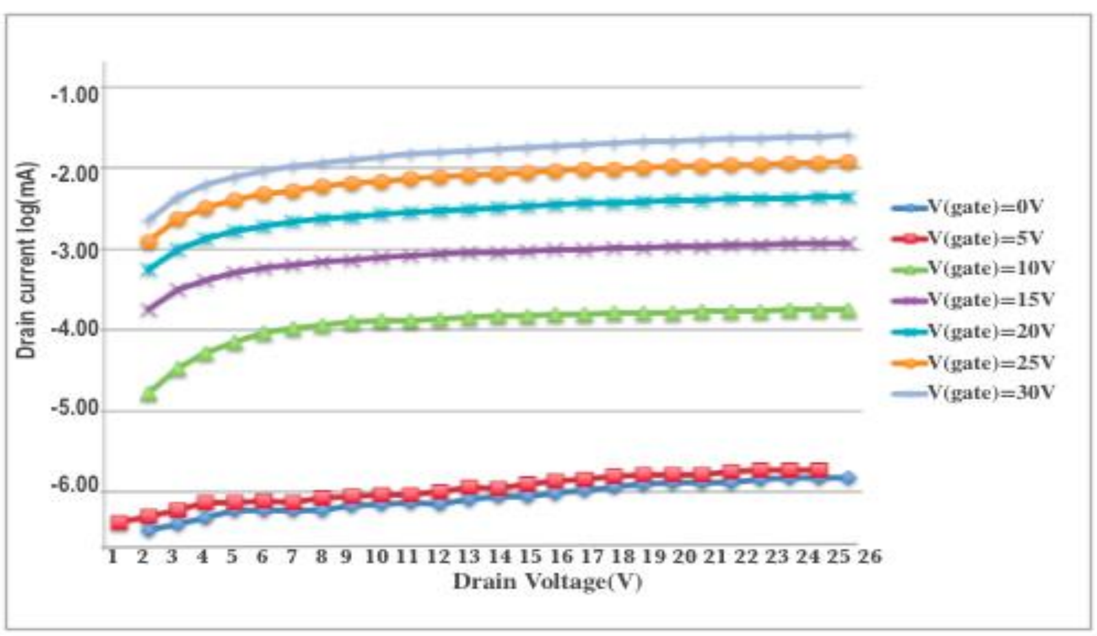


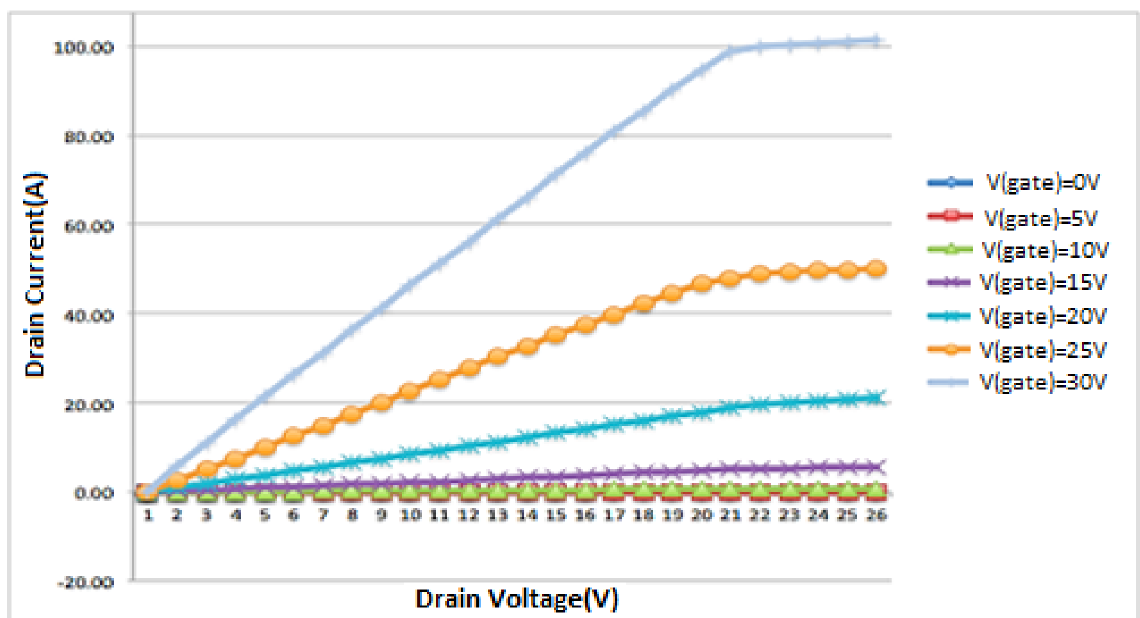
Figure 5.41: Comparison of current densities for trench MOSFETs with different post etch and post oxidation treatments (Vg=20 for all the cases)



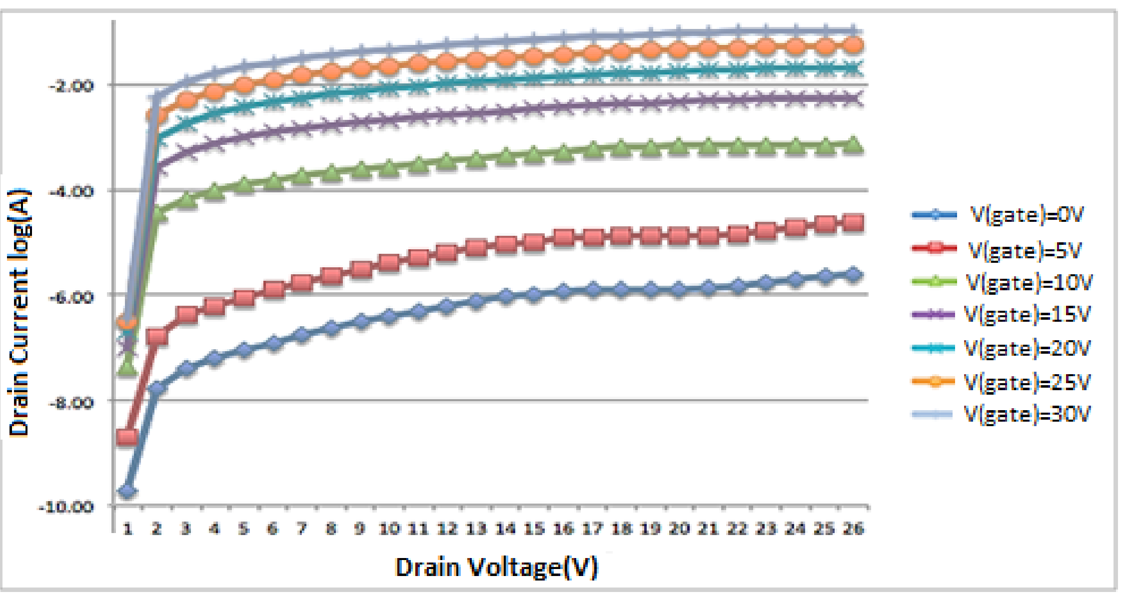
(A) I-V characteristics of a trench MOSFET with 9 trenches (100μm long)



(B) Log(I)-V characteristics of a trench MOSFET with 9 trenches (100μm long)



(C) I-V characteristics of a trench MOSFET with 9 trenches (500μm long)



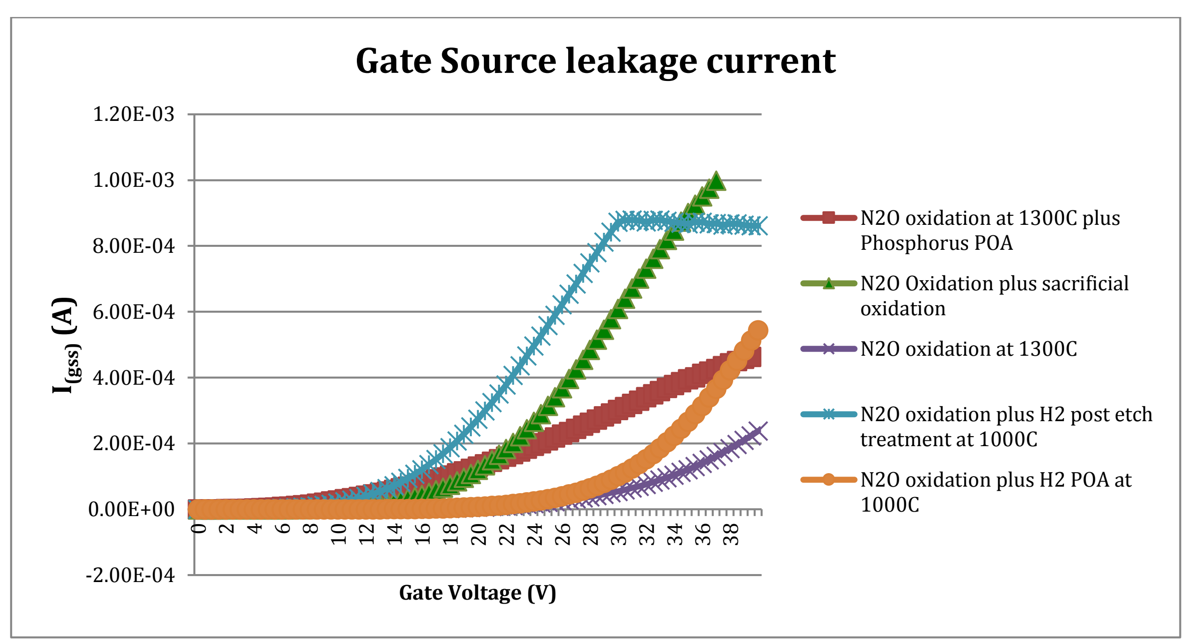
(D)Log(I)-V characteristics of a trench MOSFET with 9 trenches (500μm long)

Figure 5.42: I-V characteristics of trench MOSFETs with different number of trenches and different trench length. The current is proportional to the total trench length

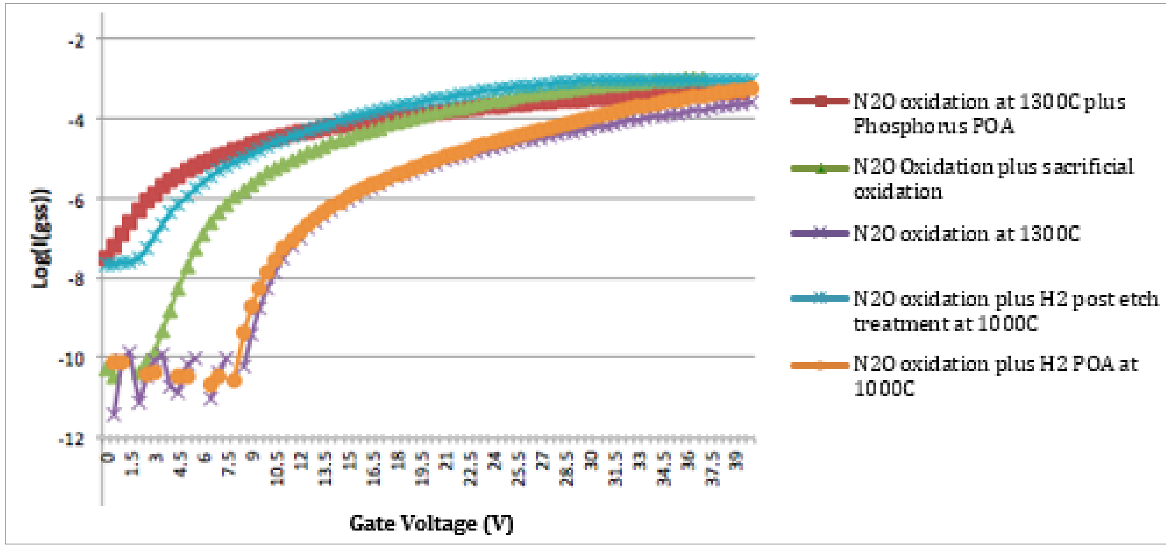
Figure 5.42 shows the I-V characteristic of trench MOSFETs (using phosphorus POA) with different trench length. This graph clearly shows that numbers of trenches are linearly proportional to the current. Hence we can assume that if we keep the same number of trenches and reduce the trench width and the distance between trenches to 2 µm, we should achieve the same current, but in a smaller area, hence the current density will increase. Table 5.7 lists the optimised current density. The assumption is that trenches have width of 2 µm and are located 2 µm from each other (Total area of 2,000 $µm^2$ for 9 trenches with width of 500).

The commercialised devices usually do not include the area (specially the active area) in their datasheets. From limited information [47] ROHM first commercialised SiC trench MOSFET had 100 A for active area of 3×3 mm^2. This results in current density of $1.1 kA/cm^2$. The current has increased to 500A but the area is not disclosed.

When looking at current density it is important to measure the leakage current to make sure high current is not due to the leakage current.



(A) I_{gss} vs. gate voltage



(B) Log(I_{gss})vs. gate voltage

Figure 5.43: Gate source leakage current (I_{gss}) of trench MOSFETs with different post etch and post oxidation treatments

Gate source leakage current ($\boldsymbol{I_{gss}}$) (Figure 5.43) and subthreshold leakage current(Figure 5.44) both confirms that the highest leakage current belongs to post etch treatment, white the devices without any treatment and the trench MOSET with H_2 POA have the lowest gate source leakage current

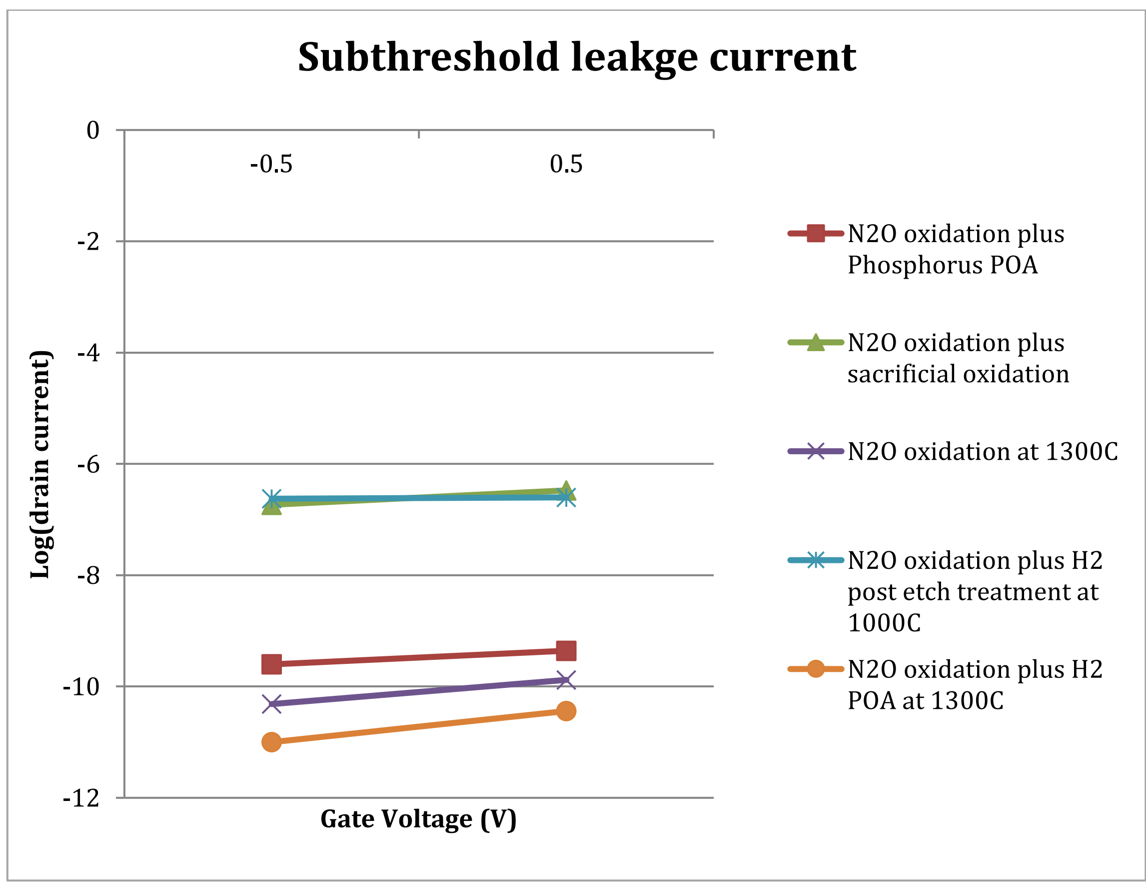


Figure 5.44: Subthreshold leakage of trench MOSFETs with different post etch and post oxidation treatments

Gate oxide recipe	**Vbr Vg= 0 V I_{DS} =0.01 mA**	**Measured Current density** A/cm^2	**Optimized Current density** A/cm^2	**Measured** $R_{DS(on)}$ $(m\Omega.cm^2)$	**Optimized** $R_{DS(on)}$ $(m\Omega.cm^2)$
1 hour O2 plus 3 hours N2O annealing	435	5	370	1.18E+05	1.62E+03
4 hour N2O oxidation plus phosphorus POA at 1000C	354	27	2000	3.72E+02	5.09E+00
4 hours N2O oxidation plus 4 hours sacrificial oxidation in N2O	195	70	5000	2.27E+02	3.12E+00
4 hours N2O oxidation at 1300C	410	17	1200	1.16E+03	1.59E+01
4 hours N2O oxidation plus 1 hour H2 post etch treatment	405	70	5000	1.03E+02	1.40E+00
4 hours N2O oxidation plus 1 hour H2 POA	363	34	2900	5.09E+02	6.97E+00

Table 5.7: Comparison of electrical parameters measured from trench MOSFETs with different post etch and post oxidation treatments

The $R_{DS(on)}$ values are also listed in Table 5.7 under measured$R_{DS(on)}$. Same as the current density, the measurements are based on the fabricated devices with area of 0.146 mm^2 and optimised values are based on the area of 2,000 μm^2(trenches of width 2 μm and distance of 2 μm). This is not a good

estimation for $R_{DS(on)}$ as the relationship between the trench distance and/or width and on resistance is not linear though this was solely used to get an estimation values of what could be expected from the second generation of trench MOSFETs.

The $R_{DS(on)}$ of commercial devices from ROHM are in the range of 0.79 to 2.4 $m\Omega.\mathbf{c}m^2$. Comparing the values of $R_{DS(on)}$ with current density, shows that at higher $R_{DS(on)}$, the current density is usually much lower. The values of measured and optimised $R_{DS(on)}$ for direct O_2 growth (with N_2O POA) and direct N_2O growth are still much higher compared to the rest of trench MOSFETs with post etch treatment or post oxidation annealing, Therefor some kind of treatments(post etch or POA) is necessary to reduce $R_{DS(on)}$.

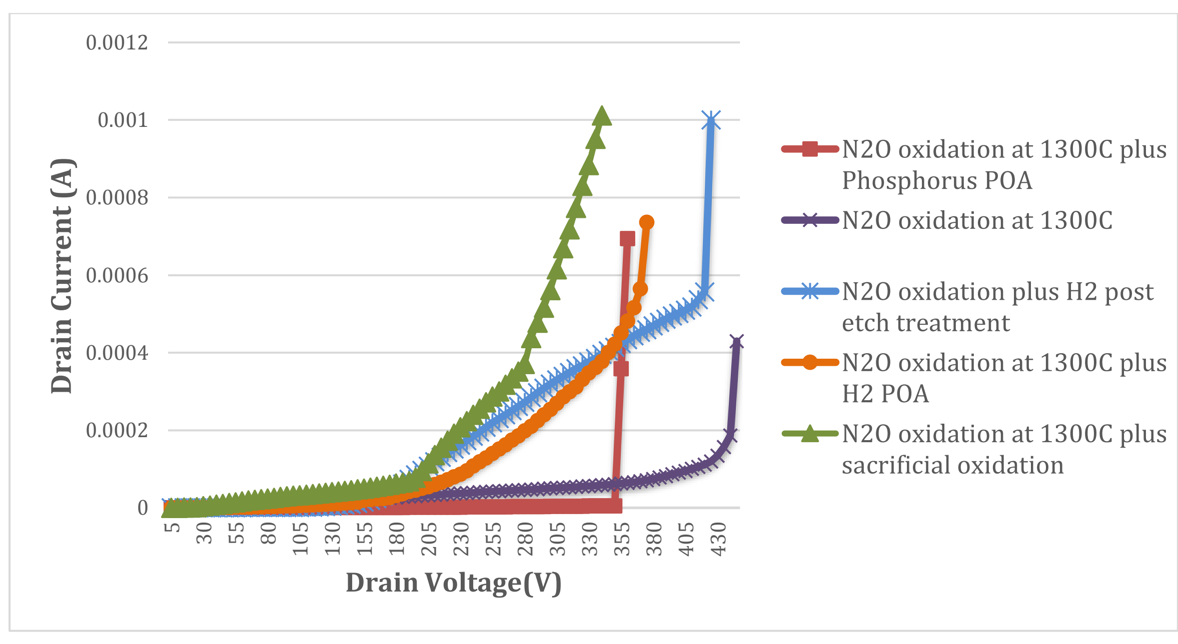
The on resistance of devices with post etch treatments are lower than the devices with post oxidation annealing. Since all the structures are using the same structures and same wafer, it can be concluded that the change in on resistance is representing the channel resistance.

The last parameter to compare is the breakdown value. The breakdown voltage expected from simulation results (Chapter 3) is around 350 V. The breakdown is measured on the devices of size equal to 0.146 mm^2 with only 9 trenches of length 500 μm.

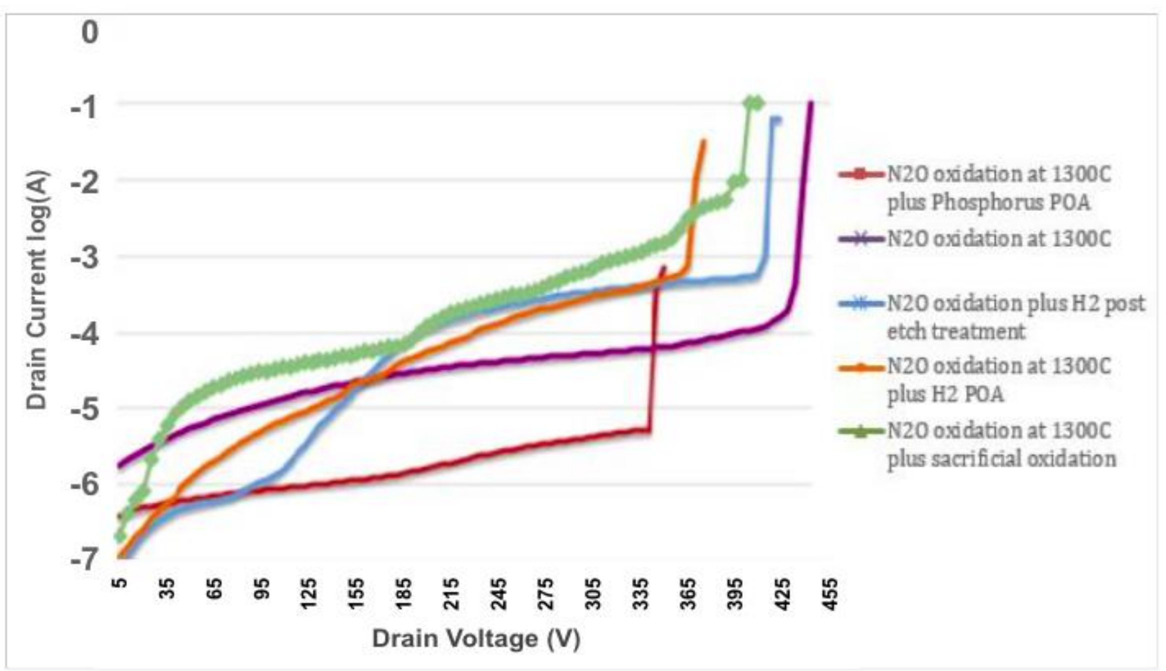
While devices with direct N_2O growth or with phosphorus POA enter hard breakdown, other devices seem to have a soft breakdown and a hard breakdown.

This can be because of the poorer quality of the gate oxide in the bottom of trench (as discussed before) since the breakdown in all devices happen in the oxide in the trench bottom.

Increasing the drain voltage has resulted in more leakage source drain leakage current and hence the devices have entered a soft breakdown. In an ideal device, the leakage current should be independent of the drain voltage until the point of breakdown. Though it is expected that the leakage current before breakdown could be easily controlled using a gate shield, or sacrificial trenches that help to attract the high electric field. Therefor increasing the electric field does not affect the bottom of gate oxide and hence the leakage current would be more independent of the voltage. This will also increase the breakdown voltage.



(A) Breakdown voltage (showing current)



(B) Breakdown voltage (showing log(current))

Figure 5.45: Comparison of breakdown voltages of trench MOSFETs with different post etch and post oxidation treatments

5.4 Conclusion

It is clear that the quality of oxide is still the biggest problem in these devices. The oxide quality needs to be improved to achieve a device comparable to the commercialised device. As the results show the quality of the surface after etch, is as important as the oxidation process. Leakage current from roughness and low mobility due to the oxidation process seems to be the two area that needs to be improved. Though the hydrogen post oxidation annealing seems to be the best results, one must notice that the reliability of different devices in higher temperatures are still unclear. The other main aspect that was not considered in this work and is recommended for the second generation devices is: which annealing results in stronger bonds in higher temperature or electric field? How would Si-N or Si-H bonds react at these conditions?

The other question is why mobility was lower in comparison to the literature? To study if etching has caused the reduced mobility in comparison with the planar MOSFETs, a set of trench MOSFETs and planar MOSFETs were fabricated together in the same batch undergoing the exact same process at the same time. The results shows that the highest achieved mobility is 9 $cm^2/V.s$ for planar MOSFETs using phosphorus passivation and around 3.9 $cm^2/V.s$ for direct N_2O growth without annealing. This shows that the source of the low mobility is the quality of the oxide and not the etching process.

There were patterns similar to contamination on the surface of samples after thermal oxidation and also the thickness of oxide was different throughout on a small sample. Due to the lack of time to carry on more experiments on oxide to improve the high tech furnace, the experiments were set to improve the mobility with the goal of comparing different annealing recipes together to decide how annealing affects other electrical. It is very important to expect a complete overview of the results instead of focus on one or two parameters. A clear example was the sacrificial oxidation in the previous section, where mobility was improved but more experiments prove that the leakage current and breakdown voltage was degraded.

Our expectation is that once the furnace is fixed, the best recipe could be chosen in future to fabricate a trench device with higher mobility.

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Chapter

6

Recommendation

6. Introduction

In this chapter, a few suggestions are provided on how to improve the device and fabricate the second generation of Trench MOSFETs. The goal is to improve the electrical properties of the device such as current density and breakdown voltage. It is important to improve these parameters further to make sure the device can operate in higher voltages as well. This would also help to test parameters such as leakage current and mobility in high voltages and optimise these values. The same parameters as the fabricated trench

MOSFETs have been used in all the simulation and hence a breakdown voltage of at least 1.2kV is expected.

6.1 Improving Current Density and Breakdown Voltage

The first suggestion is to improve the structure in order to increase the current density and breakdown voltage. This will help to test the device at higher voltage and current. Structure of the device has an important role in increasing current and breakdown voltage. By increasing channel length, or number of channels in trench MOSFETs, we can increase the current density. The results for increasing number of channels were presented in Chapter 5.

The structure could be improved to get higher number of channel in less area to make the device smaller and reduce on resistance. The same improvement to the structure can improve the breakdown voltage as well. Using Warwick University cleanroom, if the mask aligner microscope is improved, trenches as close as 1 μm could be achieved without any gate protection (Figure6.1). The simulation results show that if the distance between trenches is reduced to 1μm, the highest breakdown voltage is achieved. The current structure is made with trench space of 32μm and hence there is a hug space to improving current density and breakdown voltage by reducing the space between trenches.

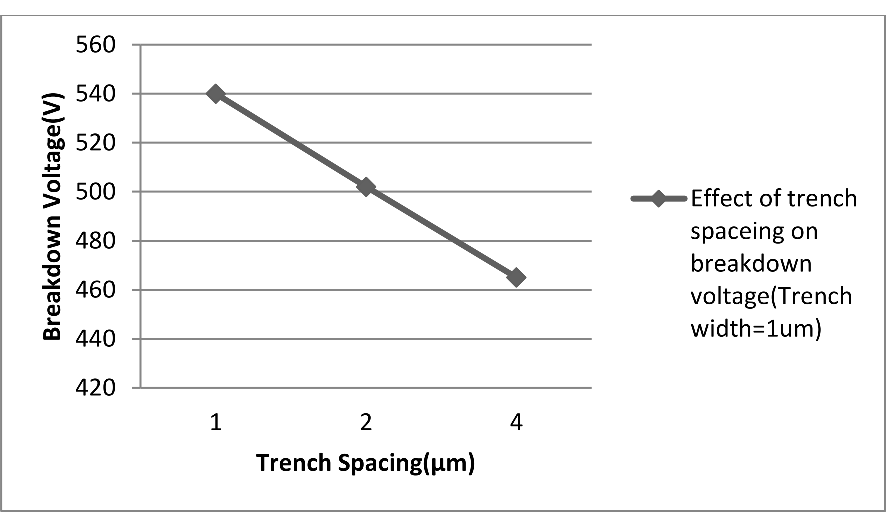
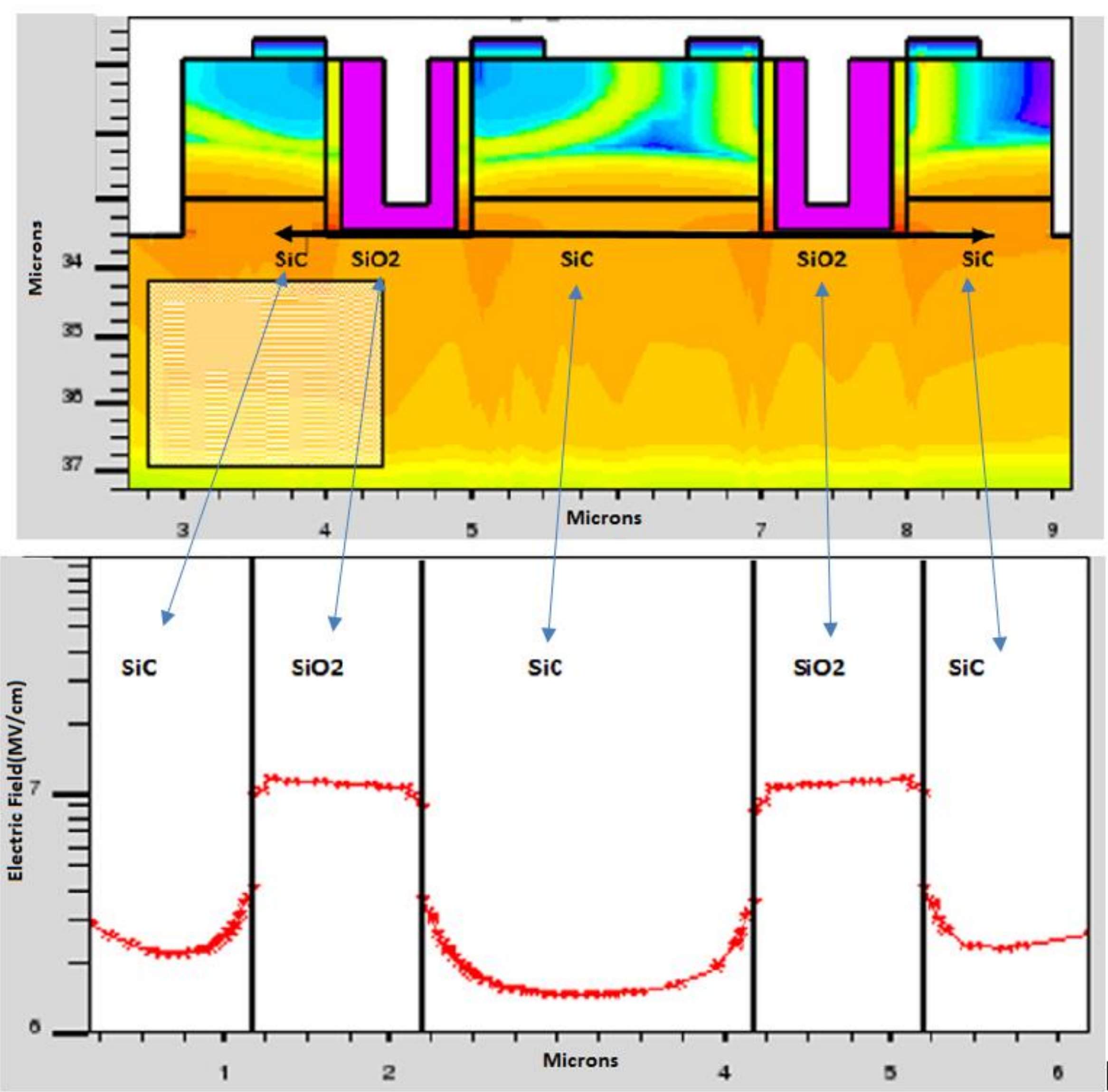
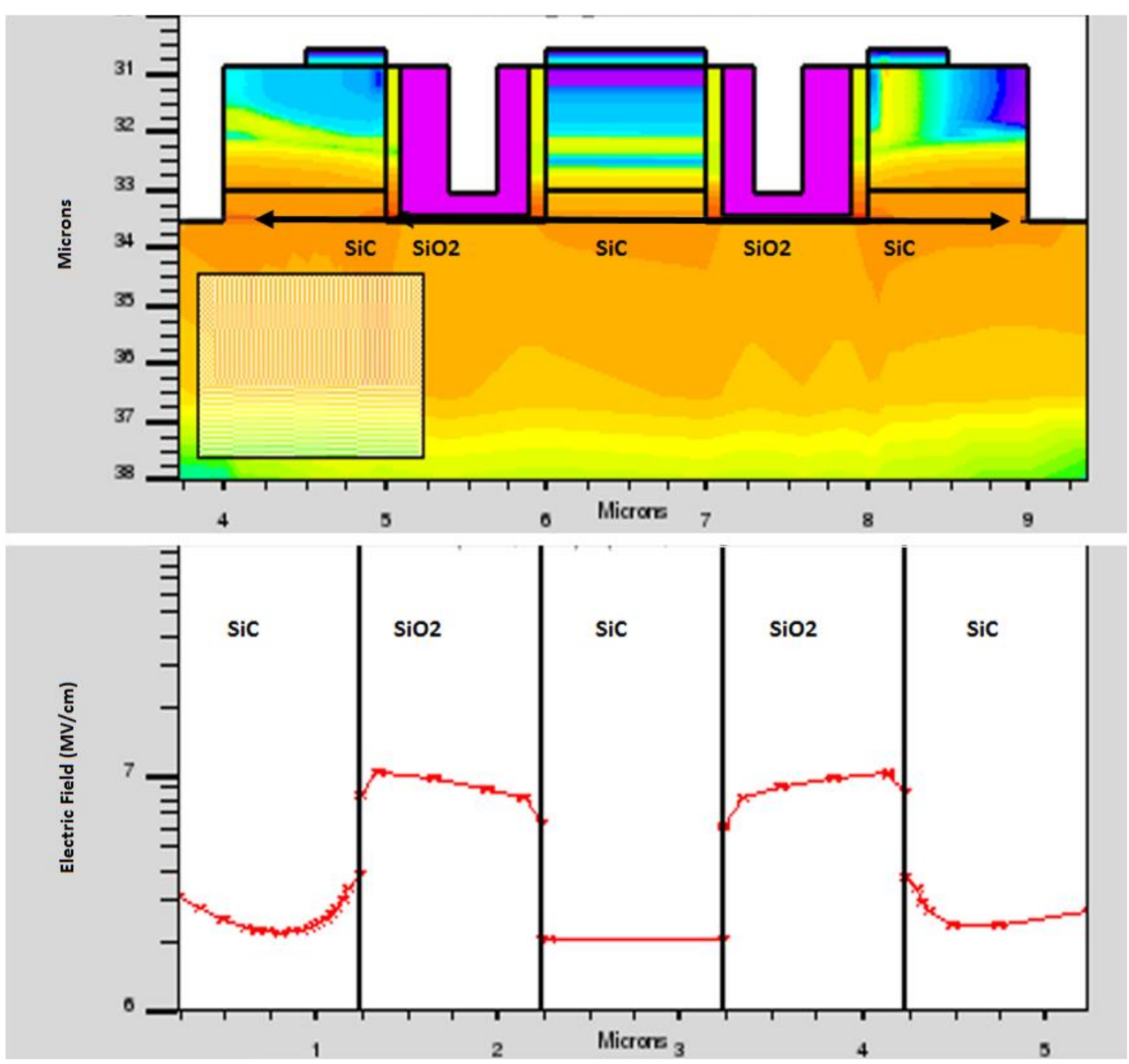


Figure 6.1: Effect of space between trenches on breakdown voltage

The results from simulation show that breakdown happens in the corners of trenches in all these cases. Decreasing the trench spacing, decrease electric field at the corners of the trenches and hence increases the breakdown voltage. Corner of trench is exposed to electric field in P-N junction as well as gate electric field. As simulation shows trench corners attract crowding of electric field. When reducing trench spacing, the P-N junction electric field is supported by more trenches and hence the electric field in the trench corners decreases.



(A) Space between trenches 2 μm



(B) Space between trenches=1μm

Figure 6.2: Effect of trench spacing on the electric field in a Trench MOSFET with (A) trench spacing=2μm (B) trench spacing=1μm. It can be seen that when trenches are closer, the electric field in the oxide layer at the trench corners is reduced

Though simulation confirms that trench width, does not play an important rule. Only when the trench gate width is reduce to 1 μm there is a small increase in breakdown voltage equal to 20V. At higher trench width the breakdown voltage stays the same

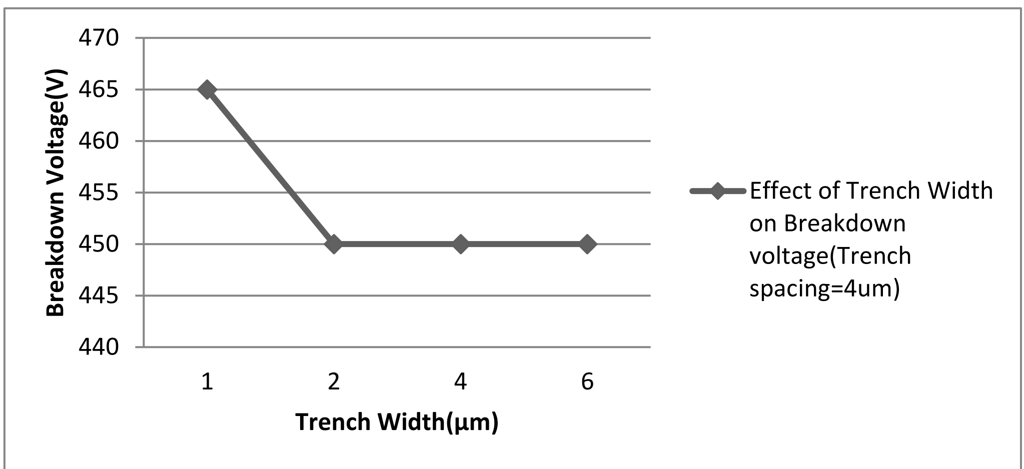


Figure 6.3: Effect of trench width on breakdown voltage

In both cases the breakdown happens in the corners of trenches. The result shows the highest breakdown voltage is achieved with spacing of 1µm and trench width of 1 µm. The breakdown in this structure happens at the corner of trenches at 540V. This prove that without a solution to protect the gate, even when the structure is optimised, 1.2 kV breakdown voltage will not be reached.

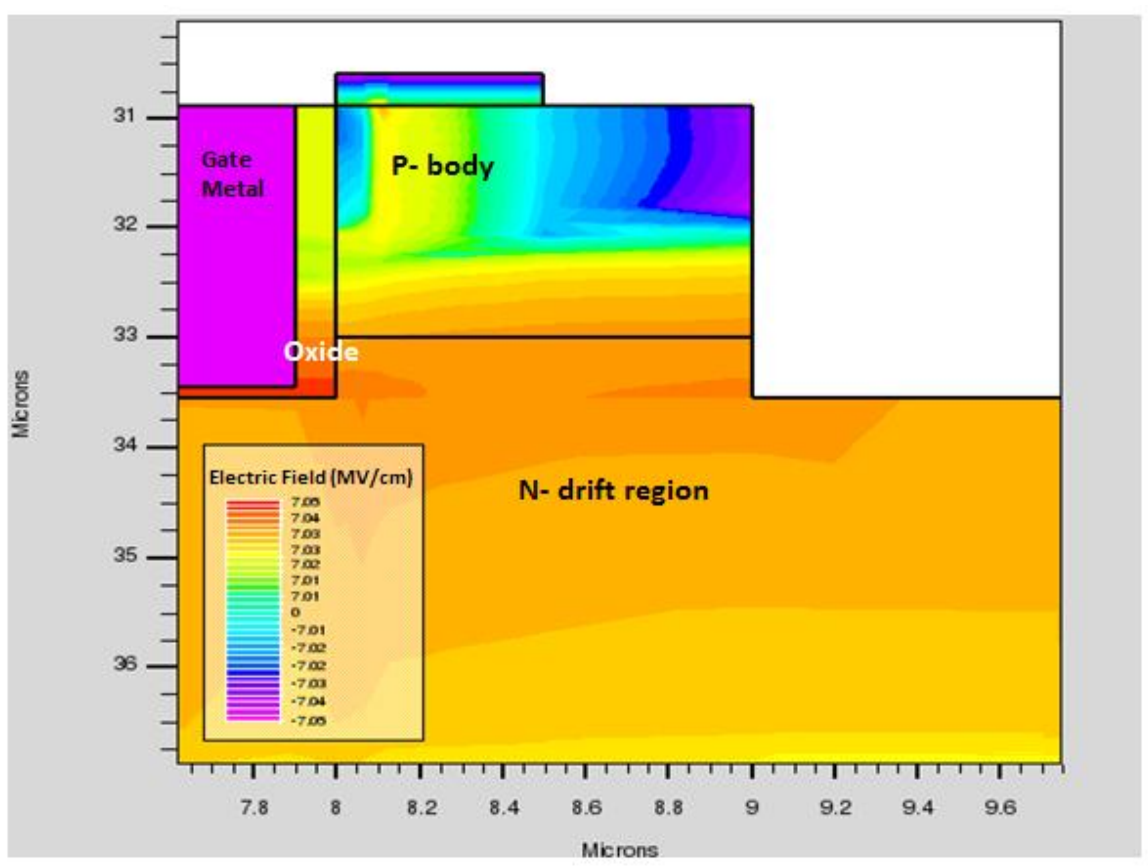


Figure 6.4: Trench MOSFET design with 1µm cell pitch, the breakdown happens in trench bottom and trench corners

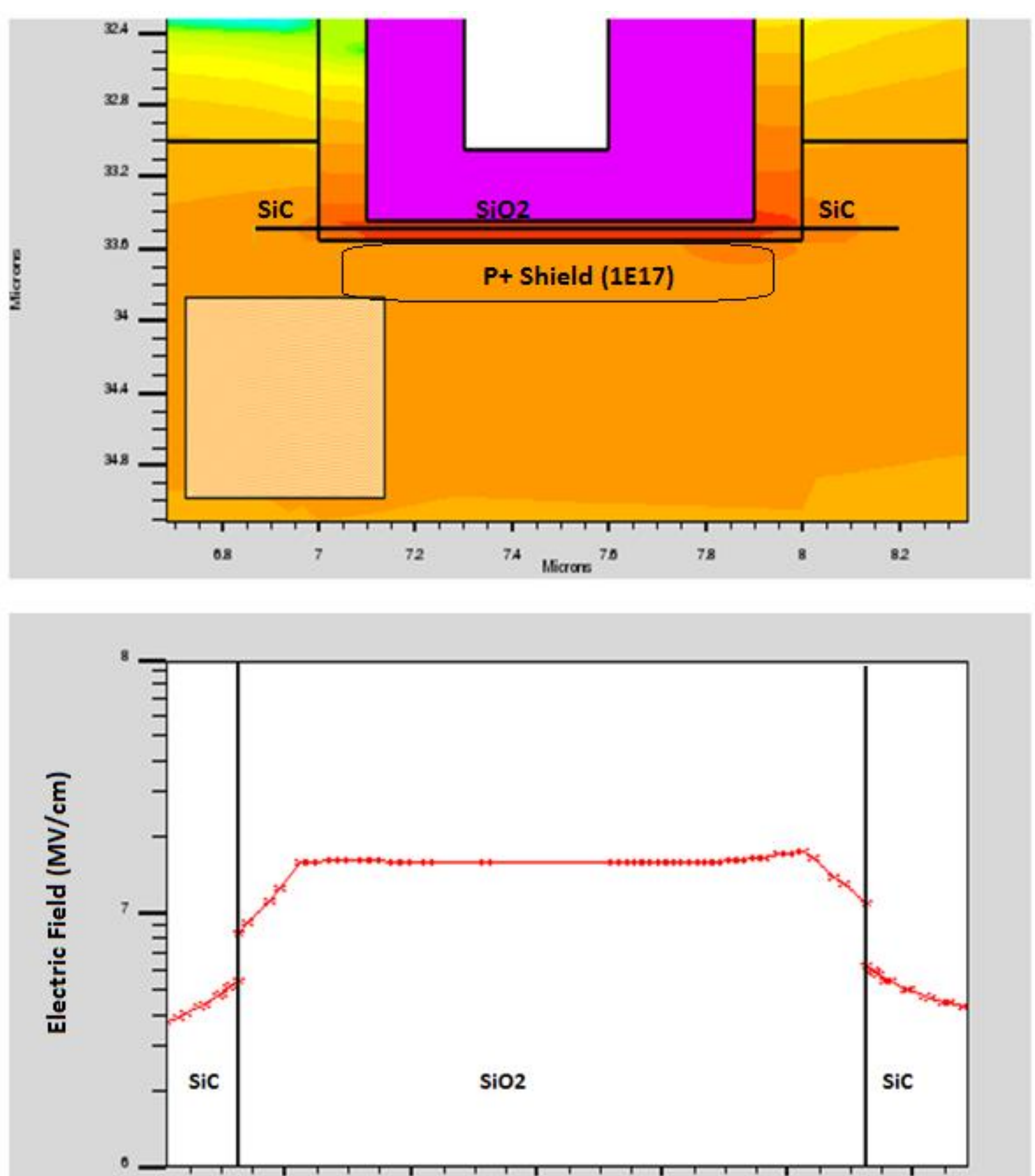
As mentioned earlier the drift region of this wafer is designed for breakdown voltage of at least 1.2 kV. Though as expected the breakdown in insulator layer has limited the device performance. To protect the gate insulator two options has been tested: 1) P+ shield layer 2) sacrificial trench.

6.1.1 Gate Shield

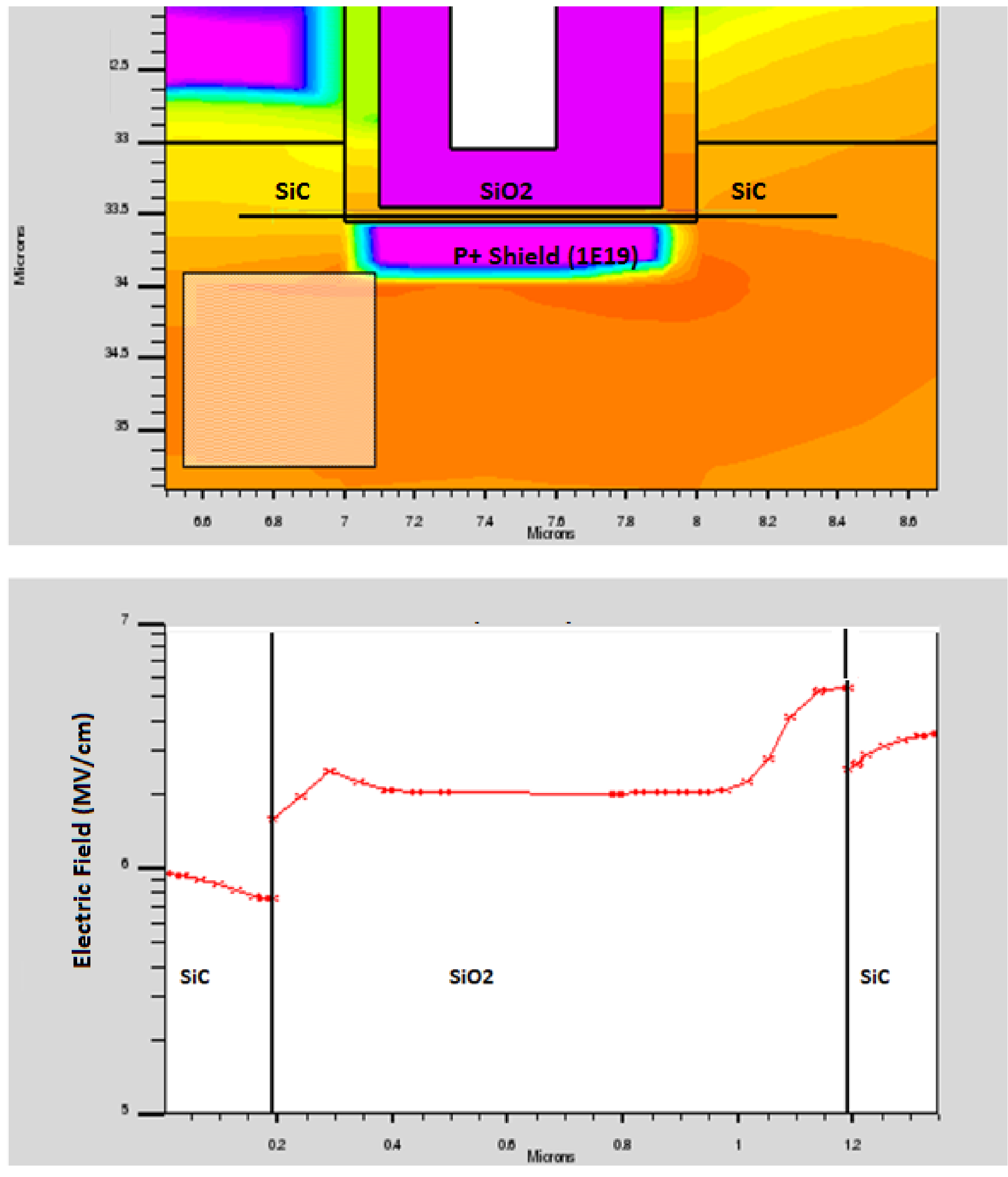
Using a P+ gate shield can help to protect the gate. Figure 6.5 shows the simulation results using two different doping (A) P+ shield with doping of $1 \times 10^{17}\ cm^{-3}$ (B)P+ shield with doping of $1 \times 10^{19}\ cm^{-3}$. The result shows that for case (A), even though breakdown increase to 1050V but the point of breakdown is still in the gate oxide. Case (B) results show that the point of breakdown in

this case is under the P+ shield region in SiC not the insulator. The other point of breakdown in this design is the corner of mesa etch.

The breakdown in this case is much higher at around 1305. The other advantage is that by using high doping the electric field on the trench bottom has decreased to around 6 MV/cm. This can help with reliability of the oxide. Baliga [1] has stated that by using P+ shield we can reduce the channel length to less than 1 μm while avoiding punch through in the P^- base. This can reduce the channel resistance and threshold voltage.



(A) Electric field across the device(shown with black line) with gate protection with the dopig of $1 \times 10^{17}\ cm^{-3}$



(B) Electric field across the device(shown with black line) with gate protection with the dopig of of $1 \times 10^{19}\ cm^{-3}$

Figure 6.5; Effect of P+ gate shield with different doping on the breakdown voltage, with lower doping like case (A), the breakdown still occurs in the SiO_2 layer, at voltages much closer to the breakdown voltage

As mentioned by using P+ shield with doping in range of $1 \times 10^{19}\ cm^{-3}$, the breakdown can happen in the corner of mesa trench. To help prevent breakdown in the edge of the device, there is a need for some sort of junction termination edge (JTE) solution. In this design we have used double trench JTE and the device can reach 1650 V. As can be see the simulation shows that highest electric field is located around the P+ region and the first trench corner. As you notice the breakdown voltage is higher than calculated parallel breakdown voltage. This can be due to the depletion region caused by P+ shield/n- drift region that is added to the P- body/n- drift region.

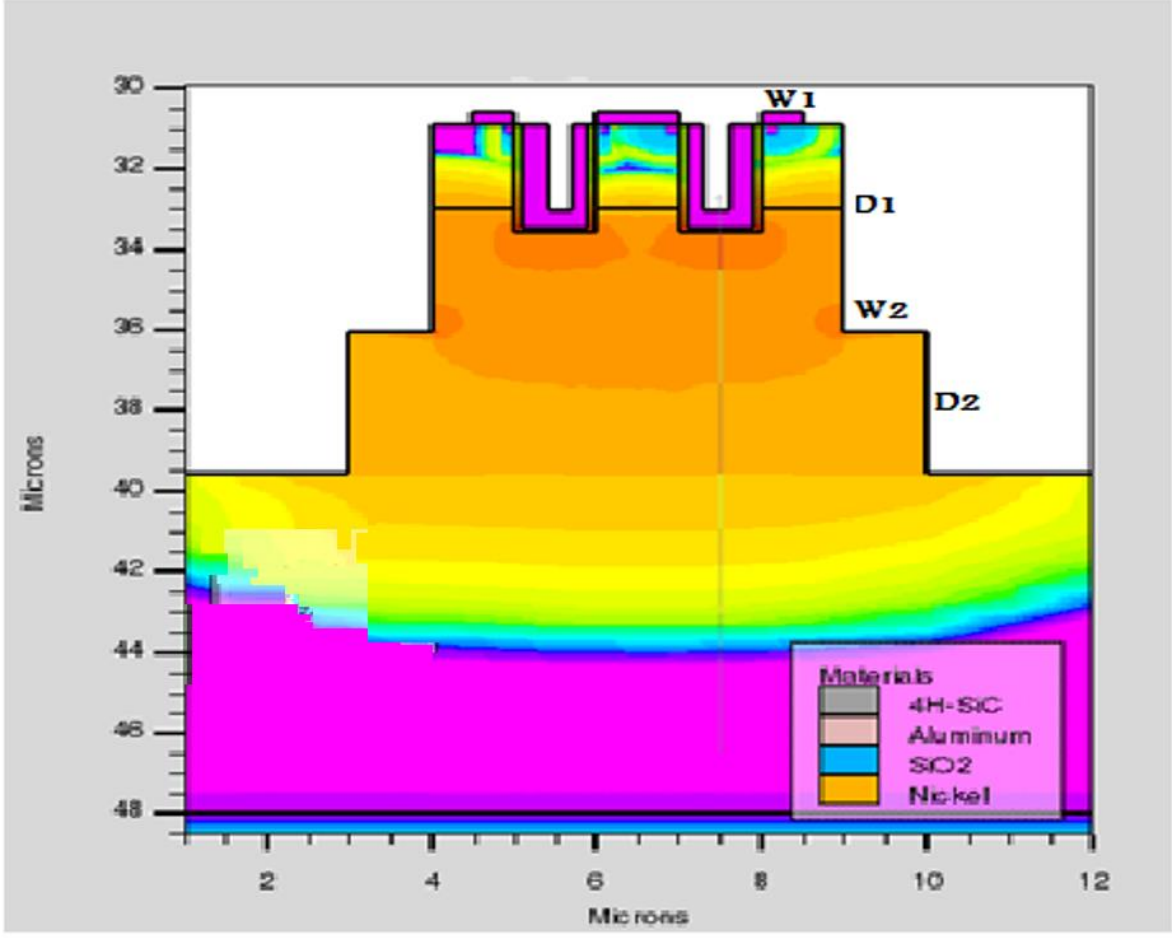


Figure 6.6: Trench MOSFET design with P+ gate shield and double trench JTE, highest breakdown voltage of 1650V is achieved.

Table 6.1 summarize the parameters that are used to design the junction termination. More details on how double trench JTE helps to improve breakdown voltage could be found in Chapter 3.

W1(μ)	D1(μ)	W2(μ)	D2(μ)
1	5	1	3.5

Table 6-1: Double trench junction termination parameters. The parameters corresponds to the parameters shown in Figure 6.6

6.1.2 Sacrificial Trench

The other method to decrease the high electric field on gate oxide and prevent breakdown at this point, is to use sacrificial trench structures. This includes using trenches between gates. As mentioned before, since trench corner attract crowding of electric field, they could be used to spread the electric field, hence if a trench deeper than gate oxide is etched between trenches, then breakdown voltage as high as 1500V could be achieved.

The disadvantage of this techniques is that the cell pitch would be bigger (for example in Warwick clean room, we need at least 3 μm cell pitch to achieve this structure) and hence to achieve the same current density the device would need to be bigger, the advantage is that we do not need to implant the bottom of trench and put the device through implant activation at high temperature.

Width of sacrificial trenches (μ)	Depth of sacrificial trenches (μ)
1	5

Table 6-2: Parameters used to simulation sacrificial trenches in middle of gate trenches. These parameters resulted in breakdown voltage of 1500V

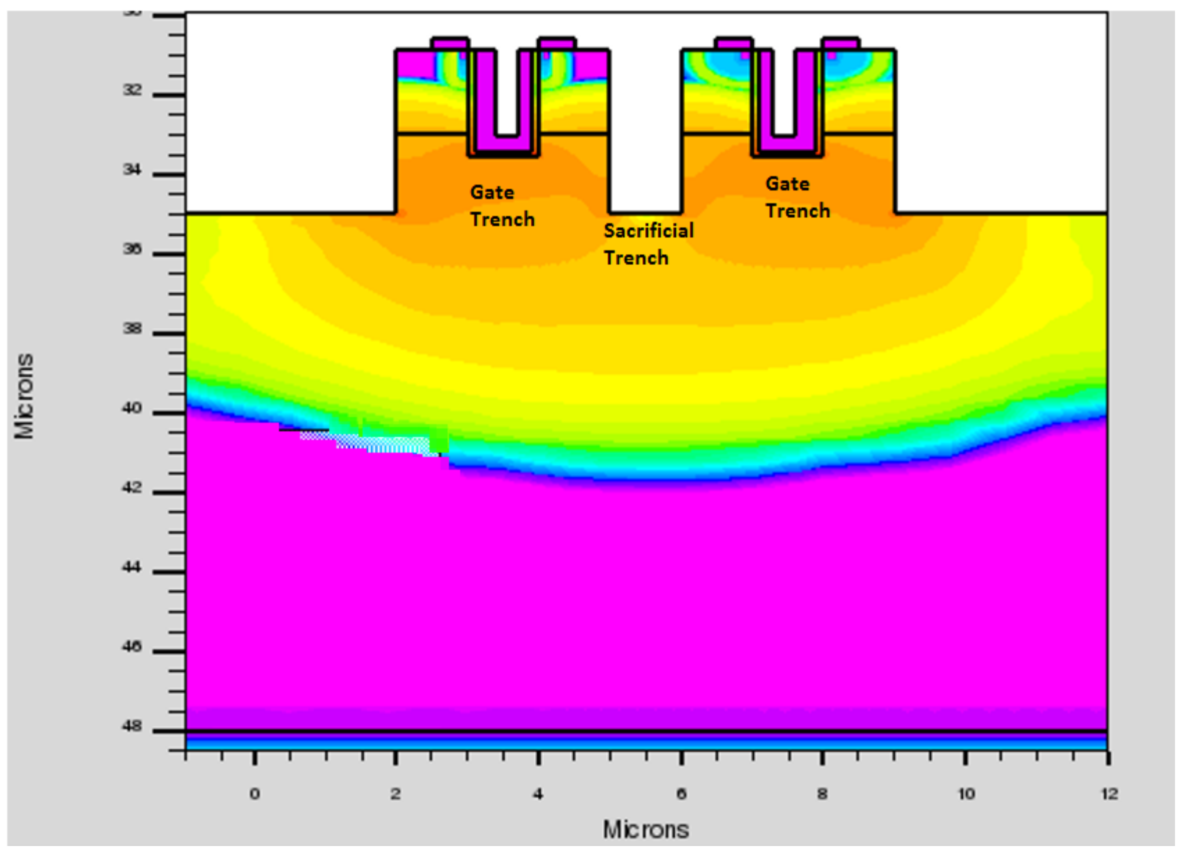


Figure 6.7: Structure of trench MOSFET with sacrificial trenches in the middle of gate trenches. The breakdown voltage is 1500V.

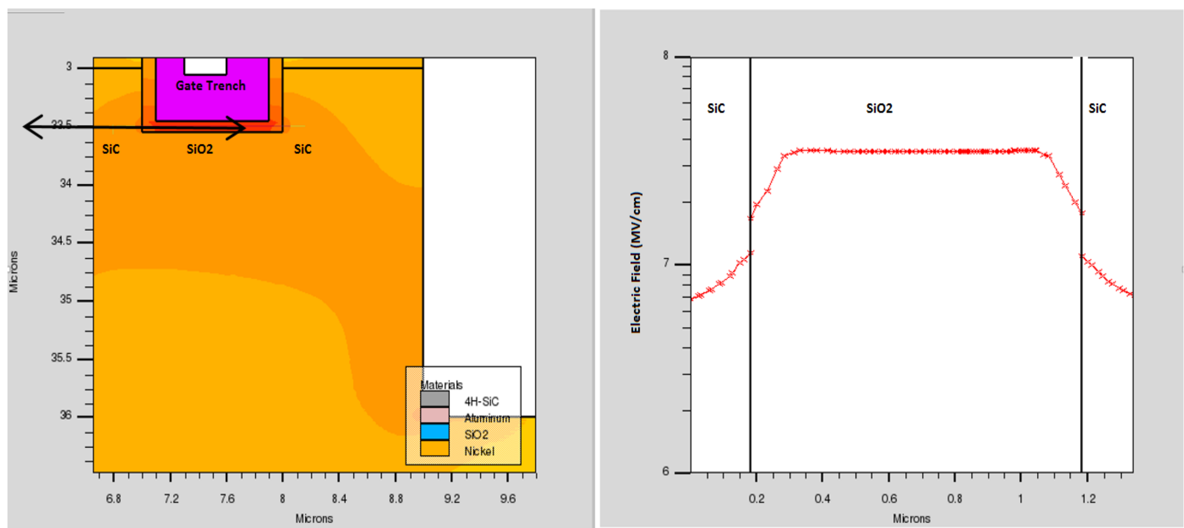


Figure 6.8: Electric field across trench corners and oxide layer with sacrificial trench design. The design is shown in Figure 6.7.

The electric field at the bottom of trench reaches 7 MV/cm at breakdown which is higher than the P+ shield with the dopig of of $1 \times 10^{19}\ cm^{-3}$. With the P+ shield the electric field at breakdown was 6 MV/cm. Further investigation is needed to determine If this difference has any effect on the reliability of the device.

6.2 Sacrificial Oxidation

The results shows that long sacrificial oxidation usually results in higher leakage current but better mobility. The main problem with long sacrificial oxidation was that most devices were unreliable and not functional. To improve this process, two shorter time (1.5 hours) sacrificial oxidation in N_2O were tested on MOS capacitors. 2 batches of samples (2 samples in each batch, and 30 trench MOS capacitors on each samples) were fabricated in separate process. The results showed that 100% of the MOS capacitors were functional and even though there was slight increase in the traps density but the increase was not significant. The trench MOS capacitors were not fabricated using this process due to the lack of time but this process is highly recommended for the second generation of trench MOSFET. In the conversation with different researchers during this work, it was always agreed that even though sacrificial oxidation does not eliminate pre-mature breakdown of the oxide, but the following gate oxide on the rounded corners are much more uniform.

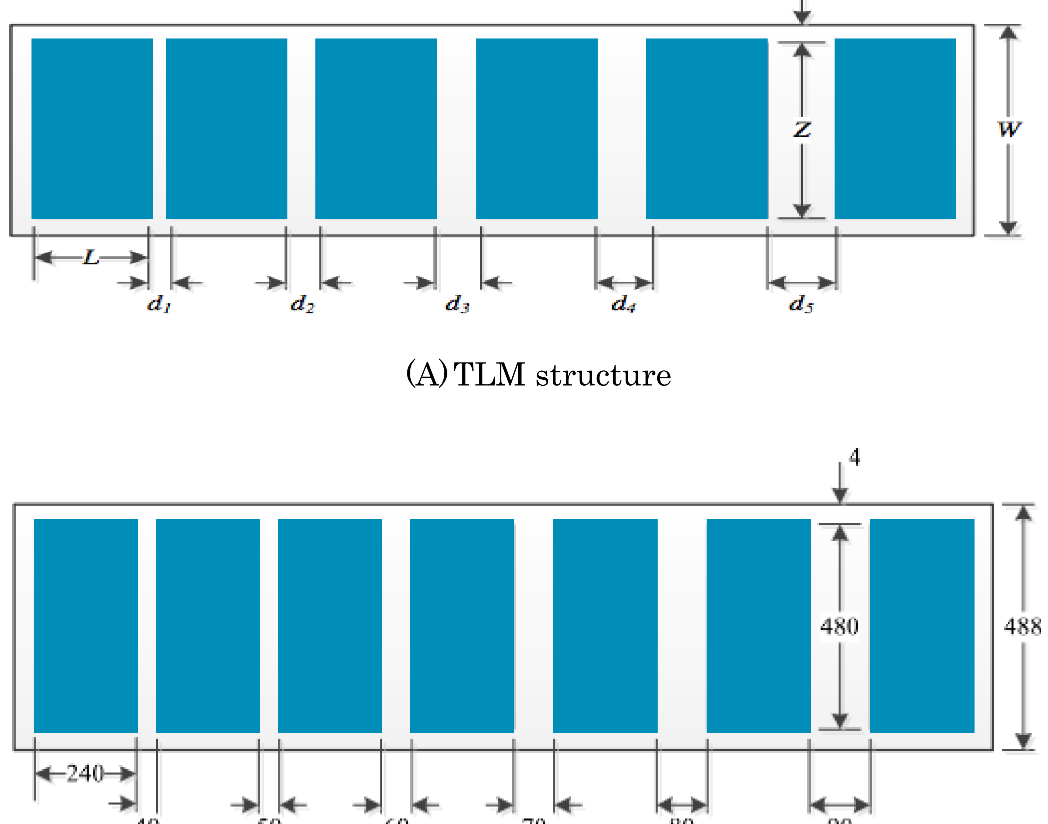
Method	Plane	Traps Density ($cm^{-2}eV^{-1}$) at $E_c = 0.2eV$
Dry O2-Diluted N2O annealing – 4hours sac oxide	$11\bar{2}0$	2.2x10e11
Dry O2-Diluted N2O annealing – 4hours sac oxide	Si Face	9.5x10e11
Dry O2-Diluted N2O annealing – 2 sac oxide(1.5hr)	$11\bar{2}0$	2x10e12
Dry O2-Diluted N2O annealing -2 sac oxide(1.5hr)	Si Face	8x10e12

Table 6-3: Comparison of sacrificial oxidation method and traps density for different trench plane.

6.3 Test Structures

6.3.1 Transfer Length Method (TLM)

One of the challenges in fabricating SiC MOSFET is forming low resistance ohmic contacts to p-type 4H-SiC. As mentioned in Chapter 5, this has been studied elsewhere [2][3] and the results from the literature were used in this work. It is recommended to include test structures on the wafer in future works, to measure the electrical performance of the contacts to make sure they have ohmic I-V properties. The most common method is transfer length method (TLM) that is used to measure the resistance of ohmic contacts. The test structure is illustrated in Figure 6.9A.



(A) TLM structure

(B) Suggested test structure, all dimensions are in μm [2]

Figure 6.9: TLM structure used to measure the resistance of ohmic

From the Figure 6.9A, the total resistance between any two adjacent contacts could be calculated by

$$R_T = \frac{R_{sh}d}{Z} + 2R_C \approx \frac{R_{sh}}{Z}(d + 2L_T) \qquad \text{Equation 6.1}$$

where R_T is the total resistance, R_{sh} is the sheet resistance, d is the distance, R_C is the contact resistance and L_T is the transfer length, which is defined as the distance over which most of the current transfers from the semiconductor into the metal, or vice versa. The assumption is that the contact length L is $\geq 1.5L_T$, where

$$L_T = (\rho_C/R_{sh})^{0.5} \qquad \text{Equation 6.2}$$

where ρ_C is the specific contact resistance. The total resistance is then plotted against various contact spacing as can be seen in Figure 6.10.

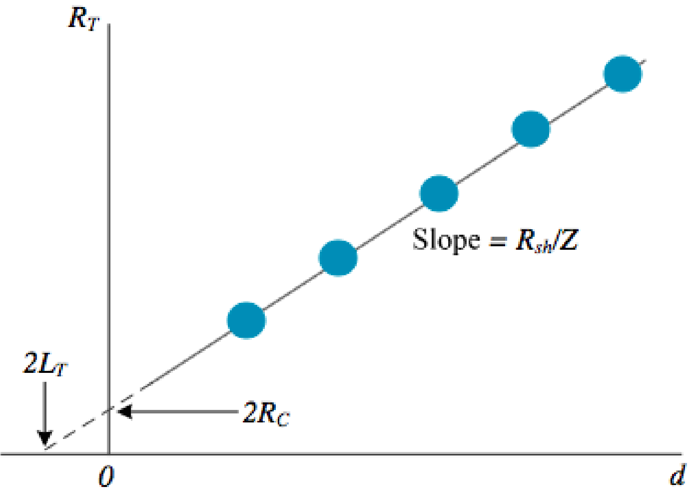


Figure 6.10: TLM plot of the total resistance as a function of contact spacing

Using this plot the sheet resistance could be extracted from the slope, and the contact resistance is the intercept at d=0, and specific contact resistance could be calculated from extrapolating the plot to $R_T = 0$ [2].

Since the sheet resistance underneath a contact is different from elsewhere, the front contact resistance (R_{cf}) and the total resistance could be calculated by [4]

$$R_{cf} = \frac{\rho_C}{L_{TK}Z}\coth(\frac{L}{L_{Tk}}) \qquad \text{Equation 6.3}$$

$$R_T = \frac{R_{sh}d}{Z} + 2R_C \approx \frac{R_{sh}}{Z}[d + 2\left(\frac{R_{sk}}{R_{sh}}\right)L_{Tk}] \qquad \text{Equation 6.4}$$

where R_{sk} is the sheer resistance underneath the contact. The transfer length is given by

$$L_{Tk} = (\rho_C/R_{sk})^{0.5} \qquad \text{Equation 6.5}$$

The value of the R_{sk} is obtained from the end resistance measurement[2]. A current is passed between two contacts and the voltage is measured between one of these contacts and another contact outside the current loop. The end resistance is then calculated by R_{ce} =V/I and L_{Tk} and thus ρ_C could be calculated after knowing the end resistance using the following equation

$$R_{ce} = (\frac{\rho_C}{ZL_{Tk}\sinh\left(\frac{L}{L_{Tk}}\right)}) \qquad \text{Equation 6.6}$$

Sheet, contact resistance can then be extracted from the total resistance versus distance plot as explained above.

6.3.2 Van der Pauw method

Van der Pauw (VDP) structure could be used to measure the sheet resistance of the semiconductor. the schematic of the test structure is shown in Figure 6.11.

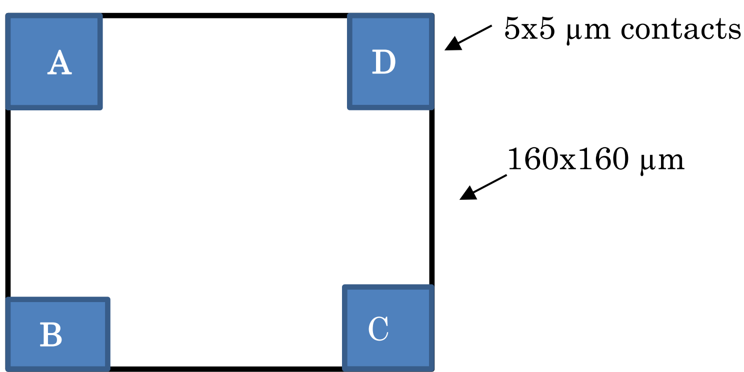


Figure 6.11: The schematic diagram of the VPD test devices

The very small ohmic contacts are located at the corners of the VDP structure which has equal width and length (160x160 µm). A current is passed through the contacts A,B ($I_{A,B}$), while the voltage across the opposite contacts C,D ($V_{C,D}$) is measured. The resistance is then given by

$$R_{AB,CD} = \frac{V_{C,D}}{I_{A,B}} \qquad \text{Equation 6.7}$$

This is called the vertical resistance, the horizontal resistance is given by

$$R_{BC,AD} = \frac{V_{A,D}}{I_{B,C}} \qquad \text{Equation 6.8}$$

If we assume all the vertical and horizontal measurements are equal then we can define the average horizontal and vertical resistances to be

$$R_{horizontal} = \frac{R_{BC,AD} + R_{AD,BC} + R_{DA,CB} + R_{CB,DA}}{2} \qquad \text{Equation 6.9}$$

$$R_{vertical} = \frac{R_{AB,CD} + R_{CD,AB} + R_{BA,DC} + R_{DC,BA}}{2} \qquad \text{Equation 6.10}$$

The sheet resistance R_S is related to horizontal and vertical resistances through the van der Pauw equation

$$\exp\left(-\frac{\pi R_{horizontal}}{R_S}\right) + \exp\left(-\frac{\pi R_{vertical}}{R_S}\right) = 1 \quad \text{Equation 6.11}$$

6.4 Accurate measurement of the channel mobility

Drift resistivity at the voltages close to 1000V is very high compared to the channel resistivity, hence to accurately measure the channel mobility, drift resistivity should be excluded in the calculation of mobility.

In this project, the mobility calculation was based on the total resistivity as the structures of the MOSFETs were kept the same and therefor the drift resistivity was constant. Hence the changes in mobility was concluded to be due to change in the channel resistance. It is recommended to accurately measure the mobility of the channel in future works. This section describes the calculation for such measurements.

Since V_{DS} is very small during mobility measurement, the drain current can be re-written as [5] [6]

$$I_D = \frac{W}{L}\mu_{FE}C_{OX}(V_{GS} - V_{Th})(V_{DS} - I_D R_d) \quad \text{Equation 6.12}$$

Hence gate conductance is given by

$$g_m = \frac{\partial I_D}{\partial V_{GS}}|_{V_{DS}} = \frac{W}{L}\mu_{FE}C_{OX}V_{DS}(1 + \frac{R_d}{R_{ch}}) \quad \text{Equation 6.13}$$

Where I_D is the drain current and R_d the total resistance between the source and the drain excluding the channel resistance (R_{ch}). Equation 6.13 could be used to calculate the channel mobility excluding the resistances other than channel resistance.

R_d and R_{ch} could be calculated by the following equation as previously described by Equation 5.7 and 5.8

$$R_{ch} = R_{DSON} - R_d = \frac{LW}{2\mu_{FE} C_{ox}(V_G - V_{TH})} \qquad \text{Equation 6.14}$$

Where L is the channel length and W is the channel width. The drain to source resistance R_{DSON}, could be measured from the I-V characteristic as described in Chapter 5.

6.5 Reference

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