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Investigation of buffer charging effects in GaN-based transistors

Investigation of buffer charging effects in GaN-based transistors

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Abstract

GaN based transistors are investigated in this work. GaN devices have already been introduced for commercial applications for RF and power markets. Due to excellent performance achieved with GaN devices, predictions for even greater commercial success have been made. Some major reliability issues though still exist which prevent the devices from showing their full potential. One such issue is the current collapse phenomena which can be related to buffer charging effects. Those buffer charging effects are investigated in this work.

The impact of carbon doping in the buffer on current collapse is tested for devices grown on Si substrate. The results are interpreted with the help of simulations. A clear relation between doping and current collapse is seen.

Different current collapse behaviour is observed on otherwise similar samples. To get better insight characterisation techniques involving illumination are developed and effects otherwise not accessible are detected. The observations have implications for devices operating under light.

Devices grown on SiC substrates are also tested. Strong impact of ohmic contacts on leakage is observed. Different doping profiles including carbon and iron are tested. Based on the findings new structures are proposed and simulated which have the potential to prevent detrimental effects.

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Finally I want to thank my wife Stephanie for her support and patience during my studies.

I declare that the work in this dissertation was carried out in accordance with the requirements of the University's *Regulations and Code of Practice for Research Degree Programmes* and that it has not been submitted for any other academic award. Except where indicated by specific reference in the text, the work is the candidate's own work. Work done in collaboration with, or with the assistance of, others, is indicated as such. Any views expressed in the dissertation are those of the author.

Alexander Pooth
Essen, 4th January 2018

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Chapter 1

Introduction

Gallium nitride (GaN) is a compound of gallium and nitrogen. It has first been produced as a single crystal in the laboratory in 1969 [1]. Since then GaN and other III-nitrides, such as AlN, have attracted increasing interest in science and industry due to their remarkable characteristics. The III-nitrides have a direct band gap and including their alloys they span a band gap energy range from ultra violet to infrared covering the full visible spectrum. Hence, unsurprisingly optoelectronic applications involving GaN material have been a focus of interest leading to the development of violet, blue and white light emitting diodes (LED), which have now replaced most other commercial light sources, and blue laser diodes used in bluray disc players and recorders [2, 3]. In the shadow of the very energy efficient and successful LED, GaN-based transistors have emerged as another application with previously unseen performance and potential for various commercial applications [4].

GaN heterostructure field effect transistors (HFET) have first been demonstrated in the year 1993 in [5]. The spontaneous polarisation of the III-nitrides can cause the formation of high density two dimensional electron gases (2DEG) at interfaces in a III-nitride heterostructure without the need of additional doping. Those 2DEGs are used as channel in HFETs and enable values for power density in combination with high frequencies not achievable by other technologies.

15 years ago first commercial GaN transistors became available and excellent market predictions in areas like broadband wireless, (hybrid) electric vehi-

cles, electric grid converters and compact, rugged radar were made. Today GaN transistor technology is heavily used in commercial products of the large RF and power markets. Application examples are mobile base stations and DC/DC converters [6, 7]. GaN RF devices usually grown on SiC have matured over the past decade and are widely used for several applications. The GaN power device usually grown on Si in contrast faces tough competition in other technology and has to fulfil high expectations for reliability which often are challenging to achieve. The investigations of this work have implications for devices aimed at both, RF and power market.

Market predictions are still showing huge growth potential for the coming years, in particular for the power segment [7]. Global players such as Cree (Wolfspeed), Infineon (International Rectifier) and Panasonic are offering GaN transistor products or are in advanced development of such products. Also several new companies specialised on GaN related technology have been founded, e. g. GaN Systems, Transphorm, EpiGaN.

Despite the commercial adoption GaN device production still poses big challenges. The material is far more defective than other commercial semiconductors resulting in issues with uniformity and reliability which reduce performance and price competitiveness. For commercialisation in the RF sector most issues have been overcome and the devices have shown excellent reliability. For the power segment though there still is a lack of market confidence in reliability. Ultimately GaN devices are predicted to overtake Si in the 600 V segment, but it will not be a part-for-part replacement. To take advantage of the higher speed new packaging and circuit level solutions need to be developed in parallel. Another major problem is the current collapse phenomena which can be linked to either surface effects that can be mitigated [8] or buffer effects which are investigated here.

The work presented here has been done in a collaboration between epitaxy foundry IQE in Cardiff and the University of Bristol (UoB). An Innovate UK knowledge transfer partnership (KTP) with support by the Welsh government was established between IQE and UoB. The main objective of this partnership was to share and extend knowledge between the partners to the benefit of all stakeholders. A KTP associate position was created which represents the core of the program responsible for keeping the link and performing the scientific and en-

gineering work which took place at both locations. Holding the position as the KTP associate the author's main work location was at IQE where the epitaxial growth was performed and developed in a small team. Also some characterisation of the material was performed at IQE. At UoB the device testing was the main activity. Simulations were run on UoB hardware via remote access. The KTP was enhanced by an international collaboration with Chalmers University, Sweden. Cardiff University was also involved in parts of the work presented.

The experiments described in this work were performed by the author if not mentioned otherwise. Data analysis was also done by the author. Simulation programs and programs for control of newly developed experiments were amended and extended by the author based on programs available in the CDTR-group at the University of Bristol.

Different epitaxial structures are designed, grown and tested to understand how they are linked to charging effects and current collapse. During those testing it was found that the processing of the devices can also impact the behaviour in the buffer region. Different approaches were compared in regard to device performance. Understanding of the underlying physics was the main objective rather than a pure empirical approach. Electrical and optical characterisation techniques were used, developed and improved to gain those insights together with simulations of the structure which help to visualise the electric fields and position of charges within the structures.

Chapter 2 contains the theory of the semiconductor material, the device details and physics, how they are produced and introduces some reliability issues. The unique characteristics of the III-nitrides are described, how they can be used to build transistors showing excellent performance and what challenges still remain.

In chapter 3 characterisation techniques are introduced which have been used during the studies.

The first experimental chapter, chapter 4, is concerned with the role of carbon in a typical GaN HFET structure. Current collapse behaviour is observed and linked to carbon doping of the buffer with the help of simulations. The material is grown on silicon substrates and contains a graded strain relief layer.

In chapter 5 a sample is introduced which does not show signs of current collapse and is compared to the sample investigated in chapter 4. Understanding of

the differences and their origins is this chapter's main objective. A novel characterisation approach that combines substrate bias and the illumination of the sample surface is used to investigate charge trapping effects that take place in those samples.

Devices grown on SiC substrates are introduced in chapter 6. These were produced at Chalmers University. The impact that different ohmic processes have on device performance in regard to current collapse is investigated. Different doping configurations are also compared. Based on the findings a structure is proposed and tested in simulations that has the potential to suppress current collapse.

Conclusion and outlook are given in chapter 7.

Chapter 2

Theory

In this chapter a theoretical background is given on the materials, namely the Group-III-nitrides. Their characteristics and specific properties, which make them attractive for transistor devices, are described. These transistor devices are then introduced and how material and devices are processed is discussed. Major reliability issues are also explained.

2.1 Group-III-Nitrides

Compound semiconductors consisting of one or several group III metals and nitrogen are called Group-III-Nitrides. They have attracted great interest because of the direct band gap that enables optical emission in a broad spectral range from infrared to ultra violet on the one hand and on the other hand the possibility to form a two dimensional charge carrier gas at interfaces because of abrupt changes in polarisation. In those two dimensional charge carrier gases very high charge carrier concentrations and mobilities are achieved. Together with the wide band gap compared to other semiconductors like silicon this renders the Group-III-Nitrides a preferred material choice for transistor devices with high power at high frequencies.

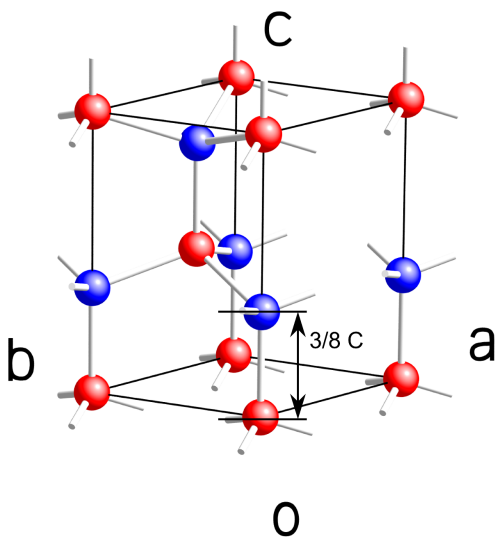

Figure 2.1: Crystal Structure of the Group-III-Nitrides. Metal atoms are depicted in red, nitrogen atoms in blue.

2.1.1 Crystal Structure

Group-III-nitrides commonly crystallise in the wurtzite structure. Group III and nitrogen atoms each are hexagonal close-packed with a shift along the c-axis between them of 3/8 of the c-constant as shown in figure 2.1. The ratio of group III to nitrogen atoms is 1:1. With Ga and Al as group III material binary and ternary compounds described by $Al_xGa_{1-x}N$ are possible. Indium compounds are also possible enabling a larger parameter window. In this work the focus is on ternary AlGaN and binary GaN though. The wurtzite structure seen in figure 2.1 has neither inversion nor axis symmetry. The positive c-axis is defined as the [0001]-direction in which the bonds point from metal towards nitrogen atom. Growth in positive c-direction is called Ga-polar. Growth in opposite direction is called

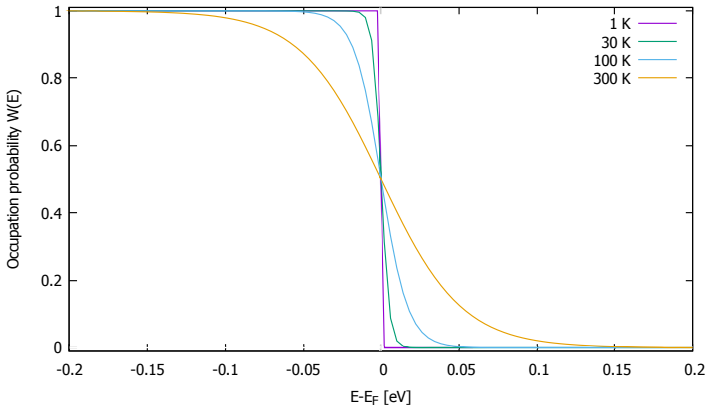

Figure 2.2: Fermi-Dirac distribution.

nitrogen polar or N-polar. The lattice constant of AlGaN depends linearly on the lattice constants of the binary compounds and is calculated by Vegard's law [9]

$$a_{Al_xGa_{1-x}N} = x \cdot a_{AlN} + (1 - x) \cdot a_{GaN} \tag{2.1}$$

with a lattice constant of 0.3112 nm for AlN and 0.3189 nm for GaN.

2.1.2 Band Structure and Doping

The discrete energy levels of electrons in a single atom smear out to energy bands within the periodic potential inside a crystalline solid. Between those energy bands gaps exist without possible energies for electrons. The occupation of energy levels follows the Fermi-Dirac distribution: $f(E,T) = \frac{1}{\exp{(E-\mu)/kT+1}}$ [10]. Where E, T are energy and temperature and μ is the chemical potential. At 0 K the Fermi-Dirac distribution is a step function. With increasing temperatures the gradient of the step lowers, see figure 2.2, the centre of symmetry at which the occupation probability for electrons is $\frac{1}{2}$ defines the Fermi level. The position of the Fermi level defines whether a material is a conductor, Fermi level inside an energy band, or an insulator or semiconductor, with Fermi level lying outside the energy bands. The energy between the band above and below the Fermi level is the band gap. Classic semiconductors like silicon or germanium have relatively small band gaps (1.1, 0.7 eV at RT) [10]. The Fermi level gives the energy at which

energies below are mostly occupied and above remain mostly unoccupied. With increasing temperatures the conductivity of an intrinsic semiconductor rises since more charge carriers of both types become available due to the characteristics of the Fermi-Dirac distribution. Maximum charge carrier densities for intrinsic semiconductors of the order of $10^{12}\,\mathrm{cm}^{-3}$ at room temperature are achievable in germanium. By doping though it is possible to greatly exceed the intrinsic charge carrier density by creating either additional electrons in the conduction band above Fermi level or holes in the valence band below the Fermi level. The semiconductor becomes n- or p-type, i.e. conductive with either electrons or holes being the majority charge carrier. The physics of n and p semiconductors, in particular space charges accruing at interfaces of n and p regions, form the basis for most semiconductor devices. Doping is usually done by adding impurities to the material which act as donor or acceptor. A donor's electron configuration is such that an electron can be lifted into the conduction band easily. The donator is ionised and an additional free electron has been donated. An acceptor is easily ionised by an additional electron from the valence band creating an additional free hole in the valence band. Doping moves the Fermi level closer to the band edge. Ideally dopant's energy levels are close to the band edge since the distance defines the energy needed to ionise the dopant and release the additional charge. Most materials with band gaps of 2 eV and more do not have effective dopants and therefore show insulating characteristics. GaN and other III-nitrides need quite high doping concentrations to achieve sufficient concentrations of charge carriers for p-type conductivity. Figure 2.3 shows ionisation energies of common dopants in GaN. Magnesium has the lowest p-type ionisation energy of about 170 meV [11]. That makes it the preferred p-type dopant, since no lower ionisation energy acceptor exists. In addition to the relatively high ionisation energy only a small number of the magnesium atoms can be activated to act as dopants due to self compensating effects [12] in GaN. The number of impurities therefore exceeds the number of holes created leading to very high concentrations of Mg necessary for effective p-type doping. N-type doping is less problematic with the preferred dopant being Si which has an ionisation energy of only 20 meV. Due to inevitable incorporation of some impurities (see section 2.1.5) GaN and other nitride compounds often have a n-type background doping. To compensate the n-type background and to bring

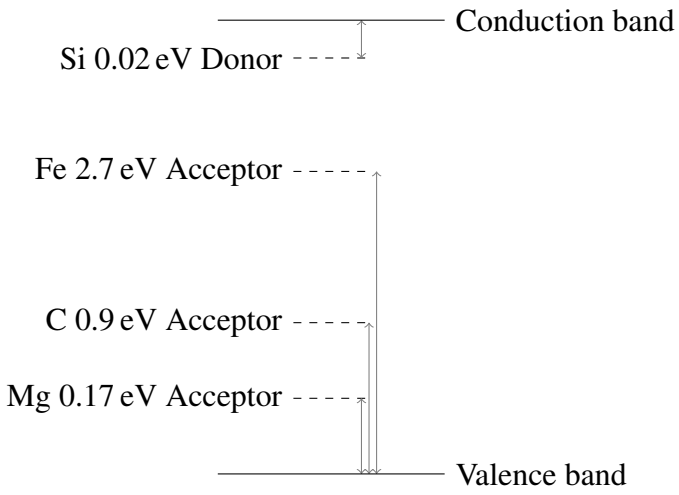

Figure 2.3: GaN band diagram with energy levels of common dopants.

the fermi level closer to a midgap position deep acceptors such as Fe and C are used.

A large number of dopants introduces scattering effects and reduces the performance of transistors build from those materials. Due to their unique polarisation characteristics III-nitrides can be doped in a way that circumvents these issues and that is not possible in any other commercial semiconductor technology to date. Abrupt changes of polarisation at hetero interfaces or gradual variation of composition allow to build charges without the need of any potentially detrimental dopant. The polarisation of the III-nitrides is described in detail in the next section 2.1.3.

2.1.3 Polarisation

In wurtzite III-nitrides the probability function for electrons is higher in the vicinity of the nitrogen atom due to partially ionic nature of the bond and since the electronegativity is significantly higher for the metals than for nitrogen. An electrical dipole therefore forms along the metal-nitrogen-bond. In an ideal wurtzite structure those dipoles compensate each other [13]. When the ratio between a and c lattice constant differs from that in the ideal structure, which it does in III-nitrides, a dipole remains along the c axis. Spontaneous polarisation is the result. Spon-

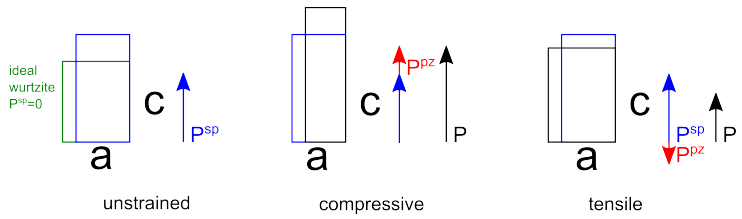

Figure 2.4: Sketches illustrating how strain changes the a to c lattice constant relation and the effect on polarisation.

taneous polarisation depends only on the composition and is present in strained and unstrained material. In bulk material the dipoles compensate each other but at interfaces and surfaces sudden changes in polarisation can create significant charges. The spontaneous polarization P_{sp} of ternary AlGaN is nonlinearly dependent on both binary P_{sp}. Vegard's law therefore needs to be extended by an additional term with bowing parameter b leading to the following equation [14]:

$$P^{sp}_{Al_xGa_{1-x}N} = x \cdot P^{sp}_{AlN} + (1-x) \cdot P^{sp}_{GaN} - b_{AlGaN} \cdot x \cdot (1-x)\,. \tag{2.2}$$

Strain within the crystal can also change the ratio between a and c lattice constant. The total polarisation can be increased or reduced by this so called piezoelectric effect. Hetero structures of III-nitrides are commonly grown pseudomorphic along the positive c axis. The growth plane dictates the a lattice constant $a_{substrate}$, which is different to a_{free} of free-standing material, leading to isotropic tensile or compressive strain, see figure 2.4. The strain causes a deformation along c direction. This results in the change in total polarisation and is defined by:

$$\epsilon_c = -2\frac{c_{13}}{c_{33}} \cdot \epsilon_a\,.$$

With $\epsilon_a = \frac{a_{substrate} - a_{free}}{a_{free}}$ being the relative deformation in the growth plane and c_{13}, c_{33} are components of the Young's elastic modulus tensor of the material. Tensile strain of the a lattice constant therefore leads to compressive deformation in c direction and vice versa. Hence, the piezoelectric polarisation is given by:

$$P^{pz} = e_{33}\epsilon_c + 2e_{31}\epsilon_a\,. \tag{2.3}$$

Bernadini and Fiorentini though showed in [15] that the linear eq. 2.3 differs from the actual values and that an additional square dependency gives a better description. For binary compounds the value of P^{pz} therefore calculates as [16]:

$$\begin{aligned} P^{pz}_{AlN} &= -1.808\frac{C}{m^2}\cdot\epsilon_a + 5.624\frac{C}{m^2}\cdot{\epsilon_a}^2 \quad \text{for} \quad \epsilon_a < 0\,, \\ P^{pz}_{AlN} &= -1.808\frac{C}{m^2}\cdot\epsilon_a - 7.888\frac{C}{m^2}\cdot{\epsilon_a}^2 \quad \text{for} \quad \epsilon_a > 0\,, \\ P^{pz}_{GaN} &= -0.918\frac{C}{m^2}\cdot\epsilon_a + 9.541\frac{C}{m^2}\cdot{\epsilon_a}^2\,. \end{aligned} \tag{2.4}$$

The piezoelectric polarisation of AlGaN has linear dependency on the binary composition and can be derived analogous to the lattice constants using the results of eq. 2.4 and Vegard's law (eq. 2.1 with $a \rightarrow P^{pz}$).

The total polarisation is the sum of spontaneous and piezoelectric polarisation $\vec{P} = \vec{P}^{sp} + \vec{P}^{pz}$.

2.1.4 Two Dimensional Electron Gas

In free standing homogeneous III-nitrides no internal fields build up due to surface charges which fully compensate the polarisation charge. For hetero structures with different polarisations though full compensation is no longer possible resulting in polarisation charges at interfaces. At those interfaces conditions can be met that allow the build up of free charges in close vicinity. Two dimensional electron and hole gases (2DEG, 2DHG) can appear in which sheet carrier densities of up to $5\times10^{13}\,\text{cm}^{-2}$ are possible [17]. In addition to that mobilities of 2000 $\frac{\text{cm}^2}{\text{Vs}}$ and more can be achieved in those 2DEGs [18] making them attractive for use as a channel in a transistor structure. In figure 2.5 a schematic band diagram of an AlGaN/GaN interface with 2DEG is depicted with characteristic energies and charges of the structure. $a_{1,2}$ are the AlGaN (1) and GaN (2) layer thicknesses, σ_{S1} and σ_{S2} are the surface charges, σ_n is the 2DEG charge and the σ_P repre-

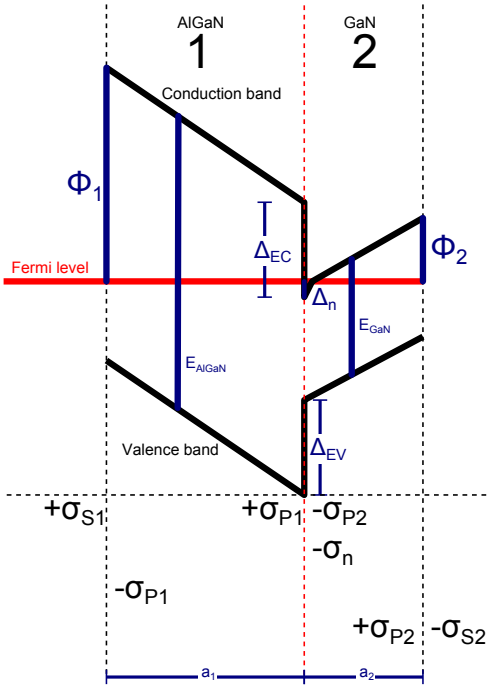

Figure 2.5: Band diagram of a AlGaN/GaN interface with 2DEG (Ga-faced growth from right to left).

sent polarisation induced charges. Application of Gauss' law for the surfaces and interface in image 2.5 leads to the following equations:

$$\varepsilon_b E_1 = \sigma_{S1} - \sigma_{P1} \tag{2.5}$$

$$\varepsilon_g E_2 - \varepsilon_b E_1 = \sigma_{P1} - \sigma_{P2} - \sigma_n \tag{2.6}$$

$$-\varepsilon_g E_2 = \sigma_{P2} - \sigma_{S2}\,. \tag{2.7}$$

$E_{1,2}$ are the electric fields in region 1 and 2. $\varepsilon_{g,b}$ are the dielectric constants of GaN and the AlGaN in the barrier. No external fields were assumed. Charge neutrality requires $\sigma_n = \sigma_{S1} - \sigma_{S2}$. For the energies along the conduction band in figure 2.5 the following equations can be deduced:

$$\phi_2 - a_2 E_2 = 0 \tag{2.8}$$

$$\phi_1 + a_1 E_1 - \Delta E_C + \Delta_n = 0\,. \tag{2.9}$$

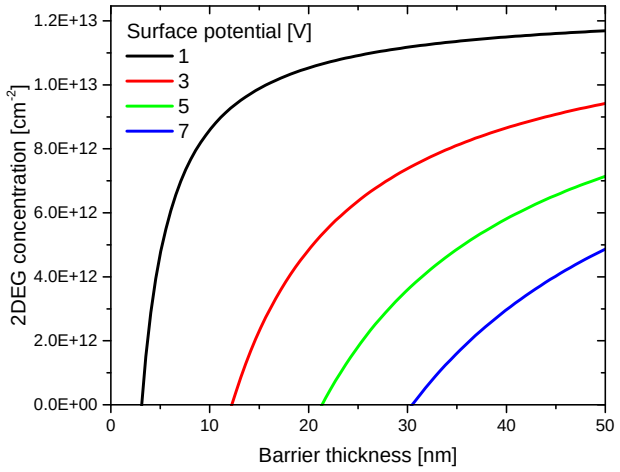

Figure 2.6: Calculated 2DEG charge concentration of a AlGaN/GaN structure plotted over AlGaN-barrier thickness for different surface potentials.

With $\phi_{1,2}$ representing the surface potentials and ΔE_C being the conduction band offset. Δ_n is the energy depth of the 2DEG potential. Under the simplifying worst case assumption that only the lowest subband in the 2DEG potential is occupied [19], σ_n is proportional to the 2DEG charge's density of states N_s:

$$\Delta_n = \sigma_n \underbrace{\frac{1}{q^2 N_s}}_{\gamma} . \tag{2.10}$$

Using equations 2.6, 2.8, 2.10 and the relation $\mathrm{C} = \frac{\epsilon}{\mathrm{a}}$ between capacity and thickness of the layer equation 2.9 can be transformed to:

$$\sigma_n = \frac{\sigma_{P1} - \sigma_{P2} - \mathrm{C}_2\phi_2 - \mathrm{C}_1\phi_1 + \mathrm{C}_1\Delta E_C}{1 + \mathrm{C}_1\gamma} . \tag{2.11}$$

The polarisation difference at the interface $\sigma_{P1} - \sigma_{P2}$ induces the 2DEG charge σ_n, which is altered by the potentials ϕ and also depends on the thicknesses of the layers. In figure 2.6 the dependencies described by equation 2.11 are depicted for a GaN thickness of 3 µm and a potential ϕ_2 of 1 V. It can be seen from the plot that at a surface potential of 1 V, which is a realistic value [20], a minimum

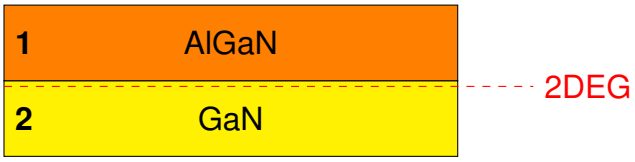

Figure 2.7: Layer stack of a AlGaN/GaN interface with two dimensional electron gas.

thickness for the barrier of $\sim$3 nm is needed for a 2DEG to form and that the charge increases quickly with barrier thickness to then slowly saturate. The 2DEG decreases when the potential ϕ_1 is increased. This behaviour is in good agreement with observations on real structures although no doping has been considered in the model and the band structure in particular close to the 2DEG is strongly simplified. To get more accurate representations of the band diagram simulations like those described in section 3.4 are used. Figure 2.7 shows the position of the 2DEG within the layer stack.

2.1.5 Defects and Trapping Mechanisms

Although no intentional doping is needed for the formation of a 2DEG there can be defects and impurities in the material that are unintentionally created during growth. Point, line, planar and 3D defects are possible. Table 2.1 lists the different types of defects. Additional energy levels within the band gap are often associated with point defects. A point defect can either be a vacancy where an atom is missing on its lattice site or an impurity where a foreign atom replaces an atom on its position. Interstitial positions are also possible, i.e. an atom has moved to an off lattice position. The number of defects and impurities in III-nitride material is rel-

Table 2.1: Defects in Semiconductors

Point defect	Line defect	Planar defect	Bulk defect
vacancies interstitials impurities antisites combinations of these	edge- screw- dislocations	stacking faults grain boundaries	pores cracks inclusions precipitates

atively high when compared to other semiconductors. In commonly used growth techniques the dislocation density is around 1×10^9 cm^{-2}. The 2DEG mobility in a real structure can be reduced by those defects due to scattering effects [21]. Also additional localised energy levels can appear changing the electrical properties of certain regions. Acceptor- and donor-like electrical behaviour is possible. Besides polarity, energy depth and concentration the capture cross section σ of a trap is an important parameter that defines the recombination rate for minority charge carriers. The minority carrier lifetime is defined as: $\tau = \frac{1}{\sigma v_{th} N_t}$ with carrier thermal velocity v_{th} and trap density N_t [22]. Those energy levels can cause wanted or unwanted charges. The former would be dopants if incorporated intentionally. When the effects are not intended they are called traps. Traps often appear in greater numbers nearby defects of greater dimension. Threading dislocations and metal intrusions under contacts are often found to provide leakage path due to a high number of traps and associated charge carriers [23].

Table 2.2 shows the large amount of traps that have been observed in III-nitrides. Since most GaN material has a considerable number of impurities some background doping will be present. The intentional doping needs to at least compensate this background to have the desired effect. Also some dopants e.g. carbon can incorporate in different ways leading to significantly different trap levels, which can also have compensational effects on each other and often depend on growth conditions [66]. When there are two dopants of the same kind, either both acceptor or both donor, the dopant with lower ionisation energy pins the Fermi level and defines electrical properties. To move the Fermi level to the deeper doping level, i.e. higher ionisation energy, the lower energy dopant needs to be fully compensated by dopants of opposite polarity [67]. Figure 2.8 illustrates the position of the fermi level in case of two acceptor levels and a donor level for different concentration ratios. When trying to achieve the desired doping profile these effects must be taken into account.

Table 2.2: List of deep energy level defects published by Bisi et al. in [24] illustrating the large number of different defects and associated energy levels in III-nitride material.

Reference	Analysed samples	Deep level energy (eV)	Interpretation
[25–34]	Various GaN-based devices	EC - 0.09/0.27	Nitrogen vacancies
[34]	n-GaN	EC - 0.12	Surface
[35]	TMGa GaN	EC - 0.14	Carbon or hydrogen impurity
[36]	p-GaN	EC - 0.15	Mg ionisation
[37, 38]	AlGaN/GaN HFET	EC - 0.3/0.34	Possibly AlGaN surface
[39]	Fe doped GaN	EC - 0.34	Fe3+/2+
[25]	n-GaN	EC - 0.355	Mg impurity
[26]	Si doped GaN	EC - 0.37/0.4	Si dopant
[35, 40, 41]	Various GaN-based devices	EC - 0.44/0.49	C/O/H impurities
[28, 30, 32, 34, 42–46]	Various GaN-based devices	EC - 0.5/0.62	Nitrogen antisites
[47]	Fe doped GaN	EC - 0.5	Fe dopant
[48]	AlGaN/GaN HFET	EC - 0.57	Influenced by Fe dopant
[49]	n+p GaN diode	EC - 0.59	Si dopant
[50, 51]	Mg doped p-type GaN	EC - 0.6/0.62	Mg-H complex formation
[43]	AlGaN/GaN HFET	EC - 0.6/0.64	VGA + oxygen complex
[29]	n-type GaN	EC - 0.613	Nitrogen vacancy
[38]	AlGaN/GaN MIS-HEMT	EC - 0.68	Surface
[52]	Fe-doped AlGaN/GaN HFET	EC - 0.72	Fe dopant
[53]	GaN pn diode	EC - 0.76	Nitrogen interstitial
[47, 54]	Fe-doped or uid GaN	EV + 0.85/0.94	Gallium vacancy
[46]	n-type GaN on sapphire	EC - 0.89	Nitrogen interstitial
[53]	GaN pn diode	EC - 0.96	Ga vacancy or N interstitial
[55–57]	Various GaN-based devices	EC - 0.95/1.02	Threading dislocation
[43]	AlGaN/GaN HFET	EC - 1.118	VGa + oxygen complex
[32, 51, 58, 59]	Various GaN-based devices	EC - 1.28/1.35	Carbon interstitial
[60]	AlGaN/GaN on SiC HFET	EC - 2.3	Surface
[61]	c/m plane GaN	EC - 2.47/2.49	VGa + hydrogen complex
[62]	Fe doped GaN	EV + 2.5/3	Fe dopant
[32, 51, 58]	Various GaN-based devices	EC - 2.6/2.64	VGa, VGa-H or VGa-2H
[63]	AlGaN (Al 30 %)	EC - 3.11	Cation vacancy
[32, 51, 64]	Various GaN-based devices	EC - 3.2/3.22	Residual Mg acceptor
[32, 58, 60, 61, 65]	Various GaN-based devices	EC - 3.24/3.31	CN substitutional
[59, 60]	AlGaN/GaN HFET	EC - 3.7/3.76	Mg or C substitutional in AlGaN
[63]	AlGaN (Al 30 %)	EC -3.93	Mg impurity

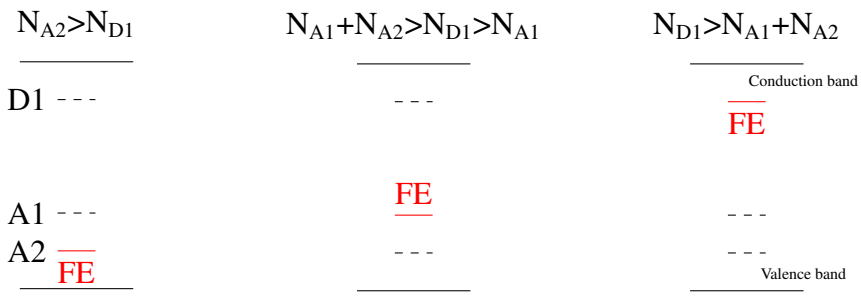

Figure 2.8: Position of the fermi level FE for different doping scenarios with acceptor levels A1 and A2 and a donor level D1. N_X is the concentration of dopant X.

2.2 Hetero Structure Field Effect Transistor

Transistor devices utilising the 2DEG at a hetero interface in a III-nitride structure as the channel are called hetero structure field effect transistors (HFET). A simple description of a GaN HFET is shown in figure 2.9. The 2DEG usually forms under a ternary AlGaN barrier layer in the underlying GaN layer when those were grown Ga-faced as discussed in section 2.1.4. Equation 2.11 which is illustrated in figure 2.6 describes how the 2DEG charge can be varied by changing the surface potential or the barrier thickness. For a certain barrier the 2DEG can be controlled by the surface potential for example by a schottky diode. The actual transistor device consists of two ohmic contacts forming source and drain and a schottky-type contact in between which is used as the gate to control the charge carrier concentration in the 2DEG underneath. Large enough bias on the gate creates a field that can completely deplete the 2DEG. The common GaN HFET is therefore a depletion mode device which is normally on. Typical barrier thicknesses that

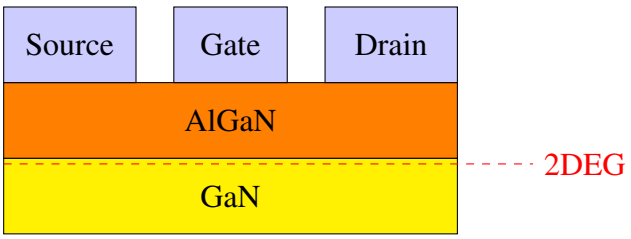

Figure 2.9: Sketch of AlGaN/GaN-HFET-structure

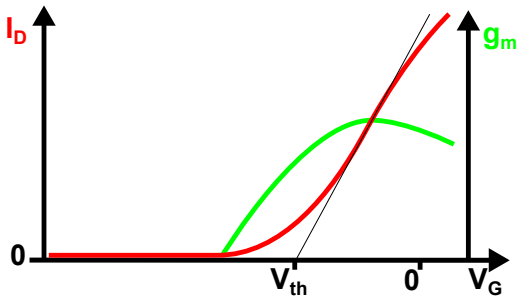

Figure 2.10: Transfer characteristics schematic of a depletion mode GaN HFET. The drain current I_D is plotted against the gate voltage V_G. g_m is the transconductance which is defined as the slope of the IV curve and V_{th} is the threshold voltage at which the transistor switches between on and off state.

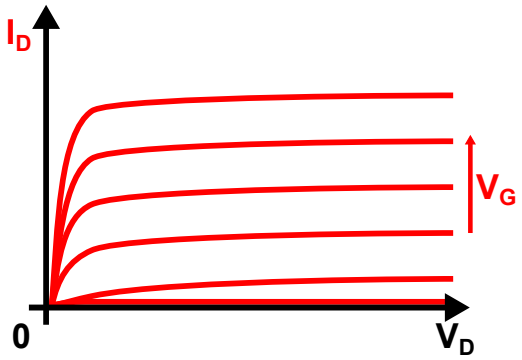

Figure 2.11: Output characteristics schematic of a depletion mode GaN HFET. The drain current I_D is plotted against the drain voltage V_G. Stepwise increasing of the gate voltage V_G leads to curves with larger drain current.

allow for large enough 2DEG concentrations at low enough threshold voltage and low leakage but decent ohmic contacts are at about 20-30 nm for Al concentrations of 20-30% in the AlGaN barrier which can be grown crack free on relaxed GaN layers. Transfer and output characteristics of the GaN HFET displayed in figures 2.10, 2.11 is similar to those of other field effect transistors with the exception that the gate threshold voltage v_{th} is below 0 V in the depletion mode device. The distance between ohmic contacts and gate are called access regions and their size is associated with an access resistance which also impacts the characteristics.

Fast switching under high voltages is where those devices outperform other technologies. Operation at output power densities of up to 40 W/mm at 4 GHz

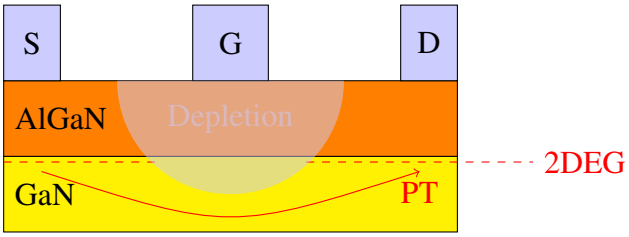

Figure 2.12: Punch Through (PT)

is not achievable with other technologies and frequencies of 100 GHz and beyond can be reached [68]. The combination of high voltage operation of several hundred volts with low on resistance is also possible enabling record efficiencies in power applications [7]. Commercial adoption in RF has started around 2005 with GaN devices replacing its GaAs counterparts in Radar applications. For the power market devices are available since 2011 replacing silicon based technology for DC/DC conversion [7].

2.2.1 Short Channel Effects

Devices are scaled down in size for price reduction with more devices per wafer area and for performance enhancement. In particular shorter gate lengths promise to be able to handle higher frequencies per dissipated heat/power. When gate length is reduced short channel effects begin to appear which can have detrimental effects on reliability and overall performance. In GaN HFETs punch through is an example for such a short channel effect. Charge carriers flow past the gate depletion region via deeper layers in an off state device, as can be seen in figure 2.12. The effect on the output characteristics is depicted in figure 2.13. It can be seen that when a certain drain voltage is exceeded the transistor no longer pinches off. To prevent punch through buffer layers are often intentionally doped with carbon or iron. Both dopants provide deep level acceptor traps that pin the Fermi level midgap and better confine the channel by preventing the 2DEG charges from penetrating into those layers, see figure 2.14.

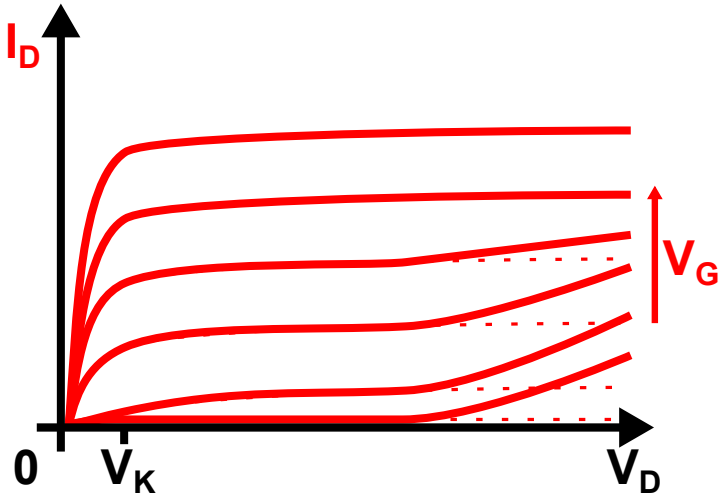

Figure 2.13: Output characteristic schematic for a transistor affected by punch through. V_K marks the knee voltage at which the currents start to saturate.

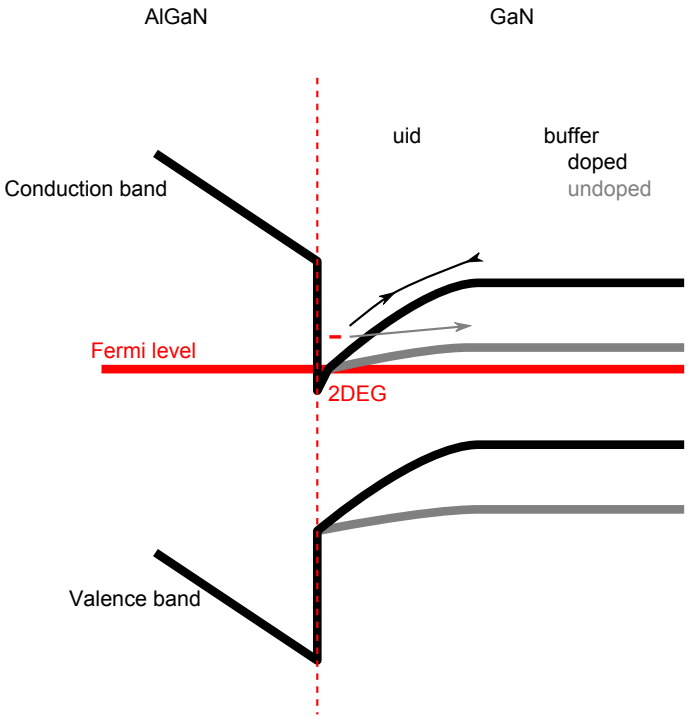

Figure 2.14: Band diagram showing the difference between doped and undoped GaN buffer. The confinement of electrons by adding a deep acceptor state to the buffer for punch through prevention is illustrated. The unintentionally doped GaN channel is labelled uid.

2.3 Production Methods

2.3.1 Epitaxial Growth

III-nitrides are usually grown by either molecular beam epitaxy (MBE) or metal organic chemical vapour-phase deposition (MOCVD) with MOCVD enabling faster growth and being the more cost effective method which is often preferred for commercial applications. Material discussed in this work is exclusively MOCVD grown.

In MOCVD growth metal organics are mixed with ammonia and controlled to flow over a heated up substrate where metal and nitride deposit in thin epitaxial layers [14, 69]. Nitrogen or hydrogen atmospheres are used. Flow rates and ratios of the metal organics and ammonia, the temperature and pressure form the parameter space. The metal organic precursors used are trimethylgallium $(Ch_3)_3Ga$ and trimethylaluminium $(Ch_3)_3Al$. The chemical reactions are of the form $(Ch_3)_3Ga + NH_3 = GaN + 3CH_4$. Ammonia to metal organics ratio is usually high at $\sim$1000, GaN growth temperatures are slightly above 1000 °C and typical pressures are around 100 mbar. The reactor used is a closed coupled showerhead reactor in which the gases flow downwards onto the substrates through the many small holes of the showerhead. Figure 2.15 shows such a showerhead. Metal organics and ammonia have separate inlets and only mix just above the susceptor which holds the substrates. The gas flows to the sides of the susceptor which is rotating to improve uniformity of conditions. Other reactor types exist which differ in size and handle the gas flow differently.

Due to the lack of native substrates of decent size and crystal quality at affordable costs other materials are used as substrates leading to strain induced by lattice mismatch. Table 2.3 shows the lattice mismatch of some substrates. The substrates used are sapphire, silicon carbide (SiC) and silicon. All three have advantages and disadvantages and are used in different commercial applications [14]. Sapphire is cheap, but has a low heat conductivity which is bad for transistor applications. Commercially it is mainly used in LEDs. SiC has the best lattice match with GaN and very good heat transport. SiC though is the most expensive foreign substrate. SiC is used for commercial RF devices in the high frequency at mod-

Figure 2.15: Showerhead of a MOCVD reactor [Aixtron SE]. At the bottom the susceptor with loaded wafers can be seen.

erate power regime. Silicon is much cheaper than SiC and also offers good heat transport. Potential integration into large scale Si processes and the availability of high quality, large diameter Si substrates promise a reduction in cost that will enable GaN power devices with superior performance at lower costs compared to their silicon counterparts.

Growth on all substrates usually starts with a low temperature AlN nucleation layer that promotes 2D growth, reduces dislocation density and in case of Si also prevents meltback etching of a GaSi alloy into the Si substrate. GaN on Si devices for operation in the high voltage regime >600 V need to have a total epitaxial thickness of 3 µm or more which leads to the formation of fatal cracks unless strain relief strategies are incorporated. Lattice and thermal expansion mismatch between the favoured Si substrate and the nitride deposit need to be controlled. Strain engineering and control of bow and warp during growth and during heating and cooling phases therefore is an important factor, increasingly so when substrate

Table 2.3: Structural and thermal mismatch of GaN and substrates [70, 71]

	GaN	silicon	silicon carbide	sapphire
lattice mismatch		17%	3.1%	14%
thermal expansion coefficient α_a averaged over 300-900 K	5.59	3.77	4.2	7.5
thermal conductivity [W/cmK]	1.3	1.3	3.7	0.23

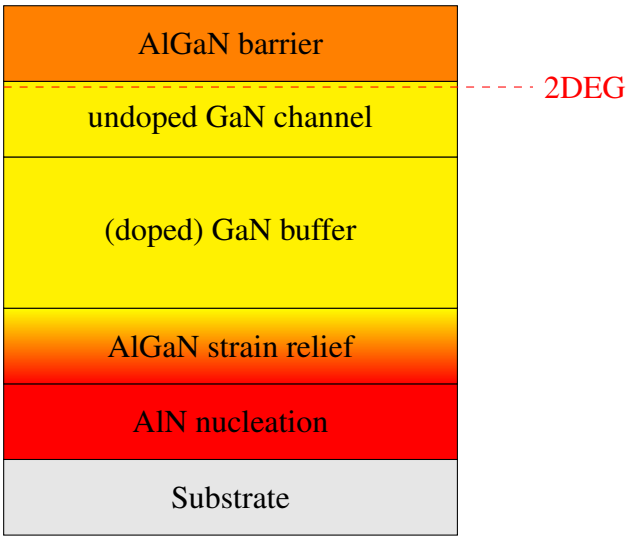

Figure 2.16: Typical epitaxial structure of a GaN HFET.

diameters are becoming larger. To achieve the desired thick epitaxy Al containing layers are added to the structures either in form of potentially graded AlGaN layers or several AlN interlayers [72]. A typical GaN on Si HFET structure consist of a nucleation layer followed by a strain relief section and a GaN buffer, on top of which the actual hetero structure is grown. An example for the described layer stack with a graded AlGaN strain relief section is shown in figure 2.16. Potential doping of the buffer section is mentioned in the figure. Additional metal organics or other gases are used to grow doped material, e.g. ferrocene $(C_5H_5)_2Fe$ or CP_2Fe for Fe doping and silane SiH_4 for Si doping. Carbon can also be incorporated without an additional gas source. The carbon concentration then depends strongly on growth conditions, in particular gas flow and temperature, and is adjusted by

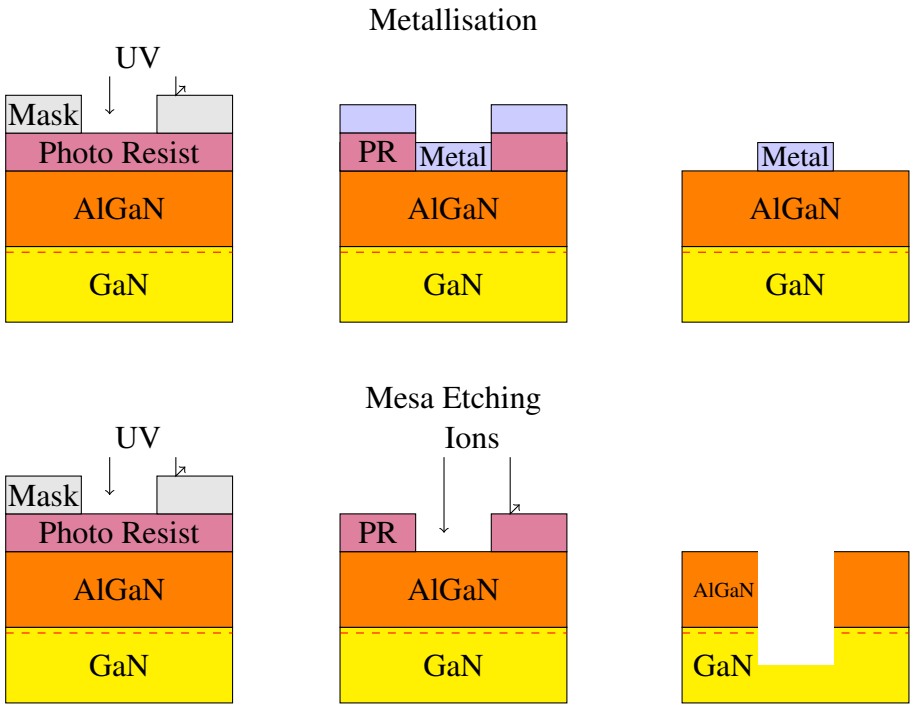

Figure 2.17: Schematic examples of device processing.

changing those. When other dopants are intentionally added carbon levels have to be carefully controlled to prevent compensational effects.

2.3.2 Device Processing

To build transistors on epitaxial material several processing steps are necessary each including lithography in which patterns of photo resists are formed [73]. Masks are used to expose the deposited photo resist with UV light and then partially lift off the deposit. Devices are isolated from each other by etching or ion implant isolation. Schottky gate and ohmic Drain/Source metal is evaporated and deposited in a vacuum chamber. Typically ohmic metal consists of 4 metals in a Ti/Al/x/Au configuration with different metals used for x [74–76]. Those stacks are usually annealed in a nitrogen atmosphere at ∼750-900 °C. Alternative ohmic metal stacks have recently been developed [77]. A Ta based metallisation is described and compared in the experimental part of this thesis. Unannealed Ni/Au

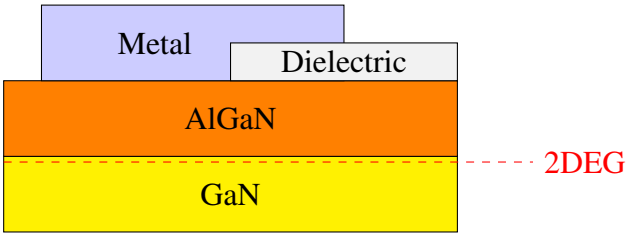

Figure 2.18: Field plate metal contact with dielectric.

is commonly used as schottky metal. In figure 2.17 basic processing steps are described. Dielectrics like SiN are often used to passivate the structure or as a filler to form special contact shapes like field plates, see figure 2.18. The T-shape of the described field plate design helps to reduce the peak electric fields at the gate edge. Field plates at the drain edge are used for the same reason and other geometries like slanted, triangular shapes or multiple layer structures can further improve device performance [8, 78].

2.4 Reliability Issues

2.4.1 Current Collapse

A major reliability issue for GaN based HFETs is the current collapse (CC) phenomena also known as dynamic ON resistance. After application of gate and/or drain bias stress the current is reduced in the on state for a significant period of time resulting also in higher ON resistance. Figure 2.19 illustrates how the output characteristic of a GaN HFET changes due to current collapse. The reduction of IV area covered with CC visible in figure 2.19 shows that RF power of the operating transistor will be reduced compared to what the DC characteristics with moderate bias suggests [79].

The CC effect stems from negative charges affecting the 2DEG either in form of surface, barrier or buffer traps. Surface charging usually appears at the gate edge of the access region between gate and drain. The surface charge is altered in this region forming a virtual gate which reduces the 2DEG and increases device resistance. A passivation of the surface with a dielectric as described in section 2.3.2 can mitigated this effect [80]. Trapping of hot electrons in the Al-

GaN barrier is associated with high peak electric field near the gate drain edge and can be reduced by a field plate device design also described in section 2.3.2 [78]. The remaining current collapse effects which are often related to high drain voltages are linked to buffer charging effects which are investigated in this work. The strength of the current reduction and how it recovers can vary greatly and depends on many factors. The phenomenon causes performance reduction and instabilities in real device applications. It also often occurs only on parts of wafers resulting in yield reduction.

2.4.2 Electrical Breakdown

When an applied voltage exceeds the operating voltage enough to permanently damage the device and often destroy the device the electrical breakdown condition is reached [81]. Physically the material in a broken down device has been altered so that the device is effectively shorted. Ultimately the breakdown voltage defines the maximum operating voltage of a device. An increase of breakdown voltage therefore enables higher power operating regimes. Electrical breakdown can happen either lateral between contacts on top of the wafer or vertical when a grounded conducting substrate is used. Figure 2.20 shows example images of broken down structures.

With typical HFET for power switching device dimensions, i.e. source drain distance (>10 µm) is more than twice the total epitaxy thickness (3-5 µm) on a conducting substrate, and proper isolation of devices, preferably by ion implant that renders the surroundings highly resistive, it is usually the vertical breakdown that defines the overall breakdown capabilities. Major strategies to enhance the breakdown capabilities are to increase the overall epitaxial thickness, have more high Al content nitrides with larger band gap or to reduce the number of dislocations and potential leakage along those.

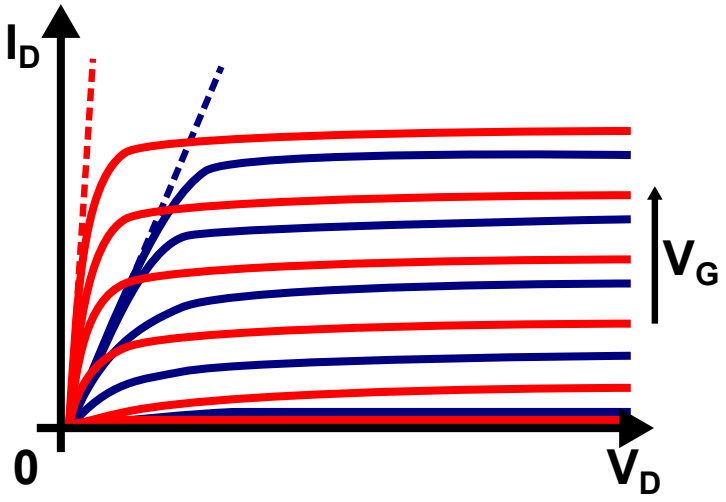

Figure 2.19: Schematic output characteristic of a GaN HFET not affected by current collapse (red) and suffering from current collapse (blue). The change in slope of the dashed lines indicates the change in On resistance.

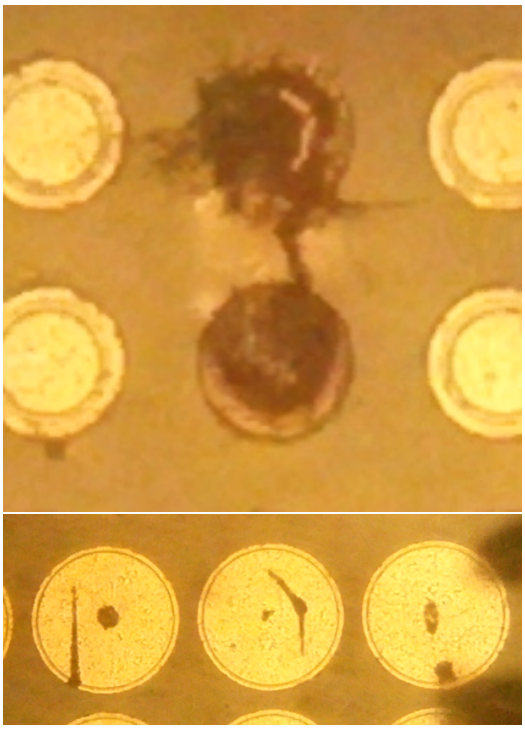

Figure 2.20: Breakdown test structures with visible marks along the surface and on the contact area only (indicating vertical breakdown).

Chapter 3

Characterisation Techniques

In this chapter techniques are introduced which are used to investigate the buffer charging and its relation to detrimental effects on transistor performance.

3.1 Pulsed IV

Pulsed IV measurements are commonly used to illustrate dynamic effects of transistor devices [82]. Equipment typically used for those measurements, like Accent's dynamic IV Analyser (DIVA) system, are able to perform pulsed output characteristics measurements. In those measurements the drain current is measured over a drain voltage range for a number of fixed gate voltages in continuous or DC mode as well as pulsed from defined quiescent points. DC mode measurements replicate the output characteristics described earlier (see figure 2.11). 0 V drain voltage and 0 V gate voltage quiescent point is often used as a reference and then compared to stress voltages on either drain or gate or both to show how the output characteristics change. Figure 3.1 shows an example of a pulsed IV curve.

Pulsed IV measurements can be used for current collapse measurements. The change in On resistance is immediately apparent from the output characteristics plot. The pulsed IV technique though is not well suited to illustrate the recovery process, because it only covers short time scales, or to differentiate between effects stemming from either surface/gate or buffer, since trapping in both regions can

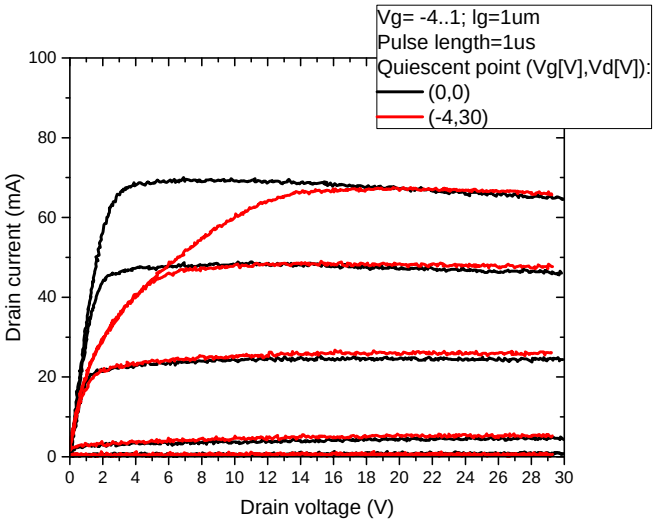

Figure 3.1: Pulsed IV measurement showing output characteristics of a transistor pulsed from 2 different quiescent points, namely 0 V bias on both gate and drain and off state drain stress with pinched off channel (gate bias: Vg = -4 V) and drain bias of 30 V. A current reduction in the knee region is observed, caused by a virtual gate effect [82].

lead to similar findings. To investigate buffer traps only and also monitor the recovery the substrate bias experiments can be used.

3.2 Ramped Substrate Bias

The ramped substrate bias measurement technique allows one to investigate buffer stemming current collapse (CC) effects only and focuses on build up and recovery of CC [83, 84]. To characterize current flow in the device structure back bias is utilised by applying a voltage to the conducting substrate. This affects the electrical fields in the epitaxial layer structure between 2DEG and substrate. These fields impact the carrier concentration in the 2DEG (n_S). Monitoring n_S, by measuring a current between two ohmic contacts, while applying the substrate bias reveals details about the electrical properties of the layers between the substrate and the 2DEG. The 2DEG measurement is not affected by gate effects nor other surface related influences that appear under certain stress voltages since the 2DEG sensing voltage can be chosen very moderate (<1 V) and the high e-field in the deeper structure is effectively screened by the 2DEG. The setup is depicted in Fig. 3.2. The equipment used for this work was a Keithley 4200 parameter analyser for sensing the 2DEG current combined with a Keithley 2657A high power source meter which provided the back bias voltage and also sensed vertical leakage currents. Both instruments were controlled over PCIB via National Instrument's Labview software running on a pc. The probe station used is inside a metal housing which provides protection from the high voltages and also enables to measure in complete darkness.

The tested layers in figure 3.2 are unintentionally doped GaN channel, GaN buffer and AlGaN strain relief layer. In the back bias ramp measurement an insulating buffer and strain relief layer, with no internal charge redistribution, would lead to a linear relation between substrate voltage and n_S, corresponding to capacitive coupling between the conducting substrate and the 2DEG. This behaviour is usually observed for small substrate voltages where all layers are still showing purely insulating behaviour. A redistribution or injection of charges into the buffer layer from 2DEG, substrate or lateral leakage paths causes the V_{sub} versus n_S relation to deviate from linear behaviour. The range of behaviour we have observed is depicted schematically in Fig. 3.3. Negative charges in the buffer region cause an additional reduction of the 2DEG current, whereas positive charges limit this reduction. Also the partial breakdown of a layer, e.g. the buffer, can lead to

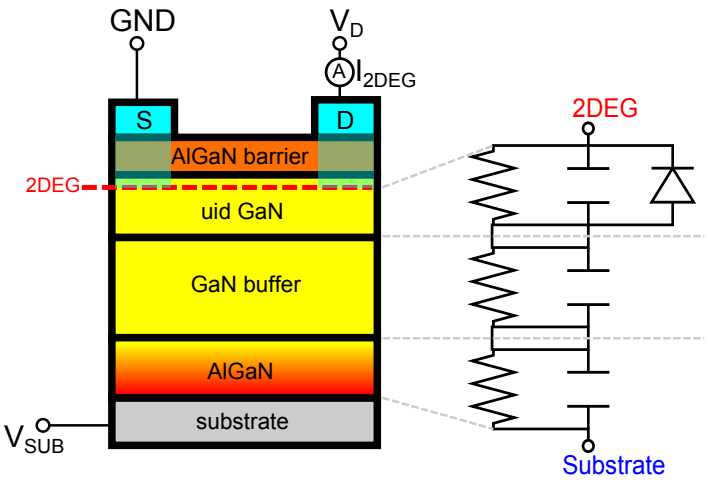

Figure 3.2: Experimental setup and equivalent circuit representation of the layers.

conduction within that layer in which then charges redistribute resulting in current reduction [85]. Lateral charge spreading along a deep hetero-interface thereby extending the capacitive area in the deeper layers can also cause reductions of the 2DEG current [86]. The effects observed during the application of a substrate bias do not necessarily remain when the back bias is ramped back to 0 V. Positive charges are usually neutralized by electrons injected from the 2DEG in a fast process leaving the 2DEG current at 0 V substrate bias unchanged. Effects that reduce the 2DEG current though can lead to a lasting reduction after the ramp. The latter behaviour is what leads to severe current collapse in real applications. Negative substrate voltages correspond to a power device application with a high positive drain voltage and a grounded substrate.

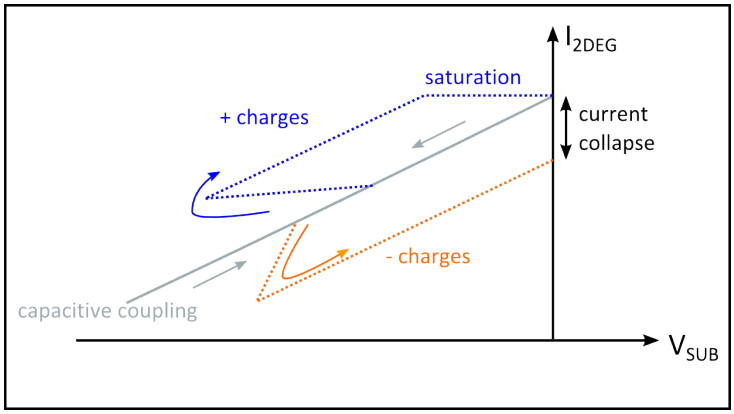

Figure 3.3: Schematic 2DEG current vs. substrate voltage plot, illustrating the impact of charging effects on a back bias ramp measurement.

3.3 Ramped Substrate Bias under Illumination

It is also possible to do substrate bias ramp measurements in combination with a light source illuminating the sample. A 175 W xenon lamp of type ASB-XE-175 combined with the monochromator CM110 both from manufacturer Spectral Products was used for that purpose to provoke excitation at specific wavelength/energy. The light was fed to the biased device via an optical fiber. The illumination angle was around 70°. The current levels at specific voltages, which are altered by effects like current collapse, can be measured for different illumination conditions. Spectral curves can then be derived that reveal the trap levels involved in the process. To get relevant and repeatable data it is very important to do effective resets between single substrate bias measurements. For this purpose light of a certain single wavelength or of a broader spectrum can be used, certain biases sometimes also help to reset a device or longer cool down periods in complete darkness are necessary. What procedure is best to quickly restore reference conditions strongly depends on material and device characteristics and effective reset procedures need to be established for individual samples.

3.4 TCAD Simulations

In addition to the experiments technology computer-aided design (TCAD) simulations were made using Silvaco's finite-element simulator Atlas Device Simulation Framework. The drift diffusion model in which currents are formulated in terms of drift and diffusion components is used to self consistently solve Poisson's equation $\nabla\phi = -\frac{\rho}{\epsilon}$ under given continuity requirements. ϕ is the electric potential field, ρ the charge distribution and ϵ the permittivity of the medium. Simulations were performed for 2D representations of the structure. Figure 3.4 shows an example of such a structure. To achieve realistic results it is most important to appropriately define the material parameters, which are composition, mobility, doping levels and concentrations and others. Before the simulation is started a mesh needs to be defined which separates the structure into smaller regions for which the solutions are derived independently in an iterative way. In figure 3.5 a mesh is shown as an overlay. Critical sections like the part of the structure containing the 2DEG and areas around edges at which the electrical fields can change rapidly need to be meshed more densely whereas in less important parts a more coarse mesh can be sufficient. A good compromise between computing time and precision needs to be found and problems with non convergence have to be avoided. In the actual simulation bias conditions are defined and how they change to replicate the actual experiment. Since charging and discharging of trap levels are of interest which are processes that are time dependent constants defining those behaviour need to be set and transient simulations with exact defined timings are necessary to address those effects. After a successful simulation 2D data of free charge carrier concentration, number of ionized dopants, electrical field, characteristic energy levels and some other parameters is available for previously defined bias conditions. A visualisation of 2D data for the electric field in the structure is shown in figure 3.6. One dimensional cuts that go vertical through the epitaxial structure can also be extracted from which band diagrams can be derived. Figure 3.7 shows such a band diagram. When good agreement between real experiment and simulation can be achieved the data gives useful insights otherwise not accessible. Also predictions on how changes to the structure impact device performance can be made.

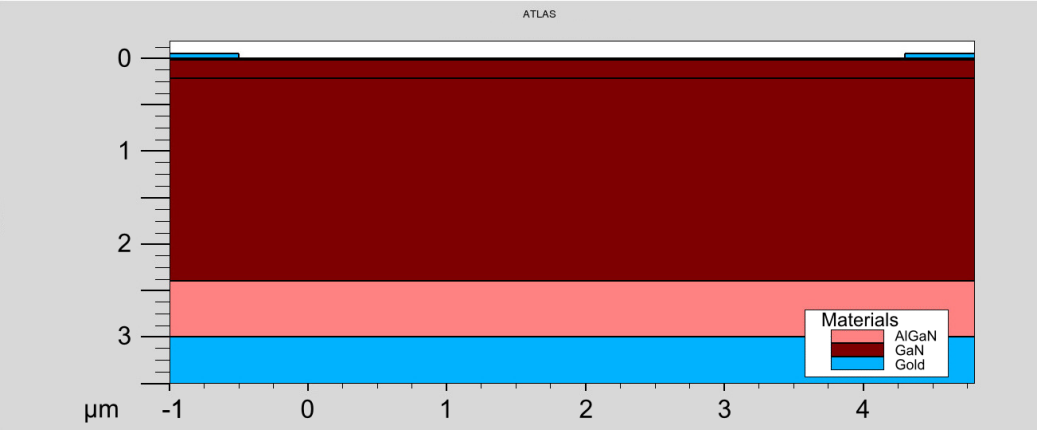

Figure 3.4: The 2D representation of a structure used for substrate bias ramp simulations. Two ohmic contacts are situated in the top corners. The bottom layer is the substrate.

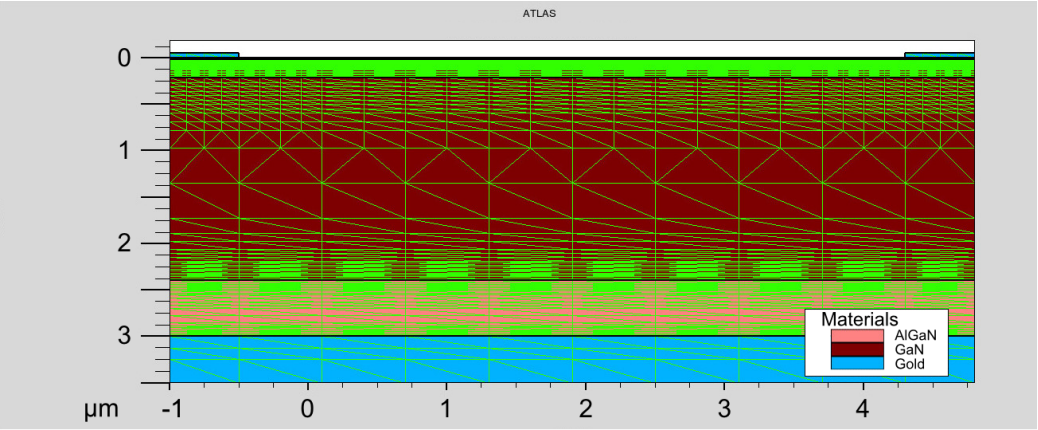

Figure 3.5: 2D representation of the substrate bias ramp structure with mesh.

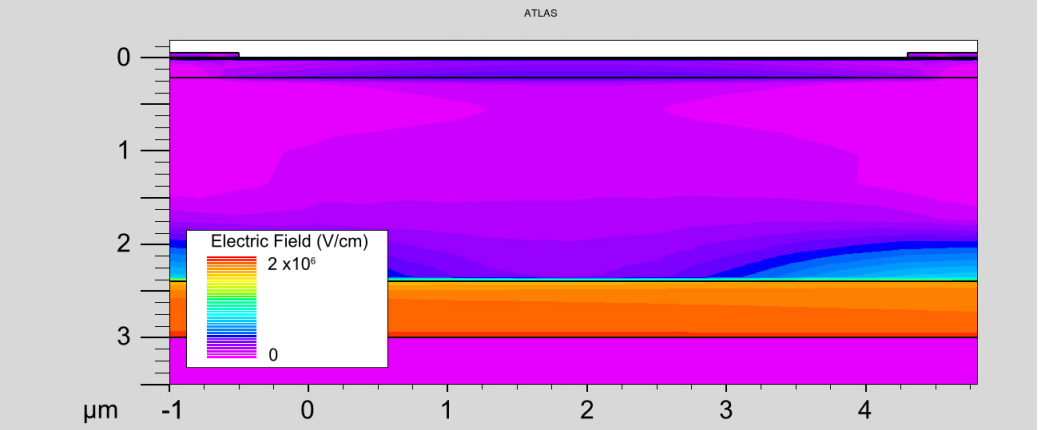

Figure 3.6: 2D image of the electrical field at 150 V substrate bias. The colouring illustrates the electric field strength for different parts of the structure.

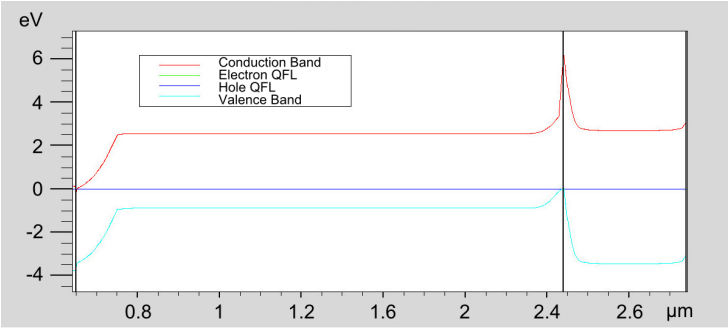

Figure 3.7: Simulated band diagram derived from a vertical cutline at 0 V substrate bias.

3.5 Focused Ion Beam and Transmission Electron Microscopy

For structural analysis of the impact that metallisation has on the epitaxy and device structure transmission electron microscopy was performed. The samples are prepared by focused ion beam milling. Thin vertical cuts are produced and then scanned by transmission electron microscopy to see details from contact area and epitaxy underneath. The destructive procedure which is very time intensive was performed by my colleagues Richard Webster and David Cherns at the University of Bristol.

3.6 Coherent Correlation Interferometry

For analysis of the topography of larger areas coherent correlation interferometry (CCI) was used [87]. The CCI tool is also located at IQE in Cardiff. In a CCI measurement white light is used together with a beam splitter and reference mirror to produce interference fringes from which the topology can be derived, see figure 3.8. With the CCI $350\times350\,\mu m^2$ squares can be measured. The process is faster than the more common atomic force microscopy (AFM) with all the mechanics never being very close to the sample. So it is non destructive and easy to be used in a production environment. The vertical resolution of the CCI is in the nanometre range. The scale of a CCI image is closer to the size of the actual devices and can reveal details easy to be missed in an AFM image which scans smaller areas with better height resolution but slower. The two techniques therefore complement one another.

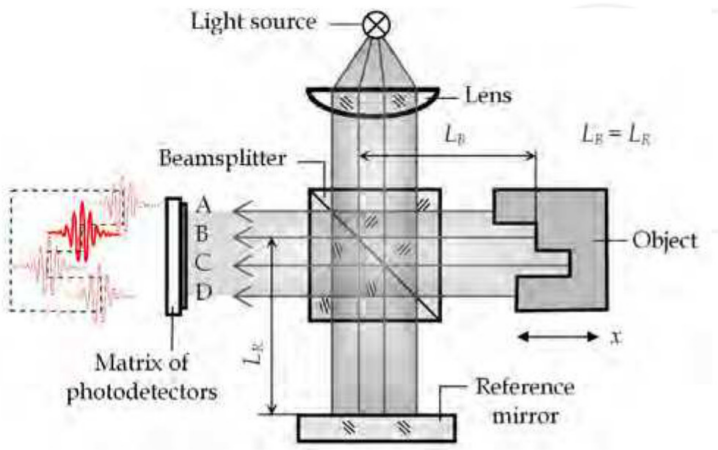

Figure 3.8: Schematic describing the coherent correlation interferometry [87].

3.7 Secondary Ion Mass Spectrometry

To get information on the concentration of impurities and dopants secondary ion mass spectrometry (SIMS) was used. During SIMS profiling the surface of the material is being sputtered with a beam of primary ions while secondary ions formed during the process are analysed in a mass spectrometer. A depth profile of the chemical concentration for the elements of interest is generated. SIMS analysis for this work was done by the commercial provider EAG laboratories.

Chapter 4

Charge movement in AlGaN/GaN on Si HFET structure with carbon doped GaN buffer and graded AlGaN strain relief layer

A GaN HFET structure with graded AlGaN strain relief layer is introduced in this chapter. The structure contains a carbon doped buffer. Carbon doping should render the material semi-insulating and is commonly incorporated to prevent punch-through and to increase the breakdown voltage. Experiments investigating the current collapse in the structure are presented and compared with simulations for a better understanding of the relation between current collapse and the epitaxial layers, in particular the carbon doped GaN. Parts of the work presented in this chapter have been published in [85].

4.1 Epitaxial and device structure

An AlGaN/GaN on Si HFET structure was produced for investigation of the impact that a carbon doped buffer has on current collapse characteristics. The epitaxy is designed to emphasize the impact of the carbon doped GaN layer. Complexity

of other layers is kept low to reduce the potential impact of other structural features and to enable precise simulation of the structure. The sample was grown by MOCVD on a conducting p-type Si substrate of 6 inch diameter. Conducting substrates are commonly used for GaN on Si power devices and allow one to use the substrate as an electrode in substrate voltage ramp experiments. The layer stack including thickness of each layer can be seen in figure 4.1. A low temperature AlN nucleation layer is deposited first onto the substrate to achieve two dimensional growth and prevent meltback etching. The AlGaN strain relief layer follows in which the Al and Ga concentrations are controlled via the TMG and TMA flows during the growth to create a linear grading from AlN to GaN. The graded strain relief section effectively reduces bow and mechanical stress during high temperature growth and cool down of the material and allows to crack-free grow layers of more than 3 µm thickness without introducing sharp interfaces. Additional hetero interfaces in the structure would provide potential barriers for free charges and could form lateral leakage paths. This could potentially impact current collapse and, due to increased complexity, would make it more difficult to properly simulate the physics. A thick, carbon doped GaN buffer is chosen to investigate the impact of such a layer on device performance. The chemical carbon concentration is constant throughout and in the range of 1×10^{18} to $1\times10^{19}\,\mathrm{cm}^{-3}$ based on SIMS measurement data from similar structures. The top two layers are the unintentionally doped (uid) GaN channel layer in which the 2DEG forms at the interface with the AlGaN barrier layer which is grown on top of the channel with an Al composition of 25 %. C, O and Si concentration in the uid layer were below $1\times10^{17}\,\mathrm{cm}^{-3}$. To perform substrate bias ramp experiments the wafer has been processed at NXP UK in Stockport within the PearGaN project. A commercially approved process has been used to deposit ohmic contacts and isolate structures via ion implant. Also a passivation layer has been applied. Because of confidentiality reasons some details of the processing can not be revealed. Sheet resistivity, 2DEG density and contact resistance of the processed HFETs are $419\,\Omega/\square$, $5.5\times10^{12}\,\mathrm{cm}^{-2}$ and $1.06\,\Omega$mm. Circular and linear test structures as described in figure 4.2 were used for the back bias tests. The circular structures exclude any leakage effects along mesa edges between the contacts since no such edges are present and allow to quantify those effects when compared to the linear structures.

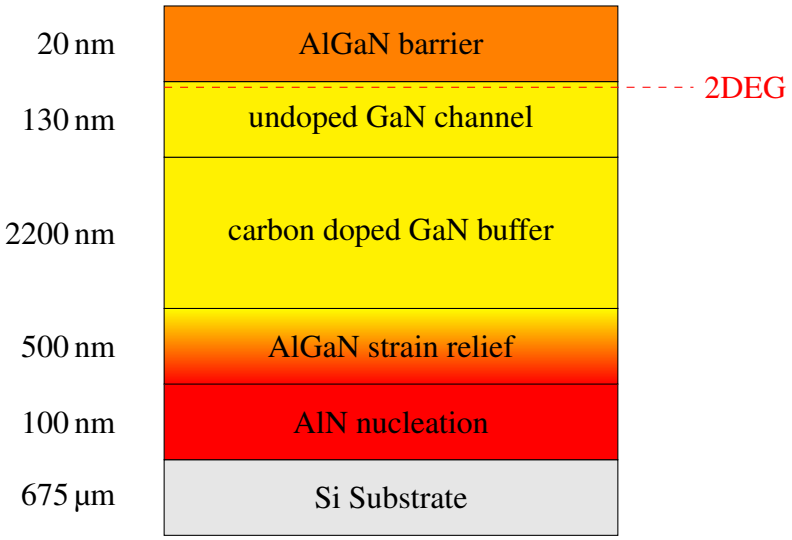

Figure 4.1: Epitaxial structure of GaN HFET with graded Strain Relief Layer. Sample ID: PearGaN GaN15 wafer 1.

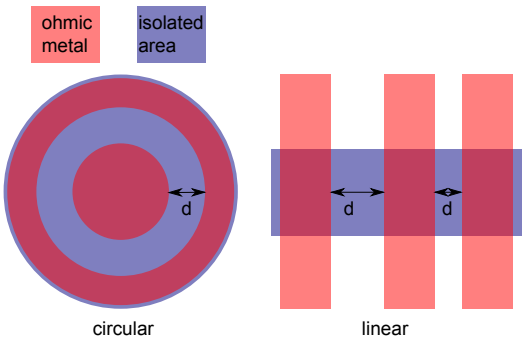

Figure 4.2: Schematic of the test structures. Different gaps d between the ohmic contacts are possible.

4.2 Substrate Bias Ramps

The substrate bias ramp technique described in section 3.2 was used to investigate the impact of high electric fields in the buffer on 2DEG charges for the carbon doped buffer sample. The results of a substrate bias ramp measurement can be seen in figure 4.3. Under applied negative substrate bias the curve bends downwards below the capacitive coupling line indicating accumulation of negative charges in the structure reducing the 2DEG concentration more strongly than pure capacitive coupling would. The effect increases with higher bias leading to a steeper slope and further drop in the 2DEG current. When ramping up the bias towards 0 V again the current only recovers slowly with a rate which is below that of the capacitive coupling indicating further charging and no neutralisation of charges with reduced electrical fields. The result is a strongly reduced 2DEG current with no bias applied.

A comparison of substrate bias ramps on linear and circular structures is shown in figure 4.4. No significant difference is observed illustrating that edge effects have no impact on the measurements on this sample. Neither is the gap distance in the 20 - 50 µm regime a relevant influence when changed and effects related to the contact area have no major impact [88].

Figure 4.5 shows how the current recovers after a negative substrate bias ramp measurement. After 2 minutes only $\sim$1.5 % of recovery is observed after the substrate bias initially reduced the current by about 20 %. Strong current collapse is therefore to be expected for a transistor device built from this structure when positive drain bias of similar voltage is applied in off-state. An accelerated current collapse recovery is possible by illumination with white light. More detailed studies on the impact of illumination on the buffer charges will follow in chapter 5. The reduction of current after application of substrate bias indicates that negative charges in the buffer structure are affecting the 2DEG which are not being neutralised during the ramp and remain after return to 0 V substrate bias. Under the electric field present in the epitaxial layers a negatively charged region only builds when either electrons move vertically towards the 2DEG or holes move into opposite direction, i.e. towards the substrate. Since the current collapse remains after applied bias charges are not immediately neutralised. Hence, either free charge

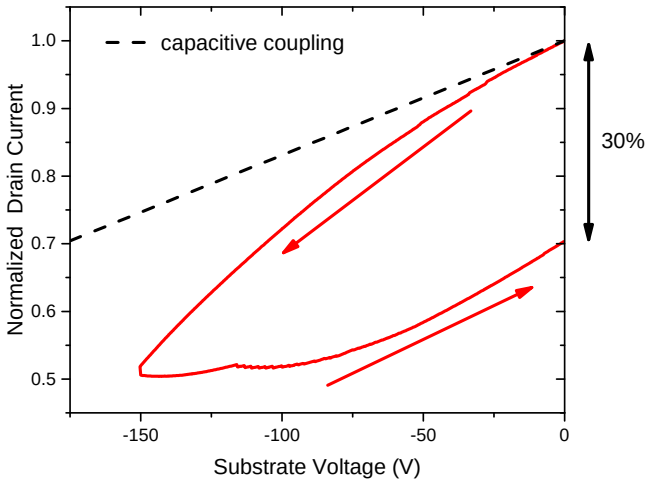

Figure 4.3: Substrate bias measurement. Drain voltage = 1 V. Circular structure, source drain gap = 25 µm, central dot diameter = 100 µm. Ramprate = 4 V/s.

carriers are trapped in a new location within the structure, charges have been injected or removed from the structure.

The vertical currents measured at the substrate, shown in figure 4.6, remain very low throughout the measurement setting an upper limit for charge injection from the substrate close to the background noise of the setup.

The impact of different ramp rates for substrate voltage on the measured drain currents is shown in figure 4.7. Decreasing the ramp rate means more time for charging effects which increase the current reduction. The displayed measurement at lowest ramp rate of 1.2 V/s has an inflexion point at about -75 V on ramping down the substrate bias indicating the beginning of saturation of the charge process. Figure 4.8 also shows what happens when the substrate is ramped to positive voltages immediately after the negative ramp for two different ramp rates. The current further increases under positive substrate bias and saturates close to the initial current level in both cases. When the voltage is ramped back to 0 V in case of the faster ramp rate the current level further decreases compared to only negative substrate bias ramping due to the additional electrons in the structure whereas at the slower ramp rate surprisingly the current ends up at a current level which is in between the initial current level and the level after negative substrate

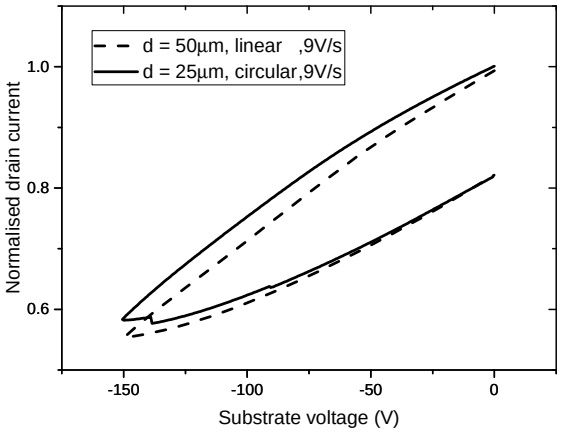

Figure 4.4: Substrate bias ramp comparison for linear and circular structure with different gaps between the contacts.

bias only. To understand this behaviour and to determine exact position and origin of the charges is difficult based on experiments only. Simulations can help to get a better insight.

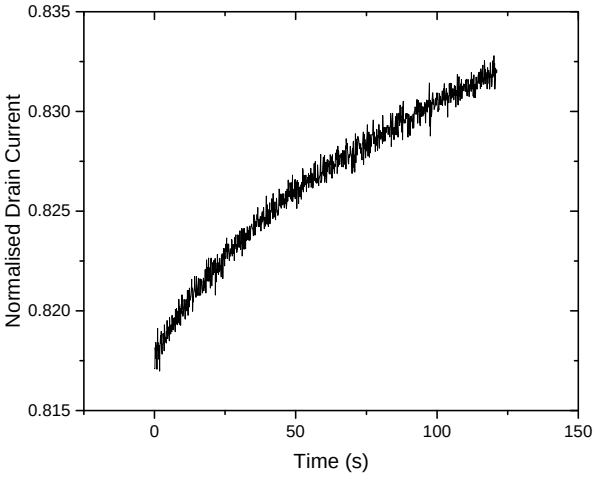

Figure 4.5: Current recovery over time after the negative substrate bias ramp shown in figure 4.4 (circular structure).

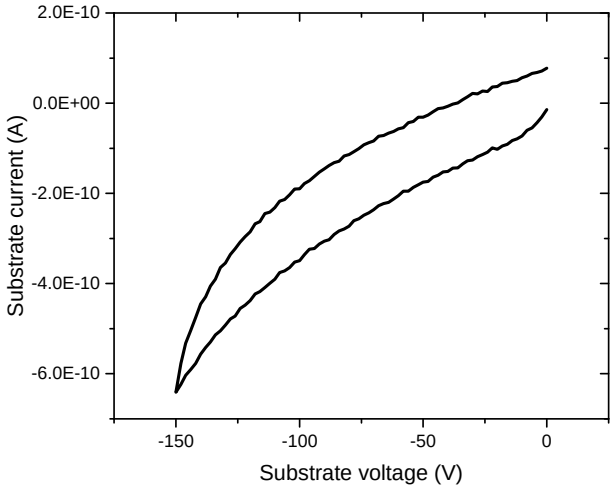

Figure 4.6: Vertical current measured at the substrate during a substrate bias ramp measurement. Device area = 0.14 mm^2.

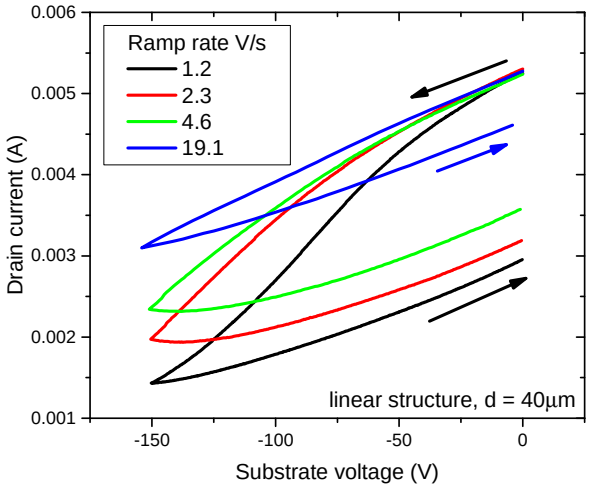

Figure 4.7: Substrate bias ramps measured for different ramp rates.

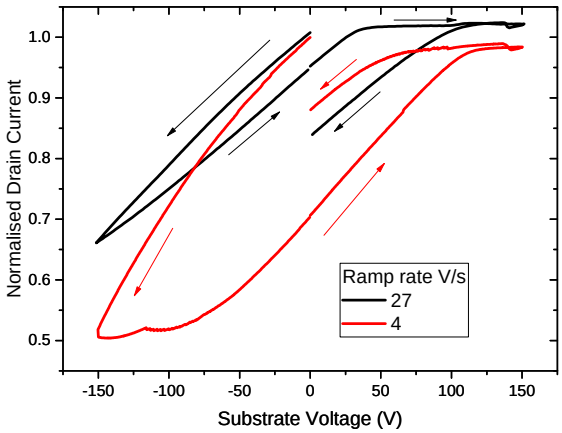

Figure 4.8: Negative and positive substrate bias ramps measured for two different ramp rates.

4.3 Simulation of Charge Movement

To understand the charging effects in the buffer responsible for current collapse simulations were performed which replicate the substrate bias experiments. When agreement between simulation and experiment can be achieved the simulation data can reveal information which is not accessible otherwise. A 2D representation of the structure was created with three contacts: source and drain ohmic on top and substrate at the bottom, see figure 4.9. Drift diffusion simulations were performed using Silvaco's Atlas Device Simulation Framework as described in section 3.4 with activated Shockley-Read-Hall recombination and Fermi-Dirac statistics models.

As illustrated in figures 4.10, 4.11 and 4.12 the results of simulated substrate bias ramps strongly depent on various parameters. Figure 4.10 shows how acceptor and donor concentrations in the carbon doped GaN buffer layer, meant to reflect the carbon doping based on the models in [66], affect the current collapse observed. Changing the donor concentration while the acceptor concentration is constant and much higher will also redefine the ionised acceptor charge. This causes the current reduction to increase as can be seen in particular for negative substrate bias. Increasing the acceptor concentration by an order of magnitude while the donor concentration remains unchanged greatly increases the current reduction for both substrate bias polarities.

In figure 4.11 the impact of changes to the acceptor capture cross sections σ in the carbon doped GaN is shown. The σ parameters are currently not well known, so their is some latitude in their value which typically are assumed to be around $10^{-15}\,\mathrm{cm}^2$. An increase of the Coulomb attractive capture cross section σ_p by one order of magnitude, causing higher acceptor ionisation rate, leads to increased current reduction for both negative and positive substrate bias. Whereas increasing σ_n, which affects the neutralisation of acceptor states, reduces the current reduction after positive substrate bias but does not change the current reduction under negative substrate bias.

How changes to the acceptor ionisation energy alter the substrate bias ramp curve can be seen in figure 4.12. A reduction of the energy needed for ionisation of the acceptor states by less than 5% from 0.9 eV to 0.86 eV causes the current re-

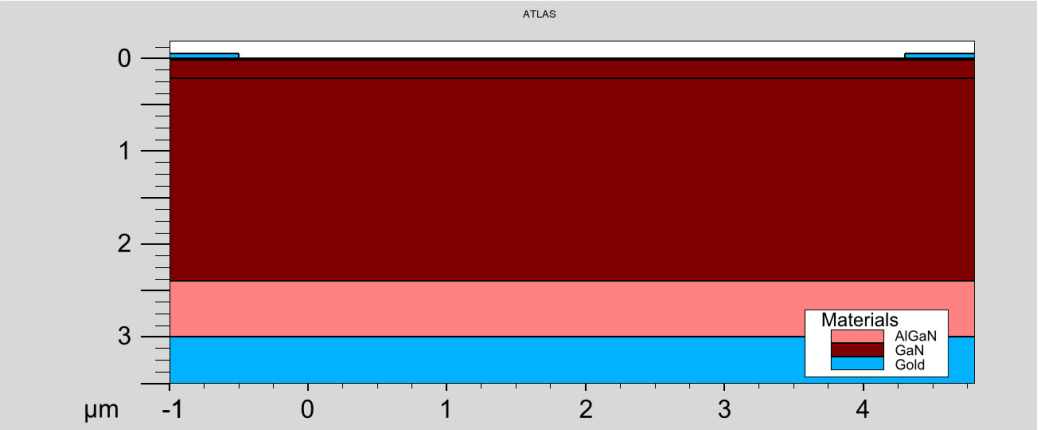

Figure 4.9: The 2D representation of a structure used for substrate bias ramp simulations.

Table 4.1: Simulation parameter for carbon doped GaN buffer layer affecting current collapse.

GaN:C parameter affecting current collapse	under negative substrate bias	under positive substrate bias
donor concentration	yes	yes
acceptor concentration	strong	weak
acceptor σ_p	yes	yes
acceptor σ_n	no	yes
acceptor ionisation energy	strong	strong

duction to significantly increase and change the behaviour under positive substrate bias from slightly reducing the current reduction to nearly doubling the reduction. A large number of other parameters needs to be defined for all different parts of the structure of which all have some influence on the outcome of the simulation. The dependencies shown and summarised in table 4.1 are examples for parameters that need to be tweaked to achieve agreement with the experiment.

In the following paragraph definitions that were crucial for good agreement between simulation and experiment are given. The capture cross sections σ_n and σ_p are $10^{-15}\,\mathrm{cm}^2$ and $10^{-13}\,\mathrm{cm}^2$ respectively for acceptor traps and vice versa for donor traps in all layers. To represent n-type background doping in the uid GaN layer $5\times10^{16}\,\mathrm{cm}^{-3}$ shallow donors are introduced. The carbon concentration in the GaN:C layer is set at $5\times10^{18}\,\mathrm{cm}^{-3}$ with the deep acceptor energy level at

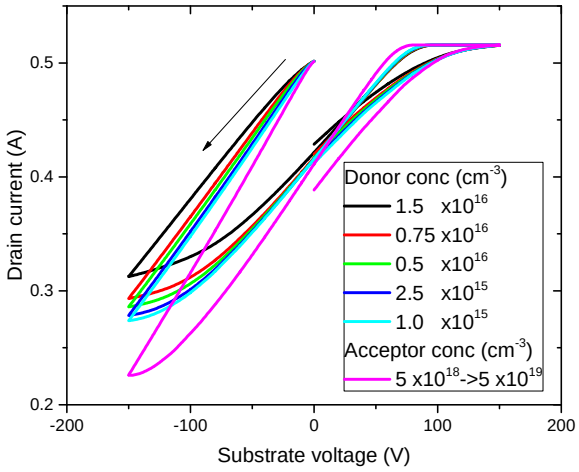

Figure 4.10: Simulated substrate bias ramp measurements for different doping concentrations in the GaN:C buffer. The first five curves, black to cyan, replicate the effect that a change in the donor concentration has, while the Acceptor concentration remains at $5\times10^{18}\,\mathrm{cm}^{-3}$. The magenta coloured curve represents the situation for an increased acceptor concentration while the donor concentrations is kept at $1\times10^{15}\,\mathrm{cm}^{-3}$. The Simulated substrate bias ramprate was 0.1 V/s.

0.9 eV above the valence band according to simulations in [89] under the assumption that carbon is incorporated mainly on nitrogen sites. Those deep acceptors are partially compensated by n-type doping of $1.5\times10^{17}\,\mathrm{cm}^{-3}$ representing a smaller number of carbon substituted on Ga sites [89, 90]. Doping in the graded AlGaN layer contains a shallow acceptor concentration of $1\times10^{18}\,\mathrm{cm}^{-3}$ representing the polarization induced charge in a linearly graded layer [91]. Those acceptors are fully compensated by shallow donors with a concentration of $1.5\times10^{18}\,\mathrm{cm}^{-3}$, which again are compensated by an acceptor with a concentration of $2\times10^{18}\,\mathrm{cm}^{-3}$ defined with constant energy below the conduction band, ensuring a smooth alignment of bands at the graded region's upper interface and a mid gap position at the interface with the Si substrate, causing insulating behaviour. The band diagram of the structure reflecting the parameter choices is shown in figure 4.13. The nucleation layer is ignored in the simulation and the conducting Si substrate is represented as an electrode. The polarisation charge at the AlGaN barrier / GaN interface is represented by a fixed charge of $0.017\,\mathrm{C/m}^2$ based on calculations for

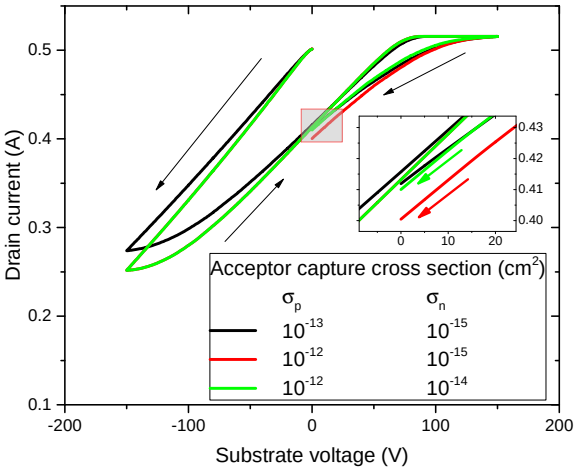

Figure 4.11: Simulated substrate bias ramp measurements for different capture cross sections of the acceptor in the GaN:C buffer. The inset is a magnification of the highlighted area at which the currents end up after the positive substrate bias ramp. The Simulated substrate bias ramprate was 0.1 V/s.

25% Al in the barrier using equation 2.2. The resulting 2DEG density is around $5\times10^{12}\mathrm{cm}^{-}2$. The mobility for electrons is increased to 1400 cm^2/Vs in the channel region where the 2DEG forms. The polarisation charge at the barrier surface is set to zero corresponding to full compensation by surface donors. Self heating and impact ionisation are being neglected, since we are only concerned with the low field regime well below breakdown. The simulated temperature was 293 K for all simulations.

In figure 4.14 the substrate bias ramp measurements of figure 4.8 are shown again together with the simulation results. At the faster ramp rate the current reduction after negative substrate bias is lower since overall stress time is reduced. Positive substrate bias leads to a current saturation at the initial value and some variation in behaviour between slow and fast ramp when returning to 0 V substrate bias again.

Ramp curves based on the simulations are also shown in figure 4.14 and show excellent agreement. The ramp rates for agreement between simulation and experiment are surprisingly close given the essentially unknown compensation level

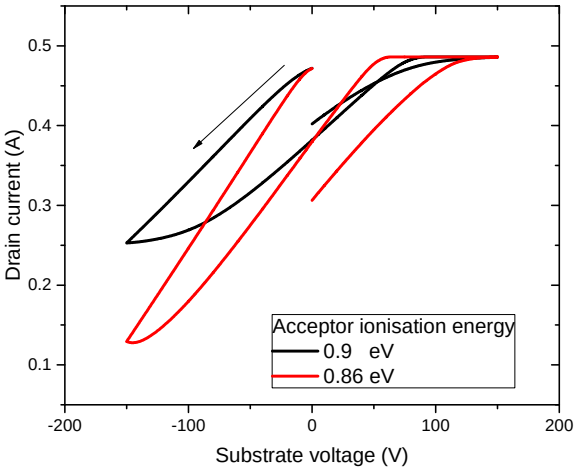

Figure 4.12: Simulated substrate bias ramp measurements for different acceptor ionisation levels in the GaN:C buffer. The Simulated substrate bias ramprate was 0.1 V/s.

with the remaining difference in ramp rate reflecting a discrepancy between experiment and simulation in the thermally activated hole density in the GaN [90].

The good agreement between experiment and simulation suggests that the assumed carbon level of 0.9 eV above the valence band is correct, since simulation results are very sensitive to changes of the dominant dopant's energy level. Also the good agreement suggests that the observations can be explained by effects based only on the physics simulated by the software. Hence, vertical leakage through the uid GaN layer as observed for both samples in [92], other trap assisted tunneling effects related to high electric fields or radiative recombination caused by hot electrons as described in [93] do not significantly influence the observed behaviour. The measured vertical leakage, see figure 4.6, is in the same order of magnitude as the simulated displacement currents suggesting no significant injection of charges from the substrate. To explain the charging effects we will focus on the slower ramp rate simulation.

Figures 4.15 and 4.16 show simulated band diagrams and charge position during the back bias ramp. Figure 4.15 b shows that flattening of bands in the GaN:C region and increasing the electrical fields in the adjacent layers, causes the ex-

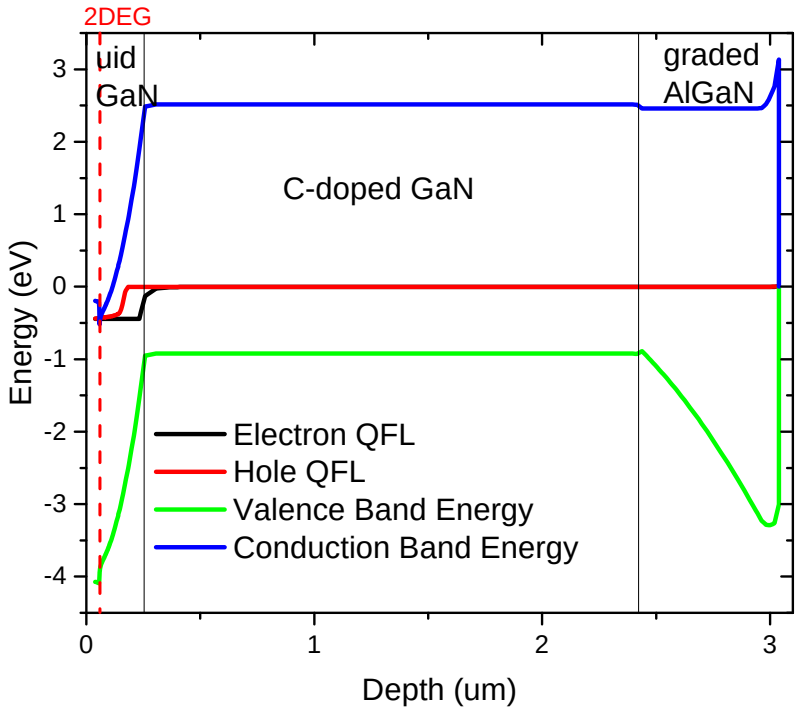

Figure 4.13: Band diagram of the simulated structure with no substrate bias. A vertical cut through the structure was used in the centre between the top contacts with 1 V bias on the drain contact.

tended current reduction under negative back bias. The reason for the flattening can be deduced from figure 4.16, where the formation of positive and negative space charges under negative back bias is depicted.

Figure 4.17 shows what happens when the substrate bias is ramped to negative bias. Near the 2DEG carbon acceptor states are thermally ionised, creating free holes that move towards the substrate where they are trapped, partially neutralising deep acceptors in the graded layer and creating the positive space charge by exposing the ionised donors.

After the back bias (c) the space charges remain. In figure 4.18 the charge position and how it alters the band structure is depicted. The negative space charge near the 2DEG causes the current reduction shown in figure 4.14 after moderate -150 V bias.

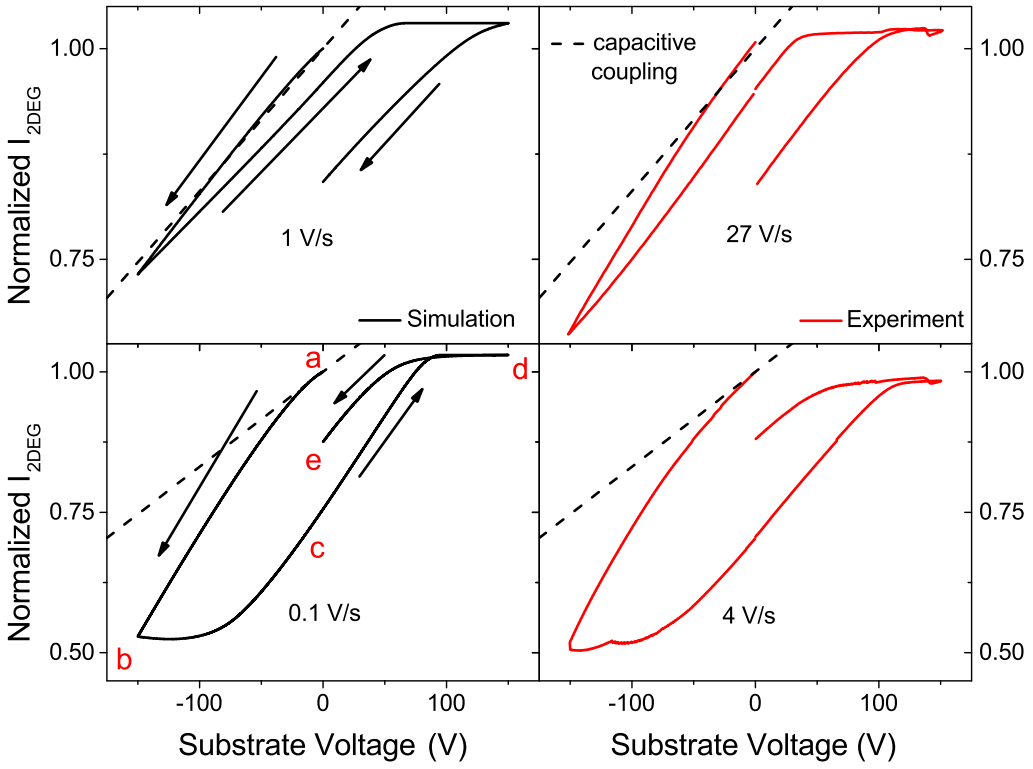

Figure 4.14: Simulated (left) and measured (right) back bias sweeps are shown for fast (top) and slow (bottom) ramp rates. Arrows indicate the direction of the substrate voltage ramps. $V_D = 1$ V. The dashed line corresponds to the prediction of capacitive coupling.

As shown in figure 4.14 ramping to a positive back bias of 150 V subsequently results in I_{2DEG} saturation near the initial current level. This is due to the injection of electrons into the structure via the forward biased np junction between 2DEG and GaN:C (figure 4.15 d). The injected electrons are trapped by acceptor states in the GaN:C, mainly at the GaN:C / graded AlGaN interface. The resulting negative charge screens the 2DEG from the substrate bias and keeps the electric field below the channel constant. Before the injection of electrons begins the electric field building in the carbon doped GaN, while ramping to positive substrate bias, is similar to that during the ramp to negative substrate bias but with changed polarity. It is therefore likely that acceptor ionisation is also appearing this time at the bottom of the GaN:C layer. Figure 4.19 illustrates both the electron injection from the 2DEG and the thermally generated holes moving towards the 2DEG where

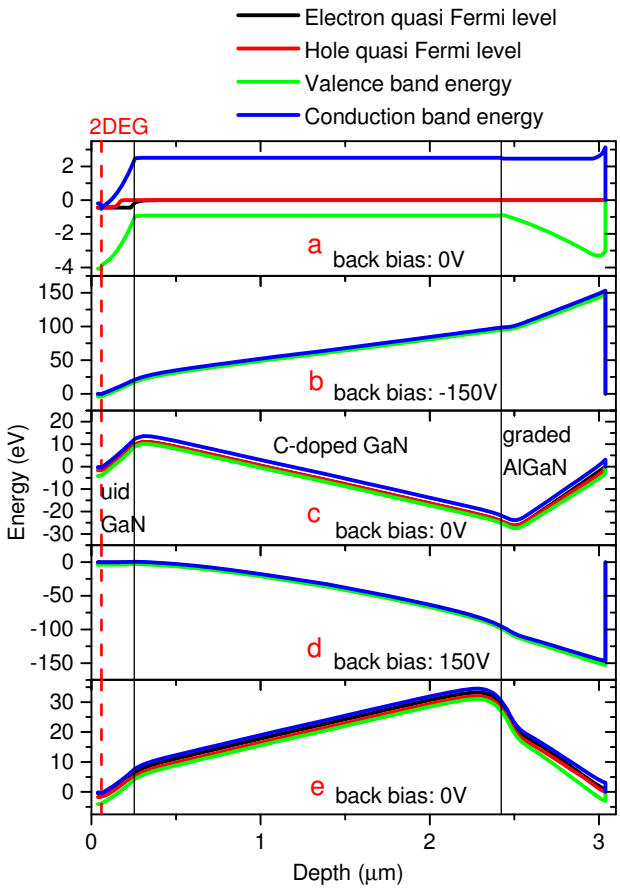

Figure 4.15: Band diagrams during the substrate bias sweep, displayed against depth. Initially the Fermi levels are leveled throughout, as no substrate bias has been applied yet (a). Under negative back bias (b) the bands are lifted on the substrate side. In the C-doped region the bands are flattened. More voltage is therefore dropped across the uid GaN channel and the graded AlGaN layer. At 0 V substrate voltage after negative back bias (c) charge accumulation in the GaN:C results in a lift of the bands. Whereas a lowering of the band energies is observed in the graded layer. Under positive back bias (d) the upper part of the structure is screened with most voltage dropped across the deeper layers. After negative and positive back bias (e) bands are lifted throughout, but mainly in the lower part of the GaN:C. Drain bias = 1V.

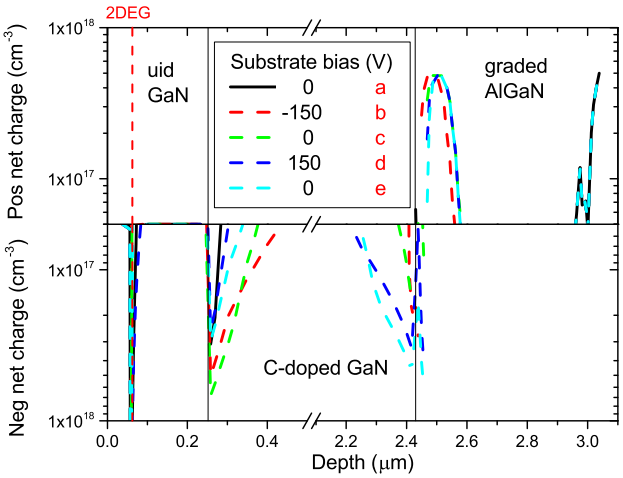

Figure 4.16: Simulated net charge concentrations versus depth under bias conditions a to e, illustrating charge position and movement in the epitaxial structure on logarithmic scales for positive (upper half) and negative (lower half) net charges. Under negative back bias (b) a negative charge accumulates at the upper GaN:C interface and a positive charge of similar size builds up in the graded layer. Both space charges remain after the back bias (c). Positive back bias (d) leads to an additional negative charge at the lower GaN:C interface, whilst the charge region at the upper interface is reduced in size.

they neutralise ionised acceptor charges. In case of the slow ramp the number of thermally generated holes in the GaN:C region that are created during the positive ramp is sufficient to mostly neutralise the excess ionised acceptor charge at the top interface. The effect is described in figure 4.20 and the result can be seen in figures 4.15 e and 4.16. Though the injected electrons create a significant negative charge at the bottom of the GaN:C the ionised acceptor concentration at the top is reduced. The impact of charge on n_S is weighted by its distance to the 2DEG based on classical electrostatics: $q\Delta n_S = -\int yQ(y)dy$. As the charges at the top interface are much closer to the 2DEG, their effect on n_S is far greater, explaining less reduction of I_{2DEG} after the positive back bias ramp. It is important to notice that the simulation does not suggest any electron injection from the substrate into the epitaxial structure. The charge redistribution within the GaN:C layer on its own is obviously sufficient to explain the observed behaviour. Experimentally, electron injection from the Si substrate is likely to occur associated with vertical leakage [94], however any electron trapping would most likely be localised to

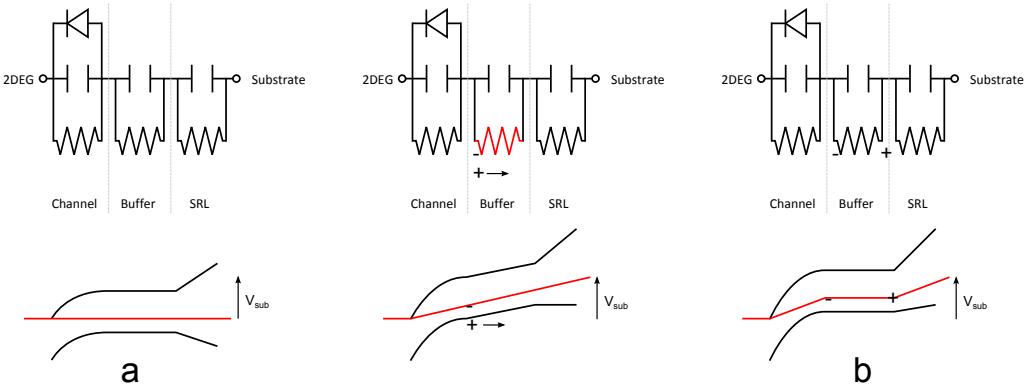

Figure 4.17: Equivalent circuit diagram and band diagram sketches illustrating the charge movement between position a and b of the substrate bias ramp.

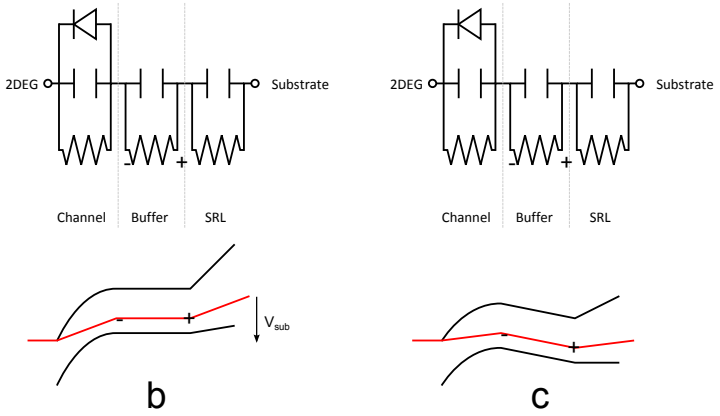

Figure 4.18: Equivalent circuit diagram and band diagram sketches illustrating the changes between position b and c of the substrate bias ramp.

those leakage paths and hence would not strongly impact our measurements. The fact that the experimentally observed current reduction lasts for a period of several 100's of seconds and that recovery can be accelerated by white light illumination is perfectly explained by the ionised deep acceptor states being its main cause.

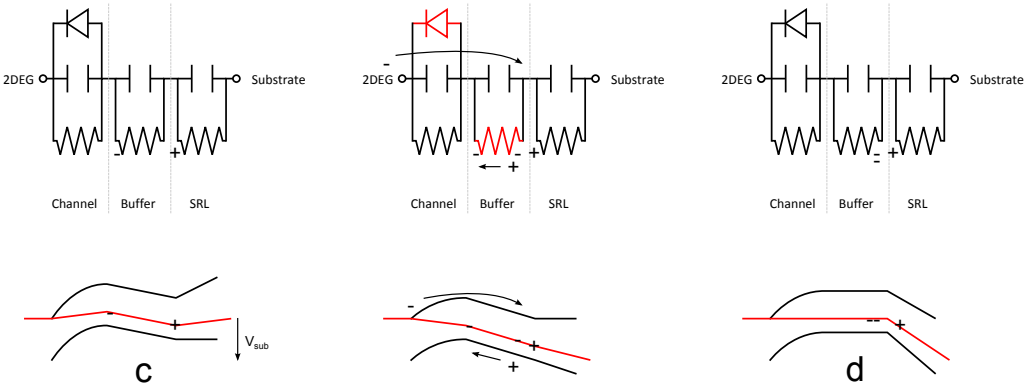

Figure 4.19: Equivalent circuit diagram and band diagram sketches illustrating the charge movement between position c and d of the substrate bias ramp.

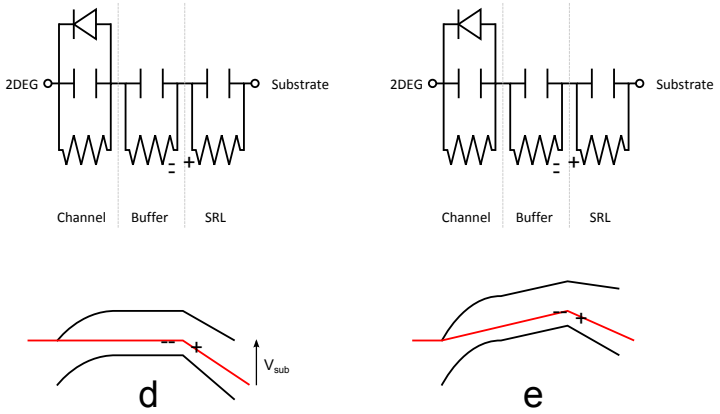

Figure 4.20: Equivalent circuit diagram and band diagram sketches illustrating the changes between position d and e of the substrate bias ramp.

4.4 Conclusion: Charge movement in AlGaN/GaN on Si HFET structure with carbon doped GaN buffer and graded AlGaN strain relief layer

The structure grown successfully enabled to show a clear relation between the carbon doped layer and current collapse. The chosen layer stack allowed to precisely simulate the effects observed. A detailed insight into charge movement and position during substrate bias ramping was established.

The current collapse after negative back bias implies high dynamic on-resistance and serious current instabilities under field polarities corresponding to those of a device with grounded substrate and positive voltage applied to the drain contact, making the device unsuitable for power applications. The investigated sample obviously lacks a vertical leakage path for holes from the 2DEG [92] and a barrier to hinder holes from moving into the strain relief layer. Intentional incorporation of dislocations into the uid GaN, which presumably establishes the vertical leakage path, could prevent the current collapse, but increasing the defect density is also likely to come with other detrimental effects.

The ionisation and redistribution of charges in the carbon doped GaN discussed here also impacts its beneficial effect regarding vertical breakdown, as the described effects cause increased voltage drop and therefore higher electrical fields in the adjacent layers. Keeping the thickness of such a layer reasonably thin in relation to the overall epitaxial structure is therefore desirable.

Chapter 5

Charge trapping under illumination in AlGaN/GaN on Si HFETs with Hetero Interfaces in Strain Relief Layer

Difference in behaviour in relation to buffer trapping is investigated for two samples. The samples are nominally very similar but from different production lines. Buffer trap configurations are not easy to be tested. Provoking excitation by for example illuminating the material and monitoring the reaction is a possible way to identify trap states. Since here the differences occurred only under illumination in combination with substrate bias ramping is used to characterise trapping mechanisms and understand the behaviour. Parts of the content of this chapter have been presented at the CSManTech conference 2016.

5.1 Epitaxial Structure

A new sample is introduced in this chapter. The sample was grown in another IQE epitaxy fab in Massachusetts USA. Like the sample described in the previous chapter 4, it also contains a large carbon doped buffer and is therefore expected to show behaviour similar to what was observed in chapter 4. Hereafter the new

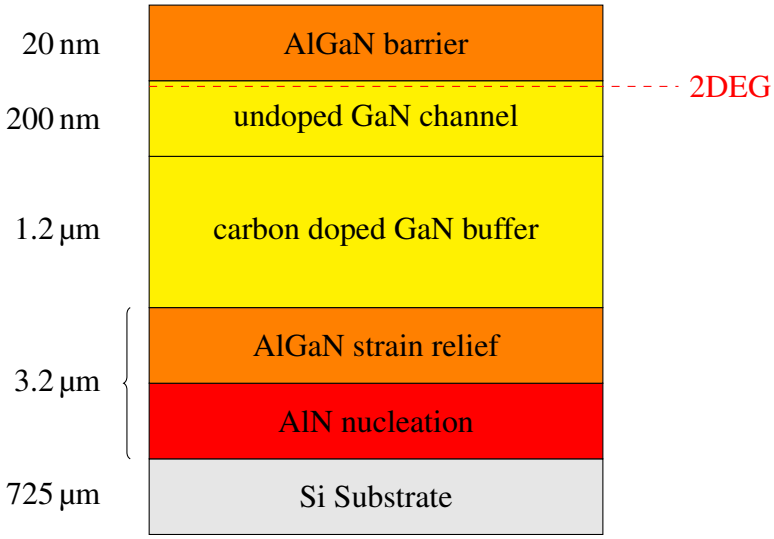

Figure 5.1: Epitaxial structure of sample B: GaN HFET with hetero interfaces in the Strain Relief Layer. Sample ID: IQEMA804.

Table 5.1: Sheet resistivity R_S and charge concentration n_S for samples A and B. Measured by TLM and mercury probe CV techniques.

	A	B
R_S [$\Omega/\square$]	419	464
n_S [1×10^{12} cm^{-2}]	5.5	7.59

sample will be referred to as sample B and the sample introduced in chapter 4 will be sample A. Sample B was grown also by MOCVD, but in a different reactor type than sample A. A sketch of the epitaxial structure is shown in figure 5.1. The substrate used is p-type Si of 8 inch diameter and 725 µm thickness. The nucleation layer and strain relief layers contain AlN sections and several hetero interfaces. Combined thickness of nucleation and strain relief layer is 3.2 µm. No further details are known for these layers. The carbon doped GaN buffer layer is 1.2 µm thick. The unintentionally doped channel and AlGaN barrier are 200 and 20 nm thick. The Al concentration in the barrier is 25 %. The barrier therefore is the same as for sample A which leads to similar 2DEG and transistor characteristics. Test structures were also processed by IQE Massachusetts. Sheet resistivity and charge concentration are given in table 5.1.

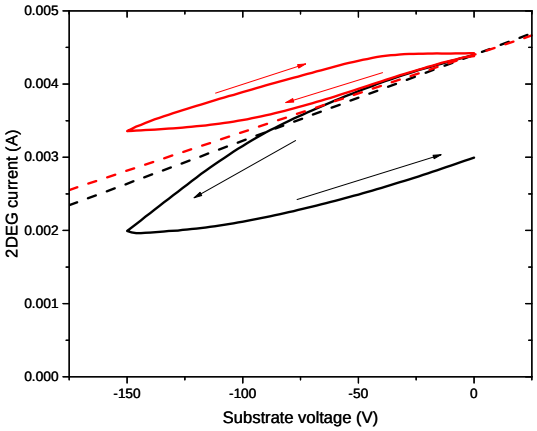

Figure 5.2: Substrate bias ramp curves. Samples A and B. Ramp rate = 4 V/s, drain voltage = 1 V, measured at room temperature. Arrows indicate the direction of substrate bias ramp. The dashed lines show the expected curves for purely capacitive behaviour of the two structures.

5.2 Substrate Bias Ramps

Substrate bias ramp measurements for samples A and B are shown in figure 5.2. Linear TLM structures with 40 µm gap length and 100 µm width are used and the initial current measured without substrate bias is nearly identical for both samples. A clear reduction of current below the capacitive coupling line is observed for sample A. This suggests accumulation of negative charges in the vicinity of the 2DEG, which are not neutralized on the return ramp, resulting in a significant current reduction after application of back bias. The curve of sample B shows completely different and much more desirable behaviour. The 2DEG current is reduced less than suggested by capacitive coupling, indicating positive charge trapping, resulting in a return at higher current levels, eventually saturating at the initial value due to electron injection from the 2DEG into the buffer. This sample demonstrates the required condition of no net charge trapping following bias stress, in contrast to sample A, which exhibits a current reduction that lasts for 100's of seconds or more and will inevitably result in severe current collapse. The behaviour of sample B can be explained only by injection of positive charges. The polarity of the electric field requires that those charges must originate from the 2DEG [92]. A leakage path for holes through the uid GaN channel is therefore

present in sample B but not in sample A. Trap assisted tunnelling along dislocation defects could provide such a leakage path. A difference in the formation of those dislocations could be related to growth or device processing conditions. Since for samples A and B both growth and processing were not identical other samples need to be tested to identify a relation.

5.3 Substrate Bias Ramps and Illumination

To further investigate the buffer trapping of samples A and B substrate bias ramps under illumination are performed. Details of the experimental setup are described in section 3.3.

5.3.1 Experiment

Back bias measurements for the two samples are shown in figure 5.3 both with and without illumination. When a back bias ramp is performed under illumination of specific wavelength / photon energy, the resulting current variation can differ substantially allowing to identify excitation effects and trap energy levels that are active. Figure 5.3 shows what happens when samples are illuminated with light of three example wavelengths. Extraction of the current at a specific substrate voltage for all wavelengths tested provides the data for a spectral response curve. A substrate voltage of -75 V on the return ramp has been chosen for the graphs shown in figure 5.4. Both samples exhibit a high current, well above the unlit level, when illuminated with above GaN bandgap (3.4 eV) photon energy. The large number of generated electron hole pairs is responsible for this effect and effectively screens the 2DEG from the back bias, resulting in the flat ramp curves at 3.44 eV in figure 5.3. At lower photon energies the current level of Sample A drops, saturating close to the value measured without any light. In contrast, sample B shows a significant drop of current at about 3.2 eV to values well below unlit level. This suggests the existence of an ionization process associated with this energy in sample B, potentially the deep donor reported in [95], excitation from a relatively shallow acceptor level to the conduction band as in [96], or from the valence band to a donor level with an ionization energy of 0.2 eV [97]. To cause

the drop in current such a process either provides additional negative charges, enables partial breakdown by making a part of the structure conductive, or enhances lateral charge spread at a deep hetero interface. A explanation for the observations is described in detail in the following section.

5.3.2 Carbon donor excitation model

A donor level with an ionisation energy of 0.2 eV has been predicted for carbon doped GaN in [97]. But based on the discussion in [89] it is likely that the donor is overcompensated by an acceptor with ionisation energy of 0.9 eV. This donor/acceptor configuration can explain the observed behaviour of sample B, where the current drops significantly under illumination and substrate bias.

Figures 5.5 to 5.7 describe the charge carrier configurations and movements. Initially all donors are ionised. The electrons provided partially ionise the acceptor level causing the Fermi level to be pinned to the latter. The excitation from valence band to donor leaves a hole in the valence band and a neutralised donor. The donor will immediately ionise again, causing ionisation of an acceptor state. Without any substrate bias applied as illustrated in figure 5.5, the hole will recombine with an ionised acceptor reestablishing the initial state. This explains that no effect of illumination is observed at 0 V back bias. If a substrate bias is present (figure5.6), it will pull the free hole deeper into the structure while the additional negative charge remains on a fixed trap state. The resulting band diagram depicted in figure 5.7 is levelled out in the carbon doped GaN region causing stronger electric fields for the 2DEG than pure capacitive coupling would. This redistribution of charges fed by the 3.2 eV excitation has some analogies with the charge movement observed for sample A in chapter 4. But the ramp curve for sample B under illumination at 3.26 eV in figure 5.3 shows no lasting reduction. This is either due to hole injection from the 2DEG fully compensating the negative charges or due to the barrier at the hetero interface between strain relief section and buffer. In case of the latter the holes stay in the valence band of the buffer, accumulating at the interface and remain available for neutralisation of acceptors when the substrate bias is lowered again.

The same model for carbon donor / acceptor configuration can be used to explain the observations in both samples with the difference in behaviour being related to the presence of a hole leakage part at the top of the structure.

5.3.3 Vertical currents

When sample B was tested at high substrate voltages up to -600 V under illumination another effect was observed. Figure 5.8 shows the measurements. Under the higher electric field the light caused a current collapse that remained after application of bias. The vertical currents measured simultaneously at the substrate show a strong increase throughout the measurement. Problematic current collapse and breakdown conditions will be met at much lower voltages in case of the illumination. A redistribution of charges by ionising acceptors under applied field again is a good explanation for the observation.

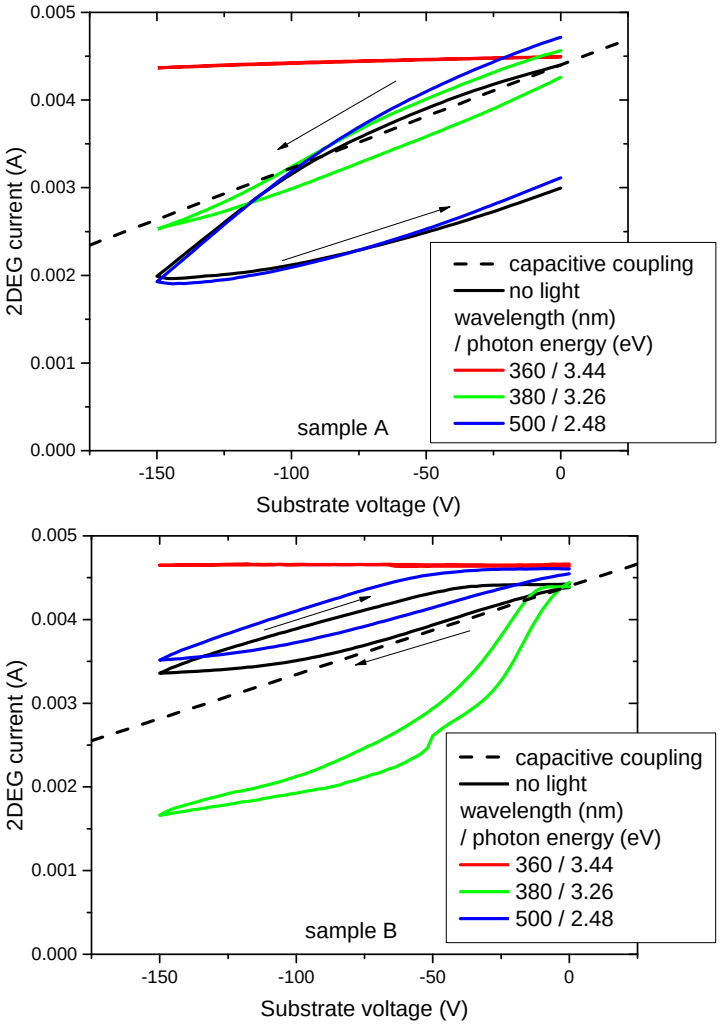

Figure 5.3: Back bias ramp curves at different wavelengths. Samples A and B. Ramp rate = 4 V/s, drain voltage = 1 V, measured at room temperature. Arrows indicate the direction for the unlit ramps.

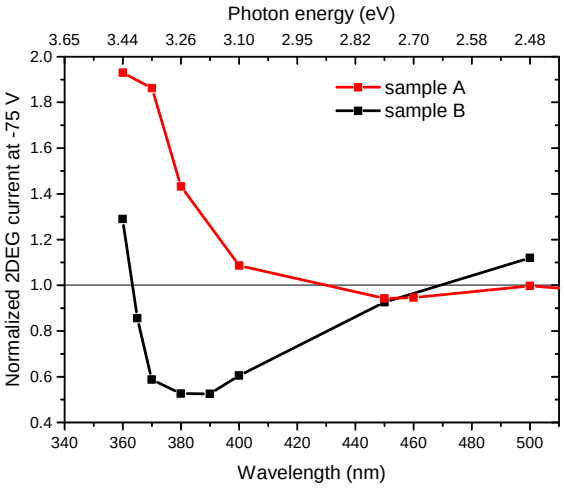

Figure 5.4: Photoionisation spectral response curves extracted at -75V back bias on the return ramp for the two samples. Normalised to the current measured without light.

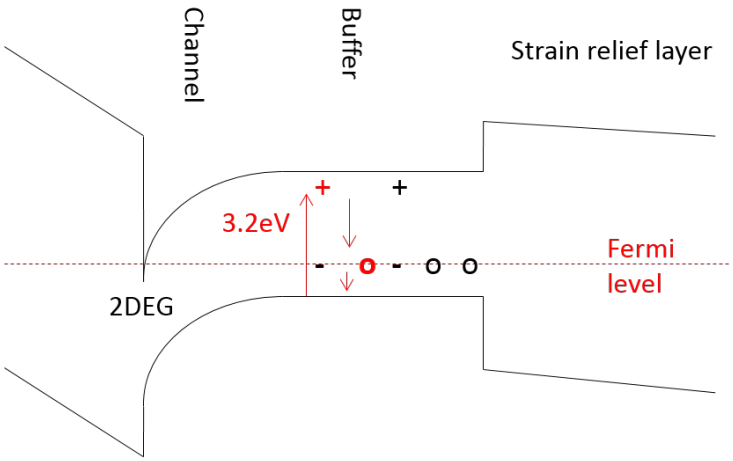

Figure 5.5: Schematic band diagram describing the valence band to donor transition at 3.2 eV without substrate bias. Plus signs represent positive charge (holes or ionized donors). Minuses are the equivalent negative charges (electrons or ionized acceptors). Circles are neutral states. Black symbols describe the initial state, red symbols the final state after change. The vertical arrows indicate excitation and emission processes. Without substrate bias the excited electron is lowered in energy by emission processes and eventually recombines with a hole in the valence band resulting in no remaining change in charge.

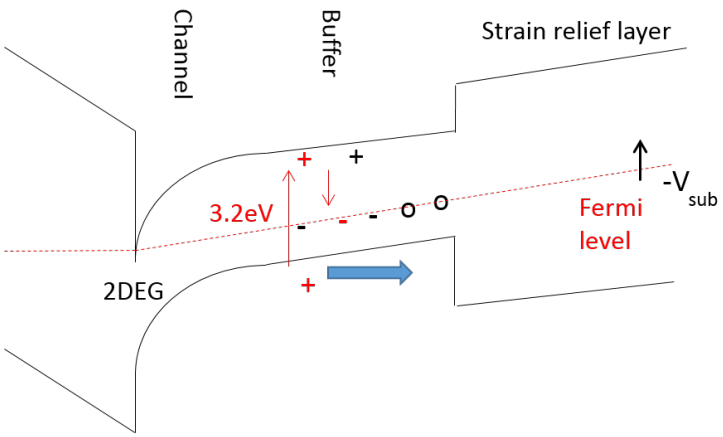

Figure 5.6: Schematic band diagram describing the proposed charge movement when substrate bias is applied involving a valence band to donor transition at 3.2 eV. The blue arrow indicates the movement of the hole created by the excitation which is pulled towards the substrate and strain relief layer.

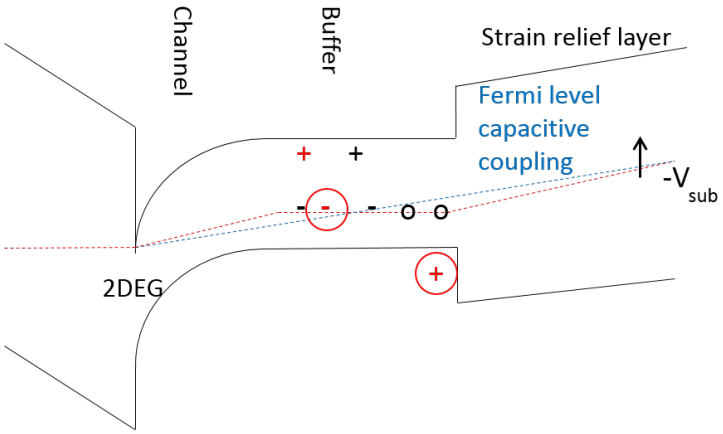

Figure 5.7: Schematic band diagram describing the state after charge redistribution. The charges in circles are a fixed ionised acceptor and corresponding hole in the valence band which have been divided by the substrate bias induced electric field. The resulting Fermi level is shown in comparison to what pure capacitive coupling suggests.

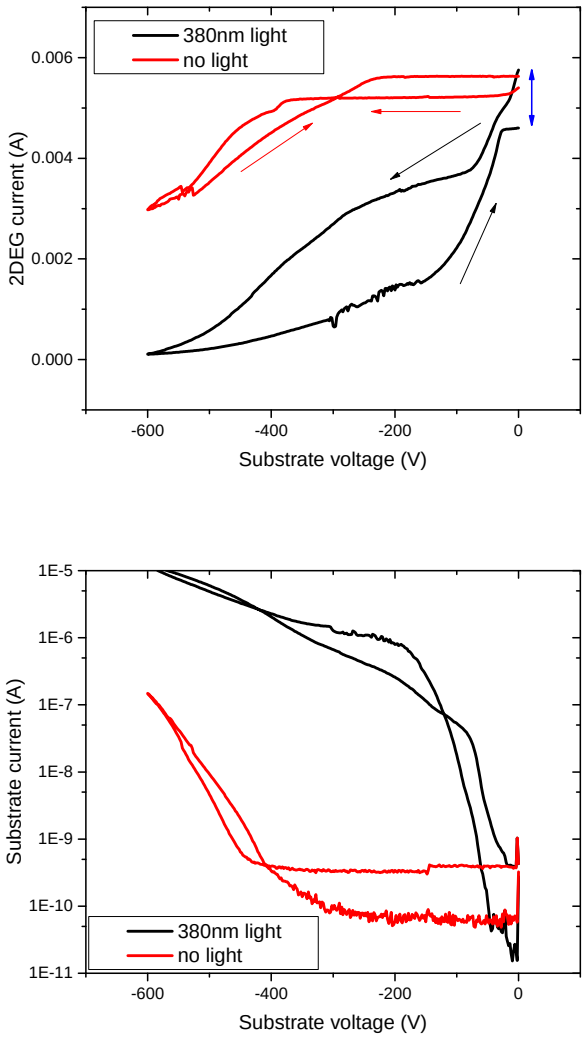

Figure 5.8: 2DEG and substrate currents measured during a substrate bias ramp to -600V with and without illumination on sample B.

5.4 Conclusion: Charge trapping under illumination in AlGaN/GaN on Si HFETs with Hetero Interfaces in Strain Relief Layer

Nominally very similar samples from different epitaxy and processing fabs show completely different behaviour in substrate bias ramp measurements. Sample A already introduced in the previous chapter showed severe current collapse rendering this device unsuitable for high voltage operation. Whereas sample B showed signs of positive charge storage which lead to reduced current collapse during substrate bias and no change in current after substrate bias which is the ideal behaviour making it a good candidate for a high voltage device. The findings illustrate the usefulness of the substrate bias ramping for identification of good or bad behaviour in this regard.

To further investigate the differences of the two samples experiments combining substrate bias ramping with illumination were performed. An excitation process was found to be present in sample B only which also had an impact on current reduction. Evidence for the process at 3.2 eV is neither available by photoionisation without back bias nor by back bias ramping without illumination for a current collapse free sample. This example shows how the combined methods provide additional information about the structure investigated.

A model was developed involving an excitation to a carbon related donor state that can explain the findings for sample B, based on the same carbon donor / acceptor configuration assumed for sample A in chapter 4. The findings mean that a hole leakage path present at the top of sample B and not sample A is responsible for the difference in behaviour.

Impact of light on breakdown and current collapse behaviour at higher substrate voltages was also observed for sample B in agreement with the models. Since the light intensity in the experimental setup was not significantly higher than under ambient light conditions, the findings have implications for real devices when those are meant to operate in an environment that is not completely dark. Performance reductions are therefore likely to occur under those circumstances.

The exact origin of the leakage path causing the difference between the two samples concerning current collapse could not be pinned down by the experiments shown here. Further experiments and additional samples are necessary to identify correlation to either growth or device processing. Epitaxy known to show current collapse and epitaxy known to be current collapse free should be processed in exactly the same way to rule out processing as the origin of current collapse. On the other hand processing variants tested on the same epitaxy can reveal the impact of processing. An experiment following the latter approach is presented in the following chapter. Also epitaxial variants with structural difference in the barrier part and processed the same way could be tested to find out more about leakage in the top part of typical HFET structures likely to be related to current collapse.

Chapter 6

Buffer doping and charge trapping in GaN on SiC HFETs

In this chapter GaN HFETs on SiC substrates are investigated. SiC substrates are commonly used for commercial RF HFET devices. Again the focus is on buffer related charge movement and trapping effects that can affect the device performance.

The observations in chapter 4 showed that current collapse can be related to carbon doping while in chapter 5 differences in current collapse behaviour were found to potentially stem from different processing of the devices. In both chapters Si substrates were used. To investigate if similar behaviour occurs in carbon containing GaN buffers on SiC substrates such samples are introduced here. Impact of variations in processing procedures are investigated in the first section. A relation between leakage behaviour and current collapse associated with buffer effects is revealed.

In the second section buffer doping profiles containing carbon, iron or both are compared. Substrate bias tests show signs of carbon dominating in all structures tested. Based on the findings a novel doping profile is proposed and tested in simulations for different structural scenarios showing promising characteristics.

The findings presented in section 6.1 have been published in [98].

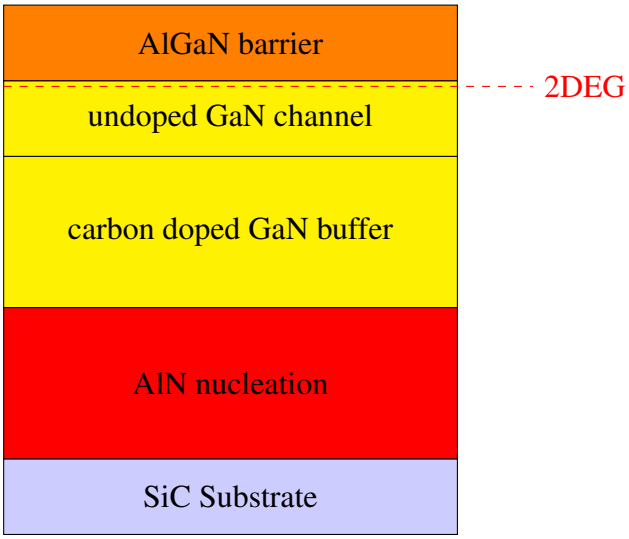

Figure 6.1: Epitaxial structure of GaN HFET on SiC substrate.

6.1 GaN on SiC HFET with carbon doped buffer and the impact of ohmic process

The morphology and impact on leakage currents of two different ohmic metal stacks for GaN based transistor devices is investigated. The results have implications for the performance and reliability of a GaN transistor device. A low temperature Ta based and a higher temperature anneal Ti based metallisation are compared. Morphology and leakage of the structures are tested. In addition to the leakage tests, back bias ramping experiments are performed to test impact on current collapse.

6.1.1 Epitaxial Structure, Device Structure and Morphological Details

The epitaxial layers, again grown at IQE in Cardiff, consist of a single hetero structure AlGaN/GaN HFET, typical of that used for RF applications, grown on n-type conducting SiC with an AlN nucleation layer. Normally semi-insulating substrates are used for RF GaN-on-SiC, but here we use a conducting substrate to measure vertical currents and enable substrate bias tests. The epitaxial structure of

the samples tested is depicted in figure 6.1. Total thickness of the epitaxial layers is $\sim 2\,\mu m$.

Both metallisations have been processed on pieces of the same epi-wafer at the University of Chalmers in Niklas Rorsman's group. Before contact formation a SiN passivation layer has been deposited by low pressure chemical vapour deposition. The metal stacks used are Ta/Al/Ta and Ti/Al/Ni/Au with thicknesses of 10/280/20nm and 20/110/40/40nm respectively. Both metallisations were deposited after a recess-etch through the passivation and part way through the AlGaN barrier. The Ta stack was annealed in a nitrogen atmosphere for $\sim$20 min with a maximum temperature of 600 °C. Whereas the Ti stack was annealed also in nitrogen for 30 s at 830 °C. Both metallisations showed ohmic behaviour. The contact resistances measured are 0.4 Ωmm for the Ta stack and 1.6 Ωmm for the Ti stack. The contact surface roughness is 101 nm and 268 nm root mean square for Ta and Ti stack respectively measured on similar areas of about 500 μm^2 via CCI at IQE. The formation of TiN protrusions that penetrate the upper epitaxial layers has been reported to occur during the annealing of the Ti contact [76] and is likely to cause localised low resistivity paths. In figure 6.2 TEM cross-section images of both metal stacks are depicted. The TEM analysis was done at the University of Bristol by Richard Webster. The inset of figure 6.2b shows a dark area within the epitaxial part is visible in a dark field image. Similar findings in [76] have been identified as TiN. In contrast no such area was observed for the Ta sample shown in figure 6.2b.

6.1.2 Impact of Ohmic Process

The commonly used metal stacks on GaN HFET epitaxial material for ohmic contact formation are Ti/Al based stacks like Ti/Al/Ni/Au, which need to be annealed at high temperatures of 800 °C and above [76]. Recently, Ta based approaches to develop alternative metallisation schemes have succeeded in achieving very reasonable contact resistances while annealing temperatures were kept low ($\sim$600 °C) resulting in a smoother contact surface and posing less thermal stress on all parts of the structure with a gold free metallisation [77]. The impact of a low temperature ohmic process in comparison to the conventional Ti

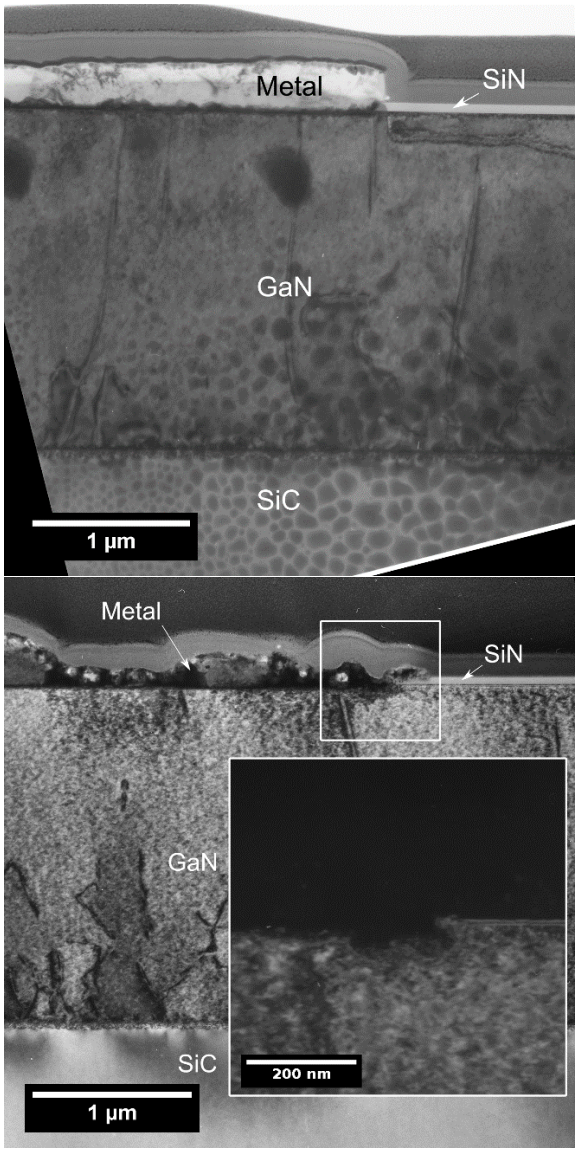

Figure 6.2: TEM cross sections of Ta based ohmic (a) and Ti based ohmic (b). The inset in (b) shows a magnified dark field image of the highlighted region.

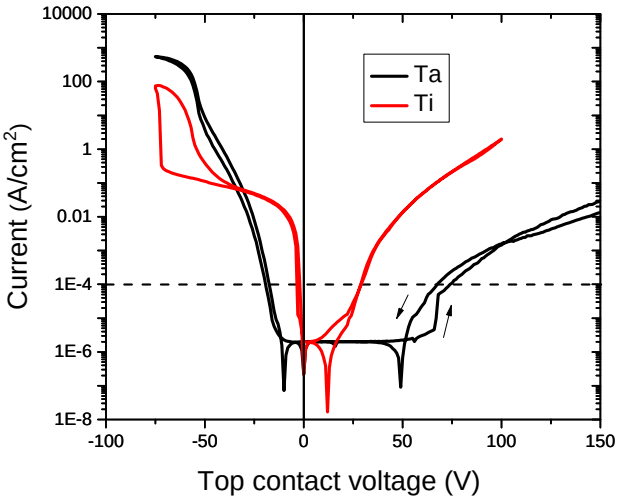

Figure 6.3: Absolute vertical currents. Both polarities. Substrate grounded. The dashed line indicates 0.1 mA/cm^2 current density for the rectangular contact of 100 µm $\times$ 70 µm size on a 104 µm $\times$ 74 µm mesa.

based one on lateral leakage currents and breakdown of GaN based HFET structures has been investigated in [99] for an InAlN/GaN double hetero structure on semi-insulating Si substrate showing superior lateral leakage and breakdown.

Here high and low temperature annealed stacks are compared and besides the lateral leakage vertical leakage is also investigated, which often defines the overall breakdown performance [100]. Back bias ramping experiments were performed to provide information on charging effects in the buffer region.

6.1.3 Leakage Currents Lateral and Vertical

Figure 6.3 shows the vertical currents measured for the different contact metallisations when biased with the substrate grounded. Asymmetric behaviour is observed in response to either positive or negative bias, related to effects at the 2DEG buffer interface. With a negative voltage on the top contact 2DEG electrons are injected into the buffer structure causing the difference in the onset of leakage. At positive voltages corresponding to typical device operation the vertical currents are generally lower than for negative voltages, but also a huge difference between the two

contacts of about three orders of magnitude can be seen. The high temperature process obviously leads to much stronger vertical leakage. The high leakage of the Ti contact is likely to be associated with the TiN protrusions and the rougher metal semiconductor interface compared to the much smoother Ta metal stack. The TiN protrusions allow electrons to penetrate into the epitaxial structure bringing charge carriers closer to areas of higher dislocation density that can act as leakage paths. Also the roughness of the surface could favour the formation of further dislocations underneath. Under a failure criterion of <0.1 mA/cm^2 the Ta sample can operate at up to 75 V before the limit is reached compared to about 25 V for the Ti sample as can be seen in figure 6.3.

In figure 6.4a the currents of a three terminal measurement are shown for the Ta based ohmic. Figure 6.5 describes the measurement setup. Two contacts isolated by a mesa etch are used. One contact is biased while substrate and the other contact are grounded with currents recorded at all terminals. Allowing to differentiate between lateral and vertical currents. The structures dimensions are similar to TLM structures but with the isolation between the ohmics.

For the Ta sample the lateral leakage current measured at the grounded top contact did not exceed 1 nA with all current flowing vertically between biased contact and substrate. In contrast, the Ti contact sample shown in figure 6.4b shows a significant lateral contribution to the leakage, apparent in the much higher current at the grounded top contact. Figure 6.6 gives a closer look at the voltage regime between 25 V and 60 V on a linear current scale. Up to $\sim$47 V lateral current between the top contacts is dominating the leakage in the Ti contact sample.

In contrast to the conventional Ti metallisation the Ta based ohmic completely suppresses lateral leakage that can hamper device performance. The experiments also demonstrate a significant reduction in vertical currents with the low temperature contacts. The TiN protrusions and high anneal temperature affecting buffer conductivity are potential cause of the leakage of the Ti based metal stack. The reduced lateral leakage as reported in [99] has been confirmed for the AlGaN/GaN on SiC structure.

6.1.4 Substrate bias ramps

Back bias ramp results for both metallisations are shown in figure 6.7. The black curve in figure 6.7 is representative for the Ta based ohmics where the results are very consistent between test structures distributed across the sample of 1 cm^2 total area. In contrast, different devices on the Ti based ohmic sample showed very different responses to the back bias. The red curves in figure 6.6 give the largest and smallest current collapse observed with Ti based ohmics. The current collapse is defined as the loss in current after returning to zero applied substrate bias. The Ta devices show a current collapse of $\sim$20 %, whereas in the Ti devices the current collapse varies between 10 and 20 %. The reduced current collapse in some Ti devices can be explained by the presence of a leakage path between 2DEG and buffer in these devices enabling neutralization of trapped buffer charges namely ionised acceptors [101]. Hence, leakage associated with the Ti based ohmic can in some circumstances have a positive effect on the current collapse.

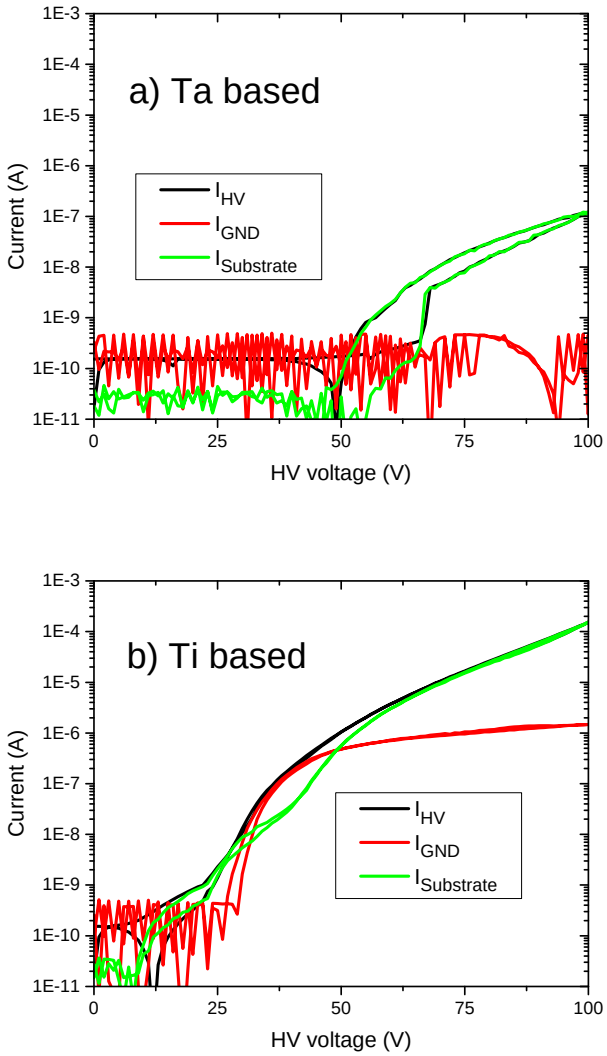

Figure 6.4: Absolute vertical and lateral leakage for Ta (a) and Ti (b) based contacts. Both were probed on mesa isolated contacts of 100 µm × 70 µm area with 50 µm distance between the 100 µm edges.

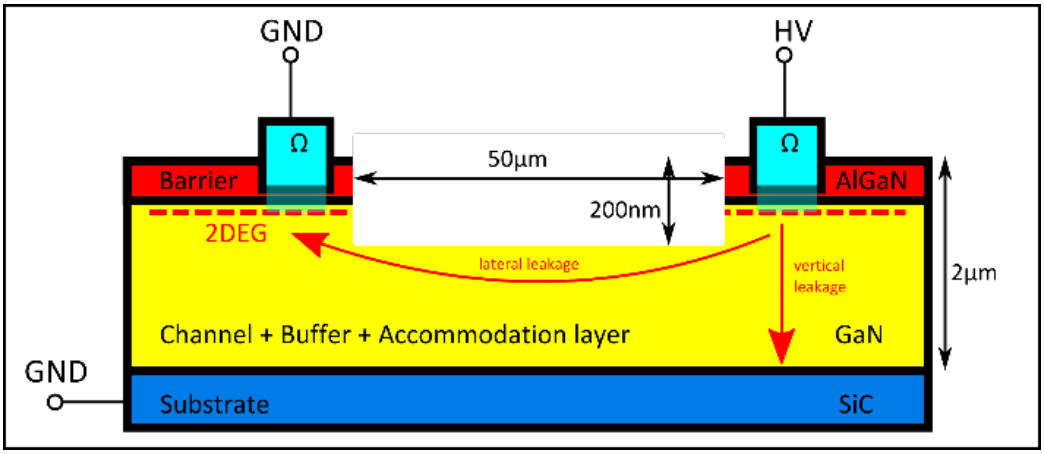

Figure 6.5: Experimental setup.

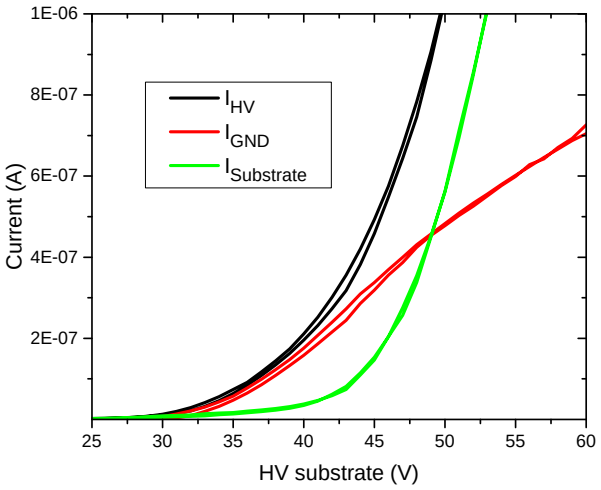

Figure 6.6: Close up of leakage currents of Ti contacts on a linear scale showing the lateral leakage exceeding vertical leakage for up to 47 V bias.

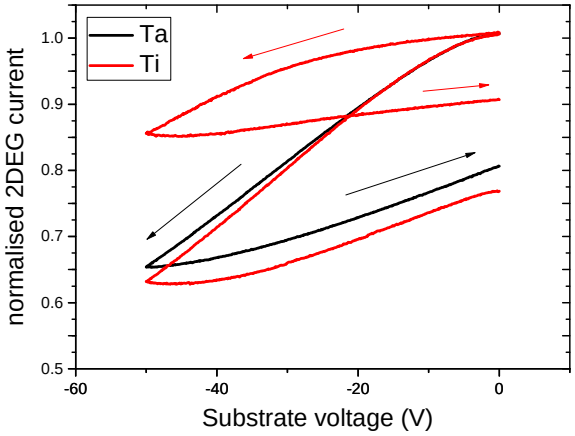

Figure 6.7: Back bias ramps measured on simple TLM structures with a 50 µm gap and 100 µm width. The red curves represent strongest and least measured current collapse on the Ti sample. Ramp rate: 0.5 V/s.

6.2 Doping profile variations

Different doping profiles in the GaN buffer region are tested which contain different concentrations of carbon and iron. How the concentration relation of those dopants affects current collapse is investigated.

Carbon concentrations of $\sim 10^{19}\,\mathrm{cm}^{-2}$ representing high carbon doping, $\sim 10^{18}\,\mathrm{cm}^{-2}$ for medium and $\sim 10^{17}\,\mathrm{cm}^{-2}$ low carbon doping. The iron doping profile used was aimed to produce a maximum concentration of $\sim 10^{18}\,\mathrm{cm}^{-2}$. Table 6.1 explains the different configurations. Substrate bias ramp experiments have been performed to investigate differences in current collapse behaviour. As can be deduced from the curves shown in figure 6.8 all samples showed current collapse after negative substrate bias. The behaviour observed is similar to what has been clearly linked to carbon in the buffer. Surprisingly no substantial difference in current collapse behaviour was found for the iron doped samples. A detailed analysis of the atomic composition of the layers for sample C4 via SIMS is shown in figure 6.9. The carbon concentration in the channel region between AlGaN barrier and highly carbon doped buffer shows a carbon concentration of $1 \times 10^{17}\,\mathrm{cm}^{-3}$ which for the set of grown samples corresponds to the low carbon concentration mentioned in table 6.1. Thus, apparently all samples still contain a fair amount of carbon in every layer and in particular in the buffer. In the iron doped samples a configuration with two acceptors, a carbon and an iron related one, as described in section 2.1.5, is therefore formed. Since no intentional compensation is present the result is that carbon will dominate the characteristics also in iron containing layers, leaving the Fe acceptor in neutral state [52, 79]. This explains the observed current collapse behaviour which is related to carbon. To prevent carbon from

Table 6.1: Doping profiles of GaN on SiC HFET structures.

sample name	sample ID	carbon concentration	iron concentration
C1	Chalmers B	medium	medium
C2	Chalmers E	low	no iron
C3	Chalmers F	low	medium
C4	Chalmers G	high	medium

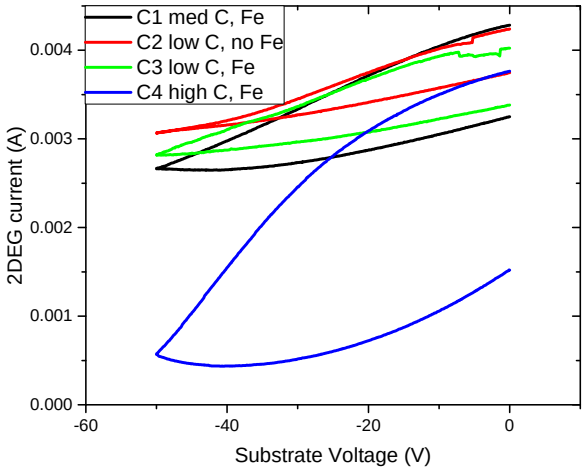

Figure 6.8: Back bias ramps of samples C1,C2,C3 and C4. All samples show current collapse after negative substrate bias with sample C4 showing strongest current reduction.

dominating the buffer region more complex doping profiles are needed. In the next section simulations of such a structure are presented.

6.2.1 Doping profile simulations

As described in section 2.1.5 and experimentally confirmed in the previous section the effectiveness of iron doping in MOCVD grown GaN buffers, which inevitable contain some carbon, is questionable. The memory effect causing the iron doping profile to exponentially drop after turning off the dopant further increases the complexity of the situation [102]. Figure 6.10 describes the situation. Carbon defines the Fermi level in the complete buffer.

A structure that circumvents the issues that occur is proposed, described and tested in simulations. For moving the Fermi level to the iron acceptor energy any carbon acceptor concentration needs to be compensated by a donor such as Si. Figure 6.11 illustrates the case where a Si compensation donor is used with concentration higher than carbon but lower than Fe. The memory effect when doping with iron means that iron incorporation cannot be stopped immediately.

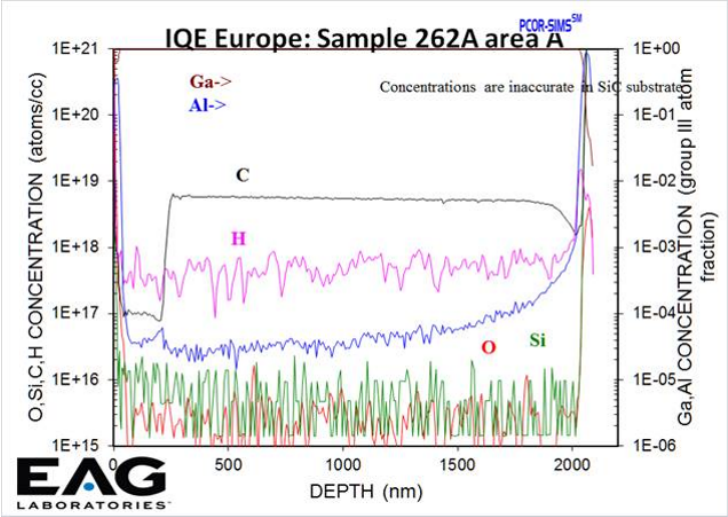

Figure 6.9: SIMS profiles of GaNonSiC sample C4. Carbon level in the channel layer: $1 \times 10^{17}\,\mathrm{cm}^{-3}$.

Table 6.2: Doping profile configurations of GaN on SiC HFET simulations.

name	contact to buffer hole leak	Si donor in Fe layer	SRL layer
S1	no	yes	AlN HI
S2	yes	yes	AlN HI
S3	yes	no	AlN HI
S4	no	no	AlN HI
S5	no	yes	graded AlGaN

Instead, the iron incorporation falls exponentially during growth after the dopant's gas source has been turned off. The iron concentration therefore will inevitably fall below the donor concentration necessary to compensate the carbon at some point in the HFET structure. The result is Fermi level pinning to the Si donor and a conductive n-type layer which will enable punch-through effects.

To prevent the occurrence of the highly conductive layer the compensation donor can be turned off before the iron concentration falls below. Turning off the compensation though creates a carbon dominated region between GaN:Fe and 2DEG. The resulting concentrations can be seen in figure 6.12 for a structure in which Fe and Si doping are turned off simultaneously. Structures corresponding to the configuration shown in figures 6.12 and 6.10 are simulated and tested for different leakage and strain relief scenarios, see table 6.2.

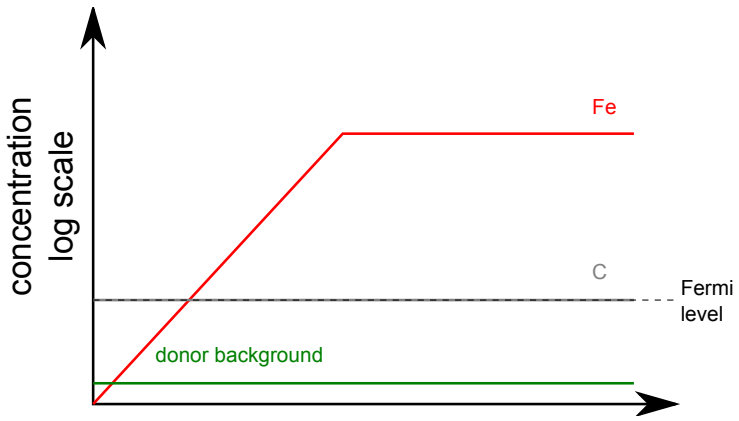

Figure 6.10: Buffer doping profile dominated by carbon. The Fermi level is defined by the carbon acceptor

In the simulations the concentrations of iron and silicon which provides the compensation replicate a growth in which both are turned off simultaneously. Only the layer that is doped with iron at highest concentration is dominated by iron if a compensation is active and the layer in which the iron concentration falls is dominated by the carbon acceptor, see figure 6.12. A AlN/GaN hetero interface is simulated at the bottom of the GaN buffer in the first scenarios, i.e. the strain relief section is pure AlN. Hole leakage from top contact to 2DEG is simulated by a heavily doped p-type region reaching from the contacts to the 2DEG. This leakage is turned on and off. The second variation is in moving the compensational Si donor concentration below and above the carbon acceptor concentration resulting in the Fermi level to move to either carbon or iron acceptor level [103] in the high Fe concentration region, i.e. switching between the doping described in figures 6.12 and 6.10. Variants S1 to S4 are formed that way. A fifth simulation S5 is set up with a graded AlGaN strain relief layer similar to the structure in chapter 4 but with added Fe and Si doping. Carbon, iron and silicon related acceptor and donor trap concentrations are chosen as 1, 5 and 2 $\times 10^{18}\,\mathrm{cm}^{-3}$ when the compensation is active in the iron dominated layer. Other parameters are similar to those mentioned in chapter 4.

A band diagram of the structure with graded strain relief layer is shown in figure 6.13. The Fermi level sits on the carbon acceptor energy level in one part of the buffer and on the iron acceptor level in the other part of the buffer.

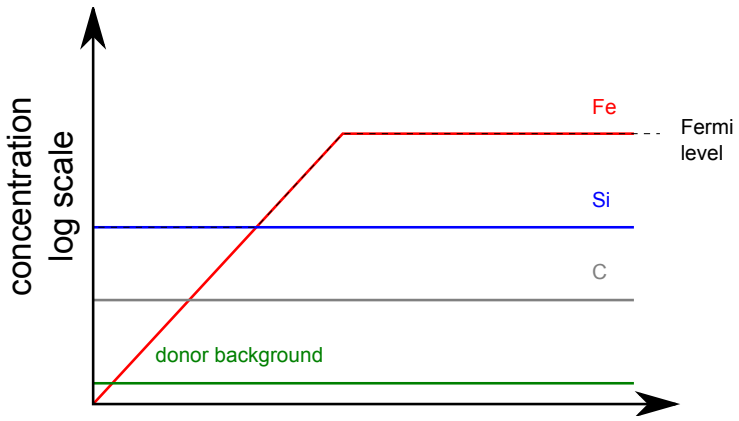

Figure 6.11: Buffer doping profile with Si donor for compensation of carbon acceptor. The Fermi level is defined by the Fe acceptor or Si donor depending on which one has higher concentration.

Back bias measurements were simulated and the results are shown in figure 6.14. Simulation S4 with no hole leakage at the top and no compensation of the Fe acceptor shows the expected current collapse behaviour similar to observations in chapter 4. Simulations S2 and S3 with hole leakage at the top are free of current collapse in agreement with the explanation given for the substrate bias behaviour of sample B in chapter 5. Holes are injected into the buffer screening the 2DEG region from the substrate bias.

Simulation S1 is different to S4 only because the compensation in the iron layer is active. Simulation S5 is similar to the simulation from chapter 4 with the main difference being the iron and silicon configurations. Thus, both S1 and S5 differ from simulations showing current collapse only in the iron, silicon doping configuration. Figure 6.14 shows that S1 and S5 do not suffer from current collapse after negative substrate bias. The addition of an iron acceptor dominated layer below the carbon dominated layer in the buffer apparently prevented the current collapse even without hole leakage in the simulations. The reason for this behaviour can be observed in figure 6.15. A positive space charge builds up at the bottom end of the iron dominated layer which screens the substrate bias effect. The space charge forms by neutralisation of ionised iron acceptors while the carbon acceptors remain ionised keeping the Fermi level in the insulating regime between the acceptor levels of 0.9 and 2.7 eV above the valence band. The neg-

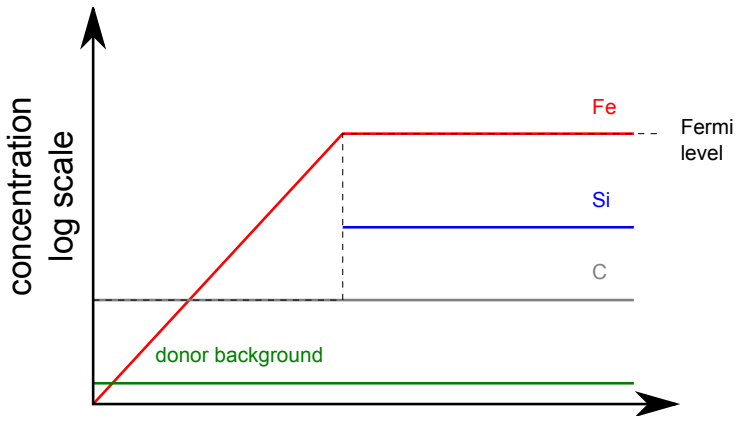

Figure 6.12: Buffer doping profile dominated by Fe on the right side representing the deeper part of the buffer and carbon on the left hand side. The Fermi level is defined by the iron and carbon acceptor.

ative charges that become available by the neutralisation of iron acceptors are moved towards the 2DEG. At low voltages they ionise carbon acceptors in the buffer layer dominated by carbon causing a current reduction (see figure 6.14) this effect though saturates at higher electric fields and when most acceptors are already ionised. Then negative charges are moved into the 2DEG leaving a large net positive charge in the iron dominated part of the buffer which is able to prevent current collapse.

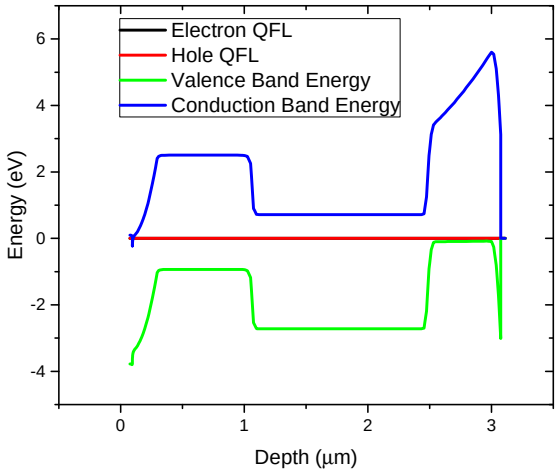

Figure 6.13: Band diagram of simulation S5.

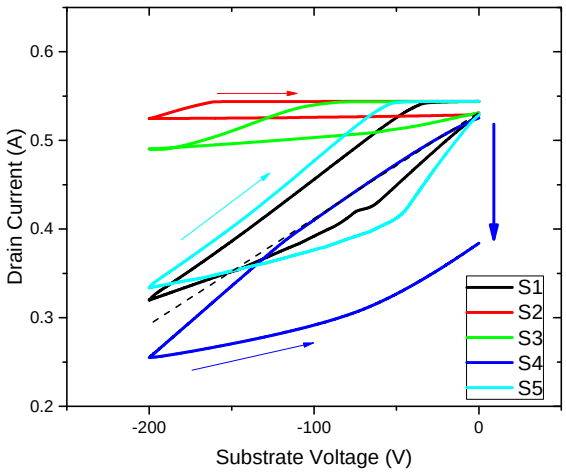

Figure 6.14: Substrate bias ramps of the simulations S1 to S5. Severe current collapse is only present in simulation S4.

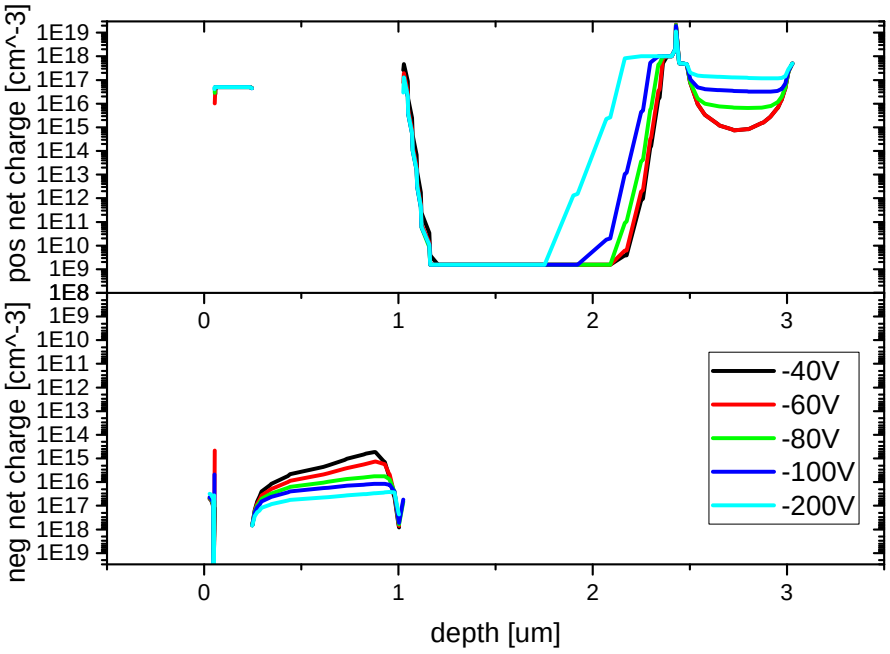

Figure 6.15: Net charge concentration profile of simulation S1 for different substrate biases.

6.3 Conclusion: Buffer doping and charge trapping in GaN on SiC HFETs

Low and high anneal temperature ohmic metal processes for GaN based transistors have been tested for buffer leakage. The results, for both vertical and lateral leakage, suggest great improvements in maximum achievable voltage in a typical RF structure using the low temperature process. Higher power at high frequencies will be achievable with such a contact compared to the conventional process assuming that RF performance is not affected by potentially increased buffer related current collapse. Similar effects are expected for GaN-on-Si power devices, but remain to be tested.

Substrate bias ramp experiments with GaN on SiC HFET structures with different doping profiles all showed behaviour associated with carbon. Apparently even iron doped buffers were dominated by the carbon inevitably present in those layers.

A structure that enables the iron related acceptor to dominate the carbon in parts of the buffer was predicted and tested in simulations. The proposed doping profile promises to prevent current collapse without the need of a hole leakage path through the channel region. The results are expected to be valid for different substrates and should mitigate current collapse also with low leakage ohmics. Experiments to validate the predictions are needed but could not be performed within the time frame of this project.

Chapter 7

Conclusion and Outlook

Buffer charging effects in GaN-based transistors have been investigated. Most experiments were performed at the centre for device thermography and reliability at the University of Bristol. The epitaxial material was specified and grown by the GaN team at IQE Europe in Cardiff which consisted of 3, later 4, people including the author of this work. Buffer doping and details of the epitaxial structure could be linked to the current collapse behaviour. Models were presented which explain the behaviour and some experiments could be replicated in simulations revealing details on position and movement of charges.

A structure was grown and processed to investigate the impact of carbon doping in the buffer. The structure was later referred to as sample A. It was tested with substrate bias ramping. Evidence for current collapse was observed and linked to the carbon doping. Precise simulation of the experiment was possible allowing a detailed look into charge positions and movement. The assumed doping levels were validated that way. What has been observed will inevitably lead to severe current collapse under realistic conditions for a power device build from the structure. The results show that apparently no leakage at the top of the epitaxial layer structure is present in this sample. The charge distribution in the carbon doped layer also means that such a layer reduces the vertical breakdown capabilities of the structures rather than increasing it. Thickness of such a layer therefore should be kept low for high voltage applications.

Another sample was introduced in chapter 5. This sample B was compared to sample A from the previous chapter and very similar 2DEG properties were measured. In substrate bias tests though very different behaviour was observed suggesting that sample B would not suffer from the severe current collapse. The findings can be explained by hole leakage present in the top part of sample B but not in sample A. Tests under illumination were performed to see if excitation happens under substrate bias and again different behaviour was observed for the samples. The reduction that certain illumination provoked on sample B only could be explained by an excitation for which no evidence is available with substrate bias only or illumination without substrate bias. The proposed trap configuration that explains the observations confirms that carbon is incorporated in a similar way in both samples but hole leakage at the top makes the difference. Vertical leakage under illumination tests validate these predictions. Potential origin of the different current collapse behaviour for the two samples are growth conditions affecting epitaxial structure or processing procedures affecting ohmic and gate metal contact structure.

In chapter 6 GaN on SiC structures were investigated. The impact of different ohmic contact processing procedures are tested. Also different structures with doping profiles containing both carbon and iron are tested and some new structures are proposed based on the findings and tested in simulations. A Ta based low anneal temperature process was compared to the conventional Ti based processing approach. Huge leakage advantages were observed for the Ta process which should enable devices with higher voltage at high frequencies. The conventional Ti based contact though showed some evidence for hole leakage that prevented current collapse effects but uniformity was not great for the sample. The doping profiles tested all showed substrate bias ramp behaviour that was clearly linked to carbon doping in chapter 4. Apparently even the iron doped samples were dominated by carbon which cannot be fully avoided in MOCVD growth. To circumvent the carbon dominance in iron doped layers a structure was proposed including C, Fe and Si doping. Simulations of this structure show very promising characteristics that could enable current collapse prevention while using a non leaky contact leading to better overall device performance.

The presented results have implications for commercial production of GaN-based transistors. The carbon doped buffer layer which is incorporated for prevention of punch-through should be kept reasonable thin to reduce current collapse and also to not lower the breakdown voltage. This is important for structures with no top leakage path for holes in particular. But also if hole leakage is possible and can be controlled in a structure premature breakdown can occur under illumination. Pinning the Fermi level at the deep iron acceptor state to utilise its great potential for insulating buffer structures is possible only with doping profiles that consider and manage the carbon levels present. For a real structure grown by MOCVD that requires a novel doping profile involving three dopants.

The origin of hole leakage at the top part of the structure could not be identified fully in this work. A dependency on the ohmic process was observed. Relation to epitaxial growth and/or other processing steps though could also have an influence. To identify influences further experiments are needed in which all differences during the production are eliminated step by step starting with samples that do and do not show current collapse. The C, Fe, Si doped structure proposed in chapter 6 could prevent current collapse without the need of a hole leakage path and should work with a low leakage ohmic combining all benefits but needs to be tested in a real device.

Appendix A

Publications

The following publications and conference contributions are closely related to this work:

- Pooth, A., Uren, M.J., Cäsar, M., Martin, T. and Kuball, M. "Charge movement in a GaN-based hetero-structure field effect transistor structure with carbon doped buffer under applied substrate bias." *Journal of Applied Physics* 118.21 (2015): 215701.
- Pooth, A., Bergsten, J., Rorsman, N., Hirshy, H., Perks, R., Tasker, P., Martin, T., Webster, R.F., Cherns, D., Uren, M.J. and Kuball, M. "Morphological and electrical comparison of Ti and Ta based ohmic contacts for AlGaN/GaN-on-SiC HFETs." *Microelectronics Reliability* 68 (2017): 2-4.
- Pooth, A., Martin, T., Cäsar, M., Uren, M.J. and Kuball, M. "Back biasing AlGaN/GaN HFETs to characterise epitaxial layer structures." UKNC Winter Meeting 2015, Nottingham.
- Pooth, A., Martin, T., Uren, M.J. and Kuball, M. "Buffer Investigations on Substrate Biased AlGaN/GaN HFETs: An Overview." UKNC Winter Meeting 2016, Cambridge.

- Pooth, A., Bergsten, J., Rorsman, N., Hirshy, H., Perks, R., Tasker, P., Martin, T., Uren, M.J. and Kuball, M. "Impact of ohmic process on vertical currents in AlGaN/GaN-on-SiC HFETs." ROCS Workshop 2016, Miami.

- Pooth, A., Martin, T., Uren, M.J., Laboutin, O., Lo, C.-F. and Kuball, M. "Back Bias Ramping and Photoionization Spectroscopy Analysis of GaN-on-Si HFETs." CSManTech 2016, Miami.

- Pooth, A., Martin, T., Uren, M.J., Bergsten, J., Rorsman, N. and Kuball, M. "Current collapse and charge movement in buffer structures of GaN-based transistors" 8th Wide Bandgap Semiconductors and Components Workshop 2016, Harwell, UK.

Appendix B

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Appendix C

List of Abbreviations

GaN	Gallium nitride
LED	Light emitting diode
HFET	Hetero-structure field effect transistor
2DEG	Two dimensional electron gas
UoB	University of Bristol
KTP	Knowledge transfer partnership
RT	Room temperature
2DHG	Two dimensional hole gas
uid	Unintentionally doped
MBE	Molecular beam epitaxy
MOCVD	Metal organic chemical vapour-phase deposition
CC	Current collapse
TCAD	Technical computer aided design
TMG	Trimethyl gallium
TMA	Trimethyl aluminium
PT	Punch through
AFM	Atomic force microscope
TEM	Transmission electron microscopy
CCI	Coherent correlation interferometry
QFL	Quasi Fermi level
SRL	Strain relief layer

TLM	Transfer length measurement
SIMS	Secondary ion mass spectrometry