THE UNIVERSITY OF SHEFFIELD

Current Limiting Devices for Short-Circuit Protection of DC Systems in Aerospace Applications

By

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Abstract

The use of DC systems to power high-power loads offers many advantages over AC in terms of efficiency and flexibility. Due to the increasing demand for electric power in aircrafts, the need for wider adoption of DC-based networks has been growing. This demand for higher power has originated from various efforts to electrify aircrafts ranging from replacing some of the mechanical components of jet engines with lighter electrical alternatives up to completely replacing jet engines with electric propulsors. Most of these efforts have been experimental, and no electric or "more-electric" aircrafts are commercially available as of the writing of this thesis. One of the main challenges hindering wider adoption of DC-based networks in aircraft systems is addressing concerns pertaining to system reliability. These concerns are emphasized by the lack of detailed analyses of possible fault scenarios and appropriate technologies for fault protection. This thesis aims to address these concerns by first presenting detailed analyses of the most severe fault scenario in AC/DC power converters, which are common components in DC-based power systems used to interface with AC networks or electric machines. Then, using the information provided by the analyses, current limiting devices are developed for fault protection. These are unique devices which take advantage of recent developments in Silicon Carbide materials that have produced Junction Field Effect Transistors (JFETs) with significantly higher performance than their Silicon counterparts. The resistance of the JFET is varied with the magnitude of current so that the circuit experiences the most amount of resistance under a fault condition and the least amount of resistance under nominal conditions. Two circuit configurations are presented one having the least complexity (maximum reliability) and one which is more complex but offers significant performance benefits.

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Chapter 2:

Symbol	Definition	Unit
A	Conductor cross-sectional area	m^2
A_n	Initial conditions constants, where *n = 1, 2, 3…*	-
C	Capacitance	F
C_i	Capacitance of Foster thermal network's i^{th} branch, where *i = 1, 2, 3, …*	F
D	Distance between two cables	m
ESL	Equivalent series inductance	H
ESR	Equivalent series resistance	Ω
I_0	Initial current	A
I_{0x}	Initial current of phase *x*, where *x = a, b,* or *c*	A
I_1	Initial current at diodes conducting stage	A
i_{Cap0}	Initial capacitor branch's current	A
i_{CB}	Capacitor branch current during diodes conducting stage	A
i_{DB}	Current during diodes blocking stage	A
i_{DL}	Current through the lower diodes of a converter's leg (D2, D4, and D6)	A

i_{Dn}	Current of diode *n*	A
i_{DU}	Current through the upper diodes of a converter's leg (D1, D3, and D5)	A
i_{FB}	Fault branch current during diodes conducting stage	A
I_S	Diode saturation current	A
i_{S0}	Initial rectified AC side current	A
I_{t_0x}	Initial current of phase *x* at t_0, where *x = a, b,* or *c*	A
i_x	Current of phase *x*, where *x = a, b,* or *c*	A
I_{xRMS}	Root-mean-square current of phase x, where *x = a, b,* or *c*	A
j	Imaginary $j = \sqrt{-1}$	-
L	Cable length	m
L_{self}	Cable self-inductance	H
L_{short}	Inductance of the short-circuit path	H
L_{total}	Loop inductance	H
M	Mutual inductance	H
n	Diode emission coefficient	-
P	Active or real power	W
P_{nom}	Nominal real output power	W
Q	Reactive or imaginary power	Var
R	Electrical resistance	Ω
R_i	Resistance of Foster thermal network's ith branch, where *i = 1, 2, 3, …*	Ω
R_S	Diode equivalent series resistance	Ω
R_{short}	Resistance of the short-circuit path	Ω
S	Apparent power	VA
t	Time	s
t_0	Time at which DC side voltage is zero	s

t_b	Diodes blocking to conducting time boundary	s
V_0	Initial Voltage	V
V_1	Initial voltage at diodes conducting stage	V
V_D	Diode voltage drop	V
V_D'	Diode voltage accounting for series resistance	V
V_{DC}	DC side voltage	V
V_j	Diode equivalent forward voltage	V
V_m	Peak line to neutral voltage	V
V_T	Diode thermal voltage (25.7mV at 25°C)	V
v_x	Voltage of phase *x*, where *x = a, b,* or *c*	V
V_{xRMS}	Root-mean-squared voltage of phase *x*, where *x = a, b,* or	V
Z	Line impedance	Ω
$Z_{th(J-c)}$	Junction to case thermal impedance	°C/W
α	Phase angle of v_a at which the fault occurs	rad
β	Damping factor	-
β_{xn}	Commutation state coefficient, where *x = a, b,* or *c* and *n = 1, 2, 3*..	-
ΔT_j	Junction temperature rise	°C
μ	Magnetic permeability of material	H/m
ρ	Electrical resistivity	Ω.m
ϕ	Impedance phase shift	rad
ϕ_0	Impedance phase shift prior to fault instance	rad
ω	Fundamental frequency	rad/s
ω_r	Ringing frequency	rad/s
ω_o	Resonance frequency	rad/s

Chapter 4:

Symbol	Definition	Unit
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j	Imaginary $j = \sqrt{-1}$	-

L	Cable length	m
L_{self}	Cable self-inductance	H
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L_{total}	Loop inductance	H
M	Mutual inductance	H
n	Diode emission coefficient	-
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R_i	Resistance of Foster thermal network's ith branch, where *i = 1, 2, 3, …*	Ω
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ϕ_0	Impedance phase shift prior to fault instance	rad
ω	Fundamental frequency	rad/s
ω_r	Ringing frequency	rad/s
ω_o	Resonance frequency	rad/s

Chapter 1: Introduction

This chapter is organized as follows: in the first section, factors that have historically limited the use of DC-based power systems are discussed. This section also includes a review of recent technology developments which have eliminated those factors. In the second section, the benefits of using DC networks are reviewed. In the third section, the use of DC in power systems of modern aircrafts is described. In the fourth and fifth sections, challenges hindering wider adoption of DC-based power systems for aircrafts are presented. In the sixth section, an outline of this thesis is presented. Finally, in the seventh section, a list of peer-reviewed publications which have resulted from this work is provided.

1.1. The Uprising of DC: Historical Background and Technology Influence

Although most power systems today use AC to power heavy loads instead of DC, there has been an old and ongoing debate on the benefits and shortcomings of each. This debate goes back to the days of Edison and Tesla, who each advocated their preferred systems. It is obvious that Tesla, whose AC system has been the most commonly used had won. However, many arguments that resulted in the adoption of his system are no longer valid, and DC is now being widely considered in many high-power applications.

Previously, the lack of techniques for stepping up generated DC voltages for transmission required that generation occur close to the loads, so that power losses in transmission was minimized. The noise and pollution from generation made this impractical. It also meant that power had to be generated and transmitted at the same low voltage used by the loads, or slightly higher to account for voltage drop in transmission, because DC voltages could not be easily stepped up or down. This resulted in the distribution lines having to be made of thick and expensive wires to handle the large current with minimal losses, which was another important argument against DC. In addition, the lack of methods to convert electricity from AC to DC and vice versa meant that power had to be generated in DC and only DC loads could be used. This was problematic since DC motors and generators required brushes to commutate the current, which restricted their reliability, lifespan, and maximum speeds [1].

With modern power electronics, DC voltages can be stepped up as high as desired, resulting in more efficient power transmission with thinner cables than those used in AC. DC voltages of

600kV are being considered for new installations, compared to the typical 400kV AC transmission voltage [2]. Nowadays, power can also be efficiently converted from DC to AC and vice versa to accommodate different requirements of loads, sources, and auxiliaries. So that power can be generated in AC using synchronous generators or DC from solar arrays, combined and converted to High Voltage DC (HVDC) for transmission, then back to AC at the loads. It may also be advantageous to directly deliver DC power to loads instead of AC [3]. This is because most loads nowadays can more efficiently and easily be powered using DC.

At the times of Edison and Tesla, the most power consuming loads were AC motors, which thanks to modern power electronics can now be more efficiently powered with DC using motor drivers. Many other loads can more easily and efficiently be powered with DC without conversion, like modern electronics, LED lighting, and electric vehicles. Likewise, the sources of electricity have changed: a large portion of power is now generated from renewable energy sources, such as solar and wind, which can more easily be interfaced to DC networks. Furthermore, modern distribution networks are likely to contain energy storage devices, such as batteries and supercapacitors, which can be connected to DC networks without the need for inverters, rectifiers, or synchronization.

1.2. Advantages and Shortcomings of DC-based Power System Architectures

One of the key advantages of DC networks is that for the same conductor size DC power transmission is typically more efficient than AC. This is partially due to the absence of skin effect, which results in an increase of transmission lines resistances in AC, as current is constrained to the outer portions of the conductors. This effect can be minimized by using cable laminations or twisted bundles of thinner isolated conductors (litz wires) [4], at the expense of higher monetary cost. In addition, AC lines must typically carry both active (useful) power and reactive (useless) power, while DC lines naturally only carry active power. Therefore, there are no power losses due to the transmission of reactive power in DC systems, which can be substantial in AC. In addition to the improved transmission efficiency, cables used in DC networks require lower insulation voltages for the same power ratings. Transmission cables are rated based on the highest voltages their dielectric materials can isolate, which is the sinusoidal peak voltage in AC and the average voltage in DC. However, power transferred is proportional to the Root Mean Square (RMS) values,

which is 0.707 of the peak value in AC and the same DC voltage in DC. Therefore, a cable rated for certain voltage can carry around 1.4 the AC power, if used in a DC network.

Despite the preceding advantages, the use of DC networks is not always desired, especially when considering the monetary cost and difficulty of protection. Due to the high cost of power conversion and control equipment required, it is only economically viable to use DC for long distance power transmission. This distance is typically around 400-600km for overhead lines and 30-40km for cable lines [2]. The use of DC below these lengths is not economical because the cost savings from increased efficiency does not make up for the higher equipment costs. A more serious problem with DC networks is the difficulty of protection. Unlike AC power, DC power does not periodically go to zero, which means that an arc resulting from breaking a DC circuit is not eventually extinguished by a zero crossing, like in AC. Instead, if not extinguished by other means, like gases or liquids, the arc is maintained in the circuit. This can result in a fire hazard and damage to the contacts of the breakers. Thus, DC systems require special power controllers like Solid-State Circuit Breakers (SSCBs) for protection.

1.3. DC in Aircrafts Power Systems

Hybrid aircrafts, like the Boeing 777, include both AC and DC distribution networks, as shown in Figure 1.1 below. Under normal operation conditions, AC power is sourced from the main engines of the aircraft (left and right Integrated Drive Generators (IDGs)), external ground power, or Auxiliary Power Unit (APU) typically located in the tail of the aircraft. This 115VAC power is then rectified using Transformer Rectifier Units (TRUs) to generate 28V DC power, which is used to interface with the onboard batteries and power the avionic systems. Some aircrafts also include Ramp Air Turbines (RATs) driven by engine bleed air and backup generators/converters that assist the batteries and APUs in case of emergency.

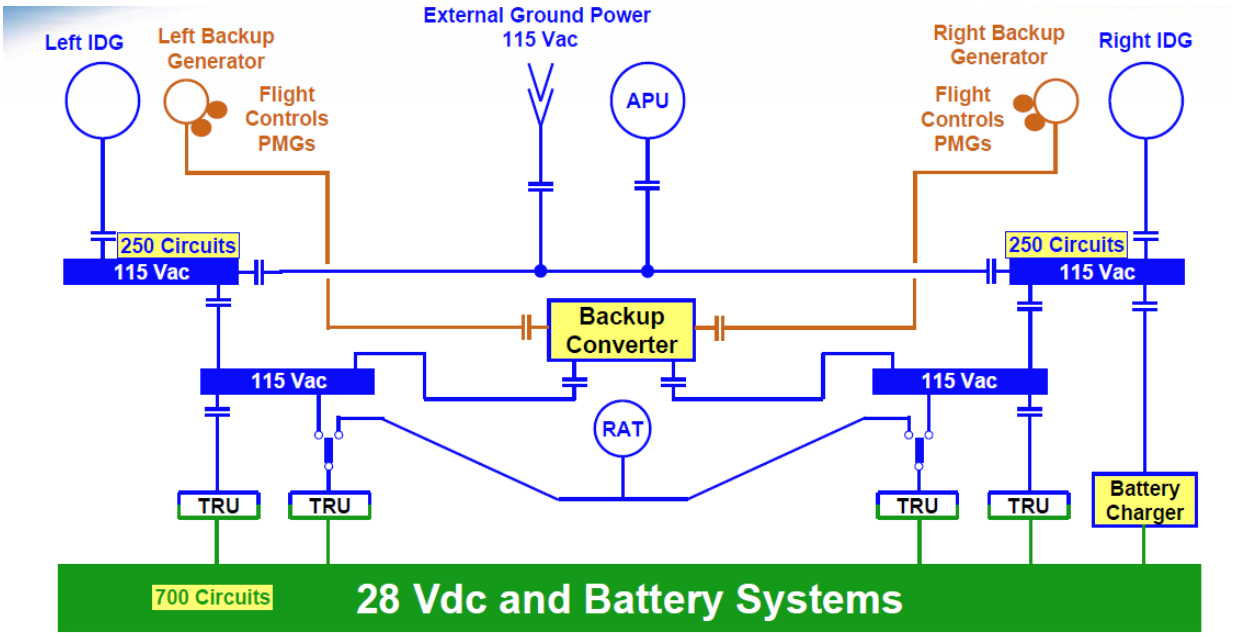


Figure 1.1: Electrical system architecture of Boeing 777 [5]

Modern airplanes, like the Boeing 787 Dreamliner, include more sophisticated architectures that increase the dependency on electrical power, as shown in Figure 1.2. In addition to the 28VDC system, it includes higher voltage DC power at ±270V, as well as 540V power that can be obtained from the differential ±270V outputs [6]. This enables the delivery of large amounts of power sourced from the Starter Generators (SGs) of the engines and converted to DC via Transformer Rectifiers (XFRs) units to several motors (M) driven by variable frequency drives. These motors are used for various functions in the airplane, such as the Environmental Control System (ECS), engine starting, and driving pumps (P) that provide hydraulic pressure during takeoff and landing [6]. Unlike in older aircrafts, where DC power was mainly used to interface with the onboard batteries, modern aircrafts use DC for the most critical and power consuming loads. The Boeing 787 uses the ±270V DC bus to power large motors for the hydraulic pumps used during takeoff and landing and the 28V DC bus for the power control units and flight deck equipment [6].

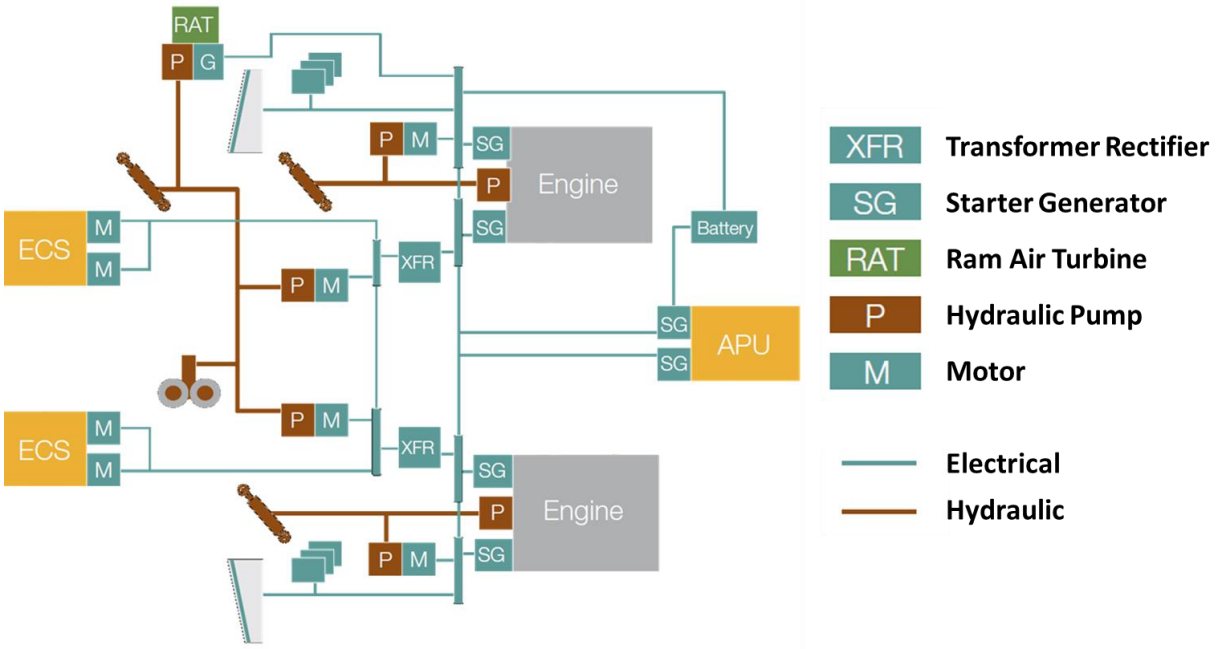


Figure 1.2: System architecture of Boeing 787 Dreamliner, simplified from [7]

1.4. Fault Analyses of DC-based Power Systems

One of the main challenges hindering wider adoption of DC-based networks in aircraft systems is addressing concerns pertaining to system reliability. These concerns are emphasized by the lack of detailed analyses of possible fault scenarios. Brief analysis of line-to-earth and line-to-line faults have been reported for the purpose of cable fault location [8, 9], which was followed by more detailed studies of the line-to-earth case [10, 11]. Other efforts to characterize DC networks under line-to-line short-circuit fault conditions have been reported in [12, 13] for a single output system, [14] for a back-to-back typology, and [15-19] for a distributed typology (microgrid). These papers have mainly based their analyses on simulation results with some including limited analytical equations to support their key findings. However, a comprehensive study of the line-to-line fault condition that includes analytical, simulation, and experimental results has yet to be presented.

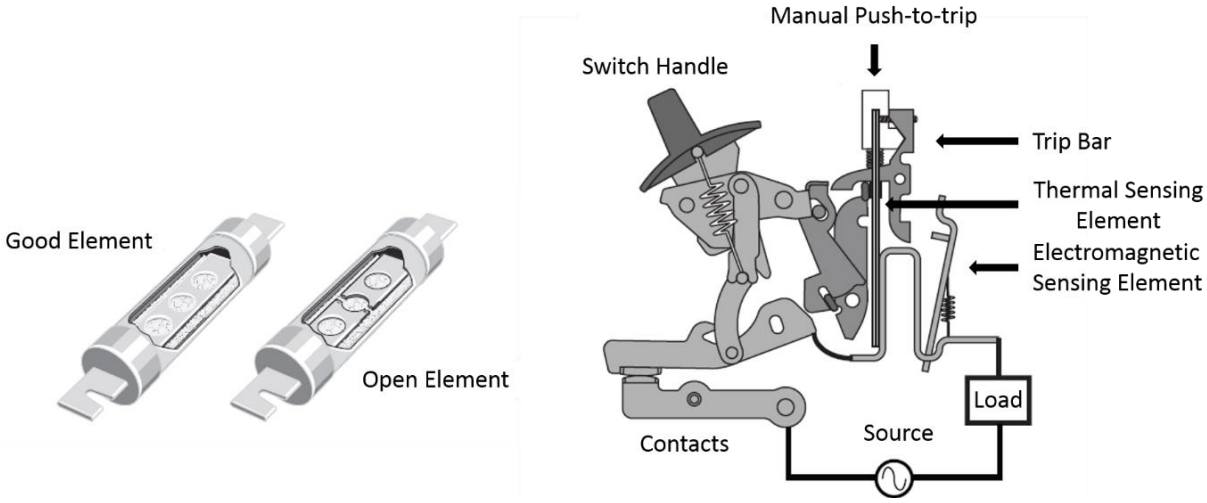
DC systems are highly capacitive, as opposed to inductive AC systems. This is due to large bulk capacitors typically inserted across the lines of DC systems to smooth voltages during load switching. During a short-circuit event, these capacitors can produce currents that can far exceed components ratings and lead to unrecoverable failures. This can occur due to various conditions internal and external to the system, such as: cable faults [8, 10], switching devices failure (shoot-

through) [20, 21], and capacitors breakdown [22]. It is therefore important to develop thorough understanding and detailed characterization of this condition, especially when determining suitable remedies, such as: the type, location, reaction time, and operational conditions of the required protection devices. The aerospace industry is known for prioritizing reliability over other aspects of systems development. Wider adoption of DC-based power systems is a pressing need in the industry due to the many advantages discussed previously, which are emphasized by the growing demand for electrical power in aircrafts. Addressing reliability concerns is therefore a major step to enable this adoption.

Many factors contribute to the likelihood of DC line-to-line short-circuit faults, such as the geometrical arrangement (spacing), and the insulation rating and material selection for cables. Twisting DC cables is a common practice used to reduce susceptibility to noise which increases the risk of line-to-line faults. This risk can be reduced by routing the power (+) and return (-) cables through different paths. In addition, the voltage between cables must not exceed the isolation ratings of insulations accounting for altitude effects. Suppression devices can be inserted across DC lines to limit voltages during transient events, such as lightning strikes. Furthermore, some insulation materials are more susceptible to damage during installation or operation increasing the likelihood of cable faults. These vulnerable insulation materials are typically used to reduce the weight of cables and increase their flexibility, such as the Glenair TurboFlex® and Duralectric™ cables. Some cable manufacturers, such as TE Connectivity, use the process of radiation hardening/crosslinking to increase the durability of cable insulations while maintaining low weight and high flexibility. For capacitors, the likelihood and severity of faults is mostly determined by the type of dielectric materials used. Electrolytic capacitors are known to explode when abused and may fail in either open-circuit short-circuit modes [14]. In comparison, film capacitors are much more stable typically failing in open-circuit mode and including an internal fusing structure that isolates faulty sections of the capacitor making this type of capacitors more suitable for high reliability applications. Finally, the likelihood of shoot-through faults is a function of the deadtime during which both the top and bottom transistors of the converter are OFF. This is a safety time that ensures the two transistors are not ON at the same time causing a line-to-line short-circuit fault through the converter switches.

1.5. Fault Protection Technologies for DC-based Power Systems

One of the oldest, simplest, and most popular fault protection devices are fuses, shown in Figure 1.3 (a). They have been part of electric systems and distribution networks since the first half of the 19th century [23]; providing simple and reliable protection against damage due high currents. However, they have a major disadvantage: they are one-shot devices and must therefore by replaced after each fault for the system to return to its normal operating state. There is also a delay associated with the time it takes the conducting element to heat up, melt, and break after a fault. This dramatically limits their use in high reliability applications.



(a) (b)

Figure 1.3: (a) Typical fuse and (b) circuit breaker structures [24]

The use of circuit breakers is an attractive alternative to fuses. Mechanical circuit breakers have been in use since the end of the 19th century [23], implementing fault interrupt capability with simple mechanical methods that can be reset manually or automatically after a fault is cleared. They are typically tripped by bimetallic strips, which when heated from overcurrent bends in a certain direction releasing a trip bar and breaking the current's path [24]. This thermal trip mechanism can be complemented by an electromagnetic sensing element for faster response times. A typical structure of a thermally and electromagnetically tripped circuit breaker is shown in Figure 1.3 (b). Some breakers can also be controlled remotely by controlling DC solenoids to open and close the contacts.

The use of fuses and circuit breakers in DC systems is more problematic than AC because of the lack of zero crossing. While AC power goes to zero twice in a cycle (100 times per second for 50Hz systems), DC power stays constant. The zero crossing in AC systems suppresses arcs that occur during circuit making (closing), breaking (opening), and contact bouncing. These arcs, if not suppressed quickly, increase the contacts resistances by damaging their metals, which can significantly reduce breakers' lifetimes [25]. The duration of arcs is dependent of the separation speed of the contacts and the type of liquid or gas surrounding the contacts. Older breakers used oil to extinguish arcs, while newer breakers use vacuum or gases like SF6, Hydrogen, and Nitrogen [25]. The type of material used for contact metallization also determines its life expectancy [25]. Materials with higher melting points and hardness can withstand higher arcing times and more switching cycles.

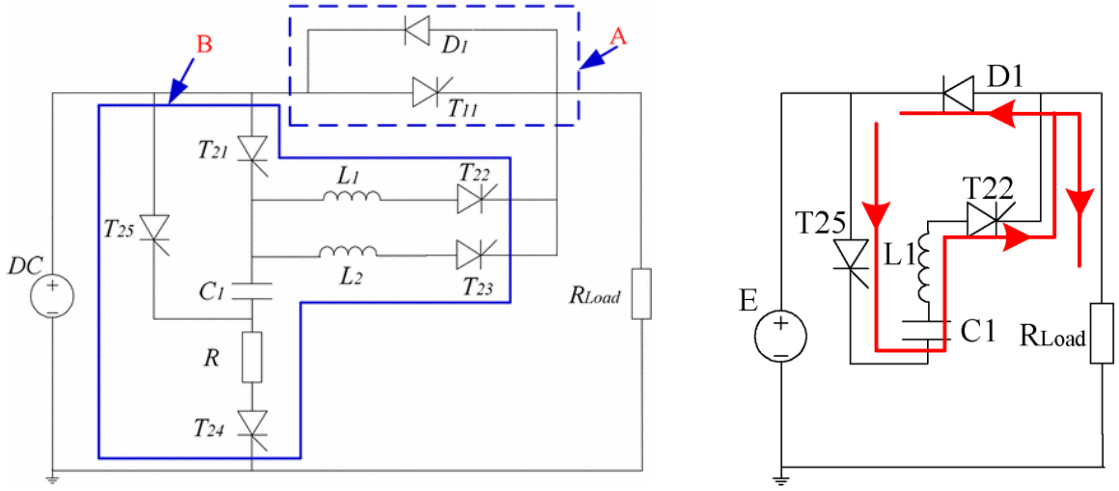
In more recent years, Solid-State Circuit Breakers (SSCB) have been reported. They use power transistors, like Insulated Gate Bipolar Transistors (IGBTs), Thyristors, or Field-Effect Transistors (FETs) as the main switching devices. Compared with mechanical circuit breakers, SSCBs mainly have the advantage of faster response time, programmable threshold, and absence of arcing. Their disadvantages are higher power losses in the ON-state due to the resistance of the semiconductor devices, lack of physical isolation in the OFF-state, and the requirement for bulky transient suppression devices to absorb inductive energy during switching.

1.5.1. DC Solid-State Circuit Breakers

Many topologies have been proposed for SSCBs, using various semiconductor device technologies. this review will cover the most promising topology per device technology, starting with Thyristors and ending with Silicon Carbide Junction Field Effect Transistors (SiC-JFETs) and Gallium Nitrite High-Electron-Mobility Transistors (GaN-HEMTs) based SSCBs.

Because Thyristors can only be switched off when their currents fall below a certain value (called the holding current), their use in DC requires additional resonance circuits to bring down the current for turn off. This has been realized in [26, 27] by additional components, shown as B in Figure 1.4 (a). During turn-off, the resonance circuit (B) is arranged to provide current through D1 that is larger than or equal to the load current, which in turn decreases the current through the main Thyristor (T11) to zero, or even below zero, naturally turning off the Thyristor. Although additional components are required in this case, Thyristors have very high-power capacities, which

makes Thyristor-based SSCB topologies suitable for high-power transmission applications, such as HVDC. They typically have on-state resistance of a few milliohms and can isolate faults within milliseconds.



(a) (b)

Figure 1.4: (a) Thyristor based SSCB topology with resonance, and (b) its equivalent circuit during turn-off [26, 27]

Although IGBTs and Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFETs) have less power handling capabilities than Thyristors, they are faster to switch and easier to drive. Because of their fast switching capabilities, additional components are typically needed in parallel with the devices to protect them from the effects of rapid current change (*di/dt)*, which can induce large voltages across parasitic and non-parasitic inductances in the circuit. These voltage spikes, when exceeding the blocking voltage capabilities of the devices, can result in breakdown failures. Metal oxide Varistors (MOVs) and/or Transient Voltage Suppressors (TVSs) are typically used in combination with snubber circuitries to limit the voltage stress on the switches [28], as shown in Figure 1.5. IGBT based SSCBs require two devices in a back-to-back configuration for bidirectional power blocking. Thus, the typically have twice to three times the on-state resistance of Thyristor-based breakers. However, IGBTs are capable of isolating faults a lot faster that Thyristors (within 10s of microseconds). Therefore, they are more suitable for protecting against fast transient faults such as DC line-to-line short-circuit faults.

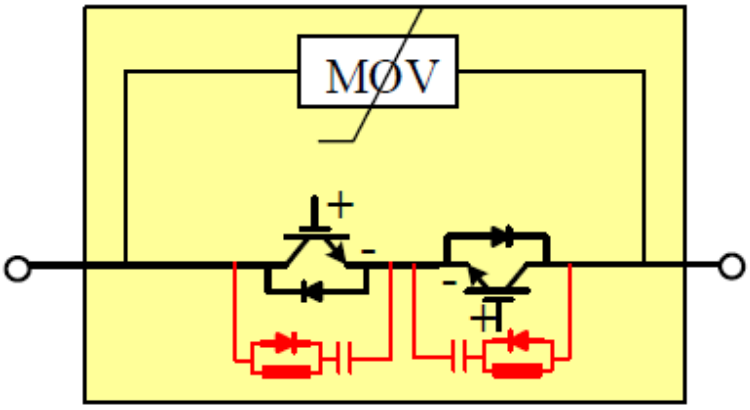
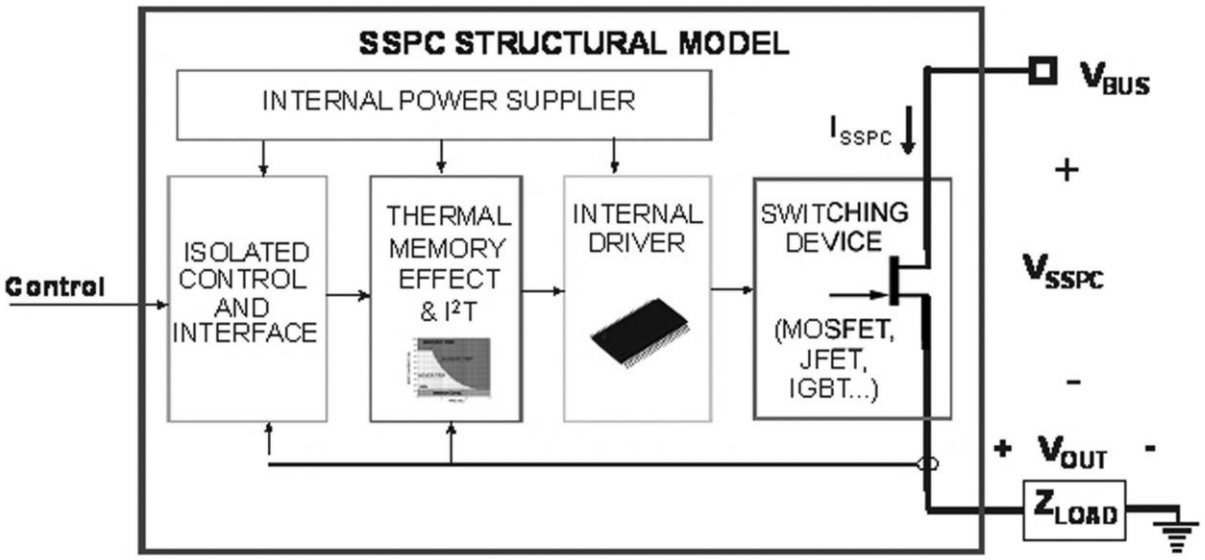
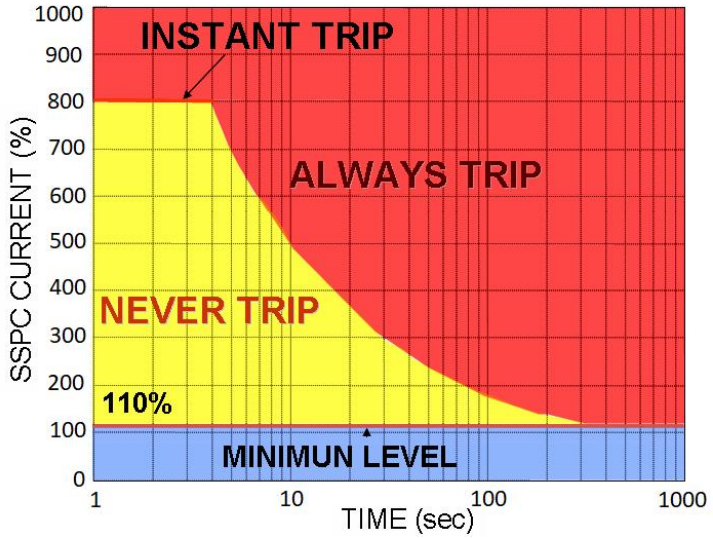


Figure 1.5: Bidirectional IGBT based SCCB topology with MOV and snubbers [28]

Multiples devices can be combined in a module that also includes gate drive, sensing, control, and communication functionalities, which is referred to as a Solid-State Power Controller (SSPC), with a typical functional diagram shown in Figure 1.6 (a). The devices currents are sensed and compared to a current-squared time (i^2t) trip curve, like that shown in Figure 1.6 (b). When faults are detected, the controller triggers the gate drivers to turn off the switches. Additional status reporting and control can be achieved through the isolated control and interface block.



(a)



(b)

Figure 1.6: (a) Typical SSPC model, and (b) i^2t based trip curves [29, 30]

Many SSPC modules have been reported, integrating various switching devices technologies, control approaches, and additional functionalities. Typical devices used in SSPCs are IGBTs, MOSFETs, and JFETs, as in [31-33] respectively, due to their high switching speeds compared with Thyristors. For control, conventional i^2t based trip curves are mostly used. However, some load based trip characteristics and current control strategies have also been reported, such as in [34] where the control is optimized for capacitive loads. Finally some research has reported SSPC modules with additional functionalities such as self-testing, status reporting, and active short-circuit current control in [30], changeable reset time, ambient temperature compensation, and thermal memory in [35]. Some commercial SSPC modules also exist, such as those manufactured by Data Device Corporation (DDC) [36] and shown in Figure 1.7.

(a) (b) (c)

Figure 1.7: Commercial SSPCs (a) power distribution units (b) cards, and (c) point-of-load modules [36]

Recently, wide-bandgap based semiconductors have been gaining a lot of attention due to their superior performance compared with Silicon-based devices. Among their most important advantages are: lower on-state resistance for the same breakdown voltage ratings, faster switching speeds, and higher operation temperatures. These are consequences of the materials' superior physical properties compared with silicon, as demonstrated in Figure 1.8.

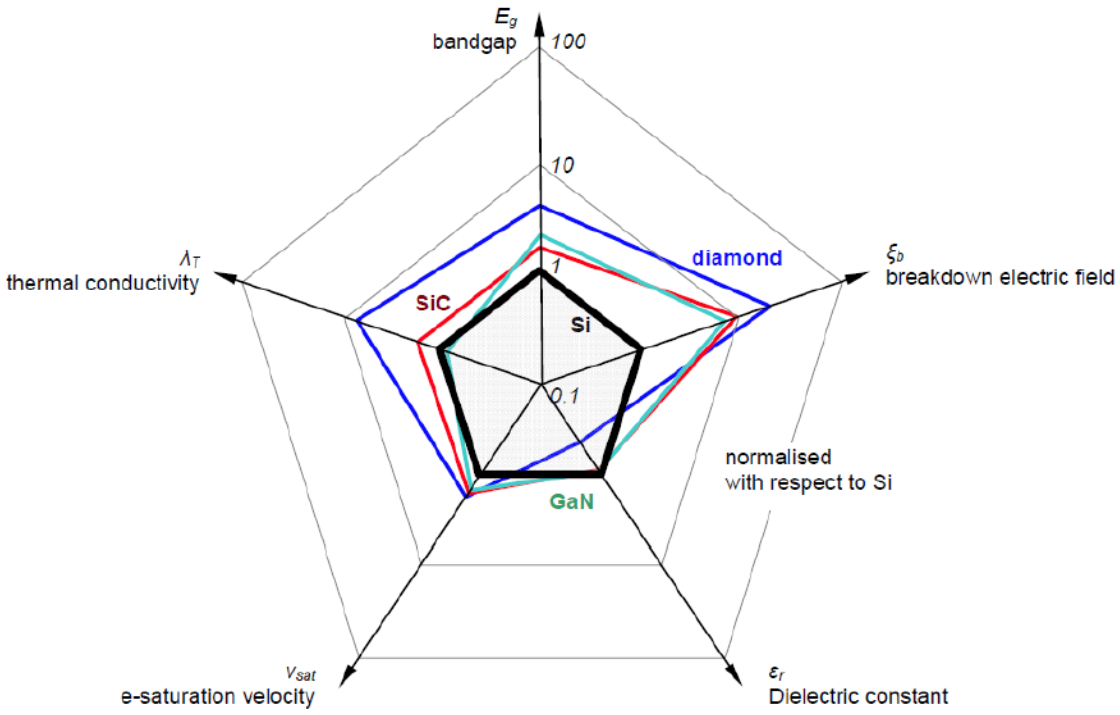


Figure 1.8: Normalized comparison of wide band-gap materials' properties compared with Silicon [37]

The higher energy bandgaps of wide-bandgap materials result in higher operation temperatures until intrinsic carriers sufficiently degrade the performance of the devices. While the higher breakdown electric fields increase the voltage handling capabilities of the devices for the same drift region length resulting in lower on-state resistance for the same breakdown voltage. The dielectric constant is directly proportional to the capacitances of the devices which influence switching speeds, also enhanced by the higher saturation velocity. Finally, the higher thermal conductivities of Diamond and Silicon Carbide means that heat can more easily be removed from devices made of these materials.

Multiple SSPCs using wide-bandgap semiconductors have been reported. The work in [38] takes advantage of SiC-JFETs normally-ON characteristics to demonstrate a fast-acting and self-

powered SSCB, where the SSCB is powered from the voltage induced across the device during a fault. This SSCB was shown to be capable of isolating a fault within 1µs. However, it has an on-state resistance of 45mΩ at 25°C which is significantly higher than IGBT and Thyristor based SSCBs. This same concept has been simulated in [39] for GaN-HEMTs, though no reports of switching times or on-state resistance were included. The work reported in [40] used two SiC-JFETs in a back-to-back configuration to demonstrate the bidirectional capability of a 60A/600V SSCB at the expense of doubling the on-state resistance of the device. Finally both [33] and [41] demonstrated SiC based SSPC modules with i^2t tripping characteristics using JFETs and MOSFETs respectively.

1.5.2. Current Limiting Diodes

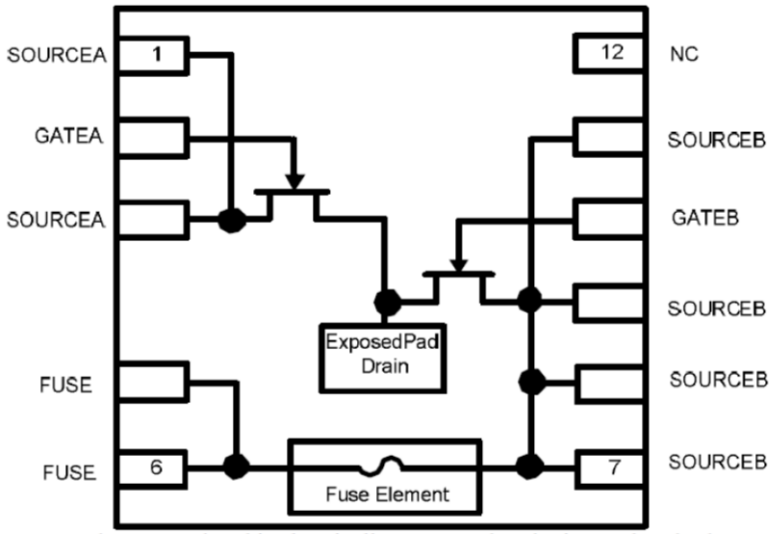
Current limiters operate based on introducing additional resistance in the path of the current during a fault. This limits the magnitude of the fault current and therefore the resulting damage. It can be realized using semiconductor switching devices: When the current is low, a semiconductor switch operates in the linear-ohmic region, and therefore has small resistance mostly equal to its bulk resistance. During a fault, a large voltage appears across the device, causing it to operate in the saturation region where its channel is pinched off, resistance is higher, and current is therefore limited. Furthermore, when a fault occurs, the large fault energy induces self-heating in the transistor, causing the current to decrease further. This combination of saturation and self-heating effects make power transistors suitable for current limiting application. Furthermore, normally-ON transistors, like depletion mode MOSFETs, JFETs, and HEMTs, can be used to eliminate the need for external gate control. A normally-ON transistor can limit current even at $V_{GS}=0$, which is simply realized by connecting the Gate (G) terminal to the Source (S).

Having this variable impedance element in the path of the current for fault protection was first introduced for AC systems using capacitors and inductors [42]. In the same year, the design and fabrication of a depletion mode MOSFET for current limiting application was reported [43]. This was followed by another design which combined this current limiting device with IGBTs for dual current limiting and interrupting functions [44]. A few years later, the design of a SiC current limiter based on depletion mode MOSFET structure was reported [45]. A bidirectional current limiting device based on the AccuFET structure was then simulated and studied in [46]. The optimization of Vertical JFET (VJFET) structure and layout for current limiting application was

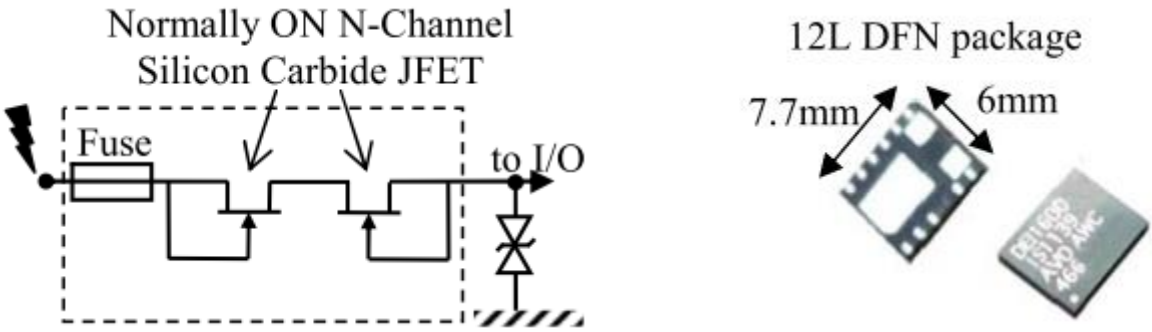
reported in [47] and [48] respectively. The advantages of using SiC current limiters in terms of operation temperate and on-state resistance, as well as some of the applications where a current limiter can be used were presented in [49]. Previous work was focused on developing current limiting diodes for lightning protection. As of the writing of this thesis, there have been no reports of current limiters developed for short circuit protection. This work will focus on demonstrating the benefit of including CLDs in power converters as well as designing, building and testing proof of concept limiters.

A) Current Limiting Diodes for Lightning Protection

SiC-JFETs have been shown to be very robust when subjected to short energy pulses [50], which was the motivation for using them for lightning protection application. Combining SiC-JFETs with Transient Voltage Suppressors (TVS) to provide both voltage and current protection have been shown to significantly reduce the capacitance and physical size of the TVS [51]. A commercial device with the layout shown in Figure 1.9 (a) have been manufactured and deployed on the Airbus A350 XWB [52]. The device contains two SiC-JFETs in a back-to-back configuration for bidirectional limiting capability and a fuse for fail safe operation, as shown in Figure 1.9 (b). It is packaged in 12 lead DFN form, as shown Figure 1.9 (c).



(a)



(b) (c)

Figure 1.9: (a) Structure of reported device [52], (b) suggested connection, and (c) package [53]

The current limiter is placed on lines connecting embedded equipment in combination with TVSs, as shown in Figure 1.10. During a lightning strike to that line, the TVS acts to limit the voltage seen by the equipment and the current limiter to limit the current seen by the TVS. The additional resistance of the current limiter during a fault reduces the peak power stress on the TVS, as demonstrated in Figure 1.11, and therefore decrease its required size and weight.

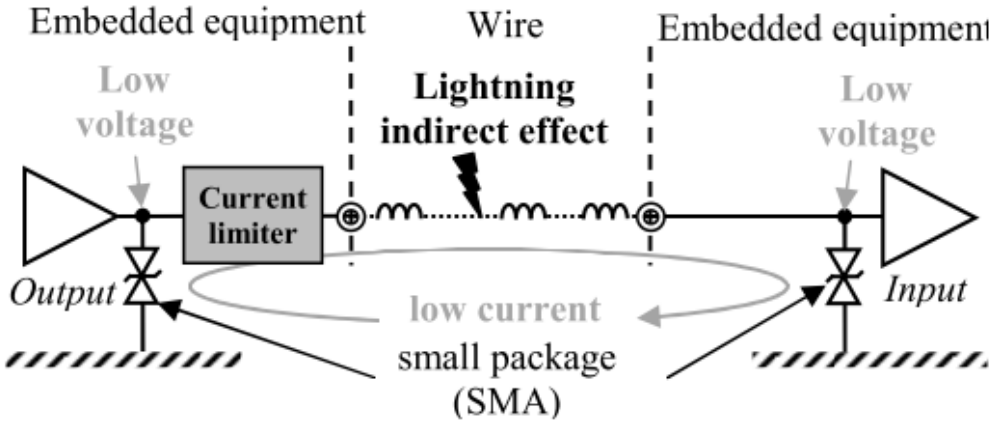


Figure 1.10: Location of CLD in the system on lines connecting embedded equipment [53]

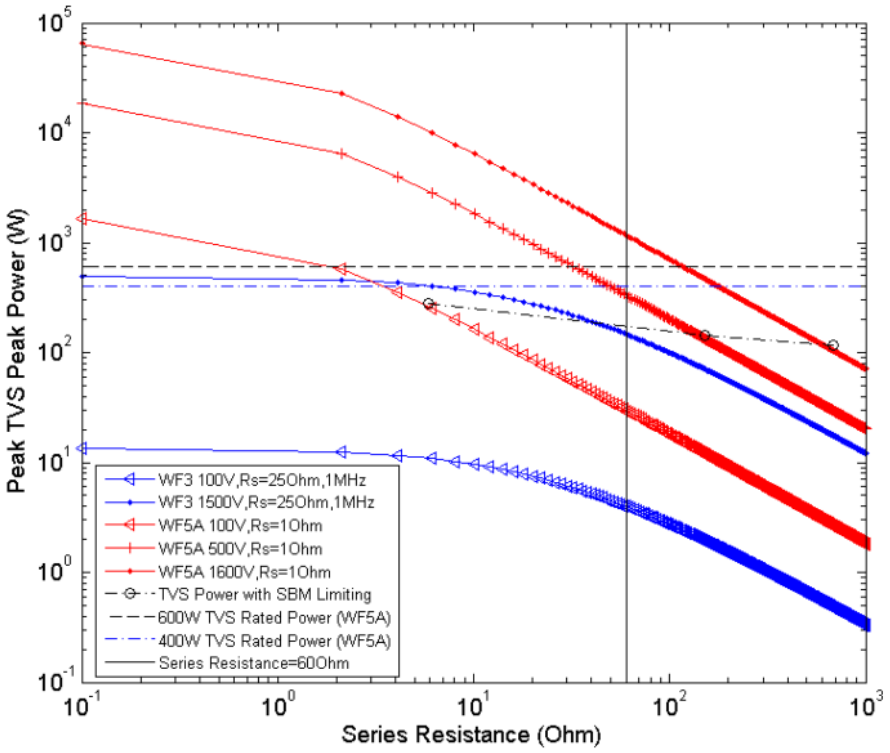


Figure 1.11: Required TVS power rating vs. series resistance under fault condition [51]

B) Current Limiting Diodes for Short-Circuit Protection of Power Converters

The use of CLDs for short-circuit protection offers significant advantages over conventional mechanical or solid-state circuit breakers. Specifically, it eliminates the need to set hard limits for protection. As discussed earlier, the response of conventional protection devices is based on comparing current flow to an I^2t curve. When current exceeds this limit, the protection device opens, and power flow is interrupted. The device would then have to be reset (or replaced in case of fuses) for normal operation to resume. When setting this limit, the designer often faces a major dilemma: if the limit is set low, false trips would compromise system reliability. On the other hand, if set high, components would have to be oversized to withstand additional power flow during a fault. The time for which components would have to carry fault current can be as long as 1ms after a fault is detected, if ultrafast mechanical circuit breakers are to be used [54]. However, as short as this period may seem, it is still challenging for the power semiconductors. Power semiconductor modules have substantially less thermal capacity than other components of the power system, such as electric machines. This issue is exacerbated by the recent trend in power semiconductor module design to eliminate the base plate layer to reduce thermal resistance.

With CLDs, fault currents can be limited within a certain range (such as 2-3 per-unit (PU)), yet instantly reset to nominal value (1 PU) when the fault is cleared. Thus, no interruption of power occurs. Due to the significant amount of heat generated, CLDs are not capable of operating indefinitely. Thus, requiring a circuit breaker to eventually isolate the faulty system, if the fault persists for long duration of time. This time is substantially longer than that imposed on circuit breakers when operating without a CLD. Furthermore, current that must be interrupted by the circuit breaker when the CLD's thermal limits is reached (2-3 PU) is substantially less than that without the CLD (8-10 PU). Thus, increasing the expected life of the breaker and eliminating the need for ultrafast response. The overall i^2t limit of the system when a combination of circuit breaker and CLD is used can be illustrated as shown in Figure 1.12. The magnitude at which current must be limited (2-3 PU) and duration of time for which the current limiter must be operational (10µs to 5 seconds) were specified by Rolls-Royce plc according to their system level requirements.

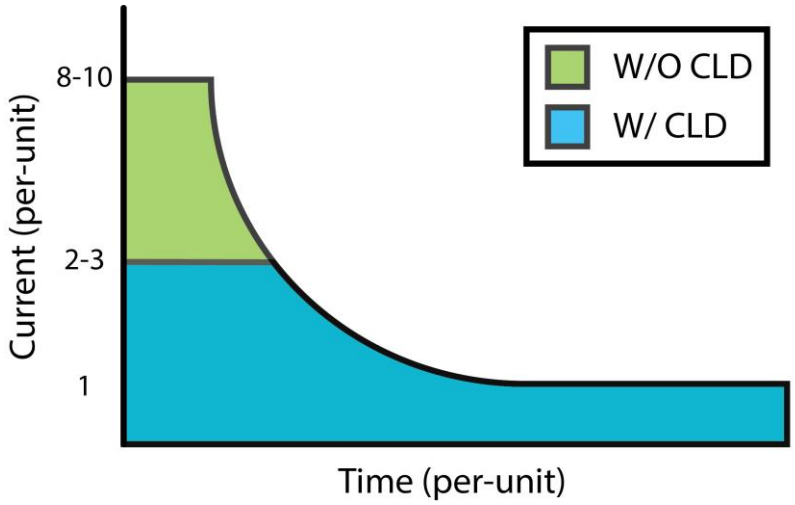


Figure 1.12: Expected power system I^2t curves with and without a CLD (from Rolls-Royce plc)

C) Packaging Requirements and Design For Current Limiting Diodes

CLDs dissipate significant amount of heat during fault conditions as they operate in the saturation region where both their currents and voltages are high. However, these losses are only generated for a short period of time. Therefore, with the appropriate packaging design, the maximum temperature of the SiC-JFETs can be maintained within its limit. This limit is up to 660°C [55] which is significantly higher than typical values for other Si and SiC power semiconductor devices (150-250°C). Furthermore, the packaging requirements for CLD are

different than those of power modules and discretes used in power converters. Typical packaging requirements for devices used in converters are:

1- Provide mechanical support and protection for the devices against environmental conditions, such as vibration and foreign object damage. This is accomplished by appropriate design of the power module casing and encapsulation.
2- Provide good electrical connections with minimal resistance between the terminals of the devices and the package. This is typically accomplished using wire bonds to make connections to the top side terminals of the die and solder to attach the bottom side of the die to a substrate.
3- Provide a good thermal conductivity path between the devices and packaging heatsink interface. This is typically accomplished by minimizing the thicknesses of material layers between the dies and heatsink interface (solder, thermal grease, baseplate, substrate).
4- Provide electrical isolation between the devices in a power module, and between the devices and heatsink interface. This is needed so that multiple modules can be mounted on the same heatsink, and so that in the case of liquid-cooled systems, the liquid is not electrified. The substrate typically includes a ceramic layer to achieve this isolation.

Recent trends in packaging technologies have focused on the use of more advanced materials and techniques to improve reliability and performance of power modules. The use of sintered silver is an attractive alternative to SnAg based solder for die attachment as it offers higher operation temperature and lower thermal resistance [56]. The dies can also be pressure contacted so that no soldering is required whatsoever. Furthermore, the use of spring contacts eliminates the need for wire bonds which have poor thermal cycling capability [57]. The reliability can further be improved by eliminating the baseplate layer in the module, which also lowers the thermal resistance [57]. The resistance can be further reduced by replacing the ceramic insulation layer in the substrate with advanced materials, such as synthetic Dimond [58].

CLDs are only operational for short periods of time. Thus, there is no need for continuous cooling using a heatsink, and therefore, no requirement for electrical isolation. The packaging must still provide good electrical connection and mechanical support to the die and be capable of operating up to 660°C. Heat generated by the SiC-JFET die must flow through a low thermal resistance path to a thermal mass where it can be stored. This energy is then slowly released to the

environment after the fault is cleared through conduction or convection. The low thermal resistance path can be established by making contacts to both the top and bottom sides of the die (double side cooling). SiC-JFET dies in CLD configuration (gate and source pads connected) are well suited for double side cooling as both terminals can be internally connected during die fabrication so that a flat top surface is obtained [59]. The use of double side cooling for CLD packaging was recommended by Rolls-Royce.

1.6. Aims and Objectives

The aim of this PhD is to design, build, and test a current limiter according to the specifications provided by Rolls-Royce plc. This current limiter must limit the magnitude of fault current to 2-3 times its nominal value and must be operational for 10μs to 5 seconds at an ambient temperature of up to 85°C. The device would be integrated with a voltage source converter and permanent magnet machine acting as a starter/generator for an aircraft jet engine. This starter generator system was designed, built, and tested by the Rolls-Royce university technology center in advanced machines and drives at the University of Sheffield. The 100kW power rating of this system is split among two identical channels (two power converters and two sets of machine windings) feeding a common DC bus regulated at 540VDC. A derivative objective was to demonstrate the value of adding this current limiter to the system. To accomplish that, analyses were carried out to derive the fault response and components stress under a fault condition with and without the current limiter.

1.7. Outline of Thesis

- In the second chapter of this thesis, the reaction of Voltage Source Converters (VSCs) to the worst-case fault scenario (short-circuit across the DC terminals) is analyzed. Multiple stages of the fault event are identified, with the equivalent circuits generated, and analytical expressions for voltages and currents of interest at each stage derived. The analyses presented provide detailed characterization of the converter circuit under this condition, including the effects of various circuit parameters on the fault response. The findings are validated against simulations of a dual-channel 100kW rated motor drive designed and built for aerospace application.

- In the third chapter, the analyses presented in the second chapter are validated experimentally using a single channel replica of the dual-channel motor drive.
- In the fourth chapter, the feasibility of using SiC-CLDs for short-circuit protection of power converters is investigated. A physics-based SiC-CLD SPICE model is created. This model accounts for the CLD's junction temperature and physical features effects on the response. An equivalent fault circuit including the developed CLD model is then studied. The fault response of the circuit is analyzed accounting for various CLD and fault circuit parameters. Multiple stages of the response are identified, with the equivalent circuits generated, and analytical expressions derived for currents and voltages of interest. The analytical results are validated against simulations using typical SiC-JFET device parameters demonstrated in literature, packaging parameters extracted for a packaged SiC-JEFT with similar footprint, and equivalent fault parameters derived in Chapter 2.
- In the fifth chapter, the design, build, and test of a proof-of-concept current limiting diode demonstrator are presented. This demonstrator utilizes a commercial off-the-shelf Silicon Carbide Junction Field Effect Transistor (JFET) with the gate and source terminals externally connected, as discussed in Chapter 4. The SiC JFET die is integrated into a custom designed high temperature package which is inserted in-line with the DC-link capacitor. The die is pressure contacted by copper busbars acting as the electrical connections (cathode and anode) and thermal masses for heat generated by the CLD to be dissipated to.
- In the sixth chapter, the concept of an Integrated Current Limiting Diode (ICLD) is presented. The proposed device can achieve significantly higher operation times than a CLD by distributing the losses among multiple SiC JFETs. The design, build, and test of a proof-of-concept demonstrator are also presented in this chapter.
- Finally, in the seventh chapter, conclusions of this thesis and proposed future work are presented.

1.8. List of Publications

- M. Alwash, M. Sweet, E. M. S. Narayanan and G. Bruce, "Short-circuit protection of power converters with SiC current limiters," *2016 IEEE Energy Conversion*

Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-6.

- M. Alwash, M. Sweet and E. M. S. Narayanan, "Analysis of voltage source converters under DC line-to-line short-circuit fault conditions," *2017 IEEE International Electric Machines and Drives Conference (IEMDC)*, Miami, FL, 2017, pp. 1-7.

- M. Alwash, M. Sweet and E. M. S. Narayanan, "Analysis of voltage source converters under DC line-to-line short-circuit fault conditions," *2017 IEEE 26th International Symposium on Industrial Electronics (ISIE)*, Edinburgh, 2017, pp. 1801-1806.

- M. Alwash, M. Sweet and E. M. S. Narayanan, "DC Line-to-Line Short-Circuit Fault Analyses of Voltage Source Converters," in *IEEE Transactions on Power Electronics* (conditionally accepted).

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Chapter 2: Analyses of Voltage Source Converters DC Line-to-line Fault Response

2.1. Introduction

DC line-to-line short-circuit are the most severe fault condition in AC-DC Voltage Source Converters (VSCs) [1-5]. These fault conditions cause current magnitudes which exceed components ratings and lead to unrecoverable failures. They can occur due to various conditions internal and external to the converter, such as cable faults [3, 6], switching devices failure [7, 8], and capacitor breakdown [9]. It is therefore important to develop a thorough understanding and detailed characterization of this condition, especially when determining suitable mitigation strategies, such as the type, location, reaction time, and operational conditions of the protection devices. In depth analyses of VSCs line-to-line fault response are presented in this chapter to aid the development of protection technologies, in terms of:

1) *Operation conditions:* Defining the fault current that the protection devices must be capable of isolating or limiting, which influences their required current interruption capacity, and thus, size and weight. In this work, expressions describing fault currents at multiple locations of interest in the system are presented and validated against simulations and experiments.

2) *Locations:* Defining the contributions of the various sources in the system to faults, which enables determining the effectiveness of isolating these sources. For example, this enables comparing the effectiveness of isolating the AC side, capacitor branch or DC output, which is influenced by system parameters.

3) *Reaction time:* Accurate predictions of fault currents enables determining the required reaction time before component limits are reached. For example, times at which the capacitor or diodes reach their maximum rated currents are found directly from expressions derived in this work. Furthermore, diode currents are used to determine times at which they reach their maximum rated junction temperatures. This can be accomplished by finding the losses that these currents induce ($P(t) = V_j\, i(t) + R_s\, i(t)^2$), where R_s and V_j are found from the I(V) characteristics of the diodes [10]. The losses are then used in conjunction with its thermal impedance to determine their transient temperature rise.

4) *Allowable weight:* A trade-off can be made between oversizing or derating the system to be capable of withstanding a fault for a certain duration of time and including a device which protects the system during this period, such as a current limiter. This tradeoff can be used to determine the allowable weight of the protection device. For example, if it was found from (3) that the junction temperature of the diodes rises by 50°C within 100μs of the fault, the diodes would have to be de-rated by 50°C in order for them to maintain their thermal rating under this fault condition. This leads to a reduction in power density that can be translated into an effective increase of weight. The weight of a current limiter operating for up to 100μs cannot exceed this limit.

Brief analysis of line-to-earth and line-to-line fault responses have been presented for the purpose of cable fault location [2, 3], which was followed by more detailed studies of the line-to-earth case [6, 11]. However, a comprehensive study of the more problematic line-to-line condition has yet to be presented. The work presented in this chapter accounts for parameters and stages that were not previously considered, which significantly influence the obtained characteristics, as will be demonstrated. The most important of those parameters are: the equivalent series inductance and resistance of the capacitors, which induces significant additional stress on the converter diodes that was not previously accounted for, and the on-state voltage drop and turn-on voltage of the diodes, which also influence fault characteristics and time boundaries. In addition, the interaction between AC and DC side contributions were not previously considered, causing discrepancies within the results, that has now been addressed in the Combined Response section of this chapter. As compared to simulations, the analytical model shows the contributions of the various sources to the fault response (AC side, DC side, DC bus capacitor, etc.) and their dependences on the various system parameters. The expressions derived can also be used to generate three dimensional curves that demonstrate the sensitivity of the fault response to the various system parameters.

The fault response was analyzed by studying the contributions of the AC and DC sides separately. Interactions between the two contributions were then analyzed, leading to the combined response. Detailed analyses of the DC side contributions are presented in the third section of this chapter. Whereas analyses of the AC side contributions, represented by the AC input currents, are presented in the fourth section of this chapter. Finally, the interactions between the two contributions leading to the combined response are presented in the fifth section. The findings are

validated against simulation results in the sixth section. The flowchart shown in Figure 2.1 demonsatrtes the use of equations presented in this section for fault response calculations.

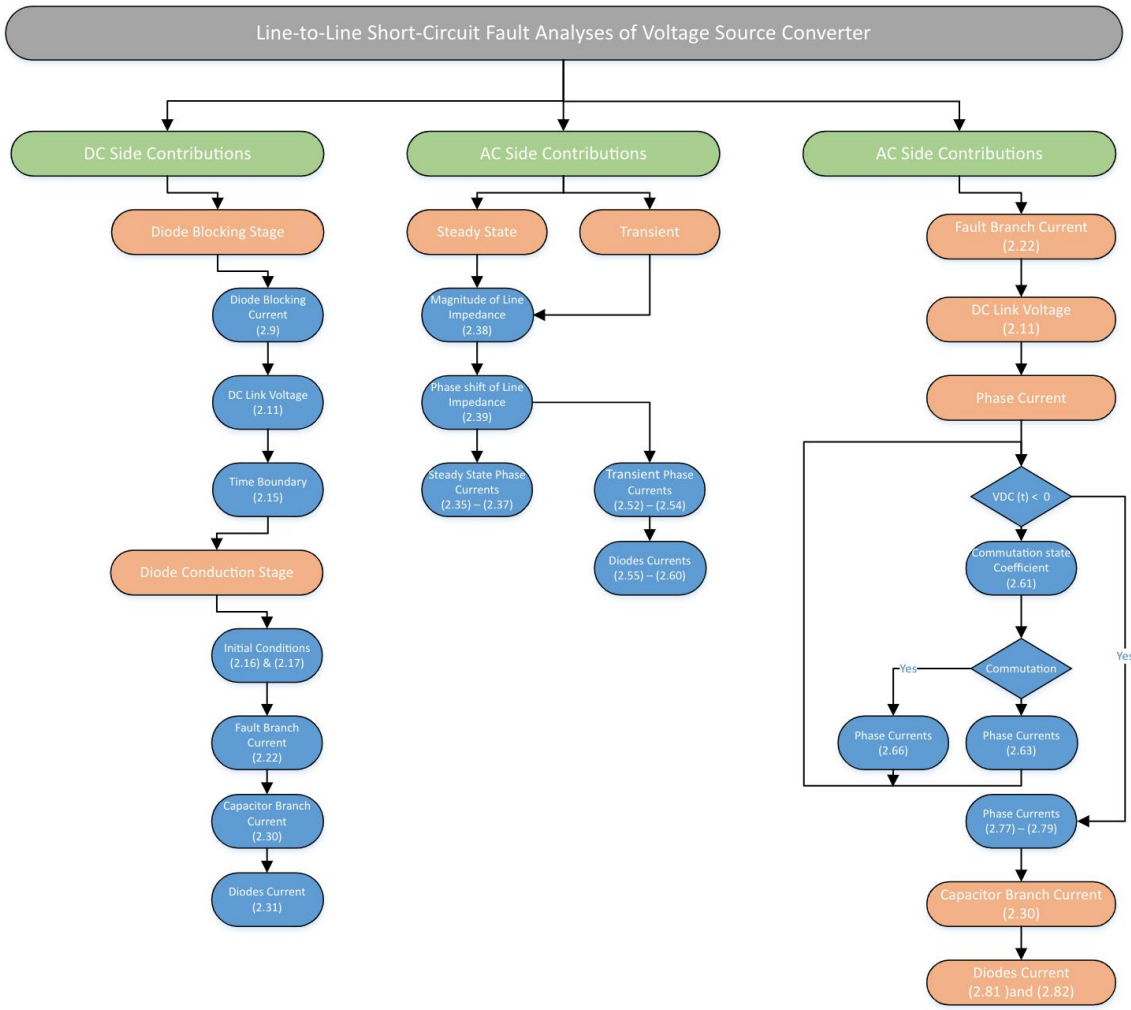


Figure 2.1: Fault response calculations flowchart

2.2. DC Side Contributions

The equivalent circuit of the converter due to the DC side contribution is shown in Figure 2.2, where the AC side is disconnected and the converter switches are omitted, assuming they were protected by the desaturation mechanism of the gate drivers. This protection functionality is included in most gate drivers used in industrial drives, typically operating within less than 10μs of the transistors saturation. For faster isolation of the transistors, gate drives used in high reliability applications may include inhibit functionality which is triggered by current transducers at the DC side through analog circuitry. In the figure, L_{short} and R_{short} are the inductance and resistance of the short-circuit path,

C is the DC-link capacitance, *ESR*, and *ESL* are the Equivalent Series Resistance and Inductance of the capacitor respectively. The bus capacitor is initially charged with a voltage of V_0, while the fault branch has an initial current of I_0.

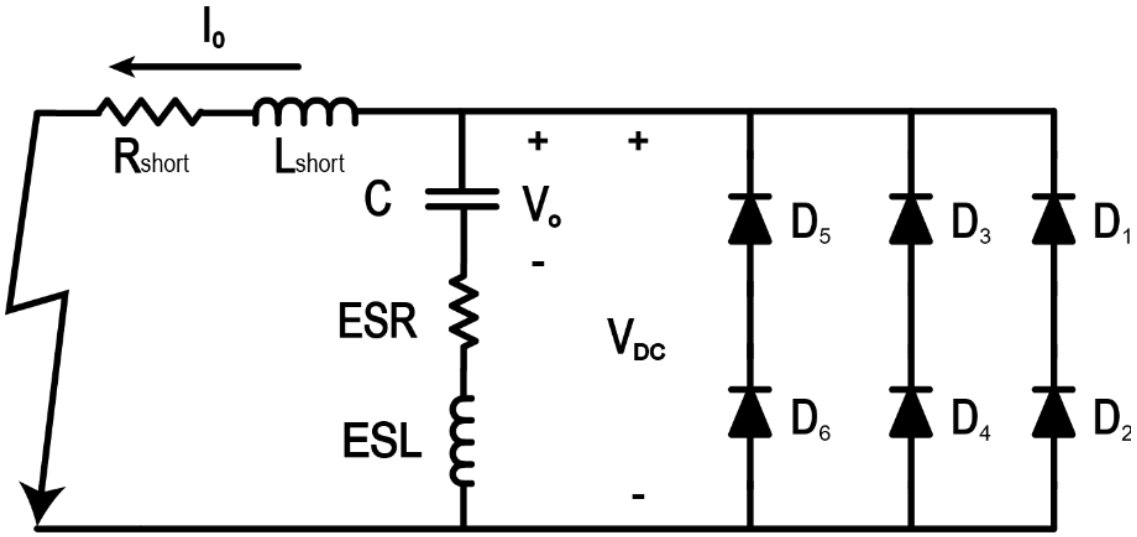


Figure 2.2: Equivalent circuit of converter due to DC side fault contribution

The converter goes through two stages due to the DC side components; diode blocking and conduction. During the first stage (diode blocking), the converter diodes (D1-D6) are all reverse biased. Therefore, the capacitor only discharges through the fault path (R_{Short} and L_{Short}). This stage ends when the DC-link voltage (V_{DC}) becomes negative and falls below the turn-on voltage of the converter diodes (D1-D6). This marks the start of diode conduction stage where currents flow through the diodes from both fault (R_{short} and L_{short}) and capacitor (*C*, *ESR*, and *ESL*) branches.

2.2.1. Diode Blocking Stage

During this stage, the DC-link voltage is positive, and therefore, the converter diodes (D1-D6) are reverse biased. The DC side contribution circuit shown in Figure 2.2 can therefore be simplified as shown in Figure 2.3, where i_{DB} is the fault and capacitor branch current during this stage.

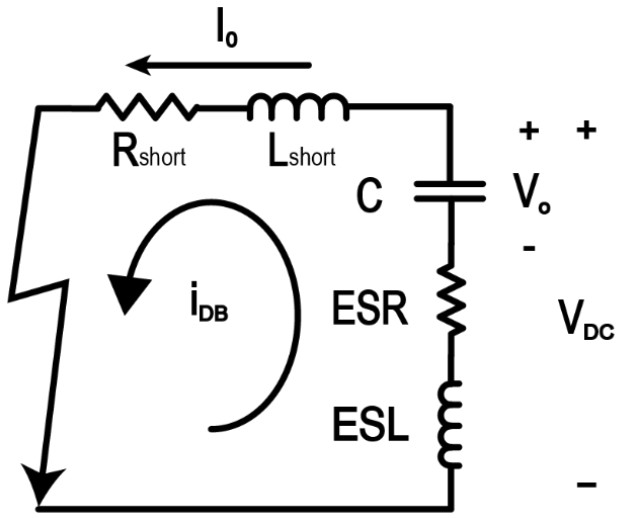


Figure 2.3: Equivalent circuit during diode blocking stage

According to Kirchhoff Voltage Law (KVL), summation of voltage drops across components in a closed circuit path is equal to zero. Applying this law to the circuit shown Figure 2.3 yields this expression:

$$ESL\ \frac{di_{DB}}{dt} + ESR\ i_{DB} + \int \frac{i_{DB}}{C}\ dt + L_{short}\ \frac{di_{DB}}{dt} + R_{short}\ i_{DB} = 0 \tag{2.1}$$

which after differentiating and rearranging becomes:

$$\frac{d^2 i_{DB}}{dt^2} + \frac{di_{DB}}{dt}\ (\frac{ESR + R_{short}}{ESL + L_{short}}) + \frac{i_{DB}}{(ESL + L_{short})\ C}\ = 0 \tag{2.2}$$

The solution to this second order differential equation in the time domain has the form [12]:

$$i_{DB}(t) = e^{-\beta t}(A_1\ cos\ \omega_r t + A_2\ sin\ \omega_r t) \tag{2.3}$$

for which, the damping factor (β), resonance frequency (ω_0), and ringing frequency (ω_r) are defined as [12]:

$$\beta = \frac{ESR + R_{short}}{2\ (ESL + L_{short})} \tag{2.4}$$

$$\omega_o = \frac{1}{\sqrt{(ESL + L_{short})\ C}} \tag{2.5}$$

$$\omega_r = \sqrt{\omega_o^2 - \beta^2} \tag{2.6}$$

The constants A_1 and A_2 can be found from the initial conditions. Given that the initial current at time zero is I_o, A_1 can be found as:

$$i_{DB}(t = 0) = I_o = A_1 \tag{2.7}$$

Given that the rate of rise of fault current ($\frac{di_{DB}}{dt}$) at time zero is only limited by inductances in the current path ($ESL + L_{short}$), A_2 can be found from the relationship:

$$\frac{di_{DB}}{dt}(t = 0) = \omega_r A_2 = \frac{Vo}{(ESL + L_{short})} \tag{2.8}$$

After substituting A_1 and A_2 found from (2.7) and (2.8) respectively into (2.3), the expression for fault and capacitor branch current during this stage can be found as:

$$i_{DB}(t) = e^{-\beta t}(I_o \cos \omega_r t + \frac{Vo}{\omega_r(ESL + L_{short})} \sin \omega_r t) \tag{2.9}$$

Expression (2.9) can then be used to derive and expression for the DC-link voltage, using the relationship:

$$V_{DC}(t) = L_{short}\frac{di_{DB}}{dt} + R_{short}\, i_{DB} \tag{2.10}$$

After substituting (2.9) into (2.10), the expression for the DC-link voltage becomes:

$$V_{DC}(t) = e^{-\beta t}(A \cos \omega_r t + B \sin \omega_r t) \tag{2.11}$$

where,

$$A = L_{short}\left(\frac{Vo}{ESL + L_{short}} - \beta\, I_0\right) + R_{short} I_0 \tag{2.12}$$

$$B = R_{short}\, \frac{Vo}{\omega_r(ESL + L_{short})} - L_{short}\left(\omega_r I_0 + \beta\, \frac{Vo}{\omega_r(ESL + L_{short})}\right) \tag{2.13}$$

Next an expression for the time boundary at which the converter diodes transition from blocking to conduction is derived. As discussed earlier, this transition occurs when the DC-link voltage falls below the turn-on voltage of the converter diodes. The diodes are distributed among three legs that

are connected across the DC-link, with each leg containing two series-connected diodes. The transition therefore occurs when the DC-link voltage falls below the turn-on voltage of two series connected diodes ($V_{DC}(t_b)$=-$2V_j$), where V_j is the turn-on voltage of each diode (≈0.7-2V) and t_b is the time boundary.

Due to the form of (2.11), it is not possible to explicitly solve for t_b. However, by observing that (2.11) includes two multiplied terms; an exponential decay ($e^{-\beta t}$) and a sum of sinusoids ($I_o\ cos\ \omega_r t + \frac{Vo}{\omega_r(ESL+L_{short})}\ sin\ \omega_r t$). Due to the nature of this RLC network, the exponential decay is expected to be significantly slower than the sinusoidal ringing. Therefore, the exponential decay term can be approximated from a known close by point. This point is the zero crossing where (V_{DC}=0). Time at which the zero crossing occurs can be found as:

$$t_0 = \frac{tan^{-1}\frac{A}{B}}{\omega_r} \tag{2.14}$$

The exponential term of (2.11) at the time boundary can then be approximated as $e^{-\beta t_0}$. Finally, using this information, the time boundary at which V_{DC}=-$2V_j$ can be approximated as:

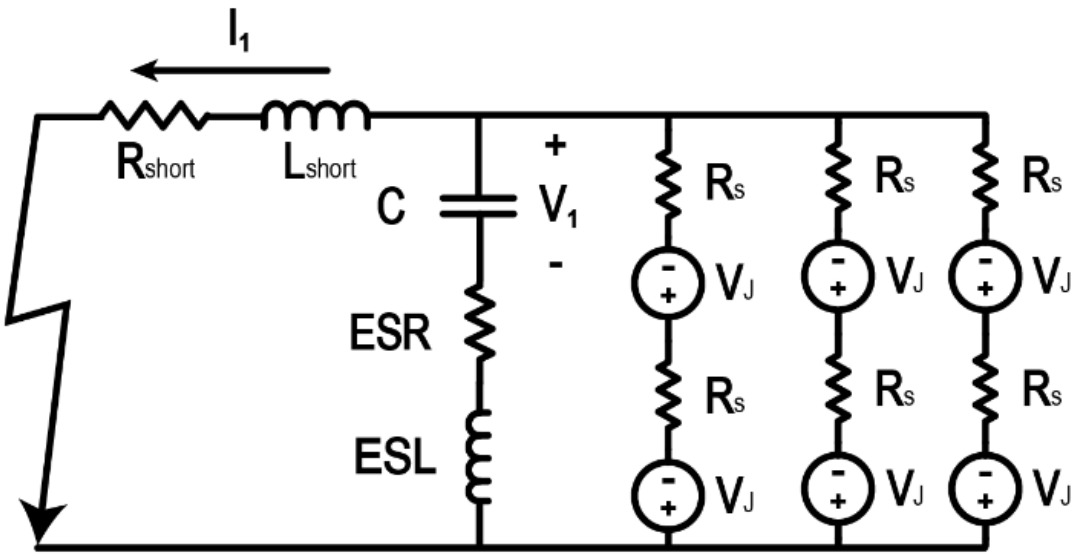
$$t_b \approx \frac{sin^{-1}\frac{-2V_j\ e^{\beta t_0}}{\sqrt{A^2+B^2}} - sin^{-1}\frac{A}{\sqrt{A^2+B^2}}}{\omega_r} \tag{2.15}$$

2.2.2. Diode Conduction Stage

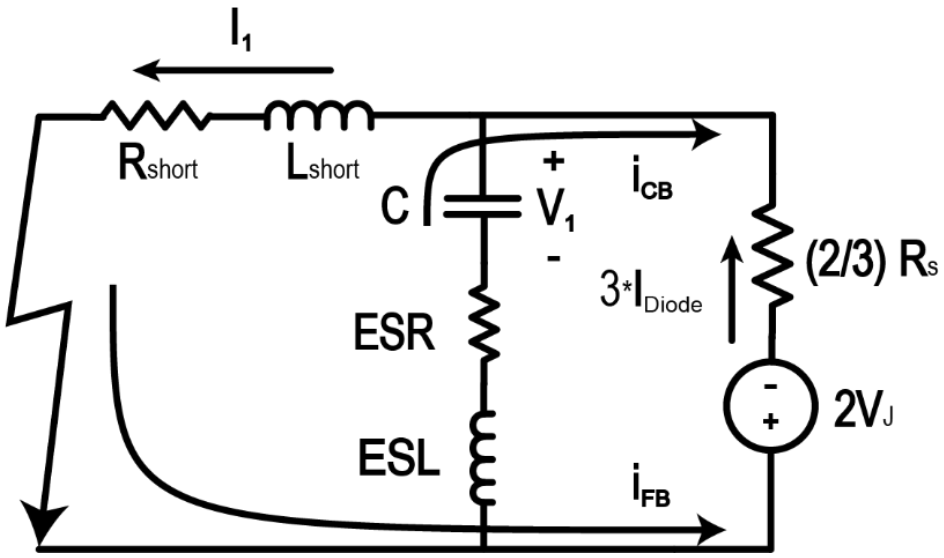
After the DC-link voltage reaches $-2Vj$, the remaining energy in the circuit start flowing through the diodes. The equivalent circuit of the converter in this stage is shown in Figure 2.4 (a), where the diodes are represented by their forward conduction equivalent circuits (turn-on voltage (V_j) in series with on-state resistance (R_S)). The circuit can be further simplified by taking the Thevenin equivalent of the converter diodes, as shown in Figure 2.4 (b). The initial fault bench current (I_1) and capacitor voltage (V_1) at the time boundary (t_b), can be found as:

$$I_1 = i_{DB}(t_b) \tag{2.16}$$

$$V_1 = V_0 - \frac{1}{C}\int_0^{t_b} i_{DB}(t)\, dt \tag{2.17}$$



(a)



(b)

Figure 2.4: (a) Equivalent circuit during diode conduction stage, and (b) further simplified circuit

In this stage, current through the diodes is sourced from two branches: the capacitor (*C*, *ESL*, *ESR*) and fault (R_{short} and L_{short}). In this section, current resulting from each branch is analysed separately and then combined to express the total current seen by the diodes.

A) Fault Branch Current

Using KVL around the outer closed circuit path containing $2V_j$, $(2/3)Rs$, R_{short} and L_{short} a general expression with respect to fault branch current (i_{FB}) can be found as:

$$R_{short}\, i_{FB} + L_{short}\frac{di_{FB}}{dt} + (2/3)\, R_s\, i_{FB} - 2\, Vj = 0 \tag{2.18}$$

which has a solution of the form [12]:

$$i_{FB}(t) = A_1\left(1 - e^{-t\,\frac{(2/3)\,R_s + R_{short}}{L_{short}}}\right) + A_2 e^{-t\,\frac{(2/3)\,R_s + R_{short}}{L_{short}}} \tag{2.19}$$

The constants A_1 and A_2 can be found from the initial and final conditions at ($t=0$) and ($t=\infty$) respectively:

$$i_{FB}\,(t = 0) = I_1 = A_2 \tag{2.20}$$

$$i_{FB}\,(t = \infty) = \frac{-2V_J}{(2/3)\,R_s + R_{short}} = A_1 \tag{2.21}$$

The resulting expression for the fault branch current after substituting A_1 and A_2 then becomes:

$$i_{FB}\,(t) = \frac{-2V_J}{(2/3)\,R_s + R_{short}}\left(1 - e^{-t\,\frac{(2/3)\,R_s + R_{short}}{L_{short}}}\right) + I_1\, e^{-t\,\frac{(2/3)\,R_s + R_{short}}{L_{short}}} \tag{2.22}$$

B) Capacitor Branch Current

Using KVL around the inner closed circuit path containing *ESL*, *ESR*, *C*, $(2/3)Rs$, and $2V_j$ a general expression with respect to the capacitor branch current (i_{CB}) can be found as:

$$\frac{di_{CB}}{dt}\, ESL + i_{CB}\, ESR + \int \frac{i_{CB}}{C}\, dt + i_{CB}\left(\frac{2}{3}\right) R_s - 2V_j = 0 \tag{2.23}$$

Like the RLC circuit described in section 2.2.1. , the solution for (2.23) also takes the form:

$$i_{CB}(t) = e^{-\beta t}(A_1\, cos\, \omega_r t + A_2\, sin\, \omega_r t) \tag{2.24}$$

where,

$$A_1 = I_1 \tag{2.25}$$

$$A_2 = \frac{V_1 - 2V_j}{\omega_r \, ESL} \tag{2.26}$$

$$\omega_o = \frac{1}{\sqrt{ESL \, C}} \tag{2.27}$$

$$\beta = \frac{ESR + \left(\frac{2}{3}\right) R_s}{2 \, ESL} \tag{2.28}$$

$$\omega_r = \sqrt{\omega_o^2 - \beta^2} \tag{2.29}$$

The final expression for the capacitor branch current after substituting A_1 and A_2 then becomes:

$$i_{CB}(t) = e^{-\beta t}(I_1 \cos \omega_r t + \frac{V_1 - 2V_j}{\omega_r ESL} \sin \omega_r t) \tag{2.30}$$

Total current through the diodes due to DC side contributions can then be expressed with respect to capacitor and fault branch currents ($i_{CB}(t)$ and $i_{FB}(t)$) as:

$$i_{D1}(t) = i_{D2}(t) = i_{D3}(t) = i_{D4}(t) = i_{D5}(t) = i_{D6}(t) = \frac{i_{FB}(t) - i_{CB}(t)}{3} \tag{2.31}$$

2.3. AC Side Contributions

In this section, expressions for AC side contributions represented by the phase currents ($i_a(t)$, $i_b(t)$, and $i_c(t)$) are derived. The equivalent circuit under this condition is shown in Figure 2.5 where the AC side is represented by three wye connected AC voltage sources ($v_a(t)$, $v_b(t)$, and $v_c(t)$) each in series with a line inductance and resistance (L_{Line} and R_{Line}). These inductances and resistances represent the windings of a generator, grid impedance, and/or AC line impedance. Whereas the three voltage sources represent the Back Electromotive Force (BEMF) voltages of a generator or grid voltage. It is assumed that under a DC short-circuit fault condition, the converter output impedance (R_{short} and L_{short}) is negligible compared to the AC line impedance (L_{Line} and R_{Line}). Therefore, analyses presented in this section disregard the converter by assuming ideal short-circuit paths across its AC terminals when deriving expressions for phase currents.

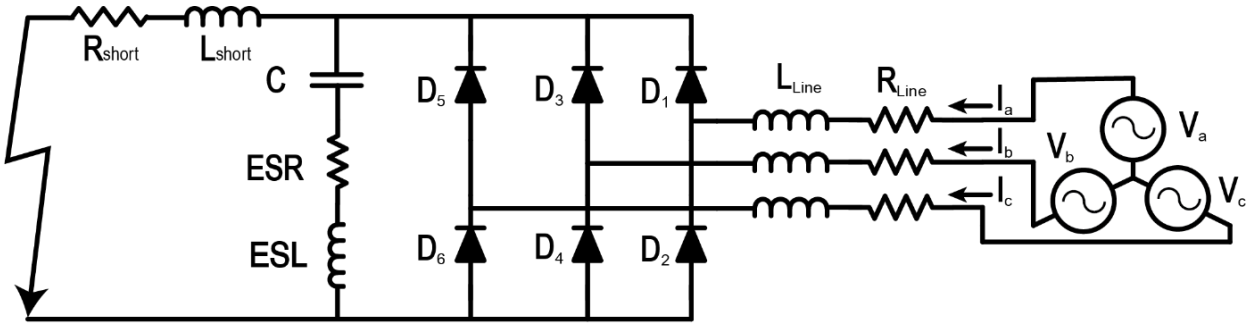


Figure 2.5: Schematic of equivalent AC side contribution circuit

2.3.1. Phase Currents Under Steady-State Condition

If the AC line-to-neutral voltages are defined as:

$$v_a(t) = V_m \, sin(\omega t) \tag{2.32}$$

$$v_b(t) = V_m \, sin(\omega t - 2\pi/3) \tag{2.33}$$

$$v_c(t) = V_m \, sin(\omega t - 4\pi/3) \tag{2.34}$$

where, ω is the line frequency and V_m is the peak line-to-neutral voltage, the steady-state phase currents can then be found as:

$$i_a(t) = \frac{V_m}{Z} \, sin(\omega t - \phi) \tag{2.35}$$

$$i_b(t) = \frac{V_m}{Z} sin(\omega t - 2\pi/3 - \phi) \tag{2.36}$$

$$i_c(t) = \frac{V_m}{Z} sin(\omega t - 4\pi/3 - \phi) \tag{2.37}$$

where,

$$Z = |\, j\omega L_{Line} + R_{Line}| = \sqrt{R_{Line}^2 + (\omega L_{Line})^2} \tag{2.38}$$

$$\phi = \angle(j\omega L_{Line} + R_{Line}) = tan^{-1} \frac{\omega L_{Line}}{R_{Line}} \tag{2.39}$$

2.3.2. Phase Currents Under Steady-State and Transient Condition

The AC side line-to-neutral voltages can be defined as:

$$v_a(t) = V_m \sin(\omega t + \alpha) \tag{2.40}$$

$$v_b(t) = V_m \sin(\omega t - 2\pi/3 + \alpha) \tag{2.41}$$

$$v_c(t) = V_m \sin(\omega t - 4\pi/3 + \alpha) \tag{2.42}$$

where, α is the V_a angle in radians at which the fault occurs, as illustrated in Figure 2.6.

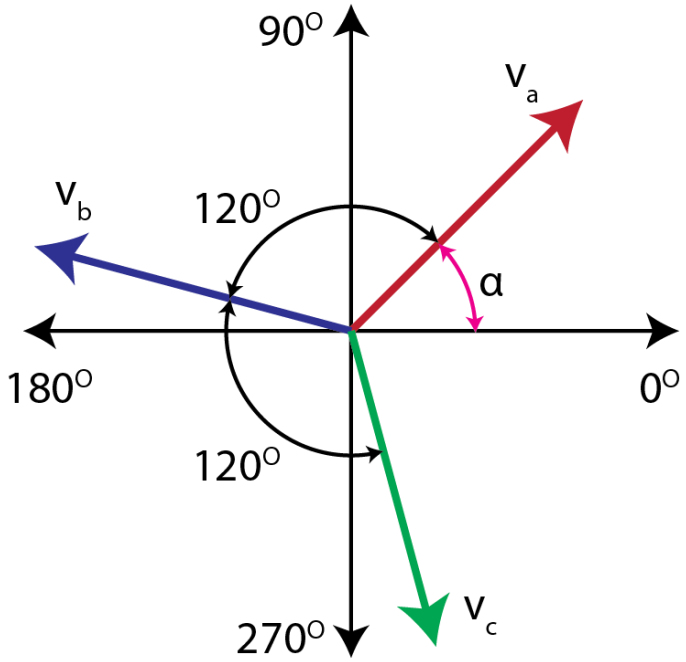


Figure 2.6:Phasor diagram at t=0 illustrating α

The complete response for the phase currents (transient and steady-state) then have the form:

$$i_a(t) = \frac{V_m}{Z} \sin(\omega t - \phi + \alpha) + A_1 \, e^{-t \frac{R_{Line}}{L_{Line}}} \tag{2.43}$$

$$i_b(t) = \frac{V_m}{Z} \sin(\omega t - 2\pi/3 - \phi + \alpha) + A_2 \, e^{-t \frac{R_{Line}}{L_{Line}}} \tag{2.44}$$

$$i_c(t) = \frac{V_m}{Z} \sin(\omega t - 4\pi/3 - \phi + \alpha) + A_3 \, e^{-t \frac{R_{Line}}{L_{Line}}} \tag{2.45}$$

The constants A_1, A_2, and A_3 can be found from the initial conditions. If the initial phase currents at $t = 0$ are defined as:

$$i_a(t=0) = I_{0a} = I_0\, sin(\alpha - \phi_0) \tag{2.46}$$

$$i_b(t=0) = I_{0b} = I_0\, sin(\alpha - 2\pi/3 - \phi_0) \tag{2.47}$$

$$i_c(t=0) = I_{0c} = I_0\, sin(\alpha - 4\pi/3 - \phi_0) \tag{2.48}$$

where, I_0 is the peak phase current, and ϕ_0 is the phase shift prior to the fault, A_1, A_2, and A_3 can then be found by substituting the initial conditions at *t=0* in (2.43) - (2.45) as:

$$A_1 = I_{0a} - \frac{V_m}{Z} sin(-\phi + \alpha) \tag{2.49}$$

$$A_2 = I_{0b} - \frac{V_m}{Z} sin(-2\pi/3 - \phi + \alpha) \tag{2.50}$$

$$A_3 = I_{0c} - \frac{V_m}{Z} sin(-4\pi/3 - \phi + \alpha) \tag{2.51}$$

The resulting expressions for phase currents after substituting A_1, A_2, and A_3 then become:

$$i_a(t) = \frac{V_m}{Z} sin(\omega t - \phi + \alpha) + \left(I_{0a} - \frac{V_m}{Z} sin(-\phi + \alpha)\right) e^{-t\frac{R_{Line}}{L_{Line}}} \tag{2.52}$$

(Steady-state) + (Transient)

$$i_b(t) = \frac{V_m}{Z} sin(\omega t - 2\pi/3 - \phi + \alpha) + \left(I_{0b} - \frac{V_m}{Z} sin(-2\pi/3 - \phi + \alpha)\right) e^{-t\frac{R_{Line}}{L_{Line}}} \tag{2.53}$$

$$i_c(t) = \frac{V_m}{Z} sin(\omega t - 4\pi/3 - \phi + \alpha) + \left(I_{0c} - \frac{V_m}{Z} sin(-4\pi/3 - \phi + \alpha)\right) e^{-t\frac{R_{Line}}{L_{Line}}} \tag{2.54}$$

Using phase currents information, currents through the converter diodes due to AC side contributions can be found. Phase currents are rectified through the diodes, such that positive portions of the phase currents flow through the top diodes (D1, D3, and D5), and the negative portions through the bottom diodes (D2, D4, and D6). This relationship between phase and diode current can be expressed as:

$$i_{D1}(t) = \begin{cases} i_a(t), & i_a(t) > 0 \\ 0, & i_a(t) \leq 0 \end{cases} \quad (2.55)$$

$$i_{D2}(t) = \begin{cases} 0, & i_a(t) \geq 0 \\ i_a(t), & i_a(t) < 0 \end{cases} \quad (2.56)$$

$$i_{D3}(t) = \begin{cases} i_b(t), & i_b(t) > 0 \\ 0, & i_b(t) \leq 0 \end{cases} \quad (2.57)$$

$$i_{D4}(t) = \begin{cases} 0, & i_b(t) \geq 0 \\ i_b(t), & i_b(t) < 0 \end{cases} \quad (2.58)$$

$$i_{D5}(t) = \begin{cases} i_c(t), & i_c(t) > 0 \\ 0, & i_c(t) \leq 0 \end{cases} \quad (2.59)$$

$$i_{D6}(t) = \begin{cases} 0, & i_c(t) \geq 0 \\ i_c(t), & i_c(t) < 0 \end{cases} \quad (2.60)$$

2.4. Combined AC and DC Side Contributions

After analyses of the AC and DC side contributions were presented separately in the previous sections, the combined/complete response due to both contributions is detailed in this section. First, initial conditions must by modified to account for the presence of both AC and DC side contributions. Specifically, the initial capacitor branch current was assumed to be equal to that of the fault branch (both I_0). However, when considering the combined response, initial rectified AC side current (I_{S0}) should also be taken into account, as illustrated in Figure 2.7. The initial capacitor current (I_{Cap0}) is then equal to the difference between the fault branch and rectified AC side initial currents ($I_0 - I_{S0}$).

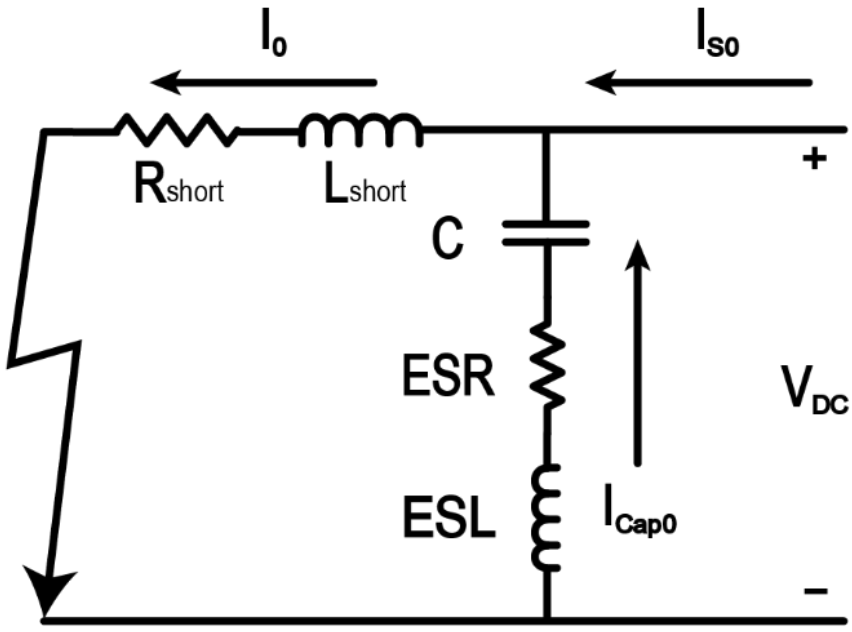


Figure 2.7: illustration of initial currents on DC side accounting for rectified AC side current

2.4.1. DC-Link Voltage Considering Both AC and DC Side Contributions

The expression derived in the DC side contributions section provides a good approximation of the DC-link voltage irrespective of the AC side contributions. This is because under a DC line-to-line short-circuit fault condition, the bus voltage is supported by the DC-link capacitor (DC side contribution) and not the AC source. The AC source is not capable of supporting the DC-link voltage because the AC line impedance (L_{Line} and R_{Line}) is significantly larger than the output impedance of the converter (L_{short} and R_{short}). In other words, the AC side impedances limit the maximum amounts of phase currents that can be supplied to the converter. Although these phase currents can be large under a DC line-to-line fault condition, they are not capable of supporting the DC-link voltage.

2.4.2. Phase Currents Considering Both AC and DC Side Contributions

Due to the presence of an initially large DC-link voltage, the AC side does not immediately begin conducting phase currents as defined in the AC contributions section. Instead, the converter goes through a transitional period where the phase currents are proportional to the DC-link voltage. The per-phase equivalent circuit during this transition stage is shown in Figure 2.8. An illistartion of phase current commutation stages is shown in Figure 2.9.

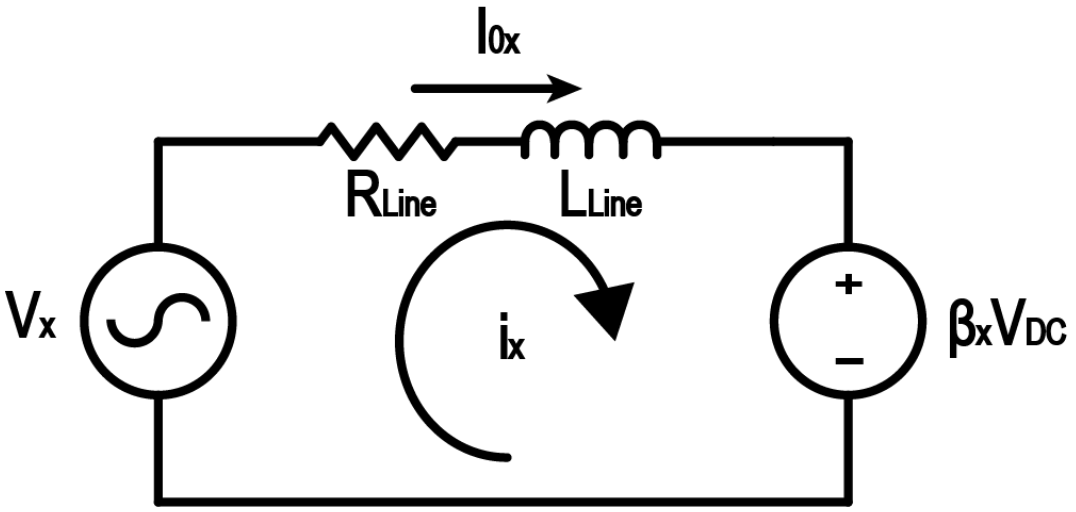


Figure 2.8: Equivalent circuit during phase currents transition stage

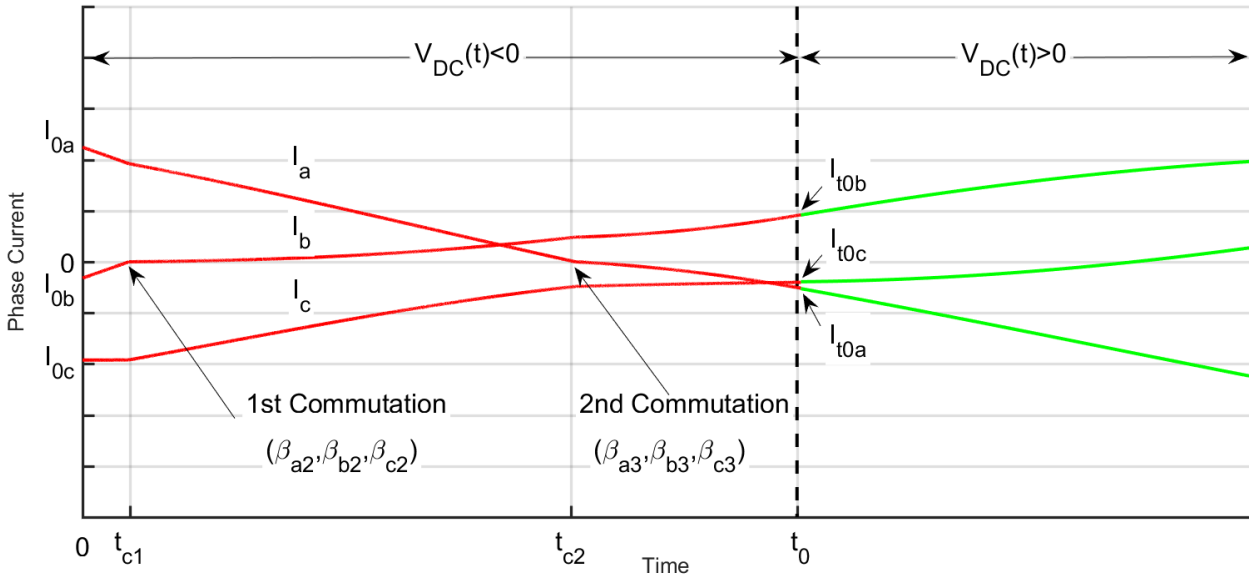


Figure 2.9: Illistartion of phase current commutation stages

In Figure 2.8, x represents phases a, b, or c, V_x is the line-to-neutral voltage of the corresponding phase, V_{DC} is the DC-link voltage, and β is a commutation-state dependent coefficient, which can be calculated from Table 2.1 or (2.61).

Table 2.1: β_x per commutation state ($sgn(i_a(t))$, $sgn(i_b(t))$, and $sgn(i_c(t))$)

$sgn(i_a(t))$	$sgn(i_b(t))$	$sgn(i_c(t))$	β_a	β_b	β_c
+	+	-	$1/3$	$1/3$	$-2/3$
-	+	+	$-2/3$	$1/3$	$1/3$
+	-	+	$1/3$	$-2/3$	$1/3$
-	-	+	$-1/3$	$-1/3$	$2/3$
+	-	-	$2/3$	$-1/3$	$-1/3$
-	+	-	$-1/3$	$2/3$	$-1/3$

$$\beta_x(\mathrm{t}) = \frac{sgn(i_x(\mathrm{t}))}{3}\Big(\big(sgn(i_x(\mathrm{t})) \neq sgn(i_y(\mathrm{t}))\big) + \big(sgn(i_x(\mathrm{t})) \neq sgn(i_z(\mathrm{t}))\big)\Big) \tag{2.61}$$

where *x*, *y*, and *z* represent phases *a*, *b*, or *c*, and $x \neq y \neq z$.

Phase current ($i_x(t)$) can be found by applying KVL around the closed circuit path shown in Figure 2.8, which yields the expression:

$$-V_x + R_{Line} i_x + L_{Line} \frac{di_x}{dt} + \beta_x V_{DC} = 0 \tag{2.62}$$

An approximate solution for $i_x(t)$ can be found by integrating (2.62), such that:

$$i_x(t) = I_{0x} + \frac{1}{L_{Line}} \int_0^t V_x(t) - \beta_x \, V_{DC}(t) \, dt \tag{2.63}$$

This solution disregards the resistive term due to its small influence in this fast-transient stage.

As phase currents flow through the converter, it is possible for them to change signs, such that the effective DC voltage seen by the AC side ($\beta_x V_{DC}(t)$) changes. This change is due to the dependency of β_x on the commutation state ($sgn(i_a(t))$, $sgn(i_b(t))$, and $sgn(i_c(t))$). A commutation occurs when any of the line currents ($i_x(t)$) changes signs from its initial value's (I_{0x}) sign, as:

$$sgn(i_x(t)) \neq sgn(I_{0x}) \tag{2.64}$$

The time at which commutation occurs (t_c) is defined as the time at which any of the phase currents is zero:

$$i_x(t = t_c) = 0 \tag{2.65}$$

It is possible to modify (2.63) to accommodate multiple commutation state coefficients (β_{x1}, β_{x2}, etc..). Phase currents before commutation ($t < t_c$) can still be as expressed by (2.63) with a commutation state coefficient of β_{x1}. Whereas, phase currents after the commutation ($t > t_c$) include an additional integration period from t_c to t with a commutation state coefficients of β_{x2}.

$$i_x(t) \tag{2.66}$$
$$= \begin{cases} I_{0x} + \dfrac{1}{L_{Line}} \displaystyle\int_0^t V_x(t) - \beta_{x1}\, V_{DC}(t)\, dt & , t < t_c \\ I_{0x} + \dfrac{1}{L_{Line}} \displaystyle\int_0^{t_c} V_x(t) - \beta_{x1} V_{DC}(t) dt + \dfrac{1}{L_{Line}} \displaystyle\int_{t_c}^t V_x(t) - \beta_{x2} V_{DC}(t) dt & , t > t_c \end{cases}$$

where β_{x1} and β_{x2} are found using Table 2.1 or (2.61).

It is also possible that the line-to-neutral AC side voltages of any of the phases ($V_x(t)$) to be less than the effective DC voltage seen by the AC side ($\beta_x V_{DC}(t)$), as:

$$|V_x(t)| < |\beta_{x2} V_{DC}(t)| \tag{2.67}$$

During this period, the diodes do not conduct current from this phase ($i_x(t)$), as:

$$i_x(t) = 0 \tag{2.68}$$

Current through the other two phases ($i_y(t)$ and $i_z(t)$), can be given as:

$$i_y(t) = I_{0y} + \frac{1}{L_{Line}} \int_0^{t_c} V_y(t) - \beta_{y1} V_{DC}(t) dt + \frac{1}{L_{Line}} \int_{t_c}^t V_y(t) - 1/2(V_{DC}(t) - V_x(t))\, dt, for\ i_y(t) > 0 \tag{2.69}$$

$$i_z(t) = I_{0z} + \frac{1}{L_{Line}} \int_0^{t_c} V_z(t) - \beta_{z1} V_{DC}(t)\, dt + \frac{1}{L_{Line}} \int_{t_c}^t V_z(t) + 1/2(V_{DC}(t) + V_x(t))\, dt, for\ i_z(t) < 0 \tag{2.70}$$

Finally, expressions for phase currents after the transition period ($t > t_0$) can be found by modifying (2.40) - (2.42) so that the boundary conditions are defined at $t = t_0$ instead of $t = 0$. If the phase currents when t=t_0 are found from (2.61) - (2.70) as:

$$i_a(t = t_0) = I_{t_0 a} \tag{2.71}$$

$$i_b(t = t_0) = I_{t_0 b} \tag{2.72}$$

$$i_c(t = t_0) = I_{t_0 c} \tag{2.73}$$

the constants $A_1, A_2,$ and A_3 can be re-derived by substituting the new initial conditions at $t = t_0$ in (2.40) - (2.42), as:

$$A_1 = (I_{t_0 a} - \frac{V_m}{Z} sin(\omega t_0 - \phi + \alpha))/e^{-t_0 \frac{R_{Line}}{L_{Line}}} \tag{2.74}$$

$$A_2 = (I_{t_0 b} - \frac{V_m}{Z} sin(\omega t_0 - 2\pi/3 - \phi + \alpha))/e^{-t_0 \frac{R_{Line}}{L_{Line}}} \tag{2.75}$$

$$A_3 = (I_{t_0 c} - \frac{V_m}{Z} sin(\omega t_0 - 4\pi/3 - \phi + \alpha))/e^{-t_0 \frac{R_{Line}}{L_{Line}}} \tag{2.76}$$

The expressions for phase currents after the transition period ($t > t_0$) can then be given as:

$$i_a(t) = \frac{V_m}{Z} sin(\omega t - \phi + \alpha) + (I_{t_0 a} - \frac{V_m}{Z} sin(\omega t_0 - \phi + \alpha))\, e^{(-t+t_0)\frac{R_{Line}}{L_{Line}}} \tag{2.77}$$

$$i_b(t) = \frac{V_m}{Z} sin\left(\omega t - \frac{2\pi}{3} - \phi + \alpha\right) + (I_{t_0 b} - \frac{V_m}{Z} sin\left(\omega t_0 - \frac{2\pi}{3} - \phi + \alpha\right))\, e^{(-t+t_0)\frac{R_{Line}}{L_{Line}}} \tag{2.78}$$

$$i_c(t) = \frac{V_m}{Z} sin\left(\omega t - \frac{4\pi}{3} - \phi + \alpha\right) + (I_{t_0 c} - \frac{V_m}{Z} sin\left(\omega t_0 - \frac{4\pi}{3} - \phi + \alpha\right))\, e^{(-t+t_0)\frac{R_{Line}}{L_{Line}}} \tag{2.79}$$

2.4.3. Fault Branch Current Considering Both AC and DC Side Contributions

Fault branch current (i_{FB}) can still be obtained from (2.22), with the initial condition (I_1) modified to account for AC side contributions. When considering AC side contributions, I_1 becomes composed of three elements: the initial current seen by the fault branch (I_0), the contribution of capacitor branch obtained from (2.16) setting $I_0 = I_{cap0}$, and the rectified source current ($I_s(t_b)$) found from (2.77) - (2.79), as described by (2.80).

$$I_1 = I_0 + I_s(t_b) + i_{DB}(t = t_b, I_0 = I_{cap0}) \tag{2.80}$$

2.4.4. Capacitor Branch Current Considering AC and DC Side Contributions

The capacitor branch current (i_{CB}) can still be calculated from (2.30), with the initial condition modified to account for the AC side contributions. As discussed at the beginning of this section, the initial current of the capacitor branch considering AC side contributions (I_{cap0}) is equal to ($I_0 - I_{S0}$).

2.4.5. Diodes Currents Considering AC and DC Side Contributions

As discussed earlier, during the diode blocking stage, there is no current flow through the diodes due to the DC side contributions. Therefore, only AC side currents flow through the diodes during this stage, according to (2.55) - (2.60). However, during the diode conduction stage ($t > t_b$), the diodes conduct both AC and DC contributed currents, according to the equivalent circuit shown in Figure 2.10. Combined (AC and DC side) currents seen by the upper (D1, D3, and D5) and lower (D2, D4, and D6) diodes are expressed by (2.81) and (2.82) respectively.

$$i_{DU}(t) = \frac{i_{FB}(t) - i_{CB}(t)}{3} + \frac{i_x(t)}{2} \tag{2.81}$$

$$i_{DL}(t) = \frac{i_{FB}(t) - i_{CB}(t)}{3} - \frac{i_x(t)}{2} \tag{2.82}$$

where, $i_x(t)$ is the current of the corresponding phase ($x = a$ for D1/D2, $x = b$ for D3/D4, and $x = c$ for D5/D6).

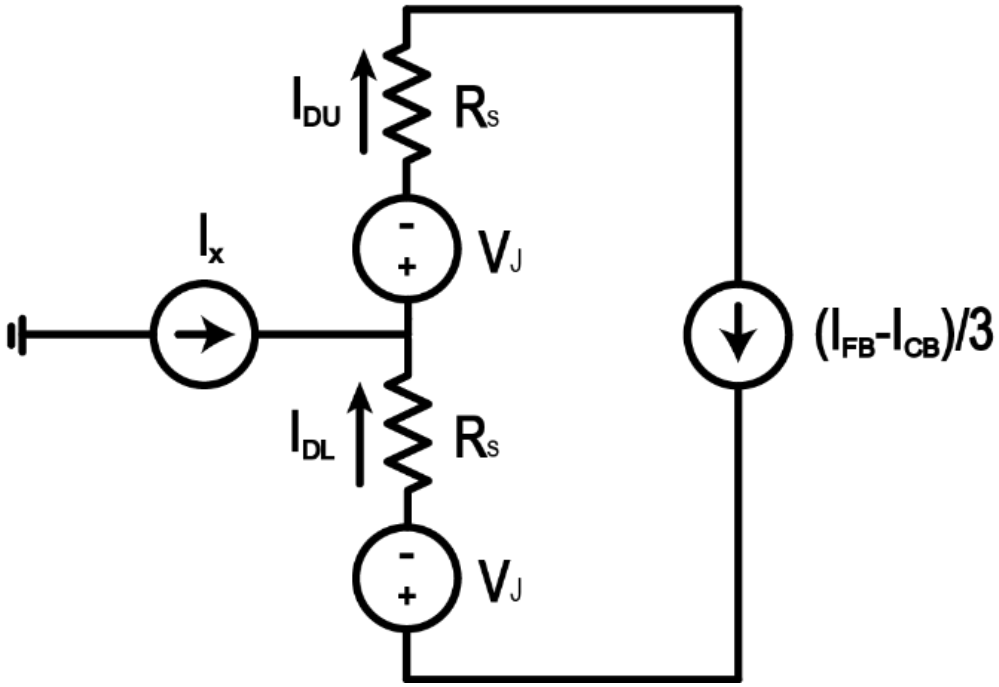


Figure 2.10: equivalent diode conduction circuit accounting for both AC and DC side contributions

After current through the diodes due to DC side contributions decay to zero, the diodes return to conducting AC side contributions only, according to (2.55) - (2.60).

2.5. Simulation Validation of Short-Circuit Fault Analyses

In this section, the analyses presented in the previous sections are validated against SPICE simulations of a single-channel equivalent of a 100kW dual-channel motor drive designed and built for aerospace application. The parameters used for this simulation are summarised in Table 2.2.

Table 2.2: Summary of simulation parameters

Component	Parameter	Value
Converter nominal output levels	Power (kW)	50
	Voltage (V DC)	±270 (540)
	Current (A)	92.6
DC-link capacitor [13]	Capacitance (μF)	500
	ESL (nH)	5
	ESR (mΩ)	1.7
Permanent magnet machine	Line Inductance (μH)	36.22
	Line Resistance (mΩ)	3.05
	Peak BEMF phase voltage at max speed (V)	208 at 26,584rpm
	Peak BEMF phase voltage at idle speed (V)	121.24 at 14,666rpm
	Number of poles	8
Fault characteristics	Cable size (AWG/ømm)	2/6.54
	Cable length (m)	0.5-5
Semiconductor module [14]	Diode turn-on voltage V_J (V)	1.3
	Diode on-state resistance R_s (mΩ)	1.87

2.5.1. Extraction of Fault Impedance Parameters

A) Cable Size

A cable size of 2 AWG (diameter of 6.54 mm) is selected according to MIL-STD-975, which specifies a maximum current of 108A at up to 70°C for this gauge, as shown in Table 2.3.

Table 2.3: Recommended cable size and maximum current at up to 70°C (from MIL-STD-975)

Wire size (AWG)	Wire diameter (mm)	Maximum current at up to 70°C
14	1.62	19.0
12	2.05	25.0
10	2.59	33.0
8	3.26	44.0
6	4.12	60.0
4	5.19	81.0
2	6.54	108.0
0	8.25	147.0
00	9.27	169.0

B) Cable Inductance

The self-inductance in micro-henry of a cable with length (L) and radius (r) in meters can be expressed as [15]:

$$L_{self} = 0.2L\left[ln\frac{2L}{r} - \frac{3}{4}\right](\mu H) \tag{2.83}$$

The self-inductance of a 2 AWG cable is plotted vs. length in Figure 2.11.

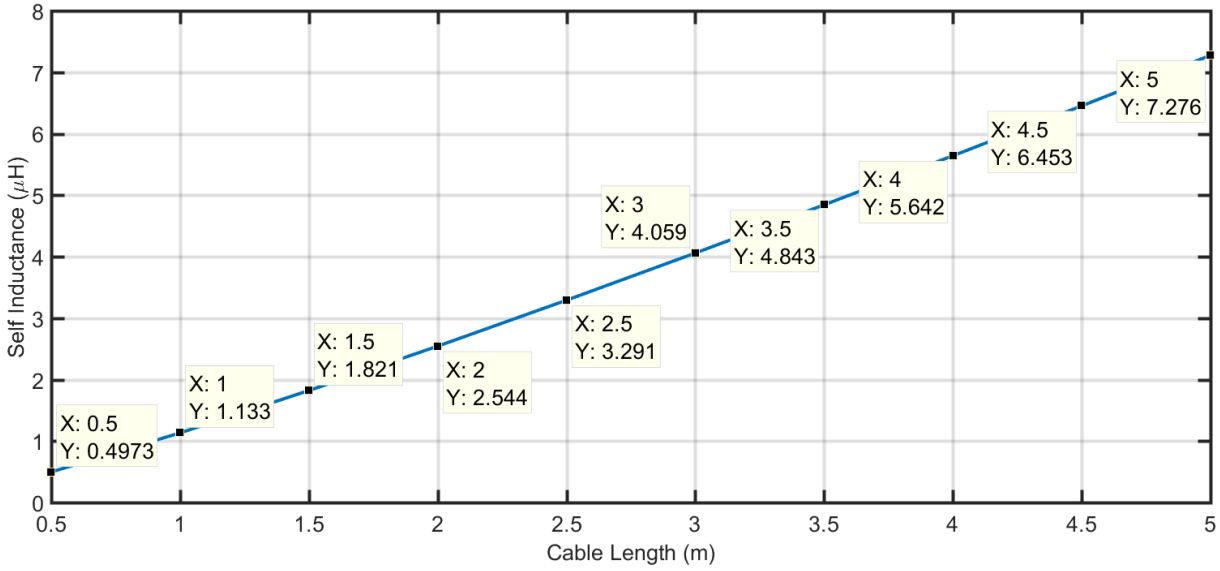


Figure 2.11: Self-inductance vs. cable length for 2 AWG cable

Whereas, the mutual-inductance in micro-henry between two cables of lengths (L) and distance between centres (D) can be expressed as [15]:

$$M = \frac{\mu L}{2\pi}\left[ln\left(\frac{L}{D} + \sqrt{1 + \left(\frac{L}{D}\right)^2}\right) - \sqrt{1 + \left(\frac{D}{L}\right)^2} + \frac{D}{L}\right](H) \tag{2.84}$$

where μ is the permeability of the medium between the cables.

The total inductance of two cables with self-inductance L_{self} and mutual-inductance M forming a return path can then be expressed as [15]:

$$L_{Total} = 2(L_{self} - M) \tag{2.85}$$

C) Cable Resistance

The resistance of the cable per unit length in Ω/meter can be found from [13]:

$$\frac{R}{L} = \frac{\rho}{A} \tag{2.86}$$

where ρ is the resistivity of the material in Ω.meter, and A is the cross-sectional area of the conductor in meters^2.

Assuming a copper conductor with resistivity of 1.68x10^{-8} ohms/meter and wire core diameter of 6.54mm (2 AWG), the resistance per unit length can then be found as:

$$\frac{R}{L} = \frac{1.68\,x10^{-8}}{\pi\,(3.3x10^{-3})^2} = 0.5\frac{m\Omega}{meter} \tag{2.87}$$

2.5.2. Extraction of Diodes SPICE Parameters

In SPICE, diodes are represented by the Schockly diode equation [12].

$$I_D = I_S\,(e^{\frac{V_D}{nV_T}} - 1) \tag{2.88}$$

where, I_D, I_S, V_D, n, and V_T are the diode's current, leakage current, voltage, emission coefficient, and thermal voltage (25.7mV at 25°C) respectively.

In addition, a series resistance parameter (R_s) can be specified such that the voltage across the diode and resistor combination (now called V_D') is [12].

$$V_D' = V_D + I_D\,R \tag{2.89}$$

Expressions (2.88) and (2.88) were found to best fit the diode parameters listed in Table 2.2, when *n=2*, *Rs=1.74mΩ*, and *Is=1nA*, as demonstrated in Figure 2.12.

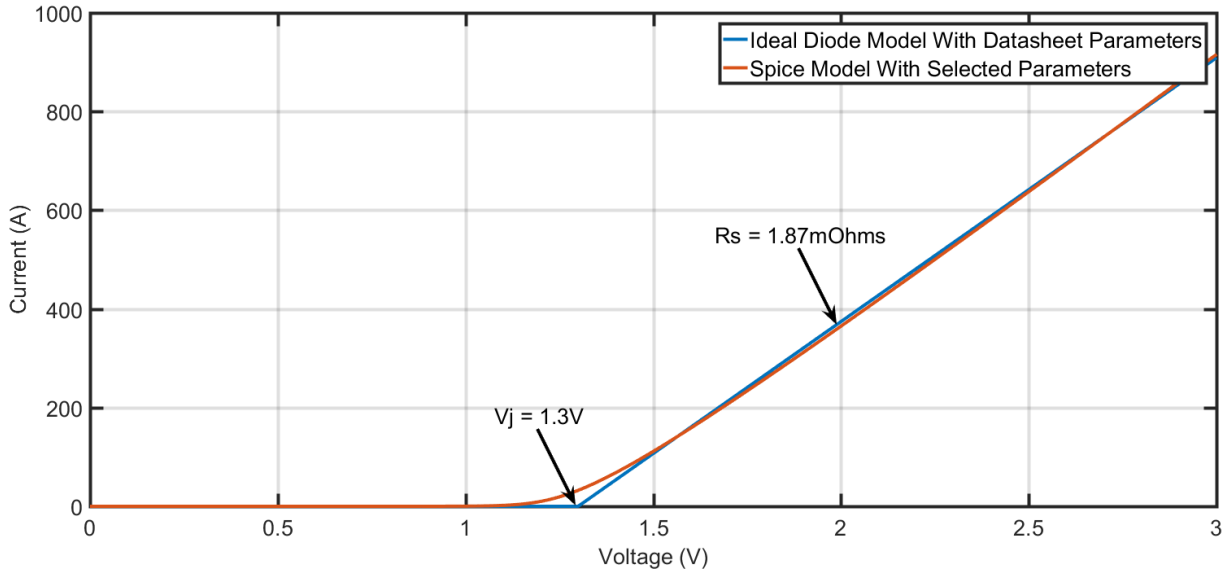


Figure 2.12: Ideal diode with datasheet parameters vs. spice diode with selected parameters

2.5.3. Simulation Analyses of DC Side Contributions

In this section, analytical results of DC side contributions are validated against simulations of the circuit shown in Figure 2.13. The initial capacitor voltage and inductors currents (V_0 and I_0) are set to 540V and 92.6A respectively using ".ic" commands. Whereas, *C*, *ESL*, and *ESR* parameters are set according to Table 2.2. The short-circuit path's inductance and resistance parameters are assumed to be the self-inductance and resistance of a 2 AWG cable, as calculated in **Error! Reference source not found.**. The length of this cable is varied from 0.5 to 5m at steps of 0.5m. The simulated fault current (I_{Fault}) is shown in Figure 2.14, where the arrow indicates increasing cable lengths from 0.5 to 5m at steps of 0.5m. The minimum cable length of 0.5m was specified by Rolls-Royce plc based on the assumption that this length of cable would be internal to the jet engine casing. For this length of cables, the positive and return wires would be routed separately to insure no line-to-line fault condition would occur.

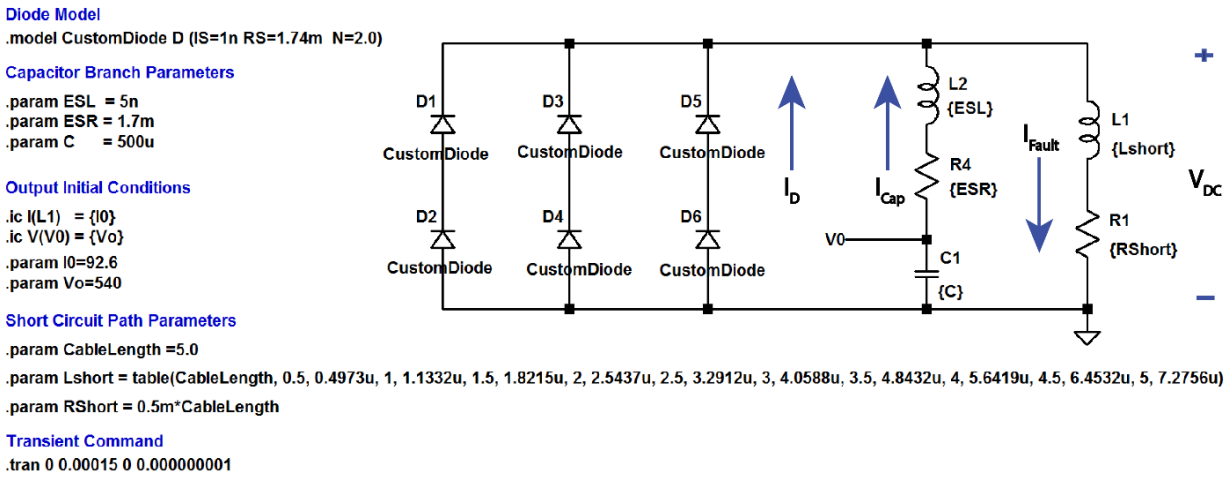


Figure 2.13: Schematic of DC side contributions simulation circuit

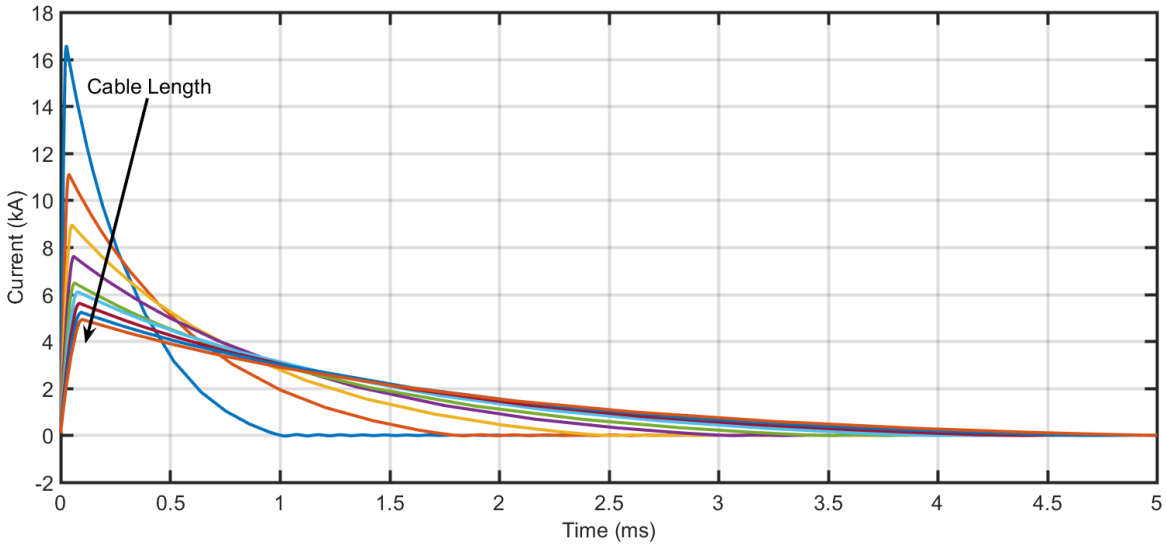


Figure 2.14: Simulated fault current (I_{Fault}) for 0.5m-5m cable fault with 0.5m steps

Simulation results demonstrate that cable length significantly influences peak fault current and settling time. Fault current is proportional to $e^{-\beta t}$ according to (2.9) such that a shorter cable with lower damping factor (β) would results in exponentially higher peak value. The time constant for the fault current (time to reach 36.8% of its maximum value) can be found from (2.19) to be $L_{short}/((2/3)R_s + R_{short})$. While $R_{short}$is linearly proportional to cable length, L_{short} decreases more rapidly as shown in Fig. 2.9. Furthermore, due to the presence of $((2/3)R_s)$ factor in the denominator, the settling time decreases faster as cable length become shorter.

The analytical results for the fault path's current during the diode blocking stage (I_{DB}) obtained from (2.9) were compared with those from simulation at the maximum and minimum cable lengths of 0.5m and 5m respectively. It can be seen from Figure 2.15 that the analytical results match simulation very well, up until the boundry condition given by (2.15) and calculated to be 24.538µs and 94.039µs for the 0.5m and 5m cable lengths respectively.

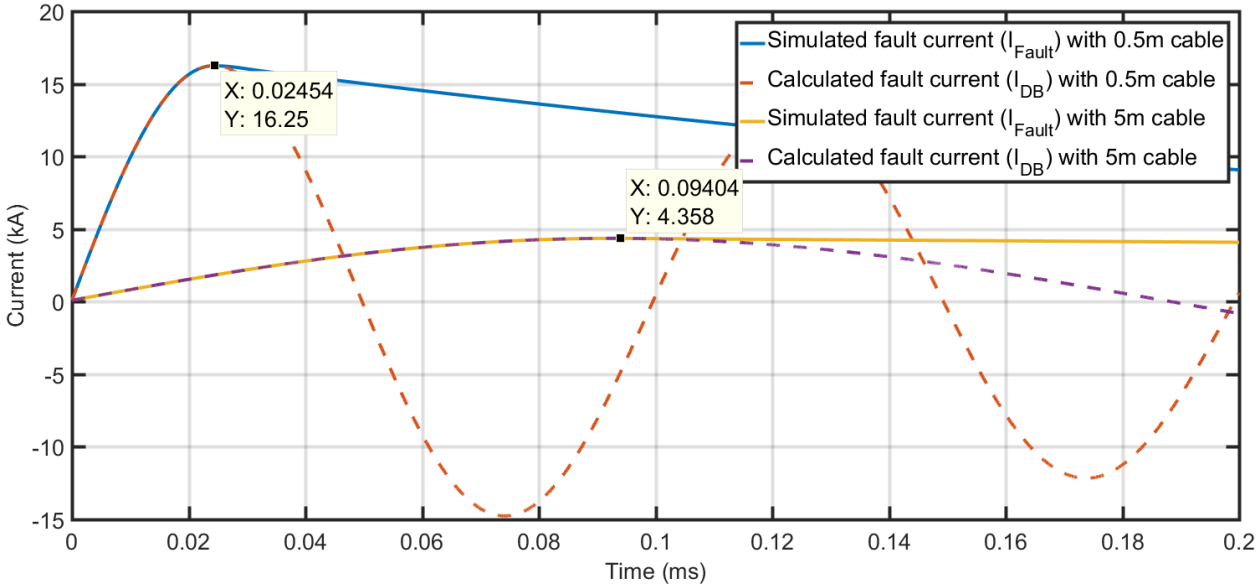


Figure 2.15: Comparison of simulated and calculated fault current (I_{Fault}) during diode blocking stage

Analytical results of the DC-link voltage obtained from (2.11) were also compared to simulation results (V_{DC}) at the two cable lengths, as shown in Figure 2.16. The time at which the DC- link voltage reaches zero, was calculated from (2.14) to be 24.458µs and 93.741µs for the 0.5m and 5m cable lengths respectively. It can be seen from the data points on the figure that the approximations for the time boundary (t_b) at which the DC-link voltage reaches $-2V_j$ (or -2.6V for the diode considered in this work) are almost exact.

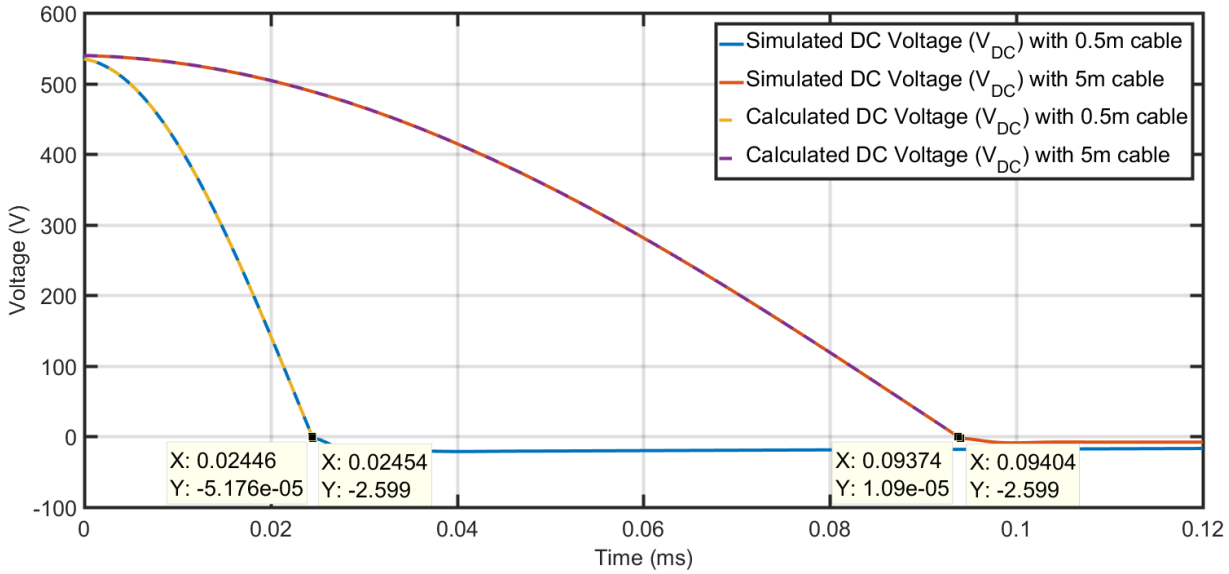


Figure 2.16: Comparison of simulated and calculated DC-link voltage (V_{DC})

After the time boundary is reached ($t > t_b$), the diodes become forward biased. In this stage, current is supplied from two sources, the fault branch (i_{FB}) and the capacitor branch (i_{CB}). The contribution of the fault branch expressed by (2.22) matches simulation very well, as shown in Figure 2.17. The initial current (I_1) was calculated from (2.16) to be 16.25kA and 4.357kA for the 0.5m and 5m cable lengths respectively.

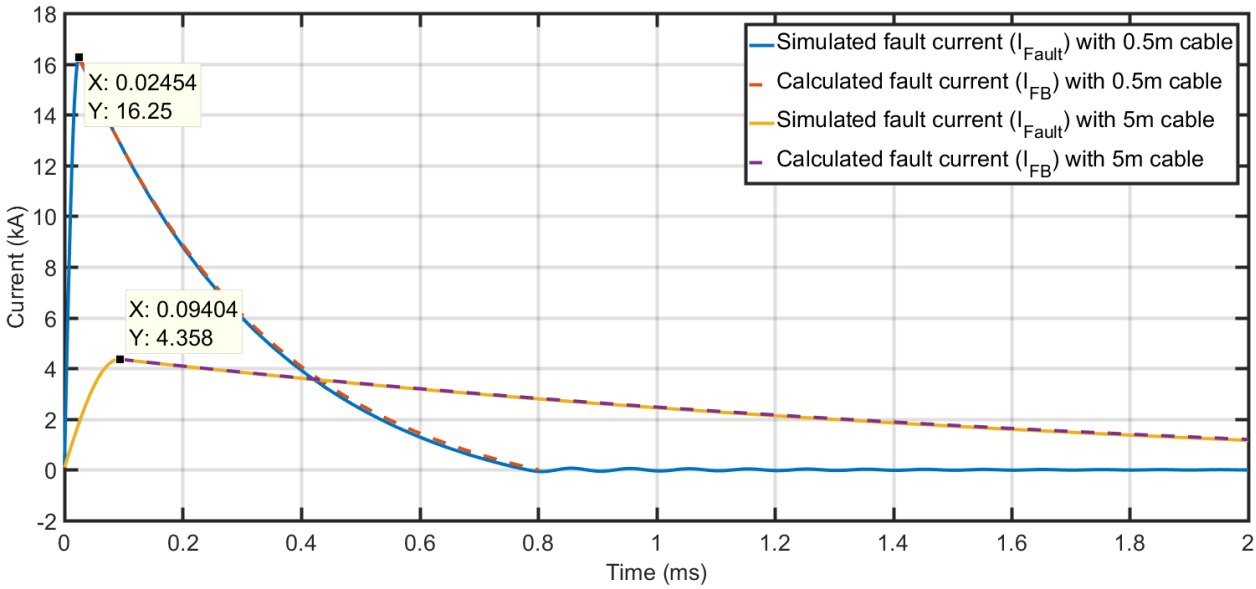


Figure 2.17: Comparison of simulated and calculated fault branch current during diode conduction stage

The contribution of the capacitor branch in this stage (i_{CB}) as given by (2.30), with an initial capacitor voltage calculated using (2.17) to be 26.12V and 4.95V for the two cable length respectively, was also compared to simulations and shows good matching, as demonstrated in Figure 2.18.

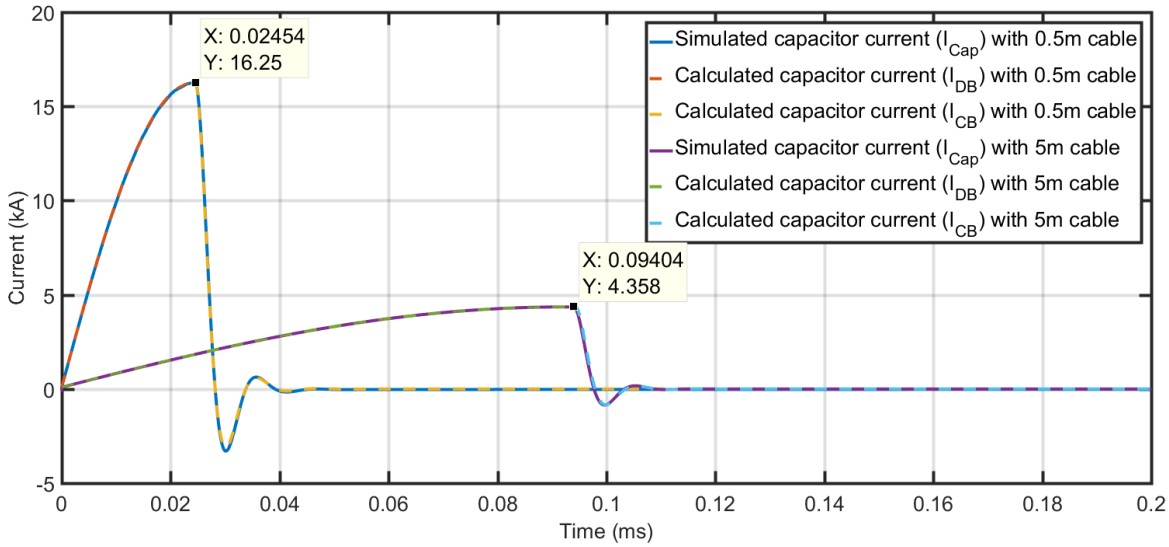


Figure 2.18: Comparison of simulated and calculated capacitor branch current during diode conduction and blocking stages

Finally, diodes currents calculated from i_{CB} and i_{DB} according to (2.31), were compared with simulation results as shown in Figure 2.19 and Figure 2.20.

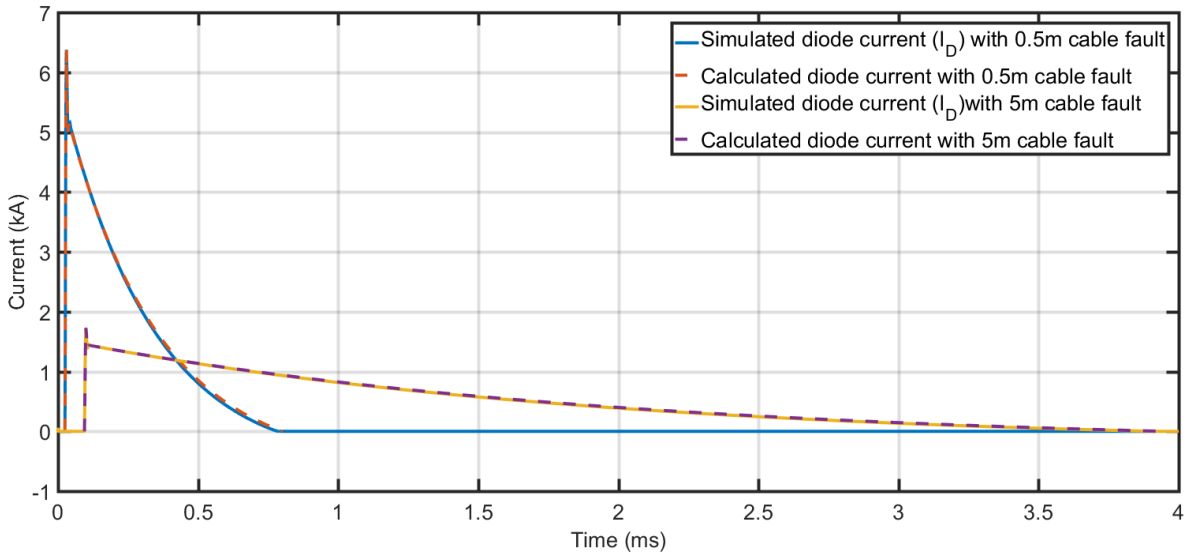


Figure 2.19: Comparison of simulated and calculated diodes current during diode conduction stage

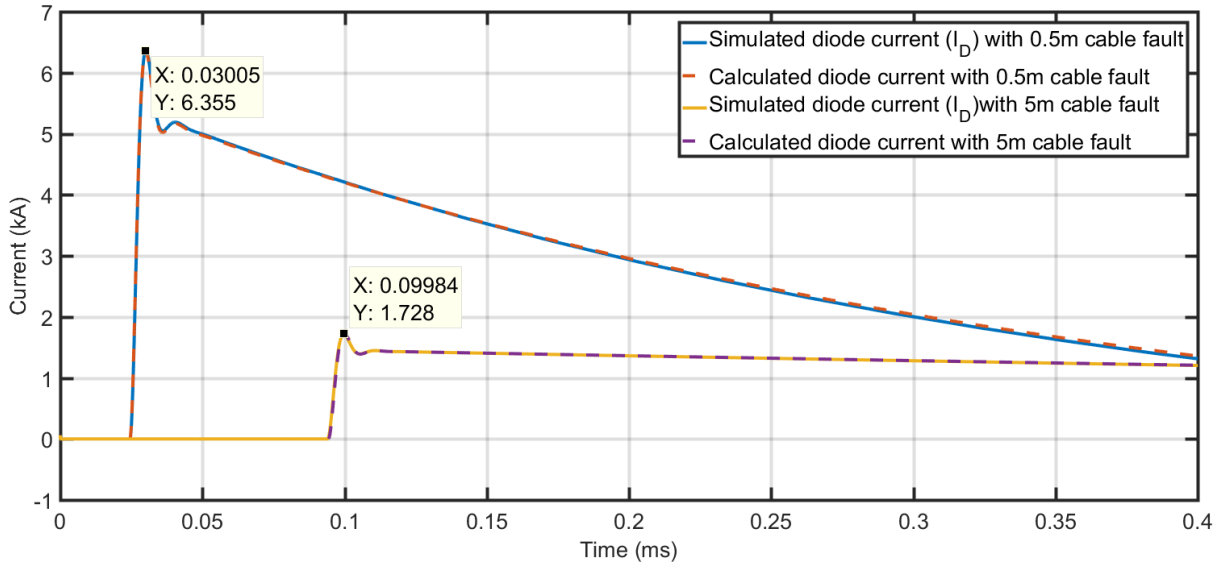


Figure 2.20: Comparison of simulated and calculated diode current during diode conduction stage (Enlarged)

2.5.4. Simulation Analysis of AC Side Contributions

A) Steady-State Phase Currents

Steady-state phase currents calculated from (2.35) - (2.37) were compared to simulation results obtained for the circuit with the schematic shown in Figure 2.21. The comparison was performed at the maximum and minimum machine speeds and for cable lengths of 0.5m and 5m, as shown in Figure 2.22-2.26. Parameters "*Speed*" and "*CableLength*" are changed according to the desired simulation scenario. The figures demonstrate excellent matching (within 5%) between analytical and simulation results at both the maximum and idle speeds and at both cable lengths. For all conditions, the simulation results are shown for an alpha angle of 0°. At other alpha angles, phase currents would be identical in magnitude and frequency but advanced by alpha. For example, an alpha angle of 90° would advance phase A current at idle speed by 255.7μs.

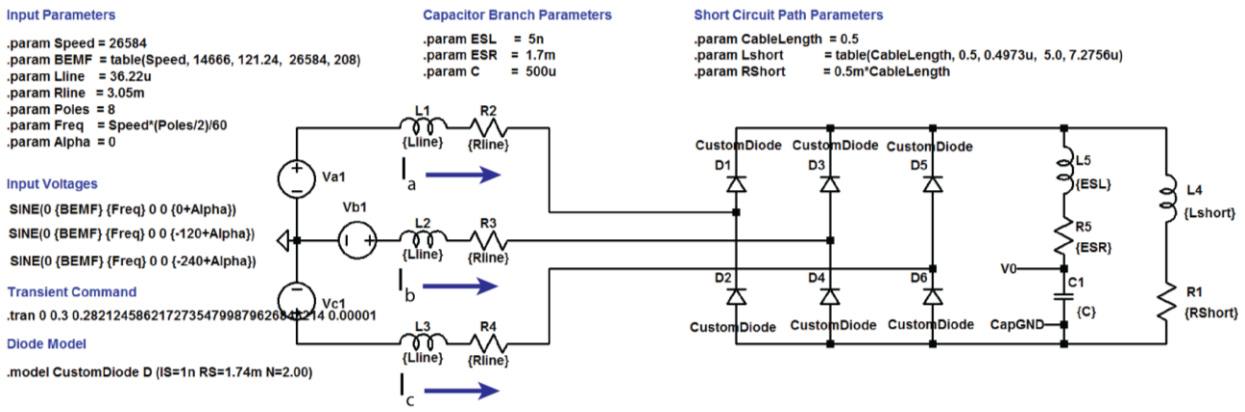


Figure 2.21: Steady-state response simulation circuit showing 26,584RPM (max speed) and 0.5m cable fault case

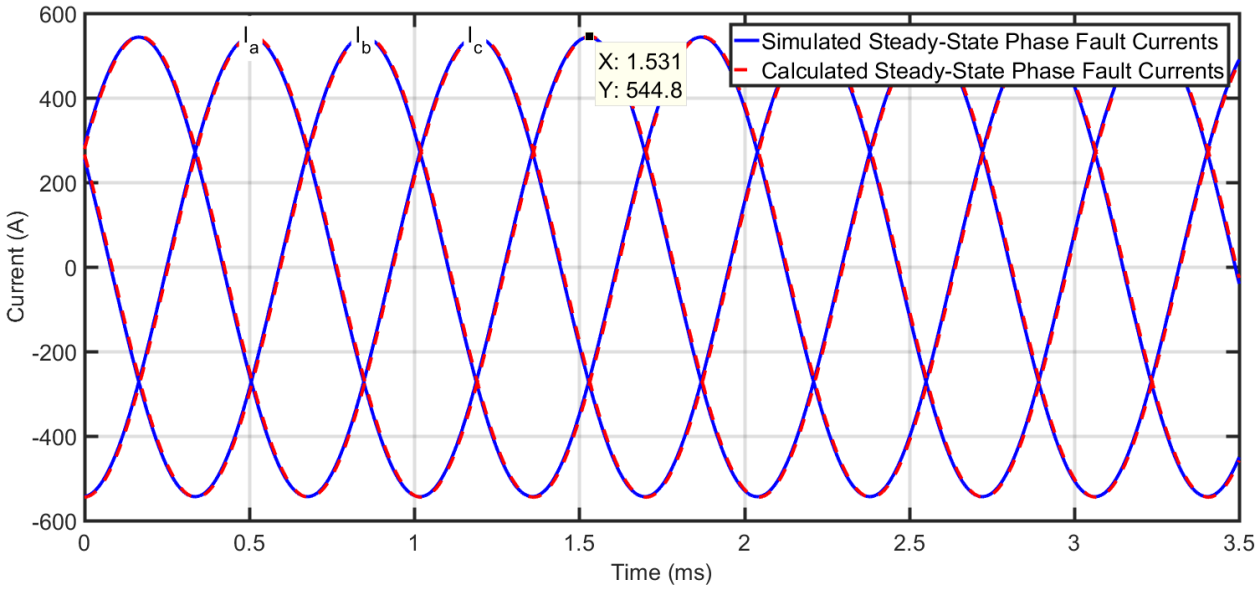


Figure 2.22: Comparison of simulated and calculated steady-state phase currents for 0.5m cable fault at idle speed

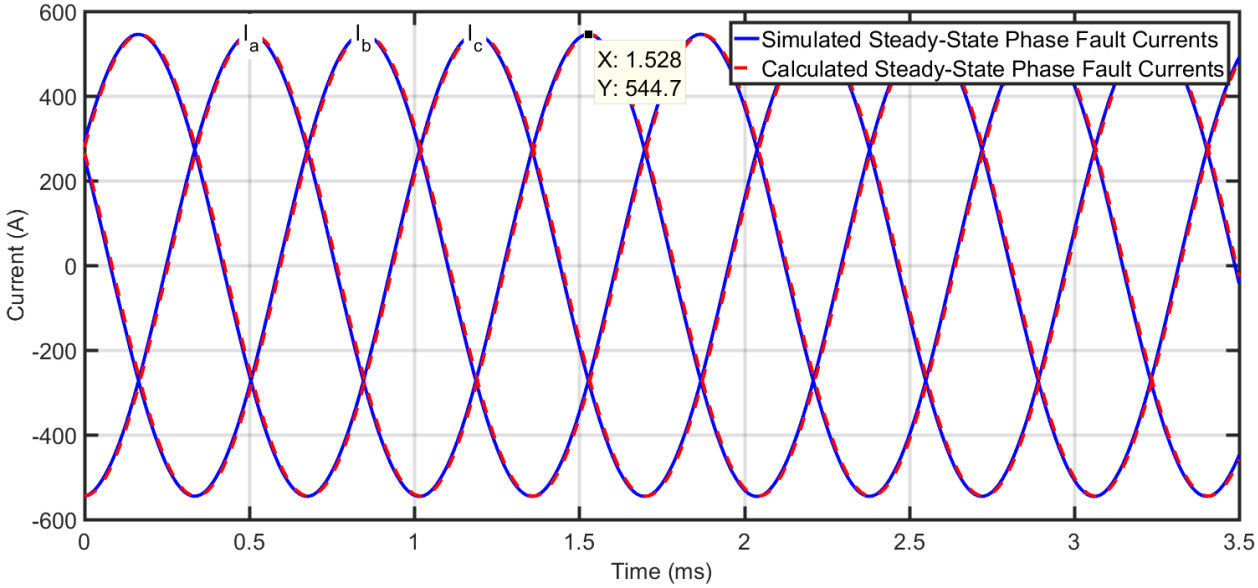


Figure 2.23: Comparison of simulated and calculated steady-state phase current for 5m cable fault at idle speed

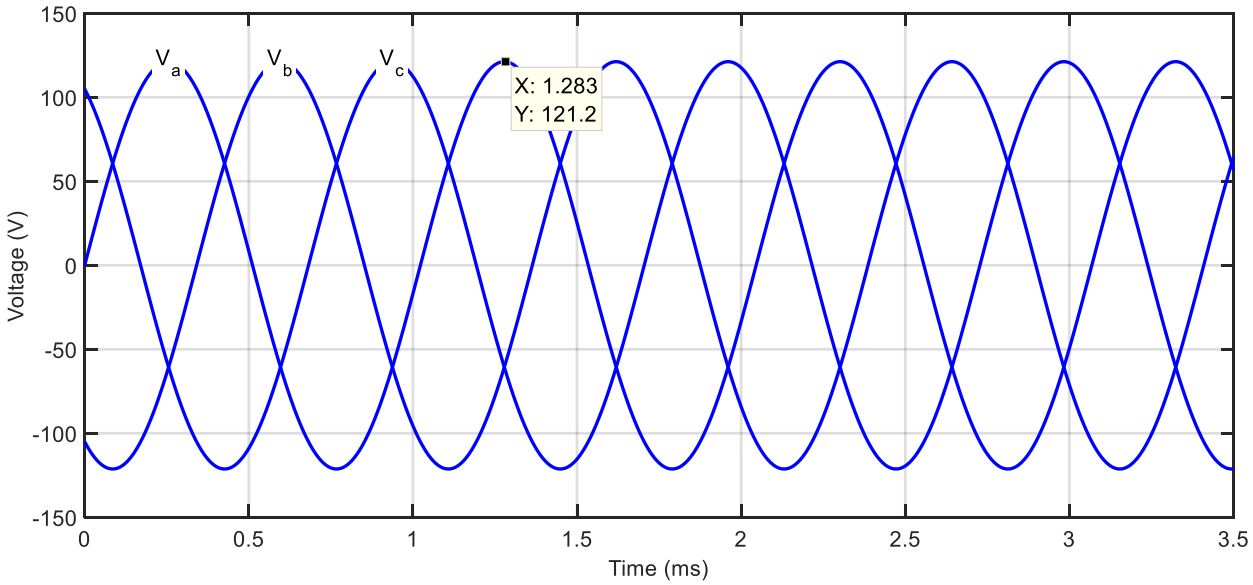


Figure 2.24: Phase voltages at idle speed and $\alpha = 0°$

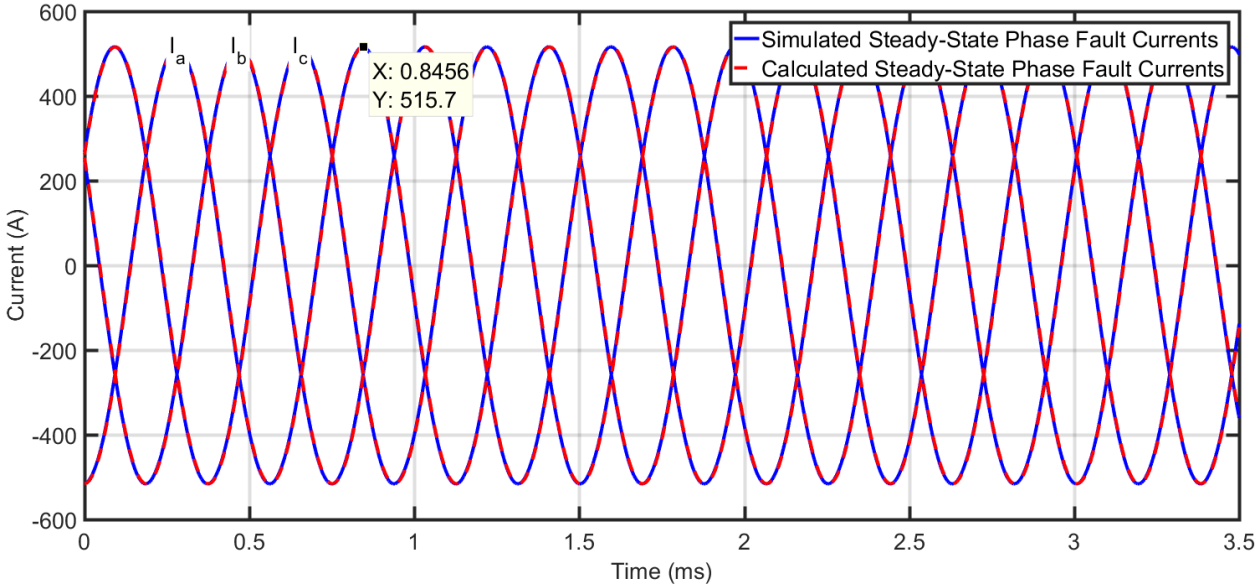


Figure 2.25: Comparison of simulated and calculated steady-state phase currents for 0.5m cable fault at max speed

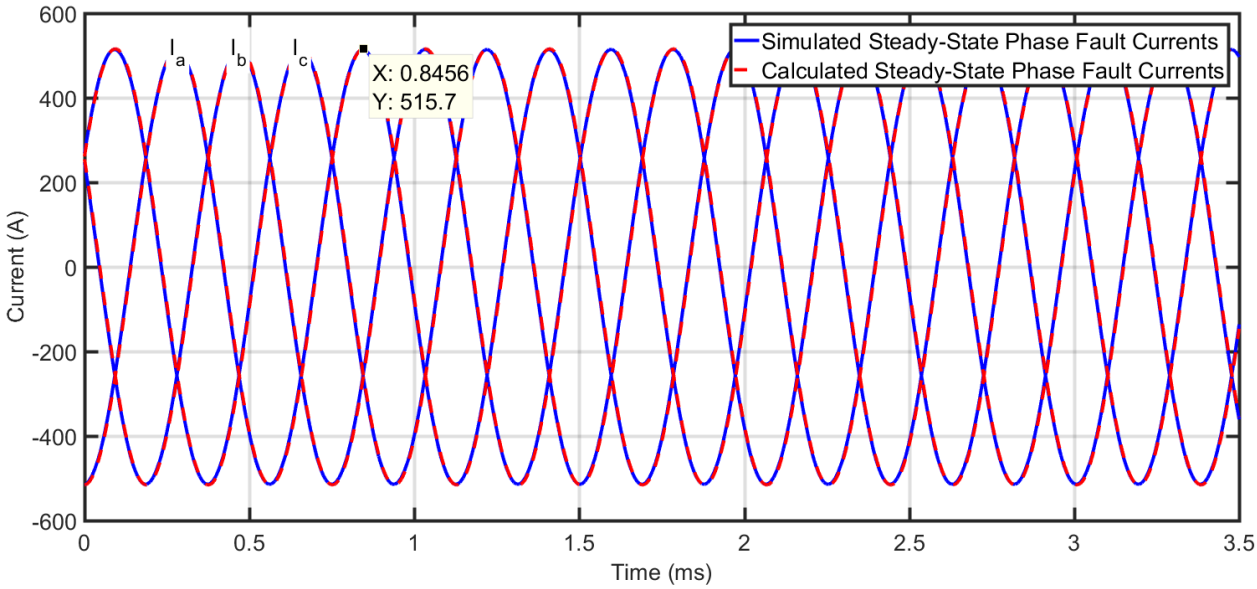


Figure 2.26: Comparison of simulated and calculated steady state phase currents for 5m cable fault at max speed

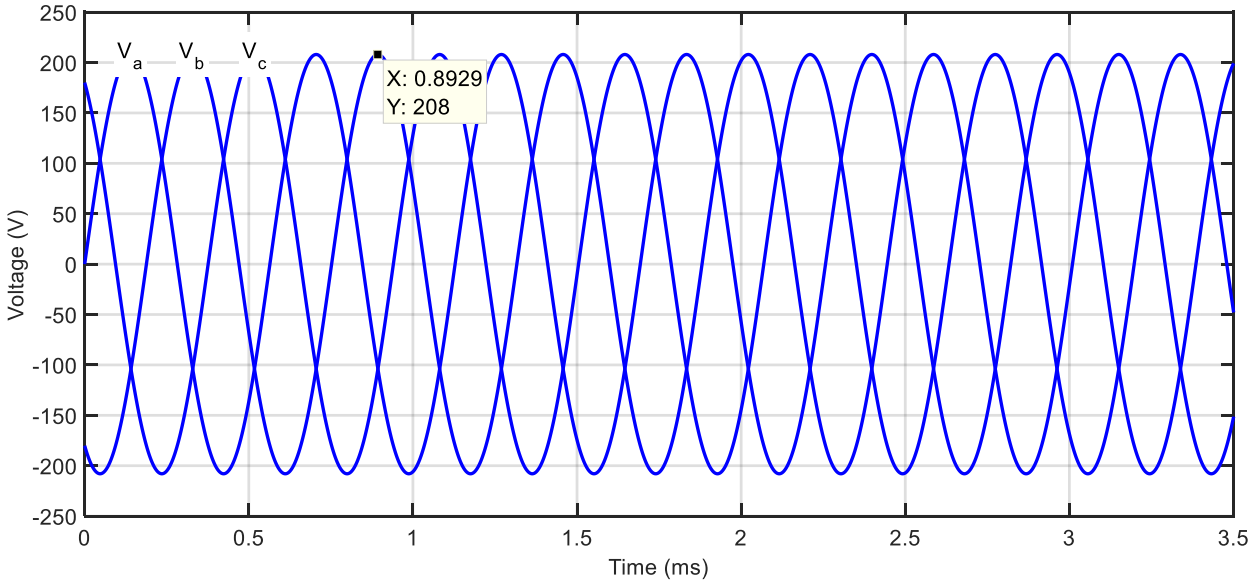


Figure 2.27: Phase voltages at maximum speed and $\alpha = 0°$

B) Combined (Steady-State and Transient) Phase Currents

To simulate the combined response, the initial phase currents prior to the fault must first be calculated. If the system is initially operating at a nominal output power (P_{nom}) and the converter has unity power factor, the initial RMS phase current (I_{xRMS}) can be found by solving the apparent power balance equation:

$$\sqrt{P^2 + Q^2} = |S| \tag{2.90}$$

where P, Q, and S are the active, reactive, and apparent powers consumed by the system respectively. Substituting parameters of this system into (2.90) gives:

$$\sqrt{\left(\frac{P_{nom}}{3} + I_{xRMS}^2 R_{Line}\right)^2 + (I_{xRMS}^2 \omega L_{Line})^2} = I_{xRMS} V_{xRMS} \tag{2.91}$$

where I_{xRMS} and V_{xRMS}, are the RMS line current and line-to-neutral voltage prior to a fault. The peak phase current (I_0) can then be found as:

$$I_0 = I_{xRMS}\sqrt{2} \tag{2.92}$$

and the initial phase angle as:

$$\phi_0 = cos^{-1}\frac{P}{|S|} = cos^{-1}\frac{\frac{P_{nom}}{3} + I_{xRMS}^2 R_{Line}}{I_{xRMS}V_{xRMS}} \quad (2.93)$$

With 50kW nominal output power and idle speed condition, the peak phase current (I_0) was found using (2.91) and (2.92) to be 386.88A. Whereas, under maximum speed condition the peak current was found to be 485.52A. The initial phase angle (ϕ_0) was found to be 43.91° and 70.29° lagging for the idle and maximum speed conditions respectively using (2.93).

Initial phase currents (I_{0a}, I_{0b}, and I_{0c}) vs. V_a phase angle at the fault instance (α) can then be found using (2.46) - (2.48) as plotted in Figure 2.28 and Figure 2.29 for the idle and maximum speed conditions respectively.

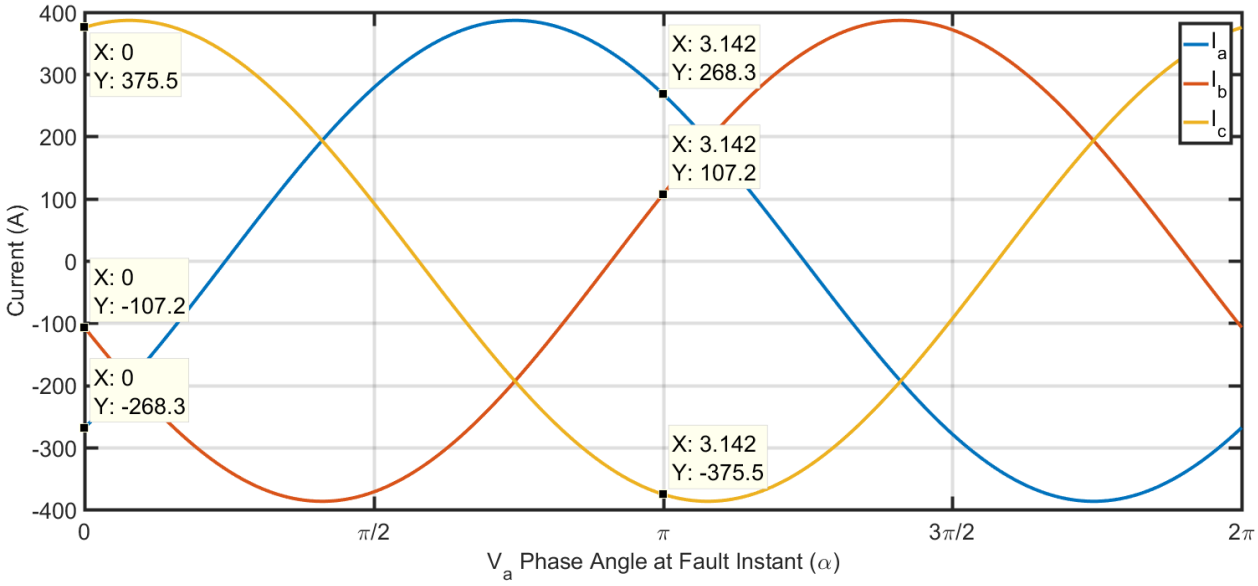


Figure 2.28: Initial phase currents vs. α at the idle speed condition

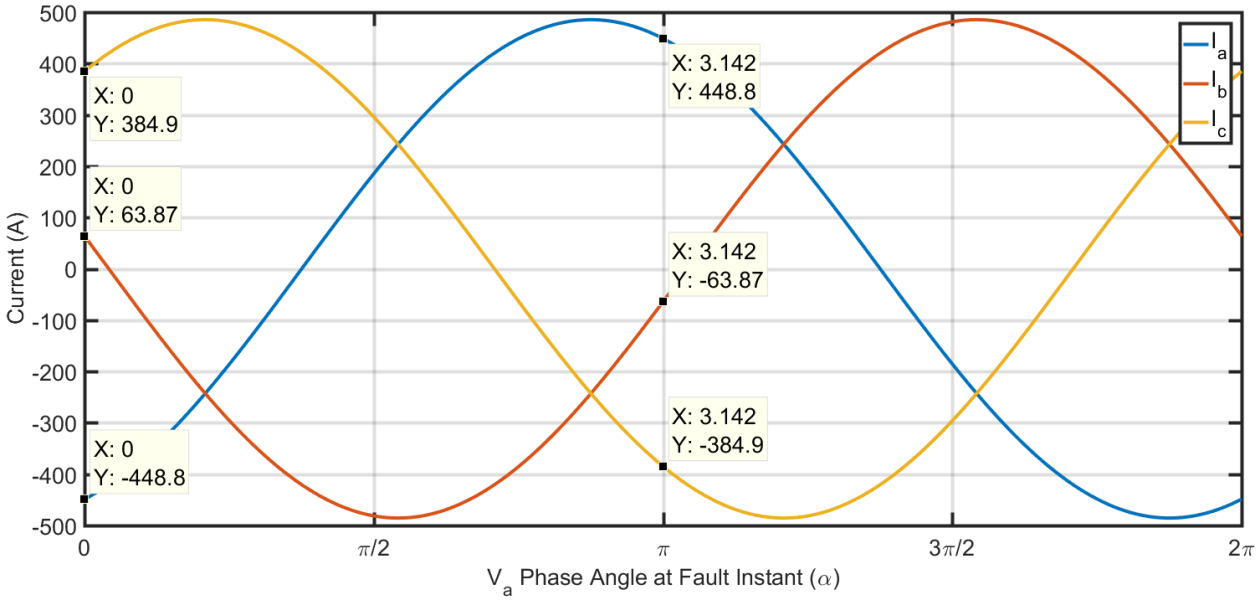


Figure 2.29: Initial phase currents vs. α at max speed condition

The analytical results are compared to simulations of the circuit shown in Figure 2.30, with parameters I_{0a}, I_{0b}, I_{0c}, *CableLength*, *Alpha*, and *Speed* changed according to the desired scenario.

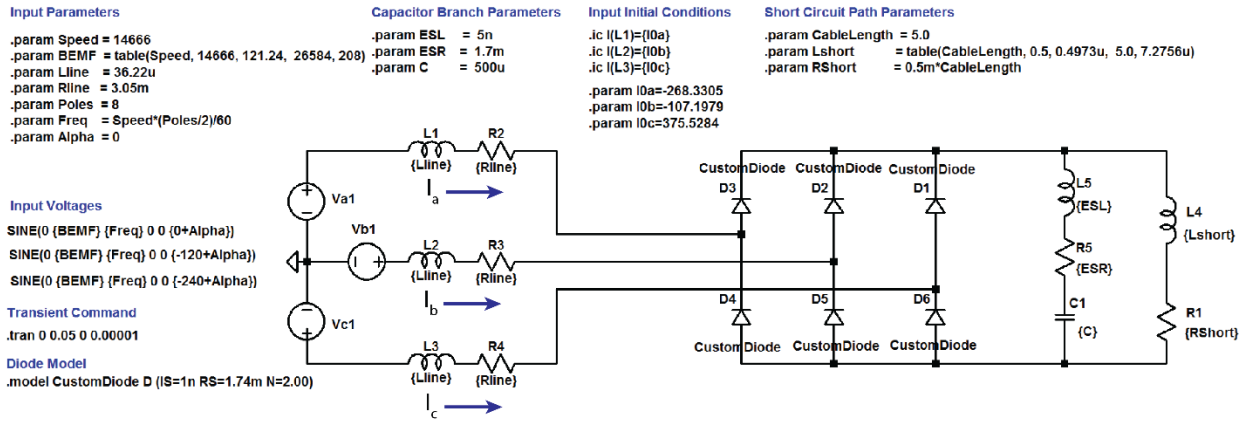


Figure 2.30: AC complete response simulation circuit showing idle speed, α=0, and 5m cable fault case

Analytical results at idle speed condition are compared to simulations for cable length of 0.5m and α of both zero & π, as shown in Figure 2.31 and Figure 2.32 respectively. The simulation results show reasonable matching with those obtained from (2.52) - (2.54) except for a small error due to the on-state voltage drop and resistance of the diodes (V_J and R_S). The error can be reduced by accounting for the on-state resistance of the diodes in (2.52) - (2.54) as demonstrated in Figure

2.31 and Figure 2.32. The expressions for phase current accounting for the on-state resistance of the diodes then become:

$$i_a(t) = \frac{V_m}{Z} sin(\omega t - \phi + \alpha) + \left(I_{0a} - \frac{V_m}{Z} sin(-\phi + \alpha)\right) e^{-t\frac{R_{Line}+\boldsymbol{R_S}}{L_{Line}}} \quad (2.94)$$

$$i_b(t) = \frac{V_m}{Z} sin(\omega t - 2\pi/3 - \phi + \alpha) + (I_{0b} - \frac{V_m}{Z} sin(-2\pi/3 - \phi + \alpha)) e^{-t\frac{R_{Line}+\boldsymbol{R_S}}{L_{Line}}} \quad (2.95)$$

$$i_c(t) = \frac{V_m}{Z} sin(\omega t - 4\pi/3 - \phi + \alpha) + (I_{0c} - \frac{V_m}{Z} sin(-4\pi/3 - \phi + \alpha)) e^{-t\frac{R_{Line}+\boldsymbol{R_S}}{L_{Line}}} \quad (2.96)$$

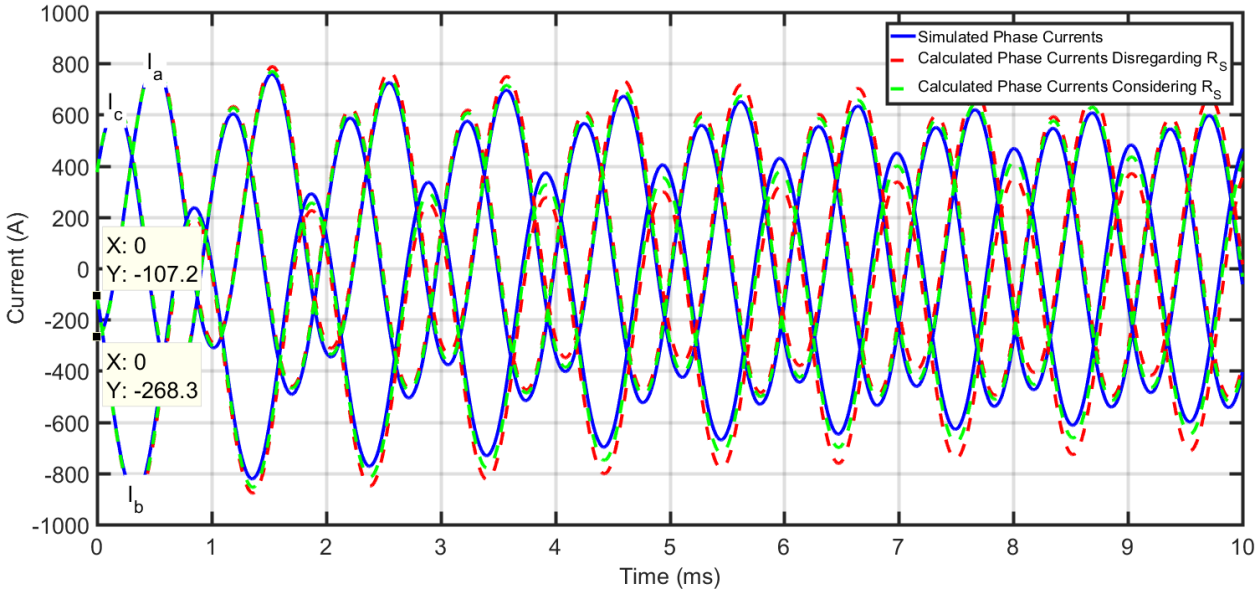


Figure 2.31: Comparison of simulated and calculated phase currents at idle speed, $\alpha=0$, and 0.5m cable fault. Also showing reduced error when R_S is considered.

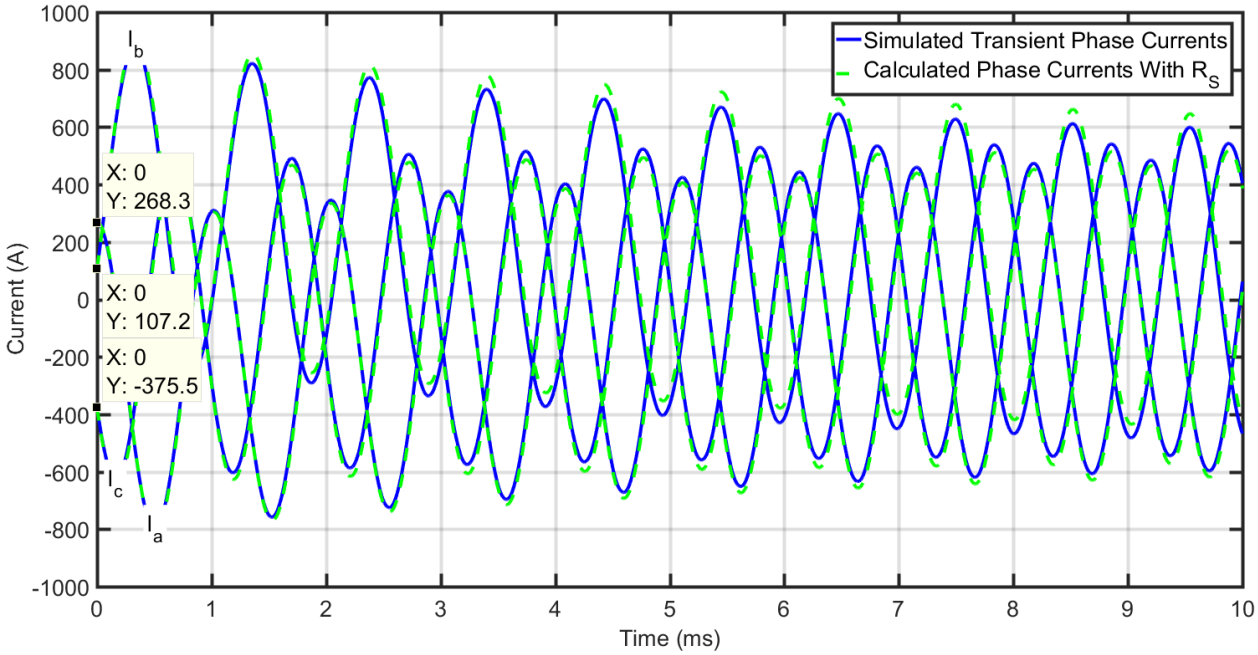


Figure 2.32: Comparison of simulated and calculated phase currents at idle speed, $\alpha=\pi$, and 0.5m cable fault

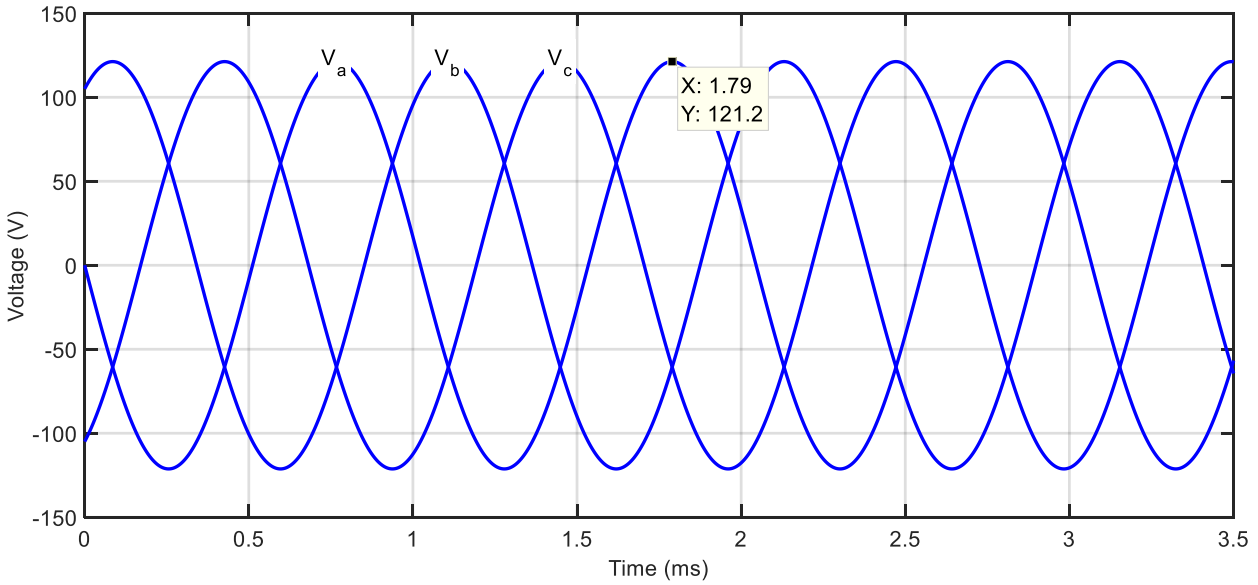


Figure 2.33: Phase voltages at idle speed and $\alpha=\pi$ case

Near ideal diode models were used for simulations at maximum speed condition with 0.5m cable fault and α of zero & π to demonstrate that the discrepancies in the previous case were due to the

on-state voltage drops and resistances of the diodes, as shown in Figure 2.34 and Figure 2.35 respectively. Phase voltages at maximum speed and $\alpha=\pi$ is shown in Figure 2.36.

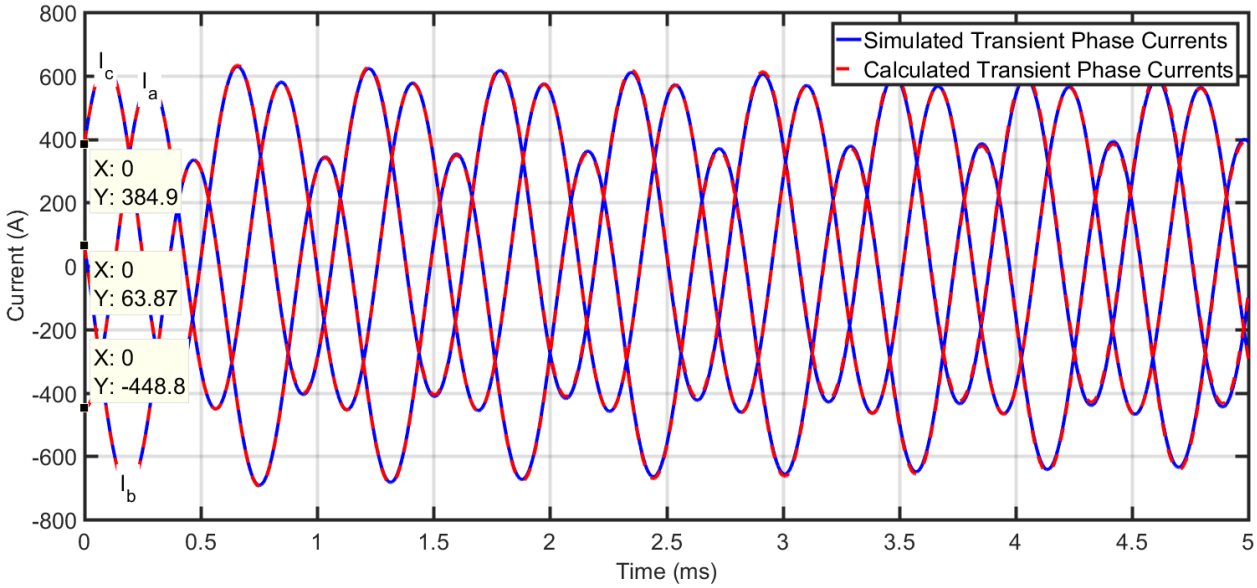


Figure 2.34: Comparison of simulated and calculated phase current for 0.5m cable fault at max speed and $\alpha=0$

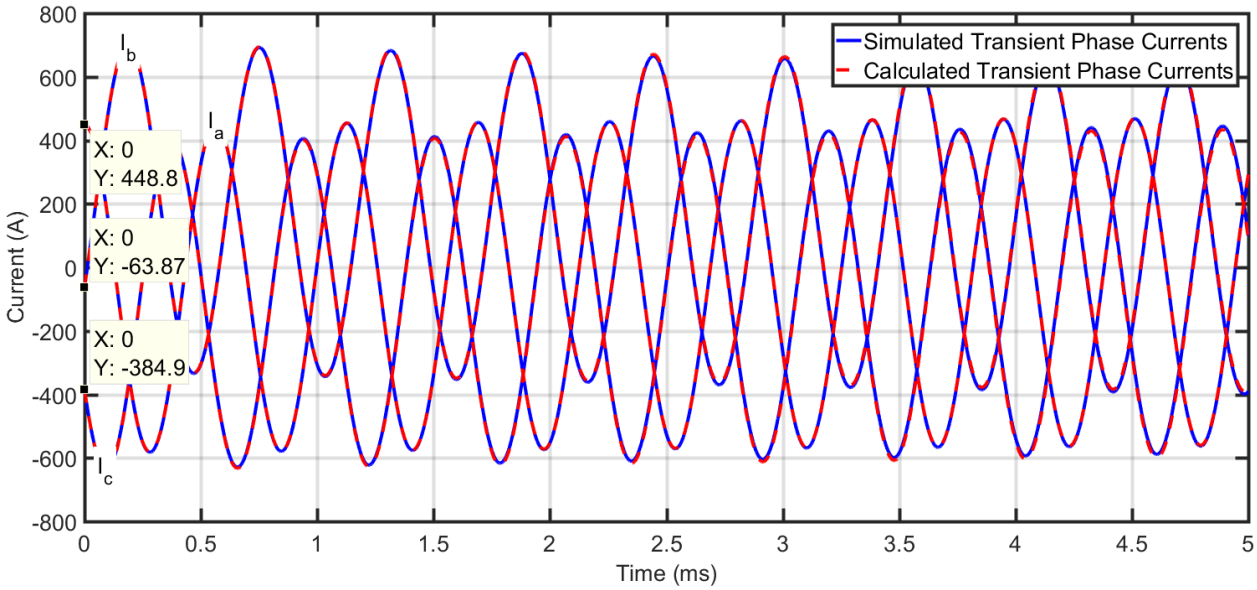


Figure 2.35: Comparison of simulated and calculated phase current for 0.5m cable fault at max speed and $\alpha=\pi$

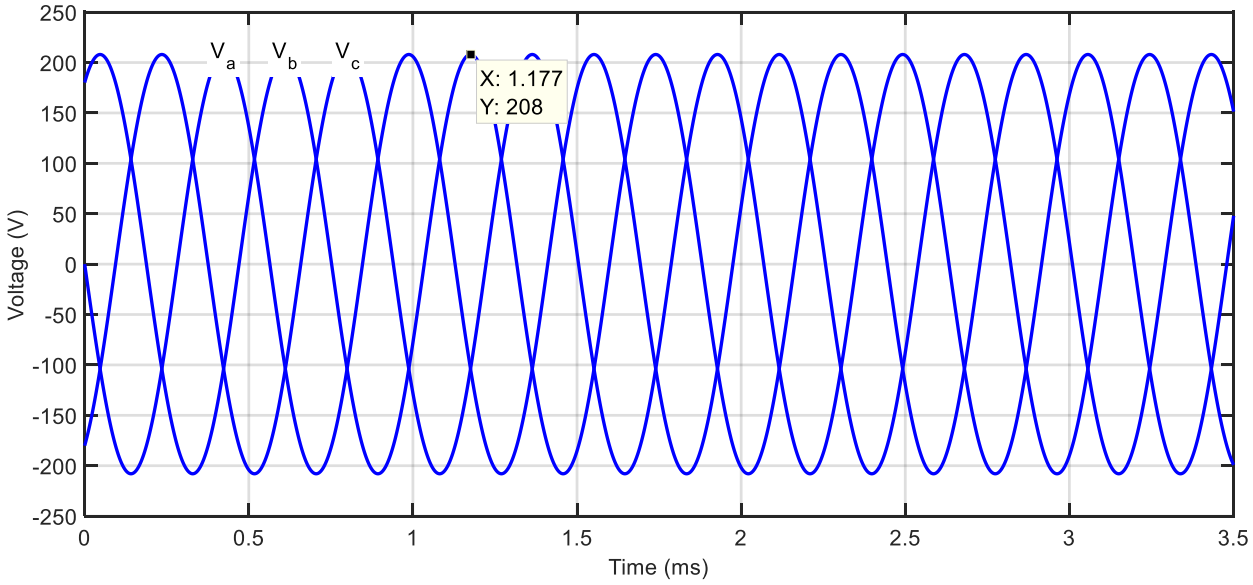


Figure 2.36: Phase voltages at max speed and $\alpha=\pi$ case

2.5.5. Simulation Analysis of Combined Response Accounting for Both AC and DC Side Contributions

In this section, the analytical results for the combined response are compared to simulations at both idle and maximum speed conditions, and for cable lengths of 0.5m and 5m, while α is fixed to 180° ($\alpha = \pi$), which was chosen arbitrary. A schematic of the simulation circuit is shown in Figure 2.37, where parameters "*Speed*" and "*CableLength*" are changed according to the desired scenario.

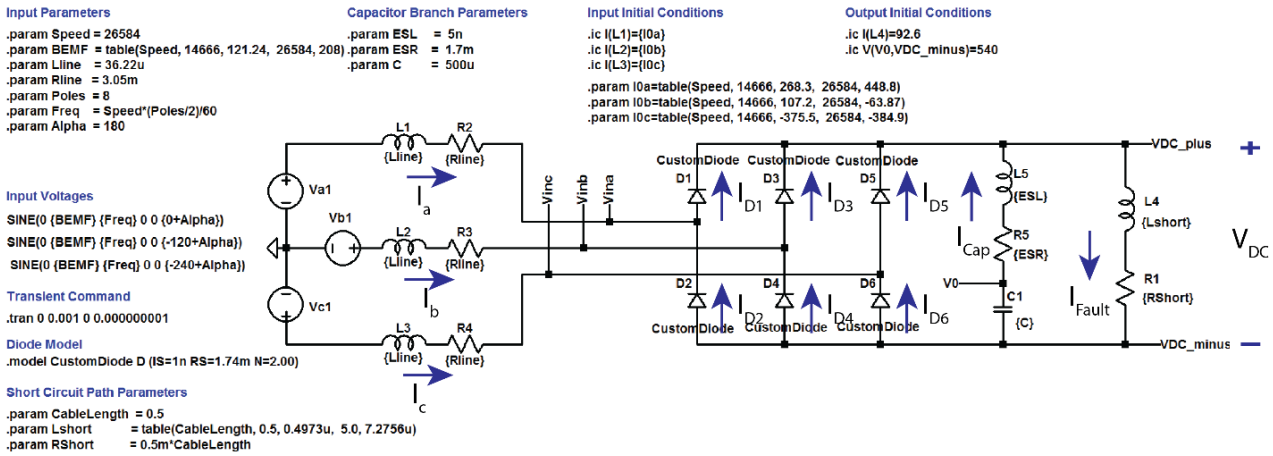


Figure 2.37: Combined response simulation circuit (max speed case shown)

A) DC-link Voltage Accounting For Both AC and DC Side Contributions

The simulated DC-link voltage (V_{DC}) was compared to results of (2.11) with an initial current value (I_0) equal to ($I_0 + I_{capo}$=92.6-282.9=-190.3A) and (92.6-356.2=-263.6A) for the idle and maximum speeds respectively, as shown in Figure 2.38 and Figure 2.39. For the idle speed condition, the zero voltage time boundaries (t_0) were calculated to be 24.72µs and 97.55µs, while the $-2V_j$ (-2.6V) time boundaries (t_b) were found to be 24.8µs and 97.85µs for the 0.5m and 5m cable faults respectively. The time boundaries for the maximum speed were found as shown in Figure 2.39.

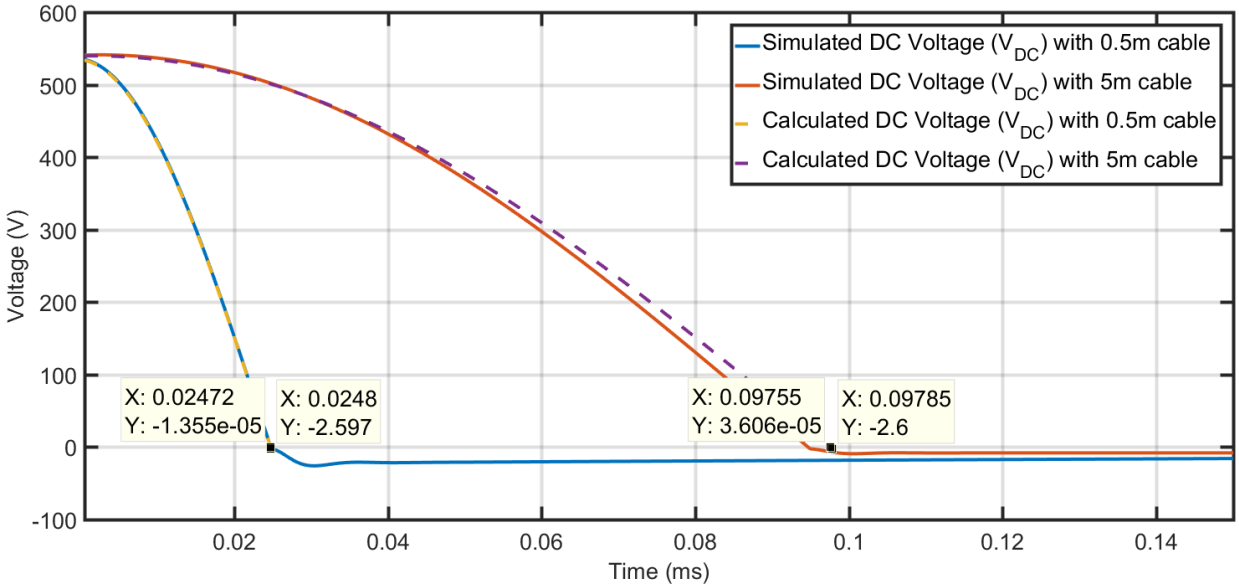


Figure 2.38: Comparison of simulated and calculated DC-link voltage during a fault at idle speed operation

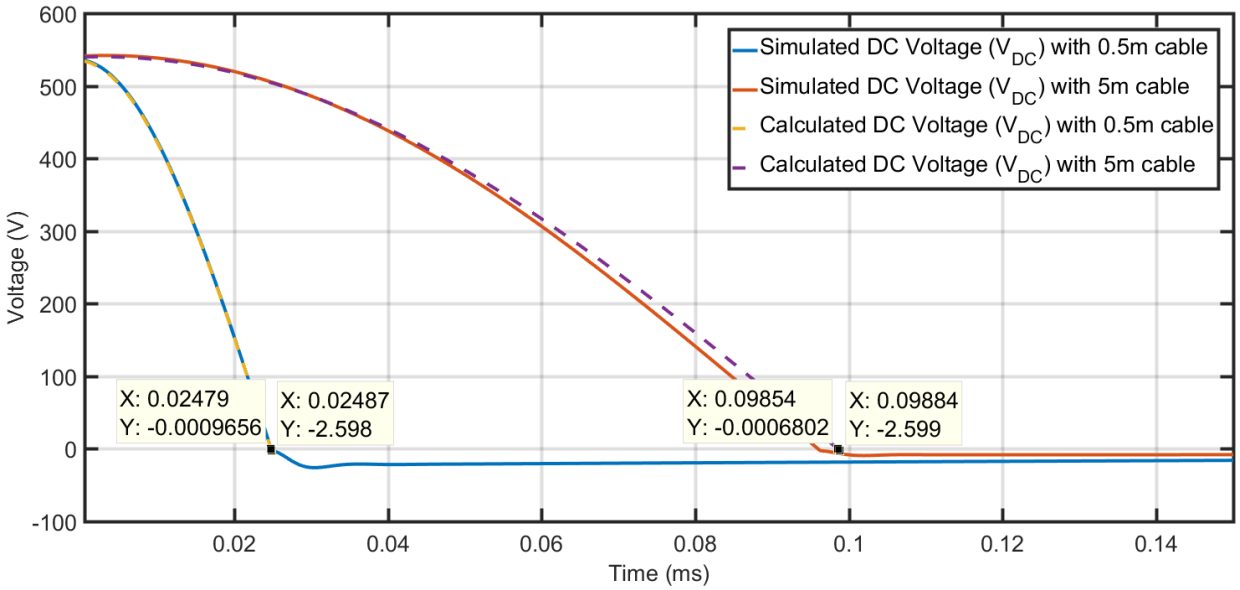


Figure 2.39: Comparison of simulated and calculated DC-link voltage during a fault at maximum speed operation

B) AC Side Currents

AC side currents during the transition period ($t < t_0$) were found for the 0.5m cable fault at idle speed using (2.63), as shown in Figure 2.40 and 3.39. Commutation state coefficients (β_a, β_b, and β_c) were found using (2.61) to be 1/3, 1/3, and -2/3 respectively. Phase currents at the time boundary ($I_{t_0 a}, I_{t_0 b},$ and $I_{t_0 c}$) were found to be 186.3A, 105.9A, and -292.2A respectively. These initial conditions were then substituted in (2.77) - (2.79) so that phase currents after the time boundary ($t > t_0$) can be determined, as also shown in Figure 2.40. Comparisons with simulation results show excellent matching (within 5%) demonstrating the validity of the presented analyses.

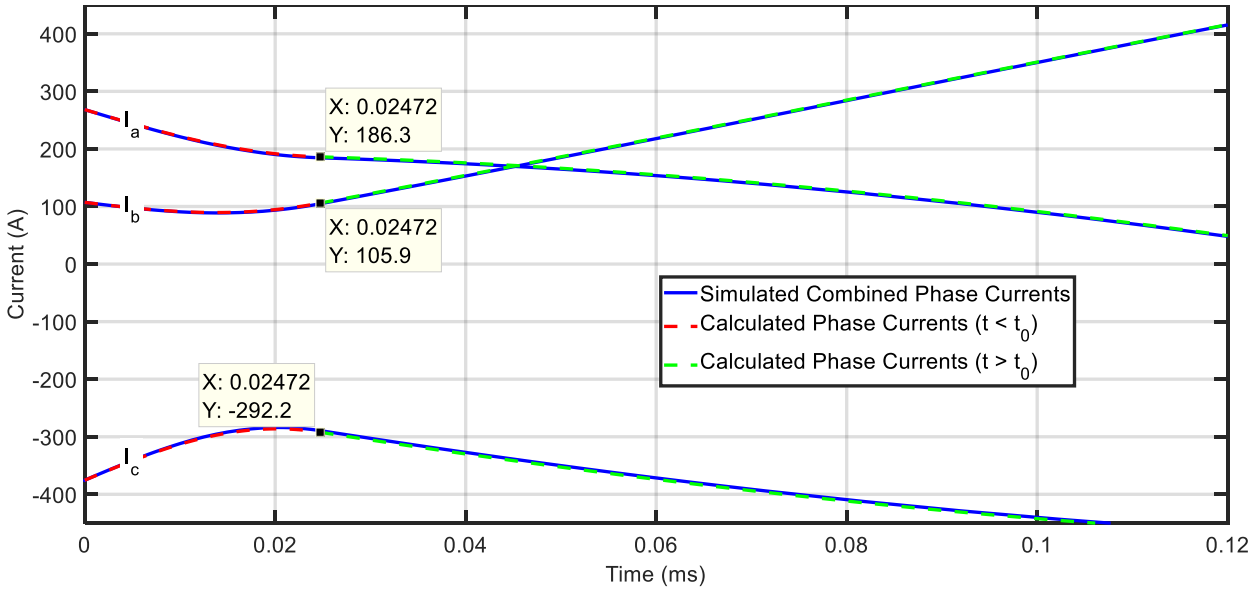


Figure 2.40: Comparison of simulated and calculated phase currents (i_a, i_b, and i_c) during a 0.5m cable fault at idle speed operation - Zoomed

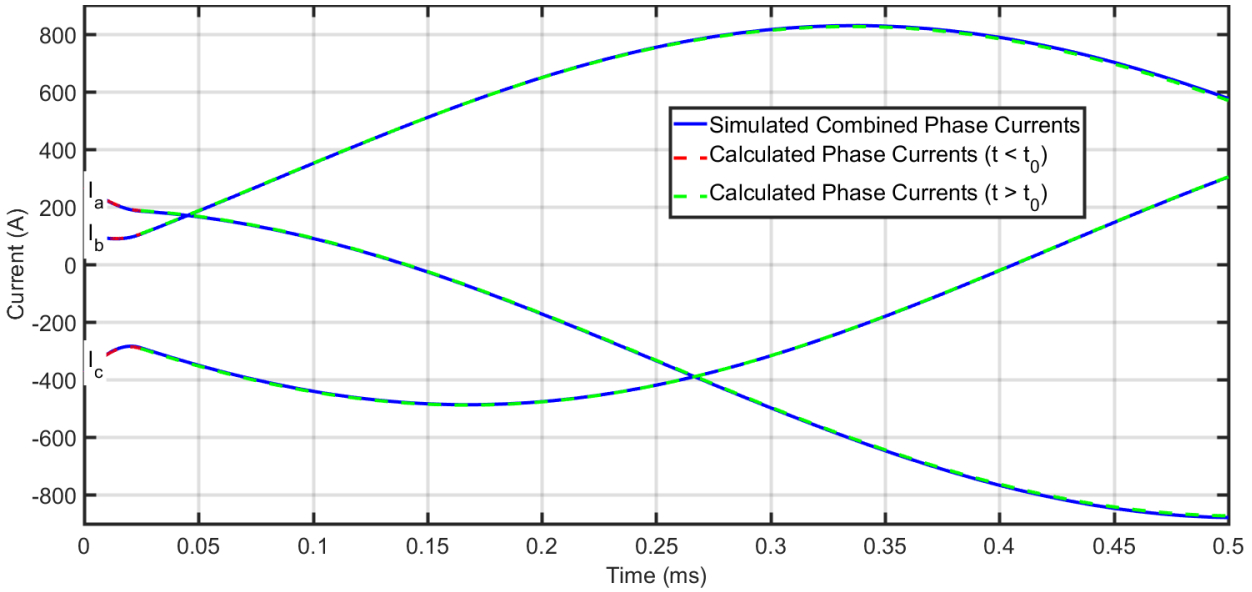


Figure 2.41: Comparison of simulated and calculated phase currents (i_a, i_b, and i_c) during a 0.5m cable fault at idle speed operation

For the 5m cable fault during idle speed operation, the comparisons are shown in Figure 2.42 and 2.43. Commutation state coefficients (β_{a1}, β_{b1}, and β_{c1}) were found using (2.61) to be 1/3, 1/3, and -2/3 respectively. A commutation occurs on *phase a's* current (i_a) at $t_c = 53.93\mu s$, after which the commutation coefficients (β_{a2}, β_{b2}, and β_{c2}) were expected to be 2/3, -1/3, and -1/3 respectively. However, due to magnitude of phase "a" voltage ($|V_a|$) being lower than $|2V_{DC}/3|$,

$i_a, i_b,$ and i_C follow (2.68) - (2.70) with $x = a, y = b,$ and $z = c$. This period ends when $|V_a|$ becomes larger than $|2V_{DC}/3|$ at $t = 75.74\mu s$. Phase currents at the time boundary ($I_{t_0a}, I_{t_0b},$ and I_{t_0c}) were found to be -16.6A, 50.08A, and -33.48A respectively. These initial conditions were then substituted in (2.77) - (2.79) so that phase currents after the time boundary ($t > t_0$) are determined, as also shown in Figure 2.42.

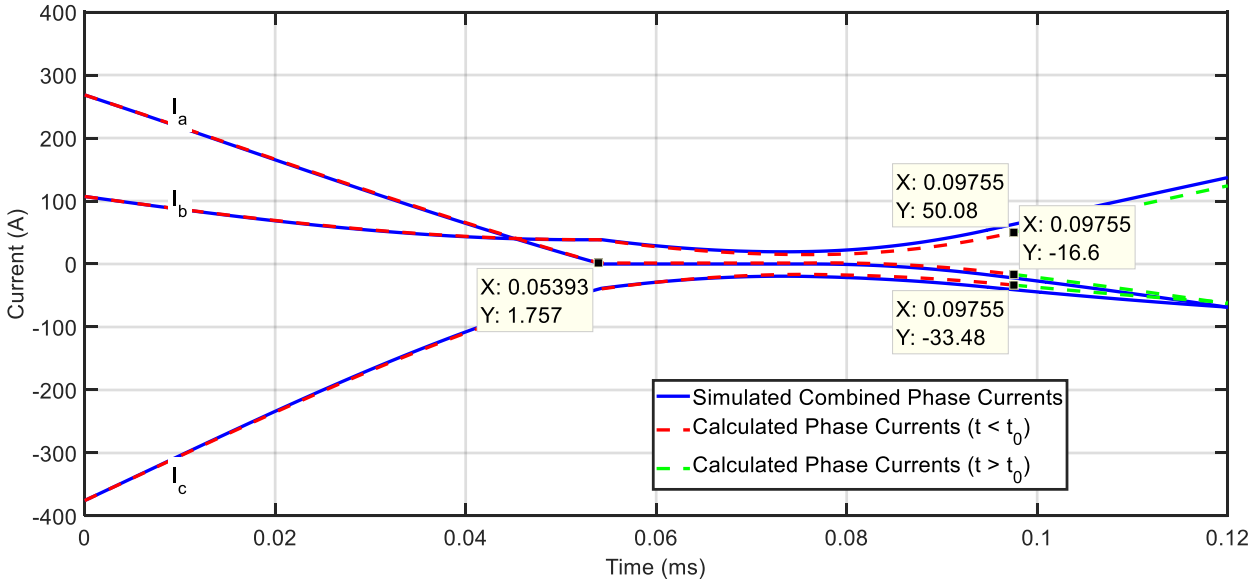


Figure 2.42: Comparison of simulated and calculated phase currents (i_a, i_b, and i_c) during a 5m cable fault at idle speed operation – Zoomed

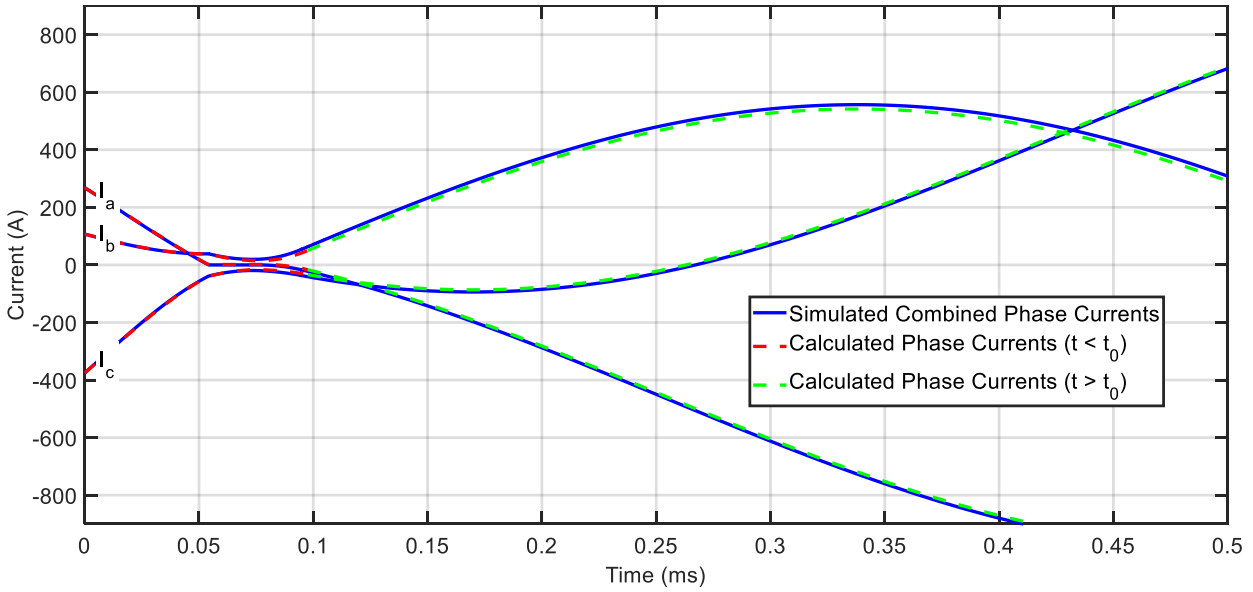


Figure 2.43: Comparison of simulated and calculated phase currents (i_a, i_b, and i_c) during a 5m cable fault at idle speed operation

Simulated phase voltages at the AC side of the converter (v_{ina}, v_{inb}, and v_{inc}) are shown in Figure 2.44, and compared to the magnitudes of ($2V_{DC}/3$, $(V_{DC}-V_a)/3$, $V_{DC}/3$, V_a, $-V_{DC}/3$, $-(V_{DC}+V_a)/3$, and $-2V_{DC}/3$). This demonstrates that the AC side voltages seen by the converter follow expected values.

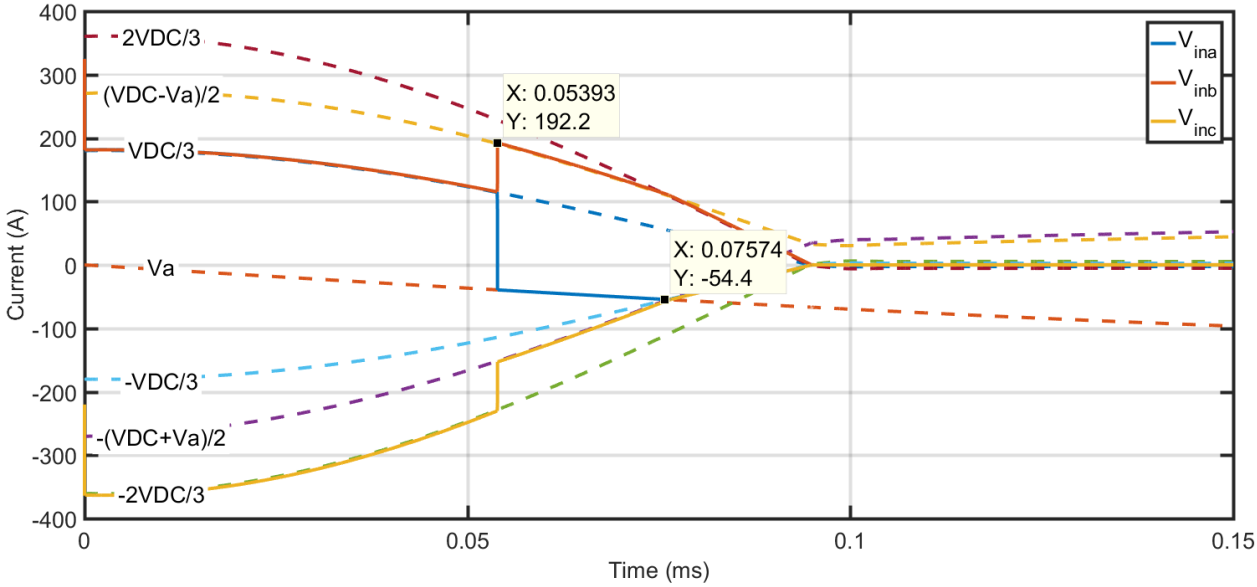


Figure 2.44: Simulated phase voltages at the converter's input (v_{ina}, v_{inb}, and v_{inc}) for a 5m cable fault at idle speed operation

For the 0.5m cable fault during maximum speed operation, the comparisons are shown in Figure 2.45 and 2.46. The commutation coefficients (β_{a1}, β_{b1}, and β_{c1}) were found using (2.61) to be 2/3, -1/3, and -1/3 respectively. A commutation occurs on i_b at $t_c = 6.5\mu s$, after which the commutation coefficients are (β_{a2}, β_{b2}, and β_{c2}) 1/3, 1/3, and -2/3. Phase currents at the time boundary (I_{t_0a}, I_{t_0b}, and I_{t_0c}) were found to be 322.2A, 53.16A, and -375.4A respectively. These initial conditions were then substituted in (2.77) - (2.79) so that phase currents after the time boundary ($t > t_0$) are determined, as also shown in Figure 2.45.

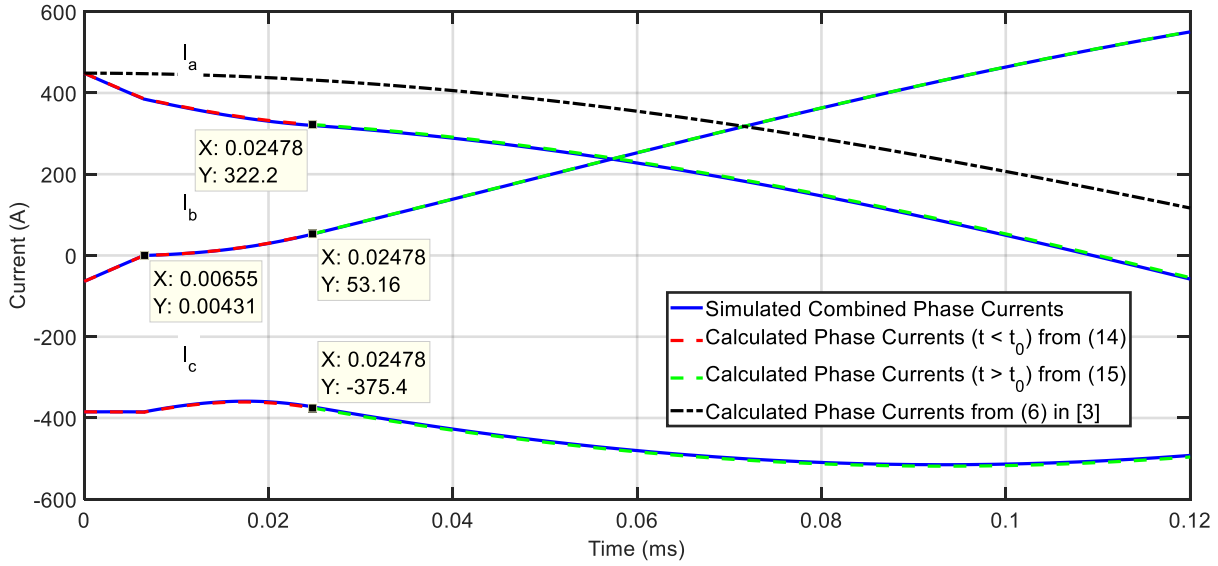


Figure 2.45: Comparison of simulated and calculated phase currents (i_a, i_b, and i_c) during a 0.5m cable fault at maximum speed operation – Zoomed

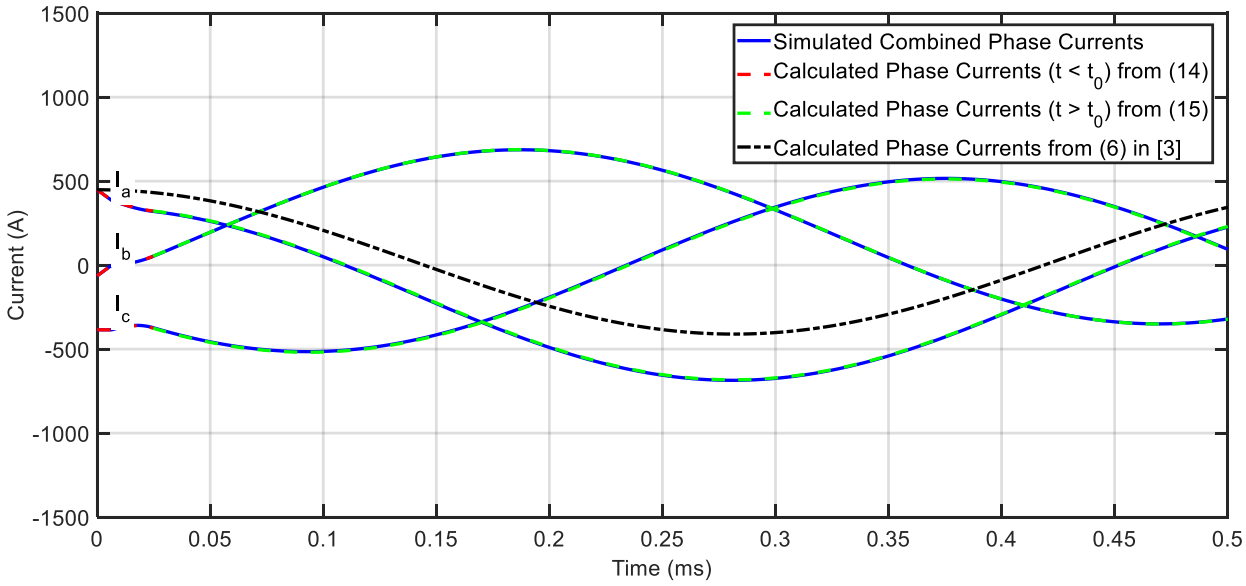


Figure 2.46: Comparison of simulated and calculated phase currents (i_a, i_b, and i_c) during a 0.5m cable fault at maximum speed operation

Finally, for the 5m cable fault during maximum speed operation, the comparisons are shown in Figure 2.47 and 2.48. The commutation coefficients (β_{a1}, β_{b1}, and β_{c1}) were found using (2.61) to be 2/3, -1/3, and -1/3 respectively. A commutation first occurs on i_b at $t_{c1} = 6.48\mu s$, after which the commutation coefficients (β_{a2}, β_{b2}, and β_{c2}) are 1/3, 1/3, and -2/3 respectively. A second commutation then occurs on I_a at $t_{c2} = 67.6\mu s$, after which the commutation coefficients

(β_{a3}, β_{b3}, and β_{c3}) are -1/3, 2/3, and -1/3 respectively. Phase currents at the time boundary ($I_{t_0 a}, I_{t_0 b}$, and $I_{t_0 c}$) were found to be -103.4A, 183.7A, and -80.32 respectively. These initial conditions were then substituted in (2.77) - (2.79) so that phase currents after the time boundary ($t > t_0$) can be found, as also shown in Figure 2.47.

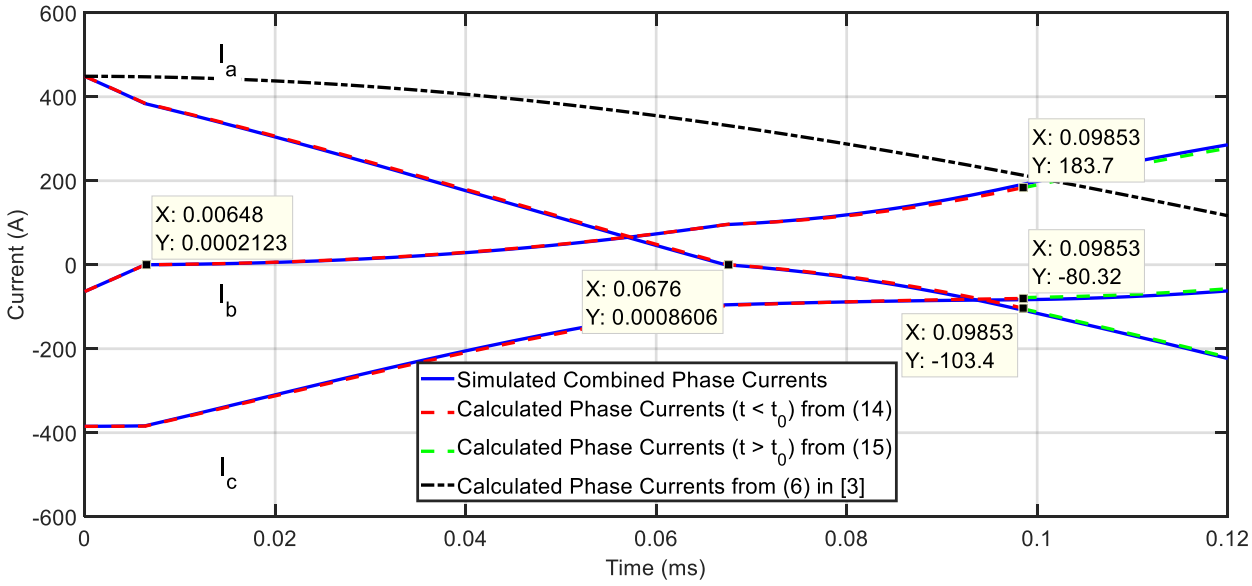


Figure 2.47: Comparison of simulated and calculated phase currents (i_a, i_b, and i_c) during a 5m cable fault at maximum speed operation – Zoomed

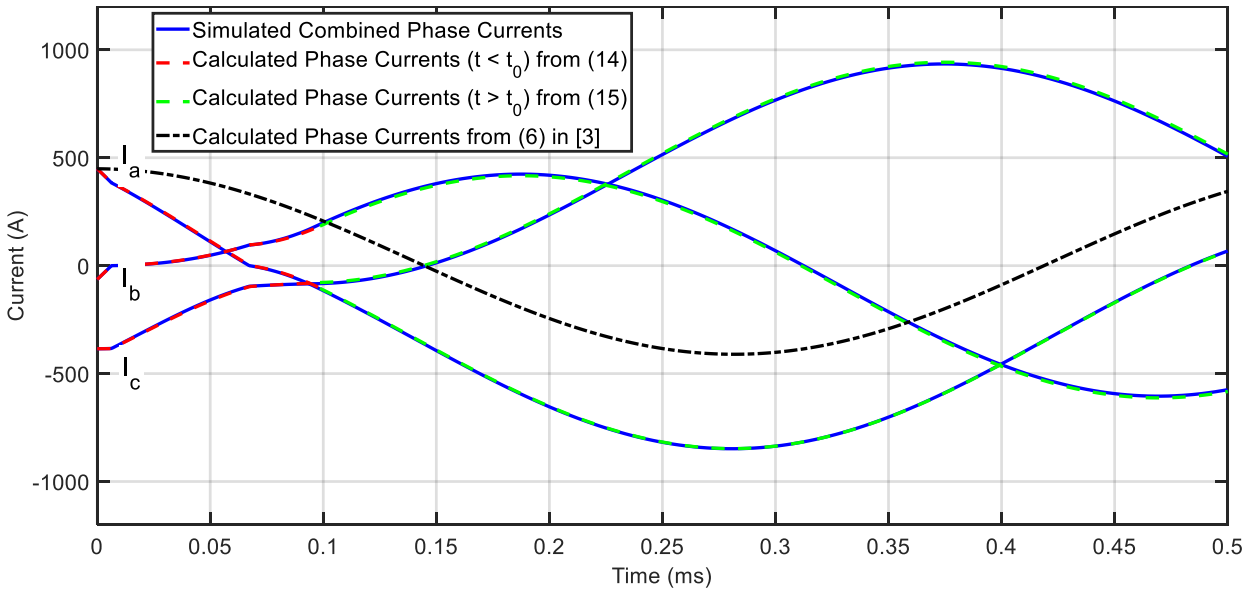


Figure 2.48: Comparison of simulated and calculated phase currents (i_a, i_b, and i_c) during a 5m cable fault at maximum speed operation

All comparisons demonstrate excellent matching (within 5%) between calculated and expected results, validating the presented analyses. It can also be seen from Figure 2.45-2.48 that the previous approach [3, 11, 16] did not consider the transition period ($t<t_0$) during which phase currents are proportional to V_{DC}, which results in inaccurate predictions of the c0urrents.

C) Fault Branch's Current

The fault branch's current obtained from simulation (I_{Fault}) was compared to that from (2.22) for the two cable lengths and at both idle and maximum speeds as shown in Figure 2.49 and Figure 2.50 respectively. The initial current (I_1) was calculated using (2.80) as marked in the figures.

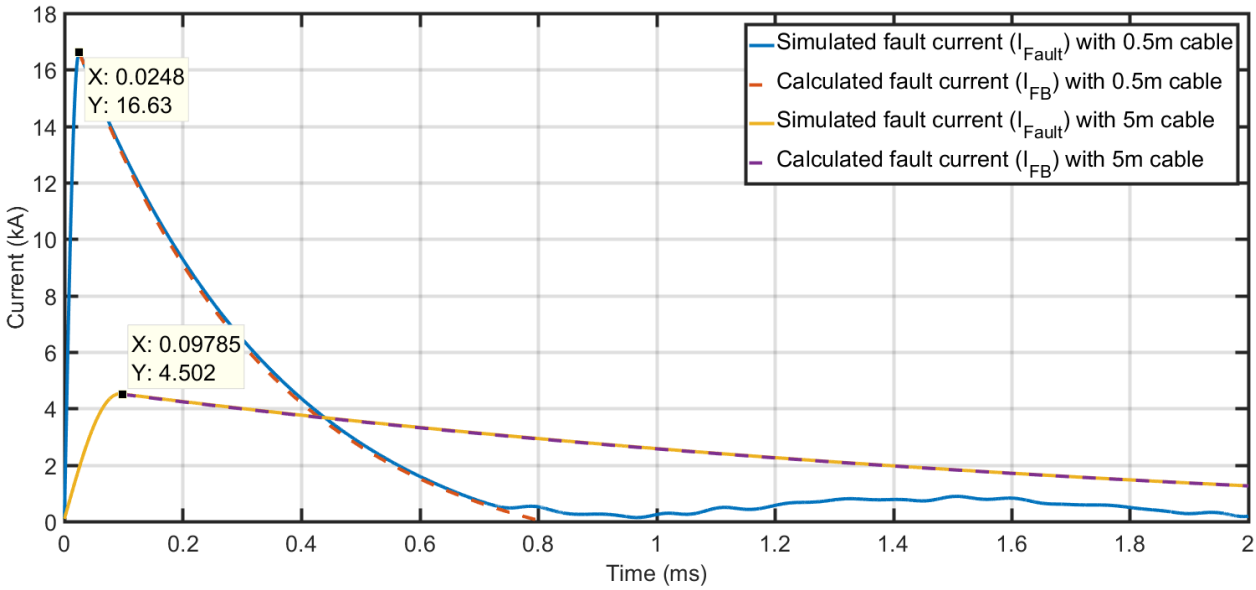


Figure 2.49: Simulated vs. calculated combined fault branch's current at idle speed

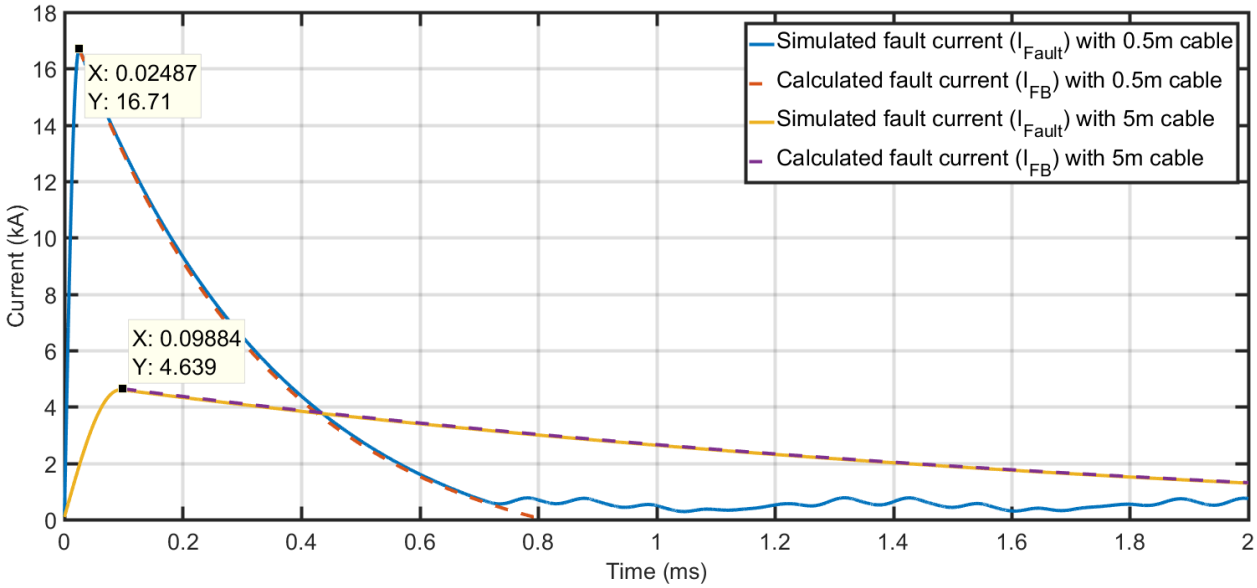


Figure 2.50: Simulated vs. calculated combined fault branch's current at maximum speed

D) Capacitor Branch's Current

The capacitor branch's current obtained from simulation (I_{Cap}) was compared to that obtained from (2.30) for the two cable lengths and at both idle and maximum speeds as shown in Figure 2.51 and Figure 2.52 respectively. The initial capacitor current (I_{cap0}) was calculated to be -282.9A and -356.2A for the two speeds respectively.

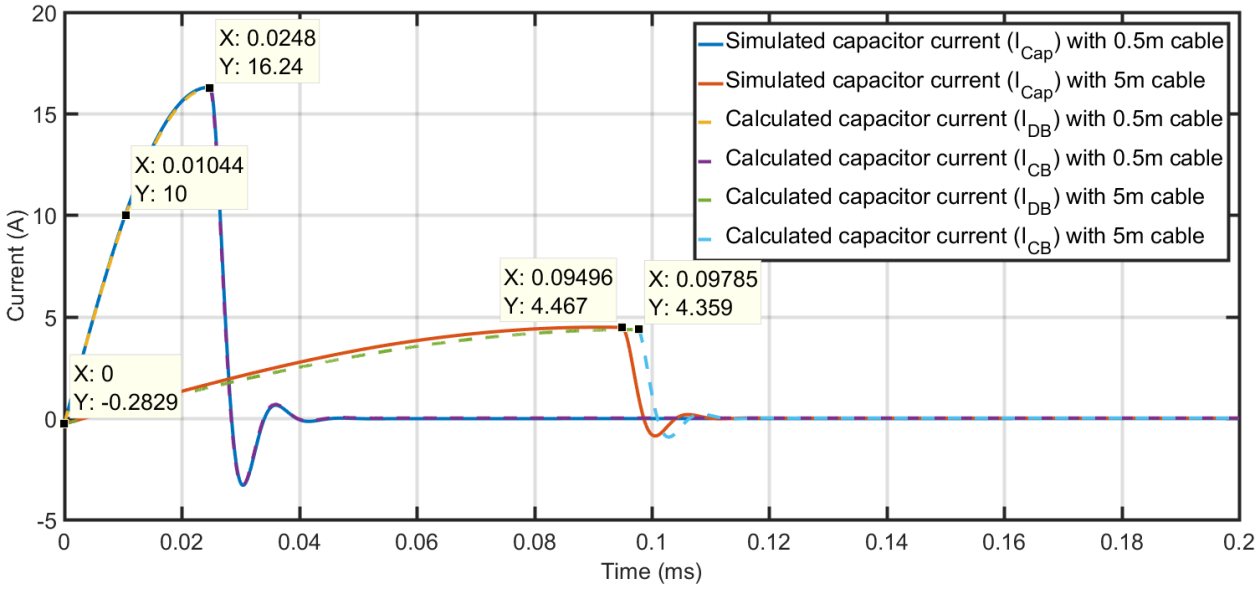


Figure 2.51: Comparison of simulated and calculated combined capacitor branch's current during a fault at idle speed operation

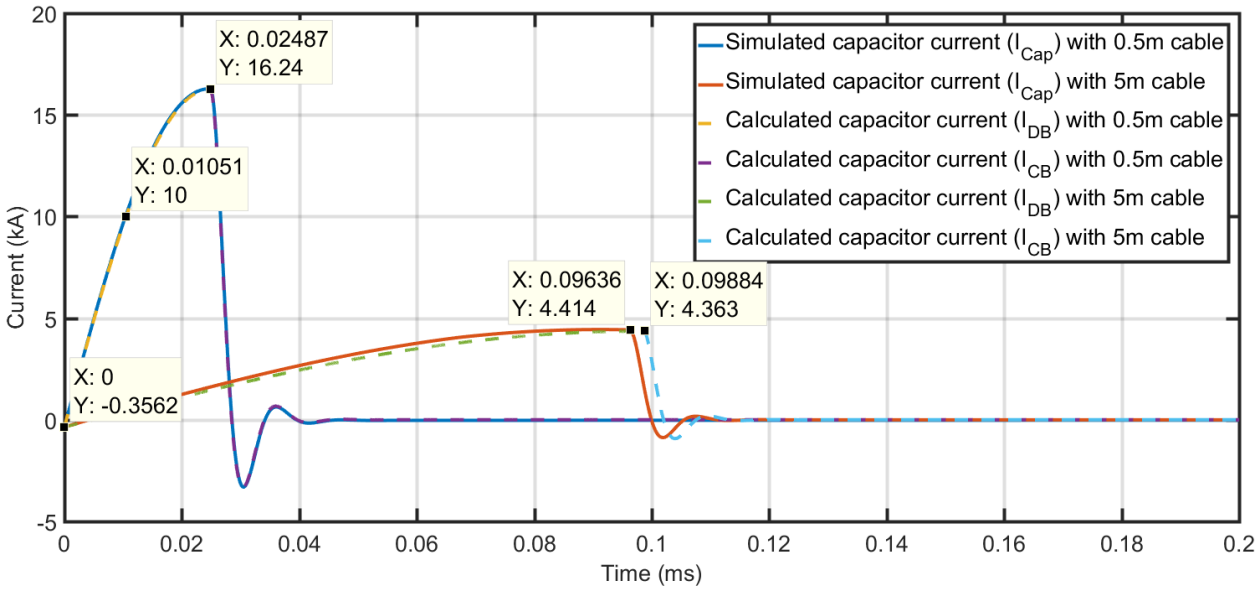


Figure 2.52: Comparison of simulated and calculated combined capacitor branch's current during a fault at maximum speed operation

E) Diodes Currents

Calculated diodes currents are compared to simulation results (I_{D1}through I_{D6}) as shown in Figure 2.53-2.55 for the 0.5m cable fault at maximum speed operation, and Figure 2.56-2.58 for the 5m cable fault at maximum speed operation. Current before the time boundary ($t < t_b$) were calculated using (2.55) - (2.60), such that positive phase current flows through the upper diodes, and negative through the lower. Current after the time boundary ($t > t_b$) is calculated using (2.81) and (2.82) for the upper and lower diodes respectively, up until these currents fall below zero when the current is again calculated using (2.55) - (2.60).

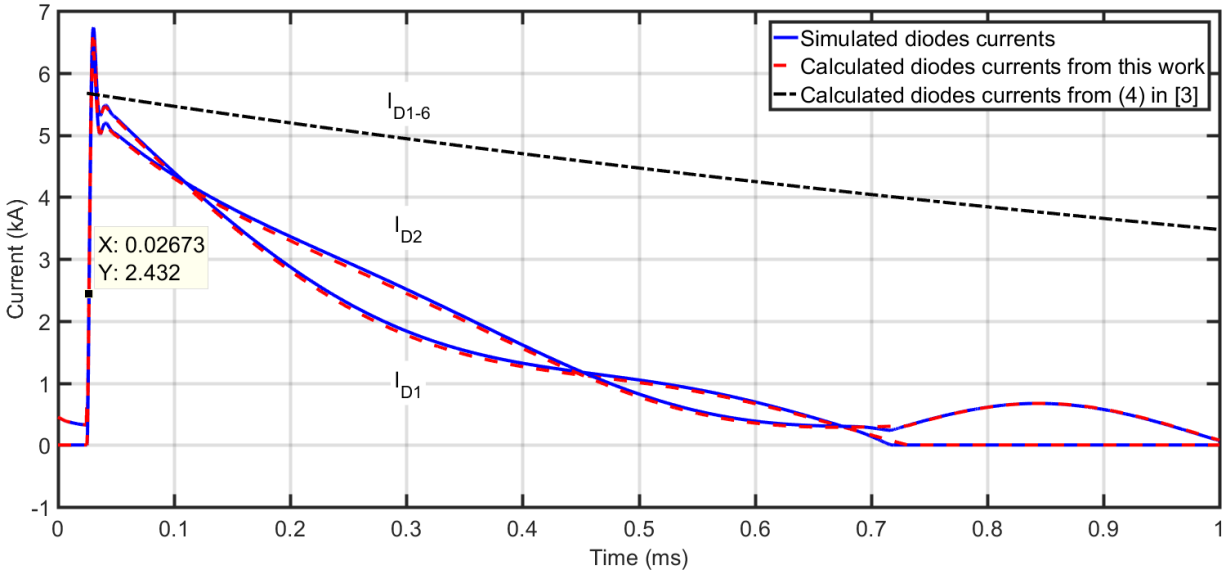


Figure 2.53: Comparison of simulated and calculated diodes 1 and 2 currents at maximum speed condition with 0.5m cable fault

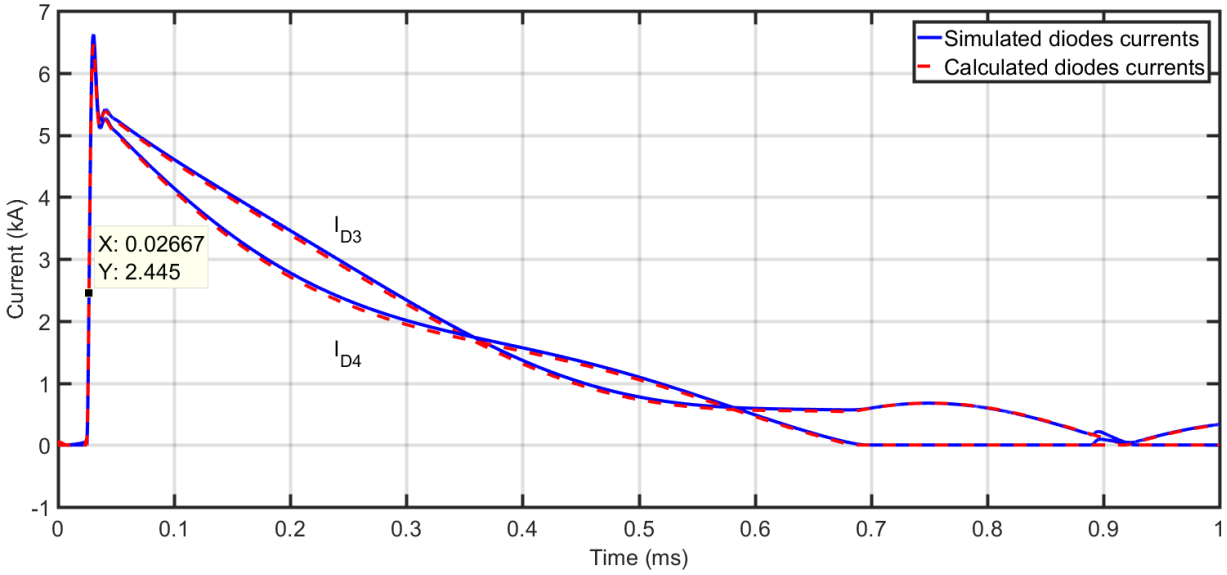


Figure 2.54: Comparison of simulated and calculated diode 3 and 4 currents at maximum speed condition with 0.5m cable fault

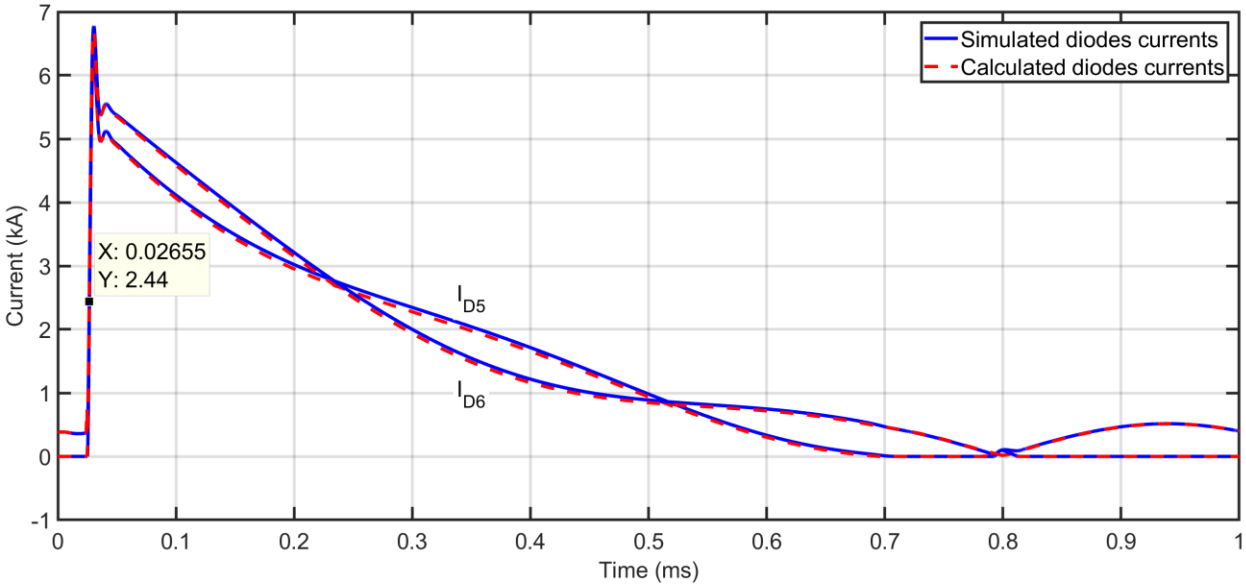


Figure 2.55: Comparison of simulated and calculated diodes 5 and 6 currents at maximum speed condition with 0.5m cable fault

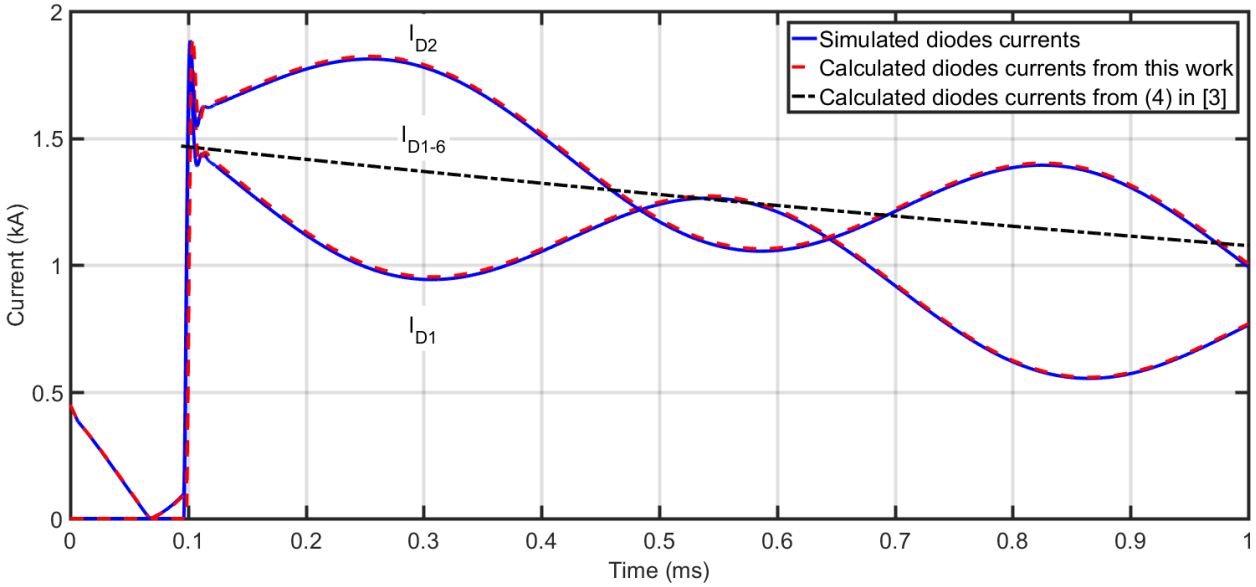


Figure 2.56: Comparison of simulated and calculated diode 1 and 2 currents at maximum speed condition with 5m cable fault

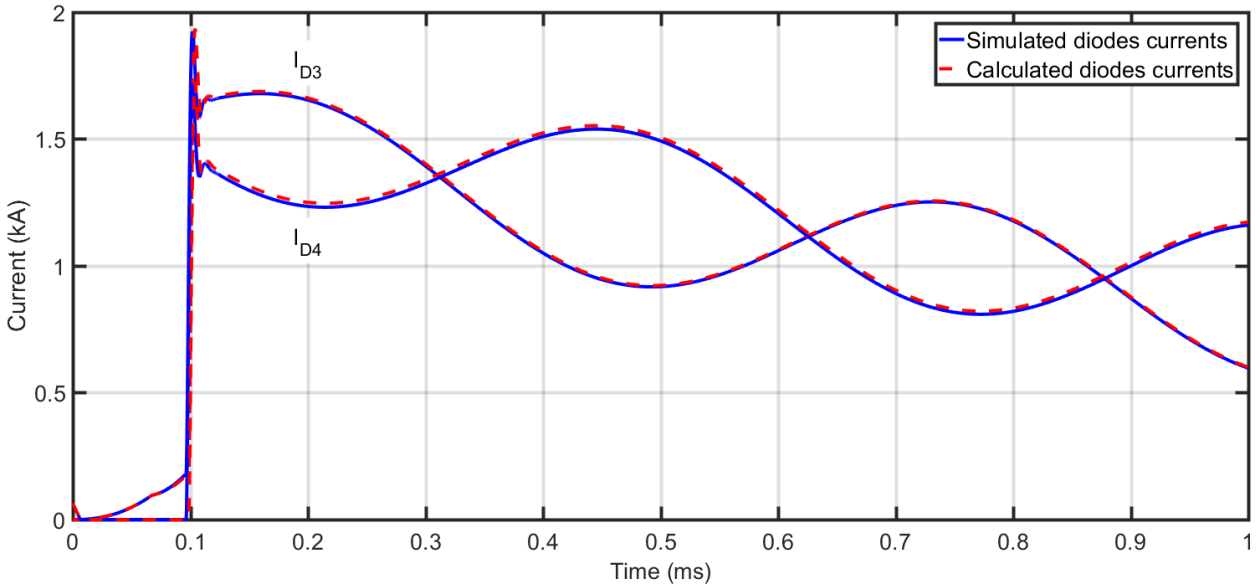


Figure 2.57: Comparison of simulated and calculated diode 3 and 4 currents at maximum speed condition with 5m cable fault

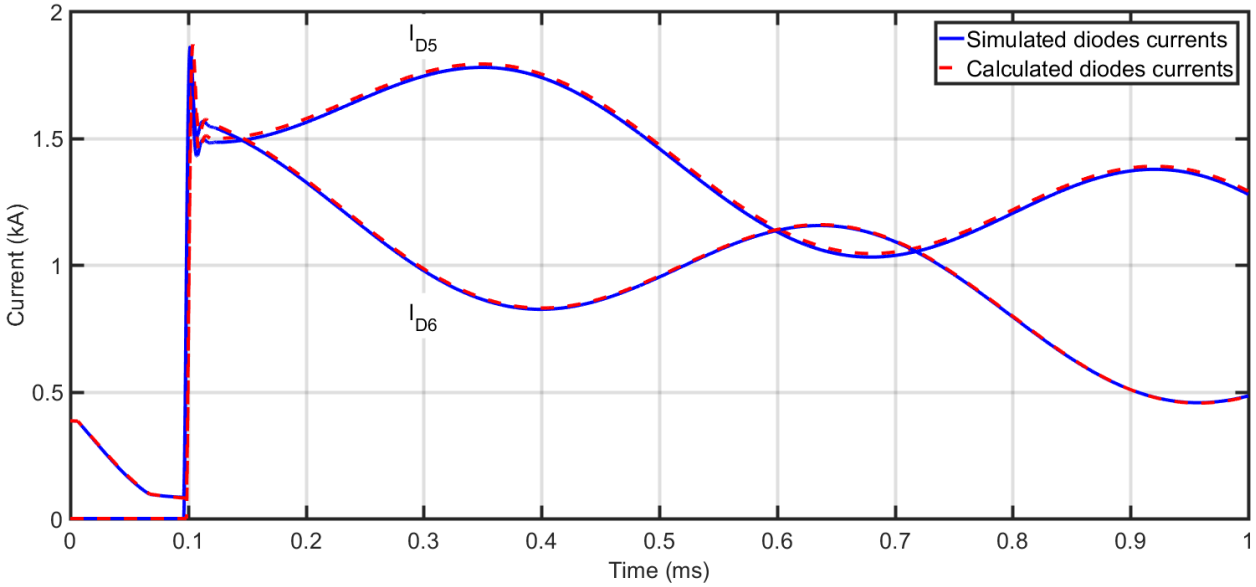


Figure 2.58: Comparison of simulated and calculated diodes 5 and 6 currents at maximum speed condition with 5m cable fault

Figure 2.53-2.58 demonstrate excellent matching (within 5%) between expected and simulated diodes currents. They also demonstrate significant improvement in accuracy compared with previous work [3]. This is because previous work:

1) Underestimated the time at which the peak magnitude is reached, due to the time boundary between diode blocking and conduction stages being taken as the time at which the DC-link voltage reaches 0V (not *-2Vj*). This is a relatively insignificant error.
2) Underestimated the magnitude of the peak, due to the capacitor's branch contributions being disregarded. This error is especially significant for the 0.5m case where the actual magnitude of peak diode current exceeds that expected from [3] by about 1kA. For the 5m case, the magnitude of peak diode current is about 400A higher than expected from [3].
3) Underestimated the amount of damping the DC side contributions experience, due to the diodes being considered ideal (without any voltage drop or resistance). This error is most significant for the 0.5m case as less overall damping is present in the circuit. The damping caused by the cable impedance dominates that caused by the diodes for the 5m case.
4) Did not consider AC side contributions. This error is most significant for the 5m case as AC side contributions represent a larger portion of the overall diode current. Not accounting for these contributions can results in significant under or over estimation of the diode stress, depending on the diode's location in the converter circuit.

2.5.6. Diodes Temperatures Rise

Based on diodes currents found in the previous section and the thermal impedance of the semiconductor module, the increase in diodes junction temperatures ($\Delta T_j(t)$) are determined in this section. Power losses incurred by a diode from conducting current ($i_D(t)$) can be found as:

$$P(t) = V_j\, i_D(t) + R_s(i_D(t))^2 \tag{2.97}$$

Furthermore, the thermal impedance seen by the diodes (junction-to-ambient) during a transient event of less than 1s in duration can be approximated to be that from junction-to-case, disregarding the effect of the heatsink [10]. This simplifies the problem as the junction-to-case thermal impedance is typically given in the semiconductor module's datasheet, and can be curve fitted to the following function [17]:

$$Z_{th(J-c)}(t) = \sum_{i=1}^{n} R_i\,(1 - e^{-\frac{t}{R_i C_i}}) \tag{2.98}$$

where R_i and C_i are the resistances and capacitances of the ith branch in a Foster equivalent thermal network, as shown in Figure 2.59.

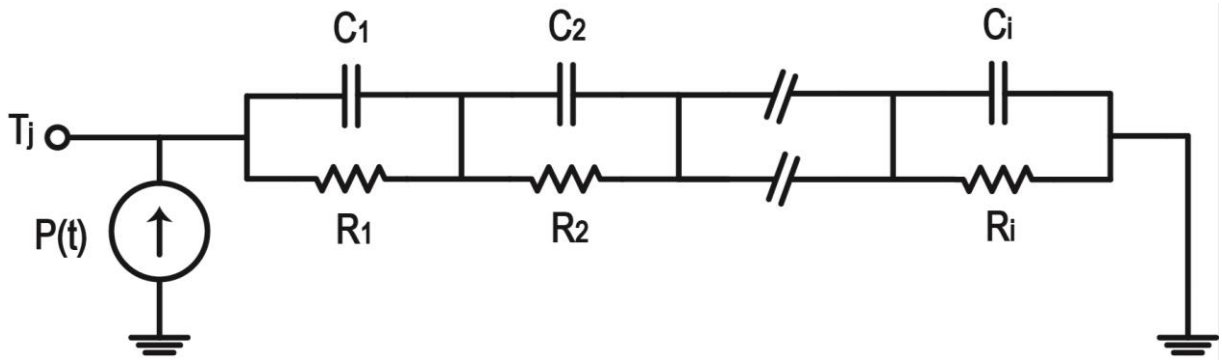


Figure 2.59: Illustration of Foster equivalent thermal network

Thermal impedance represents the thermal response of the module to a 1W step in power (step response). The impulse response can therefore be found as the derivative of the step response, such that:

$$\frac{d}{dt}Z_{th(J-C)}(t) = \sum_{i=1}^{n} \frac{e^{-\frac{t}{R_i C_i}}}{C_i} \tag{2.99}$$

Finally, if the power loss are found from (2.97) as *P(t)*, and the thermal impedance is found from curve fitting datasheet's curves to (2.98) as $Z_{th(J-C)}$, the junction temperatures rise can then be found using the convolution integral [17], as:

$$\Delta T_j(\tau) = \int_0^{\tau} P(t)\frac{d}{dt}Z_{th(J-C)}(\tau - t)dt \tag{2.100}$$

For the semiconductor module under consideration in this work [14], the junction-to-case thermal impedance was found to fit (2.98) best when the foster model resistances and capacitances are as shown in Table 2.4, as compared in Figure 2.60.

Table 2.4: Foster thermal network curve fitting parameters

i	R_i (mΩ)	C_i (F)
1	73.35	1.433
2	18.26	0.1099
3	60.05	4.406

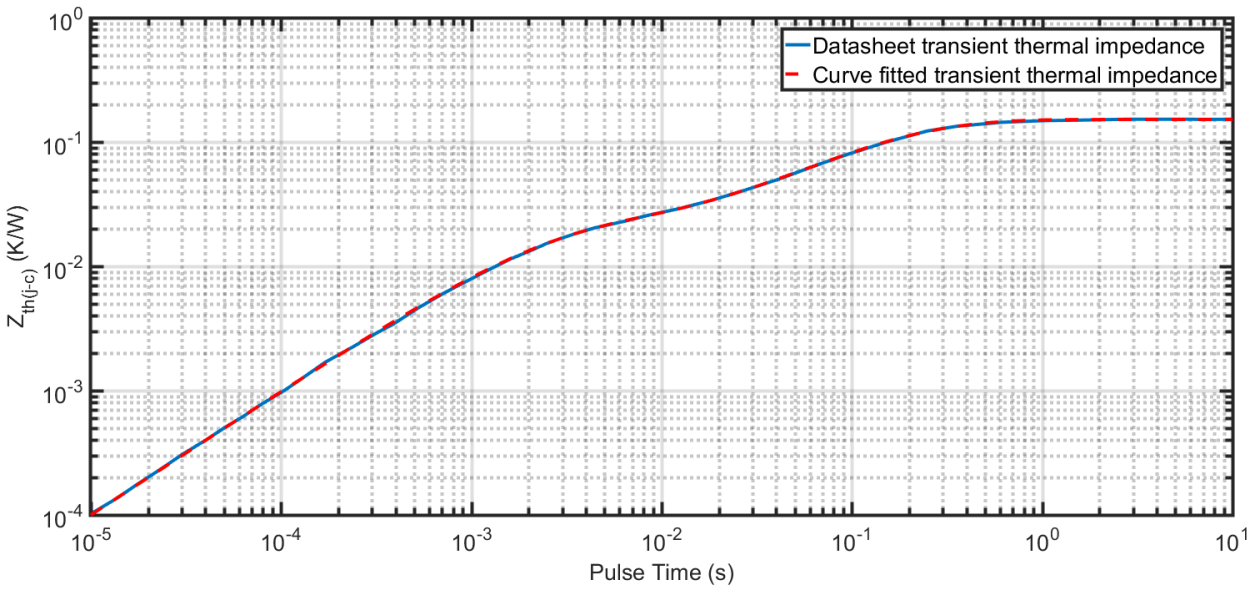


Figure 2.60: Comparison of datasheet thermal impedance with that obtained from curve fitting (2.98) using parameters in Table 2.4

Thermal networks with resistance and capacitance parameters specified in Table 2.4 were included in the simulation circuit of the combined fault response, as shown in Figure 2.61. Results obtained from this simulation were compared to those obtained analytically as shown in Figure 2.62-2.64 and Figure 2.65-2.67 for the 0.5m and 5m cable faults respectively. Comparisons demonstrate that simulation results match predictions very well, validating the presented analyses.

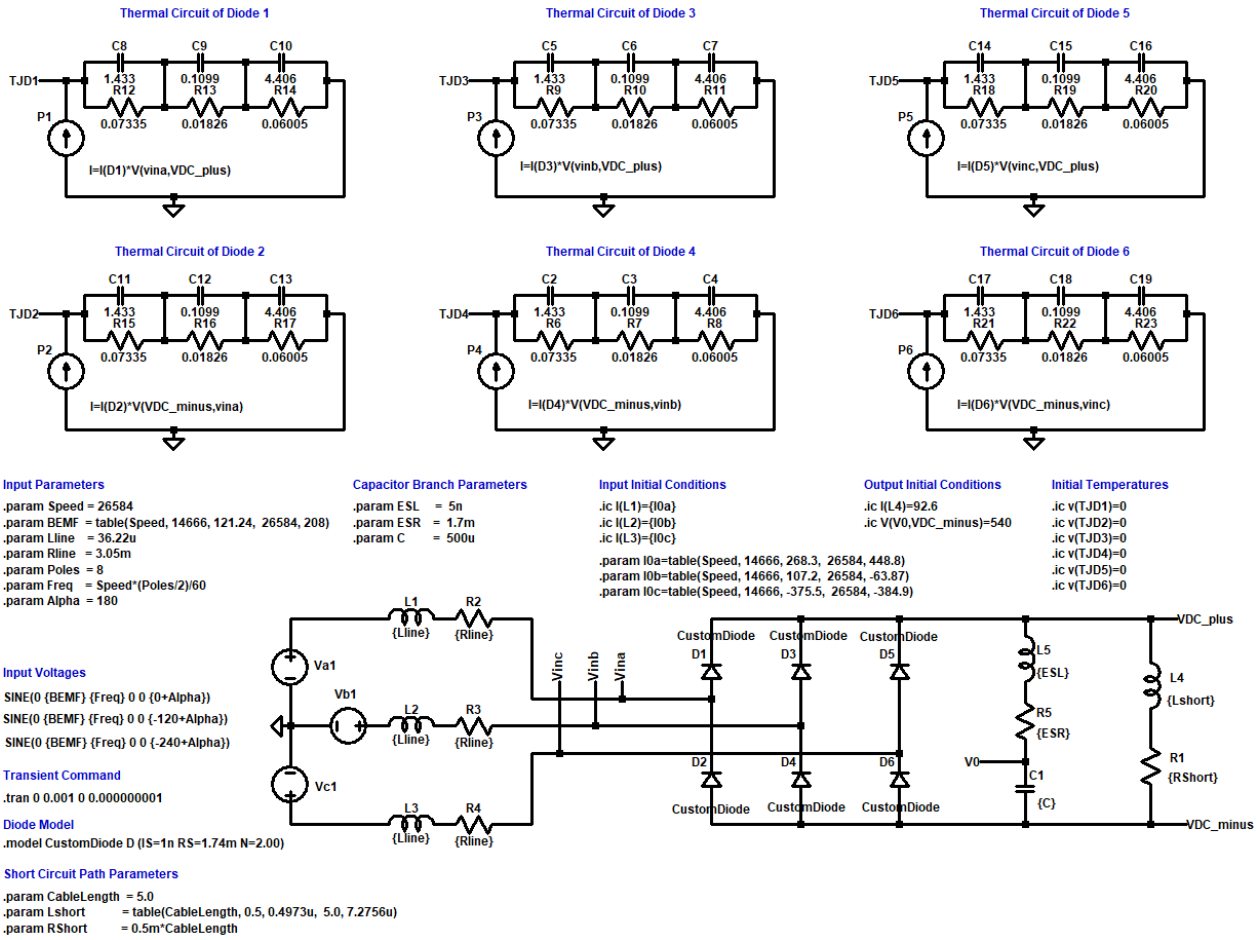


Figure 2.61: Diodes junction temperatures rise simulation circuit (combined response at maximum speed, 5m cable fault, and $\alpha = \pi$)

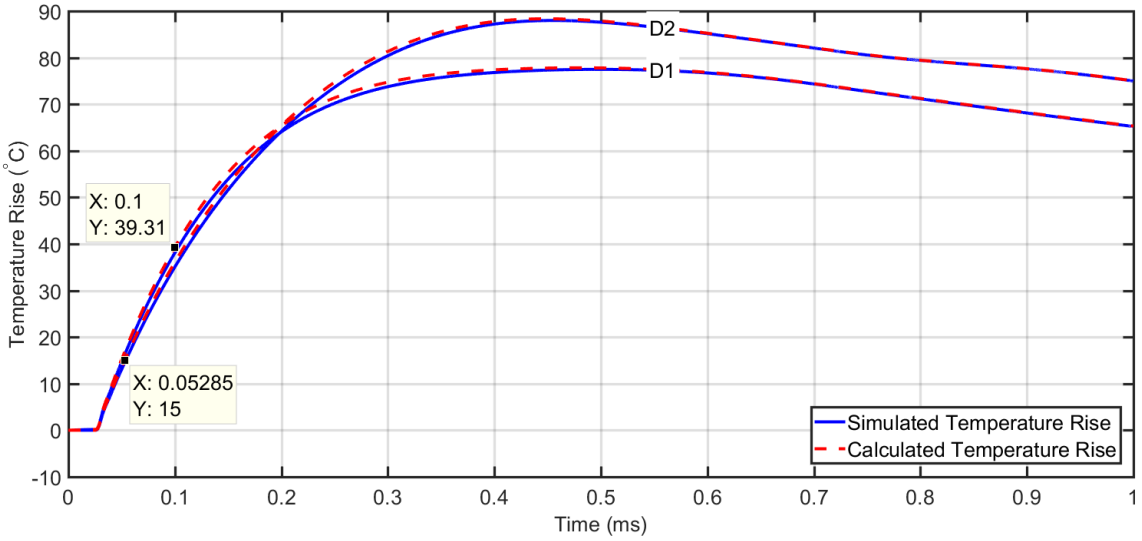


Figure 2.62: Comparison of simulated and calculated D1 and D2 temperature rise for a 0.5m cable fault at maximum speed

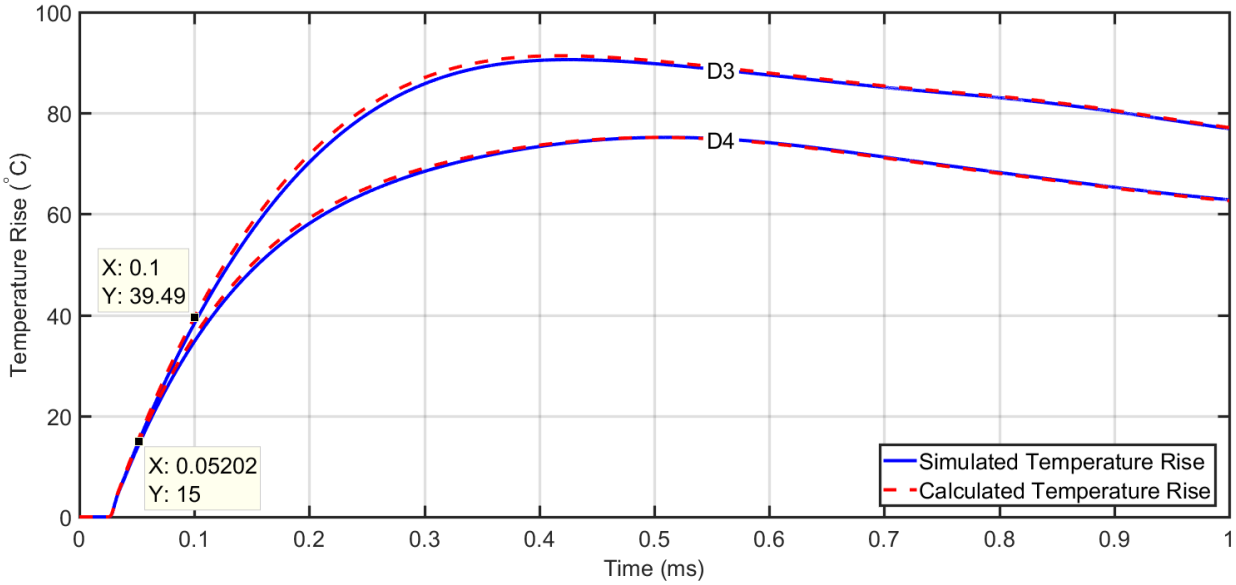


Figure 2.63: Comparison of simulated and calculated D3 and D4 temperature rise for a 0.5m cable fault at maximum speed

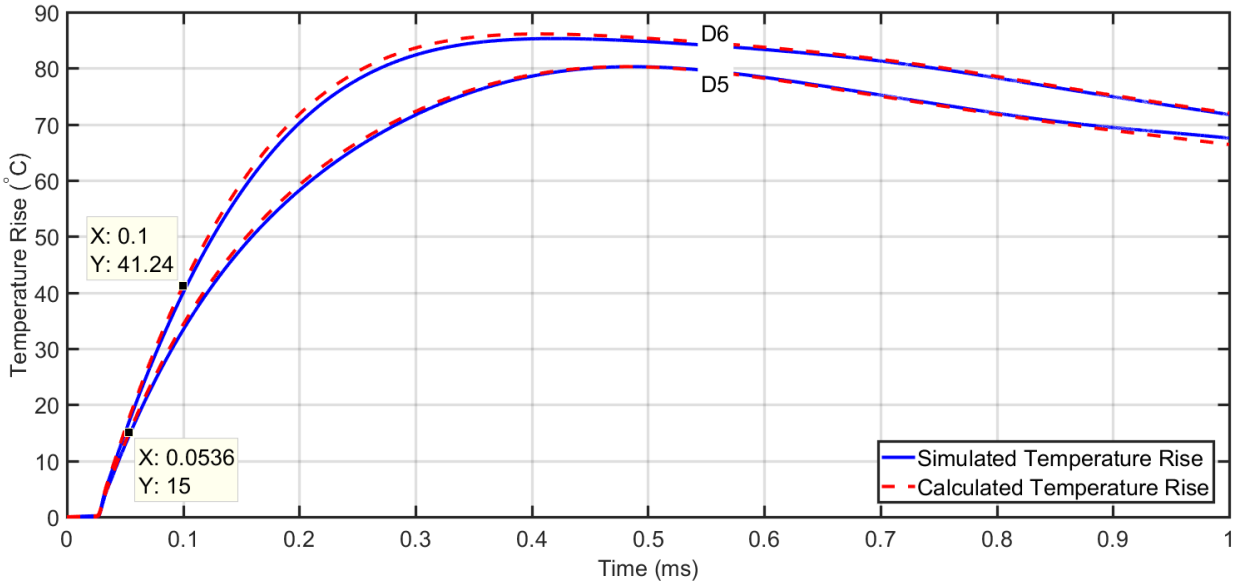


Figure 2.64: Comparison of simulated and calculated D5 and D6 temperature rise for a 0.5m cable fault at maximum speed

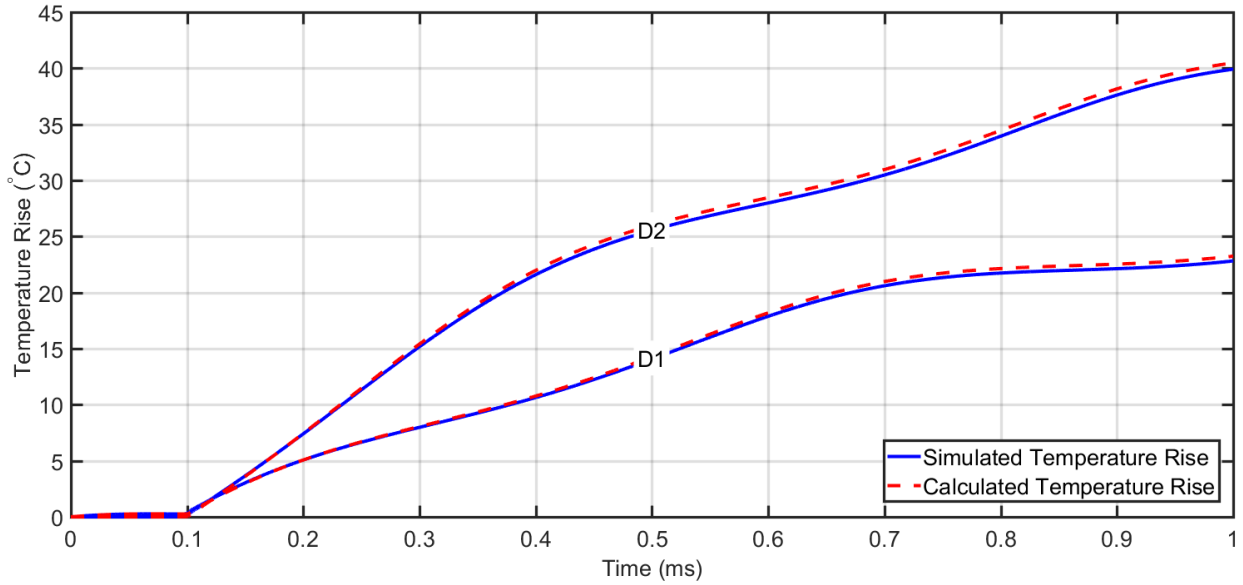


Figure 2.65: Comparison of simulated and calculated D1 and D2 temperature rise for a 5m cable fault at maximum speed

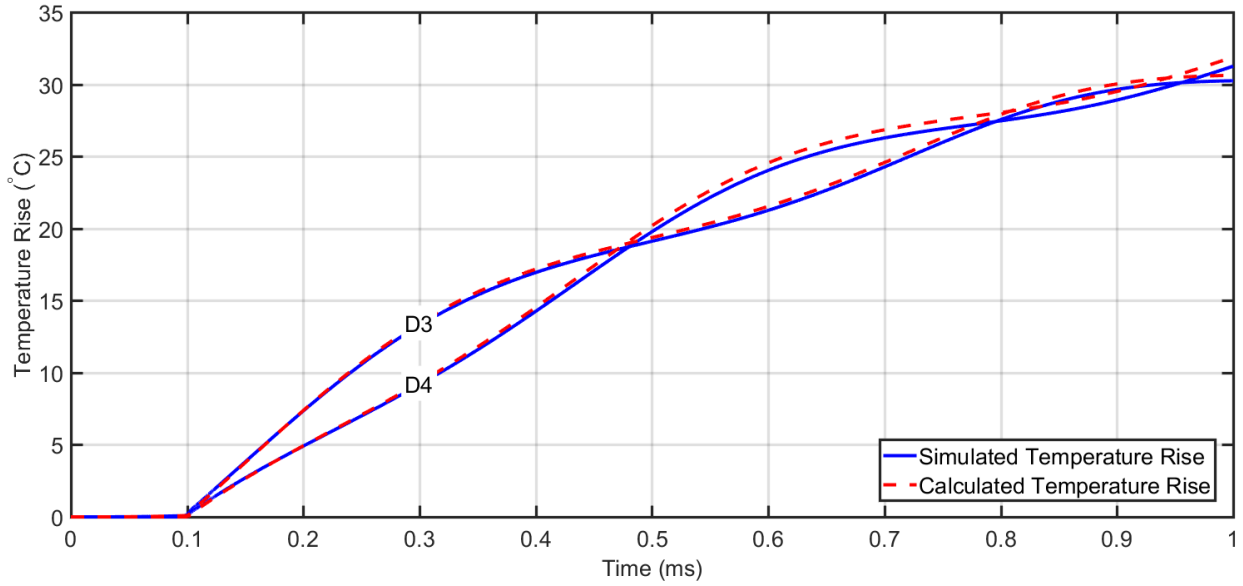


Figure 2.66: Comparison of simulated and calculated D3 and D4 temperature rise for a 5m cable fault at maximum speed

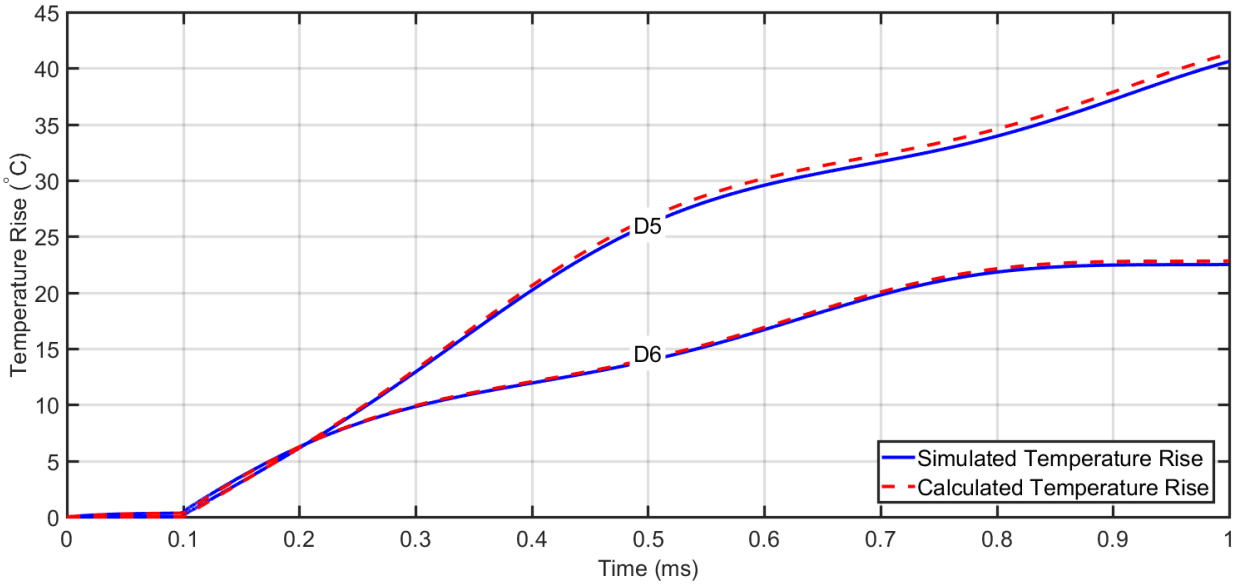


Figure 2.67: Comparison of simulated and calculated D5 and D6 temperature rise for a 5m cable fault at maximum speed

Figure 2.62 - 2.67demonstrate excellent matching (within 5%) between calculated and expected rise is diodes junction temperatures for both the 0.5m and 5m fault conditions. The diodes temperatures rise rapidly exceeding the typical 15°C safety margin within less then 50µs during the worst case 0.5m condition and 300µs during the 5m condition.

2.6. Conclusions

In this chapter analyses of voltage source converters under the worst-case fault scenario (DC line-to-line short-circuit condition) were presented to aid in defining the requirements of the protection devices in terms of operation conditions, locations, reaction times, and allowable weights. Outcomes regarding each of these objectives are presented next:

1) *Operation conditions:* in this work, expressions for currents and voltages at various locations of interest in the system were derived. Those expressions describe the reaction of the system during the fault and its dependency on various system parameters. The derived characteristics will be used to:

    a. Determine the amount of current the protection devices must be capable of isolating or limiting, which influences their required capacity, and thus, size and weight.

b. As baselines to compare against the obtained characteristics when protection devices are included, so that any benefits can be demonstrated.

2) *Locations:* the contributions of various sources in the system to fault currents were defined, which enables determining the effectiveness of isolating these sources. It was found that for the system under consideration, the contributions of the DC side capacitors to fault currents are most significant. Thus, rapid isolation of the capacitors can significantly alleviate resulting damage. Isolation or limiting of the AC side only is ineffective.

3) *Reaction time:* Obtained fault currents characteristics enable determining the required reaction time before components limits are reached. Times at which the capacitor or diodes reach their maximum rated currents can be found directly from characteristics derived in this work. For the system under consideration, it was found that the capacitor reaches its maximum current of 10kA [13] after only ≈ 10µs of the fault under the worst case 0.5m cable fault, as shown in Figure 2.51 and Figure 2.52. Whereas, the diodes reach their maximum single event current ratings (I_{FSM}) of 2.43kA [14] after only ≈ 25µs of the fault under the worst case 0.5m cable fault, as shown in Figure 2.53 - 2.55. Furthermore, depending on the amount of safety margin implemented in the design, times at which the maximum diodes junction temperatures are reached can also be determined. For the system under consideration, a 15°C safety margin was implemented, providing only ≈ 50µs of spare time before the maximum junction temperature of the diodes is exceeded under the worst case 0.5m cable fault, as shown in Figure 2.62-2.64.

4) *Allowable weight:* a trade-off can be made between oversizing or derating the system to be capable of withstanding a fault for a certain duration of time, and including a device which protects the system during this period (current limiter). This tradeoff can be used to determine the allowable weight of the protection device. For example, for the system under consideration in this work, it was found that the junction temperature of the diodes rises by ≈ 40°C within 100µs of the fault. This means that the diodes would have to be de-rated by more than 40°C under nominal conditions for them to maintain their ratings under a fault condition lasting up to 100µs. This can only be accomplished by reducing the output power of the converter to approximately the half, which leads to an effective increase of weight to

the double, if nominal output power are to be maintained. Therefore, the allowable weight for a limiter that operates for up to a 100µs is as much as the weight of the converter itself.

2.7. References

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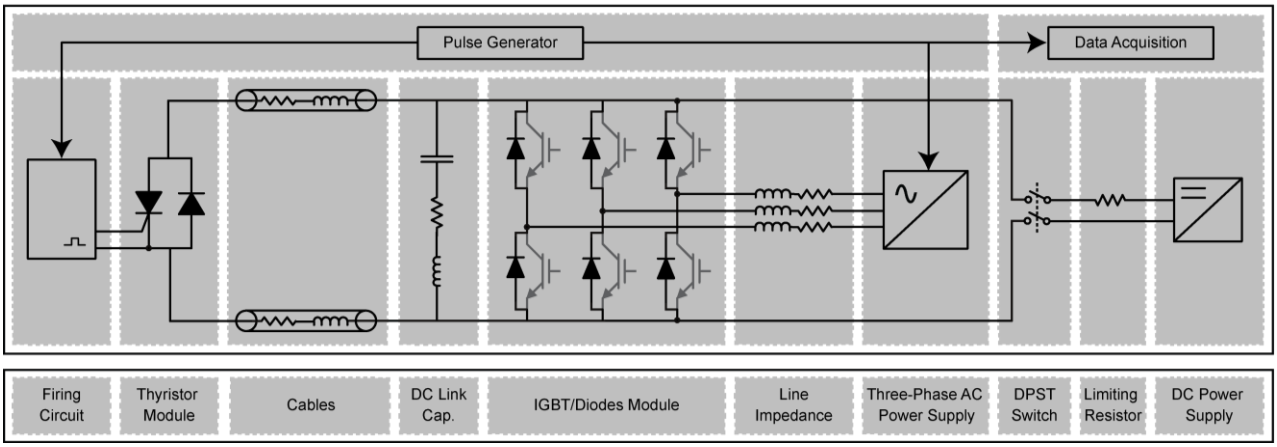
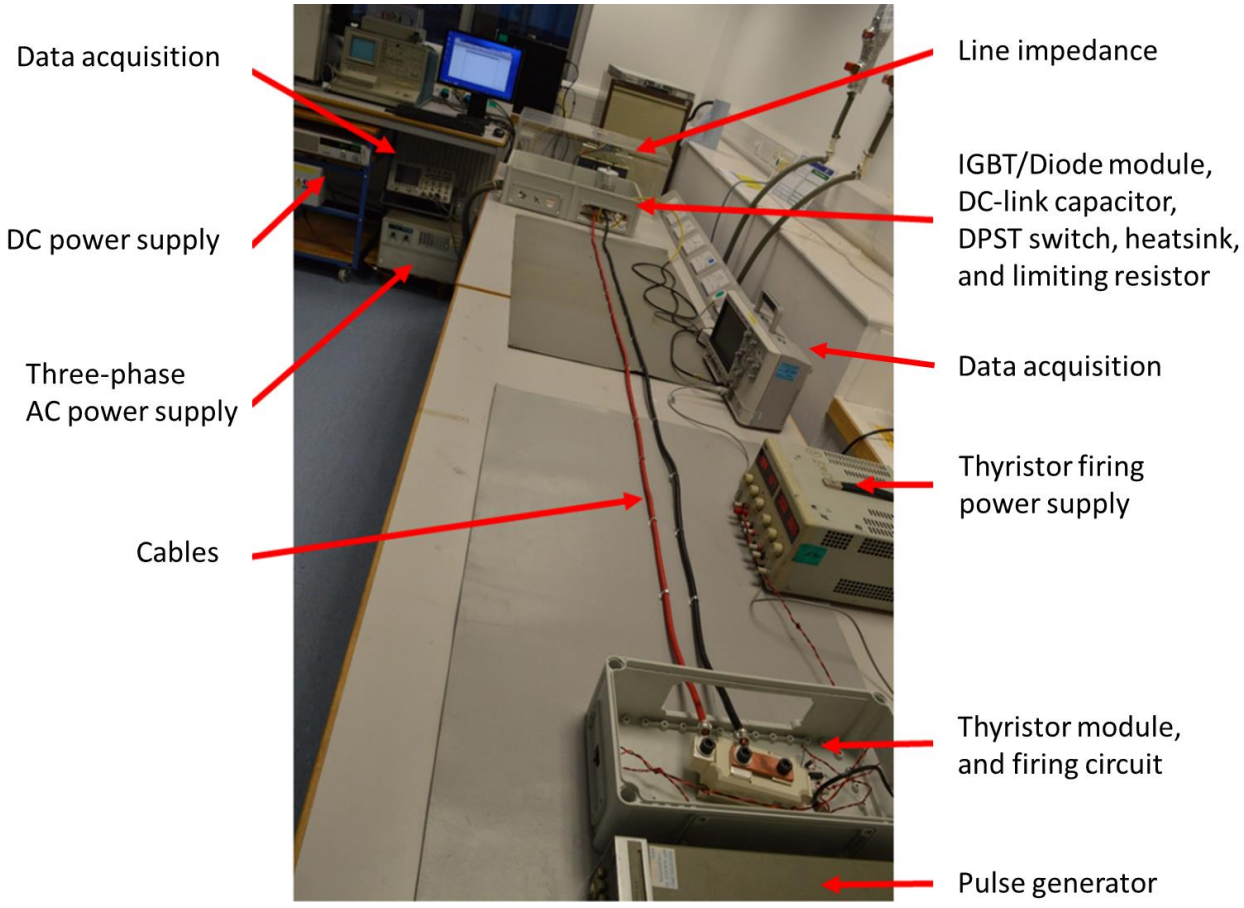
Chapter 3: Experimental Validation of Voltage Source Converters' DC Line-to-Line Fault Response Analyses

3.1. Introduction

This section details the experimental validation of the DC line-to-line short-circuit fault analyses presented in Chapter 2. The validation setup is based on a single channel replica of a dual channel motor drive designed and built for aerospace applications. This type of fault testing was not possible with the original system due to the high risk of causing damage and high cost of repair. The system was also not available at the time this work was completed as it was undergoing dyno testing at a Rolls-Royce facility. The setup, shown in Figure 3.1, utilizes as many components of the original system as possible; including the same converter module and heatsink. The DC-link capacitor used in the original system [1] could not be utilized in this experiment due to its complex geometry which requires specialized busbars. The capacitor in the original system has 16 terminals arranged circumferentially on the top side of its packaging to reduce the ESL and ESR. This is not a feature of standard aerospace capacitors but rather a feature of the specific capacitor technology used in the original system. Furthermore, the converter in original system is integrated vertically so that the top side of the heatsink is utilized for cooling the power module and the bottom side for cooling the busbars and capacitor. An alternative capacitor with the same capacitance but simpler geometry is used for the experiments carried out in this chapter. In addition, the converter is arranged horizontally for easy access to terminals. A programmable AC power source generates phase voltages that has comparable BEMF and frequency to the original system's machine. However, it has significantly lower output power capacity forcing the line impedances to be increased, compared to the original system, to ensure phase currents are maintained within the limits of the supply. Finally, the DC-link voltage used in this experiment matches the original system's voltage (540V).



(a)



(b)

Figure 3.1: (a) Overview diagram, and (b) picture of experiment setup

Prior to testing the DC-link capacitance is initially charged by a DC power supply. This provides the initial conditions to the circuit, referred to as V_0, which is isolated prior to testing via a Double

Pole Single Throw (DPST) switch. A pulse generator then simultaneously triggers the fault switch to emulate a DC line-to-line fault condition, the AC power supply to generate the phase input voltage and oscilloscope to capture the fault response.

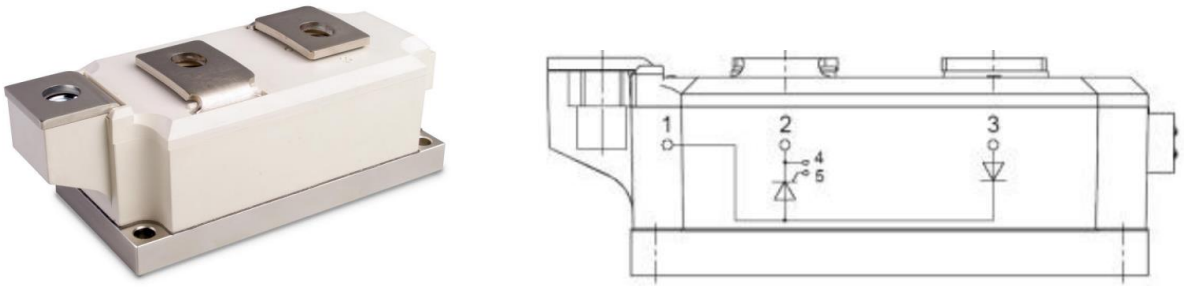
The next section of this chapter describes the main components used in this experiment, and presents analyses and measurements carried out to characterise these components. The extracted characteristics are then used in the following section to facilitate comparing measured and expected fault response. The final section summarises the conclusions of this chapter.

3.2. Experiment Setup Components

3.2.1. Fault Switch

A) Thyristor and Diode Module

A thyristor module with an integrated antiparallel diode was selected to act as the fault switch due to its high peak-current capacity and approximately linear output characteristics (no current saturation) when compared to MOSFETs and IGBTs. The power module, shown in Figure 3.1, is capable of handling 18kA peak current [2], which is sufficient considering the expected fault currents, as analysed in Chapter 2. The thyristor is used to trigger the fault event, whereas the anti-parallel diode is included to provide reverse current conduction path (freewheeling path) for inductances in the circuit. Lack of this path can result in a reverse voltage across the thyristor that exceeds its reverse breakdown rating of 1.7kV (V_{BR} shown in Figure 3.3).



(a) (b)

Figure 3.2: Thyristor/diode module (a) picture, and (b) internal connections [2]

Given that sufficient current is supplied to the gate of the thyristor by the driving circuit ($IG>>0$), its output characteristics, shown in Figure 3.3 can be represented by a forward voltage drop (V_F)

and a series resistance (R_F). The series resistance is taken as the slope of the line connecting rated current (I_{FAV}) and 25% of the rated current points, while the forward voltage drop is taken as the point where that line intersects the voltage axis [3]. The maximum values of those parameters are given for this module as 0.88V and 0.45mΩ respectively [2].

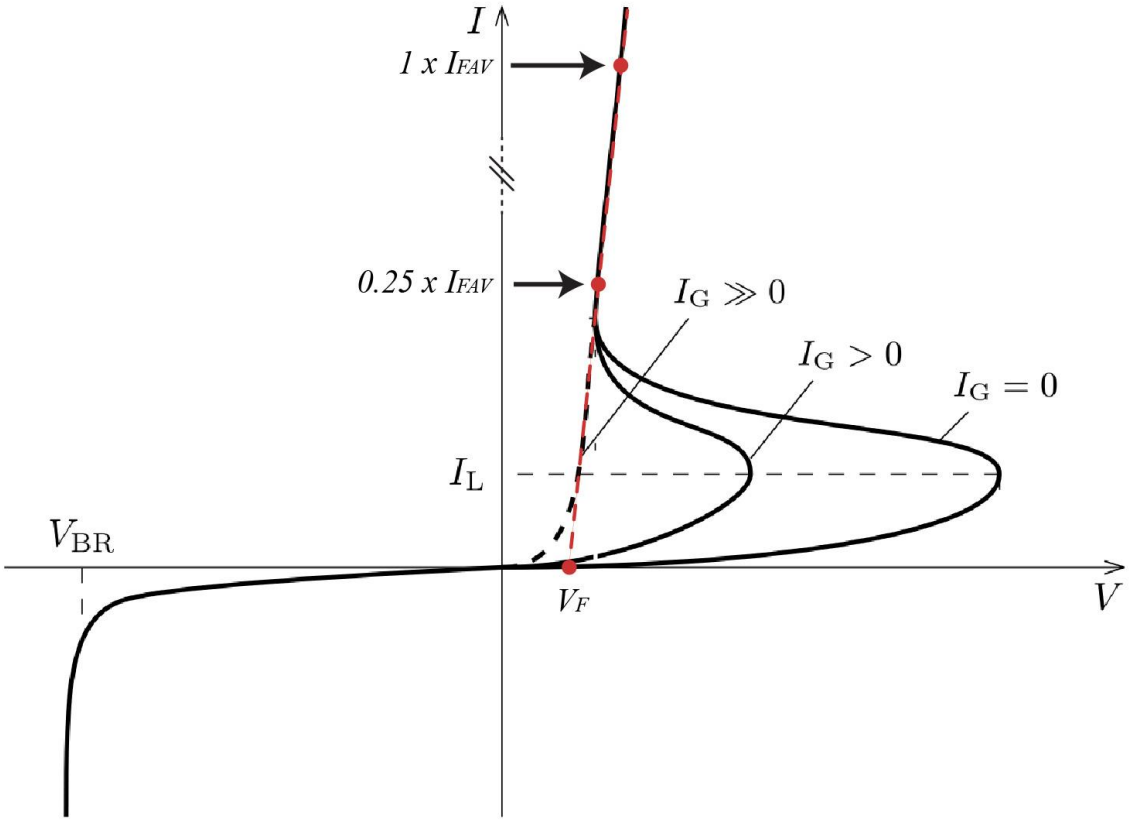
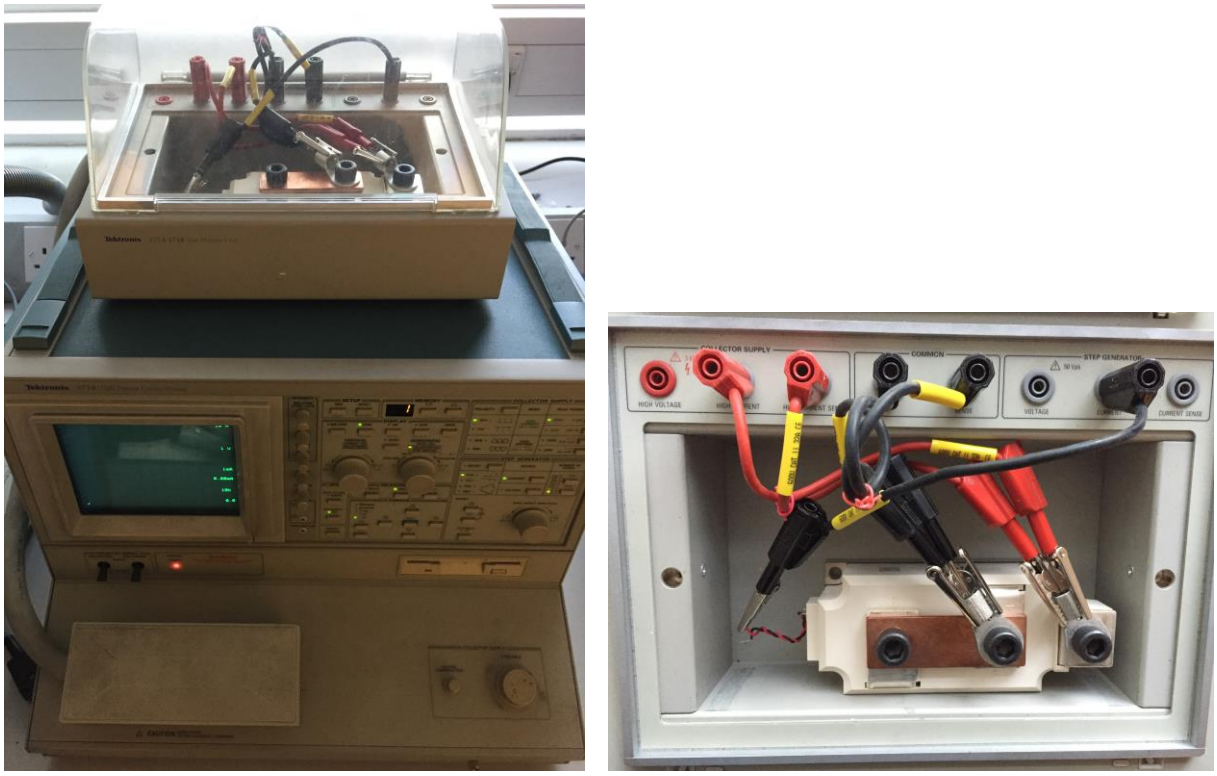


Figure 3.3: Typical thyristor output characteristics. Modified from [4]

Datasheet specifications for the thyristor are given for the typical operation frequency of the device. Since thyristors are typically operated in line commutated converters, their characteristics are optimized for low frequency switching (50-60Hz) [3]. Higher forward voltage drop (V_F) and resistance (R_F) are therefore expected in higher switching applications. To account for the increase in the thyristor's forward voltage drop and resistance, the output characteristics of the device was measured using the Tektronix 371B curve tracer. This instrument measures the thyristor's output characteristics using current pulses of 250µs in duration [5]. The results represent the thyristor's response to 4kHz frequency currents (1/250µs), as opposed to 50-60Hz given in the datasheet. The

setup used for this measurement is shown in Figure 3.4. The measured output characteristics are shown in Figure 3.5 for 200mA steps of thyristor gate currents (I_G) from 200mA to 1A.



(a) (b)

Figure 3.4: (a) Output characteristics measurement setup, and (b) connections

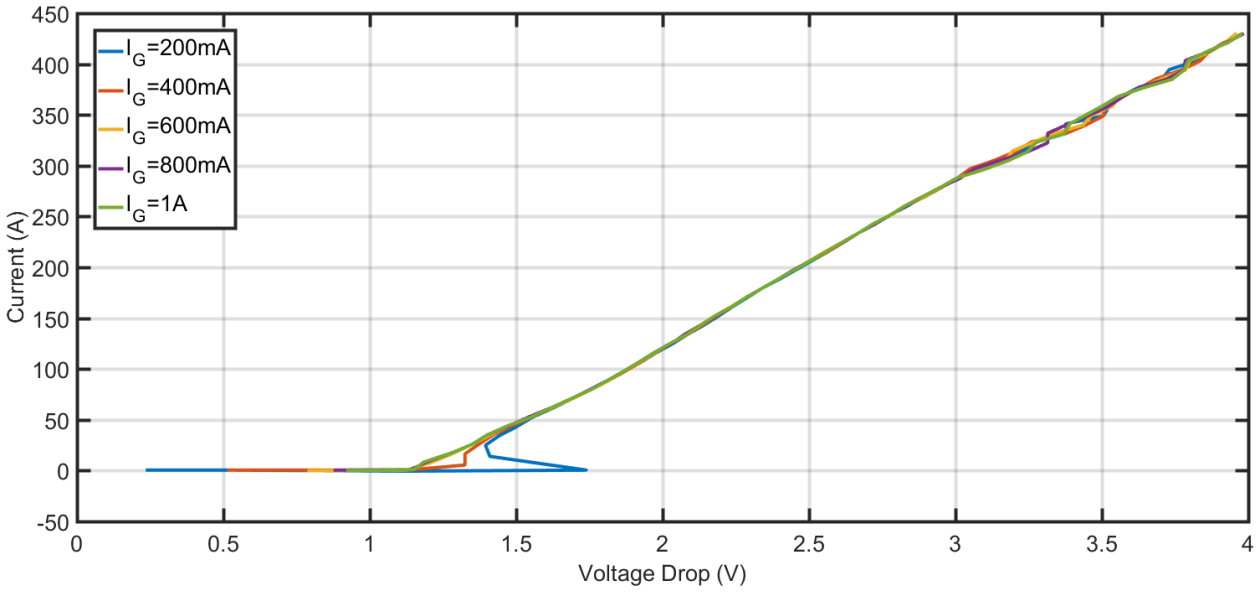


Figure 3.5: Measured thyristor output characteristics

The method described previously to extract the equivalent forward voltage and resistance (V_F and R_F) of the thyristor was applied to the measured output characteristics of the thyristor at 1A gate current as shown in Figure 3.6. This gate current magnitude was selected because the firing circuit was designed to supply this current.

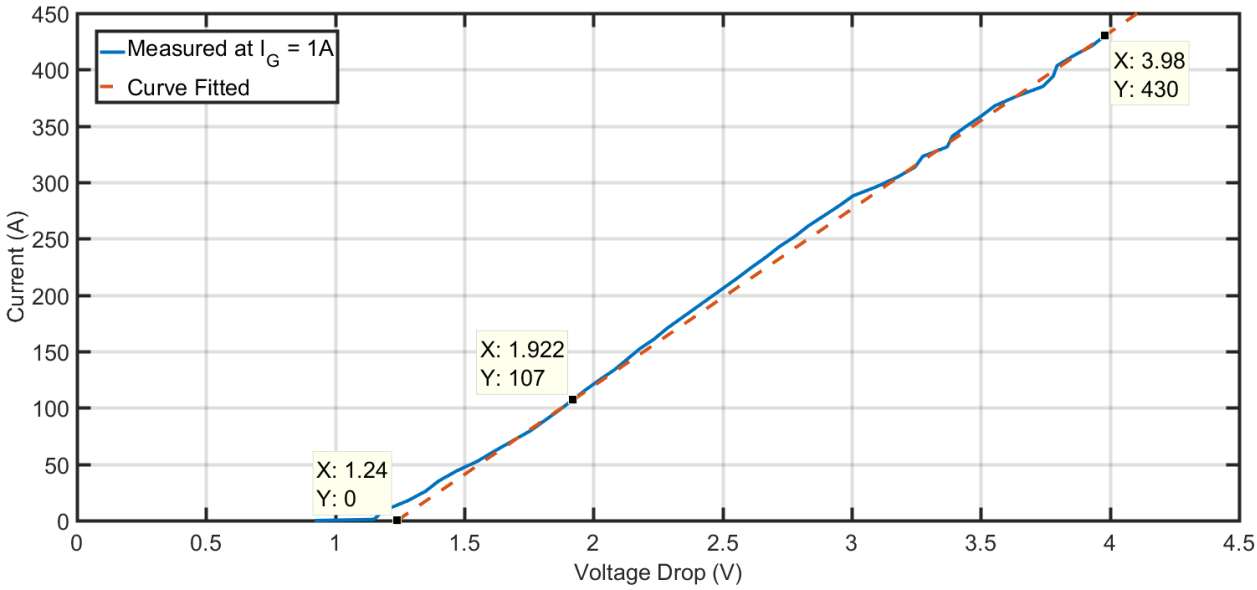


Figure 3.6: Comparison of measured and curve fitted thyristor output characteristics. Curve fitting extraction points shown.

Extracted voltage drops and resistances are compared to datasheets values as shown in Table 3.1. As expected, measured parameters exceed datasheet values due to the higher frequency of measurement.

Table 3.1: comparison of measured and datasheet thyristor parameters

Component	Parameter	Measured Value	Datasheet Value
Thyristor	V_F (V)	1.24	0.88
	R_F (mΩ)	6.4	0.45

B) Firing Circuit

To trigger the thyristor emulating a fault event, a firing circuit was designed with the following objectives:

A) Ensure that sufficient current is supplied to the thyristor's gate to result in safe turn-on ($I_G >> I_{GT}$), where the gate threshold current (I_{GT}) is given as 100mA for the thyristor used, as shown in Figure 3.7.

B) Ensure that gate current is maintained until the device's main current exceeds latching level (I_L), as illustrated in Figure 3.3. The maximum latching current is given for this device as 2A [2].

C) Ensure that while the gate current is high enough in magnitude and duration to result in safe turn-on and latching, it is limited in power so that gate's power rating (P_{Gate}) is not exceeded. For the thyristor module used, the maximum power that can be dissipated through the gate is 150W for 0.1ms, as shown in Figure 3.7.

D) Protect the thyristor from reverse gate voltage. A reverse voltage of a few volts can result in device damage [3].

E) Limit the rate of rise and peak gate to cathode potentials. Excessive gate-to-cathode potentials can occur as result of stray inductances in the gate current's path, and result in gate-to-cathode junction breakdown.

F) Provide means of isolating controls from power potentials, since the pulse generator is not capable of floating up to the high potentials of the converter circuit.

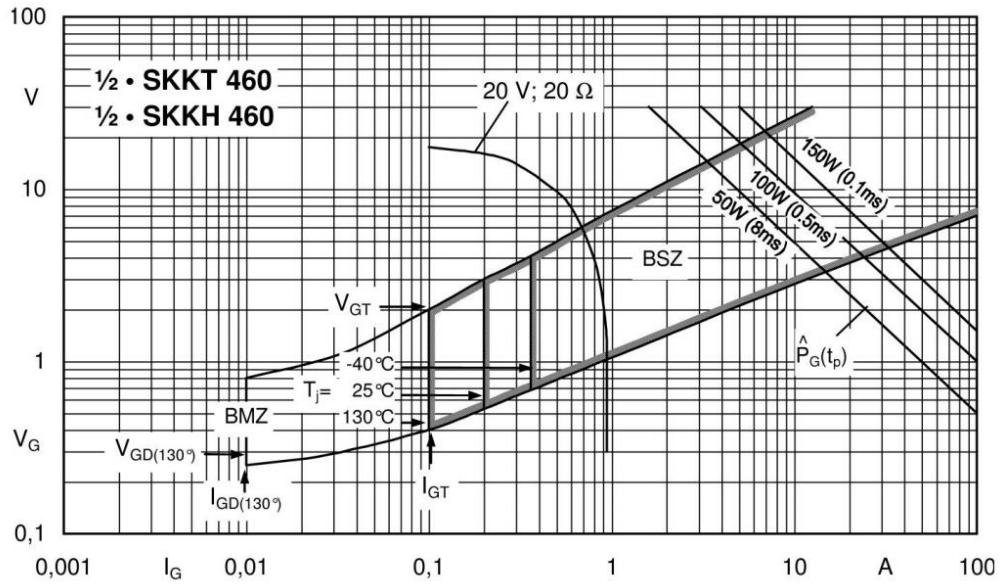
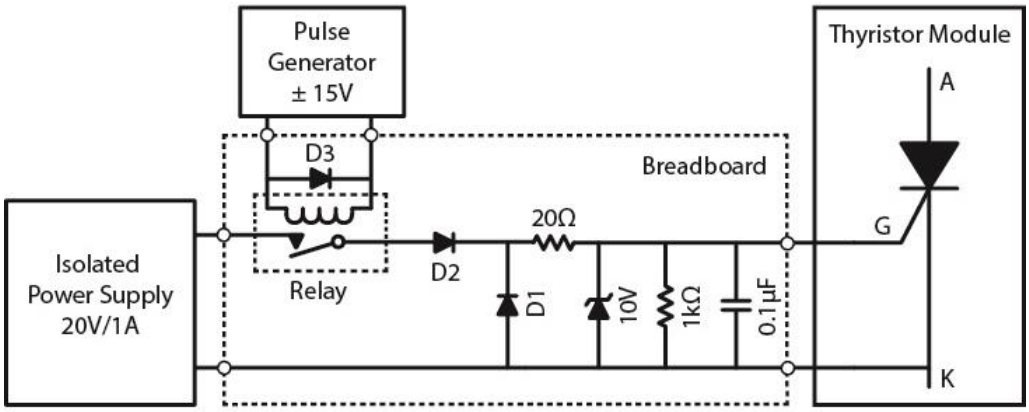
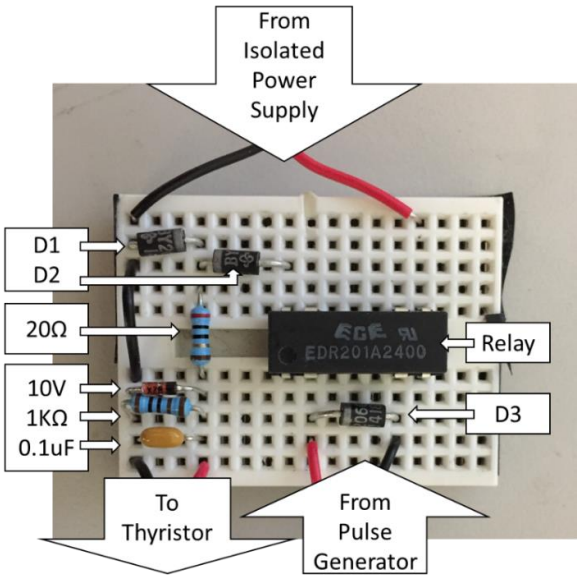


Figure 3.7: Thyristor gate trigger characteristics [2]

The firing circuit was realized as shown in Figure 3.8. A 0.1µF capacitor is placed at the output of the driving circuit to limit the rate of rise of gate to cathode potential, with a 10V Zener diode in parallel to limit the peak value. A 1kΩ resistor in parallel with the capacitor and Zener diode provides a discharge path for the thyristor when it is disengaged, whereas diodes (D1 and D2) provide reverse current and potential protection. A 20Ω current limiting resistor sources sufficient firing current when combined with a 20V power source, as shown in the firing characteristics of Figure 3.7. Finally, a relay provides means of triggering the firing circuit from a pulse generator that is isolated from the high potentials of the main circuit. Due to the simplicity of this circuit, it was implemented on a breadboard, as shown in Figure 3.8.



(a)



(b)

Figure 3.8: (a) Schematic and (b) picture of implemented firing circuit

3.2.2. Cables

It was determined in Section 2.5.1 that a cable size of 2AWG is suitable for carrying the 92A DC current nominally produced by the converter under consideration, in accordance with MIL-STD-975. However, a cable size of 3AWG was selected for this experiment due to its availability. This is appropriate since cable current ratings specified in MIL-STD-975 are often exceeded in aerospace to reduce weight, driving temperatures beyond the 70°C limit specified in the MIL-STD. Cable length was selected to produce sufficient fault inductance (L_{short}), so that the thyristor's *di/dt* rating is not exceeded. It was found in section 2.2 that the maximum rate of rise of fault current occurs at the initial fault time ($t=0$) and is equal to V_0/L_{short}, where V_0 is the initial capacitor current, and L_{short} is the short-circuit path's inductance. Given the thyristor's maximum *di/dt* rating of 250A/µs [2] and the capacitor's initial voltage of 540V, the minimum loop inductance required was found to be 2.16µH. The distance between the positive and return cables was fixed at 4.5cm using clips, as shown in Figure 3.9. This distance was selected to match that between the capacitor's terminals (4.5cm) [6] and between the thyristor module terminals (4.4cm) [2], so that the mutual inductive coupling between the two cables is uniform throughout their lengths.

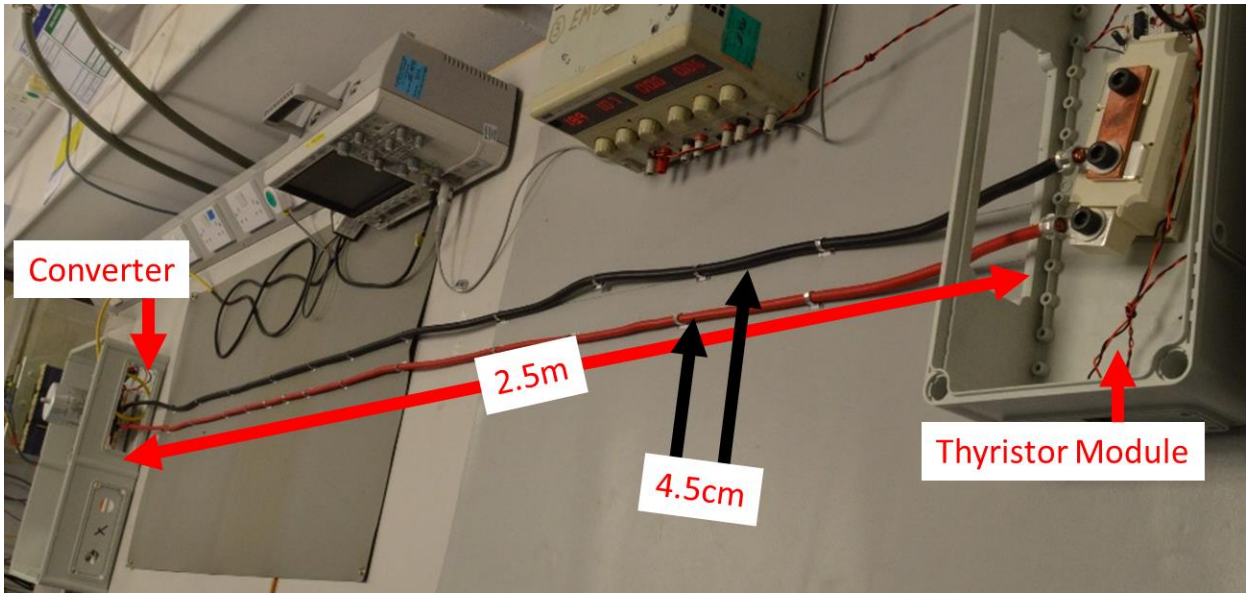


Figure 3.9: Picture of cables arrangement

The inductance and resistance of the cables were extracted, so that they can be accounted for when calculating the expected fault response (as L_{short} and R_{short}). The inductance and resistance are first calculated using (2.83) - (2.86), and then measured using an LCR meter to extract frequency dependent values. The LCR meter measurement was performed to account for the skin effect, which results in current being constrained in the outer portions of conductors at high frequencies, decreasing the effective cross-sectional areas, and thus, increasing resistance and decreasing inductance.

A) Calculation of Cables DC Inductance and Resistance

Given the cables' radius (r) of 2.915mm (3AWG) and separation distance (D) of 4.5cm, the self and mutual inductances vs. length were calculated using (2.83) and (2.84) respectively as shown in Figure 3.10.

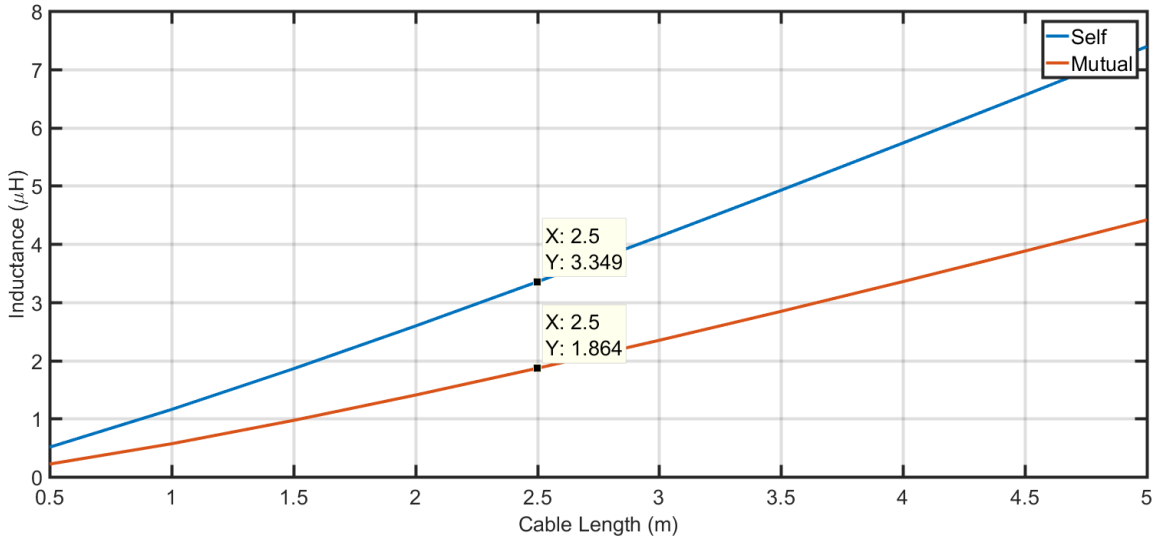
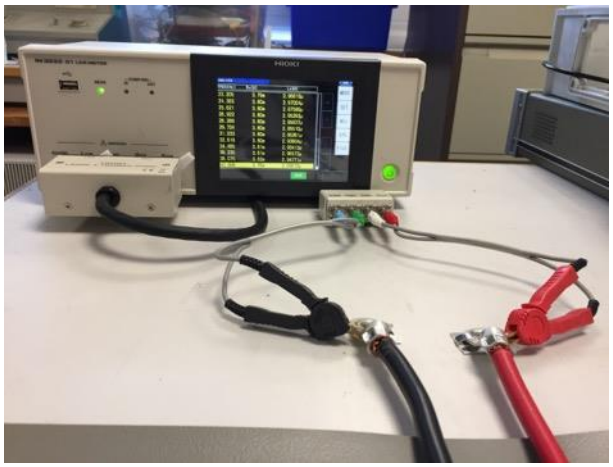


Figure 3.10: Calculated cables self and mutual inductances vs. length

To maintain the total fault path's inductance (L_{short}) above that required by the thyristor module, a cable length of 2.5 meters was selected. The total inductance for this length was calculated using (2.85) to be 2.97μH. The per-meter resistance of the cable was calculated using (2.86), given a resistivity (ρ) of $1.72x10^{-8}$ohms. m for annealed copper [7] to be 0.64mΩ/meter. This results in a total fault path's resistance (R_{short}) of 3.22mΩ for the total cable length.

B) Measurement of Cables' AC Inductance and Resistance

The frequency dependent resistance and inductance of the cables were then measured using the HIOKI IM3533-01 LCR Meter in the setup shown in Figure 3.11, as plotted in Figure 3.12 and Figure 3.13 respectively.



(a)

(b)

(c)

Figure 3.11: LCR meter measurement setup (a) view from converter side, (b) from thyristor module side, and (c) overview

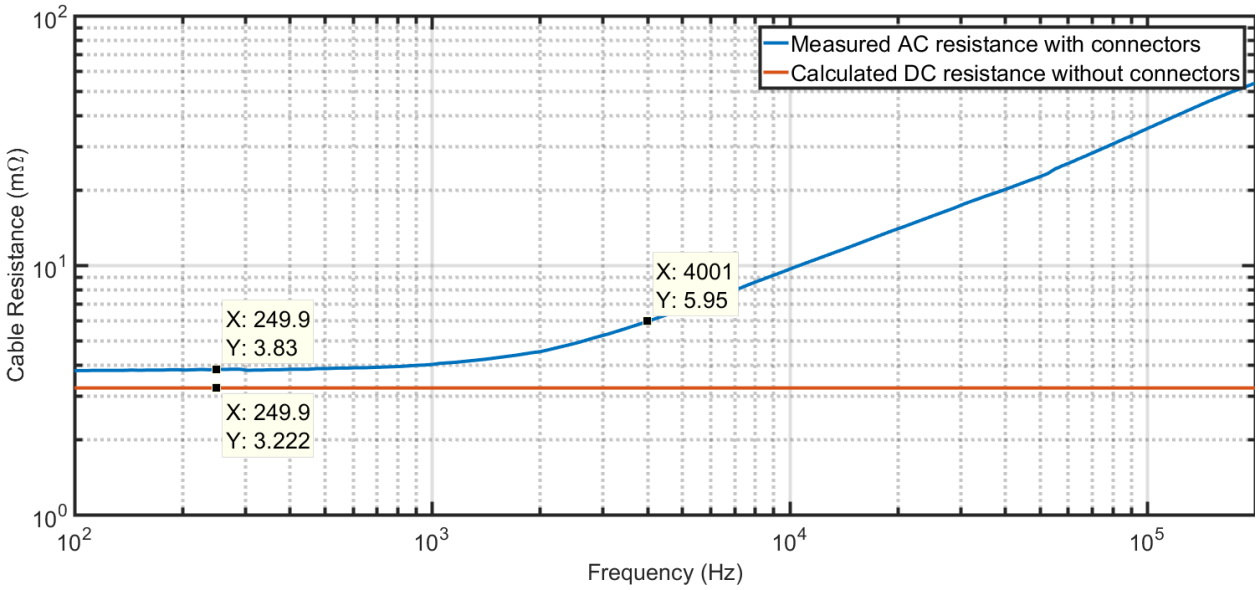


Figure 3.12: Measured and calculated cables resistance

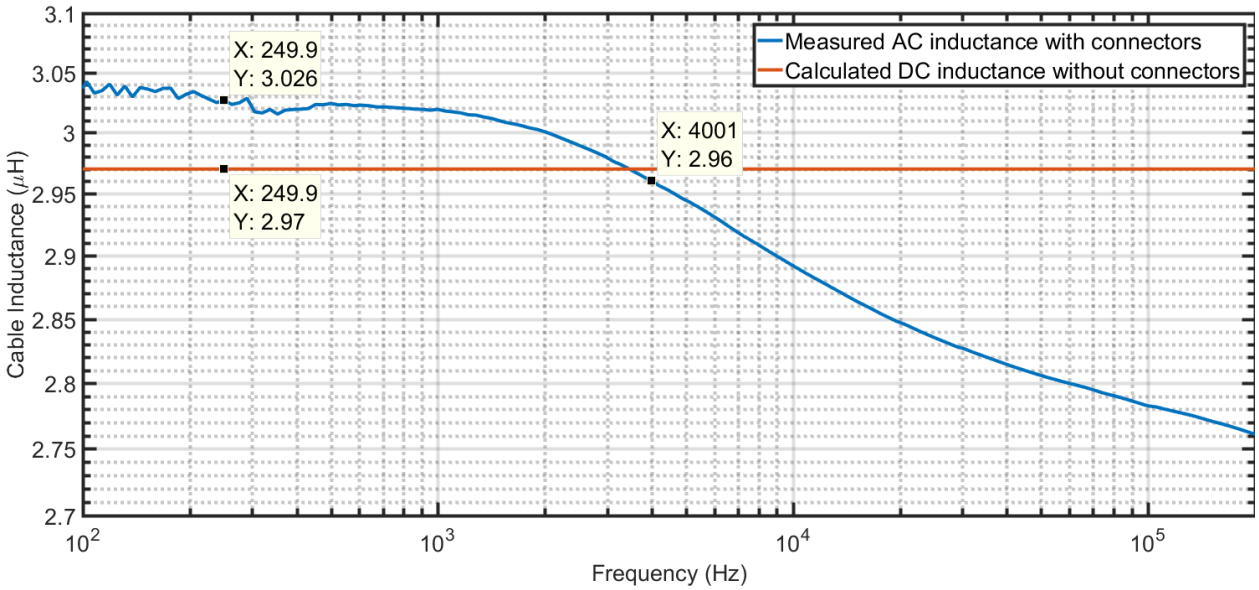
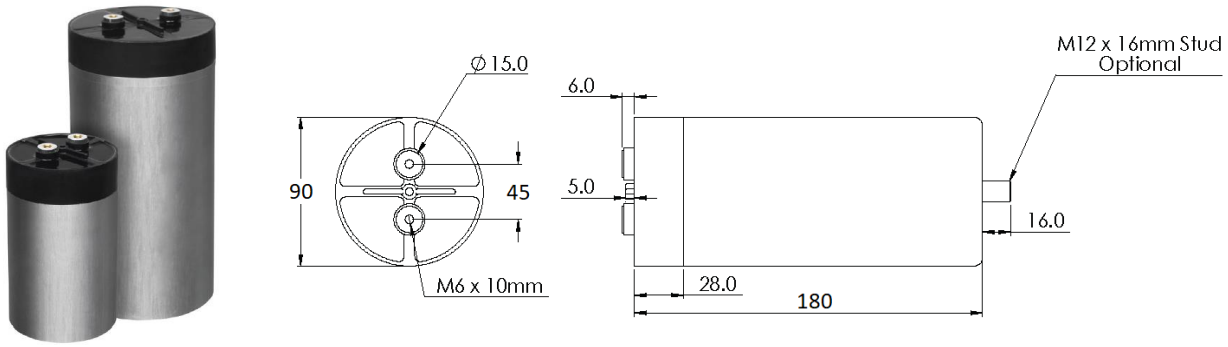


Figure 3.13: Measured and calculated cables inductance

The results show good matching between calculated and measured DC inductance values with an error of only 1.8%. A 16% error is present between calculated and measured DC resistances, expected to be due to the higher resistivity of the cables' material than that of pure annealed copper. Some of the discrepancies observed between measured and expected values can also be attributed to the impedance of the wire connectors, which was not accounted for in the calculations. AC resistance of the cables was found to be highly dependent upon frequency, approximately doubling in magnitude at 4kHz compared with DC. The AC inductance, on the other hand, was found to only slightly decreased with frequency (2% between DC and 4kHz).

3.2.3. DC-Link Capacitor

A 500μF metalized polypropylene film capacitor [6], shown in Figure 3.14, was selected for this experiment due to its high peak current capacity (10kA) and electrical parameters (C, ESL, ESR) stability over temperature and frequency [6].

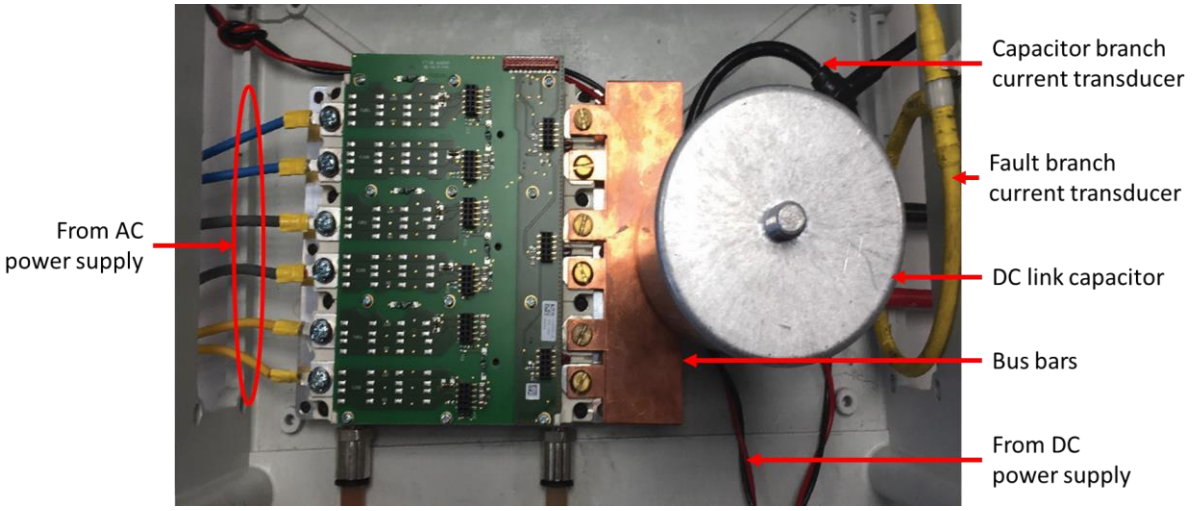


(a) (b)

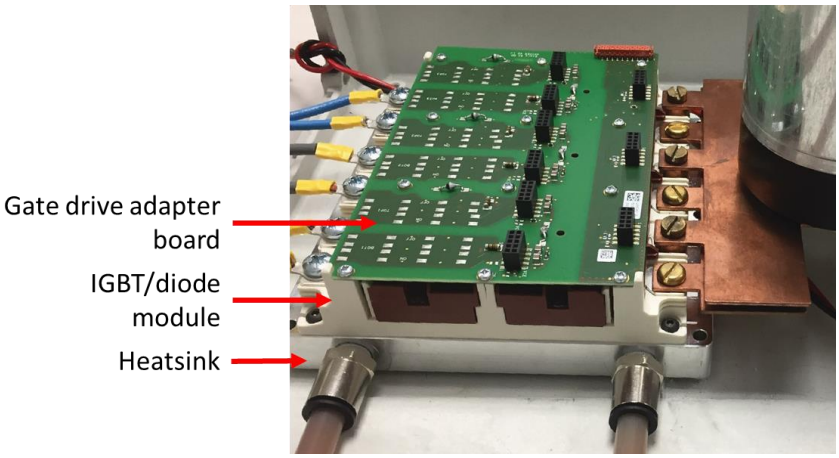
Figure 3.14: DC-link capacitor's package (a) picture, and (b) dimensions in mm [6]

3.2.4. Converter Module and Accessories

This section discusses components related to the converter module. This includes the IGBT/diode module, gate drive adapter board, heatsink, and busbars, as shown in Figure 3.15.



(a)

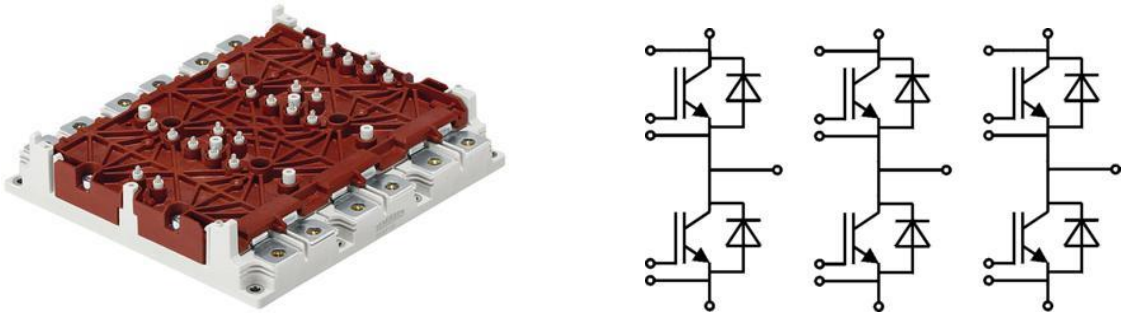


(b)

Figure 3.15: (a) Top and, (b) side pictures of converter module and attachments

A) IGBT/diode Module

The IGBT/diode module used in this experiment is the Semikron SKiM459GD12E4 [8], with the picture and internal connections shown in Figure 3.16. This is a 1200V rated module capable of handling a steady state current of 452A at a heatsink temperature of 70°C. Transiently, the diodes in this module are capable of handling up to 2.43kA of peak current for up to 10ms at a maximum junction temperature of 150°C. Since the diodes in this experiment were operated at initial temperatures of only 15°C, they are expected to handle significantly higher peak currents.



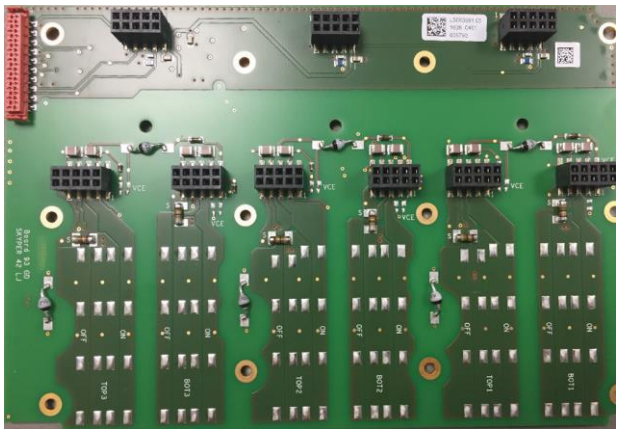
(a) (b)

Figure 3.16: Converter module (a) picture and (b) internal connections [8]

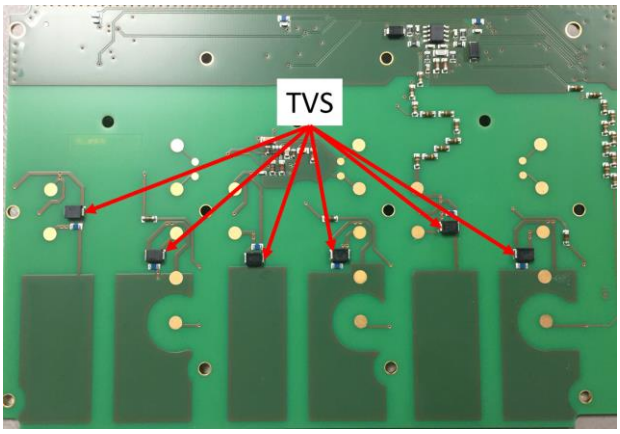
B) Gate Drive Adapter Board

A SKiM 93 gate driver adapter board [9], shown in Figure 3.17, was used to interface to the spring contacts on the converter module. The adapter board was modified to short circuit the gate and

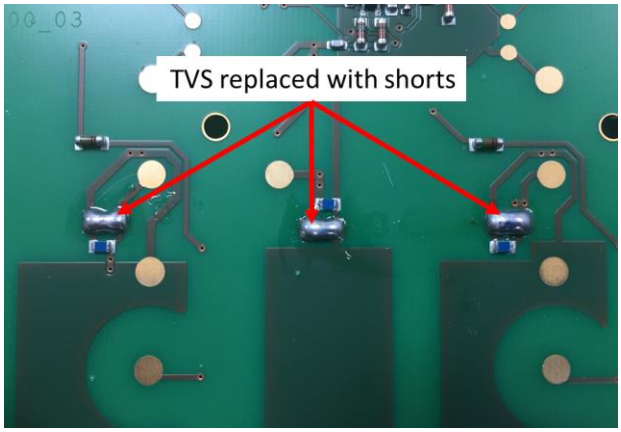
emitter contacts of each IGBT, as shown in Figure 3.17 (c) and Figure 3.18, to ensure the IGBTs are fully turned off during the experiment.



(a)



(b)



(c)

Figure 3.17: Picture of adapter board's (a) front side and (b) back side without modifications, and (c) back side after modifications (zoomed)

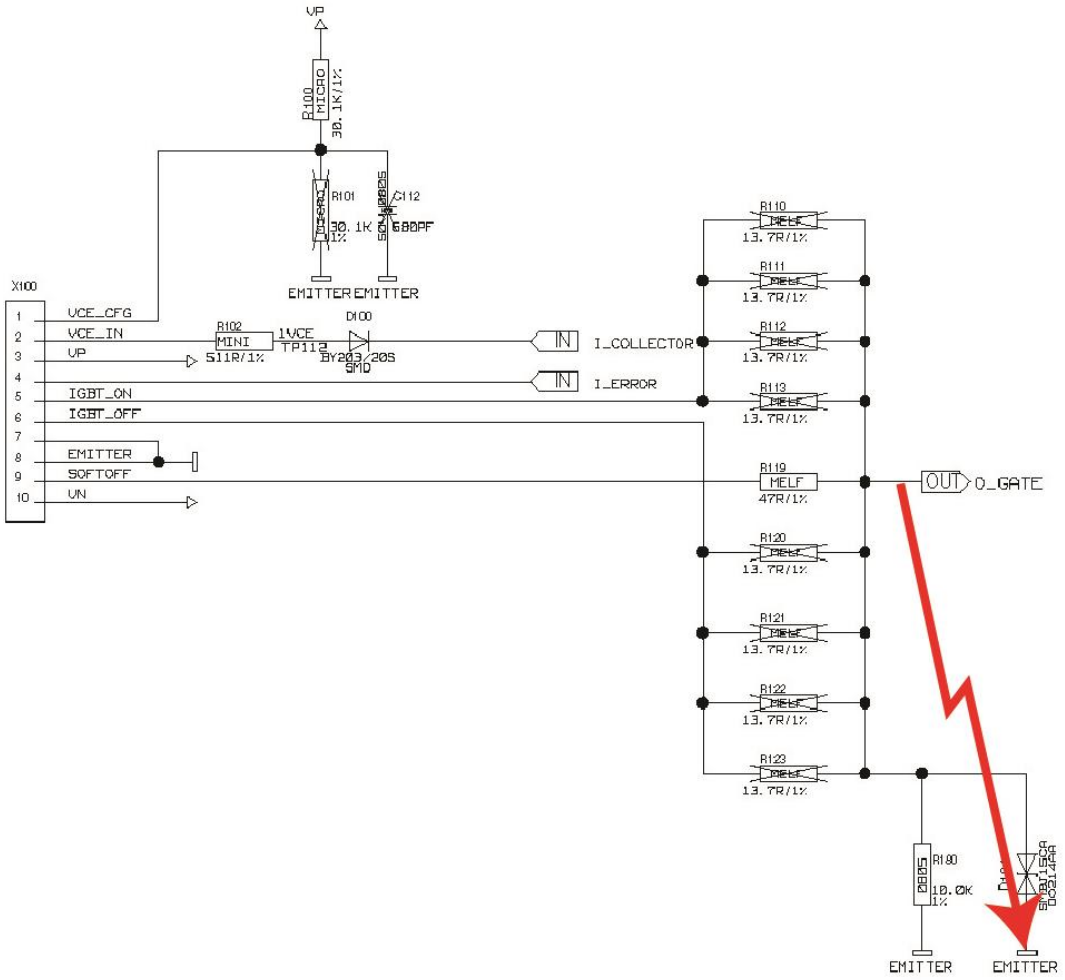
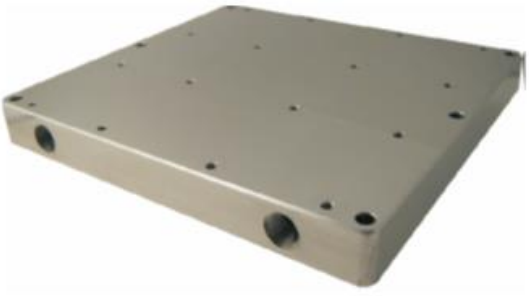


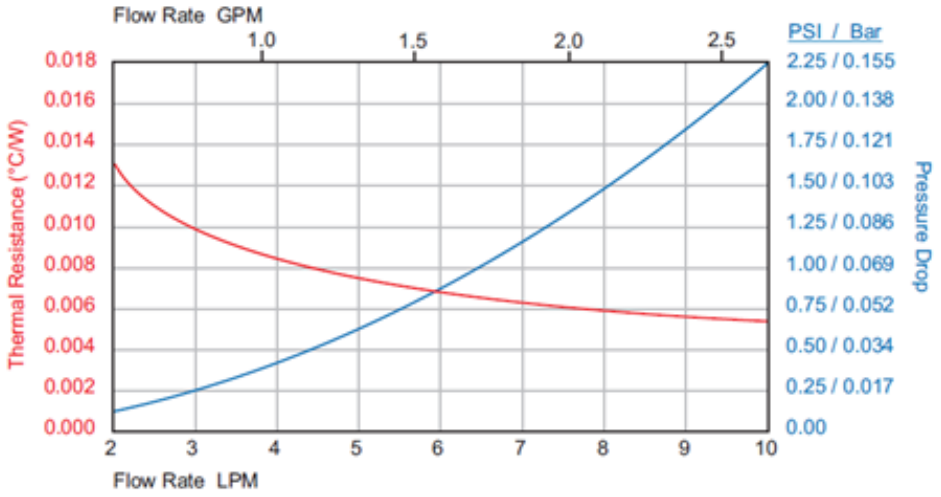
Figure 3.18: Location of shorts in adapter board's schematic [10]

C) Heat-Sink

A heatsink [11] was utilized to absorb the heat generated by the diodes. The picture and performance of used heatsink are shown in Figure 3.18. The inclusion of a heatsink is especially important for the SkiM module used in this experiment, since no baseplates are included in these modules. Lack of a baseplate improves the thermal performance of the module by decreases the thermal resistance between the semiconductor devices and module case. However, it also increases the module's sensitivity to short energy pulses [3] by decreasing the thermal mass.



(a)



(b)

Figure 3.19: Heatsink (a) picture, and (b) performance vs. flow rate [11]

A closed-loop water system was used to supply chilled water to the heatsink. The water temperature was measured using thermocouples at the terminals of the heatsink, shown in Figure 3.20, and found to be 9°C. The flow rate of the water was measured using the Dataflow Compact Flow Transmitter (DFC9000100), also shown in Figure 3.20, and found to be 11.1LPM.

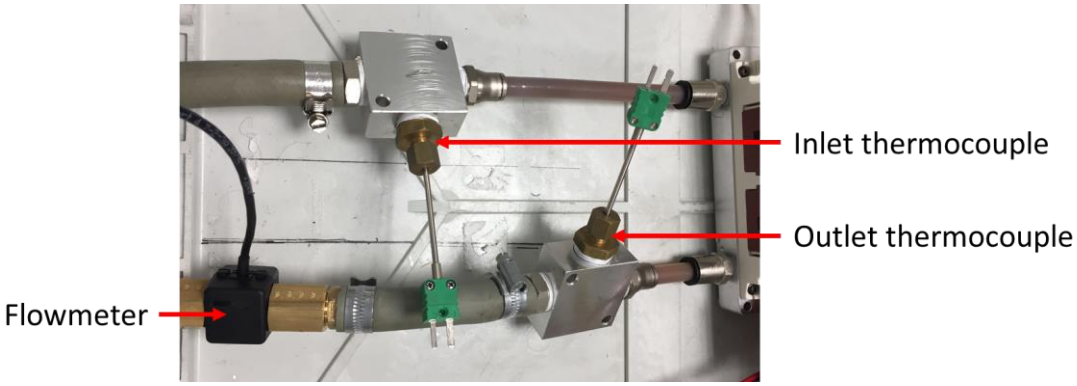
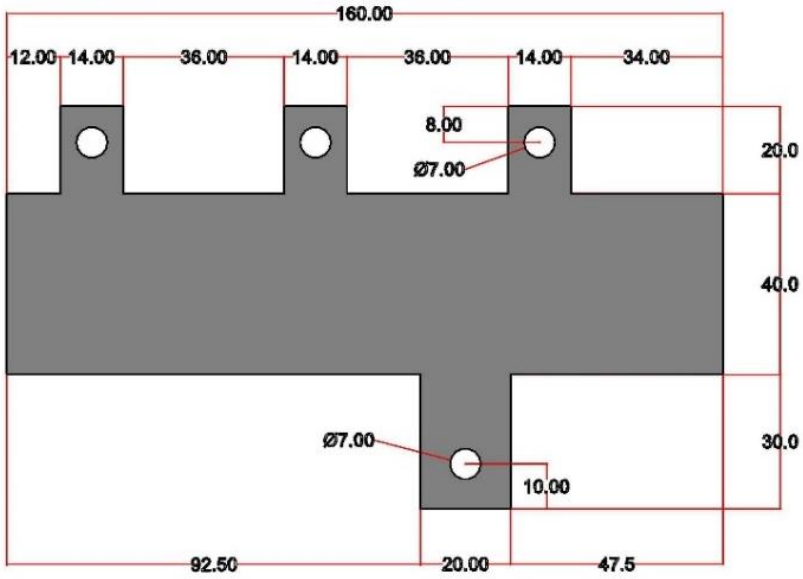


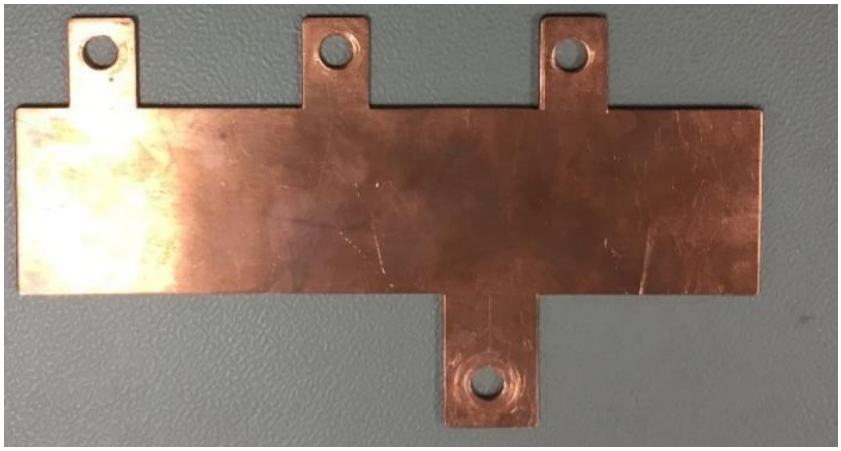
Figure 3.20: Picture of thermocouples and flowrate meter

D) Busbars

The busbars were designed and machined out of 3mm thick copper to establish the electrical connections between the converter module, DC link capacitor, and cables. The dimensions of the busbars are shown in Figure 3.21, along with a picture of the machined part. The busbar thickness was chosen based on available materials at the university workshop. The remaining dimensions were chosen so that the busbar can be connected directly to the terminals of power module and DC-link capacitor. No mechanical or electrical optimizations were performed on this design beyond a fit check.



(a)



(b)

Figure 3.21: Busbars (a) dimensions (in mm), and (b) picture of machined part

Finite-element software ANSYS Q3D Extractor was utilized to compute the frequency dependent inductance and resistance of the busbars. The geometry analysed is shown in Figure 3.22, where the positive and negative busbars are placed 3mm apart. The material for the solids was set to copper, with a resistivity of $1.72x10^{-8}$ohms. m and relative permeability of 0.999991.

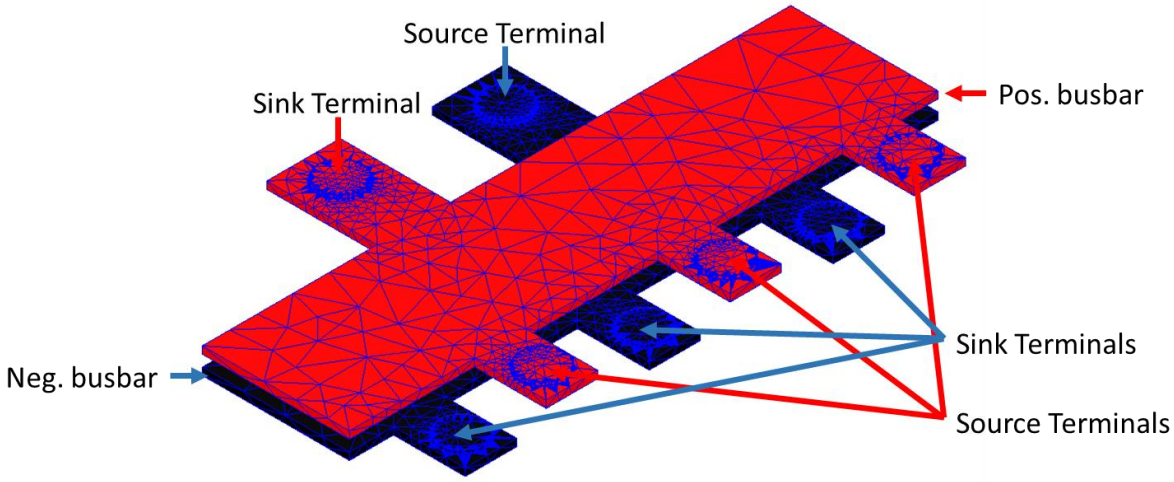


Figure 3.22: Isometric view of analyzed busbars geometry and mesh

The inductances and resistances obtained are plotted against frequency in Figure 3.23- Figure 2.27.

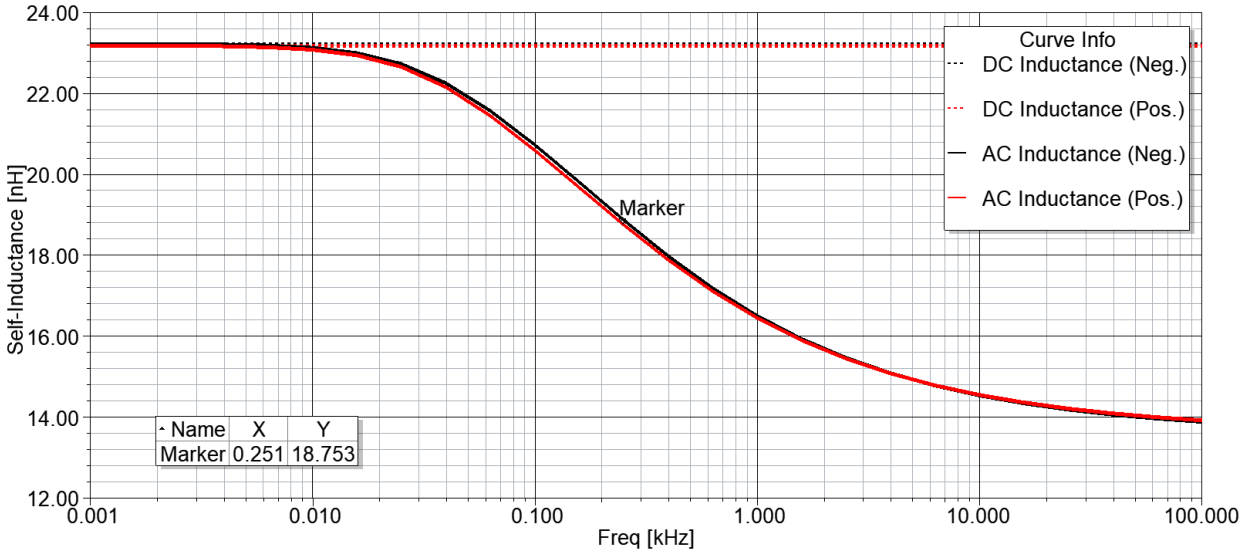


Figure 3.23: AC and DC self-inductances of positive (Pos.) and negative (Neg.) potential busbars vs. frequency

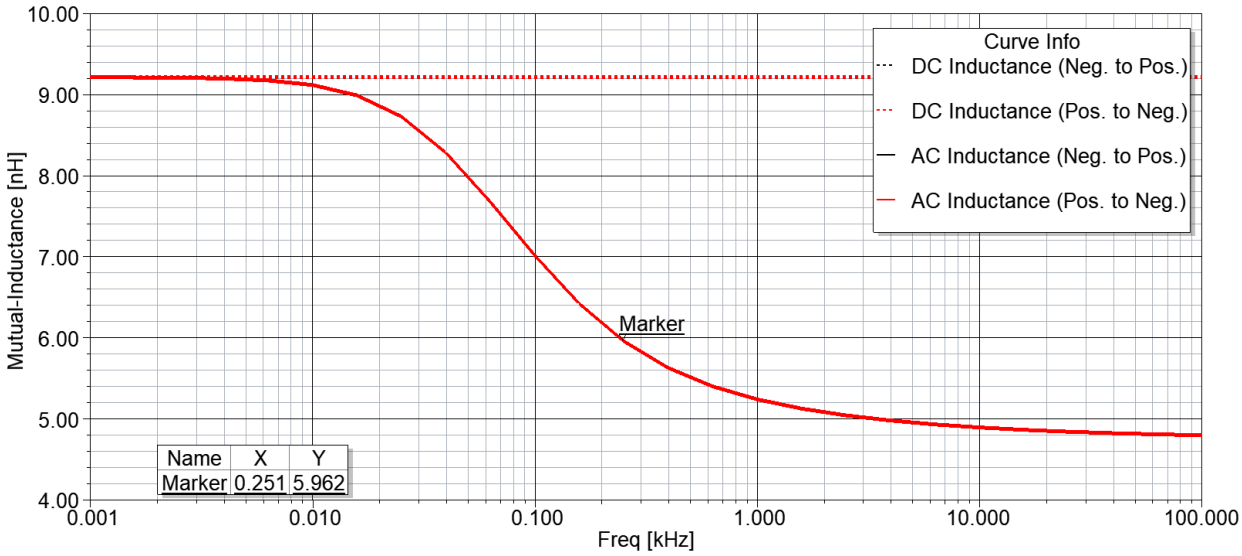


Figure 3.24: AC and DC mutual-inductances of positive (Pos.) and negative (Neg.) potential busbars vs. frequency

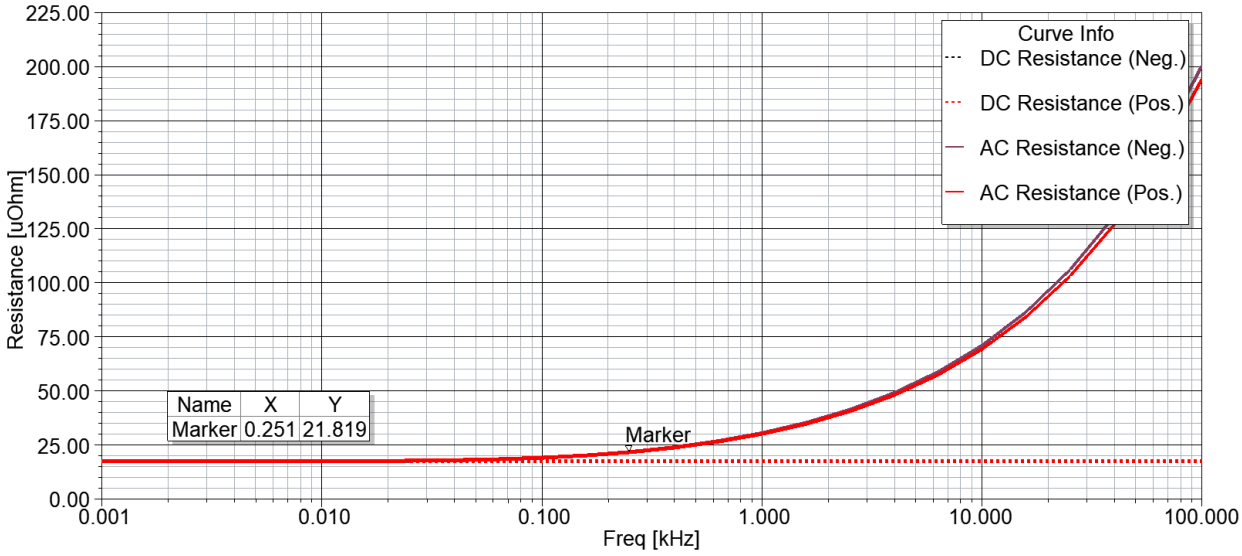


Figure 3.25: AC and DC resistance of positive (Pos.) and negative (Neg.) potential busbars vs. frequency

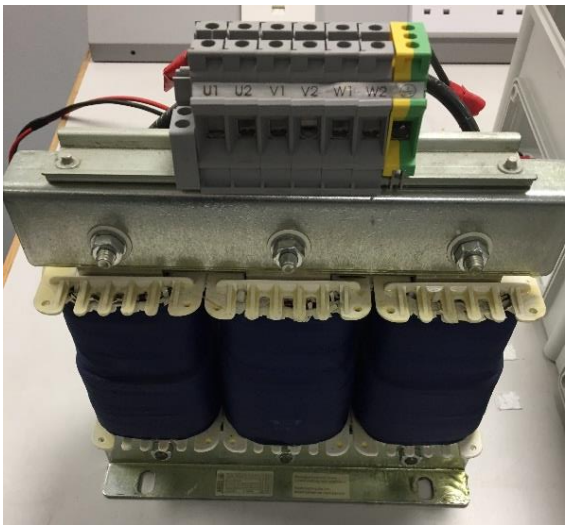
3.2.5. Three-Phase AC Power Supply

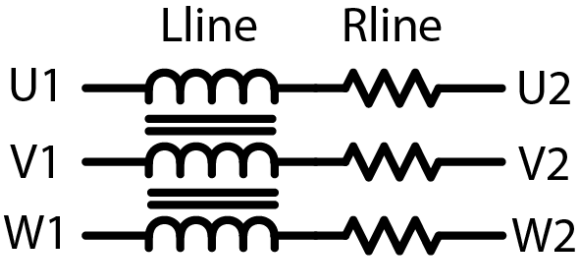
The California Instrument's 4500iL AC power source, shown in Figure 3.26, was used in this experiment to generate AC phase voltages. It is capable of sourcing up to 40A of maximum repetitive peak phase currents, with a voltage of up to 150V RMS line-to-neutral and frequency of 45Hz-5kHz [12].

Figure 3.26: Picture of AC power source [12]

3.2.6. AC Line Impedance

A three-phase AC choke [13], shown in Figure 3.27, was inserted between the AC source and converter to limit the AC supply's current within its capacity.





(a) (b)

Figure 3.27: AC choke's (a) picture, and (b) equivalent circuit

The line-to-line inductance and resistance of the choke was measured using the HIOKI IM3533-01 LCR Meter in the setup shown in Figure 3.28, as plotted in Figure 3.29 and Figure 3.30 respectively.

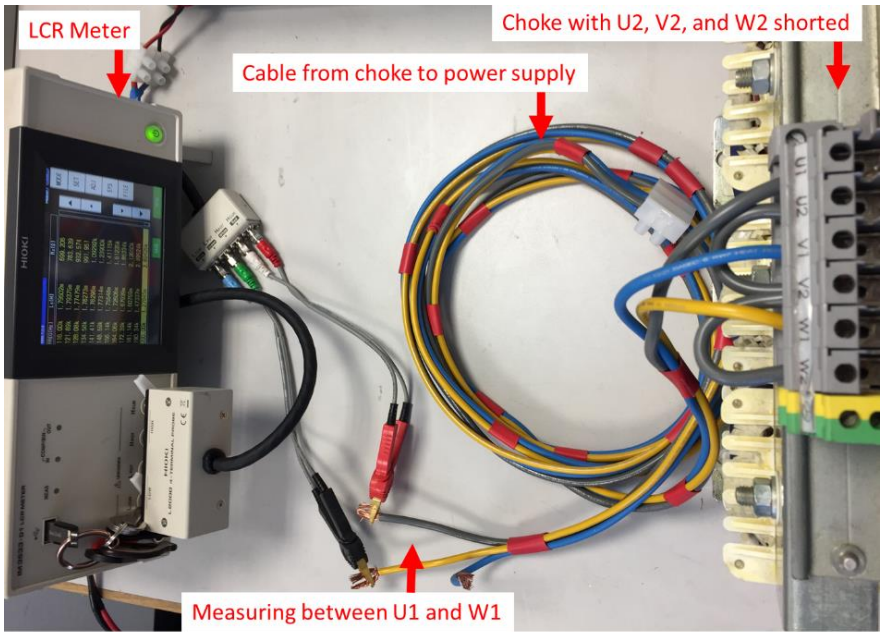


Figure 3.28: LCR meter measurement setup

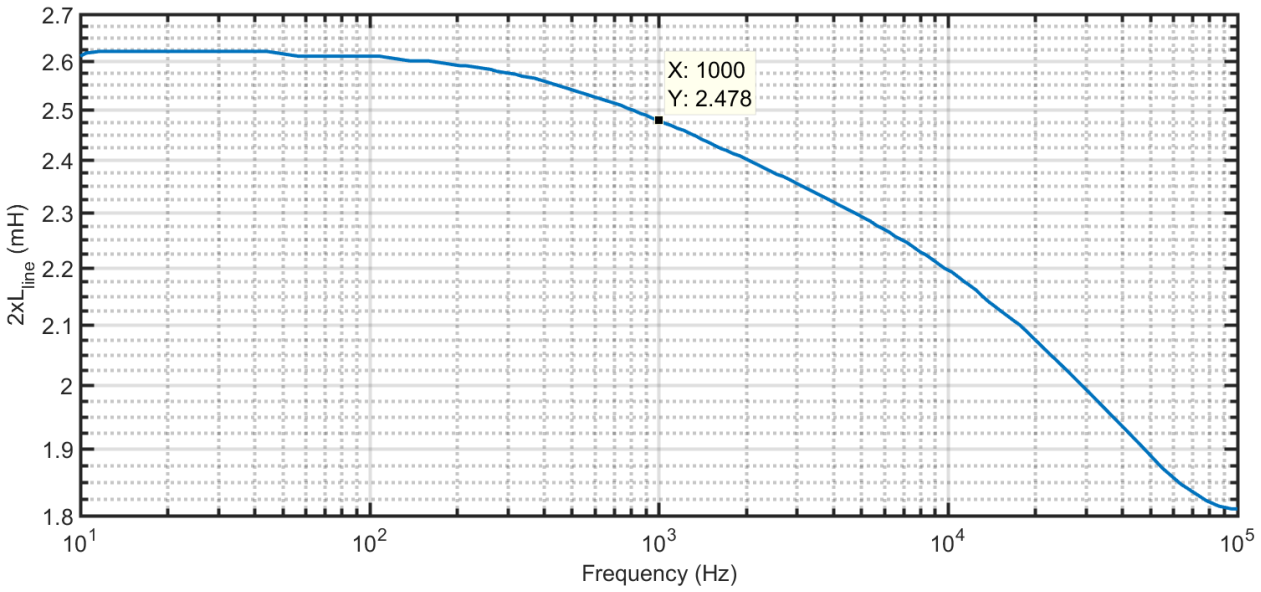


Figure 3.29: Line-to-line inductance vs. frequency

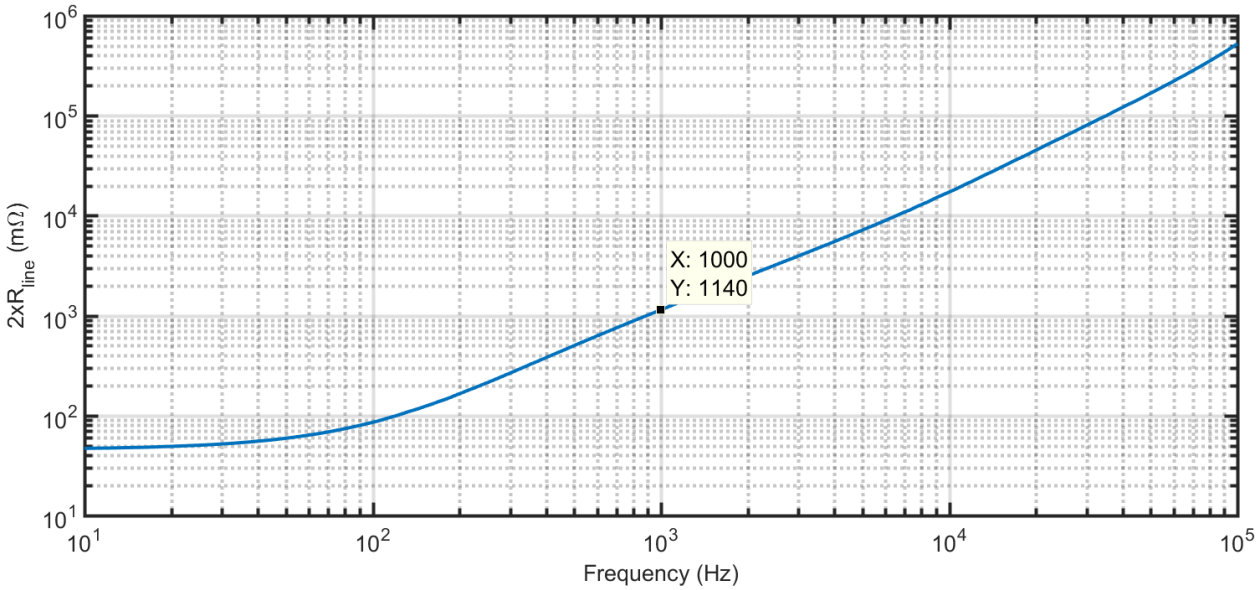


Figure 3.30: Line-to-line resistance vs frequency

3.2.7. DC Power Supply

The XANTREX XFR 600-4 DC power source, shown in Figure 3.31, was used to supply the DC capacitor's charging current, so that the initial DC link voltage can be set. It is capable of sourcing up to 4A of continuous current and up to 600V. A Double Pole Single Throw (DPST) switch was placed at the output of the supply, so that it can be isolated after the capacitor is fully charged, as well as a 1kΩ series resistor to limited the charging current's magnitude.

Figure 3.31: Picture of DC power supply's front panel

3.3. Experiment Results

This section presents experimental results obtained using the setup described in the previous sections, which are compared with those expected from the analyses carried out in Chapter 2. Three experiments were performed to validate the DC side, AC side, and combined contributions, as presented in sections 3.3.1-3.3.3 respectively.

3.3.1. DC Side Contributions

An overview of the setup used in this part of the experiment is shown in Figure 3.32, where AC side components are disconnected. The DC power supply is used to charge the DC link up to 270V, while the thyristor is in the OFF state. After the capacitor is fully charged, the supply is disconnected by opening the DPST switch, and the thyristor is then triggered. Currents are measured at the fault and capacitor branches using the Power Electronics Measurement's CWT300 and CWT15 Rogowski coil based current transducers. These transducers are ideal for pulsed currents measurements, adding minimum inductance to the monitored path, and maintaining wide current ranges of up to 60kA and 3kA for the CWT 300 and CWT15 models respectively [14].

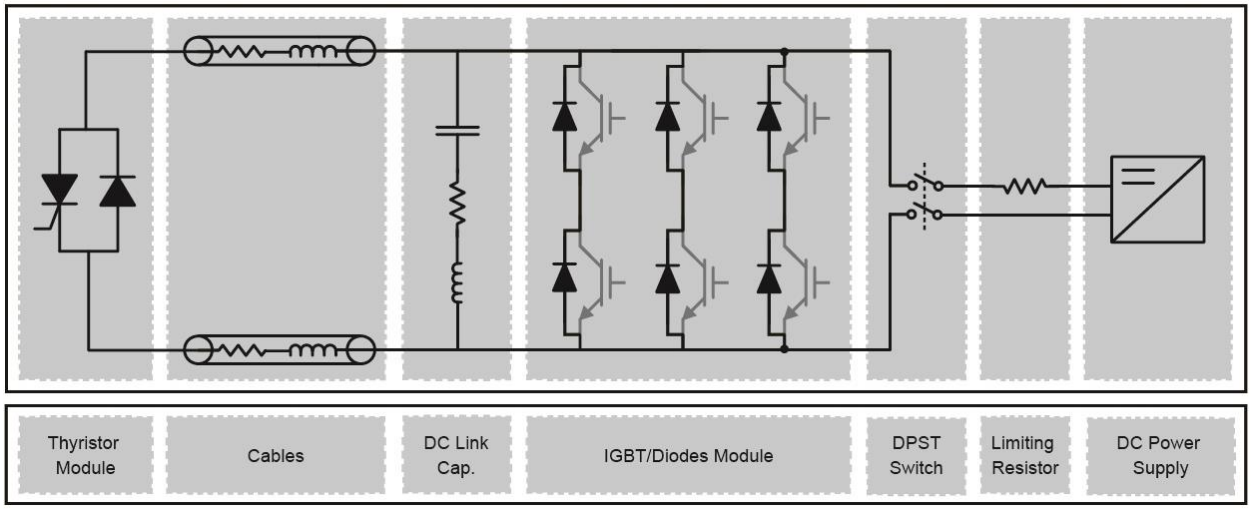


Figure 3.32: Overview of DC side contributions experimental setup

A) Fault Branch's Current

Analytical expressions for the fault branch's current during the diodes blocking stage were derived in section 2.2.1. Those equations were modified to account for the thyristor's forward voltage (V_F) and resistance (R_F), as highlighted in bold:

$$\beta = \frac{ESR + R_{short} + \boldsymbol{R_F}}{2\,(ESL + L_{short})} \tag{3.1}$$

$$i_{DB}(t) = e^{-\beta t}\left(I_o\, cos\, \omega_r t + \frac{Vo - \boldsymbol{V_F}}{\omega_r (ESL + L_{short})}\, sin\, \omega_r t\right) \tag{3.2}$$

To account for the dependency of cable parameters on frequency, the ringing frequency (ω_r) was first evaluated using LCR meter measurements taken at DC frequency, and found to be 4.09kHz. Cable resistance and inductance were then re-evaluated from LCR meter measurements at 4.09kHz, and found to be approximately 5.95mΩ and 2.96μH respectively, as shown in Figure 3.12 and Figure 3.13 respectively. The ringing frequency was then recalculated to be 4.08kHz. Subsequent iterations can be made. However, minimal changes of impedance and frequency are expected. The analytical expression for the fault branch's current during diodes conducting stage derived in section 2.2.2 were also modified to account for the thyristor's effect, as highlighted in bold:

$$i_{FB}(t) = \frac{-2V_j - \boldsymbol{V_F}}{(2/3)\,R_s + R_{short}}\left(1 - e^{-t\,\frac{(2/3)\,R_s + R_{short} + \boldsymbol{R_F}}{L_{short}}}\right) + I_1\, e^{-t\,\frac{(2/3)\,R_s + R_{short} + \boldsymbol{R_F}}{L_{short}}} \tag{3.3}$$

Fault branch's current in this stage was found to be at much lower frequency than in the diodes blocking stage. Therefore, low frequency cable impedances and thyristor parameters were used. The frequency of the current response was approximated to be 250Hz, by regarding the response as a quarter of a sine wave. Measured fault currents are compared to those obtained analytically as shown in Figure 3.33. The equivalent circuits and parameters used in these comparisons are shown in Figure 3.34 for the diodes blocking and conduction stages.

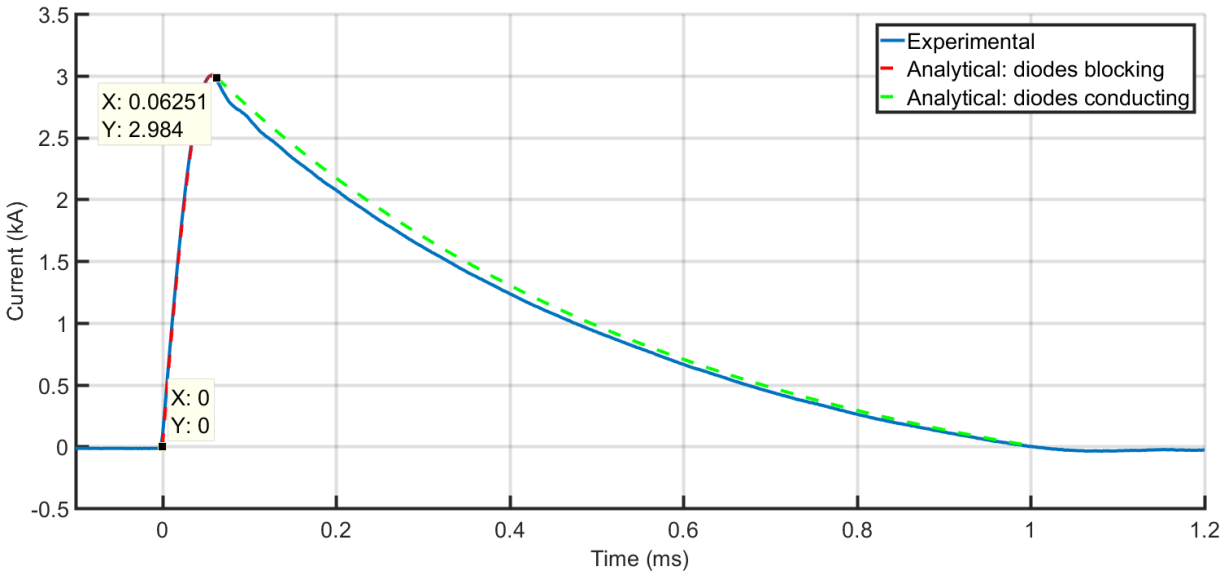
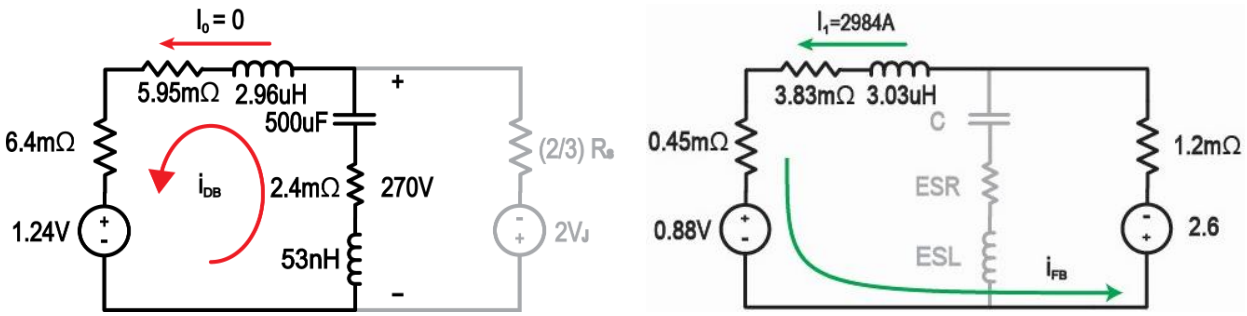


Figure 3.33: Comparison of experimentally and analytically obtained fault branch's currents



(a) (b)

Figure 3.34: Equivalent circuits during (a) diodes blocking, and (b) diodes conduction stages

Comparisons shown in Figure 3.33 demonstrate excellent matching (within 5%) between experimental and analytical results. However, some deviation during the diodes condition stage was observed. This error was further investigated in simulation and found to be due to the module side inductance. This error was investigated in simulation due to the ease of setting up the schematic and comparing simulation results. It should also be noted that the analytical expressions for fault branch current were not modified to account for module side inductance as that would add significant unnecessary complexity. The inductance consists of the module's internal inductance (typically 10nH for this module [8]) and that of the busbars. The inductance of the busbars was analysed in section 3.2.4 D), giving a loop inductance of 25.6nH *(2(18.75-5.96))* at 250Hz, where 18.75nH is the self-inductance of each section of the busbar and 5.96nH is the mutual inductance between the two sections, as shown in Figure 3.23 and Figure 3.24 respectively. These inductances result in coupling between fault and capacitor branch currents resulting in this mismatch. Two circuits, with and without module side inductances were simulated in SPICE as shown in Figure 3.35. Fault current is the two circuits are compared in Figure 3.36, validating this finding.

Diode Model

.model CustomDiode D (IS=1n RS=1.74m N=2.0)

Capacitor Branch Parameters

.param ESL = 53n
.param ESR = 2.4m
.param C = 500u

Output Initial Conditions (b)

.ic I(L1) = {I0}
.ic V(V0) = {Vo}
.param I0=0.0
.param Vo=270

Short Circuit Path Parameters

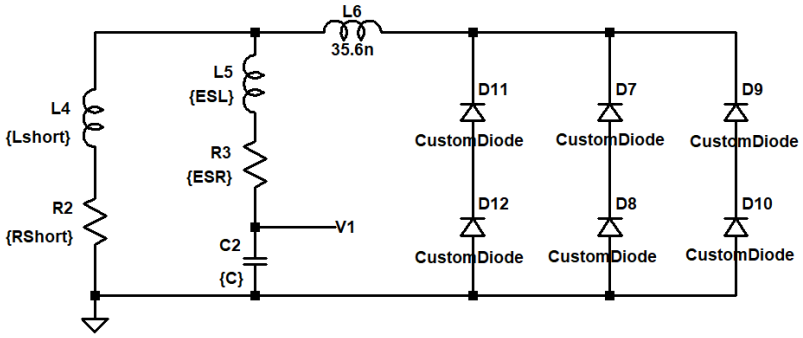
.param Lshort = 3u
.param RShort = 3.9m

Transient Command

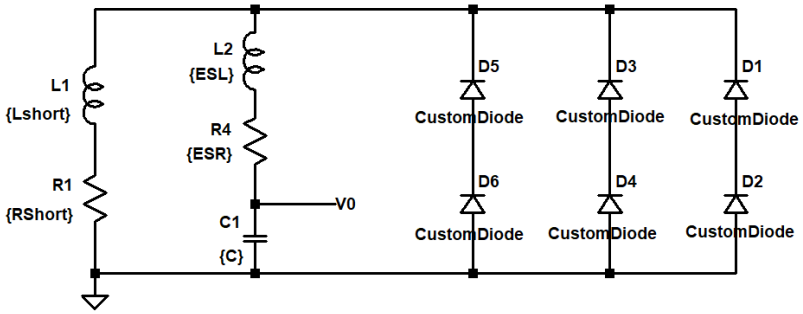
.tran 0 0.0012 0 0.000000001

Output Initial Conditions (a)

.ic I(L4) = {I0}
.ic V(V1) = {Vo}



(a)



(b)

Figure 3.35: Simulation circuits (a) including and (b) disregarding module side inductances

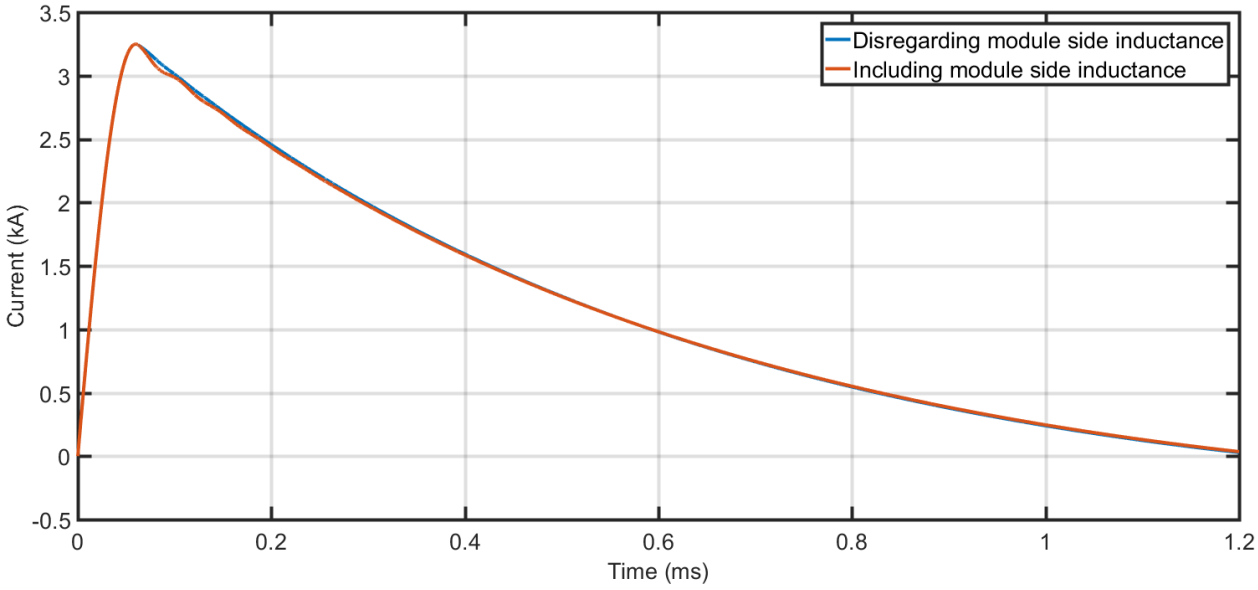


Figure 3.36: Simulation results comparing fault branch's currents including and disregarding module side inductances

B) Capacitor Branch's Current

Capacitor branch's current during the diodes blocking stage is equal to the fault branch's, and was therefore also calculated from (3.2) to account for the thyristor's voltage drop and resistance. On the other hand, capacitor branch's current during the diodes conduction stage does not flow through the thyristor, and was therefore calculated from the same expressions previously derived in section 2.2.2. Experimental capacitor branch's current is compared to that obtained analytically as shown in Figure 3.37. The equivalent circuits and parameters used for these comparisons are shown in Figure 3.38 (a) and (b) for the diodes conduction and blocking stages respectively. It was found that experimental results match expected very well, especially when including a 10nH module side inductance, as shown in Figure 3.38 (c).

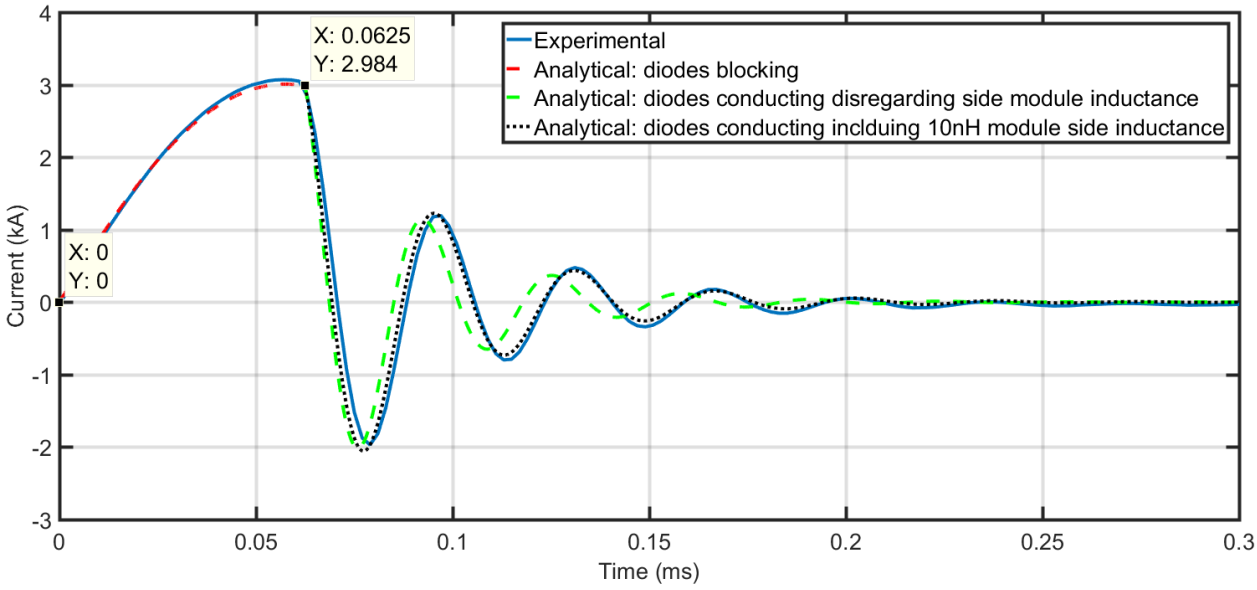
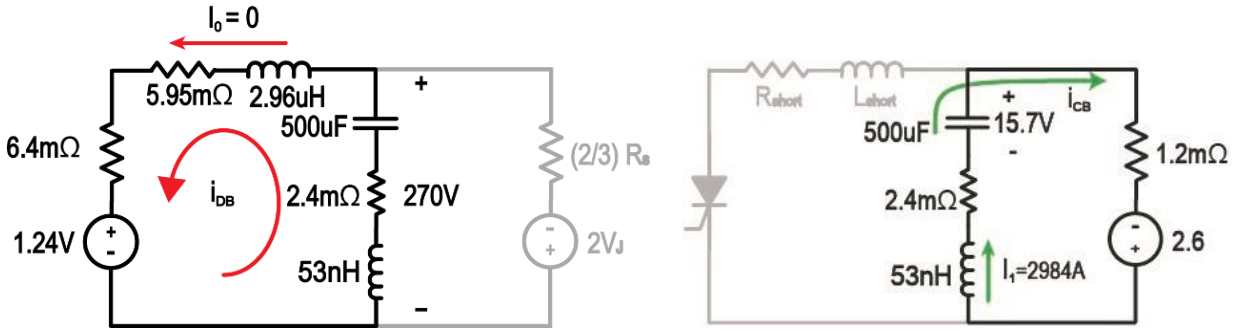
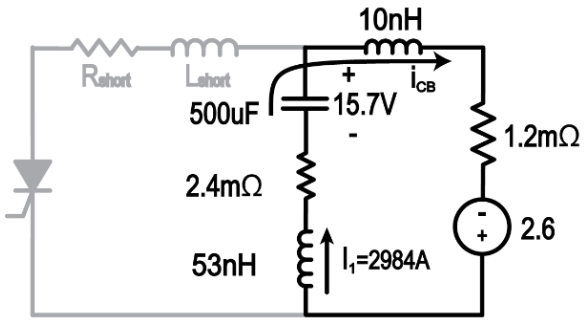


Figure 3.37: Comparison of experimentally and analytically obtained capacitor currents



(a) (b)

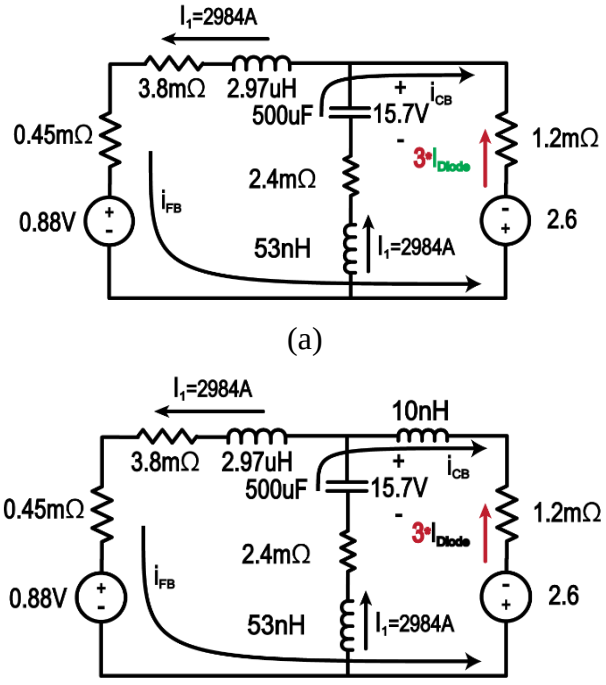


(c)

Figure 3.38: Equivalent circuits during (a) diodes blocking, and (b) diodes conduction stages disregarding, and (c) including 10nH module side inductance

C) Diodes Branch Current

Diodes currents are taken as the difference between capacitor and fault branch currents divided among the three converter legs, as shown in the equivalent circuit of Figure 3.39. Measured diodes currents from taking the difference between capacitor and fault branch measurements are compared to those obtained analytically, as shown in Figure 3.40, and demonstrate excellent matching (within 5%), especially when including the effect of module side inductance.



(a)

(b)

Figure 3.39: Equivalent circuit during diodes conduction stages (a) disregarding and (b) including module side inductance

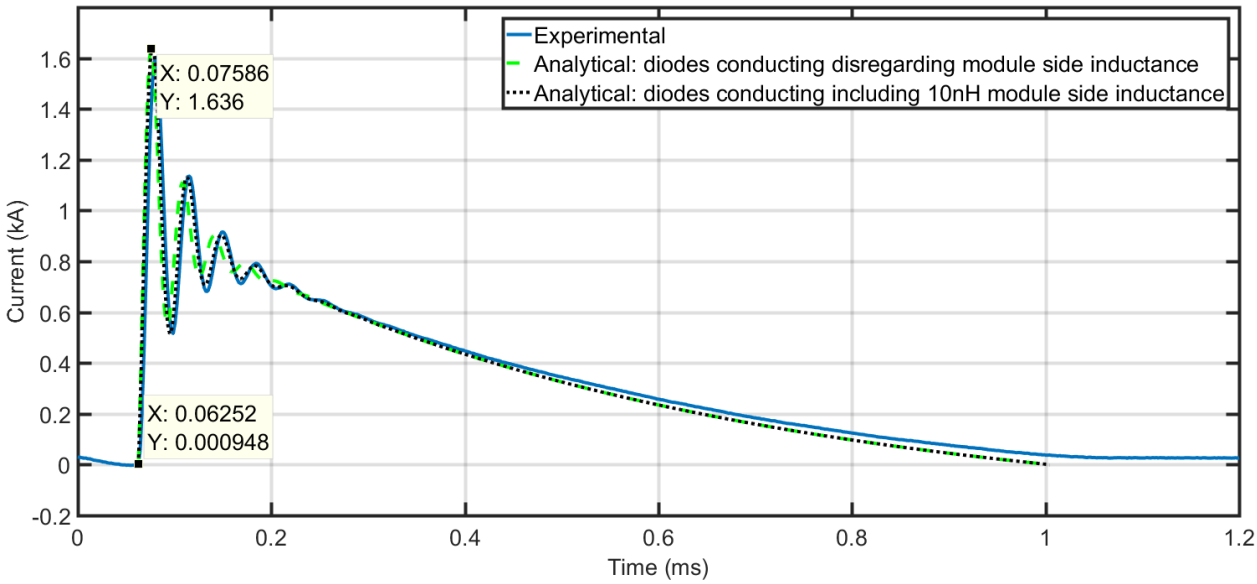


Figure 3.40: Comparison of experimentally and analytically obtained diodes currents

3.3.2. AC Side Contributions

An overview of the setup used for this part of the experiment is shown in Figure 3.41, where the AC power supply is connected to one side of the AC choke while the other side is short-circuited. A computer with MATLAB Instrument Control Toolbox was used to setup and trigger the power supply to generate a phase voltage pulse. The voltage transient was setup to last 9 electrical cycles in duration at a frequency of 1kHz, and have the maximum amplitude achievable by the supply (150VRMS). The script used for this setup is provided in Appendix A. Phase current and line-to-natural voltage of *Phase A* are measured using two Agilent 10073C voltage probes, and an Agilent N2783A current transducer respectively.

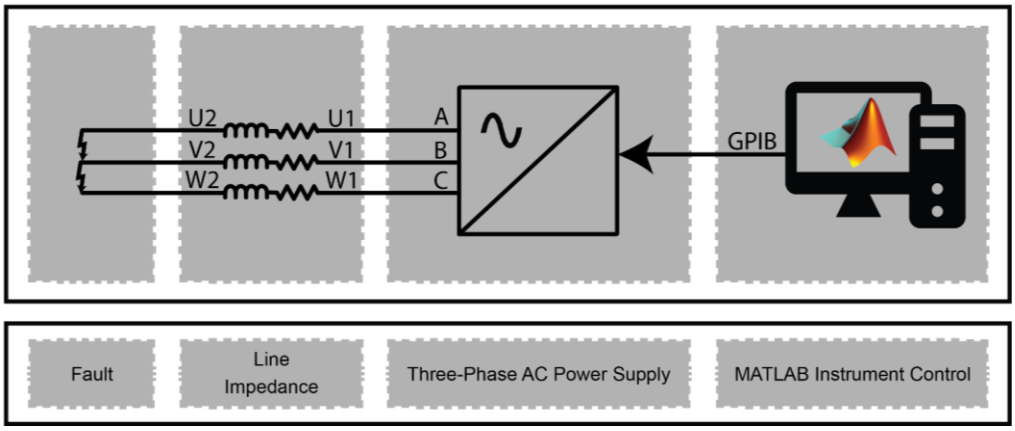


Figure 3.41: Overview of AC side contributions experimental setup

Distortion in phase voltage waveforms was observed, which was most significant during the first cycle of the transient and when high power is demanded. To overcome this issue, measured and expected results were compared at the end of the first cycle, as shown in Figure 3.42. When high transient currents are demanded from the supply by increasing the voltage commanded beyond 170V peak (120.2VRMS) or decreasing the frequency below 1kHz, the voltage waveform became significantly distorted by a third harmonic component, as shown in Figure 3.43. Working within the capabilities of the power supply, measured *phase a* current and voltage were compared to those analytically calculated as shown in Figure 3.44. The equivalent circuit used in this comparison is shown in Figure 3.45, where line inductance and resistance are found from the AC choke's LCR meter measurements at 1kHz of frequency shown in Figure 3.29 and Figure 3.30.

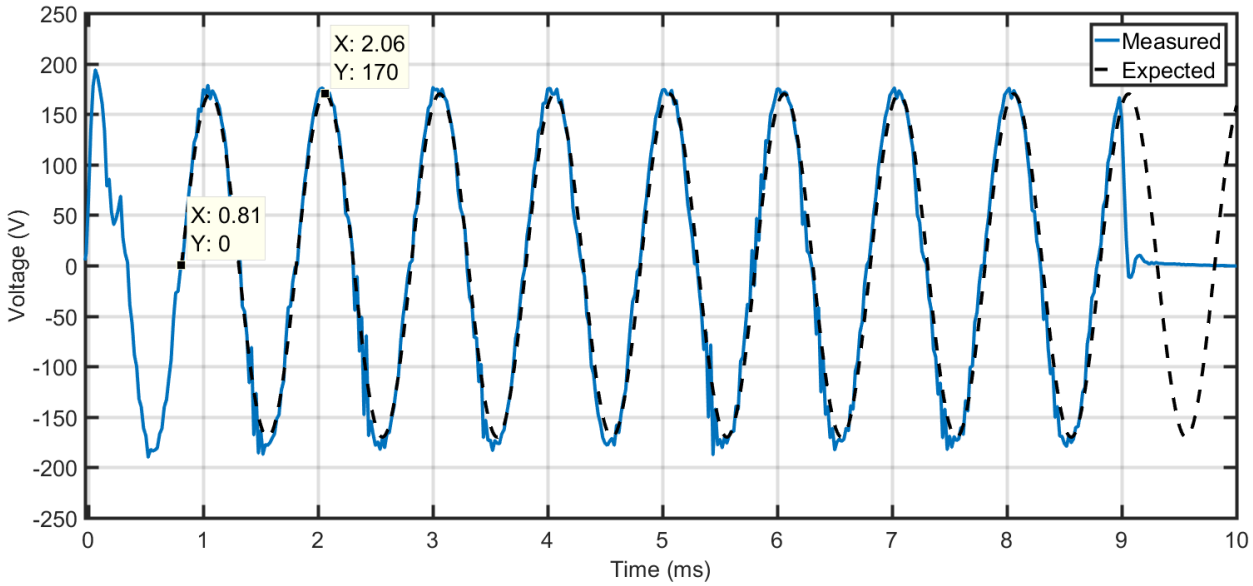


Figure 3.42: Measured and expected *Phase A* voltages when 170V peak is commanded

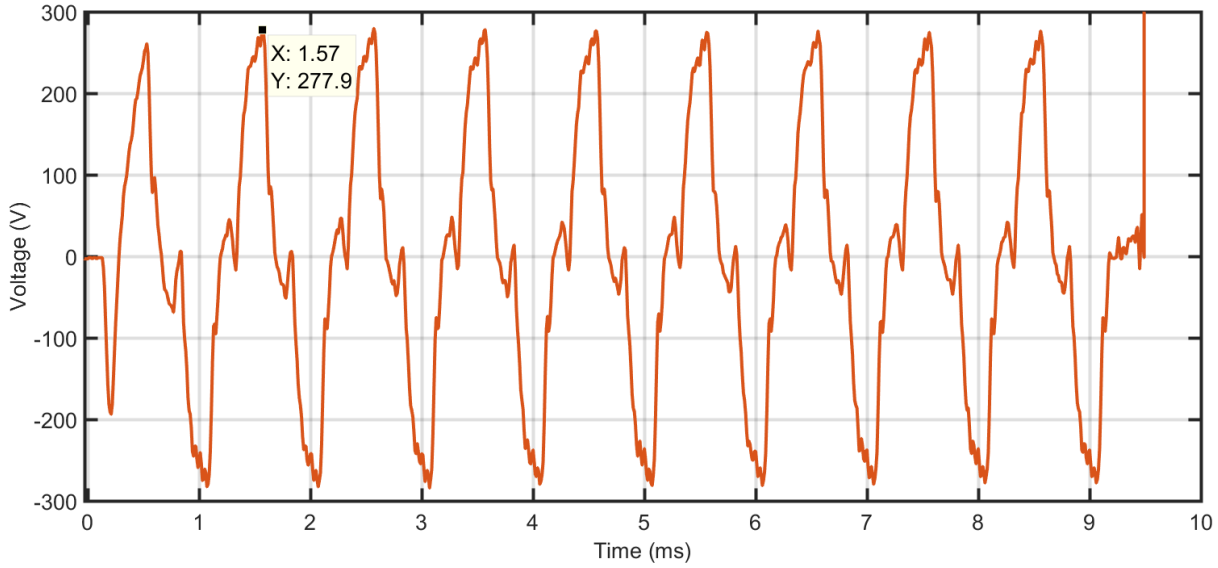


Figure 3.43: Measured *phase a* voltage when 150VRMS is commanded

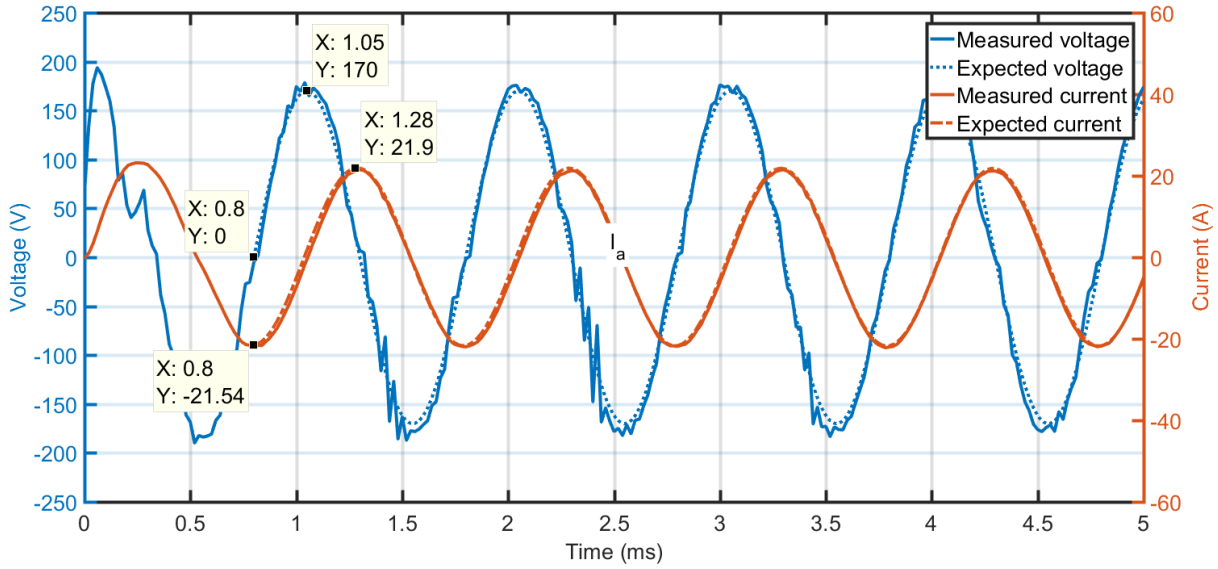


Figure 3.44: Comparison of measured and expected *Phase A* voltage and current

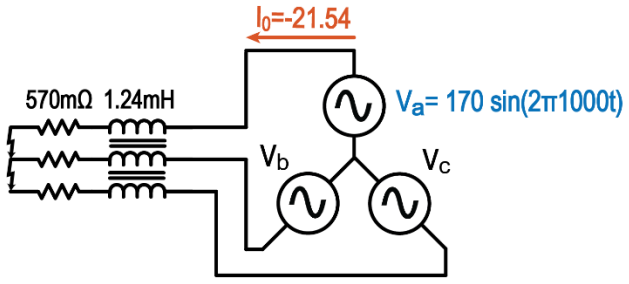


Figure 3.45: Equivalent circuit of AC side contributions

3.3.3. Combined Response

The setup shown in Figure 3.46 was used to experimentally validate the converter's combined response. The DC power supply charges the DC link up to 540 volts, and is then isolated using a DPST switch. Since the fault switch is initially OFF, the capacitor maintains its voltage while the DC supply is disconnected. The AC power supply is then triggered to generate an AC side voltage. Since the line-to-line peak of that voltage is below the DC side voltage, no phase currents initially flow. After a few cycles of the phase voltage, the fault switch is triggered and both AC and DC side contributions start flowing through the converter. The delay between the start of the AC side transient and thyristor triggering is controlled using the pulse generator to avoid the initially noisy phase voltage and control the phase angle at which the fault occurs (α). Measured *Phase A* voltage and current, as well as fault branch's current are shown in Figure 3.47 for an initial DC side voltage of 540V, and time at which fault occurs corresponding to a *phase a* angle (α) of 18°.

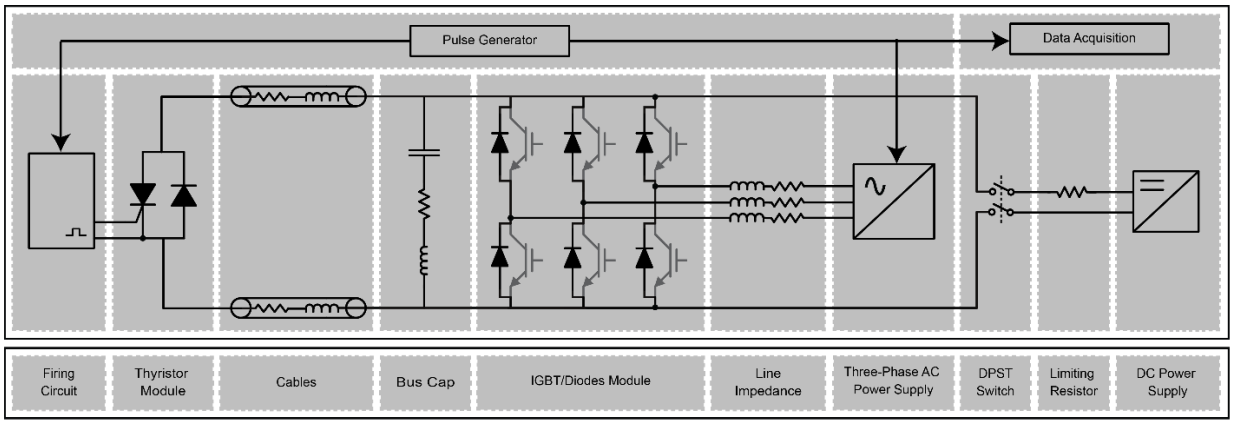


Figure 3.46: Combined response experiment setup

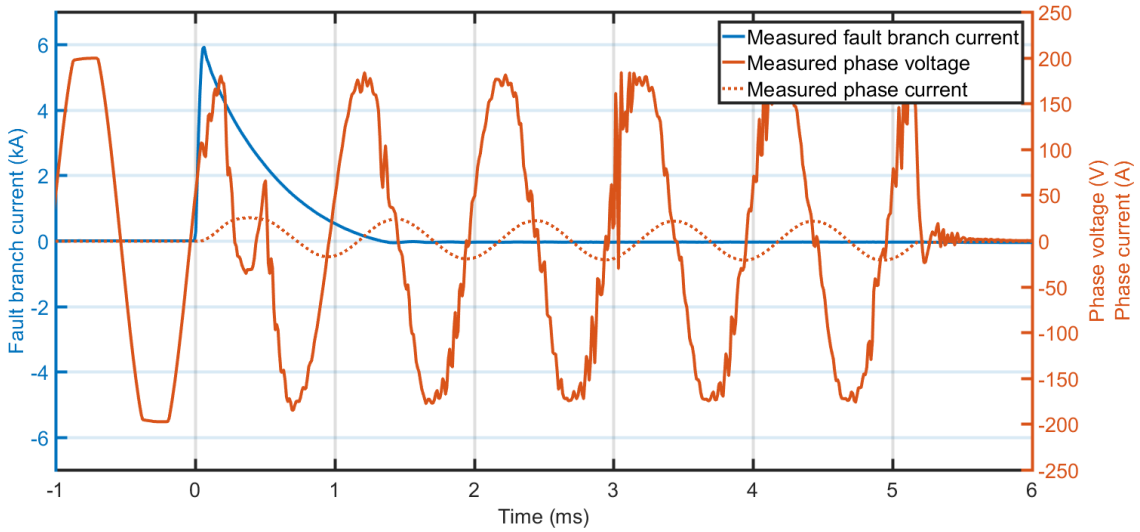


Figure 3.47: Measured AC and DC side contributions with initial DC link voltage of 540V and α of 18°

Measured phase current shown in Figure 3.47, is compared to that calculated from (2.77) in Figure 3.48. The equivalent circuit and components' values used for this comparison are shown in Figure 3.49. For t<0, the voltage waveform is clipped as the magnitude exceeds the maximum limit of the voltage probe used to measure the signal (±200V). For t>0, the distortion is likely caused by the inability of the power supply to regulate the output. To work around the limitations of the power supply, the analytical results were compared to measurements after the distortion period (at *t=2.783ms*). The comparison then demonstrates excellent matching (within 5%) between measured and derived (expected) results.

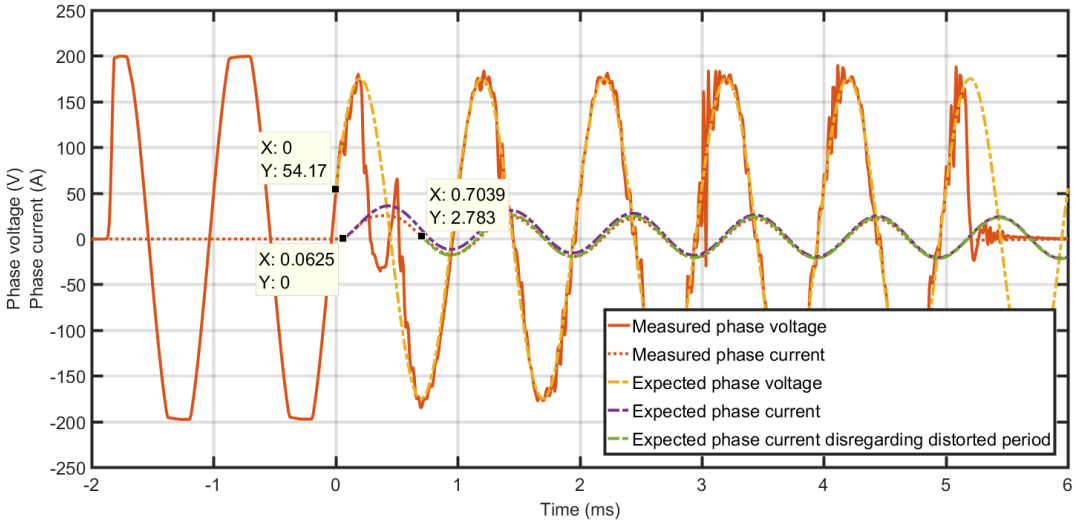
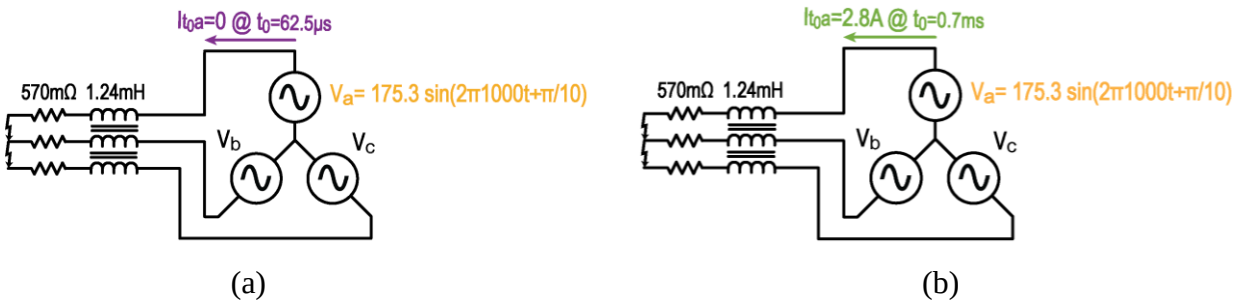


Figure 3.48: Comparison of measured and expected AC side contributions with α of 18°



(a) (b)

Figure 3.49:Equivalent circuit and used parameters (a) accounting for, and (b) disregarding voltage distortion period

Measured DC side contribution shown in Figure 3.47, are compared to expected in Figure 3.50. The equivalent circuit and components values used for this comparison are shown in Figure 3.51.

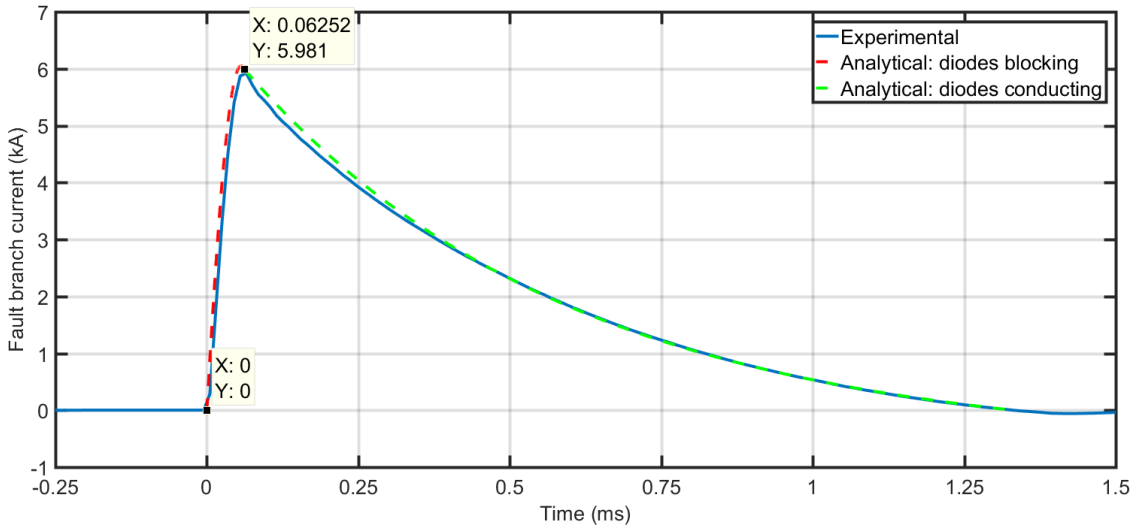
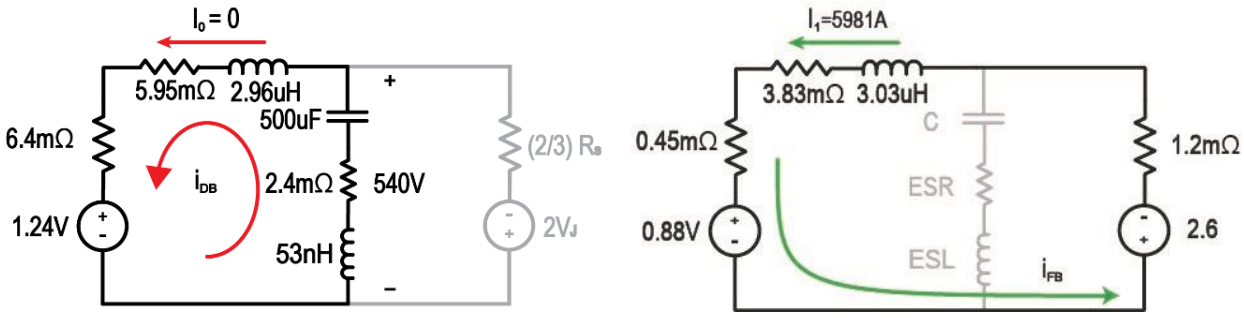


Figure 3.50: Comparison of measured and expected fault branch's current with α of 18°



(a) (b)

Figure 3.51: Equivalent DC side contribution circuits during (a) diodes blocking, and (b) diodes conduction stages

Measurements were also taken for an (α) angle of 110° by changing the delay time of the pulse generator, while maintaining the initial DC link voltage at 540V, as shown in Figure 3.52. The AC and DC side contributions under this condition are compared to expected in Figure 3.53 and Figure 3.54 respectively, and show excellent matching (within 5%).

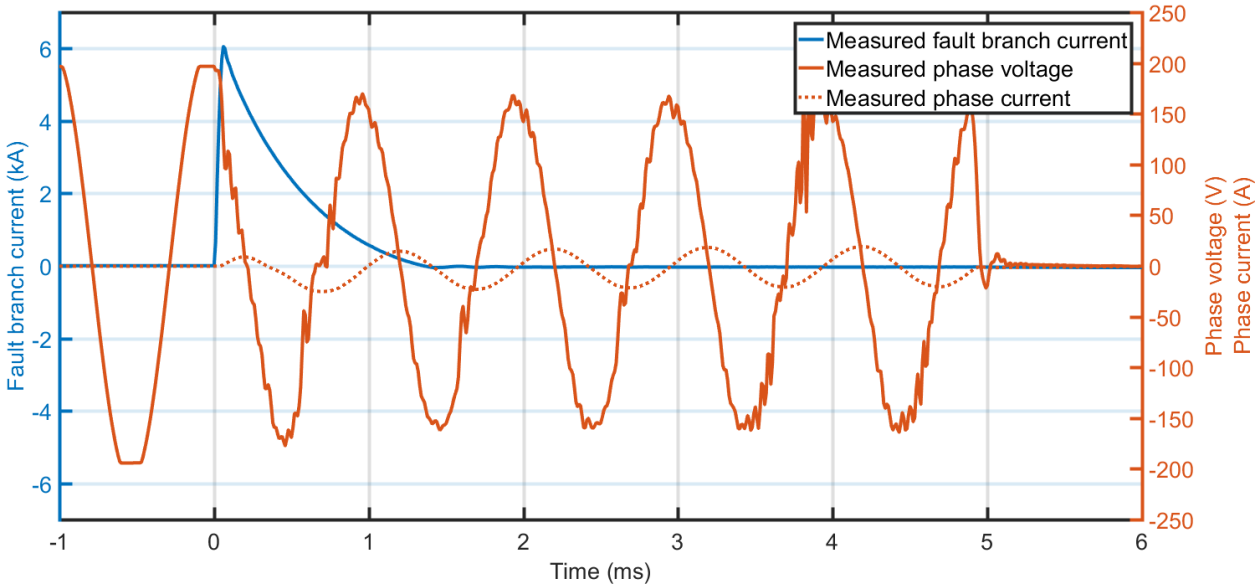


Figure 3.52: Measured AC and DC side contributions with initial DC link voltage of 540V and α of 110°

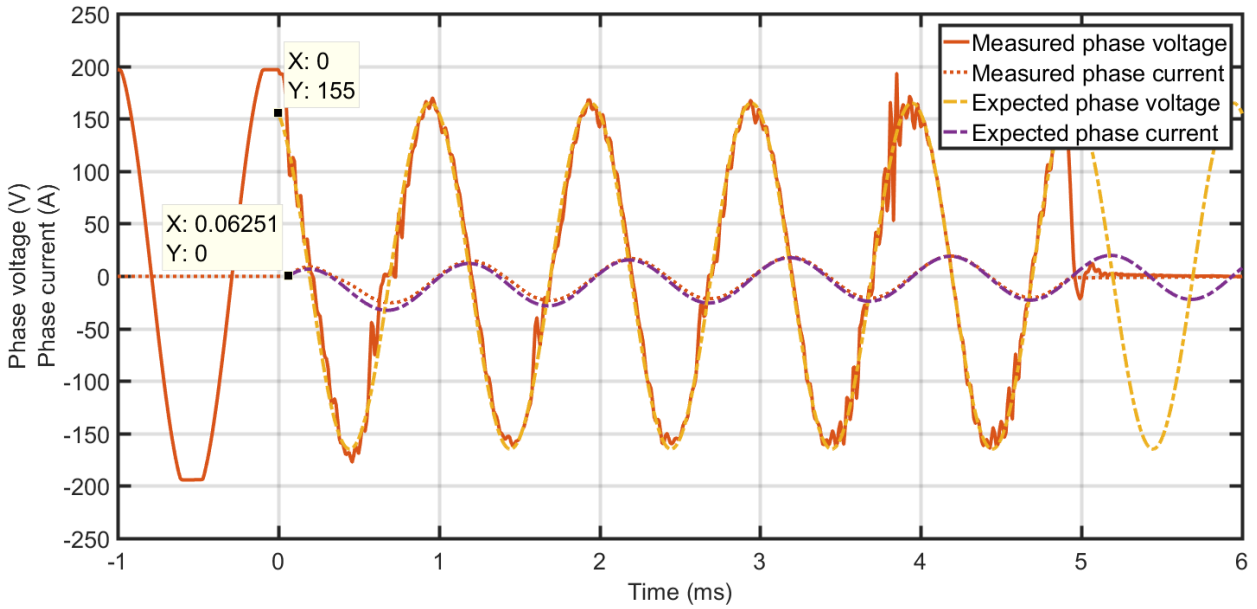


Figure 3.53: Comparison of measured and expected AC side contributions with α of 110°

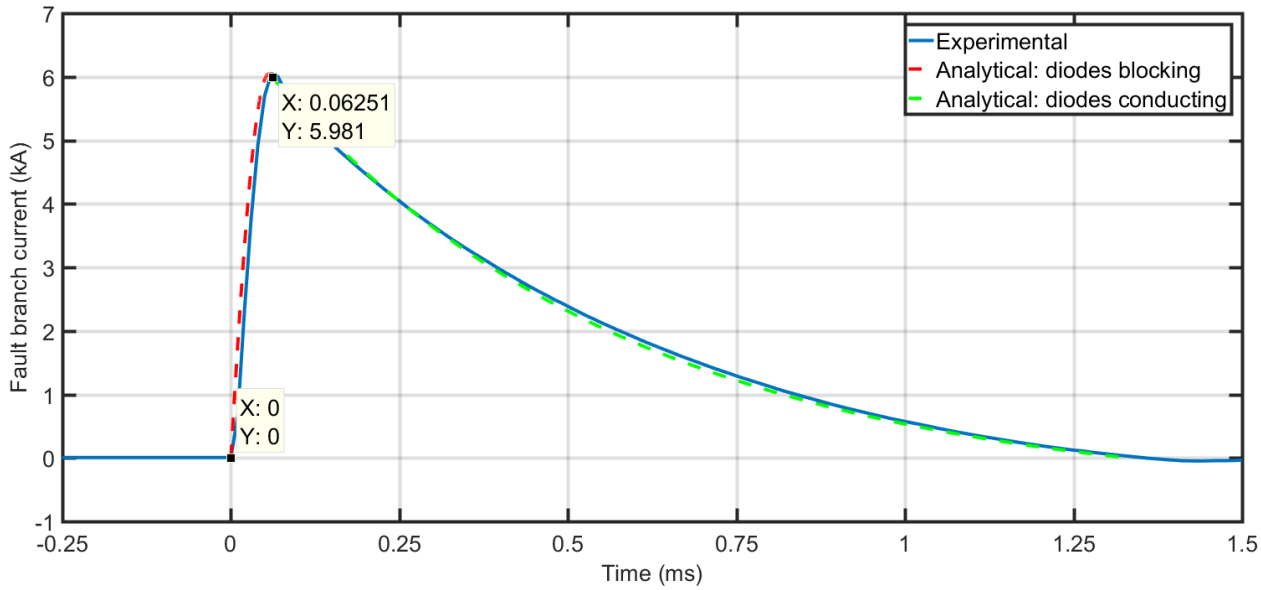


Figure 3.54: Comparison of measured and expected fault branch's current with α of 110°

3.4. Conclusions

This chapter experimentally validates analyses presented in Chapter 2. Three experiments were carried out to validate DC side contributions, AC side contributions, and combined response. Experimental results were shown to match those expected from the analyses presented in Chapter 2 very well under all conditions tested. It was found that the module side inductance, although small, influence the fault response. Some modifications to previous analyses were presented to account for this inductance improving the accuracy of the analytical expressions. With the worst-case DC line-to-line fault response analyses experimentally validated, the following chapters take advantage of this work to develop DC fault protection technologies.

3.5. References

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[2] SEMIKRON International GmbH, "Thyristor / Diode Modules" SKKH 460 Datasheet, Sept. 2012.
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Chapter 4: DC Short-Circuit Fault Protection of Power Converters Using Silicon Carbide Current Limiting Diodes

4.1. Introduction

DC short-circuit faults are one of the most damaging scenarios in power electronic converters. They can result from various conditions inside and outside the converter causing current flow that can reach many times the rated current, leading to significant damage at system and component levels. Therefore, it is important to protect the system from these faults by developing appropriate protection methods, especially in high reliability applications. This chapter presents one possible solution to this problem; using Silicon Carbide Junction Field Effect Transistors (SiC-JFETs) as Current Limiting Diodes (CLDs).

The use of CLDs for fault protection offers many advantages over conventional approaches. Firstly, the device requires no external gate power or control, simplifying its operation and increasing its reliability. Previous approaches utilizing normally-OFF semiconductors required a large number of components to control the devices. For example, the approach presented in [1], which implements an IGBT-based protection device requires 16 additional components to operate the semiconductor, in addition to a 12V power supply and a microcontroller. Secondly, conventional approaches typically operate semiconductors in a binary mode, where the devices are either ON or OFF. Modulation of semiconductors' gate voltages to control their resistances has been very limited in application. This is due to the limited junction temperatures Normally-OFF devices can operate at (typically up to 175°C) which in turn limits the amount of power they are capable of dissipating, even momentarily. In contrast, commercially available SiC normally-ON JFETs have been shown to be capable of operating up to ≈ 660°C [2], which significantly extends their capabilities for operating as current limiters.

The use of current limiters, as opposed to mechanical or semiconductor based switches, can enhance the reliability of the system without compromising its power density. Conventional ON/OFF based protection devices operated based on set thresholds (typically i^2t). The designer is often faced with a dilemma when determining this threshold: if the threshold is set too low, the system becomes susceptible to transients triggering false trips, and thus compromising reliability.

On the other hand, if the threshold is set too high, many components would have to be unnecessarily oversized to be capable of operating up to that threshold. As there is no tripping involved when using current limiter, the current magnitude at which limiting occurs can be minimized without risking a false trip, after which the system would have to be reset. However, it should be noted that reduction of the current limit (saturation current) comes at the expense of higher on state resistance of the CLD, and thus, losses, as will be discussed later in this chapter.

This chapter investigates the feasibility of using SiC based CLDs for short-circuit protection of power converters. First, a physics-based SiC-CLD SPICE model is created. This model accounts for the CLD's junction temperature (T_j) and physical features effects on its response. An equivalent fault circuit, including this model of the CLD is then analyzed. This circuit, shown in Figure 4.1, includes a charged bulk capacitor (C), its Equivalent Series Inductance and Resistance (ESL & ESR), and an equivalent fault path's inductance and resistance (L_{short} and R_{short}), with an initial current of I_0 flowing through the circuit.

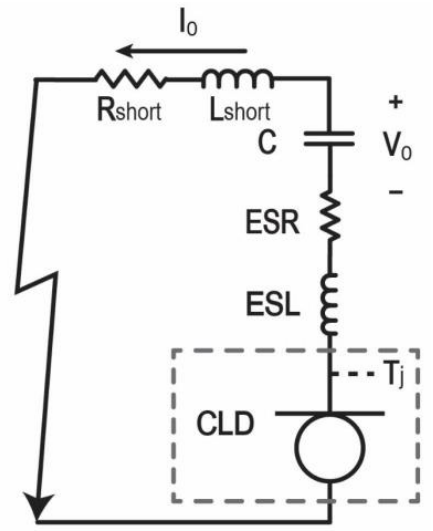


Figure 4.1: Equivalent fault circuit under investigation

The equivalent fault circuit including a CLD was thoroughly studied, by analyzing the circuit's fault response and its dependences on various CLD and fault circuit parameters. Multiple stages of the response have been identified, with the equivalent circuits generated, and analytical expressions derived for all currents and voltages of interest. The analytical results are validated against simulations using typical SiC-JFET device parameters demonstrated in the literature,

packaging parameters that have been analytically extracted for this device, and equivalent fault circuit parameters derived in Chapter 2.

4.2. Physics-based Silicon Carbide Current Limiting Diode Model

To study the interactions between the CLD and equivalent fault circuit and their dependency upon device characteristics, a physics-based model of the CLD was considered. This model accounts for the CLD's temperature and physical features effects on its short circuit response. Multiple analytical models of Si and SiC JFETs have been proposed [3-5], with different methods of representing the velocity vs. electric field relationship, using constant mobility, 2-piece linear approximation (piece-wise function), or empirical formula, as compared in Figure 4.2. Due to its improved accuracy in the saturation region, a physics based SiC-JFET model with empirical approximation of the electric field vs. velocity relationship was implemented [3]. The gate and source contacts of the JFET are assumed to be connected, to produce a two-terminal current limiting diode ($V_{GS}=0$). The derivations of this model and implementation in SPICE are presented in this section.

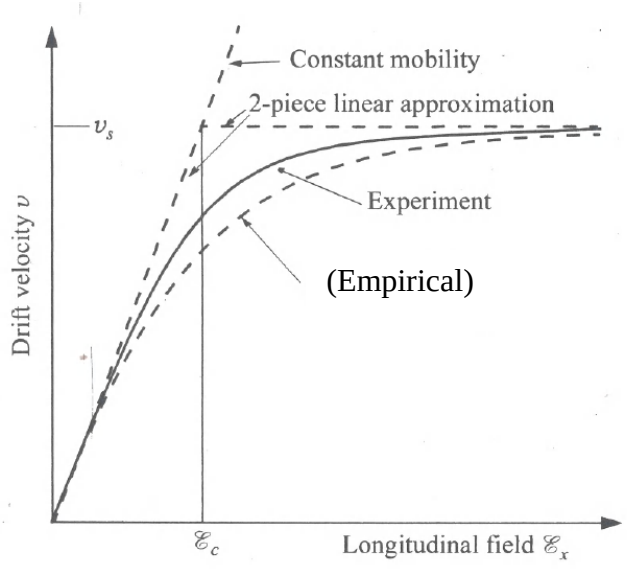


Figure 4.2: Comparison of drift velocity vs. electric field representations [5]

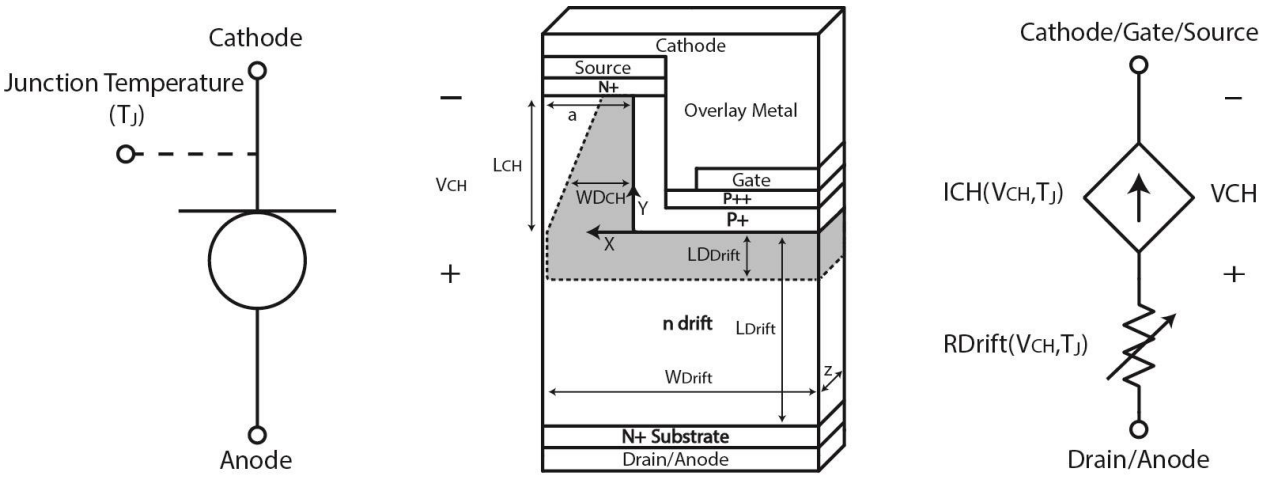
The symbol of the CLD model implemented is shown in Figure 4.3 (a), where under forward bias, current enters through the Anode terminal and exits through the Cathode. The voltage at the T_J terminal represents the junction temperature of the device in Kelvin.

Internally, the device cell contains two main physical regions, the mesa and drift regions, as shown in Figure 4.3 (b). The drift region represents the bulk area of the device which supports drain-to-source voltage across the device when it's in blocking mode (OFF-state), and typically has the highest resistance. The length (L_{Drift}) and dropping concentration of this region determine the voltage blocking capability of the device. Whereas the depth (Z) and width (W_{Drift}) of each cell and number of cells in a die determine the current capacity of the die. The length, width, depth, and doping concentration of the drift region also influence the resistance of the drift region, and consequently, the total resistance of the device. The drain contact is located at the bottom side of the die and separated from the drift region by a heavily doped (N++) substrate which improves the resistance of the contact. The mesa region extends above the drift region connecting to the source contact at the top side through a heavily doped N+ region, and to the gate contact on the side of the cell through P and P++ regions. The length (L_{CH}) and width (a) of the mesa region determine the magnitude of current at which the device saturates. Both the L_{CH} and a also influence the resistance of the mesa region and the total resistance of the device.

In a CLD configuration, the gate and source contacts may be connected at the cell level using an overlay metal, as shown in Figure 4.3 [6]. This arrangement has the advantages of [6]:

1) A simpler, higher yield, and lower cost manufacturing process.
2) A much greater surface area for heat dissipation from the upper surface of the die.
3) A flat top surface ideally suited for a compression package allowing heat transfer to take place from both the top and bottom surfaces.

In the equivalent circuit model, shown in Figure 4.3 (c), the drift region is represented by a variable resistor that is proportional to the junction temperature and channel potential ($RDrift(V_{CH},T_J)$). As temperature increases, the mobility of electrons in the device decreases leading to higher resistivity, and thus, resistance of the drift region. In contrast, as channel potential increases, the depletion region extends further into the drift region (LD_{Drift} increases) decreasing the effective length of the drift region, and therefore its resistance. The channel region is represented by a current source that is also proportional to channel potential and junction temperature ($I_{CH}(V_{CH}, T_J)$). Expressions for these two components ($I_{CH}(V_{CH}, T_J)$ and $RDrift(V_{CH},T_J)$) are next derived, starting with the channel region's current.



(a) (b) (c)

Figure 4.3: (a) CLD symbol, (b) structure [4], and (c) equivalent circuit

4.2.1. Current Limiting Diode's Model Derivation

Gauss's law of electrostatics in the differential form states that:

$$\nabla . E = \frac{dE_x}{dx} + \frac{dE_y}{dy} + \frac{dE_z}{dz} = \frac{\rho}{\varepsilon_s} \tag{4.1}$$

where E is the electric field in the channel region and $E_x, E_y, \& E_z$ are its components in the directions of *x*, *y* and *z* axes respectively, ρ is the charge density, and ε_s is the permittivity of the material [7]. Assuming the electric field in the channel only varies gradually in the *y* and *z* directions, this expression can be simplified to only include the *x*-axis component as:

$$\frac{dE_x}{dx} = \frac{\rho}{\varepsilon_s} = \frac{qN_D}{\varepsilon_s} \tag{4.2}$$

where q is the elementary charge, and N_D is the doping concentration of the mesa region in cm^{-3}. By double integrating (4.2), an expression with respect to the potential at the depletion region's boundary can be found as:

$$\frac{qN_D WD_{CH}^2}{2\varepsilon_s} = \phi_{bi} + \phi_{CH} \tag{4.3}$$

where ϕ_{CH} is the channel region's potential in volts, and ϕ_{bi} is the built-in potential across the gate/channel (P+/n) junction in equilibrium in volts, defined as:

$$\phi_{bi} = \frac{kT}{q} ln(\frac{N_A N_D}{n_i^2}) \quad (4.4)$$

where k is Boltzmann's constant, N_A in the gate's P+ region's doping concentrations in cm^{-3}, and n_i is the intrinsic carrier concentration in cm^{-3} given in [8] for 4H-SiC with respect to temperature as:

$$n_i = 1.70x10^{16} T^{3/2}\, e^{-2.08x10^4/T} \quad (4.5)$$

Channel potential varies in the *y* direction due to current flow through the channel, and thus, voltage drop across the channel. Therefore, depletion region's width in the channel also varies as:

$$WD_{CH}(y) = \sqrt{\frac{2\varepsilon_s(\phi_{ch}(y) + \phi_{bi})}{qN_D}} \quad (4.6)$$

The charge density in the channel *Q(y)* can be found as:

$$Q(y) = qN_D(a - W_{DCH}(y)) \quad (4.7)$$

where *a* is the mesa region's width in cm. Channel current then becomes:

$$I(y) = ZQ(y)v(y) \quad (4.8)$$

where *Z* is the depth of the device in the *z* direction and $v(y)$ is the velocity of electrons in the channel region.

A) Constant Mobility

The expression for channel current will first be derived based on constant mobility relationship between velocity and electric field, and then adjusted to account for velocity saturation. Constant mobility implies that:

$$v(y) = \mu E_y \quad (4.9)$$

where μ is the mobility of electrons in the channel, defined in [8] for 4H-SiC with respect to temperature as:

$$\mu_n(T) = 1140\left(\frac{T}{300}\right)^{-2.70} \tag{4.10}$$

and with respect to doping concentration N_D also in [8] as:

$$\mu_n(N_D) = \frac{4.05\text{x}10^{13} + 20N_D^{0.61}}{3.55\text{x}10^{10} + N_D^{0.61}} \tag{4.11}$$

The combined expression for the mobility can be expressed as:

$$\mu_n(T, N_D) = \frac{4.05\text{x}10^{13} + 20N_D^{0.61}}{3.55\text{x}10^{10} + N_D^{0.61}} \left(\frac{T}{300}\right)^{-2.70} \tag{4.12}$$

Using the constant mobility model, and integrating along the channel length, the magnitude of the current can be found as:

$$I_{CH} = \frac{Z}{L_{ch}} \int_0^{Lch} Q(y)v(y)\, dy \tag{4.13}$$

where L_{CH} is the length of the channel in the y direction. After substituting $Q(y)$ and $v(y)$ from (4.7) and (4.9) respectively in (4.13), the expression for the current becomes:

$$I_{CH} = \frac{ZqN_D}{L_{ch}} \int_0^{L_{ch}} \big(a - W_D(y)\big)\mu E_y\, dy \tag{4.14}$$

which after substituting $d\phi_{ch}$ for $E_y dy$, so that the integration is now performed with respect to channel potential, becomes:

$$I_{CH} = \frac{ZqN_D\mu}{L_{ch}} \int_0^{V_{ch}} \left(a - \sqrt{\frac{2\varepsilon_s(\phi_{ch} + \phi_{bi})}{qN_D}}\right) d\phi_{ch} \tag{4.15}$$

Using the following relationship, the integration in (4.15) can be evaluated as (4.17).

$$\int \sqrt{x + b}\, dx = \frac{2\sqrt{(x + b)^3}}{3} \tag{4.16}$$

$$I_{CH} = G_i \left(V_{ch} - \frac{2}{3\sqrt{\phi_p}} \left(\sqrt{(V_{ch} + \phi_{bi})^3} - \sqrt{(\phi_{bi})^3} \right) \right) \tag{4.17}$$

where,

$$G_i = \frac{ZqN_D\mu a}{L_{ch}} \tag{4.18}$$

$$\phi_p = \frac{qN_D a^2}{2\varepsilon_s} \tag{4.19}$$

B) Empirical Approximation

Using an empirical formula to account for velocity saturation with electric field was found in [5] to result in a reduction of current by a factor of $(1 + V_{ch}/\varepsilon_c L_{ch})$, as:

$$I_{CH} = \frac{G_i}{(1 + V_{ch}/\varepsilon_c L_{ch})} \left(V_{ch} - \frac{2}{3\sqrt{\phi_p}} \left(\sqrt{(V_{ch} + \phi_{bi})^3} - \sqrt{(\phi_{bi})^3} \right) \right) \tag{4.20}$$

The drain voltage at which saturation occurs (V_{CHSAT}), can be found by solving the following relationship, obtained by setting $\frac{dI_{CH}}{dV_{ch}} = 0$, for V_{CHSAT}:

$$\epsilon_c L_{ch} = \sqrt{\frac{\phi_{bi} + V_{CHSAT}}{\phi_p}} (\epsilon_c L_{ch} + V_{CHSAT}) - \frac{2}{3\sqrt{\phi_p}} [\sqrt{(\phi_{bi} + V_{CHSAT})^3} - \sqrt{(\phi_{bi})^3}] \tag{4.21}$$

After the channel saturates, the voltage at the pinch off point remains at V_{CHSAT}, so that current in saturation is found as:

$$I_{CHSAT0} = \frac{G_i}{(1 + V_{CHSAT}/\varepsilon_c L_{ch})} \left(V_{CHSAT} - \frac{2}{3\sqrt{\phi_p}} \left(\sqrt{(V_{CHSAT} + \phi_{bi})^3} - \sqrt{(\phi_{bi})^3} \right) \right) \tag{4.22}$$

An additional term is added to account for the decrease of channel's length with increasing drain voltage in saturation (channel length modulation λ):

$$I_{CHSAT}(V_{ch}) = I_{CHSAT0}(1 + \lambda\,(V_{ch} - V_{CHSAT})\,) \tag{4.23}$$

For the calculation of the effective drift region's resistance with respect to channel voltage and temperature ($R_{Drift}(V_{CH}, T_J)$), the depletion region's extension into the drift region (LD_{Drift}) is first found as:

$$LD_{Drift} = \sqrt{\frac{2\varepsilon_s(V_{CH} + \phi_{bi})}{qN_D}} \tag{4.24}$$

and then the effective drift region's resistance is found as follows, where electrons mobility (μ) is temperature dependent per (4.10):

$$R_{Drift} = \rho\frac{L}{A} = \frac{1}{q\mu N_D}\frac{L_{Drift} - LD_{Drift}}{ZW_{drift}} \tag{4.25}$$

4.2.2. Current Limiting Diode Model Implementation

A CLD model was realized in SPICE, as shown in Figure 4.4. This model is based on implementing the equations derived in the previous section as functions (".func"), that take a fixed set of device physical parameters (".param"), and variable junction temperature represented by the voltage on the *T* terminal (*V(T)*). A summary of the parameters used in this model are given in Table 4.1. These parameters are based on typical values demonstrated for this structure in literature. Due to the complexity of (4.21), channel saturation voltage (V_{CHSAT}) was solved for with respect to temperature for the set of device parameters in Table 4.1, then curve-fitted to a second order polynomial function used by the simulation. The results obtained from solving (4.21) are compared to those from the curve fitted function as shown in Figure 4.5. The resulting I(V) output characteristics of this device are plotted for junction temperatures of 300-500K with steps of 50K in Figure 4.6.

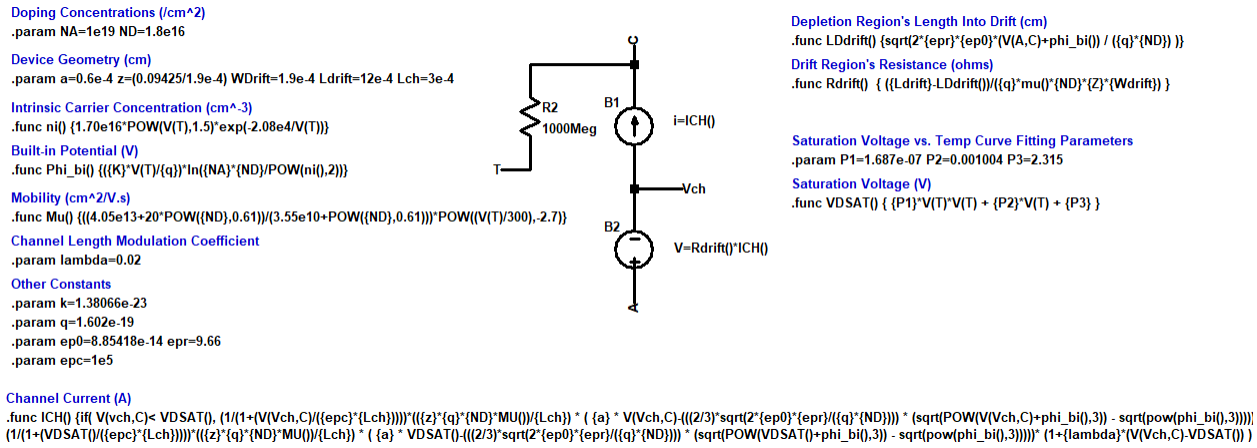


Figure 4.4: Implementation of CLD SPICE model

Table 4.1: Summary of SPICE model's parameters

Device Parameter	**Value**	**Source/Comments**
Gate P+ region doping concentration (NA)	$1\text{x } 10^{19}\ \text{cm}^{-3}$	Typical value used in application [8]
Drift and channel regions doping concentration (ND)	$1.8\text{x } 10^{16}\ \text{cm}^{-3}$	Demonstrated for this structure in [9]
Mesa width (a)	$0.6\text{ x } 10^{-4}\ \text{cm}$	Values in this range demonstrated for this structure in [10]
Channel length (L_{ch})	$3\text{ x } 10^{-4}\ \text{cm}$	Demonstrated for this structure in [9]
Drift region's length (L_{Drift})	$12\text{ x } 10^{-4}\ \text{cm}$	Demonstrated for this structure in [9]
Drift region's width (W_{Drift})	$1.9\text{ x } 10^{-4}\ \text{cm}$	Demonstrated for this structure in [9]
Device area (Z x W_{Drift})	$0.307\text{x}0.307\ \text{cm}^2$	Die area of commercial SiC-JFET [11]
Channel modulation coefficient (λ)	0.02	Demonstrated for this structure in [12]
Constants	**Value**	**Source/Comments**
Boltzmann Constant (K)	$1.38066\text{x}10^{-23}\ \text{J/K}$	Given in [13]
Elementary charge (q)	$1.60218\text{x}10^{-19}\ \text{C}$	Given in [13]
Permittivity of material (ϵ_s)	$85.53\text{x}10^{-14}\text{F/cm}$	Given for 4H-SiC in [13]
Critical Electric Field (ε_c)	$1\text{ x } 10^{5}\text{V/cm}$	Given for 4H-SiC in [14]
Channel Saturation Voltage (V_{CHSAT}) vs. Temperature Curve Fitted Function		
Form	$P_1T_j^2 + P_2T_j + P_3$	
Parameters	$\text{P}_1 = 1.687\text{x}10^{-7}, \text{P}_2 = 1.004\text{x}10^{-3}, \text{P}_3 = 2.315$	

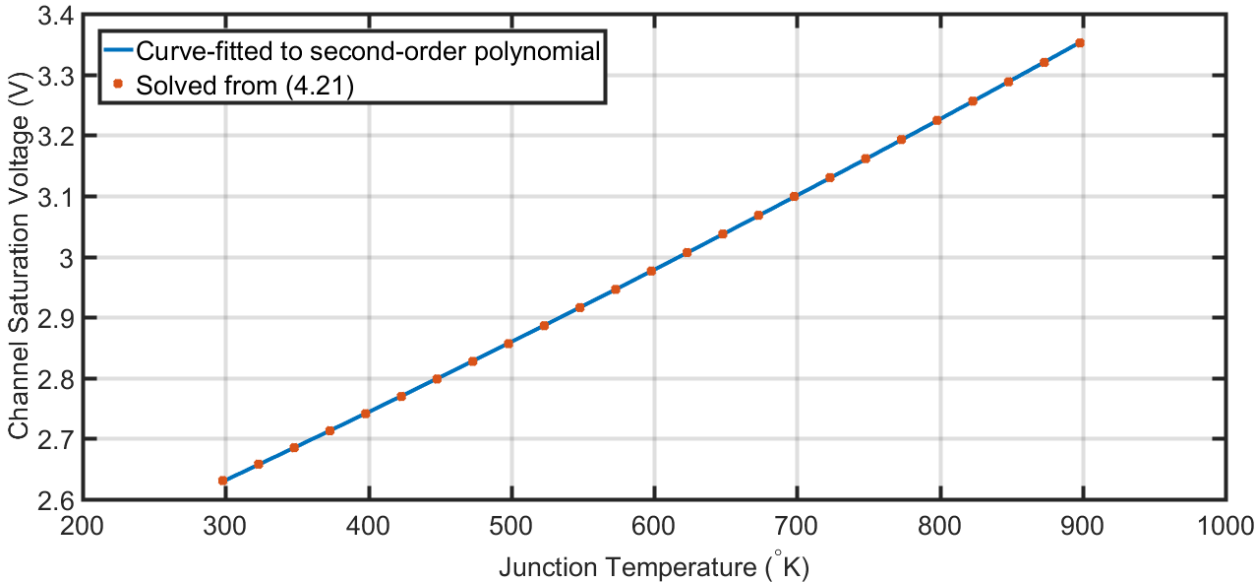


Figure 4.5: Comparison of channel saturation voltage (*VCHSAT*) vs. junction temperature found by solving (4.21), and curve fitted using a polynomial function with the form and parameters in Table 4.1.

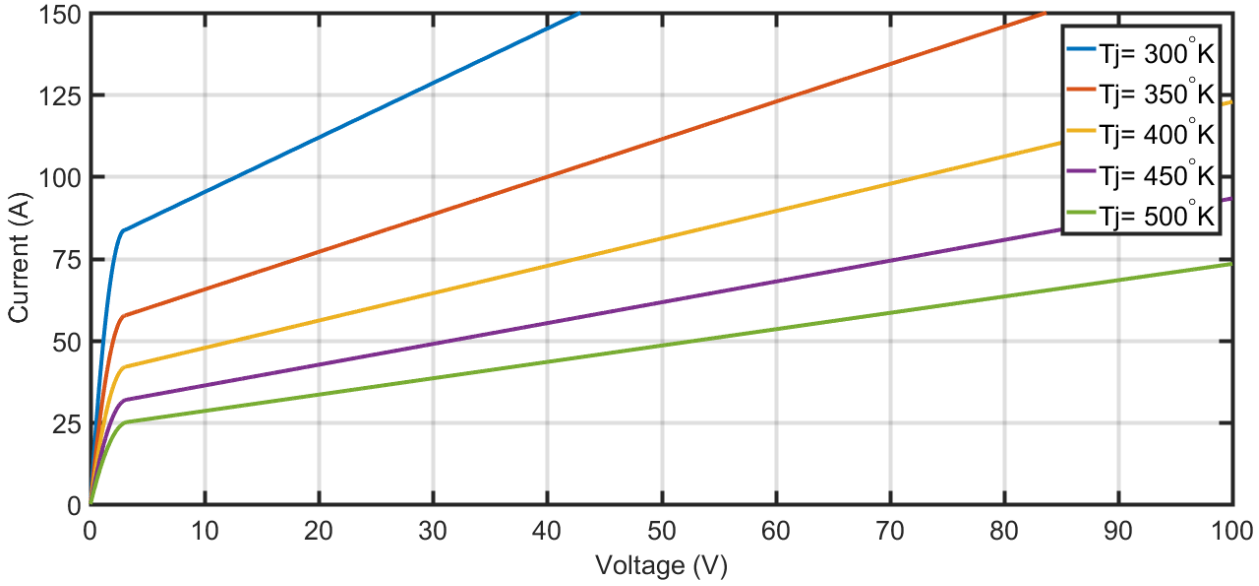


Figure 4.6: Output characteristics of SPICE modelled device for 350-500K junction temperatures with steps of 50K

Output current of the device significantly decreases with temperature due to its dependency on mobility (μ) as given by equations (4.17) and (4.18). The mobility of electrons given by (4.11) and plotted in Fig. 4.14 decreases rapidly with temperature due to electrons scattering.

4.3. Analyses of Current Limiting Diodes' Fault Response

Using the device model derived in the previous section, the reaction of the CLD under a fault condition and its dependency on converter, fault, and device parameters are presented in this section. The equivalent fault circuit was simplified as shown in Figure 4.7. In this circuit, the DC side capacitor (C) is initially charged with a voltage of (V_0). An initial current (I_0) flows through the fault resistance (R_{Short}), inductance (L_{Short}), and the capacitor's Equivalent Series Resistant (ESR) & Inductance (ESL).

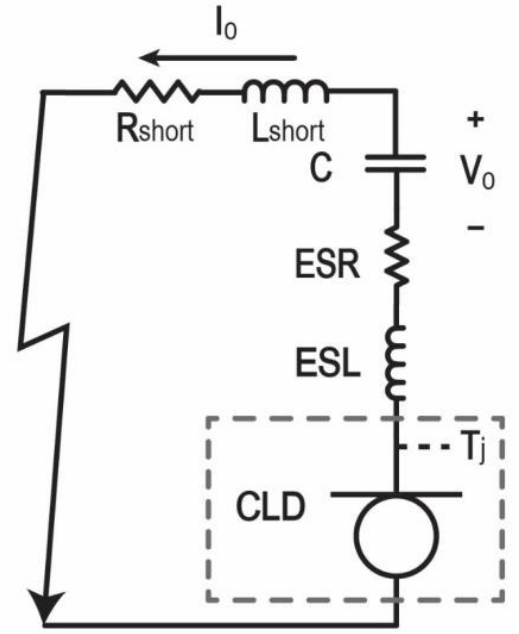


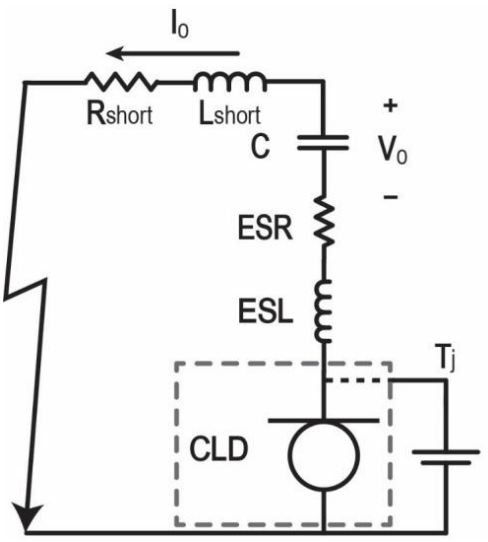
Figure 4.7: Equivalent fault circuit under consideration

Analysis of this circuit was carried out in two stages:

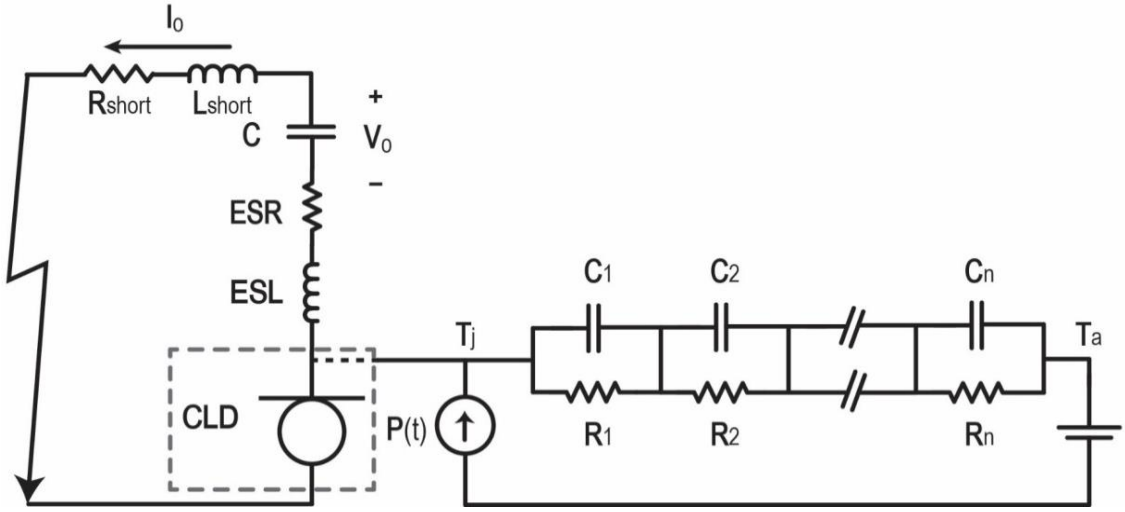
1- Assuming constant junction temperature of the CLD (isothermal condition), as shown in the equivalent circuit of Figure 4.8 (a), where constant voltage is applied to the T_J terminal. Under this simplified condition, multiple stages of the response have been identified, with the equivalent circuits at each stage generated, and analytical expressions describing current and voltage characteristics of the CLD derived, for a set of converter's, fault's, and CLD's parameters (C, ESL, ESR, L_{short}, R_{short}, I_0, V_0, R_{ON0}, V_{CHSAT}, I_{CHSAT0}, and λ).

2- The influence of device heating was then considered by modeling the junction temperature (T_J) as a power ($P(t)$), thermal impedance (R_1-R_n & C_1- C_n), and ambient temperature (T_a)

dependent parameter, as shown in the equivalent circuit of Figure 4.8 (b). Due to the complex dependencies under this condition, the response of the circuit was mainly investigated in simulation, and then related to analytical relationships.



(a)



(b)

Figure 4.8: Equivalent circuits under (a) isothermal, and (b) thermal conditions

4.3.1. Fault Response Under Isothermal Condition

The CLD's current response under isothermal condition is illustrated in Figure 4.9. Here, three operation stages can be identified: linear, current limiting, and second linear. Since the initial current prior to a fault event is expected to be below the CLD's channel saturation level (I_{CHSAT0}),

the device begins operation in the first linear region, where it has relatively small resistance. In this stage of operation, current begins to rise from its initial value (I_0) with a slope of $V_0/(ESL+L_{short})$, until reaching current saturation level (I_{CHSAT0} given by (4.22)) where the resistance of the device becomes significant, and the current limiting stage begins. After the CLD is saturated, current continues to rise until reaching a peak shortly after, then decays in a damped response. As current continues to decay, it reaches saturation level again and starts operating in its second linear stage. Detailed analyses of the circuit response during each one of these stages are presented next.

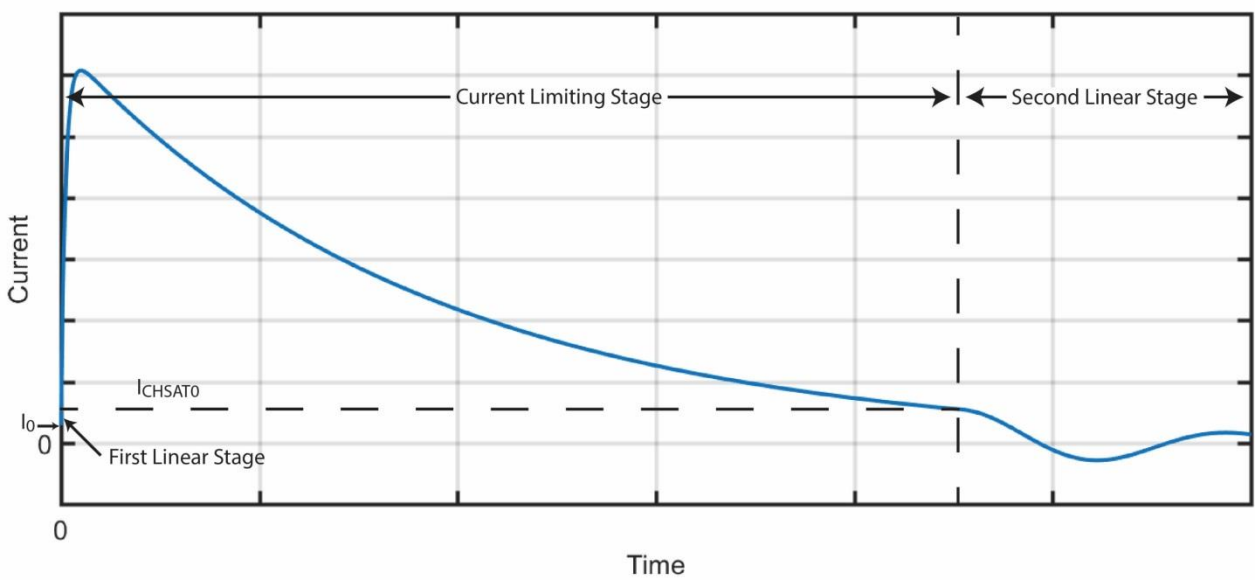


Figure 4.9: Typical CLD fault response under isothermal condition

A) First Linear Stage

In the first stage of the fault event, the CLD operates in the linear region of its I(V) curve, where it can be represented by its ON-state resistance (R_{ON0}), as shown in the equivalent circuit in Figure 4.10. The value of that resistance is current magnitude dependent and is typically given at the rated current of the device. However, for this analysis, this can be approximated by the zero current resistance given by equation (4.26). The actual on-state resistance is expected to be higher due to the increase of channel resistance with current as the channel approaches pinch-off. However, this approximation is sufficient at this stage as the fault path's reactance during this fast-transient period is much more significant than the CLD's resistance. Thus, small variation or error in the CLD's ON-state resistance has little influence on the circuit response in this stage.

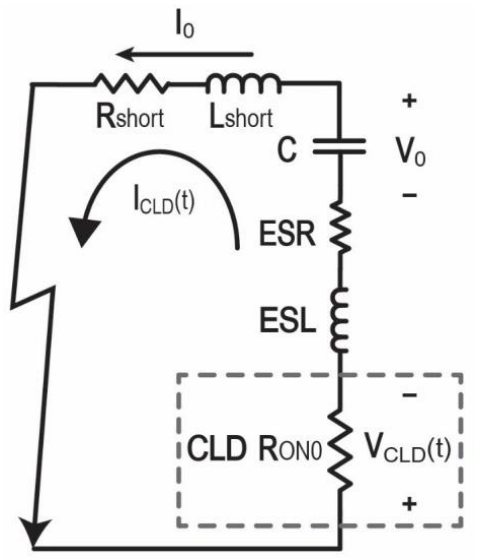


Figure 4.10: Equivalent circuit during first linear stage

The on-state resistance of the CLD is the sum of drift and channel regions resistances:

$$R_{ON0} = \ R_{Drift0} + R_{CH0} \tag{4.26}$$

where R_{Drift0} is obtained by substituting the diffusion length at $V_{CH} = 0$ $\left(LD_{Drift}(V_{CH} = 0)\right)$ into (4.25), and R_{CH0} is obtained using first order approximation of (4.17) with respect to V_{CH} at $V_{CH}=0$, as [5]:

$$R_{CH0} = \frac{1}{G_i\ (1 - \sqrt{(\phi_{bi}/\phi_p)})} \tag{4.27}$$

Following the same procedure used to derive (2.9), an expression for current in this stage can be derived as:

$$i_{CLD}(t) = \ e^{-\beta t}(I_0\ cos(\omega_r t) + A\ sin(\omega_r t)) \tag{4.28}$$

where,

$$A = \ \frac{\frac{V_0}{ESL + L_{short}} - \beta I_0}{\omega_r} \tag{4.29}$$

$$\beta = \frac{ESR + R_{Short} + R_{ON0}}{2\ (ESL + L_{Short})} \tag{4.30}$$

where, ω_r can be found from (2.5) and (2.6). Using the current obtained from (4.28), the voltage across the CLD can be found as:

$$v_{CLD}(t) = \ R_{ON0}\ i_{CLD}(t) \tag{4.31}$$

B) Current Limiting Stage

When fault current reaches (I_{CHSAT0}) given by (4.22), the device begins operating in the current limiting stage, where the channel is saturated, and can therefore be represented by an equivalent resistance and voltage drop (V_{SATeq} and R_{SATeq}), as shown in Figure 4.11.

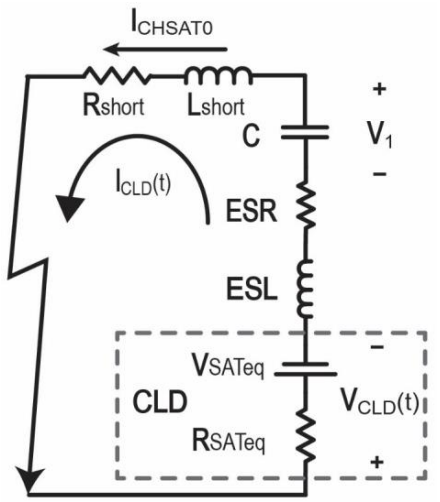


Figure 4.11: Equivalent circuit during saturation stage

The values of these equivalent parameters can be derived from (4.23) as:

$$V_{SATeq} = \ V_{CHSAT} - 1/\lambda \tag{4.32}$$

$$R_{SATeq} = \frac{1}{\lambda I_{CHSAT0}} \tag{4.33}$$

This equivalent circuit disregards the drift region's resistance due to its insignificant value compared with the equivalent channel resistance in saturation (R_{SATeq}), as will be demonstrated later in this chapter. Given the equivalent circuit above, current in this stage can be derived as:

$$i_{CLD}(t) = \ e^{-\beta t}\ (I_{CHSAT0}\ cos(\omega_r t) + A\ sin(\omega_r t)) \tag{4.34}$$

where,

$$A = \frac{\frac{V_1 - V_{SATeq}}{ESL + L_{short}} - \beta I_{CHSAT0}}{\omega_r} \tag{4.35}$$

$$\beta = \frac{ESR + R_{short} + R_{SATeq}}{2\ (ESL + L_{short})} \tag{4.36}$$

and the value of the capacitor's initial voltage (V_1) can be found by integrating the current from the previous stage, like in (2.17). The voltage across the device can be found as:

$$v_{CLD}(t) = \ i_{CLD}(t)\ R_{SATeq} + \ V_{SATeq} \tag{4.37}$$

C) Second Linear Stage

After reaching a peak, current decay in a damped response manner due to the high resistance of the CLD, until reaching (I_{CHSAT0}) again. At that point, the device returns to operating in the linear region, where it can again be represented by R_{ON0}. The equivalent circuit during this stage is shown in Figure 4.12. Except for the initial conditions (I_0 replaced by I_{CHSAT0}, and V_0 by V_2), the equivalent circuit and fault response expressions in this stage are identical to those of the first linear stage.

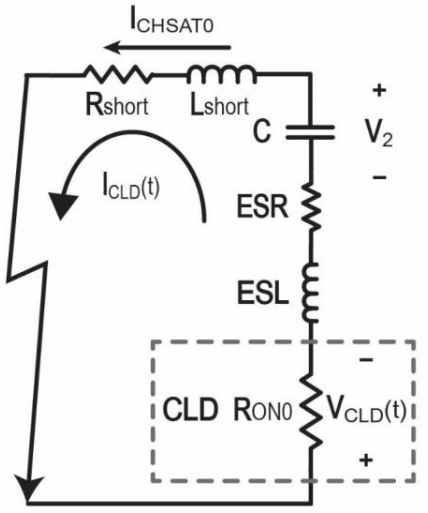


Figure 4.12: Equivalent circuit during second linear stage

4.3.2. Fault Response Under Thermal Condition

When thermal conditions are considered, fault current can no longer be described by a single relationship. Instead, it becomes dependent on the CLD's junction temperature (T_j), which is related to power loss ($P(t)$), thermal impendence ($R_1 - R_n$ & $C_1 - C_n$), and ambient temperature (T_a), as shown in (2.100) and in Figure 4.13. Moreover, power loss itself is proportional to current ($p(t) = i_{CLD}(t)v_{CLD}(t)$). Solving this relationship requires an iterative process, which is most suitable to be carried out in a simulation environment. The response of the circuit under this condition was therefore investigated in SPICE simulations, and then related to analytical relationships.

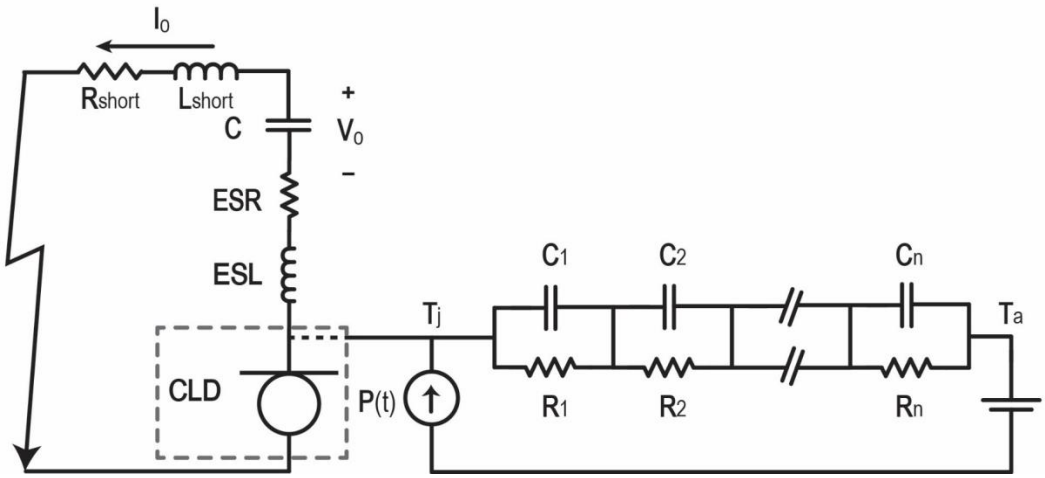


Figure 4.13: Equivalent circuit during second linear stage

During the first linear stage, the CLD's resistance, power losses, and thus, temperature rise are insignificant. Current in this stage, is limited by the loop inductance (L_{short}+ESL) while the CLD has almost no effect. It is therefore expected that the response in the linear stage under thermal condition be identical to the isothermal case. The effects of heating on the circuit response becomes notable when the device begins to operate in the saturation region (current limiting stage), where the losses become significant, and temperature rises rapidly. As temperature increases, electrons mobility decreases due to the increase in electrons scattering, following the relationship given by (4.10), as shown in Figure 4.14. This reduction in mobility proportionally increases the resistance of the drift region. The channel region's resistance also increases with temperature, but at a slower rate than mobility, due to its dependency on the built-in potential, following the relationship given

by (4.4), and plotted in Figure 4.15. As discussed earlier, due to the complex dependencies involved when considering thermal effects, the fault response will mainly be investigated in simulations presented in next section, and then related back to the physical properties (electrons mobility and built-in potential) discussed in this section.

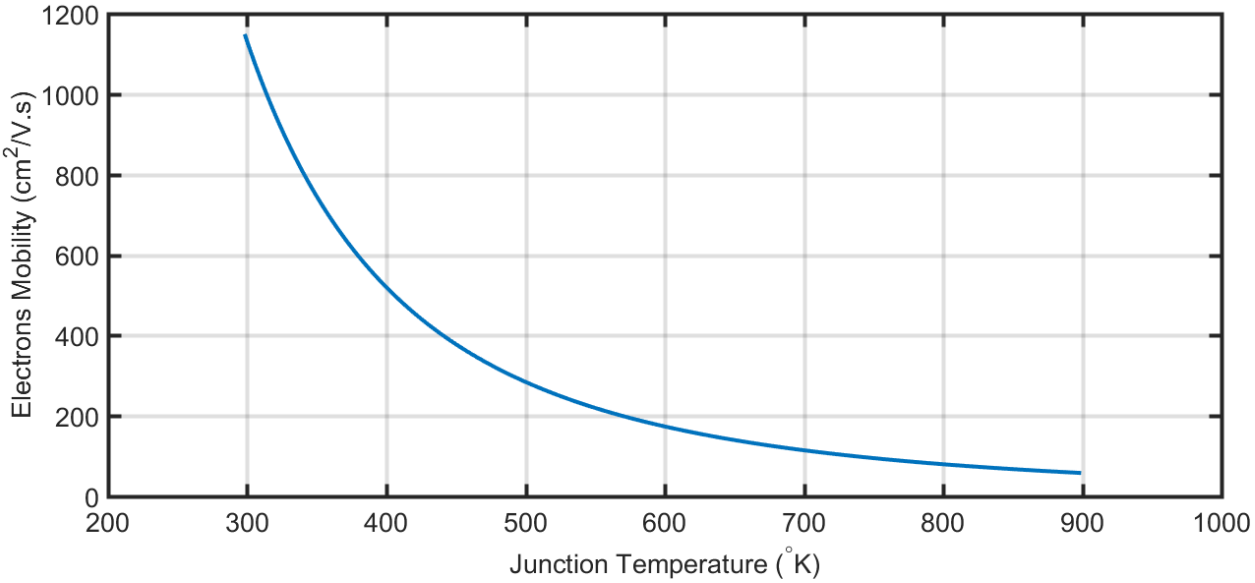


Figure 4.14: Electrons mobility of SiC vs. temperature [8]

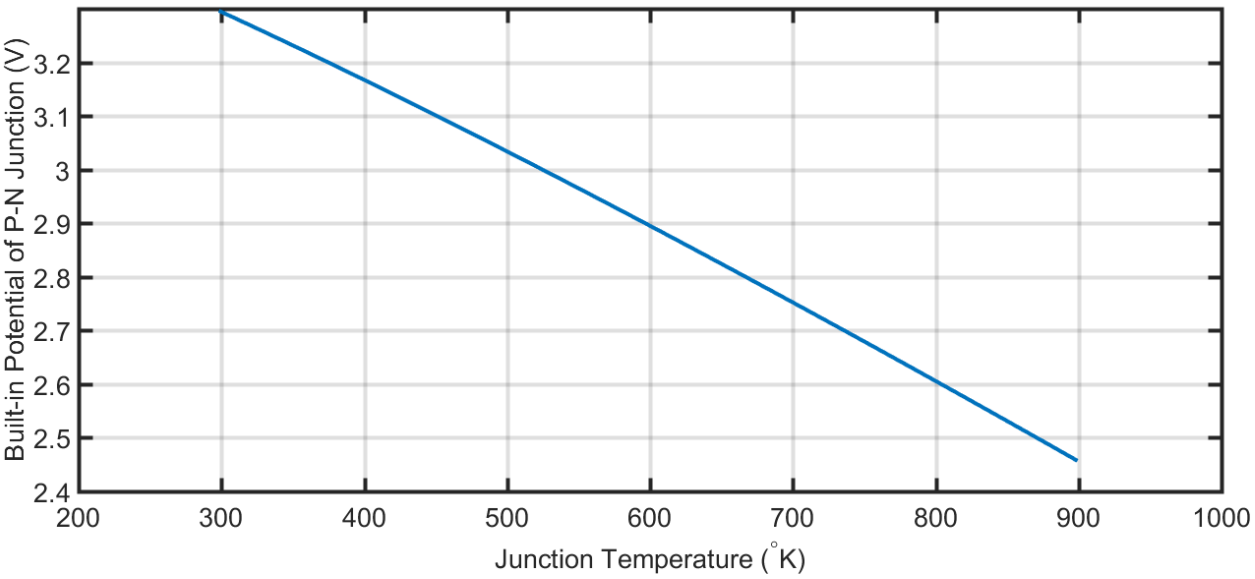


Figure 4.15: Built-in potential of SiC vs. temperature [8]

4.4. Simulation Validation

This section details the simulation-based validation of the above analyses under both thermal and isothermal conditions.

4.4.1. Isothermal Condition

The equivalent fault circuit was simulated in SPICE with the CLD at a fixed junction temperature of 358.15K (85°C) in the schematic shown in Figure 4.16. The fault impedance was assumed to be a 0.5-5.0m 2AWG cable, as shown in Chapter 2. The capacitor's *C*, *ESL*, and *ESR* were set to 500µF, 5nH, and 1.7mΩ respectively, the initial capacitor voltage (V_0) to 540V, and initial fault path's current to zero. These parameters were selected to match those used in Chapter 2, so that fault response with and without the CLD can be compared. The only difference is the initial fault current set to zero instead of 92.6A so that the fault response during the first linear stage can be included in the following comparisons between simulated and analytically calculated responses.

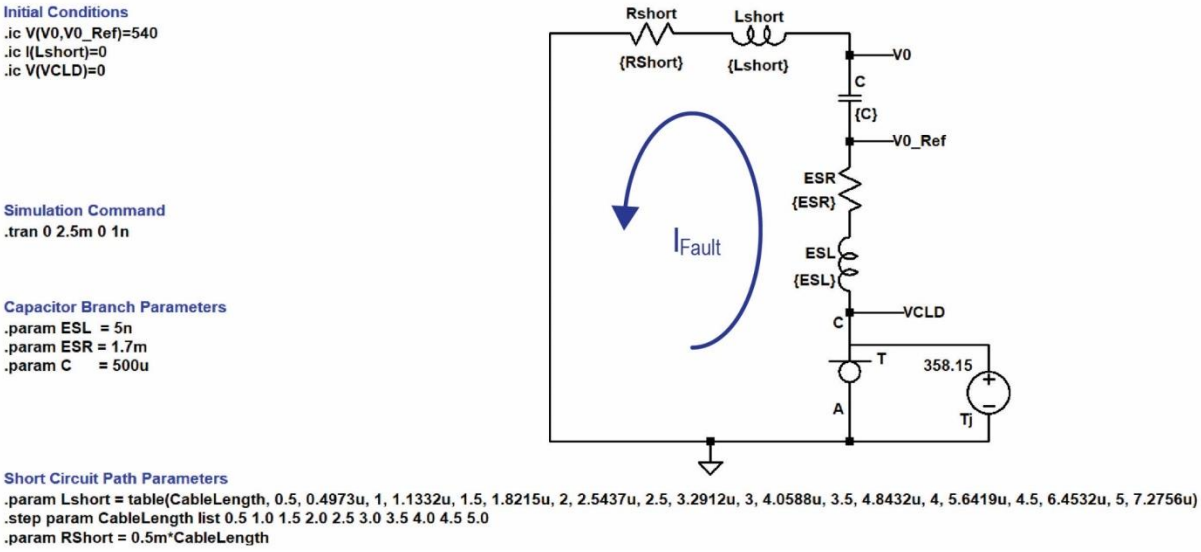


Figure 4.16: Simulation circuit under isothermal condition

Simulated fault currents (I_{Fault}) are shown in Figure 4.17 & Figure 4.18. They demonstrate a significant reduction in peak current to less than 700A, compared with up to 16kA without the CLD, as shown in the Chapter 2. The value of the peak current is mainly influenced by the mesa width (a) which is the width of the channel area of the device where current saturation occurs. By decreasing this width, peak fault current can be decreased at the expense of higher ON-state resistance and losses. These figures show that the cable length, and hence short circuit impedance,

significantly influences the current slew rate during the first linear stage, with the shorter cables having more rapid current surge due to their lower inductances. Whereas, after the peak is reached and before the second linear stage, the CLD's resistance becomes dominant, and the fault response is almost independent of cable length, as shown in Figure 4.18. When the second linear stage is reached, the CLD's resistance decreases, reinstating the effects of cable length.

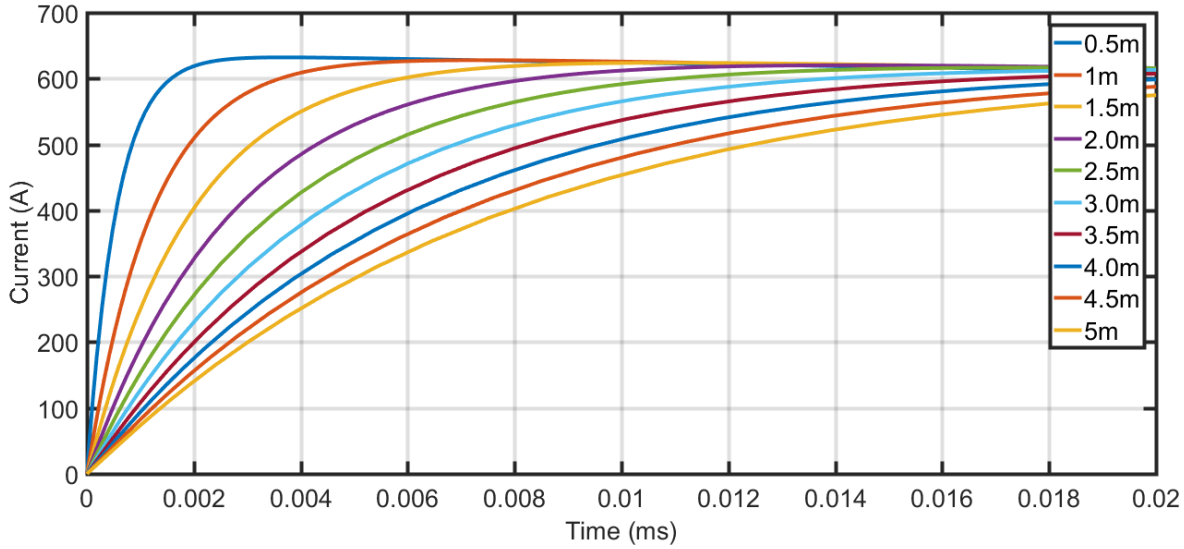


Figure 4.17: Simulated fault current (*IFault*) for cable lengths of 0.5 to 5 meters with 0.5m steps (zoom to initial stage)

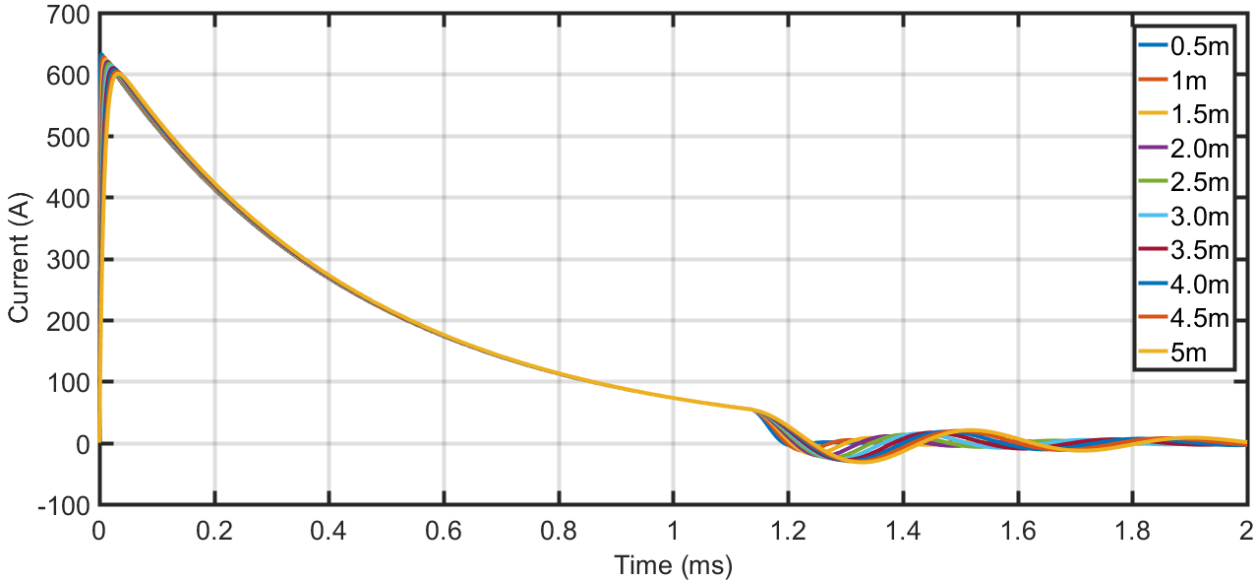


Figure 4.18: Simulated fault current (IFault) for cable lengths of 0.5 to 5 meters with 0.5m steps

The above simulated current response at a cable length of 0.5m was compared against calculations from equations (4.28) and (4.34) in Figure 4.19 and Figure 4.20. As shown, the simulation and calculated values match almost ideally: fault current rises from its initial value of 0A following (4.28), with (R_{ON0}) calculated from (4.25 - 4.27) to be 30mΩ, until reaching saturation level, calculated from (4.22) to be 54.55A. The device then operates in the current limiting stage where fault response follows (4.34). The current decays after the peak, until reaching saturation boundary again at 1.134ms. Like the first linear stage, current in the second linear stage follows (4.28), with some observed error due to the on-state resistance approximation. At this later stage of the response, the CLD's on-state resistance is no longer dominated by the loop inductances. Thus, error due to the on-state resistance approximation becomes more apparent. This is due to the resistance being estimated at 0A, while the actual resistance seen by the circuit is higher. This was demonstrated in Figure 4.21 by plotting the response for higher on-state resistances of *(*x*1.3*-x*1.9)* of the value calculated at 0A (R_{ON0}). The response better resembles the x1.6 case. However, some error is still present with this resistance. This is due to the dynamic behavior of the CLD's on-state resistance with current. The actual resistance in the linear region dynamically decreases as current falls to 0A.

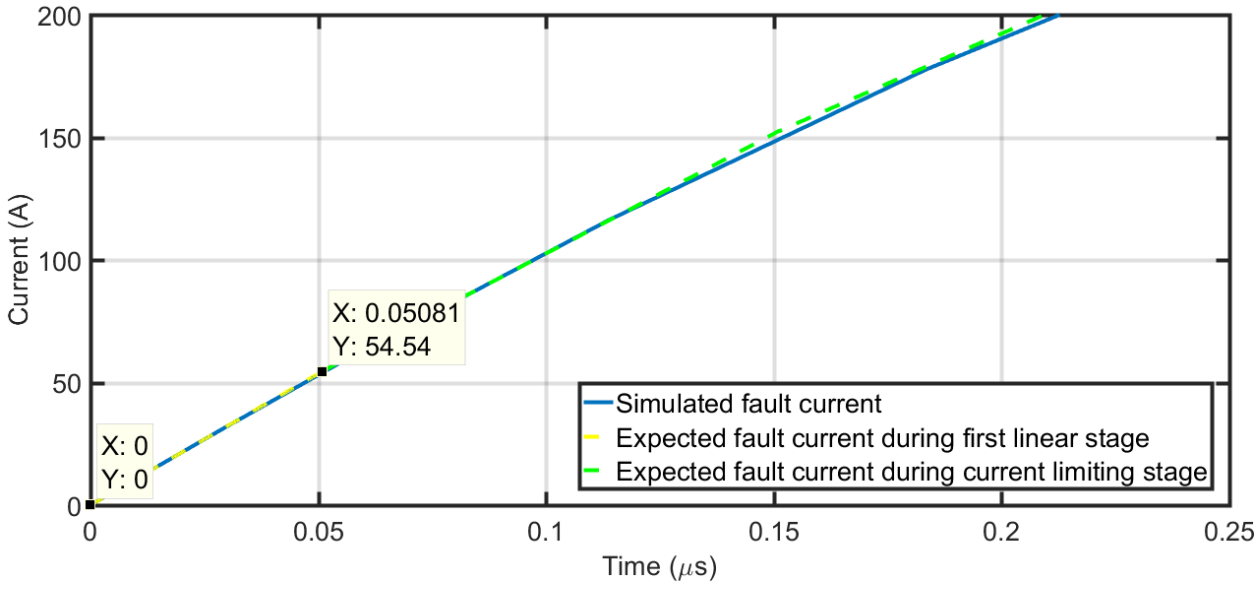


Figure 4.19: Comparison of simulated and expected fault currents during initial stage for the 0.5m line-to-line cable fault condition

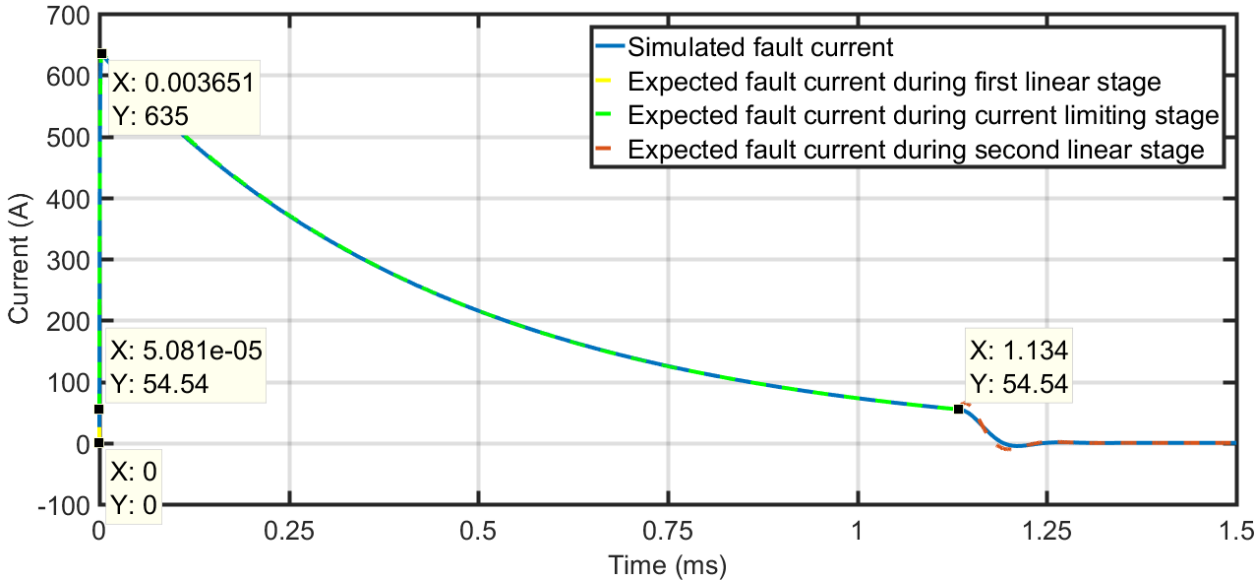


Figure 4.20: Comparison of simulated and expected fault current during all stages of the 0.5m line-to-line cable fault condition

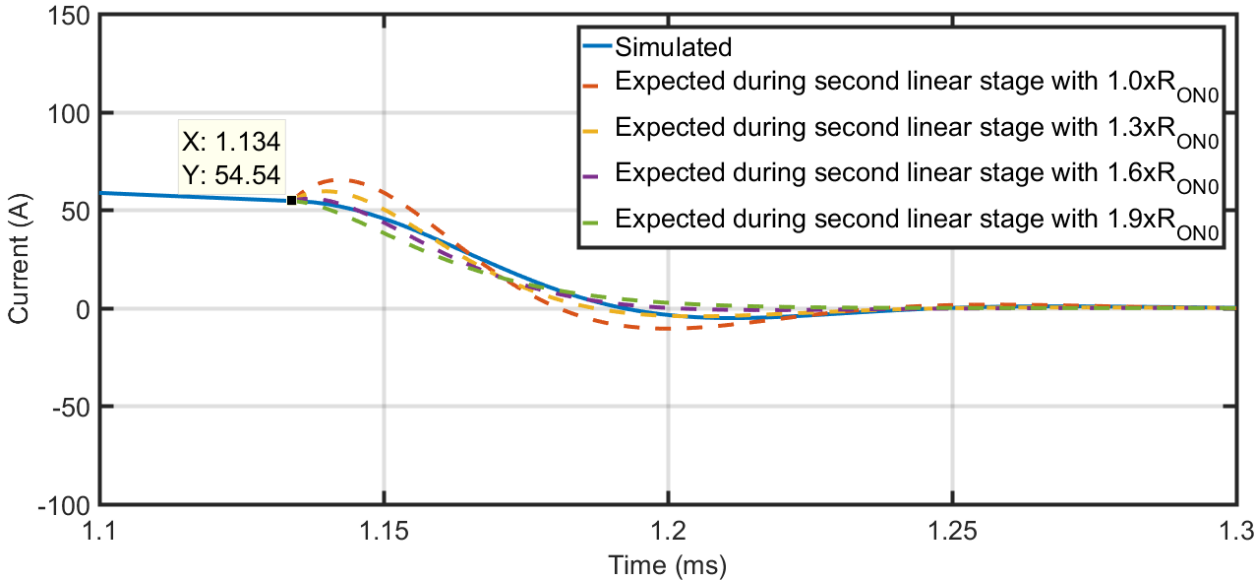


Figure 4.21: Comparison of simulated and expected fault current during second linear stage of a 0.5m line-to-line cable fault condition with x1-x1.9 of 0A CLD on-state resistance (R_{ON0})

The CLD's voltage response computed from (4.31) in the linear stages and from (4.37) in the current limiting stage was also compared to simulation (-VCLD in schematic), as shown in Figure 4.22 and Figure 4.23, and show excellent matching (within 5%). The results have also been compared at the longest cable length of 5m as shown in Figure 4.24 and Figure 4.25, to further confirm the analyses. For this longer fault cable length condition, the CLD reaches saturation level

slightly after the 0.5m case at 0.7µs, and a slightly lower peak of 602.2A compared with 635A in the 0.5m case. The most notable difference is the better matching of expected and simulated response in the second linear stage. Due to the higher fault impedance, the error in CLD resistance in that stage results in less mismatch with expected.

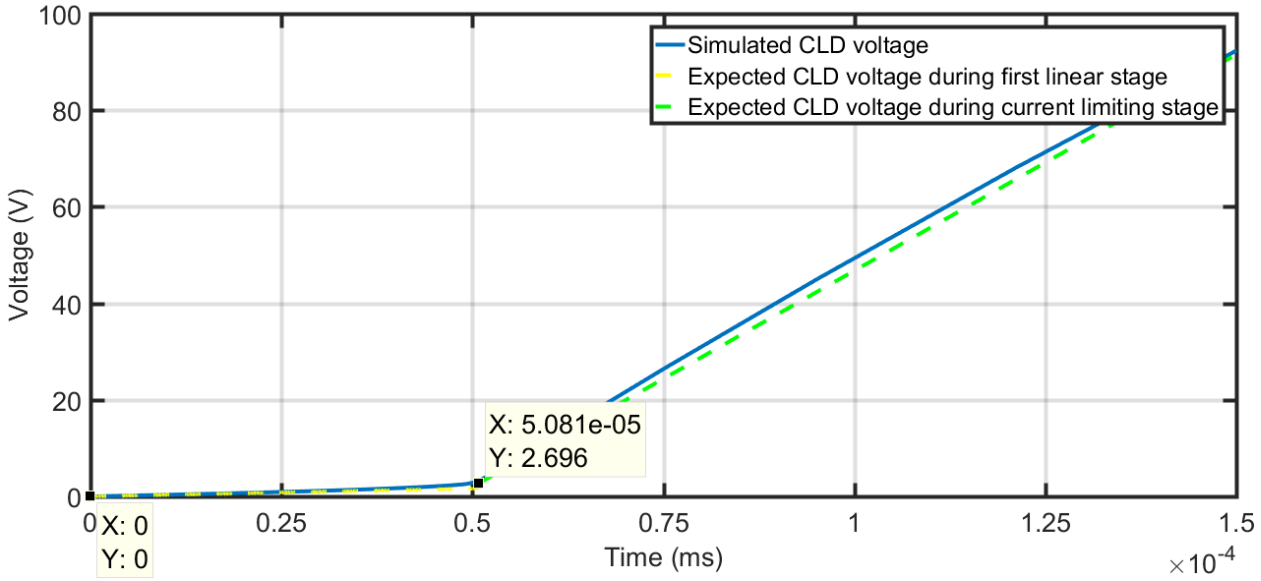


Figure 4.22: Comparison of simulated and expected CLD voltage during first linear stage of a 0.5m line-to-line cable fault condition

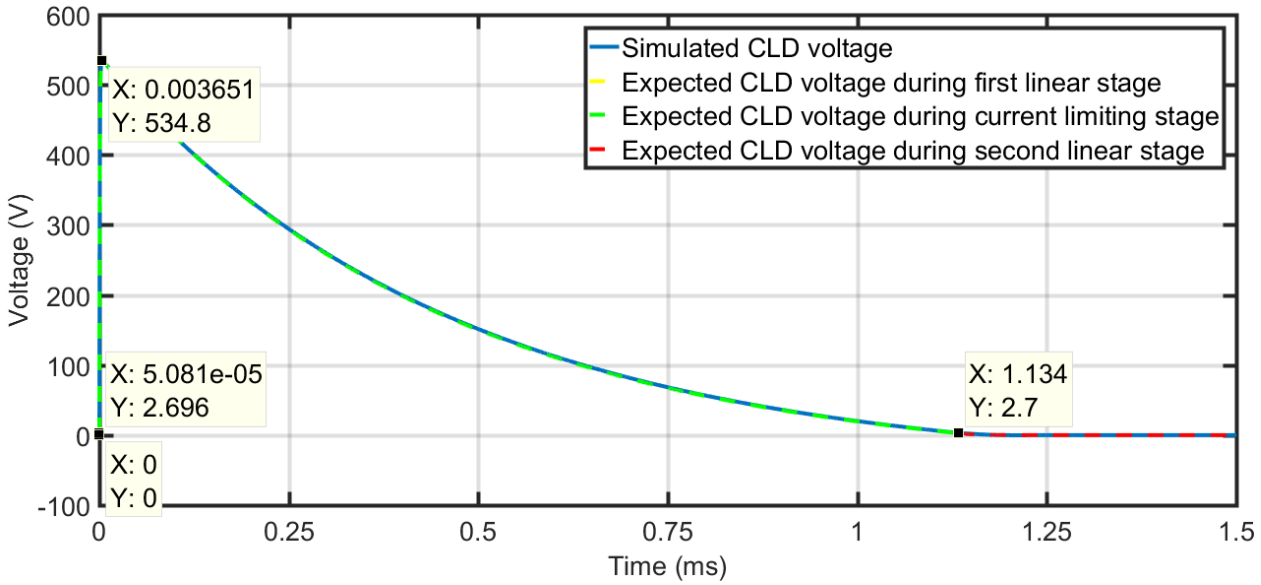


Figure 4.23: Comparison of simulated and expected CLD voltage during full period of the 0.5m cable fault condition

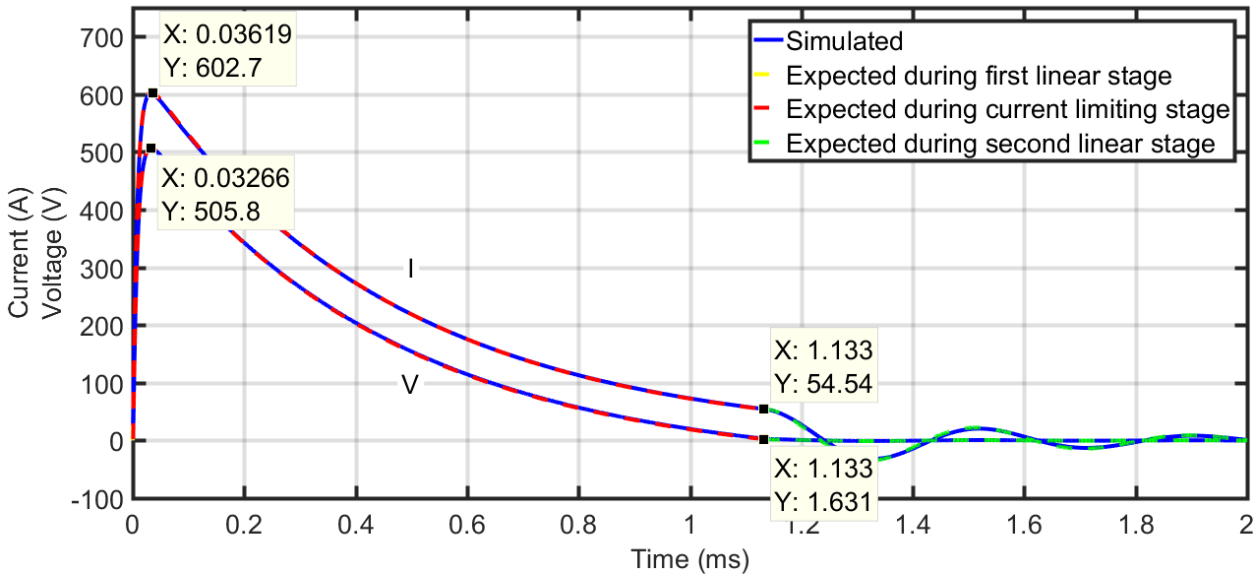


Figure 4.24: Comparison of simulated and expected fault current, and CLD voltage during full period of a 5m cable fault condition

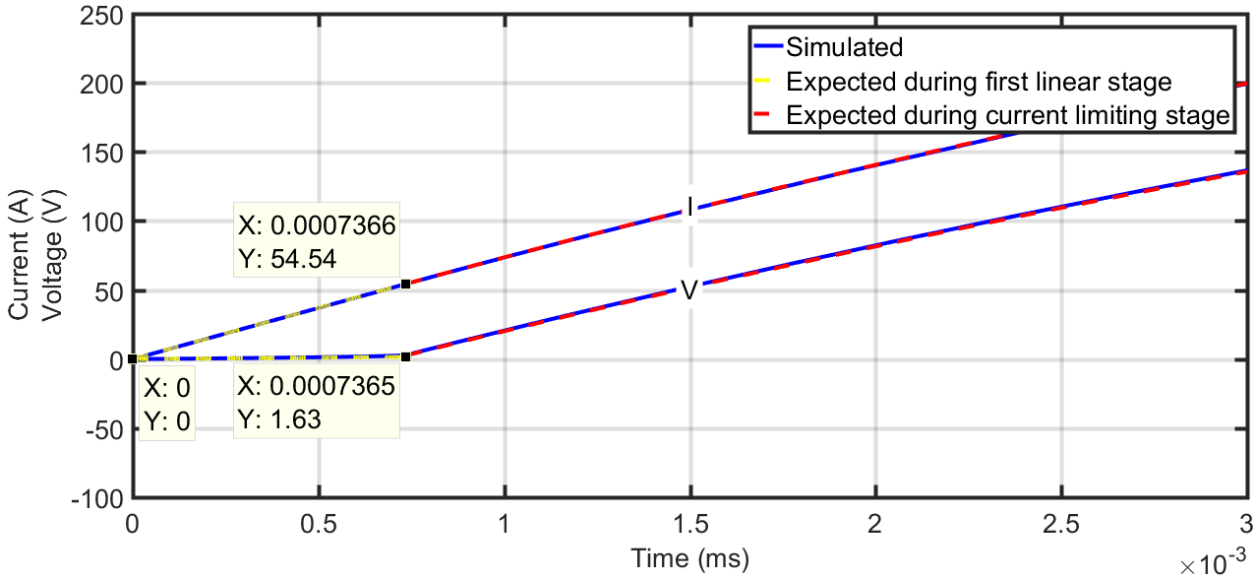


Figure 4.25: Comparison of simulated and expected fault current, and CLD voltage during first linear stage of a 5m cable fault condition

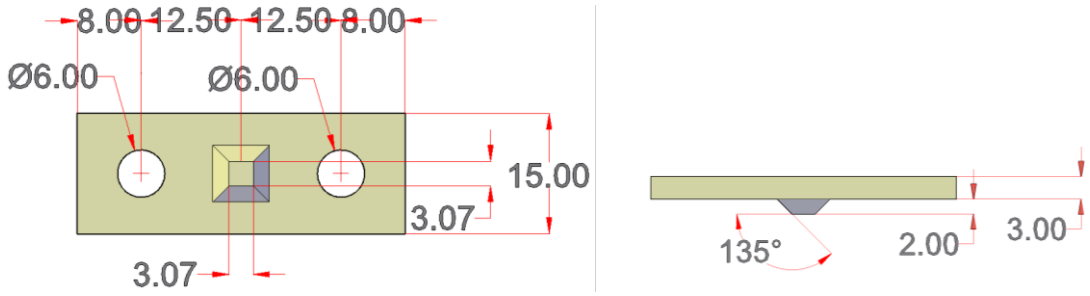
4.4.2. Thermal Condition

A) Extraction of Packaging Thermal Equivalent Circuit

To consider the effects of the CLD's self-heating on the fault response, a certain packaging design must be assumed so that the thermal characteristics of that design can be used. A suitable location

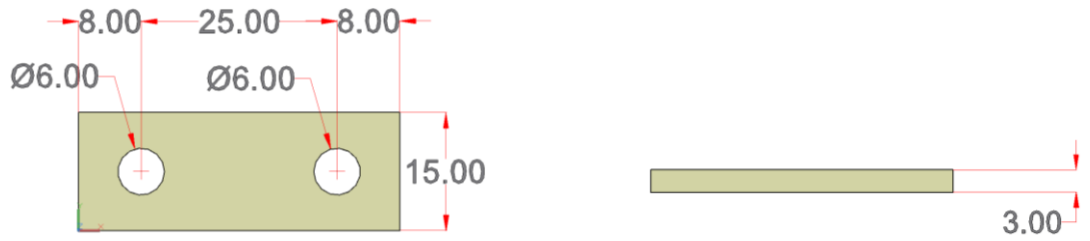
for the CLD in this circuit configuration is to be integrated with the busbars. They can provide a solid structure to support the devices, as well as a thermal mass where the instantaneous energy of the CLDs can be dissipated.

A SiC-JFET die is placed between anode and cathode of the copper structure, shown in Figure 4.26 and Figure 4.27 respectively. Surfaces making contacts with the die are mirror finished and the structure is pressured using two ceramic M6 screws to provide optimal electrical and thermal connections. This approach enables packaging the device without using die attach materials, which degrade the reliability and thermal performance of the devices.



(a) (b)

Figure 4.26: (a) Bottom, and (b) side views of cathode structure

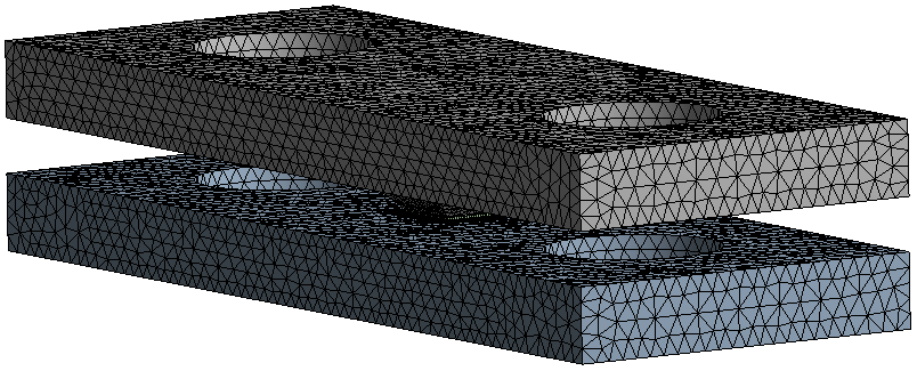


(a) (b)

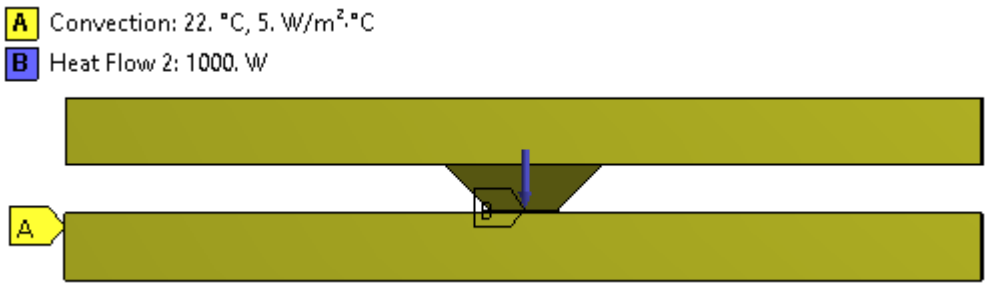
Figure 4.27: (a) Bottom, and (b) side views of anode structure

The structure shown was analyzed in ANSYS to extract its thermal characteristics. The thermal conductivity, specific heat, and density of the die was assumed to be that of 4H-SiC (370 W/m.°C, 690 J/Kg.°C ,3211 Kg/m^3 respectively [15]). As for the copper busbars, the thermal conductivity, specific heat, and density were assumed to be 400 W/m.°C, 385 J/Kg.°C ,8933 Kg/m^3 respectively (from ANSYS's material properties library). A heat load of 1kW was applied to the top surface of the die at *t=0* and a Heat Transfer Coefficient (HTC) of stagnant air given in ANSYS as 5W/m^2

was assumed on the remaining surfaces, as shown in Figure 4.28. This HTC has no influence on the results and was only set to comply with the requirements of the problem setup in ANSYS.



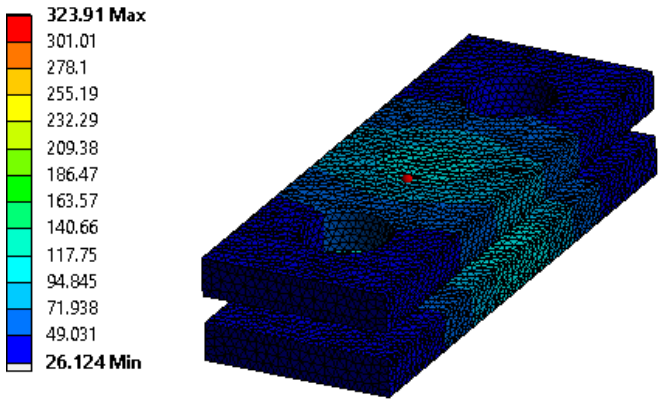
(a)



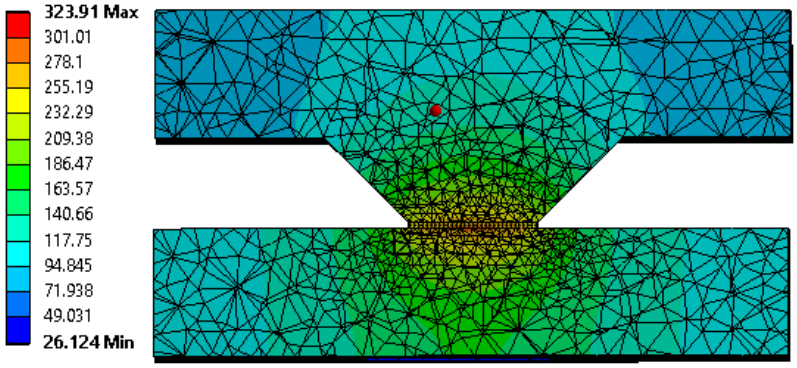
(b)

Figure 4.28: (a) Isometric view of geometry and mesh, and (b) side view of geometry with boundary conditions

The temperature distribution seen by the structure after 0.5 seconds was found as shown in Figure 4.29. A cross-sectional view of the analyzed structure shows a maximum temperature of 352.37°C at the center of the top surface of the die. This is expected as the heat load was applied to that surface. The maximum temperature rise in the structure from the initial temperature of 22°C was found with respect to time as shown in Figure 4.30.



(a)



(b)

Figure 4.29: Temperature distribution in an (a) isometric and (b) cross-sectional view of geometry after 0.5s

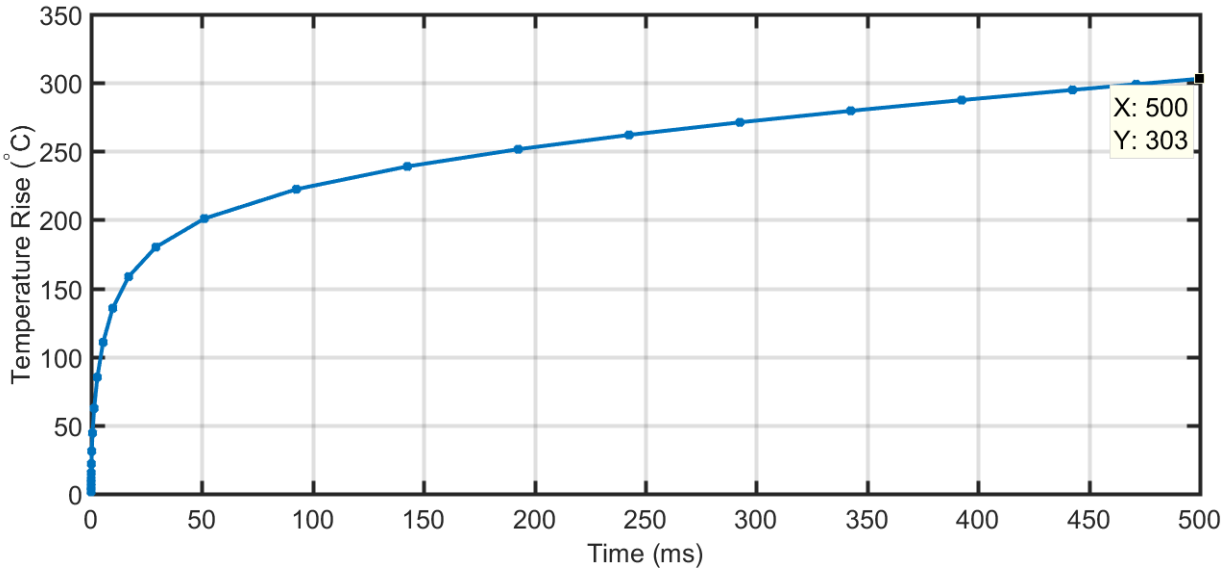


Figure 4.30: Maximum temperature rise in CLD structure vs. time after 1kW heat load at *t=0*

The thermal impedance of the structure was found by dividing the maximum temperature rise by the heat load, as shown in Figure 4.31. A foster thermal network was then curve fitted to this impedance, as compared in the same figure. The RC parameters of the fitted network are given in Table 4.2. The form of the fitted function was given by (2.98).

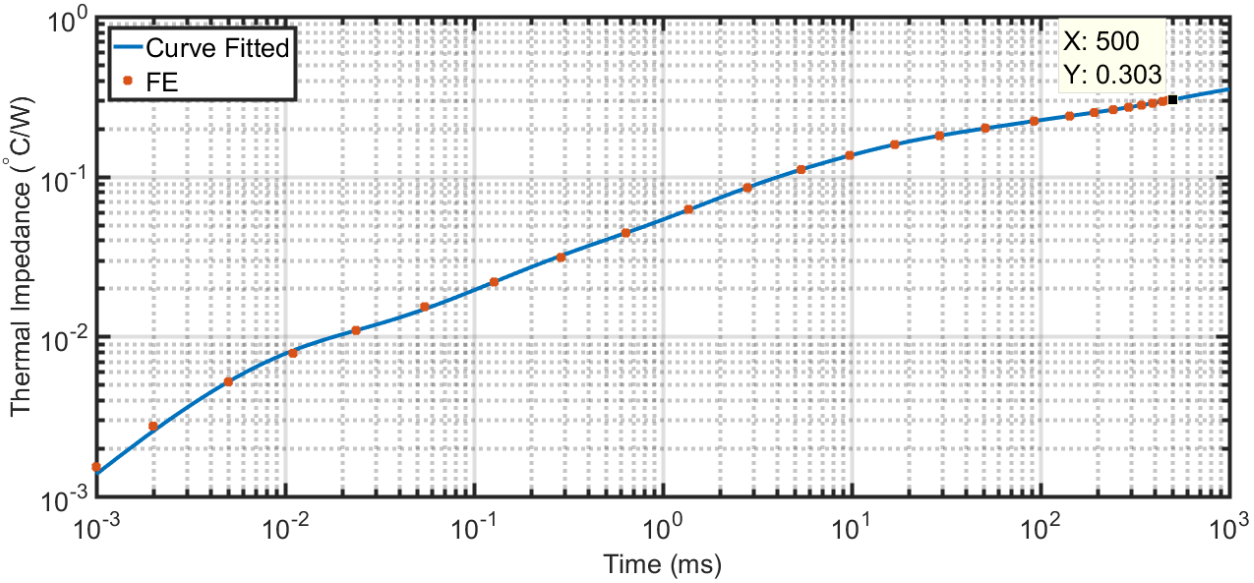


Figure 4.31: FE-based thermal impedance vs. curve fitted foster network impedance

Table 4.2: Foster equivalent thermal circuit parameters

i	R_i (mΩ)	C_i (F)
1	197.9	3.974
2	61.45	0.8
3	79.95	0.1106
4	43.36	0.04063
5	7.717	0.0007475
6	17.31	0.008816

B) Electro-thermal Simulations

This thermal network was then included with the SPICE model of the CLD, as shown in Figure 4.32, for the same simulation parameters used in the isothermal case. The resulting current, voltage, and temperatures of the CLD are shown in Figure 4.33-4.35 respectively.

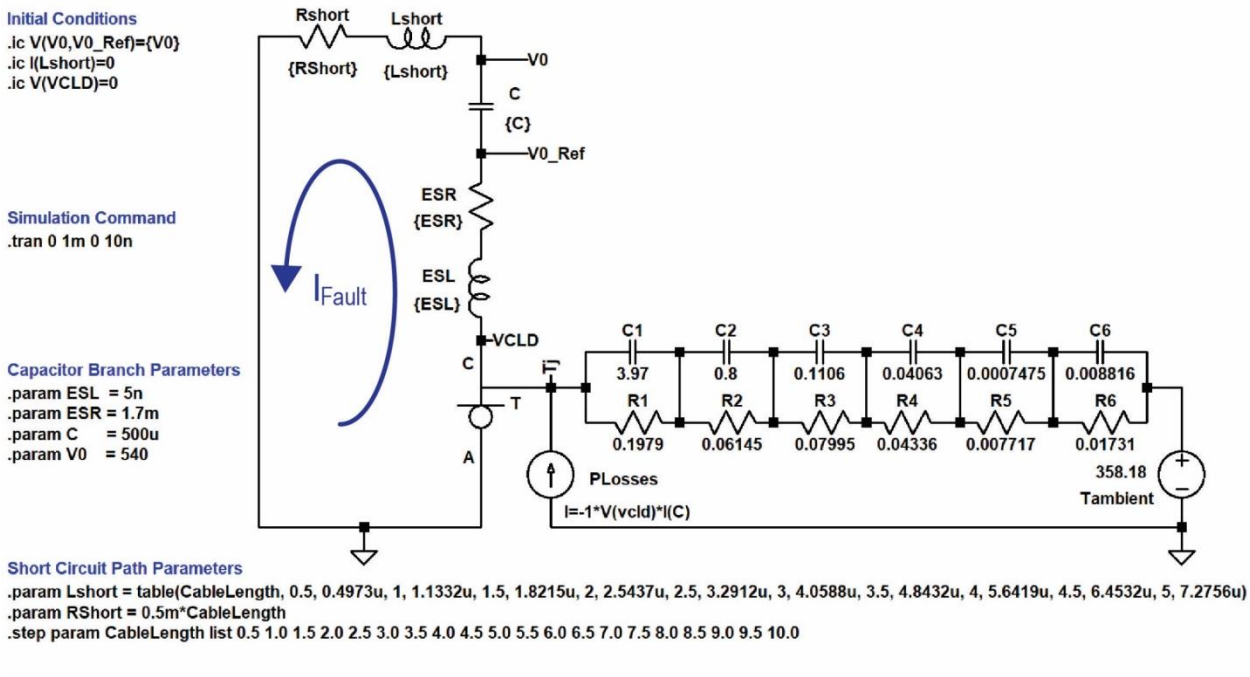


Figure 4.32: Schematic of simulated circuit including thermal effects

As expected, due to the relatively insignificant power loss of the CLD in the first linear stage, current response in that stage is independent of thermal effects, as shown in Figure 4.33. However, as current rises above saturation level (I_{CHSAT0}), power loss become substantial, and thermal effects more apparent. Thermal effects cause the current to be limited at a lower value than in the isothermal condition due to the higher resistance of the CLD when temperature rise is considered. This peak is fault impedance dependent, so that the shorter cables have peaks of larger magnitudes due to their more rapid current rise. After the peak, current falls off to a stable value, with shorter cables having faster decay times. The magnitude at which fault currents stabilize is independent of fault impedances, since the CLD's resistance becomes dominant by that point.

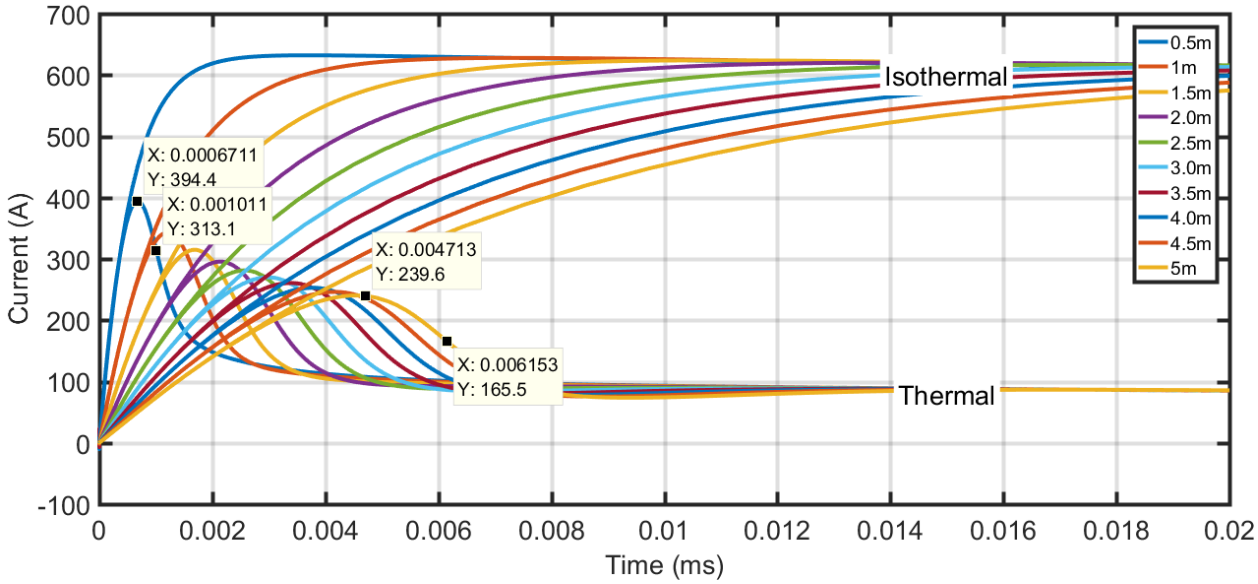


Figure 4.33: Simulated CLD current (I_{Fault}) under line-to-line fault condition with and without thermal effects for cable lengths of 0.5-5m with 0.5 steps

Simulated CLD voltages with and without thermal effects are compared in Figure 4.34. Like the currents, the response under both conditions is identical during the first linear stage due to the insignificant heat generated. During the current limiting stage, large peaks are imposed on the voltages due to heating, which increases in magnitude as cable length increases, despite the currents decreasing in magnitudes. For the 0.5m case, the voltage peaks at 730.1V compared with 1091V in the 5m case (factor of x1.49), despite the current decreasing from 313.1A to 165.5A between the two cases respectively at the same instances in time (factor of x0.528), as shown in Figure 4.33 and Figure 4.34. This is due to the temperatures at those instances being x1.63 time larger in the 5m case (897.6K/550.8K), as shown in Figure 4.35, which results in an increase of the channel region's resistance in saturation (R_{SATeq}) by a factor of x2.77, as shown in Figure 4.36. Therefore, if the increase in resistance is multiplied by the decrease in current, the resulting increase in voltage is x1.463 (2.77x0.528). The increase in the equivalent channel resistance in saturation (R_{SATeq}) accounts for approximately 98% of the increase in voltage, with the remaining 2% contributed to the increase in the equivalent channel voltage drop in saturation (V_{SATeq}) with temperature, as shown in Figure 4.37, and the increase in drift region's resistance shown in Figure 4.36.

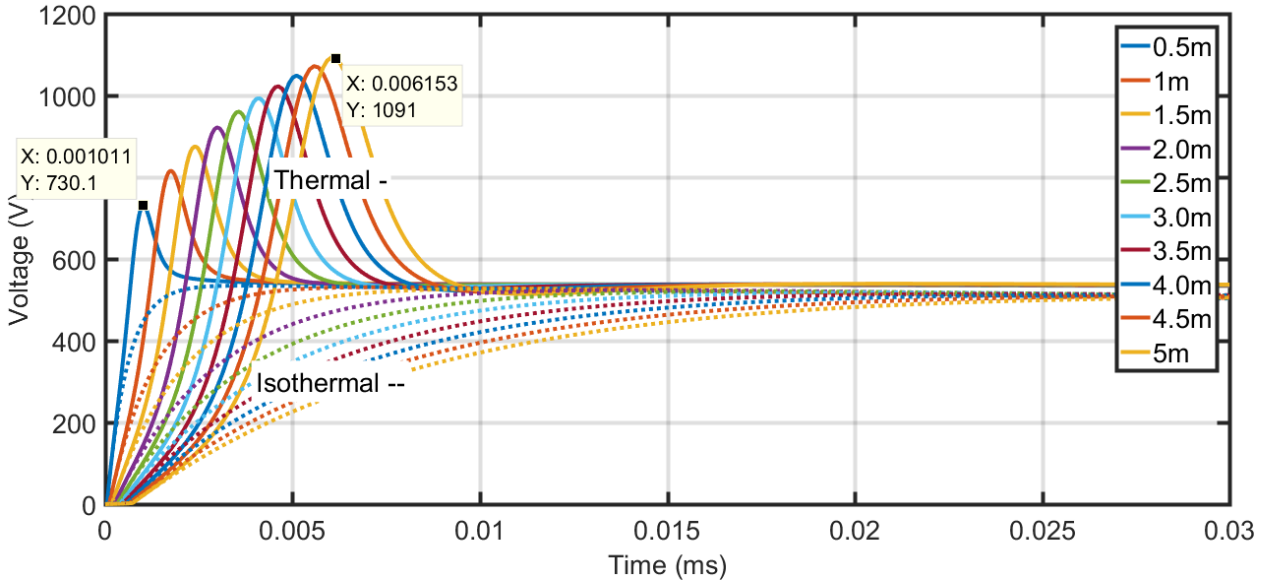


Figure 4.34: Simulated CLD voltage (-*VCLD*) under line-to-line fault condition with and without thermal effects for cable lengths of 0.5-5m with 0.5 steps

Simulated CLD temperatures are shown in Figure 4.35, with minimal increase in temperature during the first linear stage, and a peak that is proportional to cable length in the current limiting stage. Due to thermal capacitances, peak temperatures occur slightly after the peak voltage is reached, which occur slightly after current reaches its peak. For example, in the 5m cable case, the peaks occur at 4.71µs, 6.15µs, & 7.7µs for the current, voltage, and temperature respectively.

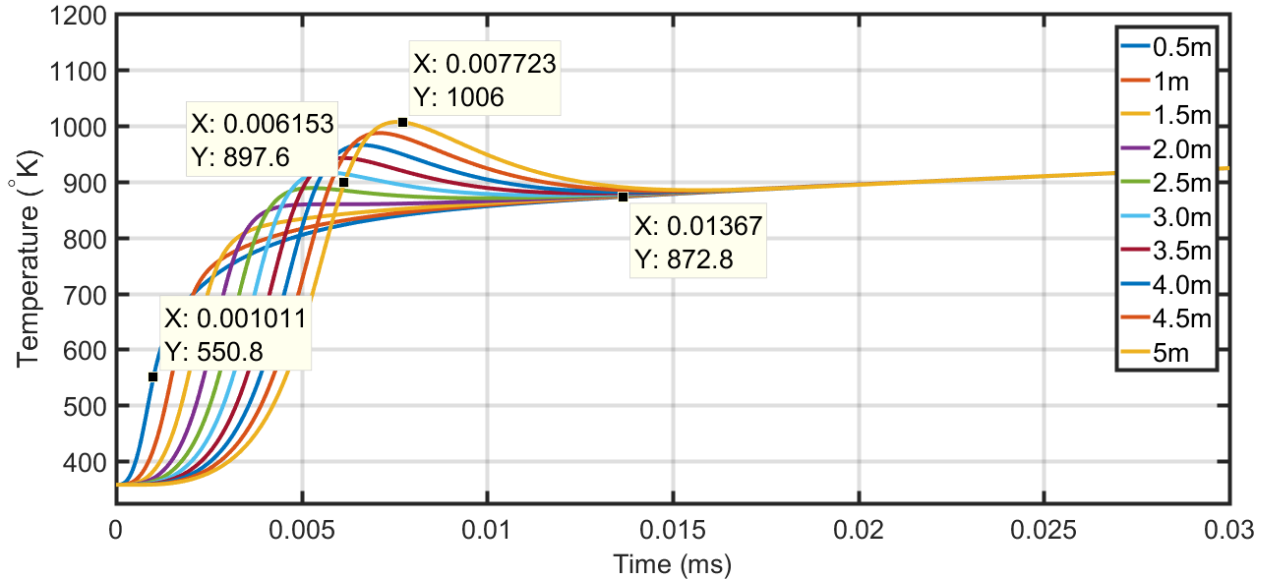


Figure 4.35: Simulated CLD temperature (V(Tj)) under line-to-line fault condition for cable lengths of 0.5-5m with 0.5 steps

The increase in the CLD's equivalent resistive parameters (R_{Drift0} and R_{SATeq}) with temperature are plotted in per-unit scale in Figure 4.36. As shown, the drift region's resistance increases with temperature proportional to electrons mobility (μ) according to (4.10) and (4.25). However, the equivalent resistance in saturation's (R_{SATeq}) increase with temperature is proportional to I_{CHSAT0} per (4.33), which in turn is proportional to both μ and V_{CHSAT0} per (4.22). This results in the value of R_{SATeq} increasing with temperature at a lower rate than μ. Despite that, the value of R_{SATeq} is still x73.84 times that of R_{Drift0} at the highest temperature plotted, validating the approximation made in section 4.3.1 to disregard the contribution of R_{Drift0} in the current limiting stage.

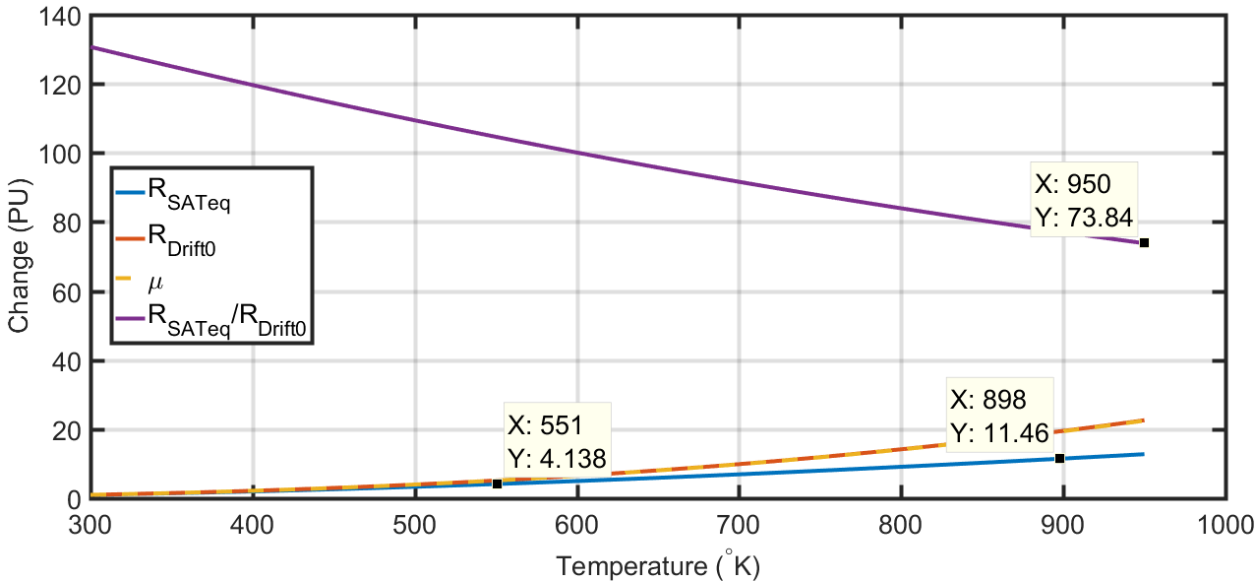


Figure 4.36: Change of CLD resistances in saturation with temperature

Change in the equivalent voltage drop of the CLD computed from (4.32) is plotted against temperature in Figure 4.37, along with the only temperature dependent parameter in that equation (*VDSAT0*). As shown, due to $1/\lambda$ being dominant and independent of temperature in that equation, only minute change with temperature can be observed (< 2% change at 900K compared with 300K).

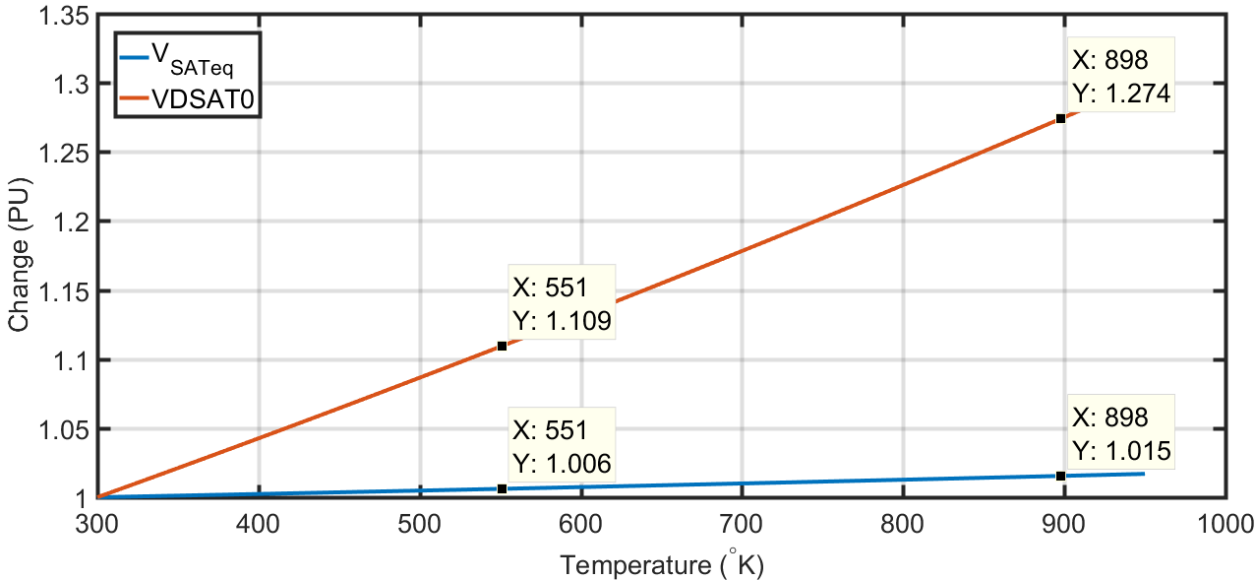


Figure 4.37: Change of CLD equivalent channel voltage drop in saturation (*VSATeq*) and saturation voltage (*VDSAT0*) with temperature

Sensitivity of the time until 500°C junction temperature rise is reached to mesa width (*a*) and fault cable length at an initial DC link voltage of 540V is shown in Figure 4.38. This junction temperature rise limit assumes an ambient temperature of 55°C for aerospace jet engines and some added safety margin. The figure demonstrates that the operational time can be extended to 37µs at the low cable length by reducing the mesa width to 0.575µm. However, this comes at the expense of higher device resistance and lower saturation current, which can lead to higher losses during nominal operation (no fault). Sensitivity of the time until 500°C junction temperature rise is reached to initial DC-link voltages and capacitances is shown in Figure 4.39. It demonstrates that the operational time slightly changes with capacitance but can be drastically extended by reducing the initial DC-link voltage (such as by placing multiple devices is series).

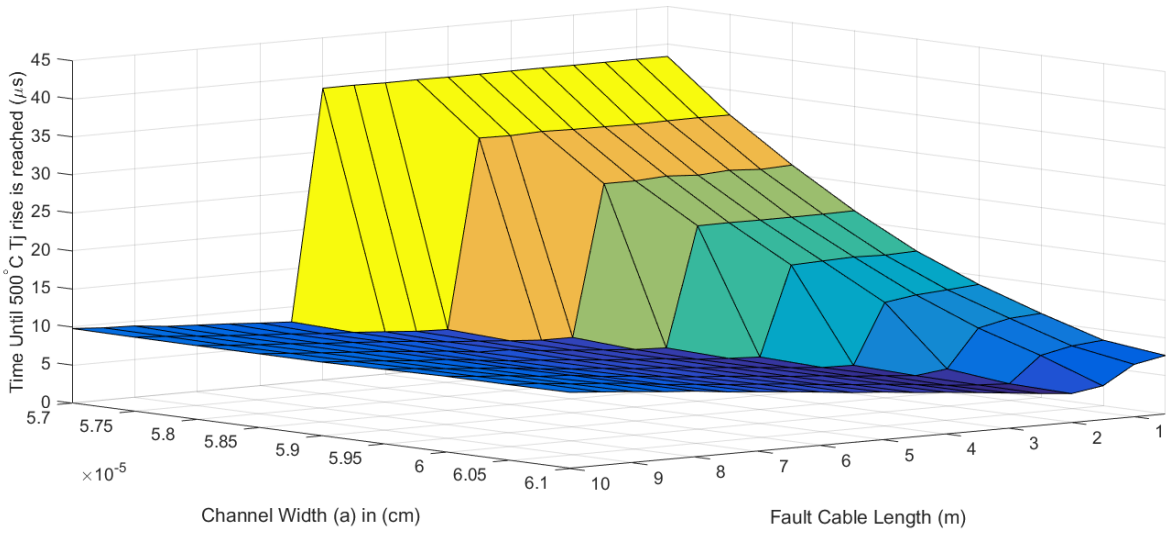


Figure 4.38: Sensitivity of the time until 500°C junction temperature rise is reached to mesa width (a) and fault cable length at V_0=540V

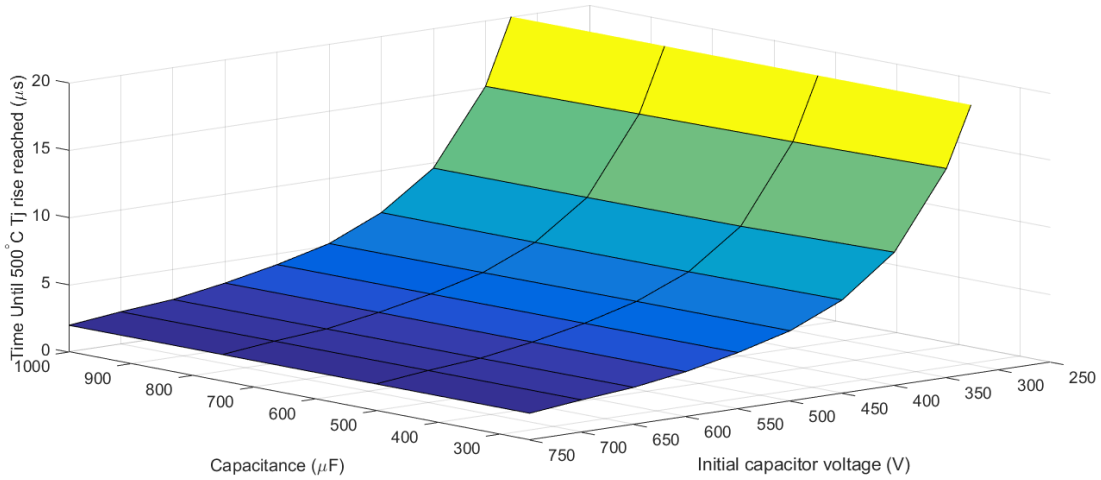


Figure 4.39: Sensitivity of the time until 500°C junction temperature rise is reached to DC-link capacitance and initial voltage (V_0) at mesa width of 0.6µm and cable lengths from 0.5 to 10m

4.5. Conclusions

This chapter demonstrated the feasibility of using SiC-JFETs for short-circuit protection of power converters. This protection technique is passive, requiring no external power or control signals, and dynamic in its response (not binary). Analyses revealed that this device can operate for 10s of microseconds, thus requiring integration with a solid-state circuit breaker which must then isolate the fault. The inclusion of this device enhances the reliability of the system by:

1) Limiting the peak currents components must withstand during a fault.

2) Limiting the amount of inductive energy (I^2L) the solid-state breaker must absorb to isolate the fault.
3) Extending the minimum required operation time of the solid-state breaker from a few microseconds to 10s of microseconds.
4) Preventing false tripping of the breaker by providing more processing/communication time for a fault event to be confirmed and eliminating the need to set low breaker i^2t limit.
5) Eliminating the need to oversize components to withstand high i^2t limits.

4.6. References

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Chapter 5: Silicon Carbide Current Limiting Diode Demonstrator for Short-Circuit Protection of Power Converters

5.1. Introduction

DC line-to-line short-circuit fault conditions typically result in significant amounts of current flow through the system. This current is made up of AC and DC side contributions, as discussed in Chapter 2 and 3. Moreover, DC side contributions were found to be most significant, and thus, the most damaging. Therefore, many schemes have been proposed to protect against DC side fault contributions, by placing current limiting devices in series with the capacitors. The work in [1] suggests the use of an IGBT with anti-parallel diode to implement a "capacitor Solid State Circuit Breaker (SSCB)" which interrupts the capacitor discharge current during a fault. Similarly, the work in [2] proposes embedding a circuit breaker based on Emitter Turn Off Thyristors in series with the capacitor and calls it a "Capacitor DC Circuit Breaker (CDCCB)". Finally, the work in [3] combines an IGBT and a relay to achieve bidirectional capacitor current limiting capability used to limit both inrush and short-circuit currents. Instead of just breaking the current path like the two previous papers, the latter research redirects the fault current to a damping resistor so that the capacitors are fully discharged.

Previous work was focused on using Normally-off switches to interrupt or redirect fault current through a higher impedance path. This chapter demonstrates the use of Normally-ON SiC-JFETs to limit the fault current's magnitude, so that no external gate power or control is required. The energy stored in the capacitors is not isolated or redirected. Instead, it is absorbed by the current limiter and dissipated via heat generation. This is supported by superior robustness of Silicon Carbide JFETs to short energy pulses, as demonstrated in [4, 5].

Silicon based JFETs have been used as constant current sources (current limiters) in low power applications for many years. Recently, Silicon Carbide based JFETs have become more commercially available. These devices have higher voltage capabilities, lower on-state resistances, and can operate at higher temperatures than their Silicon counterparts. This enables their use for new power electronics applications, such as lightning and short circuit protection [6, 7]. Previous research in this field have studied and demonstrated the benefits of using SiC-JFETs as current

limiters for lightning protection [8, 9]. This work takes advantage of the devices current limiting capabilities to demonstrate a passive protection approach from short-circuit faults in power converters.

This chapter presents the design, building, and testing of a current limiting diode demonstrator for short-circuit faults protection. This demonstrator utilizes a commercial off-the-shelf Silicon Carbide Junction Field Effect Transistor (JFET) with the gate and source terminals externally connected, as discussed in Chapter 4. The SiC JFET die is integrated into a custom designed high temperature package in the circuit configuration shown in Figure 5.1. The die is pressure contacted by a copper busbar acting as the electrical connections (cathode and anode) and thermal masses for the heat generated by the CLD to be dissipated to.

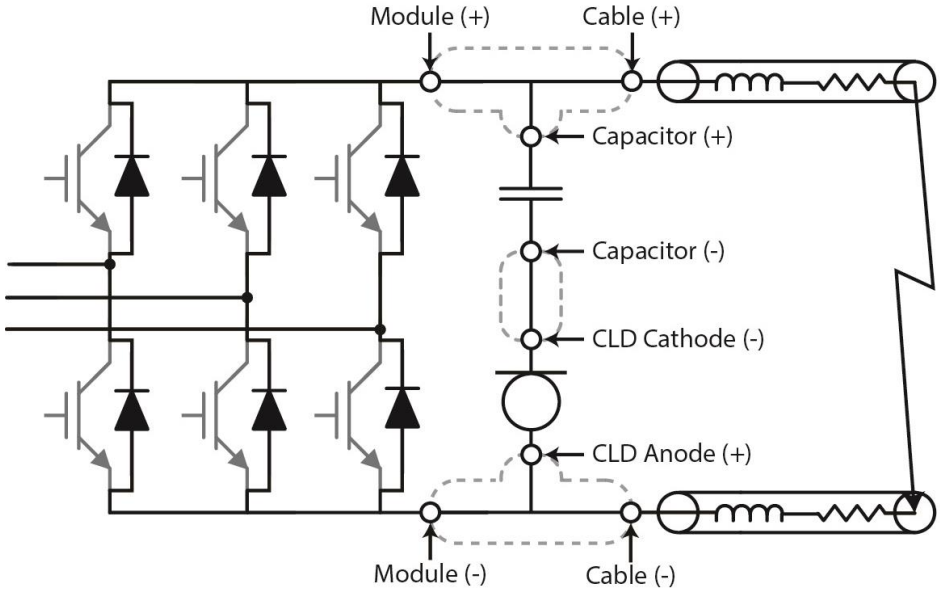


Figure 5.1: Location of current limiter in converter circuit, with busbars circled by dashed lines

The second section of this chapter details the design of the current limiter, including components selection and performance analyses. The third section details the components of the CLD, assembly and integration of the CLD into the converter. The fourth section presents the experiment setup for CLD testing and results obtained from this setup. This section also includes comparisons of measurements with simulations and with expected fault response without a CLD. Finally, the fifth section summarizes the outcome of this work, including the benefit of the demonstrated device.

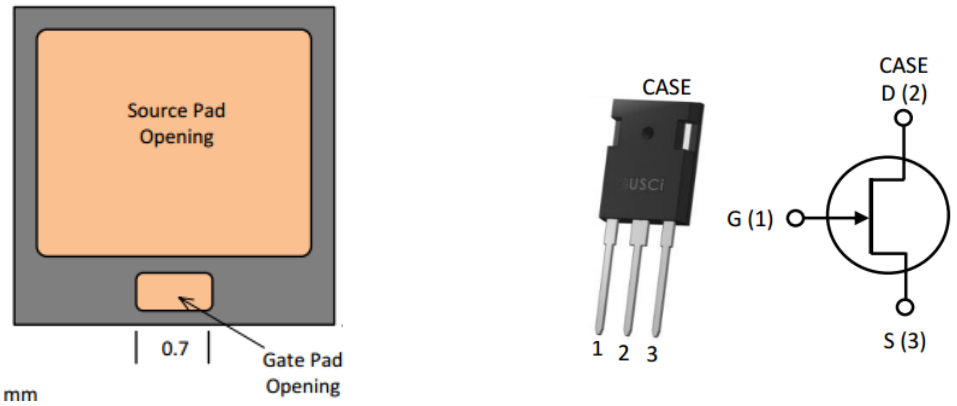
5.2. Design

This section details the design of the current limiting diode demonstrator, including components selection, and performance analyses. The performance analyses encompass generating a SPICE model of the current limiter including thermal effects. This model is then simulated with an equivalent circuit of the converter under a DC line-to-line short-circuit fault condition. The simulation results are used to demonstrate the capability and functionality of the current limiter.

5.2.1. Components Selection

A) Semiconductor Devices

The design utilizes a commercial off-the-shelf Normally-ON Silicon Carbide Junction Field Effect Transistor (JFET) from United Silicon Carbide (USCi) [10]. This manufacturer offers dies rated of 45mΩ [10] and 80mΩ [11] maximum ON-state resistances at 25°C, with a voltage rating of 1.2kV. The devices are offered directly from USCi in die and plastic packaged forms, as shown in Figure 5.2 (a) and (b) respectively. The dies are rated for continuous operation temperatures of up to 250°C, whereas the plastic packaged devices are rated for a maximum of 175°C. Transiently, the dies are marketed to be capable of withstanding a peak temperature of more than 600°C, limited by the melting point of the aluminum gate and source metallizations [12]. To achieve maximum fault limiting capacity, the 45mΩ devices were used in die form, in combination with a custom high temperature packaging solution that will be discussed in the next section.



(a) (b)

Figure 5.2: Picture of USCi JFETs in (a) die and (b) plastic packaged forms [10, 13]

These devices are also offered in hermetically sealed packages with isolated flanges from Micross Components Inc., as shown in Figure 5.3. Despite the use of metal casings, the maximum operation temperature of these devices is still limited to 175°C [14]. Therefore, these devices were not selected for this demonstrator.

(a) (b)

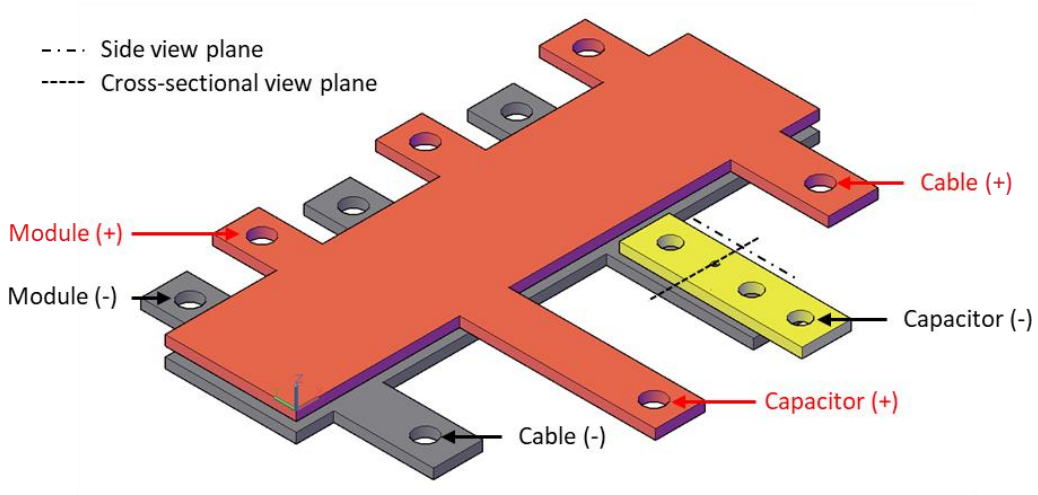
Figure 5.3: (a) Picture and (b) pinout of hermetically sealed metal-can packaged SiC JFETs from Micross Components [14]

United Silicon Carbide devices are the only available Normally-ON SiC JFETs in the market. Historically, devices were offered from two other manufacturers: Infineon Technologies AG and SemiSouth Laboratories. SemiSouth devices came in 85mΩ and 45mΩ ON-state resistance ratings at 25°C, and 1.2kV voltage blocking capabilities [15, 16]. They were discontinued after the company's closure in 2012. Infineon Technologies AG released their line of CoolSiC JFETs in 2012 with ON-state resistance ratings of 70mΩ and 100mΩ at 25°C and 1.2kV blocking capabilities [17, 18], discontinued in 2016.

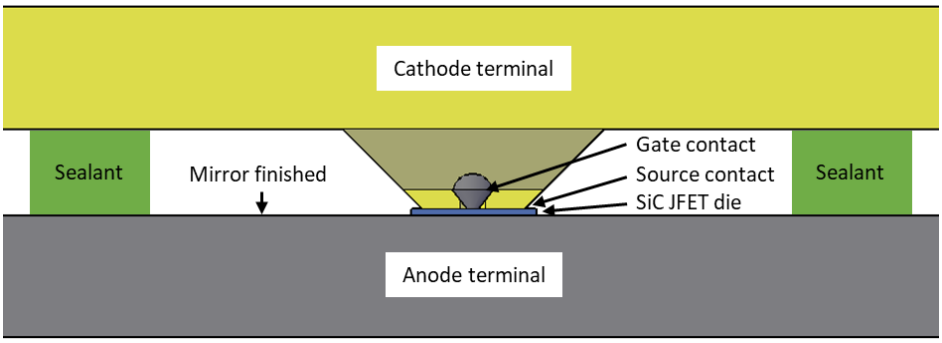
B) Custom High Temperature Packaging

To reach the maximum operation temperature potential of the dies (>600°C), a custom packaging solution was developed. The SiC JFET die is integrated with the copper bus bars, as shown in Figure 5.4, without the use of die attach materials or wire bonds which degrade the reliability and thermal performance of the devices [19]. Instead, the die is sandwiched between top and bottom copper structures acting as the electrical Cathode (Source and Gate) and Anode (Drain) connections respectively, as shown in Figure 5.5, held together only by pressure. In addition to establishing the electrical conduction paths, the copper structures represent thermal reservoirs for the instantaneous heat generated by the CLD to be stored in. Copper was selected due to its

availability, ease of machining, high thermal and electrical conductivities, and moderate specific heat capacity. Materials with higher specific heat capacities are available. However, they have lower thermal conductivities resulting in less utilization of the overall thermal mass, and are more difficult to manufacture in the desired form.



(a)



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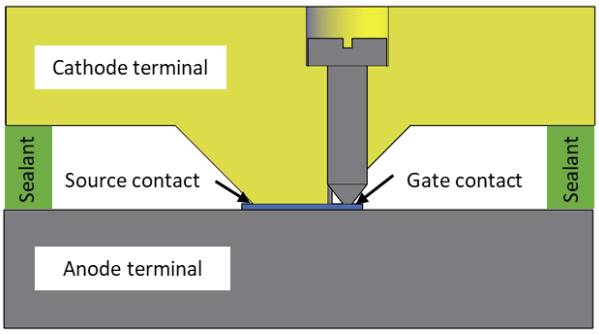


(c)

Figure 5.4: (a) Isometric, (b) side and (c) cross-sectional views of current limiter's package

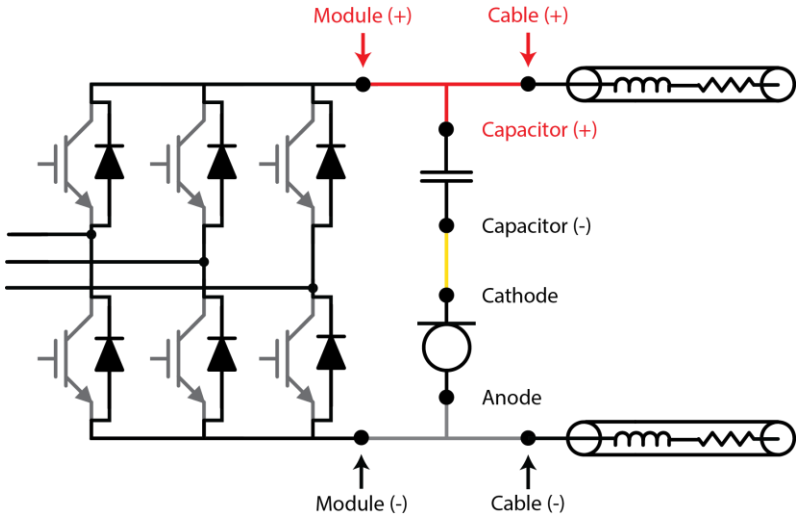


Figure 5.5: Schematic of current limiter package's electrical connections

Contact with the top side of the die were limited to the gate and source pad regions. Connection to the source terminal was achieved by sizing the lower cathode terminal's surface to be slightly smaller than the source pad's area. An end tapered M1 brass screw was utilizing to connect to the gate pad, as shown in Figure 5.4. All surfaces contacting the die were mirror finished to improve the thermal and electrical contacts, as well as provide some ability for the die to slide against the copper without causing substantial damage.

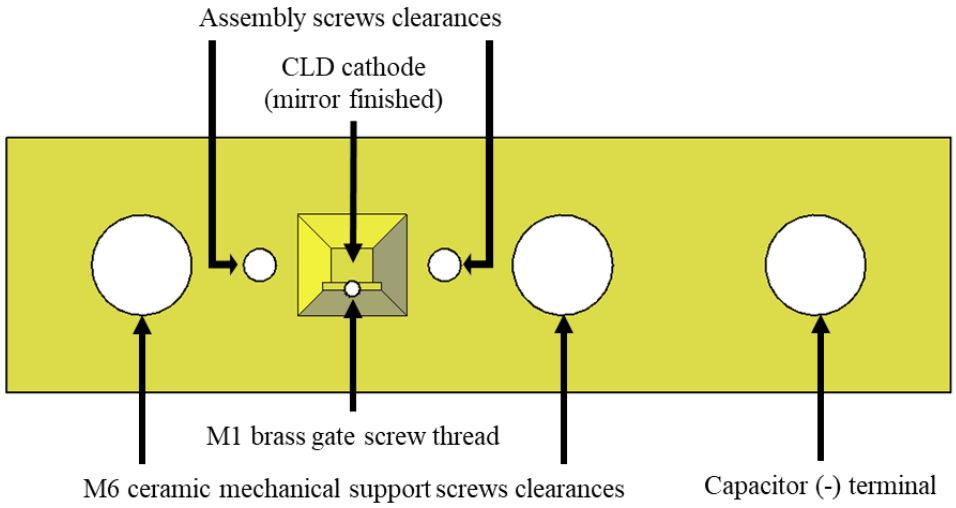


Figure 5.6: Bottom side view of cathode structure

The structure was mechanically supported by two M6 ceramic screws [20] shown in Figure 5.7, on each side of the die. Ceramic screws were selected to maintain electrical isolation between the cathode and anode terminals without increasing the complexity of the structure.

Figure 5.7: Picture of M6 ceramic screw [20]

The die from was protected from debris using a high temperature sealant [21] around the edges of the structure and in assembly holes, as shown in Figure 5.5. This sealant is capable of a maximum temperature of 300°C. Finite element analysis of this test fixture is shown in the next section.

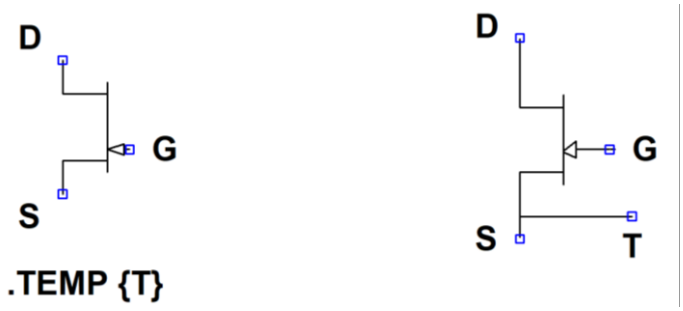
5.2.2. Performance Analyses

This section presents performance analyses carried out to demonstrate the capability and functionality of the designed CLD. It included details of simulations models not previously used in this thesis, and results of simulation analyses carried out with various DC line-to-line fault impedances, and initial DC-link voltages.

A) Semiconductor Device SPICE Model

The semiconductor die manufacturer provides electro-thermal SPICE models of the devices that empirically account for physical phenomena. These models are fitted for the typical applications of the devices in switched mode power supplies and motor drives. Thus, they have limited accuracies above the maximum rated steady-state junction temperature of the packaged devices (175°C) and are not functional above approximately 360°C junction temperatures. Furthermore, their accuracies degrade when used in the saturation region (current limiting), as noted by the device SPICE script given in Appendix B. To overcome these limitations, the simulation space was bounded so that the junction temperature of the devices is maintained within the model's limits (T_j < 360°C). Furthermore, the obtained simulation results were only used to investigate the general characteristics, and not to find the exact values of currents, voltages, or temperatures.

Another limitation of the manufacturer's models is due to the method used to define the junction temperatures of the devices. The temperature is set using a ".TEMP" SPICE directive which is executed at the beginning of a simulation. This directive sets the junction temperature to a fixed value throughout the simulation (isothermal), and does not allow for the inclusion of a thermal equivalent circuit to account for temperature dynamics. This limitation was overcome by modifying the models so that the junction temperature is defined as the voltage at a forth model terminal (T), in addition to the Gate (G), Source (S), and Drain (D), as shown in Figure 5.8 (b). The modifications made to the SPICE models definitions are provided in Appendix B. Comparison of the output characteristics obtained from the original and modified models at multiple junction temperatures are shown in Figure 5.9 and demonstrate identical characteristics.



(a) (b)

Figure 5.8: Symbols of (a) original manufacturer SPICE model and (b) modified model

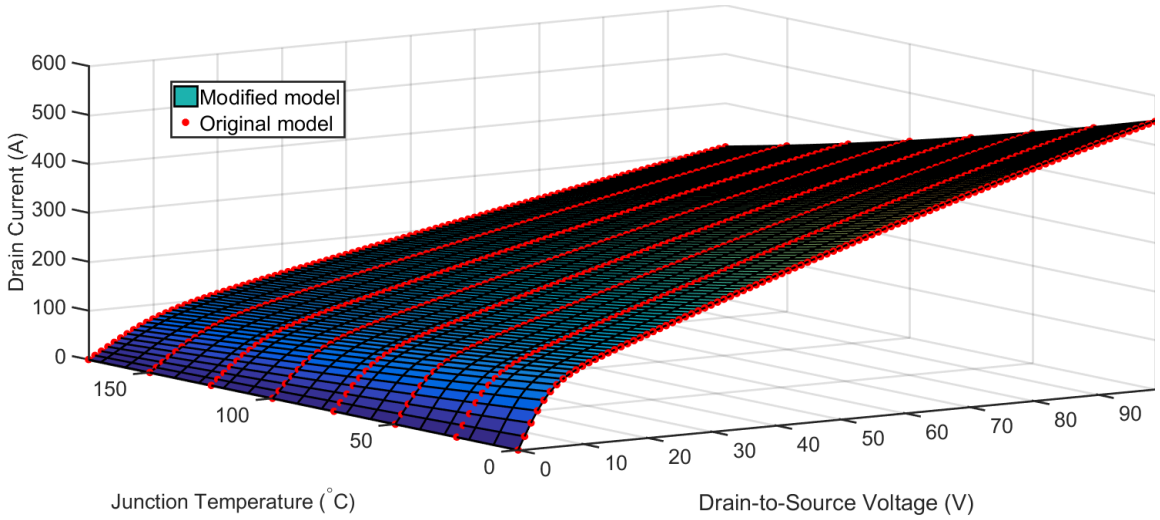


Figure 5.9: Comparison of output characteristics obtained from original and modified models

B) Packaging Thermal Equivalent Circuit SPICE Model

To generate an equivalent thermal model of the current limiter, the device was analyzed using ANSYS finite element software in the transient thermal simulation setup, shown in Figure 5.10. Areas where heat is not expected to reach have been removed to accelerate the solution process. This includes areas of the busbars distant from the die, as well as the gate contact. A heat load step of 1kW is applied to the bottom surface of the die at time 0, and a convection coefficient of 5W/m^2 for free air was applied to all other surfaces to comply with the problem setup requirement for heat sink surfaces to be present. Due to the minute value of this coefficient, it is not expected to influence the results.

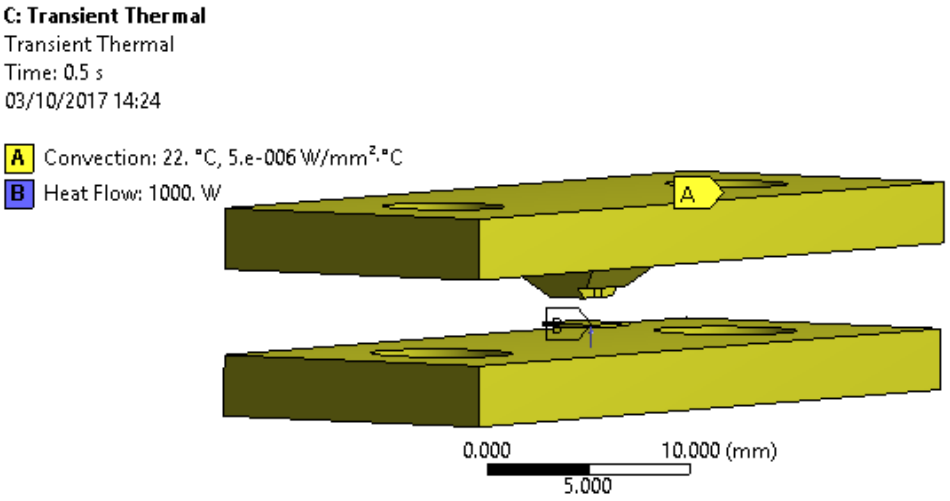


Figure 5.10: ANSYS transient thermal analysis geometry and problem setup (exploded)

The maximum temperatures recorded on the die vs time are shown in Figure 5.11. A thermal cross-section at 0.5s is shown in Figure 5.12. Comparing these results with those obtained from the geometry analyzed in Chapter 4, an increase in the maximum temperature in observed due to the smaller contact area of the cathode structure, and thus surface area for heat to be extracted from. In addition, higher non-uniformity in the temperature distribution of the die can be observed in this geometry, due to lack of cathode contact area near the gate pad's region, as shown in Figure 5.12.

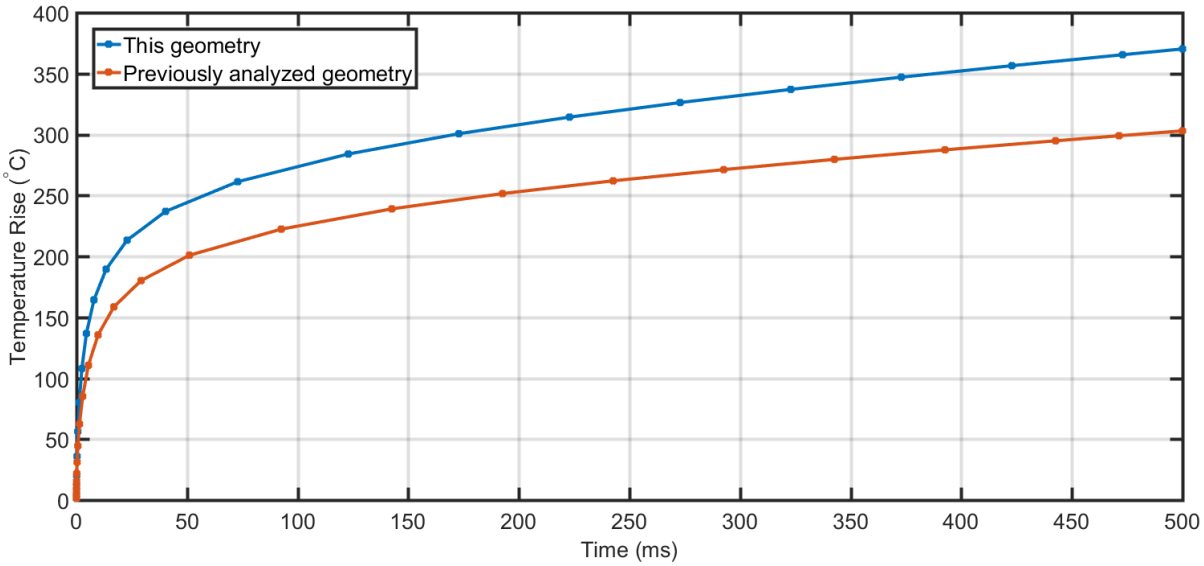


Figure 5.11: Maximum temperature rise recorded on die vs. time

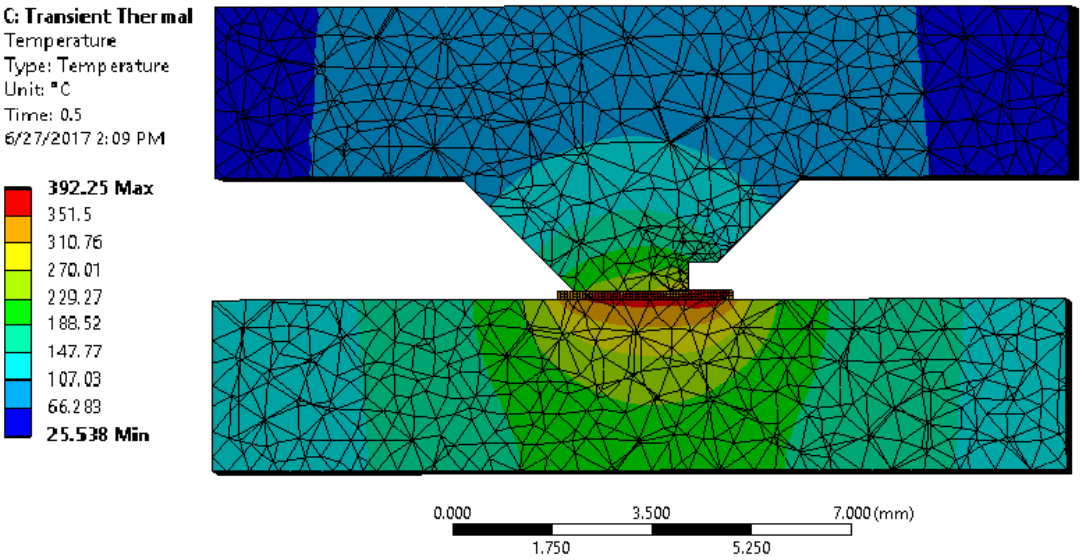


Figure 5.12: Temperature distribution at 0.5 seconds

The thermal impedance characteristic of this structure is shown in Figure 5.13. The results were then curve fitted to a 6-level equivalent foster thermal network with the *R* and *C* parameters given in Table 5.1. Curve fitted thermal impedance is compared to that obtained from finite element in Figure 5.13.

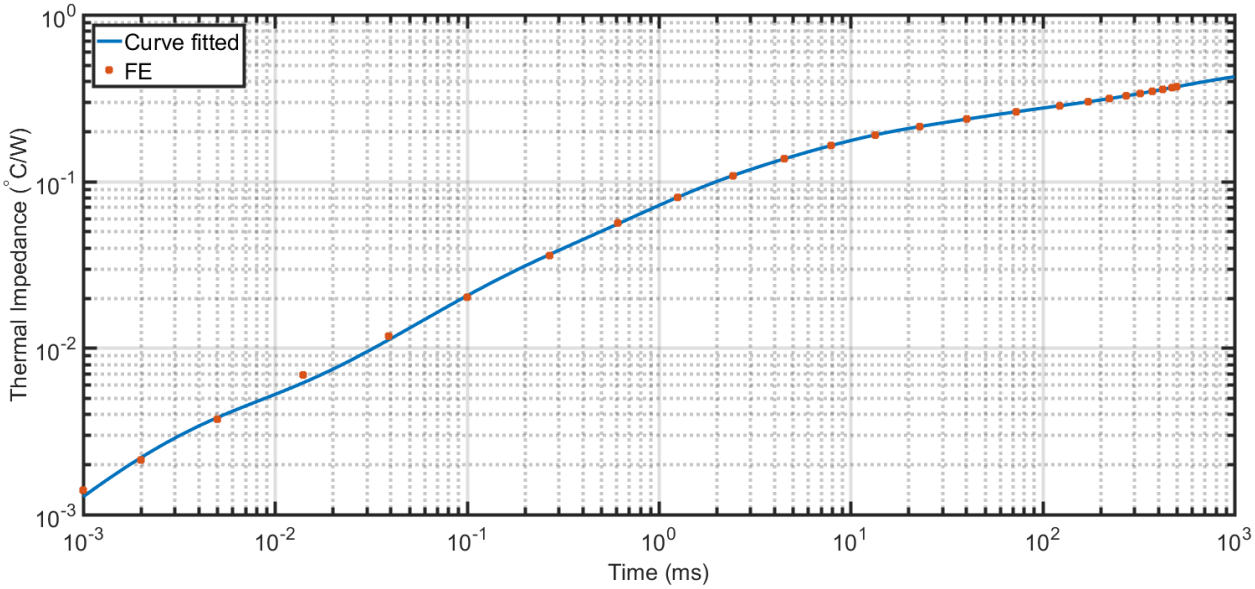


Figure 5.13: Thermal impedance vs pulse time

Table 5.1: Equivalent foster thermal network parameters

i	C_i (F)	R_i (Ω)
1	0.0007818	0.003
2	0.01862	0.05569
3	0.0618	0.09662
4	0.006005	0.0169
5	2.77	0.2206
6	0.4827	0.07441

C) SPICE Simulations

Given the generated device model and packaging equivalent thermal network, the current limiter was simulated as part of an equivalent fault circuit, as shown in Figure 5.14. In addition to the current limiter, the circuit also includes models for a capacitor (*C*), its Equivalent Series Inductance and Resistance (*ESL* and *ESR* respectively), and fault inductance and resistance (L_{short} and R_{short} respectively). So that the general characteristics obtained from this simulation can be compared to

those found in Chapter 4, the same capacitor and fault parameters were used. Like simulations carried out in Section 4.4, the initial output current was set to 0A and ambient temperature (V_a) to 85°C. However, the initial capacitor voltage was limited to 100V due to the JFET model's maximum operation temperature limitations discussed earlier. Simulated CLD current, voltage, and temperatures are shown in Figure 5.15 - Figure 5.17 respectively.

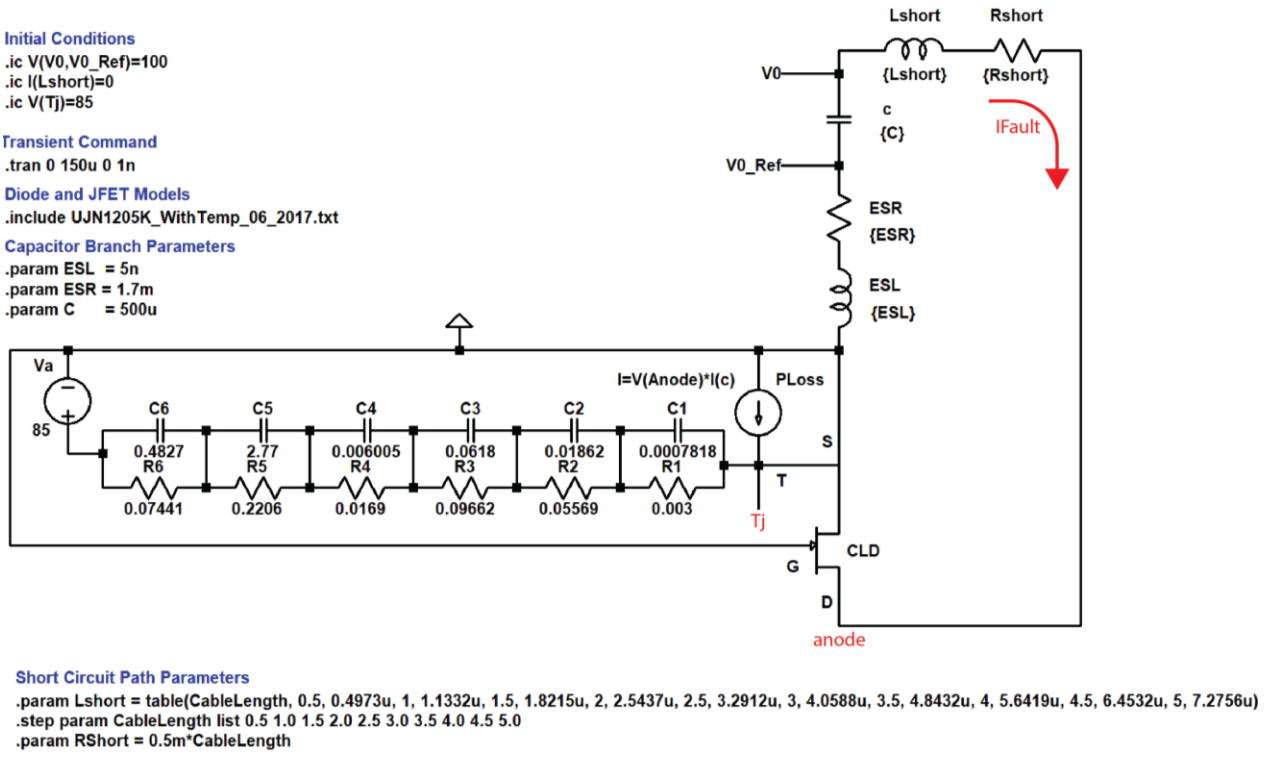


Figure 5.14: Current limiter performance simulation circuit

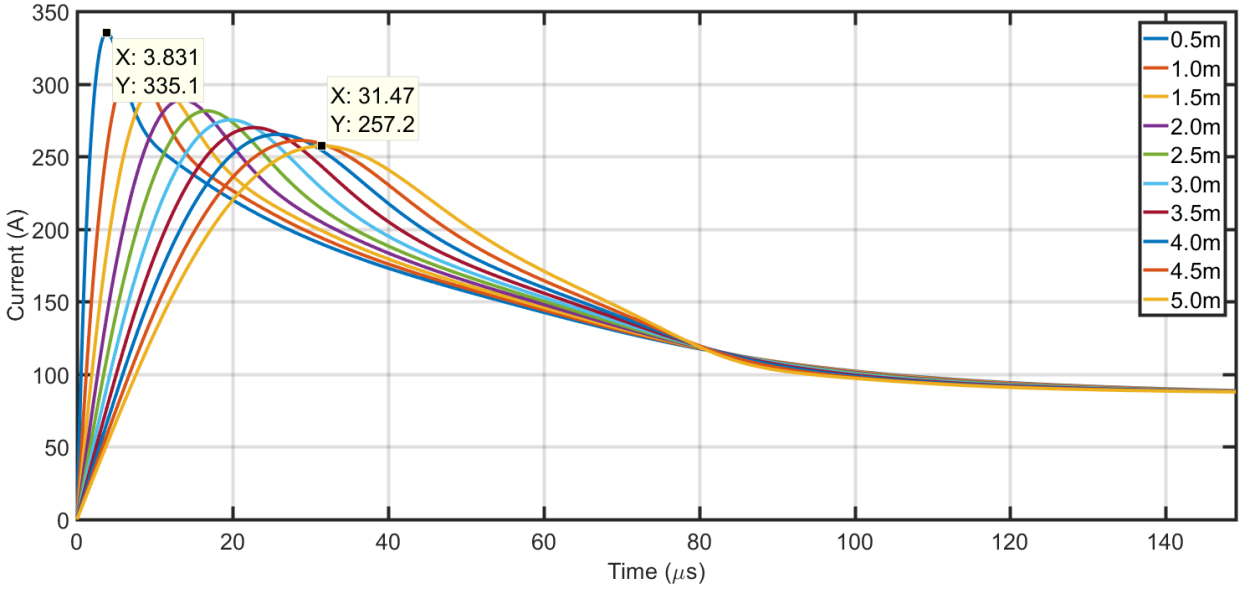


Figure 5.15: Simulated CLD/fault current (IFault)

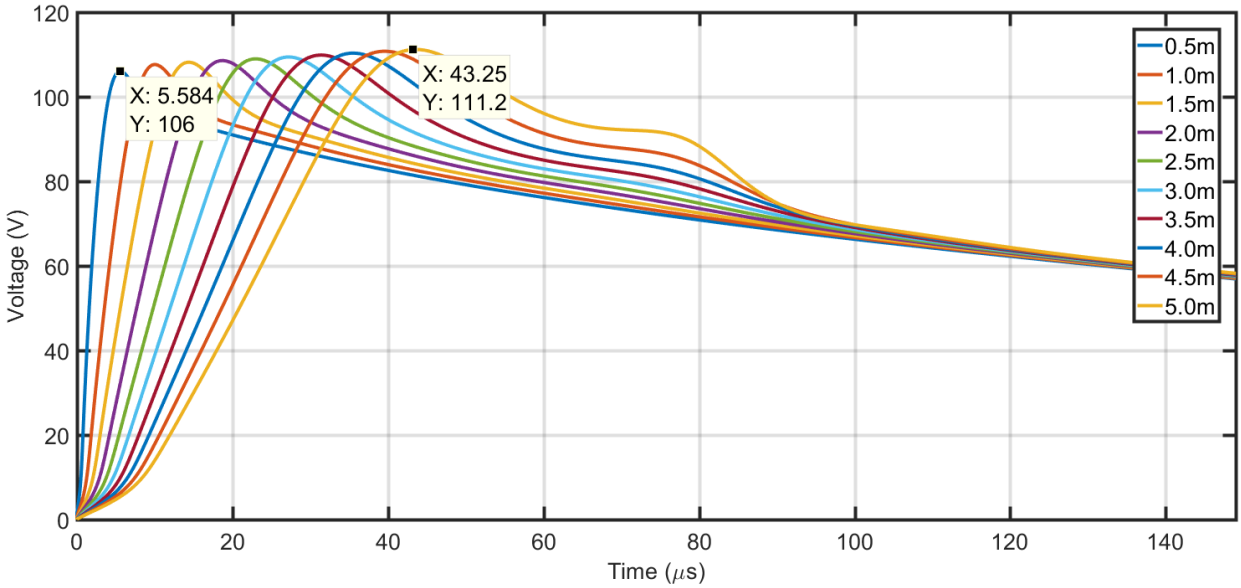


Figure 5.16: Simulated CLD voltage (V(anode))

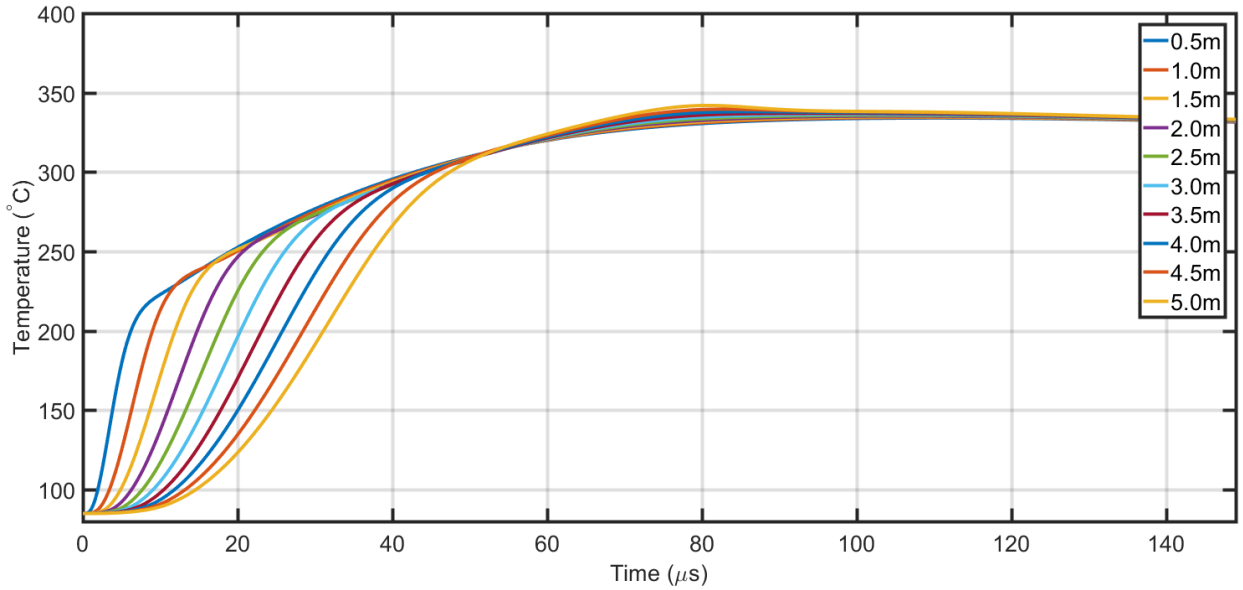


Figure 5.17: Simulated CLD temperature (V(Tj))

The general characteristics of the simulation results are as expected from the analysis carried out in Chapter 4. Current rises rapidly from its initial value with an initial slope that is inversely proportional to cable inductance. The current reaches a peak whose magnitude is also inversely proportional to cable length. Current then decays until reaching a point (around 80μs) when it becomes approximately independent of cable length. The voltage and temperature also follow expected characteristics, as detailed in Chapter 4. This simulation demonstrates that the circuit is responding as expected from previous analyses.

Further simulations were carried out with a more detailed circuit that includes the diode rectifier and a fault switch equivalent circuit. Converter diodes (*D1-D6*), DC capacitor (*C*, *ESR*, & *ESL*), and cable (L_{short} & R_{short}) parameters used in this simulation are identical to those of the experiment setup, as discussed in Chapter 3. The setup was only modified to use an Insulated Gate Bipolar Transistor (IGBT) based fault switch instead of Thyristor-based. Therefore, parameters representing the voltage drop across the fault switch (V_{IGBT}, and R_{IGBT}) in this simulation are different from those used in Chapter 3, as found in Section 5.4.1. . Like previous simulations, the initial output current is set to 0A. However, the ambient temperature (V_a) was set to 22°C. These represent more realistic conditions, under which the CLD will be tested experimentally.

Unlike previous simulations where the initial capacitor voltage was fixed and cable parameters varied, the cable impedance is fixed in this simulation to the value found in Chapter 3 for the

experiment setup, and initial capacitor voltages varied at 50, 100, 150, 200, 250, 270 volts. For initial voltages of 150, 200, 250, and 270 volts the JFET model exceeds its maximum operation temperature of approximately 360°C before the end of simulation at 84.6, 33.8, 9.9, and 8.9µs respectively, as shown in Figure 5.19-Figure 5.21. For comparison, simulation results obtained without the current limiter in the circuit are also shown.

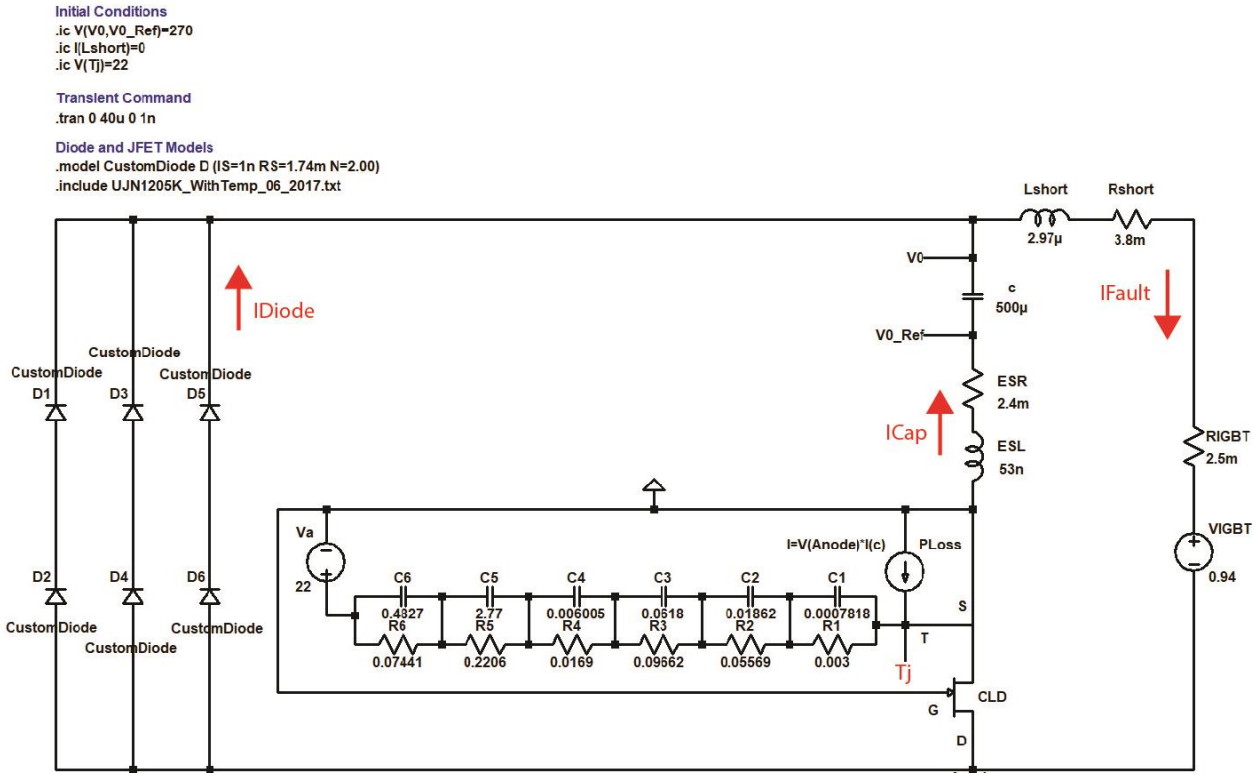


Figure 5.18: Current limiter performance simulation circuit including converter diodes and fault switch equivalent circuit (showing V_0 = 270V case)

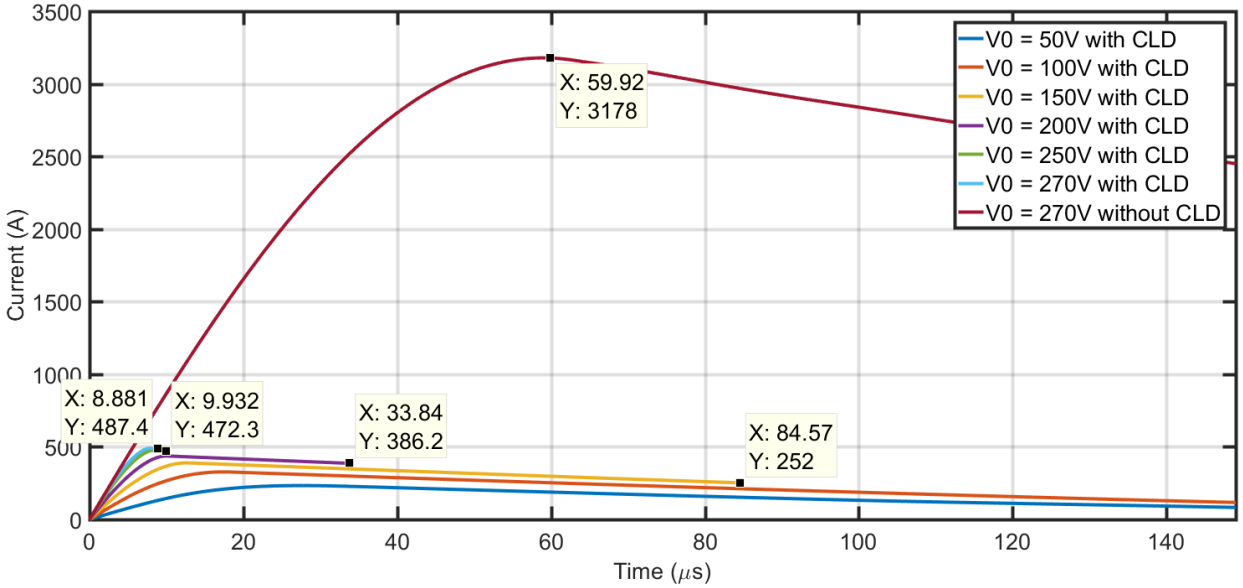


Figure 5.19: Simulated fault current (IFault)

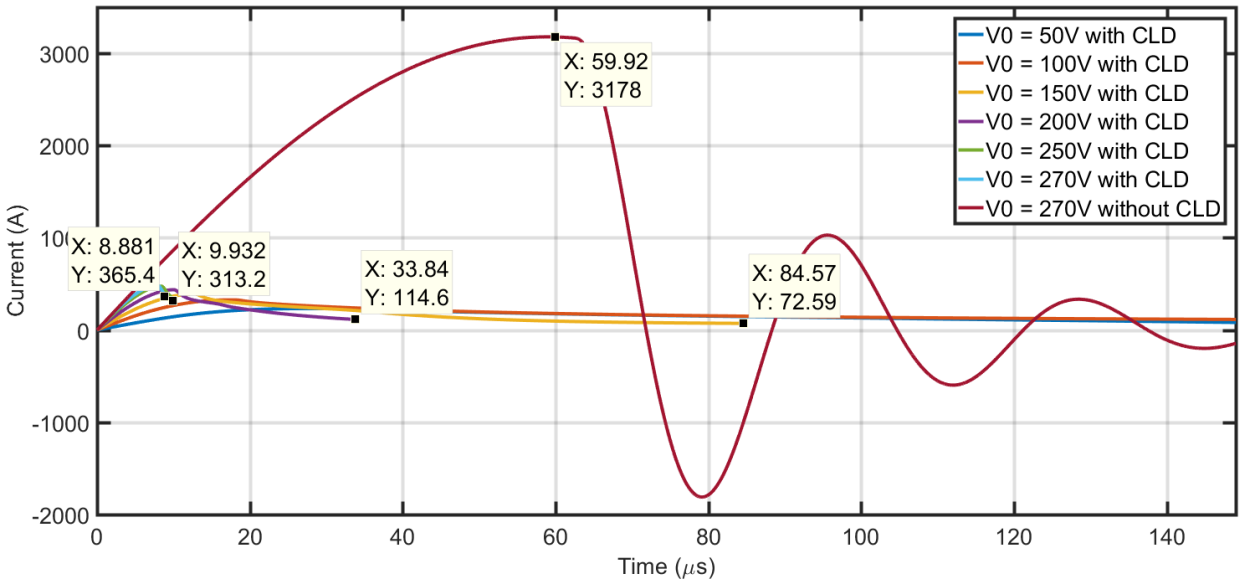


Figure 5.20: Simulated capacitor current (ICap)

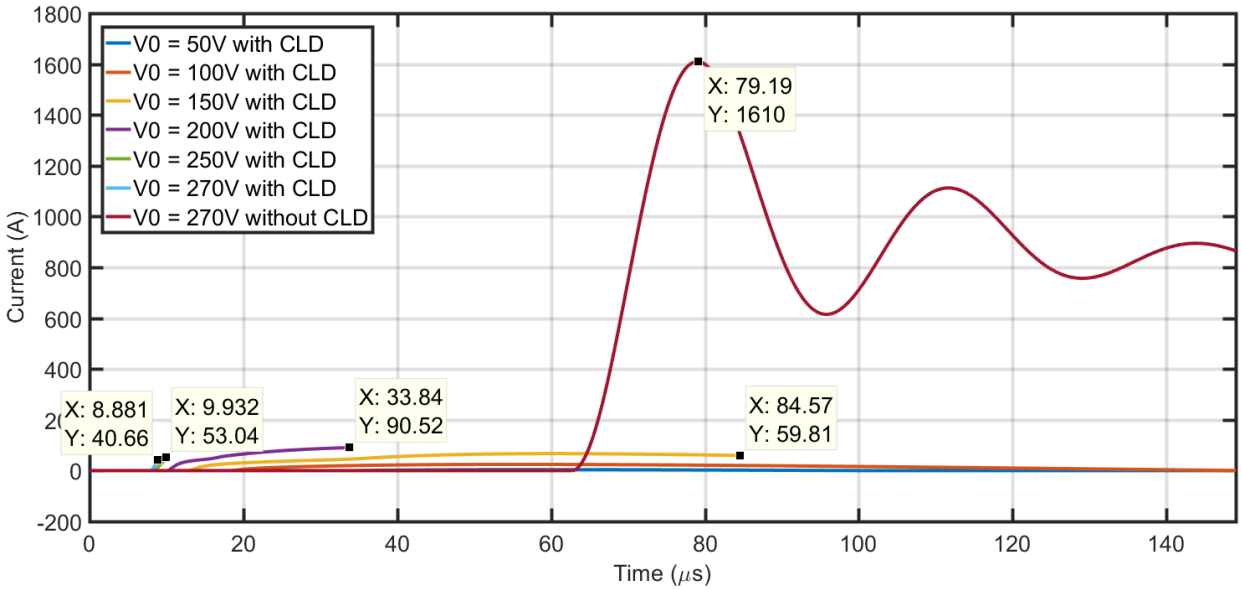


Figure 5.21: Simulated Diodes current (IDiode)

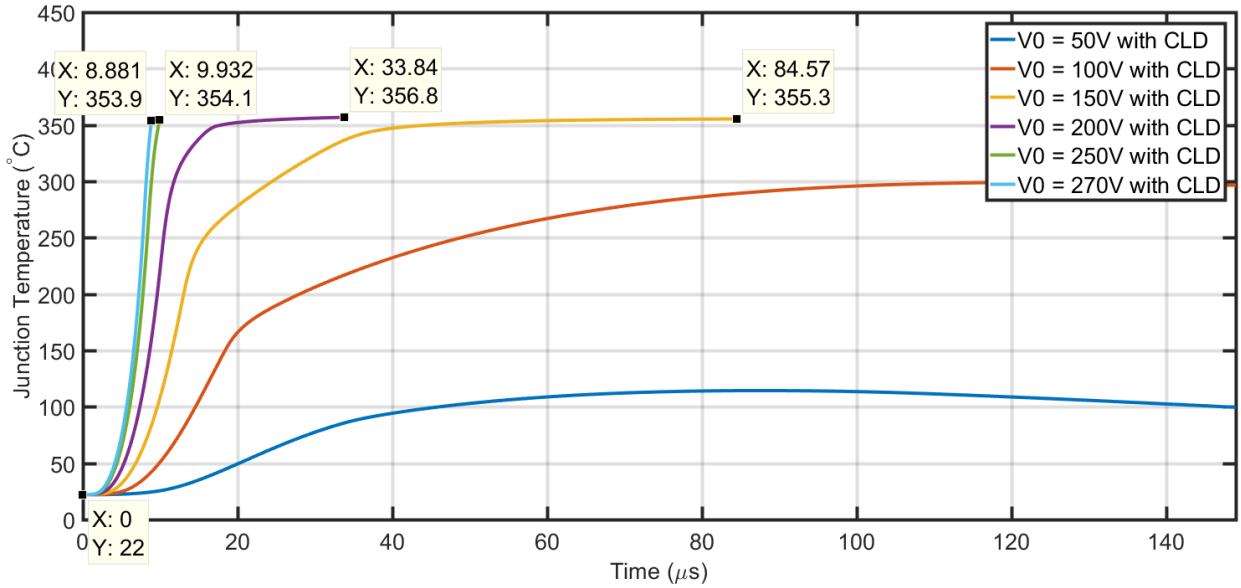


Figure 5.22: Simulated CLD temperature (V(Tj))

The results obtained from this simulation demonstrate that the CLD is effective in limiting the contributions of the DC capacitor to fault currents. By including the CLD, the peak magnitude of the capacitor current (ICap) is reduced by more than 80% of its prospective value. This significantly reduces the amount of fault current at the output of the converter (IFault), and consequently, currents that are freewheeled through the diodes (IDiode).

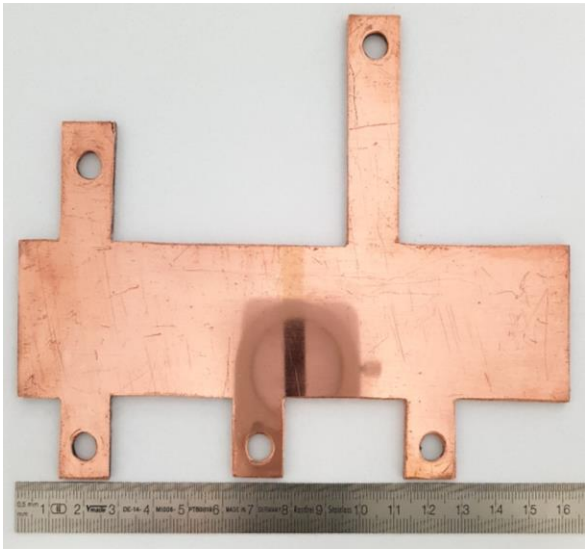
5.3. Construction

This section details built components of the CLD, assembly of these components, and integration of the CLD into the converter.

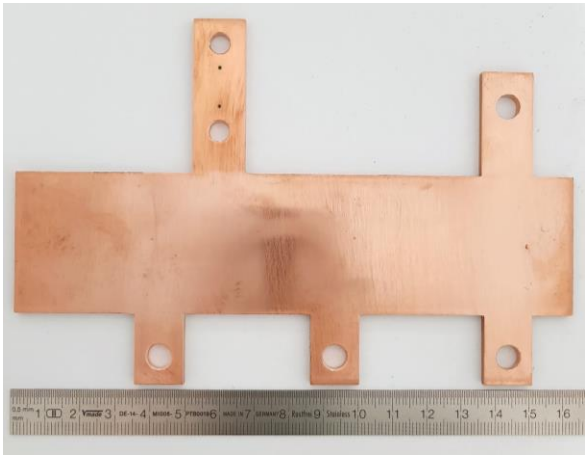
5.3.1. Built Components

A) Copper Structures

The positive and negative potential busbars were manufactured out of 3mm thick copper plates, as shown in Figure 5.23. Dimensions of these parts are specified in Appendix C.



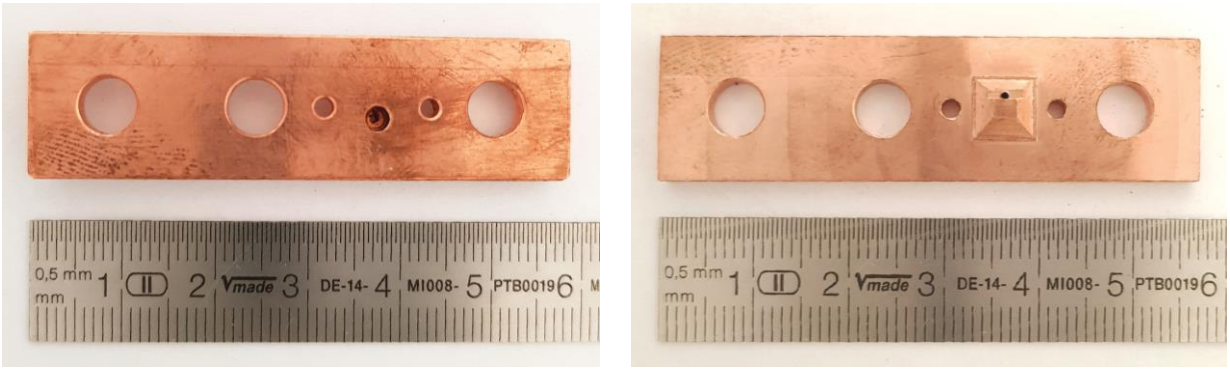
(a)



(b)

Figure 5.23: Top side view of (a) positive and (b) negative potential busbars

The cathode structure was also manufactured out of copper, shown in Figure 5.24, according to the dimensions specified in Appendix C. The surface contacting the die was polished down to the lowest possible surface roughness.



(a) (b)

Figure 5.24: (a) Top and (b) bottom side views of cathode structure

B) Fasteners

To support the structure, two M6 x 20 ceramic screws shown in Figure 5.25 were used for mechanical support on both sides of the die.

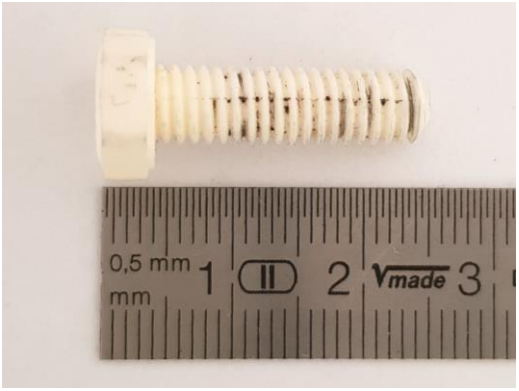
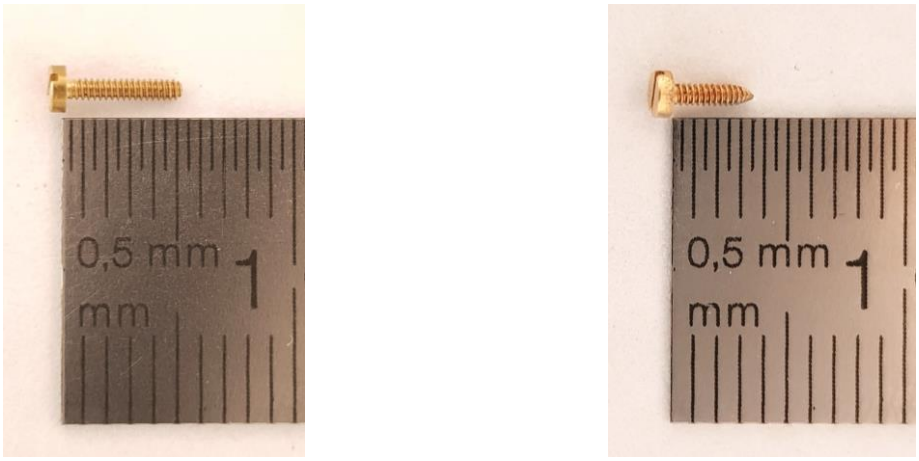


Figure 5.25: Picture of ceramic screw used for mechanical support

In addition, an M1 x 5 brass screw, shown in Figure 5.26 (a), was cut and tapered as shown in Figure 5.26 (b). This screw was used to make electrical connection to the gate pad of the die, so that the gate and source terminals are connected ($V_{GS} = 0$).

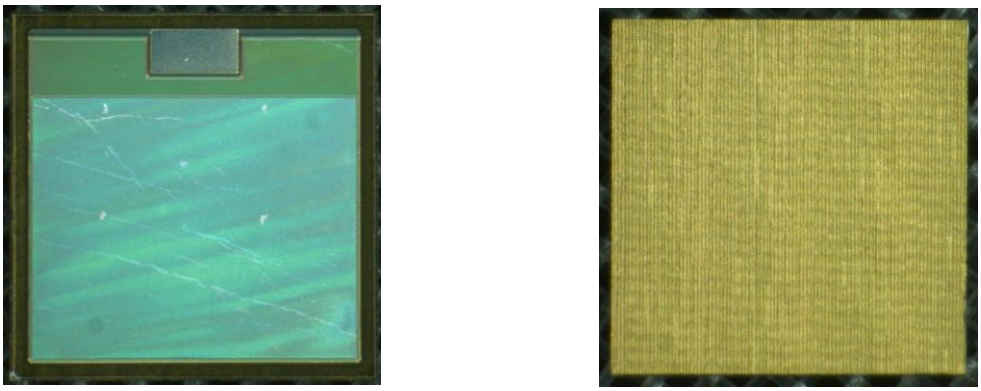


(a) (b)

Figure 5.26: Picture of M1 x 5 brass screw (a) before, and (b) after cutting and tapering

C) Silicon Carbide Junction Field Effect Transistor Die

The Silicon Carbide Junction Field Effect Transistor die, shown in Figure 5.27, was manufactured by United Silicon Carbide. The bottom (drain) side of the die is metalized with Tin, Nickle, and Gold layers of 0.07, 0.1, and 0.1µm thicknesses respectively. These layers ensure good interface when solder attaching this die to a substrate. The top side is metalized with a 5µm thick aluminum layer, to support attaching aluminum wire bonds.



(a) (b)

Figure 5.27: (a) Top and (b) bottom side views of SiC-JFET die

D) Positioning Stencils

To maintain the die's position on the anode structure during assembly, a stencil was designed and manufactured as shown in Figure 5.28. The stencil was laser cut from a 125µm think stainless steel

sheet to ensure low tolerances (within ± 15µm). Dimensions of this stencil are provided in Appendix C.

Figure 5.28: Picture of manufactured stencil

5.3.2. Current Limiter Assembly

This section details the steps that were taken to assemble the current limiter, starting with the components described above, and ending with a current limiter that is integrated into the busbars, and connected to the converter module, DC link capacitors, and cables.

1- Metal polish was used to polish surfaces of the copper structures that contact the die to remove any corrosion that may have formed since last polished. The surfaces are then cleaned with a solvent cleaner to remove any residues of dirt or grease. A zoomed view of those surfaces after this process is shown in Figure 5.29.

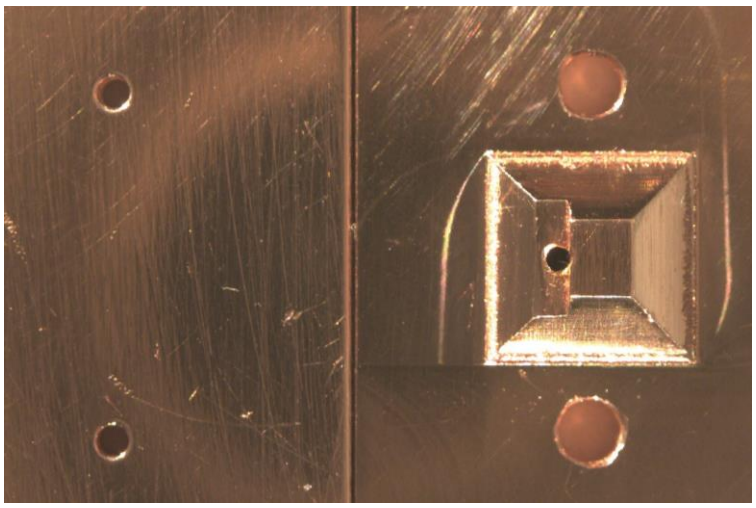


Figure 5.29: Zoomed view of surfaces that contact the die after polishing and cleaning

2- The positioning stencil is then placed on the negative potential copper structure and fixed using stainless steel M1 nuts and screws. The die is picked using and placed in the desired location using a vacuum pencil, as shown in Figure 5.30.

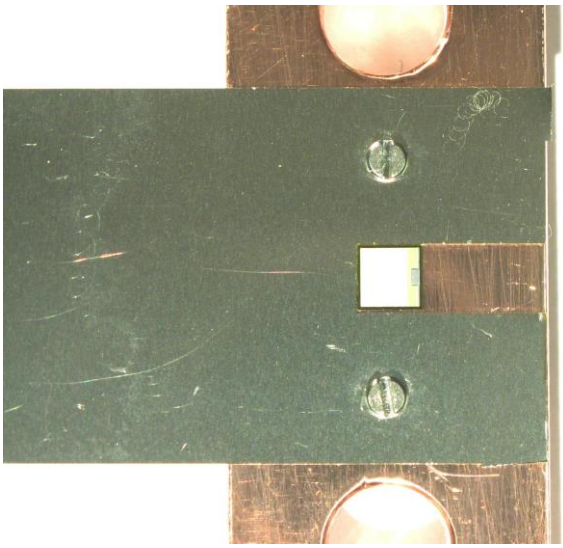
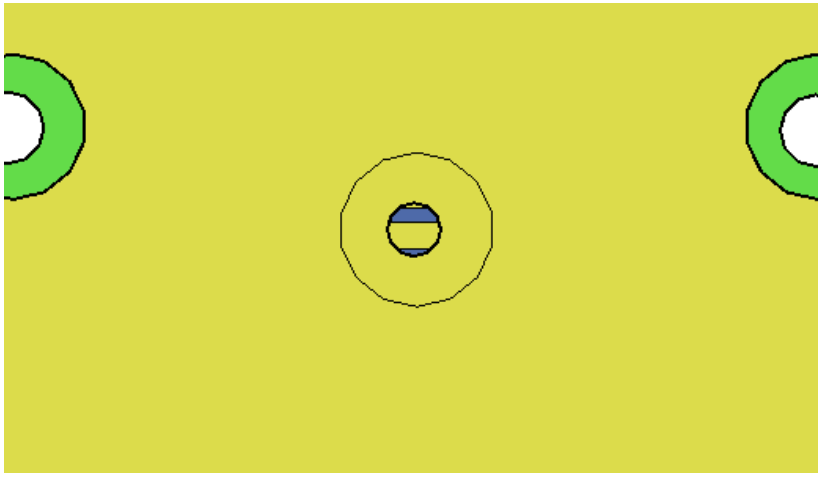
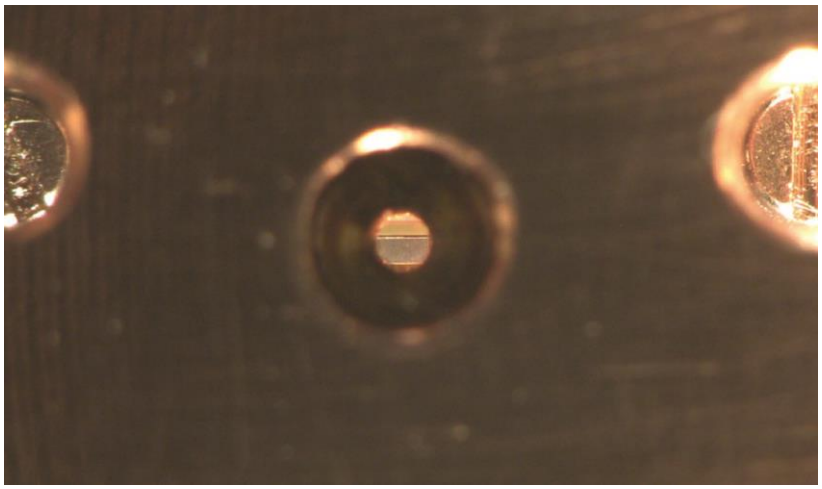


Figure 5.30: View of die positioning setup

3- The cathode structure is then attached, and the two ceramic screws tightened up, the M1 nuts are unfastened, M1 screws removed through the top, and stencil slide out through the side. Correct positioning of the die was verified by comparing the view from the gate screw's hole found using a digital microscope with that expected from Computer Aided Drafting (CAD), as shown in Figure 5.31.



(a)



(b)

Figure 5.31: (a) Expected and (b) observed views from gate screw's hole

4- The M1 brass gate screw is then fastened into its position, and sealant applied around the edges of the cathode structure, in assembly holes, and over the gate screw. This process was not completed due to safety restrictions against the use of some chemicals in university labs.

5- With the positive potential busbar connected to the DC capacitor, which is supported by a holder with the dimensions specified in Appendix C, the negative potential busbar with integrated current limiter is connected to the capacitor, as shown in Figure 5.32.

(a) (b)

Figure 5.32: Busbars and capacitor integration setup (a) before and (b) after connection of negative potential busbar with integrated CLD

6- The busbars are then adjusted in height using the capacitor holder and connected to the converter module and cables, as shown in Figure 5.33.

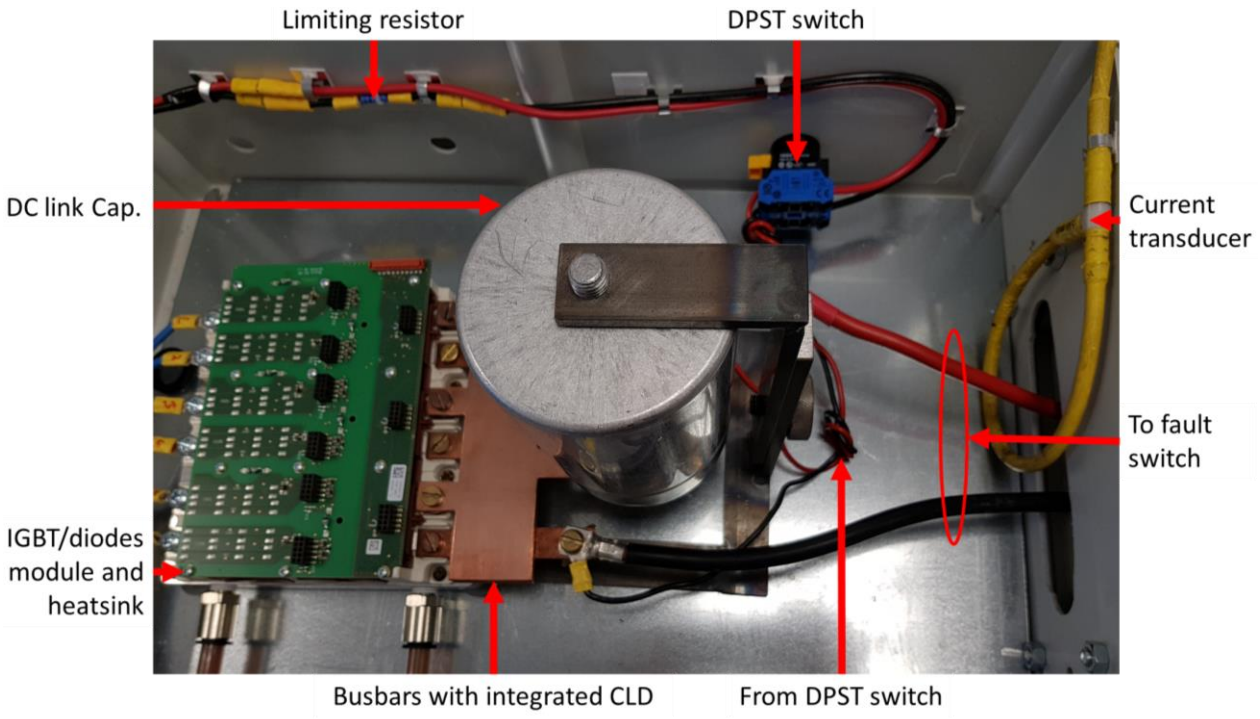


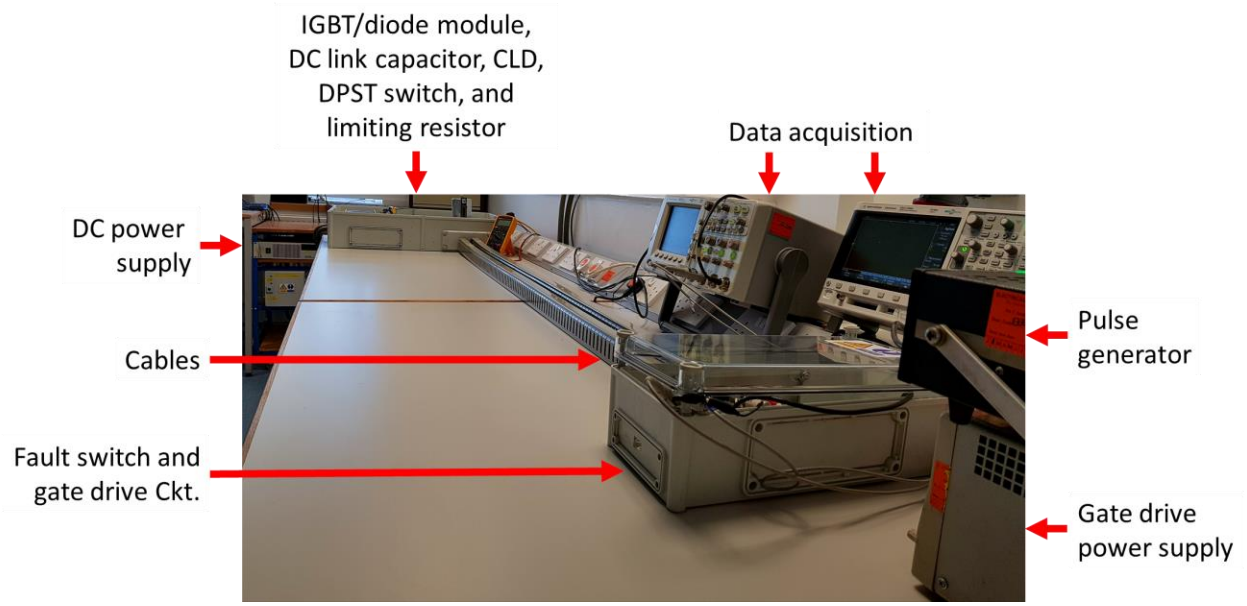
Figure 5.33: Final view of busbar integrated current limiter connected to converter module, DC capacitor, cables, and DC power supply

5.4. Current Limiter Testing

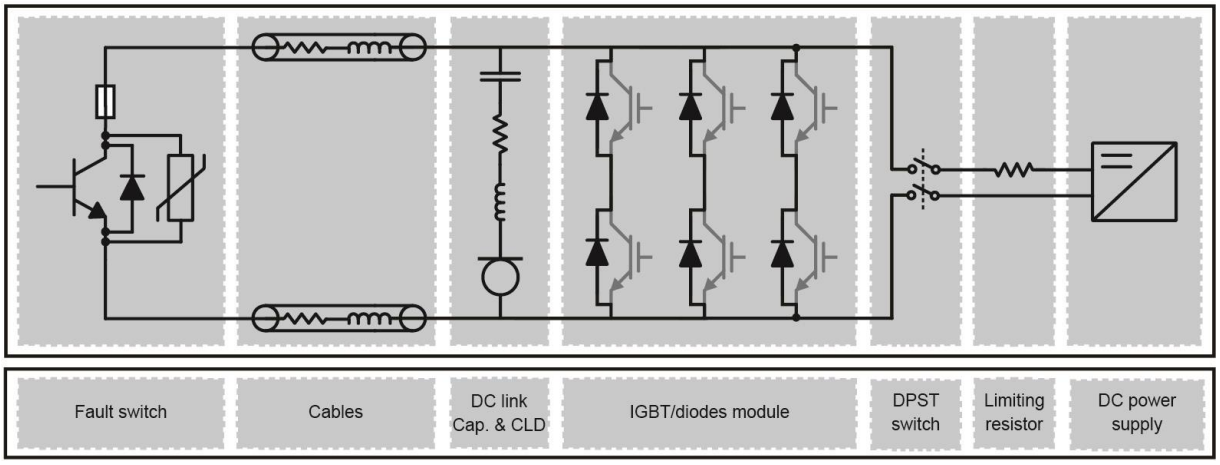
This section details testing of the current limiter as part of a single channel replica of a 100kW motor drive designed and built for aerospace application, as discussed earlier. It describes the experiment setup, presents the test results, and how the results compare with expected.

5.4.1. Experiment Setup

The current limiter was tested in a similar experimental setup to that used in Chapter 3 to characterize the converter's fault response, as shown in Figure 5.34. The two differences being the inclusion of the current limiter and replacement of the fault switch to allow for fault interruption. An Insulated Gate Bipolar Transistor (IGBT) based switch was developed, which can interrupt the fault after a few microseconds of its introduction. Unlike the Thyristor based switch, described in Chapter 3, which was only capable of isolating the fault after its current has decayed to ≈ 0A.



(a)



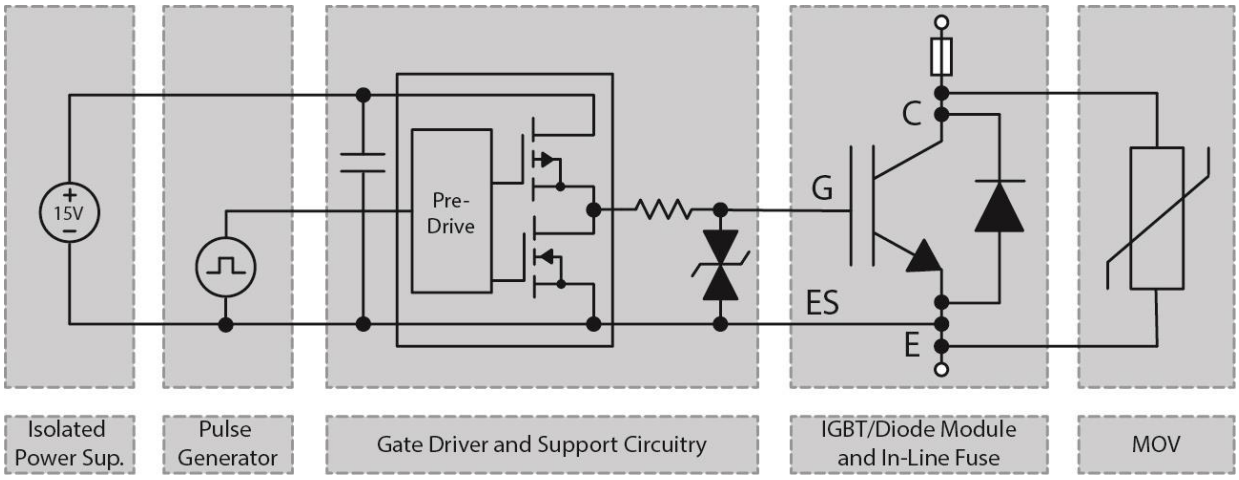
(b)

Figure 5.34: (a) Picture and (b) overview diagram of experiment setup

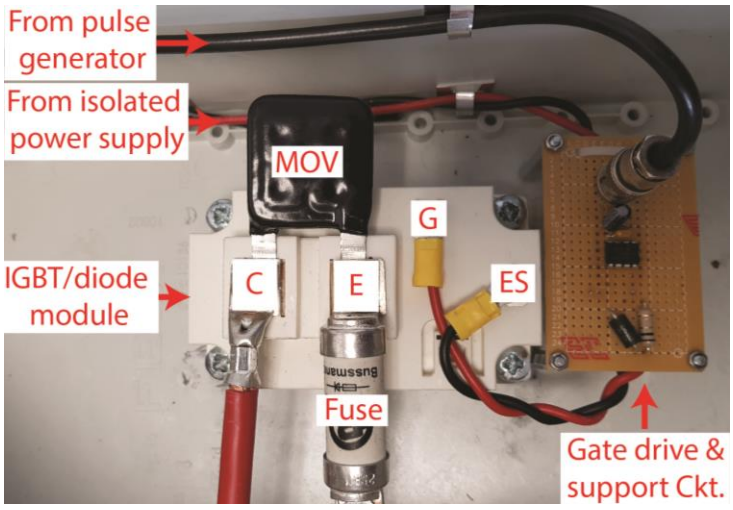
A) IGBT-Based Fault Switch

The switch contains an IGBT/diode module which represents the main switching element, connected in series to a high-speed fuse to ensure that other components are not damaged in case the CLD fails. A Metal Oxide Varistor (MOV) is connected between the Collector (C) and Emitter (E) terminals of the IGBT to protect it from overvoltage, and a gate driver circuitry is connected between the Gate (G) and Emitter Sense (ES) terminals to control its switching state (ON/OFF),

as shown in Figure 5.35. The gate driver is powered from a 15V DC power supply, and triggered from a pulse generator. More details of the components used in this switch are presented next.



(a)



(b)

Figure 5.35: (a) Schematic diagram, and (b) picture of IGBT-based fault switch

B) Insulated Gate Bipolar Transistor (IGBT) and Diode Module

The module, shown in Figure 5.36, contains an IGBT switch connected to a diode in an anti-parallel configuration [22]. The device can withstand up to 1200A of peak pulsed currents and is rated to 1.2kV. This module was selected due to its high current capacity compared with MOSFET based modules and switch off current capability compared with Thyristor based modules.

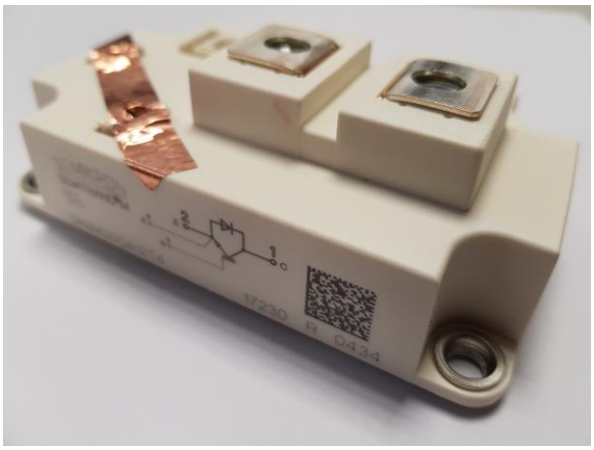


Figure 5.36: Picture of IGBT/Diode module [22]

The IGBT's output characeteristcs were extracted using the Tektronix 371B curve tracer at a gate-to-emmiter potential of 15V used by the selected gate driver, as shown in Figure 5.37. Measuered characteristics were compared to those computed using datasheet parameters (V_{IGBT} = 0.94V and R_{IGBT} = 2.5mΩ) as also shown, and found to match very well.

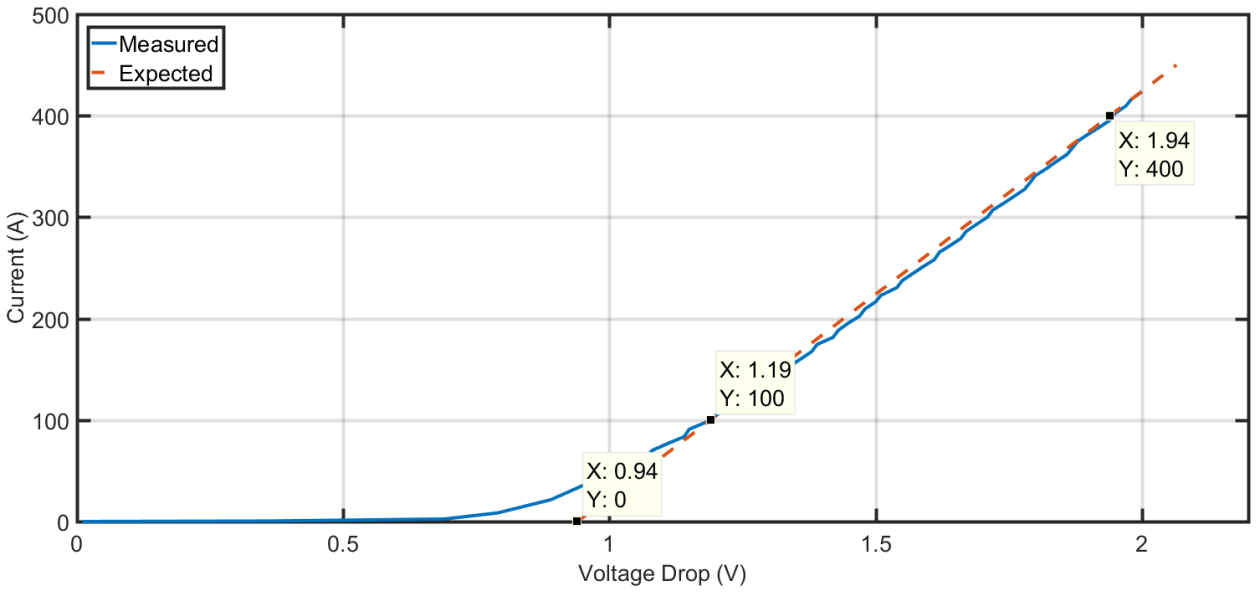


Figure 5.37: Measured IGBT output characteristics vs. expected, showing equivalent circuit extraction points

C) Metal Oxide Varistor

A Metal Oxide Varistor (MOV) [23], shown in Figure 5.38, was added to ensure that the Emitter-to-Collector voltage of the IGBT does not exceed its breakdown rating of 1.2kV. This can occur

during turn-off due to inductances in the fault current path (L_{short}). This component was selected based on its maximum clamping voltage of 845V being below the collector to emitter breakdown of the IGBT, and its maximum discharge current of 40kA being sufficiently larger than expected in this experiment.

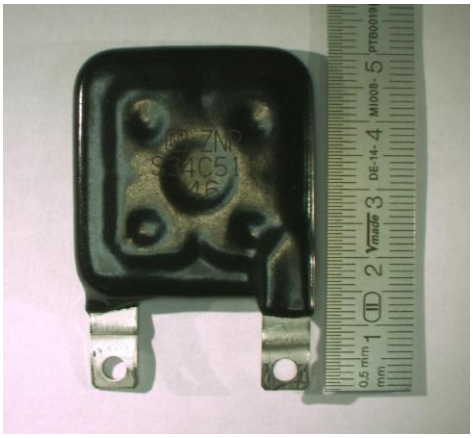


Figure 5.38: Picture of selected MOV

D) Gate Driver Circuitry

The gate driver circuitry is needed to source and sink instantaneous currents to and from the IGBT to turn the device ON or OFF. The driver chip selected [24], with the block diagram shown in Figure 5.39, is capable of sourcing and sinking up to 9A of current. This enables fast switching of the device, within a minimum of 0.32µs ON time and 0.69µs OFF time specified in the IGBT's datasheet [24].

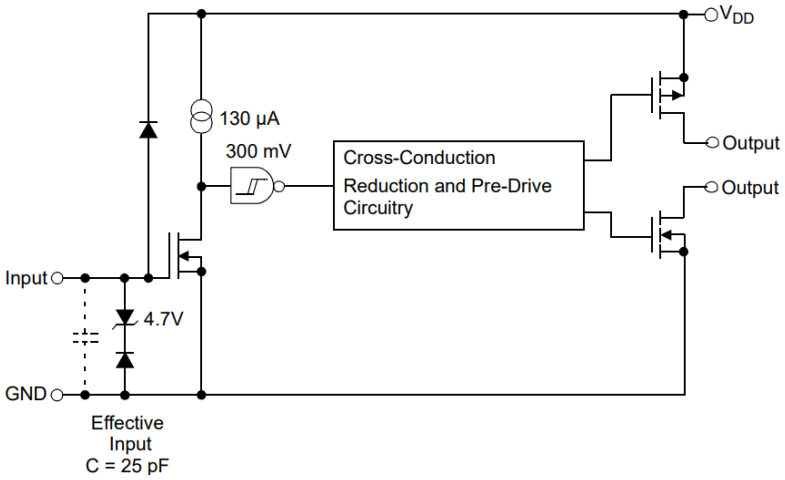


Figure 5.39: Functional block diagram of gate driver [24]

The driver's support circuitry includes a 1Ω gate resistor to damp oscillations, a Transient Voltage Suppressor (TVS) to limit the maximum gate-to-emitter voltage of the IGBT within its maximum specified ratings of ±15V [25], and a combination of ceramic and electrolytic capacitors of 11µF total to source instantaneous switching currents to the IGBT, as shown in Figure 5.40.

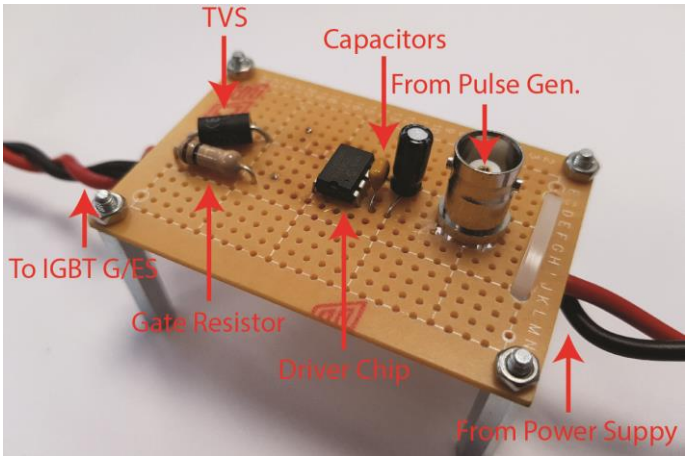


Figure 5.40: Picture of gate driver and support circuitry board

E) Baseplate

Due to the limited duration of time for which the switch is operational in this experiment (approximately 10 - 100µs), it was determined that no heatsink would be required. Instead, the IGBT module was mounted on a 1 cm thick aluminum baseplate, shown in Figure 5.41, to absorb any generated instantaneous heat. A layer of conductive thermal paste was applied on the baseplate before mounting to improve thermal resistance of contact.

(a)

(b)

(c)

Figure 5.41: (a) Bottom side view of IGBT/diode module, (b) top side view of Aluminium baseplate, and (c) side view of assembled module with baseplate

F) Fuse

A fuse was added to ensure that if the CLD fails, the resulting fault current would be limited, so that other components don't subsequently fail. The fuse selected, shown in Figure 5.42, has an i^2t pre-arcing limit of $25A^2sec$ after which the fusing element starts melting. This limit is plotted in Figure 5.43, along with the expected RMS fault current with and without the CLD, as simulated from the circuit shown in Figure 5.18. Figure 5.43 demonstrates that no fusing should occur when the CLD is in place. However, if the CLD fails, fusing should occur within 22µs.

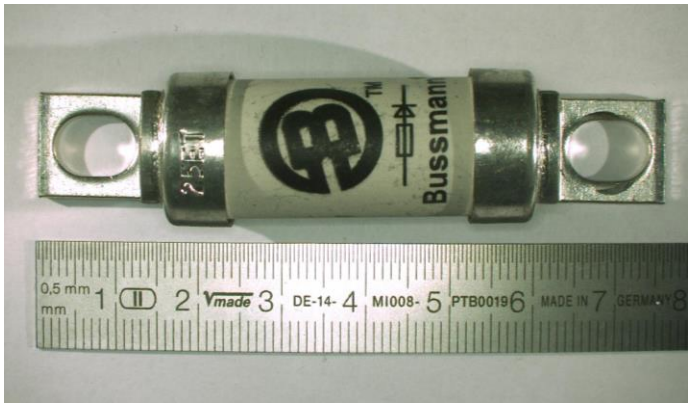


Figure 5.42: Image of selected fuse

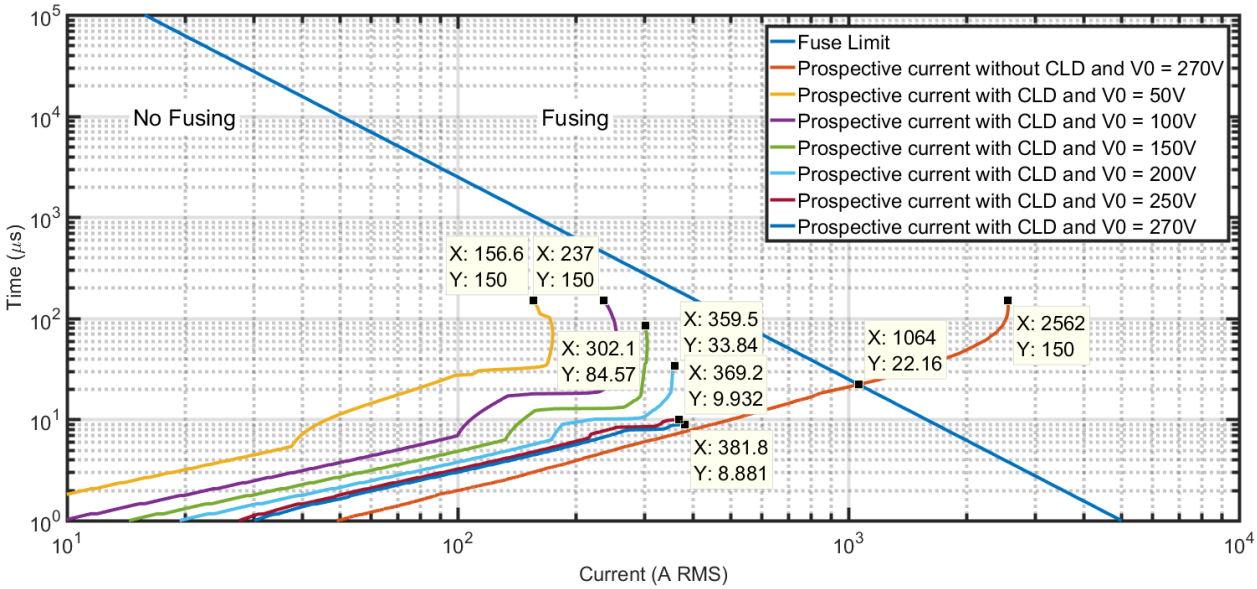


Figure 5.43: Prospective currents vs. time compared with fuse i^2t limit

5.4.2. Test Result

This section presents experimental results obtained from the setup described above. The DC link was charged up using an external DC power supply to 100, 150, 200, and 250 volts, which was then isolated via the DPST switch, and fault switch triggered for 30μs. Measured fault branch's currents with the CLD included in the circuit are compared to those obtained from the analytical model in Figure 5.44-Figure 5.46, where the expected currents are obtained from the simulation circuit shown in Figure 5.18. Prospective currents without the CLD obtained from the same simulation circuit are also included for comparison.

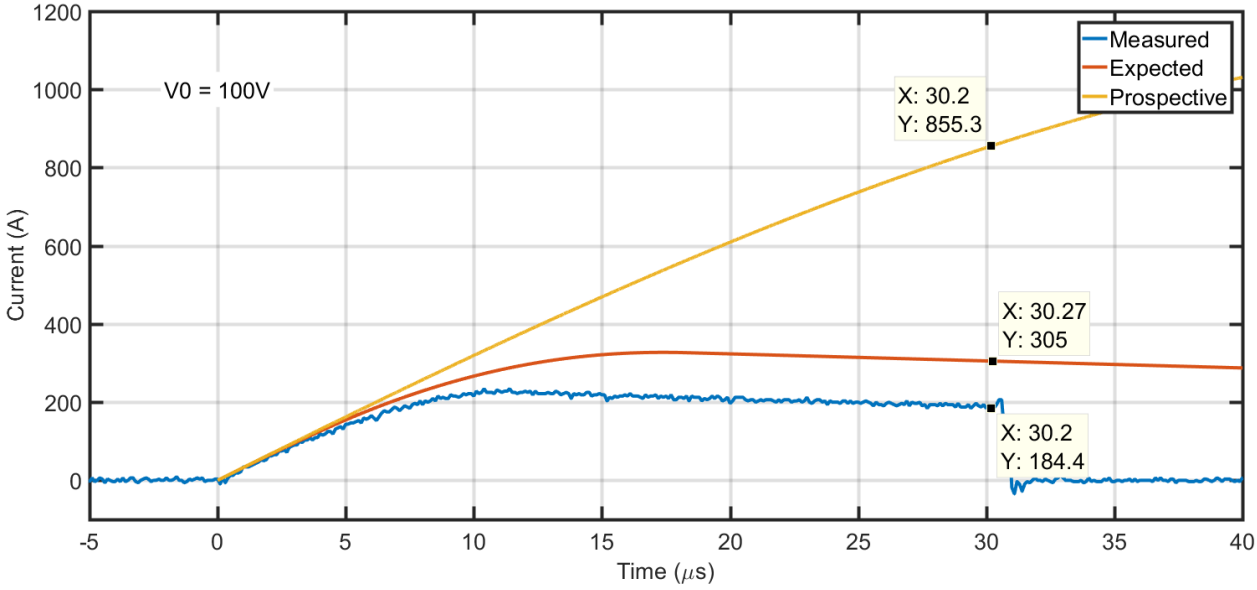


Figure 5.44: Comparison of measured, expected, and prospective fault branch's current, for an initial DC link voltage of 100V

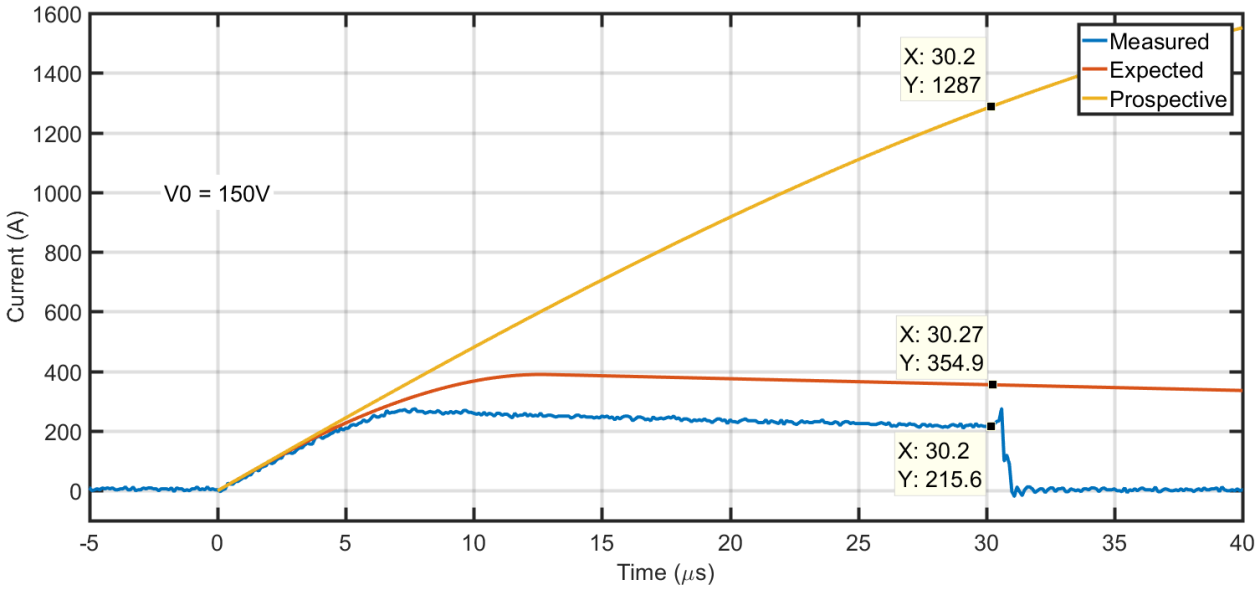


Figure 5.45: Comparison of measured, expected, and prospective fault branch's current, for an initial DC link voltage of 150V

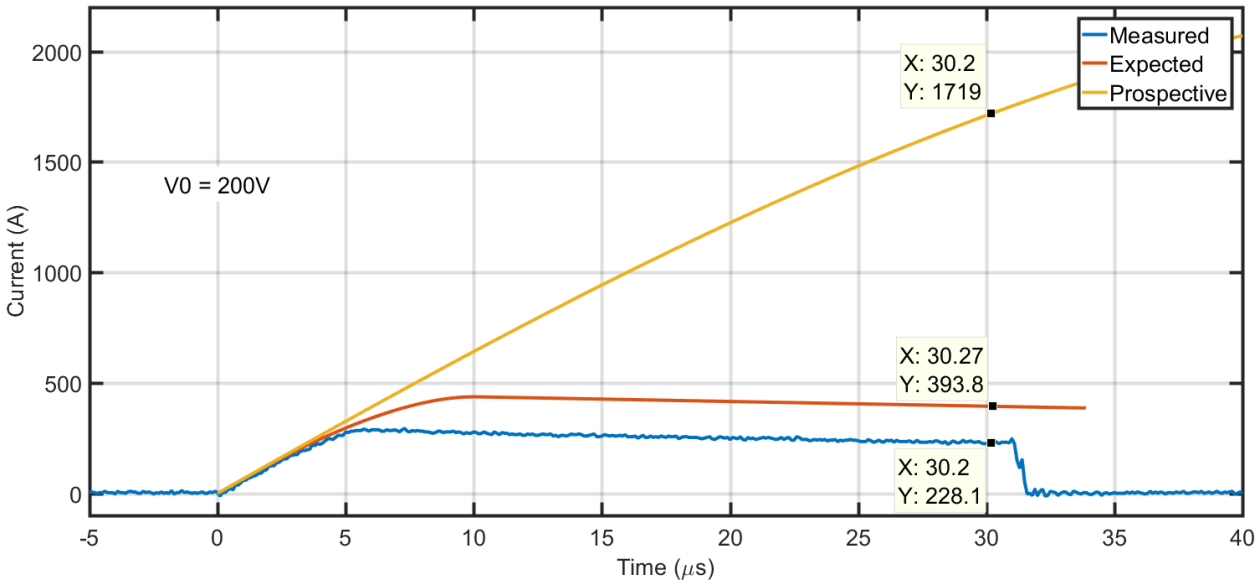


Figure 5.46: Comparison of measured, expected, and prospective fault branch's current, for an initial DC link voltage of 200V

The results demonstrate reasonable matching between measured and expected waveforms, given the limitations of the simulation models described in Section 5.2.2. . Expected short-circuit currents were found to exceed measurements by 65%, 65% and 73% for the 100, 150, and 200 volts cases respectively. This is due to the CLD's SPICE model overestimation of the current saturation level, as demonstrated by the output characteristics measurement shown in Figure 5.47. The results also demonstrate the effectiveness of including the CLD, as it results in a significant reduction of measured fault current from prospective currents without the CLD. Fault currents are reduced by up to 78%, 83%, and 87% in the 100, 150, and 200 volts cases respectively.

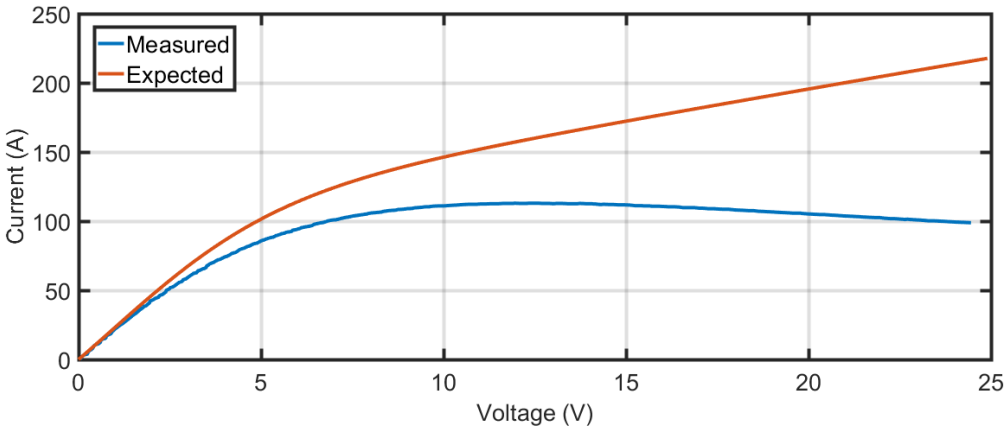


Figure 5.47: Comparison of CLD's output characterises obtained from SPICE model and measured using the Tektronix 371B curve tracer

Testing was also carried out with an initial DC link voltage of 250V, as shown in Figure 5.48. However, the CLD failed after only 6µs. Current then rose uncontrollably until reaching the input limit of the oscilloscope (≈600A) after approximately 10µs, and then exceeding this limit for the remainder of the measured waveform (although shown limited at 600A). Although fusing effect was not captured in the waveform, the fuse was found to have opened and remaining components of the test circuit survived the test. Although this CLD design failed prematurely at 250V, there is potential for this device to be used in various applications operating at or below 200V. In addition, for applications requiring higher voltage, multiple current limiters can be connected in series sharing the voltage under a fault condition, which comes at the expense of higher resistance and thus power losses during nominal conditions.

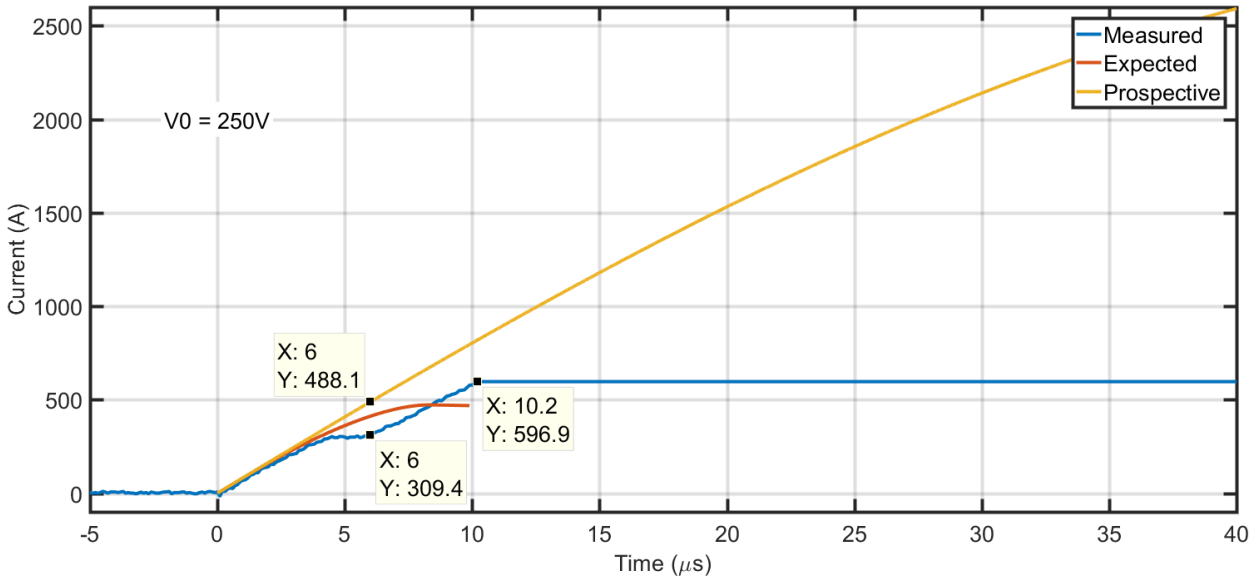
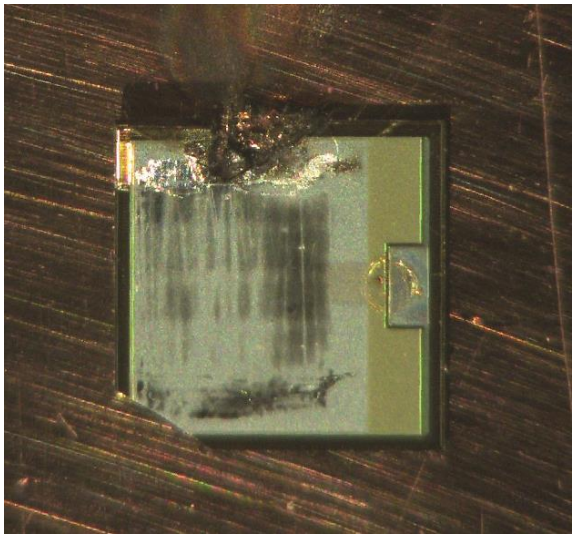


Figure 5.48: Comparison of measured, expected, and prospective fault branch's current, for an initial DC link voltage of 250V

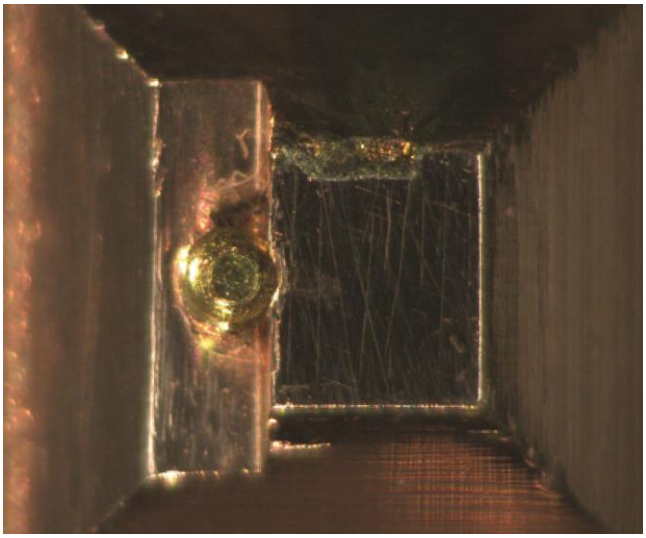
The device initially survived the 250V blocking voltage so the failure wasn't due to an over-voltage. The device started to enter current saturation mode too, further indicating that over voltage was not the case. Therefore, the device must have been operating outside its combined thermal and current Safe Operation Area (SOA). As the device didn't reach 10µs, something in the package reduced the short-circuit capability of the device. It is likely that the die was not fully contacted, i.e. the pressure contact was not uniform resulting in a filament due to current running through a proportion of the device. This would have reduced the short-circuit

withstand capability of the JFET and short-circuit time. contact scuffing can be observed in Figure 5.49 around a good proportion of the die, as well as damage to the top side of the die where the filament occurred.

(a)



(b)



(c)

Figure 5.49: (a) Overview and (b & c) zoomed captured digital microscope images of failed CLD

5.5. Conclusions

This paper presented an approach to limit DC side contributions using normally-ON SiC-JFETs in series with the capacitors. Under normal conditions, the devices operated in the linear I(V) region where they have very small resistances and thus, little influence on the converter operation. While

under a fault condition, the capacitors voltages appeared across the device causing them to operate in the saturation region where their current is limited by channel pinch-off and self-heating. This approach was supported by experimental results where a CLD was used to limit the short-circuit fault current of a charged DC capacitor up to 250V.

5.6. References

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Chapter 6: An Integrated Current Limiting Diode for Extended Operation

6.1. Introduction

A shortcoming of the CLD configuration discussed in Chapters 4 and 5 is the limited fault time duration. This is due to the significant amount of heat that must be dissipated through the SiC-JFET dies, which leads to the devices reaching their maximum junction temperatures within tens of microseconds. It was concluded in Chapter 4 that this time cannot be drastically extended by altering the JFET's physical parameters without sacrificing the ON-state resistance. Paralleling multiple JFETs does not achieve this goal either, as it leads to proportionally higher fault current levels given by nI_{SAT}, where n is the number of parallel connected devices and I_{SAT} is the saturation current of each device, as illustrated in Figure 6.1. Furthermore, anode-to-cathode voltage (V_{AC}) across the parallel combination of JFETs is approximately the same as that across a single device. This is because the voltage is typically held by a large capacitor. Consequently, power loss through each one of the parallel connected JFETs is equal to that of a single device ($I_{SAT}V_{AC}$), and the total loss seen by the combination of JEFTs is scaled by the number of devices ($nI_{SAT}V_{AC}$). To enable the distribution of losses among multiple SiC-JFETs, while maintaining low CLD current limit and losses, a novel Integrated Current Limiting Diode (ICLD) topology is proposed.

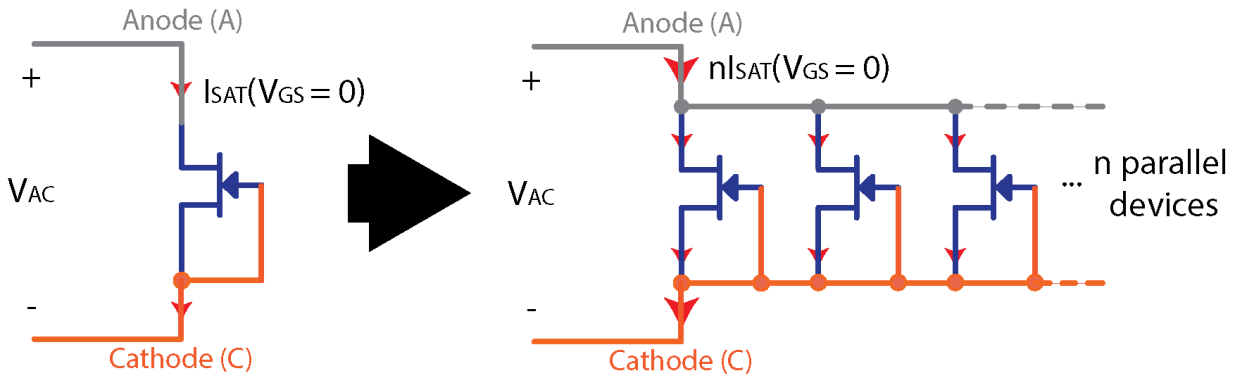


Figure 6.1: Illustration of current multiplication when parallel connecting SiC-JFETs with V_{GS}=0

The ICLD's circuit configuration, shown in Figure 6.2, utilizes a number (n) of parallel connected high-side devices which operate deep in the saturation region with drain-to-source voltages (V_{DS}) approximately equal to the input voltage (V_{AC}). These high-side devices dissipate the majority of

the ICLD's losses. The circuit also includes one or more low side devices which are operate in the quasi saturation region when a fault occurs. Therefore, their drain voltage is significantly lower than that of the high-side devices. These low-side devices provide negative potential across the gate and source terminals of the high-side devices ($V_{GS(high)} = -V_{DS(low)}$) as the gate voltages are referenced to the source of the low-side FET. This potential regulates current through the high-side JFETs to a lower value than at $V_{GS}=0$. The resultant losses are distributed among high-side devices, without total current and losses being multiplied by the number of parallel connected devices, as shown previously in Figure 6.1.

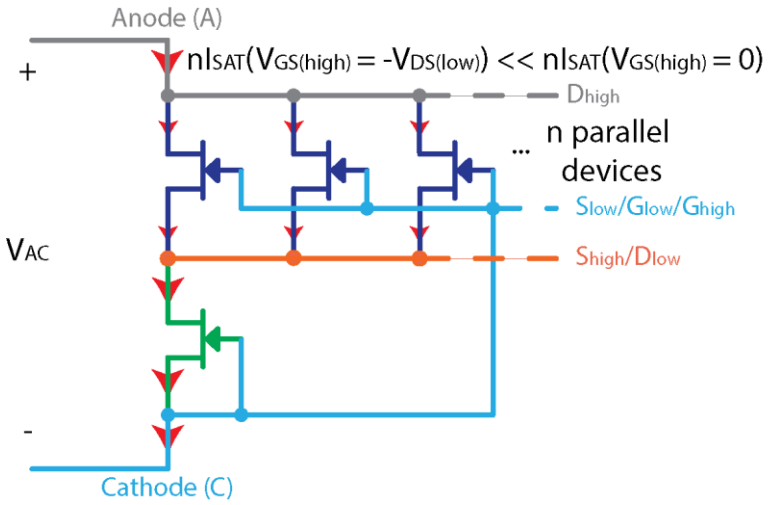


Figure 6.2: Schematic of ICLD circuit topology

In the next section, the design of a Proof-Of-Concept Integrated Current Limiting Diode (POC ICLD) is presented, including components selection and performance analyses. The analyses include thermo-electrical simulations demonstrating the operation and capability of the ICLD. In the third section, details of a built ICLD demonstrator are presented, with descriptions of built components and assembly steps. In the fourth section, I(V) tests are performed on the built ICLD demonstrator. The conclusions are then presented in the fifth section.

It should be noted that the objective of the fabricated POC ICLD is not to perform high-voltage short-circuit testing, but rather to alleviate risks that have been identified with the presented design, related to:

1- Pressure packaging multiple SiC JFET dies in a highly dense and integrated form.
2- Achieving low ON-state resistance and current saturation level at the same time.

6.2. Design

6.2.1. Components Selection

A) Silicon Carbide Junction Field Effect Transistors

Silicon Carbide Junction Field Effect Transistors manufactured by United Silicon Carbide, as discussed in Chapter 5, were selected for this design. 10 JFETs dies were used for the high-side devices, whereas a single TO-247 plastic packaged device was used for the low-side FET. This choice of packaging was made so that top side devices could be housed in a high temperature compliant (>600°C) assembly, while the low-side plastic packaged device was used due to its reduced power dissipation.

As discussed in Chapter 5, temperature dependent SPICE models of these devices are provided by the manufacturer. To include the effects of temperature dynamics in the SPICE simulations presented in the next section, the equivalent thermal networks of the high and low side devices were extracted. For the low-side plastic packaged device, the manufacturer's datasheet includes junction-to-case thermal impedance data, as shown in Figure 6.3. This data was curve fitted to an equivalent foster thermal network, with the form given by (2.98), and parameters listed in Table 6.1. Due to the limited duration of time for which the devices are operational (100s of microseconds), the case-to-ambient impedance was disregarded. The equivalent thermal network for the high-side devices are extracted next in section B.

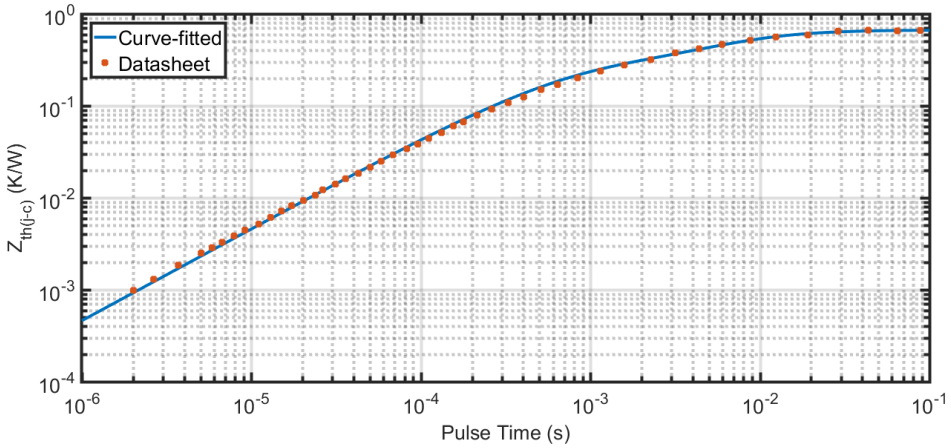


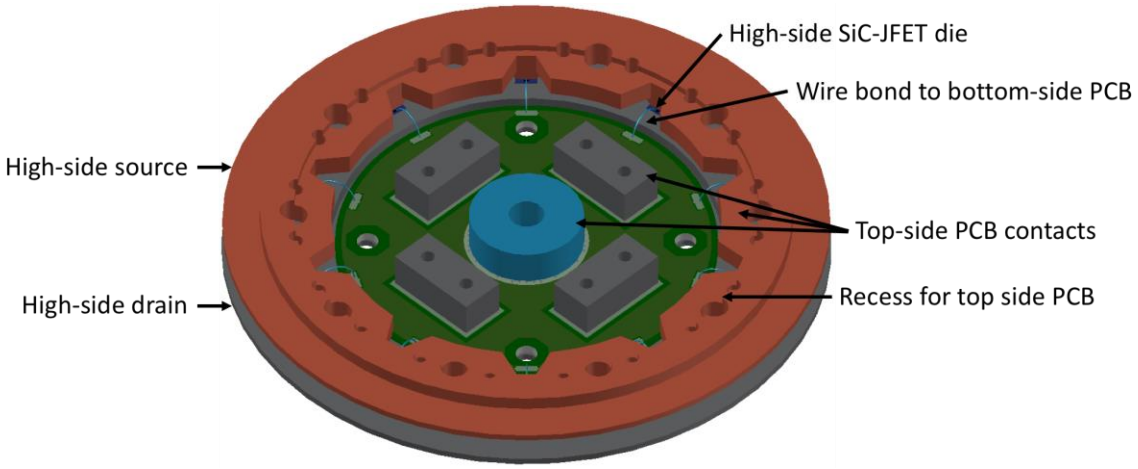
Figure 6.3: Comparison of datasheet and curve fitted thermal impedance data of bottom side device

Table 6.1: Foster network curve fitting parameters of bottom side device

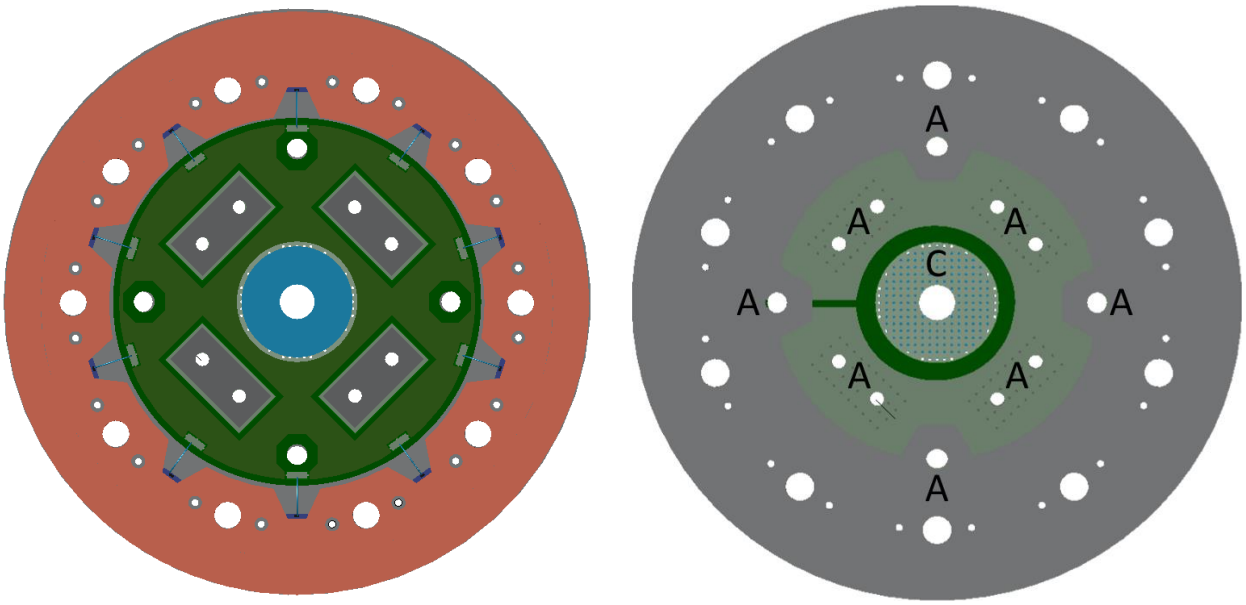
i	$R_i\ (m\Omega)$	$C_i\ (F)$
1	0.04502	0.4393
2	0.3591	0.01632
3	0.05572	0.3733
4	0.203	0.00253

B) High Temperature Packaging

Like the design of the single CLD configuration presented in Chapter 5, the ICLD's design also utilizes copper structures to pressure contact the high-side devices. Figure 6.4 shows the structure of the high side device packaging. As shown, (a) in orange and grey for the source and drain contacts respectively. The dies, shown in dark blue, are arranged symmetrically in a circular configuration to impose equal current sharing. Wire bonds, shown in light blue, connect the gate pads of the dies to a bottom side PCB. The gate signals are then routed to the cathode terminal on the bottom side of that PCB, as shown in Figure 6.4 (c). Cathode potential is also routed to a top-side PCB (not shown in Figure 6.4) through a circular copper structure at the centre of the ICLD, shown in light blue in Figure 6.4 (a). The top-side PCB also connects to the anode through four rectangular copper structures shown in grey. In addition to sealing the top side of the ICLD, the top-side PCB houses the low-side JFET and snubber circuitry. It connects the drain terminal of the low-side JFET to the source terminals of the high-side, and gate & source to the cathode terminal, as illustrated in Figure 6.5.



(a)



(b) (c)

Figure 6.4: (a) Isometric and (b) top, and (c) bottom views of ICLD packaging

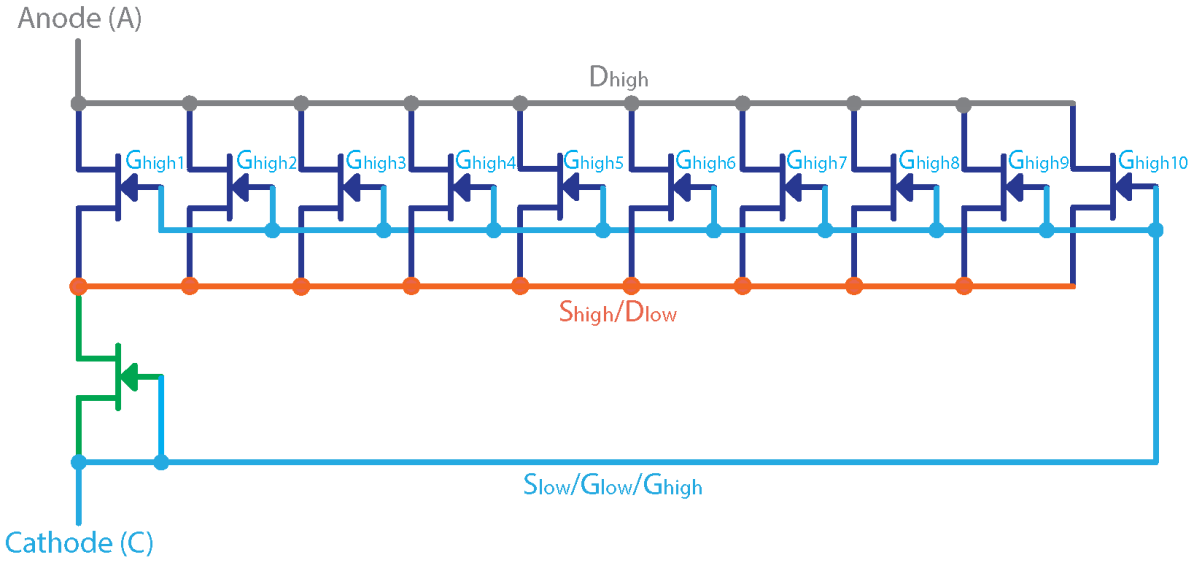


Figure 6.5: Equivalent circuit of the ICLD demonstrator

A combination of ceramic, brass, and stainless-steel fasteners are used to package the ICLD, as shown in Figure 6.6. M4 ceramic screws and nuts were used to exert pressure on high-side devices, while maintaining electrical isolation between the drain and source copper structures. M1 stainless steel fasteners were used on both sides of the ceramic screws to aid during assembly only. In addition, M2 and M5 brass retainers were used to ensure good electrical connections between the

top and bottom sides of the PCBs. The M5 brass screw also facilitates using a lug type connector on the bottom side of the ICLD for the output terminal (cathode). Finally, four M2 brass fasteners are used to fix the bottom side PCB in place, as well as to facilitate using lug type connectors on the bottom side of the ICLD for the input terminal (anode).

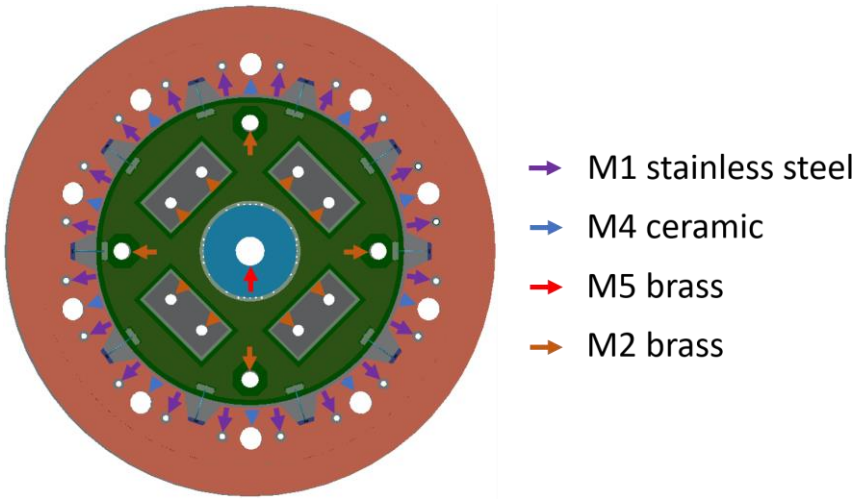
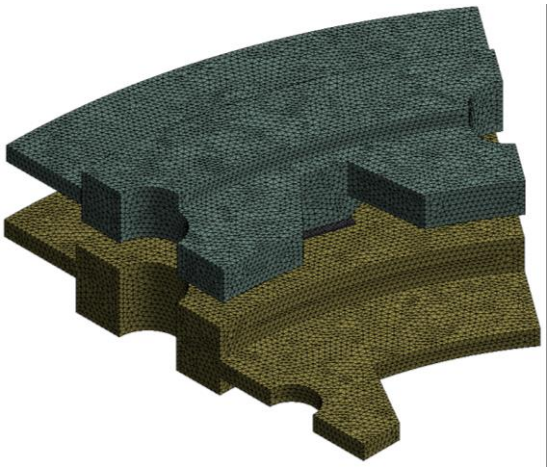
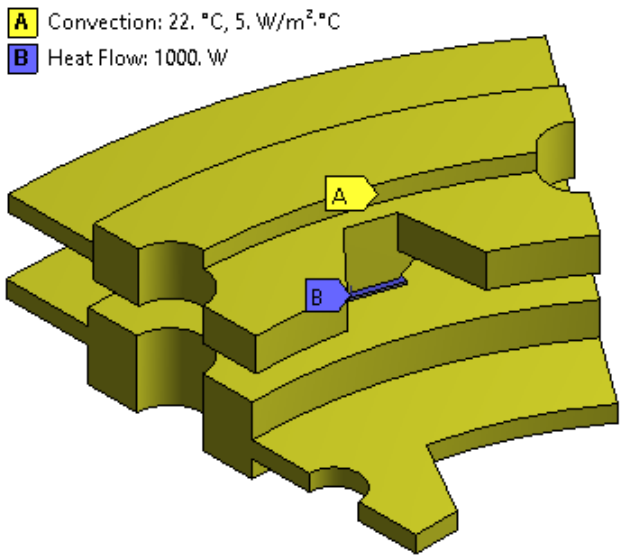


Figure 6.6: Locations and types of fasteners used in the ICLD's assembly

The equivalent thermal network of high-side devices was extracted so that it can be included in the SPICE simulations presented in the next section. Given the symmetry of the ICLD's package, analyses were only carried out for a 1/10 section of the geometry, as shown in Figure 6.7. Material properties and boundary conditions used in this transient thermal analysis are identical to those presented in section 4.4.2.



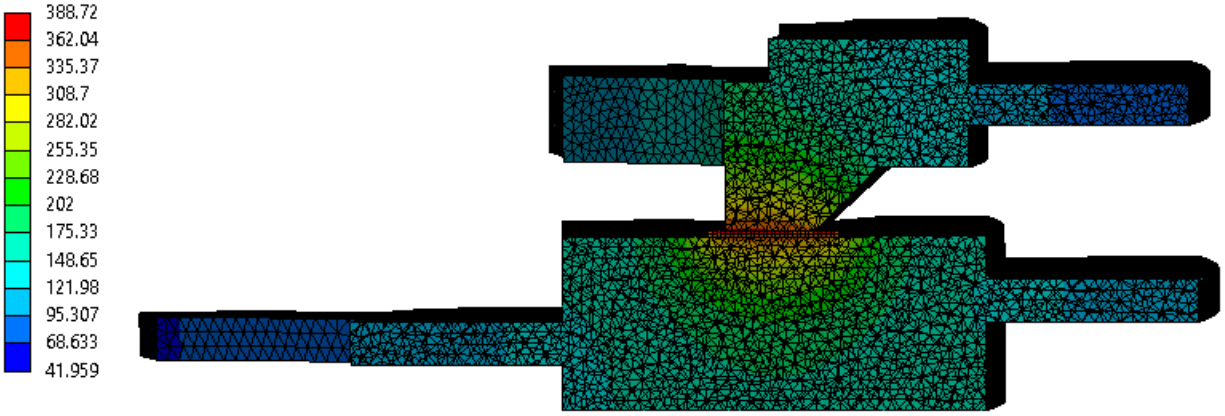
(a)



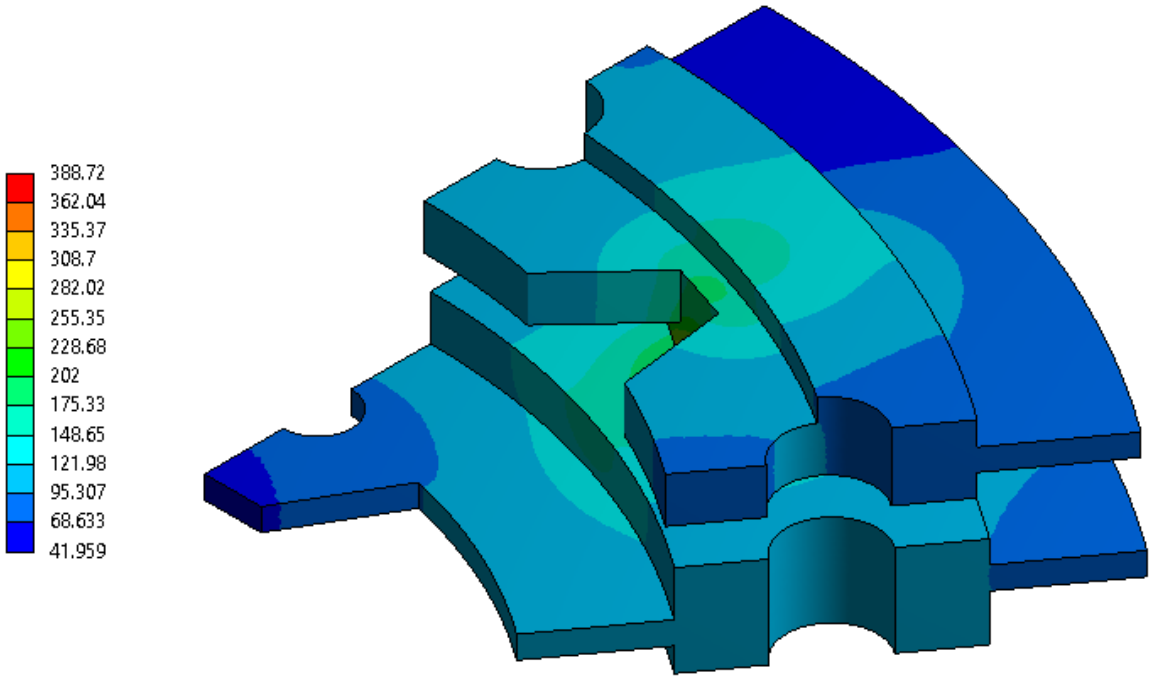
(b)

Figure 6.7: (a) Analyzed geometry & mesh, and (b) boundary conditions

The temperature distribution seen by the structure after 0.5 seconds was found as shown in Figure 6.8. A cross-sectional view of the analyzed structure shows a maximum temperature of 389°C at the center of the top surface of the die. This is expected as the heat load was applied to that surface. The maximum temperature-rise in the structure from the initial temperature of 22°C was found with respect to time as shown in Figure 6.9.



(a)



(b)

Figure 6.8: Temperature distribution in an (a) cross-sectional and (b) isometric views of analyzed geometry after 0.5s

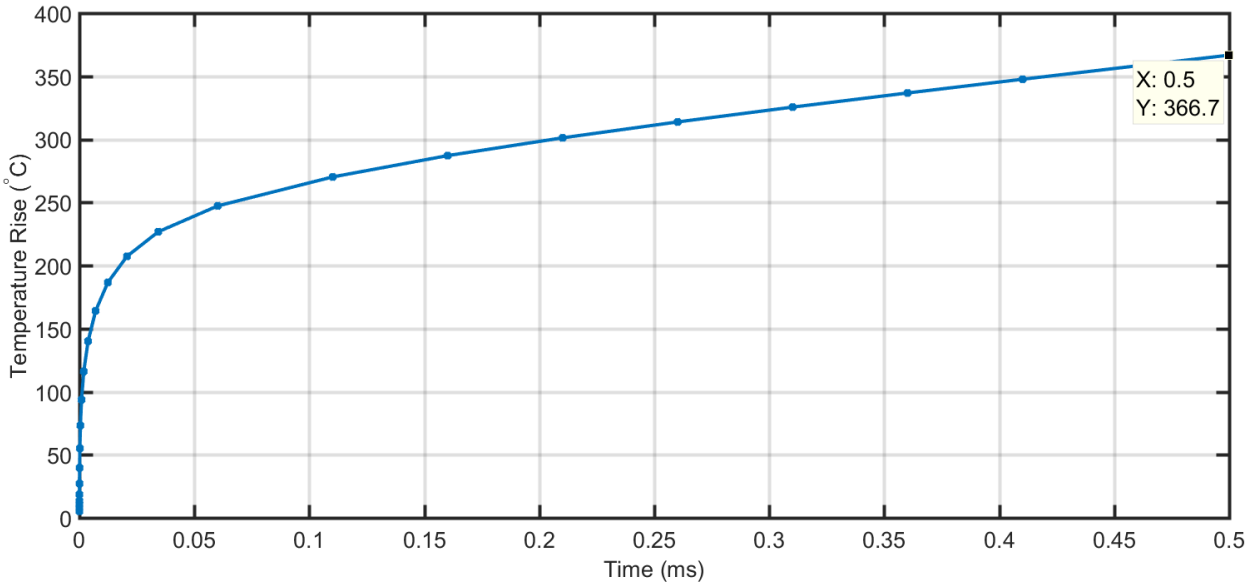


Figure 6.9: Maximum temperature rise in ICLD structure vs. time after 1kW heat load at *t=0*

The thermal impedance of the structure was found by dividing the maximum temperature rise by the heat load, as shown in Figure 6.10. A foster thermal network was then curve fitted to this

impedance, as compared in the same figure. The RC parameters of the fitted network are given in Table 6.2. The form of the fitted function was given by (2.98).

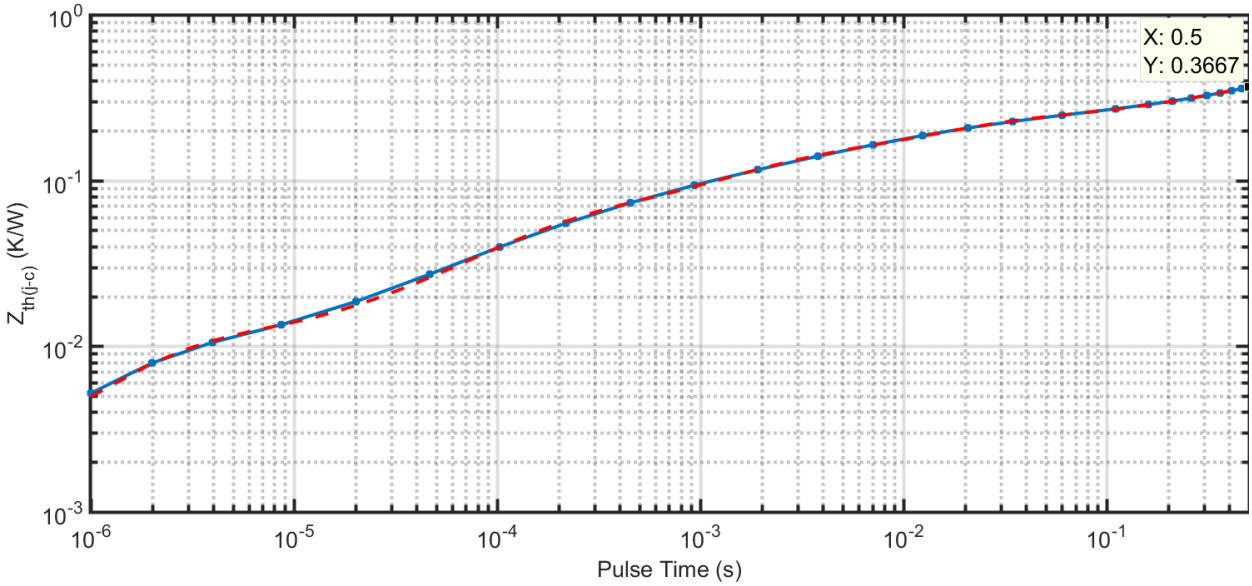


Figure 6.10: FE-based thermal impedance vs. curve fitted foster network impedance

Table 6.2: Foster network curve fitting parameters for high-side devices

i	R_i (mΩ)	C_i (F)
1	0.0719	0.0219
2	0.1124	2.8714
3	0.0101	0.0002
4	62.7124	9.6472
5	0.0996	0.1592
6	0.0434	0.0029

C) Printed Circuit Boards

Printed Circuit Boards (PCBs) are needed to establish internal electrical connections between the components of the ICLD, as well as external connections to the anode and cathode terminals. The bottom side PCB has the schematic shown in Figure 6.11, and layout shown in Figure 6.12. It establishes connections between the gate pads of the high-side devices (G_{high1}- G_{high10}) through

wire bonds, the output of the ICLD (Cathode (external)) through a ring terminal connection to the bottom side of the PCB, and the top-side PCB through a copper ring structure at the centre of the ICLD. This PCB fits in a recess on the high-side drain structure, and though this establishes electrical connection to that structure. External connection to the high-side drain (Anode (external)) is then established from the bottom side of the PCB through lug type connectors. Four copper blocks arranged around the centre of the ICLD route the anode to the top-side PCB.

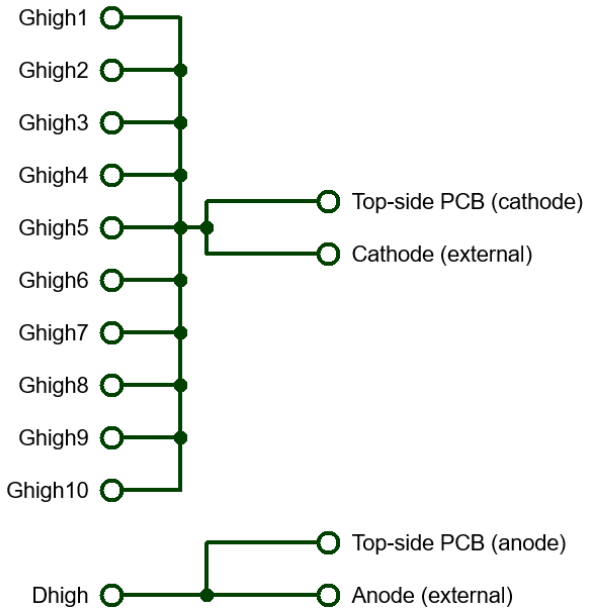
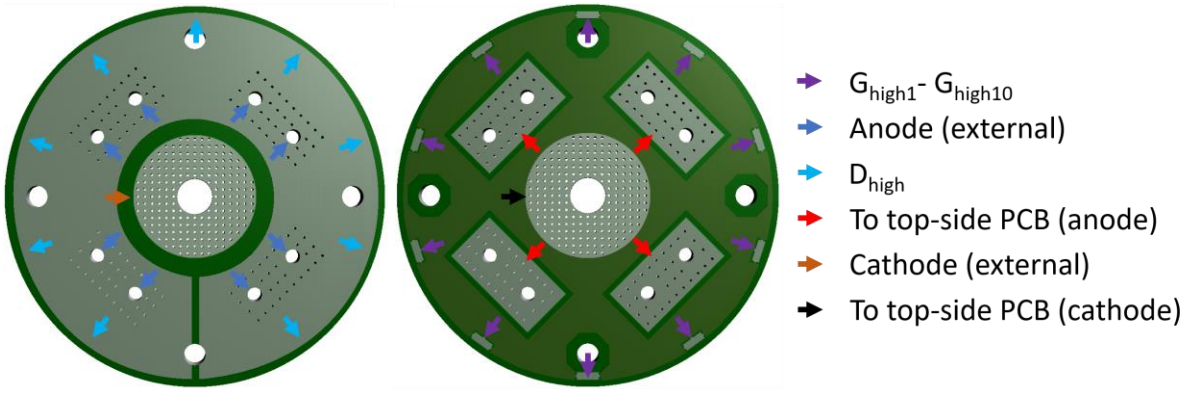


Figure 6.11: Schematic of bottom-side PCB



(a) (b)

Figure 6.12: (a) Bottom and (b) top views of bottom-side PCB

In addition to sealing the top-side of the ICLD, the top-side PCB houses the low-side JFET and snubber circuitry, as shown in the schematic diagram of Figure 6.13 and layout shown in Figure 6.14. The top-side PCB fits in a recess on the high-side source structure, and through this establishes electrical connection to S_{high}. The drain of the low-side FET is connected to S_{high}, and the gate & source terminals to the cathode. Finally four snubber branches distributed symmetrically on the PCB are connected between the anode and cathode. Values for these capacitors and resistors were found from simulations, as discussed in the next section.

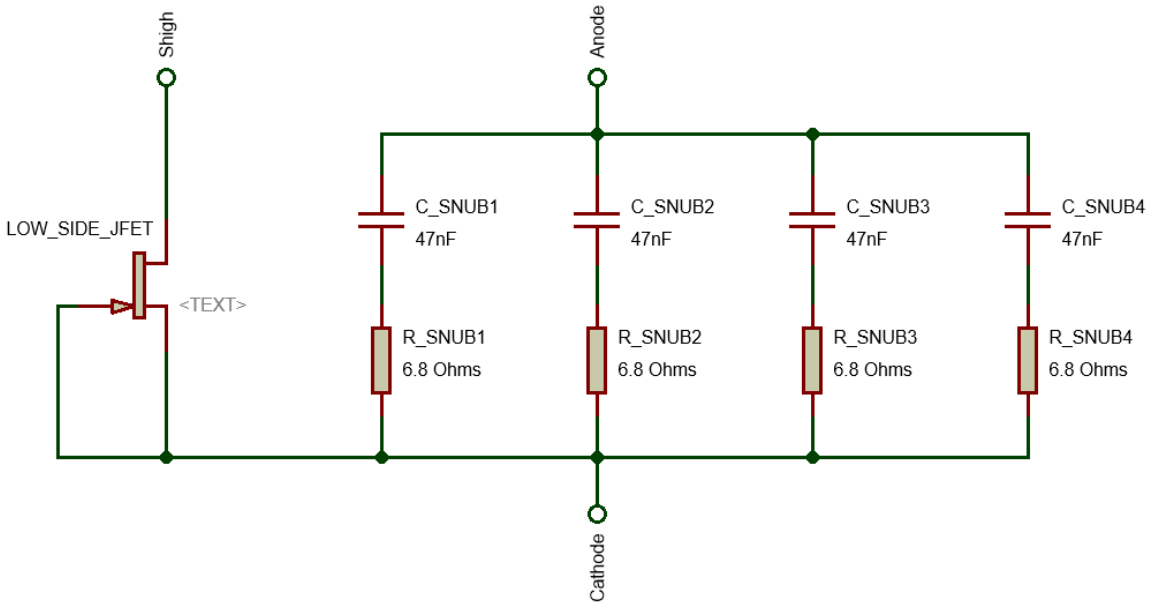
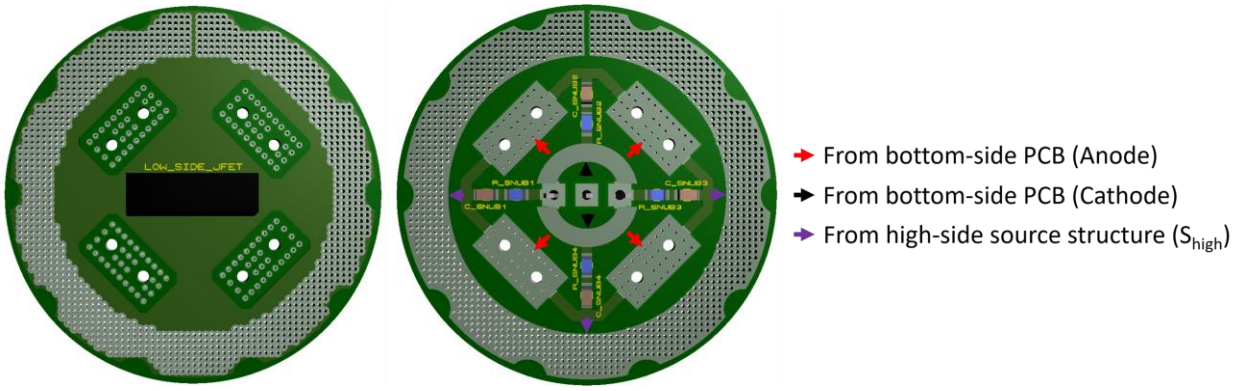


Figure 6.13: Schematic of top-side PCB

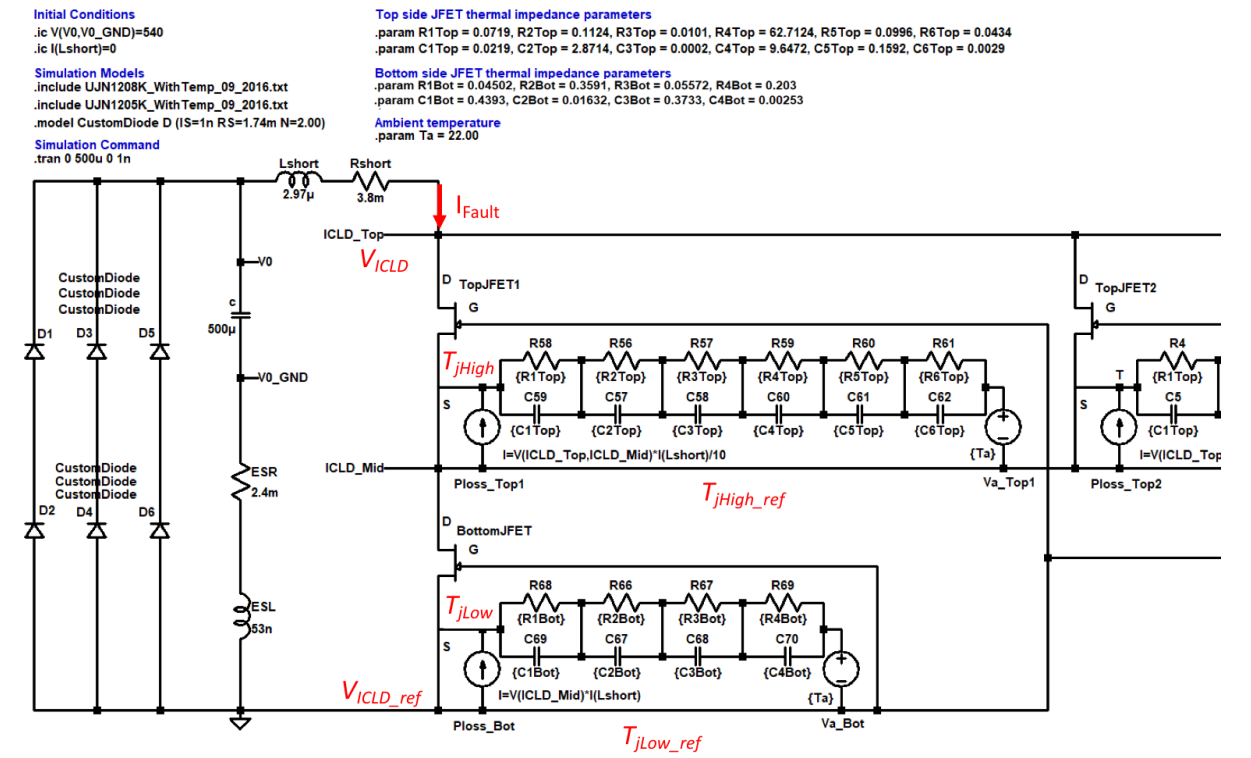


(a) (b)

Figure 6.14: (a) Top and (b) bottom side views of top-side PCB

6.2.2. Performance Analyses

This section details simulation analyses of the designed ICLD to demonstrate its functionality and capability. The simulation circuit show in Figure 6.15, includes an equivalent DC-link capacitor model with *C*, *ESL*, and *ESR* of 500µF, 53nH and 2.4mΩ respectively, and an equivalent fault impedance (*Rshort* and *Lshort*) of 3.8mΩ and 2.97µH respectively. Values for these parameters are as extracted in Chapter 3 for the experiment setup the CLD has been tested in. As with previous CLD simulations, the capacitor is initially charged up to 540V, and an initial current of 0A is flowing through the fault branch. The schematic also includes an equivalent ICLD model which utilises SiC-JFET manufacturer's SPICE models, as discussed in Chapter 5, and thermal equivalent circuits attached to these models, as extracted in 6.2.1.



(a)

(b)

Figure 6.15: (a) Zoomed, and (b) full ICLD performance simulation circuit

Simulated ICLD fault current (I_{Fault}) is shown in Figure 6.16 along with simulated currents obtained with a single and 10 parallel CLDs for comparison. The results demonstrate significant reduction in the magnitude of fault currents achieved with the ICLD (more than 72% and 96% reductions in peak currents compared with single and 10 parallel CLDs respectively). Furthermore, simulated temperatures of the high and low side JFETs (T_{jHigh} - T_{jHigh_ref} and T_{jLow} - T_{jLow_ref} respectively) demonstrate significant increase in operation time, as shown in Figure 6.17. While the CLD configuration is limited in operation to a few microseconds, the designed ICLD can operate for up to 500µs. The limit may be extended to milliseconds by replacing the plastic packaged low-side JFET (limited to 175°C junction temperature) with a higher temperature solution (metal hermetic packaging or high-side JFET like solution).

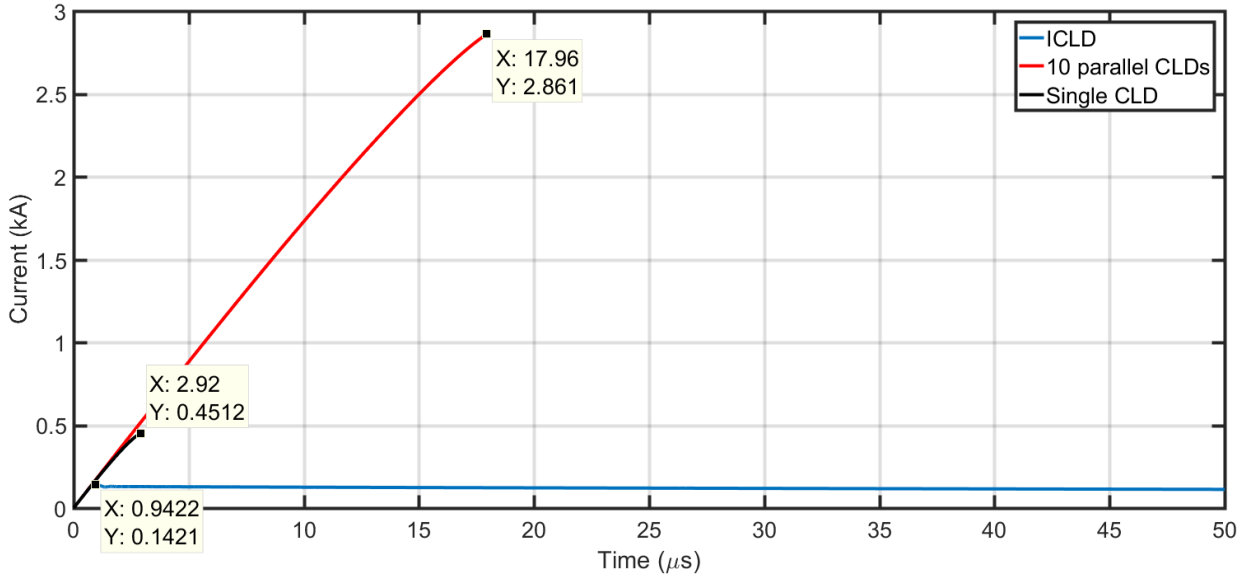


Figure 6.16: Simulated ICLD current

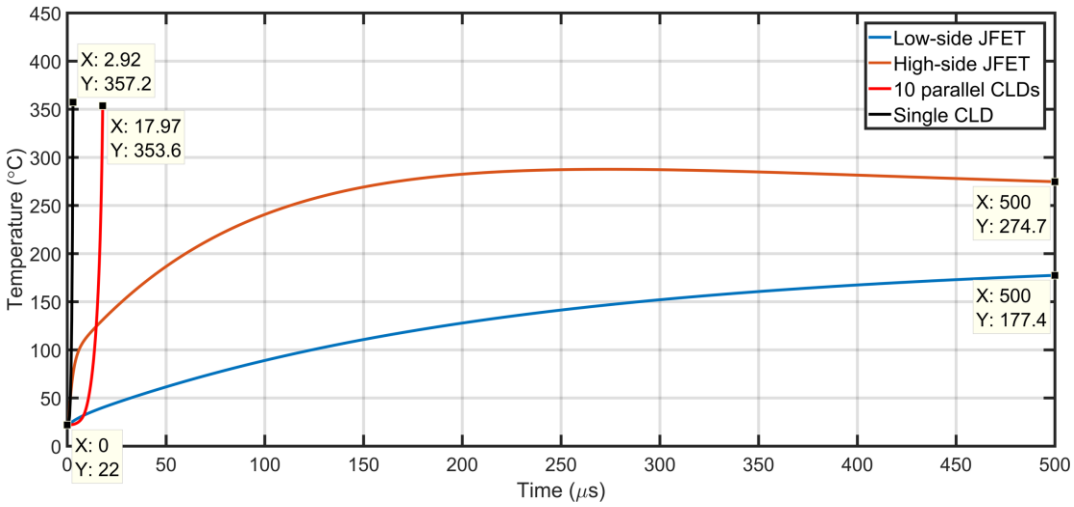


Figure 6.17: Simulated JFETs temperatures

Finally, simulated voltage across the CLD is shown in Figure 6.18. Results show a ≈100V overshoot due to stray inductances accounted for in the SPICE models of the JFETs, as specified in Appendix B. A higher overshoot is expected in application due to additional stray inductances in the packaging of the ICLD. To limit such overshoots, four snubber branches distributed symmetrically on the top-side PCB were added to the design, with 47nF of capacitance and 6.8Ω of resistance in each branch, as shown in Figure 6.13. Those are starting values that can be changed based on experimental testing. This is a more conventional approach for selecting values of snubber components, as opposed to complex finite-element based stray parameters extraction methods.

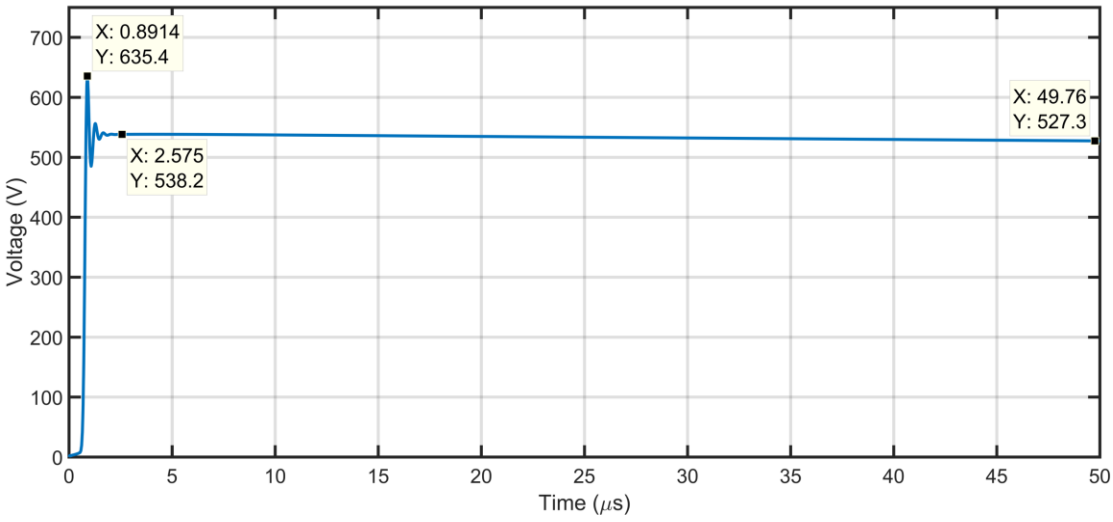
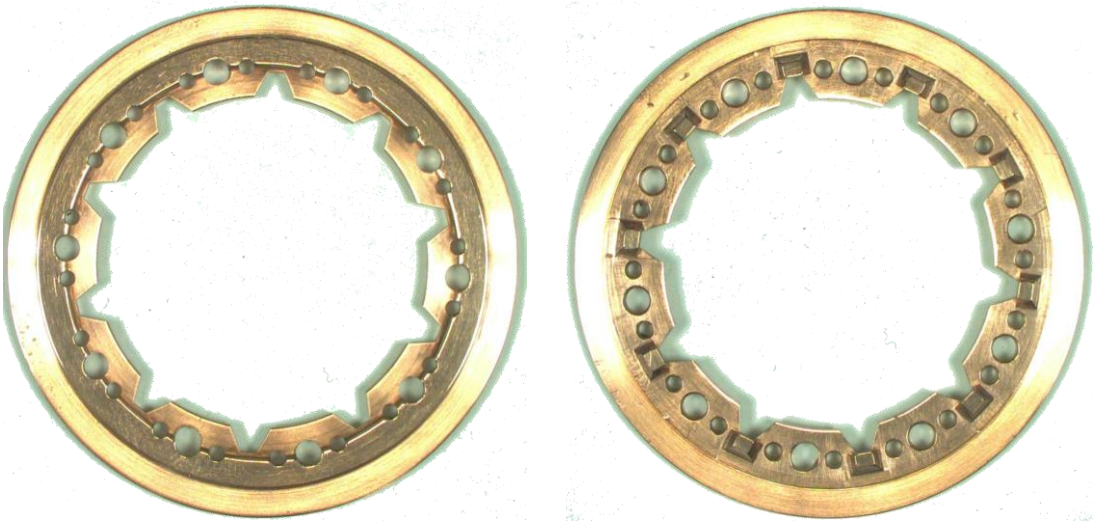


Figure 6.18: Simulated ICLD voltage

6.3. Fabrication

6.3.1. Components

Designed copper structures were machined out of copper according to the dimensions provided in Appendix D, as shown in Figure 6.19 and Figure 6.20 for the high-side source and drain structures respectively. Machining work for these parts was performed by JKP Engineering Ltd, Sheffield, United Kingdom.



(a) (b)

Figure 6.19: (a) Top and (b) bottom views of manufactured high-side source structure

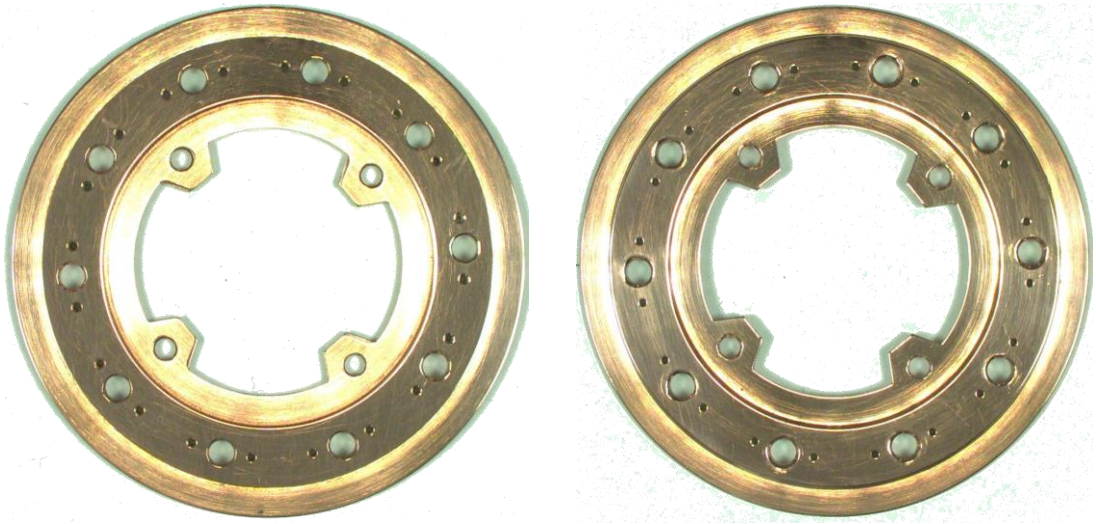
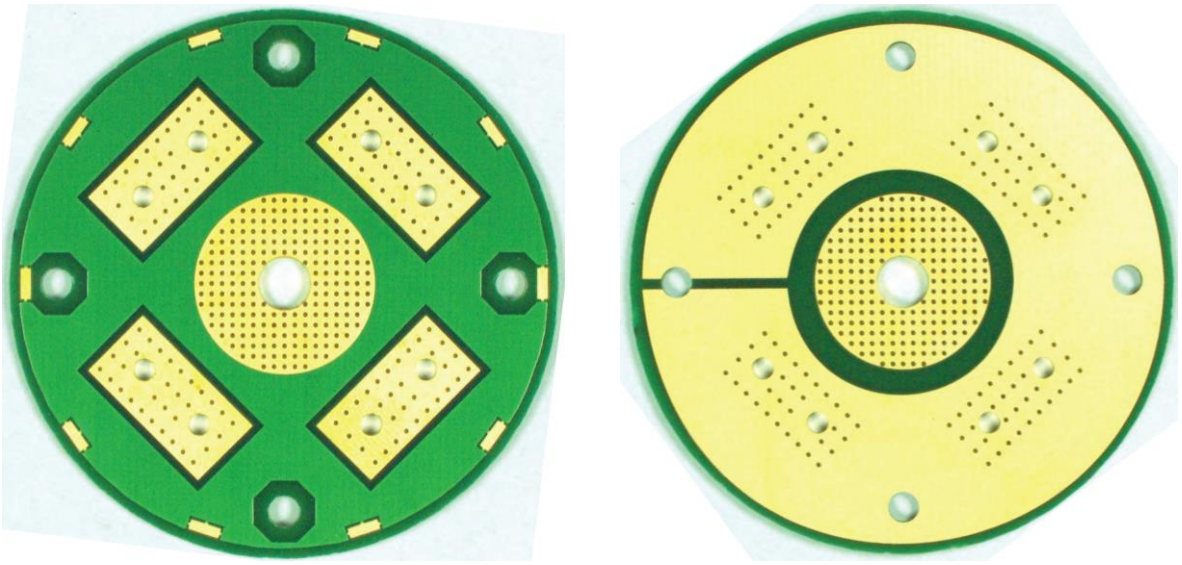


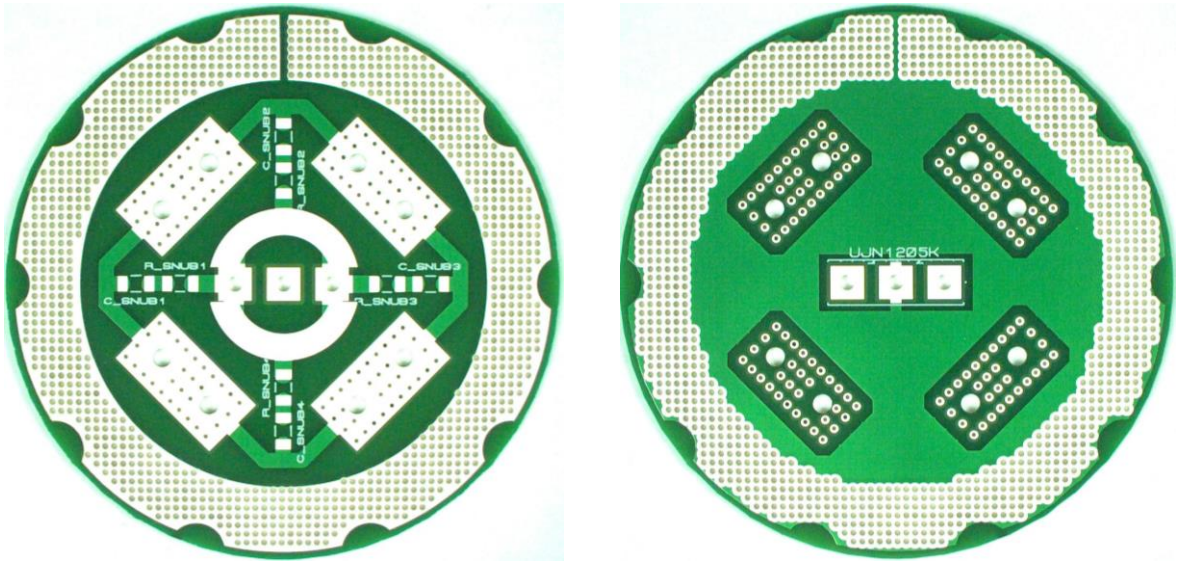
Figure 6.20: (a) Top, and (b) bottom views of manufactured high-side drain structure

The designed PCBs were manufactured according to the schematics and layouts detailed in section 6.2.1C, as shown in Figure 6.21 and Figure 6.22 for the bottom and top side PCBs respectively. Both PCBs were 2-layered with 1oz copper, FR4 laminate and gold/nickel finish for the bottom side PCB to enable wire bonding to the pads.



(a) (b)

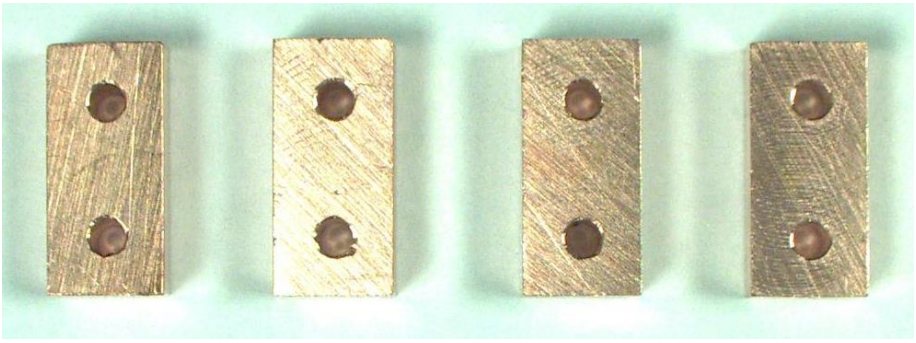
Figure 6.21: (a) Top, and (b) bottom side views of manufactured bottom-side PCB



(a) (b)

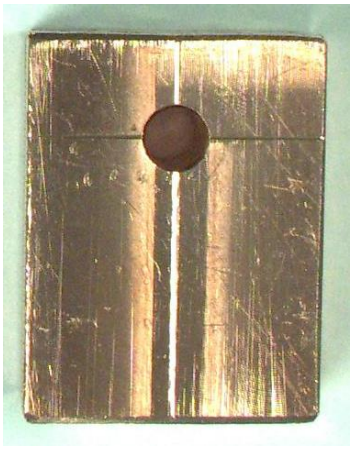
Figure 6.22: (a) Top, and (b) bottom views of manufactured top-side PCB

Some copper structures needed for the ICLD were manufactured locally at the university workshop, as they required less precision machining. Those parts include four rectangular copper blocks, shown in Figure 6.23 (a), needed for establishing an anode connection between the top and bottom side PCBs. They also include a circular copper block shown in Figure 6.23 (b), for establishing a cathode connection between the top and bottom side PCBs. That block was designed such that it can house the head of an M5 brass screw used for the cathode's ring connector on the bottom side of the ICLD. Finally, a 10m thick rectangular copper block shown in Figure 6.23 (c) was manufactured to be mounted on the back of the low-side device as a thermal mass in place of a heatsink. Dimensions of these parts are specified in Appendix D.



(a)

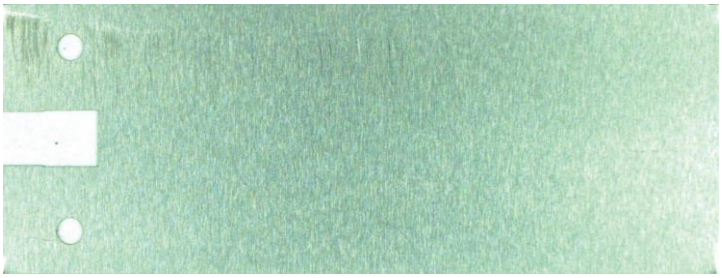
(b)



(c)

Figure 6.23: Other manufactured ICLD copper structures: (a) rectangular and (b) circular blocks for anode and cathode connection between top and bottom side PCBs, and (c) thermal mass for low-side JFET

Two stencils were designed to hold the SiC-JFET die in place during assembly of the ICLD. Specifically, these stencils were needed to restrain the dies from moving during wire bonding before they are pressured by the high-side source structure, as will be further discussed in the next section. The two stencils are to be placed on top of each other. The bottom-side stencil, shown in Figure 6.24 (a), restrains the die from moving in the planer/horizontal direction. Whereas, the top-side stencil, shown in Figure 6.24 (b), restrains the die from moving in the vertical direction. These stencils were laser cut by Newbury Electronics Ltd within ±16μm of the dimensions specified in Appendix D. More details on the use of these stencils will be presented in the next section.



(a)

(b)

Figure 6.24: Top view of manufactured (a) bottom, and (b) top stencils

Similar to the design of the CLD, the ICLD also utilizes ceramic fasteners, shown in Figure 6.25. 10 of these fasteners were distributed around the ICLD to hold the structure together and apply pressure on high side devices.

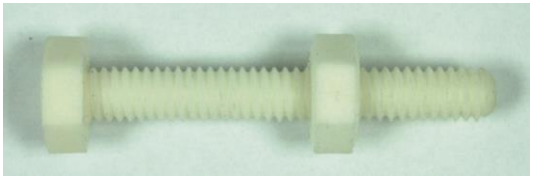


Figure 6.25: Picture of M4 x 20 ceramic fastener used in ICLD assembly

6.3.2. Assembly

This section details the steps that were taken to assemble the ICLD, starting with the components described above and ending with a packaged device that is ready for testing.

1- Metal polish was used to polish surfaces of the copper structures that contact the die to remove any corrosion that may have formed since last polished. The surfaces are then cleaned with a solvent cleaner to remove any residues of dirt or grease. A zoomed view of those surfaces after this process is shown in Figure 5.29.

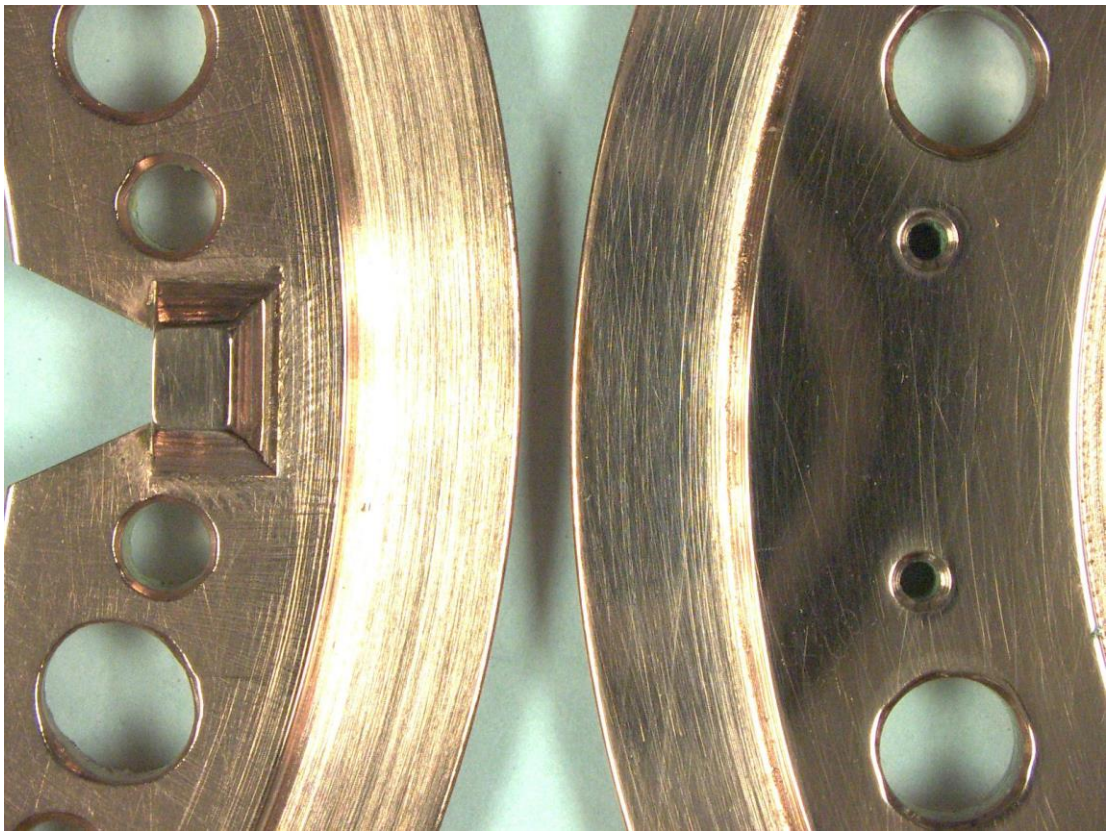


Figure 6.26: Zoomed view of surfaces that contact the die after polishing and cleaning

2- The bottom positioning stencil is placed on the high-side drain structure, the die is picked using a vacuum pencil and placed in the opening of the stencil. The top stencil is then placed over the bottom stencil, M1 stainless screws inserted, and the die is fixed in place. This process is repeated for all 10 dies, as shown in Figure 5.30.

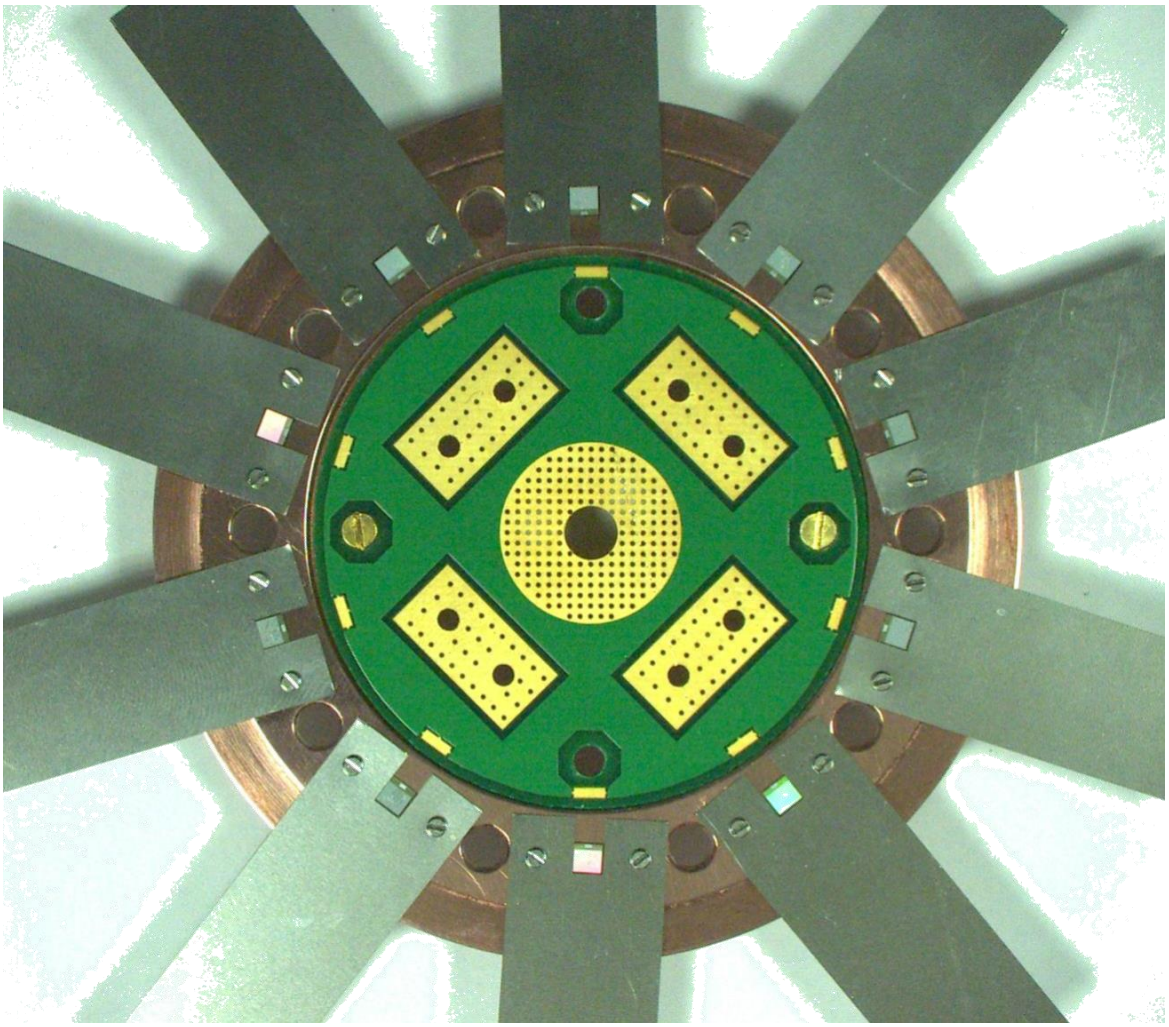
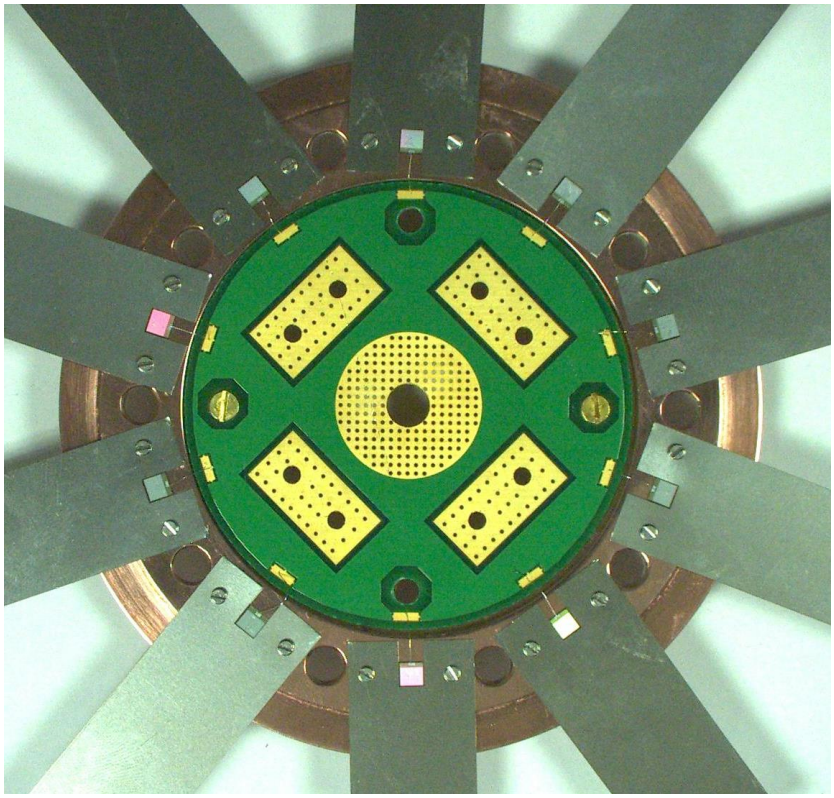
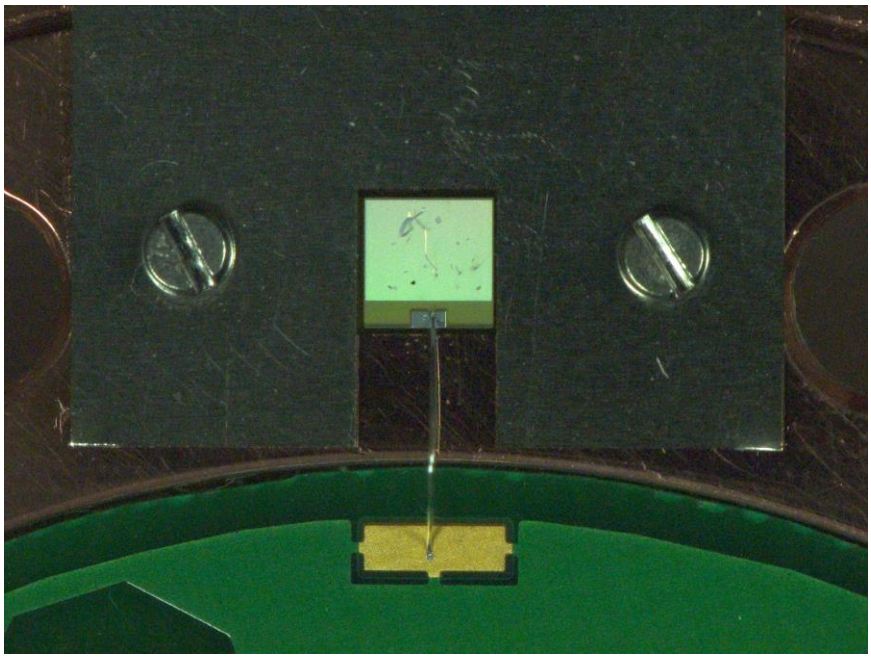


Figure 6.27: View of die positioning setup

3- The low-side PCB is then attached, and a F&K Delvotec 5410 Wire Bonder is used to connect the gate pads of the dies to the corresponding pads of the PCB, as shown in Figure 6.28. Due to the limited current flow expected through the gate and small area of the gate pads (0.7mm x 0.35mm), 100μm thick aluminium wires were used for the bonding.



(a)



(b)

Figure 6.28: (a) Full scale and (b) zoomed view of structure after wire bonding

4- The high-side source structure is then attached, ceramic screws inserted and tightened up, M1 nuts are unfastened and screws removed through the top, and stencils slide out through the side, as shown in Figure 5.31 .

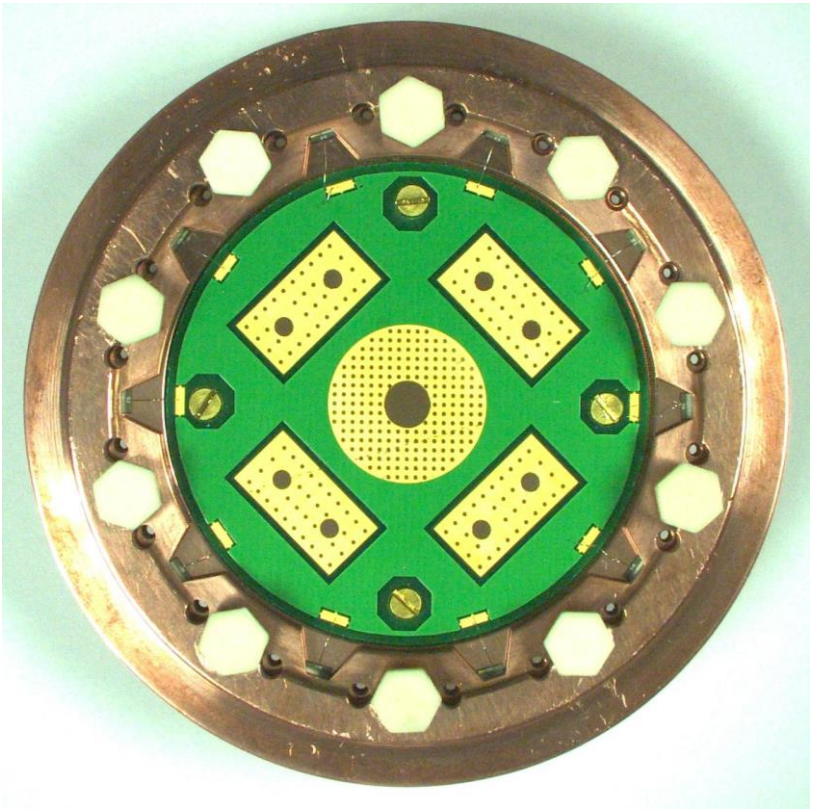


Figure 6.29: Picture of ICLD after attaching high-side source structure

5- The partially packaged device was then tested on the curve tracer to validate that the ON-state resistance is as expected. This confirms that all high-side dies are connected and functioning as expected. Results of this test are discussed in the next section.

6- After the connectivity and functionality of the partially packaged device is confirmed, the assembly is resumed. Binder clips are used to hold the high-side drain and source structures together, as shown in Figure 6.30. This was performed so that the ceramic screws can be removed, and remaining components assembled.

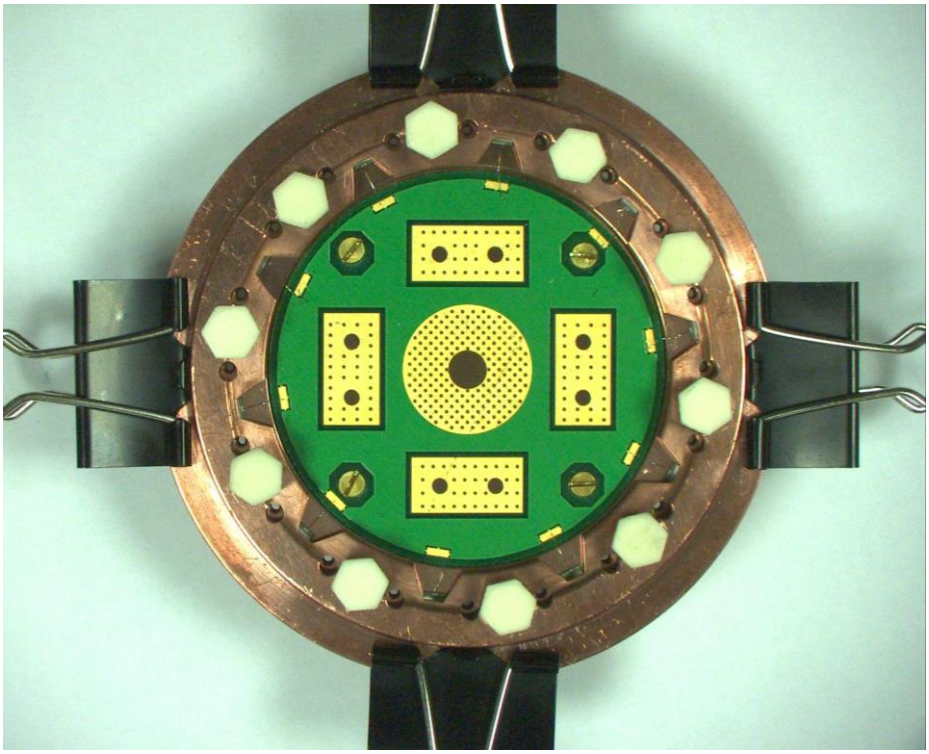
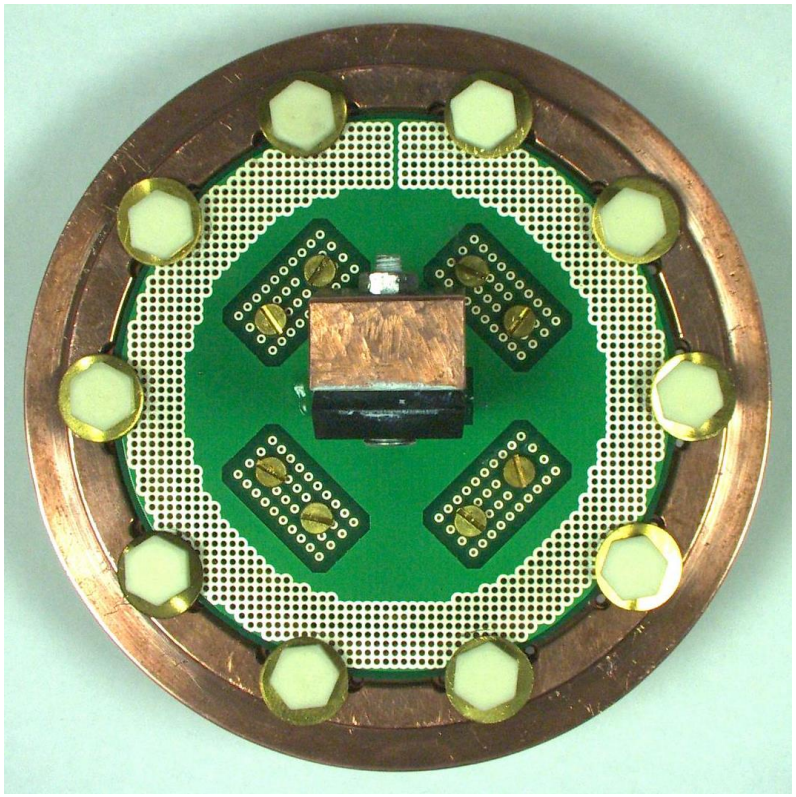
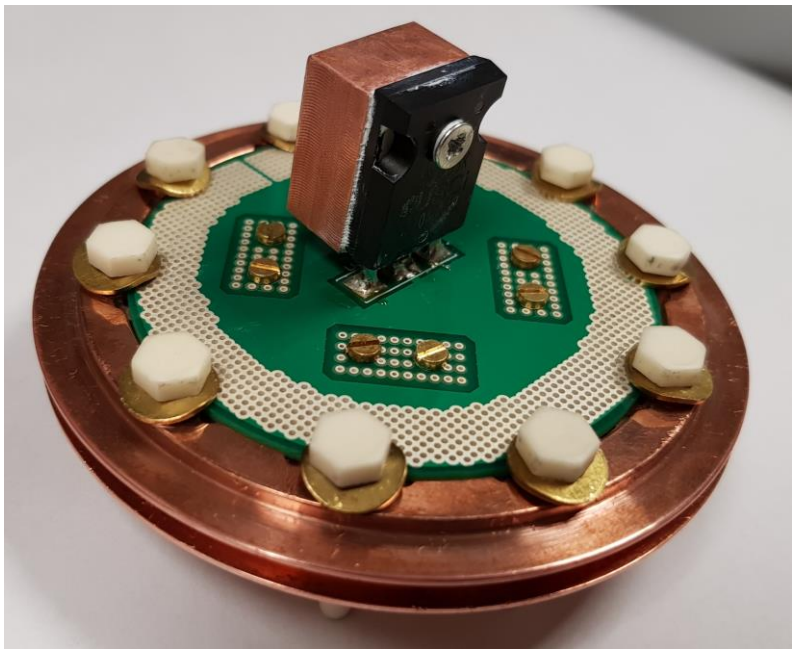


Figure 6.30: Picture of ICLD structure held by binder clips so that the ceramic screws can be removed, and remaining components assembled.

7- After the ceramic screws are removed, copper structures connecting top and bottom side PCBs are placed on their designated pads on the bottom side PCB, top-side PCB placed on the top, M2 brass screws inserted through the PCBs, and then fastened. The ceramic screws are then also fastened, and binder clips removed, as shown in Figure 6.31.



(a)



(b)

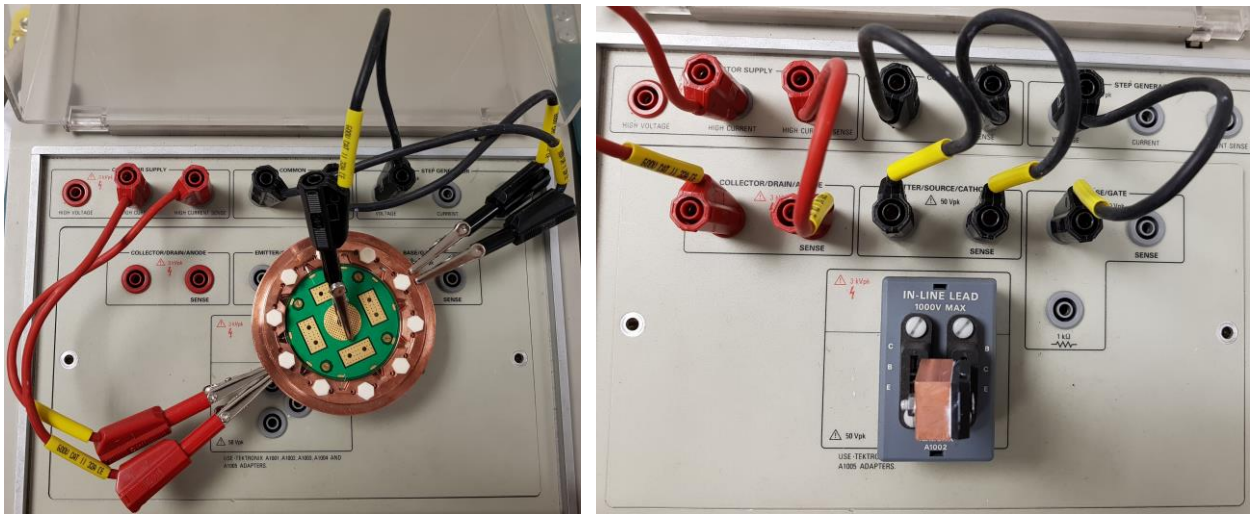
Figure 6.31: (a) Top and (b) isometric picture of assembled ICLD

6.4. Testing

This section detailed testing that was performed on the partially assembled and fully assembled ICLDs. Testing on the partially assembled ICLD was performed to verify the connectivity of high-side dies through measuring the I(V) characteristics between the drain and source structures. Whereas, testing on the fully assembled ICLD was performed to verify the current limiting characteristics of the device through measuring the anode-to-cathode I(V) characteristics.

6.5. Testing of Partially Assembled ICLD

The Tektronix 371B curve tracer was used to measure the I(V) characteristics of the partially assembled ICLD (between drain-to-source structures) to verify the connectivity of high-side devices. Measurement was also performed on a single plastic packaged device containing the same die for comparison. The setup used for these tests is shown in Figure 6.32.



(a) (b)

Figure 6.32: I(V) characteristics measurement setup of (a) partially assembled ICLD, and (b) single plastic packaged JFET

The measured I(V) characteristics of partially assembled ICLD is shown in Figure 6.33. For comparison, the figure also includes measured characteristic of a single plastic packaged device scaled by a factor of 10 with respect to current. The typical ON-state resistance of the die at 20A of current is given in the datasheet as 45mhoms at gate-to-source voltage of 0V and junction temperature of 25C. When 10 dies are paralleled, the typical resistance is expected to be 4.5mohms,

at 20A of current per device (or 200A combined) at 0 gate-to-source voltage, and 25C junction temperature. Measured resistance of the partially assembled ICLD was found to be 5.1mohms, 13% larger than typical value given for the dies only. Measured resistance of the plastic packed device was found to be 49mohms, which is equivalent to 4.9mohms if 10 of these devices are to be paralleled. This value matches that measured for the ICLD within 4%, verifying that a good electrical connection is established to all high-side devices.

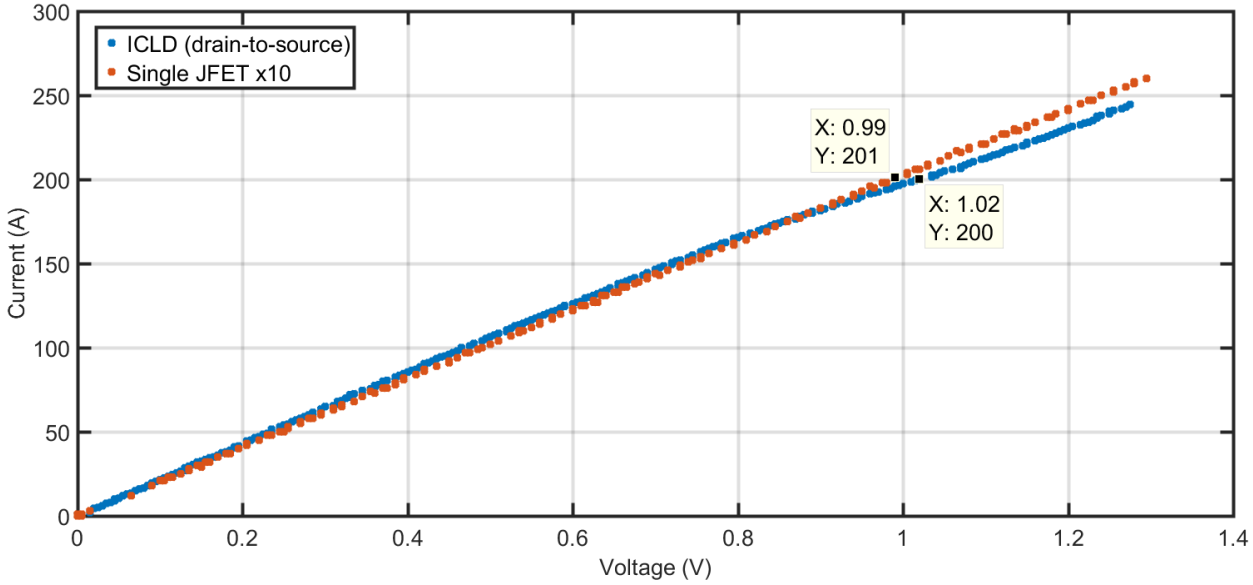


Figure 6.33: Measured I(V) characteristics of partially assembled ICLD and single plastic-packaged JFET scaled by 10 with respect to current

6.6. Testing of Fully Assembled ICLD

The fully assembled ICLD was tested to verify its current limiting characteristics. As explained in the introduction, the ICLD's circuit configuration achives current saturation at a significanlty lower value than if the high-side devices are only paralleled. Thus, achiving current sharing among multiples device, while maintianing low saturation level. This was validated expermentally by measuring the I(V) characteristics of the ICLD (anode-to-cathode) using the setup shown in Figure 6.34.

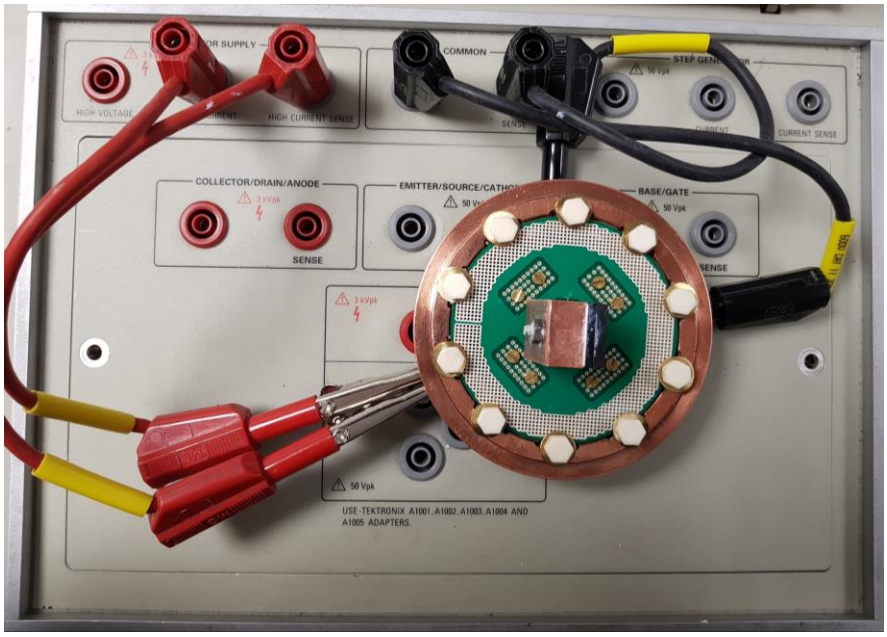


Figure 6.34: I(V) characteristics measurement setup of fully assembled ICLD

Experimental results obtained from this measurement are shown in Figure 6.35. For comparison, the figure also includes measured I(V) characteristics of a single plastic packaged JFET with V_{GS} = 0 (in CLD configuration). It can be seen that current limiting (saturation) occurs at significantly lower value with the ICLD than with a single CLD.

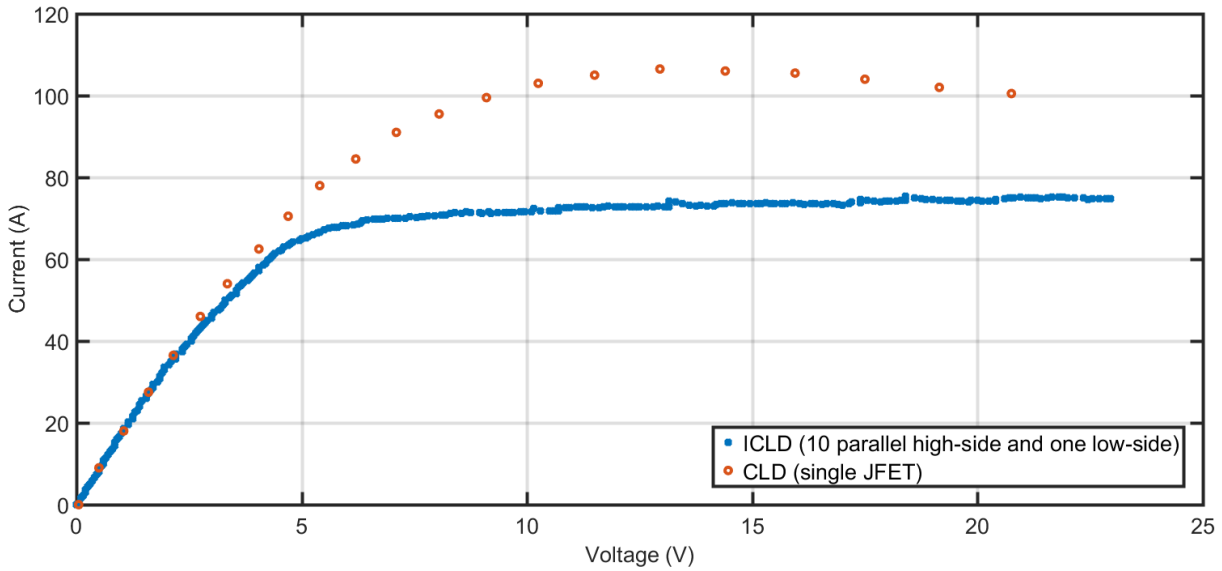


Figure 6.35: Measured I(V) characteristics of fully assembled ICLD and single plastic-packaged JFET with V_{GS} = 0 (CLD configuration)

6.7. Summary and Conclusions

In this chapter the concept of an Integrated Current Limiting Diode (ICLD) was presented, as well as the design, fabrication, and testing of a Proof-Of-Concept (POC) demonstrator. The proposed ICLD circuit topology achieves current sharing among multiple semiconductor devices without increasing saturation level (current limit). Thus, allowing for extended operation times of the current limiter. The POC design utilized 10 high-side SiC-JFETs handling and sharing most of the ICLD's power losses during a fault event, and one low-side JFET with relativity insignificant losses. The devices are integrated into a custom designed high temperature packaging, with dual side pressure contact to the high-side devices. Thermoelectrical simulations were carried out, which demonstrated significant improvement in operation time with the proposed POC ICLD. However, some risks have been identified with the proposed design related to the packing of the dies in such highly integrated form and achieving the anticipated current and voltage characteristics. To alleviate these risk, the POC demonstrator was fabricated, assembled, and tested. The assembly was found to be challenging, but possible with the aid of stencils, fasteners, and clips. Curve tracer measurements of the fabricated device demonstrated the significance of the proposed configuration: compared to a CLD, an ICLD achieves comparable on-state resistance under nominal conditions, and lower saturation level during a fault even with losses distributed amount multiple semiconductor devices (10 for the POC).

Chapter 7: Contributions and Future Work

The objective of this PhD is to design, build and test a current limiting diode which limits the magnitude of fault current to 2-3 times its nominal value and operate for 10μs to 5s at an ambient temperature of 85°C. The current limiter would be integrated with a voltage source converter used to drive a starter/generator machine for a jet engine. Before the design work can commence, the value of including such current limiter to the system had to be demonstrated. This was accomplished by analyzing the response of voltage source converters to the worst case fault condition (line-to-line short-circuit) with and without a current limiter. These analyses demonstrated significant reduction in fault current and components stresses when a CLD is included. The design, build, and test of a Proof-Of-Concept (POC) CLD was then presented. The POC CLD uses a single SiC-JFET die integrated into the converter busbars. The die is sandwiched between two copper structures providing the electrical connections and thermal mass for instantaneous heat dissipation. Thermoelectrical analyses of this device predicted that it would be capable of limiting fault current for up to 10μs at a bus voltage of 270V. However, due to manufacturing deficiencies in the copper packaging, the device prematurely failed after about 7μs at a bus voltage of 250V. To extend the operational capabilities of the current limiter, the concept of an Integrated Current Limiting Diode (ICLD) was proposed. This circuit configuration allows paralleling multiple SiC-JFETs for current sharing without proportionally increasing the magnitude of fault current. A proof-of-concept ICLD was designed, built and, tested. Experimental testing of the POC ICLD demonstrated significant improvement in output characteristics as compared to a CLD. An ICLD composed of 10 parallel SiC-JFETS sharing the power losses was shown to limit the magnitude of fault current to the same value of a CLD composed of a single device, which significantly increases the expected operational capabilities (≈10x).

The following bullet points summarize the major contributions of this thesis:

- The second chapter of this thesis presented DC line-to-line short-circuit fault analyses of voltage source converters with significant improvement in accuracy over prior literature. The analyses accounted for various parameters and stages that were not previously considered, which significantly influence the obtained characteristics. The most important of those parameters are: the equivalent series inductance and resistance of the capacitors,

which induces significant additional stress on the converter diodes that was not previously accounted for, and the on-state voltage drop and turn-on voltage of the diodes, which also influence fault characteristics and time boundaries. In addition, the interaction between AC and DC side contributions were not previously considered, causing discrepancies within the results, that has now been addressed in the Combined Response section of that chapter.

- The third chapter of this thesis presented experimental validation of the DC line-to-line short-circuit fault analyses for the first time in literature. The experimental results were obtained using a single channel replica of 100kW dual-channel machine and drive designed and built for aerospace application.
- The fourth chapter investigates the feasibility of using SiC based CLDs for short-circuit protection of power converters. A physics-based SiC-CLD SPICE model is created. This model accounts for the CLD's junction temperature (T_j) and physical features effects on its response. An equivalent fault circuit which includes this model of the CLD is then thoroughly analyzed.
- In the fifth chapter, the design, fabrication, and test of a proof-of-concept current limiting diode for short-circuit protection of voltage source converters is presented. This demonstrator utilizes a single commercial off-the-shelf Silicon Carbide Junction Field Effect Transistor (JFET) with the gate and source terminals externally connected. The SiC JFET die is integrated into a custom designed high temperature packaging. The die is pressure contacted by a copper busbar acting as the electrical connections (cathode and anode) and thermal masses for the heat generated by the CLD to be dissipated to.
- In the sixth chapter, the concept of an integrated current limiting diode is presented, as well as the design, fabrication, and testing of a proof-of-concept demonstrator.

The future work following this dissertation could be outlined as follows:

1- Inclusion of a more representative machine model in the DC line-to-line short-circuit fault analyses. This model may include secondary effects, such as machine saturation effects at high currents.

2- The experimental validation would also need to include more representative AC source such as a high power machine or supply, which were not available during the course of this work.

3- Fault analyses of more complex power system typologies such as those with distributed generation, energy storage, or modular multilevel converters.
4- Investing the effects of contact resistance on CLD performance, as well as methods to improve this resistance. This can include an optimization of the applied pressure on the die, coating of contact areas with a less corrosive material (gold flush), or adding layers of intermediate materials such as Molybodium.
5- Improving the fidelity of SiC-JFETs' simulation models in the saturation region for more accurate predictions of CLD and ICLD performances.
6- Redesign of ICLD POC for high-voltage short-circuit testing including Copper structures, snubber circuitry and PCB layout & traces.

Appendix A: MATLAB Instrument Control Toolbox Power Supply Setup and Trigger

```
%% Setup Connection

% Find a VISA-GPIB object.
obj1 = instrfind('Type', 'visa-gpib', 'RsrcName', 'GPIB0::1::INSTR', 'Tag', '');

% Create the VISA-GPIB object if it does not exist
% otherwise use the object that was found.
if isempty(obj1)
   obj1 = visa('AGILENT', 'GPIB0::1::INSTR');
else
   fclose(obj1);
   obj1 = obj1(1);
end

fopen(obj1);

%% Setup Power Supply

% Reset
fprintf(obj1, '*RST');

% Wait for instrument to reset
pause (5)

% Setup instrument in 3 phase mode of operation
fprintf(obj1, 'SYSTem:CONFigure:NOUT 3');

% Wait for instrument to change mode
pause (10)

% Set initial output voltage (immediate-level)
fprintf(obj1, 'VOLT 0');

% Set initial output frequency
fprintf(obj1, 'FREQ 1000');
```

```
% Enable the output
fprintf(obj1, 'OUTP ON');

% Enable output to generate pulses when triggered
fprintf(obj1, 'VOLT:MODE PULS');

% Set the voltage dropout (triggered level)
fprintf(obj1, 'VOLT:TRIG 150');

% Set pulse width for 9 cycles
fprintf(obj1, 'PULS:WIDT .009');

% Respond to IEEE-488 bus triggers
fprintf(obj1, 'TRIG:SOUR BUS');

% Synchronize triggers to internal phase reference
fprintf(obj1, 'TRIG:SYNC:SOUR PHAS');

% Sets internal phase reference point to 90 degrees
fprintf(obj1, 'TRIG:SYNC:PHAS 0');

% Set to Wait-for-trigger state
fprintf(obj1, 'INIT:SEQ1');

%% Trigger Transient

fprintf(obj1, '*TRG');
```

Appendix B: Silicon Carbide Junction Field Effect Transistor SPICE Models

Original Model	Modified Model
.SUBCKT ujn1205z Drain Gate Source PARAMS:	.SUBCKT UJN1205z_L1 Drain Gate Source T PARAMS:
+ beta=5.28 beta_tce=-30 vth=-7.892 vth_tc=4.0e-4	+ beta=5.28 beta_tce=-30 vth=-7.892 vth_tc=4.0e-4
+ npow=1.4480 npow_tc=-5.000e-04 lambda0=0.05 lambda1=-1.100e-01	+ npow=1.4480 npow_tc=-5.000e-04 lambda0=0.05 lambda1=-1.100e-01
+ alpha=1.800 alpha_tc=-3.000e-03	+ alpha=1.800 alpha_tc=-3.000e-03
+ cdsa0=7e-12 cds0=8.82e-12 is0g=1.5000e-14	+ cdsa0=7e-12 cds0=8.82e-12 is0g=1.5000e-14
+ cgda0=40e-12 cgd0=900e-12 cgd_FC=0.94 cgd_M=0.70 cgd_VJ=2.7	+ cgda0=40e-12 cgd0=900e-12 cgd_FC=0.94 cgd_M=0.70 cgd_VJ=2.7
+ cgsa0=150e-12 cgs0=1125e-12 cgs_FC=0.94 cgs_M=0.53 cgs_VJ=2.7	+ cgsa0=150e-12 cgs0=1125e-12 cgs_FC=0.94 cgs_M=0.53 cgs_VJ=2.7
*Parasitics	*Parasitics
LD Drain D 1n	LD Drain D 1n
R_RD D Dint 0.001	R_RD D Dint 0.001
LS Source S 1n	LS Source S 1n
R_RS S Sint 0.001	R_RS S Sint 0.001
LG Gate G 1n	LG Gate G 1n
R_RG G Gint 0.5	R_RG G Gint 0.5
R_RGAC1 Gint Gjd 1.5	R_RGAC1 Gint Gjd 1.5
R_RGAC2 Gjd Gjs 2.75	R_RGAC2 Gjd Gjs 2.75
X_IDSGjd Dint Sint IDJFET PARAMS: beta={beta} lambda0={lambda0} lambda1={lambda1}	X_IDSGjd Dint Sint T IDJFET PARAMS: beta={beta} lambda0={lambda0} lambda1={lambda1}
X_IGSGint Gjd Sint IGATETOSOURCE	X_IGSGint Gjd Sint T IGATETOSOURCE
*Current	*Current
DBDD Gjd Dint DDBRKDWN	DBDD Gjd Dint DDBRKDWN
DBDS Gjd Sint DSBRKDWN	DBDS Gjd Sint DSBRKDWN
DDGI Gjd Dint DGI	DDGI Gjd Dint DGI

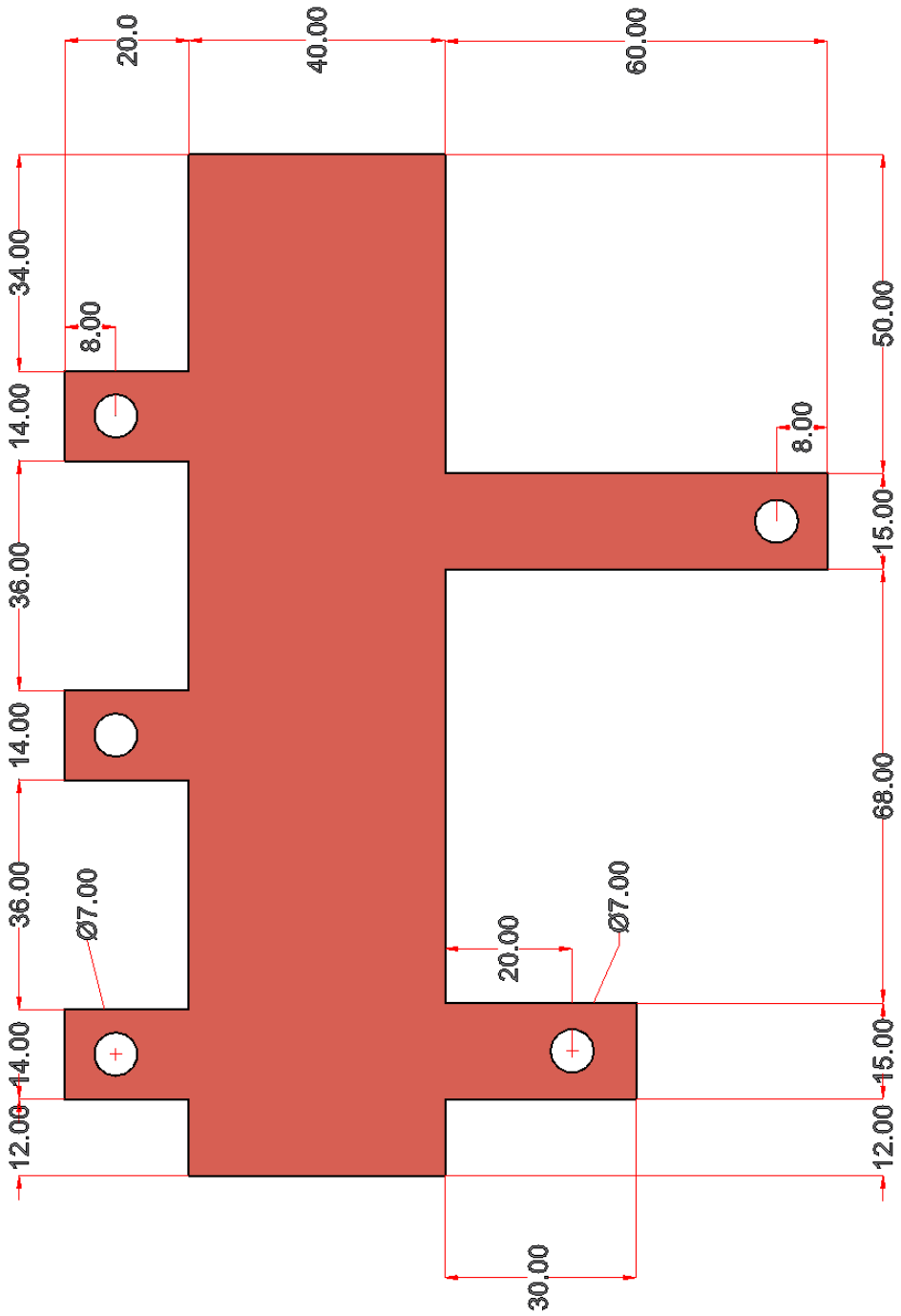
DDGSI Gjd Sint DGSI	DDGSI Gjd Sint DGSI
*Capacitance	*Capacitance
DGD Gjd Dint Diodecgd	DGD Gjd Dint Diodecgd
CGDa Gjd Dint {0.5*cgda0}	CGDa Gjd Dint {0.5*cgda0}
DGD2 Gjs Dint Diodecgd	DGD2 Gjs Dint Diodecgd
CGDb Gjs Dint {0.5*cgda0}	CGDb Gjs Dint {0.5*cgda0}
DGS Gjs Sint Diodecgs	DGS Gjs Sint Diodecgs
CGSa Gjs Sint {0.5*cgsa0}	CGSa Gjs Sint {0.5*cgsa0}
DGS2 Gjd Sint Diodecgs	DGS2 Gjd Sint Diodecgs
CGSb Gjd Sint {0.5*cgsa0}	CGSb Gjd Sint {0.5*cgsa0}
CDSint Dint Sint {cdsa0}	CDSint Dint Sint {cdsa0}
CGSint Gint Sint 1e-13	CGSint Gint Sint 1e-13
CDS D S 1e-13	CDS D S 1e-13
CGD G D 1e-13	CGD G D 1e-13
CGS G S 1e-13	CGS G S 1e-13
.Model DGI D IS=5.6e-20 N=5.8 XTI=7 ISR=0 NR=2.9 VJ=12.7 CJO=0 Rs=.9	.Model DGI D IS=5.6e-20 N=5.8 XTI=7 ISR=0 NR=2.9 VJ=12.7 CJO=0 Rs=.9
.Model DGSI D EG=3.26 IS=1.500e-14 N=3.71 XTI=15 ISR=0 CJO=0 Rs=.1	.Model DGSI D EG=3.26 IS=1.500e-14 N=3.71 XTI=15 ISR=0 CJO=0 Rs=.1
.MODEL DDBRKDWN D IS=1e-40 ISR=0 N=1000 IBV=1.133 NBV=4.004e2 BV=1600 TBV1=1e-6 Rs=0.2	.MODEL DDBRKDWN D IS=1e-40 ISR=0 N=1000 IBV=1.133 NBV=4.004e2 BV=1600 TBV1=1e-6 Rs=0.2
.MODEL DSBRKDWN D EG=3.26 IS=1e-40 XTI=1 N=1000 ISR=0 IBV=1.823e-6 NBV=87.54 BV=45 Rs=0.2	.MODEL DSBRKDWN D EG=3.26 IS=1e-40 XTI=1 N=1000 ISR=0 IBV=1.823e-6 NBV=87.54 BV=45 Rs=0.2
.MODEL Diodecgd D IS=1e-40 XTI=1 N=1000 ISR=0 CJO={cgd0} EG=3.26 FC={cgd_FC} M={cgd_M} VJ={cgd_VJ} IKF=0 RS=0.2	.MODEL Diodecgd D IS=1e-40 XTI=1 N=1000 ISR=0 CJO={cgd0} EG=3.26 FC={cgd_FC} M={cgd_M} VJ={cgd_VJ} IKF=0 RS=0.2
.MODEL Diodecgs D IS=1e-40 XTI=1 N=1000 ISR=0 CJO={cgs0} EG=3.26 FC={cgs_FC} M={cgs_M} VJ={cgs_VJ} RS=0.2	.MODEL Diodecgs D IS=1e-40 XTI=1 N=1000 ISR=0 CJO={cgs0} EG=3.26 FC={cgs_FC} M={cgs_M} VJ={cgs_VJ} RS=0.2
.ENDS ujn1205k	.ENDS UJN1205z_L1

.SUBCKT IGATETOSOURCE 1 2 3 PARAMS: is0g=1.5000e-14	.SUBCKT IGATETOSOURCE 1 2 3 4 PARAMS: is0g=1.5000e-14
.param is0_tc=0.0000e+00	.param is0_tc=0.0000e+00
.param ngs=3.7100 ngs_tc=0.0020	.param ngs=3.7100 ngs_tc=0.0020
.param xti=1.5e+01	.param xti=1.5e+01
.param egap=3.2600	.param egap=3.2600
.param egapt1=1.0000e+05	.param egapt1=1.0000e+05
.param egapt2=3.3000e-02	.param egapt2=3.3000e-02
.func ratio_t() {(TEMP+273.15)/(300)}	.func ratio_t() {(V(4,3)+273.15)/(300)}
.func vt() {1.38e-23*(TEMP+273.15)/1.602e-19}	.func vt() {1.38e-23*(V(4,3)+273.15)/1.602e-19}
.func egap_t() {egap-(egapt2*((TEMP+273.15)*(TEMP+273.15)))/((TEMP+273.15)+egapt1)}	.func egap_t() {egap-(egapt2*((V(4,3)+273.15)*(V(4,3)+273.15)))/((V(4,3)+273.15)+egapt1)}
.func is_t() {is0g*PWR(ratio_t(),(xti/ngs)) *EXP((ratio_t()-1)*(egap_t()/(ngs*vt())))}	.func is_t() {is0g*PWR(ratio_t(),(xti/ngs)) *EXP((ratio_t()-1)*(egap_t()/(ngs*vt())))}
.func IGS(vgs) {if(vgs<0, 0,is_t()(EXP(vgs/(ngs*vt())) - 1))}	*.func IGS(vgs) {if(vgs<0, 0,is_t()*(EXP(vgs/(ngs*vt())) - 1))}
.func IGS(vgs) {is_t()*(1)}	.func IGS(vgs) {is_t()*(1)}
G_GS 1 3 VALUE = {IGS(V(2,3))}	G_GS 1 3 VALUE = {IGS(V(2,3))}
.ENDS IGATETOSOURCE	.ENDS IGATETOSOURCE
* JFET drain current	* JFET drain current
.SUBCKT IDJFET Gate Drain Source PARAMS: beta=5.28 beta_tce=-30 vth=-7.892 vth_tc=4.0e-4	.SUBCKT IDJFET Gate Drain Source T PARAMS: beta=5.28 beta_tce=-30 vth=-7.892 vth_tc=4.0e-4
+ npow=1.4480 npow_tc=-5.0000e-04 lambda0=0.05 lambda1=-1.1000e-01	+ npow=1.4480 npow_tc=-5.0000e-04 lambda0=0.05 lambda1=-1.1000e-01
+ alpha=1.8000 alpha_tc=-3.0000e-03	+ alpha=1.8000 alpha_tc=-3.0000e-03
* Calculate Temperature Dependent Parameters	* Calculate Temperature Dependent Parameters
.func delta_t() {TEMP - 27}	.func delta_t() {V(T,Source) - 27
.func beta_t() {beta*PWR(1.0001, beta_tce*delta_t())}	.func beta_t() {beta*PWR(1.0001, beta_tce*delta_t())}
.func vth_t() {vth * (1 + vth_tc * delta_t())}	.func vth_t() {vth * (1 + vth_tc * delta_t())}

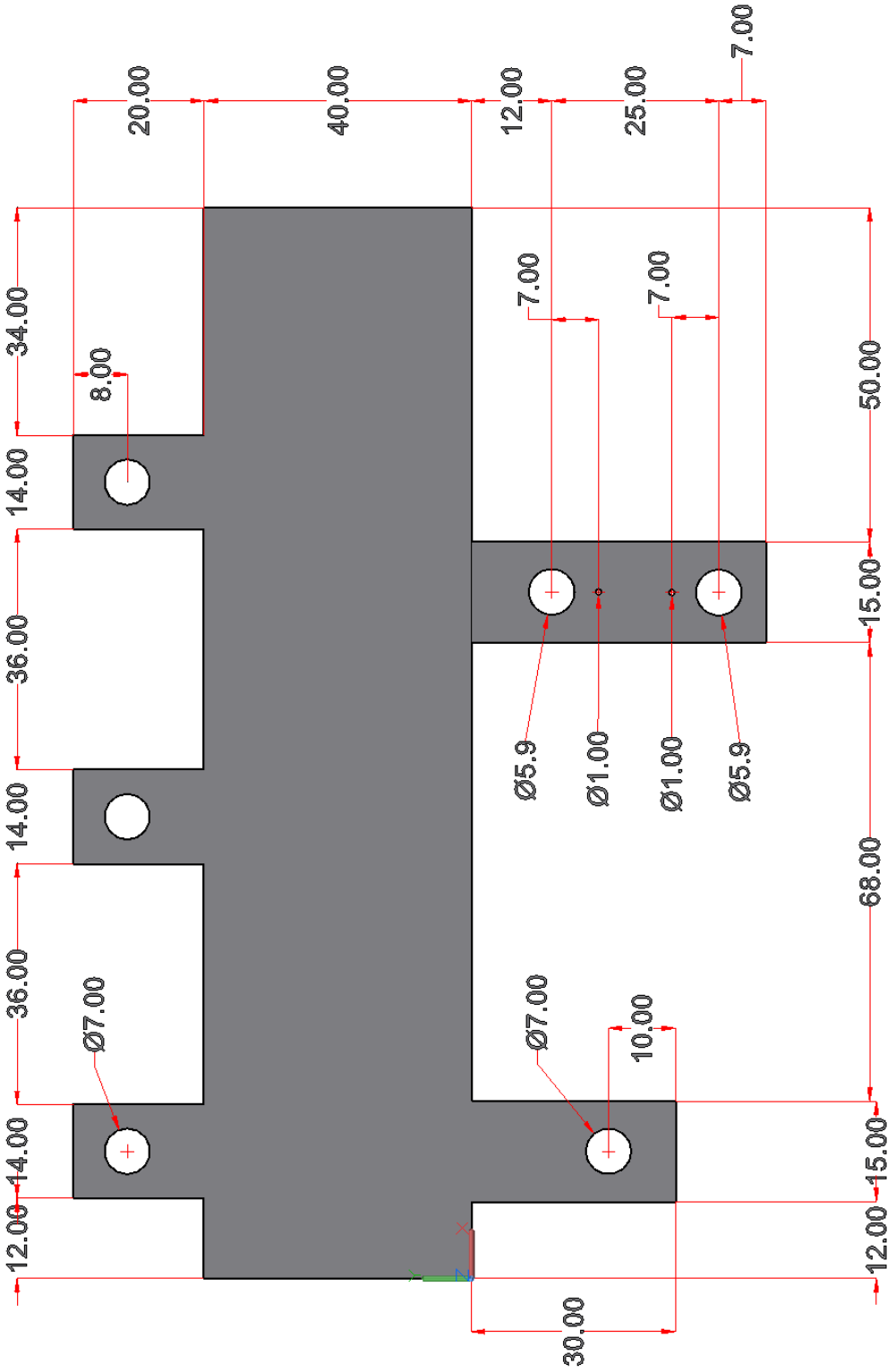
.func npow_t() {npow * (1 + npow_tc * delta_t())}	.func npow_t() {npow * (1 + npow_tc * delta_t())}
.func alpha_t() {alpha * (1 + alpha_tc * delta_t())}	.func alpha_t() {alpha * (1 + alpha_tc * delta_t())}
* Calculate the terms of the ID equation	* Calculate the terms of the ID equation
.func vod(vgs) {if((vgs-vth_t()>0), (vgs-vth_t()),(vgs-vth_t()-1e-15))}	.func vod(vgs) {if((vgs-vth_t()>0), (vgs-vth_t()),(vgs-vth_t()-1e-15))}
.func npow_term(vgs) {PWR(vod(vgs),npow_t())}	.func npow_term(vgs) {PWR(vod(vgs),npow_t())}
**(1+lambda1*vod(vgs))}	**(1+lambda1*vod(vgs))}
.func lambda_factor(vds,vgs,vds_term) {if((vds_term>0), 1+lambda0*abs(vds)*(1+lambda1*vod(vgs)*0), 1+lambda0*abs(vds))}	.func lambda_factor(vds,vgs,vds_term) {if((vds_term>0), 1+lambda0*abs(vds)*(1+lambda1*vod(vgs)*0), 1+lambda0*abs(vds))}
.func tanh_term(vds,vgs) {tanh(alpha_t()*vds/vod(vgs))}	.func tanh_term(vds,vgs) {tanh(alpha_t()*vds/vod(vgs))}
.func IDSEQ(vds,vgs,vds_term) {if(vgs>vth_t(),(beta_t()*npow_term(vgs)*tanh_term(vds,vgs)*(lambda_factor(vds, vgs,vds_term))), 0)}	.func IDSEQ(vds,vgs,vds_term) {if(vgs>vth_t(),(beta_t()*npow_term(vgs)*tanh_term(vds,vgs)*(lambda_factor(vds, vgs,vds_term))), 0)}
.func IDS(vds,vgs,vgd) {IF((vds>0), (IDSEQ(vds,vgs,vds)+ vds/5e6), -0.8*(IDSEQ(-vds,vgd,vds)+ vds/5e6))}	.func IDS(vds,vgs,vgd) {IF((vds>0), (IDSEQ(vds,vgs,vds)+ vds/5e6), -0.8*(IDSEQ(-vds,vgd,vds)+ vds/5e6))}
G_DS Drain Source VALUE = {IDS(V(Drain,Source),V(Gate,Source),V(Gate,Drain))}	G_DS Drain Source VALUE = {IDS(V(Drain,Source),V(Gate,Source),V(Gate,Drain))}
.ENDS IDJFET	.ENDS IDJFET
*	*

Appendix C: Dimensions of Manufactured CLD Testing Parts (in mm)

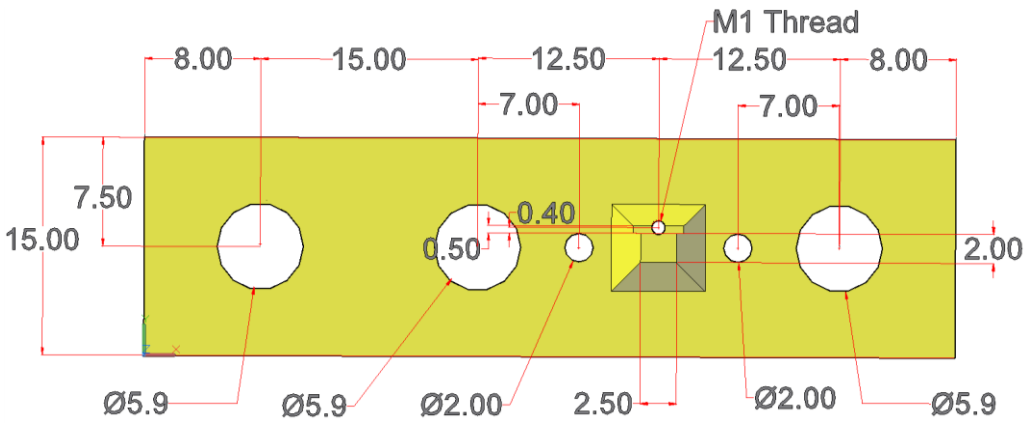
- **Positive potential busbar**
    - Top view



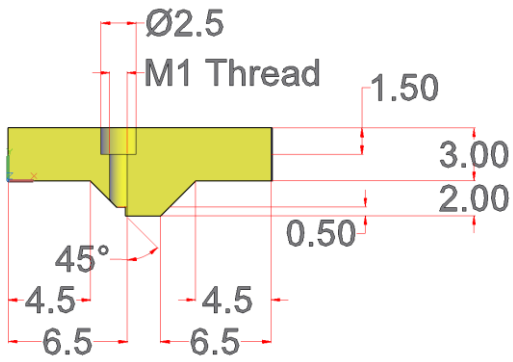
- **Negative potential busbar**
    - Top view



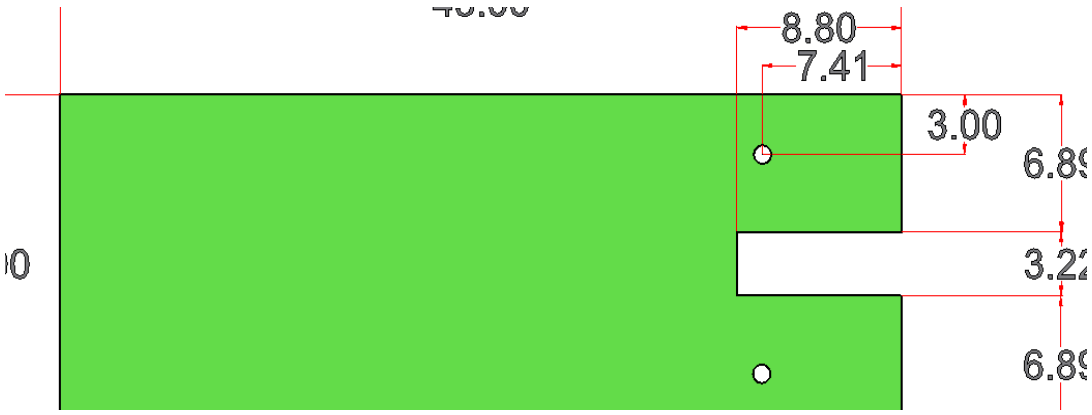
- **Cathode structure**
  - Bottom view



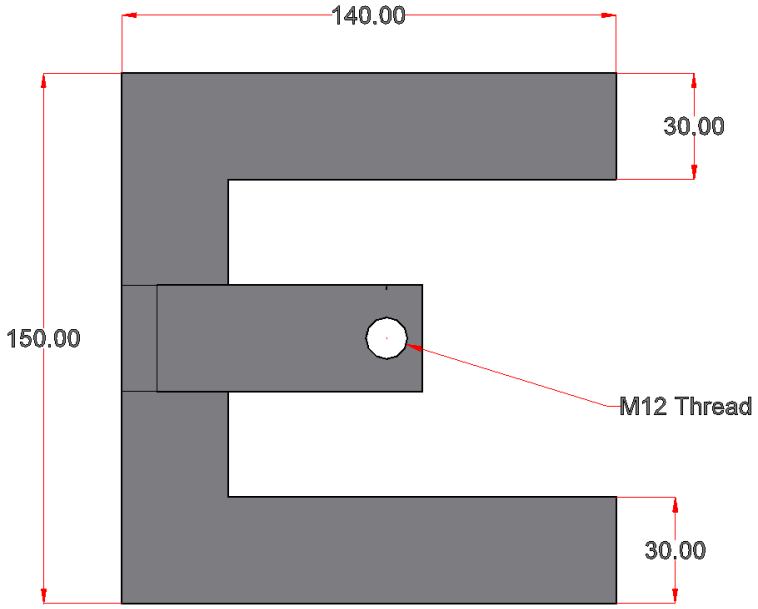
  - Cross sectional view



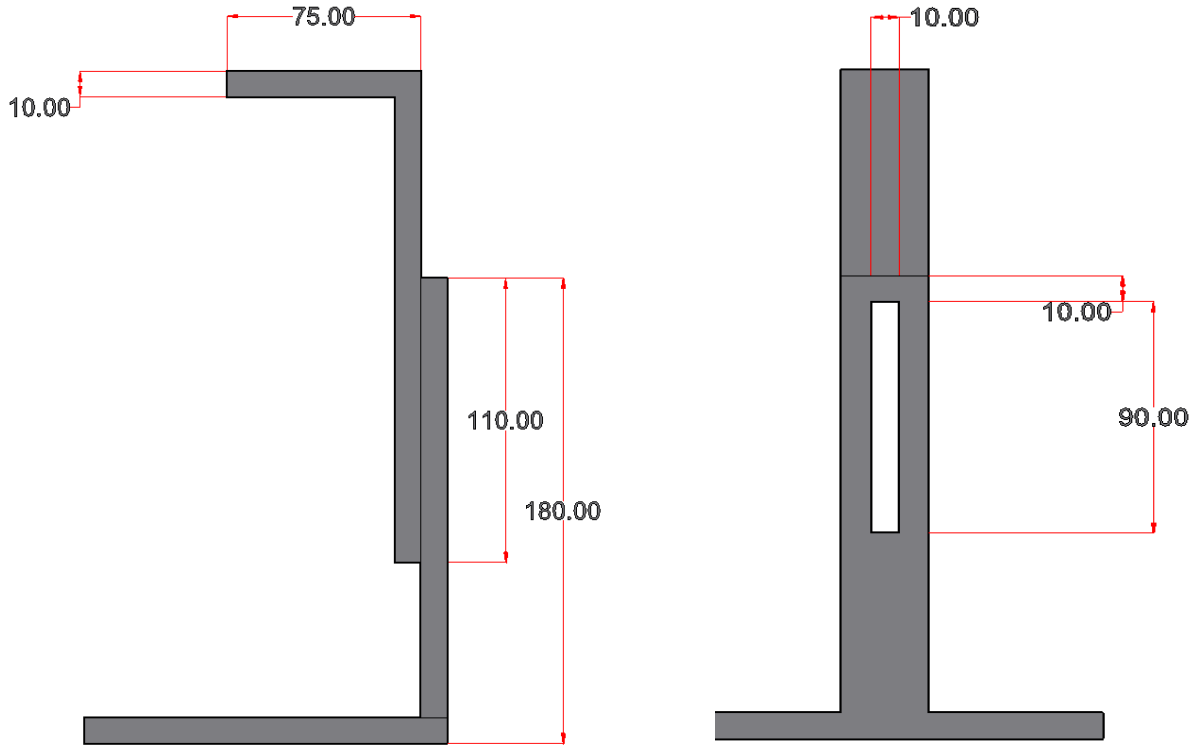
- **Positioning Stencil**
  - Top view



- **Capacitor Holder**
    - Top view

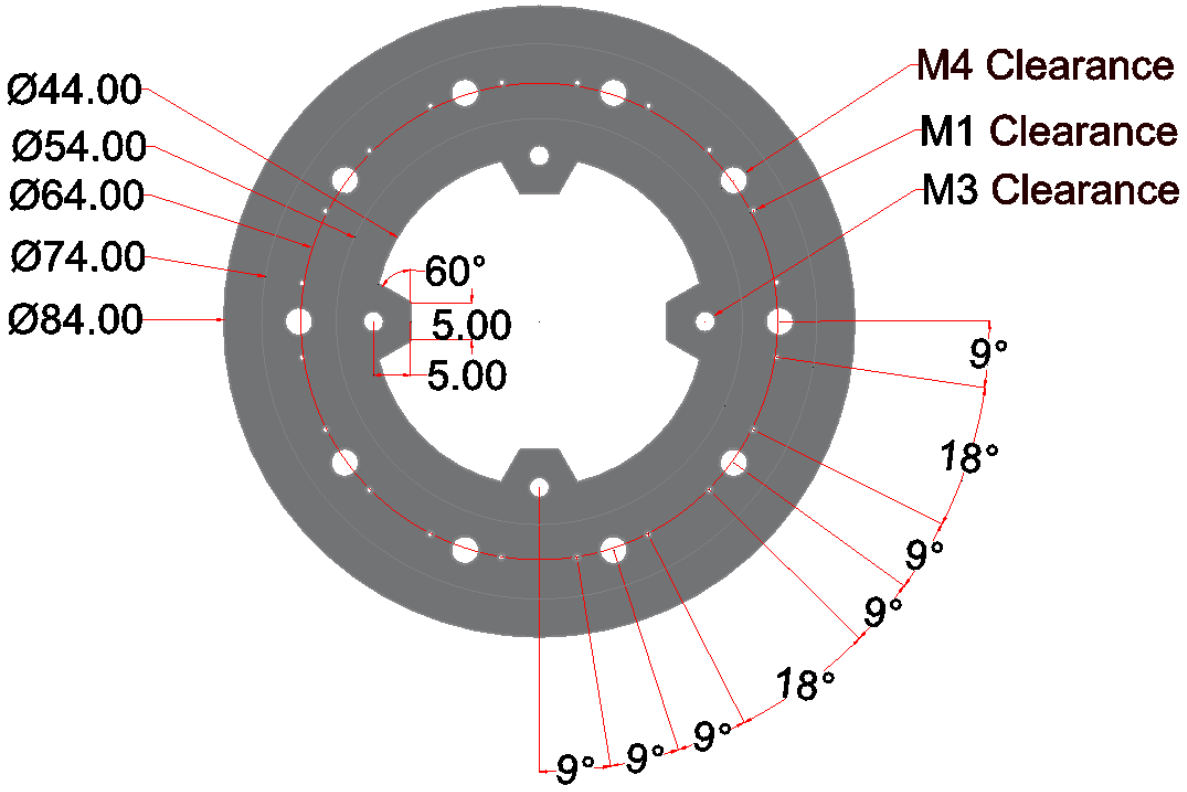


    - Side views

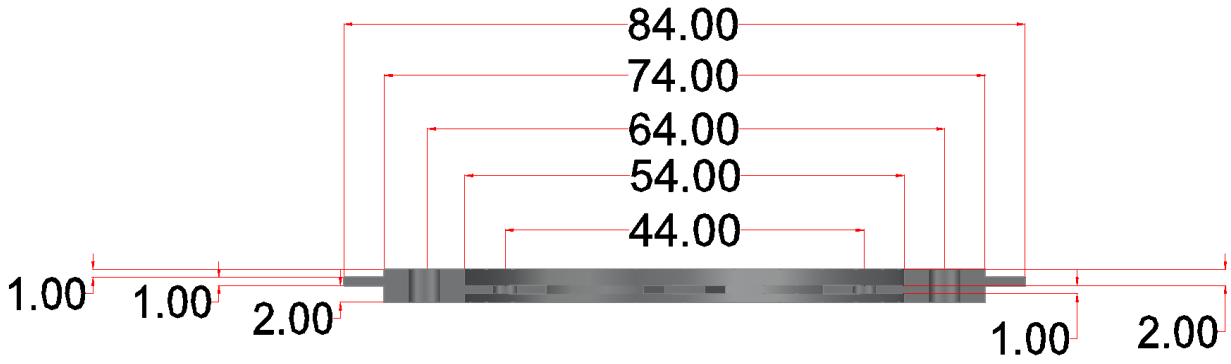


Appendix D: Dimensions of Manufactured ICLD Testing Parts (in mm)

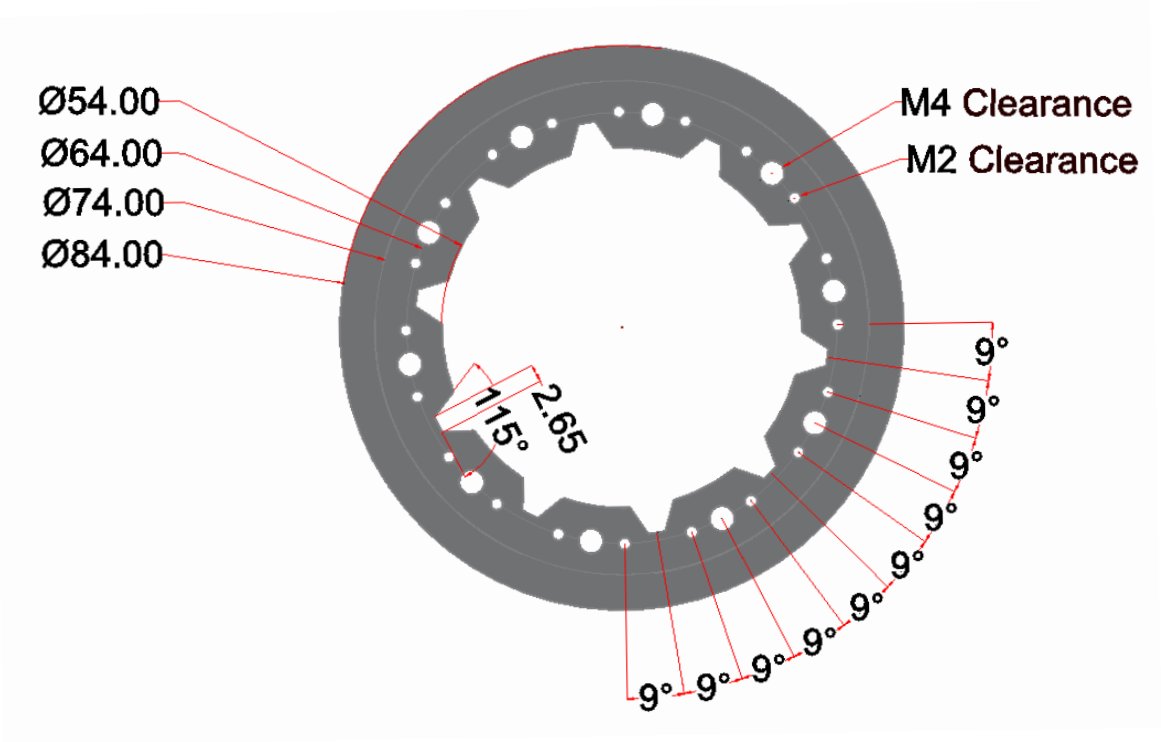
- Bottom side copper structure
  - Top view



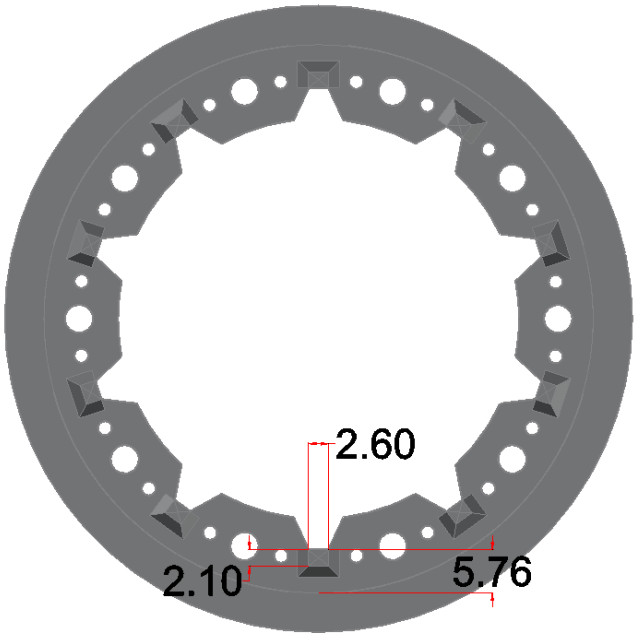
  - Side view



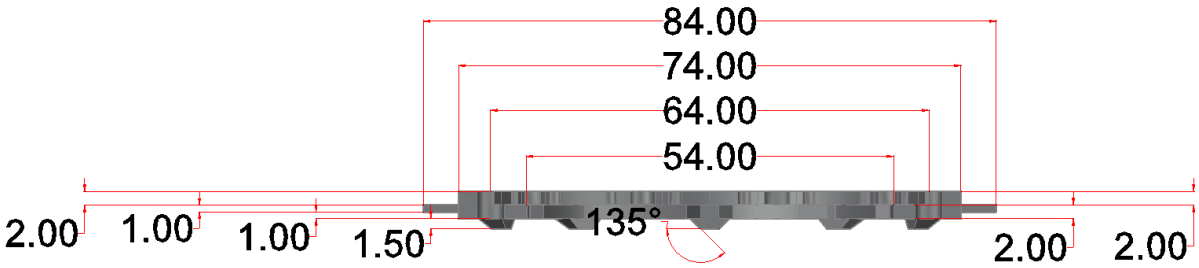
- Top side copper structure
    - Top view



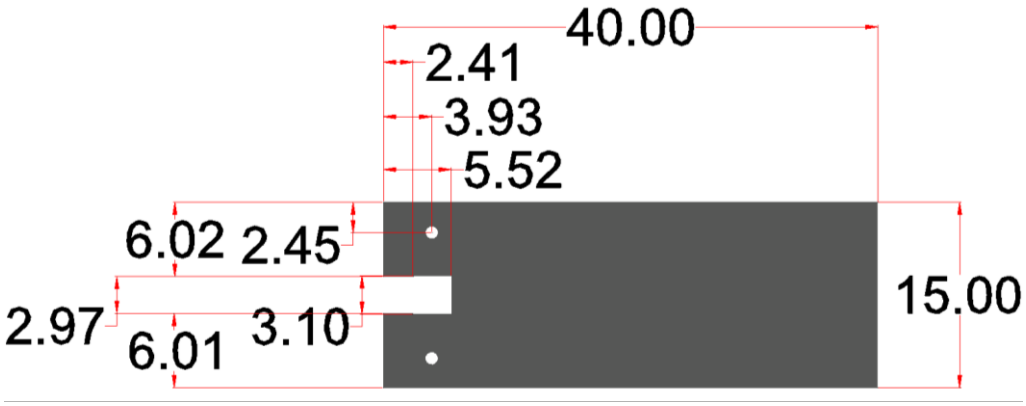
    - Bottom view



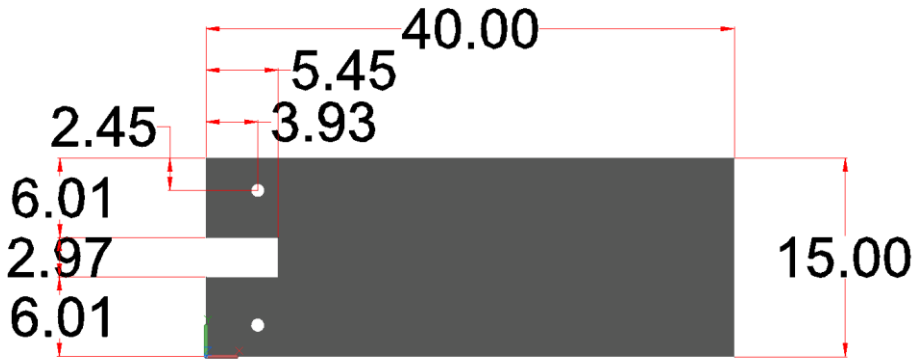
- Cross sectional view



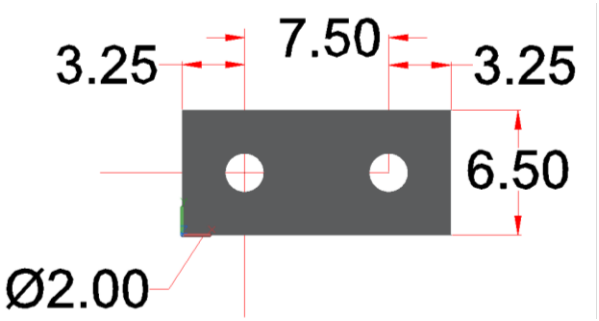
- Top side stencil
  - Top view



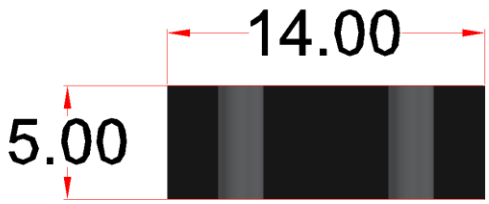
- Bottom side stencil
  - Top view



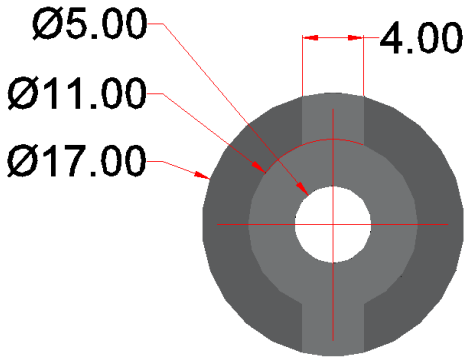
- Centre Cu structures
    - Top



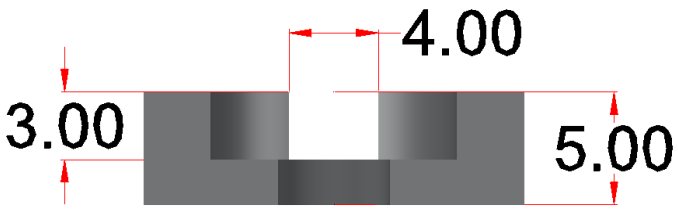
    - Cross sectional



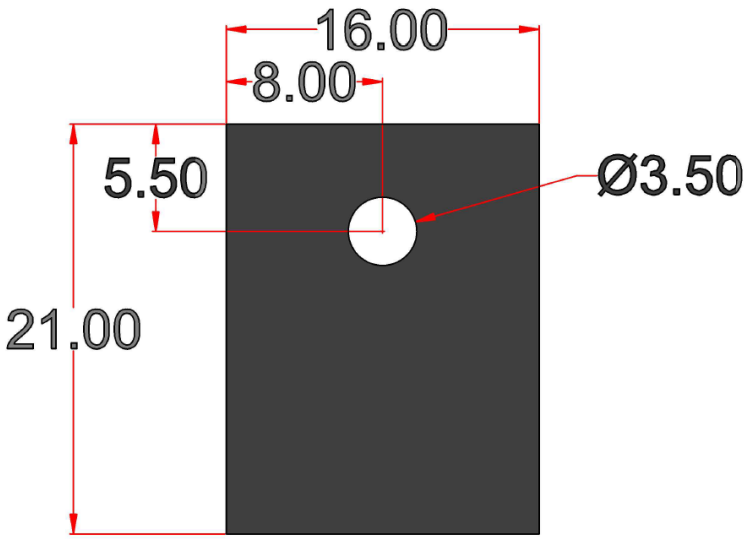
- Cathode
    - Top



- Cross sectional



- Low-side JFET thermal mass (1cm thick)
  - Top view



MATLAB Script for Line-to-Line Short-Circuit Fault Calculations

Appendix E: MATLAB Script for Line-to-Line Short-Circuit Fault Calculations

```
%% ------------------------------------------------------------------------
%% Calculation of resistance and self-inductance vs length for a 2AWG wire
%% ------------------------------------------------------------------------

% Radius of wire in meters
r=(6.54e-3)/2

% Resistivity of Copper in ohmmeter
Rho=1.68e-8

% Resistance Per meter
R_u=Rho/(pi*r^2)

% Length of wire in meter
L=0.5:0.5:5

% Inductance of wire in microhenry
L_self=0.2.*(L).*(log(2.*L./r)-3/4)

% Plot inductance vs. length
hFig = figure(1);
set(hFig, 'Position', [0 0 1500 700])

plot(L,L_self)

grid on
xlabel('Cable Length (m)')
ylabel('Self Inductance ({\mu}H)')
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14)
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
ax = gca;
ax.LineWidth = 2.5;
%% ------------------------------------------------------------------------
%% Define system parameters
%% ------------------------------------------------------------------------

% Initial fault branch current in Amps
I0=92.6;
% Initial DC-Link voltage in volts
V0=540;
% DC-link capacitor equivalent series inductance in Henry
ESL=5e-9
% DC-link capacitor equivalent series resistance in Ohms
ESR=1.7e-3
% DC-link capacitance in Farad
C=500e-6
```

```
% Freewheeling diodes resistance in Ohms
Rs=1.87e-3
% Freewheeling diodes Voltage drop in volts
Vj=1.3;
%% ------------------------------------------------------------------------
%% DC Side contributions: Diode blocking stage: Fault and capacitor Branch
Current (IDB)
%% ------------------------------------------------------------------------

% 0.5 m case

% Define variable for time
t=0:0.01e-6:0.2e-3;
% Fault branch inductance
Lshort=0.4973e-6;
% Fault branch resistace
Rshort=0.25e-3;
% Eq. 2.4
Beta=(ESR+Rshort)/(2*(ESL+Lshort));
% Eq. 2.5
omega_0=1/sqrt(C*(ESL+Lshort));
% Eq. 2.6
omega_r=sqrt(omega_0^2-Beta^2);
% Eq. 2.9
IDB05=exp(-
Beta.*t).*(I0.*cos(omega_r.*t)+((V0/(ESL+Lshort)+Beta*I0)/(omega_r)).*sin(omeg
a_r.*t))
% Plot results for 0.5m case
hFig = figure(1);
set(hFig, 'Position', [0 0 1500 700])
hold on
grid on
xlabel('Time (ms)')
ylabel('Current (kA)')
xlim([0 0.2])
ylim([-15 20])
plot(t*1e3,IDB05/1000,'--')

% Repeat calculations for 5m case

Lshort=7.2756e-6;
Rshort=2.5e-3;
Beta=(ESR+Rshort)/(2*(ESL+Lshort));
omega_0=1/sqrt(C*(ESL+Lshort));
omega_r=sqrt(omega_0^2-Beta^2);
IDB50=exp(-
Beta.*t).*(I0.*cos(omega_r.*t)+((V0/(ESL+Lshort)+Beta*I0)/(omega_r)).*sin(omeg
a_r.*t))
plot(t*1e3,IDB50/1000,'--')
set(0,'defaultlinelinewidth',3.0)
legend1=legend('Calculated fault current (I_{DB}) with 0.5m cable','Calculated
fault current (I_{DB}) with 5m cable');
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14)
style = hgexport('factorystyle');
```

```
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
ax = gca;
ax.LineWidth = 2.5;
%% ------------------------------------------------------------------------
%% DC Side contributions: Diode blocking stage: VDC and time boundary
%% ------------------------------------------------------------------------

% 0.5 m
Lshort=0.4973e-6;
Rshort=0.25e-3;
Beta=(ESR+Rshort)/(2*(ESL+Lshort));
omega_0=1/sqrt(C*(ESL+Lshort));
omega_r=sqrt(omega_0^2-Beta^2);
A=-
Lshort*(omega_r*I0+(Beta*V0/(omega_r*(ESL+Lshort))))+(Rshort*V0/(omega_r*(ESL+
Lshort)));
B=Lshort*((V0/(ESL+Lshort))-Beta*I0)+Rshort*I0;
t0_05=abs(atan(B/A)/omega_r)
tb_05=abs((asin(-2*Vj*exp(t0_05*Beta)/sqrt(A^2+B^2))-
asin(B/sqrt(A^2+B^2)))/omega_r)
t=0:0.001e-6:0.1e-3;
VDC_05=exp(-Beta.*t).*(B.*cos(omega_r.*t)+(A).*sin(omega_r.*t));
hFig = figure(1);
set(hFig, 'Position', [0 0 1500 700])
plot(t(find(t<tb_05))*1e3,VDC_05(find(t<tb_05)),'--')
hold on

% 5 m
Lshort=7.2756e-6;
Rshort=2.5e-3;
Beta=(ESR+Rshort)/(2*(ESL+Lshort));
omega_0=1/sqrt(C*(ESL+Lshort));
omega_r=sqrt(omega_0^2-Beta^2);
A=-
Lshort*(omega_r*I0+(Beta*V0/(omega_r*(ESL+Lshort))))+(Rshort*V0/(omega_r*(ESL+
Lshort)));
B=Lshort*((V0/(ESL+Lshort))-Beta*I0)+Rshort*I0;
t0_5=abs(atan(B/A)/omega_r)
tb_5=abs((asin(-2*Vj*exp(t0_5*Beta)/sqrt(A^2+B^2))-
asin(B/sqrt(A^2+B^2)))/omega_r)
VDC_5=exp(-Beta.*t).*(B.*cos(omega_r.*t)+(A).*sin(omega_r.*t));
plot(t(find(t<tb_5))*1e3,VDC_5(find(t<tb_5)),'--')
xlim([0.0000 0.12])
t=0:0.01e-6:0.2e-3;
set(0,'defaultlinelinewidth',3.0)
grid on
xlabel('Time (ms)')
ylabel('Voltage (V)')
legend1=legend('Calculated DC Voltage (V_[1]) with 0.5m cable', 'Calculated DC
Voltage (V_[1]) with 5m cable');
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14)
style = hgexport('factorystyle');
```

```
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
ax = gca;
ax.LineWidth = 2.5;

%% ------------------------------------------------------------------------
%% DC Side contributions: Diode conduction stage: Fault branch contribution
(IFB)
%% ------------------------------------------------------------------------

% 0.5 m

Lshort=0.4973e-6;
Rshort=0.25e-3;
Beta=(ESR+Rshort)/(2*(ESL+Lshort));
omega_0=1/sqrt(C*(ESL+Lshort));
omega_r=sqrt(omega_0^2-Beta^2);
t= abs(tb_05)
I1_05=exp(-
Beta.*t).*(I0.*cos(omega_r.*t)+((V0/(ESL+Lshort)+Beta*I0)/(omega_r)).*sin(omeg
a_r.*t))
t=0:0.01e-6:4.0e-3;
IFB_05=(-2*Vj/((2/3)*Rs+Rshort))*(1-exp(-
t*((2/3)*Rs+Rshort)/Lshort))+I1_05*exp(-t*((2/3)*Rs+Rshort)/Lshort)
plot((t(find(IFB_05 > 0))+(abs(tb_05)))*1e3,IFB_05(find(IFB_05 > 0))/1000,'--
')
hFig = figure(1);
set(hFig, 'Position', [0 0 1500 700])
hold on
grid on
xlabel('Time (ms)')
ylabel('Current (kA)')
xlim([0 2.0])

% 5 m

Lshort=7.2756e-6;
Rshort=2.5e-3;
Beta=(ESR+Rshort)/(2*(ESL+Lshort));
omega_0=1/sqrt(C*(ESL+Lshort));
omega_r=sqrt(omega_0^2-Beta^2);
t= abs(tb_5)
I1_5=exp(-
Beta.*t).*(I0.*cos(omega_r.*t)+((V0/(ESL+Lshort)+Beta*I0)/(omega_r)).*sin(omeg
a_r.*t));
t=0:0.01e-6:4.0e-3;
IFB_5=(-2*Vj/((2/3)*Rs+Rshort))*(1-exp(-
t*((2/3)*Rs+Rshort)/Lshort))+I1_5*exp(-t*((2/3)*Rs+Rshort)/Lshort);
plot((t+(abs(tb_5)))*1e3,IFB_5/1000,'--')
legend1=legend('Simulated fault current (I_{Fault}) with 0.5m
cable','Calculated fault current (I_{FB}) with 0.5m cable','Simulated fault
current (I_{Fault}) with 5m cable', 'Calculated fault current (I_{FB}) with 5m
cable');
set(legend1,'FontSize',14);
fig=gcf;
```

```
set(findall(fig,'-property','FontSize'),'FontSize',14)
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
ax = gca;
ax.LineWidth = 2.5;

%% ------------------------------------------------------------------------
%% DC Side contributions: Diode conduction stage: Capacitor branch contribution
(ICB)
%% ------------------------------------------------------------------------

% 0.5m
Lshort=0.4973e-6;
Rshort=0.25e-3;
Beta=(ESR+Rshort)/(2*(ESL+Lshort));
omega_0=1/sqrt(C*(ESL+Lshort));
omega_r=sqrt(omega_0^2-Beta^2);
t=0:0.01e-6:abs(tb_05);
IDB_05=exp(-
Beta.*t).*(I0.*cos(omega_r.*t)+((V0/(ESL+Lshort)+Beta*I0)/(omega_r)).*sin(omeg
a_r.*t));
V1_05=V0-(trapz(t,IDB_05)/C);
Beta=(ESR+((2/3)*Rs))/(2*ESL);
omega_0=1/sqrt(C*ESL);
omega_r=sqrt(omega_0^2-Beta^2);
A=(((V1_05-2*Vj)/(ESL))/(omega_r))
t=0:0.01e-6:4e-3;
ICB_05= exp(-Beta.*t).*(I1_05.*cos(omega_r.*t)+(A.*sin(omega_r.*t)));
hFig = figure(1);
set(hFig, 'Position', [0 0 1500 700])
plot(t(find(t<abs(tb_05)))*1e3,IDB_05(find(t<abs(tb_05)))/1000,'--');
hold on
plot((t+abs(tb_05))*1e3,ICB_05/1000,'--');

% 5 m
Lshort=7.2756e-6;
Rshort=2.5e-3;
Beta=(ESR+Rshort)/(2*(ESL+Lshort));
omega_0=1/sqrt(C*(ESL+Lshort));
omega_r=sqrt(omega_0^2-Beta^2);
t=0:0.01e-6:abs(tb_5);
IDB_5=exp(-
Beta.*t).*(I0.*cos(omega_r.*t)+((V0/(ESL+Lshort)+Beta*I0)/(omega_r)).*sin(omeg
a_r.*t));
V1_5=V0-(trapz(t,IDB_5)/C);
Beta=(ESR+((2/3)*Rs))/(2*ESL);
omega_0=1/sqrt(C*ESL);
omega_r=sqrt(omega_0^2-Beta^2);
plot(t(find(t<abs(tb_5)))*1e3,IDB_5(find(t<abs(tb_5)))/1000,'--');
A=(((V1_5-2*Vj)/ESL)+Beta*I1_5)/omega_r;
t=0:0.01e-6:4e-3;
ICB_5= exp(-Beta.*t).*(I1_5.*cos(omega_r.*t)+(A.*sin(omega_r.*t)));
plot((t+abs(tb_5))*1e3,ICB_5/1000,'--');
```

```
legend1=legend('Simulated capacitor current (I_{Cap}) with 0.5m
cable','Calculated capacitor current (I_{DB}) with 0.5m cable','Calculated
capacitor current (I_{CB}) with 0.5m cable','Simulated capacitor current
(I_{Cap}) with 5m cable', 'Calculated capacitor current (I_{DB}) with 5m cable',
'Calculated capacitor current (I_{CB}) with 5m cable');
set(legend1,'FontSize',14);
grid on
xlabel('Time (ms)');
ylabel('Current (kA)');
xlim([0 0.2]);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14)
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
ax = gca;
ax.LineWidth = 2.5;

%% ------------------------------------------------------------------------
%% DC Side contributions: Diode current
%% ------------------------------------------------------------------------

% 0.5 m

Id_05=(IFB_05-ICB_05)/3;

% 5 m

Id_5=(IFB_5-ICB_5)/3;

% Plot
hFig = figure(1);
set(hFig, 'Position', [0 0 1500 700])
plot((t(find(Id_05>0))+abs(tb_05))*1e3,Id_05(find(Id_05>0))/1000,'--')
hold on
plot((t(find(Id_5>0))+abs(tb_5))*1e3,Id_5(find(Id_5>0))/1000,'--')
grid on
xlabel('Time (ms)')
ylabel('Current (kA)')
xlim([0 0.4])
legend1=legend('Simulated diode current (I_{D}) with 0.5m cable
fault','Calculated diode current with 0.5m cable fault','Simulated diode current
(I_{D})with 5m cable fault', 'Calculated diode current with 5m cable fault');
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14)
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
ax = gca;
ax.LineWidth = 2.5;

%% ------------------------------------------------------------------------
%% AC Side Contributions: Steady State
```

```
%% ------------------------------------------------------------------------

% At maximum speed

Lline=36.22e-6;
Rline=3.05e-3;
speed_max=26584;
BEMF_max=208;
Poles=8;
Freq_max_F=speed_max*(Poles/2)/60;
Freq_max_W=Freq_max_F*2*pi;
z=1i*Lline*Freq_max_W+Rline;
z_mag=norm(z);
z_angle=angle(z);
time=0:0.01e-6:3.5e-3
Ia=(BEMF_max/z_mag)*sin(Freq_max_W*time-z_angle);
Ib=(BEMF_max/z_mag)*sin(Freq_max_W*time-z_angle-(2*pi/3));
Ic=(BEMF_max/z_mag)*sin(Freq_max_W*time-z_angle-(4*pi/3));
hFig = figure(1);
set(hFig, 'Position', [0 0 1500 700])
h2 =plot(time*1e3,Ia,'--r')
hold on
plot(time*1e3,Ib,'--r')
plot(time*1e3,Ic,'--r')
legend1=legend('Simulated Steady-State Phase Fault Currents');
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14)
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
grid on
xlabel('Time (ms)')
ylabel('Current (A)')
xlim([0 3.5])
ylim([-600 600])
text(0.2823,511.4,'I_{a}','HorizontalAlignment','center','FontSize',20,'Backgr
oundColor','w');
text(0.4658,511.4,'I_{b}','HorizontalAlignment','center','FontSize',20,'Backgr
oundColor','w');
text(0.6541,511.4,'I_{c}','HorizontalAlignment','center','FontSize',20,'Backgr
oundColor','w');
ax = gca;
ax.LineWidth = 2.5;

% At idle Speed

hFig = figure(2);
set(hFig, 'Position', [0 0 1500 700])
Lline=36.22e-6;
Rline=3.05e-3;
Poles=8;
Rshort=0.25e-3;
Lshort=0.4973e-6;
speed_idle=14666;
```

```
BEMF_idle=121.24;
Freq_idle_F=speed_idle*(Poles/2)/60;
Freq_idle_W=Freq_idle_F*2*pi;
z=1i*Lline*Freq_idle_W+Rline;
sqrt(Rline^2+(Freq_idle_W*Lline)^2)
z_mag=norm(z);
z_angle=angle(z);
time=0:0.1e-6:3.5e-3
Ia=(BEMF_idle/z_mag)*sin(Freq_idle_W*time-z_angle);
Ib=(BEMF_idle/z_mag)*sin(Freq_idle_W*time-z_angle-(2*pi/3));
Ic=(BEMF_idle/z_mag)*sin(Freq_idle_W*time-z_angle-(4*pi/3));
h2 =plot(time*1e3,Ia,'--r')
hold on
plot(time*1e3,Ib,'--r')
plot(time*1e3,Ic,'--r')
legend1=legend('Calculated Steady-State Phase Fault Currents');
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14)
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
grid on
xlabel('Time (ms)')
ylabel('Current (A)')
xlim([0 3.5])
ylim([-600 600])

text(0.5042,540.4,'I_{a}','HorizontalAlignment','center','FontSize',20,'Backgr
oundColor','w');
text(0.8438,540.4,'I_{b}','HorizontalAlignment','center','FontSize',20,'Backgr
oundColor','w');
text(1.185,540.4,'I_{c}','HorizontalAlignment','center','FontSize',20,'Backgro
undColor','w');
ax = gca;
ax.LineWidth = 2.5;

%% ------------------------------------------------------------------------
%% AC side contributions: Transient: initial currents calculation
%% ------------------------------------------------------------------------

% Idle speed
Lline=36.22e-6;
Rline=3.05e-3;
Poles=8;
BEMF_idle=121.24;
Freq_idle_F=speed_idle*(Poles/2)/60;
Freq_idle_W=Freq_idle_F*2*pi;
I0_idel=386.88;
I0_RMS_idle=I0_idel/sqrt(2);
BEMF_RMS_idle=BEMF_idle/sqrt(2);
apha_idle=acos(((50e3/3)+I0_RMS_idle^2*Rline)/(I0_RMS_idle*BEMF_RMS_idle))
Beta=0:0.01*pi:2*pi;
I0a=I0_idel*sin(Beta-apha_idle);
I0b=I0_idel*sin(Beta-apha_idle-(2*pi/3));
```

```
I0c=I0_idel*sin(Beta-apha_idle-(4*pi/3));
hFig = figure(1);
set(hFig, 'Position', [0 0 1500 700])
plot(Beta,I0a)
hold on
plot(Beta,I0b)
plot(Beta,I0c)
xlim([0 2*pi])
ylim([-400 400])
ax = gca;
ax.XTick = [0 pi/2 pi 1.5*pi 2*pi];
ax.XTickLabel = {'0','\pi/2','\pi','3\pi/2','2\pi'};
legend1=legend({'I_{a}', 'I_{b}','I_{c}'});
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14)
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
grid on
xlabel('V_{a} Phase Angle at Fault Instant (\Beta)')
ylabel('Current (A)')
hFig = figure(2);
set(hFig, 'Position', [0 0 1500 700])

% Max speed
speed_max=26584;
BEMF_max=208;
Freq_max_F=speed_max*(Poles/2)/60;
Freq_max_W=Freq_max_F*2*pi;
I0_max=485.52;
I0_RMS_max=I0_max/sqrt(2);
BEMF_RMS_max=BEMF_max/sqrt(2);
apha_max=acosd(((50e3/3)+I0_RMS_max^2*Rline)/(I0_RMS_max*BEMF_RMS_max));
Beta=0:0.01*pi:2*pi;
I0a=I0_max*sin(Beta-apha_max);
I0b=I0_max*sin(Beta-apha_max-(2*pi/3));
I0c=I0_max*sin(Beta-apha_max-(4*pi/3));
plot(Beta,I0a)
hold on
plot(Beta,I0b)
plot(Beta,I0c)
xlim([0 2*pi])
ylim([-500 500])
ax = gca;
ax.XTick = [0 pi/2 pi 1.5*pi 2*pi];
ax.XTickLabel = {'0','\pi/2','\pi','3\pi/2','2\pi'};
legend1=legend({'I_{a}', 'I_{b}','I_{c}'});
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14)
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
```

```
grid on
xlabel('V_{a} Phase Angle at Fault Instant (\Beta)')
ylabel('Current (A)')
ax = gca;
ax.LineWidth = 2.5;

%% ------------------------------------------------------------------------
%% AC side contributions: Transient
%% ------------------------------------------------------------------------

% idle Speed (Beta=0)
Lline=36.22e-6;
Rline=3.05e-3;
Poles=8;

BEMF_idle=121.24;
Freq_idle_F=speed_idle*(Poles/2)/60;
Freq_idle_W=Freq_idle_F*2*pi;
z=1i*Lline*Freq_idle_W+Rline;
z_mag=norm(z);
z_angle=angle(z);
time=0:0.1e-6:20e-3
I0_max=386.88;
I0a=I0_max*sin(-apha_idle)
I0b=I0_max*sin(-apha_idle-2*pi/3)
I0c=I0_max*sin(-apha_idle-4*pi/3)
Ia1=(BEMF_idle/z_mag)*sin(Freq_idle_W*time-z_angle                    )+(I0a-
((BEMF_idle/z_mag)*sin(-z_angle))         )*exp(-time*(Rline)/(Lline));
Ib1=(BEMF_idle/z_mag)*sin(Freq_idle_W*time-z_angle-(2*pi/3))+(I0b-
((BEMF_idle/z_mag)*sin(-z_angle-(2*pi/3))))*exp(-time*(Rline)/(Lline));
Ic1=(BEMF_idle/z_mag)*sin(Freq_idle_W*time-z_angle-(4*pi/3))+(I0c-
((BEMF_idle/z_mag)*sin(-z_angle-(4*pi/3))))*exp(-time*(Rline)/(Lline));
hFig = figure(1);
set(hFig, 'Position', [0 0 1500 700])
h2 =plot(time*1e3,Ia1','--r')
hold on
plot(time*1e3,Ib1,'--r')
plot(time*1e3,Ic1,'--r')
Ia1=(BEMF_idle/z_mag)*sin(Freq_idle_W*time-z_angle                    )+(I0a-
((BEMF_idle/z_mag)*sin(-z_angle))         )*exp(-time*(Rline+Rs)/(Lline));
Ib1=(BEMF_idle/z_mag)*sin(Freq_idle_W*time-z_angle-(2*pi/3))+(I0b-
((BEMF_idle/z_mag)*sin(-z_angle-(2*pi/3))))*exp(-time*(Rline+Rs)/(Lline));
Ic1=(BEMF_idle/z_mag)*sin(Freq_idle_W*time-z_angle-(4*pi/3))+(I0c-
((BEMF_idle/z_mag)*sin(-z_angle-(4*pi/3))))*exp(-time*(Rline+Rs)/(Lline));
h3 =plot(time*1e3,Ia1','--g')
hold on
plot(time*1e3,Ib1,'--g')
plot(time*1e3,Ic1,'--g')
hold on
legend1=legend([h2  h3],{'Calculated  Phase  Currents  Disregarding  R_{S}',
'Calculated Phase Currents Considering R_{S}'});
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14)
style = hgexport('factorystyle');
style.Bounds = 'tight';
```

```
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
grid on
xlabel('Time (ms)')
ylabel('Current (A)')
xlim([0 10])
ylim([-1000 1000])
text(0.5062,794.1,'I_{a}','HorizontalAlignment','center','FontSize',20,'Backgr
oundColor','w');
text(0.3371,-
894.3,'I_{b}','HorizontalAlignment','center','FontSize',20,'BackgroundColor','
w');
text(0.1621,636.6,'I_{c}','HorizontalAlignment','center','FontSize',20,'Backgr
oundColor','w');
ax = gca;
ax.LineWidth = 2.5;

% idle Speed (Beta=pi)

Lline=36.22e-6;
Rline=3.05e-3;
Poles=8;
BEMF_idle=121.24;
Freq_idle_F=speed_idle*(Poles/2)/60;
Freq_idle_W=Freq_idle_F*2*pi;
z=1i*Lline*Freq_idle_W+Rline;
z_mag=norm(z);
z_angle=angle(z);
time=0:0.1e-6:20e-3
I0_min=386.88;
a=pi;
I0a=I0_min*sin(a-apha_idle)
I0b=I0_min*sin(a-apha_idle-2*pi/3)
I0c=I0_min*sin(a-apha_idle-4*pi/3)
hFig = figure(2);
set(hFig, 'Position', [0 0 1500 700])
Ia1=(BEMF_idle/z_mag)*sin(Freq_idle_W*time-z_angle+a                    )+(I0a-
((BEMF_idle/z_mag)*sin(-z_angle+a))          )*exp(-time*(Rline+Rs)/(Lline));
Ib1=(BEMF_idle/z_mag)*sin(Freq_idle_W*time-z_angle+a-(2*pi/3))+(I0b-
((BEMF_idle/z_mag)*sin(-z_angle+a-(2*pi/3))))*exp(-time*(Rline+Rs)/(Lline));
Ic1=(BEMF_idle/z_mag)*sin(Freq_idle_W*time-z_angle+a-(4*pi/3))+(I0c-
((BEMF_idle/z_mag)*sin(-z_angle+a-(4*pi/3))))*exp(-time*(Rline+Rs)/(Lline));
h3 =plot(time*1e3,Ia1','--g')
hold on
plot(time*1e3,Ib1,'--g')
plot(time*1e3,Ic1,'--g')
hold on
legend1=legend('Calculated Phase Currents With R_{S}');
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14)
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
grid on
```

```
xlabel('Time (ms)')
ylabel('Current (A)')
xlim([0 10])
ylim([-1000 1000])
text(0.5069,-
794.1,'I_{a}','HorizontalAlignment','center','FontSize',20,'BackgroundColor','
w');
text(0.3371,894.3,'I_{b}','HorizontalAlignment','center','FontSize',20,'Backgr
oundColor','w');
text(0.1621,-
636.6,'I_{c}','HorizontalAlignment','center','FontSize',20,'BackgroundColor','
w');
ax = gca;
ax.LineWidth = 2.5;

% Max speed (Beta=0)

Lline=36.22e-6;
Rline=3.05e-3;
Poles=8;
speed_max=26584;
BEMF_max=208;
Freq_max_F=speed_max*(Poles/2)/60;
Freq_max_W=Freq_max_F*2*pi;
z=1i*Lline*Freq_max_W+Rline;
z_mag=norm(z);
z_angle=angle(z);
time=0:0.1e-6:50.0e-3
I0_max=485.52;
a=0;
I0a=I0_max*sin(a-apha_max)
I0b=I0_max*sin(a-2*pi/3-apha_max)
I0c=I0_max*sin(a-4*pi/3-apha_max)
Ia1=(BEMF_max/z_mag)*sin(Freq_max_W*time-z_angle)+(I0a-((BEMF_max/z_mag)*sin(-
z_angle)))*exp(-time*(Rline)/(Lline));
Ib1=(BEMF_max/z_mag)*sin(Freq_max_W*time-z_angle-(2*pi/3))+(I0b-
((BEMF_max/z_mag)*sin(-z_angle-(2*pi/3))))*exp(-time*(Rline)/(Lline));
Ic1=(BEMF_max/z_mag)*sin(Freq_max_W*time-z_angle-(4*pi/3))+(I0c-
((BEMF_max/z_mag)*sin(-z_angle-(4*pi/3))))*exp(-time*(Rline)/(Lline));
hFig = figure(3);
set(hFig, 'Position', [0 0 1500 700])
h2 =plot(time*1e3,Ia1','--r')
hold on
plot(time*1e3,Ib1,'--r')
plot(time*1e3,Ic1,'--r')
xlim([0 5.0])
ylim([-800 800])
legend1=legend('Calculated Transient Phase Currents');
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14)
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
grid on
```

```
xlabel('Time (ms)')
ylabel('Current (A)')
text(0.2794,572.6,'I_{a}','HorizontalAlignment','center','FontSize',20,'Backgr
oundColor','w');
text(0.0919,636.1,'I_{c}','HorizontalAlignment','center','FontSize',20,'Backgr
oundColor','w');
text(0.1878,-
696.8,'I_{b}','HorizontalAlignment','center','FontSize',20,'BackgroundColor','
w');
ax = gca;
ax.LineWidth = 2.5;

% Max speed (Beta= pi)
Lline=36.22e-6;
Rline=3.05e-3;
Poles=8;
speed_max=26584;
BEMF_max=208;
Freq_max_F=speed_max*(Poles/2)/60;
Freq_max_W=Freq_max_F*2*pi;
z=1i*Lline*Freq_max_W+Rline;
z_mag=norm(z);
z_angle=angle(z);
time=0:0.1e-6:50.0e-3;
I0_max=485.52;
a=pi;
I0a=I0_max*sin(a-apha_max)
I0b=I0_max*sin(a-2*pi/3-apha_max)
I0c=I0_max*sin(a-4*pi/3-apha_max)
Ia1=(BEMF_max/z_mag)*sin(Freq_max_W*time-z_angle+a                    )+(I0a-
((BEMF_max/z_mag)*sin(-z_angle+a         )))*exp(-time*(Rline)/(Lline));
Ib1=(BEMF_max/z_mag)*sin(Freq_max_W*time-z_angle-(2*pi/3)+a)+(I0b-
((BEMF_max/z_mag)*sin(-z_angle-(2*pi/3)+a)))*exp(-time*(Rline)/(Lline));
Ic1=(BEMF_max/z_mag)*sin(Freq_max_W*time-z_angle-(4*pi/3)+a)+(I0c-
((BEMF_max/z_mag)*sin(-z_angle-(4*pi/3)+a)))*exp(-time*(Rline)/(Lline));
hFig = figure();
set(hFig, 'Position', [0 0 1500 700])
h2 =plot(time*1e3,Ia1','--r')
hold on
plot(time*1e3,Ib1,'--r')
plot(time*1e3,Ic1,'--r')
xlim([0 5.0])
ylim([-800 800])
legend1=legend('Calculated Transient Phase Currents');
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14)
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
grid on
xlabel('Time (ms)')
ylabel('Current (A)')
text(0.5639,451.8,'I_{a}','HorizontalAlignment','center','FontSize',20,'Backgr
oundColor','w');
```

```
text(0.1885,696.8,'I_{b}','HorizontalAlignment','center','FontSize',20,'Backgr
oundColor','w');
text(0.0899,-
635.8,'I_{c}','HorizontalAlignment','center','FontSize',20,'BackgroundColor','
w');
ax = gca;
ax.LineWidth = 2.5;

%% ------------------------------------------------------------------------
%% Plot phase voltages
%% ------------------------------------------------------------------------

% Idle speed (Beta=0)

BEMF_idle=121.24;
Freq_idle_F=speed_idle*(Poles/2)/60;
Freq_idle_W=Freq_idle_F*2*pi;
time=0:0.1e-6:4.5e-3
hFig = figure(1);
set(hFig, 'Position', [0 0 1500 700])
plot(time*1e3,BEMF_idle*sin(Freq_idle_W*time),'b')
hold on
plot(time*1e3,BEMF_idle*sin(Freq_idle_W*time+(2*pi/3)),'b')
plot(time*1e3,BEMF_idle*sin(Freq_idle_W*time+(4*pi/3)),'b')
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14)
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
grid on
xlabel('Time (ms)')
ylabel('Voltage (V)')
xlim([0 3.5])
ylim([-150 150])
text(0.2565,121.2,'V_{a}','HorizontalAlignment','center','FontSize',20,'Backgr
oundColor','w');
text(0.595,121.2,'V_{b}','HorizontalAlignment','center','FontSize',20,'Backgro
undColor','w');
text(0.9354,121.2,'V_{c}','HorizontalAlignment','center','FontSize',20,'Backgr
oundColor','w');
ax = gca;
ax.LineWidth = 2.5;

% Idle speed (Beta=pi)

hFig = figure(2);
set(hFig, 'Position', [0 0 1500 700])
BEMF_idle=121.24;
Freq_idle_F=speed_idle*(Poles/2)/60;
Freq_idle_W=Freq_idle_F*2*pi;
time=0:0.1e-6:4.5e-3
a=pi;
plot(time*1e3,BEMF_idle*sin(Freq_idle_W*time+a),'b')
hold on
plot(time*1e3,BEMF_idle*sin(Freq_idle_W*time-(2*pi/3)+a),'b')
```

```
plot(time*1e3,BEMF_idle*sin(Freq_idle_W*time-(4*pi/3)+a),'b')
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14)
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
grid on
xlabel('Time (ms)')
ylabel('Voltage (V)')
xlim([0 3.5])
ylim([-150 150])
text(0.761,121.2,'V_{a}','HorizontalAlignment','center','FontSize',20,'Backgro
undColor','w');
text(1.106,121.2,'V_{b}','HorizontalAlignment','center','FontSize',20,'Backgro
undColor','w');
text(1.449,121.2,'V_{c}','HorizontalAlignment','center','FontSize',20,'Backgro
undColor','w');
ax = gca;
ax.LineWidth = 2.5;

% Max speed (Beta=0)
speed_max=26584;
BEMF_max=208;
Freq_max_F=speed_max*(Poles/2)/60;
Freq_max_W=Freq_max_F*2*pi;
hFig = figure(3);
set(hFig, 'Position', [0 0 1500 700])
plot(time*1e3,BEMF_max*sin(Freq_max_W*time),'b')
hold on
plot(time*1e3,BEMF_max*sin(Freq_max_W*time-(2*pi/3)),'b')
plot(time*1e3,BEMF_max*sin(Freq_max_W*time-(4*pi/3)),'b')
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14)
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
grid on
xlabel('Time (ms)')
ylabel('Voltage (V)')
xlim([0 3.5])
ylim([-250 250])
text(0.1406,208,'V_{a}','HorizontalAlignment','center','FontSize',20,'Backgrou
ndColor','w');
text(0.3283,208,'V_{b}','HorizontalAlignment','center','FontSize',20,'Backgrou
ndColor','w');
text(0.5178,208,'V_{c}','HorizontalAlignment','center','FontSize',20,'Backgrou
ndColor','w');
ax = gca;
ax.LineWidth = 2.5;

% Max speed (Beta=pi)
speed_max=26584;
BEMF_max=208;
Freq_max_F=speed_max*(Poles/2)/60;
```

```
Freq_max_W=Freq_max_F*2*pi;
hFig = figure(4);
set(hFig, 'Position', [0 0 1500 700])
plot(time*1e3,BEMF_max*sin(Freq_max_W*time+a),'b')
hold on
plot(time*1e3,BEMF_max*sin(Freq_max_W*time-(2*pi/3)+a),'b')
plot(time*1e3,BEMF_max*sin(Freq_max_W*time-(4*pi/3)+a),'b')
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14)
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
grid on
xlabel('Time (ms)')
ylabel('Voltage (V)')
xlim([0 3.5])
ylim([-250 250])
text(0.4234,208,'V_{a}','HorizontalAlignment','center','FontSize',20,'Backgrou
ndColor','w');
text(0.6109,208,'V_{b}','HorizontalAlignment','center','FontSize',20,'Backgrou
ndColor','w');
text(0.8017,208,'V_{c}','HorizontalAlignment','center','FontSize',20,'Backgrou
ndColor','w');
ax = gca;
ax.LineWidth = 2.5;

%%  ------------------------------------------------------------------------
%% Combined Response: Time boundary and VDC
%% ------------------------------------------------------------------------

% Max speed
I0_max=92.6-356.2;

% 0.5 m
Lshort=0.4973e-6;
Rshort=0.25e-3;
Beta=(ESR+Rshort)/(2*(ESL+Lshort));
omega_0=1/sqrt(C*(ESL+Lshort));
omega_r=sqrt(omega_0^2-Beta^2);
A=-
Lshort*(omega_r*I0_max+(Beta*V0/(omega_r*(ESL+Lshort))))+(Rshort*V0/(omega_r*(
ESL+Lshort)));
B=Lshort*((V0/(ESL+Lshort))-Beta*I0_max)+Rshort*I0_max;
tf05_0_max=abs(atan2(B,-A)/omega_r)
tf05_max=abs((asin(-2*Vj*exp(tf05_0_max*Beta)/sqrt(A^2+B^2))-
asin(B/sqrt(A^2+B^2)))/omega_r)
t=0:0.01e-6:0.1e-3;
VDC_05_max=exp(-Beta.*t).*(B.*cos(omega_r.*t)+(A).*sin(omega_r.*t));
hFig = figure(1);
set(hFig, 'Position', [0 0 1500 700])
plot(t(find(t<tf05_max))*1e3,VDC_05_max(find(t<tf05_max)),'--')
hold on

% 5 m
```

```
Lshort=7.2756e-6;
Rshort=2.5e-3;
Beta=(ESR+Rshort)/(2*(ESL+Lshort));
omega_0=1/sqrt(C*(ESL+Lshort));
omega_r=sqrt(omega_0^2-Beta^2);
A=-
Lshort*(omega_r*I0_max+(Beta*V0/(omega_r*(ESL+Lshort))))+(Rshort*V0/(omega_r*(
ESL+Lshort)));
B=Lshort*((V0/(ESL+Lshort))-Beta*I0_max)+Rshort*I0_max;
tb_5_0_max=abs(atan2(B,-A)/omega_r)
tb_5_max=abs((asin(-2*Vj*exp(tb_5_0_max*Beta)/sqrt(A^2+B^2))-
asin(B/sqrt(A^2+B^2)))/omega_r)
VDC_5_max=exp(-Beta.*t).*(B.*cos(omega_r.*t)+(A).*sin(omega_r.*t));
plot(t(find(VDC_5_max>-2*Vj))*1e3,VDC_5_max(find(VDC_5_max>-2*Vj)),'--')
xlim([0.0005 0.15])
set(0,'defaultlinelinewidth',3.0)
grid on
xlabel('Time (ms)')
ylabel('Voltage (V)')
legend1=legend('Simulated DC Voltage (V_[1]) with 0.5m cable','Simulated DC
Voltage (V_[1]) with 5m cable','Calculated DC Voltage (V_[1]) with 0.5m cable',
'Calculated DC Voltage (V_[1]) with 5m cable');
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14)
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
ax = gca;
ax.LineWidth = 2.5;

% Idle speed

% 0.5m

I0_idle=92.6-282.9;
Lshort=0.4973e-6;
Rshort=0.25e-3;
Beta=(ESR+Rshort)/(2*(ESL+Lshort));
omega_0=1/sqrt(C*(ESL+Lshort));
omega_r=sqrt(omega_0^2-Beta^2);
A=-
Lshort*(omega_r*I0_idle+(Beta*V0/(omega_r*(ESL+Lshort))))+(Rshort*V0/(omega_r*
(ESL+Lshort)));
B=Lshort*((V0/(ESL+Lshort))-Beta*I0_idle)+Rshort*I0_idle;
tf05_0_idle=abs(atan2(B,-A)/omega_r)
tf05_idle=abs((asin(-2*Vj*exp(tf05_0_idle*Beta)/sqrt(A^2+B^2))-
asin(B/sqrt(A^2+B^2)))/omega_r)
t=0:0.01e-6:0.1e-3;
VDC_05_idle=exp(-Beta.*t).*(B.*cos(omega_r.*t)+(A).*sin(omega_r.*t));
hFig = figure(2);
set(hFig, 'Position', [0 0 1500 700])
plot(t(find(t<tf05_idle))*1e3,VDC_05_idle(find(t<tf05_idle)),'--')
hold on
```

```
% 5 m

Lshort=7.2756e-6;
Rshort=2.5e-3;
Beta=(ESR+Rshort)/(2*(ESL+Lshort));
omega_0=1/sqrt(C*(ESL+Lshort));
omega_r=sqrt(omega_0^2-Beta^2);
A=-
Lshort*(omega_r*I0_idle+(Beta*V0/(omega_r*(ESL+Lshort))))+(Rshort*V0/(omega_r*
(ESL+Lshort)));
B=Lshort*((V0/(ESL+Lshort))-Beta*I0_idle)+Rshort*I0_idle;
tb_5_0_idle=abs(atan2(B,-A)/omega_r)
tb_5_idle=abs((asin(-2*Vj*exp(tb_5_0_idle*Beta)/sqrt(A^2+B^2))-
asin(B/sqrt(A^2+B^2)))/omega_r)
VDC_5_idle=exp(-Beta.*t).*(B.*cos(omega_r.*t)+(A).*sin(omega_r.*t));
plot(t(find(VDC_5_idle>-2*Vj))*1e3,VDC_5_idle(find(VDC_5_idle>-2*Vj)),'--')
xlim([0.0005 0.15])
t=0:0.01e-6:0.2e-3;
set(0,'defaultlinelinewidth',3.0)
grid on
xlabel('Time (ms)')
ylabel('Voltage (V)')
legend1=legend('Simulated DC Voltage (V_[1]) with 0.5m cable','Simulated DC
Voltage (V_[1]) with 5m cable','Calculated DC Voltage (V_[1]) with 0.5m cable',
'Calculated DC Voltage (V_[1]) with 5m cable');
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14)
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
ax = gca;
ax.LineWidth = 2.5;

%% ------------------------------------------------------------------------
%% Combined Response: Capacitor current
%% ------------------------------------------------------------------------

% Idle Speed

I0_idle=-282.9;
grid on
xlabel('Time (ms)')
ylabel('Current (A)')
xlim([0 0.2])
ax = gca;
ax.LineWidth = 2.5;
t=0:0.01e-6:0.2e-3;

% 0.5 m
Lshort=0.4973e-6;
Rshort=0.25e-3;
Beta=(ESR+Rshort)/(2*(ESL+Lshort));
omega_0=1/sqrt(C*(ESL+Lshort));
omega_r=sqrt(omega_0^2-Beta^2);
```

```
t= abs(tf05_idle)
I1_05=exp(-
Beta.*t).*((I0_idle).*cos(omega_r.*t)+(V0/(omega_r.*(ESL+Lshort))).*sin(omega_
r.*t))
t=0:0.01e-6:0.2e-3;
IN105_cap_idle=exp(-
Beta.*t).*(I0_idle.*cos(omega_r.*t)+(V0/(omega_r.*(ESL+Lshort))).*sin(omega_r.
*t))
t=0:0.01e-6:abs(tf05_idle);
IDB_05=exp(-
Beta.*t).*((I0_idle+92.6).*cos(omega_r.*t)+(V0/(omega_r.*(ESL+Lshort))).*sin(o
mega_r.*t));
V1_05=V0-(trapz(t,IDB_05)/C);
Beta=(ESR+((2/3)*Rs))/(2*ESL);
omega_0=1/sqrt(C*ESL);
omega_r=sqrt(omega_0^2-Beta^2);
A=(((V1_05-2*Vj)/ESL)+Beta)/omega_r;
t=0:0.01e-6:4e-3;

IN22_05_cap_idle=                                                    exp(-
Beta.*t).*(I1_05.*cos(omega_r.*t)+(A.*sin(omega_r.*t)));
hFig = figure(1);
set(hFig, 'Position', [0 0 1500 700])
hold on
plot(t(find(t<abs(tf05_idle)))*1e3,IN105_cap_idle(find(t<abs(tf05_idle)))/1000
,'--');
plot((t+abs(tf05_idle))*1e3,IN22_05_cap_idle/1000,'--');

% 5m

Lshort=7.2756e-6;
Rshort=2.5e-3;
Beta=(ESR+Rshort)/(2*(ESL+Lshort));
omega_0=1/sqrt(C*(ESL+Lshort));
omega_r=sqrt(omega_0^2-Beta^2);
t= abs(tb_5_idle)
I1_5=exp(-
Beta.*t).*(I0_idle.*cos(omega_r.*t)+(V0/(omega_r.*(ESL+Lshort))).*sin(omega_r.
*t))
t=0:0.01e-6:0.2e-3;
IN15_cap_idle=exp(-
Beta.*t).*(I0_idle.*cos(omega_r.*t)+(V0/(omega_r.*(ESL+Lshort))).*sin(omega_r.
*t))
t=0:0.01e-6:abs(tb_5_idle);
IDB_5=exp(-
Beta.*t).*((96.2+I0_idle).*cos(omega_r.*t)+(V0/(omega_r.*(ESL+Lshort))).*sin(o
mega_r.*t));
V1_05=V0-(trapz(t,IDB_5)/C);
Beta=(ESR+((2/3)*Rs))/(2*ESL);
omega_0=1/sqrt(C*ESL);
omega_r=sqrt(omega_0^2-Beta^2);
A=(((V1_05-2*Vj)/ESL)+Beta)/omega_r;
t=0:0.01e-6:4e-3;
IN22_5_cap_idle= exp(-Beta.*t).*(I1_5.*cos(omega_r.*t)+(A.*sin(omega_r.*t)));
hold on
```

```
plot(t(find(t<abs(tb_5_idle)))*1e3,IN15_cap_idle(find(t<abs(tb_5_idle)))/1000,
'--');
plot((t+abs(tb_5_idle))*1e3,IN22_5_cap_idle/1000,'--');
legend1=legend('Simulated capacitor current (I_{Cap}) with 0.5m
cable','Simulated capacitor current (I_{Cap}) with 5m cable','Calculated
capacitor current (I_{DB}) with 0.5m cable','Calculated capacitor current
(I_{CB}) with 0.5m cable', 'Calculated capacitor current (I_{DB}) with 5m
cable', 'Calculated capacitor current (I_{CB}) with 5m cable');
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14)
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
grid on
xlabel('Time (ms)')
ylabel('Current (A)')
xlim([0 0.2])

% Maximum Speed
t=0:0.01e-6:0.2e-3;

% 0.5 m
Lshort=0.4973e-6;
Rshort=0.25e-3;
I0_max=-356.2;
Beta=(ESR+Rshort)/(2*(ESL+Lshort));
omega_0=1/sqrt(C*(ESL+Lshort));
omega_r=sqrt(omega_0^2-Beta^2);
t= abs(tf05_max)
I1_05=exp(-
Beta.*t).*(I0_max.*cos(omega_r.*t)+(V0/(omega_r.*(ESL+Lshort))).*sin(omega_r.*
t))
t=0:0.01e-6:0.2e-3;
IN105_cap_max=exp(-
Beta.*t).*(I0_max.*cos(omega_r.*t)+(V0/(omega_r.*(ESL+Lshort))).*sin(omega_r.*
t))
t=0:0.01e-6:abs(tf05_max);
IDB_05=exp(-
Beta.*t).*((I0_max+92.6).*cos(omega_r.*t)+(V0/(omega_r.*(ESL+Lshort))).*sin(om
ega_r.*t));
V1_05=V0-(trapz(t,IDB_05)/C);
Beta=(ESR+((2/3)*Rs))/(2*ESL);
omega_0=1/sqrt(C*ESL);
omega_r=sqrt(omega_0^2-Beta^2);
A=(((V1_05-2*Vj)/ESL)+Beta)/omega_r;
t=0:0.01e-6:4e-3;
IN22_05_cap_max= exp(-Beta.*t).*(I1_05.*cos(omega_r.*t)+(A.*sin(omega_r.*t)));
hFig = figure(2);
set(hFig, 'Position', [0 0 1500 700])
grid on
xlabel('Time (ms)')
ylabel('Current (kA)')
xlim([0 0.2])
hold on
```

```
plot(t(find(t<abs(tf05_max)))*1e3,IN105_cap_max(find(t<abs(tf05_max)))/1000,'-
-');
plot((t+abs(tf05_max))*1e3,IN22_05_cap_max/1000,'--');

% 5m

Lshort=7.2756e-6;
Rshort=2.5e-3;
Beta=(ESR+Rshort)/(2*(ESL+Lshort));
omega_0=1/sqrt(C*(ESL+Lshort));
omega_r=sqrt(omega_0^2-Beta^2);
t= abs(tb_5_max)
I1_5=exp(-
Beta.*t).*(I0_max.*cos(omega_r.*t)+(V0/(omega_r.*(ESL+Lshort))).*sin(omega_r.*
t))
t=0:0.01e-6:0.2e-3;
IN15_cap_max=exp(-
Beta.*t).*(I0_max.*cos(omega_r.*t)+(V0/(omega_r.*(ESL+Lshort))).*sin(omega_r.*
t))
t=0:0.01e-6:abs(tb_5_max);
IDB_5=exp(-
Beta.*t).*((I0_max+92.6).*cos(omega_r.*t)+(V0/(omega_r.*(ESL+Lshort))).*sin(om
ega_r.*t));
V1_05=V0-(trapz(t,IDB_5)/C);
Beta=(ESR+((2/3)*Rs))/(2*ESL);
omega_0=1/sqrt(C*ESL);
omega_r=sqrt(omega_0^2-Beta^2);
A=(((V1_05-2*Vj)/ESL)+Beta)/omega_r;
t=0:0.01e-6:4e-3;
IN22_5_cap_max= exp(-Beta.*t).*(I1_5.*cos(omega_r.*t)+(A.*sin(omega_r.*t)));
hFig = figure(2);
set(hFig, 'Position', [0 0 1500 700])
grid on
xlabel('Time (ms)')
ylabel('Current (kA)')
xlim([0 0.2])
hold on
plot(t(find(t<abs(tb_5_max)))*1e3,IN15_cap_max(find(t<abs(tb_5_max)))/1000,'--
');
plot((t+abs(tb_5_max))*1e3,IN22_5_cap_max/1000,'--');
legend1=legend('Calculated capacitor current (I_{DB}) with 0.5m
cable','Calculated capacitor current (I_{CB}) with 0.5m cable', 'Calculated
capacitor current (I_{DB}) with 5m cable', 'Calculated capacitor current
(I_{CB}) with 5m cable');
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14)
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
grid on
xlabel('Time (ms)')
ylabel('Current (kA)')
ax = gca;
ax.LineWidth = 2.5;
```

```
%% ------------------------------------------------------------------------
%% Combined Response: AC side Current
%% ------------------------------------------------------------------------

Lline=36.22e-6;
Rline=3.05e-3;
Poles=8;

% idle speed Short Cable
BEMF_idle=121.24;
Freq_idle_F=speed_idle*(Poles/2)/60;
Freq_idle_W=Freq_idle_F*2*pi;
z=1i*Lline*Freq_idle_W+Rline+Rs;
z_mag=norm(z);
z_angle=angle(z);
I0_min=386.88;
a=pi;
I0a=I0_min*sin(a-apha_idle);
I0b=I0_min*sin(a-apha_idle-2*pi/3);
I0c=I0_min*sin(a-apha_idle-4*pi/3);
t=0:0.01e-6:tf05_0_idle;
Ia_min_short=zeros(length(t),1);
Ib_min_short=zeros(length(t),1);
Ic_min_short=zeros(length(t),1);
Ia_min_short(1)=I0a;
Ib_min_short(1)=I0b;
Ic_min_short(1)=I0c;
FirstElement=1;
time0=0;

Beta_a=1/3;
Beta_b=1/3;
Beta_c=-2/3;

for i=2:length(t)
    time_int=time0:0.01e-6:t(i);
    vina=(Beta_a*VDC_05_idle(1:length(time_int)));
    vinb=(Beta_b*VDC_05_idle(1:length(time_int)));
    vinc=(Beta_c*VDC_05_idle(1:length(time_int)));

    Va=BEMF_idle*sin(Freq_idle_W*time_int+a);
    Vb=BEMF_idle*sin(Freq_idle_W*time_int+a-2*pi/3);
    Vc=BEMF_idle*sin(Freq_idle_W*time_int+a-4*pi/3);

    Ia_min_short(i)=Ia_min_short(FirstElement)+(1/Lline)*trapz(time_int,Va-
vina);
    Ib_min_short(i)=Ib_min_short(FirstElement)+(1/Lline)*trapz(time_int,Vb-
vinb);
    Ic_min_short(i)=Ic_min_short(FirstElement)+(1/Lline)*trapz(time_int,Vc-
vinc);
end
hFig = figure(1);
set(hFig, 'Position', [0 0 1500 700])
h2=plot(t*1e3,Ia_min_short,'--r');
hold on
```

```
plot(t*1e3,Ib_min_short,'--r');
plot(t*1e3,Ic_min_short,'--r');
time=0:0.01e-6:1e-3
A1=(Ia_min_short(length(t))-((BEMF_idle/z_mag)*sin(Freq_idle_W*tf05_0_idle-
z_angle+a)))/exp(-tf05_0_idle*(Rline+Rs)/(Lline))
A2=(Ib_min_short(length(t))-((BEMF_idle/z_mag)*sin(Freq_idle_W*tf05_0_idle-
z_angle+a-2*pi/3)))/exp(-tf05_0_idle*(Rline+Rs)/(Lline))
A3=(Ic_min_short(length(t))-((BEMF_idle/z_mag)*sin(Freq_idle_W*tf05_0_idle-
z_angle+a-4*pi/3)))/exp(-tf05_0_idle*(Rline+Rs)/(Lline))
Ia1=(BEMF_idle/z_mag)*sin(Freq_idle_W*time-z_angle+a              )+(A1)*exp(-
time*(Rline+Rs)/(Lline));
Ib1=(BEMF_idle/z_mag)*sin(Freq_idle_W*time-z_angle+a-(2*pi/3))+(A2)*exp(-
time*(Rline+Rs)/(Lline));
Ic1=(BEMF_idle/z_mag)*sin(Freq_idle_W*time-z_angle+a-(4*pi/3))+(A3)*exp(-
time*(Rline+Rs)/(Lline));
h3=plot(time(find(time>tf05_0_idle))*1e3,Ia1(find(time>tf05_0_idle)),'--g');
hold on
plot(time(find(time>tf05_0_idle))*1e3,Ib1(find(time>tf05_0_idle)),'--g');
plot(time(find(time>tf05_0_idle))*1e3,Ic1(find(time>tf05_0_idle)),'--g');
legend1=legend([h2 h3],{'Calculated Phase Currents (t < t_{0})', 'Calculated
Phase Currents (t > t_[2])'});
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14);
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
grid on
xlabel('Time (ms)');
ylabel('Current (A)');
xlim([0 0.2]);
ylim([-800 800]);
text(0.00495,244.8,'I_{a}','HorizontalAlignment','center','FontSize',20,'Backg
roundColor','w');
text(0.00495,97.85,'I_{b}','HorizontalAlignment','center','FontSize',20,'Backg
roundColor','w');
text(0.00495,-
341.5,'I_{c}','HorizontalAlignment','center','FontSize',20,'BackgroundColor','
w');
ax = gca;
ax.LineWidth = 2.5;

% Idle speed Long Cable
Lline=36.22e-6;
Rline=3.05e-3;
Poles=8;
BEMF_idle=121.24;
Freq_idle_F=speed_idle*(Poles/2)/60;
Freq_idle_W=Freq_idle_F*2*pi;
z=1i*Lline*Freq_idle_W+Rline+Rs;
z_mag=norm(z);
z_angle=angle(z);
I0_min=386.88;
a=pi;
I0a=I0_min*sin(a-apha_idle);
```

```
I0b=I0_min*sin(a-apha_idle-2*pi/3);
I0c=I0_min*sin(a-apha_idle-4*pi/3);
t=0:0.01e-6:tb_5_0_idle;
Ia_min_Long=zeros(length(t),1);
Ib_min_Long=zeros(length(t),1);
Ic_min_Long=zeros(length(t),1);
Ia_min_Long(1)=I0a;
Ib_min_Long(1)=I0b;
Ic_min_Long(1)=I0c;
FirstElement=1;
time0=0;
Beta_a=1/3;
Beta_b=1/3;
Beta_c=-2/3;
for i=2:length(t)
    time_int=time0:0.01e-6:t(i);
    Va=BEMF_idle*sin(Freq_idle_W*time_int+a);
    Vb=BEMF_idle*sin(Freq_idle_W*time_int+a-2*pi/3);
    Vc=BEMF_idle*sin(Freq_idle_W*time_int+a-4*pi/3);

    if(t(i)>54e-6)
        if(FirstElement==1)
            time0=54e-6;
            FirstElement=5400
            time_int=time0:0.01e-6:t(i);
            Va=BEMF_idle*sin(Freq_idle_W*time_int+a);
            Vb=BEMF_idle*sin(Freq_idle_W*time_int+a-2*pi/3);
            Vc=BEMF_idle*sin(Freq_idle_W*time_int+a-4*pi/3);
        end
        vina=Va;
        vinb=(1/2*(VDC_5_idle(FirstElement:FirstElement+length(time_int)-1)-
Va));
        vinc=(-1/2*(VDC_5_idle(FirstElement:FirstElement+length(time_int)-
1)+Va));
    else
        vina=(Beta_a*VDC_5_idle(FirstElement:FirstElement+length(time_int)-
1));
        vinb=(Beta_b*(VDC_5_idle(FirstElement:FirstElement+length(time_int)-
1)));
        vinc=(Beta_c*(VDC_5_idle(FirstElement:FirstElement+length(time_int)-
1)));
    end
        if(t(i)>75.74e-6)
        if(FirstElement==5400)
            time0=75.74e-6;
            FirstElement=7575
            time_int=time0:0.01e-6:t(i);
            Va=BEMF_idle*sin(Freq_idle_W*time_int+a);
            Vb=BEMF_idle*sin(Freq_idle_W*time_int+a-2*pi/3);
            Vc=BEMF_idle*sin(Freq_idle_W*time_int+a-4*pi/3);
        end
        vina=((-1/3)*VDC_5_idle(FirstElement:FirstElement+length(time_int)-
1));
        vinb=((2/3)*(VDC_5_idle(FirstElement:FirstElement+length(time_int)-
1)));
```

```
        vinc=((-1/3)*(VDC_5_idle(FirstElement:FirstElement+length(time_int)-
1)));
    end
    Ia_min_Long(i)=Ia_min_Long(FirstElement)+(1/Lline)*trapz(time_int,Va-
vina);
    Ib_min_Long(i)=Ib_min_Long(FirstElement)+(1/Lline)*trapz(time_int,Vb-
vinb);
    Ic_min_Long(i)=Ic_min_Long(FirstElement)+(1/Lline)*trapz(time_int,Vc-
vinc);

end

hFig = figure(2);
set(hFig, 'Position', [0 0 1500 700])
h2=plot(t*1e3,Ia_min_Long,'--r');
hold on
plot(t*1e3,Ib_min_Long,'--r');
plot(t*1e3,Ic_min_Long,'--r');
time=0:0.01e-6:1e-3
A1=(Ia_min_Long(length(t))-((BEMF_idle/z_mag)*sin(Freq_idle_W*tb_5_0_idle-
z_angle+a)))/exp(-tb_5_0_idle*(Rline+Rs)/(Lline))
A2=(Ib_min_Long(length(t))-((BEMF_idle/z_mag)*sin(Freq_idle_W*tb_5_0_idle-
z_angle+a-2*pi/3)))/exp(-tb_5_0_idle*(Rline+Rs)/(Lline))
A3=(Ic_min_Long(length(t))-((BEMF_idle/z_mag)*sin(Freq_idle_W*tb_5_0_idle-
z_angle+a-4*pi/3)))/exp(-tb_5_0_idle*(Rline+Rs)/(Lline))
Ia1=(BEMF_idle/z_mag)*sin(Freq_idle_W*time-z_angle+a              )+(A1)*exp(-
time*(Rline+Rs)/(Lline));
Ib1=(BEMF_idle/z_mag)*sin(Freq_idle_W*time-z_angle+a-(2*pi/3))+(A2)*exp(-
time*(Rline+Rs)/(Lline));
Ic1=(BEMF_idle/z_mag)*sin(Freq_idle_W*time-z_angle+a-(4*pi/3))+(A3)*exp(-
time*(Rline+Rs)/(Lline));
h3=plot(time(find(time>tb_5_0_idle))*1e3,Ia1(find(time>tb_5_0_idle)),'--g');
hold on
plot(time(find(time>tb_5_0_idle))*1e3,Ib1(find(time>tb_5_0_idle)),'--g');
plot(time(find(time>tb_5_0_idle))*1e3,Ic1(find(time>tb_5_0_idle)),'--g');
legend1=legend([ h2 h3],{'Calculated Phase Currents (t < t_{0})', 'Calculated
Phase Currents (t > t_[2])'});
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14);
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
grid on
xlabel('Time (ms)');
ylabel('Current (A)');
xlim([0 0.4]);
ylim([-800 800]);
text(0.01,244.8,'I_{a}','HorizontalAlignment','center','FontSize',20,'Backgrou
ndColor','w');
text(0.01,97.85,'I_{b}','HorizontalAlignment','center','FontSize',20,'Backgrou
ndColor','w');
text(0.01,-
341.5,'I_{c}','HorizontalAlignment','center','FontSize',20,'BackgroundColor','
w');
```

```
ax = gca;
ax.LineWidth = 2.5;

% Max speed Long Cable
speed_max=26584;
BEMF_max=208;
Freq_max_F=speed_max*(Poles/2)/60;
Freq_max_W=Freq_max_F*2*pi;
z=1i*Lline*Freq_max_W+Rline;
z_mag=norm(z);
z_angle=angle(z);
t=0:0.01e-6:tb_5_0_max;
I0_max=485.52;
a=pi;
I0a=I0_max*sin(a-apha_max)
I0b=I0_max*sin(a-2*pi/3-apha_max)
I0c=I0_max*sin(a-4*pi/3-apha_max)
Ia_max_Long=zeros(length(t),1);
Ib_max_Long=zeros(length(t),1);
Ic_max_Long=zeros(length(t),1);
Ia_max_Long(1)=I0a;
Ib_max_Long(1)=I0b;
Ic_max_Long(1)=I0c;
FirstElement=1;
time0=0;
Beta_a=2/3;
Beta_b=-1/3;
Beta_c=-1/3;
for i=2:length(t)
    time_int=time0:0.01e-6:t(i);
    Va=BEMF_max*sin(Freq_max_W*time_int+a);
    Vb=BEMF_max*sin(Freq_max_W*time_int+a-2*pi/3);
    Vc=BEMF_max*sin(Freq_max_W*time_int+a-4*pi/3);

    vina=(Beta_a*VDC_5_max(FirstElement:FirstElement+length(time_int)-1));
    vinb=(Beta_b*(VDC_5_max(FirstElement:FirstElement+length(time_int)-1)));
    vinc=(Beta_c*(VDC_5_max(FirstElement:FirstElement+length(time_int)-1)));

    Ia_max_Long(i)=Ia_max_Long(FirstElement)+(1/Lline)*trapz(time_int,Va-
vina);
Ib_max_Long(i)=Ib_max_Long(FirstElement)+(1/Lline)*trapz(time_int,Vb-vinb);
Ic_max_Long(i)=Ic_max_Long(FirstElement)+(1/Lline)*trapz(time_int,Vc-vinc);

    if((sign(Ib_max_Long(i))~=sign(Ib_max_Long(1))) && FirstElement==1)
        time0=t(i-1);
        time0_temp=t(i-1);
        FirstElement=i-1;
        Beta_a=1/3;
        Beta_b=1/3;
        Beta_c=-2/3;
    end

    if(((sign(Ia_max_Long(i))~=sign(Ia_max_Long(1)))) && Beta_a==1/3)
        time0=t(i-1);
        time0_temp2=t(i-1);
        FirstElement=i-1;
```

```
        Beta_a=-1/3;
        Beta_b=2/3;
        Beta_c=-1/3;
    end
end

hFig = figure(4);
set(hFig, 'Position', [0 0 1500 700])
h2=plot(t*1e3,Ia_max_Long,'--r');
hold on
plot(t*1e3,Ib_max_Long,'--r');
plot(t*1e3,Ic_max_Long,'--r');
time=0:0.01e-6:1e-3
A1=(Ia_max_Long(length(t))-((BEMF_max/z_mag)*sin(Freq_max_W*tb_5_0_max-
z_angle+a)))/exp(-tb_5_0_max*(Rline+Rs)/(Lline))
A2=(Ib_max_Long(length(t))-((BEMF_max/z_mag)*sin(Freq_max_W*tb_5_0_max-
z_angle+a-2*pi/3)))/exp(-tb_5_0_max*(Rline+Rs)/(Lline))
A3=(Ic_max_Long(length(t))-((BEMF_max/z_mag)*sin(Freq_max_W*tb_5_0_max-
z_angle+a-4*pi/3)))/exp(-tb_5_0_max*(Rline+Rs)/(Lline))
Ia1=(BEMF_max/z_mag)*sin(Freq_max_W*time-z_angle+a                )+(A1)*exp(-
time*(Rline)/(Lline));
Ib1=(BEMF_max/z_mag)*sin(Freq_max_W*time-z_angle+a-(2*pi/3))+(A2)*exp(-
time*(Rline)/(Lline));
Ic1=(BEMF_max/z_mag)*sin(Freq_max_W*time-z_angle+a-(4*pi/3))+(A3)*exp(-
time*(Rline)/(Lline));
h3=plot(time(find(time>tb_5_0_max))*1e3,Ia1(find(time>tb_5_0_max)),'--g');
hold on
plot(time(find(time>tb_5_0_max))*1e3,Ib1(find(time>tb_5_0_max)),'--g');
plot(time(find(time>tb_5_0_max))*1e3,Ic1(find(time>tb_5_0_max)),'--g');

% plot ref paper's response
Rshort=0.5e-3*5;
Lshort=7.2756e-6;
z=1i*(Lline+Lshort)*Freq_max_W+Rshort;
z_mag=norm(z);
z_angle=angle(z);
A1=(I0a-((BEMF_max/z_mag)*sin(Freq_max_W*0-z_angle+a)))
Ia_ref=(BEMF_max/z_mag)*sin(Freq_max_W*time-z_angle+a             )+(A1)*exp(-
time*(Rshort)/(Lshort+Lline));
h4=plot(time*1e3,Ia_ref,'-.k');
Rshort=0;
Lshort=0;
legend1=legend([h2 h3 h4],{'Calculated Phase Currents (t < t_{0}) from (14)',
'Calculated Phase Currents (t > t_[2]) from (15) ','Calculated Phase Currents
from (6) in [3]'});
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14);
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
grid on
xlabel('Time (ms)');
ylabel('Current (A)');
xlim([0 0.5]);
```

```
ylim([-1000 1000]);
text(0.015,490.8,'I_{a}','HorizontalAlignment','center','FontSize',24,'Backgro
undColor','w');
text(0.015,-
80.85,'I_{b}','HorizontalAlignment','center','FontSize',24,'BackgroundColor','
w');
text(0.015,-
490.5,'I_{c}','HorizontalAlignment','center','FontSize',24,'BackgroundColor','
w');
ax = gca;
ax.LineWidth = 2.5;

% Max speed short Cable

speed_max=26584;
BEMF_max=208;
Freq_max_F=speed_max*(Poles/2)/60;
Freq_max_W=Freq_max_F*2*pi;
z=1i*Lline*Freq_max_W+Rline;
z_mag=norm(z);
z_angle=angle(z);
I0_max=485.52;
a=pi;
I0a=I0_max*sin(a-apha_max)
I0b=I0_max*sin(a-2*pi/3-apha_max)
I0c=I0_max*sin(a-4*pi/3-apha_max)
t=0:0.01e-6:tf05_0_max;
Ia_max_short=zeros(length(t),1);
Ib_max_short=zeros(length(t),1);
Ic_max_short=zeros(length(t),1);
Ia_max_short(1)=I0a;
Ib_max_short(1)=I0b;
Ic_max_short(1)=I0c;
FirstElement=1;
time0=0;
Beta_a=2/3;
Beta_b=-1/3;
Beta_c=-1/3;
temp_time=0

flag=0;
for i=2:length(t)

    time_int=time0:0.01e-6:t(i);
    Va=BEMF_max*sin(Freq_max_W*time_int+a);
    Vb=BEMF_max*sin(Freq_max_W*time_int+a-2*pi/3);
    Vc=BEMF_max*sin(Freq_max_W*time_int+a-4*pi/3);

    vina=(Beta_a*VDC_05_max(FirstElement:FirstElement+length(time_int)-1));
    vinb=(Beta_b*(VDC_05_max(FirstElement:FirstElement+length(time_int)-1)));
    vinc=(Beta_c*(VDC_05_max(FirstElement:FirstElement+length(time_int)-1)));
Ia_max_short(i)=Ia_max_short(FirstElement)+(1/Lline)*trapz(time_int,Va-vina);
Ib_max_short(i)=Ib_max_short(FirstElement)+(1/Lline)*trapz(time_int,Vb-vinb);
Ic_max_short(i)=Ic_max_short(FirstElement)+(1/Lline)*trapz(time_int,Vc-vinc);

    if((sign(Ib_max_short(i))~=sign(Ib_max_short(1))) && FirstElement==1)
```

```
        time0=t(i-1);
        FirstElement=i-1;
        Beta_a=1/3;
        Beta_b=1/3;
        Beta_c=-2/3;
    end

    if(((Ia_max_short(i))<1) && Beta_a==1/3)
        time0=t(i);
        FirstElement=i;
        Beta_a=-1/3;
        Beta_b=2/3;
        Beta_c=-1/3;
    end
end

hFig = figure(5);
set(hFig, 'Position', [0 0 1500 700])
h2=plot(t*1e3,Ia_max_short,'--r');
hold on
plot(t*1e3,Ib_max_short,'--r');
plot(t*1e3,Ic_max_short,'--r');
time=0:0.01e-6:1e-3
A1=(Ia_max_short(length(t))-((BEMF_max/z_mag)*sin(Freq_max_W*tf05_0_max-
z_angle+a)))/exp(-tf05_0_max*(Rline+Rs)/(Lline))
A2=(Ib_max_short(length(t))-((BEMF_max/z_mag)*sin(Freq_max_W*tf05_0_max-
z_angle+a-2*pi/3)))/exp(-tf05_0_max*(Rline+Rs)/(Lline))
A3=(Ic_max_short(length(t))-((BEMF_max/z_mag)*sin(Freq_max_W*tf05_0_max-
z_angle+a-4*pi/3)))/exp(-tf05_0_max*(Rline+Rs)/(Lline))
Ia1=(BEMF_max/z_mag)*sin(Freq_max_W*time-z_angle+a                )+(A1)*exp(-
time*(Rline+Rs)/(Lline));
Ib1=(BEMF_max/z_mag)*sin(Freq_max_W*time-z_angle+a-(2*pi/3))+(A2)*exp(-
time*(Rline+Rs)/(Lline));
Ic1=(BEMF_max/z_mag)*sin(Freq_max_W*time-z_angle+a-(4*pi/3))+(A3)*exp(-
time*(Rline+Rs)/(Lline));
h3=plot(time(find(time>tf05_0_max))*1e3,Ia1(find(time>tf05_0_max)),'--g');
hold on
plot(time(find(time>tf05_0_max))*1e3,Ib1(find(time>tf05_0_max)),'--g');
plot(time(find(time>tf05_0_max))*1e3,Ic1(find(time>tf05_0_max)),'--g');
% plot ref paper's response
Rshort=0.5e-3*5;
Lshort=7.2756e-6;
z=1i*(Lline+Lshort)*Freq_max_W+Rshort;
z_mag=norm(z);
z_angle=angle(z);
A1=(I0a-((BEMF_max/z_mag)*sin(Freq_max_W*0-z_angle+a)))
Ia_ref=(BEMF_max/z_mag)*sin(Freq_max_W*time-z_angle+a             )+(A1)*exp(-
time*(Rshort)/(Lshort+Lline));
h4= plot(time*1e3,Ia_ref,'-.k');
Rshort=0;
Lshort=0;
legend1=legend([h2 h3 h4],{'Calculated Phase Currents (t < t_{0}) from (14)',
'Calculated Phase Currents (t > t_[2]) from (15) ','Calculated Phase Currents
from (6) in [3]'});
set(legend1,'FontSize',14);
fig=gcf;
```

```
set(findall(fig,'-property','FontSize'),'FontSize',14);
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
grid on
xlabel('Time (ms)');
ylabel('Current (A)');
xlim([0 0.5]);
ylim([-800 800]);
text(0.01143,490.8,'I_{a}','HorizontalAlignment','center','FontSize',20,'Backg
roundColor','w');
text(0.01143,120.85,'I_{b}','HorizontalAlignment','center','FontSize',20,'Back
groundColor','w');
text(0.01143,-
250.5,'I_{c}','HorizontalAlignment','center','FontSize',20,'BackgroundColor','
w');
ax = gca;
ax.LineWidth = 2.5;

%% ------------------------------------------------------------------------
%% Combined Response: Fault branch Contribution
%% ------------------------------------------------------------------------

% Idle speed

I0_idle=-282.9;

% 0.5 m
Lshort=0.4973e-6;
Rshort=0.25e-3;
Beta=(ESR+Rshort)/(2*(ESL+Lshort));
omega_0=1/sqrt(C*(ESL+Lshort));
omega_r=sqrt(omega_0^2-Beta^2);
t= abs(tf05_idle)
I1_05=exp(-
Beta.*t).*(I0_idle.*cos(omega_r.*t)+(V0/(omega_r.*(ESL+Lshort))).*sin(omega_r.
*t))
I1_05=I1_05+292.2+92.6;
t=0:0.01e-6:4.0e-3;
IN21_05_idle=(-2*Vj/((2/3)*Rs+Rshort))*(1-exp(-
t*((2/3)*Rs+Rshort)/Lshort))+I1_05*exp(-t*((2/3)*Rs+Rshort)/Lshort)
hFig = figure(1);
set(hFig, 'Position', [0 0 1500 700])
grid on
xlabel('Time (ms)')
ylabel('Current (kA)')
xlim([0 2.0])
plot((t(find(IN21_05_idle                                                    >
0))+(abs(tf05_idle)))*1e3,IN21_05_idle(find(IN21_05_idle > 0))/1000,'--')

% 5 m

Lshort=7.2756e-6;
Rshort=2.5e-3;
Beta=(ESR+Rshort)/(2*(ESL+Lshort));
```

```
omega_0=1/sqrt(C*(ESL+Lshort));
omega_r=sqrt(omega_0^2-Beta^2);
t= abs(tb_5_idle)
I1_5=exp(-
Beta.*t).*(I0_idle.*cos(omega_r.*t)+(V0/(omega_r.*(ESL+Lshort))).*sin(omega_r.
*t));
I1_5=I1_5+50.08+92.6;
t=0:0.01e-6:4.0e-3;
IN21_5_idle=(-2*Vj/((2/3)*Rs+Rshort))*(1-exp(-
t*((2/3)*Rs+Rshort)/Lshort))+I1_5*exp(-t*((2/3)*Rs+Rshort)/Lshort);
hold on
grid on
plot((t+(abs(tb_5_idle)))*1e3,IN21_5_idle/1000,'--')
legend1=legend('Calculated fault current (I_{FB}) with 0.5m cable','Calculated
fault current (I_{FB}) with 5m cable');
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14)
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
ax = gca;
ax.LineWidth = 2.5;

% Max speed
I0_max=-356.2;

% 0.5 m
Lshort=0.4973e-6;
Rshort=0.25e-3;
Beta=(ESR+Rshort)/(2*(ESL+Lshort));
omega_0=1/sqrt(C*(ESL+Lshort));
omega_r=sqrt(omega_0^2-Beta^2);
t= abs(tf05_max)
I1_05=exp(-
Beta.*t).*(I0_max.*cos(omega_r.*t)+(V0/(omega_r.*(ESL+Lshort))).*sin(omega_r.*
t))
I1_05=I1_05+375.4+92.6;
t=0:0.01e-6:4.0e-3;
IN21_05_max=(-2*Vj/((2/3)*Rs+Rshort))*(1-exp(-
t*((2/3)*Rs+Rshort)/Lshort))+I1_05*exp(-t*((2/3)*Rs+Rshort)/Lshort)
hFig = figure(2);
set(hFig, 'Position', [0 0 1500 700])
hold on
grid on
xlabel('Time (ms)')
ylabel('Current (kA)')
xlim([0 2.0])
plot((t(find(IN21_05_max                                                    >
0))+(abs(tf05_max)))*1e3,IN21_05_max(find(IN21_05_max > 0))/1000,'--')

% 5 m
Lshort=7.2756e-6;
Rshort=2.5e-3;
Beta=(ESR+Rshort)/(2*(ESL+Lshort));
```

```
omega_0=1/sqrt(C*(ESL+Lshort));
omega_r=sqrt(omega_0^2-Beta^2);
t= abs(tb_5_max)
I1_5=exp(-
Beta.*t).*(I0_max.*cos(omega_r.*t)+(V0/(omega_r.*(ESL+Lshort))).*sin(omega_r.*
t));
I1_5=I1_5+183.3+92.6;
t=0:0.01e-6:4.0e-3;
IN21_5_max=(-2*Vj/((2/3)*Rs+Rshort))*(1-exp(-
t*((2/3)*Rs+Rshort)/Lshort))+I1_5*exp(-t*((2/3)*Rs+Rshort)/Lshort);
plot((t+(abs(tb_5_max)))*1e3,IN21_5_max/1000,'--')
legend1=legend('Calculated fault current (I_{FB}) with 0.5m cable','Simulated
fault current (I_{Fault}) with 5m cable', 'Calculated fault current (I_{FB})
with 5m cable');
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14)
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
ax = gca;
ax.LineWidth = 2.5;

%% ------------------------------------------------------------------------
%% Combined Response: Diode Current
%% ------------------------------------------------------------------------

Id5_idle=(IN21_05_idle-IN22_05_cap_idle)/3;
Id05_idle=(IN21_5_idle-IN22_5_cap_idle)/3;

Id05_max=(IN21_05_max-IN22_05_cap_max)/3;
Id5_max=(IN21_5_max-IN22_5_cap_max)/3;

%% ------------------------------------------------------------------------
%% Combined Response: Diode Current
%% ------------------------------------------------------------------------

% Max Speed Short Cable

% Diode 1
t_Ia_max_short=0:0.01e-6:tf05_0_max;
t_Ia_max_shift=0:0.01e-6:tf05_max
t_ID=0:0.01e-6:4e-3;
time_Ia1=0:0.01e-6:1e-3
ID1_forced_short_max1=Ia_max_short;
ID1_forced_short_max1(length(t_Ia_max_short):length(time_Ia1))=0;
ID1_forced_short_max2=Ia1;
ID1_forced_short_max2(find((time_Ia1<(t0_05))))=0;
ID1_forced_short_max=transpose(ID1_forced_short_max1)+ID1_forced_short_max2
ofset=0
Id05_forced_short=Id05_max;
Id05_forced_short(find(Id05_forced_short<0))=0;
Id05_forced_short=circshift(Id05_forced_short',length(t_Ia_max_shift));
Id05_forced_short(1:length(t_Ia_max_shift))=0;
Id05_forced_short(t_ID>time_Ia1(end))=[];
```

```
hFig = figure(1);
set(hFig, 'Position', [0 0 1500 700])
Combined_D1=(ID1_forced_short_max/2)+Id05_forced_short';
D1_less_0=find(Combined_D1<0);
Combined_D1(D1_less_0)=0;
Combined_D1(find(time_Ia1<=tf05_max))=ID1_forced_short_max(find(time_Ia1<=tf05
_max));
hold on
plot(time_Ia1*1e3,Combined_D1/1000,'--r')
legend1=legend({'Simulated D1 current (I_{D1})', 'Calculated D1 current
(I_{DU})'});
set(legend1,'FontSize',14);
xlim([0 1.0]);
ylim([-500/1000 7000/1000]);

% Diode 2
Combined_D2=(-ID1_forced_short_max/2)+Id05_forced_short';
Combined_D2(D1_less_0)=-ID1_forced_short_max(D1_less_0);
Combined_D2(find(time_Ia1<tf05_max))=0;
hold on
plot(time_Ia1*1e3,Combined_D2/1000,'--r')
legend1=legend({'Simulated diodes currents', 'Calculated diodes currents'});
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14);
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
grid on
xlabel('Time (ms)');
ylabel('Current (kA)');
xlim([0 1.0]);
ax = gca;
ax.LineWidth = 2.5;
text(0.25,3.5,'I_{D2}
','HorizontalAlignment','center','FontSize',20,'BackgroundColor','w');
text(0.25,1.5,'I_{D1}','HorizontalAlignment','center','FontSize',20,'Backgroun
dColor','w');

% Diode 3
t_Ia_max_short=0:0.01e-6:tf05_0_max;
t_Ia_max_shift=0:0.01e-6:tf05_max
t_ID=0:0.01e-6:4e-3;
time_Ia1=0:0.01e-6:1e-3
ID3_forced_short_max1=Ib_max_short;
ID3_forced_short_max1(length(t_Ia_max_short):length(time_Ia1))=0;
ID3_forced_short_max2=Ib1;
ID3_forced_short_max2(find((time_Ia1<(t0_05-0.01e-6))))=0;
ID3_forced_short_max=transpose(ID3_forced_short_max1)+ID3_forced_short_max2
Id05_forced_short=Id05_max;
Id05_forced_short(find(Id05_forced_short<0))=0;
Id05_forced_short=circshift(Id05_forced_short',length(t_Ia_max_shift));
Id05_forced_short(1:length(t_Ia_max_shift))=0;
Id05_forced_short(t_ID>time_Ia1(end))=[];
hFig = figure(2);
```

```
set(hFig, 'Position', [0 0 1500 700])
Combined_D3=(ID3_forced_short_max/2)+Id05_forced_short';
D3_less_0=find(Combined_D3<0);
Combined_D4=(-ID3_forced_short_max/2)+Id05_forced_short';
Combined_D4(D3_less_0)=-ID3_forced_short_max(D3_less_0);
D4less_0=find(Combined_D4<0);
Combined_D3(D4less_0)=ID3_forced_short_max(D4less_0);
Combined_D3(find(time_Ia1<tf05_max))=ID3_forced_short_max(find(time_Ia1<tf05_m
ax));
Combined_D3(find(Combined_D3<0))=0;
hold on
plot(time_Ia1*1e3,Combined_D3/1000,'--r')

% Diode 4
Combined_D4(find(Combined_D4<0))=0;
hold on
plot(time_Ia1*1e3,Combined_D4/1000,'--r')
legend1=legend({'Simulated diodes currents', 'Calculated diodes currents'});
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14);
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
grid on
xlabel('Time (ms)');
ylabel('Current (kA)');
xlim([0 1.0]);
ax = gca;
ax.LineWidth = 2.5;
ylim([-1 7])
text(0.25,3.5,'I_{D3}','HorizontalAlignment','center','FontSize',20,'Backgroun
dColor','w');
text(0.25,1.5,'I_{D4}','HorizontalAlignment','center','FontSize',20,'Backgroun
dColor','w');

% Diode 5
t_Ia_max_short=0:0.01e-6:tf05_0_max;
t_Ia_max_shift=0:0.01e-6:tf05_max
t_ID=0:0.01e-6:4e-3;
time_Ia1=0:0.01e-6:1e-3
ID5_forced_short_max1=Ic_max_short;
ID5_forced_short_max1(length(t_Ia_max_short):length(time_Ia1))=0;
ID5_forced_short_max2=Ic1;
ID5_forced_short_max2(find((time_Ia1<(t0_05-0.01e-6))))=0;
ID5_forced_short_max=transpose(ID5_forced_short_max1)+ID5_forced_short_max2
Id05_forced_short=Id05_max;
Id05_forced_short(find(Id05_forced_short<0))=0;
Id05_forced_short=circshift(Id05_forced_short',length(t_Ia_max_shift));
Id05_forced_short(1:length(t_Ia_max_shift))=0;
Id05_forced_short(t_ID>time_Ia1(end))=[];
hFig = figure(3);
set(hFig, 'Position', [0 0 1500 700])
Combined_D5=(ID5_forced_short_max/2)+Id05_forced_short';
D5_less_0=find(Combined_D5<0);
```

```
Combined_D6=(-ID5_forced_short_max/2)+Id05_forced_short';
Combined_D6(D5_less_0)=-ID5_forced_short_max(D5_less_0);
Combined_D6(find(time_Ia1<tf05_max))=-
ID5_forced_short_max(find(time_Ia1<tf05_max));
D6less_0=find(Combined_D6<0);
Combined_D5(D6less_0)=ID5_forced_short_max(D6less_0);
Combined_D5(find(time_Ia1<tf05_max))=ID5_forced_short_max(find(time_Ia1<tf05_m
ax));
Combined_D5(find(Combined_D5<0))=0;
hold on
plot(time_Ia1*1e3,Combined_D5/1000,'--r')

% Diode 6
Combined_D6(D6less_0)=0;
hold on
plot(time_Ia1*1e3,Combined_D6/1000,'--r')
legend1=legend({'Simulated diodes currents', 'Calculated diodes currents'});
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14);
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
grid on
xlabel('Time (ms)');
ylabel('Current (kA)');
xlim([0 1.0]);
ax = gca;
ax.LineWidth = 2.5;
ylim([-1 7])
text(0.35,2.5,'I_{D5}','HorizontalAlignment','center','FontSize',20,'Backgroun
dColor','w');
text(0.35,1.0,'I_{D6}','HorizontalAlignment','center','FontSize',20,'Backgroun
dColor','w');


%% ------------------------------------------------------------------------
%% Diode Current
%% ------------------------------------------------------------------------

% Max Speed Long Cable

% Diode 1
t_Ia_max_short=0:0.01e-6:tb_5_0_max;
t_Ia_max_shift=0:0.01e-6:tb_5_max
t_ID=0:0.01e-6:4e-3;
time_Ia1=0:0.01e-6:1e-3
ID1_forced_short_max1=Ia_max_Long;
ID1_forced_short_max1(length(t_Ia_max_short):length(time_Ia1))=0;
ID1_forced_short_max2=Ia1;
ID1_forced_short_max2(find((time_Ia1<(tb_5_0_max-0.01e-6))))=0;
ID1_forced_short_max=transpose(ID1_forced_short_max1)+ID1_forced_short_max2
ofset=0
Id05_forced_short=Id5_max;
Id05_forced_short(find(Id05_forced_short<0))=0;
```

```
Id05_forced_short=circshift(Id05_forced_short',length(t_Ia_max_shift)+ofset);
Id05_forced_short(1:length(t_Ia_max_shift)+ofset)=0;
Id05_forced_short(t_ID>time_Ia1(end))=[];
hFig = figure(1);
set(hFig, 'Position', [0 0 1500 700])
Combined_D1=(ID1_forced_short_max/2)+Id05_forced_short';
D1_less_0=find(Combined_D1<0);
Combined_D1(D1_less_0)=0;
Combined_D1(find(time_Ia1<tb_5_max))=ID1_forced_short_max(find(time_Ia1<tb_5_m
ax));
Combined_D1(find(Combined_D1<0))=0;
hold on
plot(time_Ia1*1e3,Combined_D1/1000,'--r')

% Diode 2
Combined_D2=(-ID1_forced_short_max/2)+Id05_forced_short';
Combined_D2(D1_less_0)=-ID1_forced_short_max(D1_less_0);
Combined_D2(find(time_Ia1<tb_5_max))=-
ID1_forced_short_max(find(time_Ia1<tb_5_max));
Combined_D2(find(Combined_D2<0))=0;
hold on
plot(time_Ia1*1e3,Combined_D2/1000,'--r')
legend1=legend({'Simulated diodes currents', 'Calculated diodes currents'});
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14);
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
grid on
xlabel('Time (ms)');
ylabel('Current (kA)');
xlim([0 1.0]);
ax = gca;
ax.LineWidth = 2.5;
text(0.3,1.6,'I_{D2}','HorizontalAlignment','center','FontSize',20,'Background
Color','w');
text(0.3,0.8,'I_{D1}','HorizontalAlignment','center','FontSize',20,'Background
Color','w');

% Diode 3
t_Ia_max_short=0:0.01e-6:tb_5_0_max;
t_Ia_max_shift=0:0.01e-6:tb_5_max
t_ID=0:0.01e-6:4e-3;
time_Ia1=0:0.01e-6:1e-3
ID3_forced_short_max1=Ib_max_Long;
ID3_forced_short_max1(length(t_Ia_max_short):length(time_Ia1))=0;
ID3_forced_short_max2=Ib1;
ID3_forced_short_max2(find((time_Ia1<(tb_5_0_max-0.01e-6))))=0;
ID3_forced_short_max=transpose(ID3_forced_short_max1)+ID3_forced_short_max2
ofset=0
Id05_forced_short=Id5_max;
Id05_forced_short(find(Id05_forced_short<0))=0;
Id05_forced_short=circshift(Id05_forced_short',length(t_Ia_max_shift)+ofset);
Id05_forced_short(1:length(t_Ia_max_shift)+ofset)=0;
```

```
Id05_forced_short(t_ID>time_Ia1(end))=[];
hFig = figure(2);
set(hFig, 'Position', [0 0 1500 700])
Combined_D3=(ID3_forced_short_max/2)+Id05_forced_short';
D3_less_0=find(Combined_D3<0);
Combined_D3(D4less_0)=ID3_forced_short_max(D4less_0);
Combined_D3(find(Combined_D3<0))=0;
hold on
plot(time_Ia1*1e3,Combined_D3/1000,'--r')

% Diode 4
Combined_D4=(-ID3_forced_short_max/2)+Id05_forced_short';
Combined_D4(D3_less_0)=-ID3_forced_short_max(D3_less_0);
D4less_0=find(Combined_D4<0);
Combined_D4(find(Combined_D4<0))=0;
Combined_D4(find(time_Ia1<tb_05))=0;
Combined_D4(find(Combined_D3==0))=-ID3_forced_short_max1(find(Combined_D3==0))
hold on
plot(time_Ia1*1e3,Combined_D4/1000,'--r')
legend1=legend({'Simulated diodes currents', 'Calculated diodes currents'});
set(legend1,'FontSize',14);
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14);
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
grid on
xlabel('Time (ms)');
ylabel('Current (kA)');
xlim([0 1.0]);
ax = gca;
ax.LineWidth = 2.5;
text(0.2,1.8,'I_{D3}','HorizontalAlignment','center','FontSize',20,'Background
Color','w');
text(0.2,1.1,'I_{D4}','HorizontalAlignment','center','FontSize',20,'Background
Color','w');

% Diode 5
t_Ia_max_short=0:0.01e-6:tb_5_0_max;
t_Ia_max_shift=0:0.01e-6:tb_5_max
t_ID=0:0.01e-6:4e-3;
time_Ia1=0:0.01e-6:1e-3
ID5_forced_short_max1=Ic_max_Long;
ID5_forced_short_max1(length(t_Ia_max_short):length(time_Ia1))=0;
ID5_forced_short_max2=Ic1;
ID5_forced_short_max2(find((time_Ia1<(tf05_0_max))))=0;
ID5_forced_short_max=transpose(ID5_forced_short_max1)+ID5_forced_short_max2
ofset=0
Id05_forced_short=Id5_max;
Id05_forced_short(find(Id05_forced_short<0))=0;
Id05_forced_short=circshift(Id05_forced_short',length(t_Ia_max_shift)+ofset);
Id05_forced_short(1:length(t_Ia_max_shift)+ofset)=0;
Id05_forced_short(t_ID>time_Ia1(end))=[];
hFig = figure(3);
set(hFig, 'Position', [0 0 1500 700])
```

```
Combined_D5=(ID5_forced_short_max/2)+Id05_forced_short';
D5_less_0=find(Combined_D5<0);
Combined_D5(find(time_Ia1<tf05_max))=ID5_forced_short_max(find(time_Ia1<tf05_m
ax));
Combined_D5(find(Combined_D5<0))=0;
hold on
plot(time_Ia1*1e3,Combined_D5/1000,'--r')

% Diode 6
Combined_D6=(-ID5_forced_short_max/2)+Id05_forced_short';
Combined_D6(find(Combined_D5==0))=-
ID5_forced_short_max1(find(Combined_D5==0));
D6less_0=find(Combined_D6<0);
Combined_D6(Combined_D6==0)=80.32;
hold on
plot(time_Ia1*1e3,Combined_D6/1000,'--r')
legend1=legend({'Simulated diodes currents', 'Calculated diodes currents'});
set(legend1,'FontSize',14);
ax = gca;
ax.LineWidth = 2.5;
fig=gcf;
set(findall(fig,'-property','FontSize'),'FontSize',14);
style = hgexport('factorystyle');
style.Bounds = 'tight';
hgexport(fig,'-clipboard',style,'applystyle', true);
drawnow;
grid on
xlabel('Time (ms)');
ylabel('Current (kA)');
xlim([0 1.0]);
text(0.3,1.9,'I_{D5}','HorizontalAlignment','center','FontSize',20,'Background
Color','w');
text(0.3,0.8,'I_{D6}','HorizontalAlignment','center','FontSize',20,'Background
Color','w');
```