Monolithic Integration Piezoelectric Resonators on CMOS for Radio-Frequency and Sensing Applications

Aida Raquel Colon

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ABSTRACT

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Software cognitive radios and Internet of Things (IoT) are recent interest areas that need low loss and low power consumption hardware. More specifically, the area of software cognitive radios requires that hardware be frequency agile and highly selective. Meanwhile, IoT relies on multiple low power sensor networks. By combining Complementary Metal Oxide Semiconductors (CMOS) technology with piezoelectric Micro-Electro-Mechanical Systems (MEMS), we can fabricate Systems-on-Chip (SoC) that can be used as filters or references (oscillators) and highly selective sensors.

In this work we developed a die-level compatible process for the monolithic integration of Bulk Acoustic Resonators (BAWs) on CMOS for low power, reduced area and high-quality passives for radio frequency applications. Using CMOS as a fabrication substrate some stringent requirements were added to maintain the dies and the technology's integrity. A few of these limitations were the need for a low thermal budget fabrication process, die handling and electro-static discharge (ESD) protection. The devices were first fabricated on glass for modeling extraction that was later used for the design of the integrated circuits (IC). Three integrated circuits were designed as substrates for the integration using IBM's 180nm and TSMC's 65nm technology. A monolithic BAW oscillator with a resonance frequency of 1.8GHz was demonstrated with an FOM ~186dBc/Hz, comparable to other academia work.

Using the developed process, a membrane BAW structure (FBAR) was integrated as well. Using a susceptor coating and zinc oxide's (ZnO) high temperature coefficient of frequency (TCF) the device was studied as an alternative uncooled infrared sensor. Finally, a reprogrammable IC and an RF PCB were designed for volatile organic compound (VOC) testing using self-assembled monolayers (SAMs) as the absorber layer.

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Chapter 1 **: Introduction**

The general trend for electronics has been to scale down to reduce area and lower power consumption, making it cost-effective. Complementary Metal-Oxide-Semiconductor (CMOS) technology is not an exception. There is a continuous effort for reducing transistor sizes (nodes) to produce higher density per area on wafers. This effort is fueled by the era we live in, where most of technology is now digital based and new applications with low power consumption and re-programmability needs are now possible. Up to recently CMOS technology was able to scale down at the rate Moore's Law predicted, every two years transistor density would duplicate by shrinking gate length. That gate length reduction (<Cgs) makes CMOS the preferred technology for radio frequency (RF) applications due to its low cost per area, low power consumption and large frequency response (bandwidth/ft)[1]. The foundation of RF communication systems are filters and oscillators all of which rely heavily (if not fully) on resonators (passives). Radio frequency integrated circuit (RFIC) designers are limited to the CMOS foundry toolkit, where passives are the limiting factor of the technology.

1.1 Passives: Mechanical vs Electrical (LC)

Although transistors were able to follow the predicted scaling map, its passives, such as inductors and capacitors, were not. On chip capacitors (C) and inductors (L) are large in size, this is dead area that cannot be used for circuitry, due to the magnetic fields of the inductors [1]. To characterize these components Quality Factor (Q) is an important metric that relates energy stored to energy lost, and is defined as,

$$Q = \frac{\omega L}{R} = \frac{2\pi f L}{R}$$

In filters and oscillators high Q is preferred because this parameter defines how selective or how stable the oscillation frequency is respectively. CMOS offers front end capacitors, moscaps, made alongside MOSFETs and backend Metal-Insulator-Metal (MIM) caps with quality factors (Q) of ~100. Inductors on the other hand are very lossy with Q~10[2], [3]. This high loss comes from the induced current leakage from the magnetic field generated by the inductor through the substrate, this current leakage is known as eddy current. The magnetic field is yet another reason as to why there cannot be any routing or interconnects under, it would affect and most likely change the expected circuit behavior.

Off-chip components, more specifically inductors, display higher Q and do not take up any on-chip area. These off-chip devices tend to be large making integrability and packaging complex. The only ways to connect an external device to the CMOS circuitry is either by flip chip, using ball grid arrays, or wire bonding to pads. These connection methods introduce parasitics, an undesired circuit behavior that increases power consumption at high frequencies (such as RF), this in turn, increases electrical losses and further decreases Q factor. As a result, both, on-chip and off-chip greatly limit the RF application capability due to size, power consumption and low Q (selectivity/stability) factor.

An alternative to LC components is mechanical passives, also known as micro electromechanical systems (MEMS). Mechanical resonators take an electric signal and convert it to mechanical by means of transduction mechanism [4]. These structures have lower electrical leakage, no DC path, but the mechanical coupling plays an important part in obtaining a high Q (>100)[5]. Quartz is a popular example of mechanical resonators, when connected to an amplifying circuit it can act as a crystal oscillator used in a variety of applications from RF to mass sensing due to its high stability (Q)[6], [7].

Mechanical resonators can also be found as off-chip components, but they have the same area and connection parasitic problems as their LC counterpart, albeit with higher Q[8]. One of the goals of this project was to develop a process flow for the monolithic integration of MEMS on-chip as part of the CMOS process where using the same interconnects and vias of the technology to bypass the need for wire bonds or flip chip.

1.2 Electrostatic vs Piezoelectric Resonators

There are different types of mechanical resonators and these are typically defined by the mechanism of transduction. Two of the most interesting mechanical resonators are electrostatic or capacitive and piezoelectric. Electrostatic resonators rely on high electric fields (voltage across terminals) to actuate the structure by attraction. These structures are very complex to fabricate, take up a lot of area and display high impedance values (>Mega-ohms). Piezoelectric materials are crystals, such as quartz, that when mechanically deformed they generate an electric field and vice versa if an electric field is applied a mechanical deformation occurs. Resonators using piezoelectrics have lower impedances (<500ohms) making it compatible for RF applications where 50-ohm terminations are expected. Piezoelectric transduction is more efficient than its electrostatic counterpart, making it more fitting for radio frequency applications where low losses are a must[9], [10].

1.3 CMOS ++ and 3D Integration

A relatively new concept known as CMOS ++ defines a new effort to enhance the capabilities of CMOS IC technology by effectively “patching” or filling the gaps it has in functionality. Monolithic integration of mechanical resonators, and avoiding the use of, with CMOS would allow for smaller area, high quality and low power consumption RF designs on chip. Rather than

handling and transferring on to CMOS the structures should be built as part of or on-chip after it arrives from foundry.

1.3.1Integration types

There are two fabrication modalities, bulk (intra-) and surface (post) micromachining. Bulk micromachining is a subtractive process that uses the CMOS body to make the device by specifying a pattern of release layers that will be etched after it arrives from the foundry [11]. On the other hand, surface micromachining is an additive process in which thin films are subsequently deposited on the surface of the CMOS chip after it is finalized [12]. These fabrication types can be classified further for MEMS integration as: MEMS-first and MEMS-last.

Electrostatic structures are fabricated under the MEMS-first processes, essentially structures are built along with sacrificial layers during the CMOS foundry fabrication. This style of processing dedicates an area just for MEMS and another one for CMOS, as shown in figure 1-1 [13]. MEMS-last processing allows for smaller areas by means of 3D monolithic integration piezoelectric resonators that can occupy areas directly over CMOS circuitry, as shown in figure 1-2 [14].

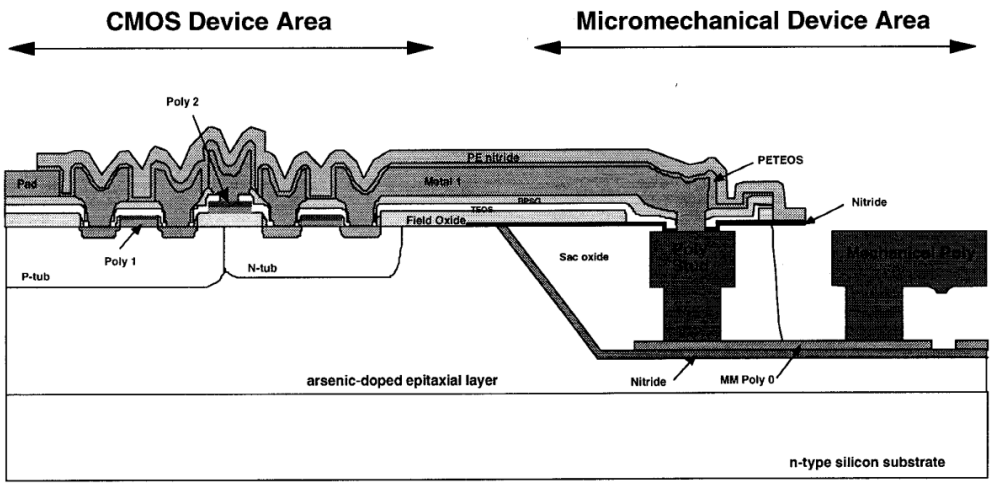

Figure 1-1: MEMS-first wafer partitioning [13]

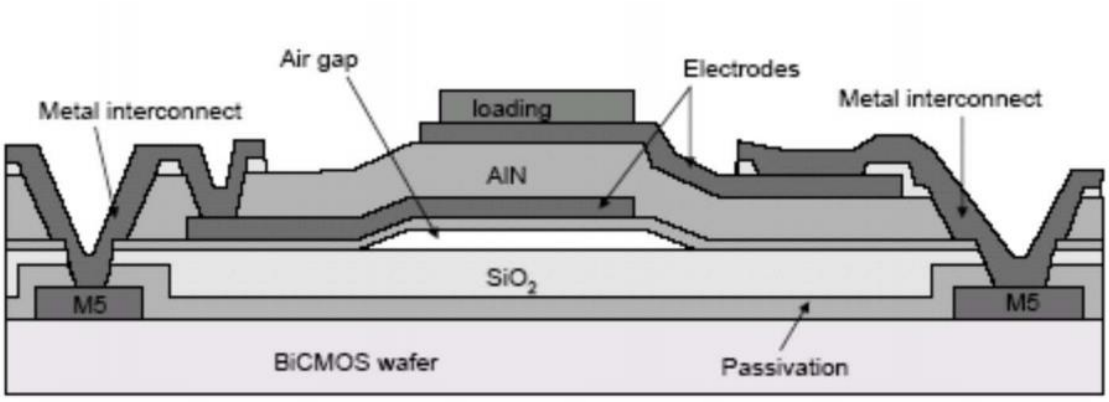

Figure 1-2: MEMS-last cross-section [15]

CMOS processing adds some new stringent requirements to the process development such as a thermal budget and the need for electrostatic discharge protection. Overcoming these obstacles will result in a high-quality MEMS on CMOS systems on chip, where the CMOS circuitry will depend on the mechanical resonator to operate, much like now a day with Xtal resonators. The xtal or piezoelectric will act as a frequency reference for the system, say an oscillator or filter. The Q factor will be much higher compared to off-chip components and on-chip LC because it is

integrated as part of the CMOS process and connected using interconnects from the technology. Therefore, 3D integration simplifies packaging

1.4 Thin Film Resonators

Radio frequency communication systems require high quality passives for their front-end filters, i.e. duplexers, that operate at high frequencies (>1GHz) with low insertion losses, small areas and low cost [16]. To obtain RF resonance frequencies the materials need to be in the submicron thicknesses, up until recent microfabrication advances this was not possible [17]. These piezoelectric devices are known as bulk acoustic wave (BAW) components, i.e. parallel plate devices, where the elastic wave travels through the body of the piezoelectric material and as such the following can be stated,

$$f \alpha \frac{1}{t}$$

where f is the resonance frequency and t is the material thickness. This relationship is missing the acoustic velocity which establishes how fast an elastic wave can travel through the medium. For these resonators to correctly operate, their device construction or topology needs to meet the boundary conditions for the elastic wave to be contained within the structure.

Quartz is still limited to MHz frequencies due to its low acoustic velocity and the thinning limitations [18], [19]. The process of thinning Quartz is complex due to large areas resulting in low processing tolerances, its low mechanical stability, and reduced mechanical coupling coefficient, k_t^2, due to non-uniform etching and rough surfaces [17]. The mechanical coupling coefficient defines the effective mechanical to electrical energy conversion and is considered one of the most important parameters, along with Q factor, for mechanical resonators [16]. A few

techniques were developed to work around the thinning challenges, one of them being bonded plate resonators, where a supporting material is used to prevent bowing of quartz while etching. The etching can occur from the top before adding the top electrode or from the backside through the hole on the supporting material [20], [21].

There was a need for higher acoustic velocity materials that could be grown on substrates instead of bonded and allowed for higher frequency applications. An alternative to thinning down was to grow piezoelectric materials with the desired thickness and this came to be known as composite resonator where the thin film is deposited onto a supporting structure. Composite structures came with their own challenges such as low coupling coefficients due to the thick supporting material. In the early 1970's a lot of work was done on developing thin film piezoelectric devices using materials such as zinc oxide (ZnO), aluminum nitride (AlN) , amongst others [22]–[25].

1.5 Applications: IoT and 5 G

Communication technology hardware developers have recently unveiled their plans for what will be the future of RF systems for 5G technology, where front-end and BAW technology is still used for filtering as shown in the following figures:

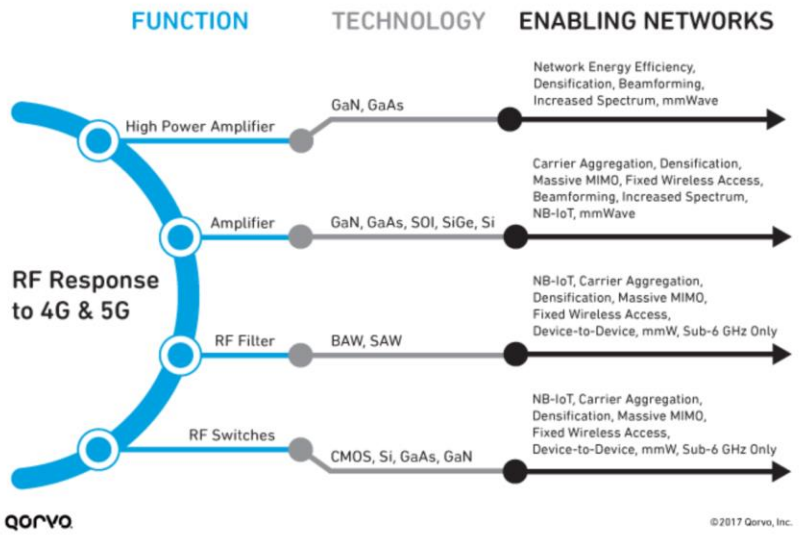

Figure 1-3: Front-end plans for 5G from Qorvo[26]

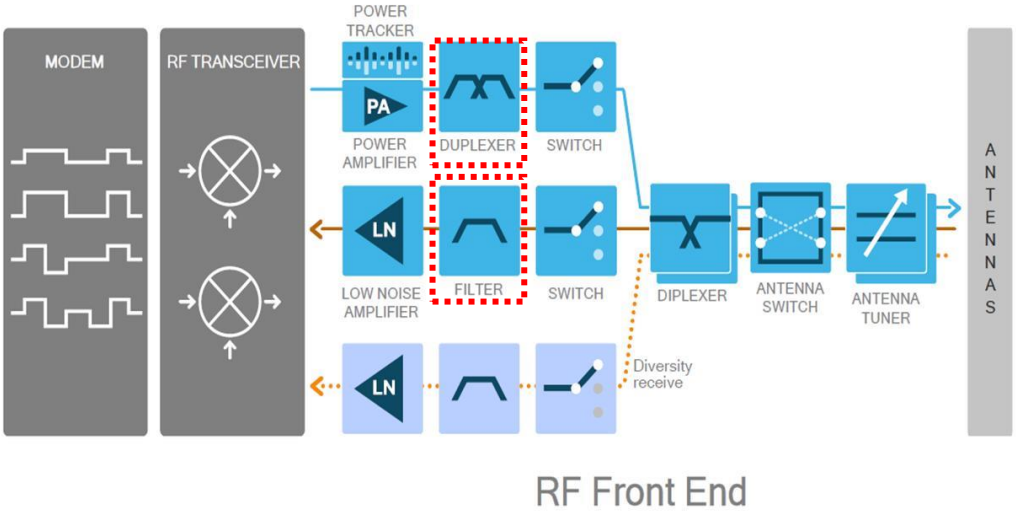

Figure 1-4: Front-end plans for 5G from Qualcomm[27]

It is clear that BAW technology will be around for a while in the RF communications industry where there is a need for highly selective, low insertion loss and high return rejection acoustic filters [28], [29].

After a monolithic process flow was developed the goal became to find other applications for this system such as Internet of Things (IoT). IoT involves a network of embedded systems communicating with multiple home appliances, automobile and sensors [30]. This project focused on developing low power infrared and gas sensors to be used in these up and coming networks.

1.5.1 Infrared (IR) Sensors

Research in IR sensing technology has increased with growing interest in military, defense, astronomical and commercial applications [31]–[33]. There are two types of detectors for IR wavelengths: optical and thermal. Optical detectors rely on the use of semiconductors and their bandgap to measure the photonic excitation. These sensors require cooling to avoid thermal noise from exciting particles and overcoming the bandgap [32]. The cooling systems needed for these sensors makes them bulky, power consuming and expensive. Thermal detectors depend on the conversion of the incident radiation to temperature and the transduction of the thermal change into an electrical signal [34], [35]. These detectors are designed to work at room temperature (300K) and do not require cooling, hence the name uncooled IR sensors. Uncooled sensors are based on MEMS devices to overcome the limitations of optical sensors, i.e. narrow bandgaps, with small areas and thermal mass, making this a high sensitivity and low-cost technology. Some of the more popular examples of uncooled IR sensors are pyroelectric sensors, thermopiles, ferroelectric and bolometers [35]. The leading technology is

microbolometer focal point array (FPA) with a noise equivalent thermal drift (NETD) of ~20mK, below figure 1-5 shows a microbolometer pixel.

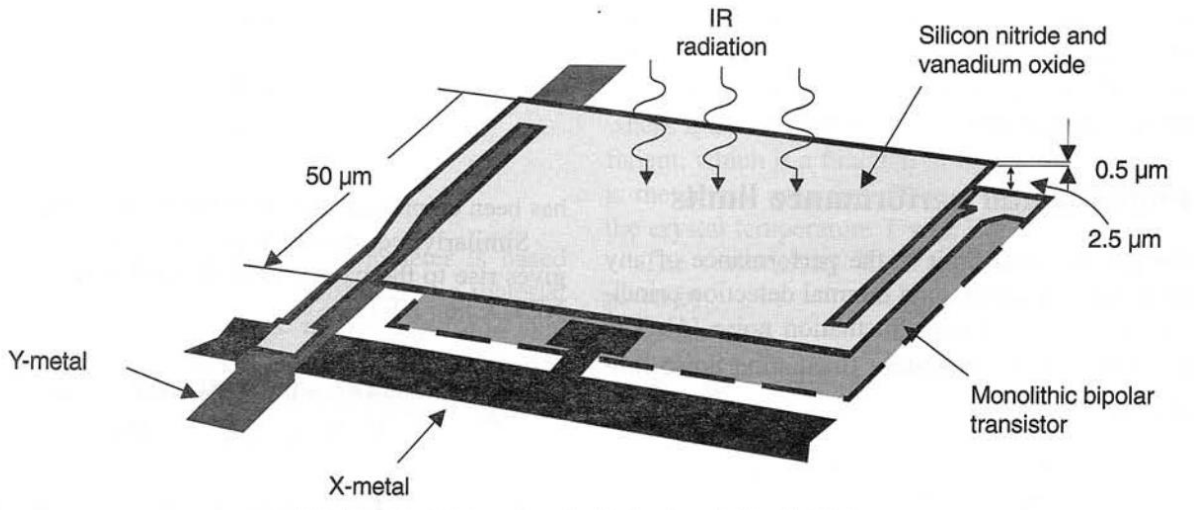

Figure 1-5: Microbolometer pixel [36]

1.5.2 Gas Sensing

There are multiple technologies for chemical vapor sensing and they are classified under four main branches defined by the sensing mechanism: optical, thermal, electrochemical and gravimetric as shown in figure 1-6.

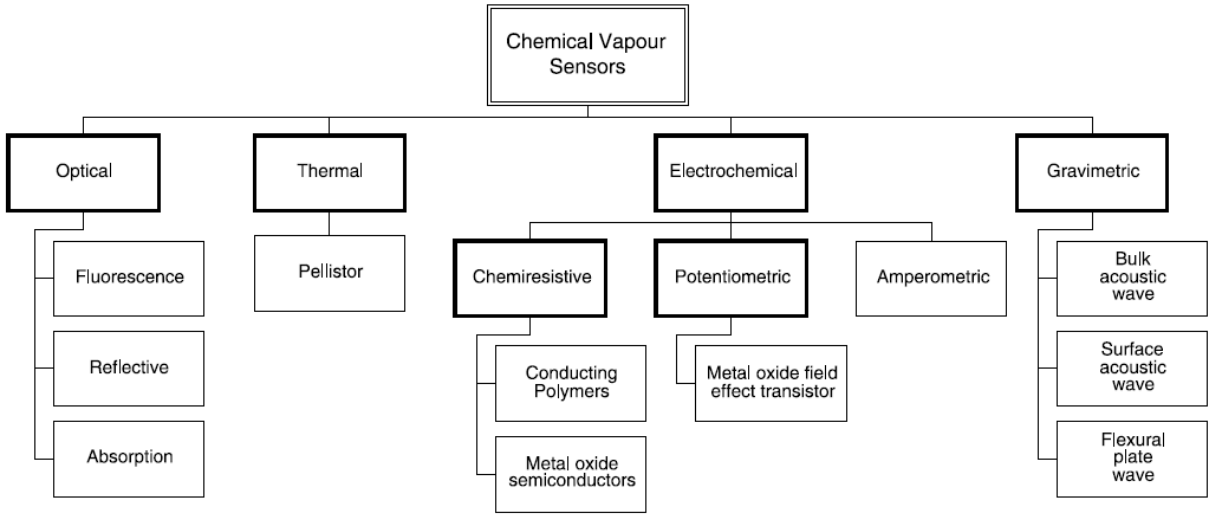

Figure 1-6: Chemical vapor sensor technology tree [37]

For electric nose (E-nose) or internet of things (IoT) applications the detectors must be small and low power and preferably low cost for consumers. Technologies such as mass spectroscopy and gas chromatography are expensive, bulky and require trained personnel. An ideal gas sensor should be reversible, robust, sensitive and selective, with this in mind the most popular technologies right now are MOS, piezoelectric sensors and conducting polymers devices[37]. MOS devices display high selectivities and long lifetimes but require high operating temperatures not compatible for IoT applications due to the power needed for operation[38], [39]. Conducting polymers (CP) do not require heating and considerably low power (<50mW) but their lifetimes are short, can range from a few weeks up to a year[40]. Piezoelectric sensors provide a low power, high sensitivity, and low-cost alternative for gas sensing. Selectivity in a piezo sensor will depend on the absorber coating layer and the frequency of oscillation as explained in the following section. Table 1-1 shows a comparative summary of the important properties.

Sensor	*Heating*	*Lifetime*	*Power Consumption*	*Limit of Detection*
MOS [38], [41]	YES ([300-500] °C)	Years	High (>800mW)	~ [5-500] ppm
BAW	NO	Years	[0.4-4] mW	~1ppm
Organic-conducting polymers	NO	Short (months- 1 year)	~20mW	~5 ppm

Table 1-1: Comparison of popular technologies for VOC sensing

Chapter 2 **: Background**

In acoustic components, phonons (acoustic waves) travel through elastic mediums by transferring energy from an excitation or actuation in the form of compression, i.e. oscillations. If stress is applied to elastic solids it causes a change in strain. This elastic behavior in acoustic devices, if the deformations are small, can be described with Hooke's law

$$F = x * k \tag{2.1}$$

where *F* is the magnitude of the force applied, *k* is the spring constant and *x* is the distance of deformation. This equation can be rewritten for solids in terms of strain and stress as follows:

$$T = cS \tag{2.2}$$

where *T* is stress, *S* is strain and *c* is mechanical stiffness which is a material dependent property.

From Hooke's law, strain can be defined as follows:

$$S = \frac{\partial u}{\partial z} \tag{2.3}$$

where *u* is the particle displacement and ∂z is material thickness. Another way to define *T* comes from using Newton's second law:

$$F = m * a \tag{2.4}$$

where *m* is mass and *a* is acceleration, and a new equation with different material parameters can be extracted.

$$\frac{\partial T}{\partial z} = \rho * \frac{\delta^2 u}{\delta t^2} \tag{2.5}$$

Here ρ is mass density of the material. Combining the above equations results in the wave equation:

$$\frac{\partial^2 u}{\partial t^2} = \frac{c}{\rho} * \frac{\partial^2 u}{\partial z^2} \tag{2.6}$$

This equation describes a wave propagating with a phase velocity, also known as acoustic velocity of the wave, as follows:

$$v = \sqrt{\frac{c}{\rho}} \tag{2.7}$$

Now, assuming a general form for particle displacement,

$$u(z,t) = [a * \sin(kz) + b * \cos(kz)] * e^{j\omega t}$$

where *k* is the propagation constant or wave number and *a* and *b* are constants that need to be solved for with the boundary conditions. By inserting the particle displacement definition into the wave equation and solving for *k*,

$$k = \frac{\omega}{v} = \frac{2\pi}{\lambda} \tag{2.8}$$

in which λ is the wavelength.

2.1 Piezoelectricity

Piezoelectricity comes from Greek, meaning electricity in result to pressure. Some solid materials, typically crystals or dielectrics, can generate charge when a mechanical deformation is forced on them. Not all crystals have piezoelectric properties, it depends on their atomic structure [10], [42]–[44]. Only non-centrosymmetric crystal structures, such as wurtzite, where there is spatial separation between the charges (dipole). When an external mechanical force is

applied such that it deforms the material an electrical field is generated as shown in figure 2-1. On the other hand, the same is true for when an electrical field is applied these charges will be displaced causing a mechanical deformation, this is called the inverse piezoelectric effect as shown in figure 2-2.

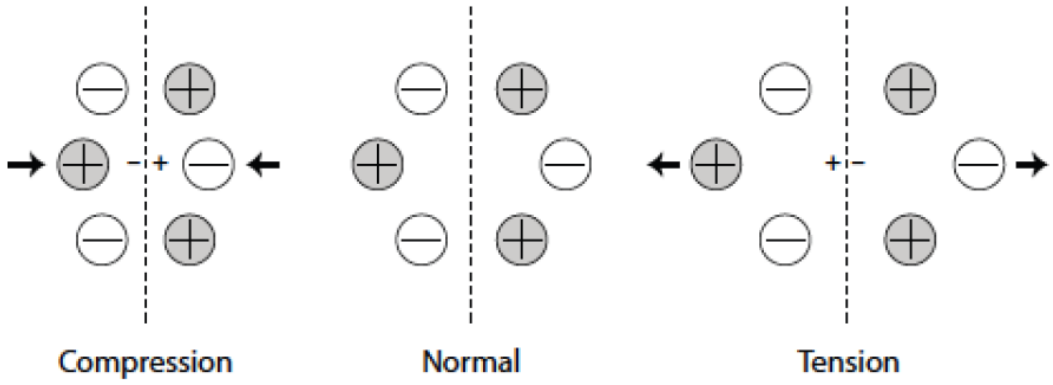

Figure 2-1: Piezoelectric polarization effect [43]

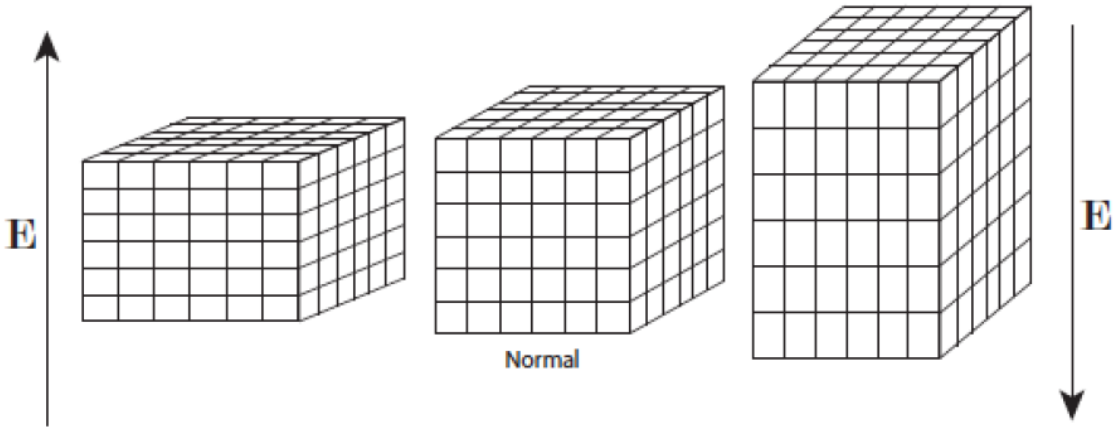

Figure 2-2: Inverse piezoelectric effect [43]

2.2 Types of Acoustic Waves: BAWS vs SAWS

Acoustic or piezoelectric resonators can be categorized in two types, surface acoustic wave (SAW) and bulk acoustic wave (BAW), depending on how the acoustic wave travels through the device. SAW waves travel through the surface as elliptical ripples known as Rayleigh waves as shown in figure 2-3.

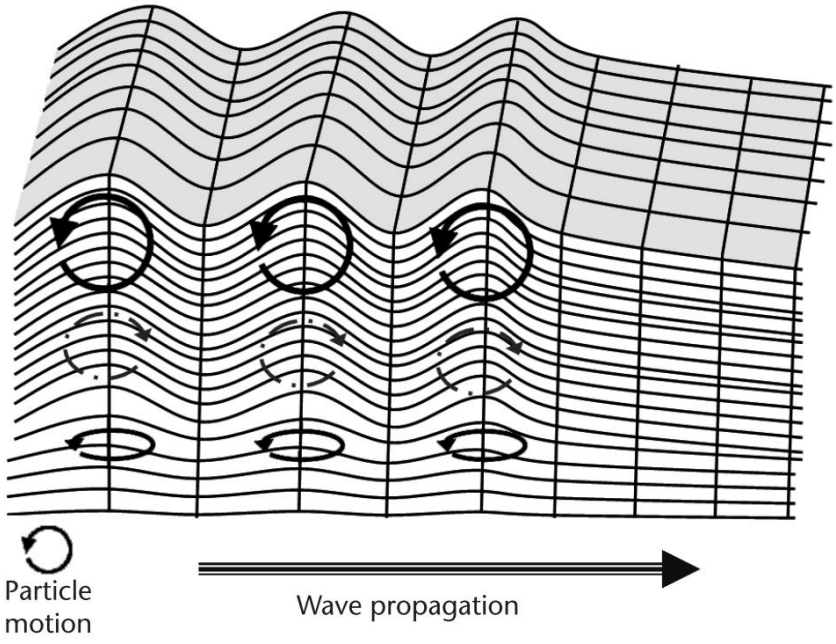

Figure 2-3: Rayleigh waves[44]

SAWs require interdigitated (IDT) generator and receiver electrodes known as fingers. The frequency of the signal generated (resonance) will depend on the finger pitch. Because there must be a gap between both transmitter and receiver these devices take up a lot of area. The fabrication of these devices is simple compared to BAWs, needing one lithography step for the IDTs. Because of the complexity of patterning submicron features these resonators are restricted to low GHz. SAWs where often used in duplexers but because of their poor power handling and

large area they were substituted with BAWs allowing cellphones to reduce their thickness [16], [45].

In BAWs the structure is comprised of a metal-piezo-metal stack, because of this it has a better power handling capacity than SAWs. The frequency of resonance is established by the thickness of the piezo. The acoustic wave travels through its body and are classified as compression waves which can be further subdivided into longitudinal and shear [16], [44], as shown in figures 2-4 and 2-5.

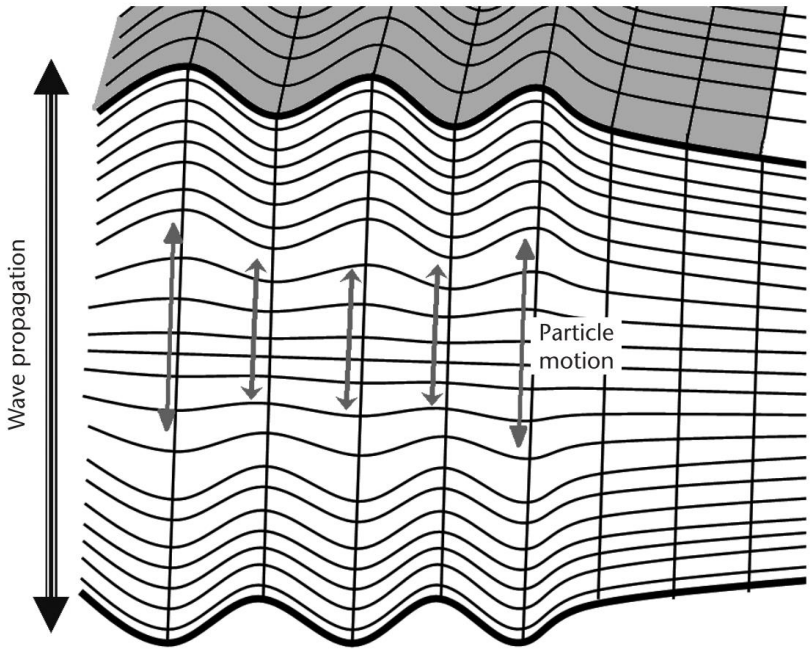

Figure 2-4: Longitudinal waves [44]

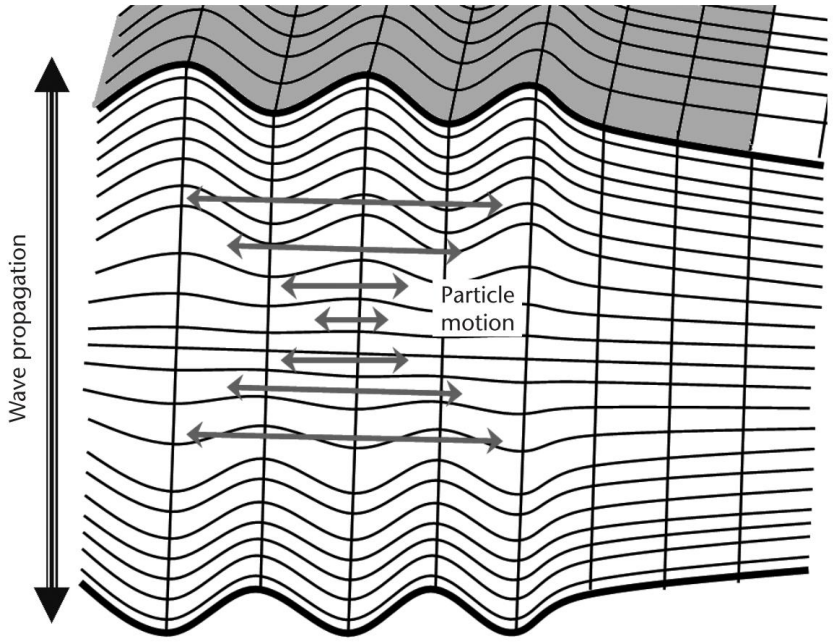

Figure 2-5: Shear waves [44]

To distinguish between both bulk waves types the key is to observe what direction the particles are oscillating. For longitudinal waves the particles vibrate in the same axis as the wave is propagating. For shear waves the particles vibrate perpendicular to the wave propagation axis.

2.3 Piezoelectric Acoustic Devices

2.3.1 Electrical Modeling

The most used method for generating acoustic waves is by using the piezoelectric effect to generate mechanical resonance from an electrical signal. The piezoelectricity also causes the reverse effect, an electrical signal is generated at the output as a response to the mechanical resonance.

To describe the piezoelectric behavior there are two equations often used:

$$T = cS - eE \tag{2.9}$$

$$D = eS + \varepsilon E \tag{2.10}$$

Where E is electric field, D is displacement and e and ε are material constants piezoelectric constant and permittivity respectively. Both equations have been modified for a piezoelectric medium by adding the piezoelectric constant. The first equation is Hooke's law modified for piezoelectric mediums by adding the piezoelectric constant, the equation now describes the emergence of an electric field due to an applied stress. The second equation defines inverse piezoelectric effect as the mechanical strain contribution to displacement current and electric charge generation.

Combining both equations and solving for stress results in,

$$T = c^E\left(1 + \frac{e^2}{c^E\varepsilon^S}\right)S - \frac{e}{\varepsilon^S}D = c^D S - \frac{e}{\varepsilon^S}D \tag{2.11}$$

where the E and S superscripts signify under constant electric field and strain, respectively. Assuming D is constant in piezoelectric mediums and inserting this in the wave equation a new acoustic velocity is obtained,

$$v^D = \sqrt{\frac{c^D}{\rho}} = \sqrt{\frac{c^E}{\rho}} * \sqrt{1 + K^2} = v * \sqrt{1 + K^2} \tag{2.12}$$

This equation shows how piezoelectricity stiffens the material and therefore increases the acoustic velocity. The K^2 is a material property of electroacoustic conversion efficiency and can be solved for from the above equation:

$$K^2 = \frac{e^2}{c^E\varepsilon^S} \tag{2.13}$$

This is different from the effective coupling coefficient (Kt^2), which relates the series frequency to the parallel (antiresonance) frequency and is defined as follows,

$$K_{eff}^2 = \frac{\pi}{2} * \frac{f_s}{f_p} * \cot\left(\frac{\pi}{2} * \frac{f_s}{f_p}\right) \quad (2.14)$$

This is an experimental parameter used to quantify the efficiency of the structure and material to transduce energy between the mechanical and electrical domains.

2.3.2 Electrical Models

There are several models used to explain and predict mechanical resonator's behavior and performance. The most popular of those are the Mason transmission line and lumped Butterworth Van-Dyke (BVD) models. The Mason model facilitates the analysis of acoustic stacks, such as in SMR, by showing the electrical response as a function of their thicknesses and physical parameters [46]. A static capacitance known as Co will show in every model of BAWs because of the metal-piezo-metal physical structure and it can be calculated from the dimensions of the device as follows,

$$C_o = \frac{\varepsilon_S A}{d} \quad (2.15)$$

where A is the active area of the device, d is the piezoelectric thickness and ε is the permittivity constant for the piezo material. An electric field in this structure is modeled, starting with the inverse piezoelectric effect, as

$$E = \frac{1}{\varepsilon^S} * D - \frac{1}{\varepsilon^S} * S = \frac{1}{\varepsilon^S} * D - \frac{1}{\varepsilon^S} * \frac{\partial u}{\partial z}$$

From here the voltage in the piezoelectric layer can be calculated by integrating the electric field over the thickness of the bulk, assuming the thickness to be 2h,

$$V = \int_{d_1}^{d_2} E(z)dz = \frac{2hD}{\varepsilon^S} - \frac{e}{\varepsilon^S} * [u(d_2) - u(d_1)]$$

The current is assumed to be only displacement current because the piezoelectric is a dielectric, defined as, $J = \frac{\partial D}{\partial t}$. Knowing this, the current flowing between the electrodes is,

$$I = j\omega A * D \tag{2.16}$$

Using the definition for particle velocity,

$$v = \frac{\partial u}{\partial t} = j\omega \tag{2.17}$$

the equation now becomes,

$$V = \frac{2h}{\varepsilon^S} * \frac{I}{j\omega A} - \frac{e}{j\omega\varepsilon^S} * [v(d_2) - v(d_1)] \tag{2.18}$$

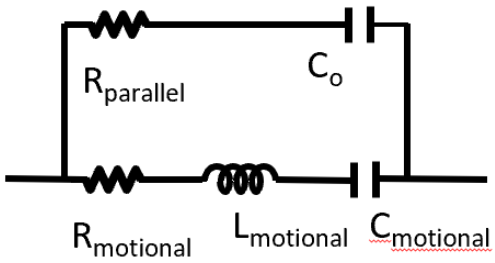

Figure 2-6: *Butterworth Van-Dyke (BVD) model*

Although the Mason model provides a simple way of analyzing acoustic stacks it isn't ideal for electrical parameter extraction. The BVD model describes the system as a lumped circuit, which can be used to extract the Q factor and as a model in circuit designs for further integration. The BVD model sees mechanical resonators as parallel branches, the static and motional, as seen in figure 2-6. The static branch consists of the capacitance C_o, this is a given from the physical

structure (metal-piezo-metal sandwich). The motional branch is a series motional resonator it has a motional inductor (L_m), a motional capacitor (C_m) and resistive loss term (R_m). This model shows two resonances a series resonance (f_s) and a parallel resonance (f_p) also known as the antiresonance. Shown below are:

$$f_s = \frac{1}{\sqrt{(L_m - C_m)}} \tag{2.19}$$

$$f_p = f_s * \left(1 + \frac{C_m}{2 * C_o}\right) \tag{2.20}$$

Kt^2 can be extracted from this model by noting that Cm/Cp is proportional to (fp-fs). How large Cm is compared to Co defines how much electrical input is transduced into mechanical energy, another way of looking at electroacoustic efficiency.

2.4 Device physics and topologies

Many applications in physics and electronic circuits need some devices that establish some signals oscillations. An oscillator is a device that establishes some periodic oscillating signals with no need of an external input. Bulk Acoustic Wave (BAW) are devices consisting of a metal-piezo-metal sandwich where when an electrical signal is applied at the input the device will oscillate at its natural frequency. The natural frequency of oscillation is called the frequency at which the device will continue oscillating without and external force or input. It means that the output signal will behave as a filtered signal, at the natural oscillation frequency of the device.

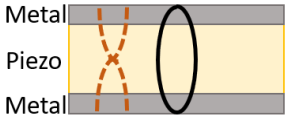

Figure 2-7: BAW acoustic wave and strain lines

That natural frequency will allow the component to come into resonance. At the resonance frequency oscillations will increase and remain. The resonance frequency of the device depends of the physical characteristics of the device, and in the BAW it will depends on the thickness of the piezoelectric material:

$$\lambda = 2d = \frac{f}{v} \tag{2.21}$$

Where λ is the wavelength of the oscillation, d is the device thickness, f is the resonance frequency and v is the acoustic velocity of the material. As shown above, the wavelength will be two times the thickness assuming a half wave operation where the wave travels half way to the first boundary and reflects back another half effectively creating a standing wave. The acoustic velocity is related to the square root of the stiffness constant c_{ii} (related to the Young's Modulus it defines the amount of force a material can resist before deformation) and inversely related to the material density, ρ, as shown below:

$$v = \sqrt{\frac{c_{ii}}{\rho}}$$

There are two types of BAW topologies, Solidly Mounted Resonators (SMR) and Thin Film Membrane Resonators (FBAR). The mechanical support and surface isolation structure, where

the intrinsic core of the device remains the same, is what defines and differentiates each of the resonators.

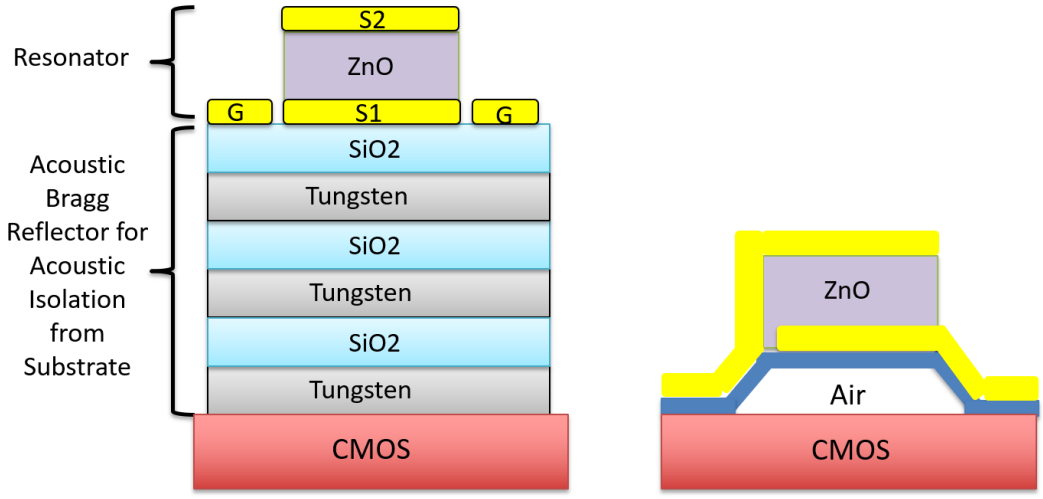

Figure 2-8: BAW topologies: From left to right is the Solidly Mounted Resonator (SMR) and the Thin Film Bulk Acoustic Resonator (FBAR)

2.4.1 Solidly Mounted Resonator (SMR)

2.4.1.1 Bragg reflector

SMRs have the resonator (metal-piezo-metal) on top of an acoustic bragg reflector. The bragg reflector is made up of alternating low and high acoustic impedance, silicon dioxide (SiO2) and tungsten (W) or alternatively molybdenum (Mo). The bragg structure will provide mechanical isolation from the substrate for a specific bandwidth of frequency. Like in the optical analog, bragg reflectors will filter out any frequencies outside of the bandwidth of oscillation, which in this case is beneficial to eliminate any possible overtones or spurious modes. Mechanical isolation happens as result of reflected waves at the interface of the low and high impedance

layers. These reflections will cause that part of the wave to go back to the resonator structure, effectively increasing the energy stored and therefore the device's quality factor.

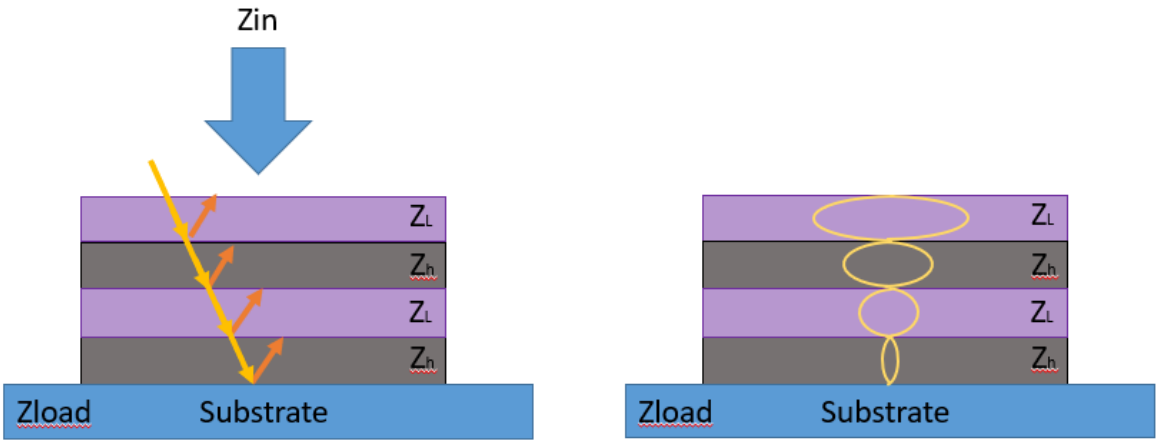

Figure 2-9: Acoustic impedance seen by the metal-piezo-metal stack

To understand how the bragg reflector (also known as mirror stack) works we can assume a periodically alternating structure as shown in figure 2-9 and apply transmission line theory to describe the input impedance, Z_{in}. Seen looking into the structure the input impedance can be represented as:

$$Z_{in} = Z_a \left(\frac{Z_L \cos(\beta l) + j Z_a \sin(\beta l)}{Z_a \cos(\beta l) + Z_L \sin(\beta l)} \right) \tag{2.22}$$

Where Z_a is the acoustic impedance of the medium or material where the acoustic wave is traveling in, Z_L is the impedance of the preceding layers, l is the thickness or length the wave must travel (propagation layer) and β is the phase constant of the propagation layer and can be defined as

$$\beta = \frac{2\pi}{\lambda} = \frac{\omega}{v_a} \tag{2.23}$$

Due to the large impedance mismatch at the interface, there will be a reflection of each mirror pair. This can be calculated using:

$$\Gamma = \frac{Z_L - Z_a}{Z_L + Z_a} \tag{2.24}$$

also known as the reflection constant for impedance mismatch at the interface.

In summary, the bragg reflector is emulating the acoustic impedance of air such as the bottom electrode meets the same boundary condition as the top electrode, effectively containing the wave. Bragg reflectors will never allow for perfect isolation due to mechanical dampening, this will result in mechanical losses that translate to lower quality factors.

2.4.1.2 Material selection

As explained in the previous section the materials selected for the bragg reflector should have high acoustic impedance mismatch and must be sputter compatible for fast deposition rates. Due to availability and because it has a low acoustic impedance, silicon dioxide (SiO_2) was selected as one of the materials. For the high acoustic impedance molybdenum (Mo) and tungsten (W) were considered. Table 2-1 shows the different materials of the stack and their equivalent acoustic impedances. Using the equation 2.22 a Matlab script was used to see the effect of the different metals and the number of layers.

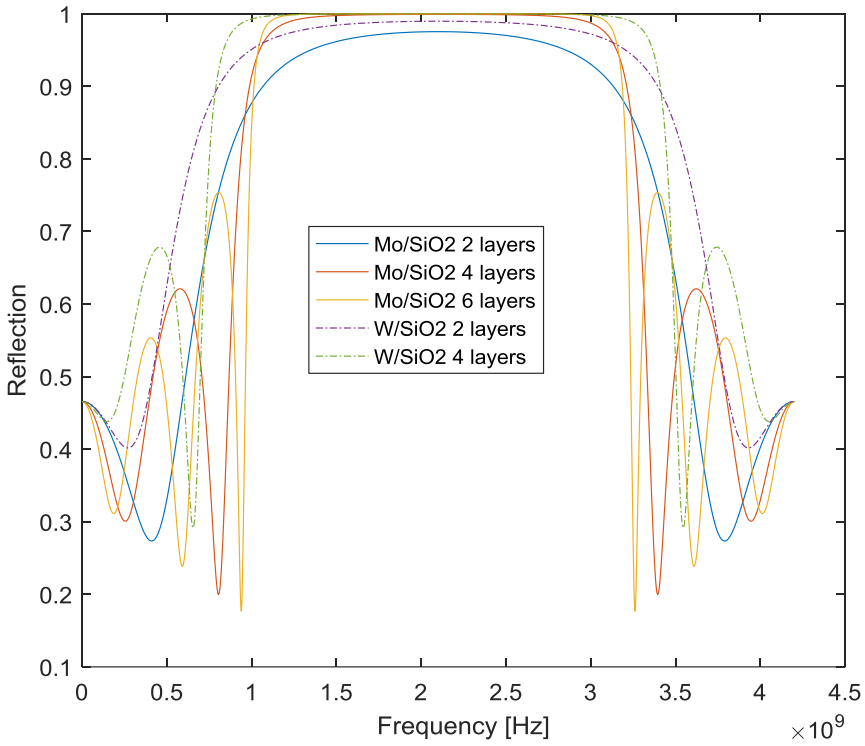

Figure 2-10: Materials reflections vs frequency of oscillations

In figure 2-10 we can see that Tungsten (W) has a higher reflection ratio for the same number of mirror pairs as Molybdenum (Mo), this is due to the higher density of W.

Material	***Density [kg/m^3]***	***Acoustic velocity [m/s]***	***Stiffness Constant [N/m^2]***	***Acoustic Impedance [ohm]***	***Thickness @1.8GHz [nm]***
Zinc Oxide	5680	6900	20.97e10	3.412e7	1300
Tungsten	19250	5200	58.1e10	10.57e7	650
Silicon Dioxide	2200	5900	7.2e10	1.258e7	680
Molybdenum	10280	6290	45e10	6.801e7	780

Table 2-1: Materials Characteristics

2.4.2 Thin Film Bulk Acoustic Resonator (FBAR)

2.4.2.1 Membranes

FBAR devices have an airgap under their resonators and use an anchored membrane for the support of their structures. The air gap can be either bulk or surface micromachined, as presented in figure 2-11. For bulk micromachining (A.1 and A.2), as the name suggests, the bulk of the substrate under the active device is removed and this is normally done by wet etching. These devices cannot be fabricated on top of other systems (i.e. CMOS) because the back side or under lying area of the active device is to be removed.

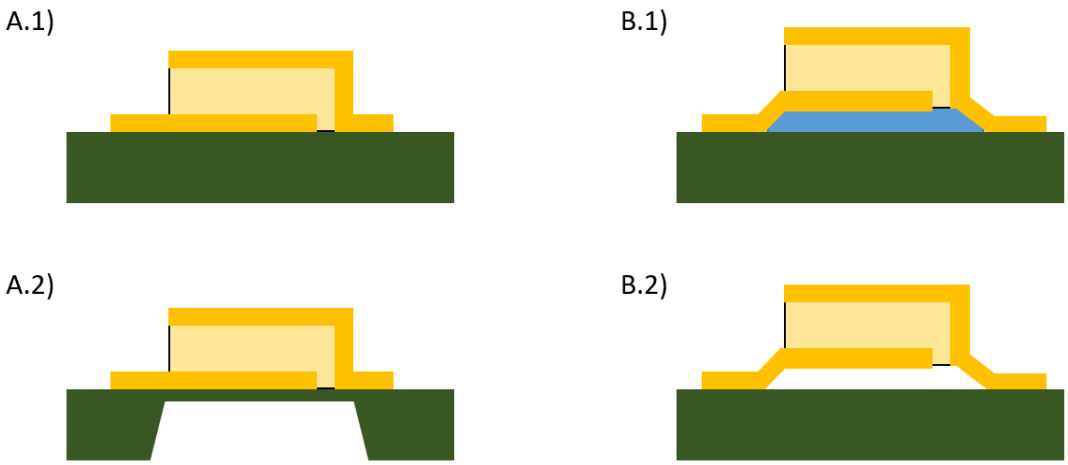

Figure 2-11: Two methods for membrane fabrication: A) bulk micromachining and B) surface micromachining

Surface micromachining, B.1 and B.2 of figure 2-11, is the process of depositing a sacrificial thin film before the device is fabricated and then selectively etching it by means of isotropic dry etch. One popular sacrificial layer is amorphous silicon which can be etched using XeF_2, a high selective gas. This method has the advantage that it is not destructive to the substrate, meaning

these devices can be fabricated on top of CMOS effectively reducing the lateral area needed. Surface micromachining is an additive fabrication process, while bulk micromachining is only subtractive.

As the resonator is surrounded by air, these devices will show higher energy storage capabilities (quality factor) than its SMR counterpart. These structures, however, are not as mechanical stable or robust as SMRs and are therefore no recommended for applications requiring liquids or high humidity environments.

Chapter 3 **: Methods**

3.1 Geometry

The devices were fabricated on glass for characterization and avoid reduce parasitics, i.e. losses through the substrate modeled as capacitive coupling. For electrodes a ground-signal-ground (GSG) topology was designed for probing with the vector network analyzer (VNA). The active area dimensions are 100µm x 100µm and 150µm pad pitch for the co-planar GSG probes, as shown in figure 3-1.

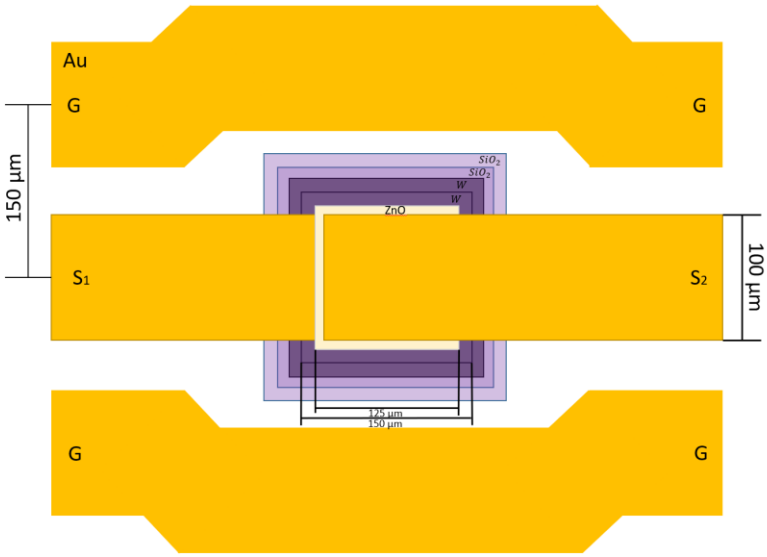

Figure 3-1: Top view of SMR device topology on glass substrates

For alignment purposes the mirror stacks were designed to be 25µm larger than the previous layer starting from the active layer, i.e. mirror #1 is 125µm and mirror #2 is150µm. For glass samples only, the metal mirror layers were patterned while the dielectric (SiO2) was blanket over to reduce edge sharpness and lower capacitive shunting, as shown in figure 3-2.

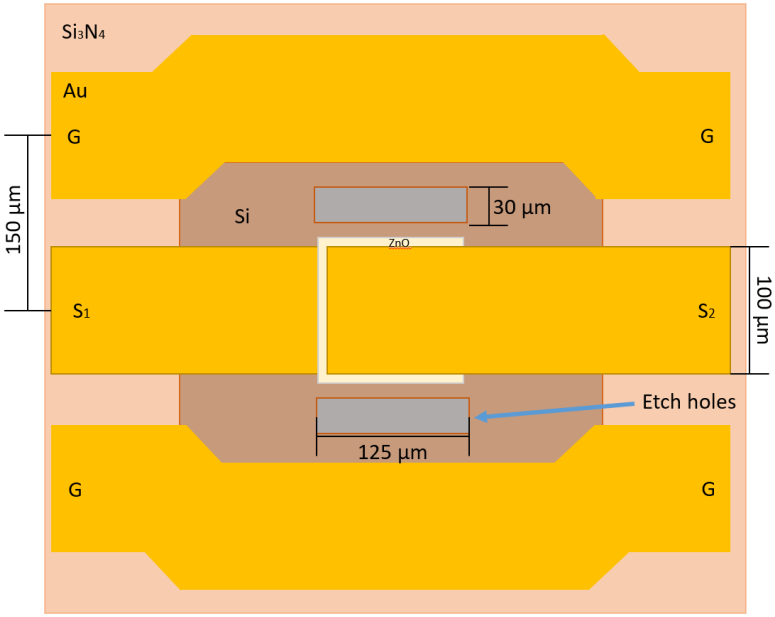

Figure 3-2 Top view of FBAR device topology on glass substrates

The FBAR device geometry is near the same as for the SMR topology but with fewer patterning steps needed. An amorphous silicon island is used as the sacrificial release layer. A blanket silicon nitride (Si_3N_4) is deposited and used for stress compensation.

3.2 Fabrication

3.2.1 Patterning

For the bragg reflector there were three approaches attempted: ziggurat, etched mirror and inverted pyramid as shown in figure 3-3. There are two methods of transferring desired patterns onto a substrate both require patterning, but one is subtractive (etching) and the other additive (lift-off). For patterning ultra-violet contact photolithography was used.

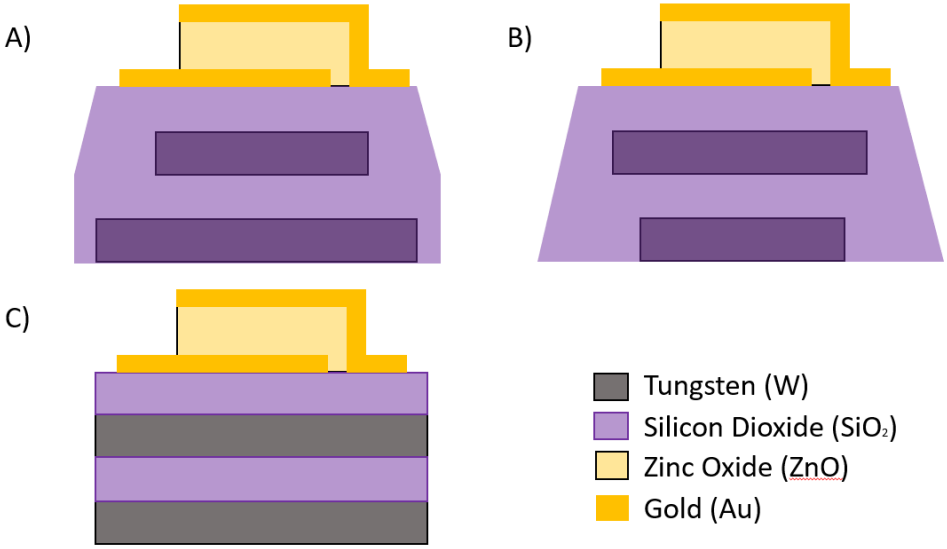

Figure 3-3: Different types of bragg reflector mirrors: a) ziggurat, b) inverted pyramid and c) etched stack

Ziggurat and inverted pyramid use the patterned bi-layer lift-off microfabrication technique, where a buffer polymer, lift off resist (LOR), is spun before the photo sensitive resist. When the bi-layer is exposed to UV through the chrome lime glass mask pattern the exposed areas of photoresist will have their bonds weakened, if the resist is positive. The sample is then developed, and these exposed areas will be removed as well as the underlying LOR, which has a higher develop rate than the photoresist. Normally the sample is developed until an undercut can be seen. After developing, the sample is placed in a reactive ion etcher (RIE) or asher to remove any remaining residue from the development process, before depositing the desired layer material. The sample is placed in a remover PG solution (M&P) to remove the patterned resist, the undercut will prevent any sharp edges from this process. This additive process, shown in figure 3-4, is preferred for some cases to prevent sharp edges that might cause shorting and for other situations were etching a specific material is not possible or is complicated.

Starting with a) cleaning a substrate with acetone and IPA the sample is b) spun with lift off resist (LOR) 30B and baked at 170℃ for 5 minutes. As part of the bi-layer lift off process a second resist (photosensitive - S1811 or SPR220) is c) spun and baked at 116℃ for 2 minutes. The sample is d) patterned with UV photolithography and the exposed areas are removed with developer (AZ 300MIF) for 1 minute, then the e) film is deposited and f) place sample in remover PG for removal of remaining resist to obtain desired pattern.

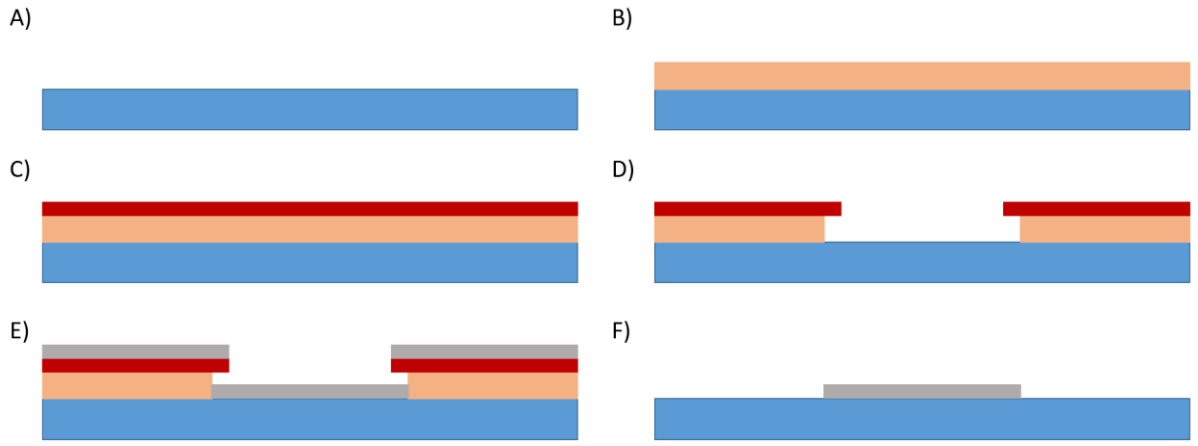

Figure 3-4: Bi-layer lift-off process starting

For the subtractive approach, shown in figure 3-5, the layers are deposited blanket, no pattern, onto the substrate and a hard mask material (aluminum or chrome) is the blanket deposited on top. For cases where a hard (metallic) mask cannot be used due to possible shorting a buffer polymer layer can be spun before the mask material. A photoresist is then spun on top, patterned, developed and hard baked to ensure robustness for the hard mask wet etch. After the hard mask is etched with the desired pattern the sample goes through a directional dry etch process in the inductively coupled plasma (ICP) RIE. Developing the recipe with the right chemistry to etch an alternating metal-dielectric stack can be challenging and while it was

possible, the finalized samples had higher electrical losses due to the stack shorting to the device electrodes.

For reduced edge roughness, which causes leakage from one port to the other and reduces the quality factor, the inverted pyramid was the method selected for most of the samples.

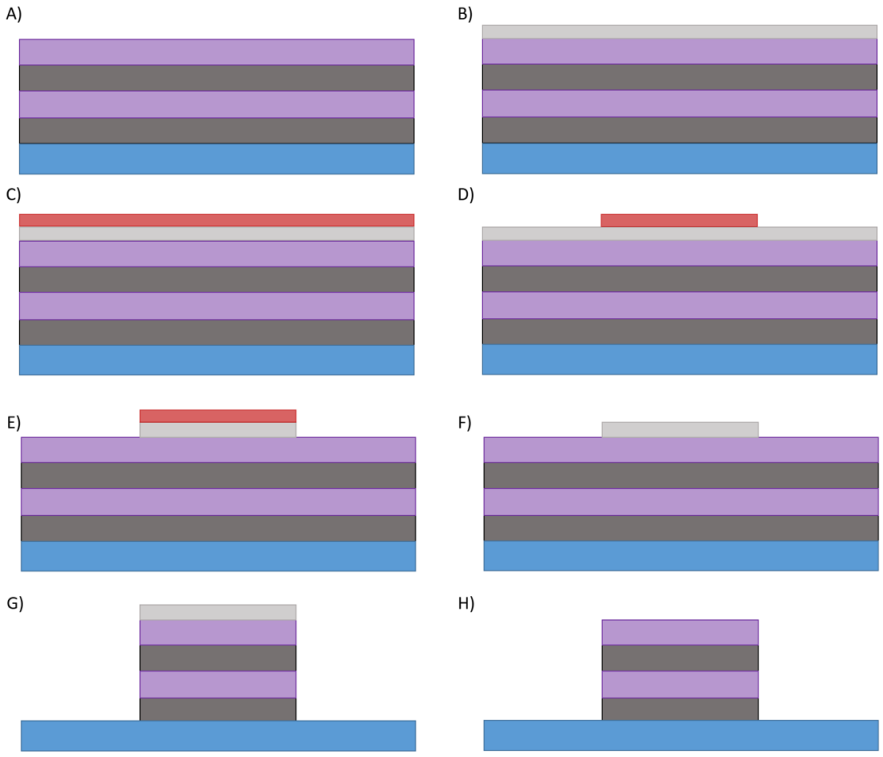

Figure 3-5: Dry etch, subtractive process

Shown in figure 3-5 is the subtractive process starting with a) blanket bragg reflector mirror stack a b) a metal hard mask (i.e. 100 nm Al or Cr) is deposited, and c) photoresist is spun and baked. Then the d) photoresist is patterned and developed, e) the hard mask is wet etched and the f) photoresist is removed. Finally, g) a dry etch is used to anistropically (directional) etch the stack and h) the hard mask is removed by wet etch. All three techniques were applied, and the results will be shown further ahead.

3.2.2 Deposition methods

Layers with thicknesses of over 100nm are considered thick and require long deposition times for most physical vapor deposition methods (PVD) or very high temperatures for chemical vapor deposition (CVD) systems. An example of this technique is the bragg reflector and piezo layers. The main goal of this project requires these devices to be integrated on a CMOS substrate, then the thermal budget needs to be below 300°C. The deposition process also has to be compatible for both metal and dielectrics. For these reasons, the preferred method for low temperature, high rate and dielectric compatible deposition is RF magnetic sputtering. The bragg reflector and piezoelectric layers have thicknesses of 650nm for Tungsten (W), 680nm for Silicon Dioxide (SiO_2) and 1.3um for Zinc Oxide (ZnO), all of these were sputtered. Out of these materials, W and ZnO have specific properties that need to be addressed for mechanical stability and electrical integrity.

Tungsten is a dense, brittle metal that when deposited as a thin film can have one or both crystalline phases known as α, a BCC stable structure, and a meta-stable β cubic structure. As the film grows in thickness the stress accumulates, depending on the deposition conditions (i.e. power, temp, pressure). That means that the film will be either tensile or compressive. If the film is deposited in the meta-stable stress domain (compressive), it will slowly transition into the α phase once it is exposed to ambient pressure and temperature. This transition will cause the film to crack or peel off. To address this issue multiple samples were studied for different pressures and temperatures and a few combinations were optimal depending on the chamber and sputter gun size.

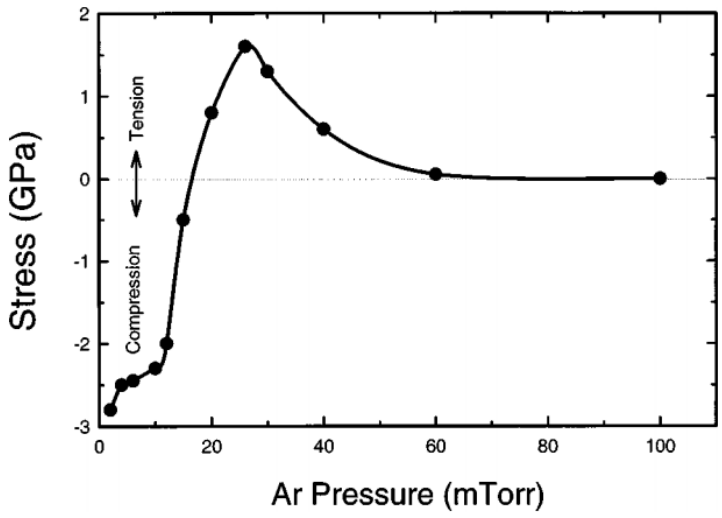

Figure 3-6: Stress for a sputtered tungsten thin film for a fixed volume and varying chamber pressures[47]

3.2.3 Piezoelectric layer

The next layer with deposition issues to investigate was the piezoelectric layer, ZnO. A high-quality piezo layer needs to be crystalline, this usually means high temperature and pressure depositions. As mentioned above the thermal budget is limited to 300°C and a high pressure would greatly slow the deposition rate. The temperature and pressure could be kept relatively low (150°C and 2mTorr) by using a seed layer that promoted c-axis growth. Another thing to mention is all the previous layers were deposited with argon (Ar) gas as the sputtering medium but for ZnO, reactive sputtering (Ar + O_2) was needed to meet stoichiometry. The films deposited without O_2 or low ratios of O_2/Ar were mostly metallic (Zinc), this translated to conductive high loss devices. Figures 3-7, 3-8 and 3-9 are some XRD images of ZnO for different deposition conditions. In figure 3-7 a comparison of ZnO growth on glass and tungsten

at no temperature and at 150°C is presented. Crystallinity improvement is observed as heat is added.

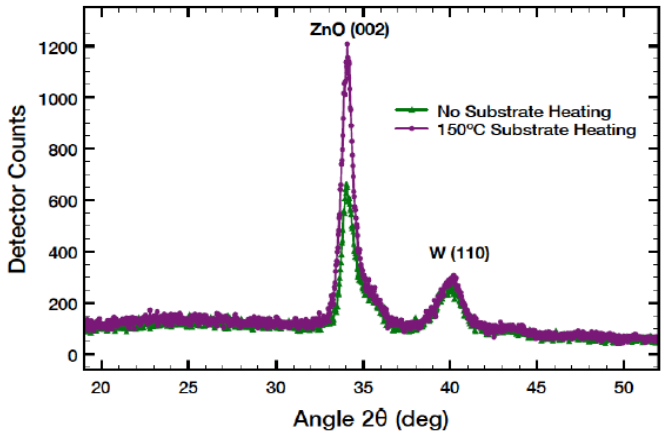

Figure 3-7: XRD for ZnO growth on glass and tungsten at no temperature and 150°C

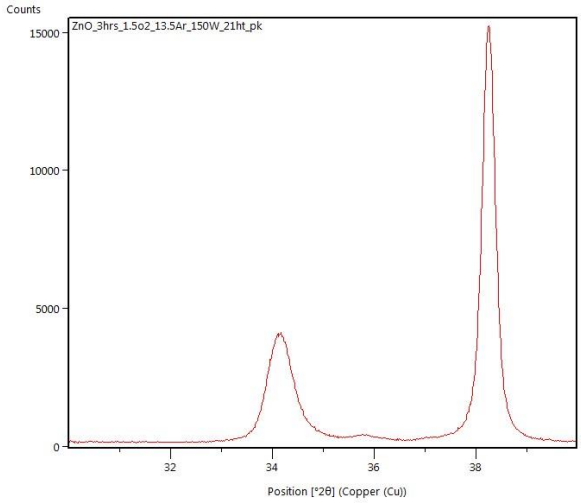

Figure 3-8: XRD image low oxygen content where the right peak is amorphous ZnO

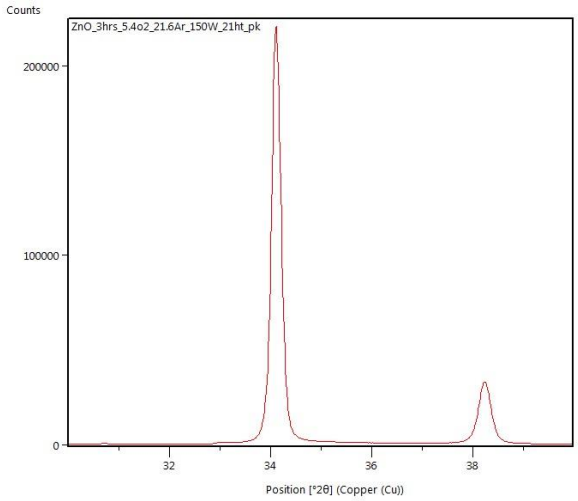

Figure 3-9: XRD images double the oxygen content showing a large peak for crystalline growth

In figures 3-8 and 3-9, are the XRD results for ZnO films of different oxygen contents. The first one has a 10:1 ratio of Ar to O_2 and the second one is 20:1. Adding oxygen improves the crystallinity of the films as shown by the dominating peak in figure 3-9 at angle 34°.

The top and bottom electrodes were made up of 2-5nm of chrome (Cr) and 75-100nm of gold (Au), or alternatively 100nm of aluminum (Al) and 10nm of platinum (Pt), both of which seed c-axis ZnO. These were deposited using PVD techniques such as evaporation or e-beam.

3.2.4 Stress Compensation for Membranes

Zinc Oxide was originally used as the membrane material but due to its compressive stress the films would buckle and either break or cause high quality factor losses [48]. Using surface micromachining a-Si was deposited by RF sputtering or plasma enhanced chemical vapor deposition (PECVD) to be the sacrificial layer. To compensate for the piezo's compressive stress a blanket layer of Si_3N_4 was deposited. The membrane stress was accurately tuned by

playing with the high and low frequency deposition times as well as the chamber pressure. Figure 3-10 shows how the samples of membranes were observed.

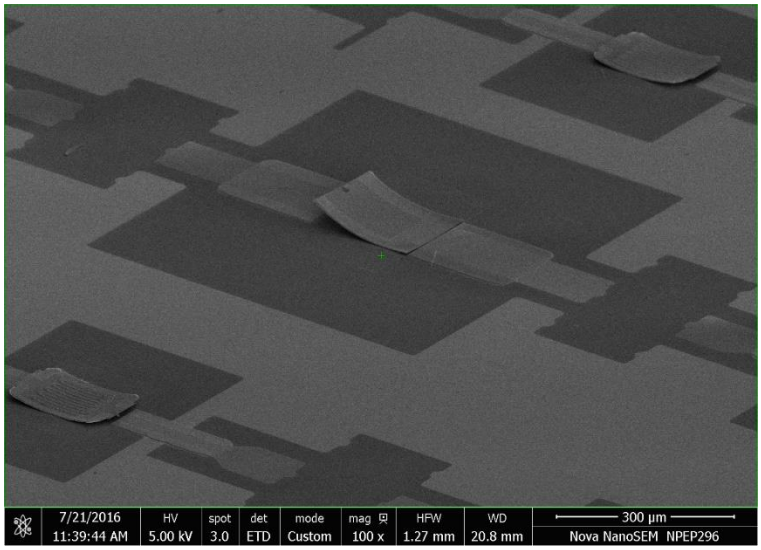

Figure 3-10: Membrane samples without nitride

Xenon difluoride (XeF_2) was used to selectively dry etch the sacrificial layer. Initially the devices were fabricated on blanket a-Si on glass. Etching into the bulk with an isotropic process took several cycles and long wait times (+12 hours) to release the membranes. To reduce etch times the a-Si was patterned into islands on glass.

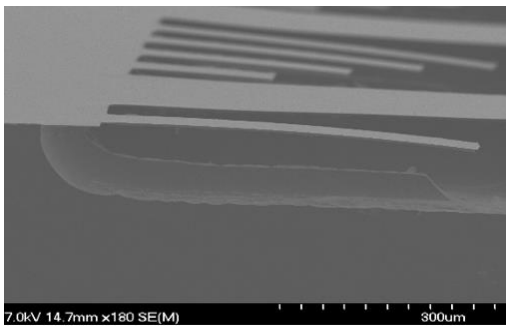

Figure 3-11: SEM images of released single anchor fingers

As seen in figure 3-11 the SEM images of released single anchor fingers to study stress compensation. From left to right: the stress for an uncompensated ZnO can be seen with the film bucking out of the substrated and next to it a tensile, almost neutral stress, using a combination of nitride and piezo.

3.3 Electrical Model Extraction

The devices fabricated on glass were used to measure the output characteristic S-Parameters and build an electrical model. S-parameters are a measurement of reflected and transmitted power in one or between multiple ports. To obtain these parameters a vector network analyzer (VNA) was used, the tool will sweep through frequency a 0dBm signal and measure power levels at the different ports. Because the device has two ports there were four measurements available: S_{11}, S_{12}, S_{21} and S_{22}. Where S_{ii} and S_{jj} define reflected power and S_{ij} and S_{ji} are transmitted power. S-parameters can then be converted to impedance, or Z-parameters, for accurate modeling. Figure 3-12 shows the impedance vs frequency extracted from the s-parameters for an SMR.

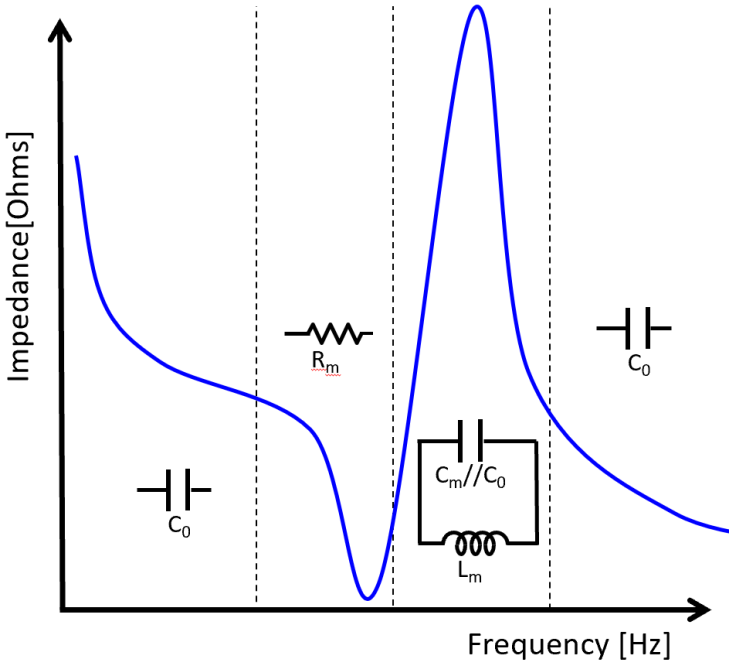

Figure 3-12: Impedance response of a piezoelectric resonator

The plot is divided in four segments, two of them being drawn as capacitors, C_o. Out of band, frequencies far from the resonance frequency, the device acts as a capacitor this is given to the physical structure, a dielectric (piezo) sandwiched between two metal parallel plates. C_o is also known as the static capacitor. As we move through frequency and reach the resonance frequency of the device the motional branch, modelled as a series RLC circuit, comes into play. The motional branch is not physically there, and it is merely a way of quantifying the oscillation frequency and quality factor. At resonance frequency the motional branch's inductor and capacitor will trade energy and act as a short, the only thing left is the motional resistance R_m. Moving again in frequency, the device moves out of resonance and the motional branch interacts with the static branch (C_o). This causes another resonance peak known as the anti-resonance where the motional inductor and capacitor trade energy with C_o and act as an open circuit.

Finally, the device goes back to having a static capacitance behavior after it has left the anti-resonance. Table 3-1 shows the extracted parameters for different glass sample generations.

	Gen 1	*Gen 2*	*Gen 3*	*Gen 4*	*Gen 5*
Q	~350	~400	~500	~500	~500
Kt2	1%	3.1%	3.5%	4.5%	4.5%
Rm (Ohms)	40	15	5	5	5.3
Rs (Ohms)	5	6	4	0.3	0.5
Csubstrate (fF)	3000	700	10	10	10
Process	Patterned mirror islands	Improved growth conditions	Insulating substrate	Pyramid mirror and thick contacts	Etched mirror

Table 3-1: Extracted parameters from samples on glass

3.3.1 Butterworth Van Dyke model

The measured s-parameters can be used to model the fabricated devices by fitting curve adjusting the electrical components equivalent. The curves were extracted from the VNA and imported into advanced design system (ADS) for extracting the circuit model equivalent. Figure 3-13 shows the direct correlation of the electrical equivalent with the physical structure. $C_o$is the static capacitance given by the physical structure, C_m, L_m, R_m are the capacitor, inductor and resistor from the motional branch, respectively and C is shunt capacitance to the substrate.

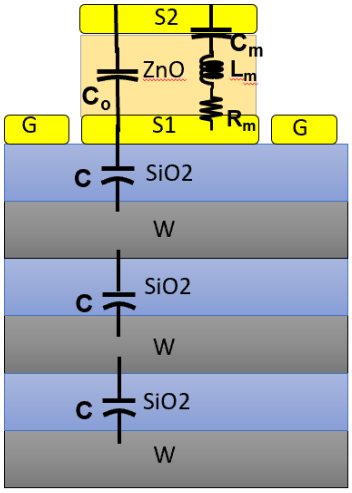

Figure 3-13: SMR structure and its equivalent BVD model

Devices with a 100µm active area were modeled and the extracted parameters were used for designing the CMOS chips to be used as substrates. Using those parameters, we could also predict the parameters for devices with different sizes of active area by developing some scaling relationships,

$$C_o = \frac{\varepsilon A}{d}$$

$$C_m \alpha\, C_o$$

$$L_m \alpha \frac{1}{A}$$

$$R_m \alpha \frac{1}{A}$$

where ε is the permittivity constant, A is the active area of the device and d is the piezoelectric thickness [49].

3.4 Monolithic Integration

A CMOS integrated circuit (IC) was designed to be used as the substrate to these devices with added functionalities that require a radio frequency resonator for operation. The process was modified to be CMOS compatible and ensure a high-quality device after post-fabrication. Three chips were designed for this work, one on 180nm IBM and the other two on TSCM 65nm technology.

3.4.1 Handling and abutting die

To deposit the devices on chip, the first challenge becomes die handling and patterning multiple times on a small (< 2mm x 2mm) area. By adhering the chips to a carrier wafer, Si or SiO_2, moving the samples throughout the processes and tools. A negative photoresist known as Su8 was used as the adhesion agent. The Su8 was either spun on the carrier wafer or dropped and spread with a small sponge. It is a resist used for optical or microfluidic applications due to its high contrast and transparency, but for this application it was selected for its robustness after being crosslinked by long bake times (i.e. 150°C overnight). Its known for being a permanent photoresist making it near impossible to remove after it has been exposed to UV light or baked [50].

As mentioned before, the surface area of the chip is relatively small which makes spinning resists required for the patterning process complicated due to the high surface tension. This surface tension will cause the resists to bead on the chip, this will both reduce patterning resolution and induce cracking during resist bake times. To overcome this an abutting die of similar thickness was placed by the chip and the sample was spun off center. Allowing the polymers to see a

larger effective surface area is extended and any beading would occur at the far end of this abutting chip.

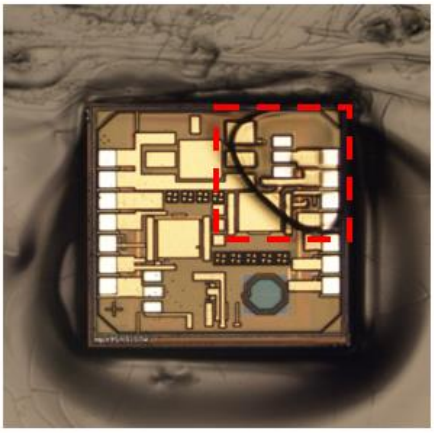

Figure 3-14: Single die resist beading

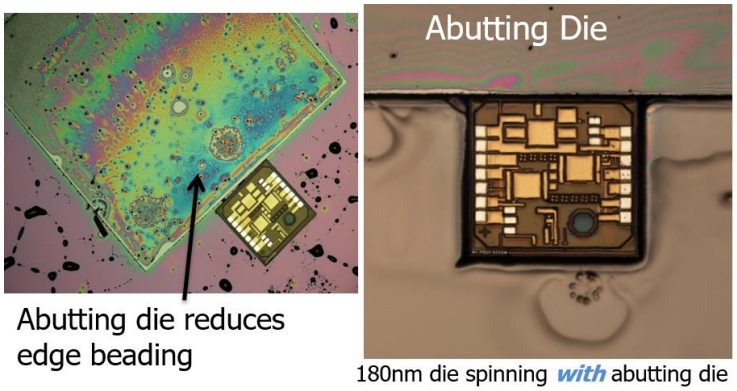

Figure 3-15: IC chip with abutting die to eliminate resist beading

These samples required ramped bakes to prevent bubbling due to the small features and difference in heights within the surface that cause thermal gradients. A normal bake time for lift off resist (LOR) would be 5 minutes at 170°C for these the bake starts at 116°C for 2 minutes, 140°C for 2 minutes and finally 170°C for 9 minutes to account for the large stack from the carrier wafer and die.

3.4.2 Pad Protection

Chips were designed for both, on chip probing and wire bonding. The pads in CMOS technology were made up of Al for that reason. To ensure mechanical stability and integrity the chips must be protected from the several plasmas and wet etch processes. Plasma processes will not only damage the pads, but it might cause an electrostatic discharge (ESD) event, that even with the ESD on chip protection might cause a burn-out and kill the chip. Patterning processes that require developing in AZ 300 MIF that include potassium hydroxide will also etch aluminum. For these reasons, the pads must have a protective layer on top. A few alternatives were used: foundry polyimide, photoresists (polymers) and PECVD oxy-nitride combination, which are explained next.

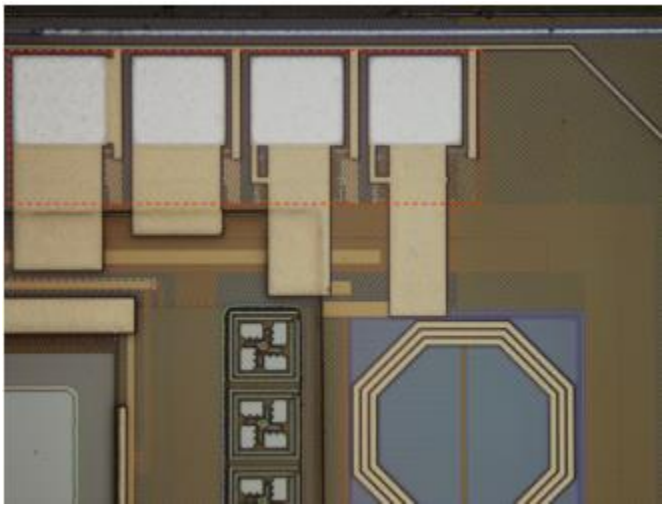

Figure 3-16: Pads on 180nm IBM IC as received from foundry

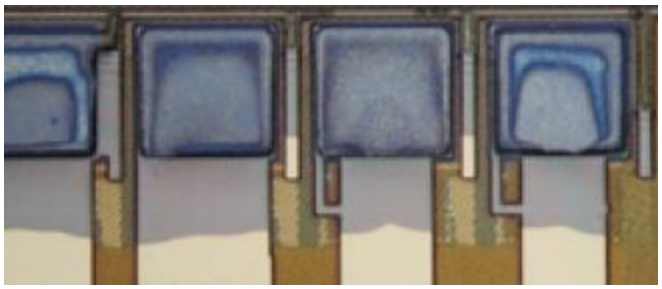

Figure 3-17: Pads exposed to TMAH

3.4.3 Polyimide

For one of the 65nm TSMC chips the passivation was left on the pads by asking to remove any glass cuts over them. The passivation layer used by the foundry is a polyimide that is spun on and patterned. It is used as an encapsulating protective layer against static discharge and humidity. The 65nm technology, unlike 180nm technology, uses a hybrid metallization process of both copper and aluminum. Copper is used on the newer nodes (after 180nm) due to its reduced electromigration effects. Aluminum (Al) is still used for the exposed bond pads for wire bonding purposes. During this work it became apparent that when the glass cut is removed from the pads the foundry does not add the Al layer making wire bonding more difficult unless another metal, i.e. Au or Al, is deposited in the post-fabrication steps. Although leaving the CMOS polyimide on the pads when doing the layout design does facilitate fabrication of the devices and removes a protective layer deposition step it complicates the process if the chip requires wire bonding for testing. Once the device fabrication process is done the polyimide over the pads is dry etched in the ICP RIE with a 24sccm O_2 and 6sccm SF6 gas flow. A patterned metal hard mask is needed for this step, to prevent shorting or damaging the finalized device a thin layer (<600nm) of LOR is spun before depositing Al. Finally, a positive

photoresist is spun, patterned and the sample is wet etched for Al, now ready for the polyimide dry etch.

3.4.4 Su8

Both the 180nm and the new 65nm were designed with glass cuts on the bond pads. The first step in the fabrication process becomes protecting the pads. The first approach was to use the same adhesion or epoxy layer used to attach it to a carrier wafer Su8 negative resist. The resist was spun at 3000rpm with an acceleration of 300rpm/s then baked for 2 minutes at 65°C and 5 minutes at 95°C. The resist was then patterned, and two different patterns were attempted: blanket exposing the chips where Su8 is everywhere and patterning a ring only on the pads. The exposure parameters used were 120mJ/cm^2, which for the MA6 mask aligner results in a 15.5s exposure time. After multiple wet processes the resist started to swell and peel off, exposing the pads that then were slowly etched and could not be used to wire bond to.

3.4.5 Oxy-Nitride

The next protective layer needed to not only be conformal but also robust against wet processes such as developing in tetra-methyl-ammonium-hydroxide (TMAH) for patterning and at the same time be easily removed by dry etching without damaging the pads. PECVD is used for depositing high quality, thick and conformal films. A combo film was deposited consisting of ~200nm of SiO_2 for improved adhesion and ~1um of Si_3N_4 at 300°C [51]–[53]. This film was tested by depositing on a chip and then putting the chip in different etchants, after hours the chips pads were intact. To etch this film the ICP RIE was employed with 30sccm O_2 and 30sccm SF6 flow and a pressure of 60mTorr. The etch is done by cycles of 30s etch time and 30s of cooling, i.e. no RF or ICP power just gas flow, to not damage the surface and integrity of hard mask.

3.4.6 Surface roughness reduction

Surface roughness causes scattering of particles that reduce the energy storage capabilities of the intrinsic device, this results in a lower quality factor (Q) as shown in the following equation:

$$\frac{1}{Q} \approx \left[(1 - exp(-4\pi\beta^2\sigma^2)]\frac{L}{\sigma\sqrt{16\pi^3}}\right]$$

where L is the extent of the surface and σ is the surface roughness[54]. A roughness reduction plan was developed starting from the layout design of the chips, where these devices were fabricated directly on CMOS. The CMOS processes from foundries are made up of multiple metal layers with dielectric spacers in between all of which are planarized except for the top (highest layer) metal layer with resulting roughness of <5 nm. The process used for this roughness reduction is known as chemical mechanical polishing (CMP)[55]. Within the stack of metal layers and spacers the foundry adds supporting structures known as metal fill to guarantee mechanical stability and robustness of the structure, a direct analogy would be support beams in a house. The thickness or height will depend on the metal layer, i.e. for the top layer this will be > 1μm, then topped off with polyimide. To avoid this added roughness a floating metal bed was designed in the IC layout. When the chip arrives from the foundry, the polyimide over the metal bed is dry etched and then the metal is wet etched, resulting in a smooth inter-layer dielectric surface where the sample can be fabricated on. Before metal etch a diffusion, barrier layer is dry etched using Cl_2/Ar ICP RIE chemistry. The CMOS technology nodes using copper metallization require this diffusion barrier to prevent copper from diffusing into the interlayer dielectrics and shorting the stack, some common materials used for this are TaN and TiN [56].

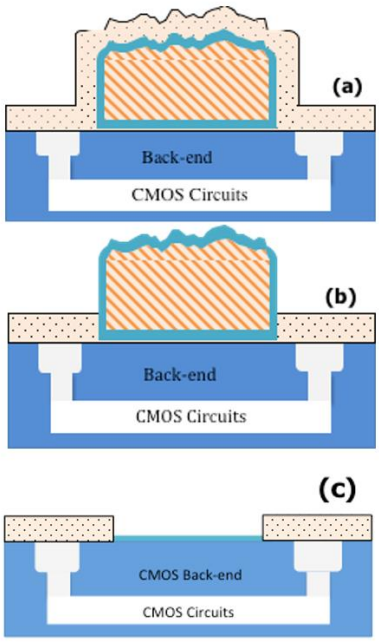

Figure 3-18: Bed etch for reduced roughness

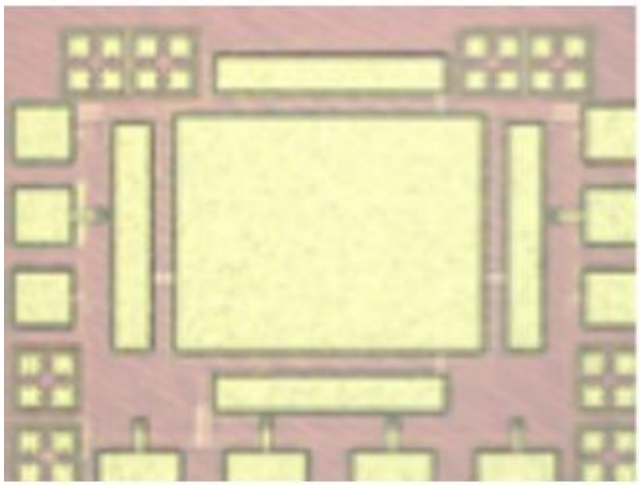

Figure 3-19: SMR bed on TSMC 65nm as received from foundry

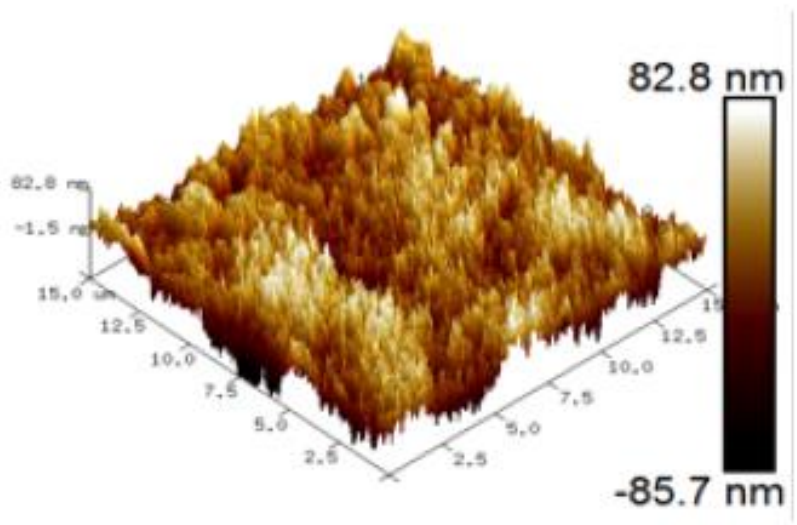

Figure 3-20: AFM of 65nm TSMC bed as received from foundry

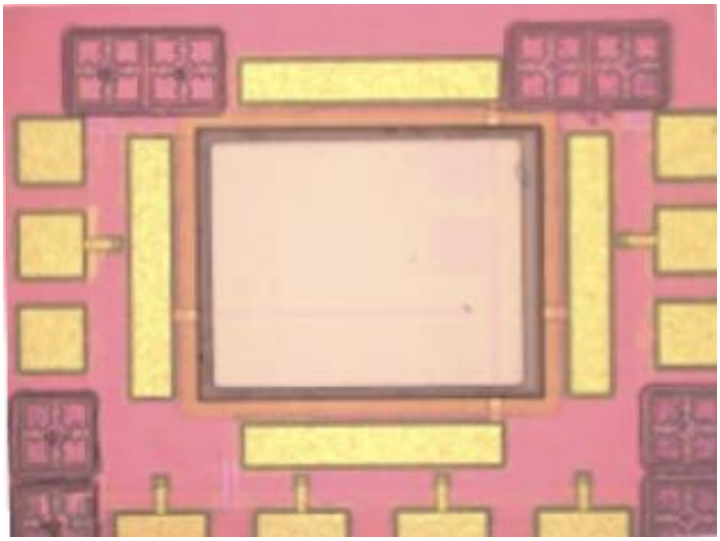

Figure 3-21: SMR bed after polyimide and metal etch

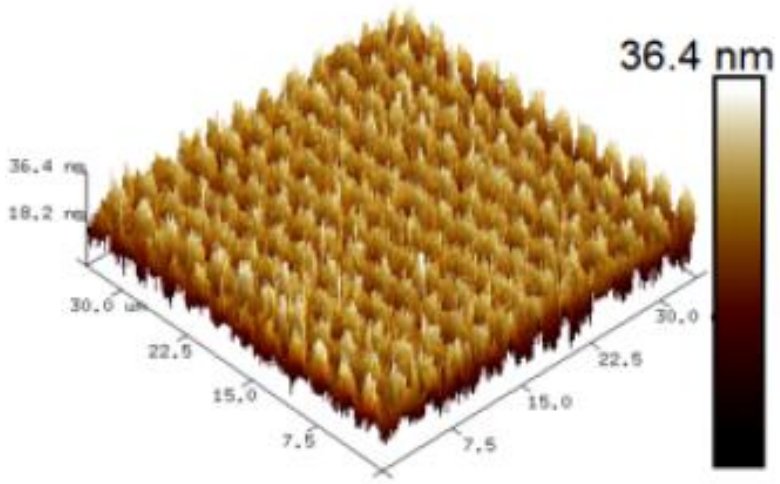

Figure 3-22: AFM of SMR bed after polyimide and metal etch

3.4.7 Process flow for monolithic integration

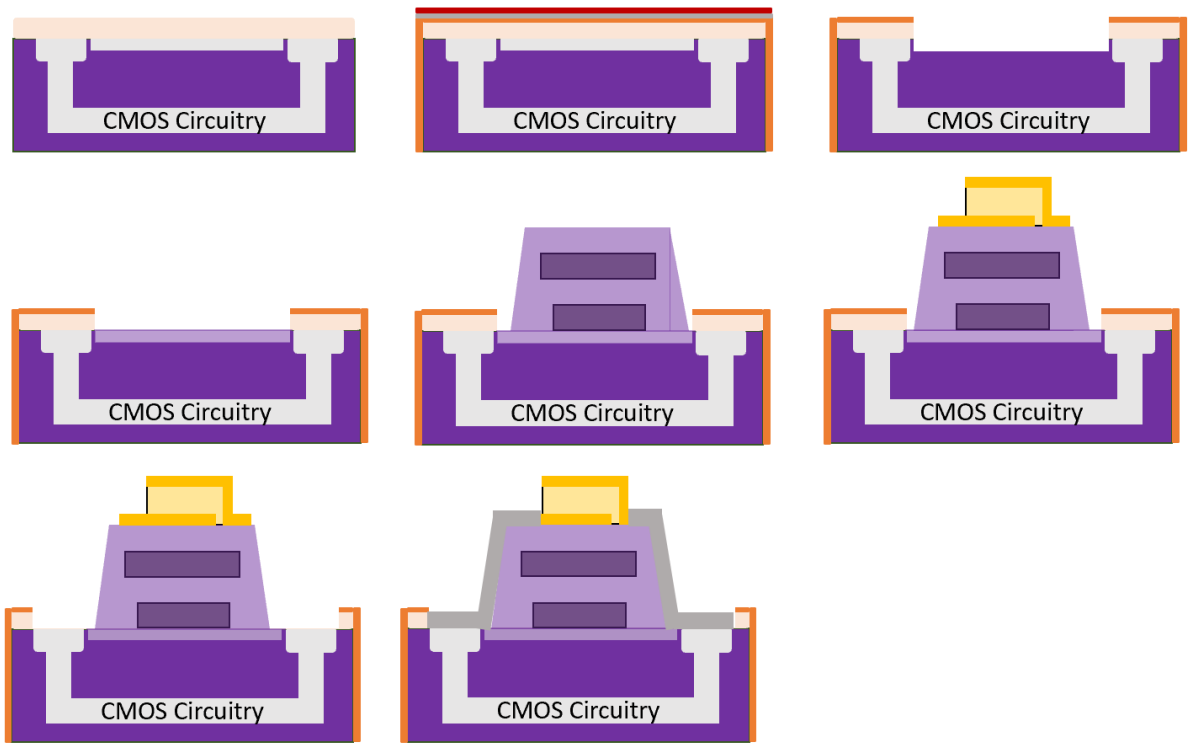

Figure 3-23: SMR monolithic integration process flow

With all the techniques developed the process flow was established as shown in figure 3-23. From left to right starting with the die as received from the foundry. A nitride protective layer is deposited by PECVD and a hard mask of Al (100nm) is deposited on top and spun with photoresist. The photoresist is patterned for bed etch and the Al wet etched, the sample is then placed in the Fl ICP RIE for a Fl_2/O_2 polyimide etch and then the metal bed is wet etched. A buffer layer of SiO_2 is deposited to reduce surface roughness and avoid sharp edges that might cause shorting. The bragg reflector mirror stack is then patterned and deposited by RF sputtering and the metal-piezo-metal sandwich is patterned and deposited by e-beam and RF sputtering. Finally, the FBAR/SMR pads for connectivity with the underlying circuitry are exposed by the same methods used for the bed etch and a thick metal (Al 1um) is patterned and deposited to connect the device to the circuitry and reduce series impedance.

Chapter 4 **: Integrated Circuit Design**

Three integrated circuits (ICs) were designed for this work. The following section will go over the techniques and design process of the different integrated circuits and their components.

4.1 Fundamental idea

High quality crystal resonators can be used as building blocks for different communication and sensing applications. The most known are filters, i.e. duplexers, and oscillators for signal reference due to their high stability. For this project, using oscillators facilitated taking real time measurements and allowed us a direct extraction of the phase noise and hence the quality factor.

Resonators are passive devices that oscillate at a specific frequency, known as the resonance or natural frequency, but due to internal losses the oscillation decays with time.

At the resonance frequency the impedance of resonators changes as well. The resonator is modeled as an inductor (L) and capacitor (C) circuit known as LC tank, with a resistor in series that represents the loss in the circuit. An oscillator can be made using a resonator, a frequency selective tank circuit, as the core and adding feedback circuitry to cancel out the losses [57]. The frequency is defined by the resonator or tank and can be calculated as

$$f = \frac{1}{2\pi\sqrt{LC}} \ .$$

The feedback circuitry is an amplifier that has enough gain to cancel out the losses in the resonator to maintain a constant oscillation. This approach to designing an oscillator is known as negative resistance, were the amplifier is modeled as a negative resistor. For oscillation $R_n \geq R_m$ for circuits in series, $R_m \geq R_n$ when in parallel circuits must be met, where R_n is the equivalent negative resistance and R_m is the resonator loss.

4.2 IBM 180nm

The first chip designed using MOSIS, a multi-project wafer (MPW) provider, and IBM's 180nm technology. It has a total of four independent circuits: two pierce oscillators, one voltage-controlled LC oscillator and a ring oscillator. The LC oscillator was designed to meet the requirements of ELEN 6350, which were to design an IC, tape out and test the circuit. The two pierce oscillators required a crystal, i.e. SMR, for operation and the ring oscillator is a test circuit to study the fabrication effects on the technology.

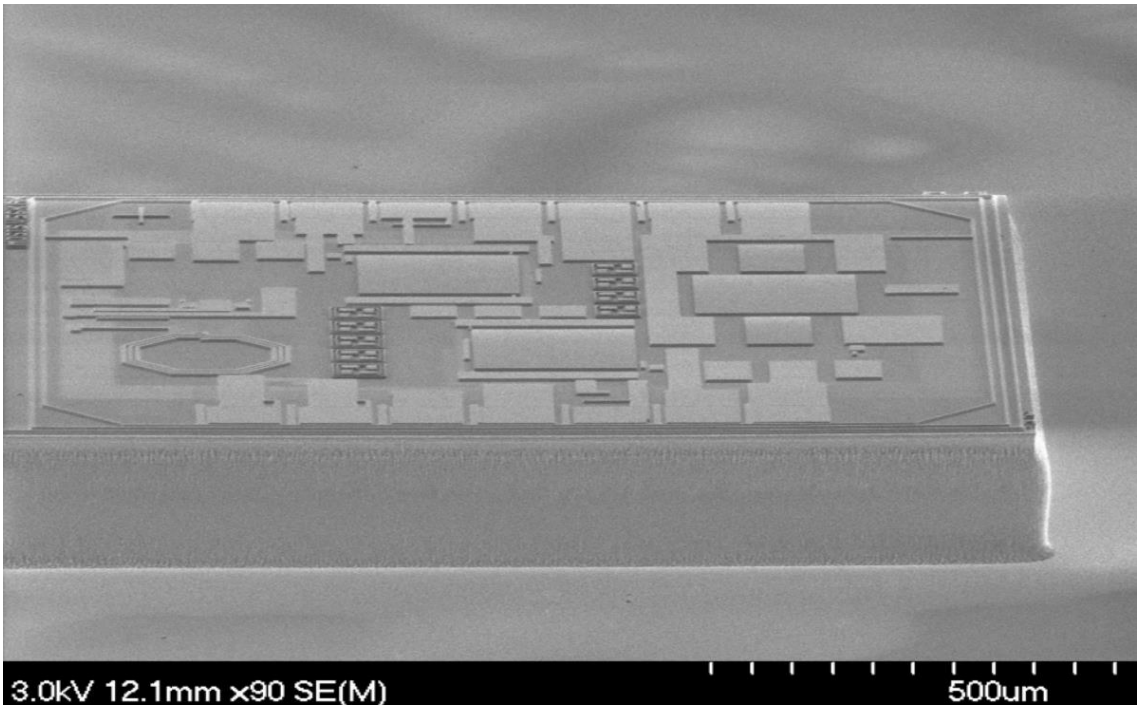

Figure 4-1: Scanning Electron Microscopy image of the 180nm IC

4.2.1 Pierce Oscillator

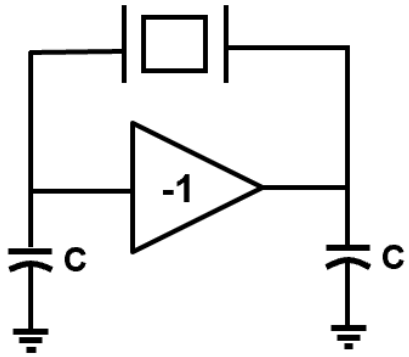

Figure 4-2: Crystal oscillator Pierce topology

The pierce topology was selected for the piezoelectric circuit as it is a well-known and widely used, i.e. digital clocks, structure for crystal oscillators [58]. The most standard structure consists of a digital inverter with a biasing resistor across it and two shunt capacitances at the input and output of the block. The resistor self-biases the inverter; both the input and output dc levels are known, in the linear region, to be used as a high gain inverting amplifier. The shunt capacitors form a *pi* network when combined with the piezoelectric device that offers a 180° phase shift of the signal [59]. For oscillators the signal going through the feedback loop must see a positive or 360° phase shift, the inverting amplifier supplies the remaining 180°, for a total 360° phase shift or positive feedback.

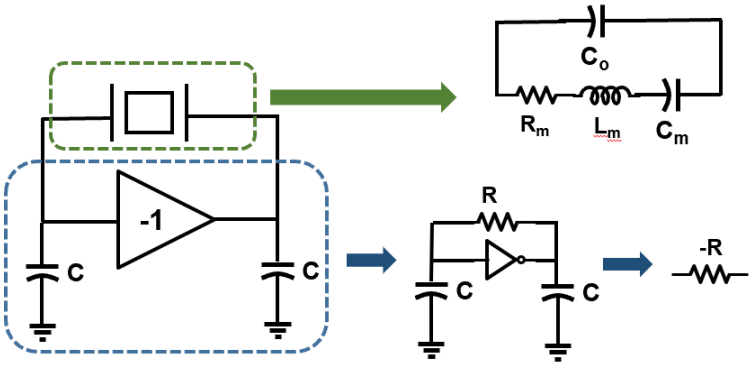

Figure 4-3: Circuit break down

The device electrical model has been shown before as a motional branch with RLC components and a static branch representing the physical capacitance of the structure, C_o. At resonance L_m and C_m will exchange energy amongst themselves and their equivalent reactances X_c and X_L, defined as:

$$X_c = \frac{1}{j\omega C}$$

$$X_L = j\omega L$$

will cancel each other out. That means that in resonance the LC tank acts as a short circuit resulting in R_m as its impedance.

To facilitate the negative resistance analysis, C_o will be lumped with the pi-network after the equivalent resistance is derived. As frequency goes up $C_o$becomes a short and will lower the gain of the amplifier, effectively limiting the negative resistance obtained from the pi-network.

$$Z_n = \frac{V}{I} = \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2} - \frac{g_m}{\omega^2 C_1 C_2}$$

Where g_m is the transconductance or gain of the transistors.

Frequency	C_m	L_m	C_o	R_m
1.8 GHz	33fF	247nH	1pF	6Ω

Table 4-1: Equivalent electrical model values used for the IC designs

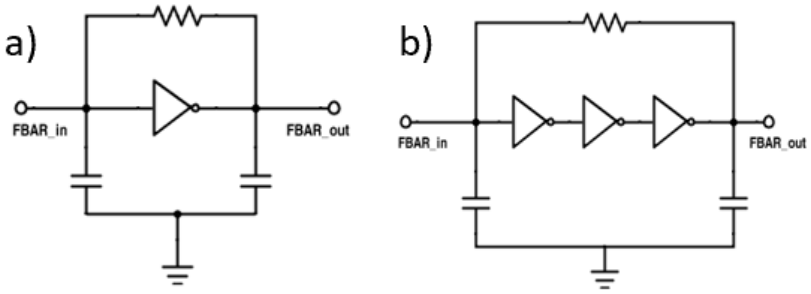

Figure 4-4: Pierce oscillators implemented a) single stage b) 3-stage inverter amplifier

4.2.2 LC Oscillator

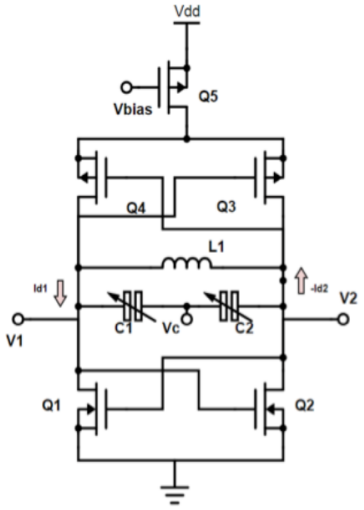

Figure 4-5: Complimentary LC oscillator topology

For the LC oscillator a complimentary topology, PMOS and NMOS, was chosen for a higher gain which is explained in the following segments. The resistive loss comes from the inductors coil resistance. Two variable capacitors are placed in parallel to the inductor for resonance and still maintaining circuit symmetry. The capacitors value can be changed by applying a voltage at node Vc, this allows for a small frequency variance (34%). In this topology the negative resistance is in parallel to the resonance resistance, therefore the condition for the amplifier gain to dominate to obtain oscillation is $R_m \geq R_n$ [60].

The LC tank's losses come from the inductor coil resistance which can be extracted after deciding on the frequency of operation. For this design, f_{osc}, was selected to be ~1.8GHz and the capacitor was designed to be greater than the parasitic capacitances of the transistors, 400fF from simulation. Knowing the capacitor value, the inductor is calculated using the frequency relationship. The coil resistance is obtained by using the quality factor relationship,

$$Q = \frac{\omega L}{R}$$

the value for Q was obtained from the IBM 180nm technology manual.

Frequency	***C***	***L***	***R***
1.8GHz	2pF	4nH	~ 10Ω

Table 4-2: Values calculated for the LC oscillator

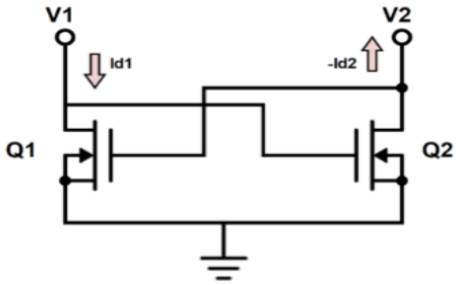

Figure 4-6: Half amplifier circuit for negative resistance derivation

To derive the negative resistance, we note the circuit is symmetric, so we take half of the amplifier circuit and calculate the impedance seen looking into *V1* and *V2*. A test voltage source can be placed at these two terminals and the following assumptions can be made:

$$I = I_{D1} = -I_{D2} \;\; ; \;\; V = V_1 - V_2$$

The current is defined by the transistor, depending on the gate voltage as follows

$$I = g_{m1} V_2 \; ; \;\; \frac{V_2}{I} = \frac{1}{g_{m1}}$$

$$I = -g_{m2} V_1 \; ; \;\; \frac{V_1}{I} = -\frac{1}{g_{m2}}$$

If both transistors are sized equally the following is also true:

$$g_m = g_{m1} = g_{m2}$$

Now applying Ohm's Law to obtain the resulting resistance and admittance:

$$R_{neg} = \frac{V}{I} = \frac{V_1 - V_2}{I} = -\frac{2}{g_m} \; Y_{neg} = -\frac{g_m}{2}$$

Assuming the PMOS (top) transistors are sized for the same gain (g_m) and output resistance (r_o) we can assume they have the same equivalent negative resistance and can simplify the equations as follows:

$$g_m = g_{mn} = g_{mp}$$

$$R_{negT} = -\left(\frac{2}{g_{mp}} || \frac{2}{g_{mn}}\right);\ R_{negT} = -\left(\frac{1}{g_m}\right)$$

This shows the gain or negative resistance is double what it would be if it were not complementary. For this system where the amplifier and the resonance tank are in parallel, using admittance, $Y = \frac{1}{R}$, simplifies the analysis.

$$Y_{neg} = -\left(\frac{g_{mn}}{2} + \frac{g_{mp}}{2}\right);\ Y_{neg} = -\left(\frac{g_m}{1}\right)$$

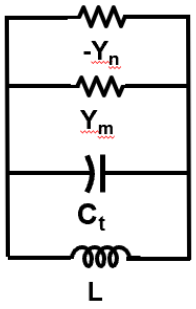

Figure 4-7: Simplified circuit for LC oscillator negative resistance analysis

4.2.3 Ring Oscillator

A ring oscillator circuit was designed as a test circuit placed directly under a stand-alone FBAR bed for the simultaneous testing of the circuit and the device. The main goal for this design is to

measure the oscillator while probing the FBAR to see if there is any electrical leakage. These oscillator circuits are based on an odd number chain of inverters in a ring. This system only requires bias for startup, making it the ideal mechanism for verifying CMOS integrity after fabrication.

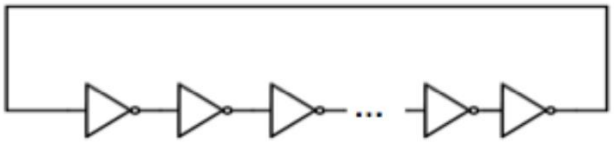

Figure 4-8: Ring oscillator circuit

The frequency of this oscillator will depend on the delay of an inverter and the length of the chain, i.e. number of inverters,

$$f = \frac{1}{2 * n * t}$$

where *n* is the number of inverters and *t* is the delay of each stage. The delay is dependent of the equivalent resistance, r_o, and capacitance, C_g, at each node and is proportional to transistor size.

$$C_g = WLC_{ox}$$

$$r_o \alpha \frac{L}{W}$$

The transistors were sized with minimum lengths and 5μm widths. The simulated delay was ~36ps for a single stage. For a frequency in the range of megahertz (MHz), thirty-seven (n=37) inverters were selected for a resulting 600MHz signal.

4.2.4 Level Shifter

To interface the oscillator with the buffers, the signal is conditioned to have a dc voltage (offset voltage) of $\frac{V_{DD}}{2}$ to avoid conversion errors.

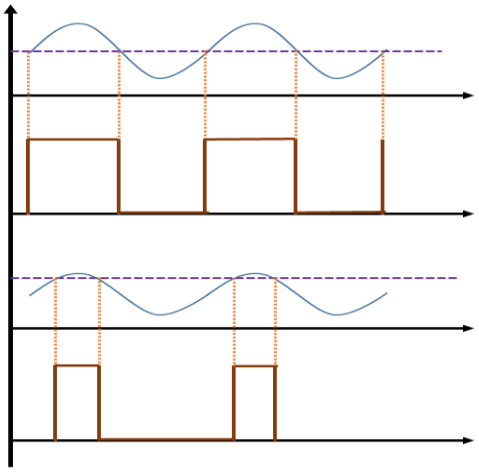

Figure 4-9: Analog to digital duty cycle conversion error from dc offset variation

The circuit is comprised of an AC coupling capacitor to strip the dc level from the signal and followed by a self-biased inverter. The signal is amplified and offset to $\frac{V_{DD}}{2}$ by means of the biasing resistor across the inverter.

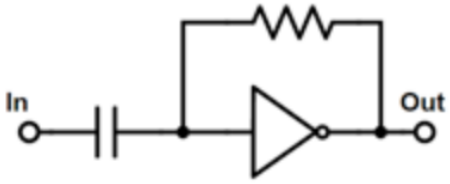

Figure 4-10: Level Shifter

4.2.5 Fifty Ohms RF Buffer

For quick troubleshooting and testing, the oscillators were designed for on-chip RF probing capable of driving GSG 50-ohms terminated probes. For buffering, a chain of inverters with increasing sizes for optimum delay was designed.

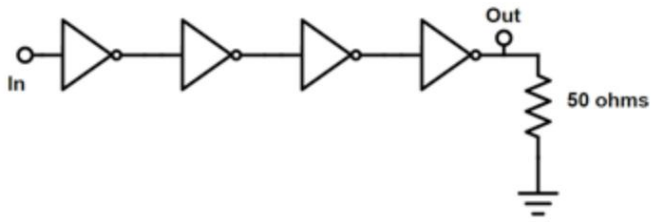

Figure 4-11: 50-ohms buffer chain

The desired output power level was chosen to be between 0-3dBm. The minimum peak to peak voltage was calculated:

$$P = \frac{V_{RMS}^2}{R}$$

Where P is power, R is the load value (50 ohms) and V_{RMS} is the root mean square (RMS) voltage at the output. The peak to peak voltage is then obtained by:

$$V_{pk-pk} = \frac{V_{RMS}}{\sqrt{2}} \quad .$$

To size the transistors in the inverters, we started with the inverter closest to the load and calculated the required r_{on} to have the minimum $V_{pk\text{-}pk}$ at the load.

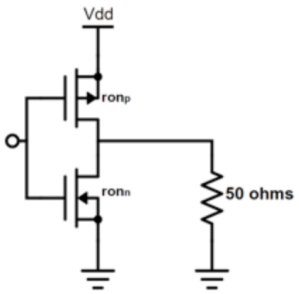

Figure 4-12: Inverter on resistance

$$r_{on} = r_{on_n} = r_{on_p}$$

$$V_{pk-pk} = \frac{V_{DD}}{2}\left(\frac{R}{R + r_{on}}\right)$$

Minimum length was assumed and having r_{on} the transistor width was extracted from simulation. For optimum delay the transistors before this one was sized 2.7 times smaller each stage.

4.2.6 Layout Considerations

The chip served as a study for developing die level compatible processes for future chips. Taking into consideration post-processing which includes patterning steps, alignment marks were designed on the top layer. Large FBAR or SMR pads were placed near the bed with some spacing to prevent shorting. A stand-alone device bed was placed over the ring oscillator to study electrical leakage and model the devices on CMOS.

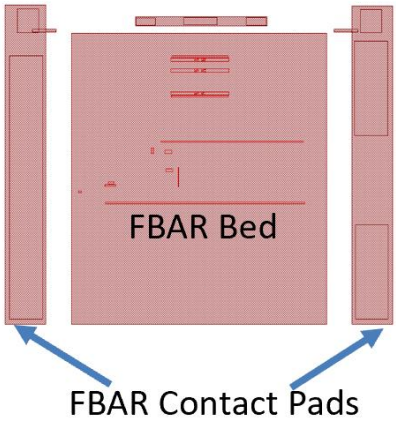

Figure 4-13: 180nm Layout

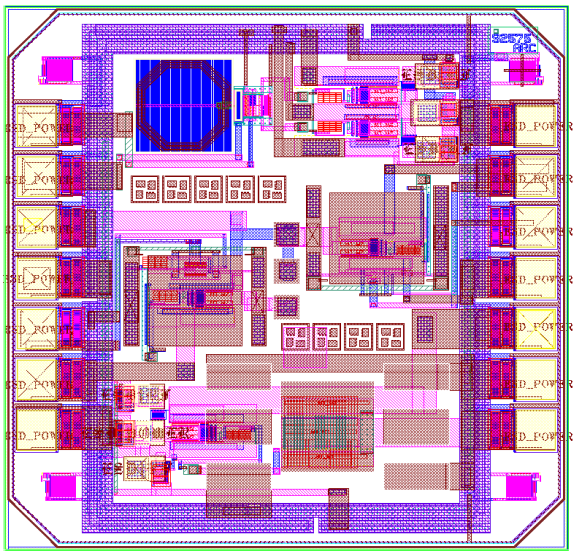

Figure 4-14: 180nm Schematic Layout

Inside the seal ring of the chip RF 100µm pitch GSG and SGS, for the LC oscillator, were placed with glass cuts, i.e. no polyimide protection, for direct probing when received from the foundry. The seal ring ESD ring was split up for different V_{DD} domains, one for each oscillator, to prevent cross-talking. When one oscillator's signal interferes with the other it might cause frequency

locking. The GND ESD ring was left mostly intact except for a small aperture to prevent antenna effects on the chip. The die size is 1.5mm x 1.5mm and has 14 probe pads for on-chip probe biasing.

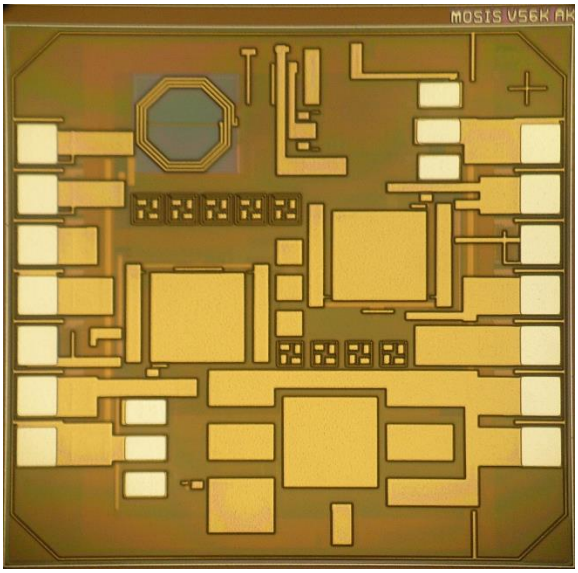

Figure 4-15: 180nm IC as received from foundry (1.5mm x 1.5mm size)

4.3 TSMC 65nm

4.3.1 Current controlled pierce oscillator

In parallel to the 180nm another chip was designed. A smaller design was implemented on a multi project die using TSMC's 65nm technology. Here two single transistor current controlled pierce oscillators were implemented. The gain is controlled directly by the bias current, unlike the 180nm where the design was limited to the technology's max voltage.

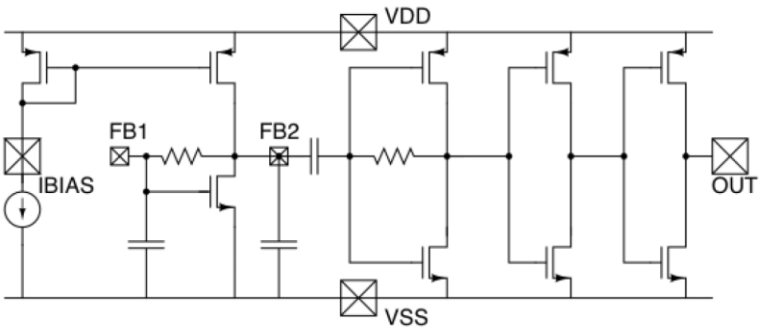

Figure 4-16: Current controlled pierce oscillator

The core transistor was sized for weak inversion, i.e. $\frac{g_m}{I_D} \geq 15$, for high gain and a low power consumption, this in turn increases parasitic capacitance sizes. To compensate for the parasitic capacitances the pierce topology MIM capacitors were designed to be much larger ($C_{pierce} \geq 2 * C_{para}$). The output of the pierce core goes through a level shifter and a 50 ohms buffer for on chip probing.

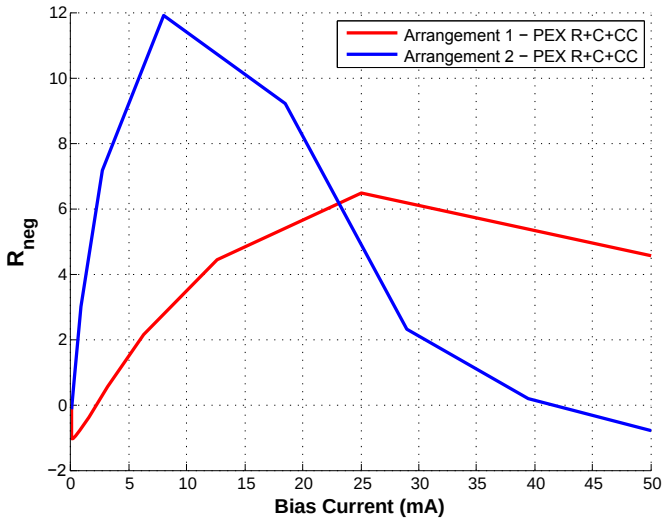

Figure 4-17: Negative resistance variation with current bias for the two pierce circuits on chip

The chip contains two designs for different sizes of SMRs, 100µm x 100µm and 200µm x 200µm, in figure 4-17 the extracted current dependent gain is shown for both. There are four FBAR pads two for each design with GSG output probe pads for each one, as seen in figure 4-18. There are four DC pads for the EYE-pass probe for biasing where the VDD and GND are shared by both and the currents, I_{BIAS1} and I_{BIAS2}, turn on the desired circuit.

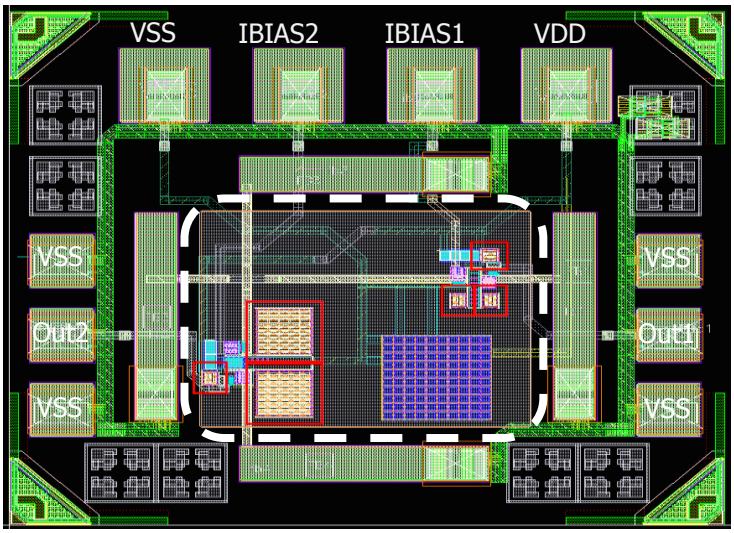

Figure 4-18: System layout on TSMC 65nm

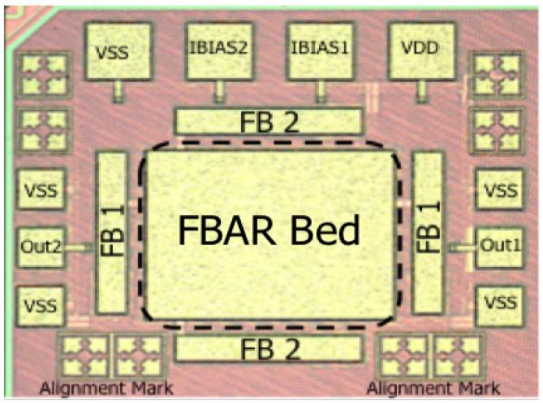

Figure 4-19: CMOS chip as received from foundry

The design of figure 4-19 was part of a bigger chip with multiple projects. The full die size is 1.1mm x 2mm but the active design area is ~1/4 of that, as shown in figure 4-20.

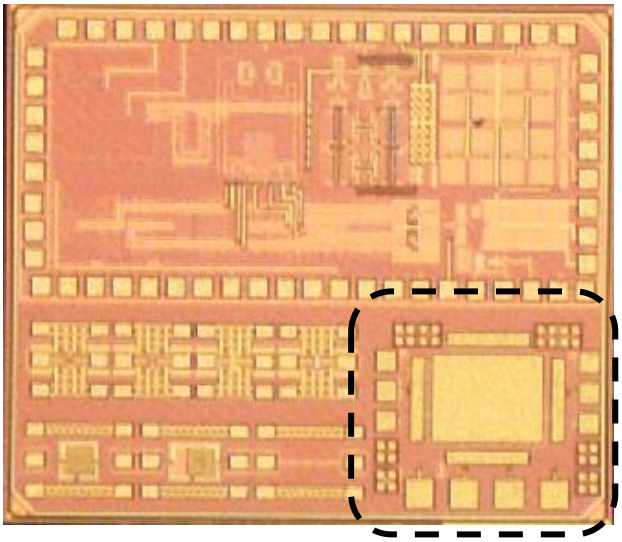

Figure 4-20: TSMC 65nm multi projected die, the box shows the area for the SMR circuits

A big difference between the 180nm design and the 65nm was the protection layer for the probe pads. For the 180nm the pads were left exposed for quick testing once the chips arrived from the foundry. On the other hand, the 65nm pads were left with the polyimide on for plasma and ESD protection. The difference between exposed pads and polyimide covered is shown in figure 4-21. One thing that was noted is the lack of a bonding metal on the polyimide covered pads. Technologies after 180nm, including the 65nm, used copper for metallization instead of aluminum for lower resistivity and reduced electro migration effect [9]. For these technologies to enable wire bonding another metal, such as aluminum, is deposited over the top exposed metal. When the polyimide is left on this bonding metal is not deposited, which in turn makes wire bonding to the pads complicated due to copper.

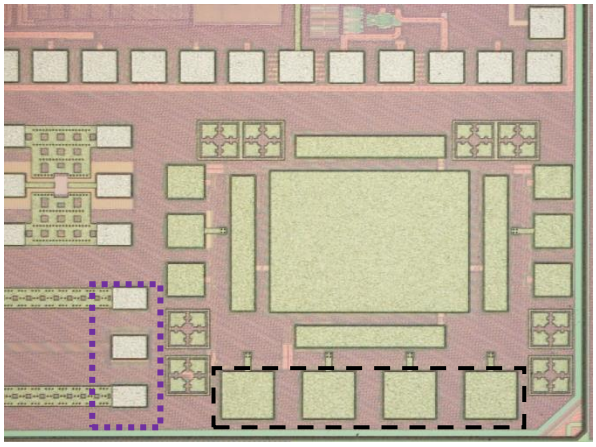

Figure 4-21: Exposed pads vs. polyimide covered pads

4.3.2 Reprogrammable pierce oscillator

A final chip was designed for sensing applications, using the processes developed and circuit design knowledge gained from the previous ICs.

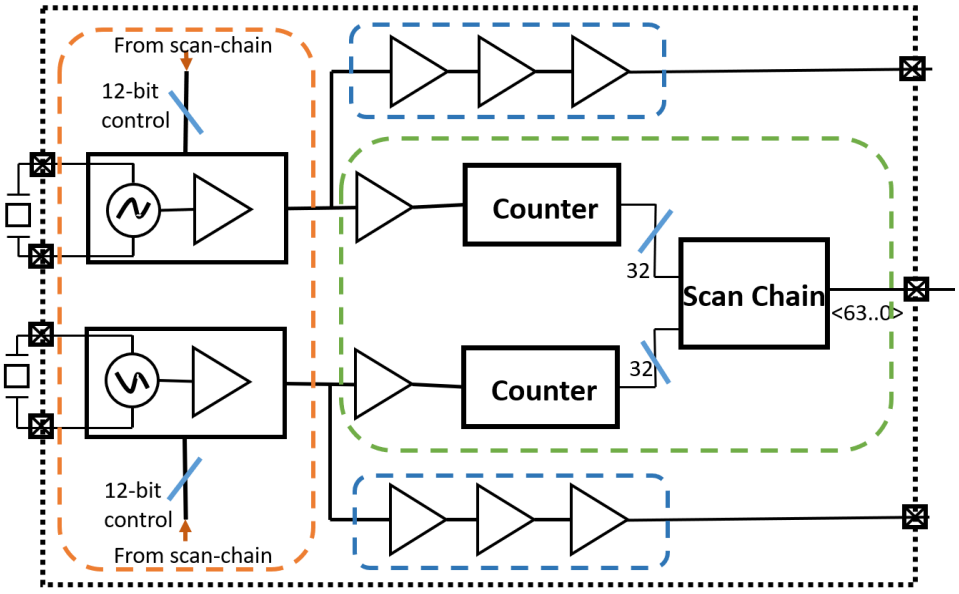

Figure 4-22: System level design for TSMC 65nm sensing chip

As is shown in figure 4-22 the system was divided into three areas: reprogrammable core which is identified with the orange box, RF outputs and digitization identified with blue box and serial read out identified with the green box. The goal of this chip was to enable sensing applications by using two oscillators and counting the frequency difference between them. One of the device sites is the control and the other device is coated in a selector or absorber, this device will have a change in frequency when exposed to IR or a specific volatile organic compound (VOC). The output can both be measured on chip with GSG probes or it is digitized, and the frequency counts extracted serially to be read into an MCU.

4.3.2.1 Reprogrammable core

Using the pierce topology for the core again, the design this time was aimed towards flexibility for both gain and power consumption. The following design was implemented:

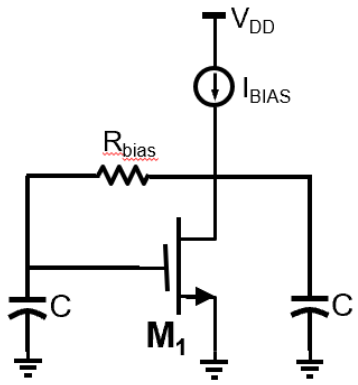

Figure 4-23: Original Pierce topology

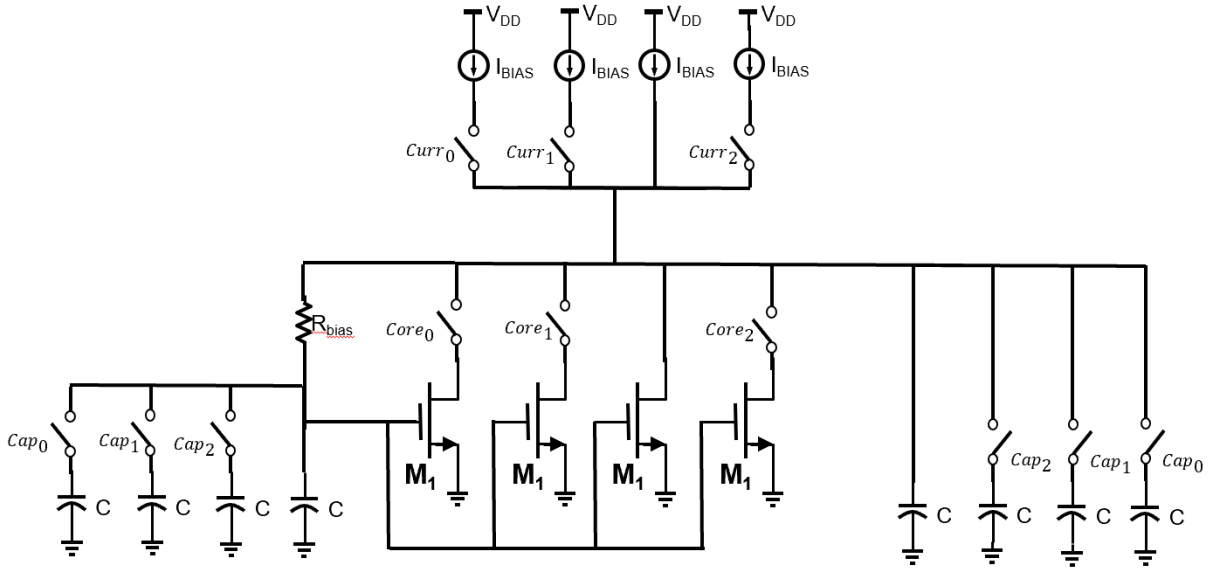

Figure 4-24: Reprogrammable Pierce core

The gain of this oscillator core can be adjusted by reducing capacitance, making the transistor equivalent size larger or increasing current. Once the oscillator starts, the current can be adjusted for lower power consumption while maintaining oscillation. Figure 4.25 shows an extracted simulation of the reprogrammable pierce gain. Maximum gain is when all the transistors and current sources are on and capacitors are off, minimum gain will be the opposite. The control signals for gain and power consumption were set by the scan chain with a serial input from an MCU. The oscillators are on different VDD domains to avoid cross-talk and accurate measure individual power consumption. In figure 4.25 the maximum gain is shown in red and minimum is shown in blue.

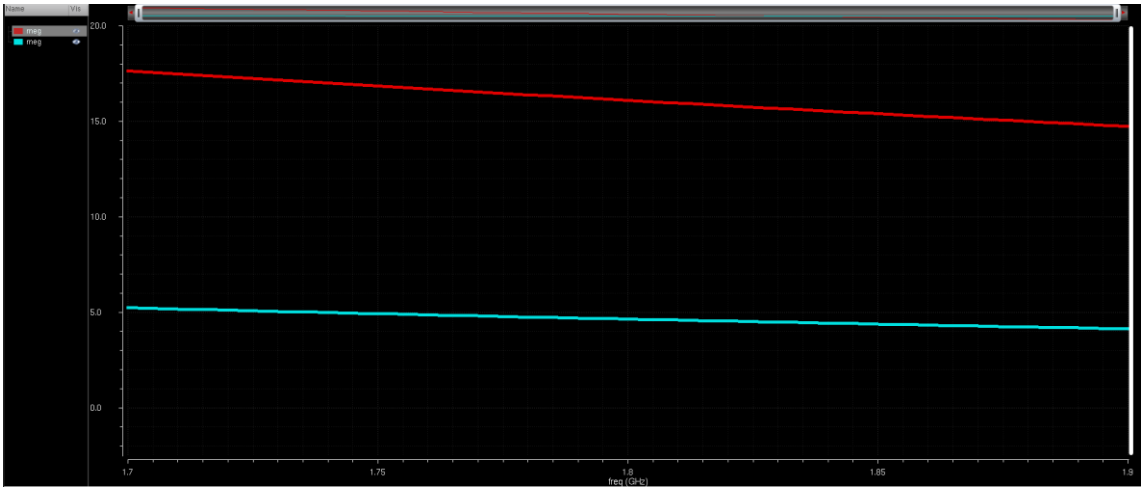

Figure 4-25: Negative resistance vs frequency simulation.

4.3.2.2 Counter and Scan Chain

A high speed 32-bit counter was coded and designed for synthesis. There were two counters in the design one for each oscillator output. The counters will trigger at each rising edge of the oscillator signal, with both an enable and reset function, the frequency of the oscillator can be calculated if the capture window is known. Table 4.3 shows the control bits for the counter.

Control	***State***	***Function***
Enable	0	Stop count/hold value
	1	Count
Reset	0	-
	1	Reset counter value to 0

Table 4-3: 32-bit counter available settings

The capture window is set by the reset period, which is controlled from an external pin. To calculate the frequency, we used:

$$f = \frac{count}{T_{window}} .$$

The counter was designed and tested for frequencies up to 3GHz in extracted simulation.

To reduce I/O pins needed, 64 pins for both counters, a 64-bit scan chain was implemented for serial read out. A simplified block diagram of the scan chain is shown in figure 4-26. A scan chain consists on shift registers, flip flops and control signals that decide the direction of data flow. For reading out of the chip the load control pin is set low (0), parallel input of the scan chain is connected to both counters and the values are stored in the flip flops. To start shifting, or serially reading, the data out the load value is set to high (1).

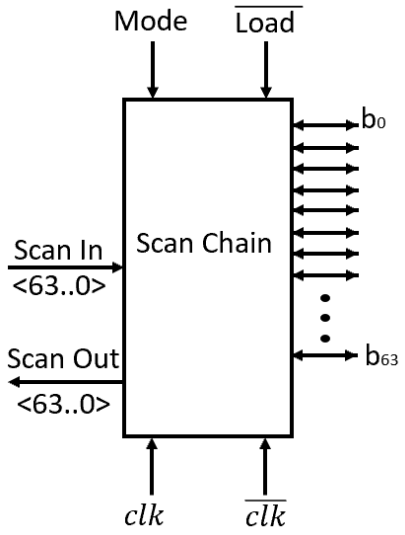

Figure 4-26: Simplified scan chain

The scan chain can also be used for loading and holding values that can be used for controlling the reprogrammable core. Taking a closer look at the scan chain topology it has a control pin called mode that switches the circuit from reading to writing. Table 4-4 shows the control bits for the scan chain.

Control	*State*	*Function*
Mode	0	Scan in/ program IC
	1	Scan out/ read from IC
$\overline{Load}$	0	Load/ store data
	1	Shift out

Table 4-4: Scan chain control functions

Both the counter and the scan chain were synthesized using a design compiler and routed using encounter. Figure 4-27, shown below, is the final implemented layout.

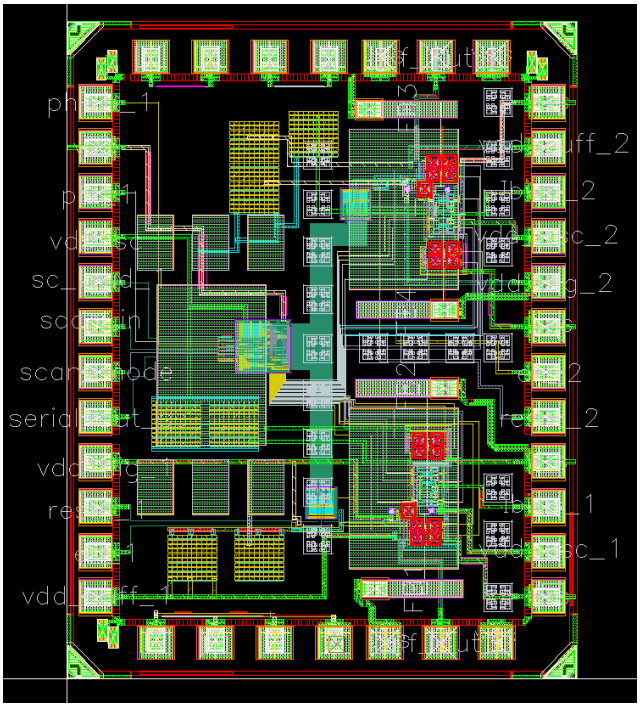

Figure 4-27: Reprogrammable 65nm layout

4.4. Monolithically integrated uncooled IR sensor

4.4.1 Resonant IR sensors

A new area of research in uncooled IR sensors has started to gain interest due to its sensitivity and improved signal-to-noise ratio compared to other thermal devices [61], [62]. Resonant MEMS use a piezoelectric material as their core to generate a signal at a specific frequency and by using an absorber susceptor or coating the IR radiation is absorbed and converted to a temperature delta. The change in temperature will cause a change in the Young's Modulus which is reflected in a change in the resonance frequency. This can be explained by looking at the acoustic velocity, remembering from earlier chapters that resonant frequency directly proportional to acoustic velocity:

$$f = \frac{v}{\lambda} = \frac{v}{2t} \ .$$

Also, the acoustic velocity is defined as:

$$v = \sqrt{\frac{c_{ii}}{\rho}}$$

where ρ is the material density and c_{ii} is the stiffness constant, and both are temperature dependent as described by:

$$c_{ii} = c_{iio}(1 + \Delta T * TC_{c_{ii}})$$

$$\rho = \rho_o(1 - 3\beta\Delta T)$$

$$t = t_o(1 + \beta\Delta T)$$

where t is the material thickness, ΔT is the temperature difference, $TC_{c_{ii}}$is the temperature dependence of stiffness and β is thermal expansion[63]. To obtain the frequency temperature relationship equations are substituted into equation:

$$f = \frac{v_o}{2t_o}\frac{\sqrt{\frac{(1+\Delta T * TC_{cii})}{(1-3\beta\Delta T)}}}{(1+\beta\Delta T)}$$

This equation is simplified by assuming $|TC_{cii}| \gg |\beta|$, this is true for ZnO where TC_{cii} is 30 times greater (-100x10^{-6} /K) than β (3.5x10^{-6}/k) [64]–[66]. Frequency difference is calculated as follows

$$\Delta f = f_o - f = \frac{f_o}{2}\frac{\sqrt{\frac{(1+\Delta T * TC_{cii})}{(1-3\beta\Delta T)}}}{(1+\beta\Delta T)}$$

with the above assumption equation was simplified to

$$\Delta f = \frac{f_o}{2}\left(1-\sqrt{(1+\Delta T * TC_{cii})}\right) \approx -\frac{f_o * \Delta T * TC_{cii}}{2}$$

As demonstrated the temperature vs frequency relationship is linear for piezoelectric resonators, a higher frequency device will result on a higher response to change in temperature.

4.5 Material selection

4.5.1 Topology thermal mass

For thermal IR sensors the temperature change induced by the absorbed radiation can be approximated by the following relationship

$$\Delta T = \frac{\eta(\lambda)\varphi(\lambda)}{\sqrt{(\omega C_{th})^2 + G_{th}^2}}$$

where ω is the rate of change of the signal, C_{th} is thermal capacity of the sensor, G_{th} is the thermal conductivity of the device, η is the absorption efficiency of the susceptor layer, φ is the IR radiation at a given wavelength [67]. The G_{th} will be limited by the geometry of the tethers of the device, whereas all the other parameters are material and thickness dependent.

An acoustic resonator has a linear relationship with temperature and it is defined as the temperature coefficient of frequency (TCF) [ppm/K] [44]. The higher the TCF of a material the more of a frequency shift will result from a temperature change. Normally a lower TCF is desired for a stable signal reference or other sensing applications, i.e. gas sensing. For IR sensing a higher TCF will result in a faster and higher response. In a structure with multiple material layers with different thermal coefficients an equivalent TCF can be extracted. The equivalent TCF will depend on the TCF of each material and their contribution to the device, i.e. thickness and placement. For example, oxides such as SiO_2 offer a positive TCF, unlike the piezoelectric materials, meaning the material's Young's Modulus increases and in turn the film becomes stiffer with rising temperature [68]–[72].

SMRs offer a higher temperature stability in comparison to FBARs, due to their equivalent thermal mass and TCF[73]. In an SMR part of the acoustic energy is stored in the top layer of the bragg reflector, in this case SiO_2. Because SiO_2 has a positive TCF and part of the acoustic wave is stored in this layer, the equivalent TCF will display a lower value than that of the expected ZnO TCF (-60 ppm/K). FBARs on the other hand are bound by air on both sides and besides the piezoelectric and electrodes there is a Si_3N_4 support layer, both the electrodes and support layer are negligible. Table 4-5 has some common BAW materials and their TCF.

Material	*TCF [ppm/K]*
AlN	-30
GaN	-17.7
ZnO	-60
SiO_2	+55
Si_3N_4	-30

Table 4-5: TCF values for some SMR common materials

4.5.2 Absorber coating

Infrared is an electromagnetic radiation with wavelengths ranging from 750nm up to 1000μm, and it can be divided into four domains, near (NIR), mid (MIR), long wavelength (LWIR) and far (FIR). Each domain has different applications of interest for example NIR (750nm – 2500nm) in fiber optic communications and NIR spectroscopy, which is widely used for medical diagnostics, atmospheric chemistry amongst others [74], [75].

To convert IR into thermal energy a layer, known as the susceptor, or absorber, is needed. The layer is selected depending on the IR region of interest and it must be CMOS compatible and achievable with microfabrication techniques. Silicon nitride has been shown before as a susceptor in the NIR domain and it is CMOS compatible [61].

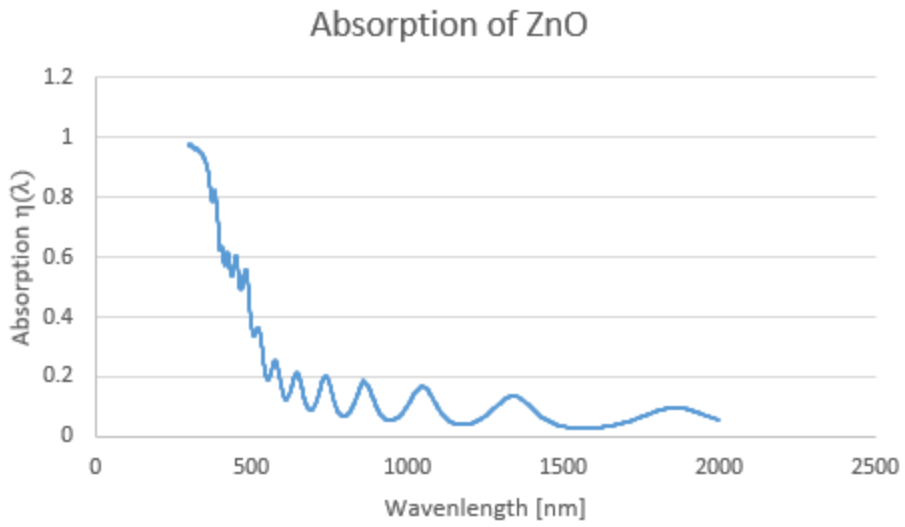

Figure 4-28: Zinc Oxide (1.3μm) absorption spectrum

The absorption was measured for 100nm of Zinc-Oxide (ZnO) and is shown in figure 4-28. Absorption is defined as:

$$A = 2 - \log(\%T)$$

where T is the transmission percentage for a given wavelength. The absorption of silicon nitride was also studied and is shown below in figure 4-29.

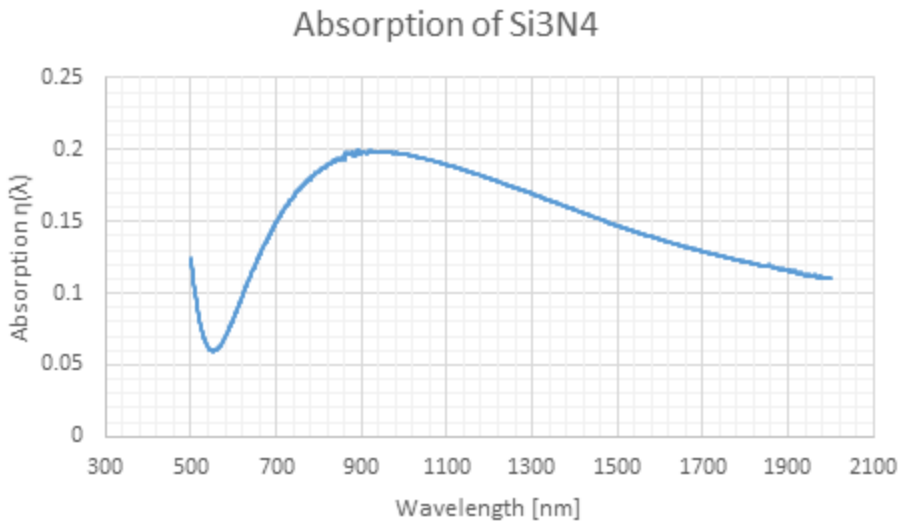

Figure 4-29: Silicon nitride absorption spectrum

Combining ZnO's higher TCF and other NIR susceptors it is possible to obtain higher sensitivity devices.

4.6 High TCF FBAR Monolithic Integration Process Flow

These SMR IR detectors were fabricated on the first generation of 65nm. Based on the FBAR topology a new process had to be developed for the monolithic integration with CMOS. Figure 4-30 shows the fabrication process starting with the chip as received from foundry in (A). The polyimide and metal bed were etched (B) and a blanket SiO_2 layer (500nm) deposited by RF sputtering for smoothing the surface and sharp etch edges. (C)Amorphous silicon (1μm) was then RF sputtered as a sacrificial layer and the whole die was coated in 600nm of neutral stress PECVD Si_3N_4 for the support membrane. (D)The bottom electrode Ti/Au (2 nm/100 nm) was patterned for bi-layer lift off and deposited by e-beam. (E)The ZnO was RF sputtered at 150°C and (F) this was topped off by patterning and depositing the top electrode. (G) The susceptor layer was then deposited by PECVD, 100nm of silicon nitride. To release the membrane, etch

holes were patterned by spinning LOR and depositing a metal hard mask (Al) and dry etching nitride. (H) The XeF_2 was used as an isotropic dry etch with high selectivity for Si, but it was worth noting that Ti etches as well. The Ti was used as an adhesion layer for Au for the electrodes, to avoid its etching a thin layer (30nm) of Cr or Al was deposited over the electrode areas not covered by ZnO.

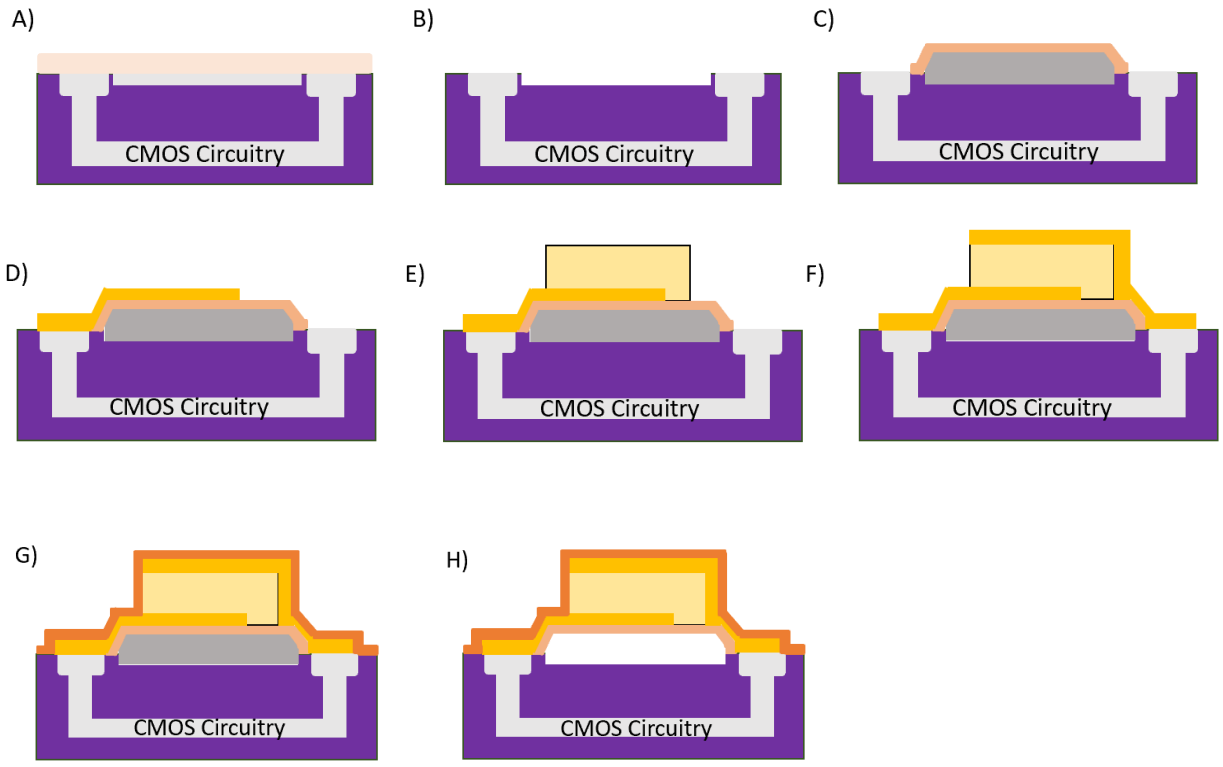

Figure 4-30: IR sensing FBAR monolithic integration process flow.

The first generation of devices showed no electrical output, when studied closely it was observed the device was shorted. Top and bottom electrode were in contact due to the ZnO being etched by the ICP the sacrificial hole etch process. For the next generation the etch holes were designed to be farther away and smaller. Figure 4-31 shows a microscope image and an SEM of the first FBAR with etched ZnO and shorting electrodes.

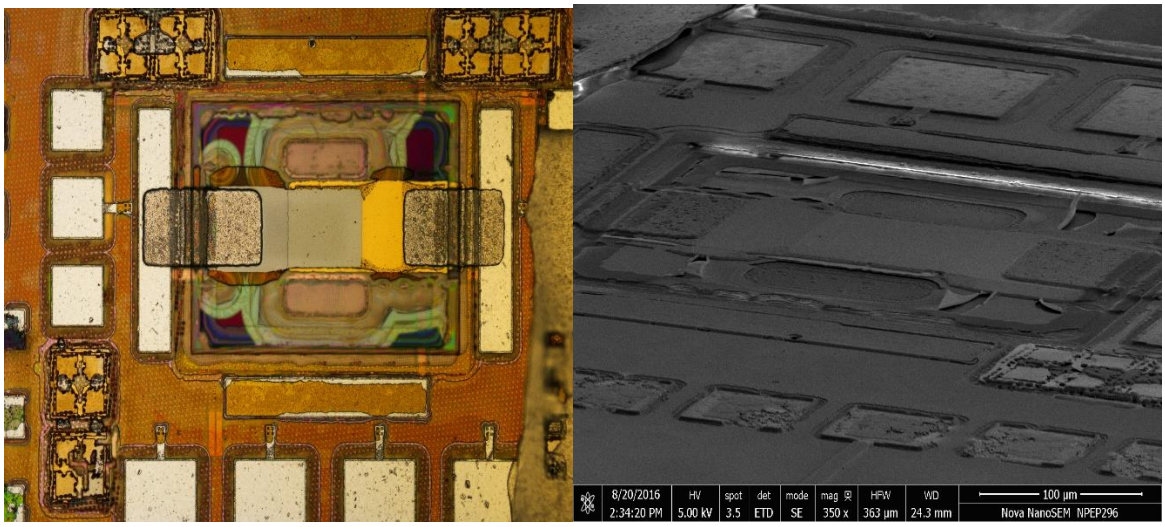

Figure 4-31: From left to right micrograph and SEM of FBAR on CMOS after etching

4.7 Volatile organic compound detection

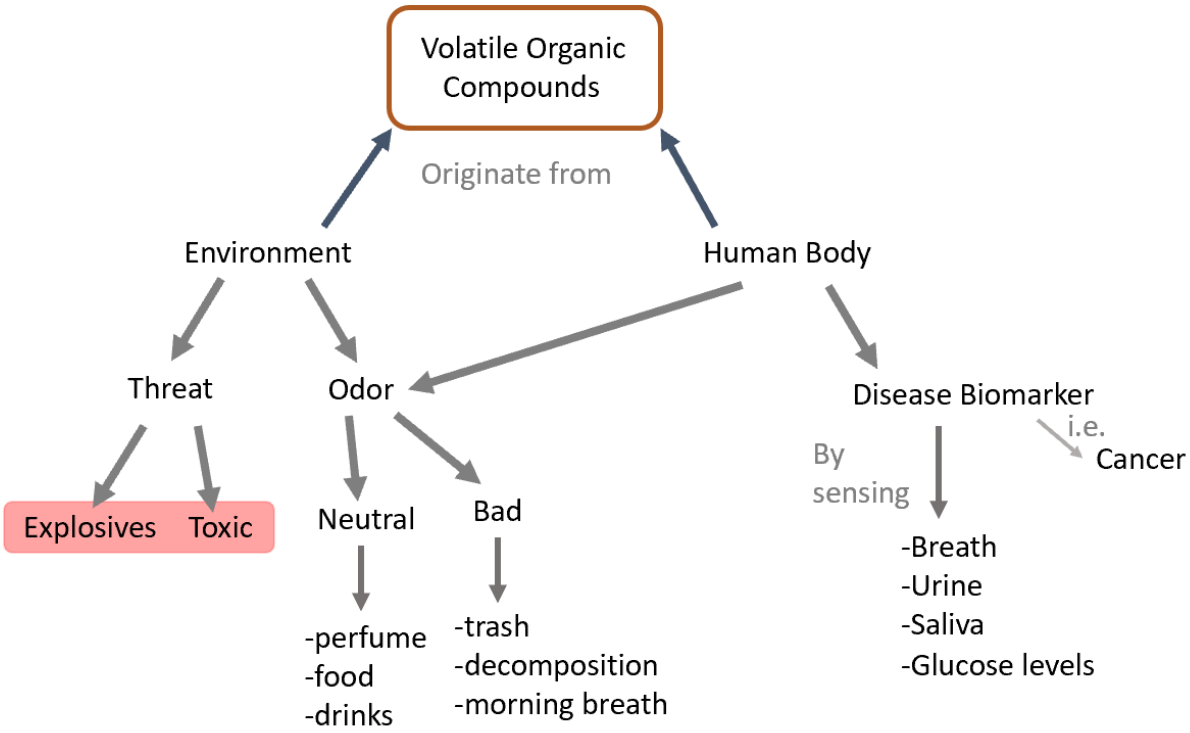

Figure 4-32: Volatile Organic Compound Detection [76]–[81]

Volatile organic compounds (VOCs) are chemicals with high vapor pressure that at room temperature can be found in their gas form [81]. These compounds can be found everywhere indoor and outdoor in our everyday life and in high concentrations they might be harmful to living beings. They can be found in organic solvents, exhausts gases, decaying plants or flesh [41], [76], [79]. In general, VOCs can originate from either the environment of living beings and if monitored it can be used as threat detection, or indicator of common things such as morning breath or if the food is fresh or in decomposition state [9], [12]. A very interesting application is to detect disease biomarkers that can help diagnose illnesses [80]. For this project the main goal is threat detection which can be classified into two areas: explosives and toxic. Here we tried to detect VOCs used in the process of fabricating explosives [77], [82], [83].

4.8 Cyclohexanone

Cyclotrimethylene trinitramine (RDX) was a widely used explosive in World War II and is still used to this day. With a higher explosive energy than TNT and moderate toxicity and possible carcinogenic to humans detecting this material is of great interest for human safety.[84] RDX a very low vapor pressure of ~ 5ppt at room temperature, this makes detection very complicated. On the other hand, cyclohexanone is a solvent used for the recrystallization of RDX and has a high vapor pressure of 5000 ppm, make it viable to detect traces left from fabrication and therefore track RDX as well [84], [85].

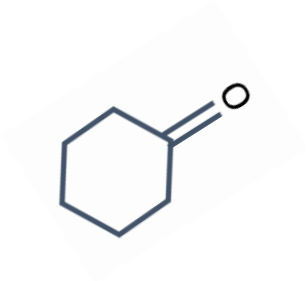

Figure 4-33: Cyclohexanone molecule

Cyclohexanone is an organic compound (98.15g/mol) and a ketone and it derivates from cyclohexane by air oxidation.

4.9 Gravimetric sensing fundamentals

Piezoelectric resonators can be used to detect gases by using an absorber layer to capture the molecules of interest[15], [86], [87]. The molecules captured are added mass on top of the resonator, this process is called mass loading and it causes a shift in frequency that is described by the Sauerbrey equation as follows,

$$\Delta f = -\frac{2f^2}{A\sqrt{\mu * \rho}}\Delta m$$

where f is the oscillation frequency, A is the electrode area (active area), Δm is the added mass, μ is the shear modulus of the piezoelectric material and ρ is the density. This relationship treats the added mass as part of bulk of the piezoelectric material and therefore it is considered part of the resonance path. As the acoustic wave path increases the frequency goes down. How much the acoustic path increases will depend on the layer's thickness. To understand how mass loading relates to the acoustic wave travel path we take the volume of the added mass as

$$\Delta V = A * \Delta t = \frac{\Delta m}{\rho}$$

where Δt is the added thickness. Remembering $v = \sqrt{\frac{\mu}{\rho}}$ the Sauerbrey equation can be rewritten as

$$\Delta f = -\frac{2f^2}{v*A*\rho}\Delta m$$

substituting equation 5.2 into 5.3 we obtain,

$$\Delta f = -\frac{2f^2}{v}\Delta t$$

this shows a direct relationship between the change in thickness of resonance path and frequency. The frequency dependence is not linear it depends on the piezoelectric thickness and as shown above the added thickness, this knowledge helps simplify the equation further. The dependence on the piezoelectric thickness comes from

$$f = \frac{v}{\lambda} = \frac{v}{2t}$$

where λ is the acoustic wavelength which defines the thickness as twice the length, assuming boundary conditions are met for half-wavelength operation. Plugging 5.5 into 5.4 results in

$$\Delta f = -\frac{f}{t}\Delta t \;\; ; \;\; \frac{\Delta f}{f} = -\frac{\Delta t}{t},$$

this relationship shows that what causes frequency shifts is the added thickness of the material not its mass[42]. This means properties such as constant of stiffness, density and acoustic velocity are neglected for the added layer, assuming it is not thick in relation to the piezo layer. Because Δm is treated as an extension of the piezoelectric film the Sauerbrey equation will only hold if the added mass is spread uniformly over the surface, the thickness is not comparable to the piezoelectric thickness and it is a rigid material. If one or more of these conditions are not

met the Sauerbrey equation breaks and cannot be used to describe that system, other methods such as impedance matching must be used to extract frequency shifts from mass loading.

4.10 Volumetric vs Surface absorption

Acoustic resonators, such as BAWs and SAWs, normally require functionalization of the surface to increase its affinity to specific materials. In other words, a selective coating is required to absorb, i.e. mass load, specific analytes of interest and cause a change in the frequency of resonance that can be calibrated to quantify VOCs. There are multiple approaches for using organic materials as selecting interfaces on BAWs, the most common examples are polymers and monolayers. Previous work in our group has demonstrated monolithically integrated SMRs on CMOS for VOC sensing using polymers such as, polydimethylsiloxane (PDMS) and polyisobutylene (PIB) for detecting toluene, acetone and ethanol[15]. Polymers are thick (several and soft materials, that often lower the Q of the device, depend on the volumetric absorption of the VOC to change stiffness. The volumetric absorption will depend on the polymer-solvent relationship characterized by the partition coefficient K, which is a ratio of the concentration of a specific analyte absorbed in the film and the surrounding gas. The partition coefficient is defined as

$$K = \frac{C_{polymer}}{C_{gas}}$$

where $C_{polymer}$ is the absorbed concentration and C_{gas} is the surrounding gas. The partition coefficient is normally extracted empirically using the Sauerbrey equation.

The other method of sensing with coatings is uses surface absorption where the surface is made reactive to specific analytes by means of monolayers. For this type of sensing the sensor is

loaded by mass trapped on the surface. These coatings are known to have faster responses than their polymer-based counterparts but are limited in their sensing dynamic range due to their direct surface area dependence. The device active area will define the saturation point and for this reason these materials are not used in high concentration environments [88], [89]. Monolayers are low cost and can be easily engineered for high selectivity, in this work a monolayer known as thiourea is studied and analyzed for selectivity and lifetime [85].

4.11 Self-Assembled Monolayers

Self-assembled monolayers can be divided into three sections: the functional group, tail or spacer and the head group. Starting from the bottom, the head group defines what type of surface the molecule will adhere to. There are two types of head groups: silanes which adhere to oxide surfaces and thiols that react with metallic surfaces. The tail can be made of different lengths and it really will depend on the application, as its second name suggests it acts as a spacer between the surface and the outside world. The functional group is the terminal that interacts with the exterior or outside world, it will also define the work function of the surface and reactive or inert it is to other particles [90].

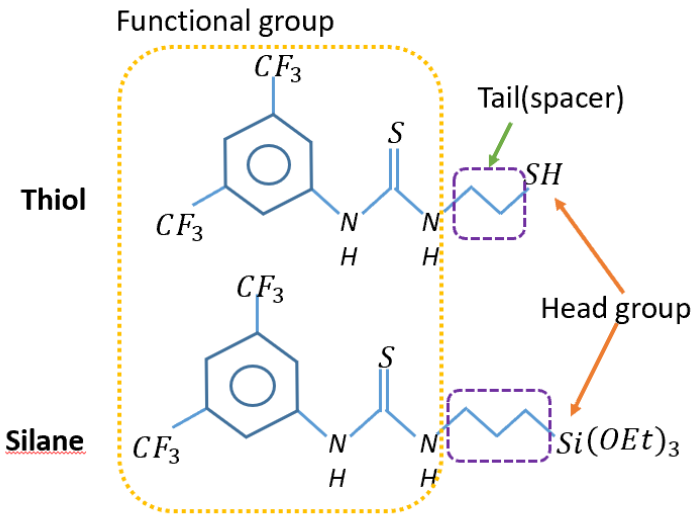

Figure 4-34: SAMs components and groups

The SAM, or selector, used in this project is a trifunctional sensor. It has three main components the first one is the head group a carbon bonded sulfhydryl (SH) group, or thiol, that forms a ligand with the metal ions of the surface of the substrate. The functional group is divided into the thiourea and a bis(trifluoromethyl) aryl group. Thiourea is the receptor that defines the selectivity of this molecule. The receptor binds to ketones by forming two hydrogen bonds, in this case it also serves as a connector between the head and functional groups. The bis(trifluoromethyl) aryl group is the interface with the external environment, from a work function perspective the surface is fluorinated making it hydrophobic. This group is known to form $\pi - \pi$ stacks, non-covalent attraction between aromatic rings, with aromatic molecules. Moreover, this group is known to have a strong electron pull or withdrawing from other molecules this in turn has been proven to improve the selectivity of receptors such as thiourea due to improved hydrogen (proton) acidity. [85]

The SAMs used in this work were synthesized and provided by our collaborators from the University of Vienna.

4.12 SAM Deposition

SAMs are deposited in liquid or gas form where the sample is placed for a certain amount of time for the reactions to happen between the organic molecules and the surface. For SAM deposition longer wait times result in denser and organized films, but this is not always desired it depends on the application and requires iteration [91].

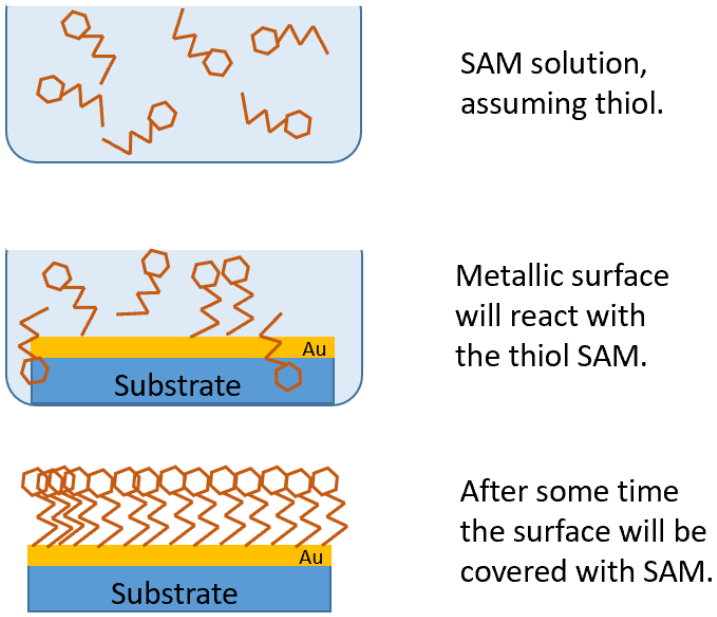

Figure 4-35: SAM Deposition

The samples were cleaned with acetone, IPA, DI water, ethanol and finally placed in UV to increase oxygen dangling bonds on the surface. The SAM solution (0.345g/Mol) was prepared for a 1mg/mL concentration with ethanol as the solvent. The sample was then placed in the

solution for 1 hr. The sample is then removed from the solution and placed in ethanol and dried in N_2.

Chapter 5 **: Results**

Bulk acoustic wave (BAW) structures were monolithically integrated on the CMOS substrates and tested. The following sections go over the measured and analyzed outputs. Moreover, these integrated systems are demonstrated for low power applications such as infrared and volatile organic compound sensing.

5.1 SMR on 65nm

For testing a four-point DC EYE-pass probe, PPPG was used for biasing and GSG RF probes for the outputs. An external printed circuit board (PCB) was made for added decoupling capacitors, reduced supply noise, and generating and controlling the bias currents with potentiometers. Both an oscilloscope and spectrum analyzer were used to obtain the time and frequency domain outputs, respectively.

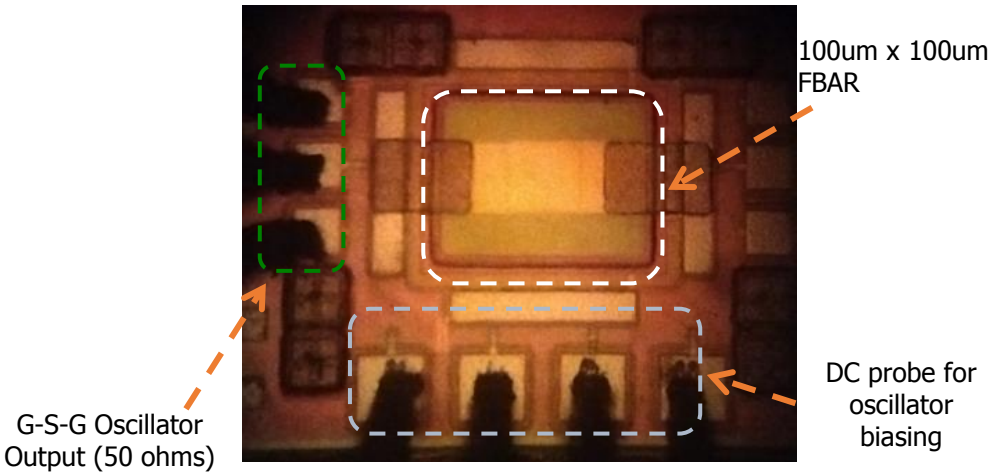

Figure 5-1: On-chip probing setup

A 100µm SMR was integrated with the underlying pierce oscillator. A frequency of 1.76GHz was obtained with a 5dBm power level and a 600mV peak to peak swing. The frequency did not

show any variation with change in supply voltage or bias current, this implies the oscillation comes from the piezoelectric material.

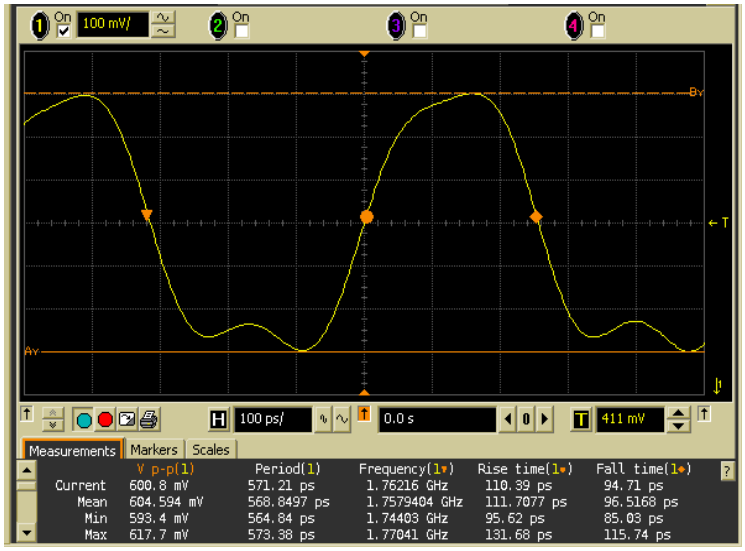

Figure 5-2: Time domain oscillator output from the oscilloscope

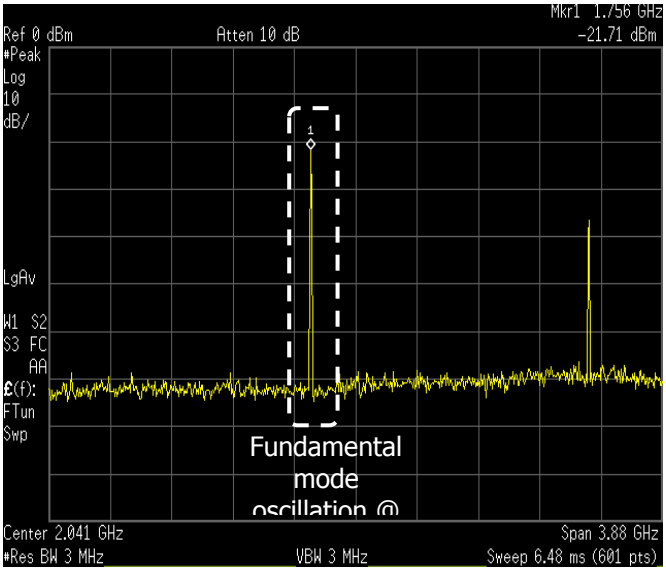

Figure 5-3: Frequency domain oscillator output as measured from SA

Phase noise was also measured to obtain the figure of merit (FOM) for the oscillator which can be described as:

$$FOM = 10\log\left(\left(\frac{f_o}{\Delta f}\right)^2 \frac{1}{L\{\Delta f\}P}\right)$$

where P is power consumed, f_o is oscillation frequency, Δf frequency offset of the measured noise and $L\{\Delta f\}$ is the measured phase noise at the specified offset [92], [93]. Below on Table 5.1 are the FOMs of this work and others compared. For future chips, lower power consumption will be required to improve the FOM.

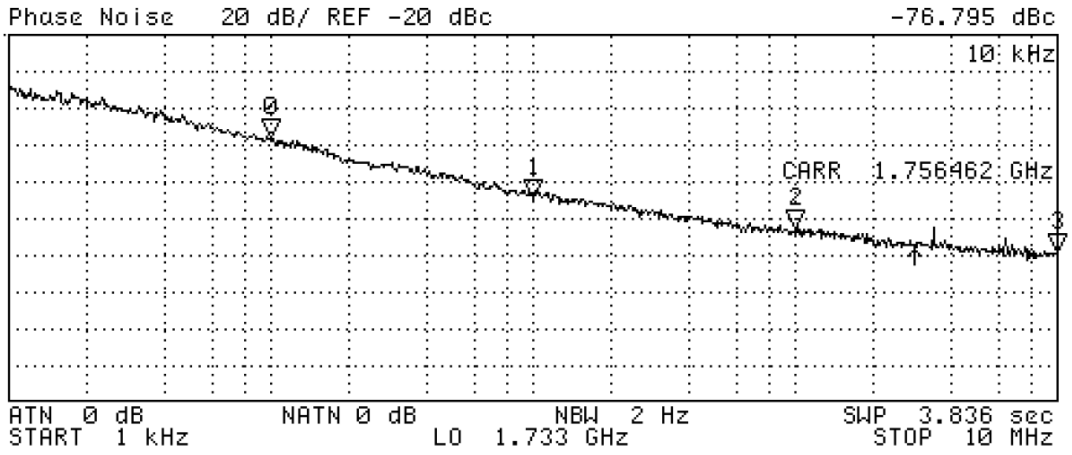

Figure 5-4: Measured phase noise for SMR on 65nm

Reference	f_{osc} *[GHz]*	*Power [mW]*	*Phase Noise @100kHz [dBc/Hz]*	*SMR*	*FOM [dB]*
[92]	1.9	0.3	-120	Off-chip	210.8
[94]	2.145	12	-124	Flip-chip	199.8
[95]	5.46	4.59	-117.7	Monolithic	205.8
[96]	2.1	58.3	-120	Monolithic	188.8
This work [97]	1.75	9.9	-109.8	Monolithic	184.7

Table 5-1: FOM summary and comparison [98]

5.2 FBAR on 65nm results

Testing was done with on-chip probing with an Eye-pass probe for DC biasing and GSG RF probes for the output. The resonator has an oscillation frequency of 1.5GHz. A micrograph of the finished integrated device is shown in figure 5-5**.** The FBAR has a 650mVpk-pk oscillation which translates to a -0.96dBm power output, seen in figure 5-6.

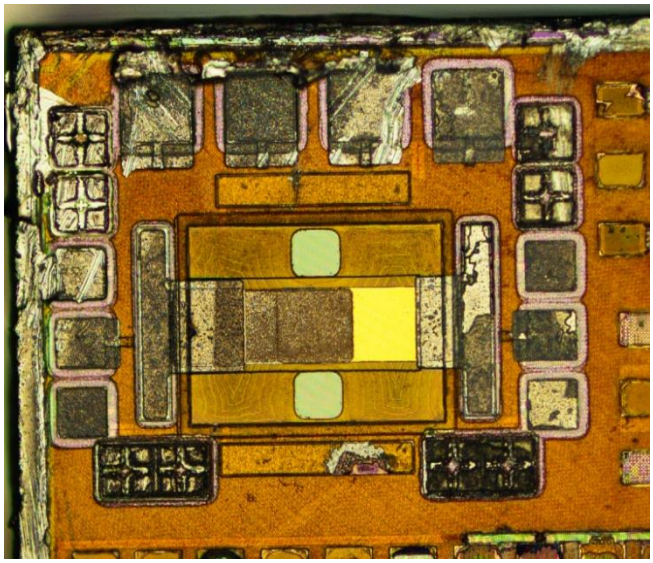

Figure 5-5: Micrograph of FBAR on 65nm

The frequency spectrum shows an overtone at 3GHz, unlike the SMR where the bragg reflector effectively filters out overtones, the membrane devices will display the fundamentals and its weaker overtones as shown in figure 5-7.

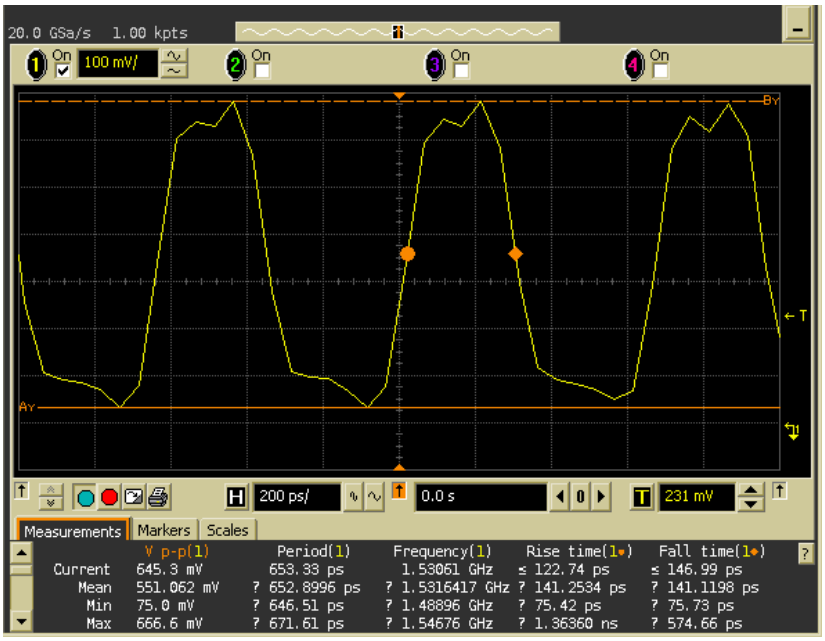

Figure 5-6: Output of oscillator in the time domain

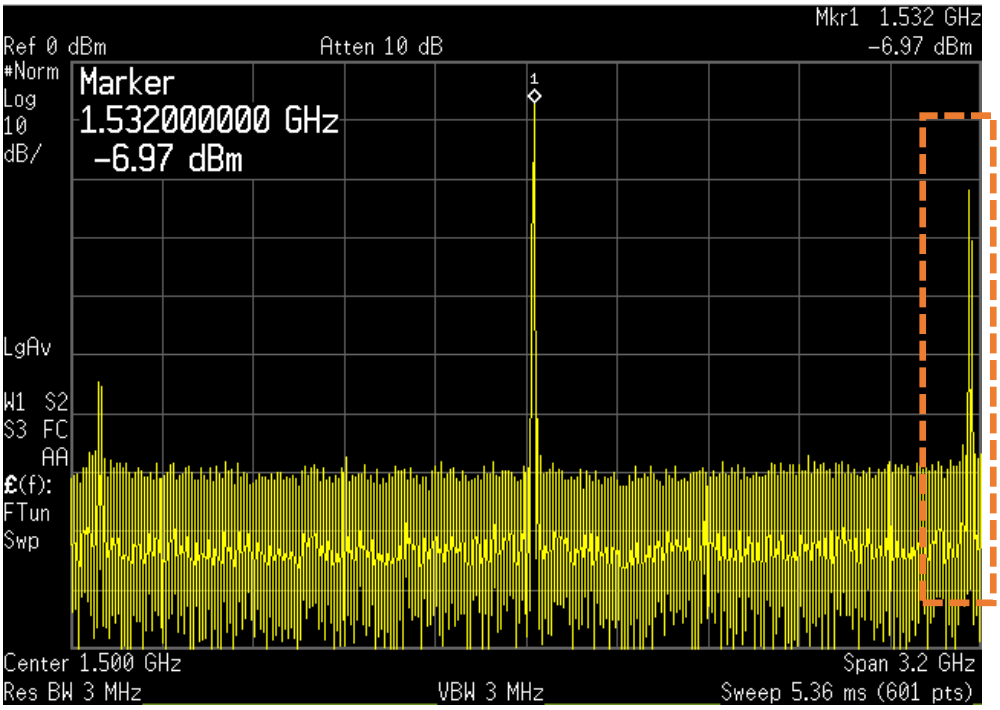

Figure 5-7: Power spectrum of FBAR on 65nm.

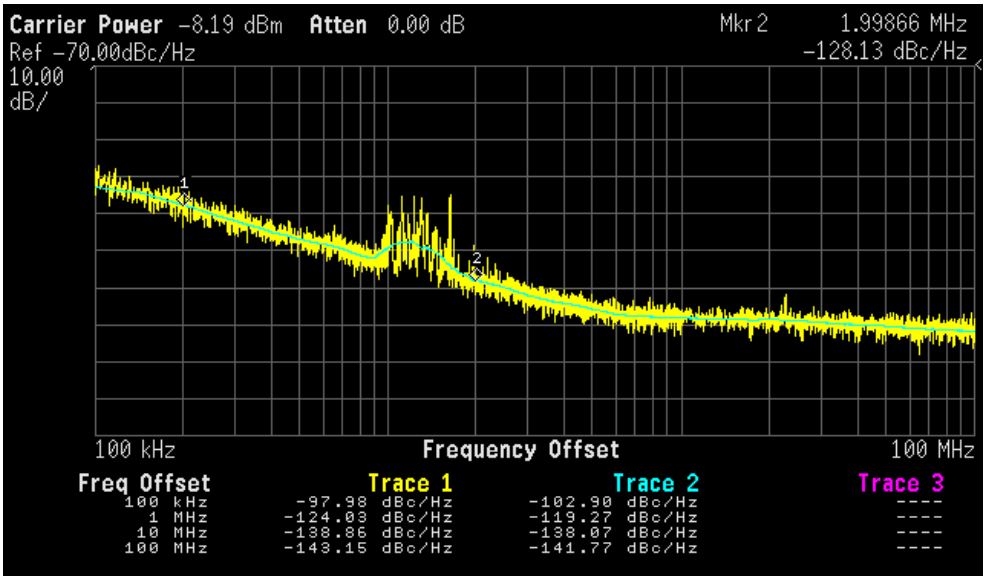

Figure 5-8: FBAR phase noise

Phase noise was also studied and used to extract the FOM and Q factor, the comparison between SMR and FBAR on 65nm is on Table 5.2**.** The FOM was lower for the FBAR due to the higher power consumption. The quality factor was half that of SMR, and two possible reasons for this are the membrane stress was still not neutral causing the film can be seen slightly bulging and using thick metal electrodes as the anchor induces higher mechanical losses. Metal anchors were used because ZnO is highly compressive and any large height change will cause the membrane to break or "pop- off". Improving the membrane stress requires some extra tooling of the PECVD support nitride.

Structure	*Phase Noise @100kHz*	*Power Consumption [mW]*	*FOM [dBc/Hz]*	*Q factor*
SMR	**-109**	**9.9**	**186**	**460**
FBAR (release)	**-103**	**36**	**181**	**212**

Table 5-2: Comparison between SMR and FBAR devices on 65nm

5.2.1 180nm Testing

Each oscillator was tested on its own and both, the time and frequency domains, were observed. A four-point DC EYE-pass probe with an PPPG output was used for biasing and a GSG and SGS 100μm pitch RF probes for measuring the three of the oscillators and the LC, respectively.

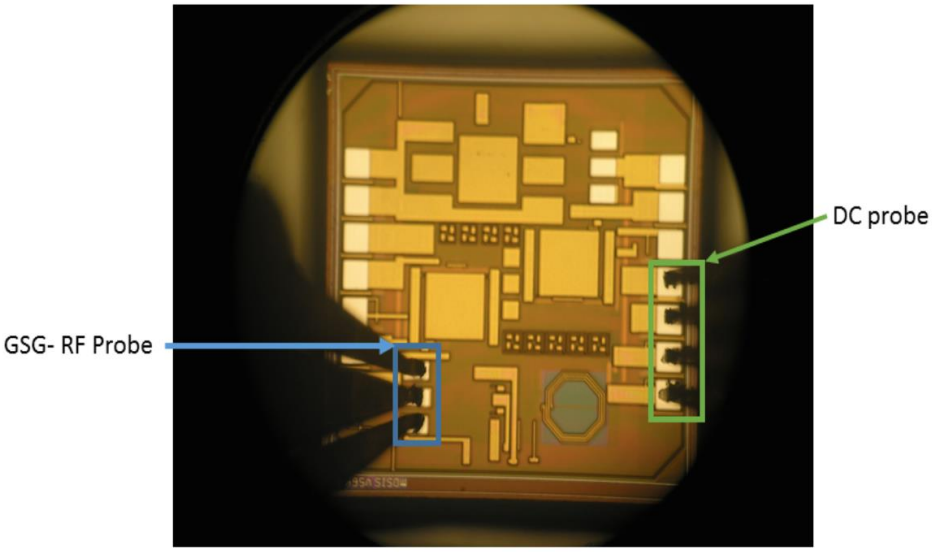

Figure 5-9: Testing oscillator setup

The LC oscillator was measured to have a 1.4 V peak to peak oscillation at ~1.5GHz when the variable capacitor value is at its minimum (Vc = 0V).

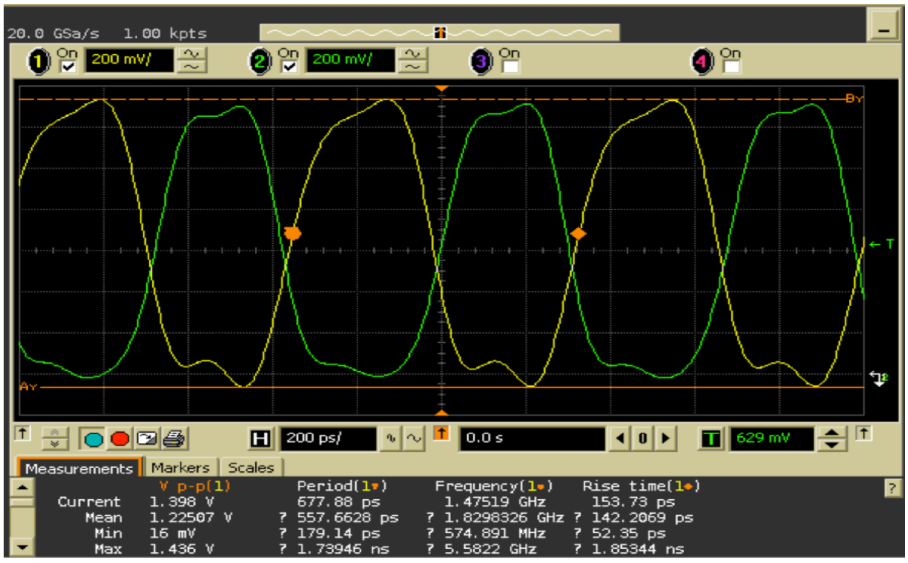

Figure 5-10: Time domain LC output

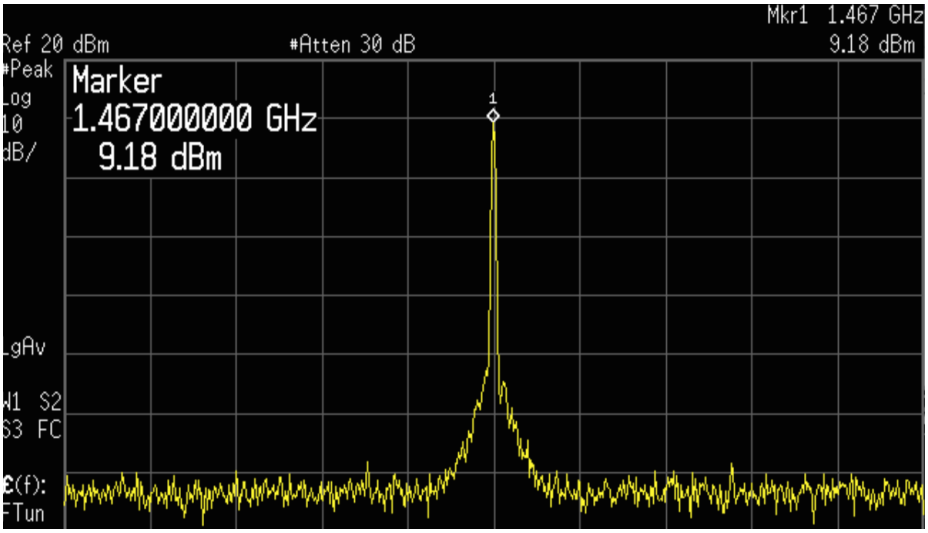

Figure 5-11: Spectrum Analyzer output for LC oscillator

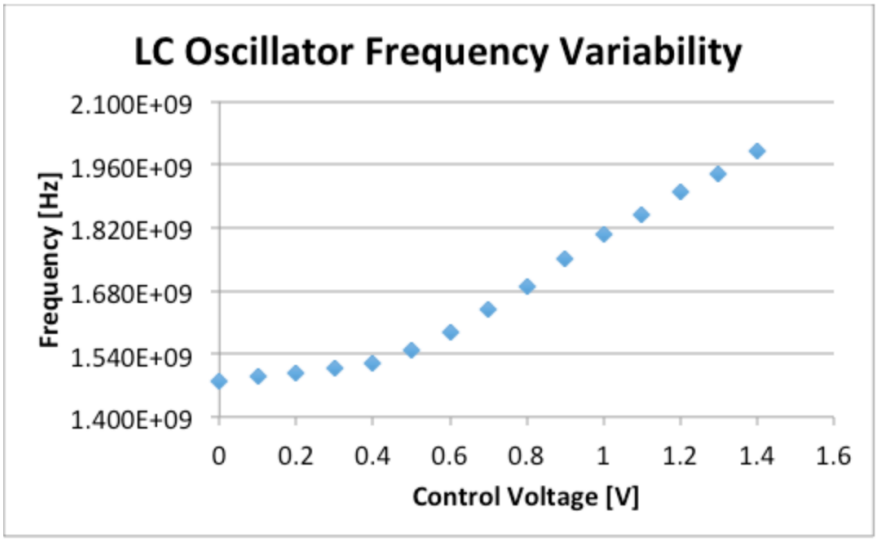

Figure 5-12: LC frequency variability

Figure 5-13: Fabricated SMRs on 180nm IC

The pierce oscillators were tested post-fabrication but there was no measurable output for either. Because the gain is voltage dependent there are not enough knobs to turn for optimization. The outputs were then observed in the spectrum analyzer, for the single stage pierce there were no noticeable tones at the frequency of interest but for the three-stage pierce there was a weak tone at 1.78GHz, but not enough gain for oscillation.

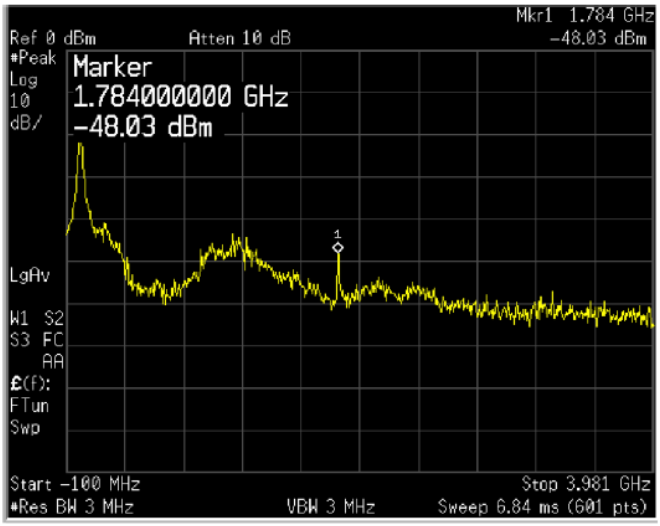

Figure 5-14: Spectrum analyzer output for the three-stage pierce oscillator

Both pierce oscillators were designed for a gain two times greater than R_m assuming it is 6-ohms. To understand what happened, the stand alone SMR S-Parameters were measured and the devices on 180nm CMOS were modeled.

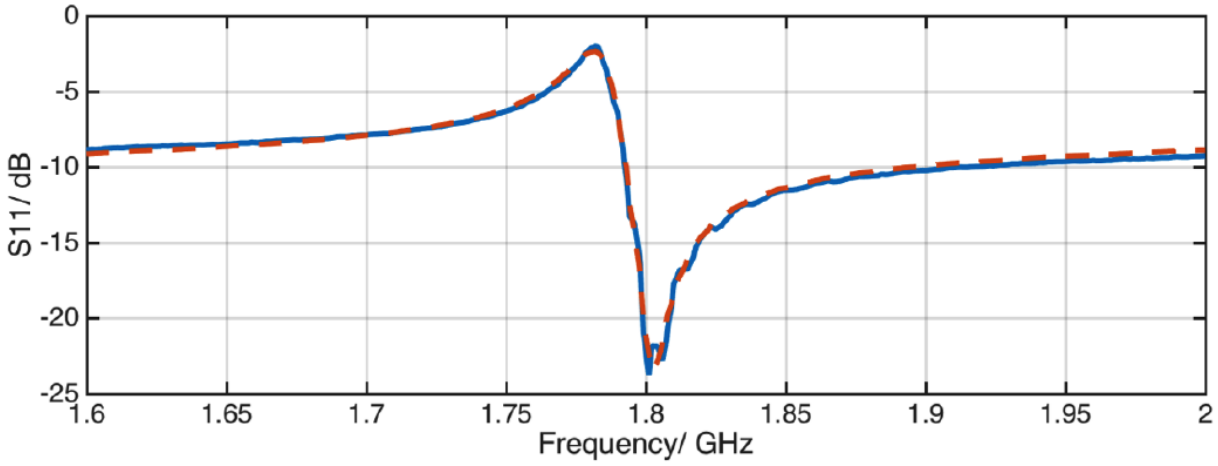

Figure 5-15: Measured and modeled S11 for stand-alone SMR on the 180nm CMOS chip

Device on:	*Quality Factor*	*Kt^2 [%]*	*Cshunt [fF]*	*Rm [Ω]*
Glass	500	4.5	10	5
CMOS	460	3.3	500	4.7

Table 5-3: Summarized comparison of extracted parameters from modeled devices

The quality factor is comparable to glass samples and the kt^2 is lower, this is due to the parasitic shunt capacitances from the CMOS substrate. There is some leakage from input to output terminal and this is modeled as a small resistor across both nodes.

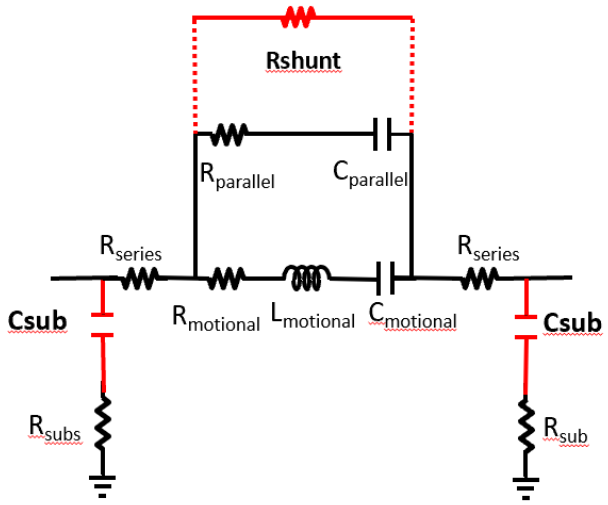

Figure 5-16: Extracted electrical model for device on 180nm CMOS

From SEM imaging a fence or wall of what is supposed to be left-over diffusion layer from the bed etch steps was found. This fence is contacting the aluminum contact extensions on both sides, as shown in figure 5-17. This finding explains the R_{shunt} obtained from modeling.

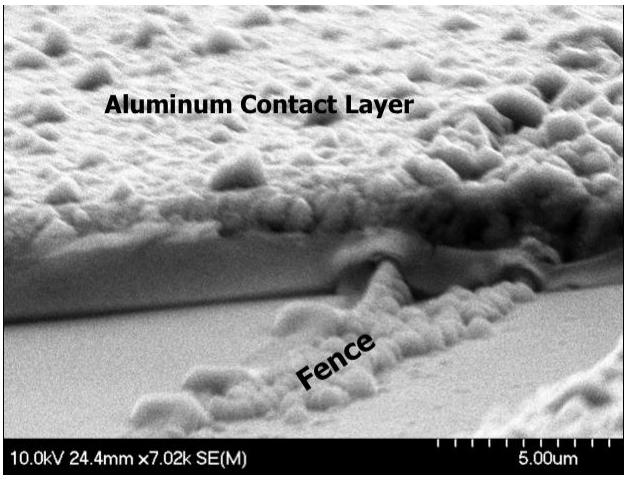

Figure 5-17: SEM of diffusion layer leftover fence

5.3 Temperature response

The device was characterized as a temperature sensor by measuring the output signal while on a controlled heated stage. The temperature was swept from room temperature to 45℃ in steps of 1℃, the result is a linear relationship as expected. As the temperature rises the material became softer and the stiffness constant was reduced. The particles in the materials vibrate with energy from the added temperature causing the acoustic wave to hit more on its path from one boundary to the other this effectively slows down the wave and downshifts the frequency as shown in figure 5-18. The equivalent TCF for the structure is extracted from next plot to be -62ppm/K.

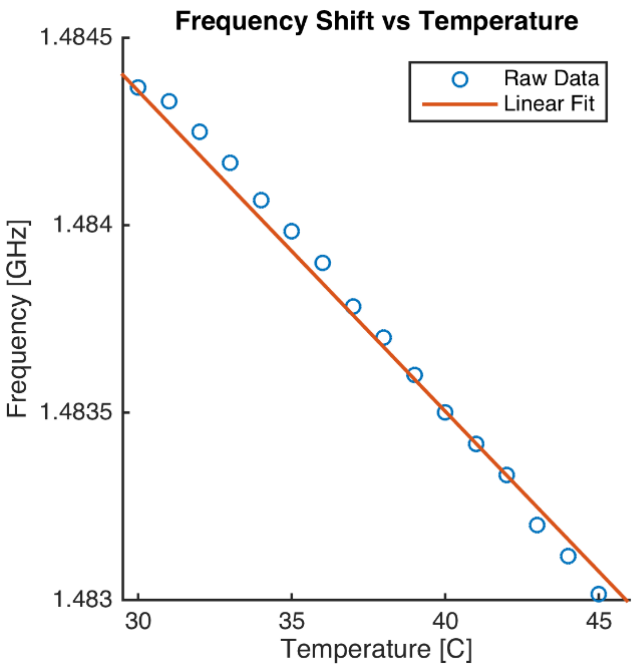

Figure 5-18: Linear frequency temperature dependence

The noise induced by temperature was measured as well and is shown for three temperatures in figure 5-19**.** For this type of sensor, the limit of detection is determined by the noise equivalent thermal difference (NETD), this was extracted from figure 4-50 to be ~6 kHz, 4ppm or alternatively 66mK. This value can be theoretically improved to be 10mK, lower than the leading microbolometer technology with 25mK.

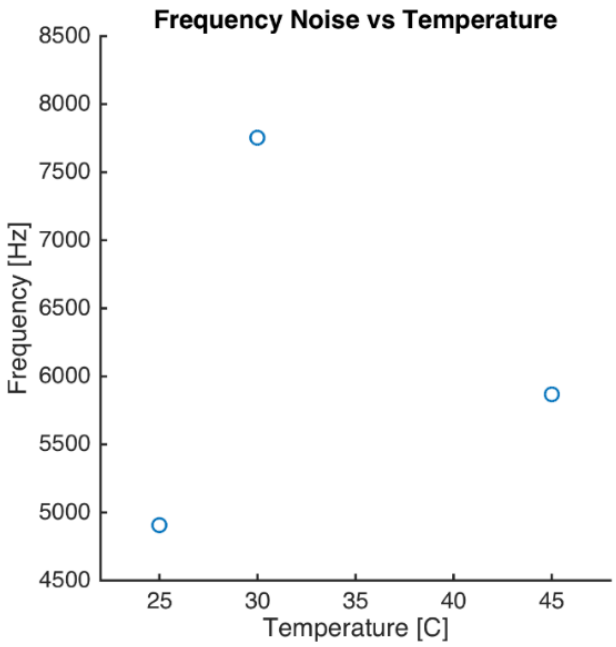

Figure 5-19: Jitter noise at different temperatures

5.4 IR detector results

A 12mW red laser (650 nm) was used to obtain the sensor long wavelength optical response within the absorption region of Si_3N_4. Nitride will absorb 10-20% from 600nm to 2.5µm wavelengths (NIR). The laser was driven up to 2W due to limitations in the driver circuits available. The incident power on the device was calculated to be 540nW, as follows

$$P_i = P_{laser} \frac{A_{device}}{A_{laser}}$$

where P_i is incident power, P_{laser} is the laser power, A_{laser} is the laser beam width area (ϕ 2mm) and A_{device} is the active area of the device. The linear relationship between temperature and frequency, derived before, is experimentally demonstrated in figure 5-20. The resulting shift was 600KHz as shown in figure 5-21, with an extracted sensitivity of 7 $\left[\frac{kHz}{\frac{\mu W}{mm^2}}\right]$.

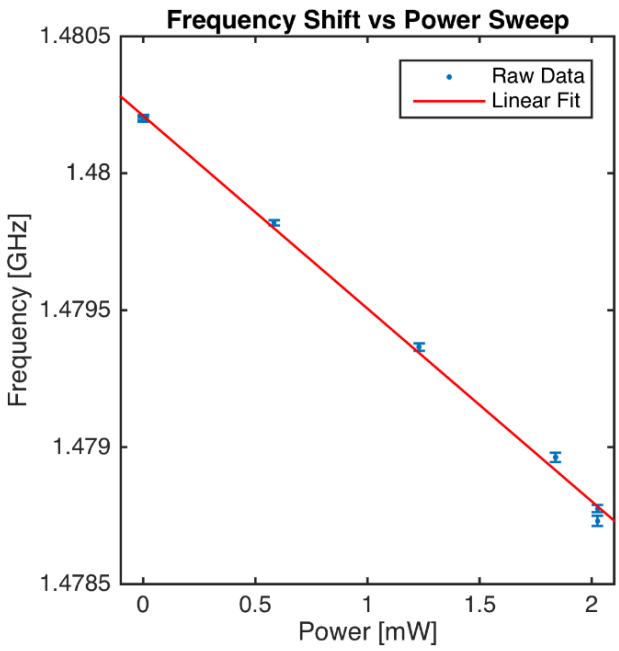

Figure 5-20: Frequency Shift vs Power Sweep

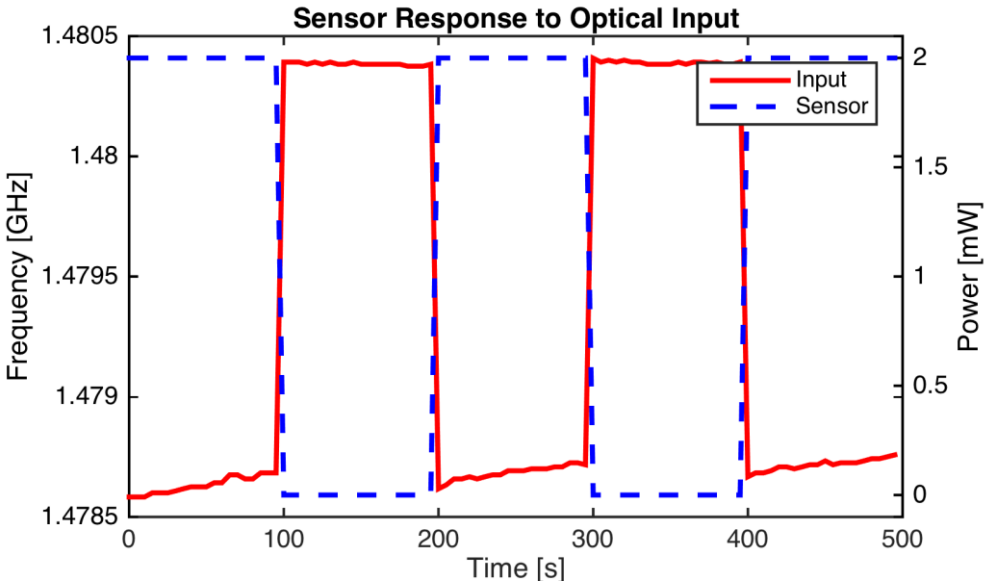

Figure 5-21: Sensor response to red laser

Parameter	[99]	[100]	[66]	*BOLOMETER*[101]	*This work*[102]
Piezoelectric	AlN	AlN	ZnO	-	ZnO
TCF [ppm/K]	-30	-27	-77	-	-62
NETD [mK]	50	-	-	30	66
Sensitivity [Khz/(uW/mm^2)]	-	-	13	-	3.5
Size	190umx128um	75umx200um	150umX150um	25um pitch	100umx100um
Operating Frequency	116MHz	397MHz	1.8GHz	-	1.5GHz
CMOS integrated	N	N	N	N	Y

Table 5-4: Results and comparison to other leading technologies

The results were compared to other technologies available and are shown in Table 5-4. These results demonstrate the capabilities of this system, by selection of other coatings with higher absorptions in NIR and improving the membrane devices this technology shows promise for a higher sensitivity and low power alternative.

5.5 Gas chamber setup for testing

A chamber was built for dynamic flow testing the SAMs on SMR and their sensitivity to different VOCs, i.e. acetone, toluene and cyclohexanone. The chamber is a 4-way stainless steel QF flange cross, that allows for quick part exchange. Two inputs were designated for electrical feedthroughs and read outs and the remaining two for gas flow and exhaust.

There are two gas input lines, one for pure N_2 flow for dilution and the other one is for the VOC flow. The VOC is in its liquid form and a bubbler was used along with a carrier gas, N_2, to flow VOC into the chamber.

5.6 Concentration equations

To calculate the VOC concentration in the chamber assuming constant flows the following equation was used:

$$C_{ppm} = \left(\frac{P_s}{P} * \frac{F_{voc}}{(F_{voc} + F)}\right) 10^6$$

where P_s is the saturated partial pressure in mmHg, P is the chamber pressure (760 mmHg), F_{voc} is the flow in sccm of the VOC and F is the dilution gas flow in sccm[103]. Antoine's equation was used to calculate partial pressure in the chamber

$$\log_{10}(P) = A - \left(\frac{B}{(T + C)}\right)$$

where A, B and C are Antoine's constants and T is temperature in Kelvin. Table 5.5 shows some of the Antoine constant values used for the VOCs tested.

VOC	*A*	*B*	*C*	*T [K]*
***Cyclohexanone** [104]*	4.1033 ± 0.00099	1495.51 ± 0.67	-63.598 ± 0.075	362.78 - 438.92
***Acetone** [105]*	4.42448	1312.253	-32.445	259.16 - 507.60
***Toluene** [106]*	4.23679	1426.448	-45.957	273.13 - 297.89

Table 5-5: Summary of Antoine's constants for VOCs used

The VOC flow requires a separate analysis taking into consideration the bubbler. The bubbler was modeled as closed volume with constant temperature with a known input flow. Some of the assumptions were the gas is in thermal equilibrium with the liquid, only vapor leaves the system and the temperature of the liquid is the same for the chamber and gas. The VOC flow was calculated as follows:

$$F_{voc} = F_c \frac{P_s}{(P_o - P_s)}$$

where F_c is the carrier flow in sccm and P_o is the output pressure. To obtain P_o the input pressure P_{in} was found by adding a pressure gauge at the input of the bubbler and then substituting in $P_o = P_{in} + P_s$.

5.7 PCB design

A PCB was designed for quick debugging and testing of the SAMs on SMRs. Below is a block diagram of the system:

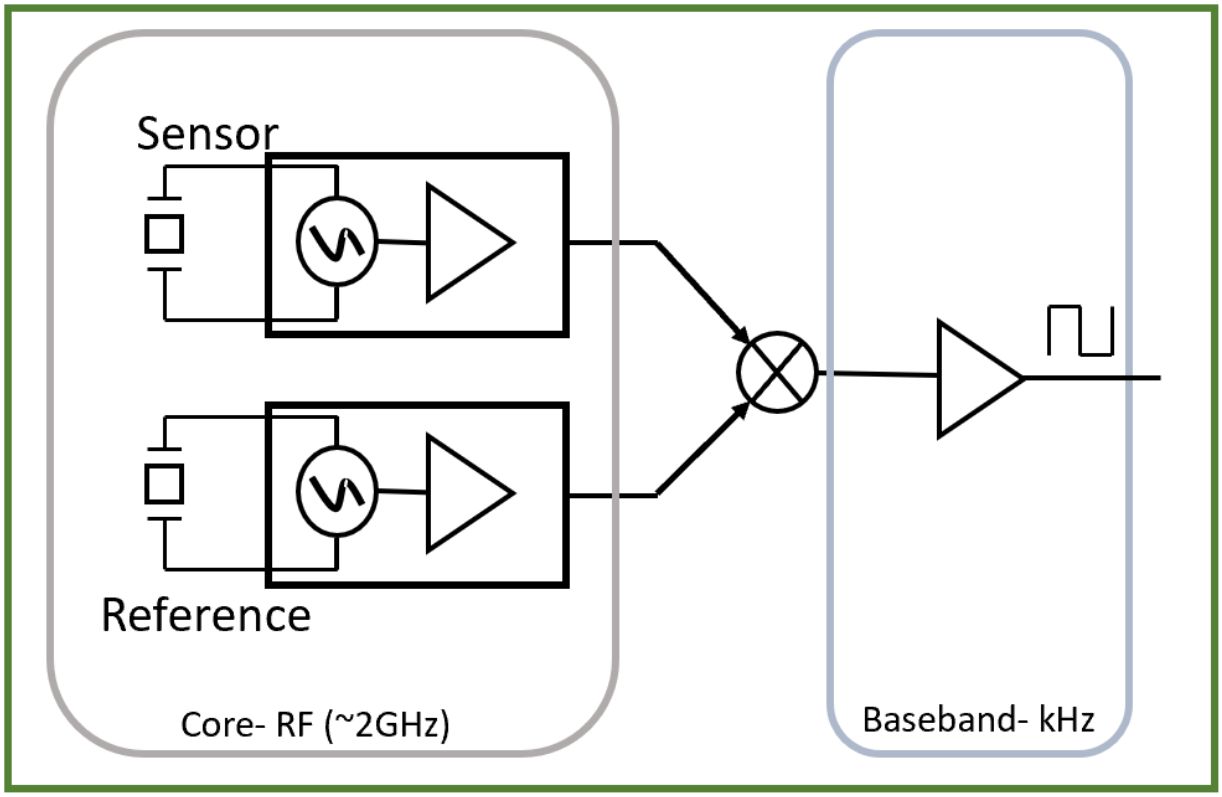

Figure 5-22: PCB system level

The PCB has two RF oscillators using HEMTs and RF buffers, the core of the oscillators were SMRs on glass then wire bonded to the board. The outputs of the oscillators then go to a mixer to eliminate common noise and drift. One of the samples was coated with SAMs before wire bonding, this was the sensor while the remaining oscillator was the reference or control variable. The PCB was designed to operate at a GHz frequency and was modeled and simulated with transmission lines in Advanced Design Software (ADS). Figure 5.23 shows an image of the finalized board layout. An USB port was used for biasing and an SMA for the output signal readout.

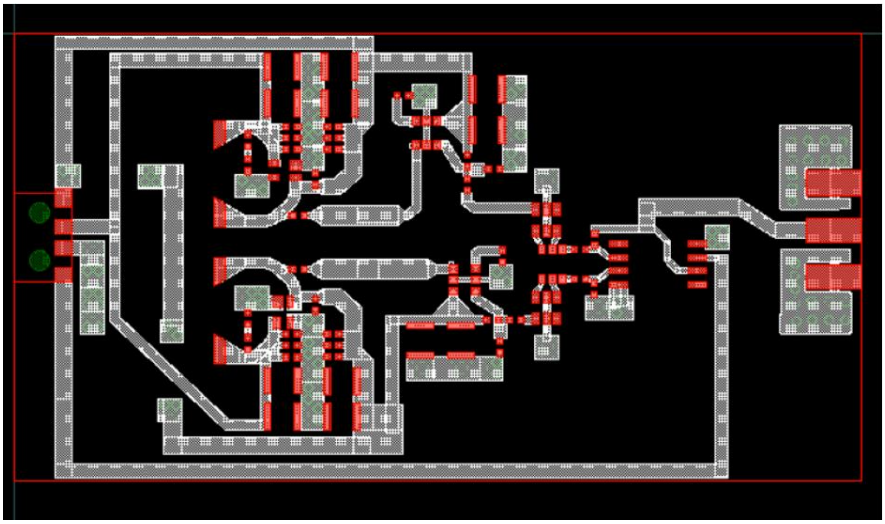

Figure 5-23: PCB Layout

Another PCB was also designed for the 65nm reprogrammable chip for integrability with a microcontroller (MCU) (Teensy 3.6), shown in figure 5-24. It was designed to fit in the gas chamber used for previous tests and uses an USB port for chip bias. The MCU was programmed to control the chip and read out the frequency counts to be compared.

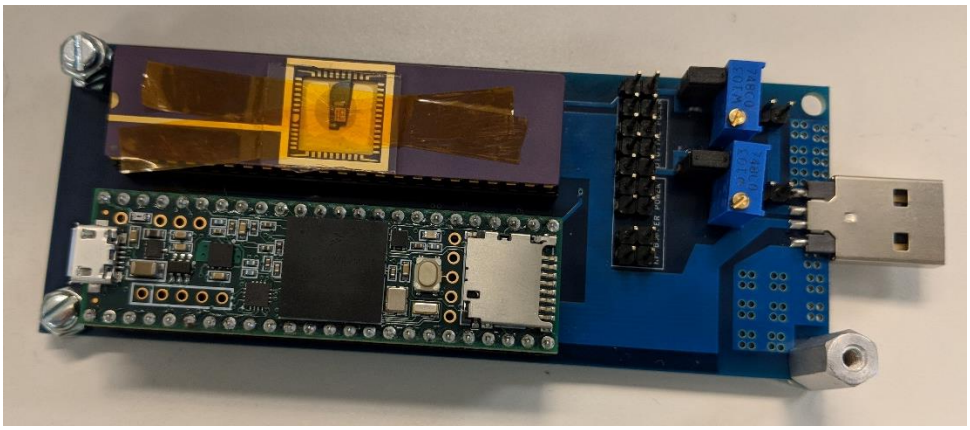

Figure 5-24: 65nm fabricated chip on PCB with MCU gas chamber ready

5.8 Results

All the tests were ran using N_2 as both the dilution gas and carrier gas for the VOC. To test sensitivity of the coating the first test was to run multiple concentrations of cyclohexanone. The VOC controller was fixed at 10sccm while the dilution gas was swept. Figure 5-25 shows the response of the sensor. From left to right the concentrations start from 3.8ppm to the max being 50ppm.

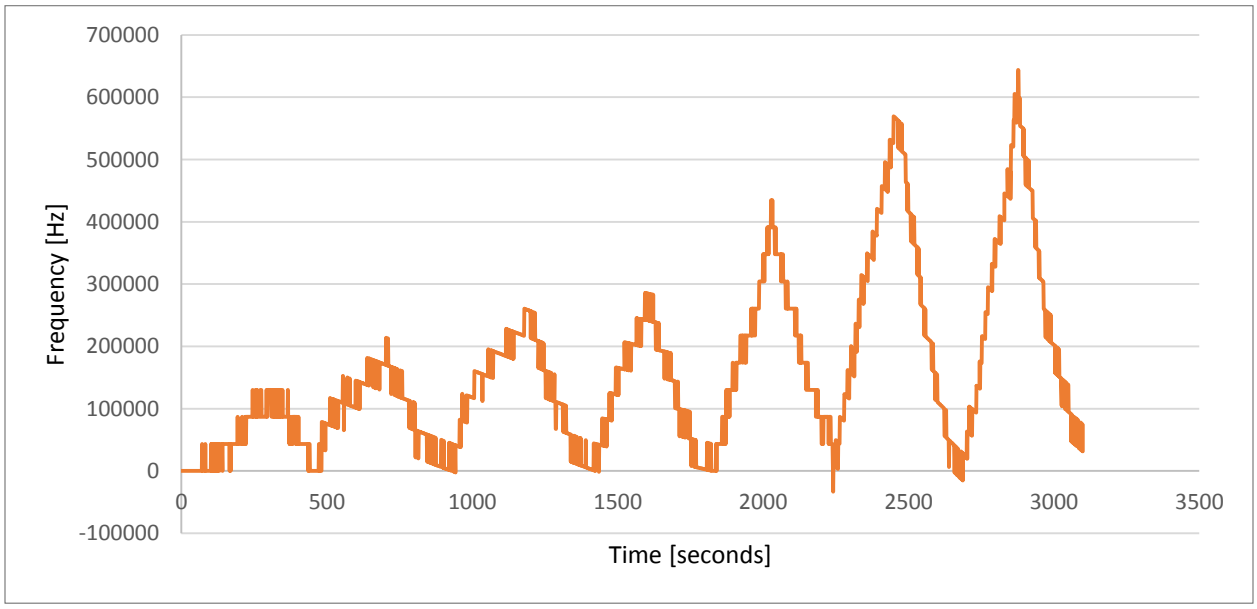

Figure 5-25: Cyclohexanone detection with SAMs on SMR on PCB

To test selectivity two other analyses were run through the system, the results are shown below in figure 5-26. This test was run without dilution, to calculate the concentration in the chamber the volume of the chamber was calculated, and the VOC value was extracted by time and flow as follows,

$$C_{ppm} = \frac{V_{VOC}}{V_{chamber}} = \frac{f_{VOC} * t_{flow}}{V_{chamber}}$$

where V_{VOC} is the VOC volume in the chamber, $V_{chamber}$ is the chamber volume (both volumes are in cm^3), f_{VOC} is the VOC flow into the chamber and t_{flow} is the time the VOC was flowing into the chamber in minutes. The minimum concentration (left) for cyclohexanone, acetone and toluene are 890ppm, 44151ppm and 5588ppm, respectively. The highest responses are for cyclohexanone with concentrations at least 5 times smaller than the other analyzes demonstrating the selectivity of the thiourea coating.

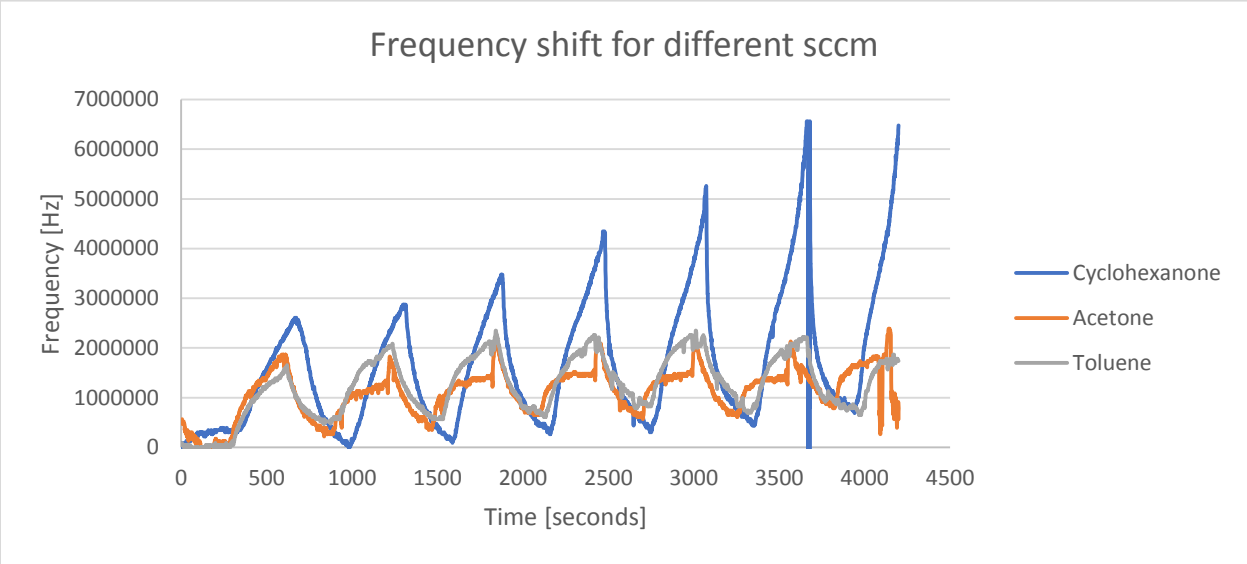

Figure 5-26: Sensitivity test for different VOCs

To ensure the sample's response was coming from the coating's sensing capabilities another PCB was prepared with two uncoated samples and placed in the chamber. For 10 minutes the VOC was inserted at the 2 minutes mark and shut off at 5 minutes with no measurable change, relaying that the measured responses are from the monolayer. This is shown in figure 5-27.

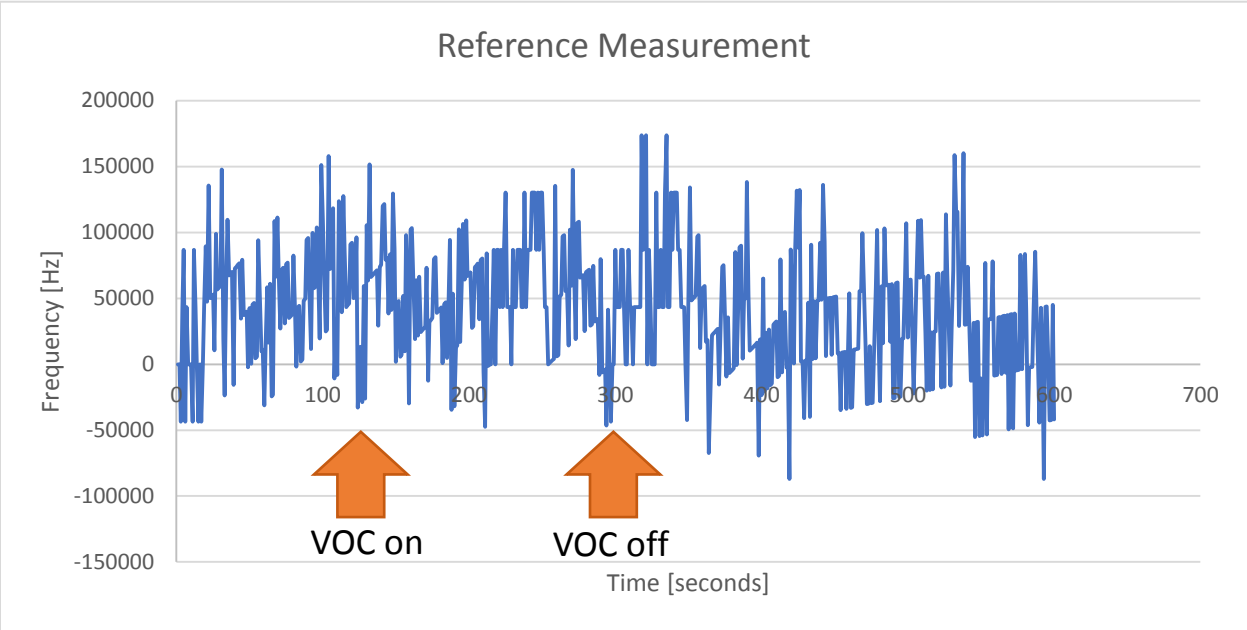

Figure 5-27: Reference measurement

The next test was to see repeatability of the measurements, figure 5-28 shows the result of three cycles of 50ppm with close frequency responses.

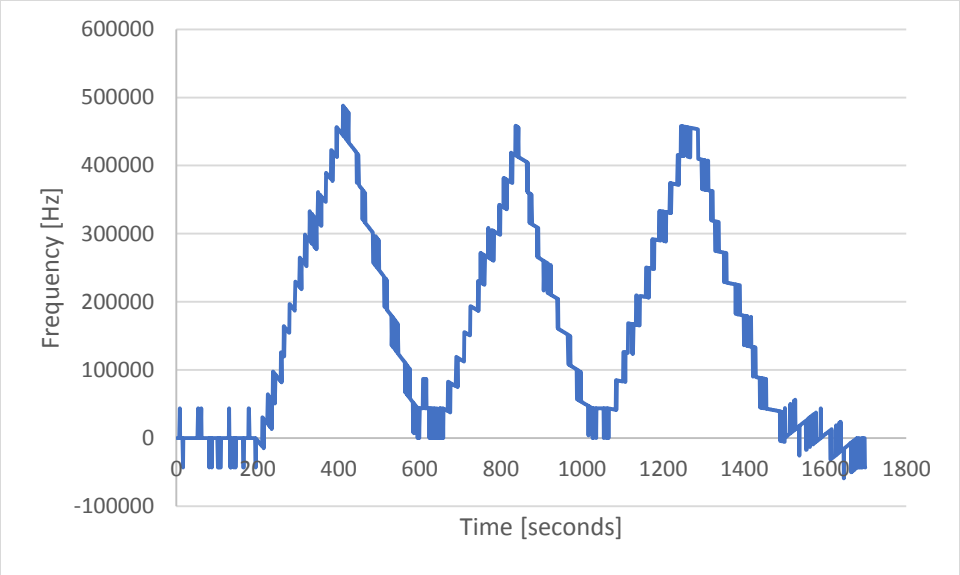

Figure 5-28: Repeatability test

The limit of detection (LOD) was extracted by plotting the sensors response and fitting the points. The noise floor was extracted from the BSL deviation to be ~14kHz [107]. When the signal-to-noise ratio (SNR) is approximately 3 the signal is pure, this is the criterion used in this work to determine the LOD [108]. The extracted LOD is shown in figure 5-29 to be ~ 1ppm, lower than the previous demonstrator of the thiourea monolayer for cyclohexanone detection.

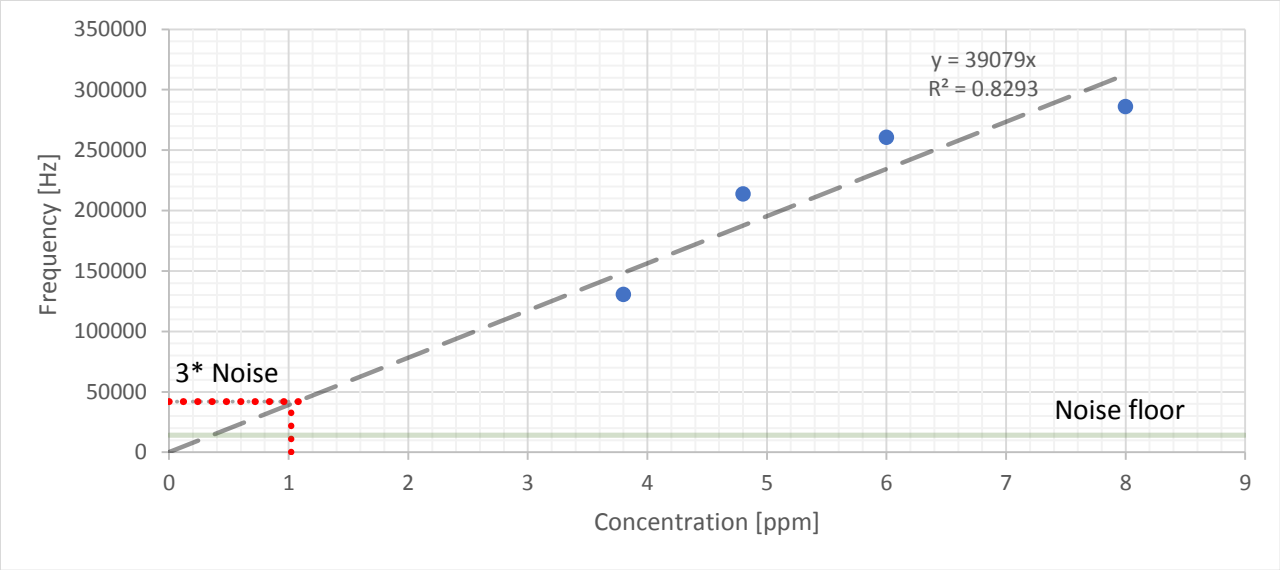

Figure 5-29: Limit of detection extraction

Chapter 6 **: Conclusion and Future Work**

This thesis goes through the development and implementation of a post-fabrication process flow for the monolithic integration of piezoelectric RF SMR and FBAR devices directly on CMOS dies. The devices were first fabricated on glass for the characterization and modeling by measuring the S-parameters. Three CMOS substrates were designed on IBM's 180nm and TSMC's 65nm technologies. The oscillator circuits were designed using the extracted electrical model of the devices on glass.

The 180nm chip was used as the main process development substrate due to its many test circuits that allowed for testing before and after processing for quick debugging thermal and electro-static discharge (ESD) limitations. It also added an extra challenge of requiring pad protection for pad mechanical integrity which the current controlled pierce 65nm did not have it due to pre-emptive designing from learning of previous mistakes on the 180nm. The 65nm served as a BAW-CMOS demonstrator. Using the developed process flow the project evolved into finding applications for these low power, high quality and small size systems.

After integrating the SMR a membrane supported structure, known as FBAR, was developed and demonstrated as well on CMOS. The FBAR served another purpose, due to its lower thermal mass compared to the SMR and higher TCF the device was coated with an IR absorber layer for functionalizing the system as an uncooled IR sensor. This application was tested using a 650nm wavelength laser.

The final chip was designed on TSMC 65nm, based on the previous current controlled pierce chip implemented a reprogrammable design for a lower power and higher FOM output. The chip has three fabrication sites, one stand-alone and two for pierce oscillator connections to be used in

sensing applications where one device is the reference and the other is functionalized as a detector. This design added frequency counters for the correct simultaneous monitoring of the frequency shifts. The pads on this chip were not protected. From the previous 65nm we learned there is no aluminum (Al) metallization for wire bonding in unexposed pads, using the techniques developed from the 180nm the fabrication was finalized without much pad degradation.

In parallel to the reprogrammable 65nm chip an RF PCB was designed in ADS for quick of testing of the SAM as a gas sensing coating. SMRs were fabricated on glass and diced into small pieces that were wire bonded to the PCB. To test its gas sensing capabilities a gas chamber was built for a dynamic flow environment. Both the PCB and the SAMs were demonstrated as a gas sensing system for the detection of VOCs with specifically high selectivity to cyclohexanone.

Contributions from this work are as follows:

- Designed different circuit topologies for testing the effects of post-fabrication and the monolithic integration of RF MEMS directly on top of circuitry.
- Development of small die (1.5mm x 1.5mm) handling techniques that enable multiple photolithography steps.
- Implemented a layout design on CMOS taking into consideration post-fabrication for both lithography steps and reducing surface roughness for higher quality passives.
- Characterized and reduced membrane stress and buckling for FBARs by compensating with a nitride support layer.
- Demonstrated and characterized monolithically integrated, the first SMR and FBAR devices on 65nm CMOS.

- First demonstration of an integrated uncooled IR resonant sensor. Using a nitride coating to improve over the ZnO's high TCF for a high sensitivity NIR detector.
- Design of a low power integrated sensing IC with a reprogrammable RF pierce oscillator core and the synthesis of a 3GHz frequency counter and scan chain for the readout.
- Demonstration of thiourea SAM on SMR using an RF PCB for VOC detection.

6.1 Future Work

6.1.1 Reprogrammable IC testing and characterization

Due to time restrictions and cleanroom logistics, the testing of the new reprogrammable 65nm CMOS chip was not completed. Devices were fabricated on the chip and the scan chain was tested for correct operation of sending control bits. The stand-alone showed the frequency was lower than what was expected, and the Rm is higher than what the circuit was designed for ~15ohms. This points to ZnO being more metallic than expected, with a slower acoustic velocity and higher conductivity, with further tooling and increasing the oxygen content, the crystallinity can be improved and be integrated with the chip for sensing applications.

6.1.2 IR sensing

The IR coating used in this work was Si_3N_4 which has an absorbance of 10% in the NIR, using other coatings such as TiN might provide for greater frequency shifts and higher extracted TCFs. A new setup should be built with a highly focused and power laser with wavelengths over 750nm for true IR testing.

6.1.3 Gas sensing

The current gas chamber is very susceptible to humidity and temperature changes. Adding sample heating or temperature control as well as pressure and temperature monitoring might simplify future testing and allow for a lower LOD. As with the IR coatings, other monolayer coatings with different VOC selectivity should be tested. With optimization of the gas lines and monitoring the chamber parameters the response time can also be improved.

6.2 Final thoughts

With the fabrication techniques and systems developed here for BAW-CMOS integration and sensing there is a future for these devices in the IoT. With intense and deeper characterization of the sensing films and the reprogrammable 65nm IC an array of sensors with different sensitivities can be built in a small area.

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