

# High Performance Local Oscillator Design for Next Generation Wireless Communication

Tsung-Hao (Jeffrey) Chuang

Submitted in partial fulfillment of the  
requirements for the degree  
of Doctor of Philosophy  
in the Graduate School of Arts and Sciences

**COLUMBIA UNIVERSITY**

2018

©2018

Tsung-Hao (Jeffrey) Chuang

All Rights Reserved

# ABSTRACT

## High Performance Local Oscillator Design for Next Generation Wireless Communication

Tsung-Hao (Jeffrey) Chuang

Local Oscillator (LO) is an essential building block in modern wireless radios. In modern wireless radios, LO often serves as a reference of the carrier signal to modulate or demodulate the outgoing or incoming data. The LO signal should be a clean and stable source, such that the frequency or timing information of the carrier reference can be well-defined. However, as radio architecture evolves, the importance of LO path design has become much more important than before. Of late, many radio architecture innovations have exploited sophisticated LO generation schemes to meet the ever-increasing demands of wireless radio performances.

The focus of this thesis is to address challenges in the LO path design for next-generation high performance wireless radios. These challenges include (1) Congested spectrum at low radio frequency (RF) below 5GHz (2) Continuing miniaturization of integrated wireless radio, and (3) Fiber-fast ( $>10\text{Gb/s}$ ) mm-wave wireless communication.

The thesis begins with a brief introduction of the aforementioned challenges followed by a discussion of the opportunities projected to overcome these challenges.

To address the challenge of congested spectrum at frequency below 5GHz, novel radio architectures such as cognitive radio, software-defined radio, and full-duplex radio have drawn significant research interest. Cognitive radio is a radio architecture that opportunistically utilize the unused spectrum in an environment to maximize spectrum usage efficiency. Energy-efficient spectrum sensing is the key to implementing cognitive radio. To enable energy-efficient spectrum sensing, a fast-hopping frequency synthesizer is an essential build-

ing block to swiftly sweep the carrier frequency of the radio across the available spectrum. Chapter 2 of this thesis further highlights the challenges and trade-offs of the current LO generation scheme for possible use in sweeping LO-based spectrum analysis. It follows by introduction of the proposed fast-hopping LO architecture, its implementation and measurement results of the validated prototype. Chapter 3 proposes an embedded phase-shifting LO-path design for wideband RF self-interference cancellation for full-duplex radio. It demonstrates a synergistic design between the LO path and signal to perform self-interference cancellation.

To address the challenge of continuing miniaturization of integrated wireless radio, ring oscillator-based frequency synthesizer is an attractive candidate due to its compactness. Chapter 4 discussed the difficulty associated with implementing a Phase-Locked Loop (PLL) with ultra-small form-factor. It further proposes the concept sub-sampling PLL with time-based loop filter to address these challenges. A 65nm CMOS prototype and its measurement result are presented for validation of the concept.

In shifting from RF to mm-wave frequencies, the performance of wireless communication links is boosted by significant bandwidth and data-rate expansion. However, the demand for data-rate improvement is out-pacing the innovation of radio architectures. A  $>10\text{Gb/s}$  mm-wave wireless communication at 60GHz is required by emerging applications such as virtual-reality (VR) headsets, inter-rack data transmission at data center, and Ultra-High-Definition (UHD) TV home entertainment systems. Channel-bonding is considered to be a promising technique for achieving  $>10\text{Gb/s}$  wireless communication at 60GHz. Chapter 5 discusses the fundamental radio implementation challenges associated with channel-bonding for 60GHz wireless communication and the pros and cons of prior arts that attempted to address these challenges. It is followed by a discussion of the proposed 60GHz channel-bonding receiver, which utilizes only a single PLL and enables both contiguous and non-contiguous channel-bonding schemes.

Finally, Chapter 6 presents the conclusion of this thesis.

# Table of Contents

<b>List of Figures</b>	<b>v</b>
<b>List of Tables</b>	<b>xi</b>
<b>Acknowledgements</b>	<b>xii</b>
<b>1 Introduction</b>	<b>1</b>
1.1 Challenge I: Extremely Congested Spectrum at Low-RF Frequency . . . . .	2
1.1.1 Local Oscillator Generation Technique for Sweeping-LO-based Spectrum- Sensing in Cognitive Radio Applications . . . . .	3
1.2 Challenge II: Miniaturization of Form-factor of Wireless Radios . . . . .	6
1.2.1 LO-Path Design for Wideband RF Self-Interference Cancellation for full-duplex wireless communication . . . . .	6
1.2.2 Ultra-low-form-factor, Low-Noise PLL Design . . . . .	7
1.3 Challenge III: Fiber-fast ( $>10\text{Gb/s}$ ) Wireless Communication for Emerging Applications . . . . .	9
<b>2 RF Instantaneous-hop Frequency Synthesizer for Energy-Efficient Spec- trum Sensing in Cognitive Radios</b>	<b>12</b>
2.1 Overview . . . . .	12
2.2 Conventional Fast-hopping LO Generation Technique . . . . .	13
2.2.1 Analog Charge-pump PLL-based Frequency Synthesizer . . . . .	13

2.2.2	All-Digital PLL . . . . .	15
2.2.3	Single-sideband Mixing-based LO Generation . . . . .	16
2.2.4	Direct-digital Frequency Synthesis . . . . .	17
2.3	Prior-Arts . . . . .	18
2.4	Concept of Proposed Zero-Initial-Phase-Error [1] . . . . .	18
2.5	Proposed 4.0-5.84 GHz Instantaneous-Hop PLL . . . . .	22
2.6	Measurement Result . . . . .	26
2.6.1	VCO Measurement . . . . .	27
2.6.2	PLL Locked-spectrum and phase noise measurement . . . . .	27
2.6.3	PLL Hopping Measurement . . . . .	28
2.6.4	Performance comparison . . . . .	30
2.7	Conclusion and Future Work . . . . .	31
<b>3</b>	<b>Embedded Phase-shifting LO-Path Design for Wideband RF Self-Interference Cancelling Receiver</b>	<b>35</b>
3.1	Introduction . . . . .	35
3.2	Challenges of Self-Interference Cancellation for FDD and Full-Duplex Radio	36
3.3	N-path-Filter-Based Wideband RF Self-Interference Cancellation . . . . .	39
3.4	Design Consideration for LO-Path Phase Shifter Design . . . . .	41
3.5	Proposed LO-Path Design for the N-path-Filter-Based Self-Interference Canceller . . . . .	42
3.6	Simulation Result of the Proposed LO Path Design . . . . .	42
3.7	65nm CMOS Radio Prototype and Highlighted System-level Measurement Result [2] . . . . .	45
3.8	Conclusion and Future Work . . . . .	46
<b>4</b>	<b>Design of Ultra-low Form-factor and Low-noise Ring Oscillator-based PLL</b>	<b>54</b>
4.1	Introduction . . . . .	54
4.2	Pathway to low-noise and ultra-compact PLL Implementation . . . . .	59

4.2.1	Dual-path PLL Architecture . . . . .	59
4.2.2	Dual-path PLL with Time-based Active Loop Filter Architecture . .	62
4.2.3	Proposed Sub-sampling Dual-path PLL with Time-based Loop Filter Architecture [3] . . . . .	62
4.3	Phase Noise Analysis of Proposed Architecture . . . . .	63
4.4	A 65nm CMOS Implementation . . . . .	67
4.4.1	Block Diagram of Proposed PLL . . . . .	67
4.4.2	Time-domain Operation of Proposed PLL . . . . .	70
4.5	Measurement Results . . . . .	72
4.5.1	Oscillator Measurement . . . . .	72
4.5.2	PLL Measurement . . . . .	73
4.6	Conclusion and Future Work . . . . .	80
<b>5</b>	<b>Fully-Integrated 60GHz Channel-Bonding Receiver with IF Channeliza- tion Supporting Flexible Bonding Scheme</b>	<b>81</b>
5.1	Introduction . . . . .	81
5.1.1	Fiber-fast mm-wave Wireless Communication . . . . .	82
5.1.2	60GHz Multi-Gb/s Wireless Communication . . . . .	83
5.1.3	Emerging IEEE 802.11ay Standard: Towards 100Gb/s . . . . .	85
5.2	60GHz Channel-Bonding for 802.11ay: Opportunities and Implementation Challenges . . . . .	86
5.2.1	Opportunities for Channel-Bonding at 60GHz . . . . .	86
5.2.2	Challenge I: High-speed Baseband ADC Design . . . . .	88
5.2.3	Challenge II: LO Tuning-range . . . . .	91
5.2.4	Challenge III: Calibration . . . . .	94
5.3	Prior-Arts . . . . .	96
5.4	Proposed Single-PLL Fully-integrated 60GHz Channel-bonding Receiver Ar- chitecture . . . . .	97

5.4.1	Proposed Single-Element Fully-Integrated mm-wave Receiver Front- End for 60GHz Channel-Bonding . . . . .	98
5.4.2	Proposed Shared-LO IF Channelizer with Harmonic Channel-Selectivity	99
5.4.3	Proposed Single LO Frequency Generation Scheme . . . . .	101
5.5	System-level Specification Requirement Analysis . . . . .	103
5.5.1	Analysis of Link Budget . . . . .	103
5.5.2	Image-Rejection-Ratio (IMRR) Requirement . . . . .	104
5.5.3	Harmonic-Rejection-Ratio (HRR) Requirement . . . . .	104
5.6	Implementation of Local Oscillator Path for the Proposed 60GHz Channel- Bonding Receiver . . . . .	105
5.7	Simulation Result . . . . .	106
5.7.1	20GHz PLL and 1GHz DLL . . . . .	106
5.7.2	IF Channelizer and Harmonic Rejection Mixer . . . . .	107
5.8	45nm CMOS SOI Prototype . . . . .	108
5.9	Conclusion and Future Work . . . . .	111
<b>6</b>	<b>Conclusion</b>	<b>112</b>
	<b>Bibliography</b>	<b>114</b>

# List of Figures

1.1	Survey and predicted number of connected devices from 2014 to 2022. (source: Ericsson Mobility Report 2017)	2
1.2	Survey of mobile data traffic over the past five years. (Source: Ericsson Mobility Report 2017)	3
1.3	Spectrum allocation chart in the US [4].	4
1.4	Overall plot of 24-hour maximum spectrum usage measured over six days in Brno, Czech Republic [5].	5
1.5	(a) General front-end architecture for CR (b) Synthesizer-based spectrum sensing for CR front-end.	5
1.6	Separation of transmission and reception in (a) time (TDD) or (b) frequency (FDD). (c) simultaneously transmit and receive at the same frequency (Full-duplex) [2].	6
1.7	Cost per unit area and per transistor from 130nm to 10nm CMOS technology. (source: 2014 Intel Developer Forum)	7
1.8	Modern SoC architectures for microprocessors [6] and wireless radios [7].	8
1.9	Worldwide frequency allocation at 60GHz [8].	9
1.10	Emerging applications for high data-rate wireless communications.	10
2.1	Conventional analog charge-pump PLL.	13
2.2	Architecture for AD-PLL.	15
2.3	Architecture for SSB LO generation.	16
2.4	Schematic of DDFS system.	17

2.5	(a) Analog integer-N PLL (b) All-digital PLL (c) Single-sideband mixing LO generation (d) Direct digital frequency synthesis (DDFS) technique. . . . .	18
2.6	Survey of locking time vs. power consumption for recently published fast-hopping LO generation works. . . . .	19
2.7	(a) PLL with a binary-sequence counter-based divider. (b) Mechanism of initial phase error in the counter-based divider. . . . .	20
2.8	(a) Multi-modulus divider first: no initial state control is necessary in the fixed-ratio divider that follows. (b) Fixed-ratio divider first: initial state control is required throughout the chain. . . . .	21
2.9	Proposed zero-initial-phase-error divider structure. . . . .	22
2.10	Potential initial phase error in the proposed divider structure for upward and downward hops. . . . .	23
2.11	4.0-5.84 GHz instantaneous-hop PLL block diagram. . . . .	24
2.12	4.0-5.84 GHz 9-bit digitally-controlled LC-VCO with analog varactor tuning. . . . .	25
2.13	Instantaneous frequency vs. time for different hop instants in (a) a conventional PLL using divide-by-2/3 asynchronous dividers, and (b) a proposed instantaneous-hop PLL. (c) Maximum dynamic frequency error vs. hop instant in both cases. . . . .	26
2.14	(a) Photo of the board assembly for testing purposes (b) Chip micro-photograph. . . . .	27
2.15	Measured 4.0-5.84 GHz 9-bit LC-VCO performance at $V_{ctrl} = 0.6V$ vs. DCW: (a) frequency (b) $K_{VCO}$ (c) frequency difference between two successive DCW (d) single-band frequency coverage as $V_{ctrl}$ is varied from 0-1.2V. . . . .	28
2.16	(a) Spectrum of the measured PLL at 4.24GHz (b) Phase noise profile of the measured PLL at 4.24GHz. . . . .	29
2.17	(a) Spectrum of the measured PLL at 5.08GHz (b) Phase noise profile of the measured PLL at 5.08GHz. . . . .	29
2.18	Block diagram of proposed PLL transient hopping measurement setup. . . . .	30

2.19	Measured (a) control voltage and (b) instantaneous output frequency for a hop from 4.644 GHz to 4.24 GHz showing a maximum dynamic frequency error of 850 kHz. Measured control voltage for upward and downward hops (maximum upward/downward dynamic frequency error) between (c) 4.136 GHz and 4.512 GHz (1.65MHz, 900kHz) (d) 4.24 GHz and 4.644 GHz (1.5MHz, 850kHz). The 4.664 to 4.24 GHz downward hop is a repeat of (a). . . . .	33
2.20	Proposed calibration engine for the proposed instantaneous-hop PLL. . . . .	34
3.1	Highlight of allocated spectrum at mm-wave frequencies [2]. . . . .	37
3.2	TX SIC in the RF domain for (a) a multiband FDD wireless system with a tunable duplexer and (b) an FD wireless system [2]. . . . .	38
3.3	Two-port $G_m - C$ N-path filter implementation with embedded variable attenuation and phase shift. (a) Block diagram. (b) Illustration of variable quality-factor (group delay), frequency shift, attenuation, and phase shift [2].	41
3.4	Block diagram and schematic of the proposed embedded phase-shifting LO path design. . . . .	43
3.5	(a) Ideal phase shift vs. simulated phase shift (b) Error between simulated phase shift and ideal phase shift from 0-45 degrees for the vector-modulator-based phase shifter. . . . .	45
3.6	(a) Post-layout simulation of duty-cycle vs. phase shift setting (b) Accuracy of non-overlapping generation between the differential I/Q signal from 0-45 degrees. . . . .	46
3.7	Simulated frequency response of the vector-modulator $G_m$ -cell. . . . .	47
3.8	Simulated rise and fall time for the output signals of both phase-shifting path and non-phase-shifting path. . . . .	48
3.9	Monte-Carlo simulation of the phase shifter at 45-degree phase shift setting under the impact of device mismatch. . . . .	49
3.10	Block diagram and schematic of the implemented 0.81.4 GHz 65 nm CMOS RX with FDE-based SIC in the RF domain featuring a bank of two filters [2].	50

3.11	Chip microphotograph of the 65 nm CMOS 0.81.4 GHz SI-canceling RX. . .	51
3.12	Custom-designed LTE-like 0.780/0.895 GHz duplexer employing surface-mount-device-based second-order LC filters: (a) schematic; (b) duplexer photo; (c) measured duplexer insertion loss; and (d) measured duplexer TX/RX isolation magnitude and phase response [2]. . . . .	52
3.13	Measured TX/RX isolation of the FDD LTE-like duplexer shown in Fig. 3.12 without SIC, and with the proposed SIC. The proposed SI canceller achieves a 20 dB cancellation BW of 17/24 MHz for one/two filters enabled, while a conventional frequency-flat amplitude- and phase-based canceller has a theoretical 20 dB SIC BW of only 3 MHz [2]. . . . .	53
4.1	Conventional ring-oscillator-based PLL architecture comparison: (a) Analog charge-pump PLL with passive loop filter. (b) Sub-sampling analog charge-pump PLL. (c) All-digital PLL. (d) Analog PLL with active loop filter. . . .	55
4.2	$FoM_J$ versus area for state-of-art ring-oscillator-based clock generation works.	57
4.3	(a) Generic dual-path PLL architecture. (b) Dual-path PLL with active time-based loop filter. (c) Proposed dual-path sub-sampling PLL with time-based loop filter. . . . .	60
4.4	(a) Phase-domain small-signal (phase) noise model for proposed PLL. (b) Phase-domain small-signal (phase) noise model for a dual-path PLL with active time-based loop filter (without sub-sampling). . . . .	61
4.5	Simulated comparison of conventional analog type-II 3rd-order PLL, PLL with active time-based loop filter (without sub-sampling), and the proposed PLL: (a) phase noise of the Keysight E8257D Analog Signal Generator 200MHz reference signal, the RF and the integrating ring oscillators, (c) closed-loop frequency response (b) noise transfer function of Integrating CCRO to the PLL output, and (d) overall phase noise with the contribution of highlighted noise sources. . . . .	66
4.6	Block diagram of the proposed PLL. . . . .	68

4.7	Schematics of various components in the proposed PLL: (a) 2.4 GHz 9-stage RF current-controlled ring oscillator (RF-CCRO), (b) sub-sampling phase detector, (c) V-to-I converter (gm-cell) for the sub-sampling path, (d) and charge pump for the time-based integrator path. . . . .	69
4.8	Time-domain operation for the proposed PLL. . . . .	70
4.9	Die micrograph. . . . .	72
4.10	Measured (a) tuning-range of RF-CCRO, (b) phase noise at 2.3GHz carrier frequency, and (c) phase noise at 1MHz offset versus carrier frequency. . . . .	73
4.11	Measured (a) tuning-range of the integrating-CCRO, and (b) phase noise at 200MHz carrier frequency. . . . .	75
4.12	PLL measurement with multiplication factor of 12 at 2.3GHz: (a) locked spectrum, and (b) phase noise vs. offset frequency. . . . .	76
4.13	PLL measurement of as a function of locked frequency (multiplication factor = 12): (a) jitter-FoM, and (b) reference spur level . . . . .	77
4.14	PLL measurement with multiplication factor of 48 at 2.3GHz: (a) locked spectrum, and (b) phase noise vs. offset frequency. . . . .	78
5.1	Highlight of FCC-allocated spectrum at mm-wave frequencies [9]. . . . .	83
5.2	Frequency allocation for IEEE 802.11ad standard (WiGig). . . . .	83
5.3	Modulation and coding scheme vs. data-rate for IEEE802.11ad standard. . . . .	84
5.4	Futuristic applications for high data-rate wireless communication. . . . .	86
5.5	Highlighted features for the upcoming IEEE 802.11ay specification and its amendment to the current IEEE 802.11ad standard. . . . .	87
5.6	Channel-bonding scheme for IEEE 802.11ay standard. . . . .	88
5.7	Survey of unit cost vs. sampling rate for commercial (Texas Instrument and Analog Device) ADC module. . . . .	89
5.8	Survey of FOM vs. $f_{sampling}$ for selected ADC published in the past 20 years [10]. . . . .	90

5.9	(a) Schematic of time-interleaved ADC architecture (b) Timing diagram of clock signal for time-interleaved ADC. . . . .	91
5.10	Highlight of mm-wave frequency generation techniques. . . . .	94
5.11	Conventional channel-bonding architecture [11]. . . . .	96
5.12	Proposed 60GHz channel-bonding architecture. . . . .	98
5.13	Proposed fully-integrated 60GHz channel-bonding receiver. . . . .	99
5.14	Proposed IF channelizer architecture. . . . .	100
5.15	Timing diagram of harmonic-rejection-based programmable LO generation technique. . . . .	101
5.16	Proposed 20GHz LO path design for the proposed 60GHz receiver. . . . .	102
5.17	Link budget analysis for the proposed 60GHz receiver. . . . .	104
5.18	(a) Image-rejection ratio vs. Amplitude and phase imbalance. (b) Harmonic-rejection ratio (HRR) vs. the error-to- $\sqrt{2}$ . . . . .	105
5.19	Proposed 20GHz LO path design for the proposed 60GHz receiver. . . . .	106
5.20	Simulated 20GHz VCO tuning-range . . . . .	107
5.21	a) Proposed PLL transient locking simulation (b) Proposed DLL transient simulation . . . . .	108
5.22	Simulated channel response for proposed IF channelizer. . . . .	109
5.23	Layout of proposed 60GHz channel-bonding receiver. . . . .	110

# List of Tables

2.1	Performance summary and comparison. . . . .	31
3.1	Breakdown of power consumption for the proposed embedded-phase-shifting LO path. . . . .	44
4.1	Design parameters for the PLL comparison in Fig. 4.5. . . . .	67
4.2	Performance summary and comparison. . . . .	79

# ACKNOWLEDGEMENTS

First and foremost, I would like to thank my advisor, Professor Harish Krishnaswamy, for his guidance over the years of my PhD study. Professor Krishnaswamy has provided me with support and resources at CoSMIC Lab. Despite the lightning fast speed of progress in our field of research, Professor Krishnaswamy has always supported us in solving fundamental and critical problems. As a student of his, I have learned to always challenge the status quo and not take anything for granted. It has been a precious experience to cultivate my research taste from working alongside Professor Krishnaswamy.

I would also like to thank Professor Yannis Tsividis, Professor Yves Baeyens, Professor Ioannis Kymissis, Professor Mingoo Seok, and Dr. Bodhisatwa Sadhu for serving on my thesis proposal and defense committee, for their valuable time spent on giving feedback on my thesis. I would also like to express my gratitude to Professor Peter Kinget for his help and feedback on my first research project and during my teaching assistantship in his course.

During my PhD career, I was fortunate to gain extensive working experience at various companies. I would like to thank Dr. Shahriar Shahramian and Dr. Ricardo Aroca (now with Acacia) at Nokia Bell Lab, Dr. Ken Suyama and Dr. Alexander Dec at Epoch Microelectronics, Director Arya Behzad (now with Broadcom), Dr. Albert Jerng, and Dr. Ehsan Adabi at Apple Inc. for providing me with such wonderful opportunities to learn and contribute.

I would also like to thank all my colleagues at Columbia, especially Ritesh Bhat, Linxiao Zhang, Jin Zhou, Tolga Dinc, Anandaroop Chakrabarti, and Jahnavi Sharma for their tremendous help over the years. It was a great pleasure to be a member of CoSMIC Lab and to be around with such sharp and brilliant minds.

I would also like to express my appreciation for all my friends in New York City and other places for their support over the years. Special thanks to the Lan family for their unconditional care and encouragement, my journey of pursuing a PhD would not have been possible without them.

Last but not least, I would like to thank my parents and brother. They have always encouraged me to be strong, positive, and courageous, and I am blessed and privileged to pursue my interests with their love.

# Chapter 1

## Introduction

The ever-increasing demands of mobile applications have driven radio design towards low-cost, low-power, high-performance, high-levels of integration, and towards the usage of the unexplored electromagnetic radio spectrum. As illustrated in Fig. 1.1, by 2020, the number of connected devices such as mobile phones, tablets, and short-range and long-range Internet-of-Things (IoT) devices will be over 25 billion [12]. Furthermore, the predicted traffic of data usage, as shown in Fig. 1.2, has grown exponentially over the last five years and this growth shows no sign of stopping.

Thanks to Moore's Law, the Complementary metaloxidesemiconductor (CMOS)-based integrated circuit has been favored over other technology over the last few decades. *To date, the opportunities and challenges of CMOS-based wireless radio design can be mainly categorized into*

- **Better usage of idle and unexplored spectrum.**
- **Miniaturization of form-factor of wireless radios.**
- **Achieving fiber-fast wireless communication for emerging applications.**

Local Oscillator (LO) is an essential building block in modern wireless radios. In modern wireless radios, LO often serves as a reference of carrier signal to modulate or demodulate

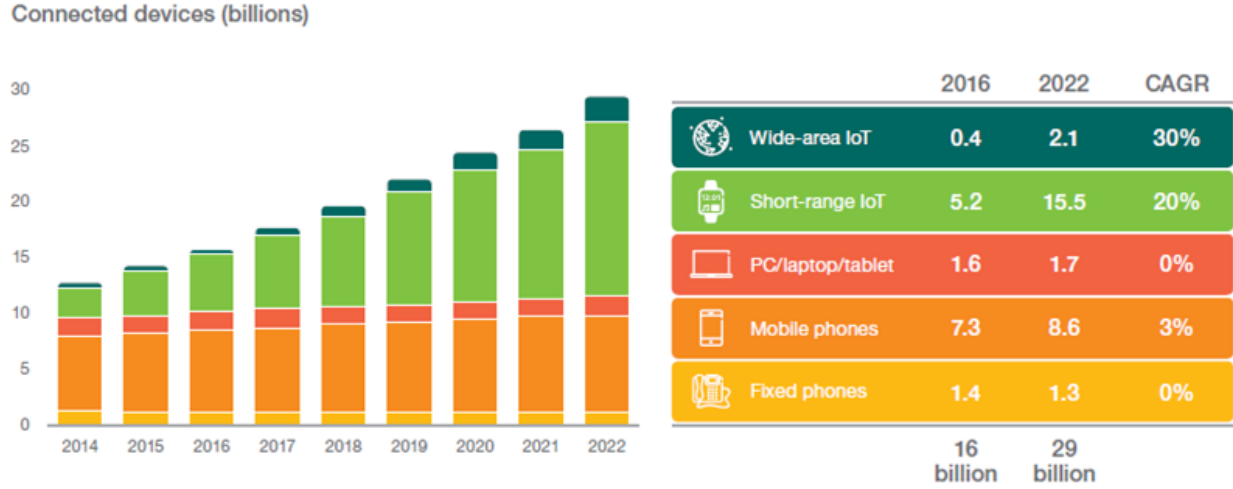


Figure 1.1: Survey and predicted number of connected devices from 2014 to 2022. (source: Ericsson Mobility Report 2017)

the outgoing or incoming data. The LO signal should be a clean and stable source such that the frequency or timing information of the carrier reference can be well-defined. However, as radio architecture evolves, the importance of LO path design has become much more important than before. Of late, many radio architecture innovations exploited sophisticated LO generation schemes to meet the ever-increasing demand on wireless radio performances. *The goal of this thesis is to address the topic of LO path design in these novel integrated wireless radio architectures.* The following sections further highlight the opportunities and challenges in recent wireless radio developments.

## 1.1 Challenge I: Extremely Congested Spectrum at Low-RF Frequency

Fig. 1.3 shows spectrum allocation in the US as of January 2016. The available spectrum is considered a limited natural resource, which is becoming extremely congested due to the explosive growth of mobile devices. Between 300MHz and 3GHz specifically, almost all the available spectrum has been assigned and any unused licensed band in this frequency range

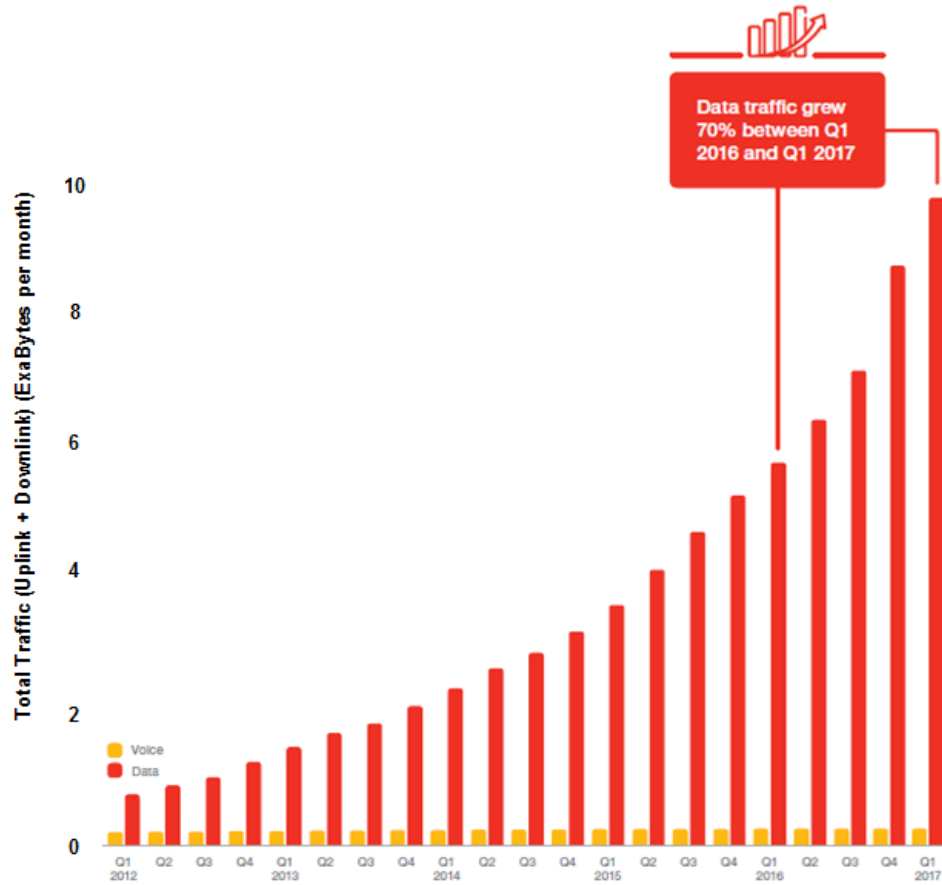


Figure 1.2: Survey of mobile data traffic over the past five years. (Source: Ericsson Mobility Report 2017)

is extremely valuable due to its rarity.

### 1.1.1 Local Oscillator Generation Technique for Sweeping-LO-based Spectrum-Sensing in Cognitive Radio Applications

Although the spectrum shown in Fig. 1.3 appears incredibly crowded at first glance, it is not in use at all times. Fig. 1.4 provides an example of uneven spectrum usage over a meaningful period of time. As can be seen, most of the spectrum are idle. Dynamic spectrum access [13, 14] is a technique that allows unlicensed users (or so called "secondary



analysis in an energy-efficient manner, meaning that dynamic action such as LO-sweeping must be as quick as possible, so that overall power consumption can be minimized.

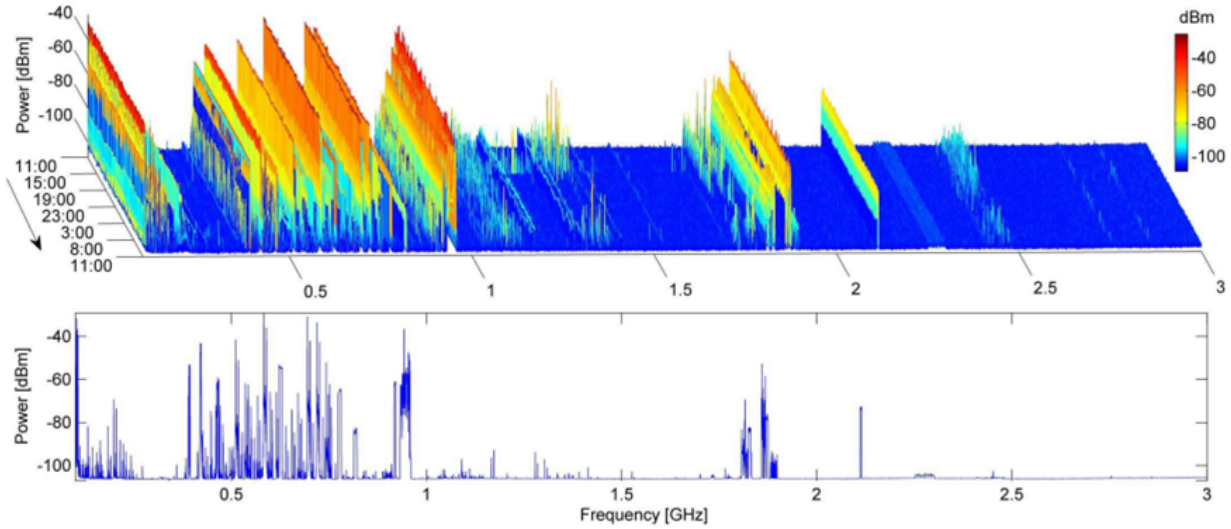


Figure 1.4: Overall plot of 24-hour maximum spectrum usage measured over six days in Brno, Czech Republic [5].

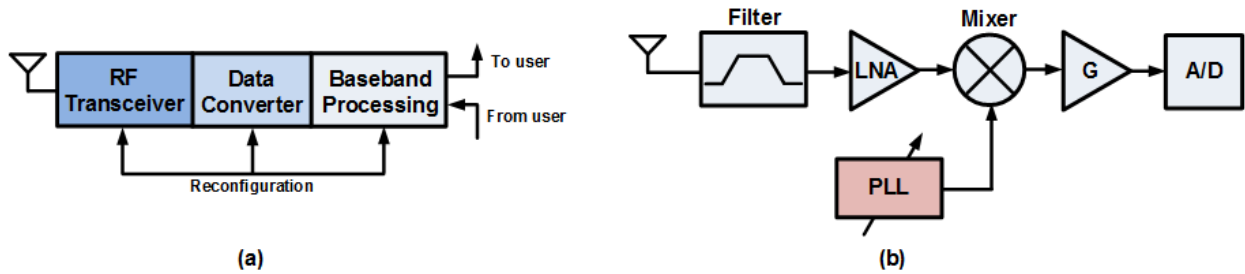


Figure 1.5: (a) General front-end architecture for CR (b) Synthesizer-based spectrum sensing for CR front-end.

Chapter 2 further highlights the challenges and design trade-offs of an LO generation scheme for LO-sweeping based spectrum analysis. It is followed by the introduction of the proposed fast-hopping LO architecture, its implementation and the measurement result of the validated prototype.

## 1.2 Challenge II: Miniaturization of Form-factor of Wireless Radios

### 1.2.1 LO-Path Design for Wideband RF Self-Interference Cancellation for full-duplex wireless communication

Modern radio design often incorporates numerous off-chip duplexers to support multi-band frequency-division duplexing (FDD) operations. FDD allows multiple users to access the spectrum with allocated channels such that their information will not interfere with the information of other users. Off-chip tuned duplexers are bulky and costly. Recently, there have been many research effort aiming at replacing the bulky tuned duplexers with tunable solutions or even integrated solutions. Full-duplex (FD) radio is another topic that has drawn a lot of research interests of late. Both FDD and FD radios, shown in Fig. 1.6, require significant self-interference cancellation.

Chapter 3 proposes an embedded phase-shifting LO-Path design for wideband RF self-interference cancellation. It demonstrates a synergistic design between the LO path and signal in performing self-interference cancellation.

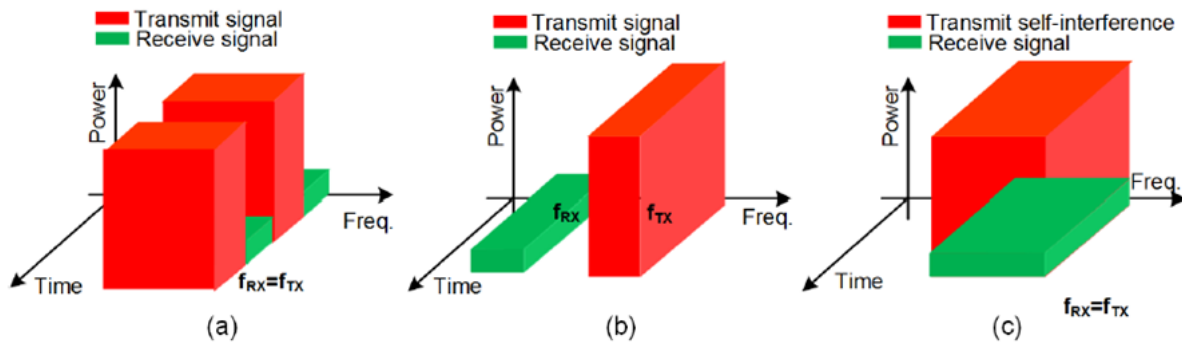


Figure 1.6: Separation of transmission and reception in (a) time (TDD) or (b) frequency (FDD). (c) simultaneously transmit and receive at the same frequency (Full-duplex) [2].

## Cost per Transistor

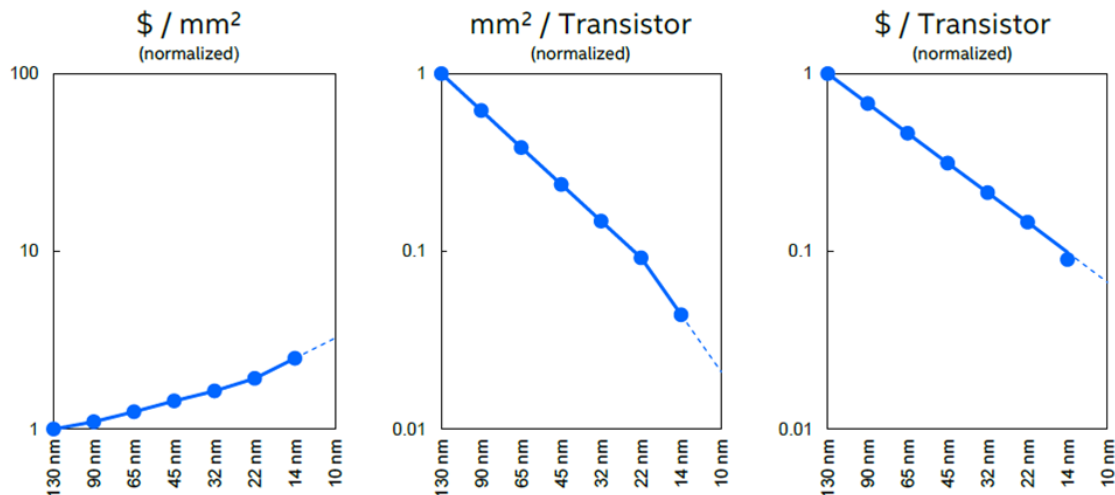


Figure 1.7: Cost per unit area and per transistor from 130nm to 10nm CMOS technology. (source: 2014 Intel Developer Forum)

### 1.2.2 Ultra-low-form-factor, Low-Noise PLL Design

For radio frequency integrated circuit designers, passive components are crucial to design building blocks, which include oscillators, PLLs, amplifiers, filters, or even just interconnections. As shown in Fig. 1.7, in advanced nodes, wafer cost increases while the cost-per-gate decreases. This means that the usage of passives in RFIC design comes at the cost of increasing the number of transistors or gates.

Phase-locked loop (PLL) is the predominant method for on-chip LO generation. The technology used in modern PLLs is vastly different from what was used when the PLL was first invented. The simplicity of the idea of a PLL, using a negative feedback loop to lock the phase of a free-running oscillator, makes it a popular choice for LO generation over time. As shown in Fig. 1.8, modern digital system-on-chip (SoC) and multi-band multi-mode radios require multiple PLLs. As cost per unit area of advanced CMOS technology increases, there is a need to miniaturize the area of PLLs without not sacrificing jitter and phase noise performance.

Ring oscillators are a popular choice for on-chip oscillators since they are compact and can

be easily tuned. Recently, in wireless radios, circuit techniques enabling ring oscillator-based PLLs to generate clean LO signal that are compatible with various wireless standards have attracted significant research interests [19–22]. As the ring oscillator-based PLL manifests itself as an attractive and feasible candidate across domains of application, pathway to further reduce area of ring oscillator-based PLLs have become a crucial topic.

Chapter 4 discusses the challenge associated with the implementation of PLLs with an ultra small form-factor. It further proposes the concept of sub-sampling PLLs with a time-based loop filter to address these challenges and presents a 65nm CMOS prototype and measurement results for validation of this concept.

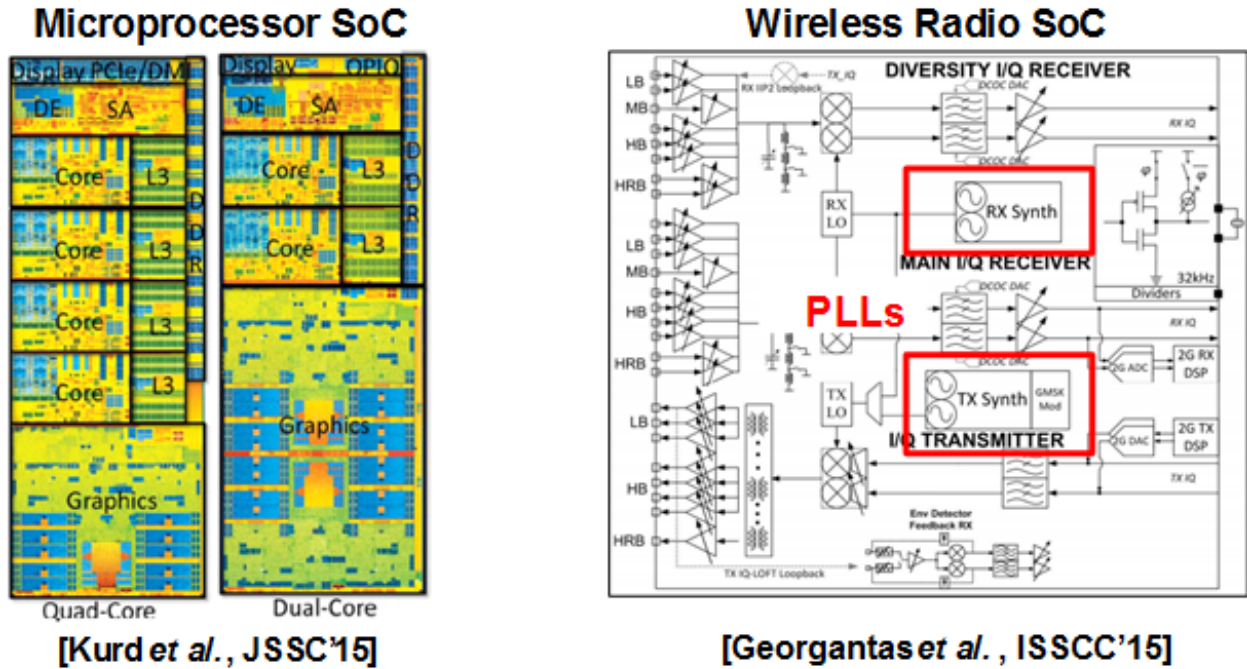


Figure 1.8: Modern SoC architectures for microprocessors [6] and wireless radios [7].

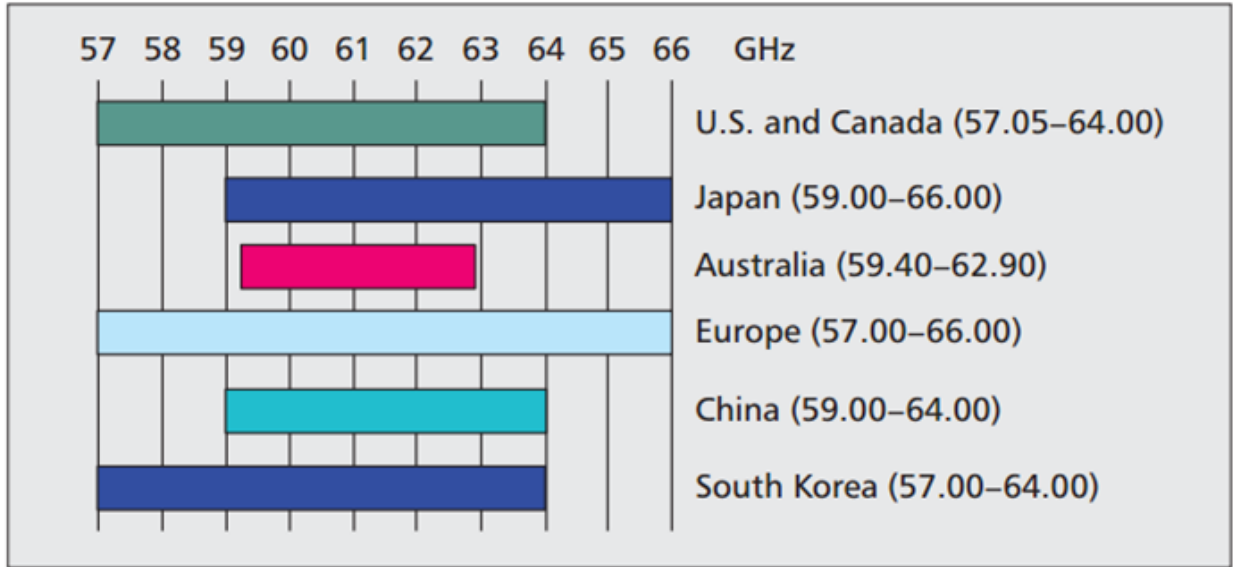


Figure 1.9: Worldwide frequency allocation at 60GHz [8].

### 1.3 Challenge III: Fiber-fast ( $>10\text{Gb/s}$ ) Wireless Communication for Emerging Applications

It is predicted that utilizing mm-wave frequencies could be another or perhaps the most promising solution to the aforementioned congested spectrum challenge below 5GHz. Based on Shannon's Theorem, channel capacity of a communication channel or data link is directly proportional to the bandwidth of the channel and the signal-to-noise ratio (SNR) of the link. By shifting to carriers at mm-wave frequencies, the available bandwidth for data transmission increases naturally. In addition, the form-factor of most the passive components is directly proportional to the wavelength of the signal traveling through them. Moving to mm-wave frequencies will inherently lower form-factor of the radio, thereby lowering cost. The scaling of CMOS technology has significantly increased the speed of the transistor such that CMOS can as well be an suitable candidate for producing radios at mm-wave frequencies. For this reason, a plethora of emerging and/or existing commercial applications such as 5G communication, wireless backhaul, short/mid-range point-to-point communication, and vehicular radars have all targeted the deployment CMOS-technology-based products for mass

production.

Among the mm-wave frequency bands of interest, the 60GHz band offers unprecedented opportunities for short/mid-range wireless personal area networks such as those in home entertainment systems. Recently, IEEE 802.11ad, Wireless Gigabit Alliance (WiGig), specification has been included by the Wi-Fi Alliance as part of next-generation Wi-Fi protocol[23]. The WiGig standard allocates four 2.16GHz wide channels centering at 58.32GHz, 60.48GHz, 62.64GHz, and 64.80GHz. For single-carrier (SC) operation, up to 16-QAM modulation can be supported by the radio. For Orthogonal Frequency-Division Multiplexing (OFDM) operation, up to 64-QAM modulation can be supported. SC 16-QAM operation can achieve up to 4.62 Gb/s while OFDM 64-QAM operation can achieve up to 6.76 Gb/s. Although this may appear sufficient for current commercial applications such as streaming high-definition TV (HDTV) or high-speed high-volume file transferring, emerging applications demand even higher wireless communication data-rates.

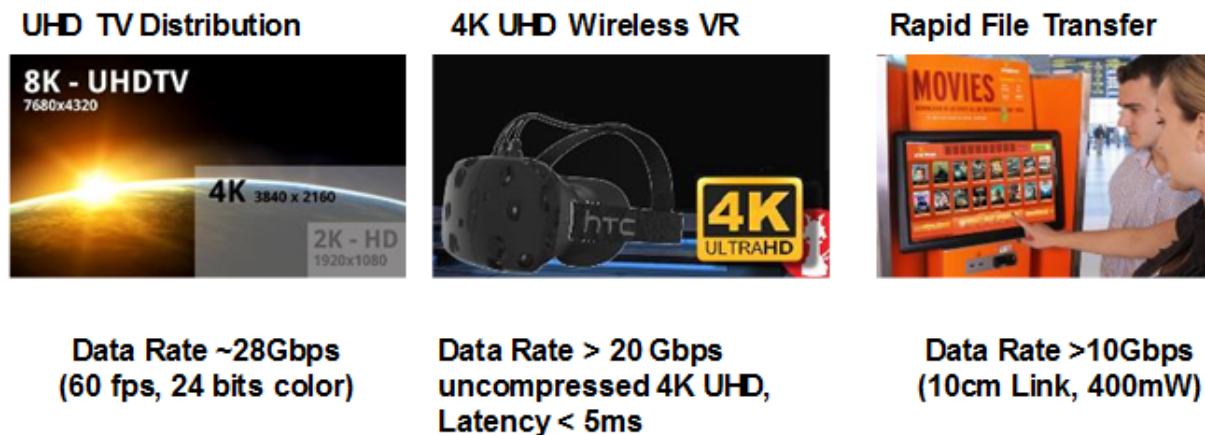


Figure 1.10: Emerging applications for high data-rate wireless communications.

These emerging applications include, among others, un-compressed Ultra-High-Definition (UHD) TV and, Wireless Virtual-Reality (VR), as shown in Fig. 1.10. The required data-rates for these applications are beyond 10 Gb/s and exceed the peak data-rate that the current IEEE 802.11ad (or WiGig) standard can support. For this reason, an upcoming specification, IEEE 802.11ay, has been proposed as an enhancement to the current 802.11ad

standard, targeting data-rate transmission of over 40 Gb/s over a 100-meter range. To support these specifications, it is expected that advanced techniques such as channel-bonding, multi-user multi-input-multi-output (MU-MIMO), and advanced modulation schemes such as 256-QAM be applied.

Chapter 5 discusses the fundamental challenges associated with channel-bonding scheme for 60GHz radio, and the prior-arts that attempted to address these issues. It also discusses the proposed 60GHz channel-bonding receiver, which requires only a single PLL and enables both contiguous and non-contiguous channel-bonding schemes.

## Chapter 2

# RF Instantaneous-hop Frequency Synthesizer for Energy-Efficient Spectrum Sensing in Cognitive Radios

### 2.1 Overview

This chapter begins with a brief discussion of the conventional fast-settling/hopping LO generation scheme with a focus on its advantages and disadvantages for sweeping-LO-based spectrum analysis in CR applications. Following a brief discussion, a zero initial phase error concept for PLL feedback loop settling is introduced. Subsequently, an instantaneous-hop frequency synthesizer architecture featuring a zero-initial-phase-error divider is proposed. An implementation of 65nm CMOS prototype and its validated measurement result are also discussed. The chapter concludes with a discussion of possible future research directions.

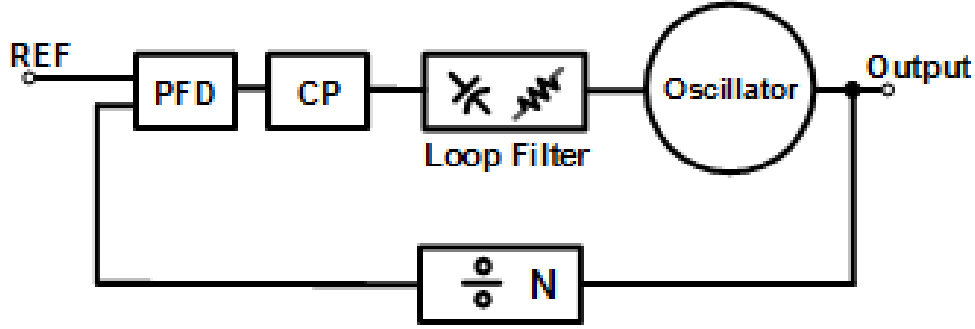


Figure 2.1: Conventional analog charge-pump PLL.

## 2.2 Conventional Fast-hopping LO Generation Technique

The conventional LO generation scheme can be briefly categorized into four architectures, namely the analog integer-N PLL-based frequency synthesizer, all-digital PLL, single-sideband-mixing-based LO generation, and direct-digital frequency synthesis (DDFS).

### 2.2.1 Analog Charge-pump PLL-based Frequency Synthesizer

The analog charge-pump PLL-based frequency synthesizer, shown in Fig. 2.1, has been the predominant method of on-chip LO generation due to its simplicity [24–26]. A low-frequency clean reference signal is introduced into the PLL to compare its phase with the frequency-divided version of the high-frequency noisy on-chip oscillator. The negative-feedback nature of the loop ensures that within the loop bandwidth of the PLL, phase errors or phase noise of the high-frequency oscillator are corrected by the clean reference signal. Due to its simplicity, analog PLL has been employed in a wide range of applications from clock synthesis for digital circuitry, clock generation for data converters, and LO design for wireless radios.

Settling time is an important metric for evaluating PLL performance. It is fairly straightforward to derive that the energy consumption for a CR to perform a sweeping-LO-based spectrum analysis is directly proportional to the settling of the PLL. Therefore, it is essential to shorten the settling time of the PLL from a loop design perspective.

For an analog charge-pump PLL, the settling time of the loop is inversely proportional to its loop bandwidth. Larger loop bandwidth results in shorter settling time and sharper in-band voltage-controlled oscillator (VCO) phase noise rejection. However, larger loop bandwidth also leads to weaker reference spurs and reference or other loop components' phase noise attenuation at out-of-band frequencies. In addition, loop bandwidth cannot be indefinitely widened due to the issues of stability. Typically, the loop bandwidth of a mixed-signal PLL is limited to 1/10 or even 1/20 reference frequency such that the continuous-time approximation for phase-domain stability analysis holds. For a given settling time, the minimum loop bandwidth,  $f_c$ , required can be expressed as [27]

$$f_c = \frac{1}{t_{lock}\xi(\phi_m)} \ln \frac{f_{step}}{f_{error}} \quad (2.1)$$

where  $t_{lock}$  is the required settling time,  $\xi(\phi_m)$  is the effective damping ratio for given phase margin,  $f_{step}$  is the frequency difference of hop, and  $f_{error}$  is the tolerable frequency error. For instance, for a loop with a phase margin of 50deg, which corresponds to a  $\xi(\phi_m)$  of five, settling error of 48kHz (20ppm at 2.4GHz), and frequency jump of 20MHz, the required open loop bandwidth,  $f_c$ , to achieve 100ns locking time is 12MHz. As previously mentioned, for a PLL to achieve a bandwidth of 12MHz, the reference frequency must be 120MHz or larger. For mobile applications, a crystal oscillator (XO) is typically employed to generate the reference frequency. Finding a cost-effective XO at 120MHz can be challenging. Also, a reference frequency of 120MHz mandates the need for adopting fraction-N PLL architecture to generate a step frequency (e.g.:20MHz), typically governed by channel-spacing in radio design, that is finer than the reference frequency itself.

The above example highlights the difficulty of designing a PLL with minimal settling time while meeting other loop design requirements. Typically, phase noise or jitter are the most critical performance metric for a PLL and the loop bandwidth is chosen to prioritize optimal phase noise or jitter performances.

### 2.2.2 All-Digital PLL

All-digital PLL or ADPLL, displayed in Fig. 2.2, is another promising candidate for fast-settling/hopping LO generation in an advanced CMOS node for modern wireless applications [28]. A typical ADPLL is comprised of a digitally-controlled oscillator (DCO), digital loop filter, and a time-to-digital converter. The DCO's frequency is controlled by a frequency digital control word (DCW) instead of an analog controlled voltage seen in an analog PLL. The frequency of the DCW is the ratio of the desired output frequency divided by the input reference frequency. There are many types of architectures for ADPLL. The one shown in Fig. 2.2 [29] resembles the conventional charge pump PLL, the DCO signal is divided by a frequency divider and its output is compared with the reference signal by the time-to-digital converter (TDC). A TDC can be thought of as the equivalent of phase-frequency detector (PFD) and a charge-pump in an analog charge-pump PLL. The phase difference of the divided signal and reference is in digital form and is fed into the digital loop filter to generate the aforementioned frequency DCW.

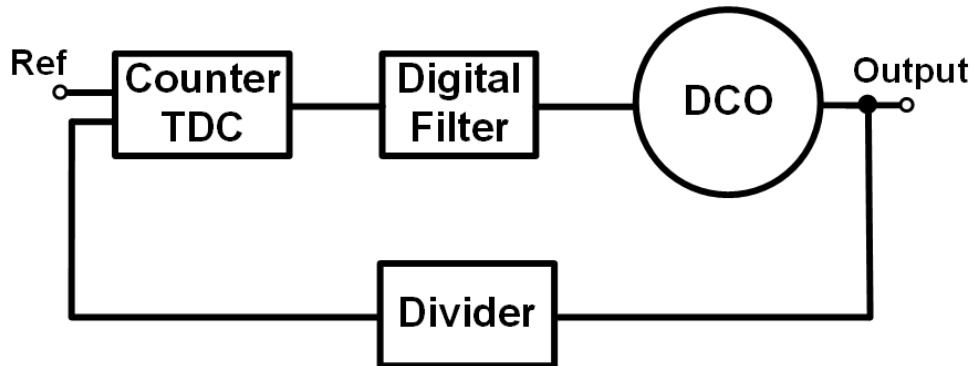


Figure 2.2: Architecture for AD-PLL.

Fast-settling/hopping capability for ADPLL has been reported and demonstrated [30]. However, the operation and challenge of implementing an ADPLL lies in the resolution of TDC. If the phase error is smaller than the time/phase resolution of the TDC, it essentially act as a bang-bang phase detector. The bang-bang operation introduces quantization noise, and the level of quantization noise introduced is a function of the resolution of the TDC. To

date, state-of-the-art ADPLLs are still plagued by this issue and this prevents them from achieving comparable performance to state-of-the-art analog PLLs [31].

### 2.2.3 Single-sideband Mixing-based LO Generation

Due to the previously mentioned stringent settling requirements of a PLL, hybrid approaches have been proposed to address this issue. Single-sideband (SSB) mixing-based technique, shown in Fig. 2.3 uses separate fixed-frequency PLLs to cover different frequency bands of interest and utilize an SSB mixer to generate mixing products between the fixed-frequency PLLs to further extend the coverage of frequency. By using a multiplexer (MUX) at the output to select the desired signal, this approach can eliminate the settling requirement of the PLL, meaning that frequency-switching speed becomes limited only by the signal switching speed of the MUX.

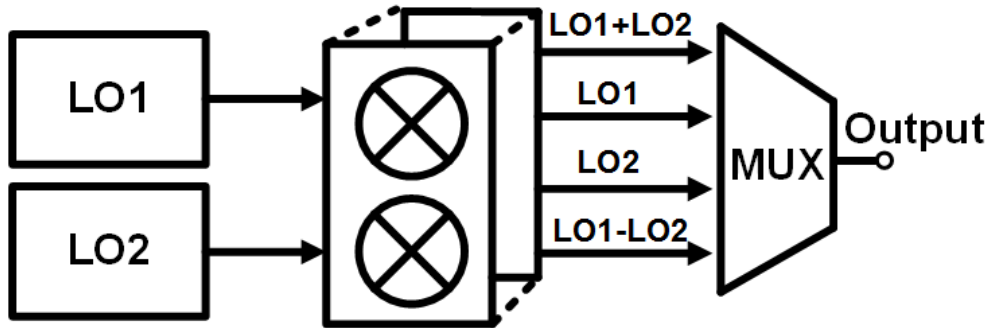


Figure 2.3: Architecture for SSB LO generation.

Though this technique may appear attractive initially, it directly introduces a variety of issues. First, quadrature phases are required from the fixed-frequency PLLs to drive the SSB mixer. Second, the SSB mixer produces unwanted mixing spurs, meaning additional filtering may be required after the SSB mixer. The mixer spurs can potentially also be alleviated by linearizing the SSB mixer, however, this comes at the cost of power consumption and noise penalty.

This approach was one of the popular candidates for Multi-band-OFDM Ultra Wideband (UWB) standard [32][33]. The 9.5ns guard-interval to switch hop between channels mandates

the usage of such an open-loop approach. However, in the context of sweeping-LO-based spectrum sensing, it is not a suitable choice since it can still generate discrete number of frequencies at the MUX output without reconfiguring the PLL.

### 2.2.4 Direct-digital Frequency Synthesis

Direct digital frequency synthesis, shown in Fig. 2.4, synthesizes a sinusoidal signal from an input DCW containing the frequency information. A typically DDFS [34–36] is comprised of a phase accumulator, a phase-to-sine map as a lookup table, and a digital-to-analog converter (DAC). The DAC can sometimes be followed by a low-passed filter. The output of the phase accumulator is a ramp with discrete levels. This ramping signal drives the preprogrammed loop-up table to generate a sampled sine-wave-like signal with discrete levels. Its period represents the corresponding frequency information of the input DCW. Finally, the DAC converts this sampled signal into a continuous sine wave.

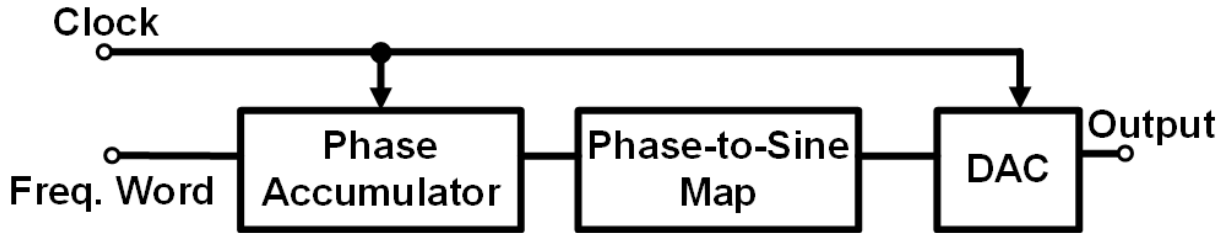


Figure 2.4: Schematic of DDFS system.

Thanks to its digital and open-loop nature, PLLs can achieve extremely fast settling time. However, implementing a DDFS at GHz frequencies requires high-speed digital circuits and DAC. While CMOS technology is achieving higher  $f_T$  as technology scales, implementing digital circuit and data-converter at GHz range remains to be challenging and most importantly, power consuming.

Fig. 2.5 briefly summarizes the conventional LO generation scheme and Fig. 2.6 shows a survey of locking time vs. power consumption for recently published fast-hopping/locking LO generation works.

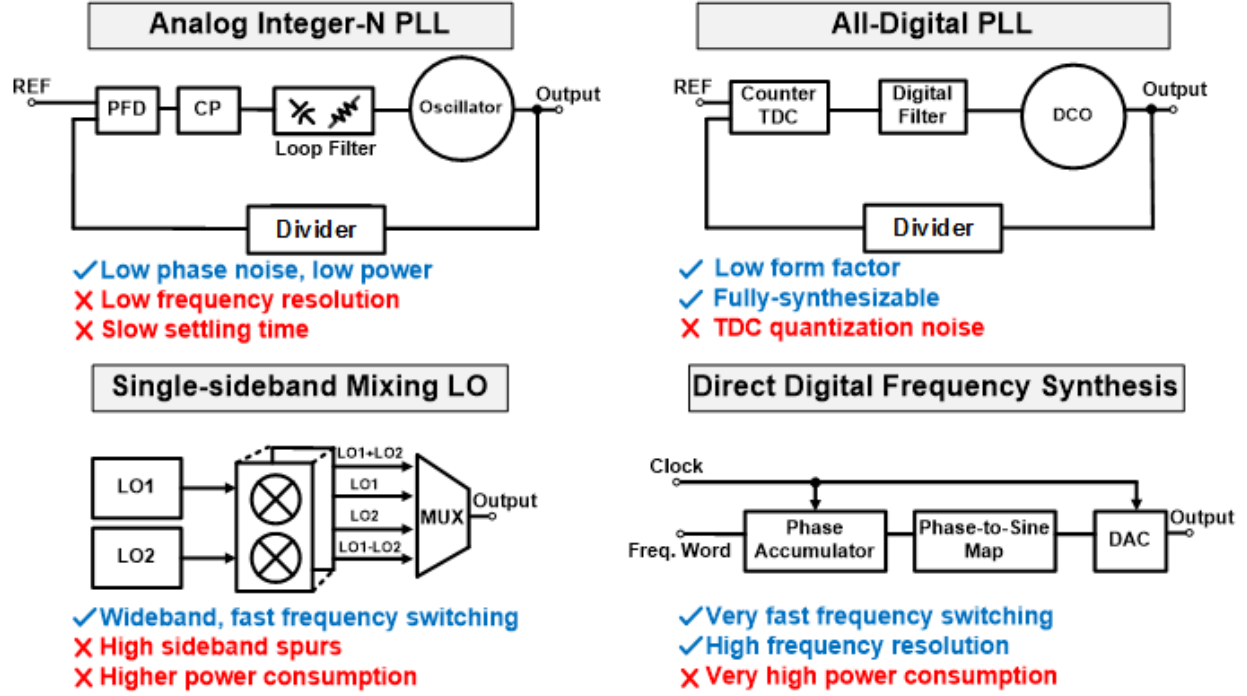


Figure 2.5: (a) Analog integer-N PLL (b) All-digital PLL (c) Single-sideband mixing LO generation (d) Direct digital frequency synthesis (DDFS) technique.

## 2.3 Prior-Arts

Prior works has sought to expedite the locking process of the PLL. Works in [37–39] have effectively varied bandwidth, mode, and type of PLL respectively between transient locking and steady-state operation to mitigate bandwidth vs. settling time trade-off in type-II integer-N PLLs. In [40], a pre-determined look-up table is utilized to preset the DCW of the VCO in the PLL. This reduces the initial VCO frequency error, but the potentially harmful initial phase error induced by the divider is not addressed.

## 2.4 Concept of Proposed Zero-Initial-Phase-Error [1]

In this work, a PLL is proposed where initial frequency and phase error at the hop instant are eliminated through digitally intensive initial-condition control. This eliminates acquisition

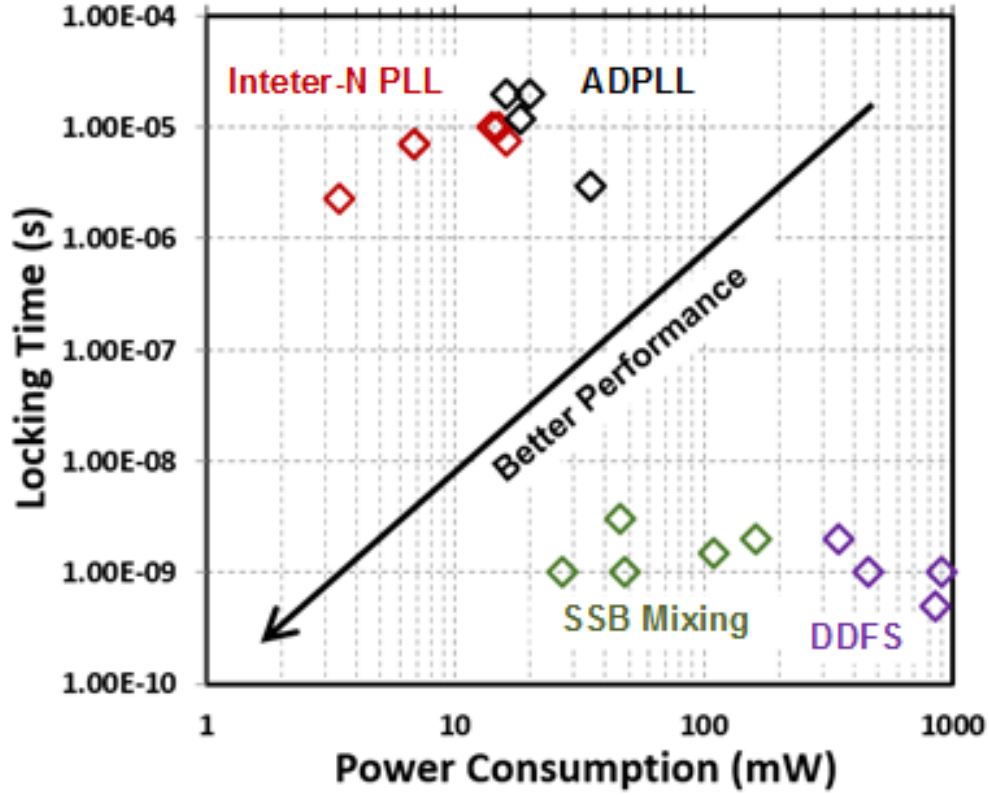


Figure 2.6: Survey of locking time vs. power consumption for recently published fast-hopping LO generation works.

and enables ‘instantaneous hops’ that fall within a frequency error limited only by the DCW resolution. The conventional integer-N charge-pump PLL (shown in Fig. 2.7(a)) is a nonlinear dynamic feedback system characterized by its state variables. Specifying the values of all state variables completely defines the system’s state. For example, an LC-VCO based charge-pump PLL is a mixed-mode system whose state variables include inductor current and capacitor voltage in the VCO, the control voltage across the loop filter’s capacitor, and the state of the digital divider (which is essentially a digital finite-state-machine (FSM) counter). Initial conditions are critical in the transient response of such systems. *This work proposes the assignment of initial conditions to each state variable in the system at the hop instant through extensive digital control and calibration to essentially hop to a locked state.*

The digital divider is essentially a counter with a programmable terminal count. Fig.

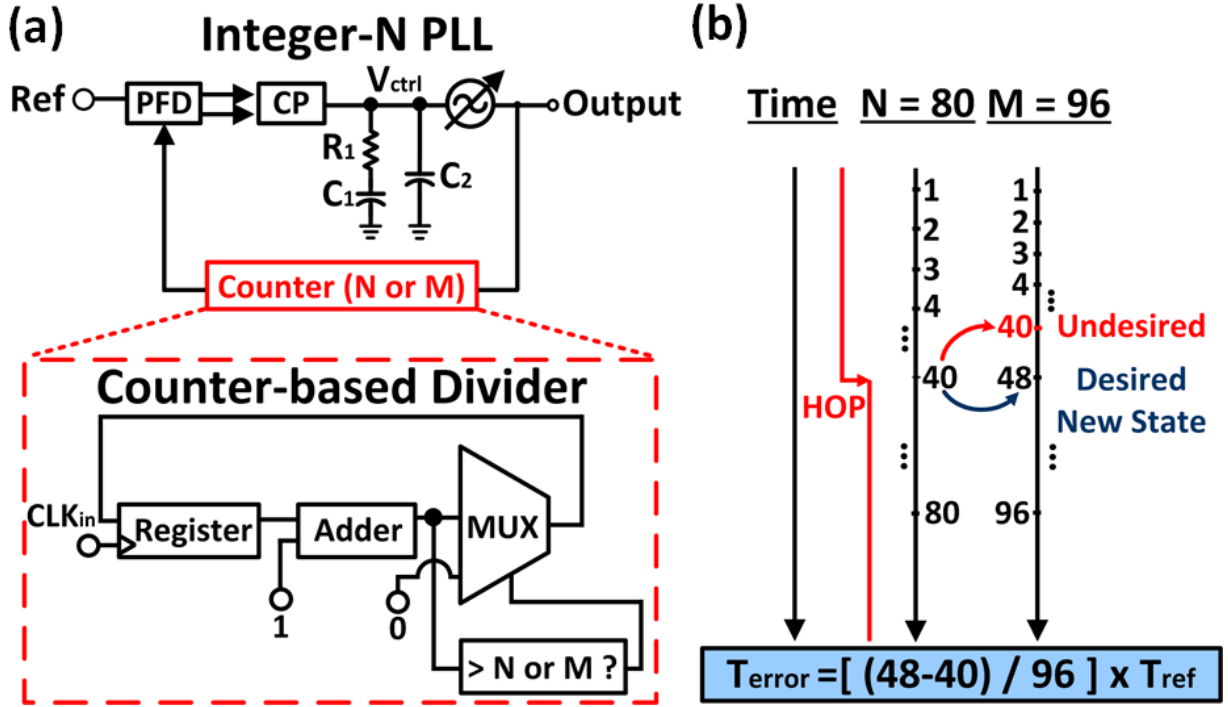


Figure 2.7: (a) PLL with a binary-sequence counter-based divider. (b) Mechanism of initial phase error in the counter-based divider.

2.7(b) illustrates the transient behavior of a conventional binary-sequence counter-based divider at the frequency hop instant. If the terminal count is set to either  $M = 80$  or  $N = 96$  at the hop instant, the counter induces an initial phase error to the reference signal if its original state (count 40 here) is maintained. Typical multi-modulus dividers use pulse-swallow counters or cascaded divide-by-2/3 structures, which have their own state-machine descriptions and so, initial-phase-error mechanisms. These initial phase errors can be eliminated by reconfiguring the state of the FSM at the hop instant.

To implement a divider with initial-state control, two aspects must be addressed. First, as seen in Fig. 2.8, assuming the divider chain has multi-modulus and fixed-ratio dividers, one aspect is whether the multi-modulus divider should be at the input or at the output of the divider chain. If zero initial phase error is achieved, this means that after reconfiguration of the divider modulus at the hop instant, the divider output is unchanged and perfectly

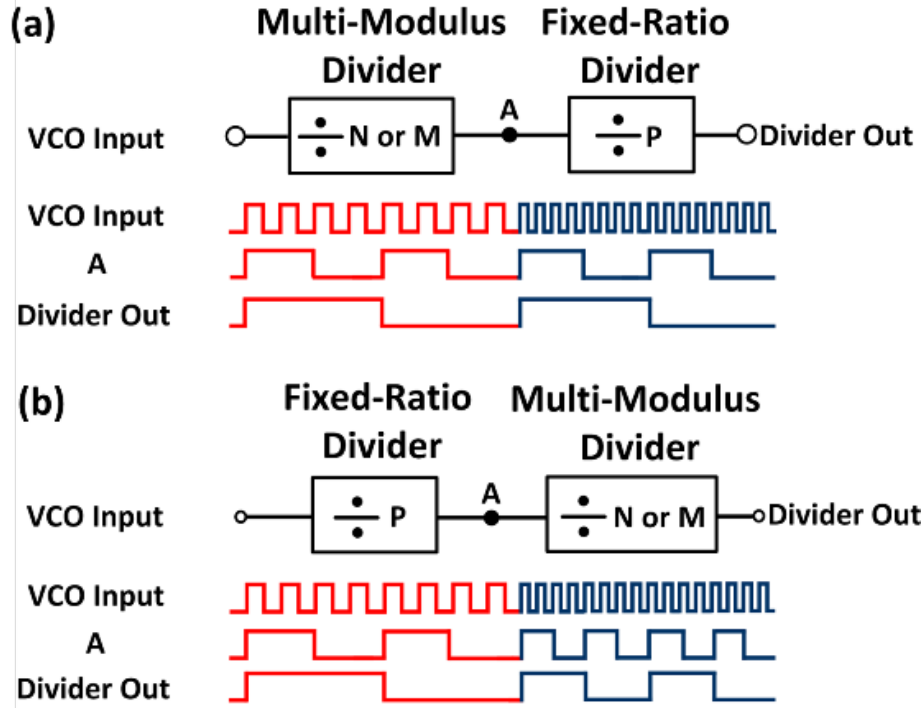


Figure 2.8: (a) Multi-modulus divider first: no initial state control is necessary in the fixed-ratio divider that follows. (b) Fixed-ratio divider first: initial state control is required throughout the chain.

aligned to the reference. Placing the multi-modulus divider at the front of the chain implies no initial-state control is necessary in the fixed ratio dividers that follow (Fig. 2.8(a)), easing the digital control exercised at the hop instant.

A second aspect is whether the front-side multi-modulus divider should be synchronous or asynchronous. Asynchronous dividers are generally used for reduction in clock frequency down the chain to reduce dynamic power consumption. In such chains the sub-dividers at different clock frequencies are mutually skewed due to divider delays. This makes initial-state control and even defining a state fundamentally problematic. Thus, to enable instantaneous hops, the multi-modulus divider must be synchronous despite the slightly higher power consumption. The following fixed-ratio divider can be asynchronous.

With these considerations, a zero-initial-phase-error divider is proposed, shown in Fig. 2.9

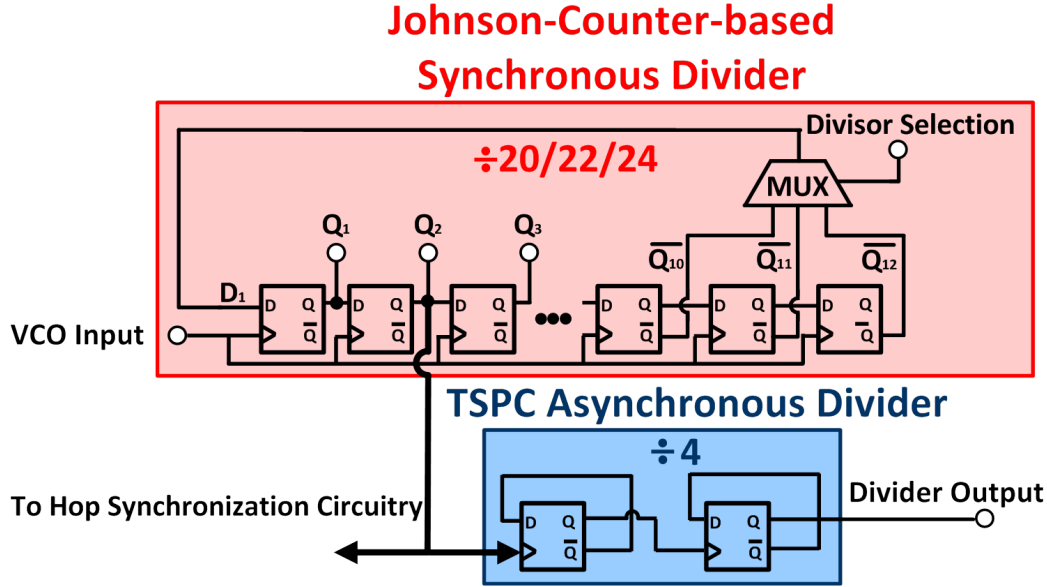


Figure 2.9: Proposed zero-initial-phase-error divider structure.

with a synchronous divide-by-20/22/24 Johnson-counter divider followed by asynchronous flip-flop-based divide-by-2 dividers. The multi-modulus nature of the Johnson-counter dividers derives from the 3-1 multiplexer (MUX), which controls feedback. As shown in Fig. 2.10, in the absence of state reconfiguration at the hop instant, the initial phase error accumulates throughout the period of the synchronous divider output and resets to zero at each rising/falling edge. Thus, if the hop instant is synchronized with the rising edge of the synchronous divider output, initial phase error is eliminated without extensive digital controls. The delay induced by this synchronization will be less than one period of synchronous divider output ( $\sim 4.7\text{ns}$  in this prototype).

## 2.5 Proposed 4.0-5.84 GHz Instantaneous-Hop PLL

A type-II third-order charge-pump PLL (Fig. 2.11) forms the core of the proposed synthesizer. The PLL has an LC-VCO operating over 4.0-5.84 GHz which is tuned with an accumulation-mode varactor and a high-resolution 9-bit DCW (Fig. 2.12), as well as the programmable 80/88/96 divider chain described earlier (Fig. 2.9). A 53 MHz off-chip XO

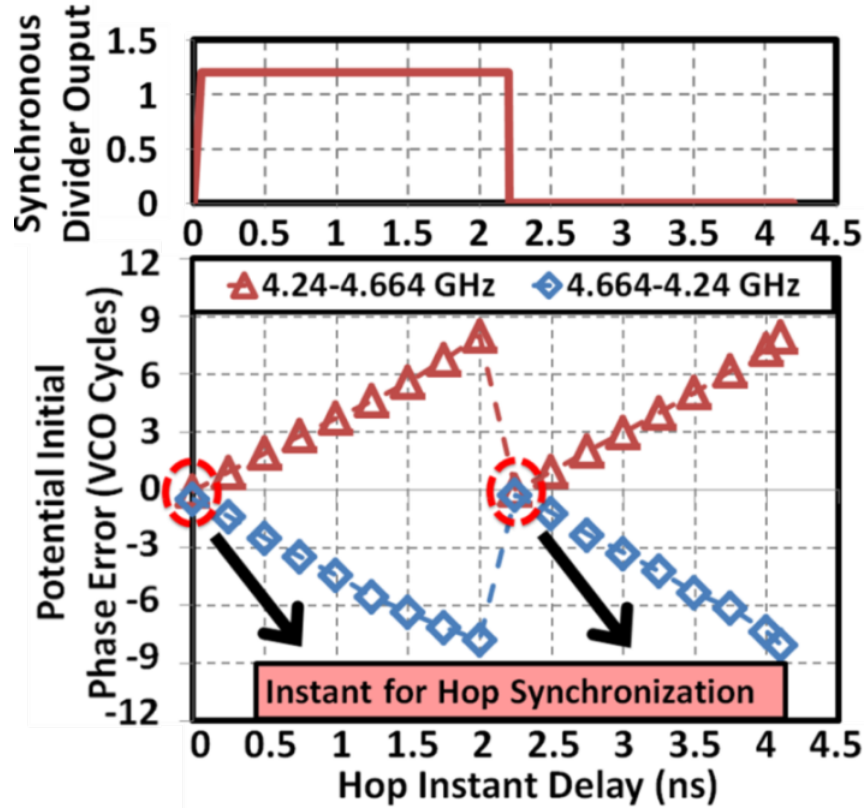


Figure 2.10: Potential initial phase error in the proposed divider structure for upward and downward hops.

enables locking of the PLL to 4.24, 4.664 and 5.088 GHz with division ratios of 80, 88 and 96 respectively. A conventional tri-state phase-frequency detector (PFD) and passive loop filter are integrated on chip. The loop parameters are designed for a bandwidth of 800 kHz and phase margin of 45 degrees. Loop filter capacitors  $C_1$ ,  $C_2$  are 35 and 5 pF respectively, and  $R_1$  is  $6k\Omega$ .

As described earlier, for zero initial phase error, the hop instant must be synchronized with the rising edge of the synchronous divider output. In addition to state variables, the charge pump current is also reprogrammed at the hop instant to maintain constant loop bandwidth due to varying  $K_{VCO}$  gain. Note that the charge pump current is not a PLL state variable and does not contribute to initial condition errors. In this prototype, an on-chip state register stores the DCW of 9-bit VCO, divider ratio control and charge pump

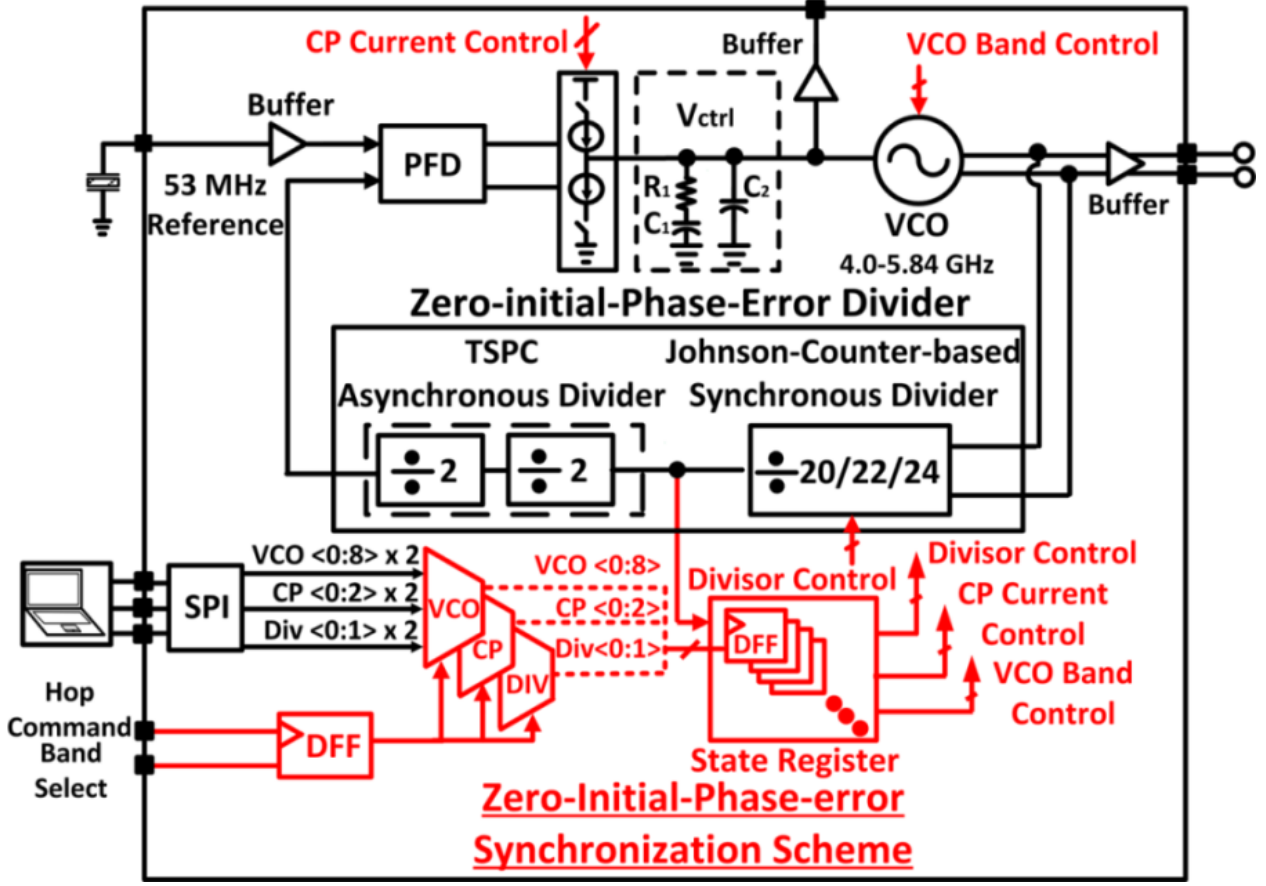


Figure 2.11: 4.0-5.84 GHz instantaneous-hop PLL block diagram.

current control. A second on-chip memory with a serial interface (SPI) stores the settings for the different frequencies between which the PLL hops (limited to two in this prototype). The externally-applied hop signal clocks a flip-flop that registers the externally-applied 1-bit band select signal. This flip-flop then selects the settings of one of the two possible output frequencies for loading into the state register which is clocked by the synchronous divider output to ensure hopping at its rising edge.

Other initial conditions include  $V_{ctrl}$ , the inductor current and the capacitor voltage of the VCO. The DCW of a 9-bit VCO ensures that the VCO can be programmed to lock with  $V_{ctrl}$  close to  $V_{dd}/2$  for any output frequency. Choosing the appropriate initial DCW prior to hop could eliminate the need for setting  $V_{ctrl}$ . Controlling the initial inductor current and capacitor voltage in the VCO is challenging as they are analog signals. However, as the

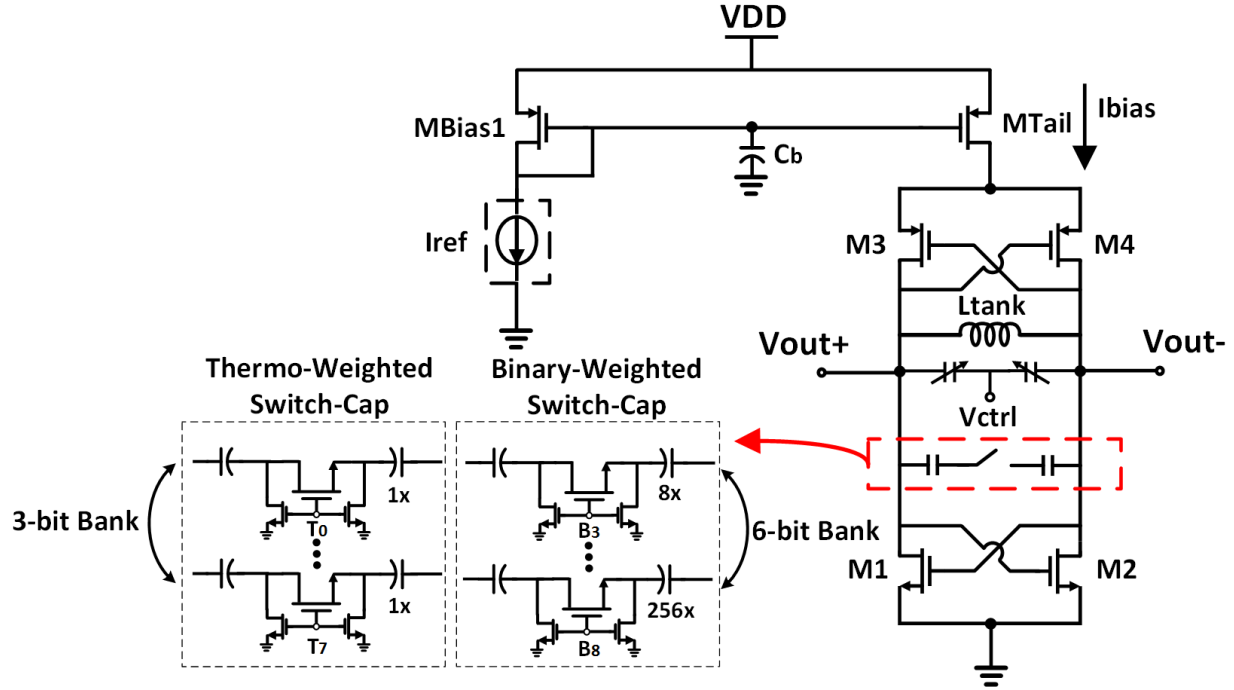


Figure 2.12: 4.0-5.84 GHz 9-bit digitally-controlled LC-VCO with analog varactor tuning.

division ratios are large, the impact of not controlling them is small. The residual errors due to finite DCW resolution, initial phase errors in the VCO due to the LC state variables, and delays in the digital control path settle at a rate determined by the loop bandwidth and their magnitude will determine the dynamic frequency error during settling. The prototype has been designed to achieve an extremely low dynamic frequency error of 3.64 MHz on average (dominated by DCW resolution), significantly lower than the varactor tuning-range. The frequency drift of the VCO due to process, voltage, and temperature (PVT) variations can be addressed by periodic calibration [41]. Increasing the resolution of the initial condition digital control can lead to even lower dynamic frequency errors.

To demonstrate the benefit of this architecture, Verilog-AMS models were simulated for the proposed divider and a conventional cascaded asynchronous divide-by-2/3 divider chain (with realistic divider delays). A Verilog-AMS VCO model is built with a tuning curve fit to the measurements. The PFD was modeled in Verilog-AMS while the charge-pump was at the transistor-level. Fig. 2.13 shows the simulated settling behavior for a hop from 4.664 to

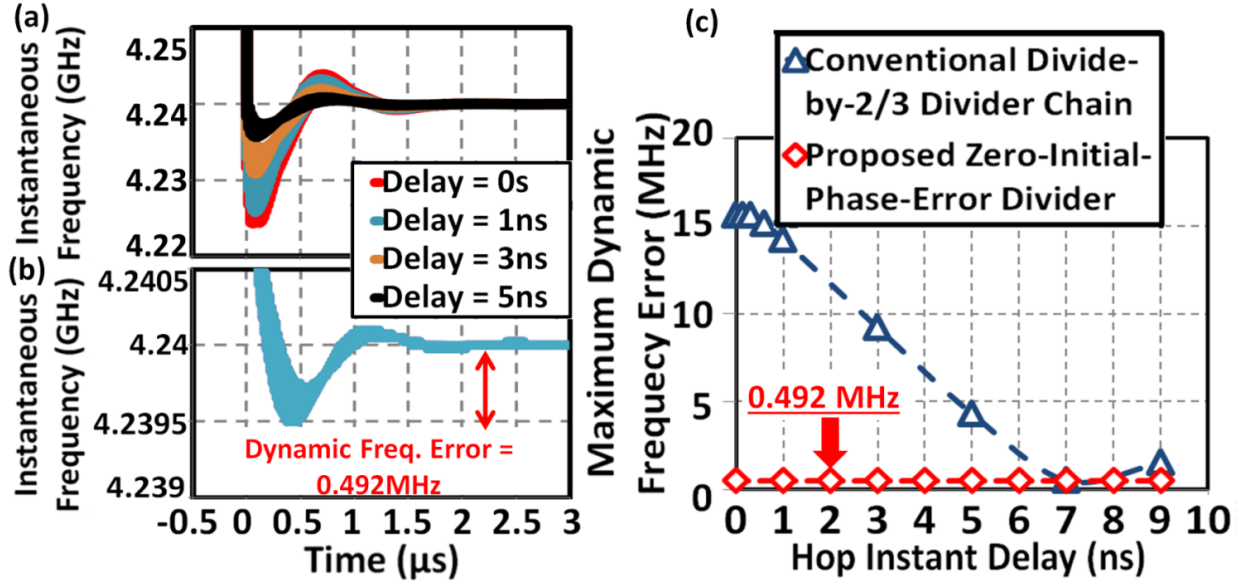


Figure 2.13: Instantaneous frequency vs. time for different hop instants in (a) a conventional PLL using divide-by-2/3 asynchronous dividers, and (b) a proposed instantaneous-hop PLL. (c) Maximum dynamic frequency error vs. hop instant in both cases.

4.24 GHz. Frequency pre-setting is done in both cases while the external hop signal is varied in time over one reference cycle. The proposed divider eliminates initial phase error, and thus minimizes  $V_{ctrl}$  overshoots and dynamic phase error by 1-2 orders of magnitude during settling.

## 2.6 Measurement Result

A 65nm CMOS prototype was fabricated with  $0.95 \text{ mm}^2$  chip-area and further mounted on a four layer FR-4 printed-circuit board for testing purpose, as shown in Fig. 4.9(a) and (b). It draws 14 mA current in total from a 1.2V supply.

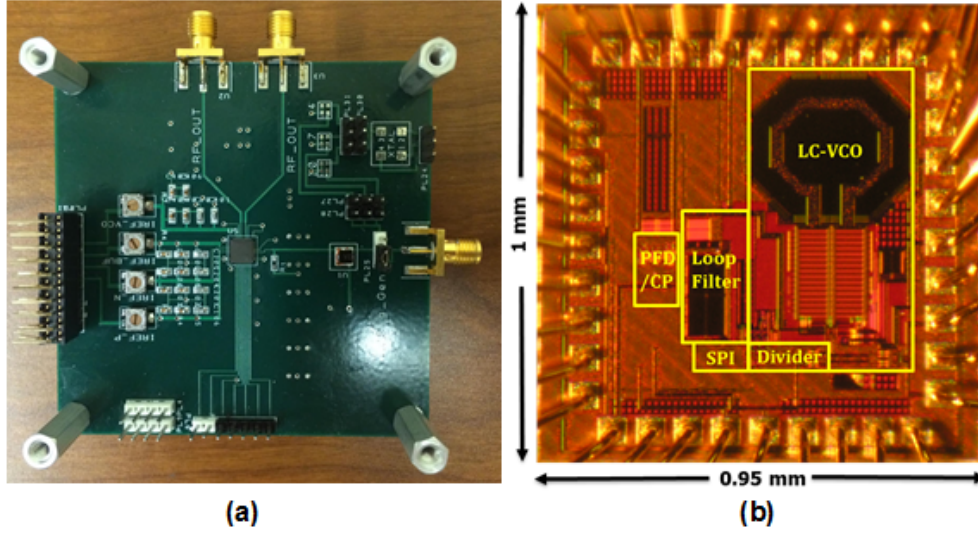


Figure 2.14: (a) Photo of the board assembly for testing purposes (b) Chip micro-photograph.

### 2.6.1 VCO Measurement

The measured tuning-range of the VCO is 4.0-5.84 GHz. Fig. 2.15(a)-(d) depicts the VCO's frequency,  $K_{VCO}$ , the frequency-difference between two successive DCW values at mid- $V_{ctrl}$ (0.6V), and the single-band frequency tuning-range across all DCW. With these, a DCW for any desired output frequency placing the required  $V_{ctrl}$  near mid-VDD with a residual initial frequency error of less than 3.64 MHz on an average can be found.

### 2.6.2 PLL Locked-spectrum and phase noise measurement

For PLL operation at 4.24GHz, the measured locked spectrum is shown in Fig. 2.16(a) and the measured phase noise profile is shown in Fig. 2.16(b). For PLL operation at 5.08GHz, the measured locked spectrum is shown in Fig. 2.17(a) and the measured phase noise profile is shown in Fig. 2.17(b). The spot phase noise for PLL operating at 4.24, 4.664 and 5.088 GHz carrier frequencies at 1MHz-offset are measured to be -115.2, -114.4 and -112.1 dBc/Hz respectively.

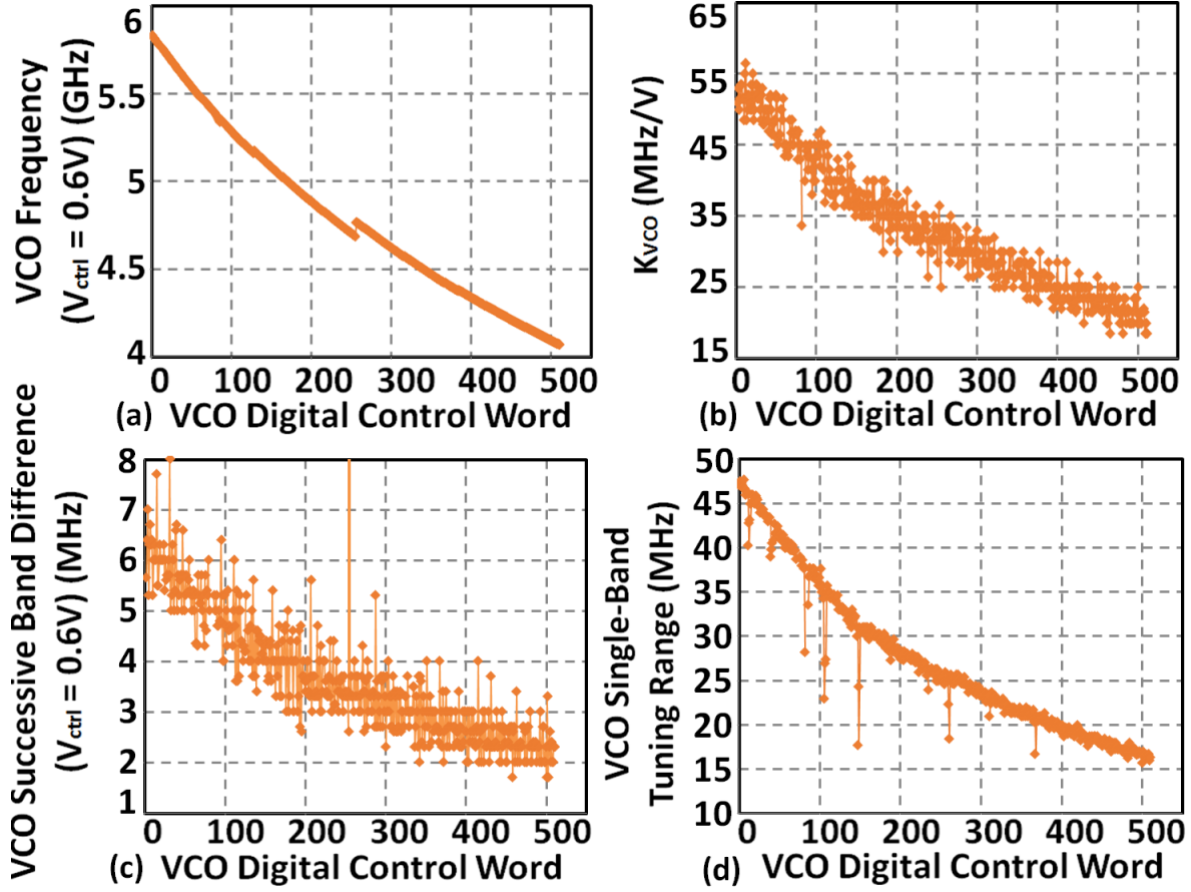


Figure 2.15: Measured 4.0-5.84 GHz 9-bit LC-VCO performance at  $V_{ctrl} = 0.6V$  vs. DCW: (a) frequency (b)  $K_{VCO}$  (c) frequency difference between two successive DCW (d) single-band frequency coverage as  $V_{ctrl}$  is varied from 0-1.2V.

### 2.6.3 PLL Hopping Measurement

Fig. 2.18 shows the measurement setup for the PLL hopping measurement. The signal from DUT, namely the VCO output, is first power-split and then quadrature-downconverted by a clean reference from a signal generator. The output at IF port of the mixer is monitored on an oscilloscope to determine the DUT's instantaneous frequency. The measured instantaneous frequency of the DUT can be expressed as

$$\omega_{Instantaneous,DUT} = \omega_{LO-TEST} + \frac{d}{dt} \left[ \tan^{-1} \frac{Q_{bb}(t)}{I_{bb}(t)} \right] \quad (2.2)$$

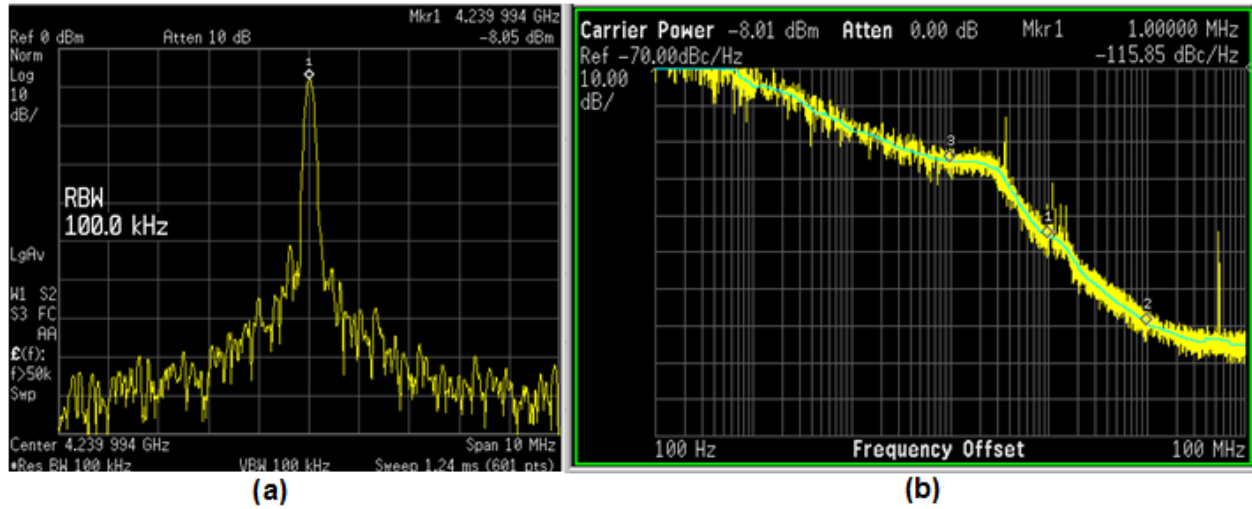


Figure 2.16: (a) Spectrum of the measured PLL at 4.24GHz (b) Phase noise profile of the measured PLL at 4.24GHz.

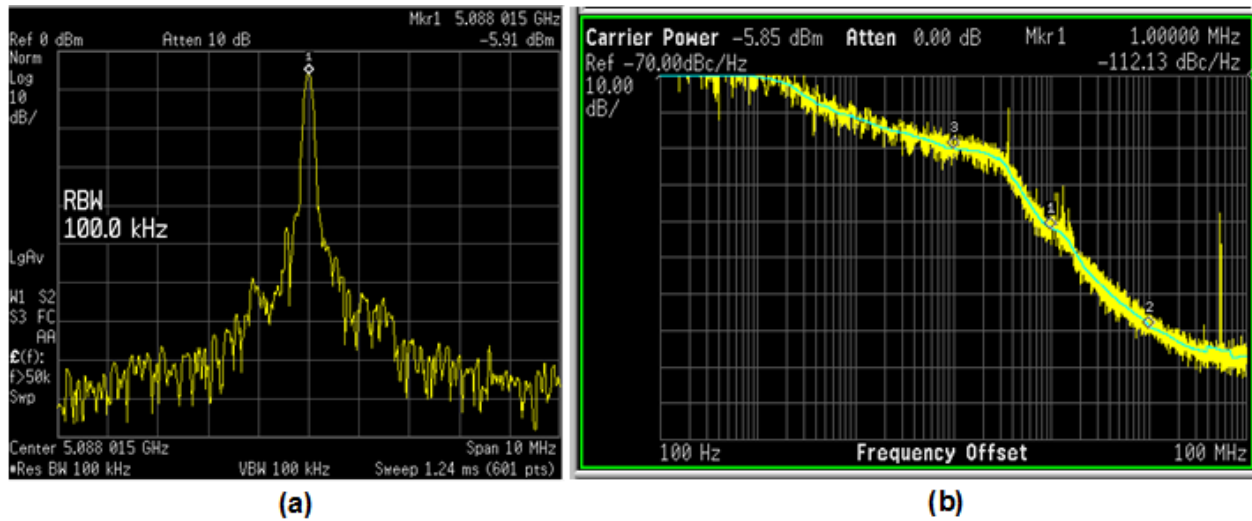


Figure 2.17: (a) Spectrum of the measured PLL at 5.08GHz (b) Phase noise profile of the measured PLL at 5.08GHz.

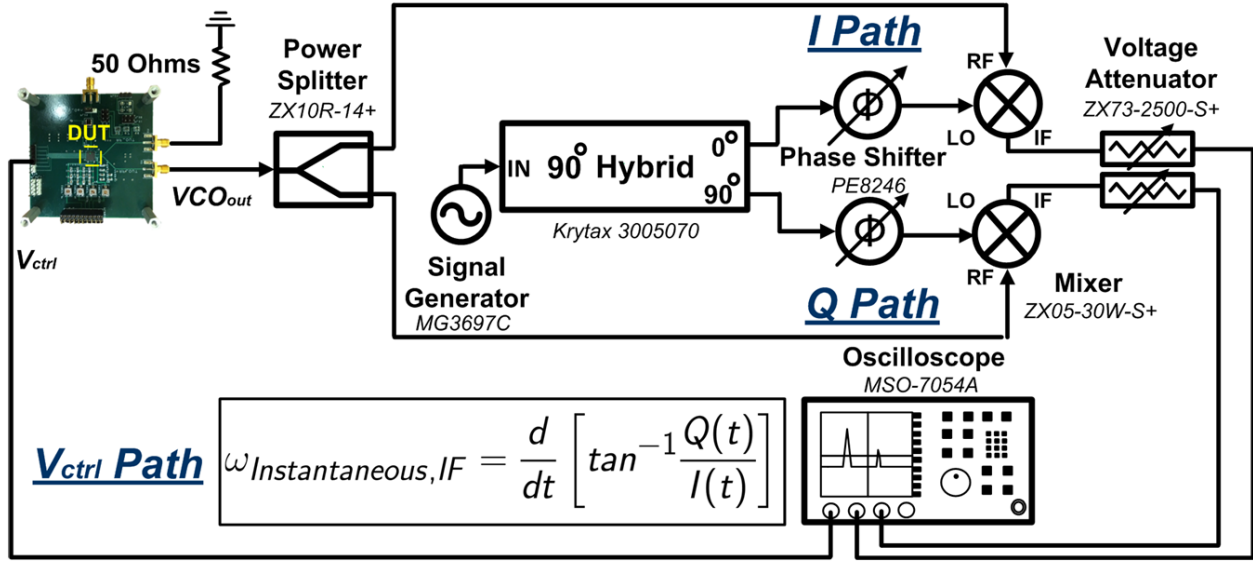


Figure 2.18: Block diagram of proposed PLL transient hopping measurement setup.

To monitor hopping, the  $V_{ctrl}$  node is also noted with a unity-gain buffer. Fig. 2.19(a) shows  $V_{ctrl}$  in a hop from 4.664 to 4.24 GHz as the divider ratio changes from 88 to 80. The PLL settles within  $4\mu s$  with minimum overshoot. Fig. 2.19 (b) shows the instantaneous frequency during this period. The dynamic frequency error never exceeds 850 kHz. Fig. 2.19(c) shows  $V_{ctrl}$  in a hop from 4.136 to 4.512 GHz with the divider ratio programmed from 88 to 96. Fig. 2.19(d) shows  $V_{ctrl}$  in a hop between 4.24 and 4.644 GHz. In all cases, a very small dynamic frequency error is maintained.

### 2.6.4 Performance comparison

Table 2.1 compares state-of-the-art fast-locking/hopping PLLs.

Table 2.1: Performance summary and comparison.

Work	JSSC'08 K. Woo and D. Ham	JSSC'10 W.-H Chiu and T.-H Lin	This work
Architecture	Hybrid-PLL	Dynamic Phase Compensation	Zero initial phase error
Technology	180nm CMOS	180nm CMOS	65nm CMOS
Frequency	2.368-2.496 GHz	5.27-5.6 GHz	4.0-5.84 GHz
Power	29.6 mW	19.8 mW	16.8 mW
Supply	1.8V	1.8V	1.2V
Reference	64 MHz	10 MHz	53 MHz
Loop BW	400 kHz	120 kHz	800 kHz
Phasennoise @ 1MHz	-113.0 dBc/Hz	-114.28 dBc/Hz	-115.2 dBc/Hz
Reference Spurs	-54 dBc	< -70 dBc	< -50 dBc
Dynamic Frequency Error	N/R	N/R	<3.64 MHz average
Hopping/Settling Time	~20 $\mu$ s	~20 $\mu$ s	~5 $\mu$ s
Chip Area	2.08 mm <sup>2</sup>	1.61 mm <sup>2</sup>	0.95 mm <sup>2</sup>

## 2.7 Conclusion and Future Work

In this chapter, a comparison between conventional fast-settling/hopping LO generation schemes were outlined with a focus on targeting sweeping-LO-based spectrum analysis in CR applications. Subsequently, a zero initial phase error concept for PLL feedback loop settling was introduced. Following the introduction of the zero-initial-phase-error concept, an instantaneous-hop frequency synthesizer architecture featuring a zero-initial-phase-error divider was proposed. An implementation of a 65nm CMOS prototype and its validated measurement result was discussed.

As was shown in Eq. 2.1, the hopping time of a conventional loop directly trades off with its loop bandwidth and the frequency jump. These trade-offs limit the design de-

degrees of freedom for the loop and can potentially compromise overall performances. The proposed instantaneous-hop frequency synthesizer was based on a zero-initial-phase-error multi-modulus divider. It breaks the fundamental trade-off between hopping time, spectral purity and frequency resolution.

There are a few avenues that can be pursued to extend the scope of the proposed architecture. Modern PLLs for mobile radios often employ fractional-N instead of integer-N architecture to relax the fundamental trade-off between reference frequency, channel resolution/selectivity, and loop bandwidth. It would be interesting to explore the possibility of incorporating the proposed technique into the schemes of fraction-N PLL. Another interesting direction to explore is calibration. Since the proposed architecture exploits a digital-intensive design, it may require a well-planned calibration scheme and algorithm such that the performance can withstands PVT variation. A possible calibration scheme is shown in Fig. 2.20.

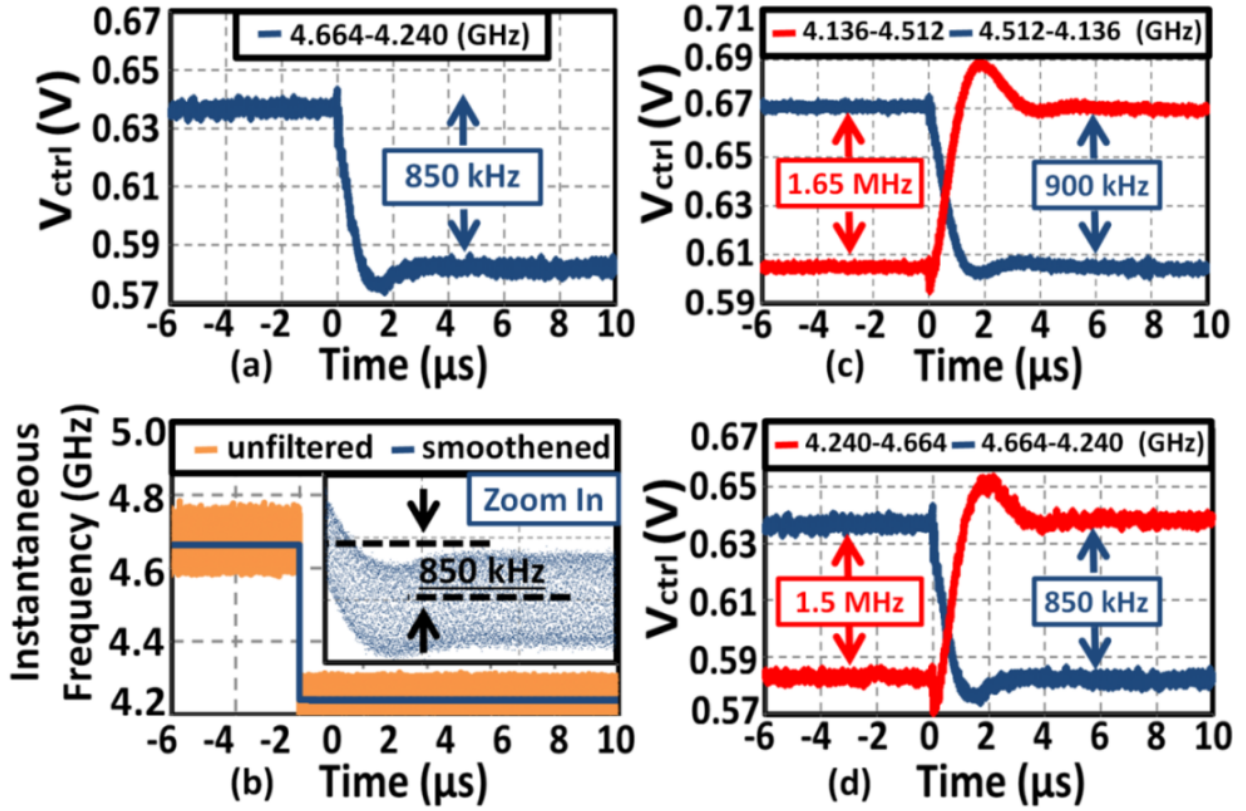


Figure 2.19: Measured (a) control voltage and (b) instantaneous output frequency for a hop from 4.644 GHz to 4.24 GHz showing a maximum dynamic frequency error of 850 kHz. Measured control voltage for upward and downward hops (maximum upward/downward dynamic frequency error) between (c) 4.136 GHz and 4.512 GHz (1.65MHz, 900kHz) (d) 4.24 GHz and 4.644 GHz (1.5MHz, 850kHz). The 4.664 to 4.24 GHz downward hop is a repeat of (a).

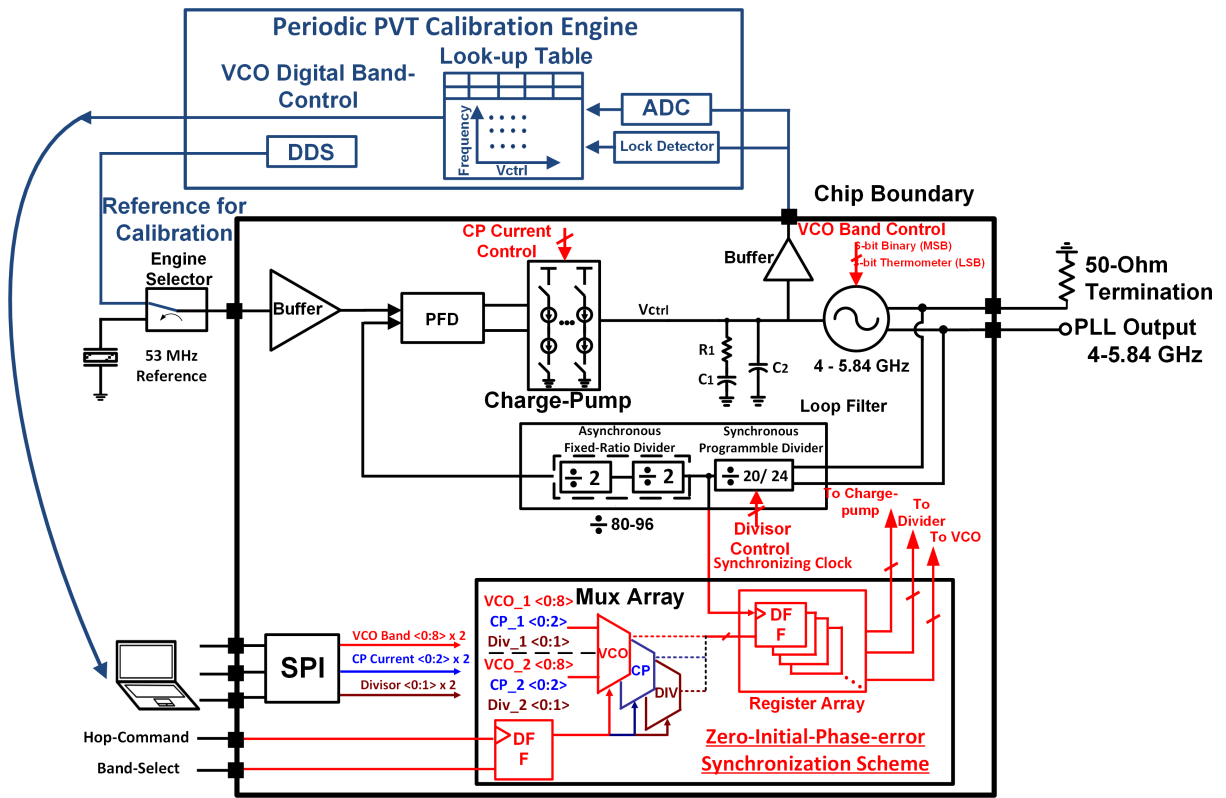


Figure 2.20: Proposed calibration engine for the proposed instantaneous-hop PLL.

## Chapter 3

# Embedded Phase-shifting LO-Path Design for Wideband RF Self-Interference Cancelling Receiver

### 3.1 Introduction

Phase shifters or phase rotators in silicon technology can be useful for numerous applications such as digital synchronous data-link [42], beam-steering phased-array systems for high data-rate wireless communication or radar applications [43, 44], and pulse generation for UWB systems [45], among others. Resolution, linearity, maximum range of coverage, and system bandwidth are critical design considerations for phase shifters or phase rotators.

Depending on the frequency of operation, available input, and required I/O signal type (analog/digital), various types of phase shifters are used on different occasions. I/Q interpolator-based phase shifters are one of the most widely-used choice among the phase shifter types. These provide a full 360 degrees of coverage with both amplitude and phase reconfigurability for calibration purposes. Due to its active nature, an I/Q interpolator-based shifter can potentially provide voltage or power gains to the system at the cost of DC power consumption. However, generating an in-phase and out-of-phase (I/Q) signal for the interpolator can be

challenging for high-frequency or broadband input signals.

This work presents an alternate method of employing I/Q interpolator-based phase shifters in modern radio design. The functionality of phase shifters is embedded in the LO path design for the radio and the embedded phase shifting capability enables the radio to perform self-interference cancellation with minimum complexity and design overhead.

The research of embedded phase-shifting LO-path design for wideband RF self-interference cancelling receiver front-end that is presented in this work [2] was performed in collaboration with Dr. Jin Zhou (now with UIUC) at Columbia CoSMIC Lab. Both the implementation of the receiver front-end signal path and measurement of the overall system were performed by Dr. Jin Zhou. The contribution of this work relates to the design and implementation for the overall LO path of the system.

## 3.2 Challenges of Self-Interference Cancellation for FDD and Full-Duplex Radio

Frequency-division multiple access (FDMA) is a critical channel access technique that is widely adopted in modern wireless communication standards. It provides users allocation of individual frequency bands or channels to transmit or receive data stream. Supporting FDD operation at the radio front-end is indispensable to enabling FDMA. As shown in Fig. 3.1, modern radio design often uses numerous off-chip duplexers to support multi-band FDD operation. While these front-end off-chip duplexers provide high-Q filtering such that the transmitting and receiving path of the radio can operate at adjacent frequency bands concurrently, they tend to be narrow-band and bulky. The combination of these two factors limits the overall system form factor. For this reason, a tunable duplexer [46] to minimize the number of duplexers that are required at the radio front-end has been an active research problem, however, the incorporation of tunability exacerbates the insertion loss vs. TX/RX isolation trade-off. To relax the TX/RX isolation vs. insertion loss trade-off for tunable duplexer, self-interference cancellation (SIC) is required [47] [48] [49] as depicted in Fig. 3.1

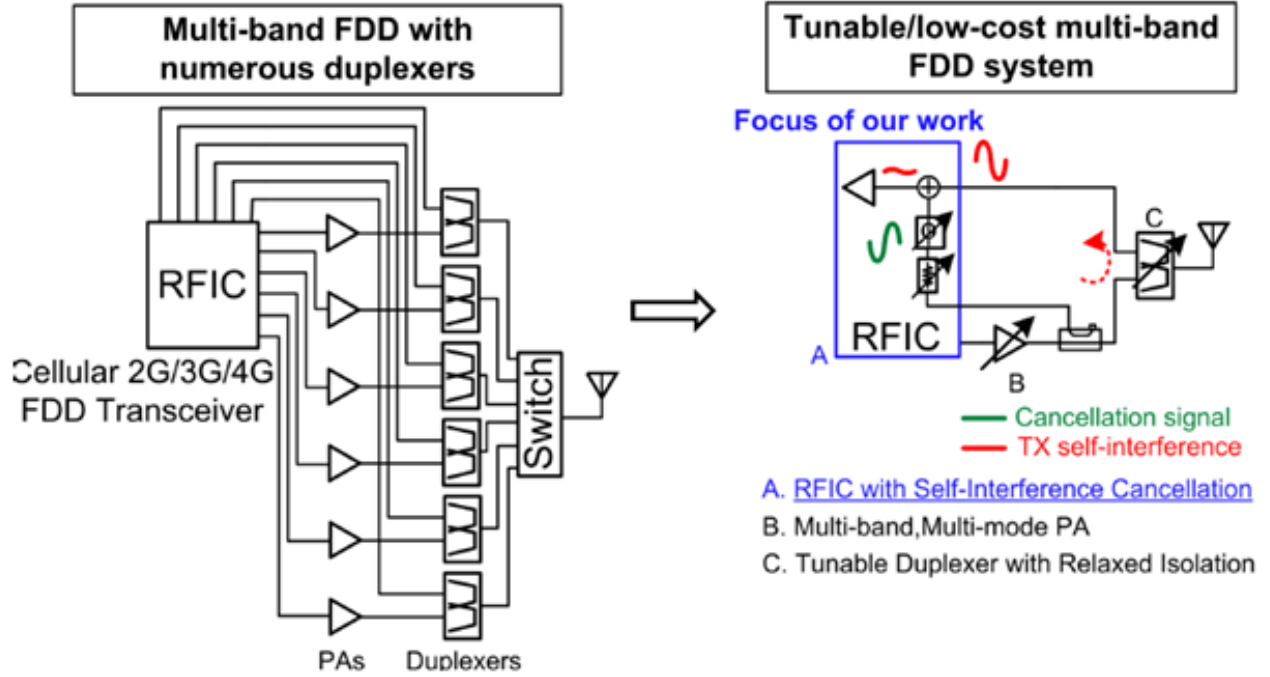


Figure 3.1: Highlight of allocated spectrum at mm-wave frequencies [2].

and Fig. 3.2(a).

Integrated radio for Full-duplex (FD) wireless communication has attracted significant research interests [6][15]. By simultaneously transmitting and receiving the outgoing and incoming information at the same frequency band (shown in Fig. 3.2), spectrum efficiency can potentially be doubled [6], [15]. However, the biggest challenge associated with FD wireless is the tremendous amount of SI in addition to the desired signal. As is required for any radio, for full-duplex radios to receive the desired signal, its self-interference must be suppressed below the RX noise floor through isolation and cancellation.

As analyzed in [2], given +15 dBm TX output power, 20 MHz RX signal bandwidth (BW) and 5 dB RX noise figure, >111 dB SI suppression is required. While discrete-component-based demonstrations have established the feasibility of FD wireless [50], [51], only recently have there been demonstrations of fully integrated RFICs incorporating SIC for FD [52], [2][53]. A fully integrated CMOS implementation imposes constraints that render the SIC techniques proposed in prior discrete-component-based implementations. The benefit of SIC

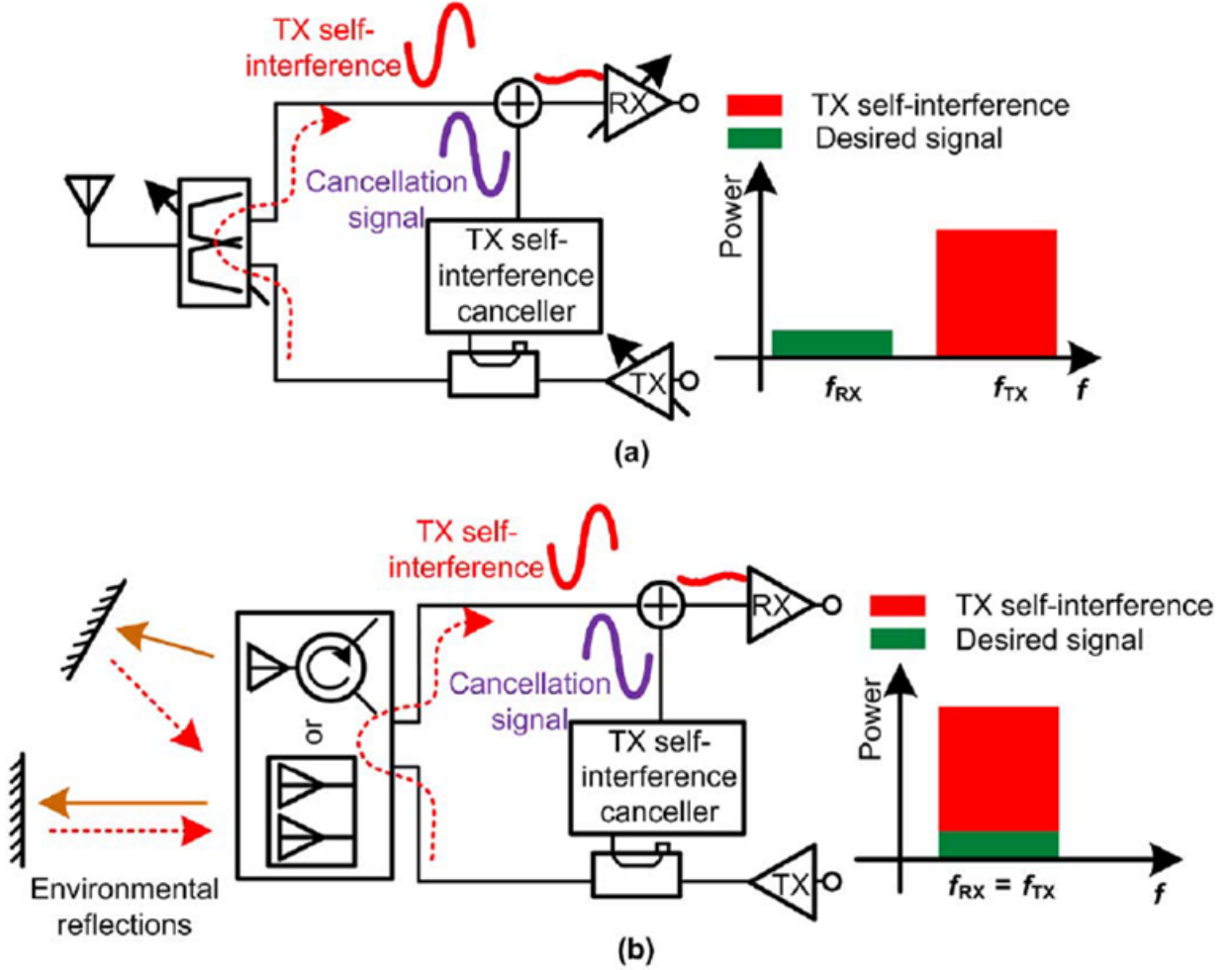


Figure 3.2: TX SIC in the RF domain for (a) a multiband FDD wireless system with a tunable duplexer and (b) an FD wireless system [2].

in the RF domain, where a replica signal is tapped from the TX output and injected prior to RX downconversion, is that the cancellation signal includes all the nonidealities from the TX chain. Furthermore, the earlier the SIC, the more relaxed is the RX front-end linearity requirement.

Wideband cancellation in the RF domain is a fundamental problem due to the highly frequency-selective nature of antenna interfaces. Conventional RF feed-forward cancellation technique emulates the magnitude and phase response of the antenna interface isolation at one frequency. Time-domain equalization wideband SIC has been proposed and demon-

strated with discrete components assembled on the printed circuit board. It resembles an RF FIR filter topology where the signals are delayed, weighted, and summed through transmission lines and attenuators. As reducing form-factors is the fundamental motivation, an integrated solution is preferred and desired. For the RF canceller to commensurate with the isolation profile of the antenna interfaces, generating nano-second scale delays is required. Generating nano-second scale true time delay on silicon requires extremely lengthy transmission line and generating narrow-band approximation of large group delay requires extremely high-Q passives, which are difficult due to their lossy substrate.

### 3.3 N-path-Filter-Based Wideband RF Self-Interference Cancellation

To enhance the cancellation BW, second-order reconfigurable BPFs with amplitude and phase control in each path are introduced in the RF canceller. The reconfigurable BPFs can be modeled using a second-order RLC BPF. It can be shown that a second-order BPF can be completely characterized by their center frequencies, amplitude, phase, and quality factor. By placing a bank of second-order BPFs in parallel and independently reconfiguring their design degrees of freedom (center frequency, amplitude, phase, Q), frequency domain equalization of the isolation profile of the antenna interfaces can be achieved.

Recently, N-path filters have emerged as a promising solution for implementing integrated widely tunable high-Q RF filters [54]. Advancement in modern scaled CMOS technology has enabled transistors to switch efficiently at gigahertz frequencies, making N-path filters a promising solution for the implementation of integrated widely-tunable high-Q RF filters as shown in Fig. 3.3 (a) [54]. In this work, a two-port N-path Gm-C filter with embedded variable attenuation and phase shifting is proposed for implementing the second-order high-Q BPF.

As shown in Fig. 3.3 (b), the aforementioned four design degrees of freedom can be independently reconfigured in the following ways.

- **Center frequency ( $f_c$ ) of the BPF:** The center frequency of each N-path filter can be reconfigured easily by changing the LO frequency of the mixer. However, this method may require more than one PLL in the system. In this work, an alternative was adopted. By reconfiguring the  $G_m$  value of the back-to-back baseband transconductance cell, the center frequency of BPF is shifted. The frequency shift,  $\Delta\omega$  can be express as [54]

$$\Delta\omega = \frac{G_m}{C_B} \quad (3.1)$$

where  $G_m$  is the baseband transconductance value and  $C_B$  is the baseband capacitor value.

- **Amplitude response of the BPF:** The amplitude response of the N-path filter-based BPF can be easily reconfigured by varying the ratio between the source impedance  $R_s$  and, the load impedance  $R_L$ . This essentially change the attenuation factor of the input signal. The magnitude response at the center frequency, ( $f_c$ ), can be expressed as [2]

$$|H(j\omega_s)| = \frac{I_{canceller}}{V_{in}} \approx \frac{8}{\pi^2} \cdot \frac{(R_L + R_{on})\omega_s C_c R_o}{R_S + R_L + 2R_{on}} \quad (3.2)$$

- **Phase response of the BPF:** A constant phase shift can be introduced by phase shifting the LO driving the mixer switches on the output side of the N-path filter. An linear periodic time-variant (LPTV) analysis [55] can be carried out to show that phase shifting the LOs driving the output side switches imparts constant phase shifts to the two-port N-path filter frequency response with no other impact on close-in response.
- **Quality factor:** The quality factor of an N-path filter may be reconfigured via the baseband capacitor  $C_B$ , given fixed  $R_S$  and  $R_L$ . LPTV analysis yields [56]

$$Q = 4\pi f_S [(R_S + R_{on}) || (R_L + R_{on})] C_B \quad (3.3)$$

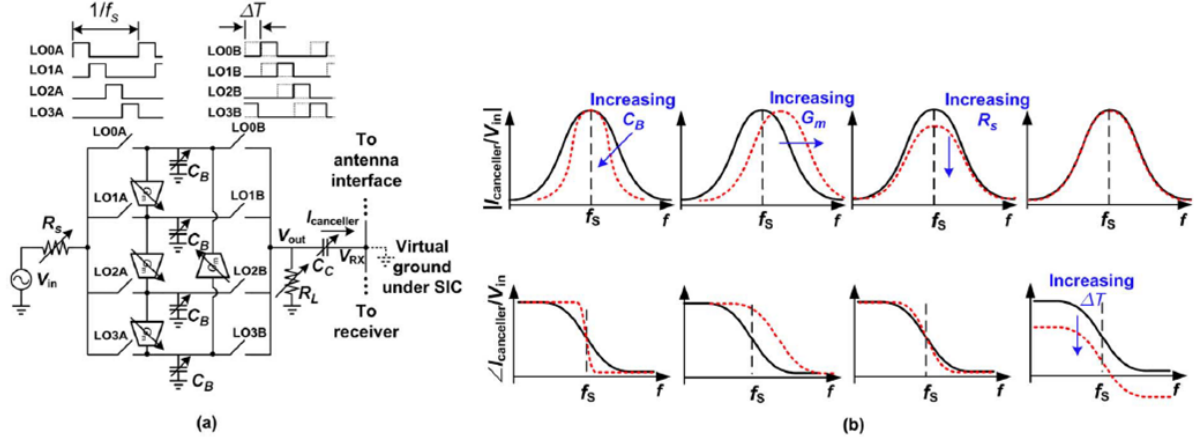


Figure 3.3: Two-port  $G_m - C$  N-path filter implementation with embedded variable attenuation and phase shift. (a) Block diagram. (b) Illustration of variable quality-factor (group delay), frequency shift, attenuation, and phase shift [2].

where  $R_{on}$  is the on-resistance of the N-path switches,  $f_s$  is the switching frequency, and the loading effect of  $C_C$  is ignored.

### 3.4 Design Consideration for LO-Path Phase Shifter Design

For a narrow-band system, the true time delay of an input signal can be approximated as a phase shift at its center frequency. An analog method of implementing a phase shift is vector-modulator-based phase shifter. A vector-modulator-based phase shifter, as shown in Fig. 3.4 assigns a phase shift to an existing in-phase/out-of-phase input signal by weighting the I/Q signals differently and summing these at the output to produce the desired phase shift. For an LO signal, typically the I and Q pair can be generated by frequency divider, RC-CR or poly-phase networks. Variable-gain amplifiers (VGAs) are often used to implement the vector modulator cell. By toggling the biasing current or switching the load of the VGA, the weighting on its input signal can be effectively applied. In comparison, digital

phase rotators combine a multi-phase generator with a MUX at the output to select the desired phase. To increase its resolution of phase shift, either the number of phase of the multi-phase generator must be increased or the output signal of the MUX requires further interpolation at the expense of system complexity. Due to the system complexity and phase resolution requirement, a VGA-based vector modulator [57] was chosen for the proposed design for the LO-path phase shifter implementation.

### 3.5 Proposed LO-Path Design for the N-path-Filter-Based Self-Interference Canceller

The proposed LO path design for an N-path-filter-based self-interference canceller is shown in Fig. 3.4. The differential LO input from the transmitter side is first divided by two to generate differential I/Q signals. The aforementioned proposed N-path-filter-based canceller requires two sets of 25% duty-cycle non-overlapping LO signals for its mixers. The output signals of the divider split into two paths. The non phase-shifting path comprises a 25% duty-cycle generator to generate the non phase-shifting version of the LO. The phase-shifting path comprises a slew-rate control filter, two sets of vector-modulator-based phase shifters, and another 25% duty-cycle generator. The purposes of inserting slew-rate-control RC filters is to attenuate the harmonics at divider output to ensure the linearity of the subsequent vector interpolators at the cost of potential (phase) noise degradation.

### 3.6 Simulation Result of the Proposed LO Path Design

Fig. 3.5(a) shows the simulation result of ideal phase shift vs. the simulated phase shift from 0-45 degrees or the vector-modulator-based phase shifter. Fig. 3.5(b) plots the error between the simulated phase shift and the ideal phase shift from Fig. 3.5(a). As can be seen, the largest errors in phase shift (pre-layout and post layout) are both smaller than 2.5 degrees, satisfying the required specification for the N-path-filter-based canceller.

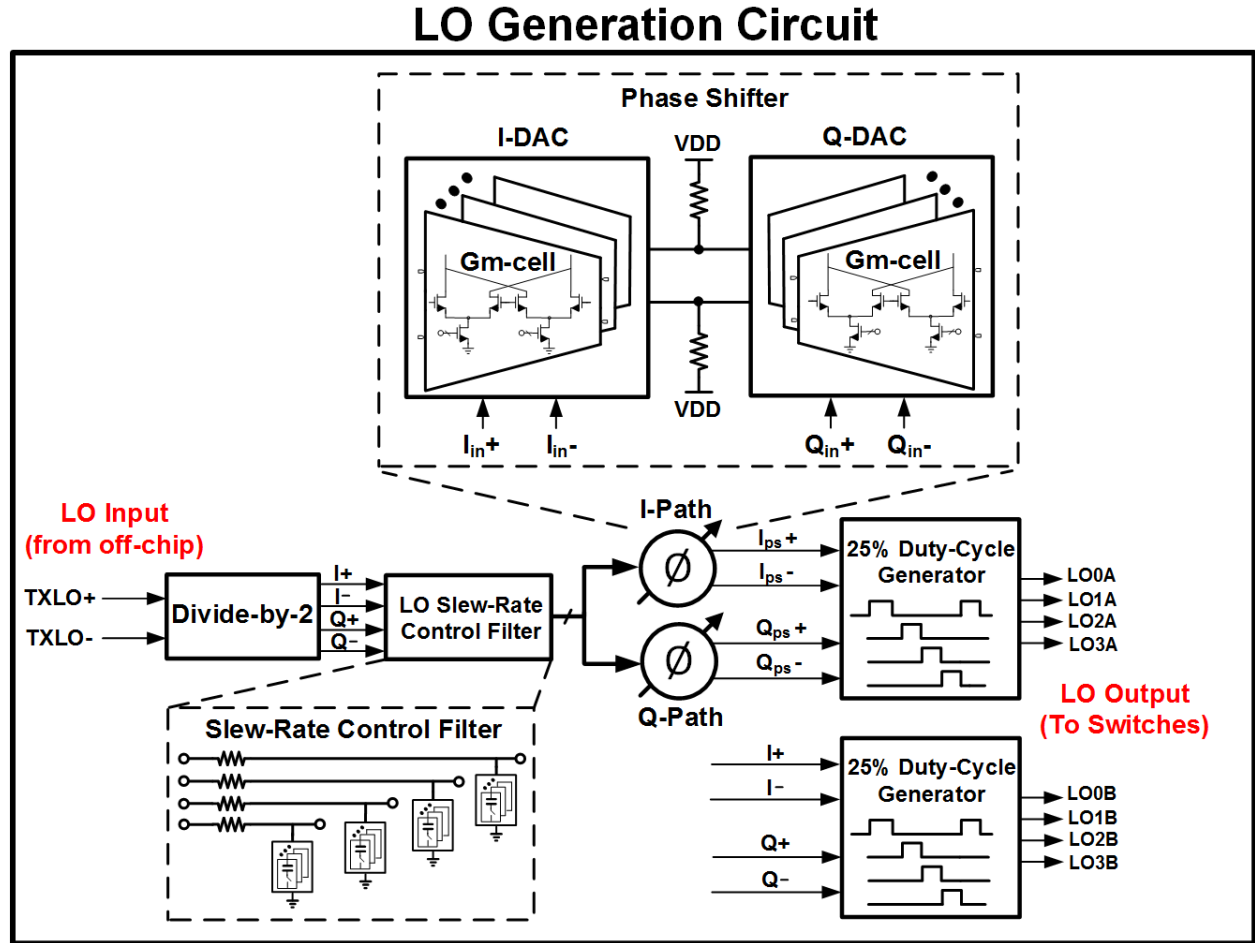


Figure 3.4: Block diagram and schematic of the proposed embedded phase-shifting LO path design.

Fig. 3.7 depicts the simulated frequency response of the  $G_m$  cell of the vector modulator. To enhance the linearity of vector modulation, the BW of the Gm cell is designed such that response at harmonic frequency should be well attenuated and only the response at fundamental input frequency should be preserved. The simulated BW of the Gm cell is around 2GHz with 20dB/decade roll-off.

Fig. 3.6 (a) shows the post-layout simulation of duty-cycle vs. phase shift setting from 0-45 degrees for both the phase-shifting and non phase-shifting path. Fig. 3.6 (b) shows the accuracy of non-overlapping generation between the differential I/Q signals at the output of both the phase-shifting and non-phase-shifting path vs. phase shift settings from 0-45 degrees. As can be seen, the relative time difference between the edges is consistently smaller than a 0.5% error from 0-45 degrees phase-shift setting.

Fig. 3.8 shows the simulation result of rise and fall time for the output signals of both the phase-shifting path and non-phase-shifting path. The generated clock frequency is 1GHz which translates to a 1ns period. For a 25% duty-cycle signal with 20ps rise/fall time, the percentage of rise/fall times over the entire period is about 10%.

Fig. 3.9 shows the Monte-Carlo simulation of the phase shifter at a 45-degree phase shift setting under the impact of device mismatch. The simulation result shows that, even with device mismatch at presence, out of 50 simulation occurrences, the average phase shift is 45.1 degrees and the simulated standard deviation is 1.13 degrees.

Fig. 3.1 shows the breakdown of simulated power consumption for each block in the LO path. The total simulated  $P_{dc}$  is 63.3mW.

Block	Divider	Divider Buffer	Phase Shifter	Phase Shifter Buffer	25% Duty-cycle Generator	Mixer Buffer
Power Consumption	4.4 mW	7.2 mW	23.6mW	7.6 mW	4.9 mW	14.9mW

Table 3.1: Breakdown of power consumption for the proposed embedded-phase-shifting LO path.

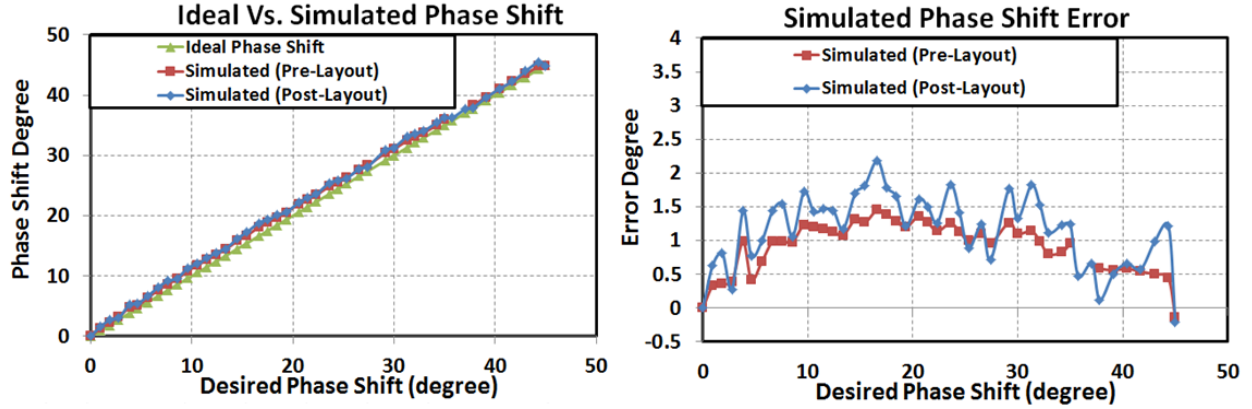


Figure 3.5: (a) Ideal phase shift vs. simulated phase shift (b) Error between simulated phase shift and ideal phase shift from 0-45 degrees for the vector-modulator-based phase shifter.

### 3.7 65nm CMOS Radio Prototype and Highlighted System-level Measurement Result [2]

A canceller bank of two reconfigurable second-order  $G_m$ -C N-path filters with a 0.81.4 GHz reconfigurable current-mode RX was implemented in a 65 nm standard CMOS process. The block diagram is shown in Fig. 3.10. The canceller filters have separate LO and TX replica signal inputs, leading to flexibility in their use (e.g., cancellation of two separate TX signals for MIMO applications). A noise-canceling common-gate (CG), common-source (CS) low-noise transconductance amplifier (LNTA) is followed by 4-phase current-driven passive mixers and baseband TIAs [58]. Programmable baseband recombination circuits combine the RX outputs from the CG and CS paths for noise cancellation [58], [59].

The chip micro-photograph shown in Fig. 3.11 has an active area of  $4.8\text{mm}^2$ . The chip is wire bonded and packaged in a QFN package, and mounted on a PCB for all measurements.

For FDD, the SI canceller enables the usage of a custom designed LTE-like duplexers employing surface-mount-device based second-order LC filters with TX band isolation as small as 30 dB, which is 25 dB relaxed compared to commercial SAW/FBAR duplexers. The TX and RX 1 dB BWs are 762798 MHz and 872918 MHz, as shown in Fig. 3.12. The highly selective duplexer has a peak isolation group delay of 11 ns and 7 dB magnitude

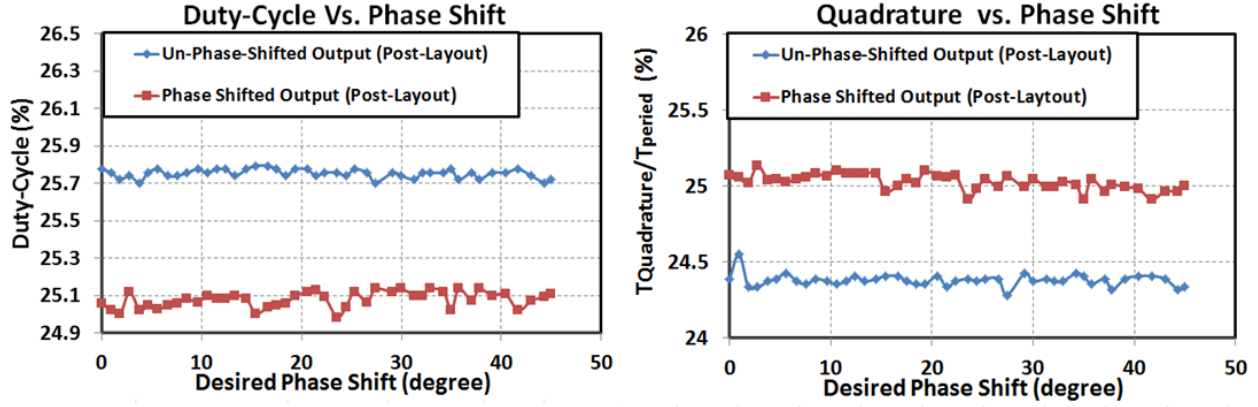


Figure 3.6: (a) Post-layout simulation of duty-cycle vs. phase shift setting (b) Accuracy of non-overlapping generation between the differential I/Q signal from 0-45 degrees.

variation across the TX band. The measured TX/RX isolation with SIC is shown in Fig. 3.13.

The SI canceller achieves a 20 dB cancellation BW of 17/24 MHz for one/two filters enabled, while a conventional frequency-flat amplitude and- phase-based canceller has a 20 dB SIC BW of only 3 MHz. Note that in measurement, the two canceller filters share the same LO, namely the TX LO frequency that is set at the center of the TX band. The  $G_m$  cells are used to impart frequency shifts. The associated NF increase is only 0.5/0.6 dB due to noise filtering, as the NF degradation is lower in the FDD region, i.e., in the vicinity of the RX frequency rather than in the vicinity of the TX frequency.

### 3.8 Conclusion and Future Work

This chapter showcases an alternate method of employing an I/Q interpolator-based phase shifter in modern radio design. The functionality of phase shifters are embedded in the LO path design for the radio and the embedded phase-shifting capability enables the radio to perform self-interference cancellation with minimum complexity and design overhead.

A two-port N-path  $G_m$ -C filter with embedded variable attenuation and phase shifting was proposed for implementing the second-order high-Q BPF. Due to the system complexity

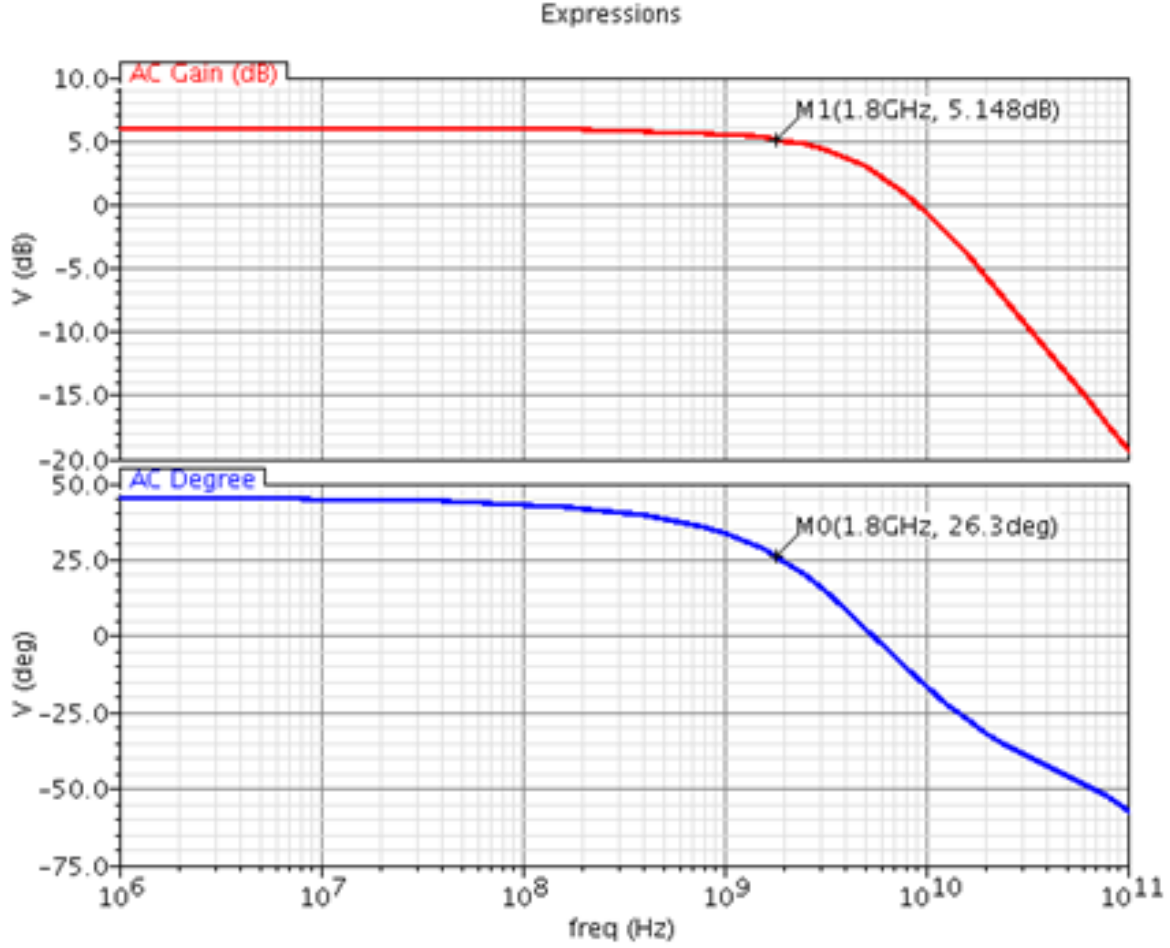


Figure 3.7: Simulated frequency response of the vector-modulator  $G_m$ -cell.

and phase resolution requirements, a VGA-based vector modulator was chosen for our design of the LO-path phase shifter implementation. The simulation result of the LO path design as well as the measurement result of the overall self-interference cancelling receiver were presented.

One potential future research direction is to incorporate digital phase rotator or digital-to-phase converter [42] for the embedded phase-shifting LO path. Currently, the I/Q signals for the vector modulator are generated by a preceding divide-by-2 circuitry. The output of the digital divider is in the form of square-wave while the  $G_m$ -cell-based vector modulator prefers sine-wave input to perform linear vector summation. The current solution incor-

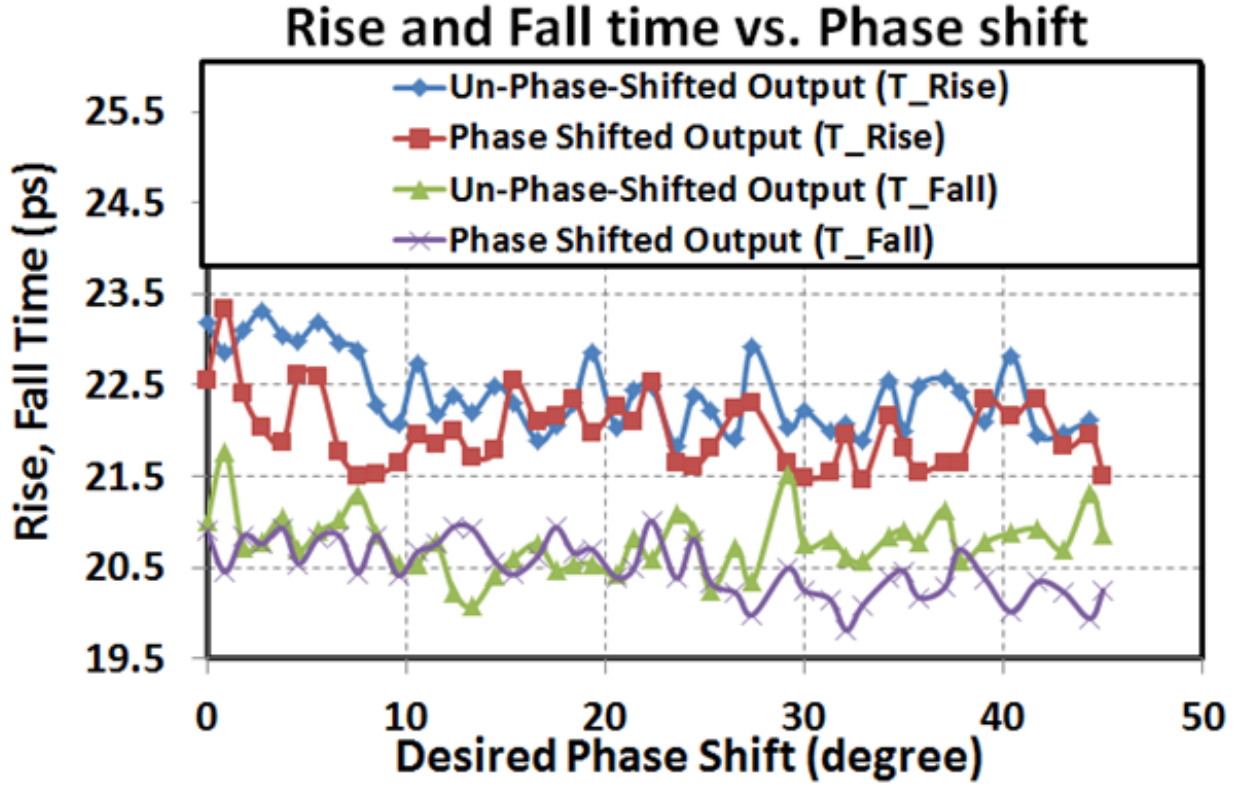


Figure 3.8: Simulated rise and fall time for the output signals of both phase-shifting path and non-phase-shifting path.

porates a slew-rate controller to mitigate the non-linearity due to the square-wave input. However, to drive the mixer at the output, buffering the output of the vector modulator output is again required to convert the sine-wave back to square-wave. This process inevitably increases power consumption and induce phase noise penalty to the overall system. Therefore, a digital-to-phase converter with sufficient resolution could be an ideal candidate for our system.

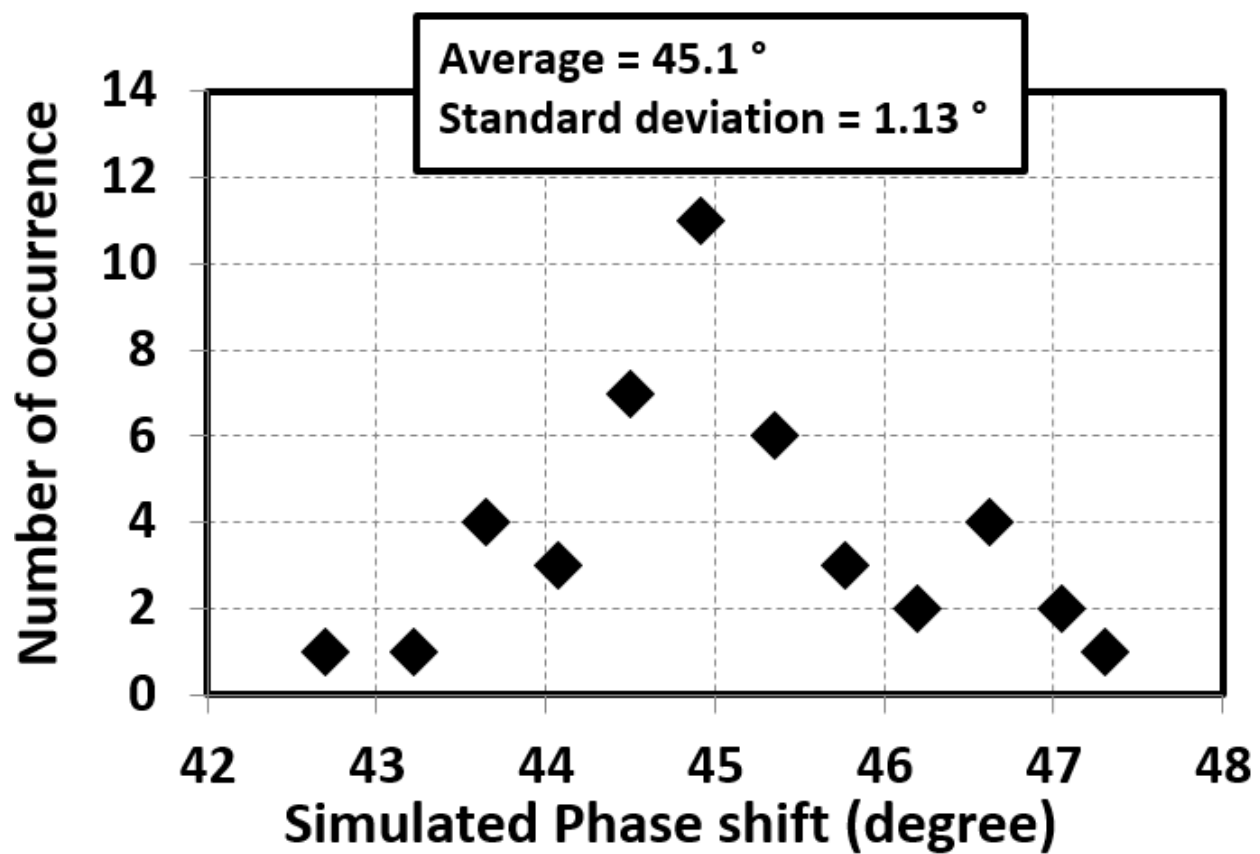


Figure 3.9: Monte-Carlo simulation of the phase shifter at 45-degree phase shift setting under the impact of device mismatch.

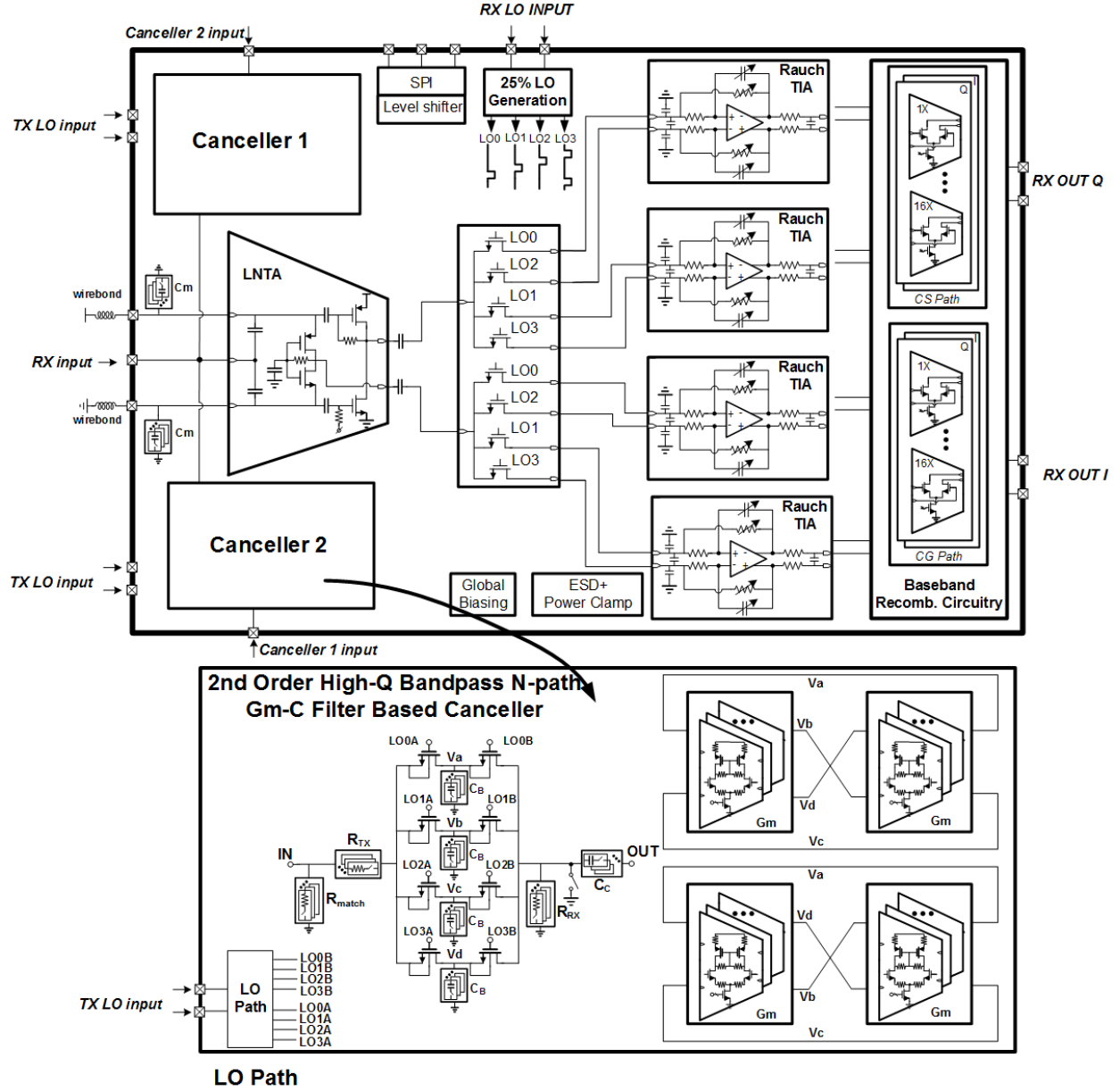


Figure 3.10: Block diagram and schematic of the implemented 0.81.4 GHz 65 nm CMOS RX with FDE-based SIC in the RF domain featuring a bank of two filters [2].

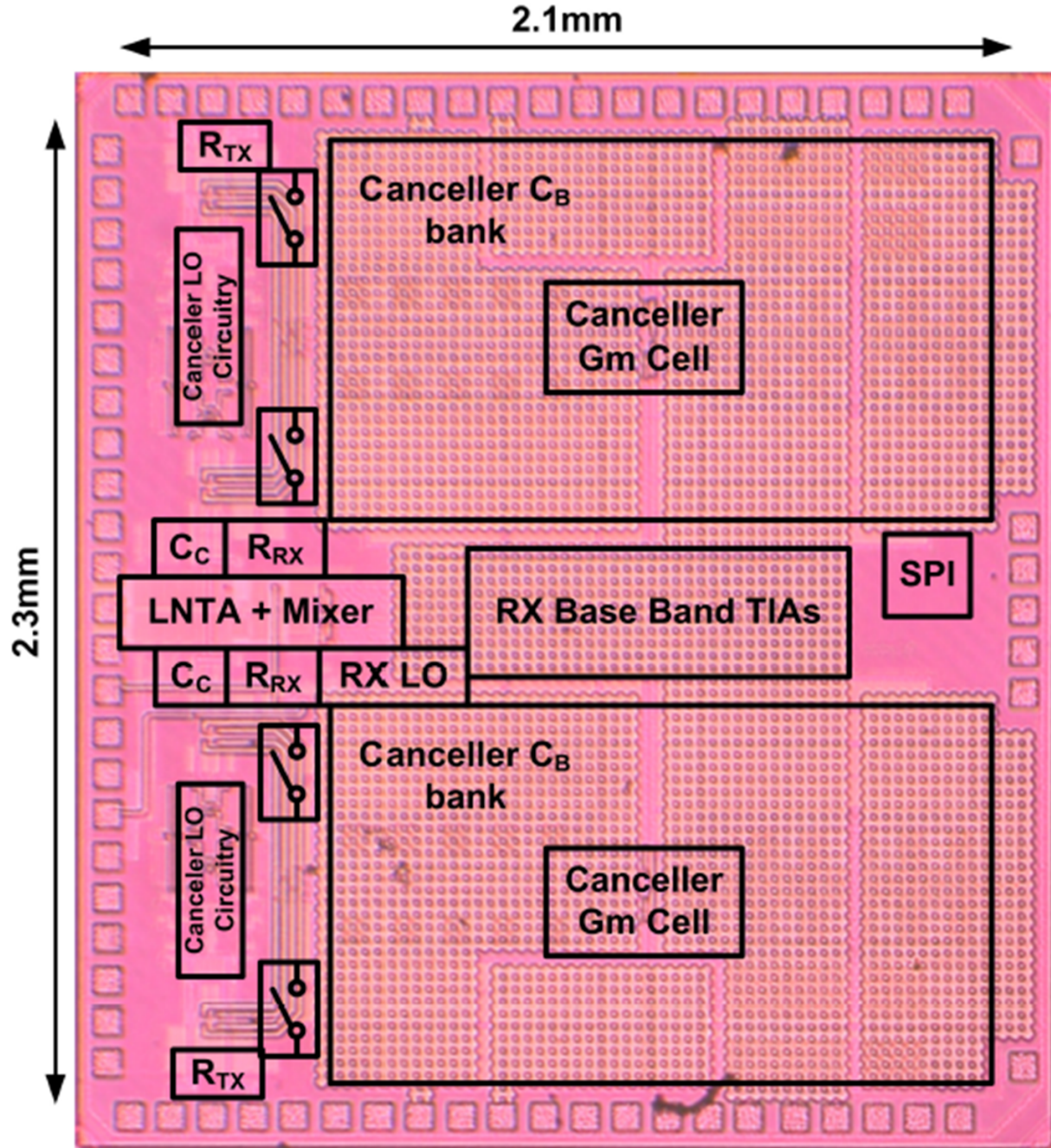


Figure 3.11: Chip microphotograph of the 65 nm CMOS 0.81.4 GHz SI-cancelling RX.

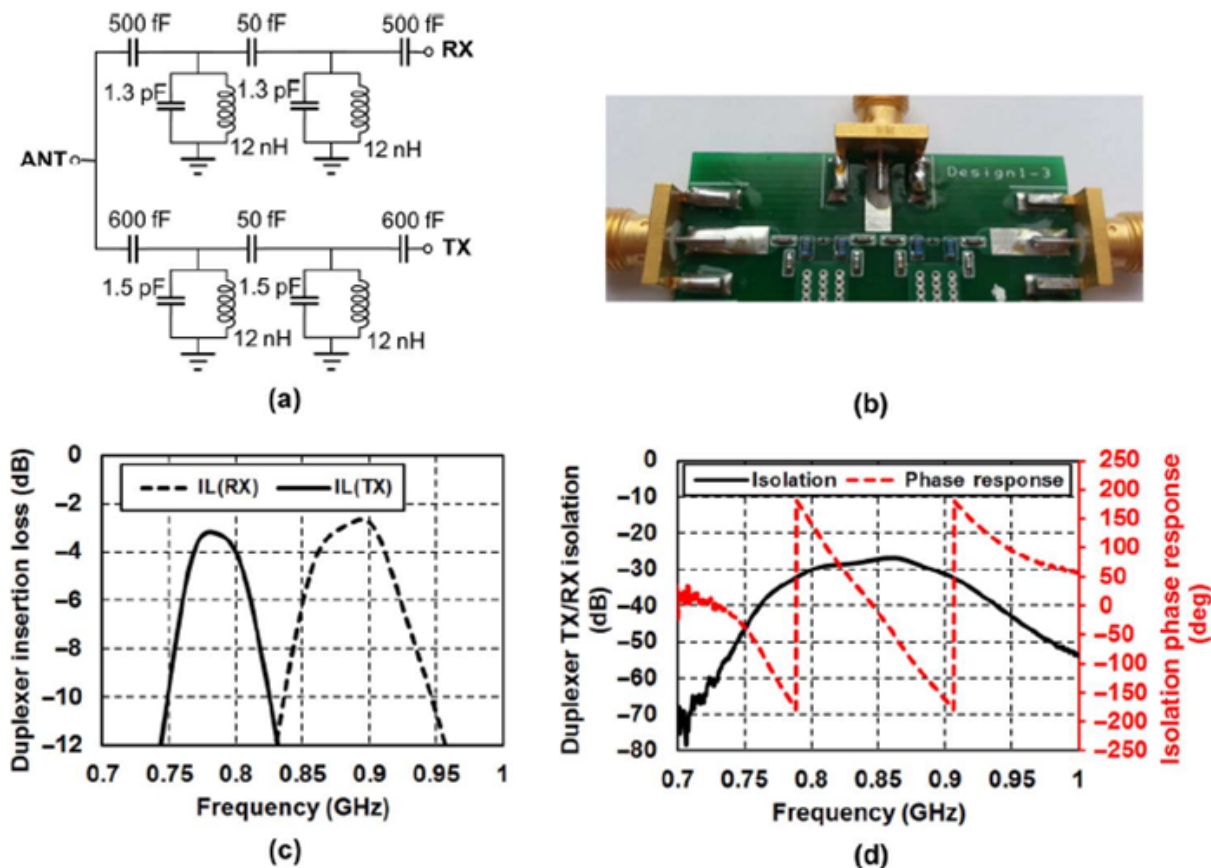


Figure 3.12: Custom-designed LTE-like 0.780/0.895 GHz duplexer employing surface-mount-device-based second-order LC filters: (a) schematic; (b) duplexer photo; (c) measured duplexer insertion loss; and (d) measured duplexer TX/RX isolation magnitude and phase response [2].

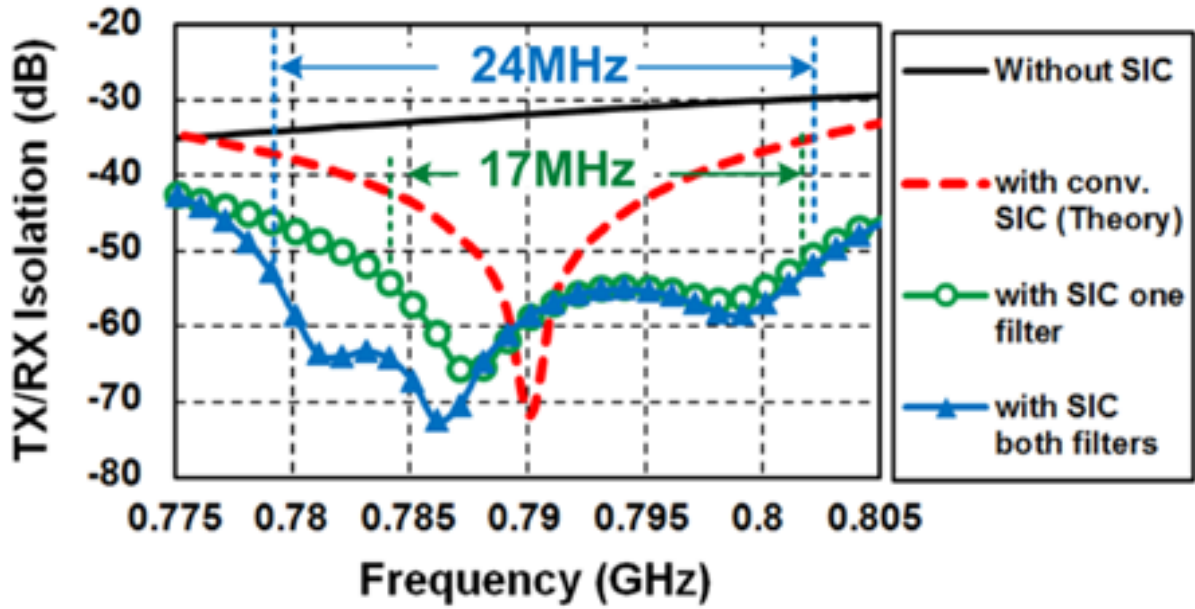


Figure 3.13: Measured TX/RX isolation of the FDD LTE-like duplexer shown in Fig. 3.12 without SIC, and with the proposed SIC. The proposed SI canceller achieves a 20 dB cancellation BW of 17/24 MHz for one/two filters enabled, while a conventional frequency-flat amplitude- and phase-based canceller has a theoretical 20 dB SIC BW of only 3 MHz [2].

## Chapter 4

# Design of Ultra-low Form-factor and Low-noise Ring Oscillator-based PLL

### 4.1 Introduction

High-performance phase-locked loops (PLLs) with low jitter/phase noise are essential for numerous applications such as wireless radios, high-speed data converters, wireline communication links and digital systems-on-chip (SoCs). Given the increasing cost per unit area of advanced CMOS nodes and the need for a multitude of PLLs in multi-band, multi-standard radios and complex SoCs, low-area PLLs with excellent jitter and phase noise performance are of critical interest.

Ring oscillators are extremely compact when compared with their LC counterparts, but exhibit typically 15-20dB worse phase noise figure-of-merit (FoM) performance [19, 60, 61]. In digital SoCs, different building blocks such as microprocessors, memories, and I/O interfaces require separate PLLs, and the ring-oscillator-based analog charge-pump PLL has conventionally been deployed to generate the clocks for such systems [6, 62]. Ring-oscillator-based PLLs (RO-PLLs) do not yet meet the challenging phase noise specifications of wireless standards. Therefore, circuit techniques to improve or compensate for the phase noise performance of RO-PLLs has been an active area of research [19–22]. As research to improve

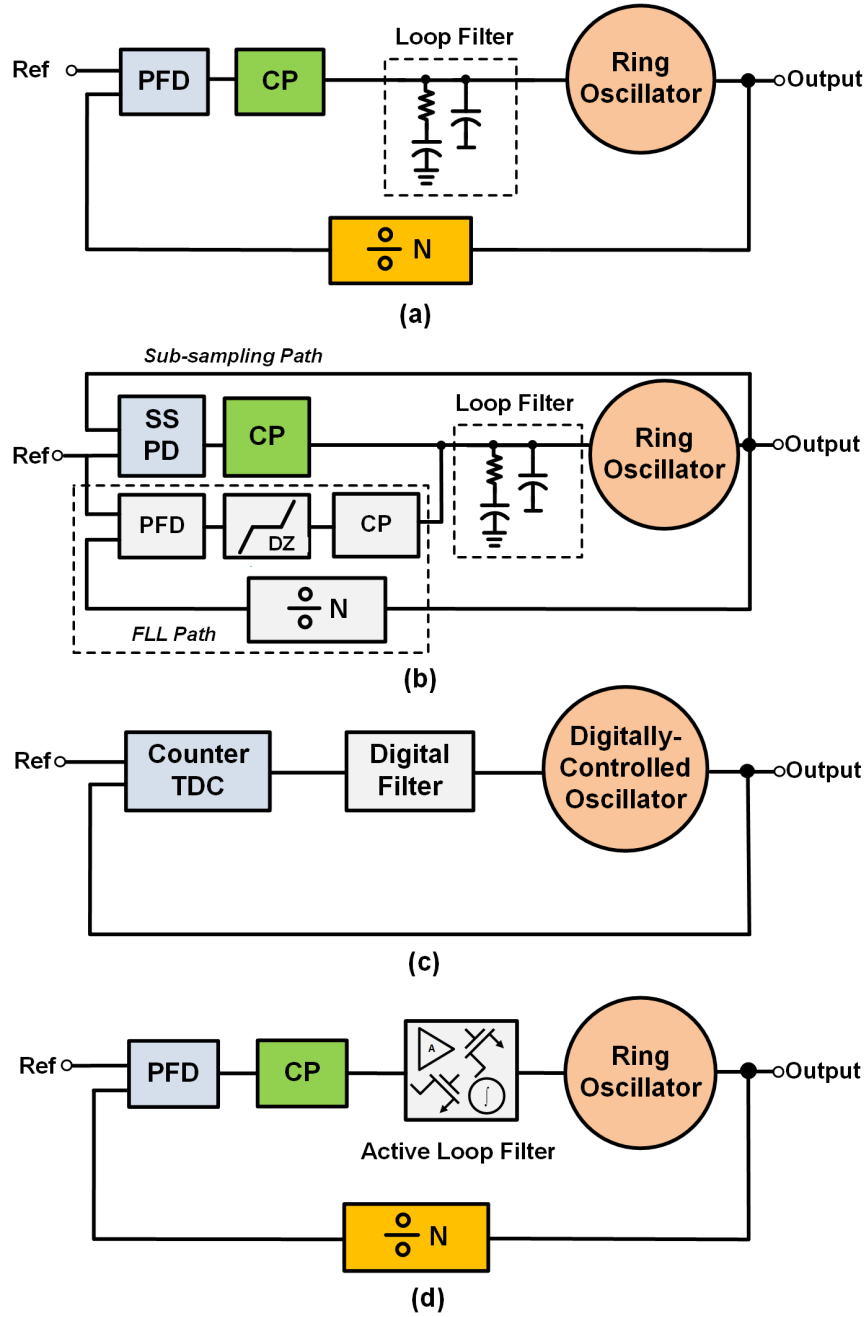


Figure 4.1: Conventional ring-oscillator-based PLL architecture comparison: (a) Analog charge-pump PLL with passive loop filter. (b) Sub-sampling analog charge-pump PLL. (c) All-digital PLL. (d) Analog PLL with active loop filter.

the phase noise performance of RO-PLLs continues, pathways to further reduce the area of RO-PLLs becomes a crucial topic.

The analog charge-pump PLL with a passive loop filter, shown in Fig. 4.1(a), has been the dominant RO-PLL architecture. Although a low-noise design can be realized [63], it requires large loop-filter capacitors to achieve a desirable frequency response, which dominate the area .

The analog sub-sampling PLL [64, 65], shown in Fig. 4.1(b), removes the feedback divider of the PLL so that the low-frequency reference directly samples the high-frequency oscillator output to perform a phase comparison. In such a configuration, the phase noise of the loop components preceding the high-frequency oscillator (except the reference signal and its buffer) will not be multiplied by  $N^2$ , where  $N$  is the division ratio. This dramatically lowers the in-band phase noise of the PLL. However, to achieve comparable loop dynamics with the conventional divider-based analog charge-pump PLL, it requires an even larger loop-filter capacitor. This concern can be addressed by incorporating a gain control mechanism in the sub-sampling phase detector (SSPD) and charge-pump, such as duty-cycling or pulsing. While lowering in-band phase noise, it does not fundamentally address the chip area associated with the passive loop filter in an analog charge-pump PLL.

Thanks to technology scaling, all-digital PLLs [28, 31, 66], shown in Fig. 4.1(c), are extremely compact and well-suited for SoC integration. In addition, the all-digital PLL offers superior loop reconfigurability since the loop filter is implemented in the digital domain and its design parameters can be easily reprogrammed. In order to achieve comparable jitter performance to analog PLLs, high-resolution time-to-digital converters (TDCs) and digitally-controlled oscillators (DCOs) are indispensable. While the resolution of the DCO can be improved by techniques such as inserting a preceding delta-sigma modulator [67], the resolution of the TDC is fundamentally related to the minimum resolvable delay in the technology node. Novel TDC architectures incorporate techniques such as a Vernier delay-line to address this challenge [68]. However, the jitter performance of state-of-art all-digital-PLLs still lag behind their analog counterparts [31].

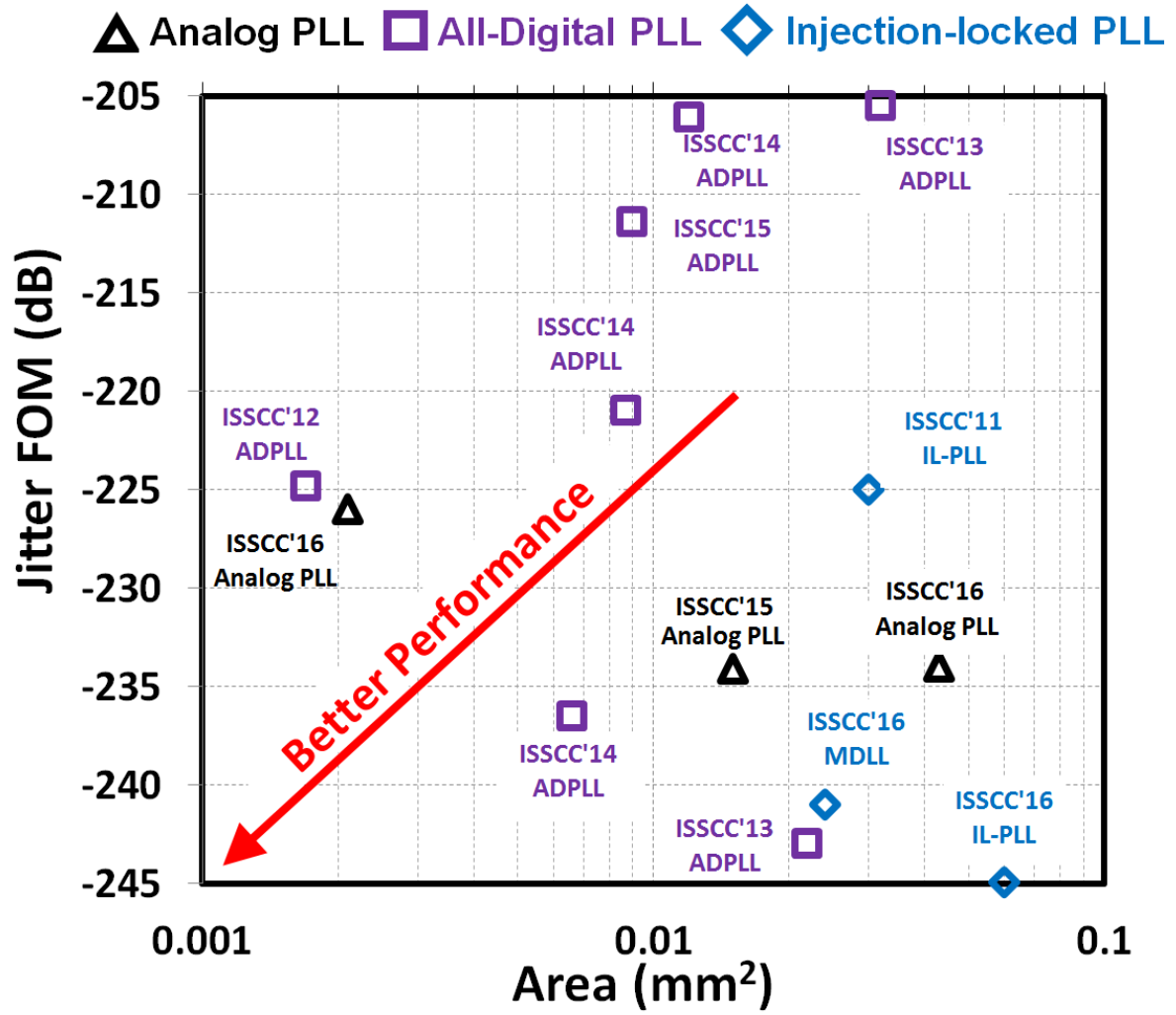


Figure 4.2:  $FoM_J$  versus area for state-of-art ring-oscillator-based clock generation works.

To overcome the limited bandwidth over which the ring oscillator's phase noise is suppressed in a traditional PLL, the jittery ring oscillator's clock edge is periodically replaced by a clean reference signal edge in a multiplying delay-locked loop (MDLL) [69]. However, such operation requires precise logic for edge selection, and the jitter performance can degrade as the ring oscillator's operating frequency increases. Injection-locked PLLs (IL-PLLs) [70, 71], on the other hand, are not plagued by the stringent timing requirements of MDLLs. However, the injection-locking bandwidth of the ring oscillator needs to be wide enough to compensate for PVT variations in the oscillation frequency, necessitating strong injection. A large injection strength of the reference signal can compromise reference spur performance [72]. Moreover, typical IL-PLLs operate in type-I fashion which can limit the in-band noise suppression of the ring oscillator [69].

Active loop-filter-based PLLs, shown in Fig. 4.1(d), can substantially lower the area requirements, but they are associated with linearity and (phase) noise penalties arising from the use of active transistors, which are further exacerbated as CMOS technology scales [73, 74]. Fig. 4.2 highlights the jitter-FoM [75] and area performance of recent RO-PLLs across these different architectures. The definition of  $FoM_J$  is:

$$FoM_J = 10 \log \left[ \left( \frac{\sigma_t^2}{1s} \right) \times \left( \frac{P_{dc,PLL}}{1mW} \right) \right] \quad (4.1)$$

where  $\sigma_t$  is the integrated jitter of the PLL and  $P_{dc,PLL}$  is the DC power consumption of the PLL. As can be seen, achieving excellent jitter-FoM and low area simultaneously remains challenging.

## 4.2 Pathway to low-noise and ultra-compact PLL Implementation

### 4.2.1 Dual-path PLL Architecture

The proposed architecture centers around a ring oscillator to eliminate the area penalty of the VCO inductor, as mentioned earlier. Type-II PLLs are a popular choice in PLL loop design. To stabilize a type-II PLL, a left-half-plane zero is placed below the cut-off frequency to achieve desired loop response. In a single-path PLL design, the zero is often implemented by inserting a resistance  $R_z$  in series with the loop-filter capacitor  $C_1$  (Fig. 4.1(a)). In a typical type-II charge-pump-based PLL design, input/output frequencies (hence, the division ratio) and the gain of the oscillator are often specified by the application, leaving only  $I_{cp}$  (charge-pump current) and loop filter resistor  $R_z$  and capacitor  $C_1$  as design degrees of freedom (assuming gain of the phase/frequency detector is a unit-less constant). This poses several design challenges [25]. (i) Charge-pump current and its noise directly trade off with loop filter impedance value (capacitor size). If the charge-pump current is increased to minimize its noise contribution, the loop filter impedance has to be inevitably reduced, and its capacitor value will increase at the expense of chip area. (ii) The loop is sensitive to VCO tuning-curve non-linearity. To maintain the same loop response across a range of output frequencies, the gain variation of the VCO analog tuning-curve must be compensated by programming charge-pump current and loop filter impedance. However, in a single-path PLL design, such a method can be carried out with limited freedom and will affect the overall noise performance.

On the other hand, a dual-path PLL architecture, shown in Fig. 4.3(a), offers many design advantages over its single-path counterpart. First of all, it introduces a degree of freedom in choosing the resistor value with a gain stage such that the location of the zero can be optimized. In addition, it enables independent control of the integral and proportional path to adjust the loop response across the nonlinear gain profile of the oscillator and PVT variations [76–78].

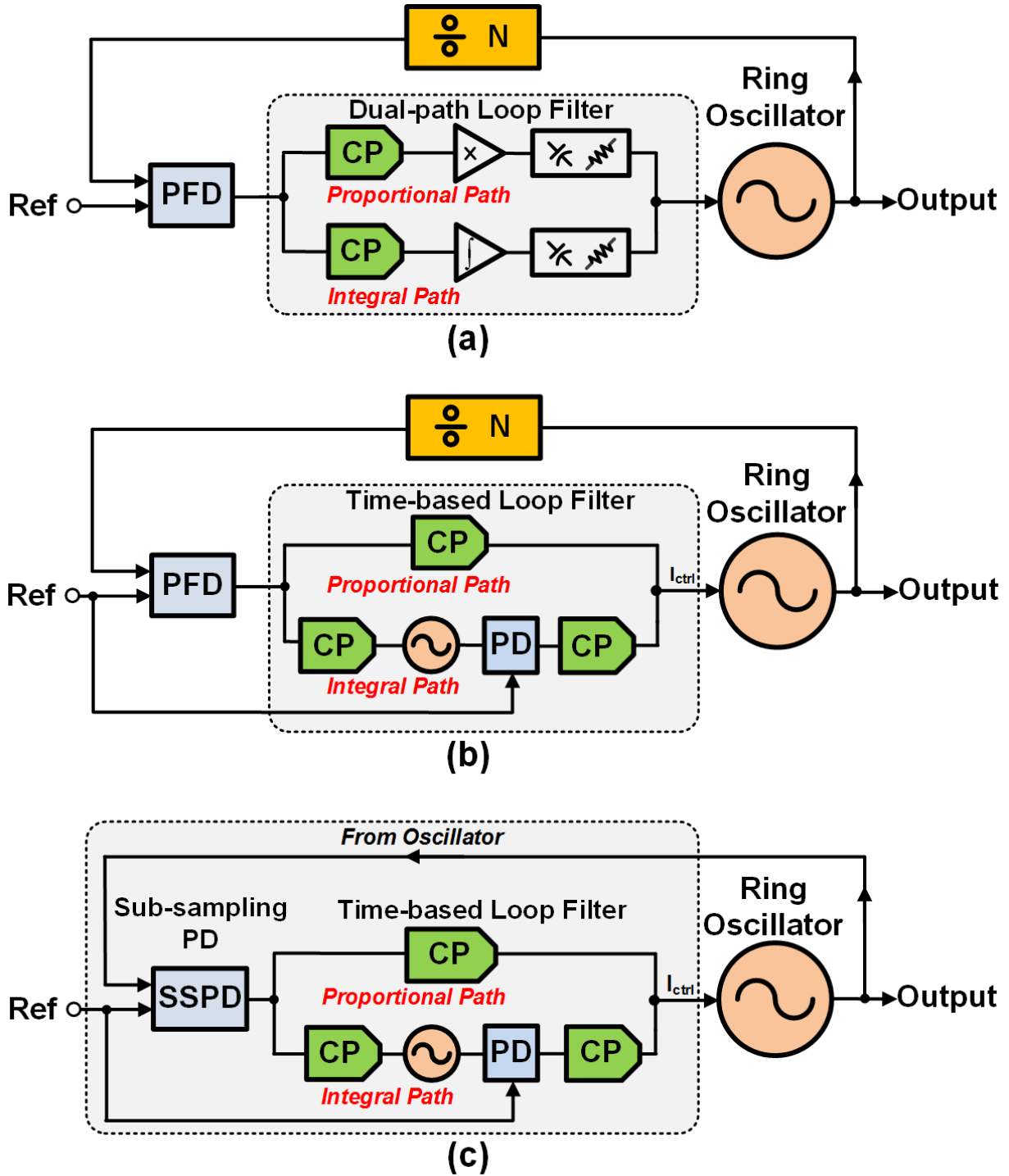


Figure 4.3: (a) Generic dual-path PLL architecture. (b) Dual-path PLL with active time-based loop filter. (c) Proposed dual-path sub-sampling PLL with time-based loop filter.

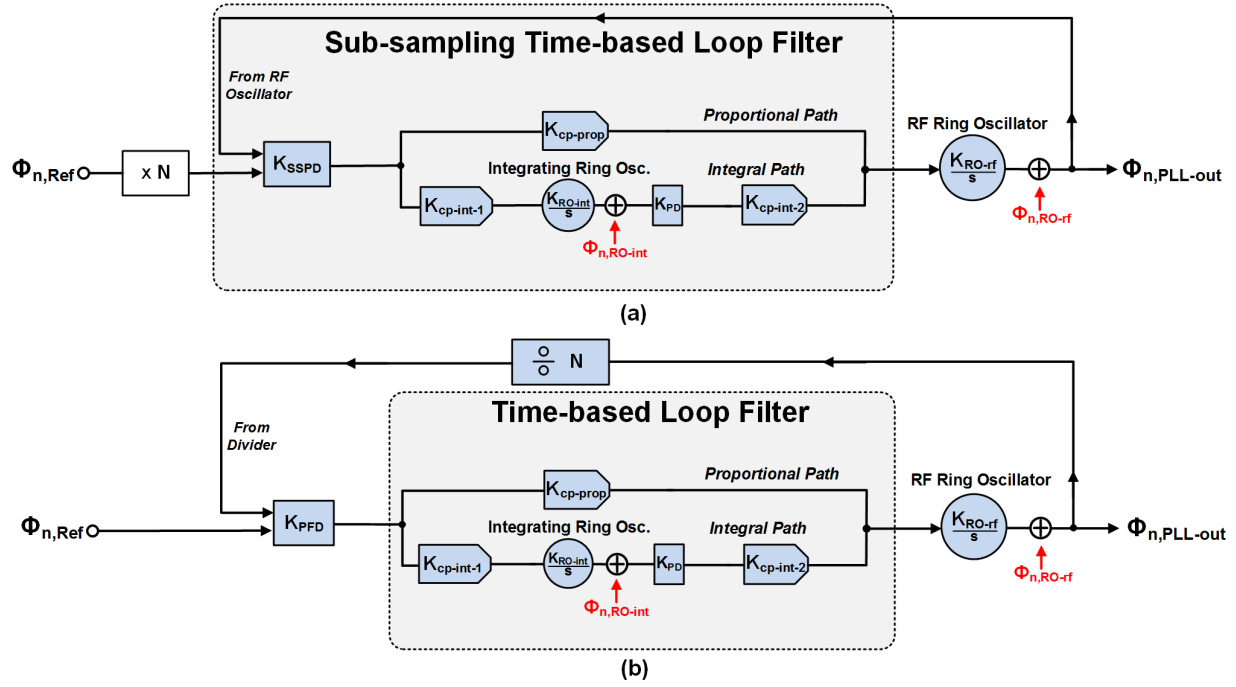


Figure 4.4: (a) Phase-domain small-signal (phase) noise model for proposed PLL. (b) Phase-domain small-signal (phase) noise model for a dual-path PLL with active time-based loop filter (without sub-sampling).

## 4.2.2 Dual-path PLL with Time-based Active Loop Filter Architecture

As cost per unit area of advanced CMOS nodes increase, circuit topologies that further remove the capacitor in the integral path become attractive. Moreover, dual-path loop filter design typically involves a high-gain amplifier to implement the ideal integrator and to sum the output of the two paths. In advanced CMOS nodes, a high-gain amplifier becomes non-trivial to design given supply voltage scaling and reduction in device intrinsic gain.

To address the challenge of implementing ideal integrators in scaled CMOS technology nodes, recently, a ring oscillator-based integrator [79] has been proposed to avoid using voltage-mode amplifiers to form ideal integrators. Instead, a current/voltage-controlled oscillator can integrate its input current/voltage to output phase, and can therefore be viewed as an ideal integrator with infinite DC gain even at low supply voltages and independent of transistor non-idealities. Interestingly, such a ring-oscillator-based integrator has been used to replace passive loop filter capacitor or an active op-amp/Gm-C filter in a conventional analog charge-pump PLL to achieve an ultra-compact PLL [80] (Fig. 4.3(b)).

Though this use of a ring-oscillator-based integrator cleverly addresses the DC gain and voltage-headroom issues in scaled CMOS by shifting the signal processing to the time domain, it inevitably worsens the phase noise performance of the overall PLL. Particularly, it is shown that the in-band phase noise of the PLL will now be dominated by the ring oscillator-based integrator [80].

## 4.2.3 Proposed Sub-sampling Dual-path PLL with Time-based Loop Filter Architecture [3]

We propose a sub-sampling dual-path PLL with the time-based loop filter architecture, shown in Fig. 4.3(c). This architecture is based on the observation that the phase noise of loop components will be not multiplied by  $N^2$  when referred to the PLL output in an analog sub-sampling PLL [64]. As shown in Fig. 4.3(c), the proposed architecture comprises

a sub-sampling loop with the loop filter implemented with an active time-based integrator and charge-pump. The sub-sampling loop lowers the phase noise contribution of the loop components (PFD, CP, and ring oscillator-based integrator) while the ring oscillator-based integrator implemented in a dual-loop architecture achieves the proportional-integral (PI) controlled filter with superior area efficiency. The proposed architecture simultaneously addresses the active loop filter's noise penalty and achieves an area-efficient loop filter implementation with minimal complexity overhead, thus resulting in an ultra-low-area PLL with low phase noise performance.

### 4.3 Phase Noise Analysis of Proposed Architecture

To theoretically illustrate the benefit of the proposed architecture, a phase-domain noise model is shown in Fig. 4.4(a), with output-referred noise of critical blocks annotated. For comparison purposes, the noise model for a PLL with an active time-based loop filter but without sub-sampling [80] is shown in Fig. 4.4(b). The overall phase noise of the proposed PLL,  $\phi_{n,PLL_{out}}$ , can be written as:

$$\begin{aligned} \phi_{n,PLL_{out}} = & \phi_{n,RO-int} \times NTF_{RO-int} \\ & + \phi_{n,Ref} \times N \times \frac{LG(s)}{1 + LG(s)} \\ & + \phi_{n,RO-rf} \times \frac{1}{1 + LG(s)} \end{aligned} \quad (4.2)$$

where  $\phi_{n,RO-int}$ ,  $\phi_{n,Ref}$ , and  $\phi_{n,RO-rf}$  are the phase noise of the integrating oscillator, reference signal, and RF ring oscillator, respectively. The phase noise of sub-sampling phase detector (SSPD), phase detector in the integral path, and charge-pumps in the integral and proportional path are ignored for simplicity. This is to highlight the dominant noise contribution of the integrating oscillator in the integral path.  $LG(s)$  and  $NTF_{RO-int}$  are the loop gain and the noise transfer function (NTF) of the integrating ring oscillator to the PLL output, respectively.  $N$  is the (virtual) division ratio.  $NTF_{RO-int}$  can be expressed as:

$$NTF_{RO-int_{proposed}} = \frac{K_{PD} \times K_{CP-int-2} \times \frac{K_{RO-rf}}{s}}{1 + LG(s)} \quad (4.3)$$

where  $K_{PD}$  is the phase-detector gain and  $K_{CP-int-2}$  is the phase-to-current gain of the second charge-pump in the integral path.  $K_{RO-rf}$  is the gain of output RF ring oscillator.  $LG(s)$  can be expressed as:

$$LG(s) = K_{SSPD} \times LF(s) \times \frac{K_{RO-rf}}{s} \quad (4.4)$$

where  $K_{SSPD}$  is the sub-sampling phase detector gain and  $LF(s)$  is the equivalent loop filter response of the proposed PLL.  $LF(s)$  can further be expressed as

$$LF(s) = K_{cp-prop} + K_{cp-int-1} \times \frac{K_{RO-int}}{s} \times K_{PD} \times K_{cp-int-2} \quad (4.5)$$

where  $K_{cp-prop}$  is the gain of the charge-pump in the proportional path,  $K_{cp-int-1}$  is the gain of the first charge-pump, and  $K_{RO-int}$  is the gain of the integrating ring oscillator. For a PLL with an active time-based loop filter but without sub-sampling, shown in Fig. 4.4(b), all the aforementioned equations hold, except that  $K_{SSPD}$  must be replaced with  $K_{PFD}$ , the phase-frequency detector gain,  $LG(s)$  has an extra division by  $N$ , and the virtual multiplication of the reference phase noise by  $N$  in (4.2) needs to be eliminated.

$K_{SSPD}$  is typically much larger than  $\frac{K_{PFD}}{N}$ .  $K_{PFD}$  is  $\frac{1}{2\pi}$  if implemented as a resettable D flip-flop, and  $N$  is typically much larger than one. On the other hand, for a sub-sampling phase detector that samples a square-wave ring oscillator signal with finite rise/fall time, its gain,  $K_{SSPD}$ , can be characterized as

$$K_{SSPD} = \frac{\delta V}{\delta \phi} \times DT_{REF} = \frac{DT_{REF}}{2\pi f_{osc}} \times SL_{osc} \quad (4.6)$$

where  $SL_{osc}$  is the slew-rate of the RF oscillator,  $f_{osc}$  is the oscillation frequency, and  $DT_{REF}$  is the duty-cycling factor of the reference signal. For a 2.4GHz oscillator with a rise/fall time

of 25ps from 0 to 1.2V (a reasonable assumption in 65nm CMOS),  $K_{SSPD}$  is  $\approx 1.6$  (duty-cycling factor = 0.5). If we assume  $K_{PFD} = \frac{1}{2\pi}$  and  $N = 12$ ,  $K_{SSPD}$  is  $\approx 120\times$  larger than the product of  $K_{PFD} \times \frac{1}{N}$ . This will result in substantial suppression of the noise contribution of the time-based loop filter.

For comparison purposes, overall phase noise and noise transfer functions of a conventional type-II third-order PLL (as shown in Fig. 4.1(a)), a time-based loop-filter PLL (as shown in Fig. 4.3(b)) and the proposed PLL (as shown in Fig. 4.3(a)), are simulated and compared in MATLAB with the constraint of having the same loop bandwidth and loop gain (Fig. 4.5(b)). The (phase) noise sources that are included in the simulation are the measured reference phase noise of a Keysight E8257D Analog Signal Generator at 200MHz reference frequency, simulated phase noise for the integrating current-controlled ring oscillator (I-CCRO) and RF CCRO (Fig. 4.5(a)), reference buffer noise and charge-pump noise. Note that charge-pump noise contribution is included in the simulation but not presented in (4.2) since the emphasized and dominant noise source is the phase noise of the integrating ring oscillators. Divider noise is ignored for the conventional PLL and the time-based loop-filter PLL. It should be noted that these noise sources, and the associated power consumptions of the various blocks, are scaled for each PLL based on the requirements dictated by the loop design. A conventional type-II third-order PLL is also included in the simulation for benchmarking purposes based on the noise formulations presented in [75]. Design parameters used for each PLL can be found in table 4.1.

Fig. 4.5(c) shows a comparison of the NTF of the integrating ring oscillator to the PLL output for the time-based loop filter PLL (without sub-sampling) and the proposed PLL. As can be seen, the noise of the integrating oscillator has a bandpass response to the PLL output, and the magnitude is about 17dB lower for the proposed PLL. Fig. 4.5(d) shows the overall phase noise of each PLL for a designed loop bandwidth of 15MHz, along with integrated RMS jitter and jitter FoM numbers. The conventional type-II 3rd-order PLL functions as a benchmark, and it can be seen that the time-based loop filter PLL without sub-sampling exhibits  $\approx 10$ dB worse jitter FoM performance due to the additional noise contributed by the

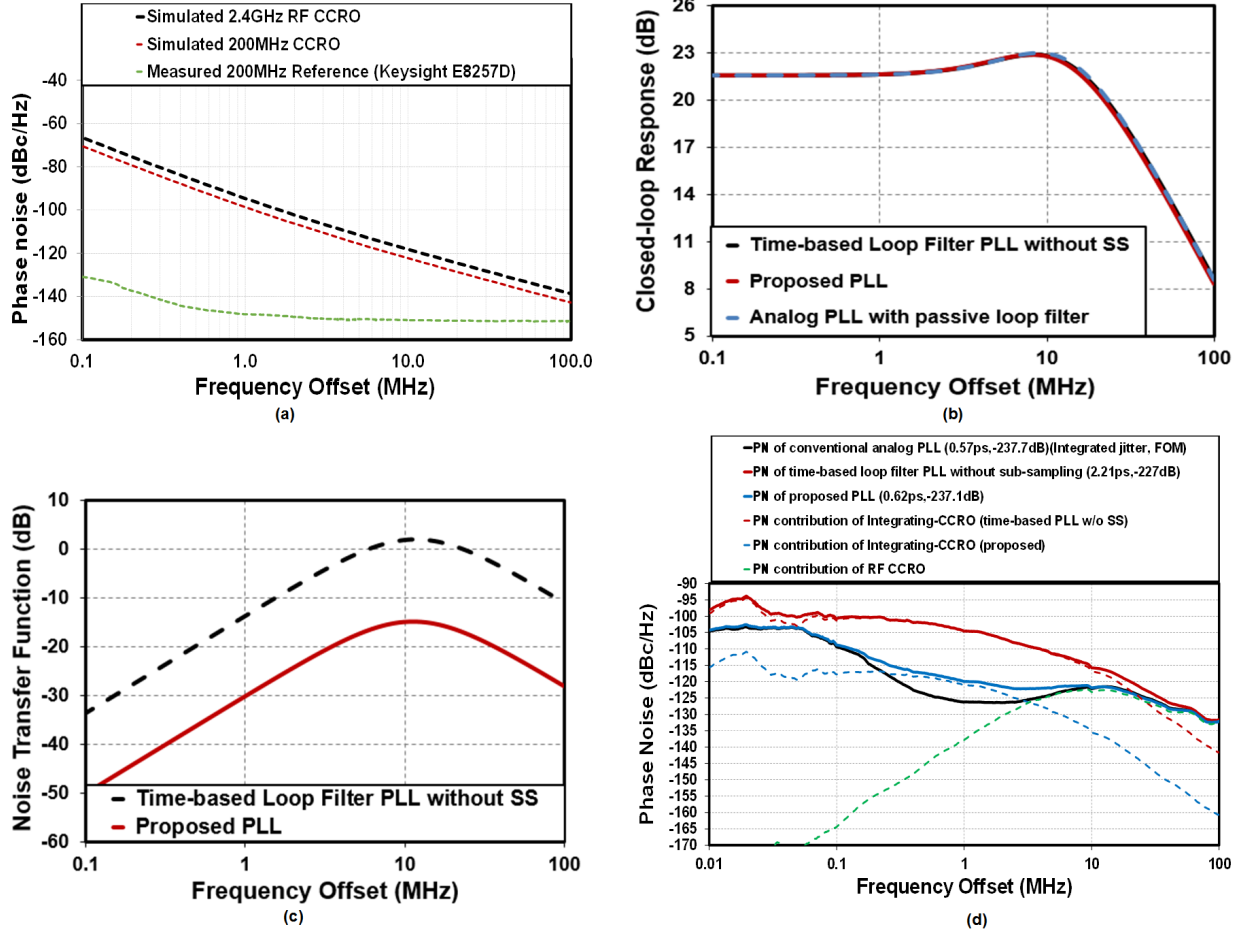


Figure 4.5: Simulated comparison of conventional analog type-II 3rd-order PLL, PLL with active time-based loop filter (without sub-sampling), and the proposed PLL: (a) phase noise of the Keysight E8257D Analog Signal Generator 200MHz reference signal, the RF and the integrating ring oscillators, (c) closed-loop frequency response (b) noise transfer function of Integrating CCRO to the PLL output, and (d) overall phase noise with the contribution of highlighted noise sources.

Table 4.1: Design parameters for the PLL comparison in Fig. 4.5.

	Design Parameter	Conventional Type-II 3rd Order PLL	Time-based Loop-filter PLL without sub-sampling	Proposed time-based Loop-filter PLL without sub-sampling
RF VCO/CCO Parameters	$F_{REF}$	200MHz	200MHz	200MHz
	$F_{VCO}$	2.4GHz	2.4GHz	2.4GHz
	Tuning Gain	$K_{VCO} = 500\text{MHz/V}$	$K_{RO-RF} = 1\text{GHz/mA}$	$K_{RO-RF} = 1\text{GHz/mA}$
	$P_{dc,RF-oscillator}$	2mW	2mW	2mW
Loop Parameters		$I_{cp} = 1\text{mA}$	$K_{cp-int-1} = 0.18 \text{ mA}/2\pi$	$K_{cp-int-1} = 80 \mu\text{A}/2\pi$
		$R_z = 2\text{K}$	$K_{cp-int-2} = 0.18 \text{ mA}/2\pi$	$K_{cp-int-2} = 40 \mu\text{A}/2\pi$
		$C_1 = 50\text{pF}$	$K_{cp-prop} = 1.7\text{mA}/2\pi$	$K_{cp-prop} = 110 \mu\text{A}/2\pi$
		Thermal Noise Constant ( $\gamma$ ) = 2	$K_{RO-int} = 2\text{GHz/mA}$	$K_{RO-int} = 2\text{GHz/mA}$
		$g_m/I_d = 2.5$	$P_{RO-int} = 1\text{mW}$	$P_{RO-int} = 1\text{mW}$
		PFD Deadzone = 200ps	$K_{PD} = 1/2\pi$	$K_{PD} = 1/2\pi$
			$K_{PFD} = 1/2\pi$	$K_{SSPD} = 1.6$
Overall Performance	simulated jitter FoM	-237.7dB	-227dB	-237.1dB

I-CCRO. The proposed PLL shows comparable jitter FoM performance to the conventional PLL as the sub-sampling architecture significantly suppresses the phase noise contribution of the I-CCRO.

## 4.4 A 65nm CMOS Implementation

### 4.4.1 Block Diagram of Proposed PLL

Fig. 4.6 shows the block diagram of the proposed PLL. It comprises a sub-sampling (SS) path, a frequency-locked loop (FLL) path with dead zone, a time-based PI-controlled active loop filter and a 9-stage differential RF CCRO. The sub-sampling phase detector (SSPD) is comprised of transmission-gate MOS switches and differential sampling MIM capacitors. The FLL re-purposes the PI-controlled loop filter, and comprises two charge-pumps ( $CP_{FLL-I}$ ,  $CP_{FLL-P}$ ), one for the integral-path and the other providing proportional control by directly pumping current into the RF CCRO.

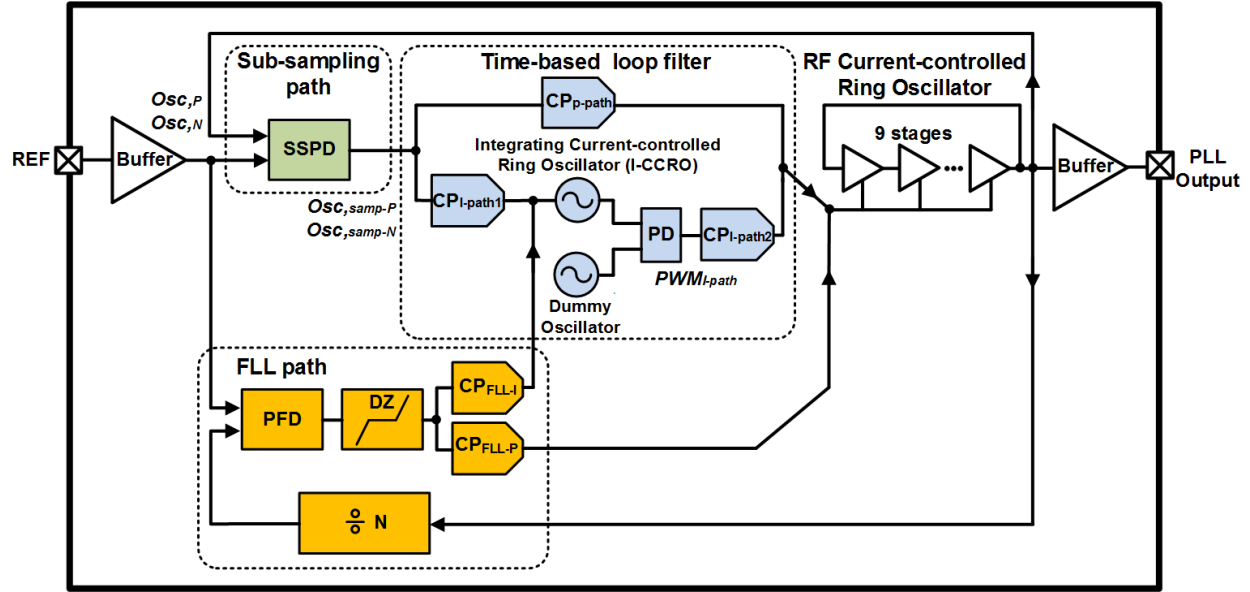


Figure 4.6: Block diagram of the proposed PLL.

Similar to [64], the FLL is designed to assist the locking of PLL. It is initially enabled to ensure that the phase difference between the reference signal and the divider output is smaller than the dead zone. Once inside the dead zone, the FLL is disabled, and the SS path takes over to phase-lock the PLL. To accommodate the sharp rising/falling edges of the ring VCO, the tri-state PFD in the FLL is implemented with a narrow dead-zone [65] ( $\pm 400$ ps) and is tunable from  $\pm 200$ ps to  $\pm 1$ ns.

The delay cell schematic of the 9-stage differential RF CCRO is shown in Fig. 4.7(a). The I-CCRO shown in Fig. 4.6 in the time-based loop filter comprises 11 stages of a similar but resized delay cell. The schematic of the sub-sampling phase detector (SSPD) is shown in Fig. 4.7(b). To be compatible with sub-sampling operation,  $CP_{p-path}$  and  $CP_{I-path1}$  are implemented with V-to-I gm-cells (shown in Fig. 4.7(c)) while  $CP_{I-path2}$  is implemented with a pulse-driven charge-pump cell (shown in Fig. 4.7(d)).

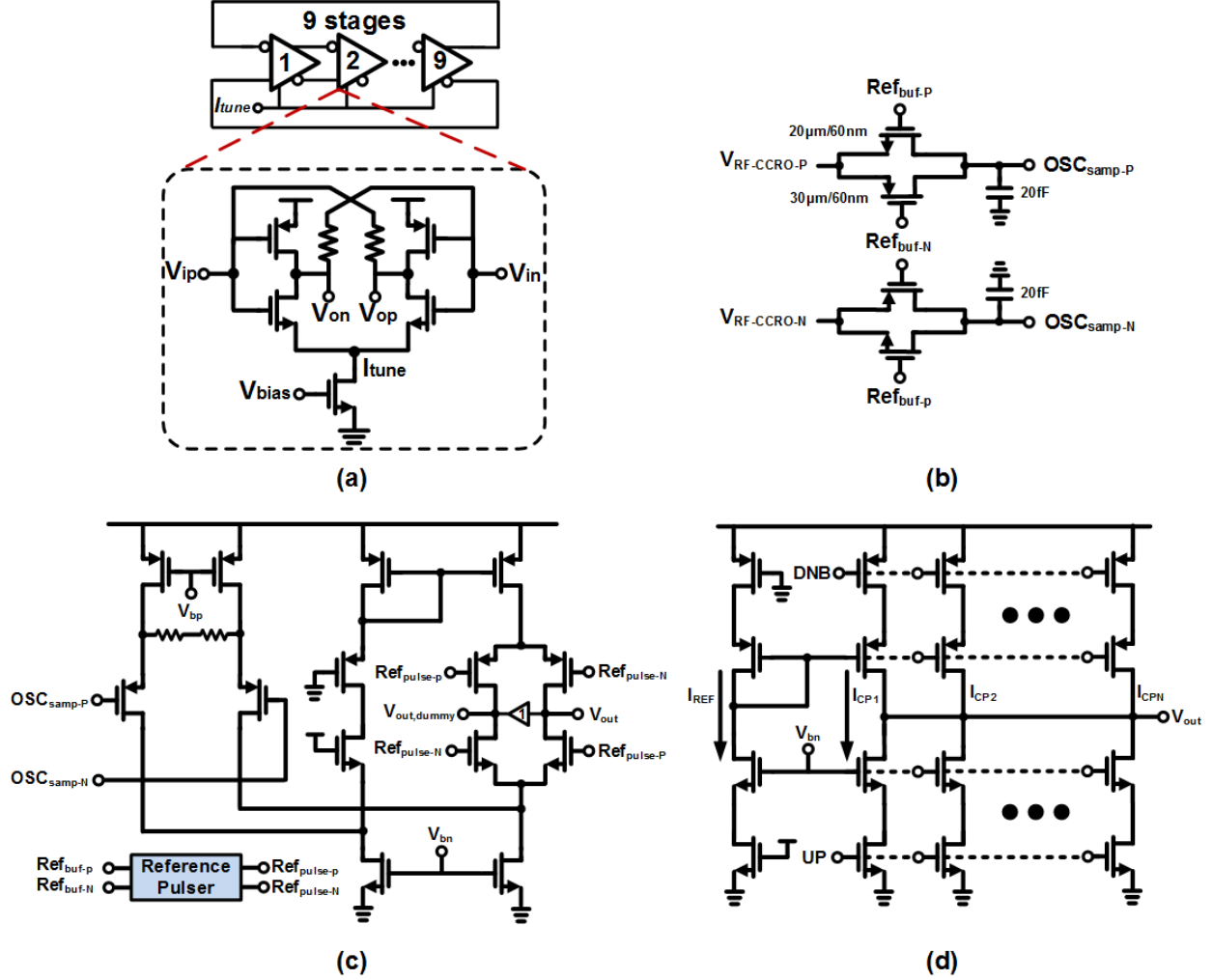


Figure 4.7: Schematics of various components in the proposed PLL: (a) 2.4 GHz 9-stage RF current-controlled ring oscillator (RF-CCRO), (b) sub-sampling phase detector, (c) V-to-I converter (gm-cell) for the sub-sampling path, (d) and charge pump for the time-based integrator path.

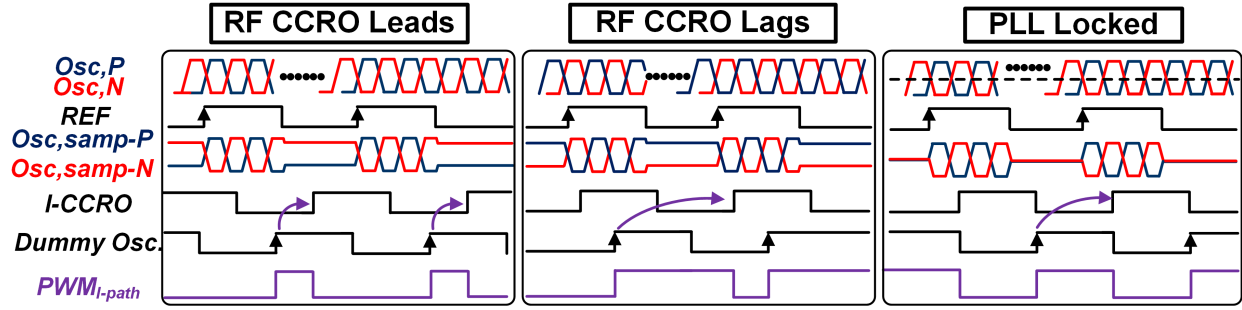


Figure 4.8: Time-domain operation for the proposed PLL.

#### 4.4.2 Time-domain Operation of Proposed PLL

The operation of the time-based PI-controlled loop filter is similar to [80] except that the input information is now taken as the form of sampled small-signal voltage value instead of duty-cycled pulse signal. The integral path comprises two CCROs, one to integrate the charge-pump current to output phase (I-CCRO) while the second dummy oscillator enables a differential phase comparison with the first. Note that in Fig. 4.3(c), reference signal is conceptually used to compare the output phase of I-CCRO through a phase detector. However, a dummy oscillator is implemented here to provide the flexibility to de-couple the reference frequency from I-CCRO's frequency.

The output of integral paths charge-pump is a pulse-width-modulated (PWM) signal ( $PWM_{I-path}$ ) that is combined with the current from the proportional path to drive the RF CCRO. Fig. 4.8 depicts the timing diagrams during operation. The differential RF CCRO signal ( $OSC_P$  and  $OSC_N$ ) is sampled and held by the reference signal (REF) in the SSPD at  $OSC_{samp-P}$  and  $OSC_{samp-N}$ , which further drive the differential charge-pumps in the integral path and proportional path of the time-based loop filter. In the integral path, a difference between  $OSC_{samp-P}$  and  $OSC_{samp-N}$  will cause current to be injected into the I-CCRO, modifying its phase compared to the dummy oscillator through an integration process. Hence, the pulse width of  $PWM_{I-path}$  is dependent on the integral of the difference between  $OSC_{samp-P}$  and  $OSC_{samp-N}$ , establishing integral control.

When the PLL is locked, the output error current of the proportional path should be

ideally zero since the type-II loop should lock without input phase offset. Meanwhile, the integral path output generates an PWM output current whose average value plus the DC current of the RF CCRO will tune the oscillator at the desired PLL output frequency.

Analogous to the conventional analog charge-pump LC-VCO PLL with passive loop filter, the average value of the PWM output current can be thought as the small-signal  $V_{ctrl}$  across the loop filter capacitor to drive the varactor of the VCO. The DC current of the RF CCRO can be thought as the digital control word (in analog form) of the switched-capacitor bank of the LC-VCO. By toggling the DC current of the RF CCRO, the locked point of the PLL will traverse through the "tuning-curves" of the current-controlled oscillator. As is the case in the LC-VCO PLL where the ideal locking point of the  $V_{ctrl}$  across the loop filter capacitor should be close to mid-VDD to minimize the gain sensitivity, once the proposed sub-sampling PLL with time-based loop filter is locked, the duty-cycle of  $PWM_{I-path}$  current should be 50%.

Namely,

$$F_{RF-CCRO} = F_{RF-CCRO,nominal} + K_{RF-CCRO} \times \overline{I_{CP,time-based-loop-filter}} \quad (4.7)$$

where

$$I_{CP,time-based-loop-filter} = I_{CP,I-path2} + I_{CP,p-path} \quad (4.8)$$

An interesting observation is that in the conventional PLL with PFD, phase error information is first converted into time-domain to generate PWM waveform, which further drives CP and Loop Filter to generate  $V_{ctrl}$  to tune the varactor of VCO. In the proposed architecture, phase error information is first sampled as small-signal voltage and then converted into time-domain by the time-based loop filter as the form of PWM signal.

As shown in Fig. 4.6 and Fig. 4.8, the operation of the time-based loop filter can be seamlessly integrated within the sub-sampling loop with almost no extra design complexity to the proposed PLL.

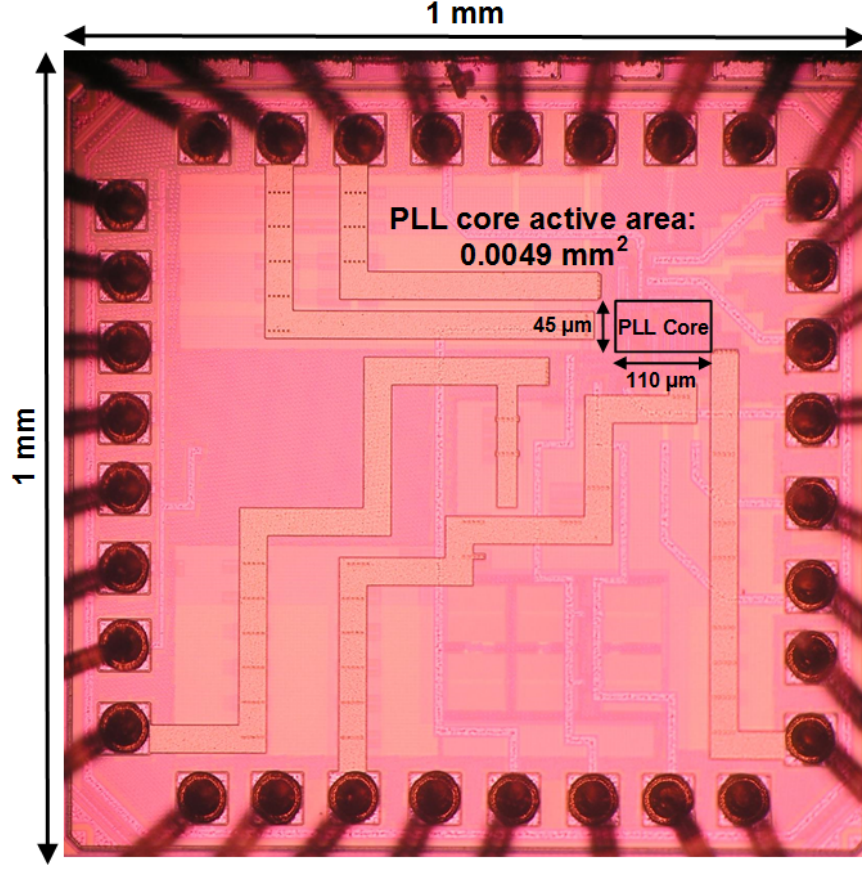


Figure 4.9: Die micrograph.

## 4.5 Measurement Results

The prototype PLL is fabricated in a 65nm standard CMOS process (Fig. 4.9), occupies an extremely compact active area of  $45\mu\text{m} \times 110\mu\text{m}$  ( $0.0049\text{mm}^2$ ), and is tested in a 40-pin QFN package with the off-chip reference signal derived from a Keysight E8257D Analog Signal Generator.

### 4.5.1 Oscillator Measurement

Fig. 4.10 shows the measurement result of RF current-controlled ring oscillator standalone. It can be tuned continuously from 0.5 to 3.8GHz (shown in Fig. 4.10(a)) with a phase noise of -95.8dBc/Hz at 1MHz offset at 2.3GHz (shown in Fig. 4.10(b)). Fig. 4.10(c) shows the

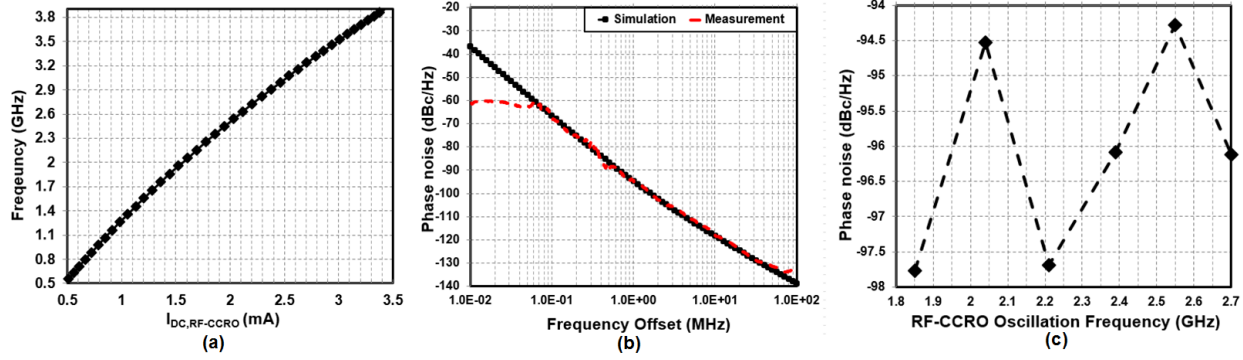


Figure 4.10: Measured (a) tuning-range of RF-CCRO, (b) phase noise at 2.3GHz carrier frequency, and (c) phase noise at 1MHz offset versus carrier frequency.

measured phase noise at 1MHz offset across the tuning range of the RF CCRO.

Fig. 4.11 shows the measurement result of Integrating-CCRO that is used in the sub-sampling time-based integrator path. It can be tuned from 50MHz to 430MHz continuously (shown in Fig. 4.11(a)) and it exhibits phase noise of -98.2 dBc/Hz at 1MHz offset at 200MHz carrier frequency.

## 4.5.2 PLL Measurement

The proposed PLL operates from 1.1GHz to 3.5GHz and the PLL core consumes 3.5 to 5.7mW. At 2.3GHz, the PLL core (excluding FLL and the output buffers incorporated for measurement purposes) draws 3.7mA from a 1.2V supply, with 1.8mA for the RF CCRO and 1mA for the I-CCROs. The FLL consumes 0.9mW and its division ratio can be programmed to be at 12 or 48 through its divider. The FLL is disabled once the PLL is locked.

Fig. 4.12 shows the measured phase noise at 2.3GHz output using a Keysight E4448A Spectrum Analyzers phase-noise-measurement personality with 200MHz reference input and a multiplication factor (division ratio) of 12. The measured integrated jitter (10k-100MHz) is 0.72ps<sub>rms</sub> with 4.5mW DC power consumption (jitter FoM = -236.2dB), and the measured reference spur is -37dBc. Fig. 4.13(a) and Fig. 4.13(b) show the measured jitter FoM and reference spur level across different output carrier frequencies keeping the multiplication ratio

between output frequency and the reference frequency constant at 12.

Fig. 4.14 shows the measured phase noise at 2.3GHz output with 50 MHz reference input and a multiplication factor (division ratio) of 48 translating to the output. The measured integrated jitter (10k-100MHz) is  $1.98\text{ps}_{rms}$  with jitter FoM of -228dB, and the measured reference spur is -41dBc.

Table. 4.2 shows the performance summary and comparison with state-of-the-art ring-oscillator-based PLLs. It can be seen that the proposed PLL achieves state-of-the-art jitter FoM performance that compares well with high-performance PLLs that require significant area while simultaneously occupying comparable (or smaller) core area to ultra-compact PLLs. In other words, the prototype PLL shows the possibility of achieving high PLL FOM with ultra-low silicon area and minimum design and system complexity overhead.

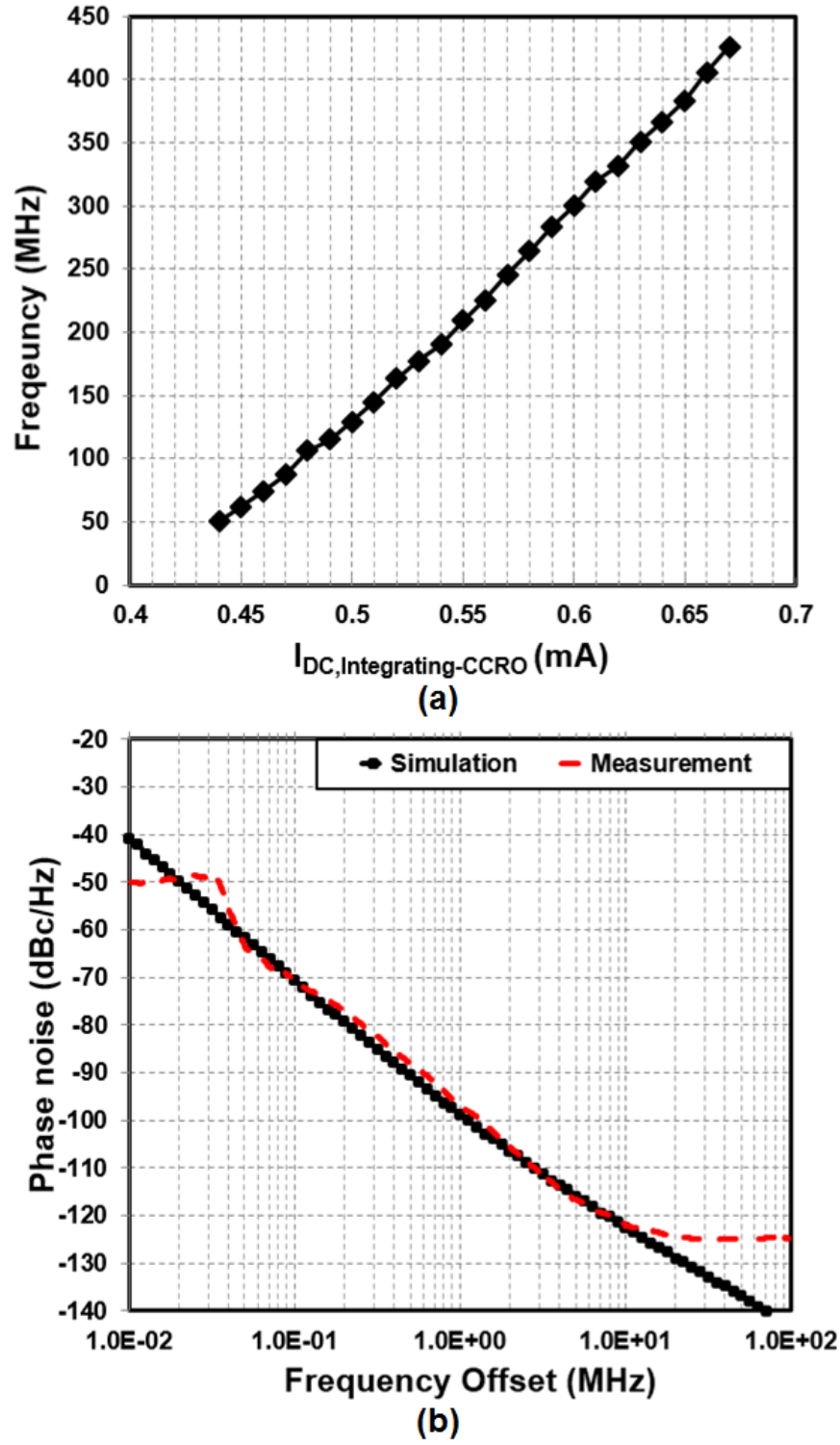
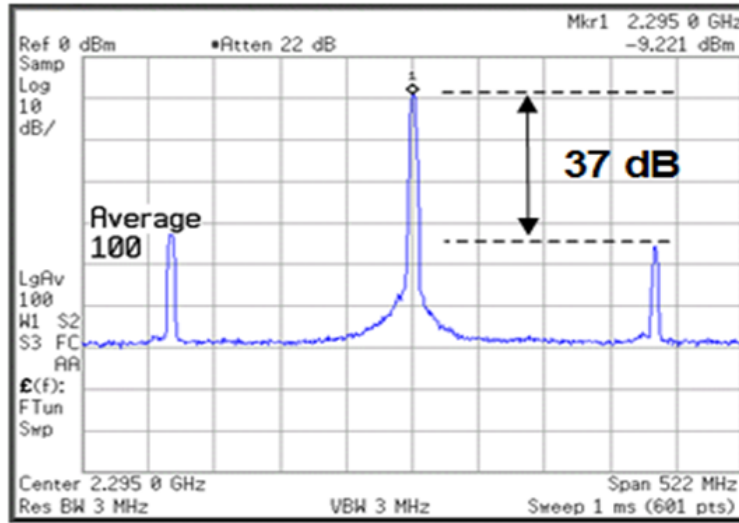
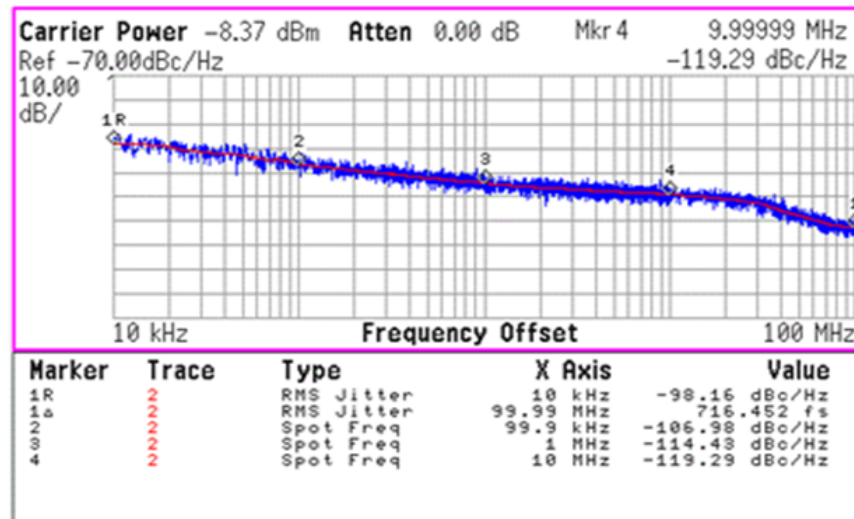


Figure 4.11: Measured (a) tuning-range of the integrating-CCRO, and (b) phase noise at 200MHz carrier frequency.



(a)



(b)

Figure 4.12: PLL measurement with multiplication factor of 12 at 2.3GHz: (a) locked spectrum, and (b) phase noise vs. offset frequency.

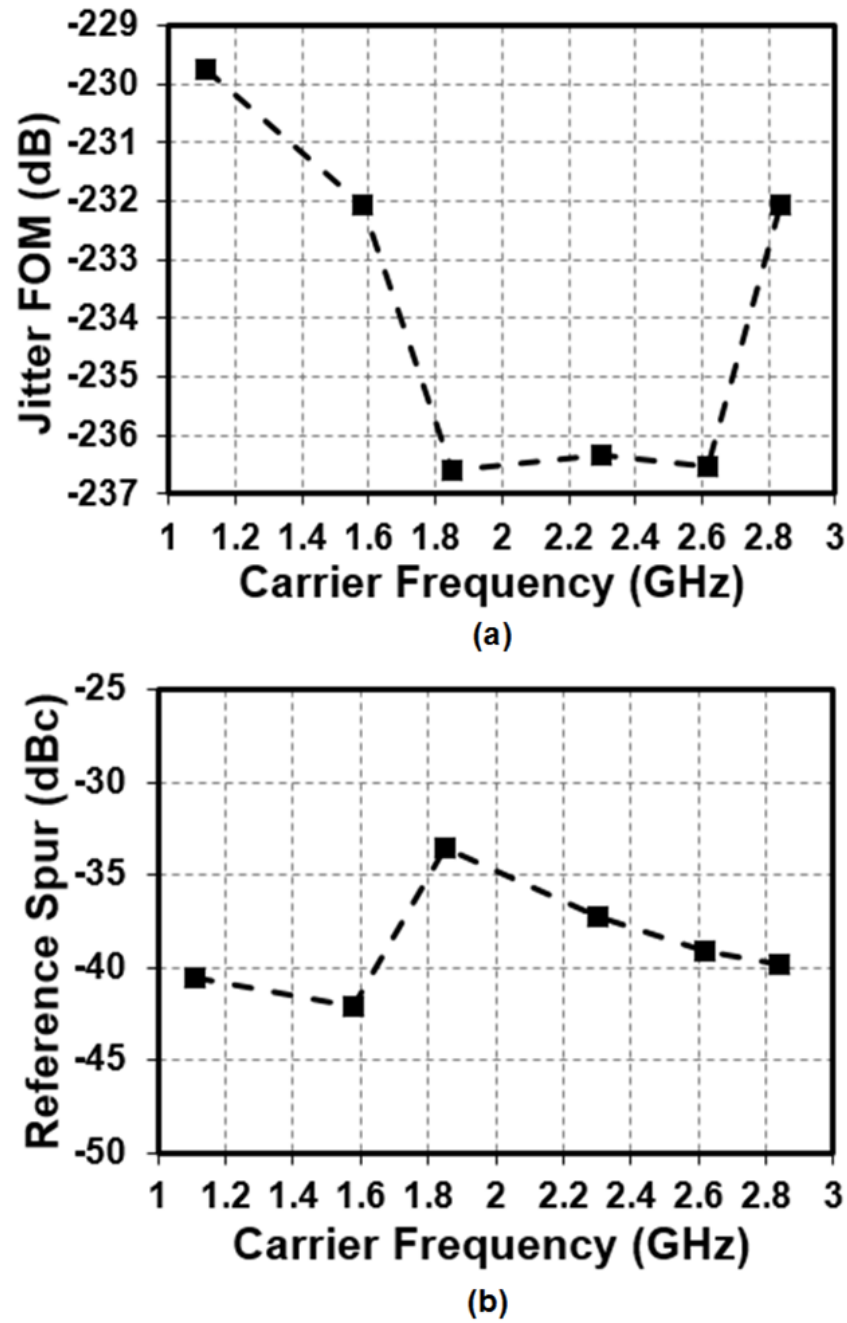
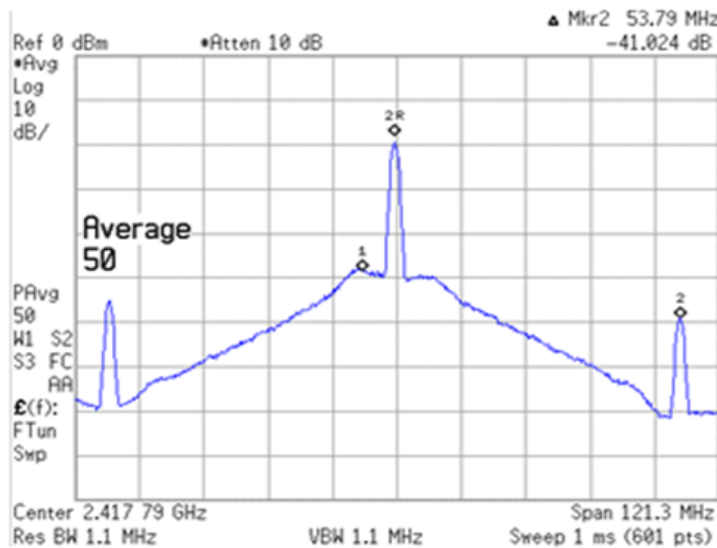
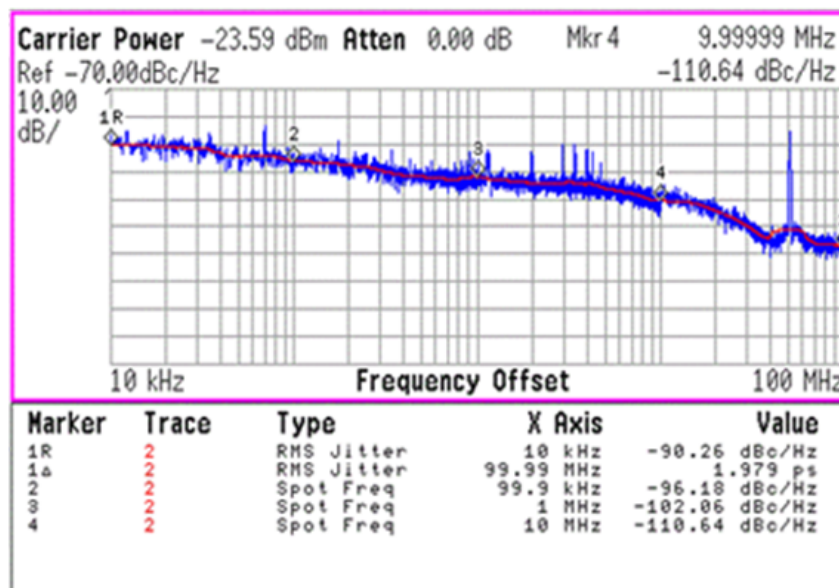


Figure 4.13: PLL measurement of as a function of locked frequency (multiplication factor = 12): (a) jitter-FoM, and (b) reference spur level



(a)



(b)

Figure 4.14: PLL measurement with multiplication factor of 48 at 2.3GHz: (a) locked spectrum, and (b) phase noise vs. offset frequency.

Table 4.2: Performance summary and comparison.

	[65]	[21]	[22]	[66]	[80]	This work
Category	High-performance			Low-area		High-performance & Low-area
Architecture	Sub-sampling PLL	Type-I PLL	Cascaded PLL	BB Digital PLL	Time-based Integrator PLL	Sub-sampling Time-based Integrator PLL
Oscillator Type	Ring	Ring	Ring	Ring	Ring	Ring
Technology	65nm CMOS	45 nm CMOS	65nm CMOS	14nm CMOS	65nm CMOS	65nm CMOS
Frequency	2.08 GHz	2.4 GHz	2.1 GHz	2.0 GHz	2.2 GHz	2.3 GHz
Reference	130 MHz	22.6 MHz	67 MHz	50 MHz	275 MHz	192 MHz
Division Ratio	16	106	31	40	8	12
Supply Voltage	1.2V	1V	1.2V	0.8V	1V	1.2V
$P_{dc}$ (mW)	20.4	4	3.84	2.06	1.82	4.59
Jitter <sub>rms</sub> (ps)	0.73	0.97	1.05	18.8	3.73	0.72
Integration BW	1k – 10MHz	1k-200MHz	1k – 50MHz	100k – 100MHz	10k-300MHz	10k-100MHz
Jitter FOM (dB)	-229.7	-234.1	-234	-211.4	-226	-236.2
Active Area	0.42 mm <sup>2</sup>	0.015 mm <sup>2</sup>	0.043 mm <sup>2</sup>	0.0087 mm <sup>2</sup>	0.0021 mm <sup>2</sup>	0.0049 mm <sup>2</sup>
Normalized Area	84	6.4	8.7	38.3	0.4	1

\* Normalized Area is  $\text{Area}/L_{\min}^2$  further normalized to this work

## 4.6 Conclusion and Future Work

This work proposed a PLL architecture that simultaneously address the active time-based loop filter's noise penalty and area-efficient loop filter implementation challenges with minimal design and complexity overhead, thus resulting in an ultra-low-area PLL with low phase noise performance. It also points to the opportunities afforded by sub-sampling, including other active loop filter topologies that can potentially incorporate other interesting functionalities. For instance, it would be interesting to combine the proposed PLL architecture with other phase noise reduction/cancellation technique for ring oscillator-based PLL to further improve the integrated jitter performance or out-of-band spot phase noise performances for wireless application. It would be also interesting to investigate how the proposed architecture can be re-purposed to operate in fractional-N mode [81].

## Chapter 5

# Fully-Integrated 60GHz Channel-Bonding Receiver with IF Channelization Supporting Flexible Bonding Scheme

### 5.1 Introduction

The research presented in this chapter, which addresses a fully-integrated 60GHz channel-bonding receiver with IF channelization supporting flexible bonding scheme, was performed in collaboration with Tolga Dinc and Linxiao Zhang at CosMIC Lab, at Columbia University. The contribution of this chapter includes proposal of radio architecture, proposal of the IF channelizer architecture, an analysis of system-level performance requirements, LO path frequency planning, and the implementation of the LO path (PLL + DLL + duty-cycle generator). The implementation of the mm-wave signal path (LNA, amplifier, mixer, frequency tripler) was performed by Tolga Dinc and the implementation of the IF channelizer was performed by Linxiao Zhang.

### 5.1.1 Fiber-fast mm-wave Wireless Communication

The ever increasing demands of wireless communication presents unprecedented challenges for physical layer (PHY) design. Circuit designers have been driven to create novel device technology, circuit-design technique, and radio architecture to meet stringent system-level requirements. With the coming era of 5G, utilization of mm-wave frequencies for wireless communication appears to be a panacea to the congested spectrum below 5GHz [82, 83].

According to the well-known Shannon Theorem, the maximum achievable data-rate for a communication link, namely the channel capacity ( $C$ ), is directly proportional to the available BW and the SNR of the channel. Namely,

$$C = BW \cdot \log_2(1 + SNR) \quad (5.1)$$

Eq. 5.1 clearly motivates that more available BW leads to more data-rate. By shifting to higher carrier frequencies, more BW is naturally available. Fig. 5.1 shows a highlight of the FCC-allocated mm-wave frequency spectrum. Owing to the demand of next-generation 5G networks and technologies in the US, in 2016, the FCC further opened nearly 11 GHz of high-frequency spectrum for flexible, mobile and fixed use wireless broadband as well as 3.85 GHz of licensed spectrum and 7 GHz of unlicensed spectrum [84]. These newly adopted rules create new upper microwave flexible use service in the 28 GHz (27.5-28.35GHz), 37 GHz (37-38.6 GHz), and 39 GHz (38.6-40 GHz) bands, and a new unlicensed band at 64-71 GHz.

A plethora of applications have been under development at mm-wave frequencies over the past 10-15 years in silicon CMOS technology thanks to technology scaling. These applications includes short-range and long-range vehicular radar at 24GHz [85, 86] and 77GHz [87, 88] respectively. They also include satellite communication for commercial and military use at 45GHz[89–91], multi-Gb/s short/mid-range wireless data link at 60GHz [92, 93], and active and passive imaging sensors at 94GHz [94–96]. The aforementioned newly opened spectrum has further catalyzed the development of high-throughput, low-cost mm-wave communication specifically at 28GHz, 39GHz, 70GHz and beyond[97, 98].

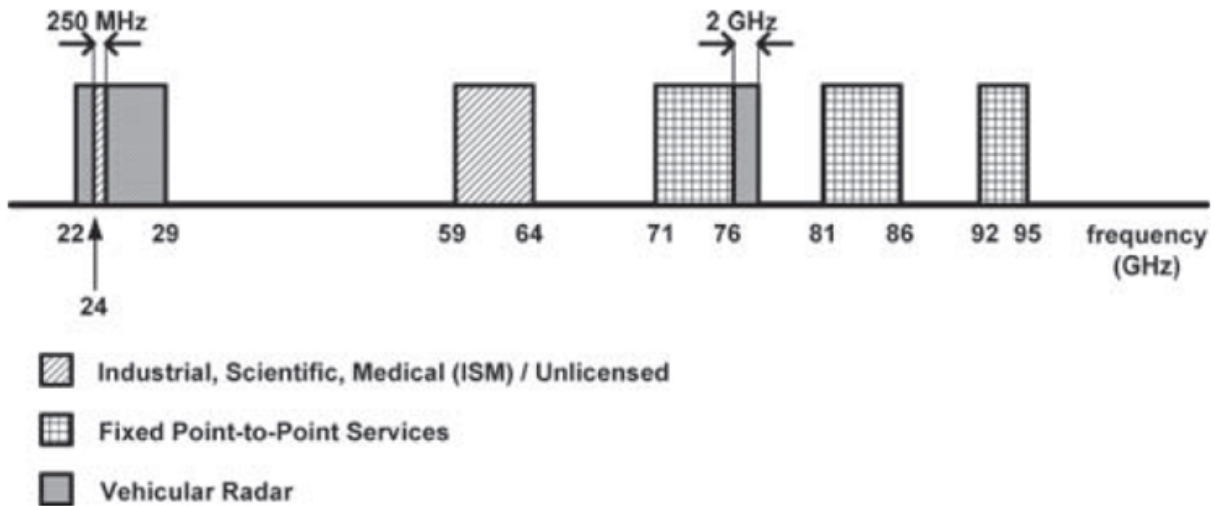


Figure 5.1: Highlight of FCC-allocated spectrum at mm-wave frequencies [9].

### 5.1.2 60GHz Multi-Gb/s Wireless Communication

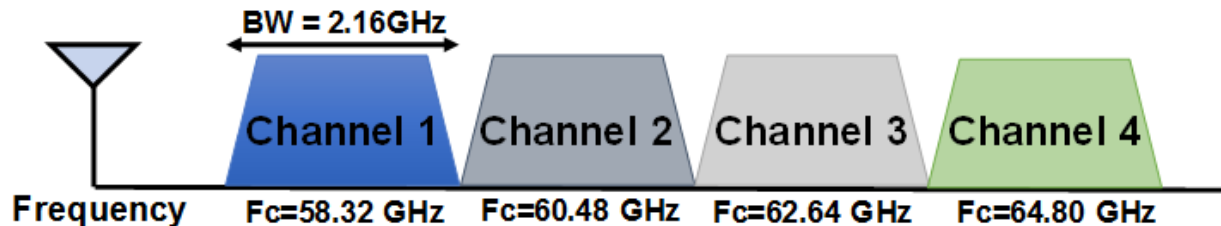


Figure 5.2: Frequency allocation for IEEE 802.11ad standard (WiGig).

Among these applications, the 60GHz band offers exciting opportunities for multi-Gb/s wireless communication [82]. Contiguous spectrum up to 7GHz has been allocated for unlicensed usage. The IEEE802.11ad, aka WiGig, specification, as shown in Fig. 5.2, allocates four 2.16GHz wide channels centering around 60GHz (58.32GHz, 60.48GHz, 62.64GHz, 64.8GHz) and defines modifications, IEEE 802.11ad, to both the PHY and MAC layers to the existing IEEE 802.11 standard for high throughput wireless communication at 60GHz. The PHY layer specification includes single-carrier (SC) transmission with data rates up to 4.6 Gb/s or orthogonal frequency-division multiplexing (OFDM) transmission with data rates

of up to 6.76 Gb/s. While all devices should support the SC transmission modes, OFDM transmission modes are meant for high-performance communication links. Fig. 5.3 provides a brief overview of the coding and modulation scheme vs. achievable data-rate for WiGig PHY layer specification in both SC and OFDM transmission mode.

Control (CPHY)			
MCS	Coding	Modulation	Raw Bit Rate
0	$\frac{1}{2}$ LDPC, 32x Spreading	$2/\pi$ -DBPSK	27.5Mbps
Single-Carrier (SCPHY)			
MCS	Coding	Modulation	Raw Bit Rate
1-12	$\frac{1}{2}$ LDPC, 2x repetition $\frac{1}{2}$ LDPC, 5/8 LDPC $\frac{3}{4}$ LDPC 13/16 LDPC	$2/\pi$ -BPSK, $2/\pi$ -QPSK, $2/\pi$ -16QAM	385 Mbps To 4620Mbps
Orthogonal Frequency Division Multiplexing (OFDM-PHY)			
MCS	Coding	Modulation	Raw Bit Rate
13-24	$\frac{1}{2}$ LDPC, 5/8 LDPC, $\frac{3}{4}$ LDPC, 13/16 LDPC	OFDM-SQPSK OFDM-QPSK OFDM-16-QAM OFDM-64QAM	693 Mbps To 6756.75 Mbps
Low-Power Single-Carrier (LPSCPHY)			
MCS	Coding	Modulation	Raw Bit Rate
25-31	RS(224,208)+ Block Code (16/12/9/8,8)	$2/\pi$ -BPSK, $2/\pi$ -QPSK	625.6 Mbps To 2503 Mbps

Figure 5.3: Modulation and coding scheme vs. data-rate for IEEE802.11ad standard.

Due to advances in technology, CMOS transistors with  $f_{max}$  of greater than 200GHz [99, 100] have been reported. Meanwhile, fundamental device parameters that are critical building blocks for design such as  $f_T$ ,  $NF_{min}$ , and Mason's Unilateral Gain (U) have improved as CMOS technology has advanced [101]. For this reason, high-performance, compact and robust 60GHz CMOS integrated wireless radio design has attracted significant interest and research efforts from both academia [11, 53, 93, 102–107] and industry [92, 108–115] in recent years. While it has been demonstrated in these prior-arts that high-throughput, low-

cost, robust, highly-integrated 60GHz CMOS radios are feasible and can be commercialized, emerging applications in the market demand radio performance far beyond what commercial products can offer.

### 5.1.3 Emerging IEEE 802.11ay Standard: Towards 100Gb/s

While fiber optics and wireline Ethernet cable provide tens of Gb/s wired communication in today's world, mobile applications are calling for 100Gb/s wireless communication with respectful range. These applications include 8k Ultra-High-Definition (UHD) video streaming (data-rate = 28Gb/s), 4k-UHD video transfer for wireless augmented-reality/virtual-reality headsets and wearables (>20Gb/s, uncompressed video, low latency), inter-rack connectivity for data center, video/mass-data distribution/video on-demand system, wireless backhaul, and others.

Using uncompressed 8k UHD video transfer as an example, to quantify the significant challenge associated with data-rate, the required data rate can be calculated as

$$\text{Uncompressed, 8k - UHD} = 7680 \times 4320(\text{pixels}) \cdot 60(\text{frames/s}) \cdot 24\text{bit/pixel} \approx 48\text{Gb/s} \quad (5.2)$$

Though it is widely accepted that chroma sub-sampling can be applied to uncompressed video files with no artificial effects on human visual systems, with 4:2:2 chroma sub-sampling applied (reducing about 1/3 of BW requirement), at least  $\approx 28\text{Gb/s}$  data rate is required.

The above example highlights the challenge of wireless communication for these emerging applications. Due to this, an upcoming amendment to current 802.11 specification, 802.11ay standard, is currently under development and is expected to be released in 2017. The upcoming 802.11ay standard targets >20Gb/s data-rate with at least a 10-meter indoor range and 100-meter outdoor range (Line-of-Sight). As it is drafted now, it also provides backward compatibility with the current 802.11 standard with fast-link setup and mobility supports. To achieve such high data rates and distances of communication, it is expected that system-level arrangements such as channel-bonding and MIMO not exploited in the current

802.11ad specification will need to be incorporated in the upcoming 802.11ay standard. Fig. 5.5 highlights the features of the upcoming 802.11ay standard and its progression from the 802.11ad specification.

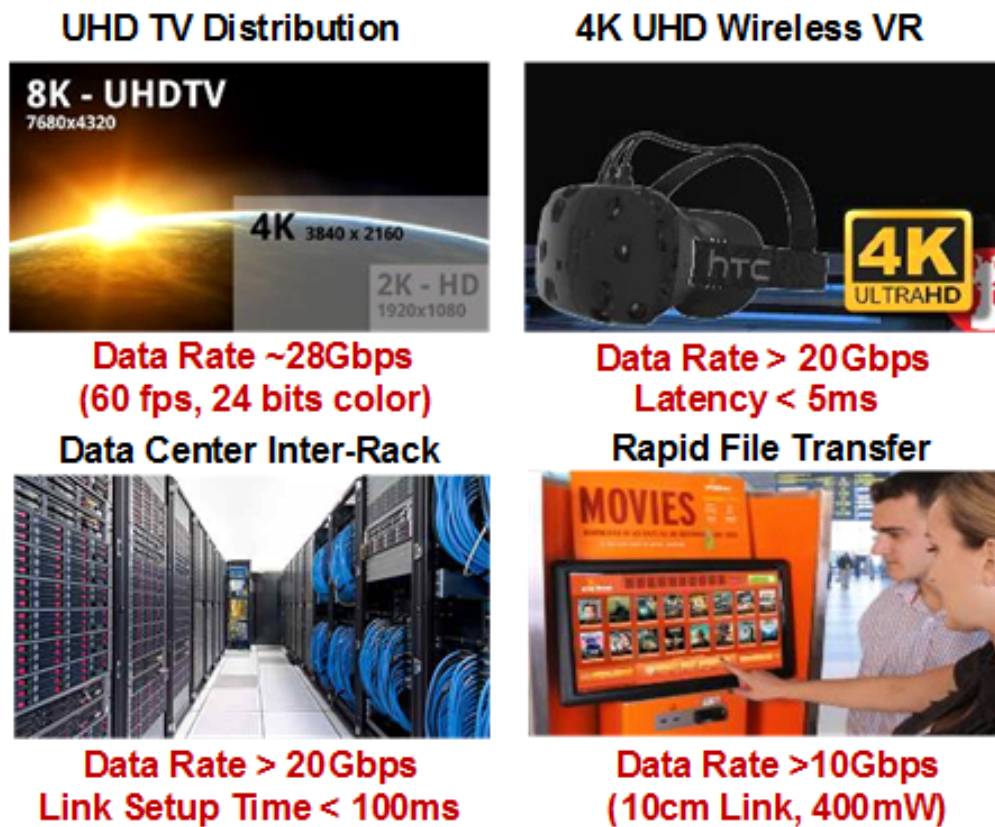


Figure 5.4: Futuristic applications for high data-rate wireless communication.

## 5.2 60GHz Channel-Bonding for 802.11ay: Opportunities and Implementation Challenges

### 5.2.1 Opportunities for Channel-Bonding at 60GHz

To maximize the spectrum utilization and the network throughput, opportunistically bonding available channels for high data rate transmissions can be a viable option. Channel-

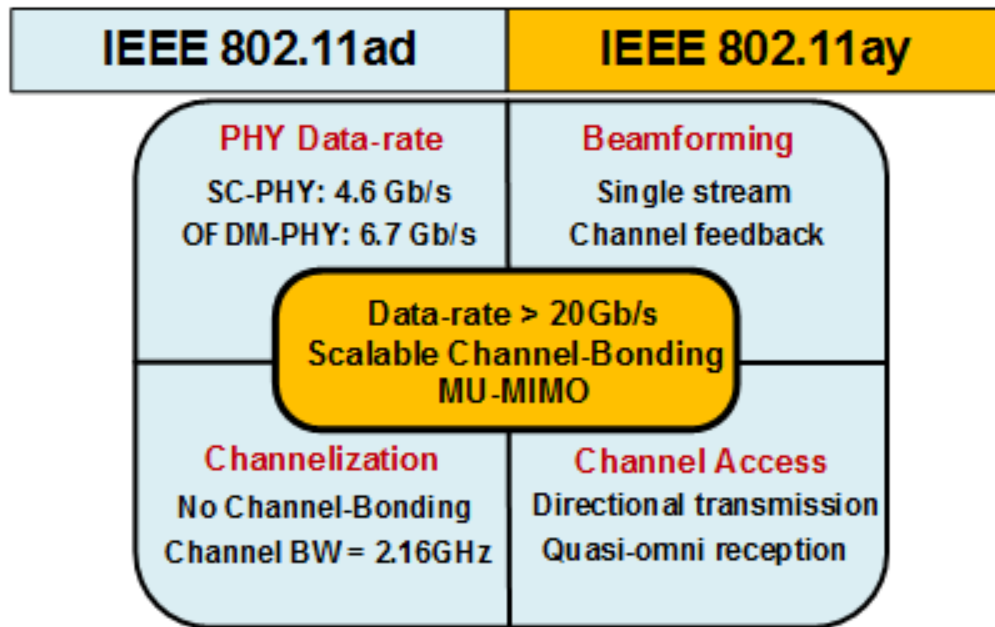


Figure 5.5: Highlighted features for the upcoming IEEE 802.11ay specification and its amendment to the current IEEE 802.11ad standard.

bonding is currently used in existing standard such as 802.11ac and 802.11n, among others. However, it has not been specified in the current 802.11ad standard at 60GHz. In the channel-bonding scheme, assuming the spectrum efficiency is not affected by implementation of bonding and the model is the same for all channels, the achievable data rate is directly proportional to the number of channels bonded.

As shown in Fig. 5.6, there are currently four channels available in the WiGig standard. As previously mentioned, the maximum data rate per channel, 6.76Gb/s, is achieved with an OFDM-64QAM modulation scheme. By bonding four channels together,  $\approx 27$ Gb/s can be achieved. If the channel environment permits a more sophisticated modulation scheme, i.e. better SNR given bit-error-rate (BER), achieving an even higher data rate is entirely possible.

Though channel-bonding brings straightforward benefit to the performance of the link and has been successfully tried out at RF frequencies (2.4/5GHz), there are a few unique challenges associated with the hardware implementation at mm-wave frequencies that it

may introduce to the current scheme.

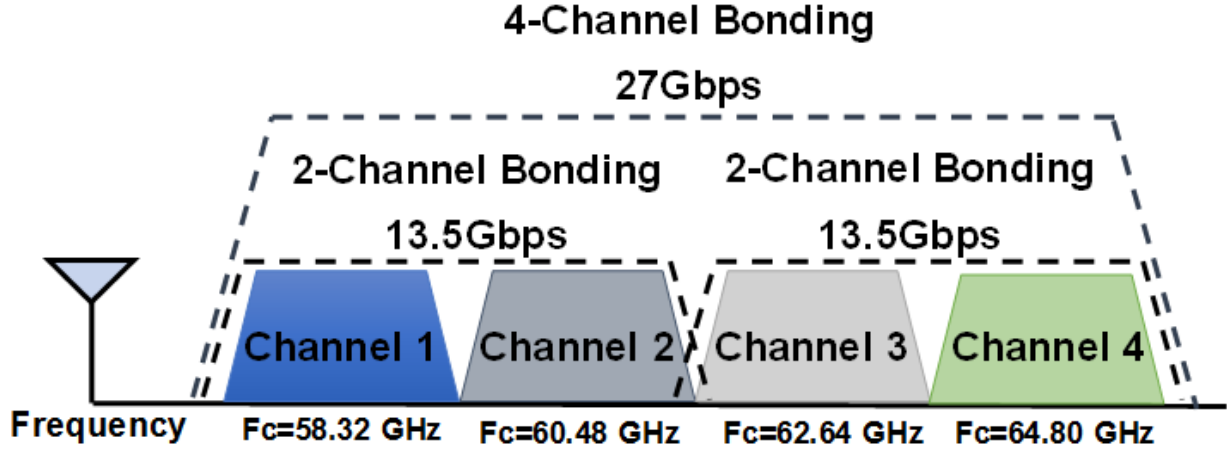


Figure 5.6: Channel-bonding scheme for IEEE 802.11ay standard.

### 5.2.2 Challenge I: High-speed Baseband ADC Design

By bonding up to four channels once, the required sampling speed for baseband analog-to-digital converter (ADC) directly increases. Depending on the dynamic range requirement, it is expected that a  $>20\text{GS/s}$  ADC is required for a channel-bonding scheme at 60GHz.

Fig. 5.7 shows a survey of commercially-available high-speed ADC from Texas Instrument and Analog Devices. It can be seen that the cost of these ADC modules increases exponentially as the sampling rate approaches G-sample/s range. For high-speed high-resolution ADC modules, the price can easily exceed 1k USD per-module, barring it from being integrated into the low-cost radio modules for mobile applications. As shown in Fig. 5.7, the power consumption of ADC modules does not faithfully follow the well-known ADC FoM trend (Eq. 5.3), the reason for this is that most of the power consumption in an ADC module is dominated by its I/O interfaces, namely the buffers to load/drive signals to/from outside world.

$$FoM = \frac{P_{dc}}{2^{ENOB} \cdot f_s} \quad (5.3)$$

where

$$ENOB = \frac{SNDR - 1.76}{6.02} \quad (5.4)$$

As shown in 5.8[10], implement integrated power-efficient >20GS/s ADC with a reasonable resolution (ex: 6bit) in CMOS technology is still an active research problem to date. For this reason, in mobile radio SoC platforms, it is also desirable to integrate ADC into the same chip as the RF radio. The state-of-the-art architecture utilizes time-interleaving architecture, as shown in Fig. 5.9(a), to overcome the speed challenge.

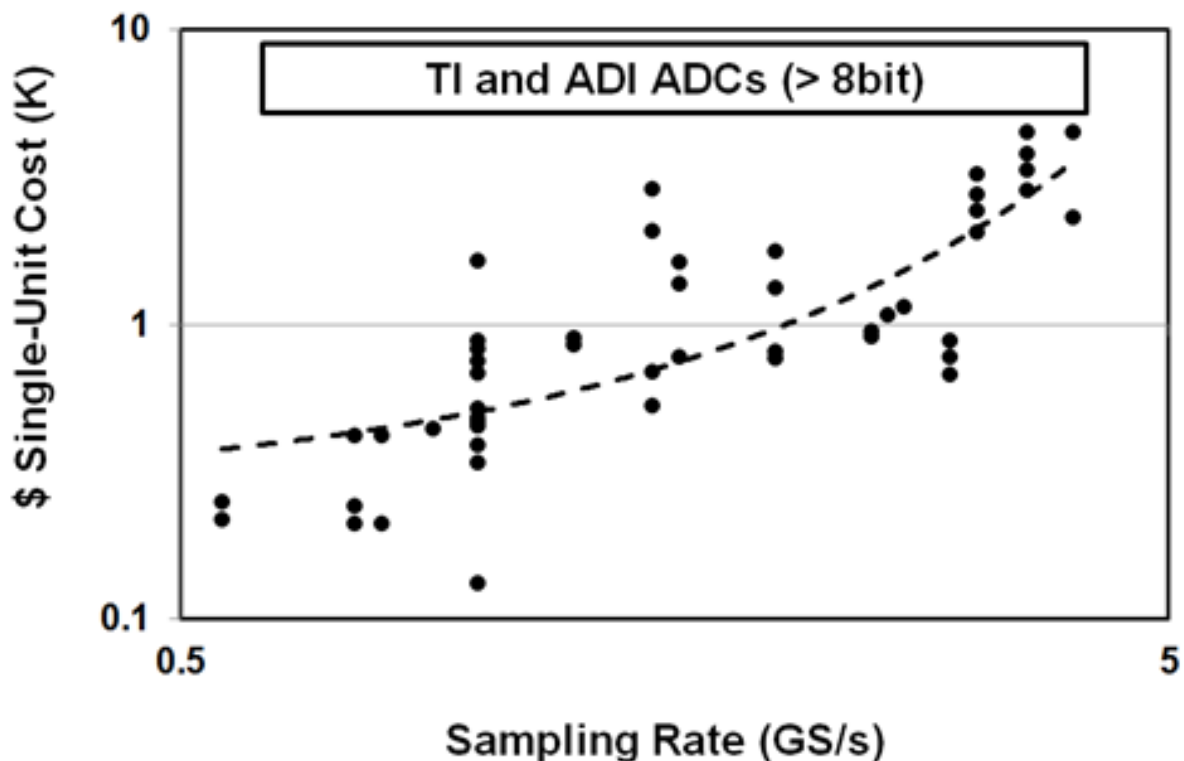


Figure 5.7: Survey of unit cost vs. sampling rate for commercial (Texas Instrument and Analog Device) ADC module.

In time-interleaving architecture, identical sub-ADCs with preceding front-end sampler can be interleaved in the time domain. To ensure the sampling process can be handed over from one sub-ADC to another, clock phases generated a PLL or a DLL needs to be uniformly

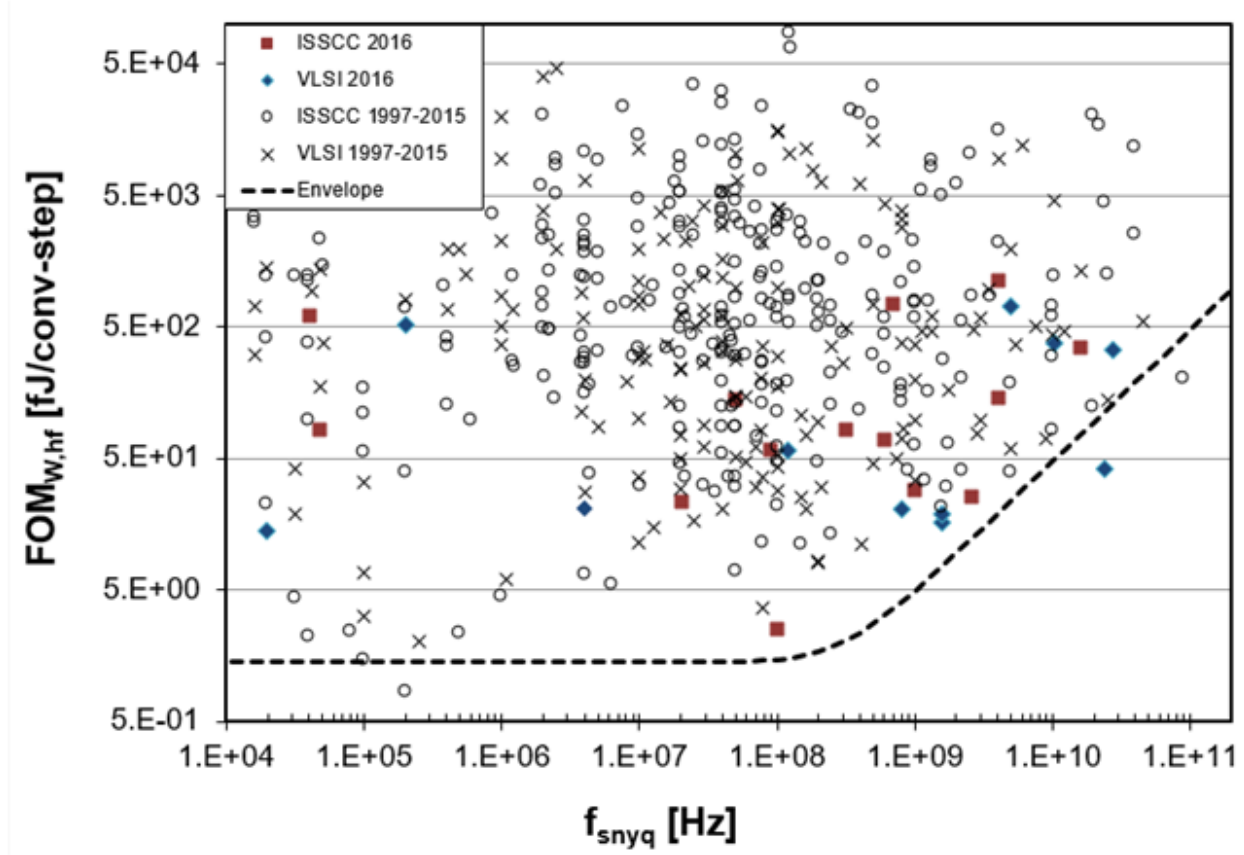


Figure 5.8: Survey of FOM vs.  $f_{\text{sampling}}$  for selected ADC published in the past 20 years [10].

distributed across the its entire period, as shown in Fig. 5.9(b). The output of each sub-ADC can be multiplexed or concatenated to reconstruct the sampled digital information. By utilizing time-interleaving architecture, FoM performance improves or follows the theoretical value more closely. The reason for this is that sampling speed of a single sub-ADC reaches its limits, namely  $f_T$  of the technology, the power-speed trade-off deviates significantly from the trend of FoM and becomes largely nonlinear, demanding a disproportionately higher amount of power for the desired increase in speed. For instance, Op-Amps and comparators will eventually exhibit limited speed improvement by raising their power consumption. Therefore, once each sub-ADC has been pushed towards its limit of power vs. speed trend, time-interleaving should be used to alleviate the power consumption overhead.

However, in time-interleaving architecture, there is still finite power consumption over-

head such as front-end sampler, output MUX, and LO generation circuitry. As the input and clock speed increases, the power consumption associated with these auxiliary blocks also increases.

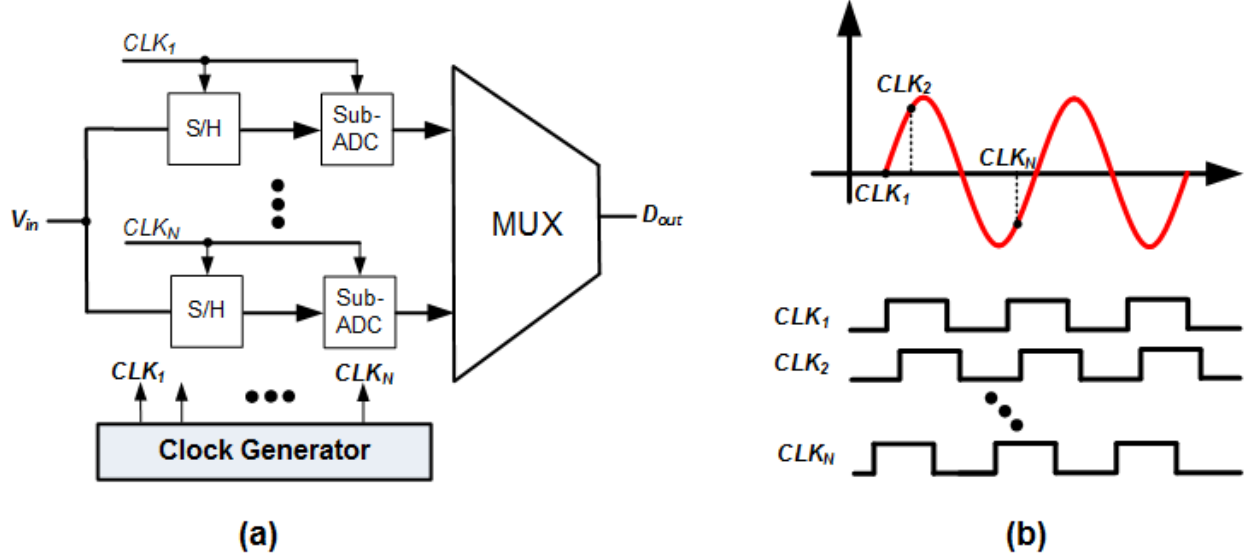


Figure 5.9: (a) Schematic of time-interleaved ADC architecture (b) Timing diagram of clock signal for time-interleaved ADC.

### 5.2.3 Challenge II: LO Tuning-range

Tuning-range vs. Q of LC-VCO has been an ongoing research problems for LO path design at mm-wave frequencies. Many works, including [116–127], have tried to address it from different perspective. CMOS frequency synthesis at mm-wave frequencies can be categorized primarily into four types [128]:

- **Fundamental PLL and VCOs:** Fig. 5.10(a) shows the architecture of PLL with fundamental VCO. The VCO oscillates at the desired carrier frequency and directly drives the high-speed (frequency) divider to compare its phase with the reference signal and close the feedback loop.

The is one of the simplest architecture to generate the LO at carrier frequencies. However, it came with several design challenges. First, tuning-range vs. phase noise trade-off gets worse at mm-wave frequencies due to the low-Q nature of capacitor, specifically varactor, at this frequency. Second, high-frequency divider design can still be challenging at the frequency moves closer to  $f_T$ . Finally, as the carrier frequency goes higher, large division ratio incurs large multiplication ratio for phase noise of loop components (reference, PFD, CP) to transfer to PLL output. This adversely worsen the in-band hence overall phase noise performance of the PLL.

- **Sub-harmonic PLL with frequency multiplier:** Due to the challenging trade-off of tuning-range vs. Q for the capacitor (varactor) at mm-wave frequencies [100], hybrid approaches can be adopted. As shown in Fig. 5.10(b), using a sub-harmonic VCO in conjunction with a frequency multiplier greatly ease the above trade-off.

The frequency multiplier can typically be implemented by exploiting non-linear amplification of a mm-wave amplifier with tuned load. Non-linear amplification will generate harmonic signals at its output and the tuned-load can be designed such that only the desired harmonics enjoys the gain while the undesired harmonics being filtered (attenuated).

While this approach is widely used for 60GHz LO generation, the biggest drawback with the approach is excessive power consumption. Typically the output power of the frequency multiplier is much weaker than output of the VCO (buffer), demanding additional buffer stage after the frequency multiplication to drive the mixer stages. In addition, leakage of fundamental tones can affect the mixer and system performance.

- **Sub-harmonic PLL with VCO harmonic extraction:** A sub-harmonic PLL with VCO harmonic extraction, shown in Fig. 5.10(c), offers the flexibility of decoupling the tuning-range vs. Q trade-off while not requiring an explicit frequency multiplication stage following the VCO (PLL). The idea of N-push oscillators is to extract the harmonic information available in a multi-phase oscillator. The desired harmonic

signal can be extracted by a properly designed passive power combining network at the oscillator output. Meanwhile the signal available at the fundamental frequency can be used to drive the frequency divider so that the operating frequency of the divider and carrier frequency can be decoupled.

This approach eliminates the need for explicit active frequency multiplication stage after the PLL, however, active buffers may still be required since the power of extracted harmonic signal may not be enough to drive the mixer. Also, the design complexity largely lies in ensuring the phase relationship between the multi-phase VCO output.

- **Sub-harmonic PLL with injection-locking oscillators:** As shown in Fig. 5.10(d), the sub-harmonic PLL with injection-locking oscillators exploits the injection-locking mechanism to lock a fundamental oscillator at the output by a sub-harmonically locked PLL. It is well known that a injection-locking oscillator bears a similar phase noise transferring profile to type-I PLL. Meaning that the phase noise of the injecting signal will be low-pass filtered while the phase noise of the oscillator-to-be-locked will be high-pass-filtered when transferred to the system output. This mechanism is exploited to again break the aforementioned tuning-range vs. Q (phase noise) trade-off.

While this approach provides superior phase noise performances, the narrow locking range makes the design sensitive to process, voltage, and temperature (PVT) variation. Many works have attempted to address this issue by incorporating sufficient tuning on the oscillator. The other challenge associated with this approach is that the injecting signal must be powerful enough to lock the oscillator, if its fails to lock and instead injection pulls the oscillator, the mixer and system performances will be compromised.

To cover the whole 60GHz band, in an direct-conversion receiver architecture for example, the LO must be able to be tuned from the centering frequency of band1 to band4, namely 58.32GHz to 64.8GHz. This 6GHz tuning-range occupies around 10% of its centering frequency at 60GHz.

Quality factor for capacitor and varactor is extremely low at mm-wave frequencies [99][116],

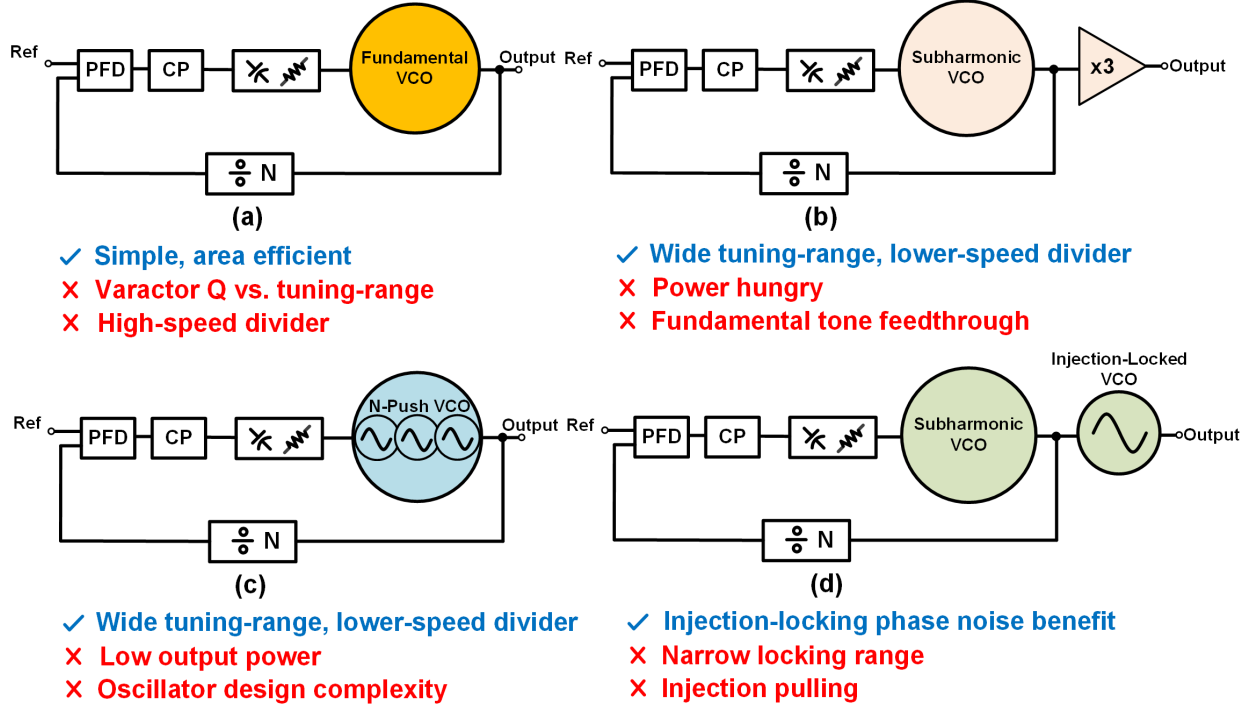


Figure 5.10: Highlight of mm-wave frequency generation techniques.

due to this reason, low phase-noise LC-VCO with wide-tuning range design is extremely challenging at mm-wave frequencies.

In the channel-bonding scheme, the LO will presumably needs to provide contiguous and non-contiguous channel-bonding capability simultaneously. Also, the fact that 802.11ay specification may require backward compatibility to the existing 802.11ad standard, the LO tuning-range vs. Q challenge will remain in place if not exacerbated.

### 5.2.4 Challenge III: Calibration

As mentioned above, recent works have demonstrated the capability of implementing high-performance and cost-effective 60GHz radio in CMOS technology. Robustness is another important aspect for mass production and mobility of CMOS 60GHz radio. To meet the stringent data-rate and link-budget requirement of 802.11ay standard, extensive calibration is necessary to overcome a few key impairment in-built in the hardware system. These key

impairment due to sensitive or unavoidable hardware implementation impairment, to list a few, are:

- Gain flatness: Due to the wideband nature of the available spectrum around 60GHz, gain can fluctuate across the frequencies. It is imperative for amplifier on both transmitter and receiver side to be equipped with gain detection and gain adjustment capability to ensure that the performance can be equalized across the entire 7GHz contiguous spectrum.
- I/Q imbalance: The impairment of In-phase/Out-of-Phase, I/Q, signal of the LO will cause imbalance between the I/Q channel of the transceiver. If image-rejection is required, the LO I/Q imbalance will further limit image-rejection ratio (IRR) of the system. These I/Q impairment can be originated from multiple sources such as mismatch of I/Q generation circuitry, LO routing, off-tuned narrow-band I/Q generation...etc. In an complexed modulation scheme such as 64-QAM or even 128-QAM, the overall error-vector-magnitude (EVM) of the system can be limited by these I/Q impairment. Therefore, it is imperative to incorporate I/Q calibration scheme to maximize the overall performance of the system.
- : LO feed-through: Local oscillator feed-through (LOFT) can cause EVM degradation or contamination of spectrum mask on receiver or transmitter. On the receiver side, LO-RF feed-through can cause DC offset at baseband and potentially saturate the following amplifier. On the transmitter side, LO-RF feed-through will cause the LO signal sit at the middle of the mask and corrupt the transmitted signal. Due to the finite parasitics of the devices and routing in the hardware implementation, this feed-through can be mitigated but not entirely eliminated. Therefore, it is critical to calibrate this unwanted feed-through through detection and cancellation mechanism to minimize its impact on the overall system performances.

### 5.3 Prior-Arts

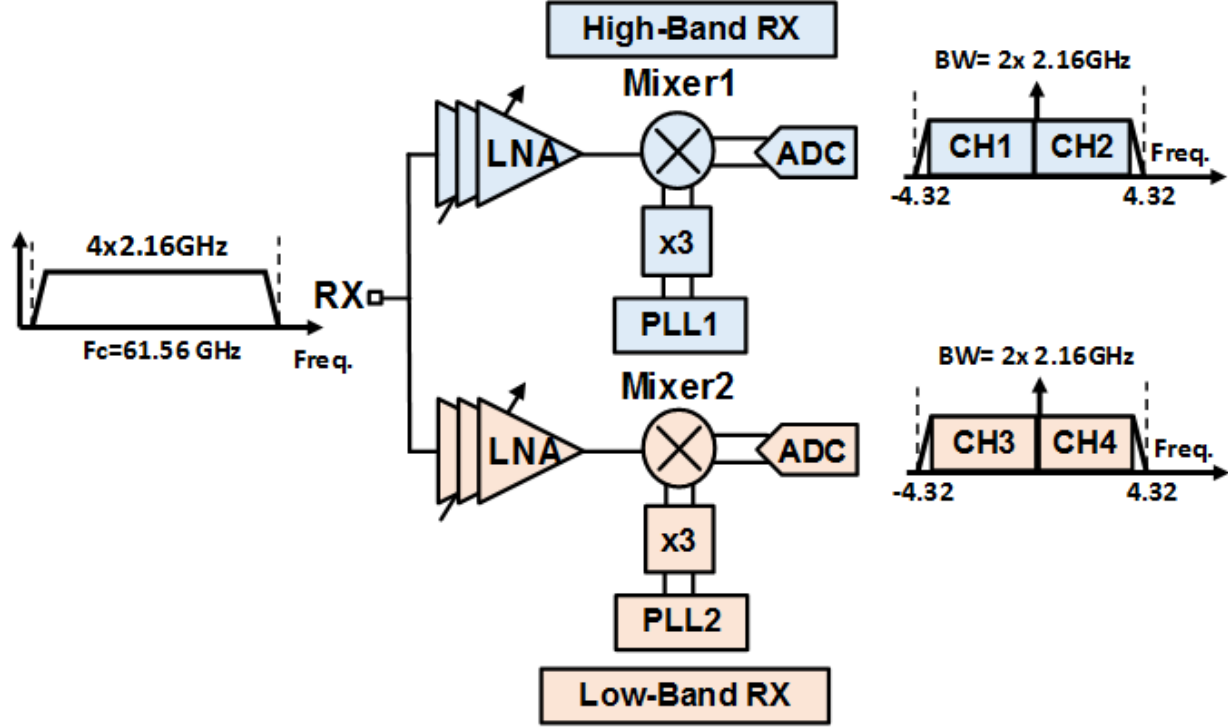


Figure 5.11: Conventional channel-bonding architecture [11].

Radio architectures that aimed to perform channel-bonding at 60GHz band and support IEEE802.11ay has been proposed, the simplified schematic is shown in Fig. 5.11. By creating a two identical hardware copies (both signal path and LO path), the radio can be configured to bond up to four contiguous channels concurrently. While this straightforward approach appears to be attractive at the first sight due to its simplicity, it does not fundamentally address the challenges mentioned in the previous section. Specifically,

**(a) For the ADC challenge:**

The aforementioned approach halved the speed requirement of ADC by halving the baseband signal bandwidth hence the required ADC sampling rate. Though reducing the sampling-rate requirement by half partially ease the design challenge on the ADC side, it still requires the speed of ADC to be twice faster than what is currently being used in the

radio compatible with 802.11ad standard. In addition, considering that it adversely doubles the power consumption and area of the up-conversion/down-conversion and the LO path, the benefit of this approach diminishes rapidly.

**(b) For the LO tuning-range challenge:**

According to FoM of VCO phase noise, two identical copies of VCO with all the corresponding nets connected should exhibit 3dB better phase noise at the cost of doubling the power consumption while attaining the same FoM.

In [11], two copies of LO are created to cover the entire 7GHz bandwidth for up to bonding 4 channels. The oscillation frequency of the VCO in the LO path will be slightly off-tuned to cover different bands around 60GHz. To the first order, the potential phase noise benefit of the copied VCO is not exploited at all, thus worsening the effective FoM of the LO path. However, considering the fact that tuning-range of each LO can be eased by covering two bands individually, the phase noise of each LO can be designed with more loosening phase noise vs. Q trade-off hence slightly better phase noise performances than the single LO case.

**(c) For the calibration challenge:**

By creating two copies of hardware on both the signal path and LO path to cover the whole range of spectrum, the complexity of calibration inevitably increases. The reason being that all the mechanism of circuit/performance impairment or non-ideality mentioned in the previous section will now double. This could leads to additional overhead of hardware or software calibration tools implementation.

## 5.4 Proposed Single-PLL Fully-integrated 60GHz Channel-bonding Receiver Architecture

Fig. 5.12 shows the proposed channel-bonding architecture. A single path RF down-conversion path is used to first translate the incoming signal of all bands around 60GHz (57-64 GHz) to baseband frequency with I/Q downconversion. The received signal at base-

band frequency is subsequently followed by the proposed IF channelizer to process and slice the received contiguous spectrum into four separate channels. At the output of the proposed IF channelizer, the received information lying in four separate channels will come out in parallel with separate pins.

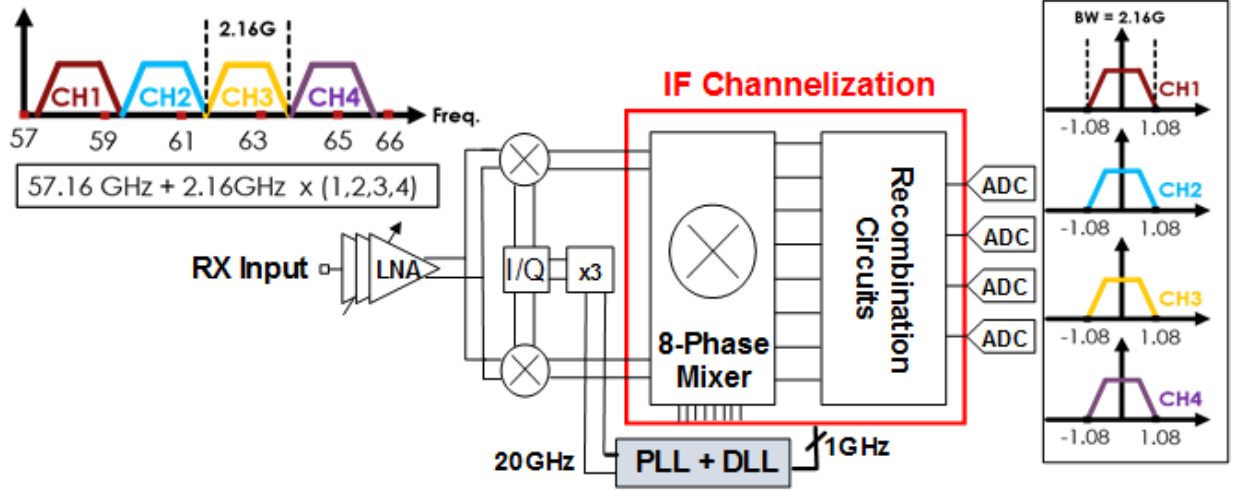


Figure 5.12: Proposed 60GHz channel-bonding architecture.

#### 5.4.1 Proposed Single-Element Fully-Integrated mm-wave Receiver Front-End for 60GHz Channel-Bonding

Fig. 5.13 shows the proposed single-element fully-integrated mm-wave receiver front-end for 60GHz channel-bonding. In the proposed receiver front-end, unlike [11], only single set of mm-wave building blocks such as low-noise-amplifier (LNA), mixer, and PLL are used to receive and translate all the information into baseband. The channelization of the four channels is achieved by the proposed IF channelizer following the mm-wave front-end.

By utilizing just a single set of mm-wave building blocks, namely a single downconversion path at mm-wave frequency, the hardware complexity, power consumption, and calibration overhead can be minimized. As will be discussed in the following subsection, the proposed architecture and frequency planning will not only perform channelization, but also address

the aforementioned ADC sampling speed challenge associated with channel-bonding and the notorious LO tuning-range issue.

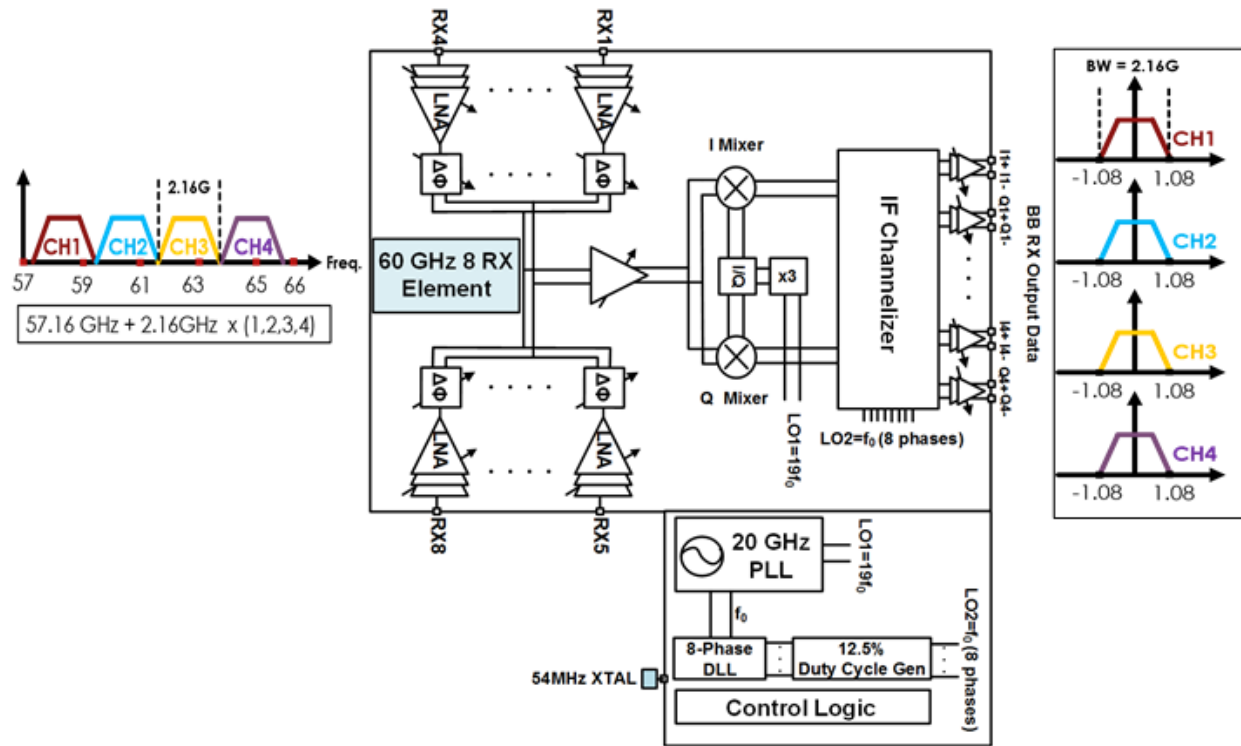


Figure 5.13: Proposed fully-integrated 60GHz channel-bonding receiver.

### 5.4.2 Proposed Shared-LO IF Channelizer with Harmonic Channel-Selectivity

Fig. 5.14 shows the proposed channelizer architecture. The proposed channelizer comprises a 8-phase harmonic-rejection mixer (HRM) and baseband recombination circuitry. The proposed channelizer enables channel selectivity at its output through harmonic rejection and image rejection.

The Harmonic rejection or harmonic selectivity associated with the proposed channelizer is achieved through effective LO synthesis and reconfigurable baseband recombining gm-cells by utilizing an 8-phase 12.5% duty-cycle non-overlapping LO. The effective LO synthesis

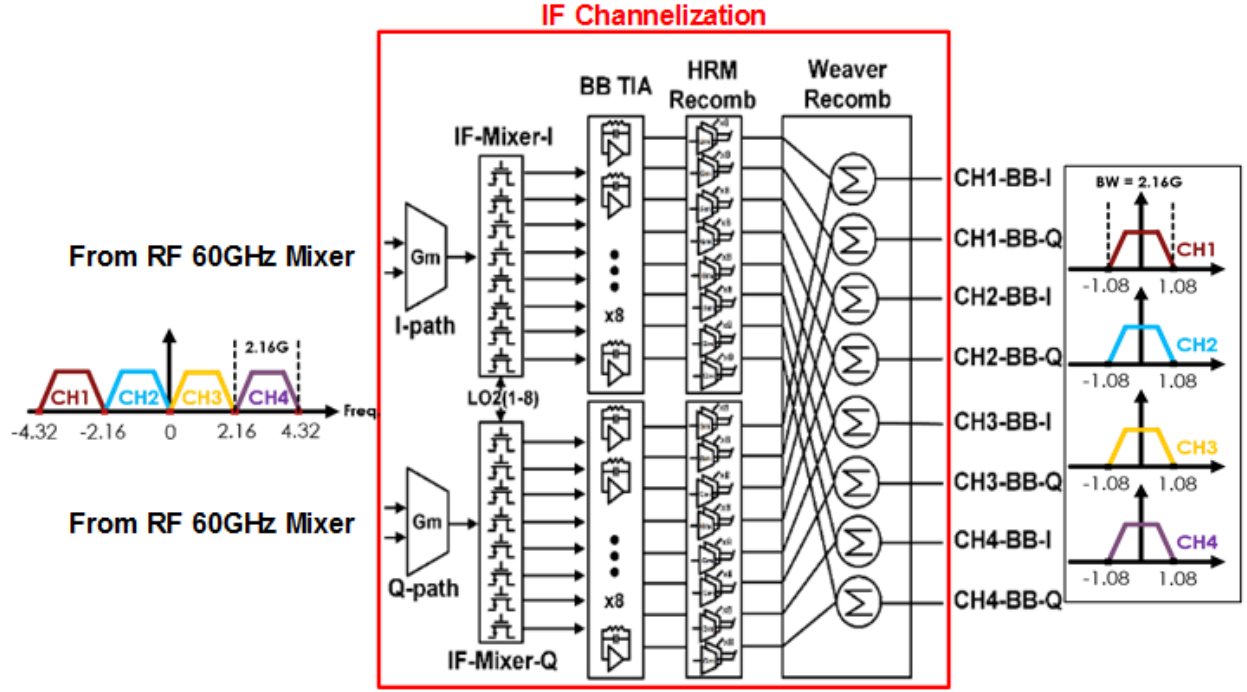


Figure 5.14: Proposed IF channelizer architecture.

technique is a way to generate an LO frequency that are harmonically-related to the fundamental frequency of the multi-phase non-overlapping LO signal without using tuned filter or resonator. Fig. 5.15 shows concept of the effective LO synthesis scheme for the proposed IF channelizer. Essentially, a multi-phase non-overlapping LO signal can be thought of as a over-sampled signal with the over-sampling ratio,  $N$ , equal to the number of non-overlapping phases. Conceptually, by purposely weighting and summing the individual non-overlapping phases of the signal, any harmonic of the LO fundamental frequency smaller than  $N$  can be synthesized.

This way one can derive an LO frequency by using a lower frequency signal or reconfigure the LO frequency by rearranging the coefficient associated with each phases. The downside of this approach is that

- (a) Multiphase LO generator needs to be incorporated.
- (b) The synthesized LO signal is always weaker than the original LO signal and is

attenuated more as the harmonic index increases.

- (c) The synthesized signal always comes with a byproduct at  $(N-M)$  harmonic frequency where  $N$  is the total number of phases and  $M$  is the harmonic index of the synthesized frequency.

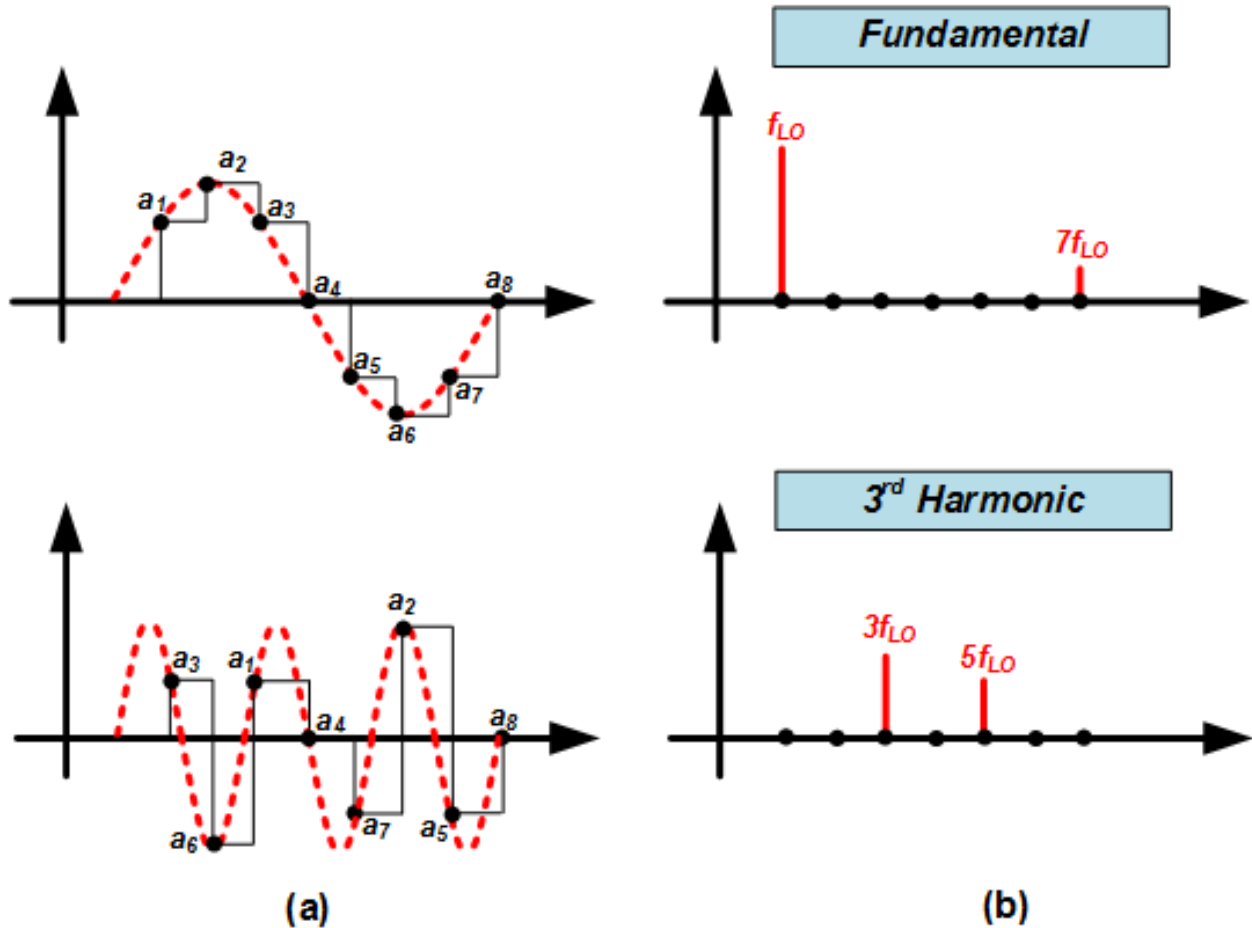


Figure 5.15: Timing diagram of harmonic-rejection-based programmable LO generation technique.

### 5.4.3 Proposed Single LO Frequency Generation Scheme

Fig. 5.16 shows the single-PLL solution for the fully-integrated receiver. It comprises a 20GHz PLL, 20GHz frequency tripler, and a 1GHz DLL with multi-phase LO generator.

The 20GHz PLL comprises a 20GHz VCO with 20% tuning-range, a divide by 400 divider nested in a conventional charge-pump PLL.

The frequency planning of the proposed LO path design is the following. The 20GHz VCO will be locked in a PLL and its frequency will be multiplied by a frequency tripler at the PLL output to generate the 60GHz LO signal. The differential 60GHz will further drive a 90 degree hybrid to generate the required I/Q signal to drive the mixer in the RF path.

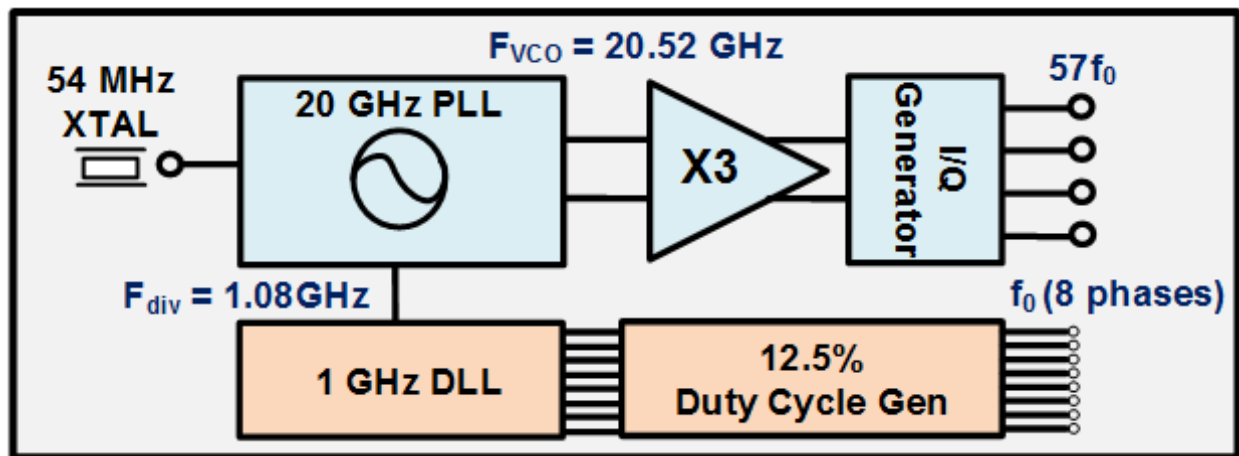


Figure 5.16: Proposed 20GHz LO path design for the proposed 60GHz receiver.

Within the PLL, the VCO signal will first be divided by an divide-by-20 high frequency divider. The frequency of this divider output will be at around 1GHz, making it suitable to be used for the harmonic-rejection mixer in the proposed IF channelizer. Therefore, this 1GHz divider output signal drive two blocks (1) Another divider in the PLL loop to close the feedback loop (2) A 1GHz DLL for multi-phase LO generation.

The DLL output will further drive a 12.5% duty-cycle generator to produce the 12.5% non-overlapping signal for the harmonic-rejection mixer of the proposed channelizer.

## 5.5 System-level Specification Requirement Analysis

### 5.5.1 Analysis of Link Budget

Fig. 5.17 shows a block diagram for a link-budget analysis for the proposed 60GHz channel-bonding receiver (with a fictitious transmitter for analysis purposes). To establish a >10Gb/s wireless link with 10-meter range, it is expected that sophisticated modulation and coding scheme such as 16-QAM or 64-QAM in conjunction with OFDM will be applied. To achieve the required SNR, a high-power PA together with phased-array transceiver arrangement is also unavoidable due to the higher free-space path loss at mm-wave frequencies. The physical dimension such as the size of antenna and its spacing of the phased-array will also benefit from the shorter wavelength at this frequency.

As shown in Fig. 5.17 and Eq. 5.5 5.6 5.7 5.8, for an 8-element transceiver with 8dBm  $P_{average}$ , 6dB antenna gain, 7dB receiver noise figure, and 3dB insertion loss due to the front-end interconnection or assembly loss, 24dB SNR can be achieved. For a BER of  $1e_{-3}$ , the SNR requirement for 16-QAM modulation of a transceiver is -24dB and it translates to  $\approx 18\text{Gb/s}$  ( $4 \cdot 4.6\text{Gb/s}$ ) data-rate.

$$P_{average,single} = P_{1dB} - PAPR = 20dBm - 12dB = 8dBm \quad (5.5)$$

Where PAPR is the peak-to-average-ratio of the transmitted signal. In an OFDM scheme, it is assumed that a PAPR of 12dB is required.

$$PL(PropogationLoss) = -\left(\frac{\lambda}{4\pi R}\right)^2 \quad (5.6)$$

Where the propagation loss is assumed to be in free-space.

$$\begin{aligned} P_{RX,sig} &= P_{average,single} + TX_{power-combined} + TX_{array-factor} + G_{ANT_{TX}} \\ &\quad - PL + G_{ANT_{RX}} + RX_{array-factor} \\ &= 8dBm + 9dB + 9dB + 6dBi - 88dB + 6dBi + 9dB \\ &= -41dBm \end{aligned} \quad (5.7)$$

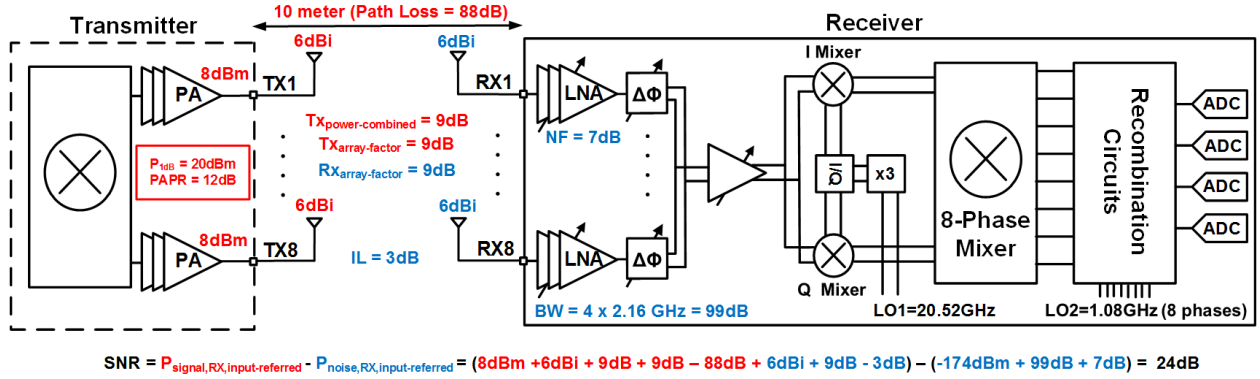


Figure 5.17: Link budget analysis for the proposed 60GHz receiver.

$$\begin{aligned}
 P_{RX,noise} &= -174\text{dBm} + 10\log(BW) + NF_{RX} + IL_{Front-end} \\
 &= -174\text{dBm} + 99\text{dB} + 7\text{dB} + 3\text{dB} = -65\text{dBm}
 \end{aligned} \tag{5.8}$$

### 5.5.2 Image-Rejection-Ratio (IMRR) Requirement

The image-rejection-ratio (IMRR) of an I/Q demodulating system with given amplitude imbalance  $\gamma$  ( $\epsilon = \gamma - 1$ ) and phase imbalance  $\phi$  can be expressed as

$$\begin{aligned}
 IMRR &= \frac{\gamma^2 + 1 - 2\gamma\cos(\phi)}{\gamma^2 + 1 + 2\gamma\cos(\phi)} \\
 &\approx \frac{\epsilon^2 + \phi^2}{4}
 \end{aligned} \tag{5.9}$$

### 5.5.3 Harmonic-Rejection-Ratio (HRR) Requirement

Harmonic-rejection-ratio can be expressed as

$$HRR = \frac{\alpha}{2 + \alpha} \tag{5.10}$$

where  $\alpha$  is the error value between the normalized coefficient of the integer approximation to  $\sqrt{2}$ . If  $\alpha$  is  $\ll 2$ ,

$$HRR \approx \frac{\alpha}{2} \tag{5.11}$$

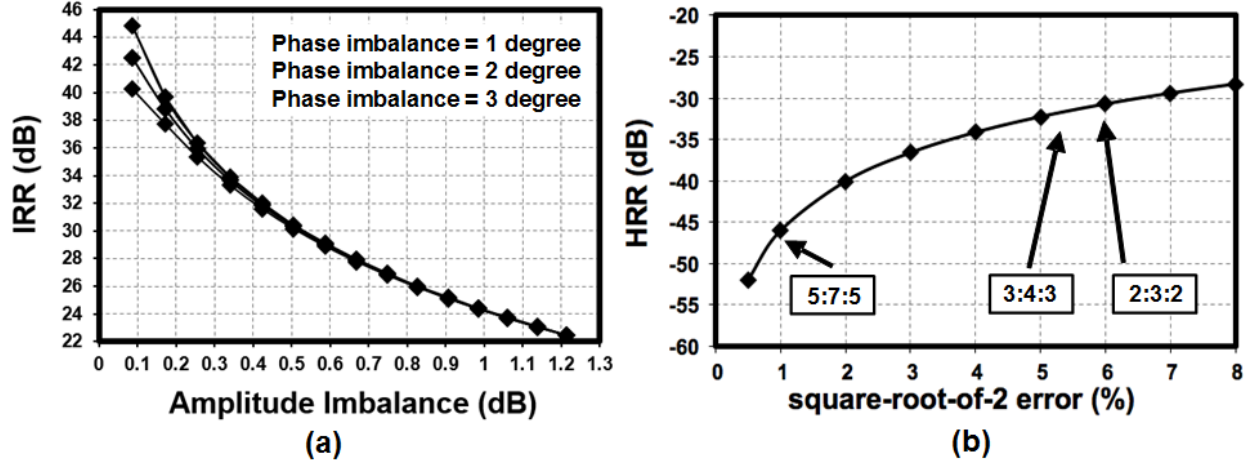


Figure 5.18: (a) Image-rejection ratio vs. Amplitude and phase imbalance. (b) Harmonic-rejection ratio (HRR) vs. the error-to- $\sqrt{2}$

## 5.6 Implementation of Local Oscillator Path for the Proposed 60GHz Channel-Bonding Receiver

Fig. 5.19 shows the implementation of the proposed LO path and frequency planning. The external 54MHz crystal oscillator will drive the PLL to generate a 20GHz differential LO signal. This 20GHz differential LO signal will further drive a frequency tripler and a passive I/Q generator (not shown in this figure) to generate the differential I/Q 60GHz LO signal for the mm-wave frequency mixer.

The PLL is implemented with conventional charge-pump integer-N architecture. Fig. x shows the schematic of the 20GHz LC-VCO. The 20 GHz LC-VCO can be tuned from 18-23GHz with 7-bit thermometer-coded digital tuning capability. The designed value for the differential inductor is 200pH with a  $Q = 20$  at 20GHz.

The LC-VCO output drives the high-frequency pre-scaler and digital divider to close the feedback loop. The high frequency pre-scaler comprises current-mode-logic (CML)-based divide-by-2 circuitry and a cascaded dual-modulus divider to further divide the signal to

1GHz. The 1GHz divider output will drive the DLL to generate multi-phase LO signal for the proposed IF channelizer.

The DLL comprises eight cascaded inverter cell to generate the required 8-phase signal for the non-overlapping 12.5% duty-cycle generator. The output of the delay-cell chain completing the delay of whole cycle will be fed back to be compared with the input of the PLL to ensure the accurate phase relationship with respect to each cell, though the device mismatch will eventually limit its accuracy.

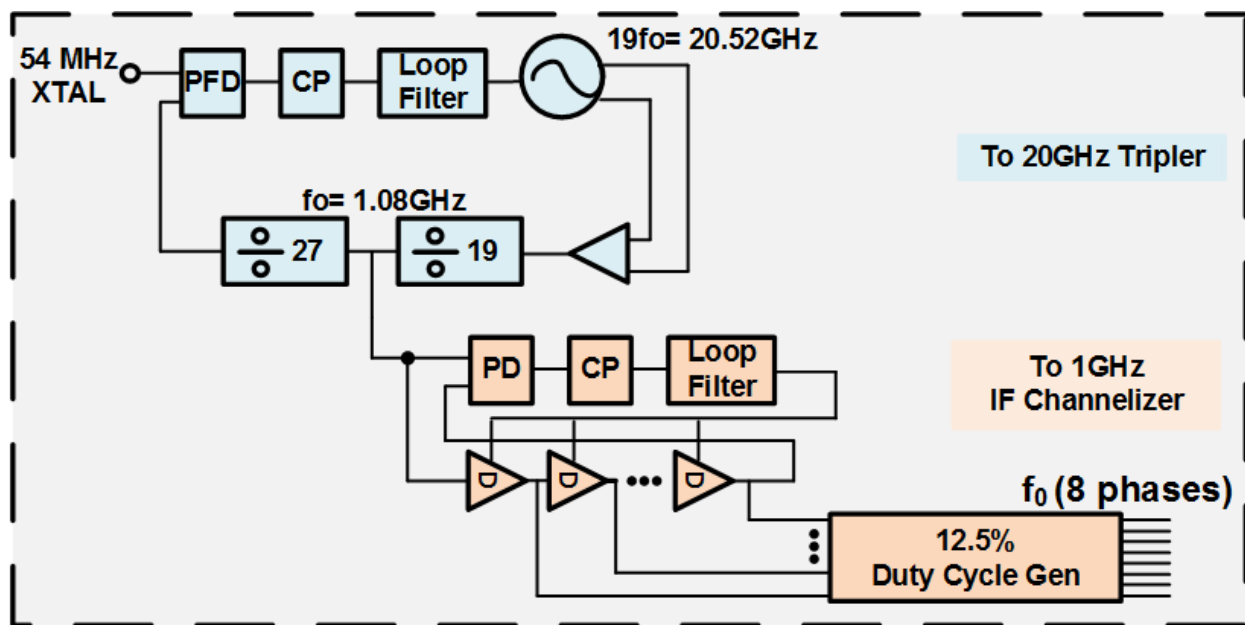


Figure 5.19: Proposed 20GHz LO path design for the proposed 60GHz receiver.

## 5.7 Simulation Result

### 5.7.1 20GHz PLL and 1GHz DLL

Fig. 5.20 shows the simulation result of the tuning range of LC-VCO. Plotted in the figure is the frequency vs.  $V_{tune}$  of the varactor being swept across the digital control word. The VCO can be tuned from 18.4 GHz to 23.2GHz covering the desired frequency at 20.82GHz. Note that the proposed channelizer and frequency greatly ease the tuning-range requirement

for the VCO since it, conceptually, only needs to oscillate at one frequency and the proposed channelizer will take care of the task of sliding channels apart.

Fig. 5.21 shows the designed loop response of the PLL and Fig. 5.21 (a) and (b) show the transient simulation result of the PLL and DLL.

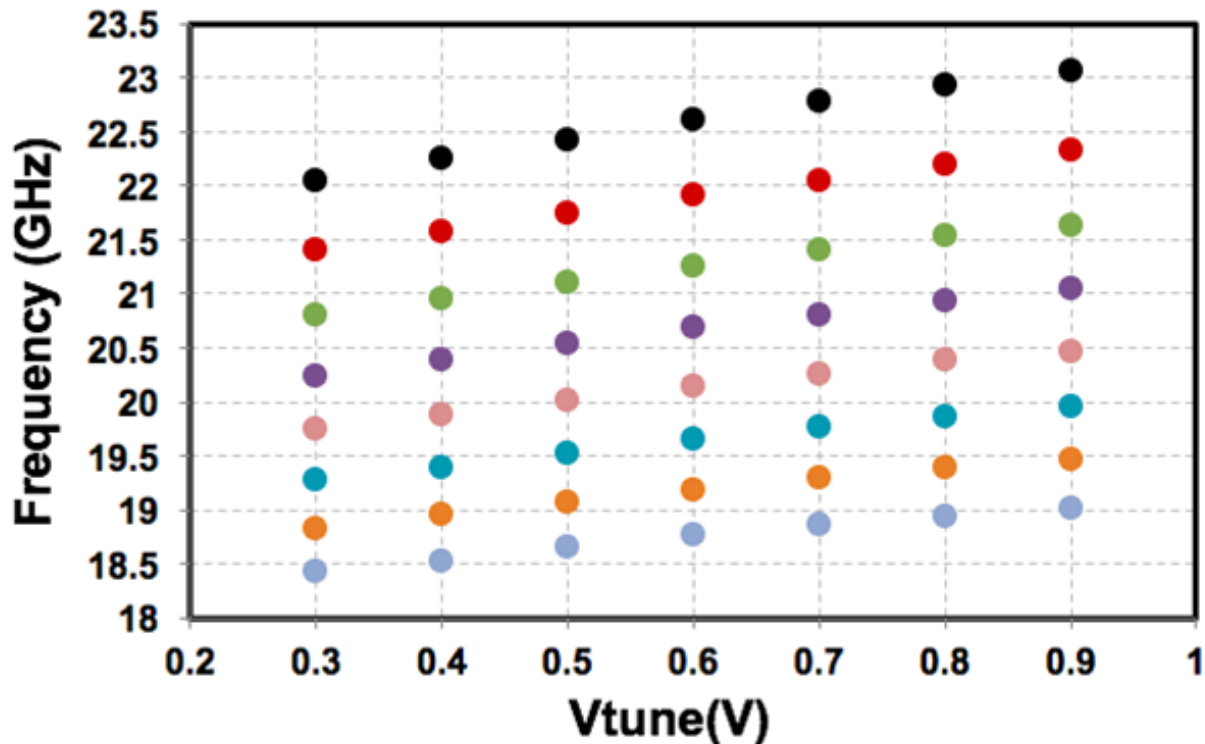


Figure 5.20: Simulated 20GHz VCO tuning-range

### 5.7.2 IF Channelizer and Harmonic Rejection Mixer

Fig. 5.22 shows the simulation result of proposed IF channelizer with ideal LOs. The gain of the desired channel is about 10dB and the harmonic rejection ratio is about 40dB. Image-rejection ratio is infinite in this simulation since I/Q signals from the LO are ideal and are perfectly 90 degree out-of-phase.

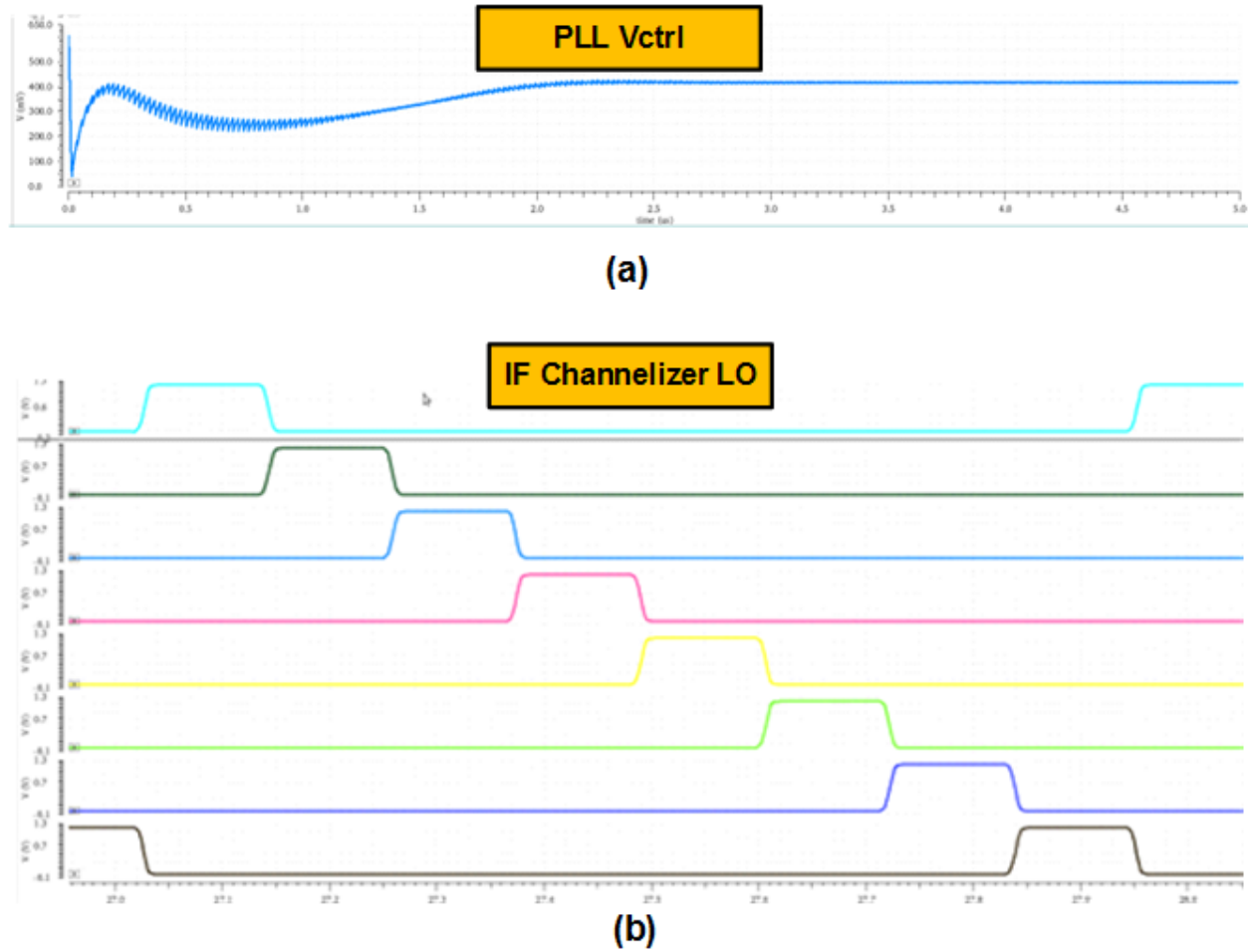


Figure 5.21: a) Proposed PLL transient locking simulation (b) Proposed DLL transient simulation

## 5.8 45nm CMOS SOI Prototype

The chip photo is shown in Fig. 5.23

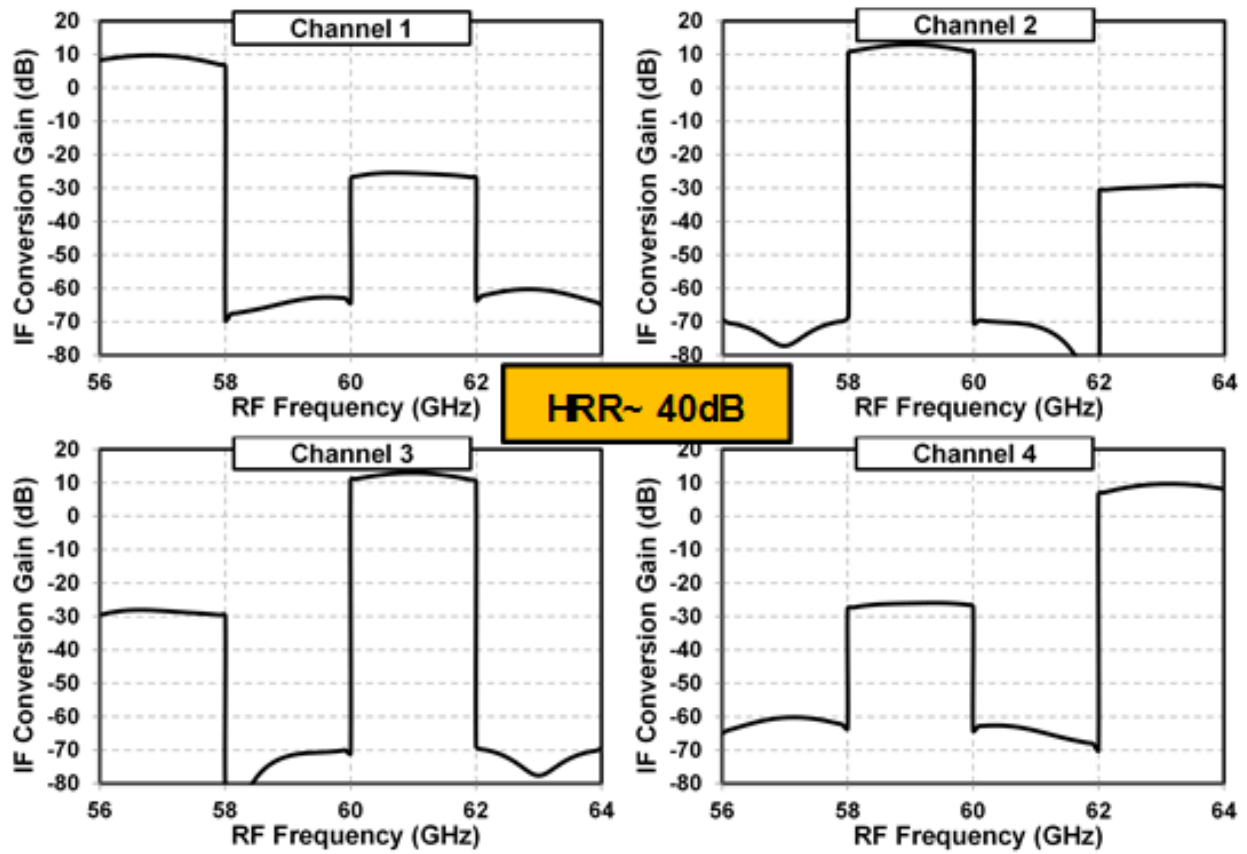


Figure 5.22: Simulated channel response for proposed IF channelizer.

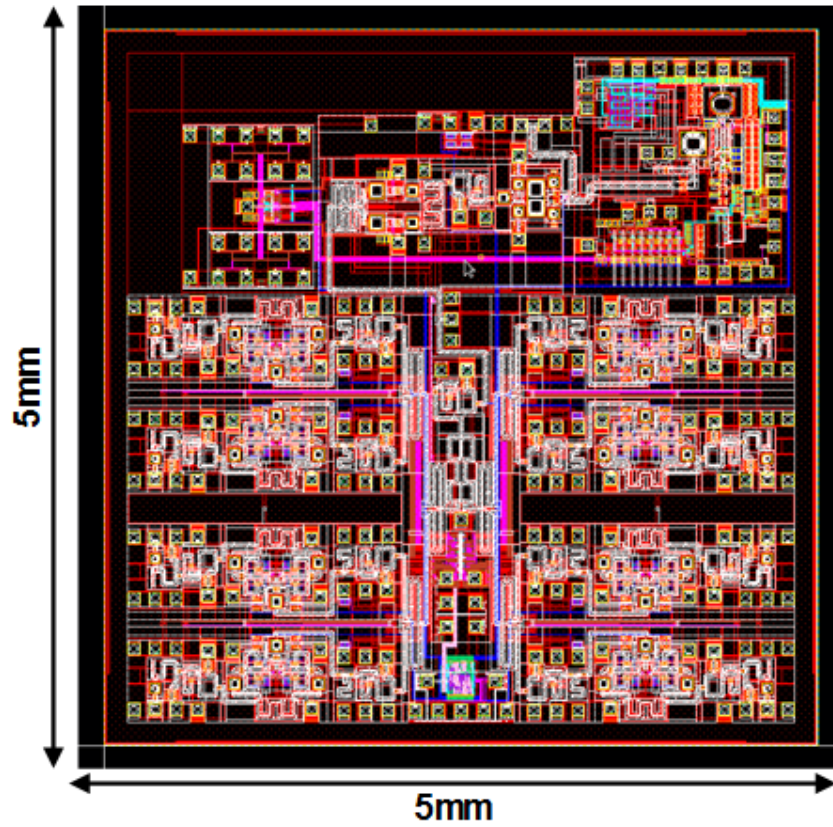


Figure 5.23: Layout of proposed 60GHz channel-bonding receiver.

## 5.9 Conclusion and Future Work

This chapter began with a discussion of the challenge of implementing 60GHz channel-bonding radio for the upcoming IEEE 802.11ay standard. The upcoming IEEE 802.11ay standard demands  $> 10\text{Gb/s}$  with respectable range of transmission and reception. To overcome these challenges, radio architectures have been proposed to ease break the baseband channel BW vs. the ADC sampling rate trade-off. However, existing architecture seeks to address this problem by adding tremendous hardware overhead in its implementation and does not fundamentally resolve the issue.

In this chapter, a fully-integrated 60GHz channel-bonding receiver with IF channelization was proposed. This architecture requires only single mm-wave signal path and a single PLL to process the entire signal band of interest around 60GHz. The channelization is performed through the proposed IF channelizer in conjunction with the programmable LO synthesis technique. By doing this, only one PLL is required for the entire receiver and the baseband BW per channel does not increase in any channel-bonding scheme. The proposed architecture also supports non-contiguous channel-bonding scheme with no design complexity overhead.

The system-level link budget and required image-rejection and harmonic rejection performances have also been analyzed. The proposed prototype of a fully-integrated 8-element 60GHz receiver with a single PLL was demonstrated.

Future research direction includes the validation of the prototype and the possibility of applying the proposed scheme on the transmitter side. Also, it would be interesting to demonstrate the capability of wireless data transmission at a  $> 10\text{Gb/s}$  data-rate for the proposed radio.

# Chapter 6

## Conclusion

his thesis has addressed several challenges associated with LO path design in modern radio. As mentioned in the introduction, modern radios technique often require high-performance LO design assistance to achieve the desire goal.

In Chapter 2, a comparison between conventional fast-settling/hopping LO generation schemes was outlined with a focus on targeting sweeping-LO-based spectrum analysis in CR applications. Subsequently, a zero initial phase error concept for PLL feedback loop settling was introduced. Following the introduction of the zero-initial-phase-error concept, an instantaneous-hop frequency synthesizer architecture featuring a zero-initial-phase-error divider was proposed. An implementation of a 65nm CMOS prototype and its validated measurement result were discussed. There are a few directions that can be pursued to extend the scope of the proposed architecture. Modern PLLs for mobile radios often employ fractional-N instead of integer-N architecture to relax the fundamental trade-off between reference frequency, channel resolution/selectivity, and loop BW. It would be interesting to explore the possibility of incorporating the proposed technique into the schemes of fraction-N PLL. Another interesting direction to explore is calibration. Since the proposed architecture exploits a digital-intensive design, it may require a well-planned calibration scheme and algorithm such that the performance can withstands PVT variation.

Chapter 3 showcased an alternate method of employing I/Q interpolator-based phase

shifter in modern radio design. The functionality of phase shifter are embedded in the LO path design for the radio and the embedded phase-shifting capability enables the radio to perform self-interference cancellation with minimum complexity and design overhead. One possible future research direction is to incorporate digital phase rotator or digital-to-phase converters for the embedded-phase-shifting LO path. Currently, the I/Q signal for the vector modulator is generated by a preceding divide-by-2 circuitry. The output of the digital divider is in the form of square-wave while the  $G_m$ -cell-based vector modulator prefers to take sine-wave input to perform linear vector summation. The current solution incorporate a slew-rate controller to mitigate the non-linearity due to the square-wave input. However, to drive the mixer at the output, buffering the output of the vector modulator is again required to convert the sine-wave back to square-wave. This process inevitably increases the power consumption and induces a phase noise penalty to the overall system. Therefore, a digital-to-phase converter with sufficient resolution can be an ideal candidate for our system.

Chapter 4 proposed a PLL architecture that simultaneously address the active time-based loop filter's noise penalty and area-efficient loop filter implementation challenges with minimal design and complexity overhead, thus resulting in an ultra-low-area PLL with low phase noise performance. This also points to the opportunities afforded by sub-sampling, including other active loop filter topologies that can potentially incorporate other interesting functionalities. For instance, it would be interesting to combine the proposed PLL architecture with other phase noise reduction/cancellation technique for ring oscillator-based PLL to further improve the integrated jitter performance or out-of-band spot phase noise performances for wireless application. It would be also of interest to investigate how the proposed architecture can be re-purposed to operate in fractional-N mode.

Finally, in Chapter 5, a fully-integrated 60GHz channel-bonding receiver with IF channelization was proposed. This architecture only requires a single mm-wave signal path and single PLL to process the entire signal band of interest around 60GHz. The channelization is performed through the proposed IF channelizer in conjunction with the programmable LO synthesis technique. In this way, only one PLL is required for the entire receiver and

the baseband bandwidth per channel does not increase in any channel-bonding scheme. The proposed architecture also supports non-contiguous channel-bonding scheme with no design complexity overhead. The system-level link budget and required image-rejection and harmonic rejection performances were also analyzed. The proposed prototype of fully-integrated 8-element 60GHz receiver with single PLL was demonstrated. Future research directions include the validation of the prototype and the possibility of applying the proposed scheme in the transmitter side. Also, it could be relevant to demonstrate the capability of wireless data transmission at a  $> 10\text{Gb/s}$  data-rate for the proposed radio.

# Bibliography

- [1] T.-H. Chuang and H. Krishnaswamy, “An RF Instantaneous-hop Frequency Synthesizer based on a Zero-initial-phase-error Multi-modulus Divider,” in *2014 IEEE Radio Frequency Integrated Circuits Symposium*, June 2014, pp. 433–436.
- [2] J. Zhou, T. H. Chuang, T. Dinc, and H. Krishnaswamy, “Integrated Wideband Self-Interference Cancellation in the RF Domain for FDD and Full-Duplex Wireless,” *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 3015–3031, Dec 2015.
- [3] J. Chuang and H. Krishnaswamy, “A 0.0049mm<sup>2</sup> 2.3GHz Sub-sampling Ring-oscillator PLL with Time-based Loop Filter Achieving -236.2dB Jitter-FOM,” in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2017, pp. 328–329.
- [4] “Spectrum Allocation Chart in the united states of america,” [Online]. Available:<https://www.ntia.doc.gov/files/ntia/publications/2003-allochrt.pdf>.
- [5] V. Valenta, R. Marlek, G. Baudoin, M. Villegas, M. Suarez, and F. Robert, “Survey on spectrum utilization in europe: Measurements, analyses and observations,” in *2010 Proceedings of the Fifth International Conference on Cognitive Radio Oriented Wireless Networks and Communications*, June 2010, pp. 1–5.
- [6] N. Kurd, M. Chowdhury, E. Burton, T. P. Thomas, C. Mozak, B. Boswell, P. Mosalikanti, M. Neidengard, A. Deval, A. Khanna, N. Chowdhury, R. Rajwar, T. M. Wilson, and R. Kumar, “Haswell: A Family of IA 22 nm Processors,” *IEEE Journal of Solid-State Circuits*, vol. 50, no. 1, pp. 49–58, Jan 2015.

- [7] J. Bouras, S. Bouras, T. Georgantas, N. Haralabidis, G. Kamoulakos, C. Kapnistis, S. Kavadias, Y. Kokolakis, P. Merakos, J. Rudell, S. Plevridis, I. Vassiliou, K. Vavelidis, and A. Yamanaka, “A digitally calibrated 5.15-5.825GHz transceiver for 802.11a wireless LANs in 0.18  $\mu\text{m}$  CMOS,” in *2003 IEEE International Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC.*, Feb 2003, pp. 352–498 vol.1.
- [8] C. J. Hansen, “Wigig: Multi-gigabit wireless communications in the 60 GHz Band,” *IEEE Wireless Communications*, vol. 18, no. 6, pp. 6–7, December 2011.
- [9] A. M. Niknejad and H. Hashemi, *mm-Wave Silicon Technology - 60 GHz and Beyond*. Springer, 2008.
- [10] B. Murmann, “ADC Performance Survey 1997-2016,” [Online]. Available: <http://web.stanford.edu/~murmman/adcsurvey.html>.
- [11] R. Wu, S. Kawai, Y. Seo, N. Fajri, K. Kimura, S. Sato, S. Kondo, T. Ueno, T. Siriburanon, S. Maki, B. Liu, Y. Wang, N. Nagashima, M. Miyahara, K. Okada, and A. Matsuzawa, “A 42Gb/s 60GHz CMOS transceiver for IEEE 802.11ay,” in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, Jan 2016, pp. 248–249.
- [12] *Ericsson Mobility Report*. Ericsson, June, 2017.
- [13] T. Yucek and H. Arslan, “A Survey of Spectrum Sensing Algorithms for Cognitive Radio Applications,” *IEEE Communications Surveys Tutorials*, vol. 11, no. 1, pp. 116–130, First 2009.
- [14] Q. Zhao and B. M. Sadler, “A Survey of Dynamic Spectrum Access,” *IEEE Signal Processing Magazine*, vol. 24, no. 3, pp. 79–89, May 2007.
- [15] J. Mitola and G. Q. Maguire, “Cognitive radio: making software radios more personal,” *IEEE Personal Communications*, vol. 6, no. 4, pp. 13–18, Aug 1999.
- [16] B. Razavi, “Cognitive Radio Design Challenges and Techniques,” *IEEE Journal of Solid-State Circuits*, vol. 45, no. 8, pp. 1542–1553, Aug 2010.

- [17] D. Cabric, I. D. O'Donnell, M. S. W. Chen, and R. W. Brodersen, "Spectrum sharing radios," *IEEE Circuits and Systems Magazine*, vol. 6, no. 2, pp. 30–45, 2006.
- [18] B. Sadhu, M. Sturm, B. M. Sadler, and R. Harjani, "Building an on-chip spectrum sensor for cognitive radios," *IEEE Communications Magazine*, vol. 52, no. 4, pp. 92–100, April 2014.
- [19] M. Mikhemar, D. Murphy, A. Mirzaei, and H. Darabi, "A Cancellation Technique for Reciprocal-Mixing Caused by Phase Noise and Spurs," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 3080–3089, Dec 2013.
- [20] H. Wu, M. Mikhemar, D. Murphy, H. Darabi, and M. C. F. Chang, "A Blocker-Tolerant Inductor-Less Wideband Receiver With Phase and Thermal Noise Cancellation," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 2948–2964, Dec 2015.
- [21] L. Kong and B. Razavi, "A 2.4 GHz 4 mw Integer-N Inductorless RF Synthesizer," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 3, pp. 626–635, March 2016.
- [22] Z. Huang, B. Jiang, L. Li, and H. C. Luong, "A  $4.2\mu\text{s}$ -settling-time 3rd-order 2.1GHz Phase-noise-rejection PLL using a Cascaded Time-amplified Clock-skew Sub-sampling DLL," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, Jan 2016, pp. 40–41.
- [23] "Part II: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications Amendment 3: Enhancements for Very High Throughput in the 60 GHz Band." *IEEE Std. 802.11ad-2012*.
- [24] F. M. Gardner, "Charge-Pump Phase-Lock Loops," *Communications, IEEE Transactions on*, vol. 28, no. 11, pp. 1849–1858, 1980.
- [25] J. Craninckx and M. S. J. Steyaert, "A Fully Integrated CMOS DCS-1800 Frequency Synthesizer," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, pp. 2054–2065, Dec 1998.

- [26] W. Rhee, "Design of high-performance CMOS charge pumps in phase-locked loops," in *Proceedings of the 1999 IEEE International Symposium on Circuits and Systems*, vol. 2, Jul 1999, pp. 545–548 vol.2.
- [27] C. S. Vaucher, "An Adaptive PLL Tuning System Architecture Combining High Spectral Purity and Fast Settling Time," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 4, pp. 490–502, April 2000.
- [28] R. B. Staszewski, J. L. Wallberg, S. Rezek, C.-M. Hung, O. E. Eliezer, S. K. Vemulapalli, C. Fernando, K. Maggio, R. Staszewski, N. Barton, M.-C. Lee, P. Cruise, M. Entezari, K. Muhammad, and D. Leipold, "All-digital PLL and Transmitter for Mobile Phones," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2469–2482, Dec 2005.
- [29] V. Kratyuk, P. K. Hanumolu, U. K. Moon, and K. Mayaram, "A Design Procedure for All-Digital Phase-Locked Loops Based on a Charge-Pump Phase-Locked-Loop Analogy," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 54, no. 3, pp. 247–251, March 2007.
- [30] R. B. Staszewski and P. T. Balsara, "All-Digital PLL With Ultra Fast Settling," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 54, no. 2, pp. 181–185, Feb 2007.
- [31] W. Deng, D. Yang, T. Ueno, T. Siriburanon, S. Kondo, K. Okada, and A. Matsuzawa, "A Fully Synthesizable All-Digital PLL With Interpolative Phase Coupled Oscillator, Current-Output DAC, and Fine-Resolution Digital Varactor Using Gated Edge Injection Technique," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 1, pp. 68–80, Jan 2015.
- [32] J. Lee, "A 3-to-8-GHz fast-hopping frequency synthesizer in 0.18 $\mu$ m CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 3, pp. 566–573, March 2006.

- [33] K. Stadius, T. Rapinoja, J. Kaukovuori, J. Rynanen, and K. A. I. Halonen, "Multitone Fast Frequency-Hopping Synthesizer for UWB Radio," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 8, pp. 1633–1641, Aug 2007.
- [34] S. Subramanian and H. Hashemi, "An 800 MSPS Quadrature DDFS and integrated nonlinear DAC-filter with <15ns instantaneous frequency hopping time," in *2013 IEEE MTT-S International Microwave Symposium Digest (MTT)*, June 2013, pp. 1–4.
- [35] C. Y. Yang, J. H. Weng, and H. Y. Chang, "A 5-GHz Direct Digital Frequency Synthesizer Using an Analog-Sine-Mapping Technique in 0.35- $\mu\text{m}$  SiGe BiCMOS," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 9, pp. 2064–2072, Sept 2011.
- [36] H. C. Yeoh, J. H. Jung, Y. H. Jung, and K. H. Baek, "A 1.3-GHz 350-mW Hybrid Direct Digital Frequency Synthesizer in 90-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 9, pp. 1845–1855, Sept 2010.
- [37] K. Woo, Y. Liu, E. Nam, and D. Ham, "Fast-Lock Hybrid PLL Combining Fractional-N and Integer-N Modes of Differing Bandwidths," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 2, pp. 379–389, 2008.
- [38] C.-S. Lin, T.-H. Chien, C.-L. Wey, C.-M. Huang, and Y. Z. Juang, "An Edge Missing Compensator for Fast Settling Wide Locking Range Phase-Locked Loops," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 11, pp. 3102–3110, 2009.
- [39] W.-H. Chiu, Y.-H. Huang, and T.-H. Lin, "A Dynamic Phase Error Compensation Technique for Fast-Locking Phase-Locked Loops," *Solid-State Circuits, IEEE Journal of*, vol. 45, no. 6, pp. 1137–1149, 2010.
- [40] X. Kuang and N. Wu, "A Fast-settling PLL Frequency Synthesizer with Direct Frequency Presetting," in *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International*, 2006, pp. 741–750.

- [41] R. Staszewski, C.-M. Hung, D. Leipold, and P. Balsara, “A First Multi-Gigahertz Digitally Controlled Oscillator for Wireless Applications,” *Microwave Theory and Techniques, IEEE Transactions on*, vol. 51, no. 11, pp. 2154–2164, 2003.
- [42] P. K. Hanumolu, V. Kratyuk, G. Y. Wei, and U. K. Moon, “A Sub-Picosecond Resolution 0.5-1.5 GHz Digital-to-Phase Converter,” *IEEE Journal of Solid-State Circuits*, vol. 43, no. 2, pp. 414–424, Feb 2008.
- [43] A. Natarajan, A. Komijani, X. Guan, A. Babakhani, and A. Hajimiri, “A 77-GHz Phased-Array Transceiver With On-Chip Antennas in Silicon: Transmitter and Local LO-Path Phase Shifting,” *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2807–2819, Dec 2006.
- [44] A. Natarajan, S. K. Reynolds, M. D. Tsai, S. T. Nicolson, J. H. C. Zhan, D. G. Kam, D. Liu, Y. L. O. Huang, A. Valdes-Garcia, and B. A. Floyd, “A Fully-Integrated 16-Element Phased-Array Receiver in SiGe BiCMOS for 60-GHz Communications,” *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 1059–1075, May 2011.
- [45] L. Smaini, C. Tinella, D. Helal, C. Stoecklin, L. Chabert, C. Devaucelle, R. Cattenoz, N. Rinaldi, and D. Belot, “Single-chip CMOS Pulse Generator for UWB Systems,” *IEEE Journal of Solid-State Circuits*, vol. 41, no. 7, pp. 1551–1561, July 2006.
- [46] A. Goel, B. Analui, and H. Hashemi, “Tunable Duplexer With Passive Feed-Forward Cancellation to Improve the RX-TX Isolation,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 2, pp. 536–544, Feb 2015.
- [47] V. Aparin, G. J. Ballantyne, C. J. Persico, and A. Cicalini, “An Integrated LMS Adaptive Filter of TX Leakage for CDMA Receiver Front-ends,” *IEEE Journal of Solid-State Circuits*, vol. 41, no. 5, pp. 1171–1182, May 2006.
- [48] J. Zhou, A. Chakrabarti, P. R. Kinget, and H. Krishnaswamy, “Low-Noise Active Cancellation of Transmitter Leakage and Transmitter Noise in Broadband Wireless Re-

- ceivers for FDD/Co-Existence,” *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 3046–3062, Dec 2014.
- [49] T. Zhang, A. R. Suvarna, V. Bhagavatula, and J. C. Rudell, “An Integrated CMOS Passive Self-Interference Mitigation Technique for FDD Radios,” *IEEE Journal of Solid-State Circuits*, vol. 50, no. 5, pp. 1176–1188, May 2015.
- [50] A. Sabharwal, P. Schniter, D. Guo, D. W. Bliss, S. Rangarajan, and R. Wichman, “In-Band Full-Duplex Wireless: Challenges and Opportunities,” *IEEE Journal on Selected Areas in Communications*, vol. 32, no. 9, pp. 1637–1652, Sept 2014.
- [51] J. I. Choi, S. Hong, M. Jain, S. Katti, P. Levis, and J. Mehlman, “Beyond full duplex wireless,” in *2012 Conference Record of the Forty Sixth Asilomar Conference on Signals, Systems and Computers (ASILOMAR)*, Nov 2012, pp. 40–44.
- [52] D. Yang and A. Molnar, “A Widely-tunable Active Duplexing Transceiver with Same-channel Concurrent RX/TX and 30dB RX/TX Isolation,” in *2014 IEEE Radio Frequency Integrated Circuits Symposium*, June 2014, pp. 321–324.
- [53] T. Dinc, A. Chakrabarti, and H. Krishnaswamy, “A 60 GHz CMOS Full-Duplex Transceiver and Link with Polarization-Based Antenna and RF Cancellation,” *IEEE Journal of Solid-State Circuits*, vol. 51, no. 5, pp. 1125–1140, May 2016.
- [54] A. Ghaffari, E. A. M. Klumperink, M. C. M. Soer, and B. Nauta, “Tunable High-Q N-Path Band-Pass Filters: Modeling and Verification,” *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 998–1010, May 2011.
- [55] N. Reiskarimian, J. Zhou, T. H. Chuang, and H. Krishnaswamy, “Analysis and Design of Two-Port N-path Bandpass Filters With Embedded Phase Shifting,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 8, pp. 728–732, Aug 2016.

- [56] M. C. M. Soer, E. A. M. Klumperink, P. T. de Boer, F. E. van Vliet, and B. Nauta, “Unified Frequency-Domain Analysis of Switched-Series-RC Passive Mixers and Samplers,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 10, pp. 2618–2631, Oct 2010.
- [57] H. Wang and A. Hajimiri, “A Wideband CMOS Linear Digital Phase Rotator,” in *2007 IEEE Custom Integrated Circuits Conference*, Sept 2007, pp. 671–674.
- [58] J. Zhou, A. Chakrabarti, P. R. Kinget, and H. Krishnaswamy, “Low-Noise Active Cancellation of Transmitter Leakage and Transmitter Noise in Broadband Wireless Receivers for FDD/Co-Existence,” *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 3046–3062, Dec 2014.
- [59] D. Murphy, H. Darabi, A. Abidi, A. A. Hafez, A. Mirzaei, M. Mikhemar, and M. C. F. Chang, “A Blocker-Tolerant, Noise-Cancelling Receiver Suitable for Wideband Wireless Applications,” *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 2943–2963, Dec 2012.
- [60] C. Zhai, J. Fredenburg, J. Bell, and M. P. Flynn, “An N-path filter enhanced low phase noise ring VCO,” in *2014 Symposium on VLSI Circuits Digest of Technical Papers*, June 2014, pp. 1–2.
- [61] M. M. Abdul-Latif and E. Sanchez-Sinencio, “Low Phase Noise Wide Tuning Range N-Push Cyclic-Coupled Ring Oscillators,” *IEEE Journal of Solid-State Circuits*, vol. 47, no. 6, pp. 1278–1294, June 2012.
- [62] N. A. Kurd, S. Bhamidipati, C. Mozak, J. L. Miller, P. Mosalikanti, T. M. Wilson, A. M. El-Husseini, M. Neidengard, R. E. Aly, M. Nemani, M. Chowdhury, and R. Kumar, “A Family of 32 nm IA Processors,” *IEEE Journal of Solid-State Circuits*, vol. 46, no. 1, pp. 119–130, Jan 2011.

- [63] Z. Cao, Y. Li, and S. Yan, "A 0.4 ps-RMS-jitter 1-3 GHz Ring-Oscillator PLL Using Phase-Noise Preamplification," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 9, pp. 2079–2089, Sept 2008.
- [64] X. Gao, E. A. M. Klumperink, M. Bohsali, and B. Nauta, "A Low Noise Sub-Sampling PLL in Which Divider Noise is Eliminated and PD/CP Noise is Not Multiplied by  $N^2$ ," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3253–3263, Dec 2009.
- [65] K. Sogo, A. Toya, and T. Kikkawa, "A Ring-VCO-based Sub-sampling PLL CMOS Circuit with -119 dBc/Hz Phase Noise and 0.73 ps Jitter," in *2012 Proceedings of the ESSCIRC (ESSCIRC)*, Sept 2012, pp. 253–256.
- [66] M. Song, T. Kim, J. Kim, W. Kim, S. J. Kim, and H. Park, "A 0.009mm<sup>2</sup> 2.06mW 32-to-2000MHz 2nd-order  $\Delta$ - $\Sigma$  Analogous Bang-bang Digital PLL with Feed-forward Delay-locked and Phase-locked Operations in 14nm FinFET Technology," in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, Feb 2015, pp. 1–3.
- [67] J. Zhuang, K. Waheed, and R. B. Staszewski, "Design of Spur-Free  $\Sigma$ - $\Delta$  Frequency Tuning Interface for Digitally Controlled Oscillators," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 1, pp. 46–50, Jan 2015.
- [68] P. Lu, A. Liscidini, and P. Andreani, "A 3.6 mW, 90 nm CMOS Gated-Vernier Time-to-Digital Converter With an Equivalent Resolution of 3.2ps," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, pp. 1626–1635, July 2012.
- [69] A. Elshazly, R. Inti, B. Young, and P. K. Hanumolu, "Clock Multiplication Techniques Using Digital Multiplying Delay-locked Loops," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 6, pp. 1416–1428, June 2013.
- [70] J. Lee and H. Wang, "Study of Subharmonically Injection-Locked PLLs," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 5, pp. 1539–1553, May 2009.

- [71] D. Coombs, A. Elkholy, R. K. Nandwana, A. Elmallah, and P. K. Hanumolu, “8.6 A 2.5-to-5.75GHz 5mW 0.3psrms-jitter cascaded ring-based digital injection-locked clock multiplier in 65nm CMOS,” in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2017, pp. 152–153.
- [72] J. Sharma and H. Krishnaswamy, “A dividerless reference-sampling RF PLL with -253.5dB jitterFOM and -67dBc Reference Spurs,” in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, Feb 2018, pp. 258–260.
- [73] A. M. Fahim, “A Compact, Low-power Low-jitter Digital PLL,” in *ESSCIRC 2004 - 29th European Solid-State Circuits Conference*, Sept 2003, pp. 101–104.
- [74] J. W. Moon, K. C. Choi, and W. Y. Choi, “A 0.4-V, 90  $\sim$  350-MHz PLL With an Active Loop-Filter Charge Pump,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 61, no. 5, pp. 319–323, May 2014.
- [75] X. Gao, E. A. M. Klumperink, P. F. J. Geraedts, and B. Nauta, “Jitter Analysis and a Benchmarking Figure-of-Merit for Phase-Locked Loops,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 56, no. 2, pp. 117–121, Feb 2009.
- [76] R. Nonis, N. D. Dalt, P. Palestri, and L. Selmi, “Modeling, Design and Characterization of a New Low-jitter Analog Dual tuning LC-VCO PLL Architecture,” *IEEE Journal of Solid-State Circuits*, vol. 40, no. 6, pp. 1303–1309, June 2005.
- [77] M. Ferriss, J. O. Plouchart, A. Natarajan, A. Rylyakov, B. Parker, J. A. Tierno, A. Babakhani, S. Yaldiz, A. Valdes-Garcia, B. Sadhu, and D. J. Friedman, “An Integral Path Self-Calibration Scheme for a Dual-loop PLL,” *IEEE Journal of Solid-State Circuits*, vol. 48, no. 4, pp. 996–1008, April 2013.
- [78] A. L. S. Loke, R. K. Barnes, T. T. Wee, M. M. Oshima, C. E. Moore, R. R. Kennedy, and M. J. Gilsdorf, “A Versatile 90-nm CMOS Charge-Pump PLL for SerDes Transmitter Clocking,” *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1894–1907, Aug 2006.

- [79] B. Drost, M. Talegaonkar, and P. K. Hanumolu, “Analog Filter Design Using Ring Oscillator Integrators,” *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 3120–3129, Dec 2012.
- [80] J. Zhu, R. K. Nandwana, G. Shu, A. Elkholy, S. J. Kim, and P. K. Hanumolu, “A 0.0021 mm<sup>2</sup> 1.82 mW 2.2 GHz PLL Using Time-Based Integral Control in 65 nm CMOS,” *IEEE Journal of Solid-State Circuits*, vol. 52, no. 1, pp. 8–20, Jan 2017.
- [81] A. T. Narayanan, M. Katsuragi, K. Kimura, S. Kondo, K. K. Tokgoz, K. Nakata, W. Deng, K. Okada, and A. Matsuzawa, “A Fractional-N Sub-Sampling PLL using a Pipelined Phase-Interpolator With an FoM of -250 dB,” *IEEE Journal of Solid-State Circuits*, vol. 51, no. 7, pp. 1630–1640, July 2016.
- [82] J. Wells, “Faster than fiber: The future of multi-Gb/s wireless,” *IEEE Microwave Magazine*, vol. 10, no. 3, pp. 104–112, May 2009.
- [83] T. S. Rappaport, S. Sun, R. Mayzus, H. Zhao, Y. Azar, K. Wang, G. N. Wong, J. K. Schulz, M. Samimi, and F. Gutierrez, “Millimeter Wave Mobile Communications for 5G Cellular: It Will Work!” *IEEE Access*, vol. 1, pp. 335–349, 2013.
- [84] “FCC Spectrum Frontiers Proceeding,” [Online]. Available: [http://transition.fcc.gov/Daily\\_Releases/Daily\\_Business/2016/db0728/FCC-16-89A1.pdf](http://transition.fcc.gov/Daily_Releases/Daily_Business/2016/db0728/FCC-16-89A1.pdf).
- [85] A. Hajimiri, H. Hashemi, A. Natarajan, X. Guan, and A. Komijani, “Integrated Phased Array Systems in Silicon,” *Proceedings of the IEEE*, vol. 93, no. 9, pp. 1637–1655, Sept 2005.
- [86] H. Krishnaswamy and H. Hashemi, “A Fully Integrated 24GHz 4-Channel Phased-Array Transceiver in 0.13  $\mu$ m CMOS Based on a Variable-Phase Ring Oscillator and PLL Architecture,” in *2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, Feb 2007, pp. 124–591.

- [87] J. Lee, Y. A. Li, M. H. Hung, and S. J. Huang, "A Fully-Integrated 77-GHz FMCW Radar Transceiver in 65-nm CMOS Technology," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2746–2756, Dec 2010.
- [88] D. Guermandi, Q. Shi, A. Medra, T. Murata, W. V. Thillo, A. Bourdoux, P. Wambacq, and V. Giannini, "19.7 A 79GHz binary phase-modulated continuous-wave radar transceiver with TX-to-RX spillover cancellation in 28nm CMOS," in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, Feb 2015, pp. 1–3.
- [89] R. Bhat, A. Chakrabarti, and H. Krishnaswamy, "Large-Scale Power Combining and Mixed-Signal Linearizing Architectures for Watt-Class mmWave CMOS Power Amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 2, pp. 703–718, Feb 2015.
- [90] A. Agah, H. T. Dabag, B. Hanafi, P. M. Asbeck, J. F. Buckwalter, and L. E. Larson, "Active Millimeter-Wave Phase-Shift Doherty Power Amplifier in 45-nm SOI CMOS," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 10, pp. 2338–2350, Oct 2013.
- [91] T. LaRocca, Y. C. Wu, R. Snyder, J. Patel, K. Thai, C. Wong, Y. Yang, L. Gilreath, M. Watanabe, H. Wu, and M. C. F. Chang, "A 45GHz CMOS transmitter SoC with digitally-assisted power amplifiers for 64QAM efficiency improvement," in *2013 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2013, pp. 359–362.
- [92] S. K. Reynolds, B. A. Floyd, U. R. Pfeiffer, T. Beukema, J. Grzyb, C. Haymes, B. Gaucher, and M. Soyuer, "A Silicon 60-GHz Receiver and Transmitter Chipset for Broadband Communications," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2820–2831, Dec 2006.
- [93] C. Marcu, D. Chowdhury, C. Thakkar, J. D. Park, L. K. Kong, M. Tabesh, Y. Wang, B. Afshar, A. Gupta, A. Arbabian, S. Gambini, R. Zamani, E. Alon, and A. M. Niknejad, "A 90 nm CMOS Low-Power 60 GHz Transceiver With Integrated Baseband

- Circuitry,” *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3434–3447, Dec 2009.
- [94] P. N. Chen, P. J. Peng, C. Kao, Y. L. Chen, and J. Lee, “A 94GHz 3D-image radar engine with 4TX/4RX beamforming scan technique in 65nm CMOS,” in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, Feb 2013, pp. 146–147.
- [95] A. Townley, P. Swirhun, D. Titz, A. Bisognin, F. Giancesello, R. Pilard, C. Luxey, and A. Niknejad, “A 94GHz 4TX-4RX phased-array for FMCW radar with integrated LO and flip-chip antenna package,” in *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, May 2016, pp. 294–297.
- [96] J. O. Plouchart, W. Lee, C. Ozdag, Y. Aydogan, M. Yeck, A. Cabuk, A. Kepkep, E. Apaydin, and A. Valdes-Garcia, “A fully-integrated 94-GHz 32-element phased-array receiver in SiGe BiCMOS,” in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2017, pp. 380–383.
- [97] B. Sadhu, Y. Tousi, J. Hallin, S. Sahl, S. Reynolds, . Renstrm, K. Sjgren, O. Haapalahti, N. Mazor, B. Bokinge, G. Weibull, H. Bengtsson, A. Carlinger, E. Westesson, J. E. Thillberg, L. Rexberg, M. Yeck, X. Gu, D. Friedman, and A. Valdes-Garcia, “A 28GHz 32-element phased-array transceiver IC with concurrent dual polarized beams and 1.4 degree beam-steering resolution for 5G communication,” in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2017, pp. 128–129.
- [98] H. T. Kim, B. S. Park, S. M. Oh, S. S. Song, J. M. Kim, S. H. Kim, T. S. Moon, S. Y. Kim, J. Y. Chang, S. W. Kim, W. S. Kang, S. Y. Jung, G. Y. Tak, J. K. Du, Y. S. Suh, and Y. C. Ho, “A 28GHz CMOS direct conversion transceiver with packaged antenna arrays for 5G cellular system,” in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2017, pp. 69–72.

- [99] J. Sharma and H. Krishnaswamy, “216- and 316-GHz 45-nm SOI CMOS Signal Sources Based on a Maximum-Gain Ring Oscillator Topology,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 1, pp. 492–504, Jan 2013.
- [100] O. Inac, M. Uzunkol, and G. M. Rebeiz, “45-nm CMOS SOI Technology Characterization for Millimeter-Wave Applications,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 6, pp. 1301–1311, June 2014.
- [101] A. M. Niknejad, S. Emami, B. Heydari, M. Bohsali, and E. Adabi, “Nanoscale CMOS for mm-Wave Applications,” in *2007 IEEE Compound Semiconductor Integrated Circuits Symposium*, Oct 2007, pp. 1–4.
- [102] J. Lee, Y. Chen, and Y. Huang, “A Low-Power Low-Cost Fully-Integrated 60-GHz Transceiver System With OOK Modulation and On-Board Antenna Assembly,” *IEEE Journal of Solid-State Circuits*, vol. 45, no. 2, pp. 264–275, Feb 2010.
- [103] K. Okada, N. Li, K. Matsushita, K. Bunsen, R. Murakami, A. Musa, T. Sato, H. Asada, N. Takayama, S. Ito, W. Chaivipas, R. Minami, T. Yamaguchi, Y. Takeuchi, H. Yamagishi, M. Noda, and A. Matsuzawa, “A 60-GHz 16QAM/8PSK/QPSK/BPSK Direct-Conversion Transceiver for IEEE802.15.3c,” *IEEE Journal of Solid-State Circuits*, vol. 46, no. 12, pp. 2988–3004, Dec 2011.
- [104] K. Okada, K. Kondou, M. Miyahara, M. Shinagawa, H. Asada, R. Minami, T. Yamaguchi, A. Musa, Y. Tsukui, Y. Asakura, S. Tamonoki, H. Yamagishi, Y. Hino, T. Sato, H. Sakaguchi, N. Shimasaki, T. Ito, Y. Takeuchi, N. Li, Q. Bu, R. Murakami, K. Bunsen, K. Matsushita, M. Noda, and A. Matsuzawa, “Full Four-Channel 6.3-Gb/s 60-GHz CMOS Transceiver With Low-Power Analog and Digital Baseband Circuitry,” *IEEE Journal of Solid-State Circuits*, vol. 48, no. 1, pp. 46–65, Jan 2013.
- [105] V. Vidojkovic, V. Szortyka, K. Khalaf, G. Mangraviti, S. Brebels, W. v. Thillo, K. Vae-sen, B. Parvais, V. Issakov, M. Libois, M. Matsuo, J. Long, C. Soens, and P. Wambacq,

- “A Low-power Radio Chipset in 40nm LP CMOS with Beamforming for 60GHz High-data-rate Wireless Communication,” in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, Feb 2013, pp. 236–237.
- [106] K. Okada, R. Minami, Y. Tsukui, S. Kawai, Y. Seo, S. Sato, S. Kondo, T. Ueno, Y. Takeuchi, T. Yamaguchi, A. Musa, R. Wu, M. Miyahara, and A. Matsuzawa, “20.3 a 64-QAM 60GHz CMOS transceiver with 4-channel bonding,” in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb 2014, pp. 346–347.
- [107] J. Pang, S. Maki, S. Kawai, N. Nagashima, Y. Seo, M. Dome, H. Kato, M. Katsuragi, K. Kimura, S. Kondo, Y. Terashima, H. Liu, T. Siriburanon, A. T. Narayanan, N. Fajri, T. Kaneko, T. Yoshioka, B. Liu, Y. Wang, R. Wu, N. Li, K. K. Tokgoz, M. Miyahara, K. Okada, and A. Matsuzawa, “A 128-QAM 60GHz CMOS transceiver for IEEE802.11ay with calibration of lo feedthrough and I/Q imbalance,” in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, Feb 2017, pp. 424–425.
- [108] A. Valdes-Garcia, S. Nicolson, J. W. Lai, A. Natarajan, P. Y. Chen, S. Reynolds, J. H. C. Zhan, and B. Floyd, “A SiGe BiCMOS 16-element phased-array transmitter for 60GHz communications,” in *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, Feb 2010, pp. 218–219.
- [109] A. Natarajan, S. K. Reynolds, M. D. Tsai, S. T. Nicolson, J. H. C. Zhan, D. G. Kam, D. Liu, Y. L. O. Huang, A. Valdes-Garcia, and B. A. Floyd, “A fully-Integrated 16-Element Phased-array Receiver in SiGe BiCMOS for 60-GHz Communications,” *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 1059–1075, May 2011.
- [110] S. Emami, R. F. Wiser, E. Ali, M. G. Forbes, M. Q. Gordon, X. Guan, S. Lo, P. T. McElwee, J. Parker, J. R. Tani, J. M. Gilbert, and C. H. Doan, “A 60GHz CMOS phased-array transceiver pair for multi-Gb/s wireless communications,” in *2011 IEEE International Solid-State Circuits Conference*, Feb 2011, pp. 164–166.

- [111] N. Saito, T. Tsukizawa, N. Shirakata, T. Morita, K. Tanaka, J. Sato, Y. Morishita, M. Kanemaru, R. Kitamura, T. Shima, T. Nakatani, K. Miyanaga, T. Urushihara, H. Yoshikawa, T. Sakamoto, H. Motozuka, Y. Shirakawa, N. Yosoku, A. Yamamoto, R. Shiozaki, and K. Takinami, "A fully Integrated 60-GHz CMOS Transceiver Chipset Based on WiGig/IEEE 802.11ad With Built-In Self Calibration for Mobile Usage," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 3146–3159, Dec 2013.
- [112] M. Boers, B. Afshar, I. Vassiliou, S. Sarkar, S. T. Nicolson, E. Adabi, B. G. Perumana, T. Chalvatzis, S. Kavvadias, P. Sen, W. L. Chan, A. H. T. Yu, A. Parsa, M. Nariman, S. Yoon, A. G. Besoli, C. A. Kyriazidou, G. Zochios, J. A. Castaneda, T. Sowlati, M. Rofougaran, and A. Rofougaran, "A 16TX/16RX 60 GHz 802.11ad Chipset With Single Coaxial Interface and Polarization Diversity," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 3031–3045, Dec 2014.
- [113] S. Saigusa, T. Mitomo, H. Okuni, M. Hosoya, A. Sai, S. Kawai, T. Wang, M. Furuta, K. Shiraishi, K. Ban, S. Horikawa, T. Tandai, R. Matsuo, T. Tomizawa, H. Hoshino, J. Matsuno, Y. Tsutsumi, R. Tachibana, O. Watanabe, and T. Itakura, "A Fully-integrated single-chip 60GHz CMOS transceiver with scalable power consumption for proximity wireless communication," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, Feb 2014, pp. 348–349.
- [114] A. Tomkins, A. Poon, E. Juntunen, A. El-Gabaly, G. Temkine, Y. L. To, C. Farnsworth, A. Tabibiazar, M. Fakharzadeh, S. Jafarlou, A. Abdellatif, H. Tawfik, B. Lynch, M. Tazlauanu, and R. Glibbery, "A 60 GHz, 802.11ad/WiGig-Compliant Transceiver for Infrastructure and Mobile Applications in 130 nm SiGe BiCMOS," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 10, pp. 2239–2255, Oct 2015.
- [115] B. Sadhu, A. Valdes-Garcia, J. O. Plouchart, H. Ainspan, A. K. Gupta, M. Ferriss, M. Yeck, M. Sanduleanu, X. Gu, C. Baks, D. Liu, and D. Friedman, "A 60GHz packaged switched beam 32nm CMOS TRX with broad spatial coverage, 17.1dBm peak

- EIRP, 6.1dB NF at <250mW,” in *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, May 2016, pp. 342–343.
- [116] C. Cao and K. K. O, “Millimeter-wave Voltage-controlled Oscillators in 0.13 $\mu$ m CMOS Technology,” *IEEE Journal of Solid-State Circuits*, vol. 41, no. 6, pp. 1297–1304, June 2006.
- [117] Z. Zong, M. Babaie, and R. B. Staszewski, “A 60 GHz Frequency Generator Based on a 20 GHz Oscillator and an Implicit Multiplier,” *IEEE Journal of Solid-State Circuits*, vol. 51, no. 5, pp. 1261–1273, May 2016.
- [118] W. Deng, T. Siriburanon, A. Musa, K. Okada, and A. Matsuzawa, “A Sub-Harmonic Injection-Locked Quadrature Frequency Synthesizer With Frequency Calibration Scheme for Millimeter-Wave TDD Transceivers,” *IEEE Journal of Solid-State Circuits*, vol. 48, no. 7, pp. 1710–1720, July 2013.
- [119] D. Murphy, Q. J. Gu, Y. C. Wu, H. Y. Jian, Z. Xu, A. Tang, F. Wang, and M. C. F. Chang, “A Low Phase Noise, Wideband and Compact CMOS PLL for Use in a Heterodyne 802.15.3c Transceiver,” *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7, pp. 1606–1617, July 2011.
- [120] B. Sadhu, M. Ferriss, and A. Valdes-Garcia, “A 52 GHz Frequency Synthesizer Featuring a 2nd Harmonic Extraction Technique That Preserves VCO Performance,” *IEEE Journal of Solid-State Circuits*, vol. 50, no. 5, pp. 1214–1223, May 2015.
- [121] V. Szortyka, Q. Shi, K. Raczkowski, B. Parvais, M. Kuijk, and P. Wambacq, “A 42 mW 200fs-Jitter 60 GHz Sub-Sampling PLL in 40 nm CMOS,” *IEEE Journal of Solid-State Circuits*, vol. 50, no. 9, pp. 2025–2036, Sept 2015.
- [122] X. Yi, C. C. Boon, H. Liu, J. F. Lin, and W. M. Lim, “A 57.9-to-68.3 GHz 24.6 mW Frequency Synthesizer With In-Phase Injection-Coupled QVCO in 65 nm CMOS Technology,” *IEEE Journal of Solid-State Circuits*, vol. 49, no. 2, pp. 347–359, Feb 2014.

- [123] A. Li, S. Zheng, J. Yin, X. Luo, and H. C. Luong, “A 21-48 GHz Subharmonic Injection-Locked Fractional-N Frequency Synthesizer for Multiband Point-to-Point Backhaul Communications,” *IEEE Journal of Solid-State Circuits*, vol. 49, no. 8, pp. 1785–1799, Aug 2014.
- [124] B. A. Floyd, “A 16-18.8-GHz Sub-Integer-N Frequency Synthesizer for 60-GHz Transceivers,” *IEEE Journal of Solid-State Circuits*, vol. 43, no. 5, pp. 1076–1086, May 2008.
- [125] B. Sadhu, M. A. Ferriss, A. S. Natarajan, S. Yaldiz, J. O. Plouchart, A. V. Rylyakov, A. Valdes-Garcia, B. D. Parker, A. Babakhani, S. Reynolds, X. Li, L. Pileggi, R. Harjani, J. A. Tierno, and D. Friedman, “A linearized, low-phase-noise VCO-based 25-GHz PLL with autonomic biasing,” *IEEE Journal of Solid-State Circuits*, vol. 48, no. 5, pp. 1138–1150, May 2013.
- [126] J. F. Osorio, C. S. Vaucher, B. Huff, E. v. d. Heijden, and A. de Graauw, “A 21.7-to-27.8GHz 2.6-degrees-rms 40mW frequency synthesizer in 45nm CMOS for mm-Wave communication applications,” in *2011 IEEE International Solid-State Circuits Conference*, Feb 2011, pp. 278–280.
- [127] E. Mammei, E. Monaco, A. Mazzanti, and F. Svelto, “A 33.6-to-46.2GHz 32nm CMOS VCO with 177.5dBc/Hz minimum noise FOM using inductor splitting for tuning extension,” in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, Feb 2013, pp. 350–351.
- [128] S. Kang, “Millimeter-wave/sub-terahertz cmos transceivers for high-speed wireless communications,” Ph.D. dissertation, EECS Department, University of California, Berkeley, May 2016. [Online]. Available: <http://www2.eecs.berkeley.edu/Pubs/TechRpts/2016/EECS-2016-19.html>