Architectures, Antennas and Circuits for Millimeter-wave Wireless Full-Duplex Applications

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ABSTRACT

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Demand for wireless network capacity keeps growing exponentially every year, as a result a 1000-fold increase in data traffic is projected over the next 10 years in the context of 5G wireless networks. Smaller cells at RF frequencies (1-6 GHz) are unlikely to deliver the demanded capacity increase. On the other hand, millimeter-wave spectrum (frequencies over 24 GHz) offers wider, multi-GHz channel bandwidths, and therefore has gained significant research interest as one of the most promising solutions to address the data traffic demands of 5G.

Another disruptive technology is full-duplex which breaks a century-old assumption in wireless communication, by simultaneous transmission and reception on the same frequency channel. In doing so, full-duplex offers many benefits for wireless networks, including an immediate spectral efficiency improvement in the physical layer. Although FD promises great benefits, self-interference from the transmitter to its own receiver poses a fundamental challenge. The self-interference can be more than a billion times stronger than the desired signal and must be suppressed below the receiver noise floor.

This dissertation presents novel architectures, antenna and circuit techniques to merge two exciting technologies, mm-wave and full-duplex, which can potentially offer the dual benefits of wide bandwidths and improved spectral efficiency. To this end, two different antenna interfaces, namely a wideband reconfigurable T/R antenna pair with polarization-based antenna cancellation and an mm-wave fully-integrated magnetic-free non-reciprocal circulator, are presented.The polarization-based antenna cancellation is employed in conjunction with the RF and digital cancellation to design a 60GHz full-duplex 45nm SOI CMOS transceiver with nearly 80dB self-interference suppression. The concepts and prototypes presented in this dissertation have also profound implications for emerging applications such as vehicular radars, 5G small-cell base-stations and virtual reality.

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Chapter 1

Introduction

1.1 Millimeter-wave Full-Duplex Overview

In recent years, demand for wireless capacity has exploded as a result of use of bandwidth (BW) hungry media applications in smart-phones, tablets and personal computers. As a result, the demand for wireless network capacity keeps doubling every year and a 1000-fold increase in data traffic is projected over the next 10 years [2]. Solutions for delivering the 1000-fold increase in capacity fall into three main categories: deploying smaller cells (especially in urban settings where the data demand is higher), allocating more spectrum and improving spectral efficiency [3]. Smaller cells at low carrier frequencies (1-6GHz) are unlikely to deliver the demanded total capacity increase due to interference and spectrum limitations at these frequencies [4]. On the other hand, millimeter-wave (mm-wave) frequencies (over 24GHz) allow integration of interference mitigation techniques (e.g. phased arrays) in a smaller form-factor and offer wider, multi-GHz channel bandwidths. Therefore, millimeter-wave beam-forming has recently gained significant research interest as one of the most promising solutions to address the data traffic demands in 5G era [5–8].

Millimeter-wave circuits and systems have been traditionally implemented in expensive III-V compound semiconductor technologies. The rapid maturation of silicon technologies has enabled the exploration of silicon-based millimeter-wave circuits and systems for short-range 60GHz WPANs [9–16], now standardized as WiGig or IEEE 802.11ad. Silicon-based millimeter-wave technology has also been adopted in the design of automotive radars in the recent years [17,18]. It is likely to become even more prevalent in the future as we speak of next-generation (5G) cellular communication,

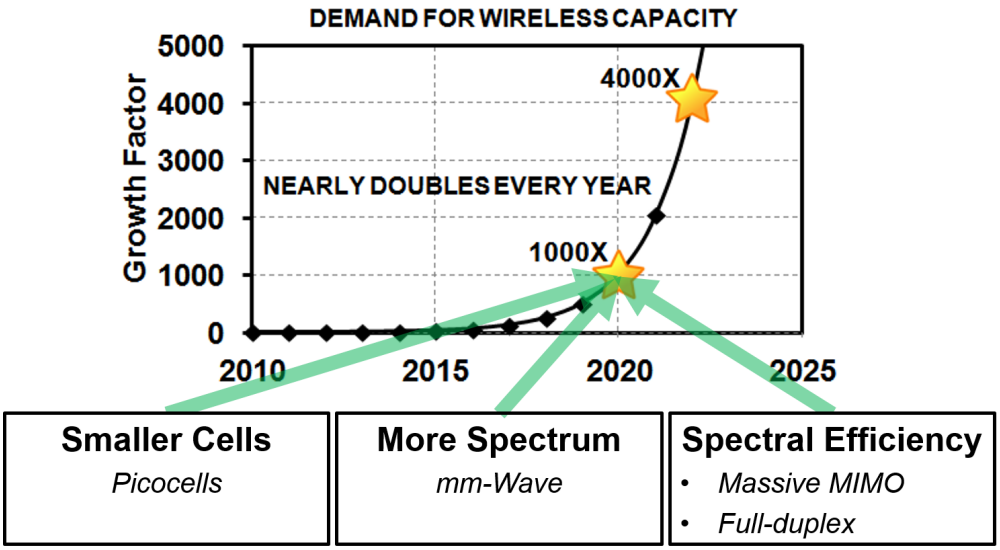

Figure 1.1: Demand for wireless capacity. A 1000-fold increase in data traffic is projected over the next 10 years.

internet of things, virtual reality (VR) and connected cars.

Another emergent technology in the recent years is same-channel full-duplex (or in-band full-duplex), which will be referred to as just full-duplex (FD) in the rest of this chapter. FD can theoretically double the spectral efficiency over time division duplex (TDD) or frequency division duplex (FDD) in the physical layer through simultaneous transmission and reception on the same frequency channel (Fig. **??**).[1] In addition to capacity gain over half-duplex, FD paves the way for revolutionizing wireless protocol design by eliminating the half-duplex constraint and thus can offer many new benefits in wireless networks, including significant increase in access-layer throughput, collision avoidance and addressing the hidden node problem [21]. Although FD promises great benefits for communication systems, self-interference (SI) from the transmitter to its own receiver poses a fundamental challenge. Depending on the application, the SI can be more than a billion times stronger than the desired signal and must be suppressed below the receiver noise floor to enable full-duplex operation. In other words, a total SI suppression of 90 dB or more must be

[1] Interference between cells and asymmetric uplink and downlink traffic are factors that must be considered when evaluating the capacity gain achieved through FD [19]. Research is ongoing to design resource allocation algorithms that maximize capacity gains under these contraints [20].

achieved across multiple domains- antenna [22–27], RF/analog [28–33] and digital [34, 35].

System-level demonstrations leveraging off-the-shelf components (e.g. [34]) have established the feasibility of full-duplex, however research efforts on fully-integrated full-duplex transceivers, especially at mm-wave frequencies, are still in their infancy. Recently, CMOS ICs for full-duplex applications have been demonstrated at low RF frequencies with analog SI cancellers using baseband noise-cancelling, duplexing LNAs in [31] and frequency flat amplitude/phase control in [30] but exhibit either limited SI power handling [31] or limited cancellation bandwidth [30]. In [28, 32, 33], CMOS ICs achieving wideband SIC have been demonstrated, but they are not amenable to mm-wave integration.

The goal of this dissertation is to present novel architectures, antenna and circuit techniques to merge two exciting technologies, mm-wave and full-duplex, which can potentially offer the dual benefits of wide BWs and improved spectral efficiency to address the future data traffic demands. Millimeter-wave full-duplex can be used in several potential applications, ranging from mm-wave backhaul, vehicular radars to virtual reality. The following section discusses these applications in more detail.

1.2 Millimeter-wave Full-Duplex Applications

1.2.1 Millimeter-wave FD Backhaul

Backhaul is one of the least addressed bottlenecks of future 5G wireless communication. Rapid growth of mobile data traffic in 5G wireless communication networks will bring great capacity pressure on the backhaul. Therefore, connecting 5G base stations to other 5G base stations and the network through low-latency, cost-effective backhauling mechanisms with fiber-like throughput is essential [36]. E-band microwave backhaul has been explored in the recent years as a cost-effective method to deliver Gbps throughput. However, it uses two different bands for simultaneous uplink and downlink (effectively FDD between 71-76GHz and 81-86GHz through the use of waveguide diplexers). In the recent past, there has also been interest in phased-array-based backhaul in the unlicensed 60GHz band over shorter distances between densely deployed base stations (Fig. 1.2(a)) [37]. Simultaneous uplink and downlink is necessary to reduce latency, and FD would enable such operation using a single frequency band.

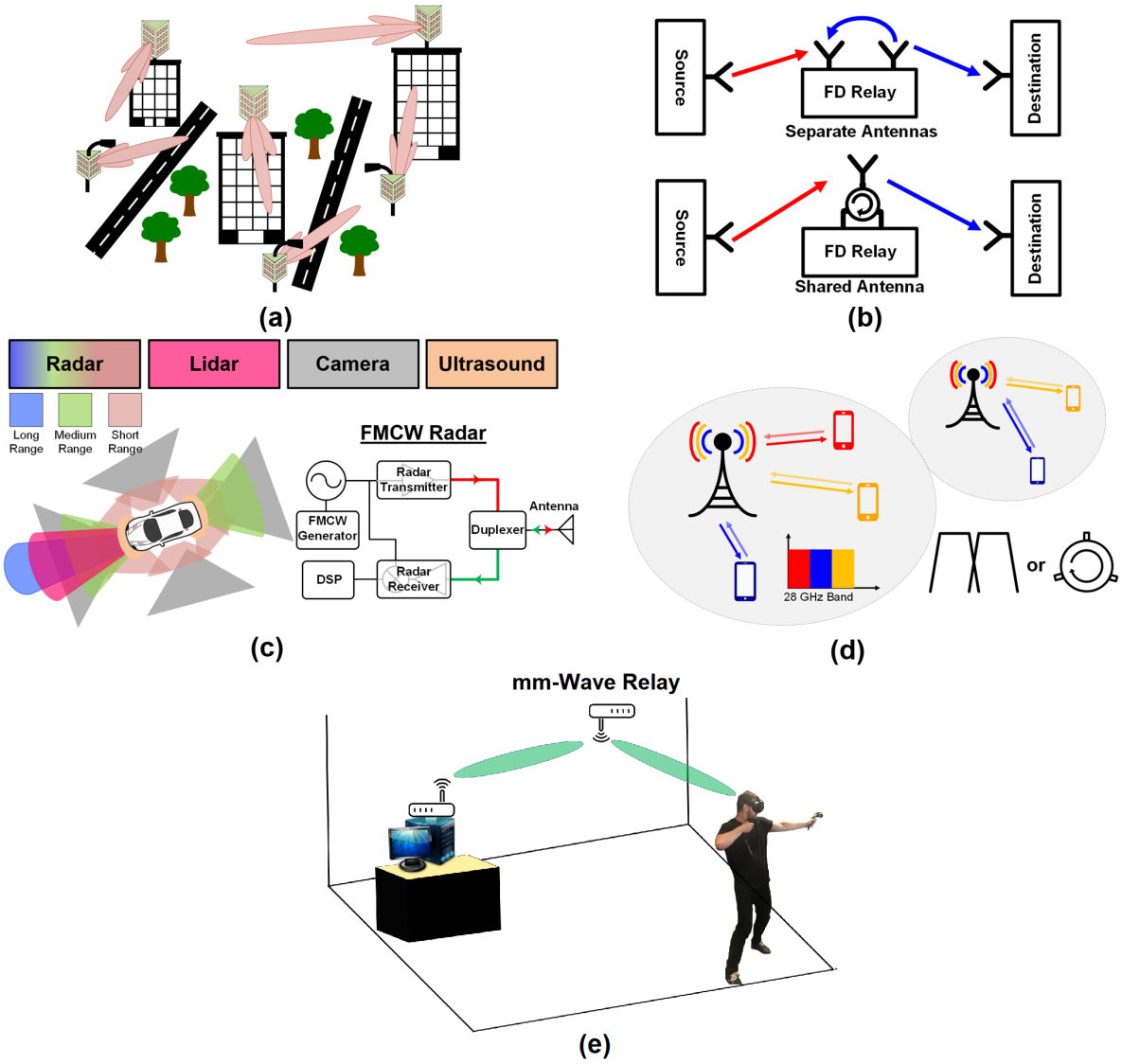

Figure 1.2: (a) A 60GHz phased-array-based FD backhaul mesh network can support up and down links simultaneously on the same channel, improving spectral efficiency and reducing latency. (b) Millimeter-wave FD relaying with separate TX and RX antennas or shared antenna with a millimeter-wave circulator. (c) FMCW vehicular radars can benefit from SI suppression techniques developed for millimeter-wave FD (e.g. a low loss, noise and high isolation duplexer) . (d) Millimeter-wave small-cell 5G Base-Stations with a circulator, eliminating the need for high-quality millimeter-wave diplexers. (e) mm-wave FD can extend the range of cordless wireless VR headsets.

1.2.2 Millimeter-wave FD Relaying

Propagation loss is one of the main disadvantages of millimeter-wave wireless communication. Due to high propagation and absorption losses at high frequencies, the wireless link range is limited. To extend the link range as well as improve link margin, it would be useful to use relay nodes between sources and destinations [38]. However, traditional relay nodes are half-duplex (HD) and therefore have poor spectral efficiency or introduce unwanted latency in the network depending on whether FDD or TDD is used. Millimeter-wave FD relay nodes (depicted in Fig. 1.2(b)) can be employed to extend the millimeter-wave link range, with significant spectral efficiency or latency improvement over existing HD relays [38]. FD millimeter-wave relays can employ either separate antennas for TX and RX or a single antenna (Fig. 1.2(b)). For the latter, a millimeter-wave circulator is required.

1.2.3 FMCW vehicular radar

One remaining problem in FMCW automotive radars is the TX-to-RX SI which is usually referred to as spillover. Spillover can result from on-chip coupling, limited isolation between the antennas or in the circulator, and from first reflections arising from very close targets such as the vehicle's fascia or bumper. The spillover power at the RX input can be much higher than the power reflected by targets that the radar aims to detect [39]. SI suppression techniques developed for millimeter-wave FD can also be adopted in automotive radars to solve the spillover problem. Additionally, another open problem in automotive radars is the design of fully-integrated low-loss circulators with high isolation to replace passive quasi-circulators (such as hybrids which have a theoretical loss of 3dB, typically 4dB) used at the shared-antenna interface.

1.2.4 Millimeter-wave Small-cell 5G Base-Stations

Millimeter-wave small-cell 5G base-stations are envisioned to increase coverage in dense areas and will need to communicate with multiple users simultaneously in uplink and downlink. Although the multiple users will occupy adjacent channels in the same band, the techniques developed in the context of FD will be important. For example, a fully-integrated low-loss, high isolation circulator with high power handling capability could be used to share a single antenna between TX and RX while eliminating the need for high-quality millimeter-wave diplexers.

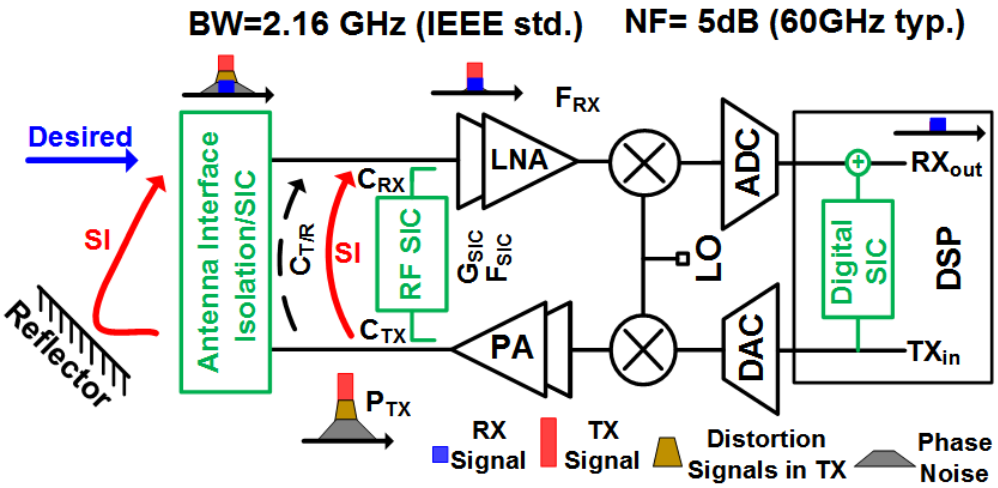

Figure 1.3: Self-interference issues in same-channel full-duplex radios. Self-interference suppression in the antenna, RF/analog and digital domains is required to prevent receiver sensitivity degradation.

1.2.5 Millimeter-wave FD wireless links for VR Headsets

Head-mounted displays create a virtual reality experience by projecting high quality video (e.g. 2160 x 1200 resolution) to each eye at a high frame rate (e.g. 90Hz) [40]. The video streams require very high data rate (approaching 20Gbps for emerging VR headsets) and need to be delivered with very low latency (less than 5ms) to prevent an adverse user experience (e.g. VR sickness) [41]. For a smooth VR experience, a huge amount of data has to be sent back and forth between the computer, the headset and the positional tracker, requiring bi-directional communication to close the feedback loop [40]. Millimeter-wave full-duplex wireless links have the potential of delivering high speed data with low latency and therefore can be a promising solution to cut the cord of VR headsets. Additionally, a millimeter-wave full-duplex relay can be used to extend the range of wireless VR headsets, improving the user's mobilility [42].

1.3 Full-duplex Challenge and System Considerations

In this section, by default, equations will be written in the linear scale unless otherwise stated. Some variables such as coupling coefficients and noise factors will be naturally assumed to be in the linear scale, while others such as power levels, noise floor and dynamic range will be naturally

assumed to be in the dB scale.

Fig. 1.3 depicts the self-interference challenge in a typical full-duplex wireless node. SI arises from the inherent coupling in typical antenna interfaces as well as environmental reflections and consists of a leakage of the main transmitted signal, the transmitter's nonlinear distortions as well as the TX-side LO phase noise. As stated in the previous section, SI should be suppressed sufficiently below the receiver noise floor (P_n) to enable reception of the weak desired signal. Therefore, a total SI suppression of P_{TX}-P_n + 6 dB must be achieved in antenna, RF/analog and digital domains, assuming a 6 dB margin for SI suppression below the noise floor. Here, P_{TX} is the transmitter output power. For example, a 60GHz FD transceiver with a typical transmit power of +14dBm, receiver noise figure of 5dB and channel BW of 2.16GHz would require +14dBm-(-174 dBm/Hz+10log(2.16GHz)+5)+6=96dB of self-interference cancellation (SIC), assuming a 6dB margin. Such a high level of SI suppression can only be achieved by enhancing the transmit-receive (T/R) isolation at the antenna [22–24, 43, 44] as well as performing self-interference cancellation (SIC) in the antenna [25–27, 45], RF/analog [28–31, 46] and digital domains [34].

If an ADC with ENOB=8 bits (effective number of bits) and an effective dynamic range of 6.02×(ENOB-2)=36 dB is used, then the remaining 60 dB SI suppression must be achieved by the antenna interface and the RF canceller in Fig. 1.3. The degradation of the receiver noise figure due to the RF canceller's noise should be taken into account while partitioning this 60 dB between the antenna and RF domain cancellers. If G_{SIC} and C_{RX} are the gain of the RF SI canceller and the coupling coefficient of the coupler at the receiver input, respectively, and assuming C_{RX} is weak, the noise factor of the full-duplex transceiver (F_{tot}) shown in Fig. 1.3 can be calculated as

$$F_{tot} = F_{RX} + (F_{SIC} - 1)\, G_{SIC} C_{RX} \tag{1.1}$$

where F_{SIC} is the noise factor of the RF SI canceller. The last term in (1.1) represents the amount of RX NF degradation due to the RF SI canceller. The magnitude of the transfer function through the antenna interface, $C_{T/R}(1 - C_{TX})$, and the RF canceller, $C_{TX} G_{SIC} C_{RX}$, must be equal for perfect RF SI cancellation. This simplifies (1.1) as

$$F_{tot} = F_{RX} + (F_{SIC} - 1) \left(\frac{C_{T/R}(1 - C_{TX})}{C_{TX}} \right) \tag{1.2}$$

From (1.2) we conclude that a lower $C_{T/R}$ reduces the noise figure degradation due to the RF

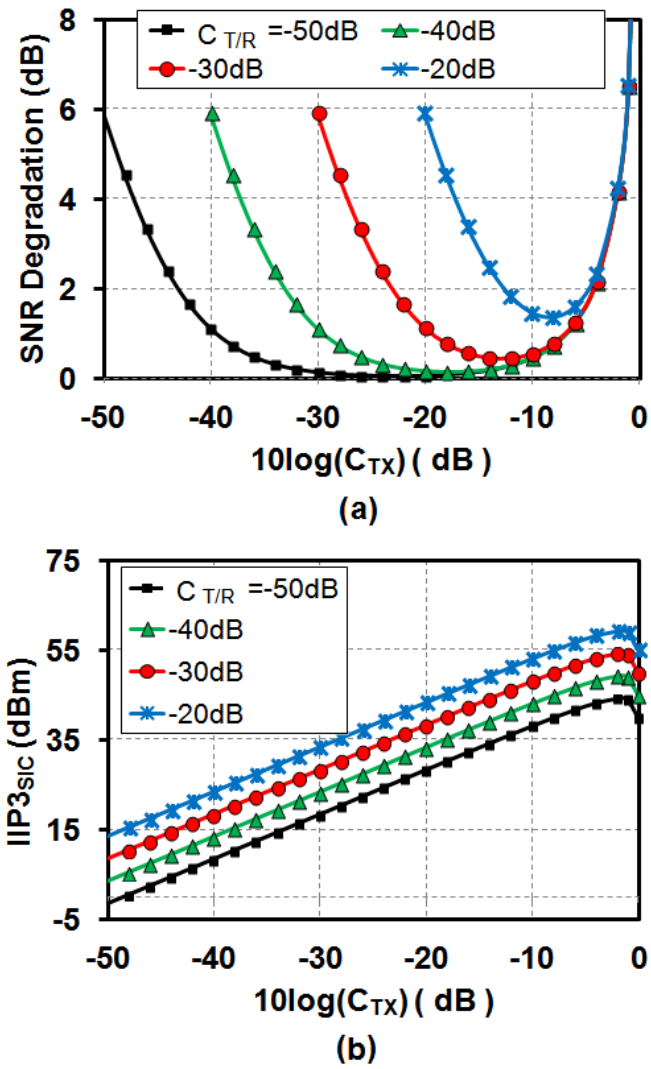

Figure 1.4: (a) SNR degradation versus the transmit side coupling coefficient assuming 10log(F_{RX})=5 dB and 10log(F_{SIC})=10 dB. SNR degradation becomes negligible for 40 dB T/R isolation at the antenna interface. (b) Required IIP3 for the RF SI canceller versus the C_{TX}. $IIP3_{SIC}$ is 18 dBm for $C_{T/R}$=-50 dB and C_{TX}=-30 dB.

canceller as it allows a lower C_{RX} in (1.1), *motivating the need for SIC in the antenna domain.* Additionally, (1.2) reveals a trade-off between the receiver NF and the transmitter efficiency degradations due to the RF SI canceller as a lower C_{TX} increases the receiver NF degradation but reduces the transmitter efficiency degradation. *It should be noted that this trade-off is also eased through higher antenna interface isolation or antenna-domain SIC.* For a fixed PA output power, SNR degradation in a full-duplex link, ΔSNR, compared to its half-duplex counterpart can be written (in dB scale) as

$$\Delta SNR = 10\log F_{tot} - 10\log F_{RX} - 10\log(1 - C_{TX}) \tag{1.3}$$

Assuming a noise figure of 10 dB for the RF canceller (F_{SIC}=10), ΔSNR versus 10log(C_{TX}) is plotted in Fig. 1.4(a) for different T/R isolation levels at the antenna interface. To keep the SNR degradation negligibly small, more than 40 dB isolation must be achieved in the antenna interface. Note that for a low C_{TX} (e.g. smaller than -20 dB for 10log($C_{T/R}$)<-40 dB), the TX efficiency degradation, namely the last term in (1.3), is extremely small so that ΔSNR is governed by the receiver noise figure degradation. On the other hand, as C_{TX} becomes larger, ΔSNR increases due to the TX efficiency degradation as more power is stolen away by the RF canceller, reducing the transmitter power going into the antenna interface.

Higher SI suppression in the antenna interface also relaxes the linearity requirement on the receiver and the RF canceller, leading to lower power consumption. Achieving low $C_{T/R}$ also opens up the possibility of performing RF SIC after some low-noise amplification as will be presented in Chapter 3, further reducing the NF degradation due to the RF canceller. The spurious-free dynamic range requirement of the receiver in dB scale is given by DR_f=P_{TX}+10log $C_{T/R}(1 - C_{TX})$-SIC_{RF}-P_n and reduces with decreasing $C_{T/R}$. Lower $C_{T/R}$ also implies that more loss can be tolerated in the RF canceller and allows designing an all passive RF canceller with higher linearity so that the third-order distortion products generated by the RF canceller (not shown in Fig. 1.3) fall below P_n. The IIP3 requirement on the RF SI canceller in Fig. 1.3 can be expressed as

$$IIP3_{SIC} = \frac{3P_{TX} - P_n + 10\log C_{T/R}(1 - C_{TX}) + 20\log C_{TX}}{2} \tag{1.4}$$

Equation (1.4) is plotted versus C_{TX} for different $C_{T/R}$ levels in Fig. 1.4(b). The RF canceller must have an $IIP3_{SIC}$ higher than +45 dBm for 10log($C_{T/R}$)=-30 dB and 10log(C_{TX})=-10 dB

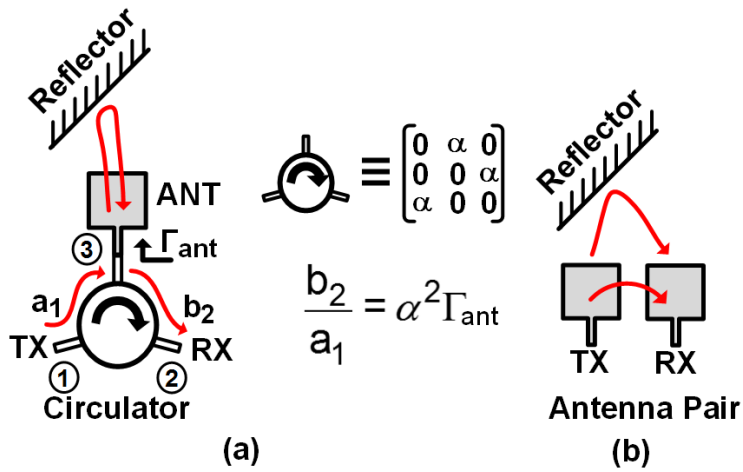

Figure 1.5: Two different antenna interfaces for full-duplex operation: (a) a shared-antenna interface such as a circulator can be used to share a single antenna between the transmitter and receiver, and (b) in a T/R antenna pair, transmitter and receiver employ dedicated antennas.

whereas an $IIP3_{SIC}$ of +18 dBm is required for 10log($C_{T/R}$)=-50 dB and 10log(C_{TX})=-30 dB. The later is more manageable, motivating the need for an isolation higher than 50 dB in the antenna interface. Alternatively, if the RF canceller is not linear enough, the distortion products can be estimated and cancelled in the digital canceller [34]. However, this may be power inefficient depending on the required computational complexity, especially at mm-wave systems.

Fig. 1.5 depicts the two main ways of implementing the antenna interface. One option is to employ a shared antenna interface such as a circulator to share the same antenna for transmit and receive. *The main challenge with a circulator is the finite reflection coefficient of the antenna.* The transmit signal reflects back to the receiver input due to imperfect matching at the antenna port. For the circulator shown in Fig. 1.5(a), assuming perfect isolation between port 2 and port 1 to start with, the T/R isolation can be expressed in dB scale as

$$|\frac{b_2}{a_1}| = 20\log|\Gamma_{ant}| + 40\log\alpha \tag{1.5}$$

where Γ_{ant} and α are the reflection coefficient of the antenna and the circulator insertion loss, respectively. According to (1.5), the T/R isolation, in terms of magnitude and bandwidth, strongly depends on the matching at the antenna port. In reality, this limitation is common to all antenna interfaces which share a single antenna port for transmit and receive. The second antenna interface

in Fig. 1.5(b) uses separate antennas for transmit and receive. The T/R isolation of an interface with separate antennas is not significantly impacted by the imperfect matching at the ports.

A common limitation for both interfaces are the reflections from nearby objects. A nearby reflector creates another interference path from the transmitter to the receiver for both cases. A near-field reflector would change the antenna impedance as well. Changing antenna impedance may exacerbate the SI reflection at the circulator ANT port. The effect of the environment on the T/R isolation is not predictable during the design process and varies in the field. In order to combat the scattering from environment, the SI suppression technique within the antenna interface must be reconfigurable.

1.4 Thesis Overview

This thesis presents novel full-duplex antenna-circuit interfaces to enable full-duplex operation at mm-wave frequencies in advanced CMOS processes. These novel antenna interfaces are realized by blending various concepts from antenna, RF, analog and digital domains (co-integrating EM, analog and digital). This dissertation is organized as follows:

Chapter 2 presents a novel wideband reconfigurable polarization-based SIC technique in the antenna domain for FD applications. This chapter presents a detailed analysis of this technique and provides a foundation for the next chapter. This technique employs collocated T/R antennas with orthogonal polarizations. An auxiliary port which is co-polarized with the transmit port is introduced on the receive antenna and terminated with a reconfigurable reflective termination. The reflective termination reflects the coupled signal at the auxiliary port to cancel the self interference at the receiver input. A higher order reconfigurable reflective termination enables wideband SIC. A prototype employing this technique is built and achieves more than 50 dB self-interference suppression over 300 MHz centered at 4.6 GHz. This is at least 4× better fractional SIC bandwidth at 10dB higher isolation compared to the other reconfigurable antenna cancellation works. The SIC can be reconfigured as the environment changes to recover the degradation in the SI suppression due to scattering from nearby objects. The polarization-based antenna cancellation technique is verified at 4.6GHz in this chapter, but it can be readily scaled up in frequency. A 60GHz FD transceiver employing the same technique will be presented in the next chapter.

Chapter 3 presents a fully-integrated 60 GHz direct-conversion transceiver in 45 nm SOI CMOS for same-channel full-duplex wireless communication. Full-duplex operation is enabled by the polarization-based wideband reconfigurable SIC technique presented in Chapter 2. The antenna cancellation can be reconfigured from the IC to combat the variable self-interference (SI) scattering from the environment during in-field operation. A second RF cancellation path with >30 dB gain control and >360° phase control further suppresses the residual SI to achieve the high levels of required SIC. With antenna and RF cancellation together, a total SI suppression of >70 dB is achieved over a cancellation bandwidth of 1 GHz and can be maintained in the presence of nearby reflectors. In conjunction with digital SIC implemented in MATLAB, a full-duplex link is demonstrated over 0.7 m with a signal-to-interference-noise-and-distortion ratio (SINDR) of 7.2 dB. To the best of our knowledge, this work demonstrates the first fully-integrated mm-wave full-duplex transceiver front-end and link.

Chapter 4 presents a shared-antenna interface, namely a fully-integrated 25 GHz circulator in 45 nm SOI CMOS, demonstrating magnetic-free passive non-reciprocity on silicon at mm-waves for the first time. This chapter presents a detailed analysis of the millimeter-wave circulator in both time and frequency domains. Millimeter-wave non-reciprocal operation is enabled by a novel concept of spatio-temporal conductivity modulation, which achieves broadband non-reciprocal gyrator functionality over a theoretically infinite BW. The 25 GHz circulator achieves minimum TX-to-ANT/ANT-to-RX insertion losses (IL) of 3.3 dB/3.2 dB, respectively, with a 1- dB BW of ∼4.6GHz. TX-to-RX isolation is 18.3-21.2 dB (limited by the measurement setup) over the same BW. The circulator IC occupies an area of 1.2 mm × 1.8mm ($\lambda/8 \times \lambda/6$). The spatio-temporal conductivity modulation concept is readily scalable across frequency and can be an enabler for higher-millimeter-wave (e.g. 77 GHz) circulators as well as optical isolators.

Chapter 5 concludes the dissertation with a summary of the key technical contributions and suggestion for future research directions.

Chapter 2

Polarization-Based Antenna Cancellation

As discussed in Chapter 1, SI suppression at the antenna is crucial for full-duplex operation. It relaxes the dynamic range requirements on the RF, analog and digital blocks in the receiver chain as well as the RF/analog and digital SIC circuits. Based on these system level discussions in Chapter 1, the specifications for a typical FD antenna interface can be summarized as:

- support wide SI suppression BWs for emerging wireless standards,
- provide more than 50 dB SI suppression to relax the receiver NF degradation as well as the receiver and RF SIC linearity requirements,
- maintain the SI suppression as the environment changes,
- present minimum degradation in the full-duplex link SNR by preserving the T/R antenna patterns while improving the SI suppression.

This chapter first reviews the previously reported SI suppression techniques in the antenna domain and then presents a novel reconfigurable polarization-based wideband antenna cancellation technique for full-duplex applications [27]. As a proofs-of-concept a 5GHz T/R antenna pair with polarization-based antenna cancellation is implemented on PCB and verified with measurements. It achieves 50 dB SI suppression over 300 MHz at 4.6 GHz (*4× better fractional SIC bandwidth at*

10 dB higher isolation compared to the other reconfigurable antenna cancellation works). It is reconfigurable and 50 dB SI suppression can be maintained in the presence of nearby reflectors. The proposed concept can easily be scaled up in frequency and can even be implemented on silicon at millimeter-wave frequencies.

This chapter builds a foundation for the 60GHz full-duplex SOI CMOS transceiver enabled by the polarization-based antenna cancellation technique in Chapter 3 by providing a step-by-step design methodology, an in-depth analysis of the SIC's effect on antenna patterns, demonstrating scalability of the technique in frequency, proposing a method for on-chip integration at mm-wave frequencies.

2.1 A Review of SI Suppression Techniques in the Antenna Domain

The SI suppression techniques in the antenna domain published in the literature can be divided into two main categories. The techniques in the first category target increasing the T/R isolation by minimizing the inherent mutual coupling between transmit and receive antennas or ports. In [22], the authors rely on the physical separation between the T/R antennas and directionality for SI suppression. This approach is area inefficient and therefore not a feasible option for small form factor radios. Other techniques in this category include exploiting cross-polarization [23,44] and shadowing the near fields of T/R antennas [24]. Although these techniques promise good isolation over wide bandwidths, they are not reconfigurable and are unable to combat environmental reflections which are unknown in the design process and vary over time.

The techniques in the second category, which will be called *antenna cancellation*, are essentially based on performing self-interference cancellation in the antenna domain. This requires either introducing an auxiliary antenna or an auxiliary coupling path between the transmit and receive antennas/ports to create an inverse replica of the main coupling signal. [47] proposes a two transmit and a single receive antenna system in which the TX antennas are placed so that the RX antenna's distance from them differs by $\lambda/2$ at the operating frequency. Similarly, in [48], the RX antenna is placed in between the TX antennas which are fed 180° out of phase to cause destructive interference at the RX antenna. This out of phase feeding technique is extended to create a wideband STAR

multi-element array consisting of four transmitting elements and a centrally-located receiving antenna in [49] and an 8-element circular TX array and a centrally-located RX element in [50,51]. All these antenna cancellation techniques rely on perfect distance and phase alignment, making them vulnerable to manufacturing and antenna excitation tolerances. The addition of a beamformer to control the excitations, as in [49, 50], can be used to combat the manufacturing and excitation errors at the expense of increased complexity and form-factor. Additionally, these approaches usually create an undesirable far-field beamforming effect since a simultaneous optimization of the far-field radiation and the antenna cancellation performance is not undertaken. Finally, it is unclear if these techniques can combat reflections that arise from a changing electromagnetic environment.

A few tunable antenna cancellation techniques which have the potential to combat variable scattering from the environment have been proposed in the literature. In [25], the authors propose placing tunable resonant baffles between antenna elements. This technique provides 40 dB isolation over 12 MHz at 3.3 GHz. Using two sets of tunable resonators between antenna elements in [26], the bandwidth of cancellation was improved but was still limited to 55 MHz for 40 dB isolation at 3.3 GHz. Although these techniques potentially combat environmental reflections, neither of them have experimentally demonstrated SIC under environmental changes.

2.2 Proposed Polarization-Based Antenna Cancellation Technique

2.2.1 Overview

Fig. 2.1 depicts the proposed SI cancellation technique in the antenna domain. It consists of a compact collocated T/R antenna pair to ensure small form factor. In the RF/analog domains, a continuous-wave signal is characterized by its frequency, amplitude and phase. *As the RF signal is converted into an electromagnetic (EM) wave in the antenna domain, polarization becomes another degree of freedom which can be exploited (Fig. 2.1(a)).* In this work, cross-polarized transmit and receive antennas are employed to enhance the initial TX-to-RX isolation. Fig. 2.2(a) shows rectangular slot-loop T/R antenna pairs with co-polarized and cross-polarized TX and RX antennas tuned at 4.6 GHz. Using cross-polarized antennas improves the TX-to-RX isolation by 5-22 dB from 4.2 GHz to 5 GHz compared to the co-polarized case (Fig. 2.2(b)).

To increase the SI suppression further, an auxiliary port co-polarized with the TX antenna

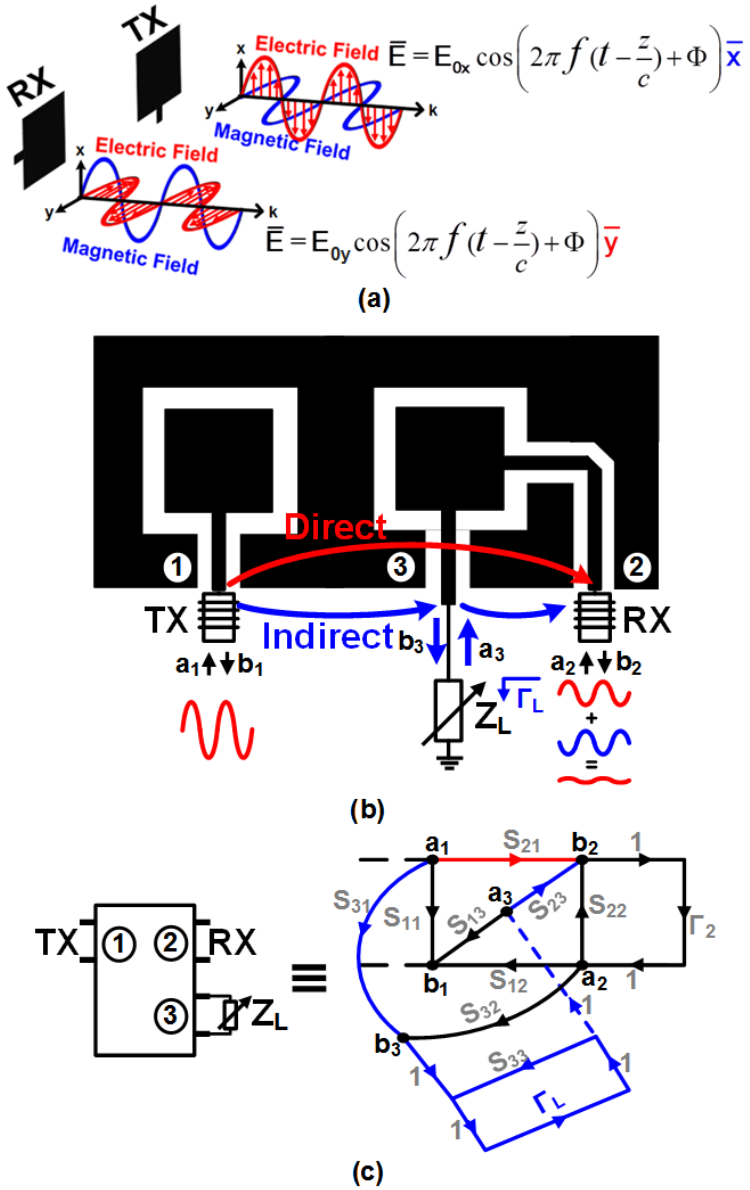

Figure 2.1: (a) Polarization is another degree of freedom in the wave propagation domain. Depicted here are the ideal radiated fields for a conceptual cross-polarized T/R antenna pair. (b) Diagram of the proposed antenna cancellation technique. It employs T/R antenna pairs with orthogonal polarizations. An auxiliary port co-polarized with TX antenna is introduced on the RX antenna and terminated with a variable reflective termination to achieve wideband SIC. (c) Self-interference signal flow graph.

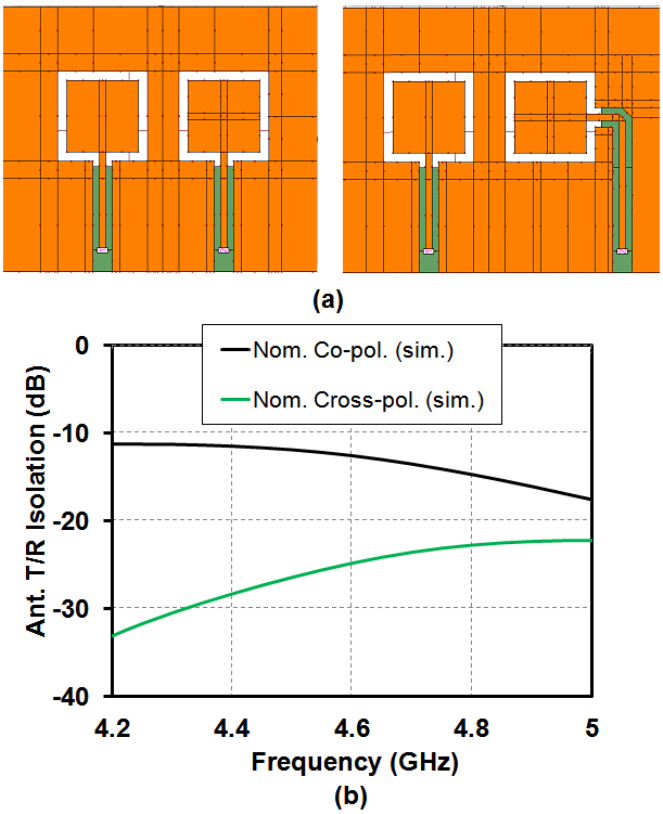

Figure 2.2: (a) Structure of the co-polarized and cross-polarized slot-loop T/R antenna pair (image taken from a layout in IE3D, a Method-of-Moments-based EM simulator [1] (b) Comparison of the simulated co-polarized and cross-polarized T/R isolation.

is introduced at the RX antenna and terminated with a reconfigurable reflective termination. As depicted in Fig. 2.1(a), introduction of the auxiliary port creates an indirect coupling path between the TX and RX ports. In the indirect path, the TX signal first couples to the auxiliary port, reflects from the variable termination and then couples into the receive port to cancel the SI from the direct path. Treating the T/R antenna pair as a microwave network, the signal flow chart is drawn in Fig. 2.1(c). From the flow chart, the total SI leakage from the transmit to the receive port can be quickly written as

$$b_2 = \left(S_{21} + \frac{S_{23} S_{31} \Gamma_L}{1 - S_{33} \Gamma_L} \right) a_1, \tag{2.1}$$

where a_1 is the incident power wave at the TX port and b_2 is the outgoing power wave at the

RX port, S_{21}, S_{31}, S_{23} and S_{33} are the S-parameters of the 3-port antenna core (ports 1, 2 and 3 are TX, RX and auxiliary ports, respectively), and Γ_L is the reflection coefficient of the variable termination at the auxiliary port. The first and second terms inside the bracket in (2.1) correspond to the transfer functions of the direct and indirect paths, respectively. When these two coupling terms are equal in magnitude and 180° out of phase, perfect SI cancellation, b_2=0, can be achieved. It should be noted that all the parameters in (2.1) are frequency dependent and the SIC bandwidth depends on how well the equal magnitude and 180° out of phase conditions are preserved across frequency.

In previously reported antenna cancellation techniques, the indirect path mimics the magnitude and the phase (with 180° difference) of the direct path at a single frequency [25, 52] or at slightly shifted frequencies [26]. In general, a cancellation path with $2N$ degrees of freedom can be used to achieve perfect SIC at N different frequencies resulting in wideband cancellation. In fact, the $2N$ degrees of freedom can be utilized in multiple ways. The magnitude and phase of the direct path can be synthesized at N separated frequencies or we can synthesize the magnitude, phase as well as their slopes at $N/2$ frequencies. *The proposed technique is based on mimicking the direct path's magnitude and phase as well as their slopes to achieve wide band cancellation.*

2.2.2 Design Methodology

An algorithmic design methodology has been followed to implement the T/R antenna pair with the proposed self-interference cancellation technique.

1) The T/R antenna pair is designed and simulated in an EM solver, in our case Mentor Graphics IE3D [1].

This step includes designing and optimizing the TX rectangular slot loop antenna, and then creating the T/R antenna pair by using an identical 90° rotated antenna for the RX and adding the auxiliary port. The design procedure for slot antennas is well established, and will not be described here. Instead, the reader is directed to [53, 54]. Fig. 2.3 shows the antenna dimensions and the PCB cross-section. Its implementation will be discussed in Section 2.3. Once the T/R antenna core is finalized, all the parameters in (2.1) except Γ_L are fixed.

2) The required reflection coefficient for SIC, $\Gamma_{L,req}$, is calculated across frequency as

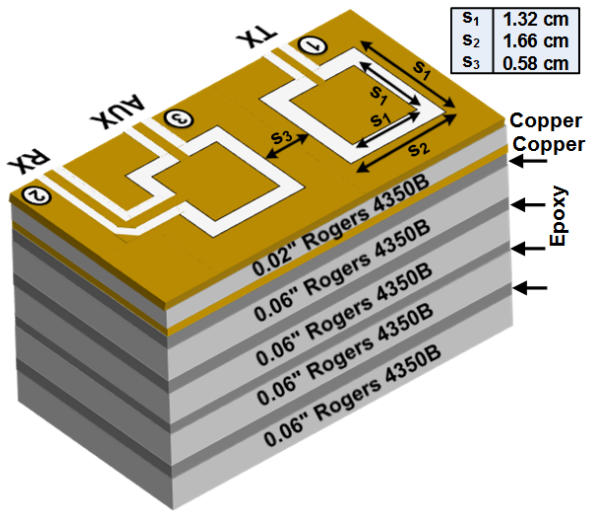

Figure 2.3: PCB cross-section and dimensions of the implemented T/R antenna pair. The radiation is taken from the bottom using a 0.24" Rogers 4350B as superstrate.

$$\Gamma_{L,req} = \frac{S_{21}}{S_{21}S_{33} - S_{23}S_{31}}. \tag{2.2}$$

Conductance and susceptance are physically more meaningful design parameters than the required reflection coefficient since they can be readily expressed in terms of the parameters of the lumped components that would be used to implement the termination. The required conductance and susceptance of the variable termination can be calculated as

$$G_{L,req} = Re\left\{Y_0 \frac{1-\Gamma_{L,req}}{1+\Gamma_{L,req}}\right\}, \tag{2.3}$$

$$B_{L,req} = Imag\left\{Y_0 \frac{1-\Gamma_{L,req}}{1+\Gamma_{L,req}}\right\}, \tag{2.4}$$

where Y_0 is the characteristic admittance. As discussed in the previous step, the $\Gamma_{L,req}$ for SIC is determined by the antenna core. This introduces a trade-off between the required $\Gamma_{L,req}$ and the antenna performance parameters such as gain, bandwidth and efficiency. To break this trade-off, the feed line length, d in Fig. 2.4(a), is used as another parameter to optimize the $\Gamma_{L,req}$ for achieving wideband SIC. Neglecting the transmission line loss, $\Gamma_{L,req}$ will be modified as follows due to the effect of extending the feed line length:

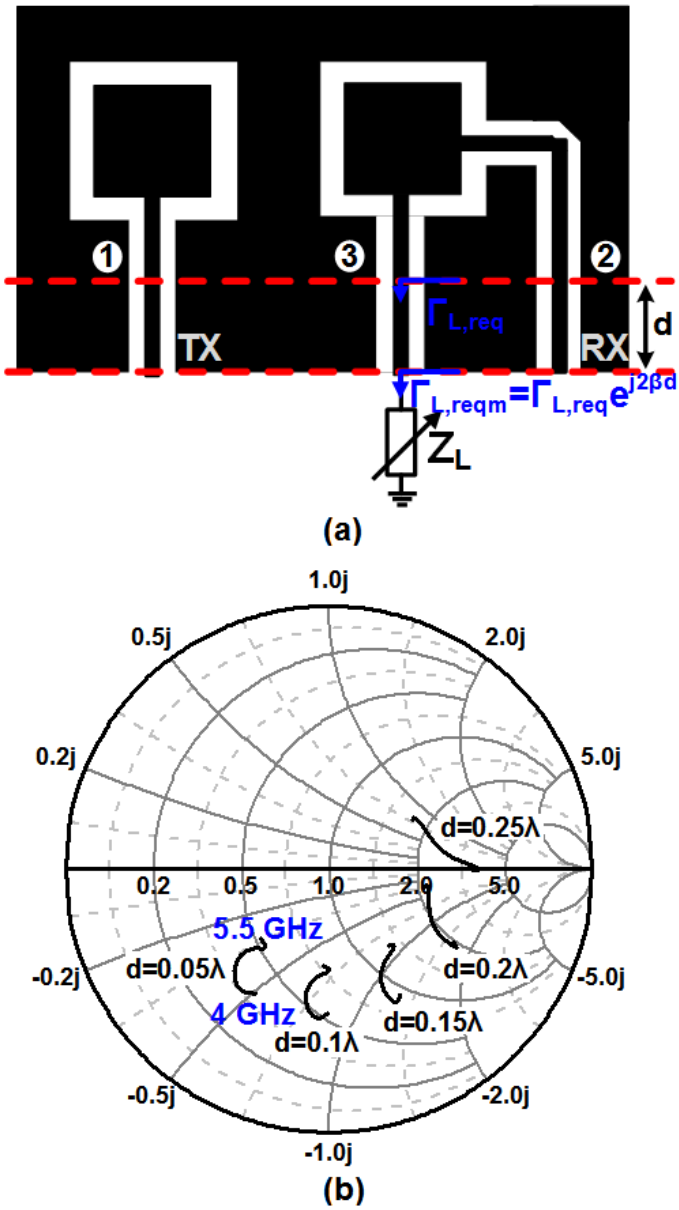

Figure 2.4: (a) The feedlines are used as a parameter to optimize the required reflection coefficient. (b) Transformation of the required admittance by extending the feedline for the T/R antenna pair depicted in Fig. 2.3.

$$\Gamma_{L,reqm}(d) = \frac{S_{21}e^{j2\beta d}}{S_{21}S_{33} - S_{23}S_{31}}, \tag{2.5}$$

where β is the propagation constant for the feedline. The line length is increased in 0.05λ steps and the new required admittance, $Y_{L,reqm}$, is plotted on a Y-Smith chart in Fig. 2.4(b) for the designed T/R antenna pair in Fig. 2.3. The required admittance flattens out and its real part ($G_{L,reqm}$) gets larger with increasing d. We would like to set d so that $Y_{L,reqm}$ falls on a constant conductance circle in the desired frequency band. Thus, the slope of $G_{L,reqm}$ would be zero and could be synthesized automatically by a parallel RLC termination as discussed in the next methodology step. Consequently, the design of the T/R antenna core is simplified to a two step procedure. First, the antenna parameters are optimized for the radiation performance in IE3D. Then, the feed line length is chosen to enforce slope of $G_{L,reqm}$ equal to 0. It should also be noted that $G_{L,reqm}$ increases with d. In this work, d is set to 4 mm, resulting in the simulated required conductance ($G_{L,reqm}$) and susceptance ($B_{L,reqm}$) shown in Fig. 2.5(a) to achieve perfect SIC.

3) Design a higher-order reflective termination to synthesize G_{reqm}, B_{reqm} *and their slopes at multiple frequency points.*

This work uses a parallel RLC termination. A parallel RLC termination with variable L, C and R has 3 degrees of freedom to control the $G_{L,synth}$, $B_{L,synth}$ and the slope of $B_{L,synth}$ at a given frequency, f. The reconfigurability of the L, C and R allow tracking of $G_{L,reqm}$, $B_{L,reqm}$ and the slope of $B_{L,reqm}$ as the environment changes. $B_{L,synth}$, the slope of $B_{L,synth}$ and $G_{L,synth}$ can be expressed as

$$B_{L,synth} = 2\pi f C \left(1 - \frac{{f_r}^2}{f^2}\right), \tag{2.6}$$

$$\frac{\partial B_{L,synth}}{\partial f} = 2C \left(\pi + \frac{{f_r}^2}{f^2}\right), \tag{2.7}$$

$$G_{L,synth} = \frac{1}{R}, \tag{2.8}$$

where f_r is the resonance frequency given by $1/2\pi\sqrt{LC}$. Note that all the parameters in (2.6), (2.7) and (2.8) can be independently set but $\partial G_{L,synth}/\partial f = 0$ in a parallel RLC. Hence the slope

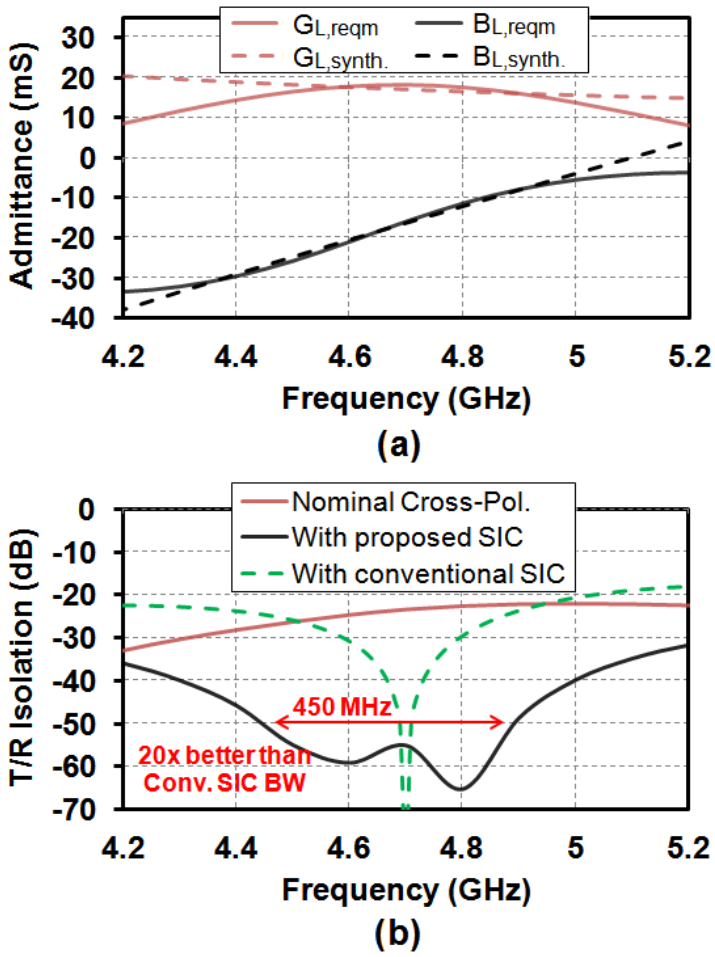

Figure 2.5: Antenna cancellation simulations: (a) required and synthesized admittance, (b) resultant antenna cancellation.

of $G_{L,reqm}$ is optimized to be relatively flat during the T/R antenna core design so that it can be automatically synthesized by a shunt R. Alternatively, the feedline length can be thought as the fourth degree of freedom in the reflective termination to set $\partial G_{L,synth}/\partial f = 0$.

In practice, a variable L is challenging to implement. In this work, L is set to replicate the slope of $B_{L,reqm}$ dictated by the EM simulation of the T/R antenna core without considering nearby reflectors. The measurements in Section 2.4 show that the SIC can be recovered by just changing the R and C values in the presence of a metallic close-in reflector. If strong reflection necessitates controlling the magnitude *and* slope of $B_{L,synth}$ independently, a variable L must be included in the reflective termination. Switches to the ground can be placed at different locations on a shorted

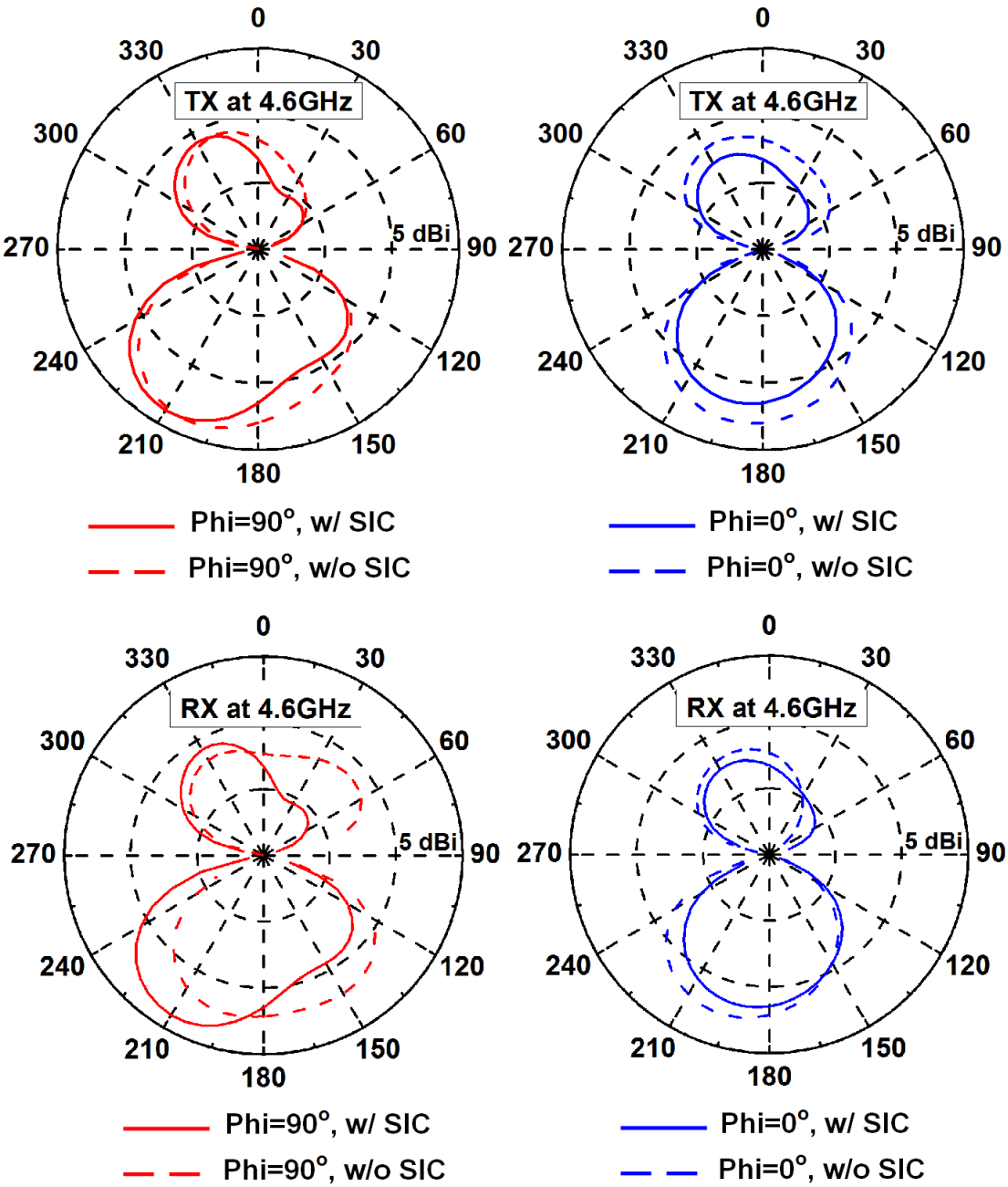

Figure 2.6: TX and RX patterns with and without SIC (simulation).

stub to implement the variable L, but this has not been pursued in this work. Fig. 2.5(a) shows the synthesized $G_{L,synth}$ and $B_{L,synth}$ to achieve wideband cancellation. In this simulation, finite quality factors are used for the L and C (based on implementation aspects, such as EM simulations of the shorted transmission line used to implement the L, varactor quality factor and typical parasitics of the varactor package), causing a slight frequency dependency in $G_{L,synth}$. An SI suppression better than 50 dB over 450 MHz is achieved in simulation in Fig. 2.5(b).

Conventional RF cancellers consist of a TX-side coupler, variable-gain amplifier or attenuator, phase shifter and an RX-side coupler to mimic the transfer function of the antenna interface [30]. Such a conventional canceller with flat amplitude and phase response across frequency theoretically achieves 20 MHz SIC bandwidth at 50 dB SI suppression in simulation (Fig. 2.5(b)). *This work improves the SIC bandwidth by 20× compared to a conventional RF canceller in simulation.* Essentially, our technique can be seen as embedding an SIC path with a tunable resonator and amplitude and phase scaling within the antenna element. The introduction of the auxiliary port on the RX antenna allows us to embed the TX-side and RX-side couplers within the antenna pair. *Thus, the couplers track the inherent TX-to-RX isolation closely across frequency*[1], resulting in wide SIC bandwidth in conjuction with the high-order reflective termination.

2.2.3 Impact of SIC on Antenna Patterns

Fig. 2.6 presents the simulated TX and RX radiation patterns at 4.6 GHz with and without SIC. The effect of SIC on the TX radiation pattern varies along the coupling axis (Φ=90°) with elevation angle θ. The maximum degradation in the TX pattern is 2 dB at around θ=15°. Fig. 2.7(a) depicts the TX pattern degradation mechanism. The signal that couples from the TX to the auxiliary port reflects from the variable termination and then radiates from the RX antenna, eventually interfering with the TX antenna radiation in the far-field. This mechanism can be analyzed using array theory. This structure can be modelled as a 2×1 antenna array with non-uniform amplitude excitations as shown in Fig. 2.7(a). Assuming a TX-to-AUX coupling coefficient of $C_1 e^{\phi_C}$, the excitation currents for the TX and AUX antennas can be expressed as I_1 and $I_1\sqrt{\frac{C_1}{1-C_1}}\Gamma_L e^{j\phi_C}$, respectively, where Γ_L is the reflection coefficient at the AUX port. Assuming I_1=1, the array factor can be calculated as follows:

[1]In other words, the main and auxiliary path transfer functions closely track each other in frequency.

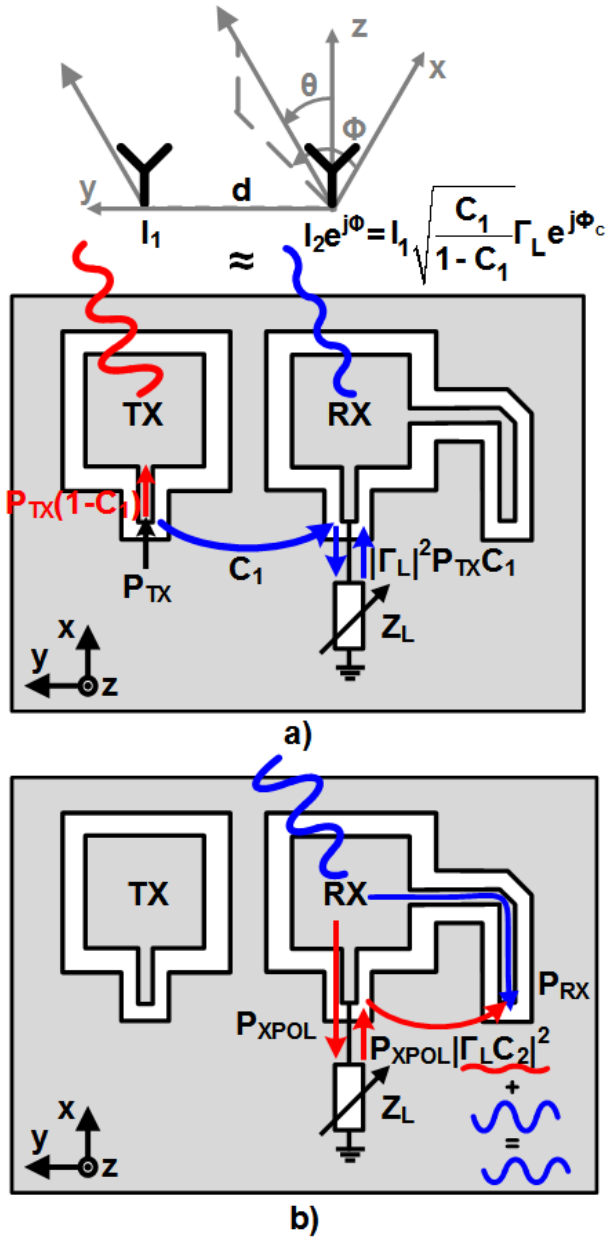

Figure 2.7: (a) TX radiation pattern degradation mechanism. (b) RX radiation pattern degradation mechanism.

$$AF(\theta, \Phi) = 1 + \sqrt{\frac{C_1}{1 - C_1}} \Gamma_L e^{j\phi_C} e^{j\beta d \sin\theta \sin\Phi}, \tag{2.9}$$

where d is the electrical spacing between the antennas. Using the simulated 10log(C_1)=-13.5 dB, Γ_L=0.486∠113°, ϕ_C=105° and d=0.34λ at 4.6 GHz, 20log(AF(θ, Φ=90°)) and 20log(AF(θ, Φ=0°)) are plotted in Fig. 2.8. As can be seen, their profiles follow the IE3D simulations considerably well across θ, verifying our analysis. The difference in the peak and null magnitudes for Φ=90° can be attributed to our assumption of identical antennas. In reality, the AUX antenna gain differs from its TX counterpart due to the presence of the RX port and therefore the second term in (2.9) should be corrected for the direction-dependent antenna gain difference. The TX pattern degradation in the $\Phi = 0°$ cross-section is relatively constant due to the symmetry. The penalty on the TX antenna gain can be reduced by increasing the TX-to-AUX isolation by increasing the separation between the antennas. It should also be noted that the indirect radiation can also be exploited by optimizing the required Γ_L to create constructive interference to increase the TX antenna gain in a specific direction and thus the full-duplex link SNR.

Fig. 2.7(b) presents the RX pattern degradation mechanism. As depicted, the received signal can follow two different paths to the RX port- the direct path and the indirect path created by the AUX port. Assuming that an EM wave hits the antenna, and would produce a power of P_{inc} at the RX port if the antenna was perfectly linear polarized with infinite axial ratio, then the power going into the RX and AUX ports is given by $P_{inc}AR/(1 + AR)$ and $P_{inc}/(1 + AR)$, respectively, where AR is the axial ratio of the antenna. In the indirect path, the signal reflects from the variable termination and then couples into the receive port with an AUX-to-RX coupling coefficient of C_2. Superposing the direct and indirect received signals at the RX port, the ratio of the total received power to the incoming power, P_{RX}/P_{inc}, assuming signals arriving at the RX and AUX port are in-phase, can be expressed as

$$\frac{P_{received}}{P_{inc}} = \frac{AR + |\Gamma_L C_2|^2 + \sqrt{AR}|\Gamma_L C_2| \cos(\Phi_\Gamma + \Phi_{C2})}{1 + AR}, \tag{2.10}$$

where Φ_Γ and Φ_{C2} are the phase of the reflection coefficient ($\angle\Gamma_L$) and C_2. Using a simulated axial ratio of 7 dB for the TX antenna, Γ=0.486∠113° and C_2=0.35∠35°, the total degradation in the RX antenna gain due to introducing the AUX port and SIC is calculated as -1.35 dB at 4.6 GHz in the broadside direction which agrees well with the broadside RX pattern degradation in Fig. 2.6.

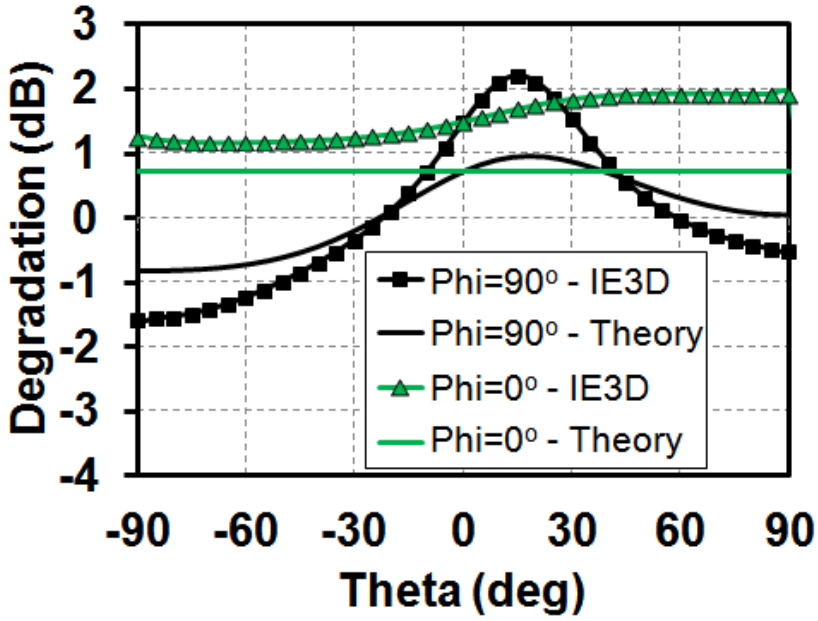

Figure 2.8: Theoretical and simulated TX antenna gain degradation in Φ=0° and Φ=0° planes.

The total degradation can be broken into two parts: degradation due to introduction of the AUX port (10log($AR/(1+AR)$)≈-0.8 dB) and due to the reflective termination (10log($P_{received}/P_{inc}$)-10log($AR/(1+AR)$)≈-0.55 dB).

2.2.4 Impact of SIC on Receiver NF

The antenna SIC also slightly degrades the RX NF. There are two different RX NF degradation mechanisms as depicted in Fig. 2.9. First, the AUX port picks up noise which is present in the orthogonal polarization. The mean square noise voltage picked up by each RX port is $\overline{v_{ant}{}^2} = 4kT_0R_0$ where k is the Boltzmann constant and assuming that the antenna temperature is T_0 and the antenna impedance is R_0 with 100% efficiency. The noise picked up by the AUX port reflects from the reflective termination and then couples into the RX port, increasing the total noise at the RX input. The total noise at the RX input also increases due to the noise generated by the passive reflective termination (with a mean square noise voltage of $\overline{v_{eq}{}^2} = 4kT_0\mathrm{Re}\{Z_L\}$ which couples into the RX port. Considering these two mechanisms, the modified noise factor of the full-duplex

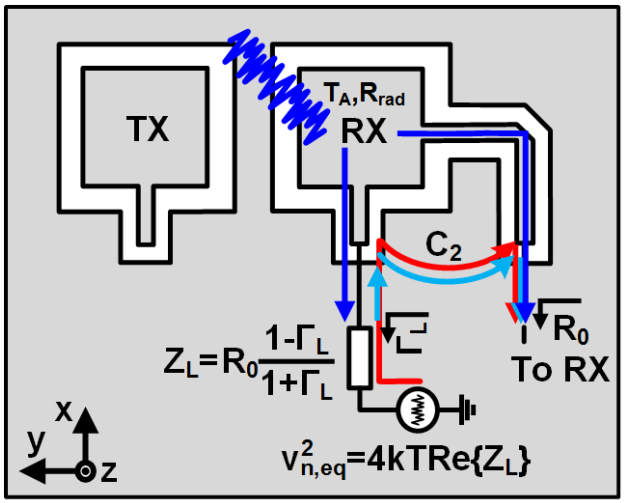

Figure 2.9: RX NF degradation mechanism.

transceiver (F_{totm}) can be calculated as

$$F_{totm} = F_{tot} + |\Gamma_L C_2|^2 + \frac{Re\{Z_L\}}{R_0}|1-\Gamma_L|^2|C_2|^2. \tag{2.11}$$

The second term in (2.11) is due to the noise picked up from the orthogonal polarization by the AUX port whereas the last term represents the contribution of the noise generated by the reflective termination. For a RX NF of 5 dB (e.g. 10log(F_{tot})=5 dB), 10log(F_{totm}) becomes 5.45 dB, 0.45 dB degradation mainly due to the last term in (2.11).

2.3 Implementation

2.3.1 5 GHz Prototype Implementation

Fig. 2.3 presents the transmit and receive antenna design and the cross-section of the PCB board. Slot antennas are chosen over patch antennas since they provide wide bandwidth and also allow integration of the proposed technique on silicon at millimeter/sub-millimeter-wave frequencies. 20 mils Rogers 4350B (ϵ_r=3.48, tan(δ)=0.0037 at 10 GHz) is used as the substrate material. The TX and RX antennas are implemented on the top copper layer. The bottom copper is assigned as the ground layer and is cut away under the antennas. A 240 mils superstrate layer is employed under the antennas to focus the radiation to the backside. Four 60 mils Rogers 4350B layers are

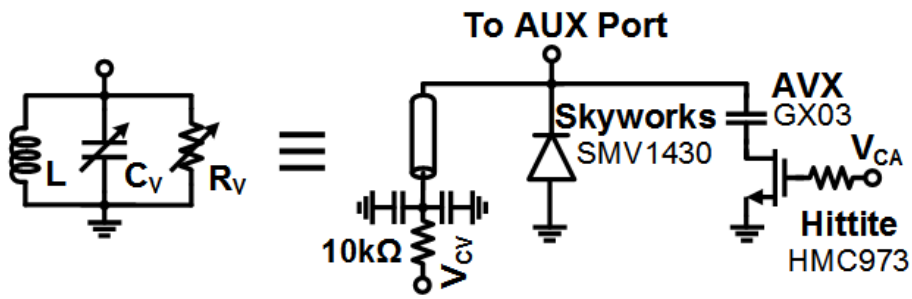

Figure 2.10: Reflective termination implementation of the 4.6 GHz T/R antenna pair prototype.

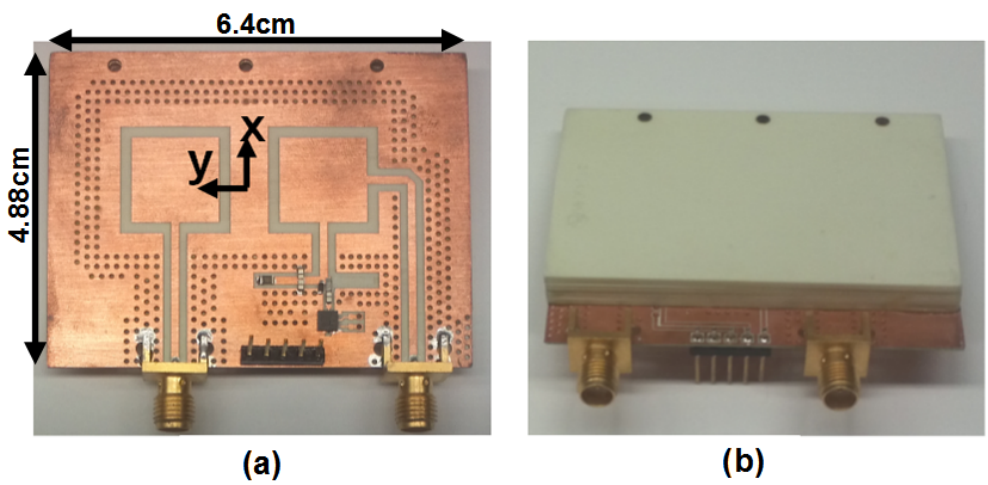

Figure 2.11: 4.6 GHz T/R antenna pair prototype: (a) top view, (b) bottom view.

glued together with very thin layers of non-conductive epoxy (dielectric constant of ≈3.6) to form the superstrate layer (Fig. 2.3).

The reflective termination is implemented using a 3.5 mm shorted stub (Z_0=50 Ω) as the fixed inductor, Skyworks SMV1430-079LF abrupt junction varactor diode as the variable capacitor and Hittite HMC973LP3E voltage controlled attenuator as the variable resistor (Fig. 2.10). The varactor diode is tunable from 0.31 pF to 1.24 pF (Q=1680 at 50 MHz and 4V) and controlled through a 10 $k\Omega$ resistance at the end of the shorted stub. The HMC973LP3E is a 0.5-6 GHz reflection type attenuator which features a variable FET-based shunt-resistor to ground between the input and output pins and is controlled by an analog gate voltage. In this work, it is used as a variable resistance by leaving the output pin floating. The attenuator is DC isolated using an AVX GX03 ultra-low-insertion-loss (less than 0.2 dB up to 16 GHz) 0.1 μF capacitor. Fig. 2.11(a) and Fig.

2.11(b) show the top and bottom views of the fabricated PCB, respectively. It occupies 4.88cm × 6.4cm x 0.66cm of space, enabling the development of compact full-duplex wireless radios. Such a compact and co-located antenna pair cannot be used in a half-duplex MIMO setting to achieve similar doubling of capacity as the spacing between the antennas is much smaller than the Rayleigh spacing required for reasonable link distances [44].

2.3.2 60 GHz On-Chip Implementation

Fig. 2.12 presents a method for the on-chip implementation of the SIC technique with on-chip slot loop antennas. The cross-section of the chip-antenna integration is shown in Fig. 2.12(a). The lossy Si substrate and CMOS back-end-of-line (BEOL) limitations pose challenges for the integration of high-gain, high-efficiency and wideband antennas. Since CMOS BEOL thickness (distance between top and bottom metal layers) is typically less than 10 μm, shielding the antenna from the lossy substrate results in current-based antennas radiating from the top with low efficiency [55,56]. High-efficiency voltage-based antennas such as slot antennas with a quartz lens [57] or superstrate above the IC [58] can be implemented on chip but they suffer from bandwidth limitations. Therefore, we propose thinning the substrate down to 50 μm and taking the radiation from the bottom. The chip containing the antennas as well as a mm-wave transceiver can be mounted on a PCB with $\epsilon_r = \sqrt{\epsilon_{air}\epsilon_{Si}}$ ≈3.45 and $\lambda/4$ thickness using a non-conductive epoxy or superglue (ϵ_r ≈3.5 for both) which can be as thin as ≈50 μm. Thus, the wave impedance in Si is matched to the wave impedance in the air, improving the antenna efficiency.

Slot loop antennas have several other advantages which make them favorable for on-chip integration. First, slot antennas help to meet the stringent CMOS metal density requirements, especially for the topmost metal, in the vicinity of the antennas. Additionally, slot loop antennas can be easily interfaced to the front-end circuits through coplanar waveguide (CPW) lines, which are the workhorses of mm-wave integrated circuit design as they easily satisfy metal density rules and provide good isolation between signal traces.

Fig. 2.12(b), Fig. 2.12(c) and Fig. 2.13 depict a 60 GHz case study of the proposed SIC technique in the IBM 45 nm SOI CMOS process. The process offers 11 metal layers (Fig. 2.12(c)), including a 2.1 μm topmost aluminum layer (LB) in which the TX and RX antennas are implemented for high efficiency. The antennas are fed using conductor-backed CPW lines in LB with

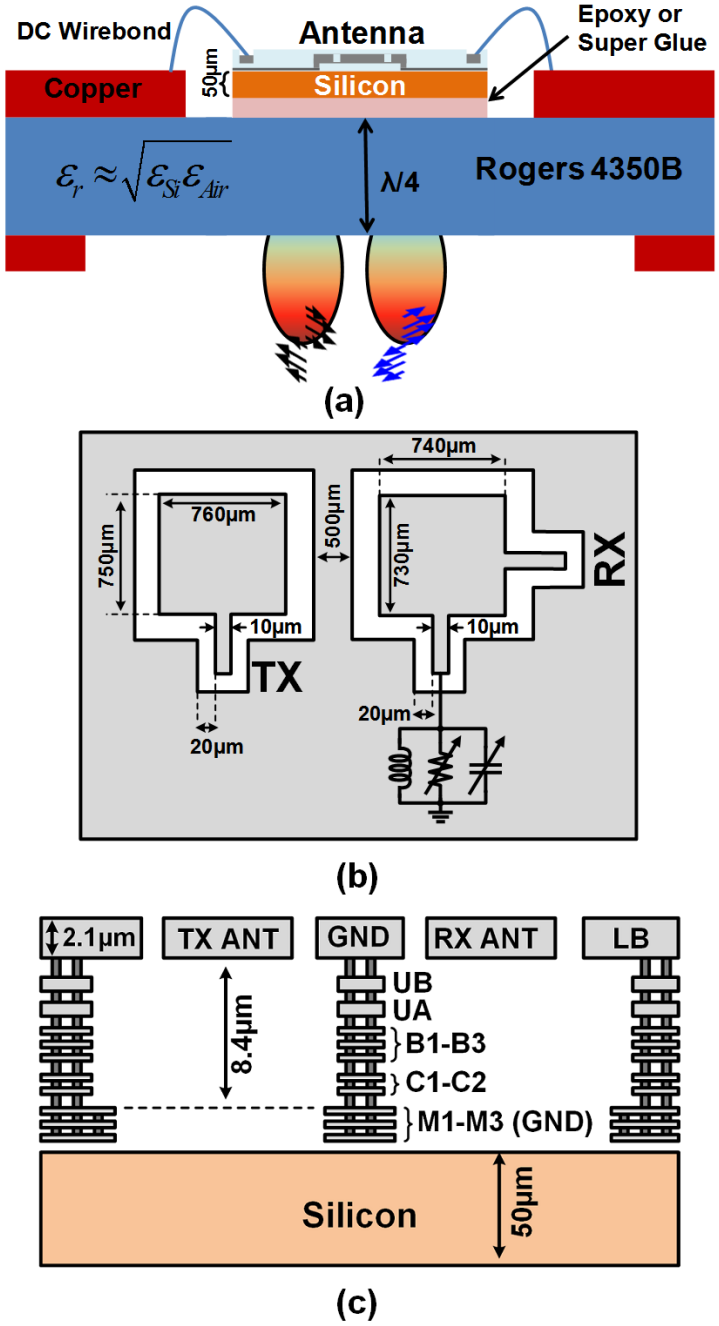

Figure 2.12: On-chip implementation of the mm-wave slot loop T/R antenna pair with the proposed reconfigurable wideband polarization-based antenna cancellation technique: (a) Cross-section of the proposed chip-PCB integration, (b) A 60 GHz implementation in IBM 45 nm SOI CMOS, (c) IBM 45 nm SOI CMOS BEOL cross-section.

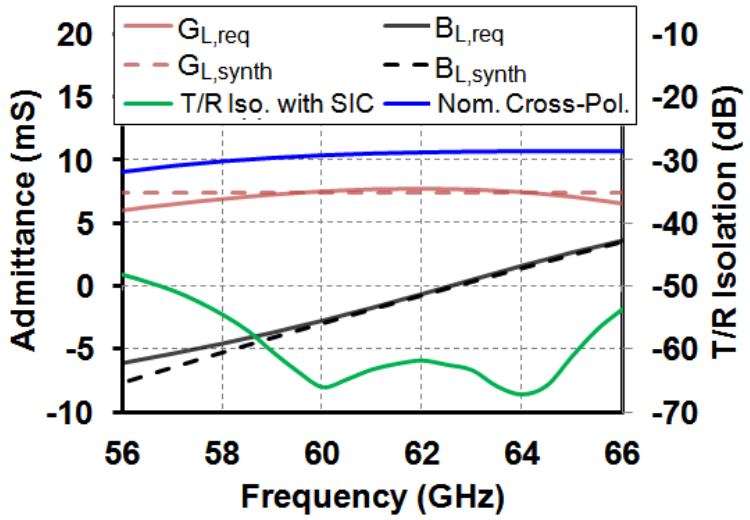

Figure 2.13: 60 GHz on-chip antenna cancellation simulations: required and synthesized admittance, and resultant SI suppression.

an M1-M3 bottom ground stack and M1-LB side grounds. The ground layer is removed under the antennas. The 60 GHz T/R antenna core is simulated in IE3D with a 650 μm Rogers 4350B superstrate layer assuming the epoxy thickness of 50 μm. Fig. 2.13 shows the simulated required and synthesized conductance and susceptance across frequency. A T/R isolation of more than 50 dB is achieved over 10 GHz bandwidth in simulation, completely covering the 60 GHz IEEE 802.11ad standard (57.24-65.88 GHz). The broadside TX and RX antenna gains are simulated without SIC as 0.15 dB with 25% efficiency and -0.45 dB with 22% efficiency, respectively.

2.3.3 60 GHz Implementation using on-PCB antennas

A 60 GHz prototype of the same technique was implemented using on-PCB antennas and its performance was verified in [45, 59], demonstrating that the proposed technique can be readily scaled up in frequency. The reflective termination was implemented on the chip using a variable resistor implemented as a deep-triode NFET, a variable capacitor implemented as an inversion-mode NFET varactor bank, and a shunt transmission line. Further details on this implementation is presented in Chapter 3.

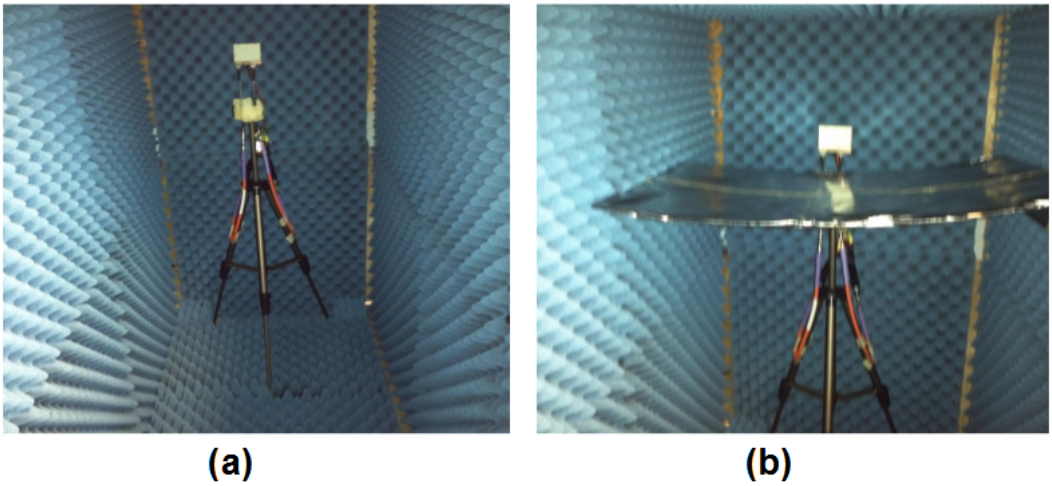

Figure 2.14: Small-signal measurement setup in the anechoic chamber: (a) without reflector, (b) with a nearby aluminum reflector.

2.4 Measurements

2.4.1 5 GHz Antenna Cancellation Measurements

Small-signal measurements of the 5 GHz antenna pair were performed in a mini-anechoic chamber from 4.2 GHz to 5 GHz using an Anritsu 37397E Lightning VNA. Fig. 2.14(a) shows the measurement setup in the anechoic chamber. Fig. 2.15 shows the measured return loss at the TX and RX ports. The TX and RX port are matched well, S_{11} <-10 dB, from 4.4 GHz to 5 GHz with and without SIC. Measured TX-to-RX isolation is shown in Fig. 2.16(a). To start with, a reference antenna pair consisting of only cross-polarized T/R antennas (i.e., without the AUX port) is characterized and its TX-to-RX isolation is -24 $\pm$1 dB from 4.4 GHz to 4.8 GHz. The measurements with SIC are compared to this curve to deduce the improvement in SI suppression. The diode and attenuator voltages (V_{CV} and V_{CA}) are set to 7 V and 1.5 V, respectively, to engage the SIC and a TX-to-RX isolation less than -50 dB from 4.45 GHz to 4.75 GHz is achieved. The antenna cancellation (i.e. improvement in TX-to-RX isolation) is higher than 20 dB from 4.4 GHz to 4.8 GHz as shown in Fig. 2.16(b). As can be seen, the measured TX-to-RX isolation with SIC compares well with the simulation. The slight shift in frequency from simulations can be attributed to modeling inaccuracy of the component packages as well as parasitics due to the soldering.

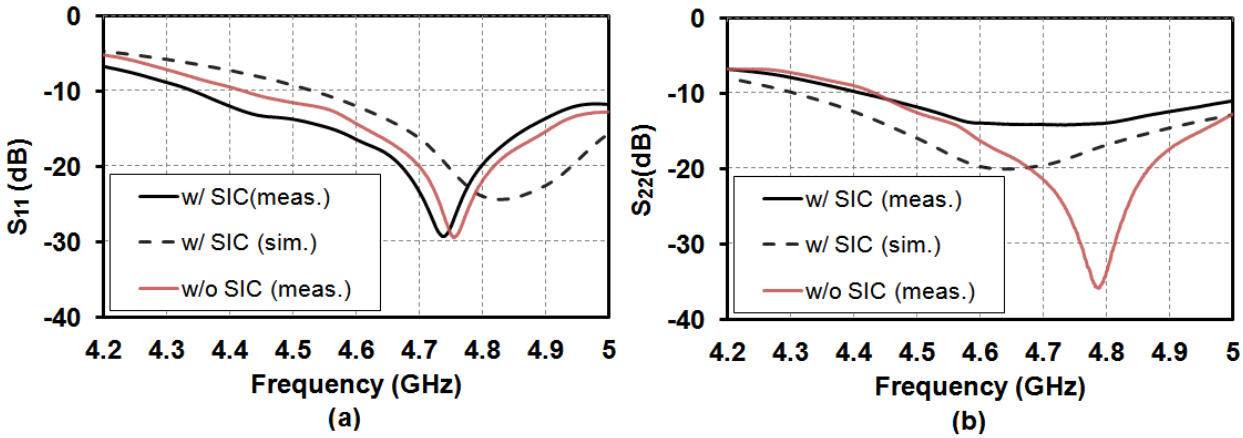

Figure 2.15: Measured and simulated (a) S_{11} (TX port return loss) and (b) S_{22} (RX port return loss) of the antenna pair.

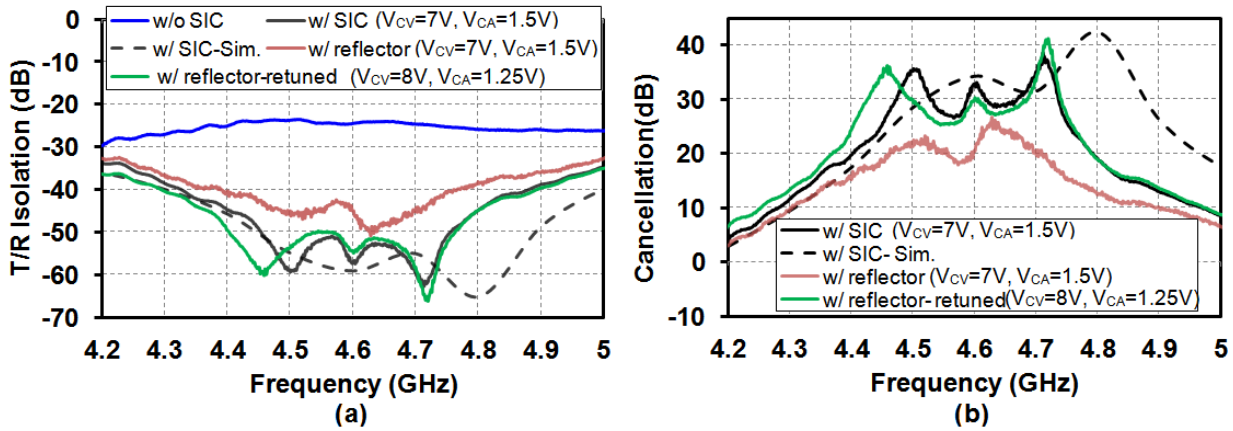

Figure 2.16: (a) Measured S_{21} with and without SIC in the anechoic chamber. (b) Achieved SIC amount across frequency. Bringing an aluminum reflector close to the antenna pair degrades the cancellation, but it can be recovered by reconfiguring the canceller settings.

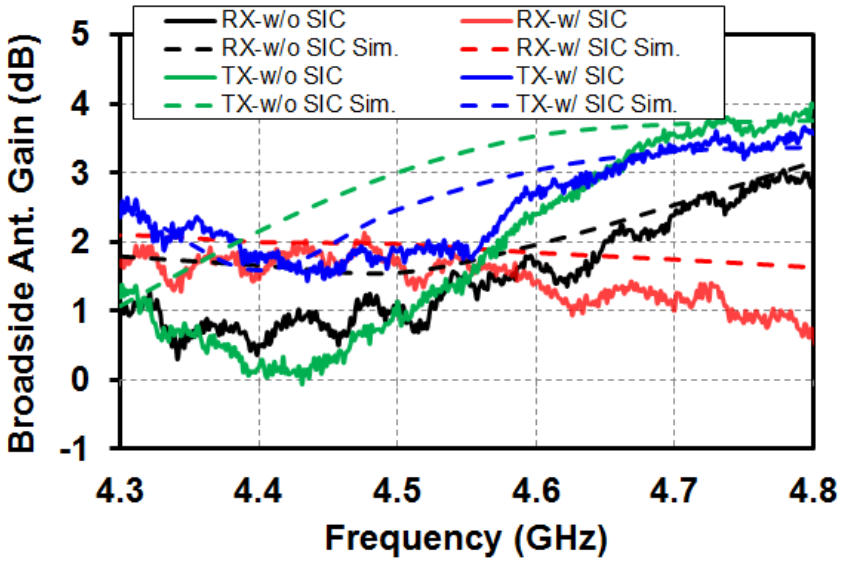

Figure 2.17: Effect of SIC on broadside TX and RX antenna gain.

The effect of nearby reflectors on the SIC is tested using the setup shown in Fig. 2.14(b). An aluminum reflector was placed 5 cm away from the antenna pair while SIC was active with 7 V and 1.5 V diode and attenuator control voltages, respectively. As can be seen in Fig. 2.16(a), the reflector degrades the overall TX-to-RX isolation by 4-16 dB in the 4.4-4.8 GHz range. The reflector creates another coupling path from TX to RX and as a result, the required Γ_L for SIC changes. However, we can recover the SIC by reconfiguring the variable capacitance and resistance values by changing the diode and attenuator control voltages to $V_{CV} = 8$ V and $V_{CA} = 1.25$ V, respectively. A T/R isolation less than 50 dB over 360 MHz bandwidth, *as high as before over a wider frequency range* (Fig. 2.16(a)-(b)), is achieved after reconfiguring the reflective termination.

The TX and RX antenna gains are measured in the broadside direction. First, the TX antenna gain without SIC is characterized by the two-antenna method, employing two identical antennas in each other's far-field. The measured TX antenna is used as a reference antenna to measure the TX antenna gain with SIC as well as the RX antenna gain with and without SIC. The measured broadside antenna gains with and without SIC are given in Fig. 2.17. The RX antenna gain degradation is essentially similar to the noise figure penalty associated with RF cancellers, while the TX antenna gain degradation is similar to the TX efficiency penalty of RF cancellers. SIC changes the RX antenna gain by ± 1 dB from 4.4 to 4.7 GHz. The change in TX gain is less than

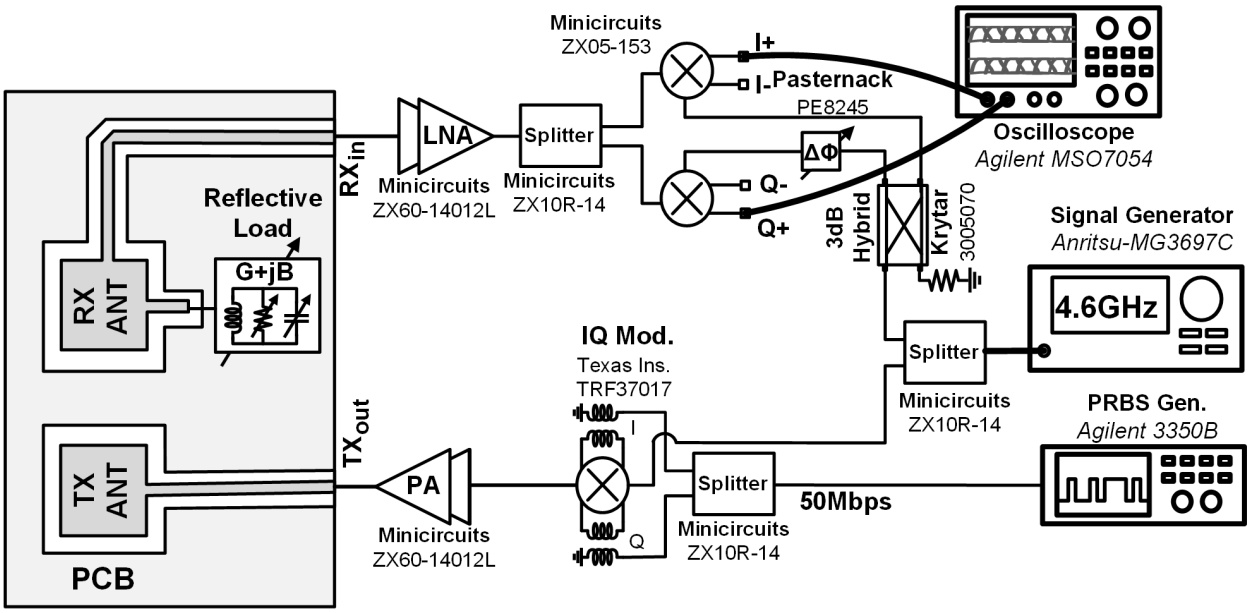

Figure 2.18: Block diagram of the full-duplex transceiver built using off-the-shelf components.

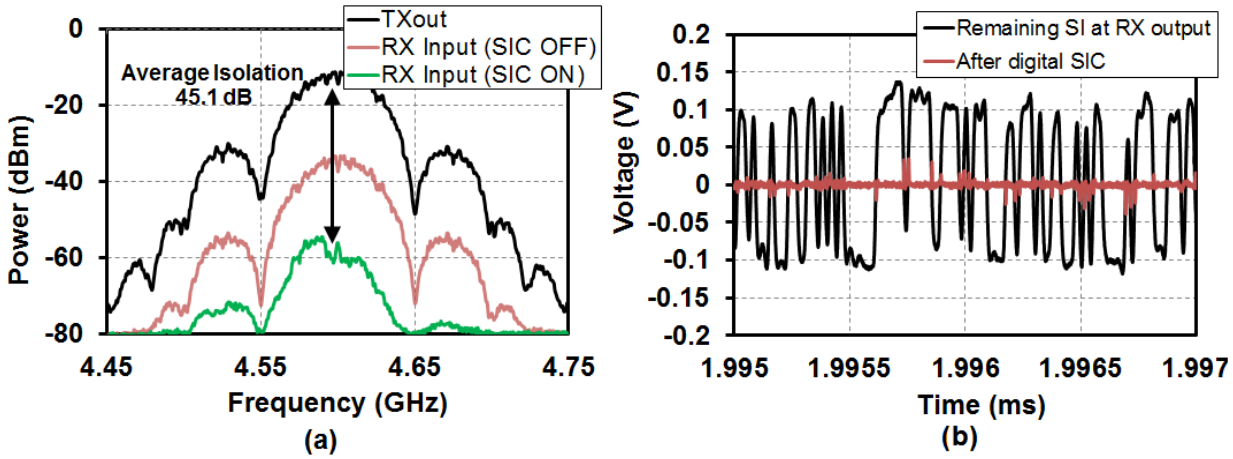

Figure 2.19: (a) Cancellation of a 50 Mbps BPSK signal in a lab environment using the full-duplex transceiver of Fig. 2.18 and (b) impact of digital SIC implemented in Matlab on the remaining SI in the time domain.

Table 2.1: Comparison with Recent SI Suppression Techniques in the Antenna Domain

Ref.	Frequency (GHz)	TX-RX Isolation (dB)	Suppression BW (MHz)	Reconfigurable	TX Gain (dBi)	RX Gain (dBi)	Form Factor cm×cm×cm
This Work	**4.6**	**50**	**300**	**2.7**	**1.5**	**Yes**	**4.9×6.4×0.7**
[52]	3.3	30-35	10	Yes#	N/R	N/R	N/R
[26]	3.47	40	55	Yes#	N/R	N/R	N/R
[24]	1.7	40	2000	No	3	3	20×23×4

Reconfigurability is not demonstrated in simulation or measurement.

N/R: Not Reported

0.3 dB from 4.55 GHz to 4.8 GHz and it improves below 4.55 GHz, increasing to 1.5 dB improvement at 4.4 GHz.

2.4.2 Measurements from a Full-Duplex Transceiver Employing the T/R Antenna Pair

Fig. 2.18 shows the block diagram of the full-duplex transceiver built using off-the-shelf components and employing the 5 GHz antenna pair. The TX chain includes an Agilent 3350B arbitrary waveform generator, a power splitter to feed the same 23-bits PRBS sequence to I and Q channels, resulting in BPSK modulation, TI TRF37017 direct I-Q modulator and two cascaded Minicircuits ZX60-14012L amplifiers driving the TX antenna. The receiver consists of two cascaded Minicircuits ZX60-14012L amplifiers as an LNA, a Minicircuits ZX10R-14 I/Q splitter and Minicircuits ZX05-153 down-conversion mixers. The transmitter and receiver share the same LO (Anritsu MG3697C signal generator) for reducing the impact of phase noise on the SIC [60]. The receiver side LO distribution also uses a Pasternack PE8245 phase shifter for calibrating I/Q mismatch.

The transmitter output power is measured as 11.1 dBm by applying 10 MHz continuous wave to the I/Q modulator for 5 dBm LO input. The cancellation of 50 Mbps BPSK signal in a lab environment is shown in Fig. 2.19 (a). The average T/R isolation is 45.1 dB over 4.45-4.75 GHz

once antenna cancellation is enabled. The remaining SI at the receiver output is digitized using an Agilent InfiniiVision MS07054A oscilloscope, essentially an 8-bit 2GSPS ADC. Digital cancellation is performed on the digitized remaining SI using an adaptive LMS filter with 5-taps and a step size of μ=0.1 in MATLAB (after adding a 44 samples delay compensation). Fig. 2.19 (b) shows the time domain waveforms before and after digital cancellation. An average 24 dB digital cancellation is achieved, bringing total SIC to approximately 70 dB. An additional 37 dB cancellation is needed to suppress the SI below the receiver noise floor and can be achieved through RF, analog baseband or improved digital cancellation.

2.5 Summary

This chapter presented a reconfigurable polarization based cancellation technique in the antenna domain for same-channel full-duplex applications. The technique is verified by a 4.6 GHz prototype achieving more than 20 dB SIC over 400 MHz. The total SI suppression with cross-polarization and SIC is more than 50 dB over 300 MHz bandwidth. The SIC is reconfigurable to combat the environmental reflections which are unpredictable during the design process and can vary in-field. This work achieves at least 4× better fractional SIC bandwidth at 10 dB higher isolation compared to the other reconfigurable antenna cancellation works in Table 2.1. It is also the only work to experimentally demonstrate reconfiguration to maintain SIC in the presence of environmental changes. [24] is able to achieve superior suppression BW but at a lower suppression and does not possess reconfigurability features which are essential for supporting a robust full-duplex link. The technique can be readily scaled up in frequency and be implemented on-chip at mm-Wave frequencies. A 60 GHz on-chip implementation method is proposed and provides more than 50 dB SI suppression over 10 GHz BW in simulation. A 60 GHz implementation with on-PCB antennas will be described in the next chapter, enabling mm-Wave full-duplex operation for the first time.

Chapter 3

A 60GHz CMOS Transceiver with Polarization-Based Antenna and RF Cancellation

When combined with full-duplex operation, mm-wave links can offer wide BWs with improved spectral efficiency, a step toward delivering the tremendous increase in capacity demanded by emerging wireless standards. However, as discussed in Chapter 1, the fundamental challenge in achieving FD operation is the strong self-interference from the transmitter to its own receiver. A total self-interference suppression of 90-100 dB must be achieved in antenna, RF/analog and digital domains to enable FD operation. Recently, the feasibility of full-duplex has been established through laboratory bench-top demonstrations leveraging off-the-shelf components [34]. However, research efforts on fully-integrated full-duplex transceivers are still in their infancy, even at low RF frequencies.

This chapter presents the first fully-integrated mm-wave full-duplex transceiver front-end, a 60 GHz direct-conversion transceiver in 45 nm SOI CMOS for FD wireless communication. Full-duplex operation is enabled by the novel polarization-based antenna cancellation technique discussed in the previous chapter. The antenna cancellation can be reconfigured from the IC to combat the variable self-interference scattering from the environment during in-field operation. A second RF cancellation path with >30 dB gain control and >360° phase control from the trans-

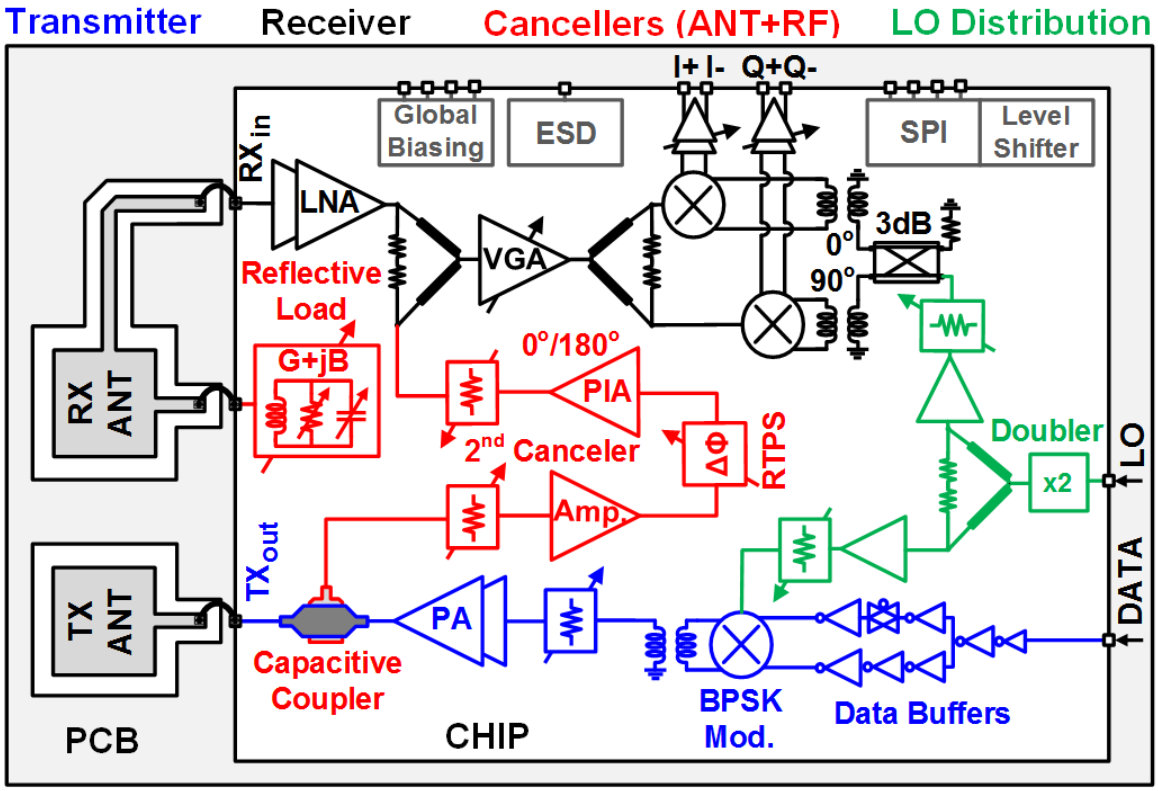

Figure 3.1: 60 GHz fully-integrated full-duplex transceiver architecture featuring polarization-based reconfigurable wideband antenna cancellation and RF cancellation.

mitter output to the LNA output further suppresses the residual SI to achieve the high levels of required SIC. With antenna and RF cancellation together, a total self-interference suppression of >70 dB is achieved over a cancellation bandwidth of 1 GHz and can be maintained in the presence of nearby reflectors. In conjunction with digital SIC implemented in MATLAB, a full-duplex link is demonstrated over 0.7 m with a signal-to-interference-noise-and-distortion ratio (SINDR) of 7.2 dB.

A detailed discussion of the 60GHz FD transceiver with a focus on system level analysis, antenna-cancellation trade-off discussions, circuit descriptions, simulations and measurements is presented in the rest of this chapter.

3.1 Millimeter-wave Full-Duplex System Analysis

3.1.1 Architecture

The 60 GHz full-duplex transceiver architecture is shown in Fig. 3.1. It is a direct conversion BPSK[1] transceiver consisting of five main parts: on-PCB T/R antenna pair with polarization-based antenna cancellation, transmitter, receiver, the second RF canceller and LO distribution. The antenna pair is based on cross-polarized slot loop antennas and a high-order on-chip termination is embedded within the antenna pair to enable antenna cancellation. It will be explained later in Section 3.2. In the transmitter, baseband non-return-to-zero (NRZ) data is applied to an inverter-chain data buffer driving a BPSK modulator, directly modulating the LO signal. A transformer balun and a 3-bit reflective-type attenuator are included after the BPSK modulator for differential to single-ended conversion and transmitter power control. A two-stage, two-stacked Class-E-like PA constitutes the final stage of the transmitter to achieve a high output power with high efficiency. The receiver consists of a two-stage, high-gain, low-noise amplifier (LNA) driving a Wilkinson combiner that injects the cancellation signal from the RF canceller, an RF amplifier followed by a 2-bit attenuator, a Wilkinson-based I/Q splitter, I/Q down-conversion mixers and two-stage baseband amplifiers.

An 18 dB coupler is integrated as the first block in the second RF canceller to couple a small copy of the transmit signal from the PA output. The TX copy is fed into an attenuator with 16 dB range driving an RF amplifier, followed by a reflection-type phase shifter (RTPS) with $>180^\circ$ analog phase-control range and a 0° /180° phase-inverting amplifier (PIA). Finally, the RF cancellation signal is injected into the receiver at the LNA output through another 16 dB attenuator and the aforementioned Wilkinson combiner.

LO distribution includes a balanced frequency doubler to allow a 30 GHz LO signal from off-chip. The LO signal is split after the frequency doubler and shared between the RX and TX to keep phase noise highly correlated between the TX and RX, reducing its impact on SIC [60, 61]. Circuit implementations of the transceiver blocks are presented in Section 2.3.

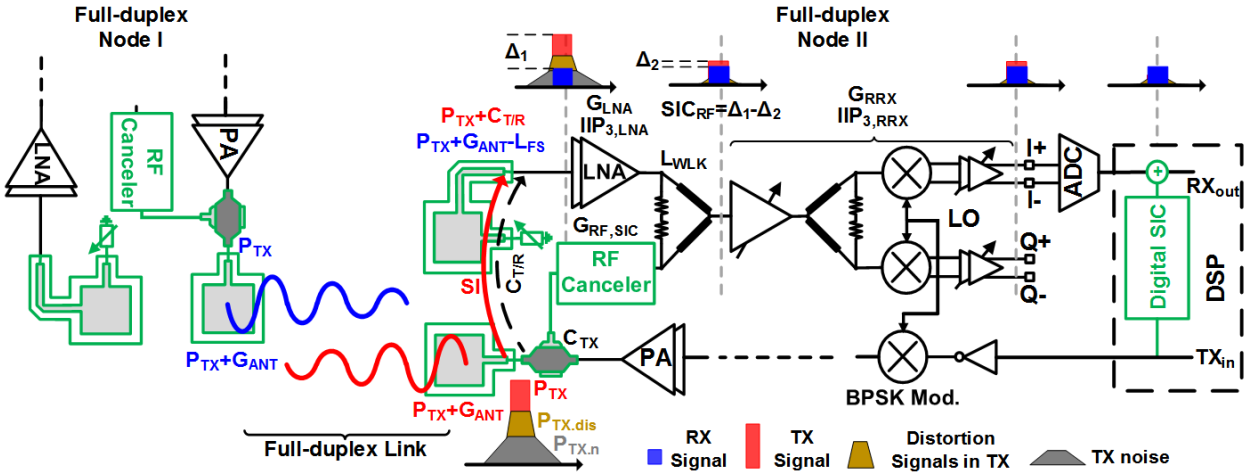

Figure 3.2: Simplified full-duplex transceiver block diagram with polarization-based antenna, RF and digital cancellation.

3.1.2 Full-duplex System Considerations

In this subsection, the system-level design trade-offs are discussed in detail. All the equations will be in dB-scale except if otherwise mentioned. Fig. 3.2 depicts the simplified transceiver block diagram used for system-level analysis, including the antenna, second RF and digital cancellation. The TX signal at the transmitter output consists of the main TX signal (P_{TX}), TX non-linear distortions ($P_{TX,dis}$) and TX noise ($P_{TX,n}$). SI arises due to the inherent coupling at the antenna interface as well as environmental reflections. In the analysis, $C_{T/R}$ represents the net coupling from the transmitter to the receiver at the antenna interface, inclusive of the inherent coupling, environmental reflections and any antenna SIC that is achieved. As discussed in Chapter 1, a total SI suppression of P_{TX}-P_{noise}+6 dB is required to suppress the main TX signal below the RX input-referred noise floor (P_{noise}=-174dBm/Hz+10log(BW)+$NF_{RX,tot}$), assuming a 6 dB margin.

Assuming RX and TX antenna gains of G_{ANT}, an RX BW of 2.16 GHz (specified in IEEE 802.11ad standard), a typical RX NF of $NF_{RX,tot}$ =5 dB and BPSK modulation with a required

[1]A BPSK modulator was included in the transmitter for simplicity, but can easily be replaced with an I/Q modulator to support full-duplex links with QAM and other complex modulation formats.

bit error rate of BER=10^{-6} (requiring SNR_{out}=12 dB), the link budget can be calculated as[2]

$$P_{TX} + 2G_{ANT} + L_{FS} > -174dBm/Hz + 10log(BW) + NF_{RX,tot} + SNR_{out} + LM\,, \qquad (3.1)$$

where L_{FS} is the free space path loss and LM is the link margin for the implementation and antenna alignment losses. Assuming LM=10 dB, a link budget of P_{TX}+2G_{ANT}>20 dBm is required to achieve a 2 m long full-duplex wireless link (L_{FS}=74 dB). The required total SIC and link budget are both a function of P_{TX}. A higher P_{TX} is desirable for reducing the BER or extending the link distance whereas a lower P_{TX} demands less SIC, *resulting in a trade-off between the link budget and SIC. On the other hand, a higher antenna gain relaxes not only the P_{TX} but also the total SIC requirement*[3]. For a state-of-the-art 60 GHz transmitter output power of 10-15 dBm, a G_{ANT} of 5-2.5 dBi is required, precluding the use of on-chip antennas. Hence on-PCB antennas are used in this work. For P_{TX}=+14 dBm (and G_{ANT}=3dBi), a total SI suppression of 14 dBm-(-174 dBm/Hz+10log(2.16 GHz)+5 dB)+6 dB=96 dB must be achieved.

An interesting question is how to distribute this 96 dB SIC along the receiver chain. At mm-waves, high-speed high-resolution ADCs form a power consumption bottleneck in the system. Considering the system in Fig. 3.2, the required ADC dynamic range can be expressed as

$$DR_{ADC} = 96dB + C_{T/R} - SIC_{RF} = 6 \times (ENOB - 2)\,, \qquad (3.2)$$

where ENOB is the effective number of bits. *According to (3.2), it is essential to achieve a high SIC in the antenna and RF cancellers to relax the ADC dynamic range requirement.* To allow an 8-bit ADC, the antenna and second RF canceller must provide more than 60 dB SI suppression.

The antenna and RF cancellers in Fig. 3.2 take a copy of not only the main TX signal but also the TX distortion and noise. The TX distortion and noise are weak compared to the main TX signal and are easily suppressed below the receiver noise floor by the antenna and RF cancellers. Therefore, we will neglect them in the system level analysis. However, the RX chain and RF canceller might introduce non-linear distortions on the TX signal which require careful treatment. All these non-linear distortions can be cancelled in the digital domain since they are predictable [34],

[2]Assuming the SI is suppressed well below P_{noise}. Note also that $NF_{RX,tot}$ includes the degradation due to SIC.

[3]This assumes that the environmental reflections are weak compared to the SI through the antenna interface, verified by the measurements.

but this can be more challenging and power inefficient at mm-wave due to the wide BW. Hence, in Fig. 3.2, we assume that the antenna interface should suppress the SI at the LNA input so that third-order inter-modulation products (IM3) generated by the LNA fall below the noise floor. The resultant LNA IIP_3 requirement ($IIP_{3,LNA}$) is given as

$$IIP_{3,LNA} = \frac{3(P_{TX} + C_{T/R}) - P_{noise} - 3}{2}. \tag{3.3}$$

Equation (3.3) indicates that a higher suppression at the antenna interface relaxes the LNA linearity requirement. This work achieves more than 50 dB suppression in the antenna canceller as will be presented in Section 3.2, so that an $IIP_{3,LNA}$ less than -17.5 dBm is required for $NF_{RX,tot}$=5 dB, BW=2.16 GHz and P_{TX}=+14 dBm.

The RF canceller further suppresses the SI in the receiver chain so that IM3 products generated by the rest of the receiver (the RF VGA, mixer and baseband circuits) fall below the noise floor as well. The linearity requirement for the rest of the receiver ($IIP_{3,RRX}$) can be written as

$$IIP_{3,RRX} = \frac{3(P_{TX} + C_{T/R} - SIC_{RF}) - P_{noise} - 3}{2} + G_{LNA} + L_{WLK}, \tag{3.4}$$

where SIC_{RF} is the SIC amount achieved by the second RF canceller, G_{LNA} is the LNA gain and L_{WLK} is the loss of the Wilkinson combiner. For P_{TX}=+14 dBm, $C_{T/R}$=-50 dB, SIC_{RF}=20 dB, P_{noise}=-76 dBm, G_{LNA}=18 dB and L_{WLK}=4 dB, the required $IIP_{3,RRX}$ becomes -25.5 dBm. *More antenna and RF SIC are essential to reduce the linearity requirement of the whole RX chain.*

Similar to the RX, the RF canceller requires careful design since it should not degrade RX NF or generate large inter-modulation products. As discussed earlier, we would like to keep IM3 products generated by the RF canceller below the RX noise floor. In this case, the IIP_3 requirement on the RF canceller in Fig. 3.2 can be expressed as

$$IIP_{3,RFSIC} = \frac{3P_{TX} - P_{noise} - 3 + C_{T/R} + 2C_{TX}}{2}, \tag{3.5}$$

where C_{TX} is the TX-side coupling. For P_{TX}=+14 dBm, $C_{T/R}$=-50 dB, P_{noise}=-76 dBm and C_{TX}=-18 dB (based on the implementation), $IIP_{3,RFSIC}$ should be higher than +14.5 dBm. The RF canceller gain ($G_{RF,SIC}$) should be equal to $C_{T/R}$+G_{LNA}-C_{TX} for perfect cancellation. Using G_{LNA}=18 dB, Fig. 3.3 compares three different configurations for the RF canceller implementation ($G_{RF,SIC}$=-14dB), and shows the IP_{1dB} requirements for each stage to achieve an

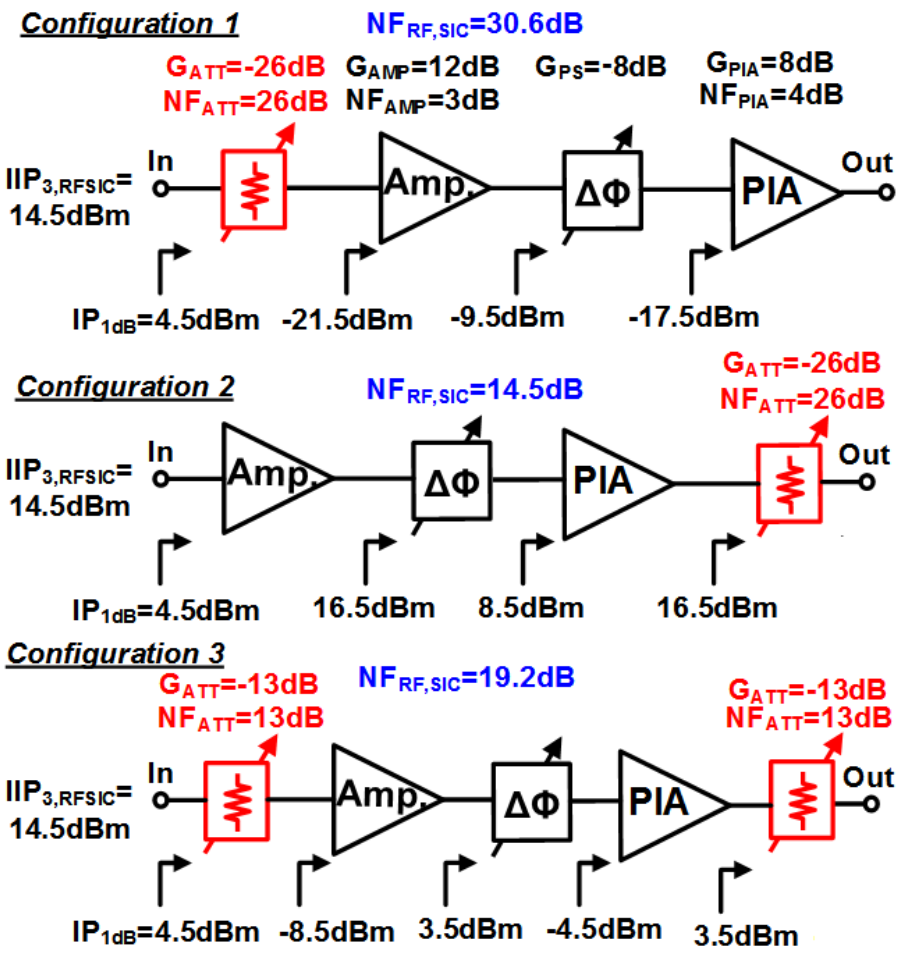

Figure 3.3: RF canceller linearity and noise figure considerations: Placing all the attenuation at the front (configuration-1) relaxes the linearity requirement of the amplifiers. To reduce the RX NF degradation, all the attenuation should be placed at the end (configuration-2). Attenuation may be distributed at the front and end to trade-off the RF canceller linearity and NF, resulting in a negligible RX noise floor increase due to the RF canceller noise and IM3 products (configuration 3). In each case, the required 1 dB compression point at the input of each stage to maintain an overall RF canceller IIP_3 of +14.5 dBm and the overall RF canceller NF are computed and shown.

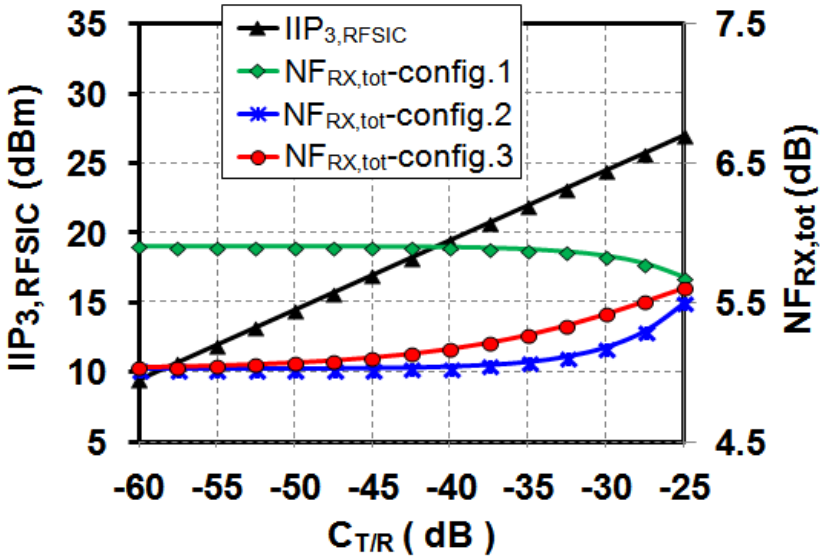

Figure 3.4: Required IIP_3 for the RF canceller versus $C_{T/R}$ to keep the generated IM3 products below the receiver noise floor and $NF_{RX,tot}$ for the three different RF canceller configurations.

$IIP_{3,RFSIC}$=14.5 dBm as well as the overall achieved NF in the RF canceller. Assuming an RF amplifier with 12 dB gain and 3 dB NF, an RTPS with 8 dB loss and a PIA with 8 dB gain and 4 dB NF (all based on the implementation), 26 dB attenuation is required, which can be distributed in the chain in various ways. A high attenuation at the front (configuration-1) is essential to relax the linearity requirement on the succeeding blocks, especially the amplifier and PIA, whereas attenuation at the end (configuration-2) reduces the canceller NF. Splitting the attenuation at the front and end trades off linearity and noise performance in the RF canceller (configuration-3). Assuming the NF of the RF canceller is $NF_{RF,SIC}$, the total NF of the RX ($NF_{RX,tot}$) can be written in linear scale as [62]

$$NF_{RX,tot} = NF_{RX} + (NF_{RF,SIC} - 1)\frac{C_{T/R}}{C_{TX}}. \tag{3.6}$$

Fig. 3.4 presents $NF_{RX,tot}$ and $IIP_{3,RFSIC}$ versus $C_{T/R}$ for the three different configurations in Fig. 3.3. To plot $NF_{RX,tot}$ in Fig. 3.4, the required attenuation G_{ATT} and corresponding $N_{RF,SIC}$ are recalculated as $C_{T/R}$ changes. NF_{RX} is assumed to be 5 dB. It should be noted that the three configurations converge to each other as expected for high $C_{T/R}$ or for G_{ATT}=0dB. *A lower* $C_{T/R}$

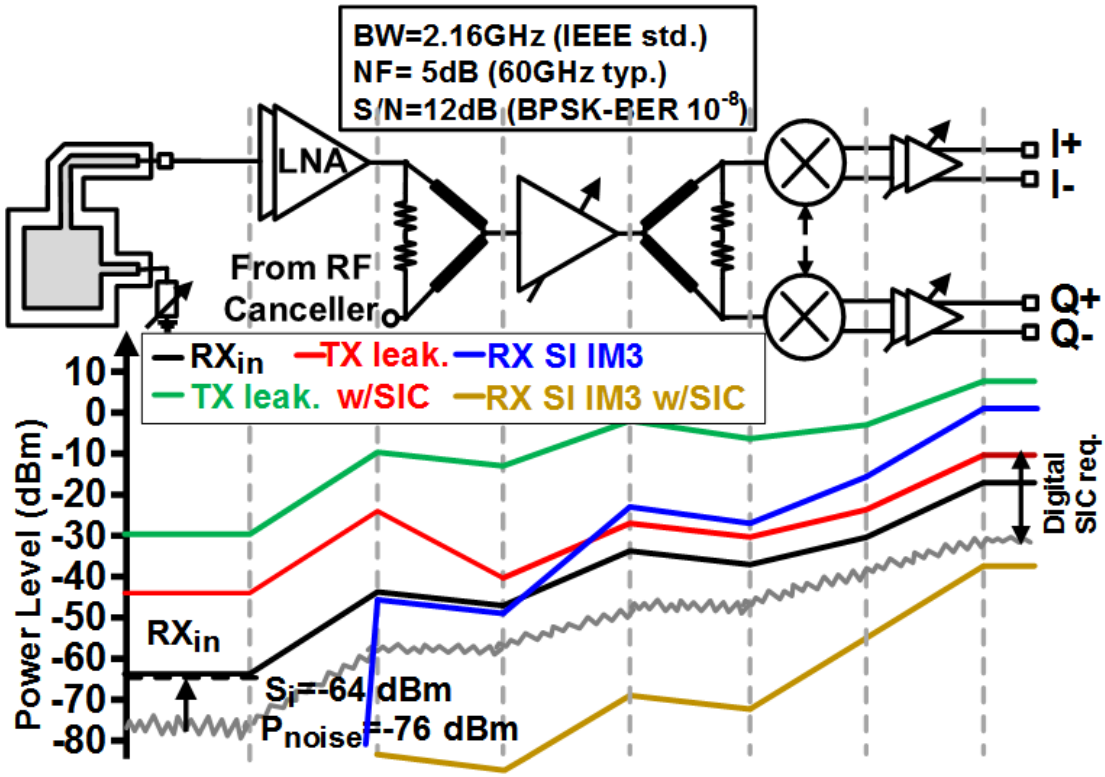

Figure 3.5: Received signal, SI, RX noise floor and SI IM3 products generated in the RX (with and without antenna and RF SIC) are tracked through the receiver chain for P_{TX}=+14 dBm, $C_{T/R}$=-44 dB without ANT SIC, ANT SIC of 14 dB and RF SIC of 20 dB. BW is assumed to be 2.16 GHz and $NF_{RX,tot}$ is assumed to be 5 dB. Without ANT and RF SIC, the TX leakage (SI) and its IM3 products generated along the RX mask the desired signal. SIC suppresses the SI so that IM3 products are suppressed below the RX noise floor. Additional cancellation of the main SI is required and can be achieved in the digital domain.

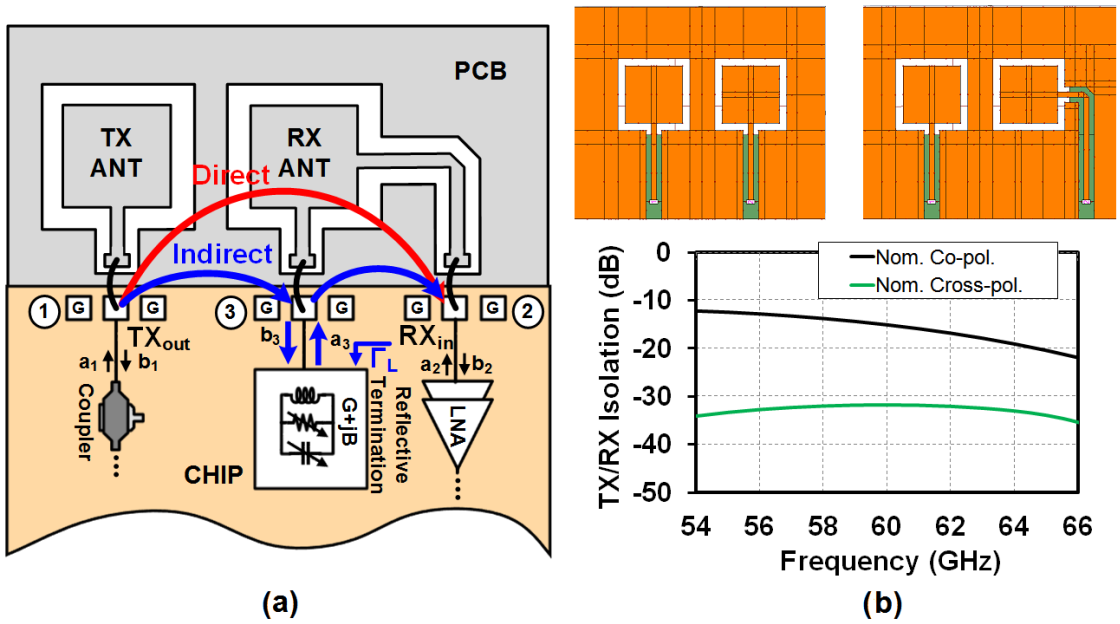

Figure 3.6: Polarization-based reconfigurable self interference cancellation: (a) T/R antenna pairs with orthogonal polarizations are employed to increase initial isolation. An auxiliary port co-polarized with the TX antenna is introduced on the RX antenna and terminated with a reconfigurable reflective termination to perform SIC. (b) Co-polarized and cross-polarized slot-loop T/R antenna pairs at 60GHz based on the dimensions and PCB cross-section shown in Fig. 7 (image taken from a layout in IE3D, a Method-of-Moments-based EM simulator) and comparison of their T/R isolation.

reduces not only the linearity requirement of the RF canceller but also the RX NF degradation so that an RF canceller configuration with a higher NF can be tolerated. As a result, at $C_{T/R}$=-50 dB, configuration-3 is as good as configuration-2 from a noise perspective and does not increase $NF_{RX,tot}$. Therefore, in this work, the attenuation is distributed at the front and back of the RF canceller (configuration-3), resulting in negligible degradation in the RX noise floor due to the canceller noise and IM3 products. Based on these concepts and assuming a P_{TX} of +14 dBm, a $C_{T/R}$ of -44 dB without antenna SIC, an antenna SIC of 14 dB and RF SIC of 20 dB (based on the measurements in Section 3.4) as well as a BW of 2.16 GHz and $NF_{RX,tot}$ of 5dB, Fig. 3.5 tracks the SI, desired signal at the sensitivity level, RX noise floor and SI IM3 products generated in the RX along the chain for this design. The contribution of the RF canceller noise and IM3 products

are not shown because the aforementioned design principles ensure that they contribute negligibly.

In reality, as mentioned earlier in Chapter 2, SI also arises from mechanisms other than the inherent coupling, such as environmental reflections and on-chip coupling. Environmental reflections are unknown at the design time and change during in-field operation. Therefore, *the antenna and RF cancellers should be reconfigurable to combat environmental reflections and thus enable robust full-duplex operation.* The receiver and transmitter are placed as far from each other as possible in the layout to reduce the on-chip coupling. Other than separating the TX and RX chains, conductor-backed CPW lines with side grounds are used to implement matching networks and interface the blocks, further reducing the on-chip coupling. Our measurements show that net coupling referenced between the TX output and RX input is lower than 78 dB over 57-66 GHz, weaker than the measured pre-digital SI suppression and hence not a significant concern.

3.2 Polarization-Based Reconfigurable Wideband Antenna Cancellation

The polarization-based SI cancellation technique in the antenna domain is shown in Fig. 3.6(a). Discussion of this technique will be significantly streamlined in this section as a detailed analysis is provided in Chapter 2. First, cross-polarized TX and RX antennas are employed to improve the initial isolation between the TX output and RX input. This increases the TX-to-RX isolation from 12-22 dB to 32-36 dB over 54-66 GHz (Fig. 3.6(b)). These simulations are for rectangular slot-loop antennas in a PCB cross-section that is described later in this section.

To improve the TX-to-RX isolation further and combat the scattering from environment, an auxiliary (AUX) port co-polarized with the TX antenna is introduced on the RX antenna. As depicted in Fig. 3.6(a), the auxiliary port creates an indirect path from the TX output to the RX input. The indirect path represents the cancellation signal which first couples to the auxiliary port, then reflects from a reflective on-chip reconfigurable termination and eventually couples into the receiver input to cancel the SI from the direct path. Assuming that the RX port is matched, the total isolation from the TX output to the RX input, $C_{T/R}$, can be expressed as

$$C_{T/R} = \frac{b_2}{a_1} = S_{21} + \frac{S_{23}S_{31}\Gamma_L}{1 - S_{33}\Gamma_L}\,, \tag{3.7}$$

where S_{21}, S_{31}, S_{23} and S_{33} are the S-parameters of the 3-port antenna structure including π-type

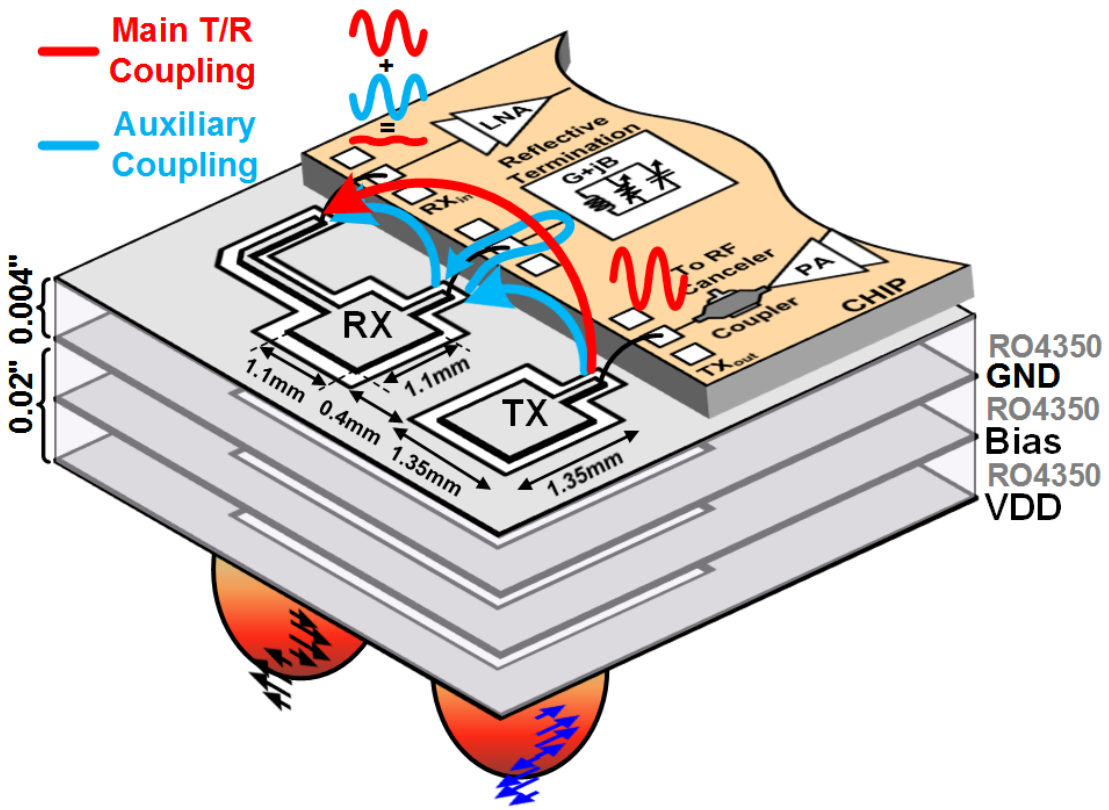

Figure 3.7: Polarization-based reconfigurable wideband antenna SIC: 3-D implementation view showing antenna and PCB dimensions and cross-section.

PCB-to-chip transitions formed by on-chip pad capacitance, wirebond inductance and on-PCB pad capacitance (ports 1, 2 and 3 are TX_{out}, RX_{in} and auxiliary ports, respectively), a_1 is the incident power wave at TX_{out}, b_2 is the outgoing power wave at RX_{in} and Γ_L is the reflection coefficient of the variable on-chip termination. The direct (first) and indirect path (second) terms in (3.7) must be set equal in magnitude and 180° out of phase to achieve perfect SIC ($C_{T/R}$=-∞ dB).

A detailed algorithmic design methodology for the polarization-based antenna cancellation technique is already described in Chapter 2. Therefore, the design procedure is briefly outlined in this section. First, the 60 GHz T/R antenna pair is designed and simulated in IE3D, a Method-of-Moments-based EM simulator [1]. The T/R antennas are implemented as rectangular slot loop antennas on Rogers 4350B because of their higher bandwidth. The TX and RX antennas are co-located *to ensure a small-form factor and allow potential scaling of the technique to arrays and MIMO*. Such a compact and co-located antenna pair cannot be used to double the capacity in a

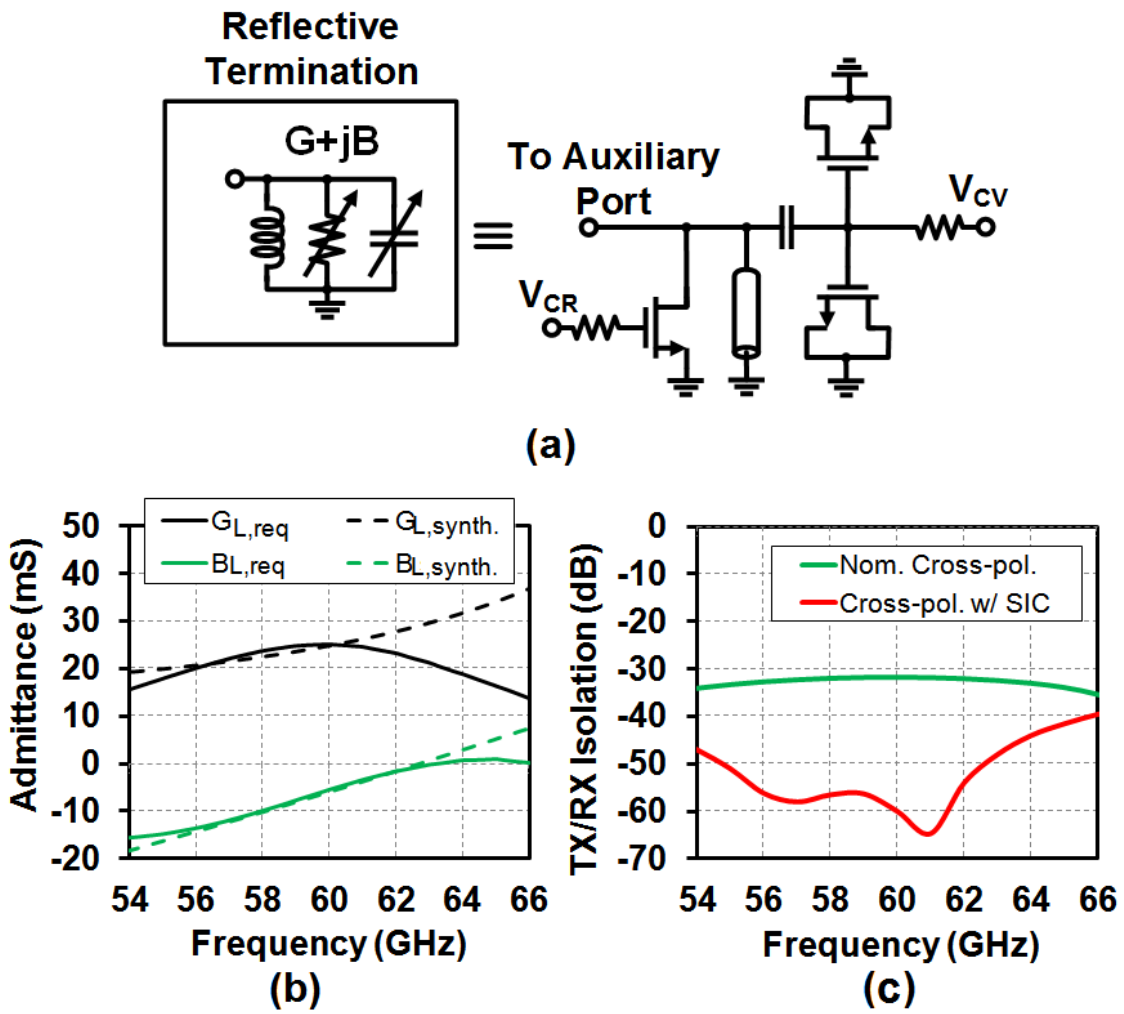

Figure 3.8: (a) Schematic diagram of the implemented fully-integrated reconfigurable parallel-RLC reflective termination, (b) comparison of synthesized conductance and susceptance to the required values across frequency for perfect SIC, and (c) resultant antenna cancellation.

half-duplex MIMO scenario since the antenna spacing is much smaller than the required Rayleigh spacings for reasonable link distances (5 cm for a 1 m link at 60 GHz), causing correlation between the MIMO paths. In other words, the proposed antenna pair does not steal any resources from MIMO and can be used to design full-duplex MIMO radios, further improving the capacity offered by MIMO. Fig. 3.7 shows the antenna dimensions and the 4-layer PCB cross-section. The TX and RX antennas are implemented on the top copper layer of a 4 mils Rogers 4350B (ϵ_r=3.48, tan(δ)=0.0037 at 10 GHz) material. A 20 mils Rogers 4350B layer is used underneath to increase the directivity on the backside.

After finalizing the 60GHz T/R antenna core, the required admittance for perfect SIC, $Y_{L,req} = Y_0 \frac{1-\Gamma_{L,req}}{1+\Gamma_{L,req}}$, is calculated across frequency where $\Gamma_{L,req}$=$-S_{21}/(S_{23}S_{31} - S_{21}S_{33})$ from (3.7). Fig. 3.8(b) shows the simulated required conductance ($G_{L,req}$) and susceptance ($B_{L,req}$) to achieve perfect SIC across frequency. As discussed in Chapter 2, a higher-order reflective termination provides more degrees of freedom to replicate the required conductance, susceptance and their slopes at more frequencies. This work employs a programmable parallel RLC termination with variable R, variable C and fixed L. The variable C and fixed L synthesize both magnitude and slope of $B_{L,req}$ at one frequency. L is set to replicate the slope of $B_{L,req}$ dictated by the EM simulation of the T/R antenna structure. The variable R in parallel can synthesize arbitrary $G_{L,req}$ but would result in a slope of $G_{L,synth}$ that is zero. We ensure that the required slope of $G_{L,req}$ is also zero by using the length of the transmission lines feeding the antennas as another degree of freedom. Fig. 3.8(a) shows the synthesized $G_{L,synth}$ and $B_{L,synth}$ to achieve wideband SIC. In this simulation, finite quality factors of the L and C cause slight frequency dependency in $G_{L,req}$. As shown in Fig. 3.8(b), an SI suppression more than 50 dB is achieved over 8 GHz bandwidth in simulation. According to our EM simulation, a similar isolation could also be achieved separating cross-polarized TX and RX antennas by 5 cm, clearly not a compact solution. As mentioned earlier, this separation is of the order of the Rayleigh separation for a 1 m 60 GHz MIMO link, implying that such an approach would steal resources from a potential MIMO implementation. This wideband cancellation corresponds to a fractional bandwidth of 13.5%, vastly superior to prior antenna [25, 26] and RF cancellation works [28–31]. *This is a direct result of the use of a higher-order termination and the replication of the magnitudes and slopes of $G_{L,req}$ and $B_{L,req}$.* This high fractional bandwidth is also a consequence of the fact that this cancellation technique is contained within the antenna pair

itself. *Essentially the antenna cancellation technique embeds the functionalities of the TX and RX side couplers within the antennas, resulting in main and auxiliary paths that are very close to each other in nature and transfer function, enhancing cancellation bandwidth.* The reconfigurable nature of the termination enables the cancellation to be maintained in the face of varying environmental reflections, as will be experimentally demonstrated in Section 2.4.

The simulated TX and RX radiation patterns at 60 GHz with and without SIC are shown in Fig. 3.9. The simulated TX antenna gain is 4.5 dB without SIC in the broadside direction and degrades by 1.1 dB with SIC. The effect of SIC on TX antenna gain varies with the elevation angle θ and is plotted in Fig. 3.10 for Φ=0° and Φ=90°. The maximum degradation in the TX pattern is 1.1 dB at around θ=0°. The variation in the TX antenna gain occurs as a result of the radiation of the coupled TX signal at the auxiliary port from the RX antenna. This indirect radiation from the RX antenna interferes with the main radiation from the TX antenna in the far-field. This mechanism can be modelled as a 2×1 antenna array with non-uniform amplitude excitations and is analyzed in Chapter 2. Based on the analysis provided in Chapter 2, the theoretical TX antenna gain degradation, the difference between the antenna gain without SIC and with SIC, is calculated for this work (using the simulated TX to auxiliary port coupling of 15.4 dB (phase of 25°), $\Gamma_{L,synth}$=0.4∠137°, and antenna separation d=0.384λ) and compared to the EM simulations in Fig. 3.10. As can be seen, the simulations compare well with the theory. SIC degrades the RX antenna gain by 0.18 dB in simulation in the broadside direction. The desired signal arriving in the desired polarization hitting the antenna splits between the RX and AUX ports due to the finite axial ratio. The signal at the AUX port reflects from the reflective termination and then couples into the RX port, interfering with the desired signal at the RX port. The total degradation in the RX antenna gain due to the introduction of the auxiliary port (due to power splitting between RX and AUX ports depending on the axial ratio) and SIC (compared to the case with zero reflection at the AUX port) is theoretically calculated as 0.41 dB based on the analysis in Chapter 2, which compares well with the simulation.

Further, the noise of the reflective termination due to its resistive part leaks into the RX input, forming another degradation mechanism for the RX NF. The NF degradation due to the reflective termination is theoretically calculated as 0.43 dB based on the analysis presented in Chapter 2, consistent with the simulated value of 0.52 dB.

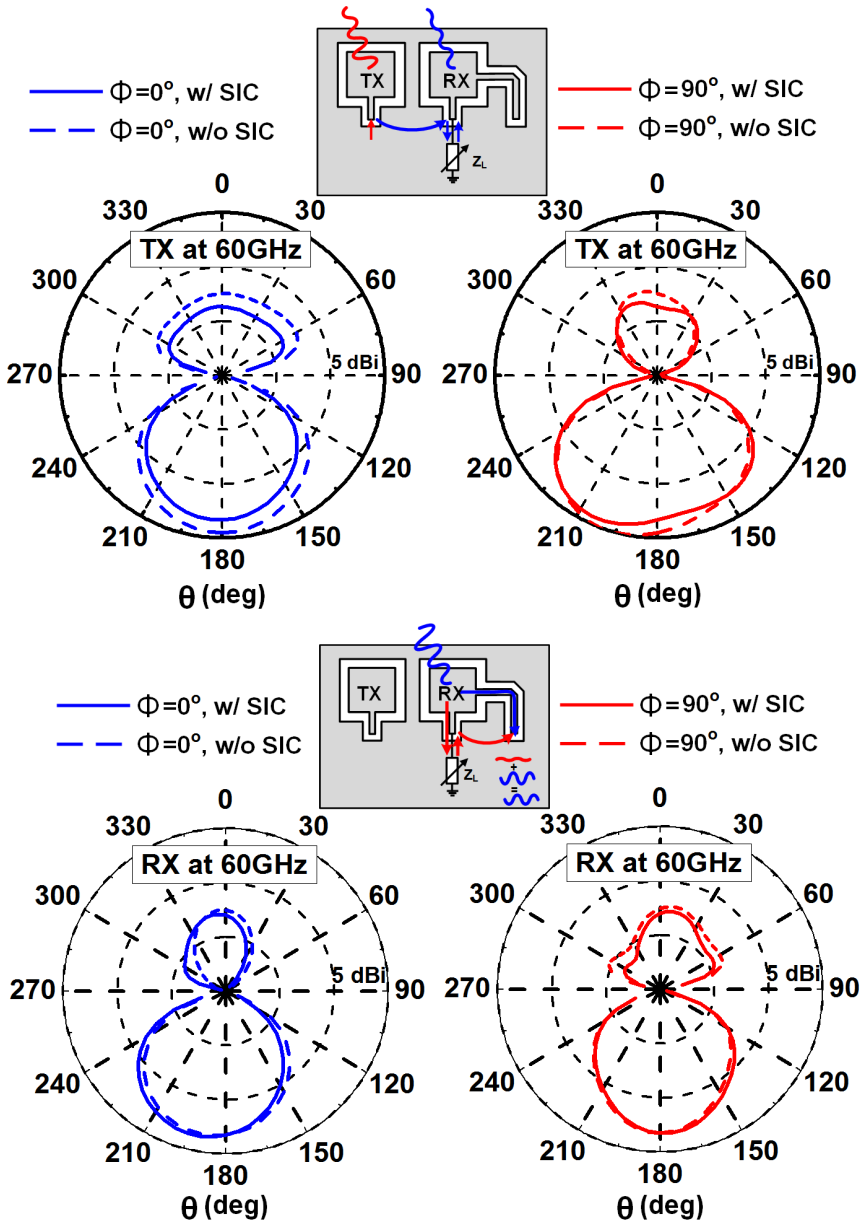

Figure 3.9: TX and RX patterns with and without SIC (simulation). The radiation of the coupled TX signal at the auxiliary port from the RX antenna interferes with the main radiation of the TX signal in the far-field, affecting TX antenna gain. The received signal going into the AUX port reflects from the variable termination and then couples into the RX port, interfering with the desired signal and affecting the RX antenna gain.

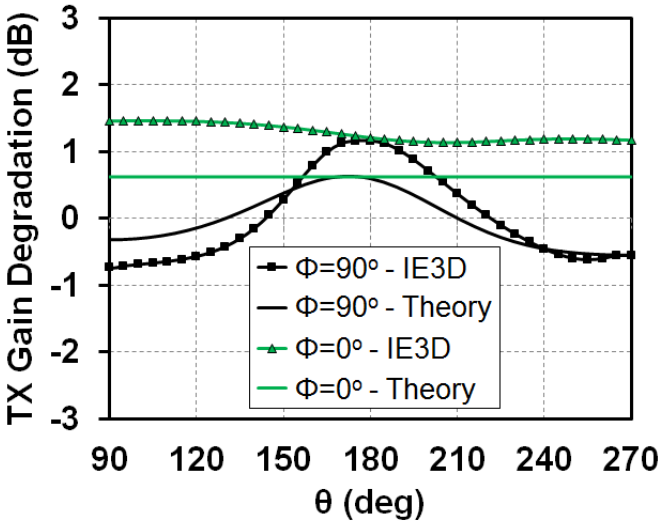

Figure 3.10: Comparison of the simulated TX antenna gain degradation (calculated by subtracting the antenna gain with SIC from the antenna gain without SIC) to the theoretical degradation based on the analysis in Chapter 2.

The penalties on the TX and RX antenna gains are similar to the TX efficiency penalty and NF penalty of RF cancellers and can be reduced by increasing the TX-AUX and RX-AUX isolations, respectively. The noise leakage from the reflective termination is also similar to the NF penalty of RF cancellers and can be reduced by increasing the RX-AUX isolation.

3.3 Implementation

3.3.1 Reflective Termination

The circuit diagram of the reflective termination is shown in Fig. 3.11. The variable R is implemented as a 15μm/40nm body-floating NFET operating in the deep triode region, providing 0.14-44 mS conductance at V_{CR}=0-1 V. A shorted transmission line with a length of 120 μm is employed as the shunt L. An inversion-mode NFET varactor bank consisting of 2x16μm/56nm and 3x16μm/56nm devices serves as the variable capacitance. 56 nm body contacted devices are preferred over 40 nm body-floating counterparts because of their higher tuning ratio. For a 2x16μm/56nm device, the simulated minimum capacitance is 38fF with a tuning ratio of 1.82, and

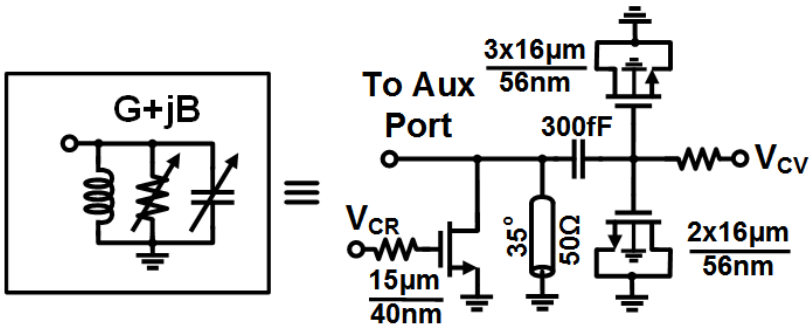

Figure 3.11: Implementation of the reflective termination: variable R and C are implemented as a deep-triode NFET and an inversion-mode NFET varactor bank, respectively. L is implemented as a 120 μm long shunt transmission line.

the quality factor varies from 27 to 10 when when the control voltage, V_{CV}, is swept from 0 to 1.2 V.

3.3.2 RF Canceller

The 3-port capacitive coupler depicted in Fig. 3.12 takes a small copy of the TX signal to feed into the RF canceller. It achieves a simulated -18 to -15.5 dB coupling with an insertion loss less than 0.3 dB over 50-70 GHz.

The RF canceller employs a reflective-type attenuator based on a variable shunt resistor implemented as an NFET operating in the deep triode region with V_{DS}=0V for no power consumption (Fig. 3.13). A 30μm/40nm body-floating NFET provides 6Ω on-resistance at a control voltage of $V_{C,ATT1}$=1.2V and achieves 16 dB attenuation range at 60 GHz. $V_{C,ATT1}$ is applied through a 6kΩ resistance to make the gate float for AC, reducing the loss at $V_{C,ATT1}$=0V (0.7 dB at 60 GHz) [63].

A single-stage RF amplifier implemented in stacked topology follows the attenuator (Fig. 3.13). The stacked topology is chosen to improve the power handling capability by increasing supply voltage to 2.1 V [64] as well as to achieve higher reverse isolation. A small degeneration inductance (TL2) is used to ease the input matching. The amplifier, biased at a current density of 0.4 mA/μm, provides a small-signal gain of 12 dB in simulation.

Fig. 3.14 shows the circuit diagram of the RTPS consisting of a 3 dB quadrature broadside coupled-line coupler and two identical reflective CLC terminations. Vertically-coupled microstrip

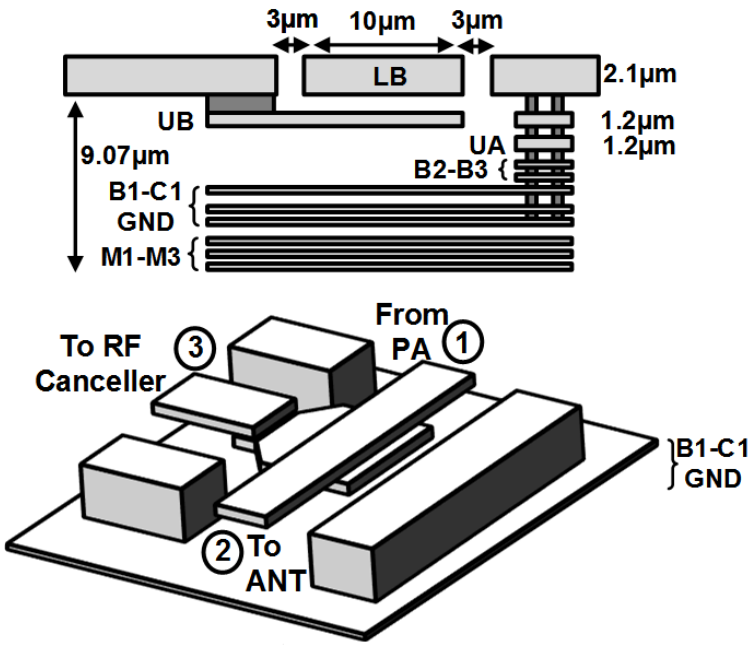

Figure 3.12: Implementation of the blocks in the RF canceller: 3-port capacitive coupler. All transmission lines have 50 Ω characteristic impedance.

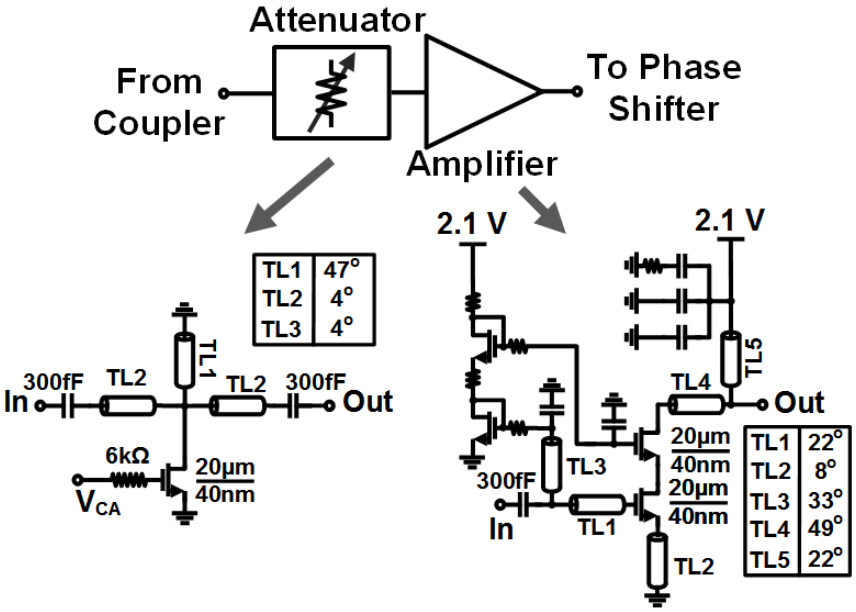

Figure 3.13: Implementation of the blocks in the RF canceller: Variable gain amplifier consisting of the 16 dB reflective-type attenuator followed by an RF amplifier. All transmission lines have 50 Ω characteristic impedance.

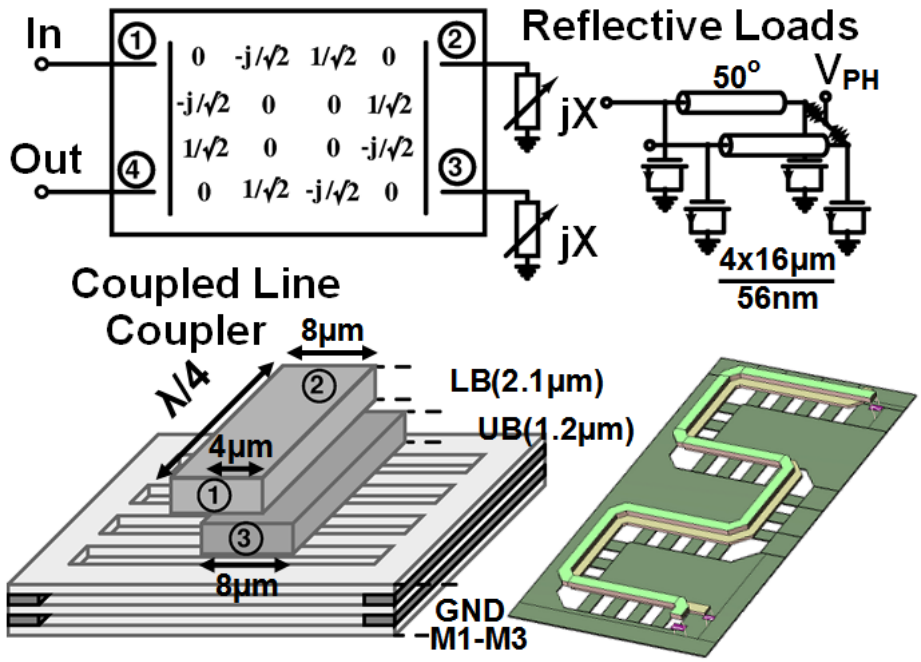

Figure 3.14: Implementation of the blocks in the RF canceller: Reflection-type phase shifter (RTPS).

lines are implemented using the top two metal layers to reduce the loss. Slow-wave technique (10μm wide slots separated by 10μm spacing in the ground plane) and asymmetry (4μm offset) between the coupled lines are introduced in the coupler as additional degrees of freedom to simplify the design procedure, allowing control of odd and even mode impedances independently, following a similar procedure described in Appendix A. 4$\times$16μm/56nm inversion-mode NFET varactors are employed in the reflection termination, resulting in a simulated phase range of 210° with a loss variation of 4.5-8.5 dB at 60 GHz.

The 0/180° PIA is derived from the RF amplifier by adding an additional cascode transistor to commutate the current at the cascode node (Fig. 3.15). The PIA is followed by a vertically coupled transformer balun. The balanced and unbalanced coils are implemented in a stack of UB and UA and LB (details are shown in Fig. 3.15). 58 fF capacitors are used in shunt and series at the balun input and output for matching to 50 Ω. The center-tap is grounded to reduce the phase imbalance. The simulated phase and amplitude imbalances are less than 1.6° and 0.5 dB over 55-65 GHz, respectively. Another reflective-type attenuator with 16 dB attenuation range is

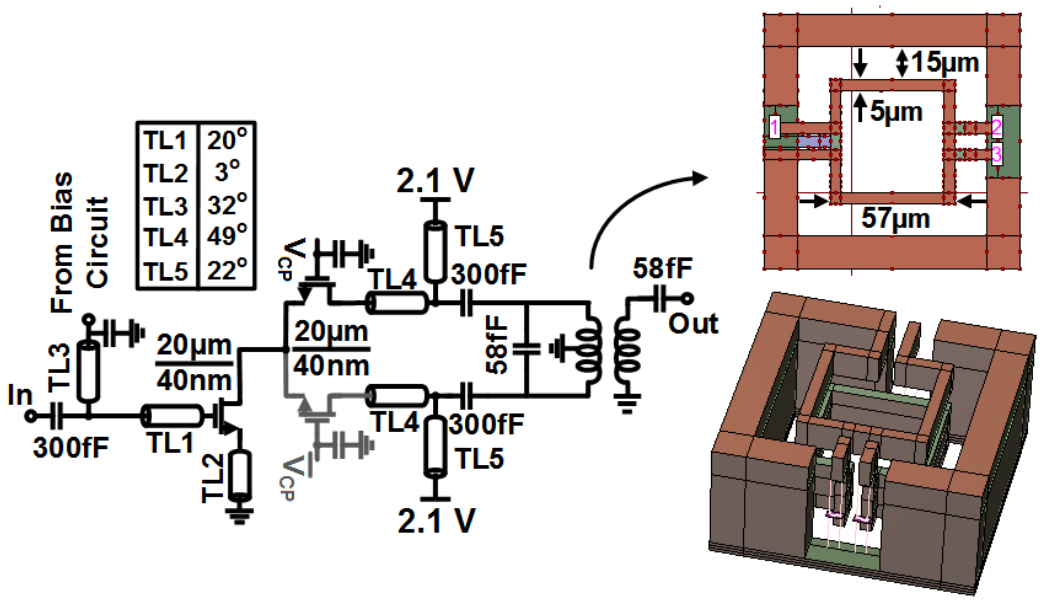

Figure 3.15: Implementation of the blocks in the RF canceller: Phase-inverting amplifier (PIA). All transmission lines have 50 Ω characteristic impedance.

placed after the PIA.

The RF canceller provides 390° phase and 32 dB gain control range in simulation. When the RF canceller is configured as shown in the configuration-3 of Fig. 3.3, the simulated NF and IIP_3 of the canceller are 15.1 dB and 14.1 dBm at 60 GHz, respectively, consistent with the system level analysis.

3.3.3 Transmitter and Receiver

Fig. 3.16(a) depicts the two-stage Class-E-like PA implemented by stacking two 4×16μm/40nm floating-body devices to increase voltage swing at the load. Device sizes, supply, bias voltages and gate capacitor values are selected based on the theoretical analysis and considerations described in [64,65]. A multiplicity-based device layout is used to keep a good balance between f_{max} and f_T. The PA achieves a simulated saturated output power of +16 dBm with 27.4% PAE at 60 GHz.

The BPSK modulator (Fig. 3.16(b)) is nothing but the PIA described earlier operating in dynamic mode with a 1.2 V supply. An inverter chain data buffer sized with a fanout of 4 drives the switching transistor pair whereas the LO signal is applied to the common source device. A

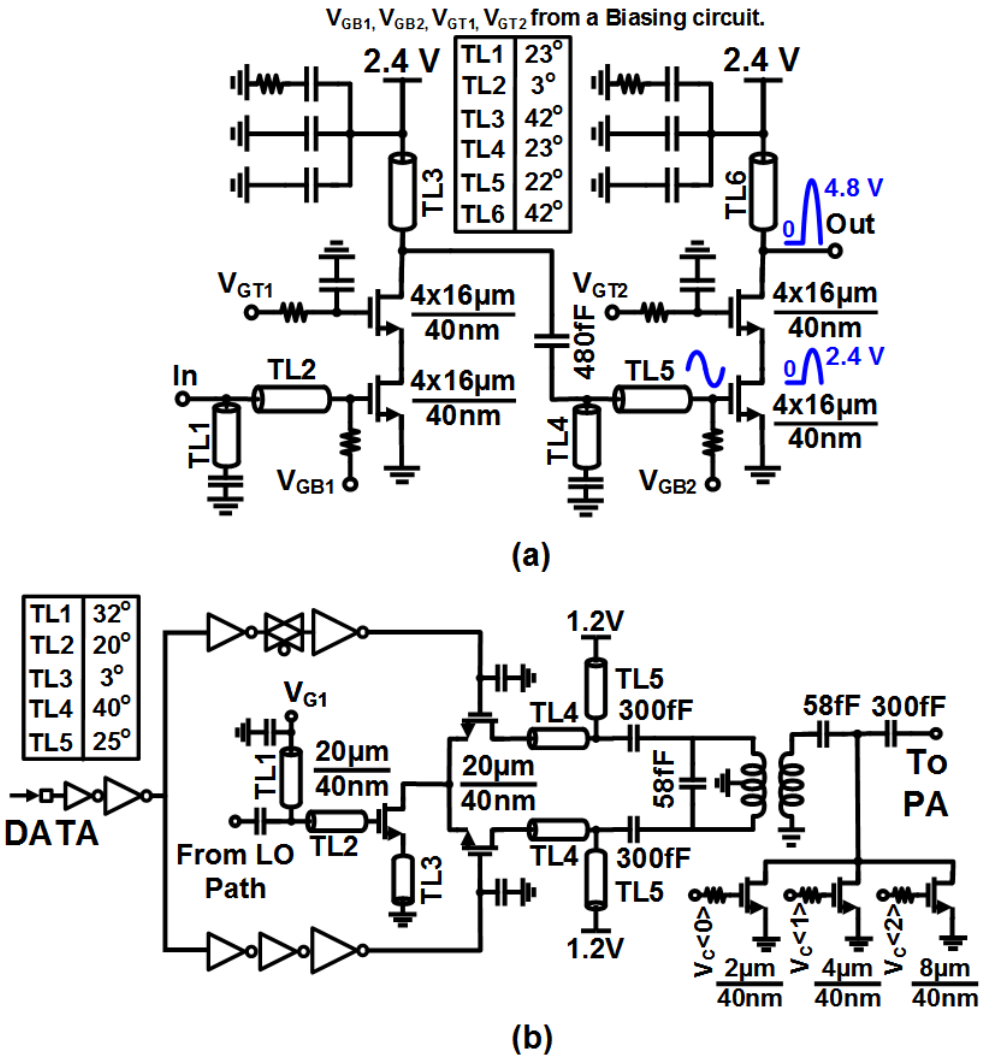

Figure 3.16: Transmitter implementation: (a) PA, and (b) BPSK modulator followed by the 3-bit attenuator. All transmission lines have 50 Ω characteristic impedance.

3-bit attenuator consisting of shunt NFET resistors is included at the BPSK modulator output for transmitter power control.

The LNA is implemented using two inductively-degenerated cascode stages, shown in Fig. 3.17(a). Each stage is biased at a current density of ≈0.25 mA/μm for minimum NF. A simulated gain and noise figure of 18.5 dB and 2.6 dB are achieved at 60 GHz, respectively. The simulated $IIP_{3,LNA}$ is -10 dBm, consistent with the system level analysis. The VGA implementation consists of a 2-bit attenuator similar to the one used at the BPSK modulator output and an RF amplifier similar to the one in the RF canceller but with a reduced supply voltage of 1.2 V. The I/Q down-conversion mixers are designed using a half-Gilbert cell topology with current-stealing to improve the conversion gain and to reduce the noise from the switching pair as well as the required LO power [66] (Fig. 3.17(b)). Similar to the LNA first stage, the trans-conductance stage of the mixer is designed for minimum noise figure (inductive degeneration and current density of ≈0.25 mA/μm). The current stealing shunt transmission line $TL2$ steals one-third of the DC current (2mA out of 6mA) and resonates the parasitic capacitance at the drain of the common source device. Fig. 3.17(c) shows the circuit diagram of the baseband amplifier consisting of a simple differential pair first stage and an open-drain last stage to ease interfacing with measurement equipments. 5-bit NFET resistance bank is included in the first stage for gain control. The IIP_3 of the VGA, I/Q mixers and baseband amplifiers is simulated as -14.9 dBm in the highest gain setting, significantly larger than the $IIP_{3,RRX}$ calculated in the system level analysis.

The amplifiers and attenuators in the RF canceller and BPSK modulator are reused for the LO distribution, and a simple balanced frequency doubler is included at the input. The LO path can deliver up to 7 dBm in simulation to the BPSK modulator and IQ down-conversion mixers.

3.4 Measurements

The transceiver IC is fabricated in an IBM 45 nm SOI CMOS process which has an f_{max} of ≈250 GHz for 40 nm floating-body devices [64, 67] and an 11-metal back-end. Fig. 3.18 shows a micro-photograph of the full-duplex transceiver IC and occupies an area of 1.3 mm×3.4 mm. Internal pads are placed at the doubler output, PA input and RX VGA output to evaluate the performance of some key sub-blocks separately. A transceiver chip is laser trimmed to create an

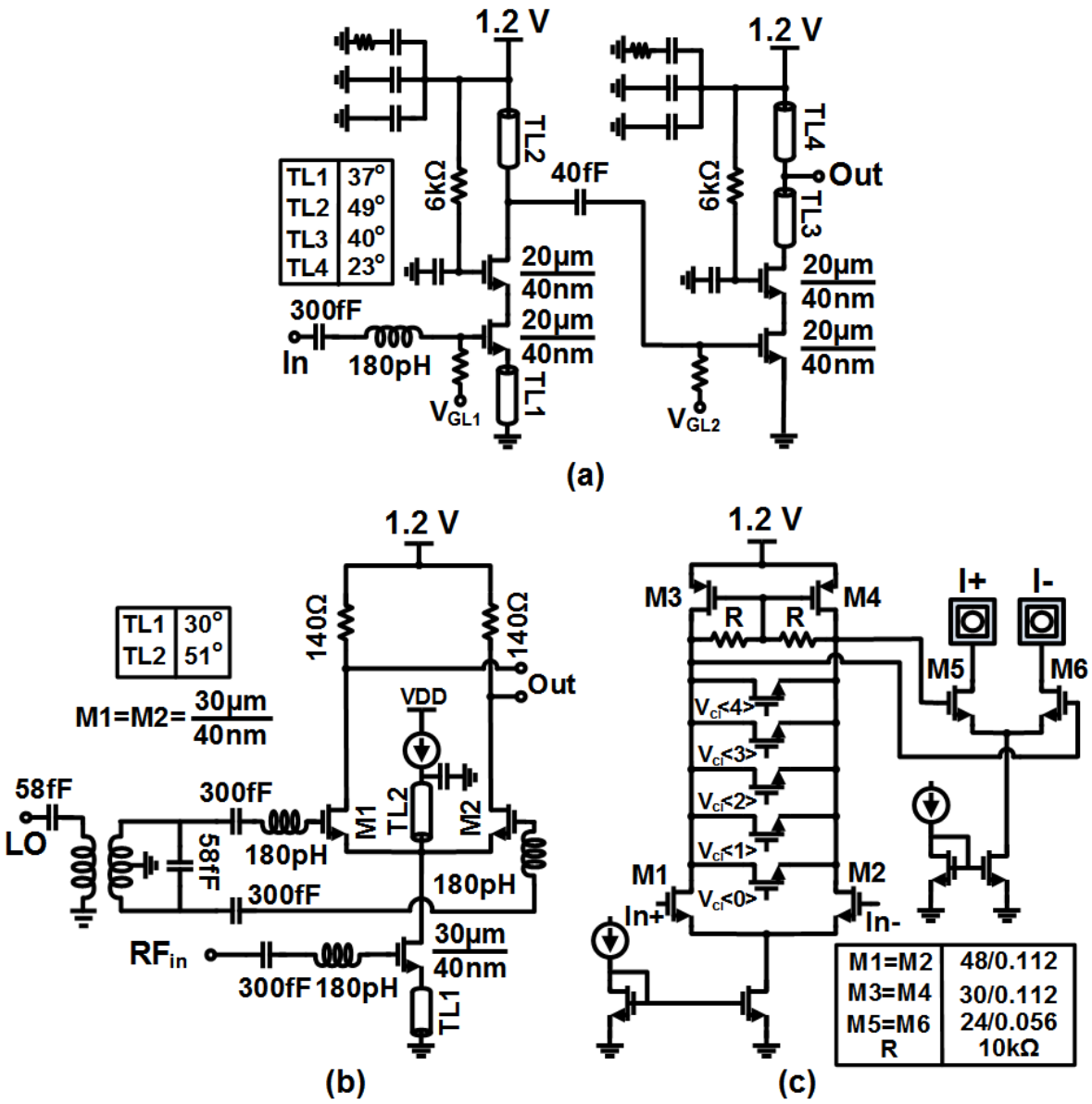

Figure 3.17: Receiver implementation: (a) LNA, (b) current-stealing single-balanced mixer, and (c) baseband amplifier.

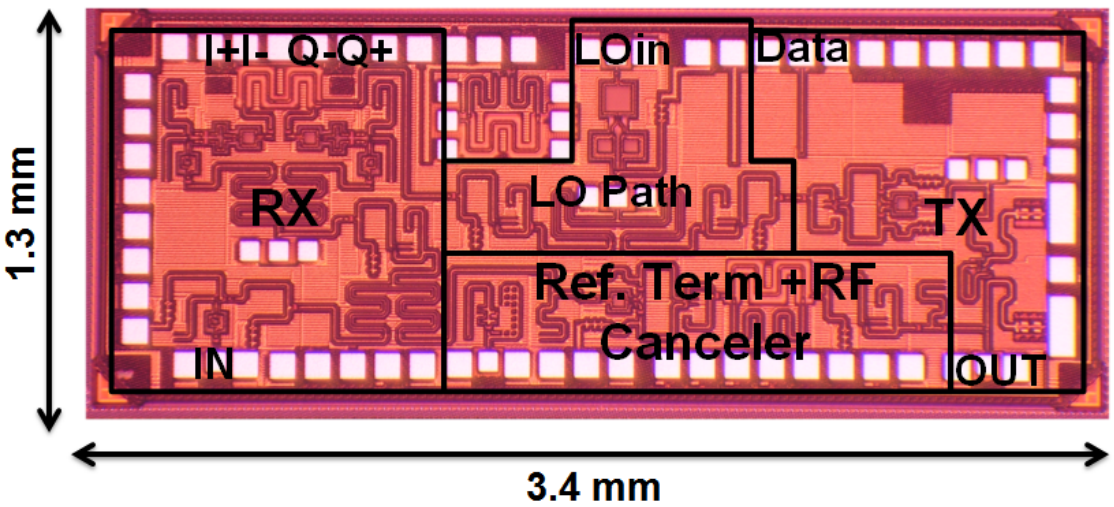

Figure 3.18: Chip microphotograph of the 60 GHz 45 nm SOI CMOS fully-integrated full-duplex transceiver IC.

LNA, Wilkinson and RX VGA break-out, an RF canceller and a PA break-out whose test results will be presented next.

3.4.1 Break-out Measurements

The LNA-Wilkinson-VGA break-out is tested through RF probing using a chip-on-board based setup while the cancellation path is powered on with the lowest attenuation (highest gain) setting, presenting ≈50 Ω at the third Wilkinson port (Fig. 3.19(a)). The connection of the VGA to the Wilkinson-based I/Q splitter is laser-trimmed to eliminate its loading. Fig. 3.19(b) shows the measured S-parameters of the LNA-Wilkinson-VGA break-out. The measured peak gain is 23.6 dB at 62.5 GHz with 5.6 dB gain control across 2 bits. The measured results agree well with the simulations, with a 2.5 GHz upward shift which is attributed to overestimation of capacitive parasitics at the design time as well as BEOL process variations.

The RF canceller phase and gain control range are evaluated from the TX output pad to the internal pad at the RX VGA output while the LNA and PA are powered on (Fig. 3.20(a)). Small-signal measurements of the RF canceller break-out, shown in Fig. 3.20(b) along with simulated results as dashed lines, display a peak gain of 1.8 dB at 59 GHz for an RTPS phase control voltage of $V_{C,PH}$=0V and attenuator control voltages of $V_{C,ATT1}$=$V_{C,ATT2}$=0V. An analog gain control range

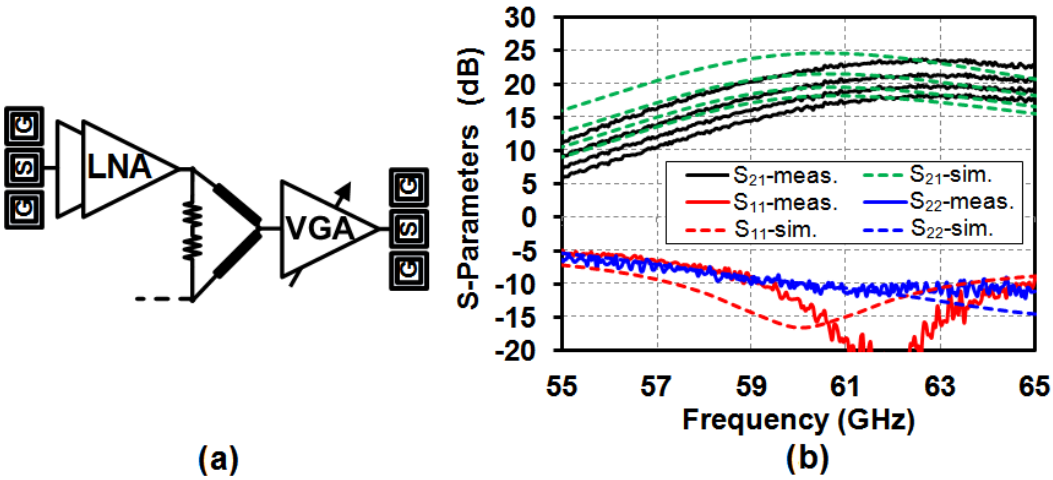

Figure 3.19: (a) Measurement setup, (b) measured and simulated S-parameters of the LNA, Wilkinson and VGA break-out through an internal test pad. The VGA provides 5.6 dB gain control across 2-bits .

of 28 dB is achieved by varying $V_{C,ATT1}$ and $V_{C,ATT2}$ from 0 to 0.8V (32 dB gain range by varying $V_{C,ATT1}$=$V_{C,ATT2}$ up to 1.2V). Fig. 3.20(c) shows the RTPS phase range and loss variation with $V_{C,PH}$ at 60 GHz at the minimum attenuation setting of the RF canceller, $V_{C,ATT1}$=$V_{C,ATT2}$=0V. The RTPS provides 206° analog phase range with 15 dB loss variation. The measured RTPS phase range compares well with the simulation and the discrepancy between the simulated and measured loss variation is attributed to an asymmetry in the layout which causes destructive interference. The large loss variation across RTPS settings is not a significant concern in this case, since the RTPS is employed in a chain which actually requires attenuation. In other words, the excess loss for some phase settings can be compensated for in the variable attenuators. Additionally, the PIA in the RF canceller provides a discrete phase shift of 180±2° over 55-65 GHz with an amplitude imbalance less than 1 dB (Fig. 3.20(d)). The DC power consumption of the RF canceller is 44 mW.

The two-stage, two-stacked Class-E-like PA with the 18 dB capacitive coupler at the output (simulated insertion loss of 0.3 dB at 60 GHz) is also characterized (Fig. 3.21(a)). The cancellation path is powered on with the lowest attenuation setting to present ≈50 Ω at the coupled port in Fig. 3.21(a). Fig. 3.21(b) and Fig. 3.21(c) present the small-signal and large-signal measurement results. The PA has a peak small-signal gain of 20.6 dB at 59 GHz, and a saturated output power of 15.4 dBm with 25.5% drain and 24.4% power added efficiencies at 60 GHz. The saturated output

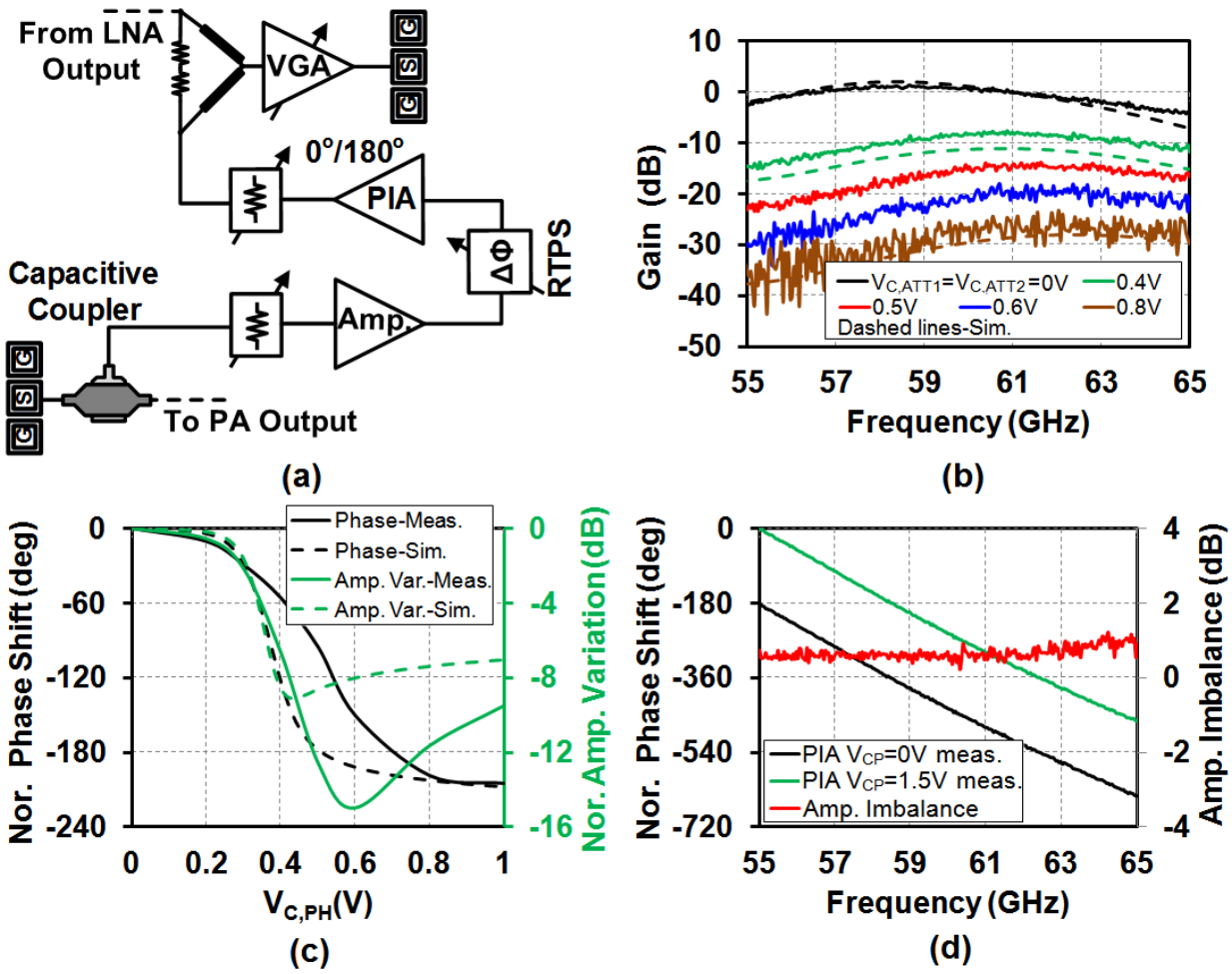

Figure 3.20: Small-signal measurements of the RF canceller: (a) measured break-out diagram, (b) measured and simulated (dashed lines) gain and gain control across frequency ($V_{C,PH}$=0 V), (c) normalized phase shift and amplitude variation versus RTPS control voltage $V_{C,PH}$ at 60 GHz ($V_{C,ATT1}$=$V_{C,ATT2}$=0 V), and (d) normalized phase shift versus frequency for both PIA settings and amplitude imbalance between the two PIA settings.

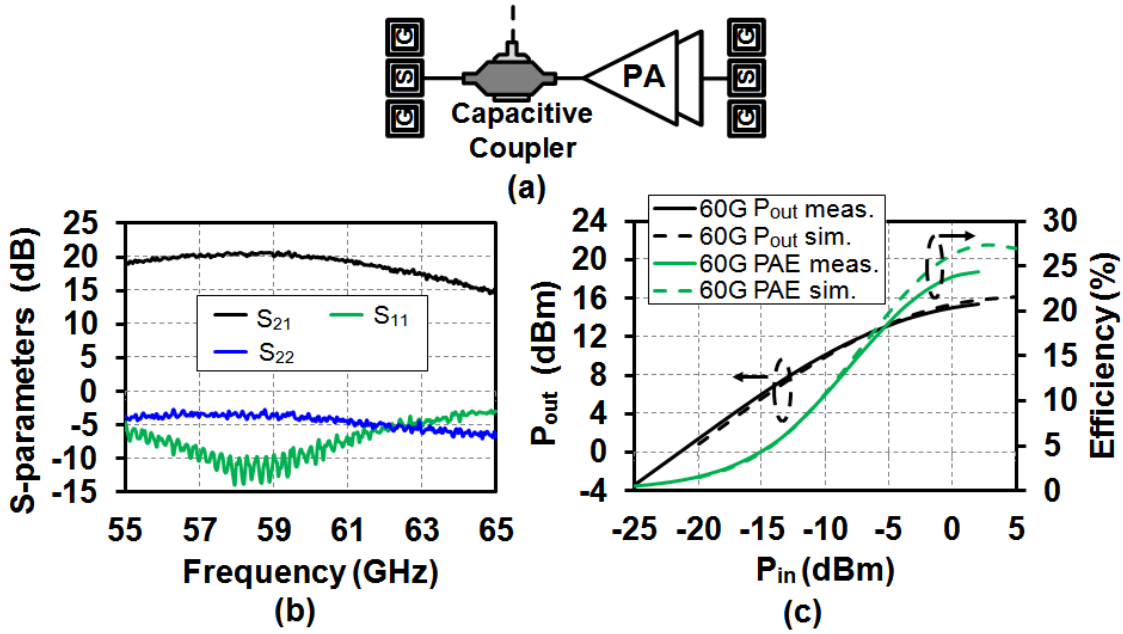

Figure 3.21: (a) Measured PA break-out diagram consisting of the two-stage two-stacked Class-E-like PA and capacitive coupler. (b) Small-signal S-parameters. (c) Measured and simulated output power and PAE versus input power at 60 GHz.

power is better than 13.7 dBm over 56-65 GHz. The large signal simulation results follow the measurements quite well.

3.4.2 Transmitter and Receiver Measurements

Static measurements of the transmitter are performed by applying a constant digital data stream to the BPSK modulator (transmitting all zeros). Fig. 3.22(a) shows the TX output power versus the LO input power for different LO frequencies. A peak TX saturated output power of 15 dBm is achieved at 57 GHz with a peak system drain efficiency of 15.3%, including the doubler which is shared by the RX path. The LO-TX conversion gain, presented in Fig. 3.22(b), is better than 15 dB at an input power level of -6.5 to -4 dBm over 57-64 GHz. The measured TX saturated output power shown in Fig. 3.23 is more than 11.5 dBm from 56 to 66 GHz.

Fig. 3.24(a) shows the RX power conversion gain in the four IEEE 802.11ad channels for highest, lowest and two intermediary selected gain settings with an LO power of 5±0.3 dBm at the doubler input. The peak RX conversion gain is 40 dB in channel-3 with a 3 dB bandwidth of 2.2 GHz and

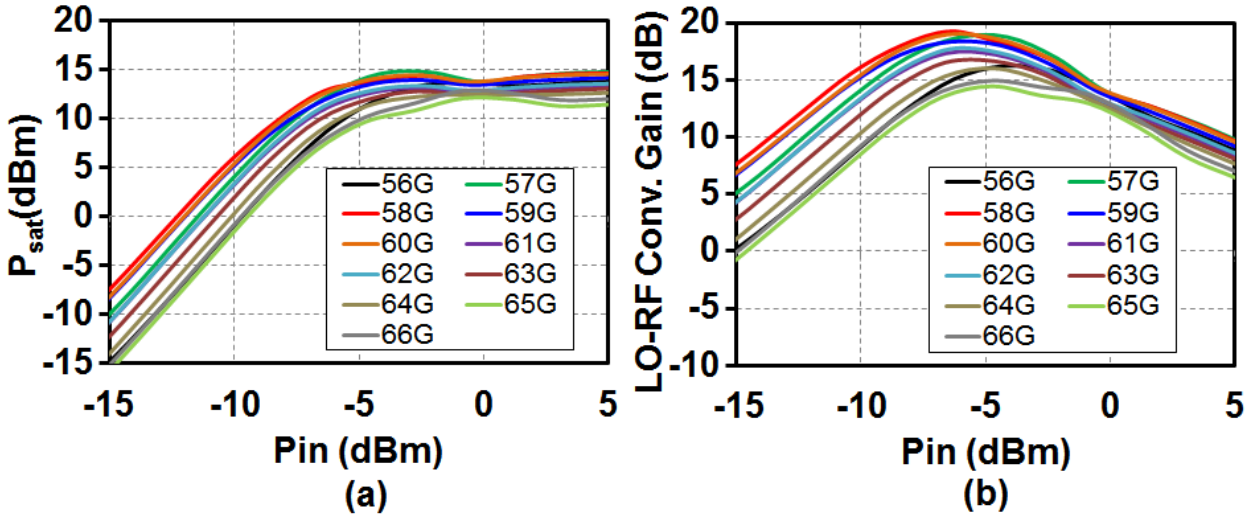

Figure 3.22: TX CW large-signal measurements (transmitting all 0s): (a) TX output power versus LO input power. (b) LO-to-RF conversion gain of the transmitter versus LO input power.

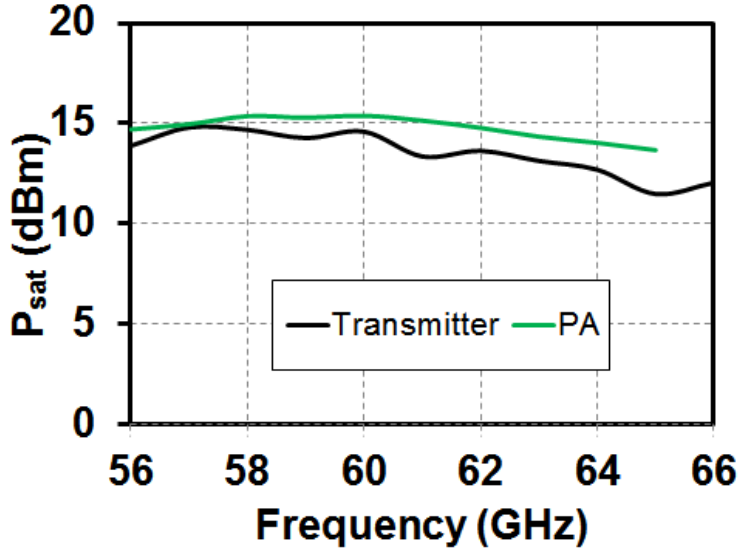

Figure 3.23: PA and TX saturated output power versus frequency.

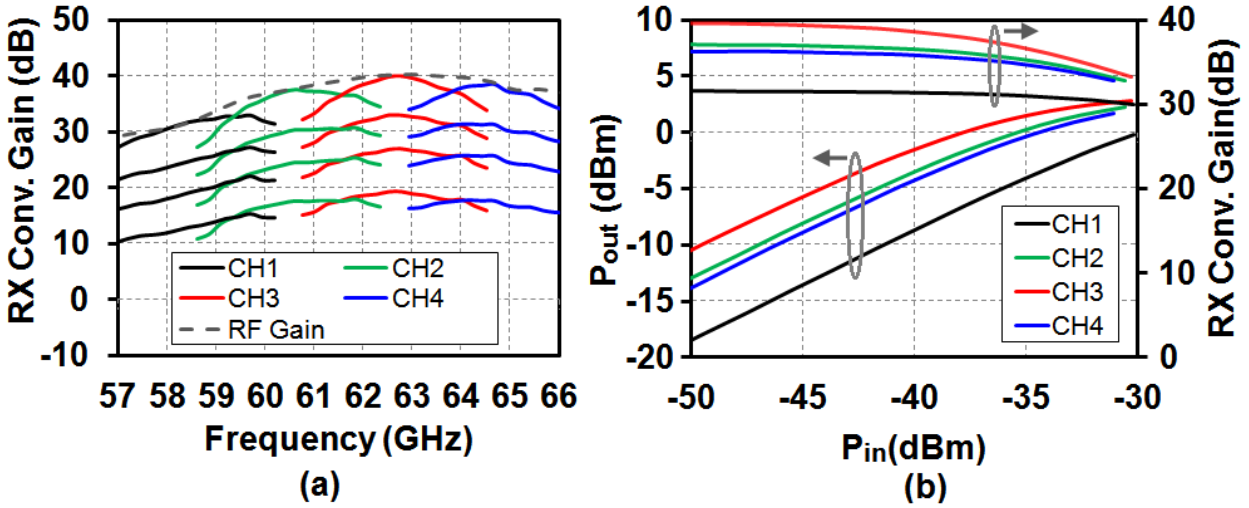

Figure 3.24: RX measurements in all 4-IEEE channels: (a) RX conversion gain for highest, lowest and two intermediary gain settings and peak RF gain across frequency. (b) Baseband output power and RX conversion gain versus RF input power for highest gain setting.

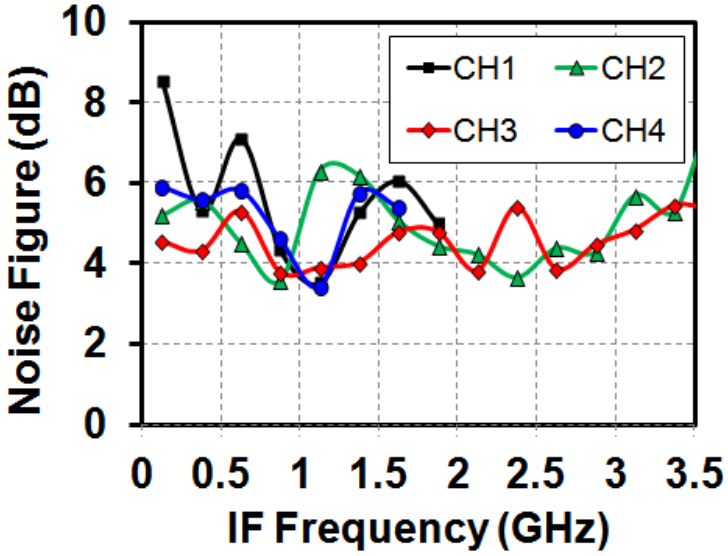

Figure 3.25: RX noise figure versus IF frequency for highest gain setting.

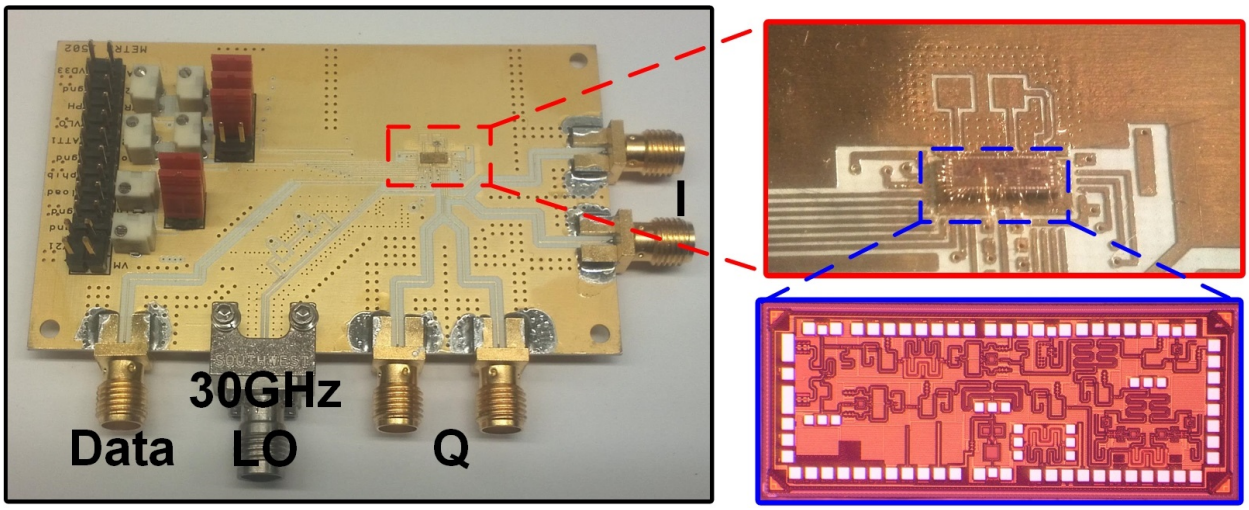

Figure 3.26: Photo of the mm-wave PCB used for system level measurements.

gain control range of 20.8 dB. The gain control range is higher than 18 dB in all the channels. The RF gain across frequency is measured by sweeping RF and LO together to keep IF fixed at 120 MHz and superimposed in Fig. 3.24(a). The receiver draws 56 mA from a 1.2 V supply. Fig. 3.24(b) presents the receiver output power and conversion gain versus the input power in high-gain mode in the four channels. The RX has an input-referred 1 dB compression point of -32 dBm, -38 dBm, -39.8 dBm and -36.6 dBm in channels 1, 2, 3 and 4, respectively. The RX noise figure shown in Fig. 3.25 is measured using gain method (cold noise) in high-gain mode and a state-of-the-art NF as low as 4 dB is achieved in channel-3.

3.4.3 System Level Measurements

Fig. 3.26 shows a photo of the mm-wave PCB with the 60 GHz antennas used for cancellation and link measurements. The transceiver die directly sits on the PCB without cavity and is thinned down to 100μm to reduce the length of the 30 and 60 GHz wirebonds. Additionally, three wires per mm-wave pad are bonded to reduce the wirebond inductance further (estimated L_{WB} is ≈100-150pH and forms an artificial transmission line with 25 fF shunt on-chip and on-PCB pad capacitances).

A pseudorandom binary sequence (PRBS) with a length of 2^{31}-1 from an Anritsu MP1763B pulse pattern generator (PPG) is applied to the transmitter and a loop-back test is performed through the cancellation path. Fig. 3.27 shows the 5 Gbps eye-diagram.

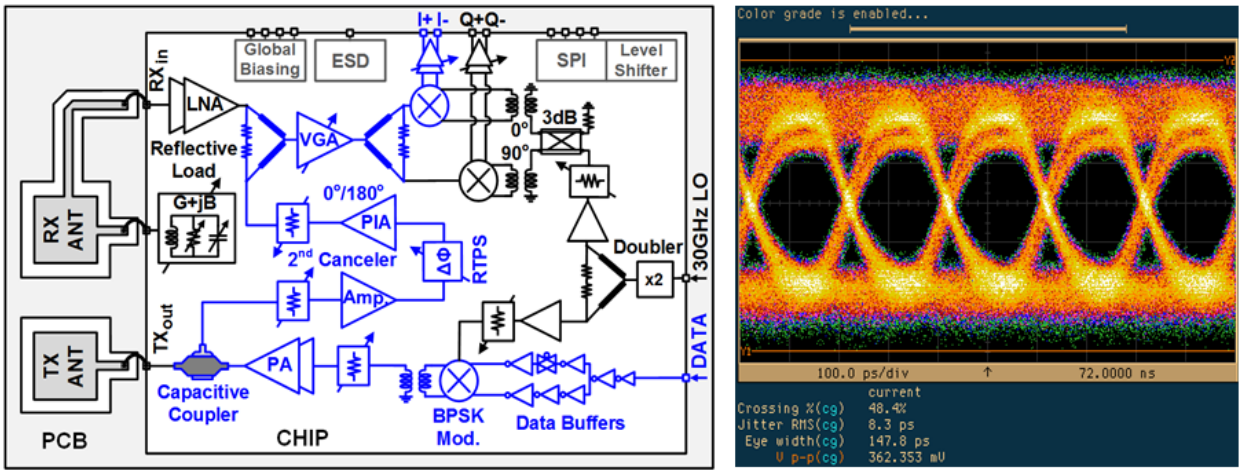

Figure 3.27: TX-RX 5 Gbps BPSK loopback test through the cancellation path.

The self-interference at the receiver output is characterized across frequency. The antenna and RF cancellation are configured together manually in the measurement. Dynamic SIC adaptation is beyond the scope of this work. Controlling antenna and RF cancellation simultaneously gives flexibility in setting the SIC and SIC BW together. Fig. 3.28(a) shows the total SI suppression referenced to the TX output (P_{TX}=11±0.4 dBm). Another board consisting of only cross-polarized TX and RX antennas is used to measure the nominal TX-to-RX isolation. With antenna and RF cancellation together, a total SI suppression of >70 dB is achieved over a cancellation bandwidth of 1 GHz centered at 59 GHz. Fig. 3.28(b) shows the individual contribution of the antenna and RF cancellation. Since antenna and RF cancellers are controlled together, the values on Fig. 3.28(b) cannot be interpreted as the maximum achievable antenna and RF cancellation individually. Effect of environmental reflections on SI suppression is investigated by bringing a copper reflector close to the transceiver PCB[4]. The reflector 1.5 cm away from the antennas as shown in Fig. 3.28(b) degrades the SI suppression by 10 dB from 58.5 to 59.5 GHz. The performance can be recovered by only reconfiguring the antenna cancellation while leaving the RF canceller untouched, verifying its capability to combat the environmental reflections. It should be noted that higher propagation losses at mm-wave frequencies work in favor of full-duplex since it alleviates the effect

[4]Wave reflection arises as a result of mismatch between the plane wave impedance (Z_i≈377Ω) and the reflector's surface impedance. Copper has a very high conductivity which leads to a very low surface impedance, making it a very good reflector. Therefore, using copper enables us to test SIC under a very stringent condition [68].

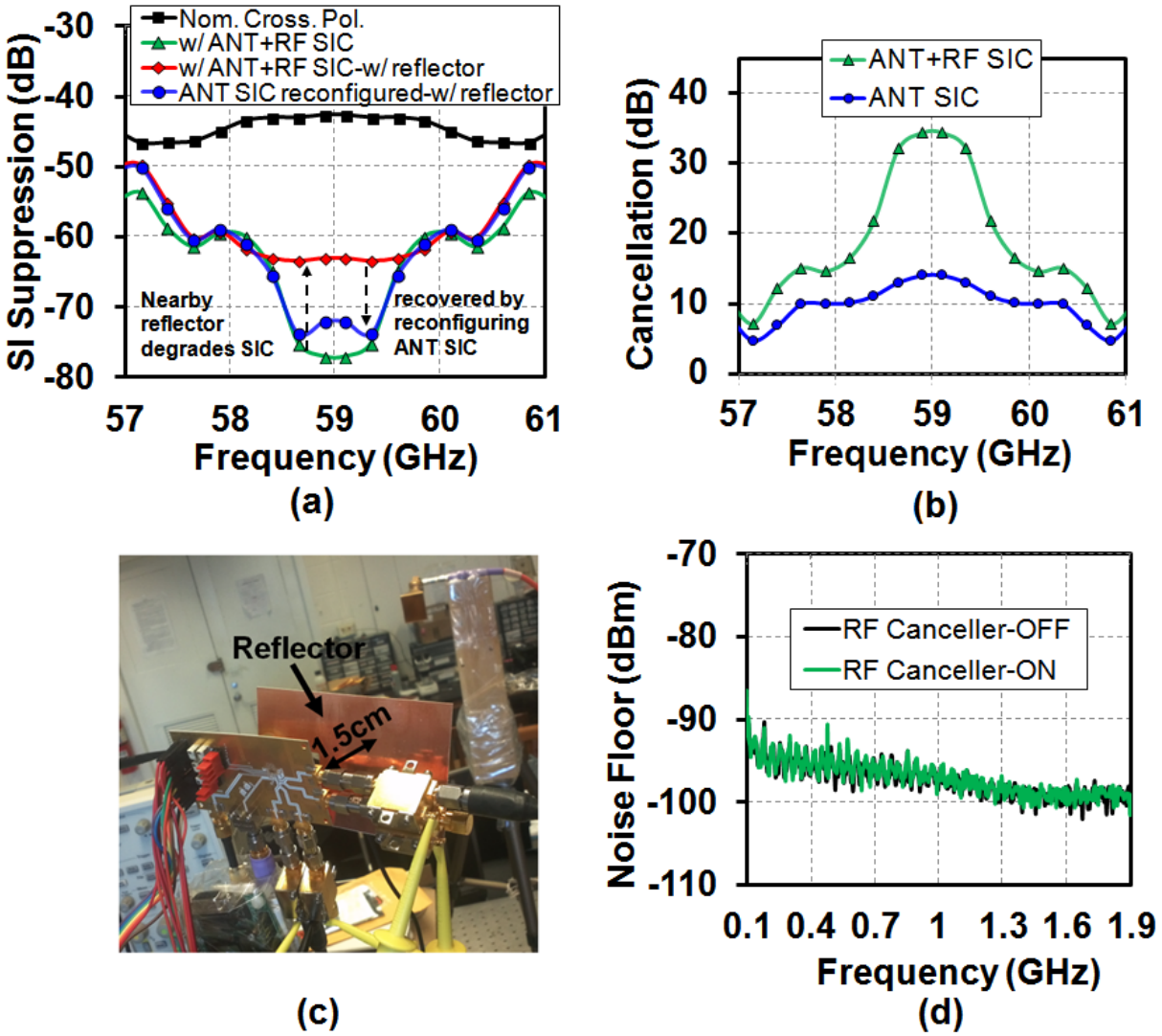

Figure 3.28: (a) Measured SI suppression across frequency with antenna and RF cancellation configured. (b) Measured antenna and RF SIC. (c) A reflector is brought 1.5 cm away from the antennas to measure the effect of environmental reflections on SIC. SI suppression degrades due to the reflector, but it can be recovered by reconfiguring the antenna cancellation. (d) RF canceller's effect on the receiver output noise (RBW=51kHz).

of environmental reflections on SI suppression. Fig. 3.28(c) shows that the RX output noise floor does not change when the RF canceller is activated (the transmitter was off in this measurement), in agreement with the system-level analysis.

Finally, a simple same-channel full-duplex link is demonstrated over 0.7 m (the demo video is available in [69]). Fig. 3.29(a) depicts the demonstration setup. A 24 dBi horn antenna transmits a CW signal from an Anritsu MG3697C at 59.34 GHz with an effective isotropic radiated power (EIRP) similar to our transmitter (≈20 dBm). Our transmitter is configured for highest CW output power setting, resulting in an estimated EIRP of 18.3 dBm (P_{TX}=14.3 dBm, simulated TX antenna gain of G_{TX}=4.5 dBi and assuming a chip-to-PCB transition loss of 0.5 dB based on EM simulation). Our transceiver transmits a 1 Gbps BPSK signal (SI) with an LO frequency of 59.24 GHz (100 MHz offset between the desired CW signal and LO). The RX output is monitored and captured using an Agilent 54855A oscilloscope with 6 GHz BW, essentially an 8-bit 20GSPS ADC. In the absence of antenna and RF SIC, the RX output is dominated by SI (Fig. 3.29(b)). Antenna and RF SIC enable the discerning of the 100 MHz desired CW signal in Fig. 3.29(c). In this plot, the captured signal is shifted by half-cycle and superimposed to show the signal quality visually like an eye-diagram. Digital SI cancellation (DSIC) is performed on the digitized signal in MATLAB using a 100-taps adaptive LMS filter with varying step size, μ, to reduce the settling time of the filter coefficients. To this end, our code initially uses a large step size of μ=0.8 during the first 80 k samples for coarse estimation of the filter weights, and as the weights converge to their final values, μ is dropped by half for every subsequent 20 k samples. The LMS filter settles in a total of 320 k samples, corresponding to a settling time of 16μs. As can be seen in Fig. 3.29(d), DSIC further suppresses the SI, resulting in an even cleaner received signal in Fig. 3.29(d) with an SINDR of 7.2 dB. To the best of our knowledge, this work achieves the highest integration level among full-duplex transceivers irrespective of the operation frequency and demonstrates a simple FD link for the first time using IC technology.

3.4.4 Performance Summary and Comparison

Table 3.1 summarizes the transceiver performance. Table 3.2 compares this work to other published state-of-the-art 60 GHz CMOS transceivers. It is worth repeating that, different from the other 60 GHz systems which are generally mature phased-array systems, this work brings a new concept

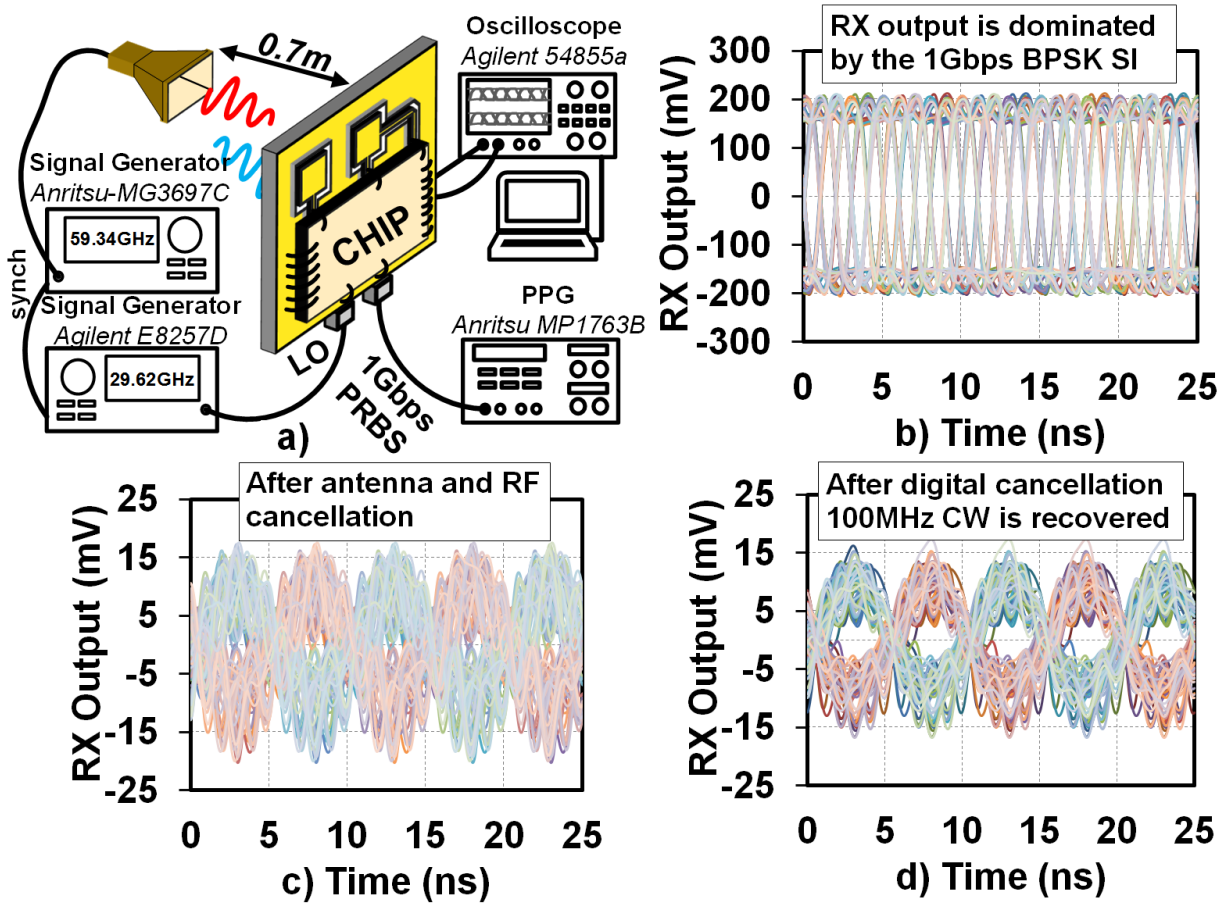

Figure 3.29: (a) Full-duplex link setup. A CW signal at 100 MHz offset from the LO frequency is transmitted as the desired signal with a similar EIRP to our transmitter whereas the 60 GHz transceiver transmits a 1 Gbps BPSK signal. (b) RX output is dominated by 1 Gbps BPSK SI when TX is on without SIC. (c) Desired signal is captured with some residual SI when antenna and RF SIC are engaged. (d) Desired signal is captured with a SINDR of 7.2 dB after digital SIC.

Table 3.1: Summary of full-duplex transceiver performance

Implementation	**Technology**	45nm SOI CMOS
	Chip Area	1.3mm x 3.4mm
Transceiver Metrics	**Frequency**	57-66GHz
	Peak RX Conv. Gain	40dB (IEEE Channel-1) 32.7dB (IEEE Channel-2) 37.7dB (IEEE Channel-3) 38.2dB (IEEE Channel-4)
	RX Gain Control Range	~18dB (IEEE Channel-1) ~20dB (IEEE Channel-2) ~21dB (IEEE Channel-3) ~21dB (IEEE Channel-4)
	RX IP1dB (High Gain Mode)	-32dB (IEEE Channel-1) -38dB (IEEE Channel-2) -40dB (IEEE Channel-3) -37dB (IEEE Channel-4)
	RF NF	4dB
	TX Output Power	11-15dBm @ 56-66GHz
	Peak TX Efficiency	15.3% @ 57 GHz
	Data Rate	>5Gbps[1]
Full-Duplex Metrics	**On-Chip ANT+ RF SI Suppression**	>70dB (ANT+RF)
	SIC BW	1GHz @ 59GHz
	TX ANT Gain Degradation Due to ANT SIC	1.1dB @ 60GHz (Simulated)
	RX ANT Gain Degradation Due to ANT SIC	0.18dB @ 60GHz (Simulated)
	RX NF Degradation Due to RF SIC	Negligible (Measured)
	RX NF Degradation Due to ANT SIC	0.52dB @ 60GHz (Simulated)
	Full-Duplex Link	0.7m (SINDR=7.2dB)[2]
Power Consumption	**TX+TX-side LO Dist**	206mW[3]
	RX+RX-side LO Dist	111mW
	RF Canceller	44mW

[1] Loop-back test through the RF Canceller. A 1.485Gbps video stream has been sent through the transceiver in half duplex mode over 1m link distance [44].
[2] In conjunction with digital cancellation in MATLAB
[3] Includes doubler power consumption

Table 3.2: Comparison to state-of-the-art 60 GHz CMOS Transceivers

	This Work	[10]	[12]	[14]	[15]	[16]
Technology	45nm SOI CMOS	65nm CMOS	40nm CMOS	90nm CMOS	65nm CMOS	40nm CMOS
Chip Area	1.3mm x 3.4mm	~8.6mm x8.1mm	5.6mm x4.7mm	~3.75mm x3.6mm	4.2mm x4.2mm	12.5mm[2]
Number of Elements	1TX/1RX	32TX/32RX	16TX/16RX+1	1TX/1RX	1TX/1RX	4TX/4RX
Duplexing	Half/Full-Duplex	Half-Duplex	Half-Duplex	Half-Duplex	Half-Duplex	Half-Duplex
RX Single-Element Conv. Gain	40dB	—	—	60dB	23dB	45dB
RX Single-Element NF	4dB	<10dB	<10dB (2dB switch)	7.1dB	<4.9dB	7.9-8.7dB (SSB)
TX Single-Element Output Power	+15dBm	+9dBm[3]	>+8dBm	+8dBm	+5.6dBm	+10.8dBm[3](Class-A) +8dBm[3](Class-AB)
TX Total EIRP	+18.3dBm (Peak CW)	+28dBm (at -19dB EVM)	+24dBm (at -23dB EVM)	+8.5dBm (at -22dB EVM)	—	—
Peak TX Efficiency	15.3%[5] / 23%[6]	22% (PA Efficiency)	<7.4% (PA at OP_{1dB})	16.4% (PA) 1.7% (entire TX[6])	—	6.6%[7] (Class-A) 4.3%[7] (Class-AB)
Data Rate	>5Gbps[1]	3.8Gbps@50m	4.6Gbps@10m 3Gbps@20m	1.8Gbps@0.4m	3.1Gbps@1.8m (QPSK) 6.3Gbps@0.05m (16-QAM)	3.5Gbps@3.6m (QPSK) 7Gbps@0.7m (16-QAM)
SI Suppression	>70dB (ANT+RF)	NA	NA	NA	NA	NA
SIC BW	1GHz @ 59GHz	NA	NA	NA	NA	NA
TX P_{DC}	206mW[2]	1820mW[6]	1190mW[6]	347mW[6]	319mW[6]	724mW(Class-A)[6] 584mW(Class-AB)[6]
RX P_{DC}	111mW	1250mW[6]	960mW[6]	274mW[6]	223mW[6]	397mW[6]
Canceller P_{DC}	44mW	NA	NA	NA	NA	NA

[1] Half-duplex mode measured with loop-back test through the RF Canceller. Supports 1080p/60Hz/8-bit video stream (1.485Gbits) over 1m [45].
[2] Includes doubler power consumption as well
[3] Output 1dB compression point
[4] with TX side LO distribution power consumption.
[5] without TX side LO distribution power consumption.
[6] Includes synthesizer
[7] Reported as P_{1dB}/P_{DC}

(mm-wave full-duplex) to the table. Additionally, the comparison shows that this work surpasses the other works in the table in output power and NF on a per-element basis as well as TX efficiency, while not our focus. Further, it has an EIRP which is better than other single-element designs and even comparable with multi-element designs. A 1080p/60Hz/8-bit 1.485 Gbps video stream has been sent through our transceiver in half-duplex mode over 1 m link distance [70], showing that this work can support high-speed file transfer between mobile devices.

3.5 Summary

This chapter presented a fully-integrated 60 GHz zero-IF transceiver with polarization-based wide-band antenna cancellation, RF and digital cancellation for full-duplex applications. The antenna cancellation can be electronically reconfigured by the transceiver IC to combat environmental reflections. The antenna and RF cancellation together provide a total SI suppression of >70 dB over 1 GHz bandwidth. In conjunction with digital SIC implemented in MATLAB, a simple full-duplex link using RFIC technology was demonstrated for the first time (irrespective of frequency) over 0.7 m.

Chapter 4

A Millimeter-wave Non-Magnetic Passive SOI CMOS Circulator Based on Spatio-Temporal Conductivity Modulation

For all the mm-wave FD applications in Chapter 1, a CMOS-compatible, low-loss, low-noise full-duplex antenna interface with small form-factor, high linearity, power handling, isolation and bandwidth is a significant challenge. Among current solutions (Fig. 4.1), a pair of antennas is bulky and does not provide channel reciprocity. On the other hand, ferrite-based magnetic circulators are not CMOS compatible, leaving passive reciprocal shared-antenna interfaces, such as the electrical balance duplexer (EBD), as the more viable solution. However, it is well known that a three-port reciprocal passive network cannot be lossless, and matched at all ports at the same time. As a result, electrical balance duplexers [71–76] or their microwave counterparts, such as the Wilkinson combiner, suffer from a 3dB fundamental loss (typically around 4dB at RF and mm-wave). In [76], a circular polarization based EBD is reported with less than 3dB loss, but it suffers from large form factor ($1.9\lambda \times 1.9\lambda$) which precludes its use in phased arrays, and more importantly, it uses two antennas to generate orthogonal polarizations for TX and RX, thus not truly realizing a shared antenna interface, and falls into the category of polarization duplexing antenna pairs, such as the

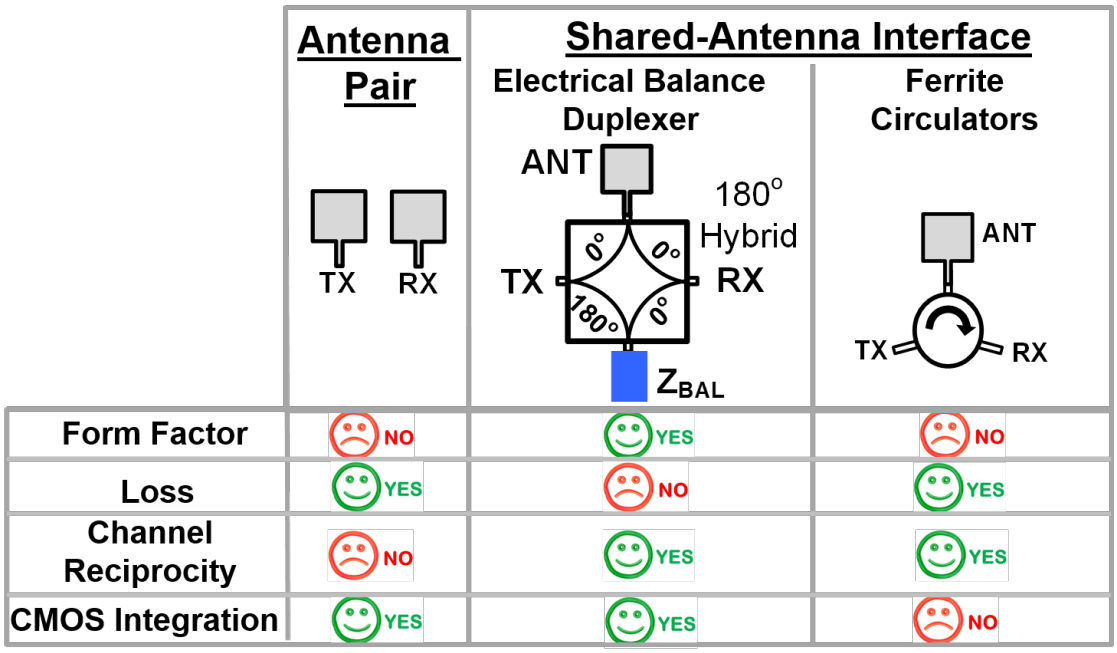

Figure 4.1: Trade-offs associated with conventional full-duplex antenna interfaces.

described in Chapter 2.

This 3dB theoretical loss can be avoided by breaking Lorentz Reciprocity to realize non-reciprocal circulators. Consequently, there has been significant recent interest in breaking reciprocity and realizing circulators in a non-magnetic IC-compatible fashion using temporal modulation [77–81]. This chapter presents a 25GHz fully integrated circulator in 45nm SOI CMOS enabled by a new concept of spatio-temporal conductivity modulation [82], marking the first demonstration of magnetic-free passive non-reciprocity at millimeter-wave. Spatio-temporal conductivity modulation breaks phase reciprocity similar to the phase-shifted N-path filter of [80, 81], but features following advantages: it 1) requires modulation or switching at a frequency lower than the operation frequency (1/3rd in this case), enabling operation at millimeter-wave; 2) uses only four 50% duty-cycle I/Q phases, as opposed to numerous low-duty-cycle non-overlapping clocks as in N-path filters, again easing millimeter-wave operation, and 3) enhances the insertion loss BW and isolation BW when compared with the N-path-filter-based approach of [80, 81] since switching is performed across transmission-line delays instead of capacitors as in N-path filters. In principle, since the modulation frequency can be arbitrarily lowered, this first demonstration of a passive non-reciprocal CMOS millimeter-wave circulator is scalable in frequency, e.g. to 60 or 77GHz,

upon addressing the additional implementation challenges associated with millimeter-wave design.

This chapter presents a detailed discussion of the circulator in [82], including extended time domain analysis, discussion of the impact of clock imperfections and architectural solutions for the same, circuit descriptions, and extended measurements. Additionally, single-ended realization of the spatio-temporal conductivity modulation concept is presented in Section 4.5, achieving a range of non-reciprocal responses in phase and amplitude.

4.1 Prior Approaches to Breaking Reciprocity

Any circuit or system that is linear, time-invariant, passive and constructed from materials featuring symmetric permittivity and permeability tensors is necessarily reciprocal [83]. Consequently, breaking reciprocity requires violating one of these necessary conditions. Magnetic circulators utilize ferrite materials that become inherently non-reciprocal under the application of an external biasing magnetic field through the Faraday effect [84], but as mentioned earlier, are not compatible with CMOS. Circulators based on active transistors have been extensively explored [85–89], but the use of active transistors limits the linearity and the noise performance. Nonlinearity can be used to violate reciprocity and have been extensively explored in the optical domain [90, 91], but these techniques exhibit non-reciprocity over certain signal power levels only (e.g. larger than 15dBm input power in [91]) and therefore have limited applicability to wireless applications which typically demand linearity to the desired signal. Consequently, there has been a strong interest in breaking reciprocity by violating time invariance through time-periodic modulation in recent years (without the use of magnetic materials) [77–80].

Prior approaches to non-reciprocity based on temporal modulation have exploited permittivity as the modulated material parameter, specifically spatio-temporal permittivity modulation using varactors in a circuit implementation. However, permittivity modulation is inherently weak due to small modulation index (for example, varactor C_{max}/C_{min} ratio is typically 2-4 in CMOS), resulting in either large form factors [77] or narrow operation bandwidths [78]. For example, [77] uses spatio-temporal permittivity modulation in a traveling wave architecture to achieve a direction dependent mode conversion along a transmission line (Fig. 4.2(a)). The length of the transmission line required is inversely proportional to the modulation index. Furthermore, it necessitates the use of filters or

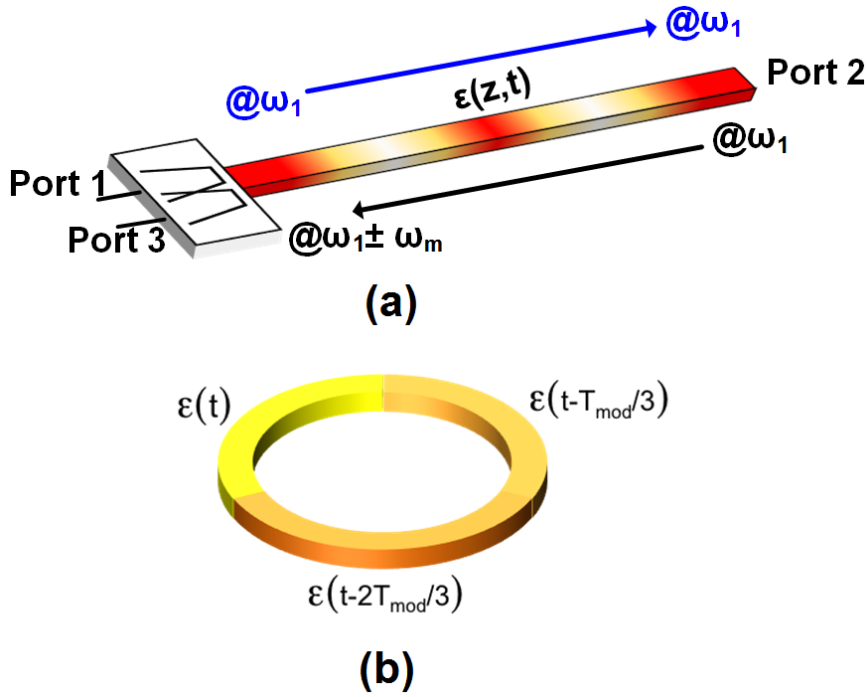

Figure 4.2: Spatio-temporal permittivity modulation (a) in a traveling wave architecture, (b) in a resonant ring.

diplexers to separate the signals the transmitted and received signals. In [78], angular momentum biasing was achieved using spatio-temporal permittivity modulation in a resonant ring (Fig. 4.2(b)). This technique, later demonstrated at microwave frequencies in [79], shrinks the size through the use of lumped LC resonators at the expense of a limited operation bandwidth. Furthermore, permittivity modulation is typically achieved through carrier injection in both varactors and optical modulators [92, 93], resulting in losses (that is, poor varactor quality factors) as the operation frequency is increased to millimeter-waves.

On the other hand, conductivity in semiconductors can easily be controlled using transistor switches, and enables a modulation index several orders of magnitude larger than permittivity over a wide range of frequencies, including millimeter-wave. For example, CMOS transistors exhibit ON-OFF conductance ratios as high as 10^3-10^5 at microwave and millimeter-wave frequencies [94]. Recently, a small form factor, very low loss, high isolation and high linearity RF CMOS passive circulator was demonstrated in [80,81] using phase-shifted N-path filters, essentially a form of spatio-temporal conductivity modulation, as transistors are being switched in a phase shifted fashion across

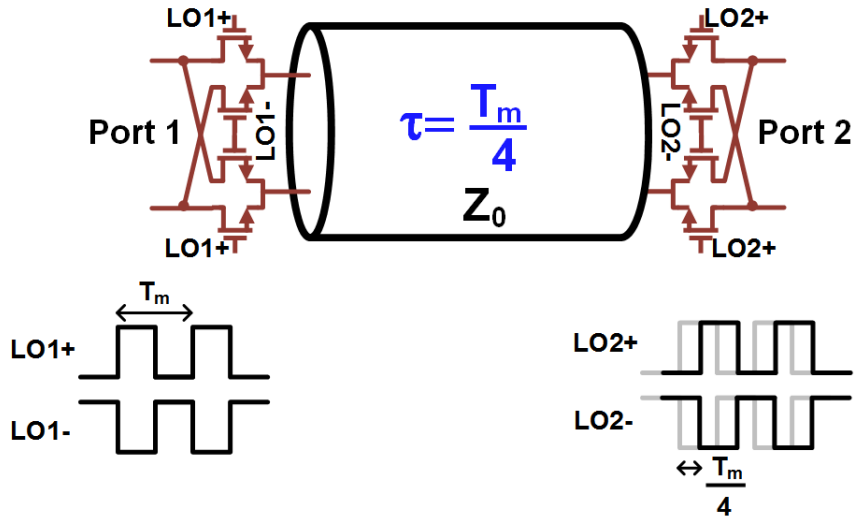

Figure 4.3: Proposed spatio-temporal conductivity modulation technique to achieve broadband phase non-reciprocity. Two sets of switches implemented in a fully-balanced fashion are placed on either end of a differential transmission line providing a delay equal to one quarter of the modulation period ($T_m/4$). The modulation clocks of the right switches are delayed with respect to the left ones by the same amount ($T_m/4$).

capacitors. However, N-path filters are not amenable to millimeter-wave operation due to stringent clocking requirements and transistor parasitics. Inspired by the N-path filter-based low-RF CMOS circulator proposed in [80, 81], this chapter presents a novel generalized concept of spatio-temporal conductivity modulation to achieve wideband millimeter-wave non-reciprocity.

4.2 Spatio-Temporal Conductivity Modulation

The spatio-temporal conductivity modulation concept consists of two sets of switches implemented in a fully-balanced fashion on either end of a differential transmission line delay, as shown in Fig. 4.3. The switches are modulated between short and open circuit states through periodic square pulses with a 50% duty cycle. The transmission line provides a delay equal to one quarter of the modulation period ($T_m/4$), and the modulation of the right switches is delayed with respect to those on the left by the same amount ($T_m/4$). Adding this delay between the two sets of switches allows incident signals from different directions to follow different paths, breaking reciprocity. Fig. 4.4 depicts the signal propagation in the forward direction (from left, or port 1, to right, or port 2). During the first

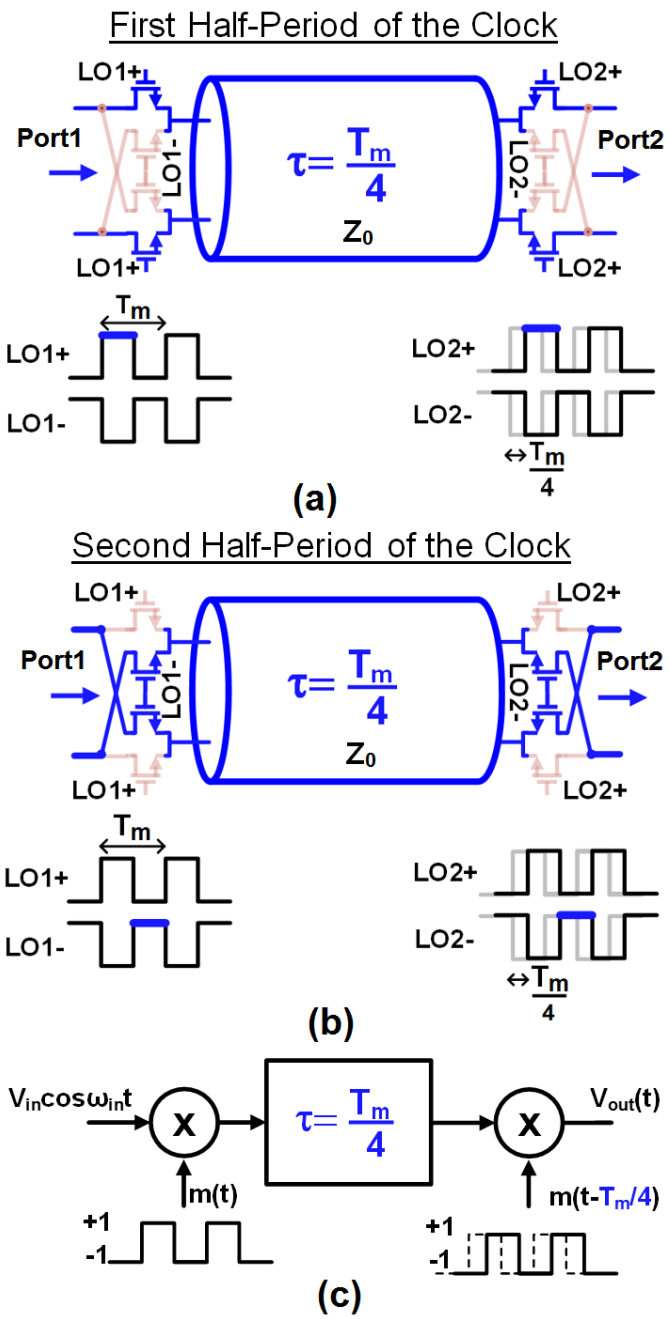

Figure 4.4: Signal propagation in the forward direction through the spatio-temporal conductivity modulation structure. (a) First half period of the clock, (b) second half period of the clock, and (c) signal flow diagram for time-domain analysis. The incident signal passes through the structure without any loss and experiences a transmission line delay of $T_m/4$.

half-period of the modulation clock (Fig. 4.4(a)), when LO1+ is high, the incident signal goes into the transmission line, gets delayed by the transmission line delay of $T_m/4$, and reaches the second set of switches. At this instant, LO2+ is high, so that the signal directly passes to the output. A similar explanation holds also for the second half-period of the modulation clock (Fig. 4.4(b)): the signal goes into the transmission line with a sign flip, gets delayed by $T_m/4$, and the sign flip is recovered by the second set of switches. In other words, signals traveling in the forward direction experience no polarity inversion in the first half cycle, and two polarity inversions that negate each other in the second half cycle. Thus, effectively, in the forward direction, signals pass through the structure without any loss and experience a delay of one quarter of the modulation period. This can be immediately described by the time domain equation $v_2^-(t) = v_1^+(t - T_m/4)$, where v_1^+ and v_2^- are the incident and transmitted signals at ports 1 and 2, respectively. Alternatively, this structure can be modeled by multiplication, delay and multiplication as depicted in Fig. 4.4(c). Here, fully-balanced switching operation is modeled as multiplication by a 50% duty cycle clock, $m(t)$, flipping between +1 and -1. Thus the output signal can be written as

$$v_2^-(t) = v_1^+(t - T_m/4)m(t - T_m/4)m(t - T_m/4) = v_1^+(t - T_m/4), \tag{4.1}$$

which takes advantage of the fact that $m(t - T_m/4)m(t - T_m/4)$=+1 for a binary (-1, +1) signal.

The signal propagation in the backward direction (from right to left) is shown in Fig. 4.5. During the first half-period of the modulation clock, when LO2+ is high, the signal goes into the transmission line and gets delayed by $T_m/4$, and the second set of switches flips the signal sign. Similarly, during the second half-period of the modulation clock (LO2- is high), the signal goes into the transmission line with a sign flip, gets delayed by $T_m/4$ and reaches the output as LO1+ is high. In brief, signals traveling from right to left experience a transmission line delay of $T_m/4$ and a polarity inversion in both half cycles. This can be immediately described by $v_1^-(t) = -v_2^+(t - T_m/4)$, where v_2^+ and v_1^- are the incident and transmitted signals at ports 2 and 1, respectively. An analysis based on the signal flow diagram in Fig. 4.5(c) gives

$$v_1^-(t) = v_2^+(t - T_m/4)m(t - T_m/2)m(t) = -v_2^+(t - T_m/4), \tag{4.2}$$

which takes advantage of $m(t - T_m/2)m(t)$=-1 for a binary (-1, +1) 50% duty-cycle signal . From (4.1) and (4.2), the resultant S-parameters can be written as

$$S_{21}(\omega_{in}) = +e^{-j\frac{\pi}{2}\left(\frac{\omega_{in}}{\omega_m}\right)}, \tag{4.3}$$

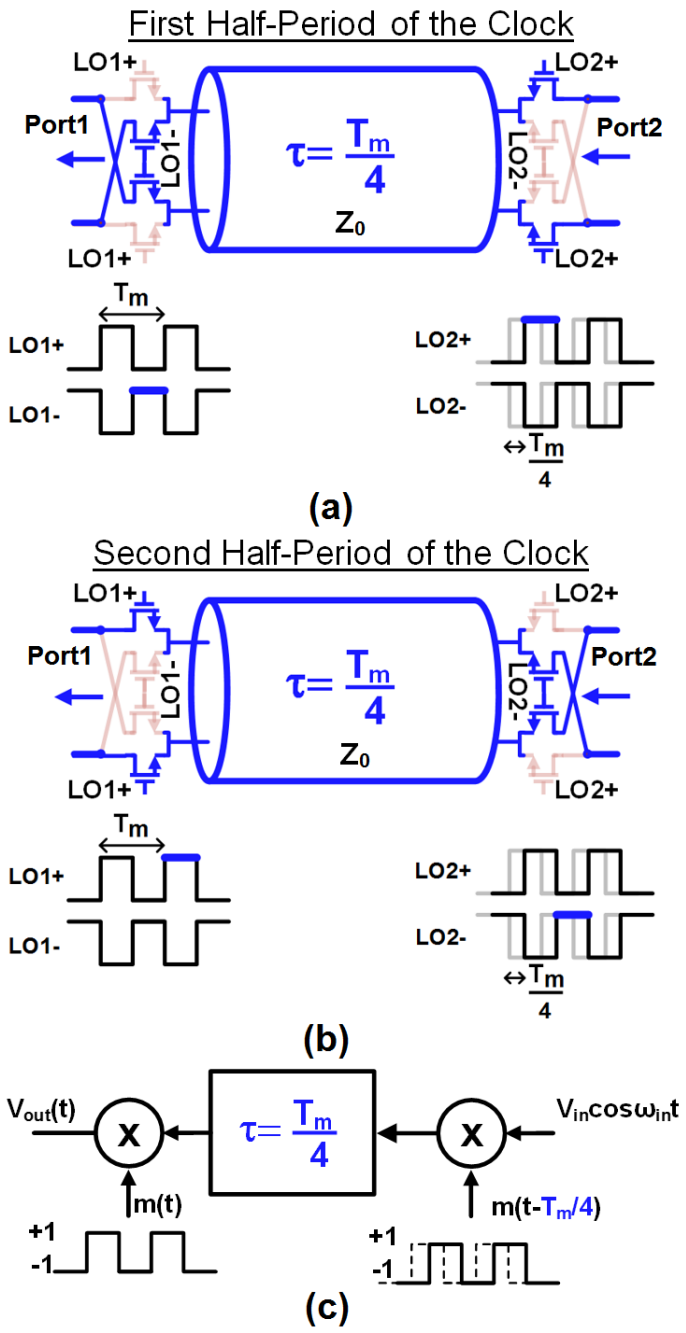

Figure 4.5: Signal propagation in the backward direction through the spatio-temporal conductivity modulation structure. (a) First half period of the clock, (b) second half period of the clock, and (c) signal flow diagram for time-domain analysis. Incident signal experiences no loss, a transmission line delay of $T_m/4$, and *a sign flip*.

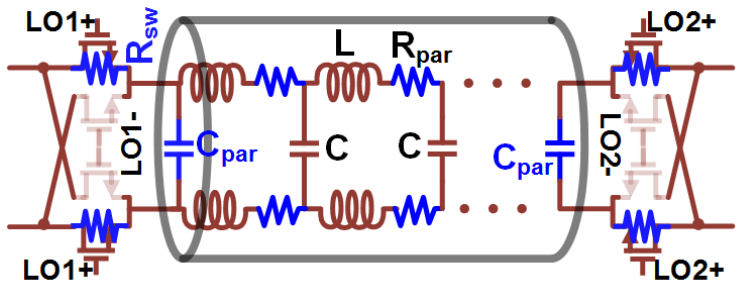

Figure 4.6: Ohmic losses in the switches (R_{sw}) and transmission line (R_{par}), and dispersion effects in the transmission line due to quasi-distributed implementation to absorb the capacitive parasitics of the switches (C_{par}) degrade the insertion loss and bandwidth in practice.

$$S_{12}(\omega_{in}) = -e^{-j\frac{\pi}{2}\left(\frac{\omega_{in}}{\omega_m}\right)}, \tag{4.4}$$

where ω_{in} and ω_m are the signal and modulation frequencies, respectively. It should be noted S_{11}=S_{22}=0 since there is a pair of switches which connects the transmission line to the input and output at any instant in both half cycles. As can be seen from (4.3) and (4.4), this generalized spatio-temporal conductivity modulation technique is ideally lossless and breaks phase reciprocity over a theoretically infinite bandwidth. More importantly, it operates as an ideal passive lossless gyrator- a basic non-reciprocal component postulated by Tellegen in [95] that provides a non-reciprocal phase difference of π and can be used as a building block to construct arbitrarily complex non-reciprocal networks - over theoretically infinite bandwidth. It should also be emphasized that although this gyrator is linear and periodically time-varying (LPTV), it contains absolutely no harmonic conversion at its ports, and therefore appears linear and time-invariant (LTI) from an external operation perspective. In practice, as depicted in Fig. 4.6, the insertion loss would be limited by ohmic losses in the switches and transmission line, and bandwidth by dispersion effects in the transmission line, particularly if it is implemented in a quasi-distributed fashion to absorb the capacitive parasitics of the switches.

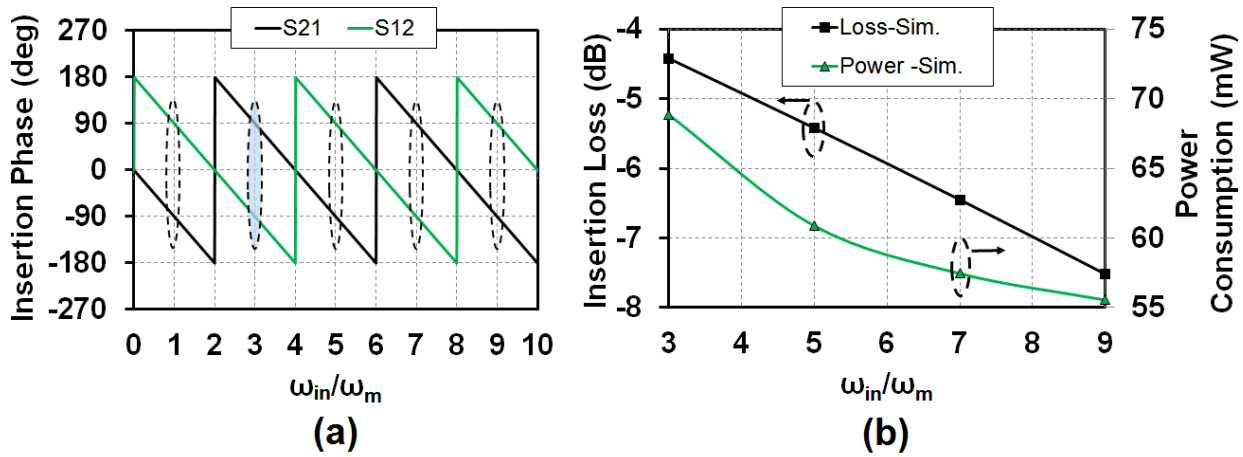

Figure 4.7: (a) Non-reciprocal phase difference of 180°, or gyrator operation, is observed over a theoretically infinite bandwidth but insertion phases of ±90°. are seen at odd multiples of the modulation frequency. (b) Insertion loss and power consumption trade-offs associated with selecting the modulation frequency (ω_{in}/ω_m).

4.2.1 Insertion Loss, Power Consumption and Area versus Modulation Frequency

Fig. 4.7(a) shows the forward and reverse insertion phases ($\angle S_{21}$ and $\angle S_{12}$ respectively) across frequency normalized to the modulation clock frequency. Achieving +90° and -90° phase shifts is important to build the circulator using the ring configuration in [80, 81], although it should be mentioned that other circulator architectures are certainly possible that exploit an arbitrary forward insertion phase. As can be seen, the spatio-temporal conductivity modulation provides a phase shift of ±90° at the odd multiples of the modulation frequency, namely ω_{in}=$(2n-1)\omega_m$, where n is a positive integer. Fig. 4.7(b) plots insertion loss and power consumption trade-offs associated with selecting the modulation frequency (ω_{in}/ω_m). The real 45nm SOI CMOS devices augmented with resistive and capacitive layout parasitics are used in this simulation. The final 3-stage self-biased inverter buffers are included in the simulation to capture the rise and fall times and dynamic power consumption accurately. A broadband *R-L-C* model is used for the transmission lines. Using higher odd multiples reduces the clock frequency, which eases clock generation, distribution and reduces power consumption. Assuming that a rise and fall time (T_r) up to $T_m/12$ can be tolerated (resulting in 0.8dB loss, based on simulations), the bandwidth of the

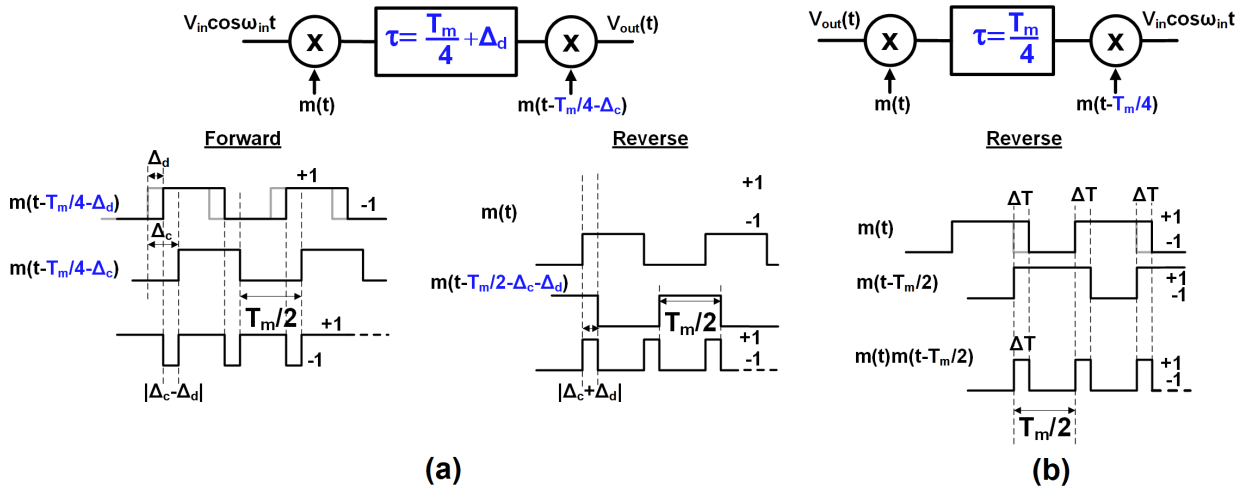

Figure 4.8: (a)Impact of transmission line delay errors and clock delay errors on both forward and reverse transmissions. (b)Impact of duty cycle impairments on the reverse transmission.

square wave can be estimated as BW=$0.35/(T_r)$=$4.2f_m$ [96]. Therefore, a modulation frequency of 25GHz will require designing a clock path with 105GHz BW compared to a 35GHz BW for an 8.33GHz clock, which is more manageable in CMOS processes. Hence, the graph in Fig. 4.7(b) considers (ω_{in}/ω_m)=3 and higher odd multiples. On the other hand, the delay required from the transmission line increases proportionally with ω_{in}/ω_m, resulting in higher insertion loss and a linearly increasing chip area. Considering all these trade-offs, an operating to modulation frequency ratio of 3 (f_m=f_{in}/3=8.33GHz) is chosen to not increase the loss and area significantly while easing the clock generation compared to f_m=25GHz. In case high quality transmission lines are available (e.g transmission lines implemented on package), a lower clock frequency can be selected to lower power consumption. For example, by implementing the transmission lines on Rogers 4350B substrate (0.02dB/mm loss at 25GHz), the clock frequency can be lowered to 1 GHz (using ω_{in}=$25\omega_m$) for a similar loss (assuming 0.5dB loss from the chip-to-package transition).

4.2.2 Impact of Clock Imperfections

4.2.3 Impact of Clock and Transmission Line Imperfections

Due to modeling errors (in the PDK or in EM simulations) as well as process and temperature variations, the transmission line delay and the delay of the second set of switches can deviate from

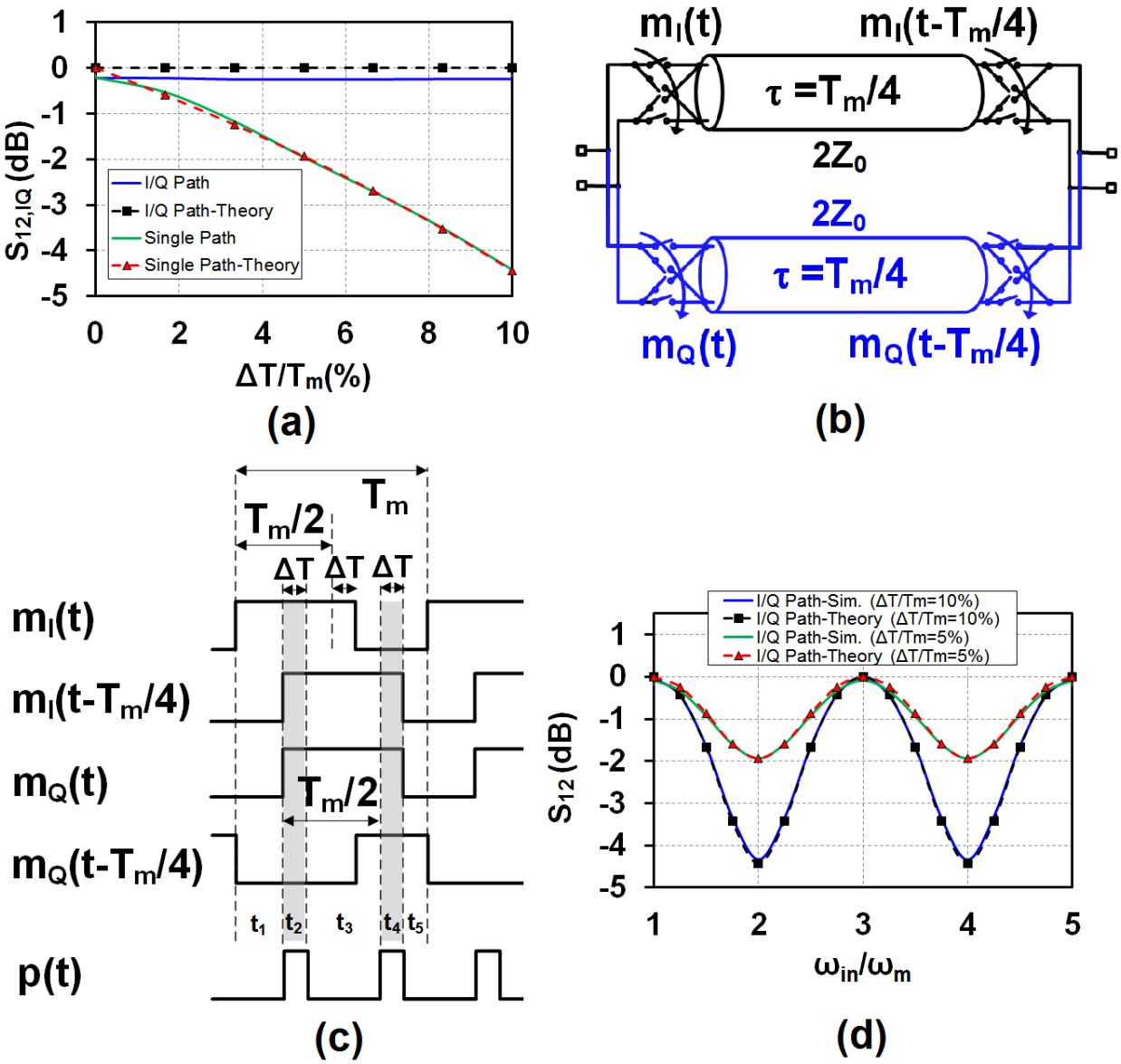

Figure 4.9: (a) Theoretical and simulated effect of deviation of the modulation clock from 50% duty cycle (ΔT) for ω_{in}=3ω_m. Adding a quadrature path mitigates the effect of duty cycle impairment, ensuring robust operation. (b)Block diagram of the gyrator with the quadrature path added. (c) Clock signals for the gyrator with the quadrature path added, including duty cycle error. (d) Theoretical and simulated effect of deviation of the modulation clock from 50% duty cycle across frequency for $\Delta T/T_m$=0.05 and $\Delta T/T_m$=0.1. Adding a quadrature path mitigates the effect of duty cycle impairment at the odd multiples of the modulation frequency.

$T_m/4$, as depicted by Δ_l and Δ_c, respectively, in Fig. 4.8(a). With these delay variations, in the forward direction, $m(t - T_m/4 - \Delta_l)m(t - T_m/4 - \Delta_c)$ results in a pulse train with a pulse width of $|\Delta_c - \Delta_l|$ instead of +1. Similarly, in the reverse direction, $m(t)m(t - T_m/2 - \Delta_c - \Delta_l)$ will give a pulse train with a pulse width of $|\Delta_c + \Delta_l|$. Thus, $S_{21,i}$ and $S_{12,i}$ (i stands for imperfection) at the operating frequency can be expressed as

$$S_{21,i}(\omega_{in}) = \left(+1 - \frac{4|\Delta_c - \Delta_l|}{T_m} \right) e^{-j\frac{\pi}{2}\left(\frac{\omega_{in}}{\omega_m}\right)}, \tag{4.5}$$

$$S_{12,i}(\omega_{in}) = \left(-1 + \frac{4|\Delta_c + \Delta_l|}{T_m} \right) e^{-j\frac{\pi}{2}\left(\frac{\omega_{in}}{\omega_m}\right)}. \tag{4.6}$$

From (4.5) and (4.6), we conclude that small variations in the transmission line and clock delay mainly cause loss, as some portion of the power would be transferred to mixing frequencies due to the harmonic content in the pulse train. For example, a total variation of $|\Delta_c - \Delta_l|$=$T_m/20$ or $|\Delta_c + \Delta_l|$=$T_m/20$ will result in a loss of ≈2dB in the forward and reverse directions, respectively. Tunability in the transmission line design and clock generation scheme can be incorporated to recover the loss. More importantly, (4.5) and (4.6) show that small delay variations do not have any effect on the non-reciprocal phase shift of π (as long as $|\Delta_c - \Delta_l|$ and $|\Delta_c + \Delta_l|$ are less than $T_m/4$).

Duty cycle impairment in the modulation clock is another imperfection that can have an adverse effect on the operation. Let us assume a deviation from ideal 50% duty cycle, say by ΔT. A similar analysis reveals that the forward direction remains unaffected, since $m(t - T_m/4)m(t - T_m/4)$ continues to be +1, but in the reverse direction, $m(t - T_m/2)m(t)$ will give a pulse train with a pulse width of ΔT and period of $T_m/2$ as depicted in Fig. 4.8(b). Thus, deviation from 50% duty cycle would result in loss in the reverse direction. S_{12} at the operating frequency becomes

$$S_{12,i}(\omega_{in}) = \left(-1 + \frac{4|\Delta T|}{T_m} \right) e^{-j\frac{\pi}{2}\left(\frac{\omega_{in}}{\omega_m}\right)} \tag{4.7}$$

Fig. 4.9(a) shows the calculated and simulated insertion loss in the backward direction versus duty cycle deviation ($\Delta T/T_m$). For example, a deviation from 50% duty cycle to 55 or 45% would degrade the loss by about 2dB in the reverse direction.

Addition of a quadrature path mitigates the effect of duty cycle impairment, ensuring a robust operation (Fig. 4.9(b)). In this architecture, the characteristic impedance of the transmission lines

should be $2Z_0$ for perfect broadband matching. Here, the control of the second sets of switches, $m_Q(t-T_m/4)$=$m_I(t-T_m/2)$, is generated by inverting $m_I(t)$ (e.g. using $m_Q(t-T_m/4)$=$\overline{m_I(t)}$). Fig. 4.9(c) depicts the control signals of each set of switches in the I/Q paths with a ΔT deviation from ideal 50% duty cycle. In this structure, the input signal splits evenly into I and Q paths at any time interval. Let us consider the signal flow in a single period. During the time intervals t_1, t_3 and t_5, signals in the I and Q path pass to output with a delay of $T_m/4$ and a sign flip, adding up. However, during the time intervals t_2 and t_4 which have a duration of ΔT, the signals from the I and Q paths reach the output (port 1) out of phase and thus create a virtual short at the output, reflecting the signals back into the delay lines. These reflected signals travel back and acquire an additional delay of $T_m/4$ and reach port 2 out of phase and reflect again. The reflected signals travel back and reach port 1, but this time they are in phase, passing to the output. Based on this operation, the reverse transmission can be expressed in time domain as

$$v_1^-(t) = -v_2^+(t-\frac{T_m}{4})[1-p(t-\frac{T_m}{4})] + v_2^+(t-\frac{3T_m}{4})p(t-\frac{3T_m}{4}) \tag{4.8}$$

where $p(t)$ is the pulse train shown in Fig. 4.9(c). Taking Fourier-transform of the time domain equation, the reverse transmission can be derived in frequency domain as

$$S_{12,IQ}(\omega_{in}) = -e^{-j\frac{\pi}{2}\left(\frac{\omega_{in}}{\omega_m}\right)}\left(1-\frac{2\Delta T}{T_m}[1+e^{-j\pi\left(\frac{\omega_{in}}{\omega_m}\right)}]\right) \tag{4.9}$$

The term inside the parenthesis goes to +1 at the operating frequency of $\omega_{in} = 3\omega_m$ (or indeed, any odd multiple of the modulation frequency), thus providing a constant loss of 0dB in the reverse direction with duty cycle deviation. Similarly, the transmission in the forward direction can be expressed as

$$S_{21,IQ}(\omega_{in}) = +e^{-j\frac{\pi}{2}\left(\frac{\omega_{in}}{\omega_m}\right)}\left(1-\frac{2\Delta T}{T_m}[1+e^{-j\pi\left(\frac{\omega_{in}}{\omega_m}\right)}]\right) \tag{4.10}$$

showing that a similar profile is achieved in the forward direction with a sign flip. Thus, a non-reciprocal phase difference of π is still achieved even in the presence of duty cycle impairments. Fig. 4.9(d) shows the simulated and derived S-parameters for different $\Delta T/T_m$ values and across frequency. It should be noted that $S_{12,IQ}$ and $S_{21,IQ}$ change across frequency with duty cycle deviation, achieving a maximum magnitude of 0dB and minimum magnitude of 20log(1-4$\Delta T/T_m$), same as the single path degradation, at operating frequencies that are odd and even multiples of ω_m, respectively. In other words, addition of the Q-path recovers the degradation due to duty cycle

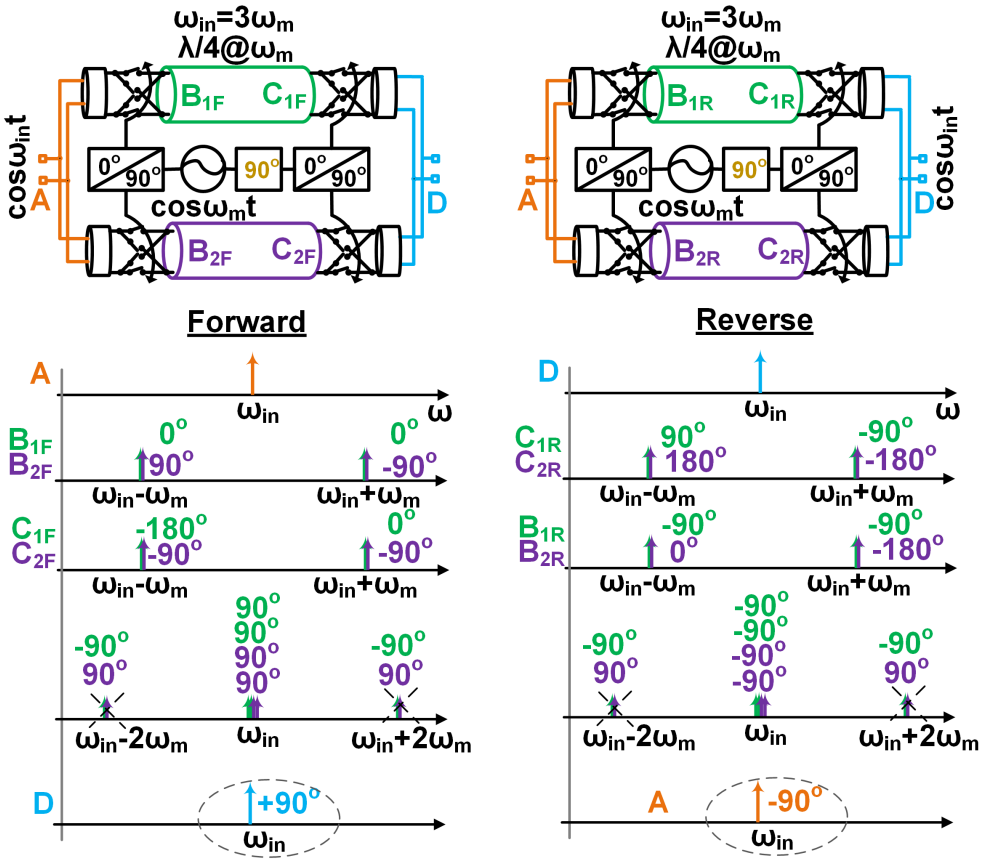

Figure 4.10: Simplified frequency-domain mixing-analysis-based explanation of the non-reciprocal phase response of the spatio-temporal conductivity modulation concept.

impairment at odd multiples of the modulation frequency, which is where the circulator is designed to operate.

4.2.4 A Mixer-Delay-Mixer-based Explanation

The spatio-temporal conductivity modulation operation can also be explained based on a simple frequency-domain mixing analysis (Fig. 4.10). The I/Q switches commutate the signal at a modulation frequency lower than the operating frequency (ω_{in}=3ω_m in this case). As a result, mixing products appear after the commutation at ω_{in}-ω_m and ω_{in}+ω_m[1]. These signals flow through the

[1]In Fig. 4.10, mixing products only at ω_{in}-ω_m and ω_{in}+ω_m are shown for simplicity, but in reality, square-wave commutation will produce mixing products at offsets equal to all odd multiples of ω_m.

transmission line, which provides -180° and -360° phase shift at ω_{in}-ω_m and ω_{in}+ω_m, respectively (since ω_{in}=3ω_m). The phase shifted signals are then commutated again at ω_m but with a phase shift of -90°, creating mixing products at ω_{in}, ω_{in}-2ω_m and ω_{in}+2ω_m. The signals at ω_{in}-2ω_m and ω_{in}+2ω_m are 180° out of phase and cancel out. On the other hand, the mixing products at ω_{in} add up constructively into a single signal with perfect lossless transmission and a phase shift of +90°. A similar analysis in the reverse direction shows lossless transmission but a non-reciprocal phase shift of -90°, achieving a non-reciprocal phase shift with 180° difference between forward and reverse directions. If there is a mismatch between the electrical lengths of the I and Q transmission lines, the mixing products at ω_{in} will add up partially, resulting in a loss The simulated loss remains less than 0.8dB up to 10% mismatch, with no effect on the non-reciprocal phase shift of π. This mixer-delay-mixer-based explanation sheds insight on the need for broad bandwidth in the transmission lines, as they must support signals at mixing frequencies that are offset from the operating frequency at all odd multiples of ω_m.

4.3 Implementation

This non-reciprocal phase shift element (gyrator) can now be embedded within a $3\lambda/4$ transmission line ring as depicted in Fig. 4.11(a) to realize a non-reciprocal circulator similar to [80]. In the clockwise direction, the -270° phase shift of the transmission line adds to the -90° phase shift through the gyrator, enabling wave propagation. In the counter-clockwise direction, the -270° phase shift of the transmission line adds to the +90° phase shift of the gyrator, suppressing wave propagation. A three port circulator is realized by introducing three ports $\lambda/4$ apart from each other (Fig. 4.11(b)). The gyrator is placed symmetrically between the TX and RX ports. The S-parameters of the circulator at $\omega_{in} = 3\omega_m$ can be derived to be

$$S(\omega_{in}) = \begin{pmatrix} 0 & 0 & -1 \\ -j & 0 & 0 \\ 0 & -j & 0 \end{pmatrix} \tag{4.11}$$

through microwave network analysis, where TX is port 1, ANT is port 2 and RX is port 3.

Fig. 4.12 shows the implementation of the circulator at 25GHz. The differential nature of the circulator reduces the LO feedthrough and improves power handling. The placement of the gyrator

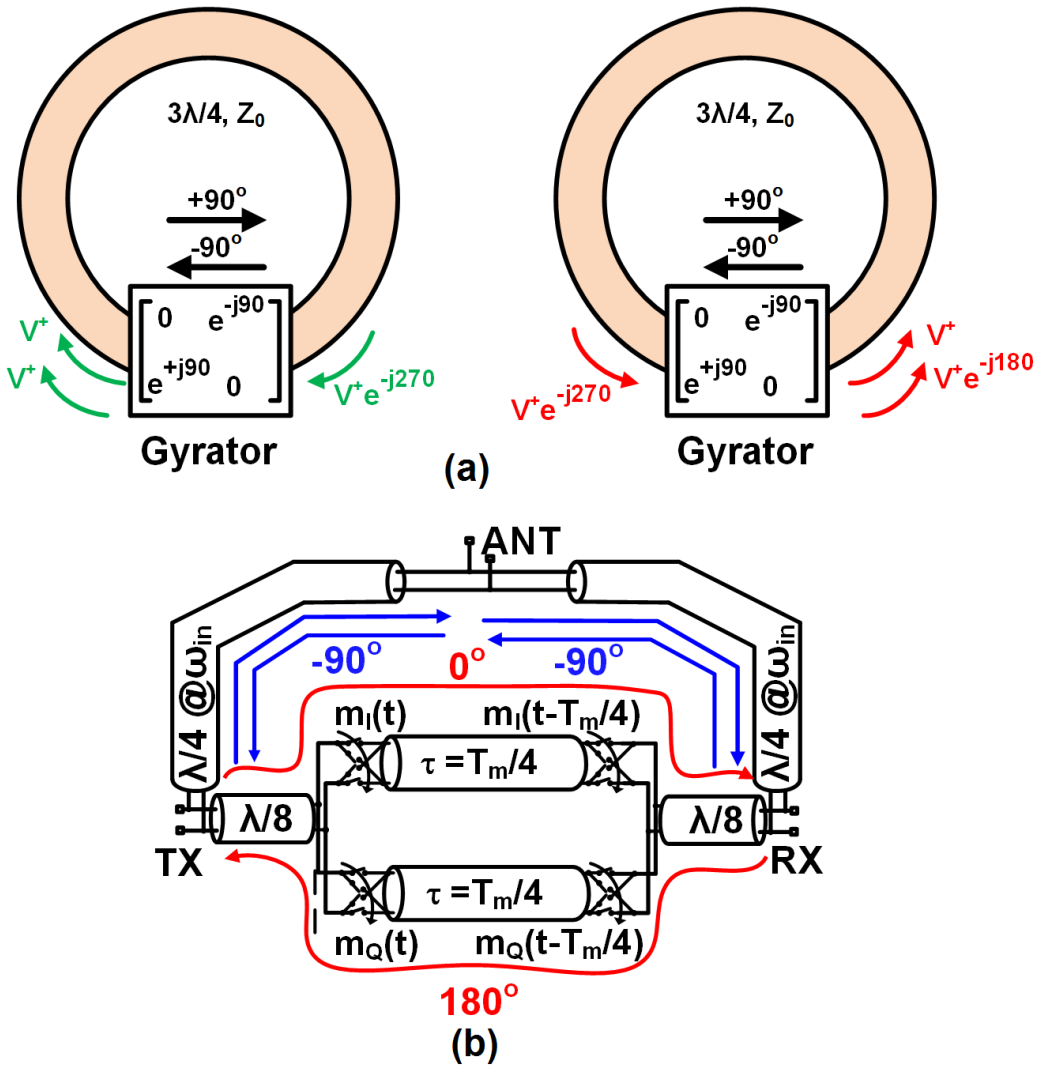

Figure 4.11: Circulator architecture: (a) A $3\lambda/4$ line is wrapped around the gyrator to support non-reciprocal wave propagation. (b) A circulator is realized by introducing three ports which are $\lambda/4$ apart. The gyrator is placed symmetrically between the TX and RX ports.

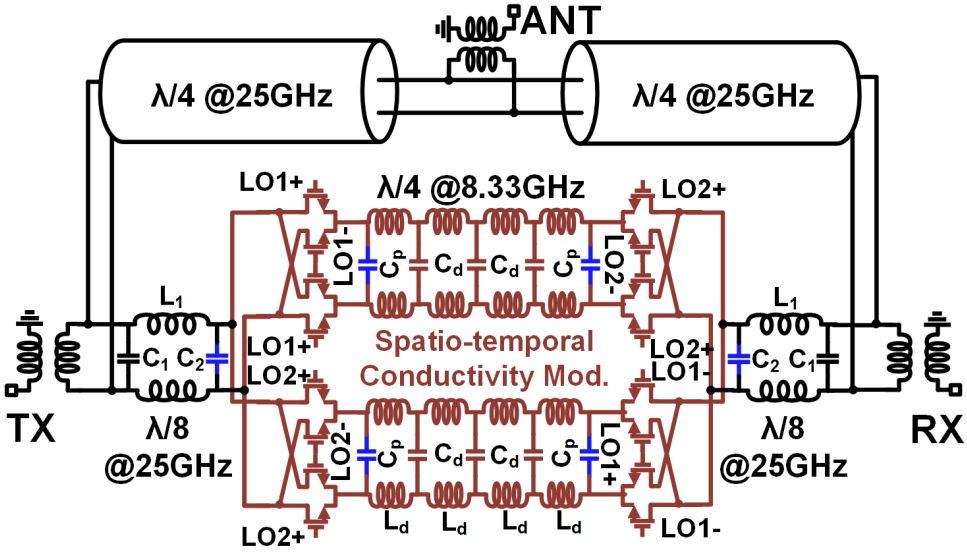

Figure 4.12: Circuit diagram of the implemented 25GHz fully-integrated non-reciprocal passive magnetic-free 45nm SOI CMOS circulator.

in a symmetric fashion between the TX and RX ports enables switch parasitics to be absorbed into the lumped capacitance of the $\lambda/8$ sections on either side which were implemented using L_1=280pH and C_1=C_2=40fF. The fully-balanced I/Q quads are designed using 2×16μm/40nm floating-body transistors. Transistor sizes are selected so that the total parasitic capacitance on the either side of the gyrator (C_2) is 40fF (no physical capacitor is used in the layout). This ensures wideband operation, but limits the switch on resistance to R_{on}=8.6Ω (causing ∼1dB loss in the circulator). Artificial (quasi-distributed) transmission lines are used in the gyrator, with four stages of lumped π-type C-L-C sections, for size reduction as well as improving insertion loss. Each π-type C-L-C section is essentially a second order filter with a corner frequency of ω_B=$2/\sqrt{2LC}$, referred to as the Bragg frequency, and provides a delay of $\sqrt{2LC}$. Signals at frequencies above the Bragg frequency are strongly attenuated because of an imaginary propagation constant. As mentioned earlier, after the first set of switches, multiple mixing products at $\omega_{in} \pm n\omega_m$ are generated where n is an odd integer. Mixing products at frequencies higher than Bragg frequency ($\omega_{in} \pm n\omega_m$¿$\omega_B$) will be filtered, forming another loss mechanism. Therefore, it is important to design for a high enough Bragg frequency to not degrade loss significantly. In this work, L_d and C_d are 200pH and 20fF, resulting in a simulated Bragg frequency of 76GHz. Four π-type C-L-C sections provide a

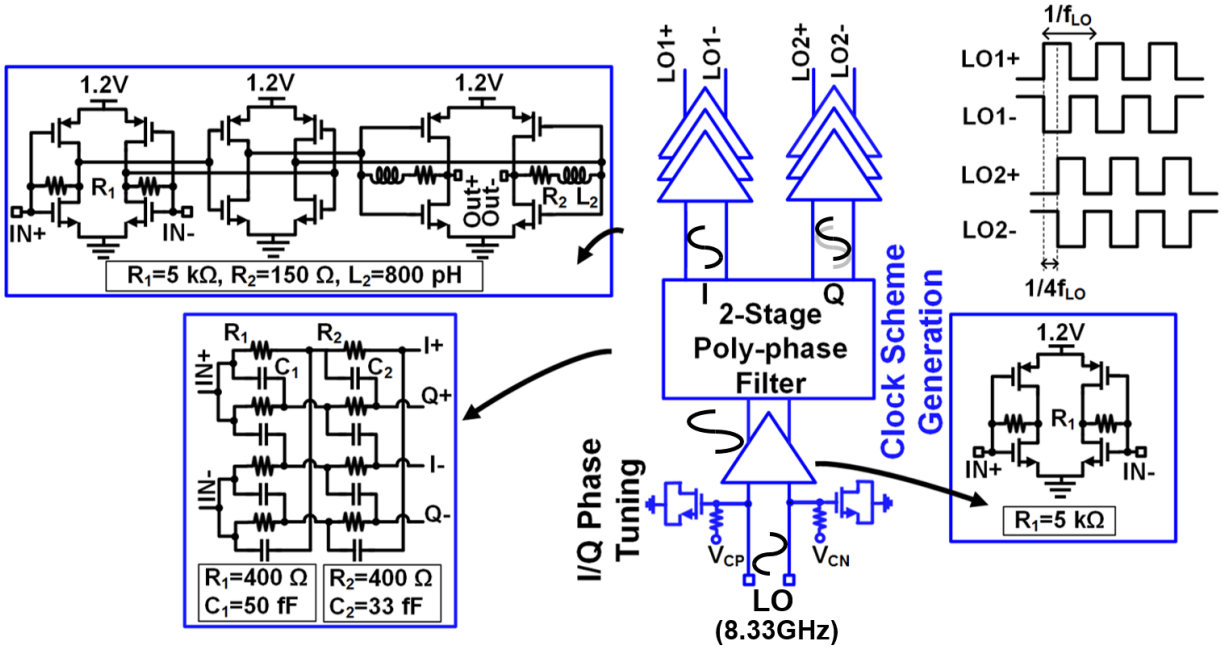

Figure 4.13: Block and circuit diagrams of the 8.33GHz LO path.

delay of 20ps and the rest (10ps) comes from G-CPW transmission lines connecting the inductors together in the layout. Inductors are implemented by stacking two topmost metals (LB and UB) to improve the inductor quality factor (achieving a simulated Q of >20 from 14GHz to 50GHz). This improves the circulator loss by 0.3dB compared to using differential conductor-backed coplanar waveguides. The complete delay line structure is EM simulated and has an insertion loss of 0.9-2.3dB from 5GHz to 50GHz. The $\lambda/4$ transmission lines between the TX and ANT and ANT and RX ports are implemented using differential conductor-backed coplanar waveguides with a loss of 0.39dB/mm at 25GHz. Baluns are included at the TX, ANT and RX ports to enable single-ended measurements, and separate test structures are included to de-embed the response of the baluns. We envision a fully differential system, including the antenna which can be implemented as a differential microstrip or slot-ring antenna [97], eliminating the need for differential to single-ended conversion. Interested readers can refer to [98] for a single-ended circulator architecture based on the spatio-temporal conductivity modulation concept.

Fig. 4.13 shows the block and circuit diagrams of the 8.33GHz LO path. The four quadrature clock signals driving the switches are generated from two input differential sinusoidal signals at

8.33GHz. A two stage poly-phase filter (phase imbalance <2° for up to 15% variation in R and C values) is used to generate the 8.33GHz quadrature signals with 0°/90°/180°/270° phase relationship. After the poly-phase filter, a three stage self-biased CMOS buffer chain with inductive peaking in the final stage generates the square wave clock signals for the switches. Independently controlled NMOS varactors (implemented using 4×40μm/40nm floating-body devices) are placed at the differential LO inputs to compensate for I/Q imbalance of the poly-phase filter. This provides an I/Q calibration range of ±10 degrees to optimize the circulator performance.

The simulated circulator loss is ∼3dB from 23 to 26GHz (Fig. 4.14(a)). In constrast to EBDs, which suffer from fundamental 3dB loss, the TX-to-ANT and ANT-to-RX insertion losses in this work are mainly the result of switch on resistance, inductor/transmission-line loss due to the finite Q, and dispersion due to the Bragg effect. Fig. 4.14(b) shows the distribution of circulator loss based on simulations, and it reveals that 34% and 40% of the total loss come from the switch on resistances and finite Q of transmission lines and inductors, respectively. Other loss mechanisms (26%) include finite Bragg frequency as mentioned earlier and clock imperfections. The switch on resistance can be reduced by half by removing the quadrature delay-line path and doubling the device sizes, thus preserving the total device parasitic capacitance and hence, the LO path power consumption. A fine duty cycle calibration mechanism can be included to counter the impact of duty cycle impairments. A better technology with lower switch $R_{on} \times C_{off}$ technology constant would also naturally improve performance. Fig. 4.14(c) shows the projected loss versus $R_{on} \times C_{off}$ values (based on Peregrine's switch technology roadmap [99] and assuming a passive Q of 20) for two different configurations-with the gyrator employing a single path or I/Q paths. Removing the I/Q path would improve the insertion loss by 0.6dB in this process and it returns diminishing improvements after $R_{on} \times C_{off}$ is lower than 100fs. Additionally, Fig. 4.14(d) shows the projected loss for the single-path architecture versus Q for different switch $R_{on} \times C_{off}$ values. For example, an $R_{on} \times C_{off}$ of 200fs and Q of 35 (achievable with high resistivity substrate and/or thicker BEOL) would enable an integrated circulator with a loss ∼2dB. To generate these plots, parasitic resistances in the transmission model and R_{on} are swept, assuming same device capacitive parasitics so that they can still be absorbed in the $\lambda/4$ sections. In this process, $R_{on} \times C_{off}$ of 2×16μm/40nm regular pitch devices is simulated to be ∼ 197fs including parasitic extraction and EM modeling up to the top metal. This compares well with the simulated $R_{on} \times C_{off}$ of 185fs reported in [100]

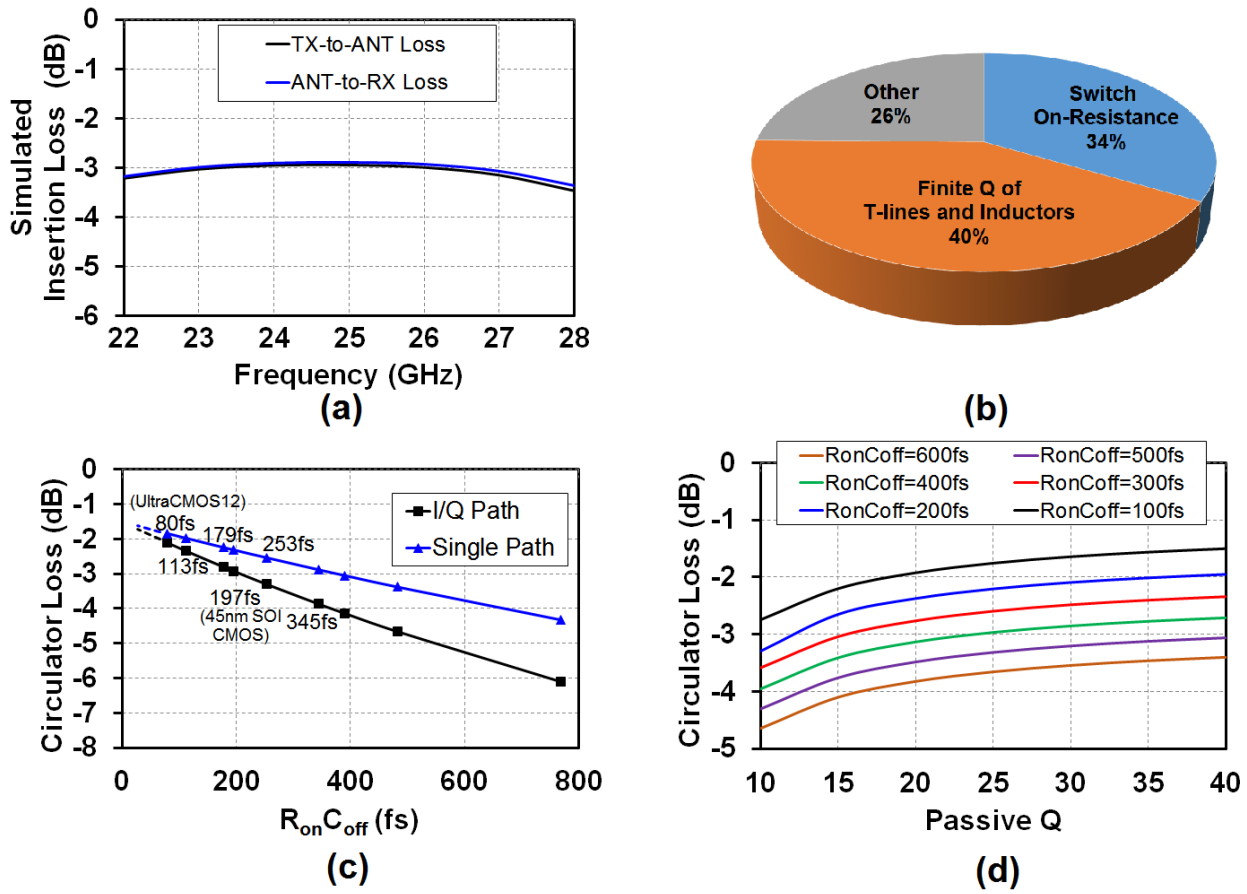

Figure 4.14: (a) Simulated circulator insertion loss. (b) Circulator simulated loss distribution: IL is dominated by switch on-resistance and finite Q of the passives. (c)Projected loss as a function of switch $R_{on}C_{off}$ (the annotated values include 45nm SOI CMOS and Peregrine's switch technology roadmap, including 80fs from UltraCMOS12 technology in 2017). Passive Q is assumed to be 20 at 25GHz. (d) Projected loss in a single path architecture as a function of the passive Q: an IL of less than 2dB is possible in a technology with lower switch $R_{on}C_{off}$ and/or higher passive Q through a high-resistivity substrate and/or thicker BEOL.

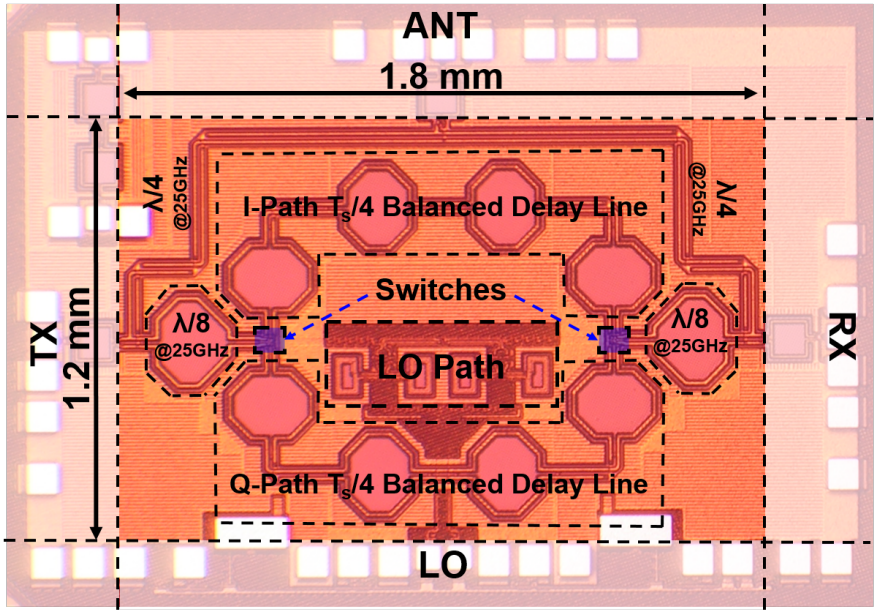

Figure 4.15: Chip microphotograph of the 25GHz fully-integrated non-reciprocal passive magnetic-free 45nm SOI CMOS circulator based on spatio-temporal conductivity modulation.

in the same process. $R_{on} \times C_{off}$ is simulated at 75fs for the intrinsic device model without any extraction, showing that the circulator would also benefit from device layout optimization (e.g. using relaxed pitch devices). Our simulations based on this method differ from measurements by only 0.3dB, agreeing well.

4.4 Measurements

The 25GHz magnetic-free passive circulator is implemented in the GF 45nm SOI CMOS process. Fig. 4.15 shows a micro-photograph of the circulator IC, which occupies 1.2 mm×1.8 mm active chip area excluding the on-chip baluns implemented for testing. S-parameter measurements of the 25GHz circulator were performed using a setup depicted in Fig. 4.16. The circulator is tested in a chip-on-board configuration through RF probing. DC supply, ground, control voltage and 8.33GHz clock input pads are wire bonded to the board. An off-the-shelf 180° hybrid (Krytar 4010265) is used to generate the differential (0°/180°) 8.33GHz signals from a signal generator to drive the clock inputs of the circulator. A two-port Anritsu 37397E Lightning VNA is used to measure the

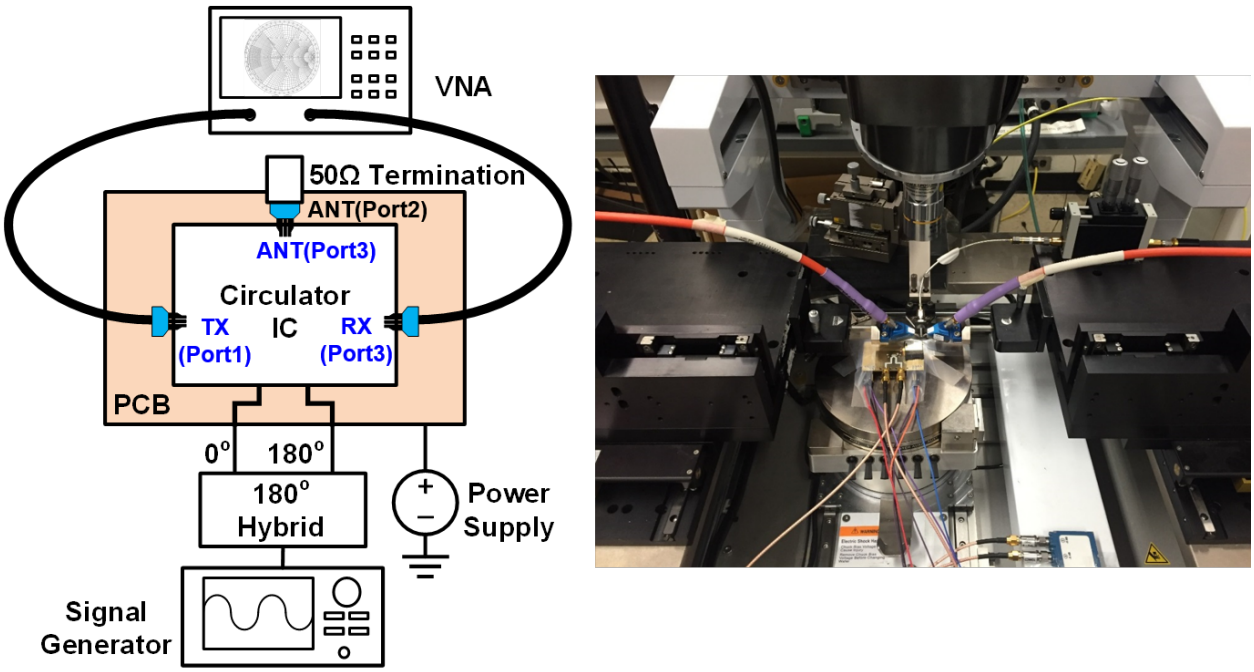

Figure 4.16: Small signal measurement setup: S-parameters are measured by probing two ports at a time. A millimeter-wave probe terminated with a broadband 50Ω termination is landed on the third port.

S-parameters by probing two ports at a time, while a millimeter-wave probe terminated with a broadband 50Ω termination is landed on the third port.

When circulator is configured for clockwise circulation with spatio-temporal conductivity modulation at 8.33GHz, a broadband non-reciprocal behavior is observed over more than 6GHz bandwidth (Fig. 4.17 and Fig. 4.18). The measured transmissions in the clockwise direction (S_{21}, S_{32}, and S_{13}) are -3.3dB, -3.2 dB and -8.7dB, respectively, at 25GHz. The measured isolation levels in the reverse direction (S_{12}, S_{23}, and S_{31}) are -10.3dB, -9dB and -18.9dB, respectively, without any port impedance tuning. The circulator is designed to exhibit best performance for S_{21}, S_{32} and S_{31} (namely TX-to-ANT loss, ANT-to-RX loss and TX-to-RX isolation) as these are the most critical parameters in wireless communication and radar applications. The insertion losses S_{21} and S_{32} degrade by 1dB over 4.6GHz bandwidth (18.4%, notably wideband compared to prior art [80]), and the isolation (S_{31}) over this bandwidth ranges from -18.3 to -20.2dB (Fig. 4.18). The circulator power consumption is 78.4mW. It is dominated by the 3-stage buffer at the LO output, consuming

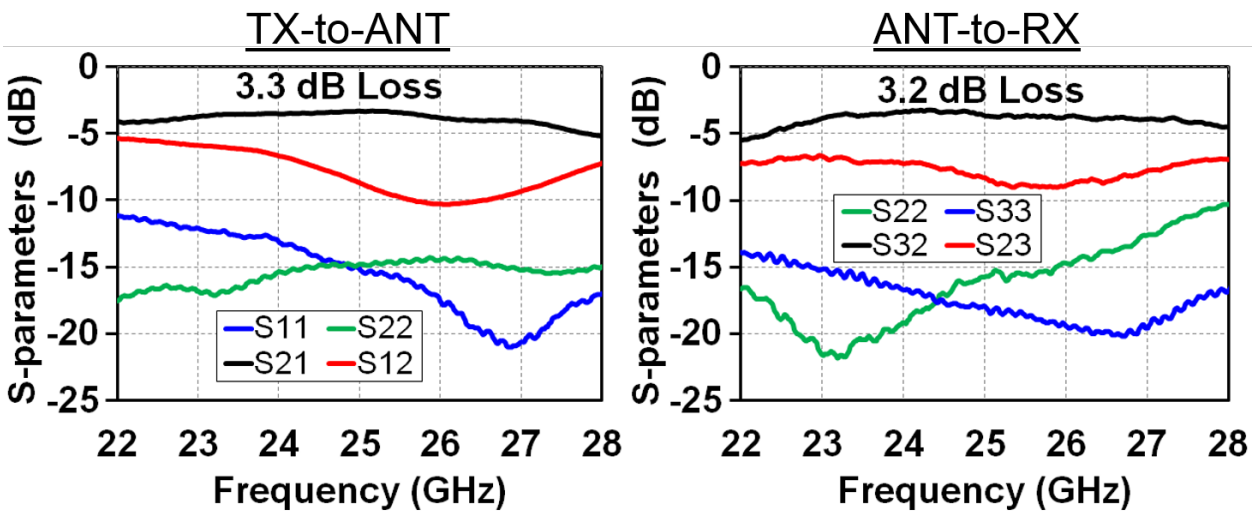

Figure 4.17: Circulator TX-ANT and ANT-RX S-parameter measurements for a clock frequency of 8.33GHz. TX, ANT and RX are ports 1, 2 and 3, respectively.

67.8mW, and the driving amplifier at the LO input consumes 10.6mW.

It should also be emphasized that the near-20dB isolation does not represent the fundamental isolation of the circulator [2], but rather is limited by reflections at the ANT port (port 2) due to imperfect termination impedance, a general limitation for all circulators and exacerbated at millimeter-wave. As was mentioned earlier, the termination of port 2 is achieved by landing a millimeter-wave probe terminated with a 50Ω termination impedance. In millimeter-wave measurements, it is challenging to obtain better than 20dB reflection coefficient from a probe and termination impedance combination. Measurements were performed using an external ANT impedance tuner, as shown in Fig. 4.19(a). It can be seen that high isolation levels are achievable, but the bandwidth of the isolation is limited by the delay of the cable that connects the probe to the tuner. In practice, achieving higher isolation over wider bandwidths requires the integration of an antenna impedance tuner on the same chip as the circulator. In Fig. 4.19(b), simulations are performed using the measured circulator S parameters, and an on-chip tuner is emulated by directly tuning the impedance at the ANT port. It can be seen that >40dB isolation is achievable over GHz-wide bandwidths.

[2]In a real system, antenna matching does not only affect magnitude of isolation but also its bandwidth

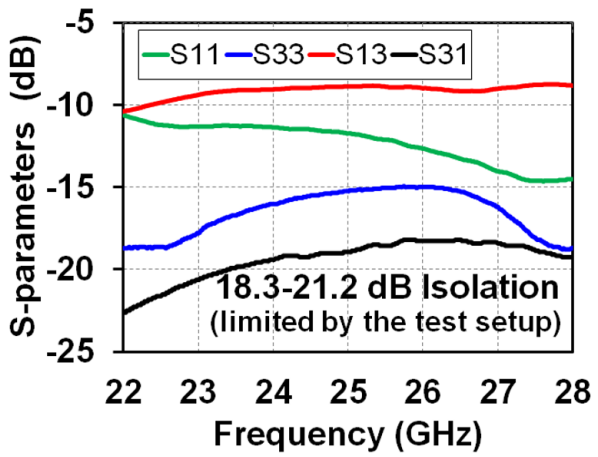

Figure 4.18: TX-RX S-parameter measurements. A broadband TX-to-RX isolation of 18.3 to 21.2dB over 4.6GHz (the 1dB BW of the ILs) is observed, limited by the reflection at the ANT port (a general limitation for all circulators and exacerbated at millimeter-wave).

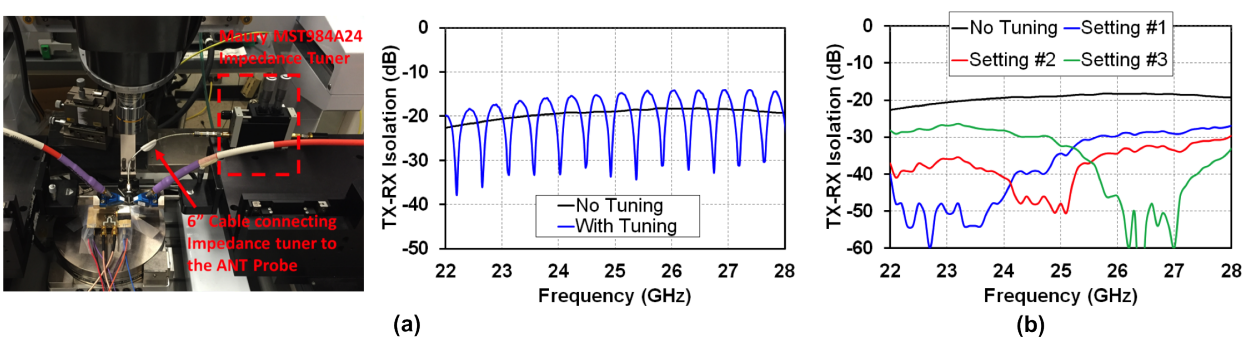

Figure 4.19: (a) Measured TX-to-RX isolation using an external ANT impedance tuner. High isolation levels are achieved but the BW of the isolation is limited by the cable that is used to connect to the tuner. (b) Simulated TX-to-RX isolation based on measured circulator S parameters through direct tuning of impedance at the ANT port.

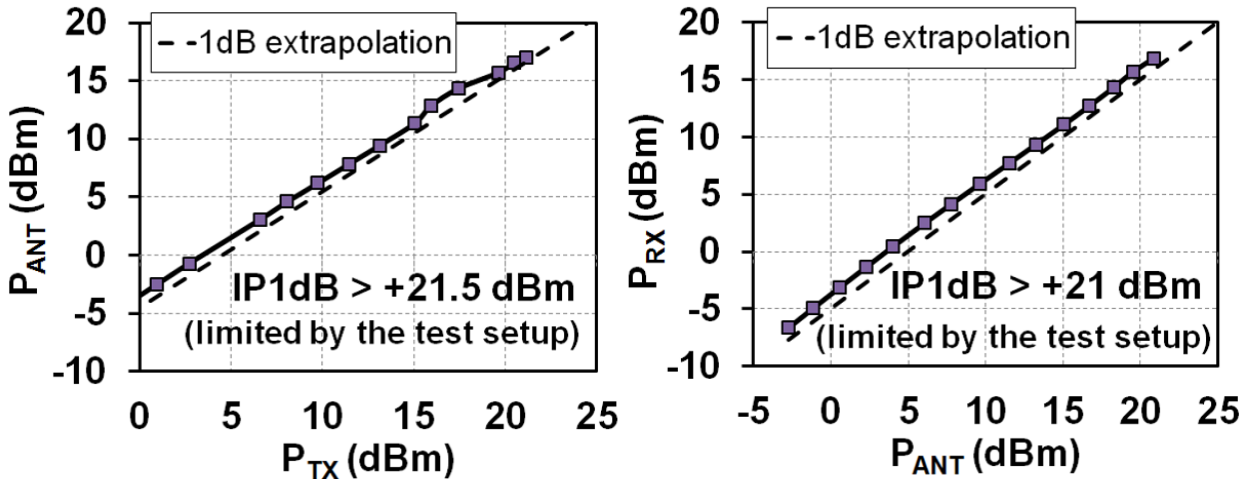

Figure 4.20: Circulator TX-to-ANT and ANT-to-RX large-signal measurements: TX-to-ANT input P1dB is +21.5dBm while ANT-to-RX input P1dB is +21dBm (limited by the test setup).

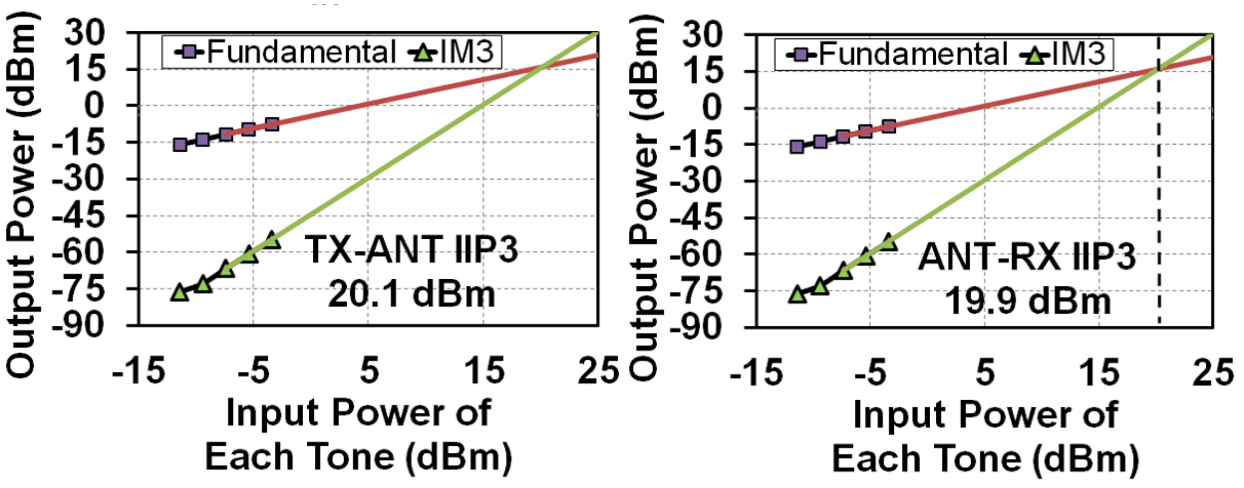

Figure 4.21: Measured TX-to-ANT and ANT-to-RX IIP3s.

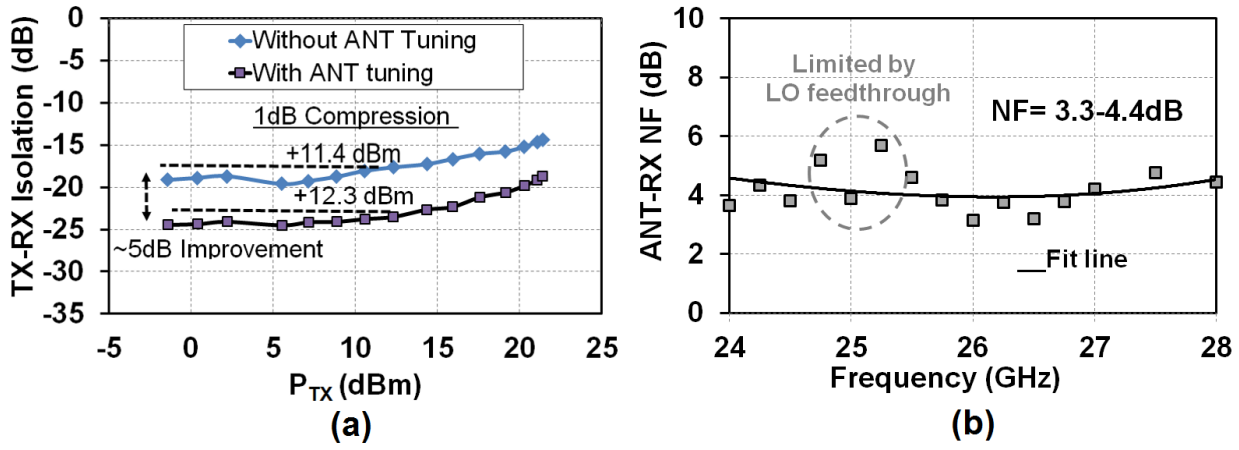

Figure 4.22: (a) Measured TX-to-RX large-signal isolation and (b) circulator ANT-RX noise figure. Without antenna tuning, TX-RX isolation compresses by 1dB at 11.4dBm and 3dB at 21.45dBm. An external ANT impedance tuner enables a higher initial isolation of 25dB (still limited by the measurement setup) and 1dB compression at +12.3dBm. ANT-RX NF is consistent with the IL, showing negligible degradation due to LO phase noise.

The TX-to-ANT/ANT-to-RX input P_{1dB}s are >+21.5/+21dBm (Fig. 4.20), respectively (setup limited). They could not be driven into compression due to the limited output power of the driving amplifier in the testing setup. The measured TX-to-ANT and ANT-to-RX IIP3s are ∼+20dBm (Fig. 4.21) using two tones at 25 and 25.1GHz. It is noteworthy that the P_{1dB}s are high relative to the IIP3s because the circulator gracefully transitions to reciprocal operation under large-signal operation as switching action is controlled by the large input signal instead of the modulation signal. Since IIP3 is an extrapolation from small signal levels, this transition is not reflected in IIP3 measurements. The measured TX-to-RX isolation performance versus the transmit power is shown in Fig. 4.22(a). TX-to-RX ISO compresses by 1dB and 3dB at +11.4dBm and +21.45dBm, respectively. This can be compensated by an external ANT impedance tuner, which enables a higher initial small-signal ISO of 25dB and 1dB compression at +12.3dBm. The measured ANT-RX NF is shown in Fig. 4.22(b), and ranges from 3.3 to 4.4 dB, consistent with the insertion loss and not degraded by LO phase noise.

Table 3.1 compares this circulator with prior art. This circulator performs better than active millimeter-wave circulators [86, 89] in all metrics (loss, linearity, NF and BW). When compared

with a passive electrical balance duplexer [101], this work achieves >1dB overall advantage in IL (the sum of TX-to-ANT and ANT-to-RX ILs) while operating at >10x higher frequency. When compared with the N-path filter-based circulator of [80,81], operation at millimeter-waves is enabled by the ability to perform modulation at a frequency much lower than the operating frequency using four square-wave clocks with 0°/90°/180°/270° phase shift and 50% duty cycle, as opposed to eight or more non-overlapping clocks with low duty cycle running at the operation frequency as is the case with N-path filters. Furthermore, the proposed conductivity modulation across transmission line delays results in far more broadband non-reciprocity than [80]. N-path switched-capacitor approaches inherently yield a second-order bandpass filter response with a bandwidth that is directly related to the capacitor value. Such a narrowband filter response is avoided here through the use of transmission line delays that are quarter-wave at the modulation frequency. While such narrowband filtering might be desirable in some applications (for instance, for tolerance of out-of-band interference at RF), other applications, such as millimeter-wave systems which inherently offer interference tolerance and spatial re-use through beamforming, would benefit from wideband operation. It should also be mentioned that the N-path approach offers the benefit of an ultra-compact, electrically-infinitesimal, inductor-less gyrator implementation, albeit with harmonic conversion effects, unlike the gyrator proposed in this work.

4.5 Other Non-reciprocal Components Based on Spatio-Temporal Conductivity Modulation

So far this chapter focused on the implementation of spatio-temporal conductivity modulation in a doubly-balanced (fully differential)configuration for implementation of mm-wave circulators. The same concept can also be implemented in a single-balanced fashion as reported in [98], paving the way for realization of other magnetic-free non-reciprocal components such as non-reciprocal phase shifter and isolator.

4.5.1 Non-reciprocal Phase Shifter

Fig. 4.23(a) shows the operation diagram of the single-balanced spatio-temporal conductivity modulation concept, leading to a non-reciprocal phase shifter. Similar to the double-balanced con-

Table 4.1: Performance summary and comparison.

	[86]	[89]	[75]	[81]	This work
Technique	Active Quasi Circulator	Active Quasi Circulator	Electrical Balance Duplexer	N-Path-Filter-based Magnetic-Free Passive Circulator	Magnetic-Free Passive Circulator Based on Spatio-Temporal Conductance Mod.
Technology	180nm CMOS	180nm CMOS	180nm SOI CMOS	65nm CMOS	**45nm SOI CMOS**
Frequency	24GHz	24GHz	1.9-2.2GHz	0.75GHz	**22.7-27.3GHz**
TX-ANT Transmission	+22.4dB	-5.7dB	-3.7dB	-1.7dB	**-3.3dB @ 25GHz (1dB BW 22-27.3 GHz)**
ANT-RX Transmission	+12.3dB	-5.7dB	-3.9dB	-1.7dB	**-3.2dB @ 24.7GHz (1dB BW 22.7-27.5 GHz)**
TX-RX Isolation	>15dB	>20 dB	>40dB	>20dB	**>18.5dB [6]**
Isolation BW [1]	~1%	~1.6%	~15%	4.3%	**18% [7]**
Center frequency/ Modulation frequency	N/A	N/A	N/A	1	**3**
Area	3.22mm^2	0.715mm^2	1.75mm^2	0.64mm^2/25mm^2 [4]	**2.16mm^2**
ANT-RX NF	17dB	N/R	3.9dB	4.3dB [5]	**3.3-4.4dB**
TX-ANT IP1dB	-19.8dBm	+9.5dBm	N/R	N/R	**>+21.5dBm**
TX-ANT IIP3	-11dBm	N/R	+70dBm	+27.5dBm	**+19.9dBm**
P_{DC}	144.8mW	7.2mW	0	59mW	**78.4mW**

[1] BW over which an isolation better than the value quoted in the row above is maintained.

[2] Additional 3dB fundamental loss, if signals are not coherent from the antennas.

[3] Includes the proposed antenna structure as a balancing network,.

[4] Includes SMD inductors on PCB.

[5] Includes 2.3dB degradation due to LO phase noise.

[6] Limited by the mmWave test setup.

[7] This is the 1dB insertion loss BW.

N/A: Not Applicable, N/R: Not Reported

figuration explained in Section 4.2, it consists of a transmission line with a characteristic impedance Z_0 (same as the port impedance) providing a delay of $T_m/4$, sandwiched between switches clocked at ω_m with 50% duty cycle and $T_m/4$ delay between them. The operation of this structure can be explained using a standard bounce diagram, used in microwave engineering to derive the transient response of a transmission line. On Fig. 4.23(a), an incident signal from the left-hand side (Port 1) is transmitted to the output (Port 2) after one pass through the transmission line, experiencing a delay of $T_m/4$. On the other hand, an incident signal from the right-hand side (at Port 2) is transmitted to output (Port 1) after three passes through the transmission line, experiencing a delay of $3T_m/4$. The reason for this non-reciprocal transmission delay is that in the first two passes the signal hits an open termination when it reaches to the left and right hand side switches, respectively, as the switches are OFF. For a single branch, this operation can be expressed in the time-domain as

$$v_1^-(t) = v_1^+(t)[1 - m_{0,1}(t)], \tag{4.12}$$

$$v_2^-(t) = v_2^+(t)[1 - m_{0,1}(t - \frac{T_m}{4})], \tag{4.13}$$

$$v_2^-(t) = v_1^+(t - \frac{T_m}{4})m_{0,1}(t - \frac{T_m}{4}), \tag{4.14}$$

$$v_1^-(t) = v_2^+(t - \frac{3T_m}{4})m_{0,1}(t - \frac{T_m}{4} - \frac{3T_m}{4}), \tag{4.15}$$

where v_i^+ and v_i^- are the incident and transmitted signals at the i-th port and m(t) is the modulation signal of the first switch (a periodic 1/0 square-wave signal). S-parameters of a single branch can be derived by taking a Fourier transform as

$$S_{11}(\omega_{in}) = S_{22}(\omega_{in}) = \frac{1}{2}, \tag{4.16}$$

$$S_{21}(\omega_{in}) = \frac{1}{2}\exp\left(-j\frac{\pi}{2}\frac{\omega_{in}}{\omega_m}\right), \tag{4.17}$$

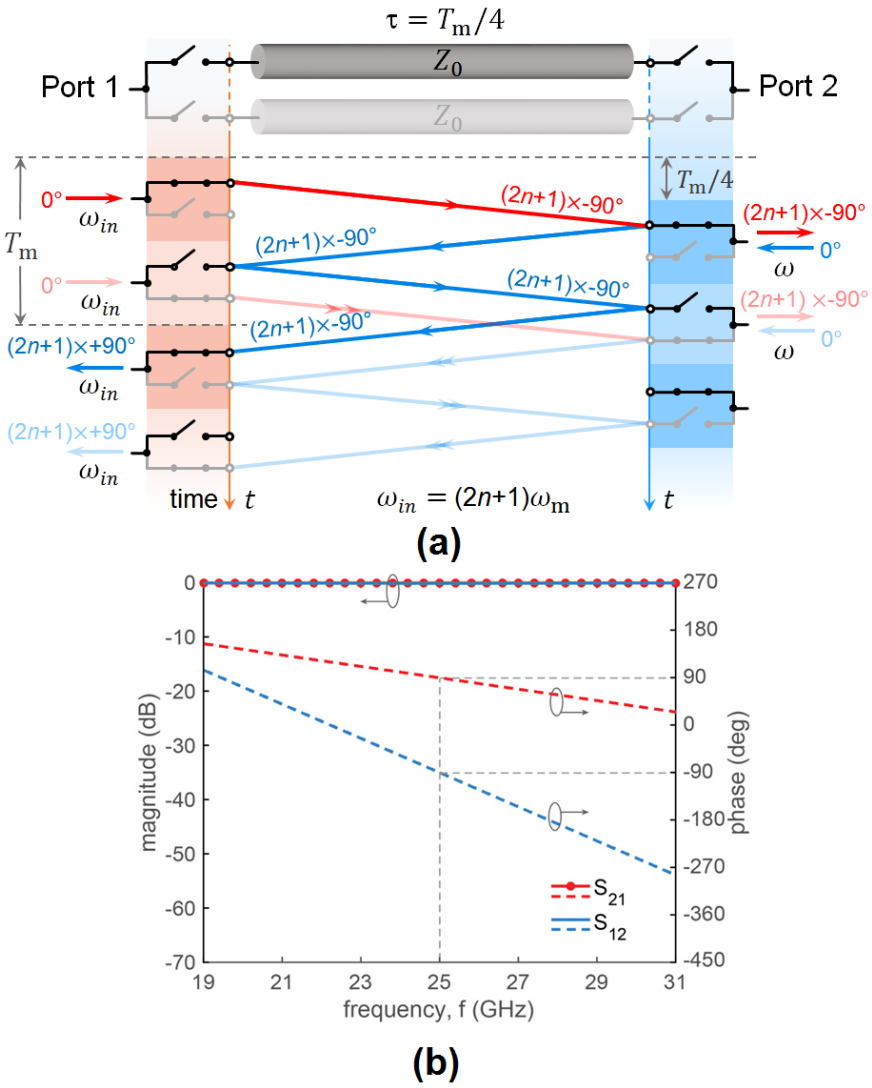

Figure 4.23: Non-reciprocal phase-shifter based on spatio-temporal conductivity modulation. (a) Bounce diagram. The incident signals in the forward and reverse directions reach to the output after one and three passes through the transmission line, respectively. (b) Scattering parameters for the single-balanced non-reciprocal phase shifter and f_m=8.33GHz. The return losses at both ports are zero for all frequencies. At 25 GHz (n=1), ideal lossless gyrator behavior is observed.

$$S_{12}(\omega_{in}) = \frac{1}{2}\exp\left(-j\frac{3\pi}{2}\frac{\omega_{in}}{\omega_m}\right), \tag{4.18}$$

where the factor 1/2 arises from the fact that the switches are off for half of the modulation period. Equations (4.17) and (4.18) shows a non-reciprocal phase response between the forward and reverse directions. Adding a second branch controlled by complementary clocks eliminates the factor of 1/2 in (4.16), (4.17) and (4.18). This also makes the structure impedance matched at all frequencies. Thus, S-parameters of the single-balanced non-reciprocal phase shifter can be expressed as

$$S(\omega_{in}) = \begin{pmatrix} 0 & \exp(-j\frac{3\pi}{2}\frac{\omega_{in}}{\omega_m}) \\ \exp(-j\frac{\pi}{2}\frac{\omega_{in}}{\omega_m}) & 0 \end{pmatrix} \tag{4.19}$$

As can be seen from (4.19), this structure behaves like a lossless non-reciprocal phase shifter over an infinite bandwidth. Fig. 4.23(b) plots the derived S-parameters of the single-balanced non-reciprocal phase shifter for f_m=8.33GHz. Additionally, this structure operates as an ideal gyrator at the odd multiples of the modulation frequency ($\omega_{in} = (2n+1)\omega_m$ where n is 0,1,2,3,...). Given the simplicity and straightforward scalability of this design, this structure holds an exciting potential for nanophotonic systems which usually achieves optical isolation by using non-reciprocal phase shifters in Mach-Zehnder interferometers [102].

4.5.2 Isolator

So far, the switches are assumed to be ideal, modulating between 0 and ∞ conductivity. However, other interesting functionalities arise, if the switches are modulated between zero resistance and a finite resistance R_{max}, as shown in Fig. 4.24(a). In this scenario, the signals partially reflect and transmit (Fig. 4.24(a)), leading to the time-domain transmission expressions

$$v_2^-(t) = v_1^+(t-\frac{T_m}{4})m_{0,1}(t-\frac{T_m}{4}) + T^2 v_1^+(t-\frac{T_m}{4})[1-m_{0,1}(t-\frac{T_m}{4})], \tag{4.20}$$

$$v_1^-(t) = T v_2^+(t-\frac{3T_m}{4})m_{0,1}(t-\frac{T_m}{4}) + \Gamma^2 v_2^+(t-\frac{3T_m}{4})m_{0,1}(t), \tag{4.21}$$

S-parameters can be derived by taking a Fourier transform as

$$S_{21}(\omega_{in}) = \frac{1}{2}(1+T^2)\exp\left(-j\frac{\pi}{2}\frac{\omega_{in}}{\omega_m}\right), \tag{4.22}$$

$$S_{12}(\omega_{in}) = T\exp\left(-j\frac{\pi}{2}\frac{\omega_{in}}{\omega_m}\right) + \frac{1}{2}\Gamma^2\exp\left(-j\frac{3\pi}{2}\frac{\omega_{in}}{\omega_m}\right), \tag{4.23}$$

where T=$2Z_0/(R_{max} + 2Z_0)$ is the transmission coefficient between the transmission line and the output ports through the resistor when the switch resistance is R_{max}, and $\Gamma = 1 - T = R_{max}/(R_{max} + 2Z_0)$ is the corresponding reflection coefficient. Fig. 4.24(a) plots (4.22) and (4.23) at $\omega_{in} = (2n+1)\omega_m$ as R_{max} is swept from 0 to ∞. For R_{max}=0, the structure is reciprocal as expected and R_{max}=∞ results in the gyrator response which is defined earlier. However, for intermediate R_{max}, the structure shows a range of amplitude and phase non-reciprocity. For $R_{max} =\sim 5.46Z_0$, the structure behaves like an isolator with infinite contrast between $|S_21|$ and $|S_12|$ becomes. This results from the fact that, withing one modulation period, the signals transmitted after one pass (first term in (4.23) and there passes (second term in (4.23) to Port 1 are out of phase, resulting in destructive interference and isolation at Port 1. . Most of the incident power at Port 2 is dissipated in the switches during their off (R_{max})state. A small fraction is converted to intermodulation products (with a conversion gain of ∼-10dB), mainly at $\omega_{in} \pm \omega_m$.

In this configuration, S_{21} is around -5.4dB, because the input and output resistors exhibit high resistance for half of the time. Similar to the non-reciprocal phase shifter, this issue can be overcome by adding a second complementary branch. However, the impedance of the transmission lines from Z_0 to $2Z_0$, and conversely tuning R_{max} to $8Z_0$ to achieve ideal isolation, perfect matching and zero insertion loss simultaneously. Since isolation is the result of destructive interference, it has a finite, yet moderately large, fractional bandwidth of 36% for $n = 1$. This operation is particularly counter-intuitive, since it shows how the presence of finite losses, through properly synchronized modulation, may be engaged to realize ideal, loss-less, broadband isolation. Specifically, absorption takes place only in the reverse path thanks to the proper synchronization of the spatio-temporal variations of conductivity, enabling ideal isolation and zero insertion loss in the forward path.

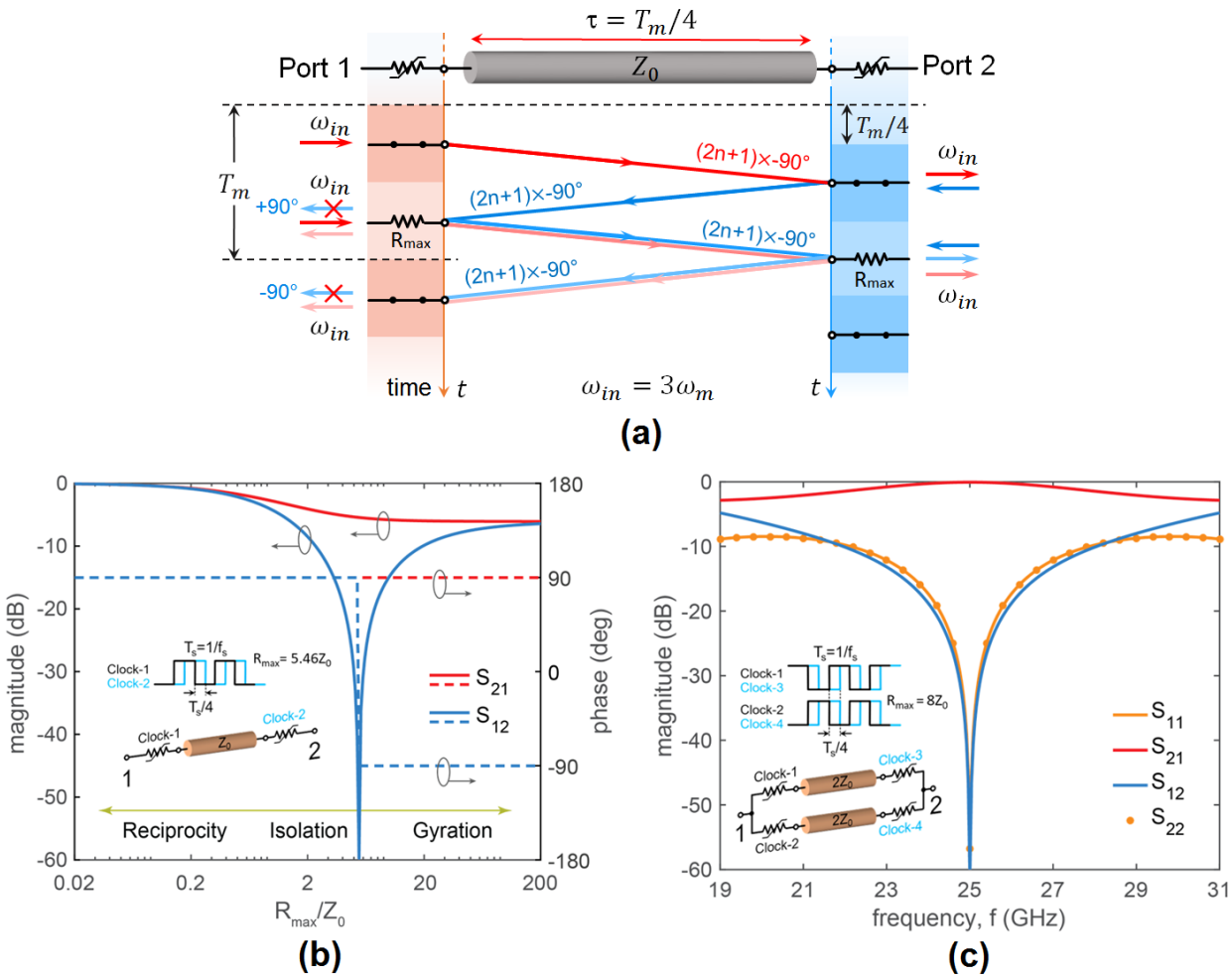

Figure 4.24: Non-reciprocal isolator based on spatio-temporal conductivity modulation. (a) Bounce diagram. The circuit is the same as in the case of the non-reciprocal phase shifter, but the switches (time-varying resistors) are modulated between 0 and a finite resitance R_{max}. (b) S_{21} and S_{12} versus R_{max} for $\omega_{in} = (2n+1)\omega_m$. (c) S-parameters of a single-balanced isolator (ω_m=8.33GHz), exhibiting ideal transmission, matching and isolation for transmission line impedance of $2Z_0$ and R_{max}=$8Z_0$.

4.6 Summary

This chapter presented the first millimeter-wave fully-integrated CMOS magnetic-free passive circulator enabled by a novel generalized spatio-temporal conductivity modulation concept. Spatio-temporal conductivity modulation achieves broadband gyrator operation over theoretically infinite BW. The 25 GHz circulator achieves 3.3 dB/3.2 dB TX-to-ANT/ANT-to-RX insertion losses (IL), respectively, with a 1 dB BW of 4.6GHz. TX-to-RX isolation is 18.3-21.2 dB (limited by the measurement setup) over the 1dB IL BW. The concept is readily scalable across frequency, and can be an enabler for 77GHz circulators as well as optical isolators.

Chapter 5

Conclusion

As a result of rising number of mobile users and their demand for data in the recent years, next generation wireless networks must handle tremendous amount of data traffic at much higher speeds. To address the future demands, this dissertation presented novel antenna interface and architecture solutions to merge two exciting technologies, mm-wave and full-duplex. Millimeter-wave FD can potentially offer wide bandwidths with increased spectral efficiency and can be used in many applications ranging from small-cell 5G base-stations, backhaul and FMCW radar to wireless links for virtual reality. However, the SI from the transmitter to its own receiver poses a tremendous challenge and novel millimeter-wave SI suppression techniques are required. To this end, two different antenna interfaces, namely a wideband reconfigurable T/R antenna pair with polarization-based antenna cancellation and a mm-wave fully-integrated magnetic-free non-reciprocal circulator, were developed.The polarization-based antenna cancellation was employed in conjunction with the RF and digital cancellation to design a 60GHz full-duplex 45nm SOI CMOS transceiver with nearly 80dB self-interference suppression.

5.1 Thesis Summary

Chapter 2 presented the novel reconfigurable polarization-based wideband antenna cancellation technique for FD applications. The technique employs collocated T/R antennas with orthogonal polarizations. An auxiliary port which is co-polarized with the transmit port is introduced on the receive antenna and terminated with a high-order reflective termination to perform SIC at the

receiver input. The technique is verified by a 4.6GHz PCB-based prototype achieving more than 50dB isolation over 300MHz SIC bandwidth, improving the SIC bandwidth 20× compared to a conventional RF canceller. The total SI suppression with cross-polarization and SIC is more than 50 dB over 300 MHz bandwidth. 50dB SI suppression is maintained even in the presence of strong nearby reflectors. The technique can be readily scaled up in frequency and be implemented on-chip at mm-wave frequencies. A 60 GHz on-chip implementation method is proposed and provides more than 50 dB SI suppression over 10 GHz BW in simulation. This chapter provided a detailed analysis of the technique, forming a foundation for the 60 GHz implementation employing on-PCB antennas described in the Chapter 3 to enable mm-wave FD operation.

Chapter 3 presented a fully-integrated 60 GHz direct-conversion transceiver in 45 nm SOI CMOS for FD wireless communication. Full-duplex operation is enabled by the polarization-based wide-band reconfigurable SIC technique presented in Chapter 2. The transceiver also employs a second RF cancellation path with >30 dB gain control and >360° phase control to suppress the residual SI further at the LNA output. With antenna and RF cancellation together, a total SI suppression of >70 dB is achieved over 1 GHz cancellation bandwidth and maintained in the presence of nearby reflectors. In conjunction with DSIC implemented in MATLAB, a full-duplex link is demonstrated over 0.7 m with a SINDR of 7.2 dB. To the best of our knowledge, this is the first demonstration of a fully-integrated mm-wave full-duplex transceiver front-end and link.

Chapter 4 presented a fully-integrated 25 GHz circulator in 45 nm SOI CMOS, demonstrating mm-wave magnetic-free passive non-reciprocity on silicon for the first time. This chapter presented a detailed analysis of the mm-wave circulator in both time and frequency domains. Millimeter-wave non-reciprocal operation is enabled by the novel concept of spatio-temporal conductivity modulation, achieving broadband non-reciprocal gyrator functionality over a theoretically infinite BW. The 25 GHz circulator achieves minimum TX-to-ANT/ANT-to-RX insertion losses (IL) of 3.3 dB/3.2 dB, respectively, with a 1- dB BW of ∼4.6GHz. TX-to-RX isolation is 18.3-21.2 dB (limited by the measurement setup) over the same BW. The spatio-temporal conductivity modulation concept is readily scalable across frequency and can be an enabler for higher-millimeter-wave (e.g. 77 GHz) circulators as well as optical isolators. The single-ended implementation of the spatio-temporal conductivity modulation technique was also discussed in this chapter, breaking amplitude and/or phase non-reciprocity and thus paving the way for realization of other magnetic-free

non-reciprocal components such as non-reciprocal phase shifter and isolator.

5.2 Future Directions

5.2.1 Millimeter-wave Full-duplex Transceivers

To date, all the reported FD efforts are single channel receivers or transceivers which focus on self-interference suppression within a wireless node. Even if they solve self-interference problem, interference from other full-duplex nodes would hamper the full-duplex operation. Additionally, beam-steering capability is essential for mm-wave full-duplex since mm-wave frequencies are sensitive to blockage by obstacles. Beamforming is an excellent solution to interference and blockage challenges to reveal the true benefits offered by mm-wave full-duplex. However, efficient SIC techniques and compact antenna interfaces are required to build a multi-element phased array full-duplex transceiver that supports SI suppression from any transmitting element to any receiving element.

In a full-duplex phased-array transceiver, there would be self-interference from any transmitting element to any receiving element. The most basic solution would be to employ previously reported RF cancellation techniques for any possible TX-RX pair. For an N×N element phased-array FD transceiver, this would imply having N^2 RF cancellers. In other words, complexity would grow quadratically with the number of antennas, which is impractical to sustain in terms of area and power consumption in large-scale phased-arrays. Therefore, it is essential to develop new antenna and RF SIC techniques which scales with a complexity close to the optimal possible (scales linearly with number of elements) to support long link distances. Additionally, these SIC techniques should achieve wide SIC bandwidths collectively to support high-speed communication (at least as wide as a single channel, 2.16GHz at 60GHz, and even wider to support channel bonding). Development of new RF and antenna techniques with low-complexity to achieve wideband self-interference suppression independent of beam-pointing direction can be an interesting research direction. FD phased-arrays can be enabled using a tunable circulator to share a single antenna between TX and RX as well as additional RF cancellation at beamforming point in a RF phase shifting architecture.

5.2.2 Millimeter-wave Circulators

Several topics may be considered for future research on mm-wave circulators. Electrical balance duplexers, such as the one in [75], achieve very high linearity and power handling through high-linearity static switch design particularly in SOI CMOS technologies. Incorporation of similar techniques to improve the linearity and power handling of integrated non-reciprocal spatio-temporally-modulated circulators is an important research direction. EBDs also feature balance impedances that are able to maintain isolation in the presence of ANT impedance variation, and exploration of such balance networks in spatio-temporally-modulated circulators is also an interesting future research topic. Additionally, device stacking techniques that are proposed in SOI process for T/R switches as well as PAs can be explored to improve power handling capability of on-chip circulators.

State-of-the-art mono-static integrated 77GHz FMCW automotive radars employs passive duplexers to achieve simultaneous transmit and receive operation, resulting in a 3dB fundamental loss. Several active quasi-circulator circuits have already been proposed to replace these passive duplexers, but their NF and linearity performance forms a bottleneck. Design of a 77GHz circulator based on the spatio-temporal conductivity modulation could be a promising topic for future research. Such a 77GHz circulator could be designed by using a higher operating to modulation frequency ratio (e.g. $\omega_{in} = 9\omega_m$, resulting in a f_m of ~8.6GHz). The delay line could be implemented on package to lower insertion loss, e.g on Rogers 4350B substrate providing 0.06dB/mm loss at 70GHz compared to 0.6dB/mm loss in GF 45nm SOI CMOS process. A mm-wave relay based on a 60GHz magnetic-free CMOS circulator could also be another promising research direction for extending the WiGig and VR link range. Design of such a mm-wave relay relatively simpler than design of mm-wave full-duplex transceiver because of the relaxed SIC and linearity requirements.

Engineering topological order in photonic metamaterials has drawn significant research interest in recent year. Inspired by the discoveries of condensed matter systems exhibiting topological order [103, 104], there have been recent research efforts to demonstrate analogous systems for classical waves (for instance, acoustic [105], [106] and photonic). To date, however, explorations of photonic topological metamaterials with non-reciprocal responses have relied on magneto-optic effects [107]. Exploration of the spatio-temporal conductivity modulation concept to enable reconfigurable magnetic-free topological photonic metamaterials can be another research direction in a more fundamental level.

Recently, non-reciprocal spatio-time modulated antennas have gained research interest. However, most of previously reported nonreciprocal antennas are based on magnetically biased ferrites [108–110] and therefore suffer from the drawbacks inherent to ferrite components discussed in Chapter 4. Extending the spatio-temporal conductivity modulation concept to fully-integrated magnetic-free non-reciprocal antennas which combine duplexing and radiation function such as in could be another interesting topic for future research.

Part I

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Part II

Appendices

Appendices

Appendix A

60 GHz RTPS and VGA Design

Nano-meter scale CMOS transistors (130nm-45nm) have maximum frequencies of oscillation (f_{max}) from 130-300GHz. As a result, high mm-wave (150-300GHz) CMOS signal sources use device non-linearity to generate harmonics in this range, either in oscillators [67, 111, 112] or in frequency multipliers [113, 114].

In [115], we demonstrated a ∼180GHz power mixer that exploits nonlinearity engineering to enhance the output harmonic content. It generates the third harmonic by mixing the fundamental with its second harmonic and engineers the amplitudes and relative phase shift of the inputs to sustain a larger swing at the device nodes. This part presents some of the 60GHz building blocks such as RTPS, VGA and Marchand balun designed in IBM 130nm CMOS for this power mixer. The dissertation author was the primary designer of these blocks.

A.0.1 60 GHz Reflection-Type Phase Shifter (RTPS)

Fig. A.1(a) shows the circuit diagram of the RTPS. It consists of a 3 dB quadrature coupler and two identical reflective loads terminating the through and coupled ports of the coupler. A broadside coupled line coupler is employed to achieve a high coupling of 3 dB in the presence of tight CMOS BEOL rules. The essential design parameters of a coupled line coupler are the even and odd mode characteristic impedances ($Z_{0,e}$ and $Z_{0,o}$) and the coupling factor (c) which are related by the equations shown in Fig. A.1(b). For 3 dB coupling, irrespective of the input matching, there should be 1 to 5.8 ratio between $Z_{0,o}$ and $Z_{0,e}$. In a 50 Ω system, this necessitates $Z_{0,e} = 120\,\Omega$ and $Z_{0,o} = 21\,\Omega$. An even mode impedance of 120 Ω is a challenging requirement to satisfy in a silicon

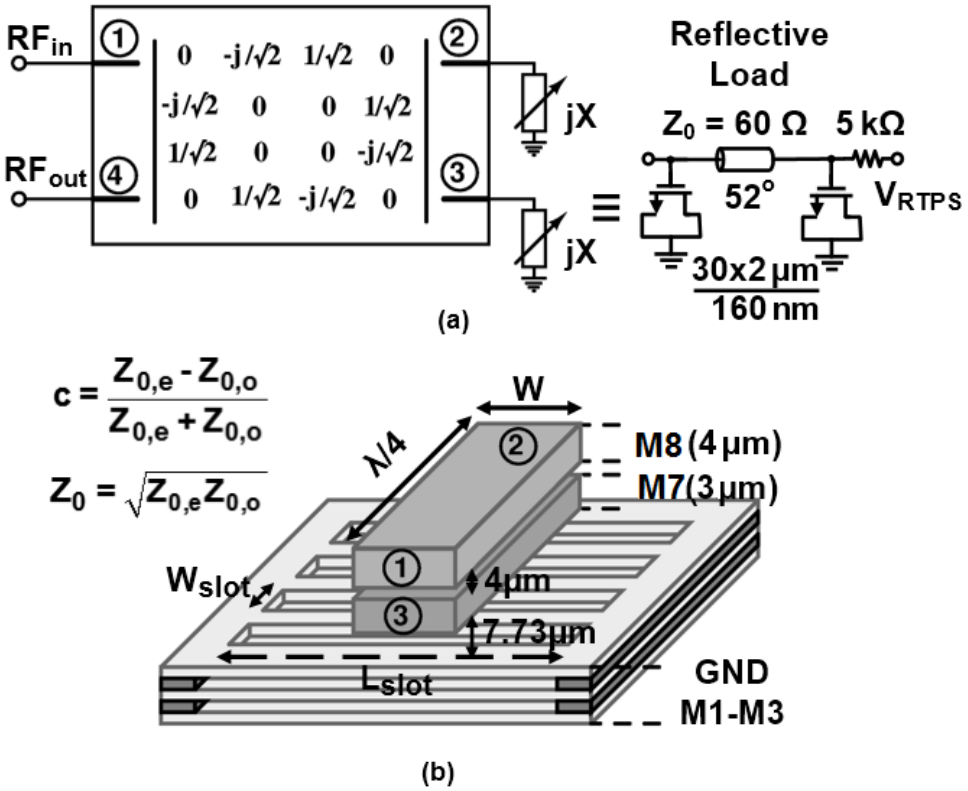

Figure A.1: (a) Circuit diagram of the RTPS. It uses a broadside coupled line 3 dB coupler and CLC reflective terminations. (b) Cross-section of the coupled line 3 dB coupler. A slow-wave technique has been used for achieving high even mode impedance as well as simplifying the design procedure.

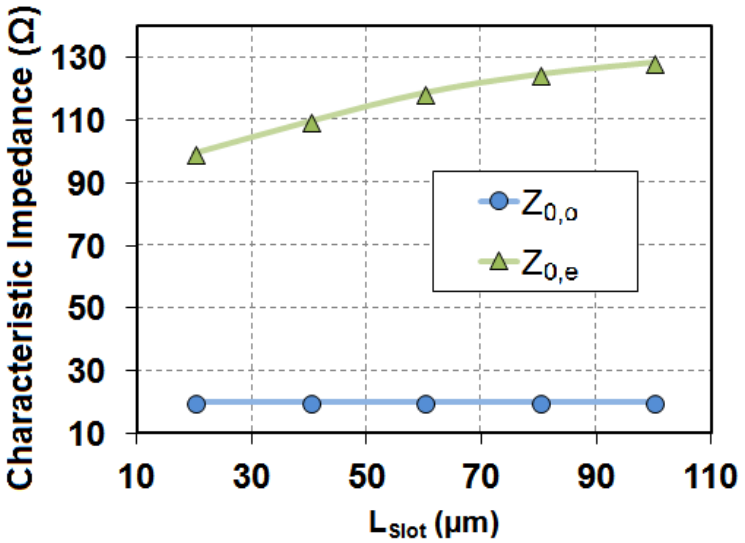

Figure A.2: Simulated characteristic impedance of the coupler in the even and odd modes. $W = 12\,\mu$m, $W_{slot} = 10\,\mu$m and L_{slot} is varied.

based process. As a result, authors in [116] sacrifice input matching, whereas authors in [117] use thinner metal layers and totally remove the ground plane underneath the coupler to achieve higher inductance per unit length at the expense of increased insertion loss. A differential broadside coupled line coupler with co-planar striplines over floating ground strips was reported in [118] and it harnesses the lateral spacing between coplanar striplines to achieve a high $Z_{0,e}$. However, this approach is not applicable to single-ended broadside couplers. In this work, the RTPS employs a slow-wave technique in the single-ended coupled line coupler design to satisfy high $Z_{0,e}$ requirement.

Fig. A.1(b) depicts the cross-section of the coupled line coupler. Vertically coupled microstrip lines are implemented using the two topmost thick metal layers, $M8$ and $M7$, of the 130 nm CMOS process BEOL to achieve lower loss. A ground plane with slots is employed under the coupled microstrip lines to shield the coupler structure from the lossy silicon substrate. The ground plane is formed by stacking $M1$, $M2$ and $M3$ metals to satisfy the metal density rules. Stacking also provides a thickness greater than 3δ, where δ is the skindepth, at 60 GHz for the return current flow and reduces the loss. $10\,\mu$m wide slots separated by $10\,\mu$m spacing are opened, orthogonal to the signal propagation direction, in the ground plane for creating the slow-wave effect [119].

The even and odd mode characteristic impedances of the coupler are simulated in IE3D. Fig.

A.2 depicts the even and odd mode characteristic impedances as the slot length is varied. In the even mode, when the coupled lines are excited with same polarity, the return current flows through the ground plane. Since the slots in the ground plane are orthogonal to the signal propagation direction, the return current in the signal direction is forced to flow far away from the microstrip lines. This increases the inductance per unit length. As a result, the even mode characteristic impedance increases with increasing slot length. The slots boost the even mode impedance by decreasing the capacitance per unit length as well. On the other hand, the current flows through one of the microstrips and returns through the other in the odd mode. Therefore, magnetic fields cancel everywhere except between the top and bottom lines. Electric field is also confined between two parallel lines in this mode. Accordingly, changing the slot length does not have any effect on the inductance and capacitance per unit length and thus the characteristic impedance in the odd mode.

The slow-wave technique also simplifies the coupler design to a two step procedure. First, the odd mode impedance can be set by changing the width, W, of the signal lines. Then the even mode impedance can be increased up to the desired value by using the slot length, L_{slot}. The physical design parameters, W and L_{slot} were found based on this two step procedure in IE3D. $Z_{0,o}$ of $21\,\Omega$ and $Z_{0,e}$ of $120\,\Omega$ require a width of $12\,\mu$m and a slot length of $60\,\mu$m. Quarter-wavelength in even and odd modes corresponds to approximately $500\,\mu$m length at 60 GHz. The coupled microstrips are bent to conserve chip area. Simulations show that the coupler achieves 3 dB coupling with 0.8 dB insertion loss (varies by 0.1 dB between the coupled and thru port) and 35 dB isolation at 60 GHz. The simulated phase difference between the through and coupled ports is $84°\pm1°$ between 40 GHz and 70 GHz. The deviation from 90° is attributed to the difference between the even and odd mode propagation constants. This can be improved by including another parameter in the design procedure which could be asymmetry in the widths as in [118], or asymmetry in the position of the coupled lines as in [120].

The effect of the coupler phase imbalance on the RTPS performance is analyzed to the first order assuming there is no amplitude imbalance. Assuming there is ϕ imbalance between S_{21} and S_{31} (e.g. $\angle S_{21}$ and $\angle S_{31}$ are -90°+ϕ and 0° respectively) the signals from reflected terminations will be -180°+2ϕ out of phase at the input port instead of 180°. Then, S_{11} of the RTPS can be expressed as

$$|S_{11,RTPS}| = \sqrt{\frac{1 - cos(2\phi)}{2}} \tag{A.1}$$

According to (A.1), S_{11} of the RTPS would be lower than -15 dB up to a coupler phase imbalance of 10°. Similarly, the forward transmission coefficient of the RTPS can be calculated in the presence of a coupler phase imbalance as

$$|S_{21,RTPS}| = |S_{21}S_{42}\Gamma_L + S_{31}S_{43}\Gamma_L| \tag{A.2}$$

where S_{21}, S_{31}, S_{42} and S_{43} are the scattering parameters of the coupler in the presence of phase imbalance and Γ_L is the load reflection coefficient. Due to symmetry, S_{31} and S_{42} are equal both in magnitude and phase and unitary condition requires $\angle S_{21}$+$\angle S_{43}$=180°. Thus, using $|S_{21}| = |S_{31}| = |S_{42}| = |S_{43}| = 1/\sqrt{2}$, $\angle S_{21} = -90 + \phi$ and $\angle S_{43} = -90 - \phi$, (A.2) simplifies to

$$S_{21,RTPS} = cos(\phi)\Gamma_L e^{-j90} \tag{A.3}$$

Equation (A.4) indicates that phase imbalance in the coupler does not cause any variation in the overall RTPS phase shift. Loss of the RTPS in dB is equal to $20log|cos\phi| + 20log|\Gamma_L|$ (the coupler is assumed to be lossless). As a result, loss of the RTPS increases with increasing phase imbalance in the coupler. 10° phase imbalance would degrade RTPS loss by 0.13 dB, which is negligible compared to the loss from the reflective termination.

Using S-parameters of an ideal coupled line coupler (Fig. A.1(a)), the phase shift of the RTPS can be expressed as [118]

$$\angle S_{21,RTPS} = -90 - 2\tan^{-1}\left(\frac{X}{Z_0}\right) \tag{A.4}$$

where X is the reactance of the reflective loads and Z_0 is the characteristic impedance of the coupler. A π-type C-L-C termination is used as variable reactance in the RTPS to achieve 180° continuous phase range. Fig. A.1(a) depicts the circuit diagram of the reflection termination. Varactors are used as shunt capacitances and are implemented using $30 \times 2\,\mu$m/160 nm FET devices whose source and drain are connected together. The control voltage is applied at the gate terminal to vary the capacitance. The impedance of the reflective load is given by

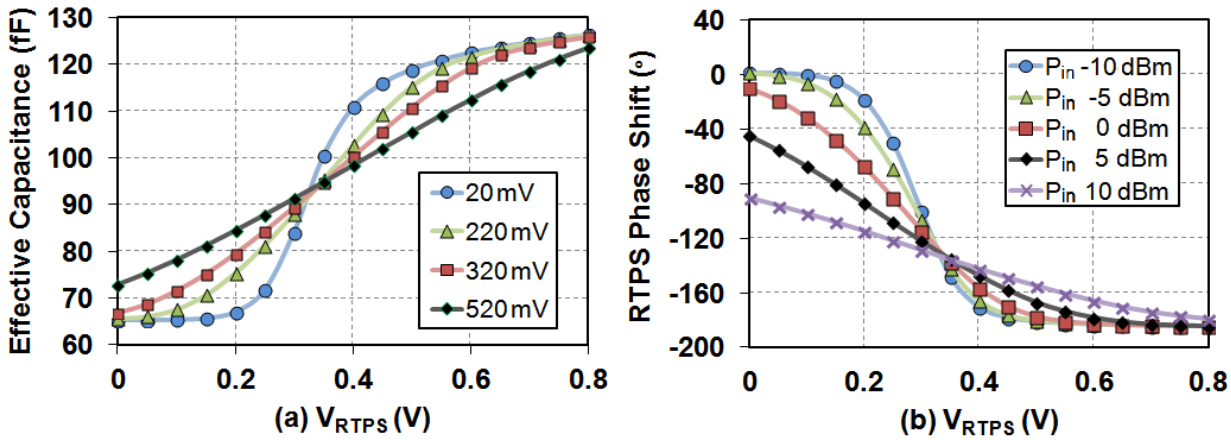

Figure A.3: (a) Simulated effective varactor capacitance for different signal amplitudes showing large signal effects. Larger signal amplitude across the varactor causes a reduction in capacitance range and tuning ratio (b) Simulated phase shift of the RTPS under large signal operation for different input power levels.

$$Z_L = \frac{1 - \omega^2 L_{eff} C_v}{(2 - \omega^2 L_{eff} C_v) j\omega C_v} \tag{A.5}$$

where C_v is the varactor capacitance and L_{eff} is the effective inductance of the transmission line. For the $30 \times 2\,\mu$m/160 nm MOS varactor, the simulated minimum capacitance, $C_{v,min}$, is 65 fF with a tuning ratio of 1.9 at 60 GHz when the control voltage is swept from 0 to 0.8 V (Fig. A.3). The quality factor of the varactor varies from 18 to 4. By setting $L_{eff} = 2/\omega^2 C$ where $C = (C_{v,max} + C_{v,min})/2$, a phase range more than 180° is achieved (Fig. A.3(b)). The effective inductance is implemented using a CPW transmission line with 60 Ω characteristic impedance and 360 μm length.

In this work, the power incident on the RTPS was +8 dBm in simulation. Therefore, the phase shift of the RTPS is also evaluated under large signal operation. Fig. A.3(b) depicts the simulated phase shift as V_{RTPS} is varied for different input powers at 60 GHz. There are two important observations from Fig. A.3(b): 1) the RTPS phase shift becomes more linear with increasing input power and 2) after some point, pushing more power into RTPS causes compression in phase range. The phase compression becomes worse as the input power is increased. These large signal effects on the RTPS phase shift have been overlooked in the literature although they are due to the same

mechanism which causes AM/PM conversion in voltage controlled oscillators. The large signal swing across the varactor device modulates the capacitance throughout the signal period and thus the effective capacitance of the varactor is averaged over each period [121]. The resulting effective capacitance (ratio of the root mean square, RMS, of the current to RMS of the derivative of the voltage with respect to time) versus RTPS control voltage (V_{RTPS}) for different signal amplitudes is shown in Fig. A.3(a). As can be seen, the effective varactor capacitance varies more linearly with V_{RTPS} for larger signal amplitudes, resulting in a more linear RTPS phase shift. Additionally, the varactor tuning ratio reduces as the signal amplitude increases and this explains the phase compression for higher input powers in Fig. A.3(b). The small signal phase shift of the RTPS should be designed with margin to make sure there is enough phase range under large signal operation. Designing the RTPS for a lower input and output impedance would also mitigate the phase compression issue since the voltage swing across the varactors would be lower for the same input power.

A.0.2 60 GHz Variable Gain Amplifier

A variable gain amplifier is used to compensate the insertion loss variation in the RTPS across the control voltage. Fig. A.4(a) shows the block diagram of the VGA. Variable gain is achieved by placing a variable attenuator between two amplifier stages as in [122]. Fig. A.4(b) depicts the circuit diagram of the amplifiers, including bias circuitry. The amplifiers are implemented in stacked topology due to its higher reverse isolation compared to a common source stage. High reverse isolation helps in keeping the VGA input and output matching independent of the attenuation settings. Supply voltage of the amplifiers is scaled to 3 V to improve the power handling capability [64]. The input and output of the amplifiers are conjugately matched to 50 Ω using L-type matching networks.

The schematic of the variable attenuator is shown in Fig. A.4(c). It uses a variable shunt resistor, implemented as a MOS transistor operating in the deep triode region ($V_{DS} = 0\,V$ for zero power consumption). S_{21} of the attenuator, neglecting the transmission line loss and assuming that the shorted stub inductance L_p and the total capacitance at the drain C_d resonate, is given by

$$S_{21} = \frac{2R_v}{Z_0 + 2R_v} \tag{A.6}$$

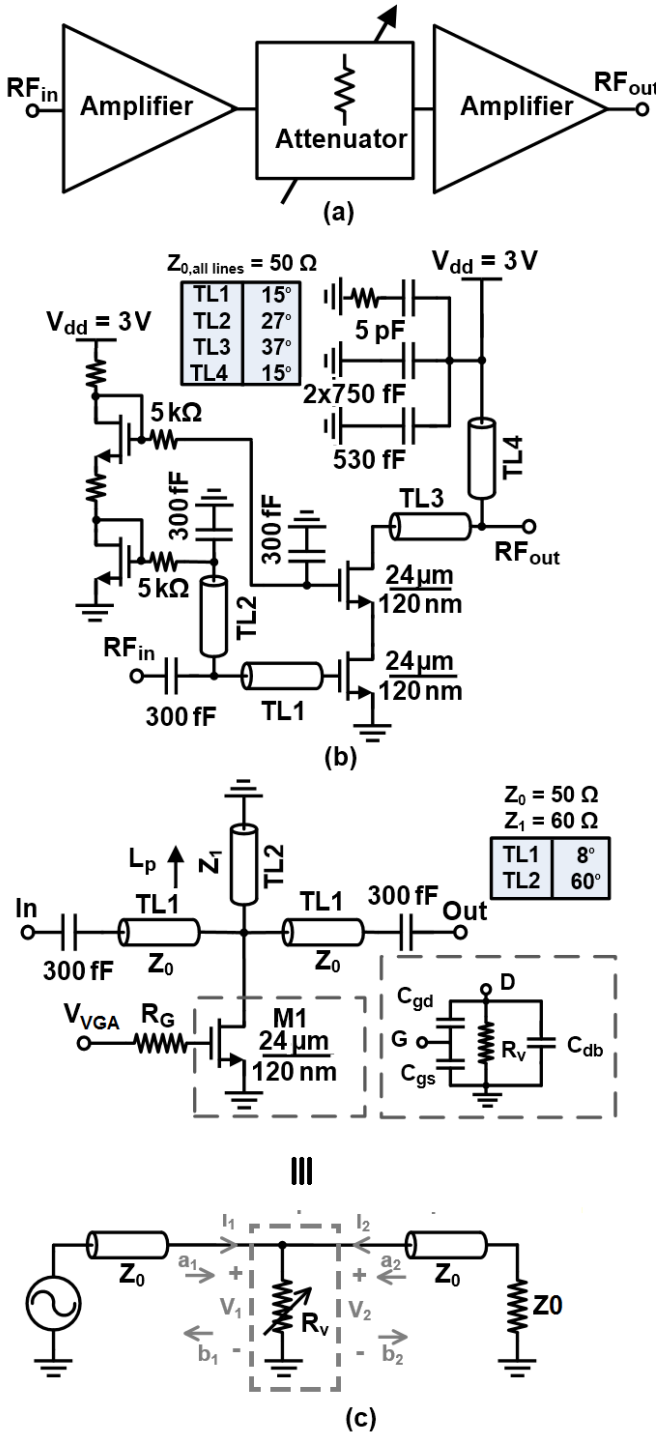

Figure A.4: (a) Block diagram of the variable gain amplifier. (b) Circuit diagram of the amplifiers. (c) Circuit diagram of the variable attenuator.

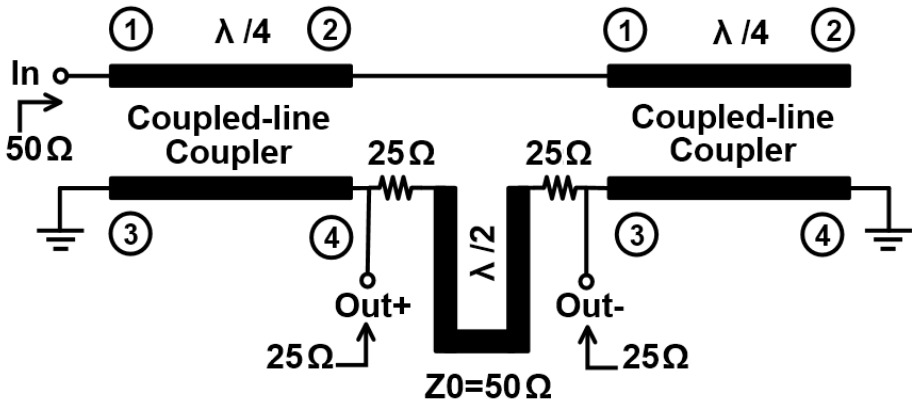

Figure A.5: Circuit diagram of the impedance transforming Marchand Balun with a passive cancellation network between the balanced outputs. The passive network improves the output return losses and the isolation between output ports.

where R_v is the channel resistance which can be varied by the gate voltage. A $24 \times 1\,\mu$m/120 nm device can provide 16 Ω on-resistance at 1.5 V, and is used to obtain approximately 8 dB attenuation range. The control voltage is applied through a 5 $k\Omega$ resistor to make the gate float at ac. A floating gate reduces the total capacitance at the drain of $M1$ to $C_{gs}//C_{gd}+C_{db}$, and in return a larger shunt inductance is required to resonate it out. Assuming a constant quality factor, the shunt parasitic resistance of the shunt inductor increases and the loss of the attenuator (insertion loss when the transistor is OFF) reduces. The attenuator is ac-coupled at the input and output to the amplifier stages with 300 fF MiM capacitors.

A.0.3 60 GHz Marchand Balun

An impedance transforming Marchand balun was integrated on chip to convert the single-ended output of the Wilkinson to a differential signal. Fig. A.5 shows the circuit diagram of the Marchand balun. It consists of two identical quarter-wave length coupled line coupler sections and a passive network between balanced output ports. The required coupling factor for the couplers is −4.8 dB when all the ports are terminated with 50 Ω [123]. Due to limited time at the design phase, two copies of the 3 dB coupled line coupler designed for the RTPS are used in the Marchand design. Using 3 dB couplers entails output impedance of 25 Ω for achieving −3 dB power transfer to each

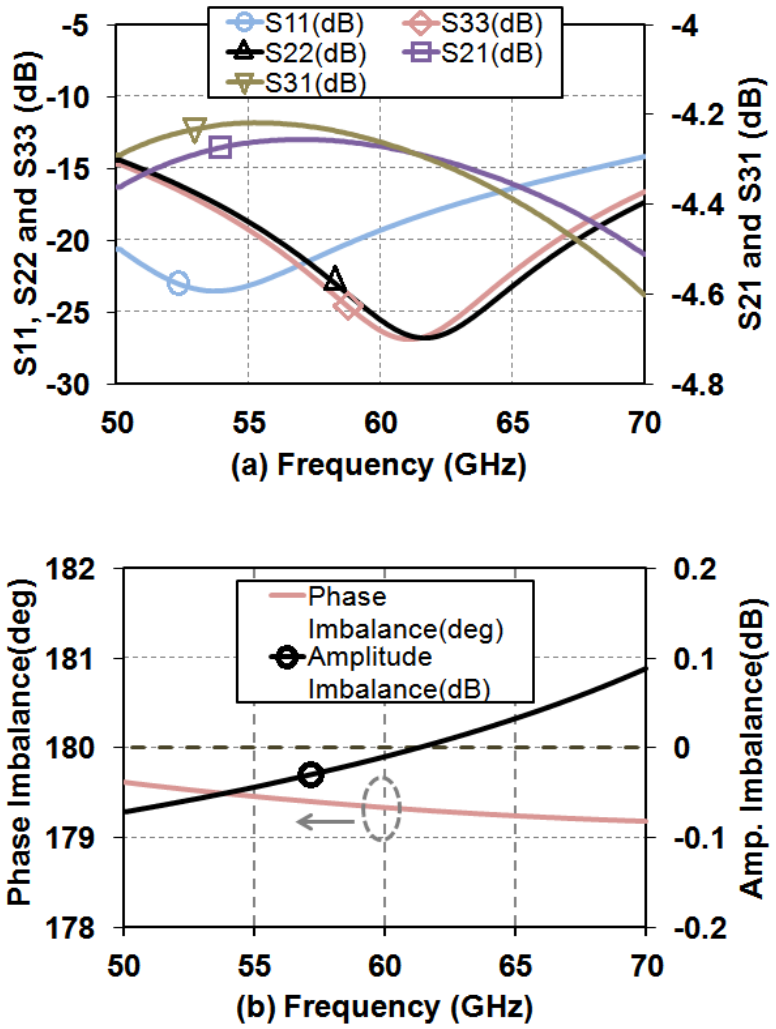

Figure A.6: Simulated performance of the Marchand Balun including (a) input and output return losses and insertion loss, and (b) phase and amplitude imbalance.

port. The conventional Marchand balun suffers from poor output matching and isolation between the balanced outputs. A passive network consisting of two 25 Ω resistances and half-wave length transmission line was integrated on chip between the balanced outputs to improve the output matching and isolation [124]. Without adding this network, the best attainable output return loss (assuming 25 Ω output port impedance) and isolation between outputs would be theoretically 6 dB [123]. The passive network introduces another path with 6 dB attenuation and 180 degree phase shift for perfect cancellation between the balanced outputs. This helps to reduce the power drive requirements of the amplifier chains feeding the doubler and improves the overall conversion loss. Additionally, the improved isolation between balanced ports enhances the stability of the differential amplifier chain.

The simulated performance of the balun is shown in Fig. A.6. The input and output return losses are better than 15 dB (Fig. A.6(a)) and the balun achieves an isolation better than 22 dB between balanced ports from 50 GHz to 70 GHz. The simulated insertion loss of the balun (Fig. A.6(a)) is lower than 1.6 dB in the same frequency range. The simulated phase and amplitude imbalances of the balun are within 1° and 0.1 dB, respectively.

A.0.4 Measurements

A cascaded RTPS and VGA breakout is tested through RF probing using a chip-on-board based setup in order to characterize the phase shift and amplitude control capability in the fundamental path. Fig. A.7 shows the die microphotograph of the RTPS-VGA test breakout which occupies $1.15 \times 0.36\,\mathrm{mm}^2$, not including pads. S-parameters of the RTPS-VGA breakout are measured up to 65 GHz using dc−67 GHz Cascade Infinity GSG probes and an Anritsu 37397E Lightning VNA. The phase shift versus RTPS control voltage V_{RTPS} is shown in Fig. A.8(a), for 60 GHz and 63 GHz with the VGA control voltage $V_{VGA} = 0\,\mathrm{V}$ so that the VGA provides maximum gain. The RTPS-VGA breakout achieves 158° and 137° phase variation range at 60 GHz and 63 GHz, respectively. The gain of the RTPS-VGA varies from −6.8 dB to −0.3 dB and from −1.2 dB to 3.6 dB across V_{RTPS} at 60 GHz and 63 GHz respectively, as seen in Fig. A.8(b). As the VGA control voltage is fixed at its highest gain setting, Fig. A.8(a) and Fig. A.8(b) reveal the phase shift and insertion loss variation characteristic of the RTPS. Large variation of the insertion loss across phase settings is the main drawback of reflection type phase shifters and it can be compensated using the VGA

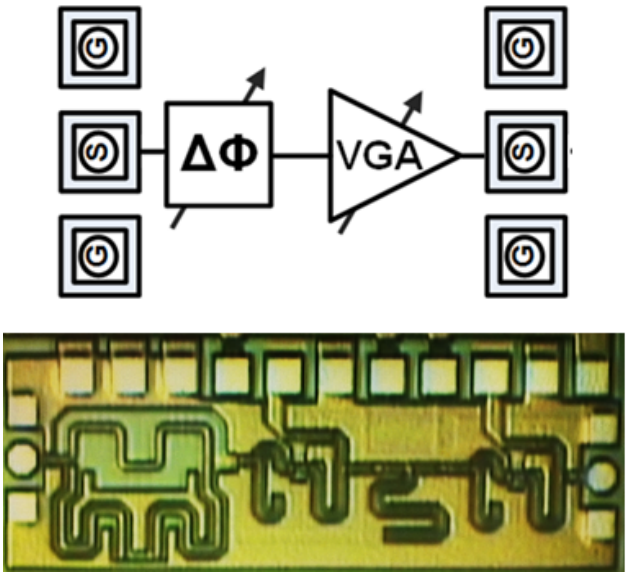

Figure A.7: Die photo of the test structure implemented to characterize the phase shift and gain of the 60GHz RTPS and VGA cascade in the fundamental path.

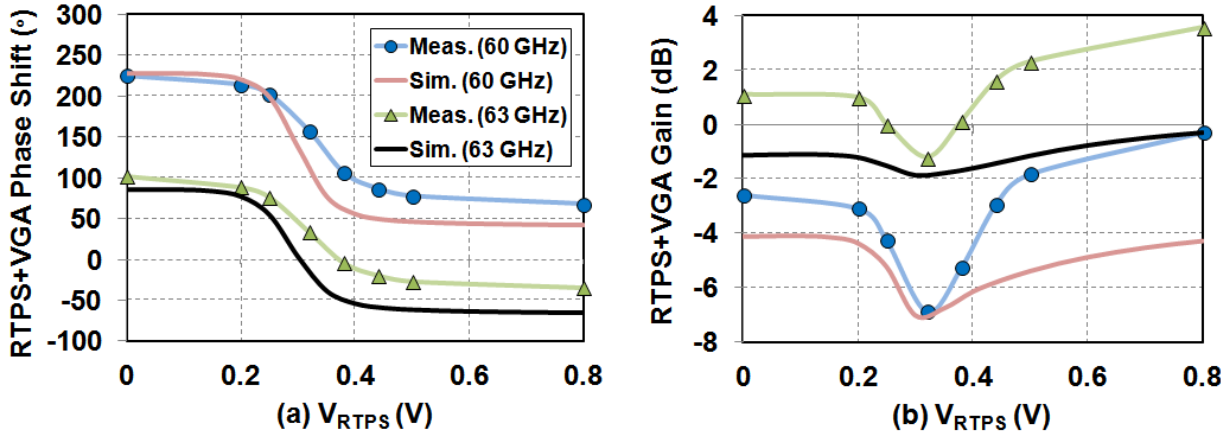

Figure A.8: Insertion (a) phase shift and (b) gain of the RTPS-VGA breakout versus RTPS control voltage at 60 and 63 GHz. For these measurements the VGA is set to maximum gain ($V_{VGA} = 0\,\mathrm{V}$).

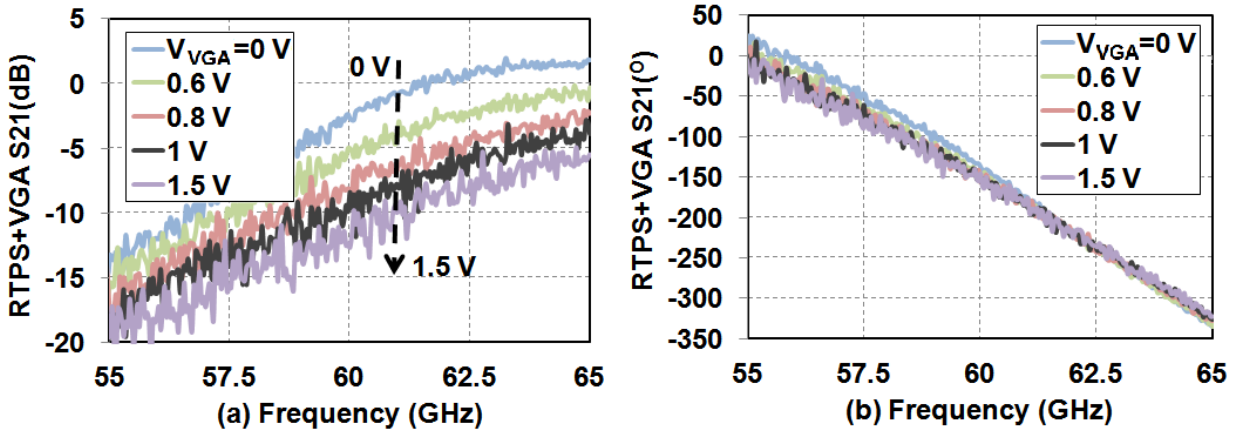

Figure A.9: Insertion (a) gain and (b) phase-shift of the RTPS-VGA breakout versus VGA control voltage. For these measurements, $V_{RTPS} = 0\,\mathrm{V}$.

in this work. Fig. A.9(a) and Fig. A.9(b) show the gain and the insertion phase of the RTPS-VGA breakout, respectively, across frequency for different attenuator control voltages, V_{VGA}, while V_{RTPS} is kept at 0 V. The VGA provides 8.4 dB analog gain control with a phase variation less than 8°.

Appendix B

Lorentz Non-Reciprocity in Spatio-Time-Varying Medium

Lorentz Reciprocity is conventionally derived from the source-free (J=0) Maxwell equations in the frequency domain, assuming a constant permittivity constant. Here, this part derives the reciprocity equation in a spatio-temporally varying medium (e.g. permittivity is a function of distance and time, $\epsilon(z,t)$).

B.1 Wave Equation

Starting from Maxwell Equation in time domain

$$\nabla \times E(z,t) = -\frac{\partial B(z,t)}{\partial t} \tag{B.1}$$

$$\nabla \times H(z,t) = \frac{\partial D(z,t)}{\partial t} + J_T \tag{B.2}$$

where $B = \mu H$ and $D = \epsilon(z,t)E$ (spatio-temporal variation in permittivity), we can derive the wave equation for time-varying permittivity. Taking $\nabla\times$ of (B.1)

$$\nabla \times \nabla \times E(z,t) = -\mu \frac{\partial \nabla \times H(z,t)}{\partial t}. \tag{B.3}$$

using vector identity $\nabla \times \nabla \times E = \nabla(\nabla.E) - \nabla^2 E$ in the source free region (J_T=0, $\nabla.D = 0$ and in return $\nabla(\nabla.E)$=0), the wave equation is

$$\nabla^2 E(z,t) - \frac{\partial^2 \epsilon(z,t) E(z,t)}{\partial t^2} = 0. \tag{B.4}$$

Assuming $\epsilon(z,t) = \epsilon_0 + \epsilon_m(z,t)$ where $\epsilon_m(z,t) = \cos(\omega_m t - \beta_m z)$, (B.4) becomes

$$\nabla^2 E(z,t) - \frac{1}{c^2}\frac{\partial^2 E(z,t)}{\partial t^2} - \frac{\partial^2 \epsilon_m(z,t) E(z,t)}{\partial t^2} = 0, \tag{B.5}$$

where $c = 1/\sqrt{\mu\epsilon_0}$. Solution to the wave equation is in the form of $E(z,t) = E_k(z)e^{j\omega_k t} + E_k^*(z)e^{-j\omega_k t}$. There would be terms at the fundamental frequency ω_s and mixing frequencies $\omega_s + \omega_m$ and $\omega_s - \omega_m$. We are not interested in the exact solution of the wave equation here.

B.2 Lorentz Non-Reciprocity

Using the general solution in (B.1)

$$\nabla \times (E_k(z)e^{j\omega_k t} + E_k^*(z)e^{-j\omega_k t}) = -\mu\frac{\partial}{\partial t}(H_k(z)e^{j\omega_k t} + H_k^*(z)e^{-j\omega_k t}) \tag{B.6}$$

Noting that we can just use $e^{j\omega_k t}$ (conjugates give the same equation),

$$\nabla \times E_k(z)e^{j\omega_k t} = -j\omega_k \mu H_k(z)e^{j\omega_k t} \tag{B.7}$$

$$\nabla \times E_k(z) = -j\omega_k \mu H_k(z) \tag{B.8}$$

Re-arranging (B.2) in source-free region and then using the general solution

$$\nabla \times H(z,t) = \frac{\partial \epsilon(z,t)}{\partial t}E(z,t) + \epsilon(z,t)\frac{\partial E(z,t)}{\partial t} \tag{B.9}$$

$$\nabla \times H_k(z) = \left(\frac{\partial \epsilon(z,t)}{\partial t} + j\omega_k \epsilon(z,t)\right) E_k(z) \tag{B.10}$$

Assuming E_{k1} and H_{k1} are the fields when the propagation and modulation in the same direction whereas E_{k2} and H_{k2} are the fields when they are in opposite directions (this can be simply achieved by changing the permittivity modulation direction, $\epsilon(z,-t) = \cos(\omega_m t + \beta_m z)$) .

$$H_{k2}(z).\nabla \times E_{k1}(z) = -j\omega_k \mu H_{k2}(z)H_{k1}(z) \tag{B.11}$$

$$E_{k2}(z).\nabla \times H_{k1}(z) = // \left(\frac{\partial \epsilon(z,t)}{\partial t} + j\omega_k \epsilon(z,t) \right) E_{k2}(z) E_{k1}(z) \tag{B.12}$$

Similarly

$$H_{k1}(z).\nabla \times E_{k2}(z) = -j\omega_k \mu H_{k1}(z) H_{k2}(z) \tag{B.13}$$

$$E_{k1}(z).\nabla \times H_{k2}(z) = \left(\frac{\partial \epsilon(z,-t)}{\partial t} + j\omega_k \epsilon(z,-t) \right) E_{k1}(z) E_{k2}(z) \tag{B.14}$$

Substracting (B.11) from (B.14) and using vector identity $\nabla.(A \times B) = (\nabla \times A).B - A.(\nabla \times B)$

$$-\nabla.(E_{k1}(z) \times H_{k2}(z)) = \left(\frac{\partial \epsilon(z,-t)}{\partial t} + j\omega_k \epsilon(z,-t) \right) E_{k1}(z) E_{k2}(z) + j\omega_k \mu H_{k2}(z) H_{k1}(z) \tag{B.15}$$

Similarly, substracting (B.12) from (B.13)

$$\nabla.(E_{k2}(z) \times H_{k1}(z)) = -\left(\frac{\partial \epsilon(z,t)}{\partial t} + j\omega_k \epsilon(z,t) \right) E_{k2}(z) E_{k1}(z) - j\omega_k \mu H_{k1}(z) H_{k2}(z) \tag{B.16}$$

Adding (B.15) and (B.16), we obtain Lorentz Reciprocity equation:

$$\nabla.(E_{k2}(z) \times H_{k1}(z) - E_{k1}(z) \times H_{k2}(z)) = \left(\frac{\partial \epsilon(z,-t)}{\partial t} - \frac{\partial \epsilon(z,t)}{\partial t} + j\omega_k \epsilon(z,-t) - j\omega_k \epsilon(z,t) \right) E_{k2}(z) E_{k1}(z) \tag{B.17}$$

Observations from (B.16)

- If $\epsilon(z,t)$ is a constant (spatio-time-invariant), the right side of (B.16) becomes zero, showing Lorentz Reciprocity, as expected.
- If $\epsilon(z,t)$ is only a function of space (time-invariant), the right side of (B.16) becomes zero, showing Lorentz Reciprocity. We conclude that spatial variation cannot break Lorentz Reciprocity by itself.
- If $\epsilon(z,t)$ is only a function of time (spatio-invariant), the right side of (B.16) becomes zero for even functions (Lorentz Reciprocal) and non-zero (Lorentz Non-Reciprocal) for odd functions conditional upon $\epsilon(z,t) \neq \epsilon(z,-t)$ and $\frac{\partial \epsilon(z,t)}{\partial t} \neq \frac{\partial \epsilon(z,t)}{\partial t}$. We conclude that periodic time modulation (e.g. $\epsilon_m(z,t) = \sin(\omega_m t)$) cannot break Lorentz Reciprocity by itself. It should also be noted that any function which can be written as superposition of $\sin(\omega_m t)$s and $\cos(\omega_m t)$s cannot break Lorentz Reciprocity by itself.

- If a spatio-time periodic modulation of $\epsilon(z,t) = \epsilon_m(z,t) = \epsilon_m \cos(\omega_m t - \beta_m z)$ is used, (B.17) simplifies to

$$\nabla.(E_{k2}(z) \times H_{k1}(z) - E_{k1}(z) \times H_{k2}(z)) = 2\omega\epsilon_m \left(\cos(\omega t) - j\sin(\omega t)\right) \sin(\beta z) E_{k2}(z) E_{k1}(z) \tag{B.18}$$

$$\nabla.(E_{k2}(z) \times H_{k1}(z) - E_{k1}(z) \times H_{k2}(z)) = 2\omega\epsilon_m e^{-j\omega t} \sin(\beta z) E_{k2}(z) E_{k1}(z) \tag{B.19}$$

As can be seen, it breaks Lorentz Reciprocity for any values of t, if $\sin(\beta z) \neq 0$.

Appendix C

List of Acronyms

ADCs Analog-to-Digital Converters

ANT Antenna

AR Axial Ratio

ATT Attenuator

AUX Auxiliary

BB baseband

BEOL Back-End-of-Line

BER Bit Error Rate

BPSK Binary Phase-Shift Keying

BW Bandwidth

CDMA Code-Division Multiple Access

CMOS Complementary Metal-Oxide-Semiconductor

CPW Coplanar Waveguide

CS Common-Source

CW Continuous-Wave

DACs Digital-to-Analog Converters

DSIC Digital Self-Interference Cancellation

DR Dynamic Range

EBD Electrical Balance Duplexer

EIRP Effective Isotropic Radiated Power

EM Electromagnetic

ENOB Effective Number of Bits

ESD Electrostatic Discharge

EVM Error Vector Magnitude

FD Full-duplex

FET Field-Effect Transistor

FDD Frequency-Division Duplexing

FIR Finite Impulse Response

FMCW Frequency Modulated Continuous Wave

HD Half-Duplex

IC Integrated Circuit

IIP3 input third-order intercept point

IL Insertion Loss

IM3 third-order inter-modulation

IM2 second-order inter-modulation

IP3 third-order intercept point

LM Link Margin

LMS Least Mean Squares

LNA Low-Noise Amplifier

LO Local Oscillator

LPTV Linear Periodically Time-Varying

LPFs Low-Pass Filters

LTI Linear Time-Invariant

LTV Linear Time-Varying

MAC Medium-Access Control

MIMO Multi-In-Multi-Out

NF Noise Figure

NRZ Non-Return-to-Zero

PA Power Amplifier

PCB Printed Circuit Board

PAE Power Added Efficiency

PIA Phase-Inverting Amplifier

PPF Polyphase Filter

PPG Pulse Pattern Generator

PRBS Pseudo-Random Binary Sequence

PS Phase Shifter

QAM Quadrature Amplitude Modulation

RBW Resolution Bandwidth

RF Radio Frequency

RTPS Reflection-type Phase Shifter

RX Receiver

SFDR Spurious-Free Dynamic Range

SIC Self-Interference Cancellation

SI Self-Interference

SINDR Signal-to-Interference-Noise-and-Distortion Ratio

SPI Serial Parallel Interface

SOI Silicon on Insulator

SNR Signal-to-Noise Ratio

STAR Simultaneous Transmit and Receive

TDD Time-Division Duplexing

T/R Transmit/Receive

TX Transmitter

VGA Variable-Gain Amplifier

VM Vector Modulator

VNA Vector Network Analyzer

VR Virtual Reality

WPAN Wireless Personal Area Network