

Switched-Capacitor RF Receivers for High Interferer Tolerance

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Abstract

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The demand for broadband wireless communication is growing rapidly, requiring more spectrum resources. However, spectrum usage is inefficient today because different frequency bands are allocated for different communication standards and most of the bands are not highly occupied.

Cognitive radio systems with dynamic spectrum access improve spectrum efficiency, but they require wideband tunable receiver hardware. In such a system, a preselect filter is required for the RF receiver front end, because an out-of-band (OB) interferer can block the front end or cause distortion, desensitizing the receiver. In a conventional solution, off-chip passive filters, such as surface-acoustic-wave (SAW) filters, are used to reject the OB interferer. However, such passive filters are hardly tunable, have large area, and are very expensive. On-chip, high-selectivity, linearly tunable RF filters are, therefore, a hot topic in RF front-end research. Switched-capacitor (SC) RF filters, such as N-path filters, feature good linearity and tunability, making them good candidates for tunable RF filters. However, N-path filters have some drawbacks: notably, a poor harmonic response and limited close-by blocker tolerance.

This thesis presents the design and implementation of several interferer-tolerant receivers based

on SC technology. We present an RF receiver with a harmonic-rejecting N-path filter to improve the harmonic response of the N-path bandpass filter. It features tunable narrowband filtering and high attenuation of the third- and fifth-order LO harmonics at the LNA output, which improves the blocker tolerance at LO harmonics. The 0.2–1 GHz RF receiver is implemented in a 65 nm CMOS process. The blocker 1 dB compression point (B1dB) is -2.4 dBm at a 20 MHz offset, and remains high at the third- and fifth-order LO harmonics. The LNA's reverse isolation helps keep the LO emission below -90 dBm. A two-stage harmonic-rejection approach offers a > 51 dB harmonic-rejection ratio at the third- and fifth-order LO harmonics without calibration.

To improve tolerance for close-by blockers, we further present an SC RF receiver achieving high-order, tunable, highly linear RF filtering. We implement RF input impedance matching, N-path filtering, high-order discrete-time infinite-impulse response (IIR) filtering and down-conversion using only switches and capacitors in a 0.1–0.7 GHz prototype with tunable center frequency, programmable filter order, and very high tolerance for OB blockers. The 40 nm CMOS receiver consumes 38.5–76.5 mA, achieves 40 dB gain, 24 dBm OB IIP3, 14.7 dBm B1dB for a 30 MHz blocker offset, 6.8–9.7 dB noise figure, and > 66 dB calibrated harmonic rejection ratio.

The key drawback of our earlier SC receiver is the relatively high theoretical lower limit of the noise figure. To improve the noise performance, we developed a 0.1–0.6 GHz chopping SC RF receiver with an integrated blocker detector. We achieve RF impedance matching, high-order OB interferer filtering, and flicker-noise chopping with passive SC circuits only. The 34–80 mW 65 nm receiver achieves 35 dB gain, 4.6–9 dB NF, 31 dBm OB-IIP3, and 15 dBm B1dB. The 0.2 mW

integrated blocker detector detects large OB blockers with only a $1\text{ }\mu\text{s}$ response time. The filter order can be adapted to blocker power with the blocker detector.

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Chapter 1

Introduction

1.1 Evolution of Wireless Communications

The demand for wireless communications has grown very quickly [1], and this high-speed communication has significantly changed people's lifestyle. Fig. 1.1 shows the data rates of different cellular standards. In 1991, when the Global Systems for Mobile (GSM) communications was released, the data rate was 9.6 kbps and only supported voice and short-message services. Twenty-six years later, the data rate of Long-Term Evolution-Advanced (LTE-A) is 1 Gbps, which is more than 100,000 times faster than GSM. Today, people can use a smartphone to watch online videos using LTE. Apart from cellular communication, other wireless connectivity systems (such as WLAN/WiFi, Bluetooth, RFID, NFC, and ZigBee) and the Global Navigation Satellite System (GNSS; as well as GPS, GLONASS, and BeiDou) also play a significant role in our daily lives.

One of the bottlenecks to achieving a high data rate in wireless communication is inefficient

frequency allocation. In the United States, the radio spectrum is regulated by the Federal Communications Commission (FCC) and the National Telecommunications and Information Administration (NTIA). Fig. 1.2 [2] shows the frequency allocation from 30 MHz to 3 GHz. Different standards are allocated in different frequency bands. However, if we measure the radio spectrum during a day [3] (Fig. 1.3), we can find some bands are very busy (e.g., GSM) while some bands are almost unused. The radio spectrum is a costly and limited natural resource. However, the current static frequency allocation leads to low spectrum-use efficiency. Going forward, dynamic frequency allocation can make the spectrum use more efficient.

Cognitive radio (CR) technology [6] was proposed to achieve dynamic spectrum access. CR is a wireless architecture in which a communication system does not operate in a fixed assigned band. Rather, each device automatically finds an appropriate empty band for its communication. There are two main methods for the secondary, cognitive, user to avoid interfering with primary or licensed users. The first is to use spectrum sensing [7], which uses a spectrum detector to sense the primary user's frequency band. The second to use a geolocation database [8]. The database system protects the primary users, ensuring that any interference is below acceptable thresholds, and enables the secondary users to access unused frequency bands. CR must be reconfigurable to adapt its RF center frequency and bandwidth to the available spectrum. Therefore, tunable receiver hardware is a key CR component.

Recently, the unlicensed devices have been allowed to operate on TV white spaces (TVWS), frequencies in the TV bands in areas where they are not used by licensed services [9]. The migration from analog TV to digital TV has freed up several VHF and UHF bands (48 MHz–860 MHz)

due to the high spectral efficiency of digital TV. Many wireless standards based on the CR concept are emerging for TVWS communications, including IEEE 802.22 [10], 802.11af [11], and 802.15.4m [12]. IEEE 802.22 provides long-range (30 km) connectivity in rural areas to build wireless regional area networks (WRAN). IEEE 802.11af is a WiFi-like wireless local area network (WLAN). IEEE 802.15.4m is a low-data-rate wireless personal area network (WPAN) suitable for the Internet of Things (IoT) and machine-to-machine (M2M) communications.

1.2 Evolution of CMOS RF Receiver Front Ends

In the early 1990s, RF receiver front ends were mainly implemented in bipolar processes with standalone circuit building blocks. The development of the CMOS RF technique [13] in the mid-1990s dramatically improved the scale of integration and reduced the cost of RF receivers. Process scaling and circuit innovation were the two main engines driving the evolution of the CMOS RF receiver front end.

In first-phase integrated CMOS RF receivers [14–16] (Fig. 1.4(a)), inductor-degenerated LNA and CMOS Gilbert-cell-based mixers were the most popular circuit typologies in micron-scale process. Inductor-degenerated LNAs achieved a good noise figure and provided RF gain. However, it required bulky on-chip or off-chip inductors and had a narrow bandwidth. The CMOS Gilbert cell also had limited linearity.

With better CMOS process, the parasitic capacitance of the MOS transistors was reduced, so that the transistors could operate at higher frequencies. In the 2000s, inductorless LNAs with smaller area and wide RF bandwidth became more popular. These were implemented with resis-

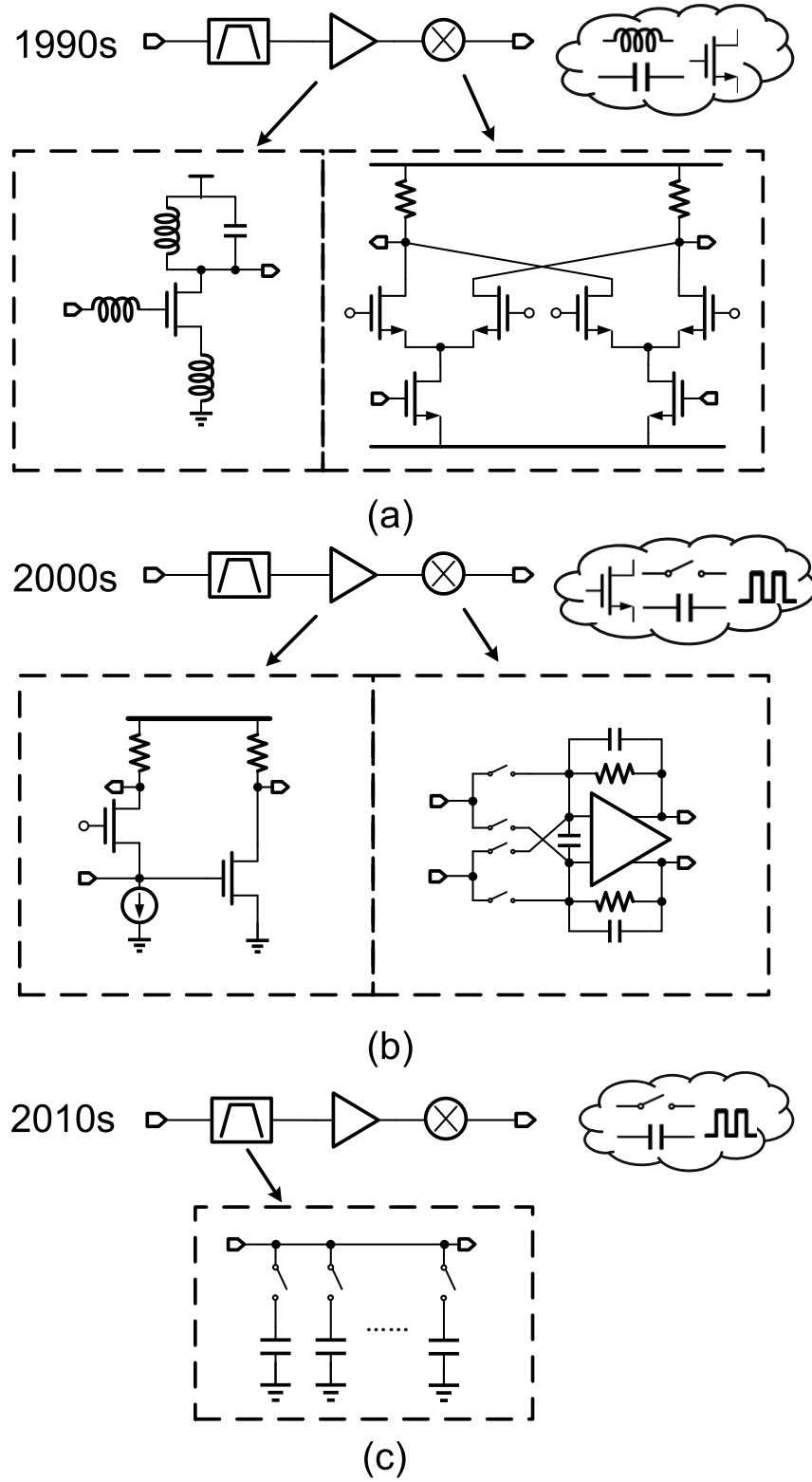


Figure 1.4: (a) In the 1990s, inductor-degenerated LNAs and active mixers were the popular RF front-end circuit. (b) In the 2000s, wideband LNAs (e.g., noise-canceling LNAs) and passive mixers became popular, thanks to faster transistors. (c) In the 2010s, switch-based RF circuits (e.g., the N-path filter) further improved receiver performance with advanced CMOS process.

tive feedback [17, 18] and innovated noise-canceling techniques [19, 20]. With faster transistors, the switch-based passive mixer [21] offered better linearity (Fig. 1.4(b)). However, without the narrowband resonance tank, the wideband LNA had limited out-of-band (OB) linearity.

In recent years (Fig. 1.4(c)), more switch-based RF techniques have appeared due to the better switch performance with advanced process. N-path bandpass filters [22–26] and mixer-first receivers [27–31] use the switches to achieve better OB linearity with tunable center frequency. My research focuses on further investigating how to use advanced CMOS process to improve receiver performance.

1.3 Motivation

To receive a narrowband signal with wide tuning range, a wideband tunable receiver is the key block in CR to achieve dynamic spectrum access. The wideband receiver front end needs to achieve a tunable center frequency, low noise, and OB interference tolerance. High OB interference tolerance is the key challenge in receiver design.

In the commercial receiver, which also needs to support different RF bands, OB interference tolerance is achieved with multiple off-chip filters. Fig. 1.5 shows the block diagram of a multiband 2G/3G/4G LTE transceiver [4]. On the receiver side, different bands can share the synthesizer, down-convert, and baseband circuits. However, dedicated off-chip filters and LNAs are used for different bands. The high-Q off-chip filter for a certain center frequency can strongly attenuate the OB interfere to relax the RF front end’s linearity requirements.

In CR systems, the goal is to replace high-quality fixed off-chip RF filters with tunable RF

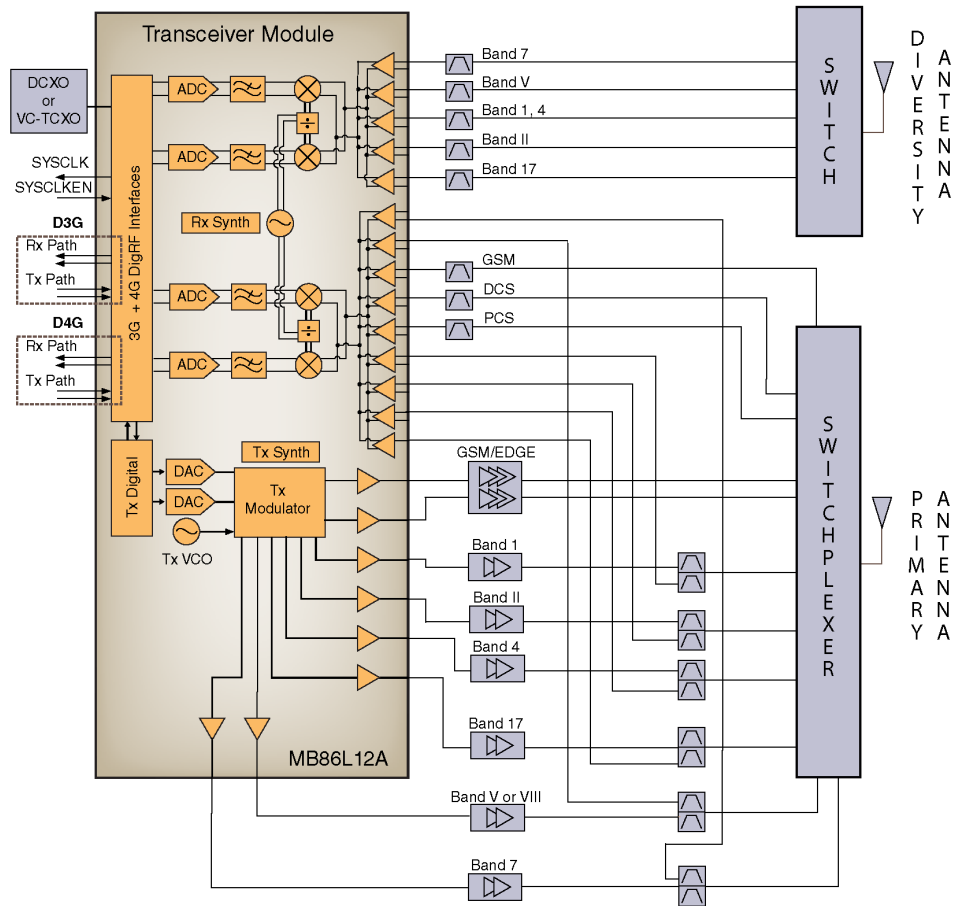


Figure 1.5: Block diagram of a multiband LTE transceiver [4].

filtering to realize an interference-tolerant tunable RF receiver front end. RF MEMS filters have been proposed to achieve the off-chip high-quality tunable filters, but they suffer from a limited tuning range, in-band loss and large size [32]. Conventional on-chip RF filters, such as LC [33] and G_m -C [34], suffer from either a low quality (Q) factor, small tuning range, or limited linearity [25]. Without wide-tuning, high-Q, linear filters, wideband receivers suffer from the impact of the large continuous-wave (CW) close-by blockers that saturate the RF front end and desensitize the receiver. Even if the interferer power is not large enough to block the desired signal, the intermodulation and cross-modulation caused by the OB interferer in FDD, along with coexistence scenarios, can degrade the signal-to-noise ratio.

Switched-capacitor (SC) RF filters, such as N-path filters implemented in CMOS, offer tunable high-quality filtering [22, 23, 26, 35–37] to improve OB linearity. Furthermore, the SC approach benefits from process scaling, which provides faster switches and a lower power clock generator [38]. In this thesis, we use the SC technique to overcome the drawbacks of conventional SC RF filters, such as harmonic response and limited filter order.

1.4 Organization of the Thesis

Chapter 2 summarize the SC techniques used in RF receivers. Chapter 3 proposes an RF front end with a harmonic-rejecting N-path filter. This front end mitigates the N-path filter's harmonic-response issue and features tunable narrowband filtering and high attenuation of the third- and fifth-order LO harmonics at the LNA output, improving the blocker tolerance at LO harmonics. Chapters 4, 5, and 6 introduce the SC RF front ends, achieving equivalent high-order, tunable,

highly linear RF filtering to improve the OB blocker tolerance. RF input impedance matching, N-path filtering, high-order discrete-time infinite-impulse response (IIR) filtering, and down conversion are implemented using only switches and capacitors. The basic SC RF front end is proposed in Chapter 4 achieving rail-to-rail blocker tolerance. Two different methods to improve the noise performance of the SCRX are proposed in Chapters 5 and 6 using chopping techniques and passive gain. Chapter 7 concludes.

Chapter 2

Review of Switched-Capacitor Techniques for RF Receiver Design

Thanks to the simple switches and high impedance nodes of the CMOS process, SC circuits can be easily implemented and play a key role in analog signal processing. Fig. 2.1 shows the trend of SC papers published in the *Journal of Solid-State Circuits* (JSSC) since the 1970s. It was a hot topic in 1980s. Most of the basic SC structures were developed (e.g., active SC filters [39–41], N-path filters [42–44]) at that time. In recent years, SC research is trending up because, with advanced CMOS process, SC applications have expanded to RF front ends such as RF N-path bandpass filter [23–26] and SC RF power amplifier–transmitters [45–48].

In RF receivers, SC techniques are used to implement filters eliminating large undesired signals and relaxing the dynamic-range requirements of subsequent circuits [49–53]. Compared with other analog filters such as active-RC and G_m -C filters, the corner frequencies of SC filters are well

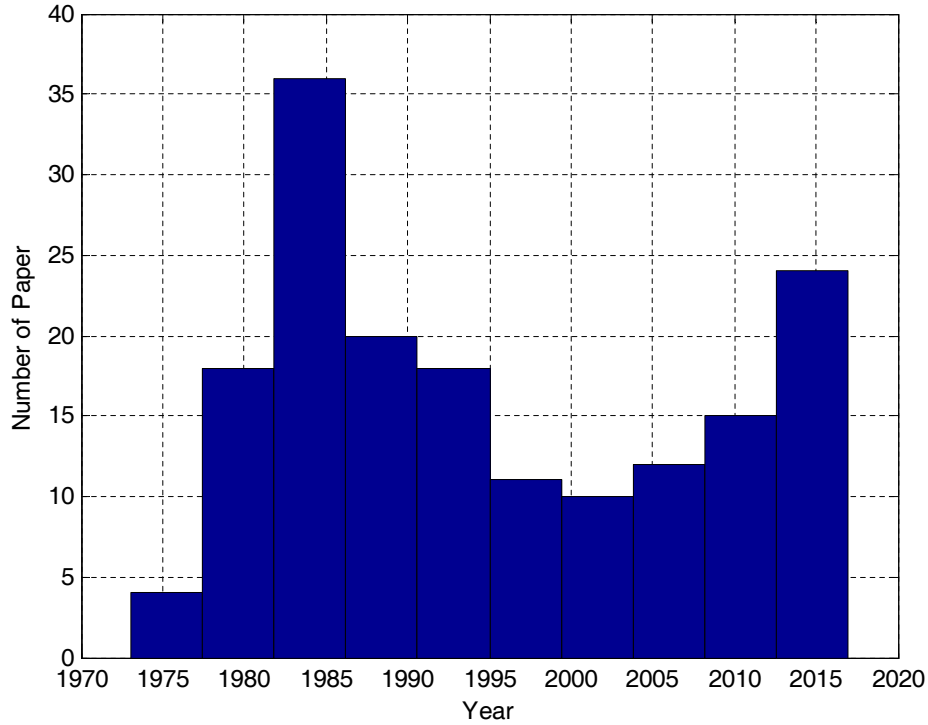


Figure 2.1: Trend of switched-capacitor publications in JSSC (1970s–Feb. 2017).

controlled and less sensitive to PVT variations since they are set by the capacitor ratio and can be programmed by the tunable capacitor banks. Active discrete-time (DT) filters, passive DT filters, and N-path filters are the three popular blocks used in RF receivers.

2.1 Active DT Filters

Active DT SC filters can be used as baseband filters in an RF receiver. Fig. 2.2 shows a simple active SC filter. The switches can be implemented by MOS transistors and driven by nonoverlapping clocks. The input voltage is sampled on C_1 in p_1 , and the charge on C_1 is transferred to C_2 in p_2 .

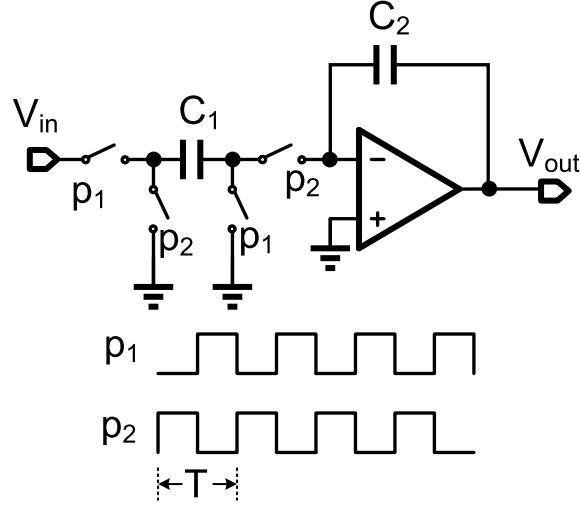


Figure 2.2: Active switched-capacitor filter.

Assuming the opamp has infinite gain, the filter's transfer function can be written as

$$H(z) = \frac{V_{\text{out}}(z)}{V_{\text{in}}(z)} = \frac{C_1}{C_2} \cdot \frac{z^{-1}}{1 - z^{-1}}. \quad (2.1)$$

With an active opamp, any type of filter can be synthesized [54]. The key drawback of the active DT SC filter is that the opamp mainly limits its performance. Considering the finite gain of the opamp, the filter's transfer function is

$$H(z) = \frac{V_{\text{out}}(z)}{V_{\text{in}}(z)} = \frac{C_1}{C_2} \cdot \frac{\frac{C_2 A}{C_2(1+A)+C_1} z^{-1}}{1 - \frac{C_2(1+A)}{C_2(1+A)+C_1} z^{-1}}, \quad (2.2)$$

where A is the opamp gain. Opamp gain drops at high frequencies due to finite bandwidth, which increases the filter's gain and phase errors. The opamp's unity-gain frequency sets the active DT SC circuit's upper-limit clock rate. The clock frequency must be less than 1/5 of the opamp unity-gain frequency to keep the effects of finite opamp bandwidth negligible [55]. The bandwidth of the

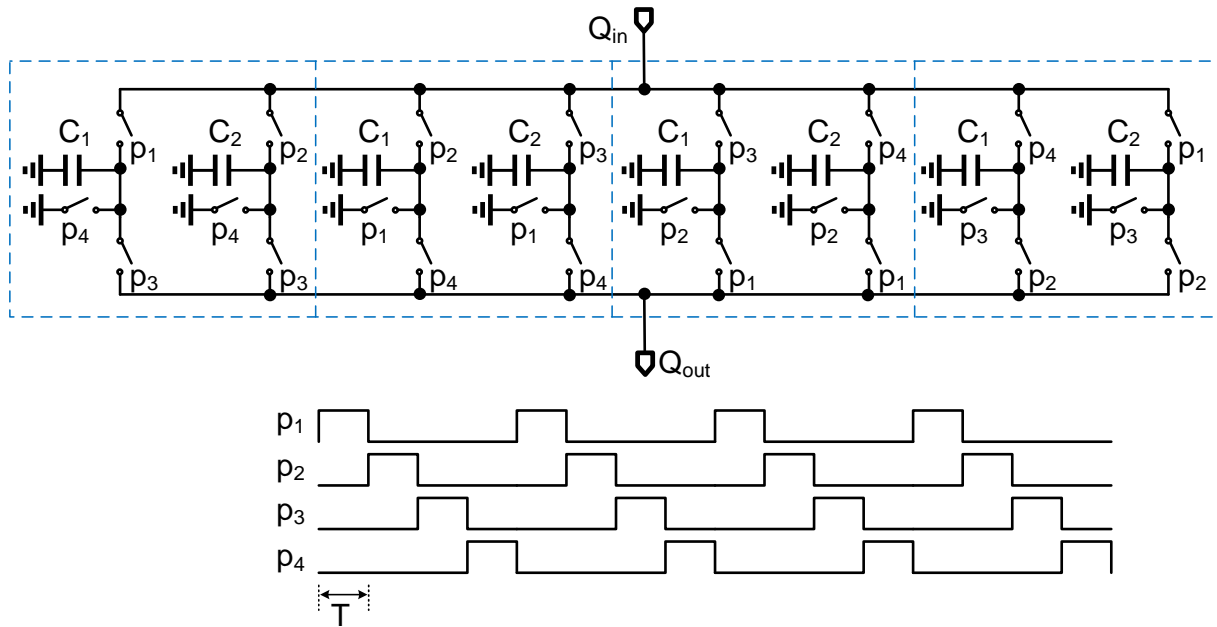


Figure 2.3: Passive switched-capacitor finite impulse response filter.

active DT SC filter is less than half the clock frequency and therefore limited to tens of megahertz.

Due to the limited clock frequency, active DT filters are always placed at the latter stages of the SC filter chain [56], and decimation is required to reduce the active filter's clock rate.

2.2 Passive DT Filters

Lacking the active opamp, passive DT SC filters simply rely on charge sharing to achieve the charge transfer. Passive SC filters' operation frequency is not limited by the opamp unity-gain bandwidth and can take full advantage of CMOS process scaling. There are two types of passive DT filters, finite impulse response (FIR) and infinite impulse response (IIR). More complex filters can be built from these basic structures.

An FIR filter is achieved by summing the delayed and weighted input signal. The capacitor can

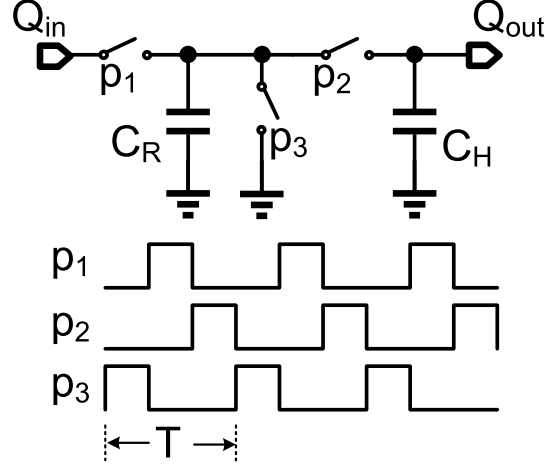


Figure 2.4: Passive switched-capacitor infinite impulse response filter.

be considered as a charge memory, and the SC circuit is a perfect delay cell with the weighting achieved by scaling the capacitors. Fig. 2.3 shows a time-interleaved, first-order FIR filter. The input charge is sampled on C_1 and C_2 in p_1 . Each capacitor stores a charge of $C_i Q_{in} / (C_1 + C_2)$. In p_3 , the capacitors sampling at p_1 and p_2 are connected to the output. Thus, the output signal is

$$Q_{out}(z) = \frac{C_2 + C_1 z^{-1}}{C_1 + C_2} z^{-1} Q_{in}(z). \quad (2.3)$$

The capacitors are reset to ground after the output is formed to prepare for the input sampling in next cycle. The input charge is consecutively sampled on the four SC banks. High-order FIR filter can be achieved by using more capacitor banks.

The IIR filter uses the input signal and past output signals to obtain the current output value, requiring less memory than the FIR filter to achieve the same filter selectivity. Fig. 2.4 shows a first-order IIR filter. In contrast to the FIR filter, C_H is not reset each cycle, so it can store the past

output charge. The output signal is

$$Q_{\text{out}}(z) = \frac{1 - \alpha}{1 - \alpha z^{-1}} z^{-1} Q_{\text{in}}(z), \quad (2.4)$$

where $\alpha = C_H / (C_R + C_H)$. High-order IIR filters can be achieved by rotating the charge among several history capacitors [57].

The passive SC filter also has some drawbacks. In contrast to active filters, it may not be able to synthesize every type of filter [57], and it is hard to achieve signal gain to suppress the noise of the next stage. Most passive SC filters are used as baseband filters and driven by transconductance (G_m) cells, which makes the filter linearity limited by G_m .

2.3 RF N-Path Filters

The N-path bandpass filter [22,58] has recently been popular in RF front-end design [23,26,35–37] because it provides narrowband filtering with a tunable center frequency. Fig. 2.5(a) shows a N-path filter with N SC banks. Each switch is driven by a nonoverlapping clock. The RF signal is first down-converted to baseband and filtered by C_{bb} . It is then up-converted back to its original frequency. N-path filters feature narrow bandwidth, tunable center frequency and good linearity. The bandwidth depends on the RC constant at the baseband frequency. Achieving narrowband low-pass filtering is much easier than narrowband bandpass filtering. The center frequency is set by the clock frequency, achieving a large tuning range. Since the N-path filter can be directly connected to the RF input, linearity is limited only by the switches, and high linearity can be achieved.

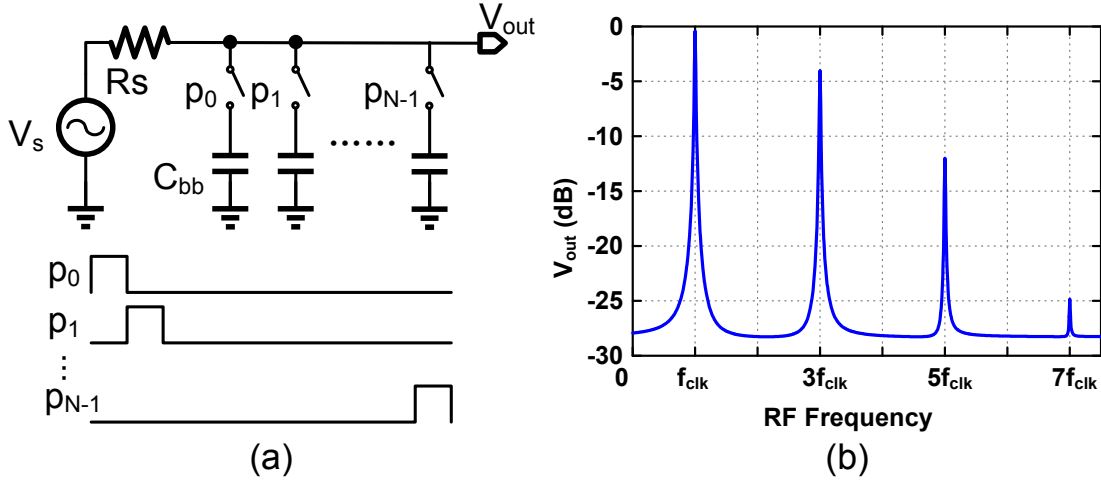


Figure 2.5: (a) Schematic and (b) frequency response of the N-path bandpass filter.

Although the N-path filter is a good candidate for high-selectivity tunable RF bandpass filtering, it has drawbacks: harmonic response, limited filter order, and poor OB attenuation. Fig. 2.5(b) shows a differential N-path filter's frequency response ($N = 8$). The desired center frequency is f_{clk} . The N-path filter has harmonic responses at $3f_{clk}$, $5f_{clk}$, and $7f_{clk}$ because the signals around those frequencies are down-converted by the clock harmonics and up-converted back to RF. The OB attenuation is limited to a certain number due to finite switch resistance. The first-order RC filter at baseband limits the N-path filter roll-off. A high-order active N-path filter [26] improves OB attenuation and filter order. However, the filter order before the active circuits is still low, making the linearity at close-by frequency is still limited by the active circuits.

2.4 Thesis Overview

We present several techniques to improve the performance of SC-based RF filtering. Chapter 3 focuses on eliminating the N-path filter harmonic responses for better band selection. Chapters

4–5 present passive DT SC filter to achieve linear, high-order RF filtering. These chapters address such key challenges as linearity limitations, RF impedance matching, and noise performance.

Chapter 3

Blocker-Tolerant Receiver with Harmonic-Rejecting N-Path Filtering

3.1 Introduction

The switched capacitor-based N-path filter (NPF) [22–26] offers a high Q factor, large tuning range, and good linearity, and is a good candidate for on-chip blocker filtering. When using N-path filtering at the RF input (Fig. 3.1(a)), the RF N-path bandpass filters [23, 25, 26] and the mixer-first receivers [27, 28] directly attenuate the OB blocker at the input resulting in an excellent blocker tolerance; however, for systems where there are strict emission limits, LO leakage can be a potential problem. Also, large capacitors are required to achieve narrow-band filtering due to the relatively small source impedance. Since the OB attenuation at the RF input node (V_{in} in Fig. 3.1(a)) is limited to the ratio of $R_{on}/(R_{on} + R_s)$, where R_{on} is the switch-on resistance, small R_{on} is also

required. These filters further exhibit spurious responses [23] at the harmonics of the LO signal which result in poor OB linearity. Preceding the NPF with an active LNA (Fig. 3.1(b)) [35, 36] offers reverse isolation and reduces the LO leakage. Also, the LNA output impedance is larger than the $50\ \Omega$ source resistance, which reduces the capacitor sizes and relaxes the switch R_{on} requirement. However, those receivers still have harmonic responses at the LNA output which reduce the blocker tolerance for blocking signals close to the LO harmonic frequencies. Various harmonic-rejection mixing techniques [36, 59–62] have been proposed. Using harmonic recombination in baseband [36] achieves a good harmonic rejection ratio (HRR), but the harmonic attenuation at the LNA output is not improved. The current-driven passive mixer and two-stage harmonic rejection approach in [59] shows high HRR and good OB linearity. However, it offers only a moderate blocker 1 dB compression point (B1dB) at low blocker offset frequencies. The harmonic-rejection TIAs proposed in [62] reduce the harmonic down-conversion after the baseband TIA for mixer-first receivers and current-driven mixers, though the harmonic down-conversion before the TIA cannot be eliminated using this technique. In [63] a bandpass filter without 3rd harmonic response was proposed and its operation and performance was evaluated in simulation. However, that approach cannot suppress the harmonic response before the recombination.

We propose a harmonic-rejecting N-path filter (HR-NPF) which reduces the harmonic responses at the 3rd and 5th LO harmonics (Fig. 3.1(c)) [64]. The active LNA provides a lower than -90 dBm LO leakage and high source impedance for the NPF. The harmonic responses are strongly attenuated by the HR-NPF, which improves the LNA blocker tolerance at LO harmonic frequencies. A receiver front-end prototype using the HR-NPF achieves a -2.4 dBm B1dB at only a

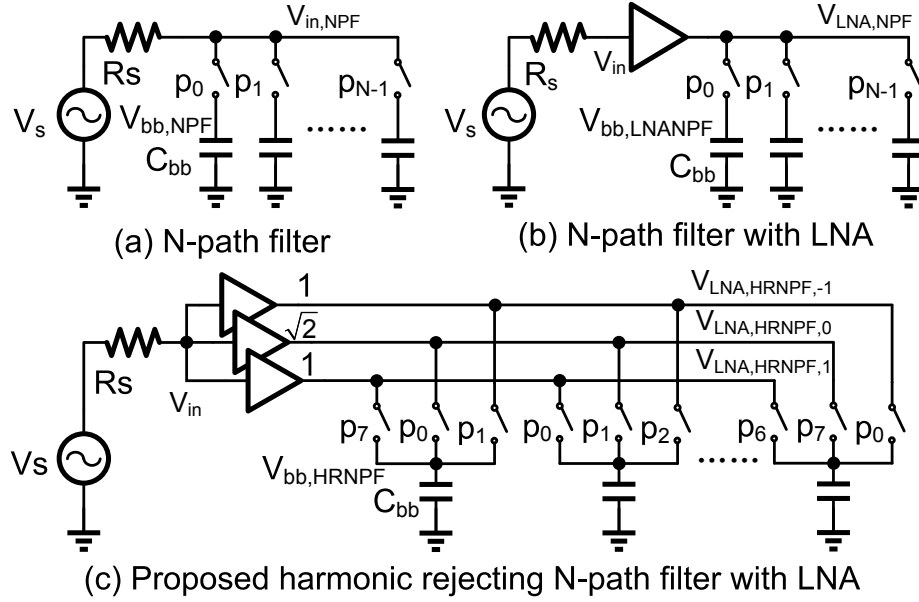


Figure 3.1: (a) Conventional N-path filter. (b) Conventional N-path filter with LNA. (c) Proposed harmonic rejecting N-path filter with LNA

20 MHz blocker frequency offset, and the B1dB remains high at LO harmonics. The HR-NPF also offers additional harmonic rejection for the down-conversion to achieve the two-stage harmonic rejection with >51 dB HRR at the 3rd and 5th LO harmonics without calibration.

The concept and analysis of the HR-NPF are developed in Section 3.2. The RF receiver with an HR-NPF and the circuit implementation are described in Section 3.3. Section 3.4 provides the measurement results, and conclusions are presented in Section 3.5.

3.2 Harmonic-rejecting N-path filter

An NPF is a continuous-time switched-capacitor bandpass filter driven by N-phase $1/N$ -duty-cycle nonoverlapping clocks, which is well analyzed in [23–25]. Due to the time-varying nature of the

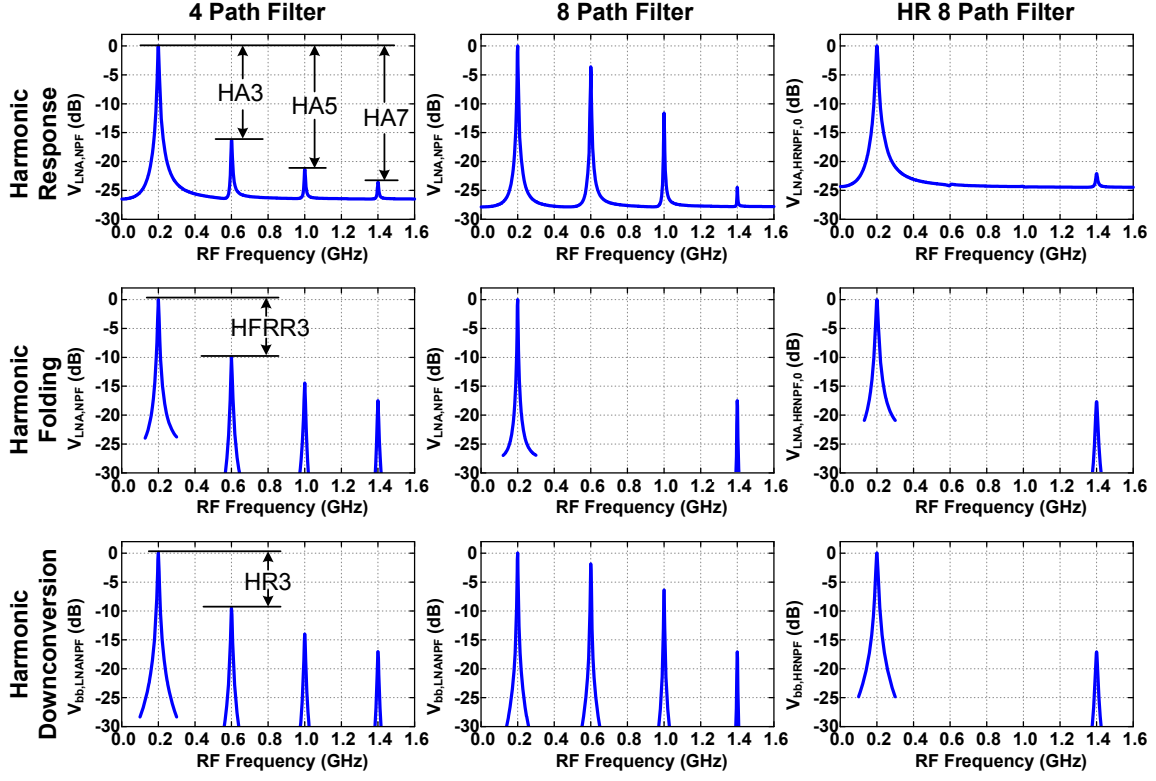


Figure 3.2: Simulated harmonic response (top row), harmonic folding (middle row), and harmonic down-conversion (bottom row) in 4-path filter (left column), 8-path filter (middle column) and proposed harmonic-rejecting 8-path filter (right column) for a 0.2 GHz clock frequency.

NPF, there are several frequency translation issues in the NPF compared to the linear-time-invariant (LTI) filter. Using a differential architecture helps to mitigate the issues due to even order harmonic.

In this section, we first discuss the harmonic folding, harmonic response, and harmonic down-conversion in a differential NPF, then show the analysis of the HR-NPF.

3.2.1 Harmonic response, harmonic folding, and harmonic down-conversion in a differential N-path filter

Fig. 3.2 shows the simulated harmonic response, harmonic folding and harmonic down-conversion of differential NPF with LNA (Fig. 3.1(b)) and proposed HR-NPF with LNA (Fig. 3.1(c)) for a $250\ \Omega$ LNA output resistor, a $10\ \Omega$ switch on-resistor, an $80\ \text{pF}$ baseband capacitor, and a $0.2\ \text{GHz}$ clock frequency. These effects in an NPF are well analyzed in [24]. Considering the signal at LNA output, the harmonic response is the bandpass filtering function around the clock harmonics (top row in Fig. 3.2). The harmonic attenuation (HA) is the ratio of the gain at desired signal frequency to the gain at clock harmonics. The HA of an NPF is

$$HA_i = \frac{\text{sinc}^2\left(\frac{\pi}{N}\right)}{\text{sinc}^2\left(\frac{i\pi}{N}\right)}, \quad (i = \text{odd}), \quad (3.1)$$

where i is the order of clock harmonic, N is the number of paths in the NPF, and $\text{sinc}(x) = \sin(x)/x$.

Low HA degrades the blocker tolerance at the clock harmonics.

The folding of unwanted signals from clock harmonics to the desired signal band at the LNA output is called harmonic folding (middle row in Fig. 3.2). The harmonic folding rejection ratio (HFRR) is the gain ratio of desired RF signal to the signal folded from clock harmonics, which is

$$HFRR_i = \frac{\text{sinc}\left(\frac{\pi}{N}\right)}{\text{sinc}\left(\frac{i\pi}{N}\right)}, \quad (i = kN - 1, k \in \mathbf{Z}). \quad (3.2)$$

Since the RF signal is down-converted to the baseband capacitor, the NPF can also be used

as a down-converter. The down-converting of unwanted RF signals at clock harmonics is called harmonic down-conversion, which reduces the SNR for the desired signal. Also, the blockers at clock harmonics can be amplified, and saturate the baseband circuits. The harmonic-rejection ratio (HRR) is the ratio of the conversion gain for the desired signal to that for the signals at clock harmonics, which is

$$HRR_i = \frac{\text{sinc}\left(\frac{\pi}{N}\right)}{\text{sinc}\left(\frac{i\pi}{N}\right)}, \quad (i = \text{odd}). \quad (3.3)$$

In the NPF, harmonic folding can be reduced by using more paths. Compared to a 4-path filter, in an 8-path, the harmonic folding from the 3rd and 5th clock harmonics filter is reduced (Fig. 3.2); however, the harmonic response is worse than that of a 4-path filter. The HA3 of an 8-path filter is only around 4 dB which is much higher than the 19 dB HA3 in a 4-path filter, and can reduce the blocker tolerance at that clock harmonic. Moreover, the HR3 of an 8-path filter is only 2 dB which is worse than the 10 dB HR3 in a 4-path filter .

In our proposed harmonic-rejecting 8-path filter (right column in Fig. 3.1), the harmonic folding is improved by employing more paths, and the harmonic response and the harmonic down-conversion are also improved. For a wideband receiver with a frequency range of 0.2-1 GHz, the HR-8PF improves the blocker tolerance at clock harmonics across the whole frequency range, since the 7th order harmonic for the lowest clock frequency 0.2 GHz is 1.4 GHz which is out of the desired input frequency range.

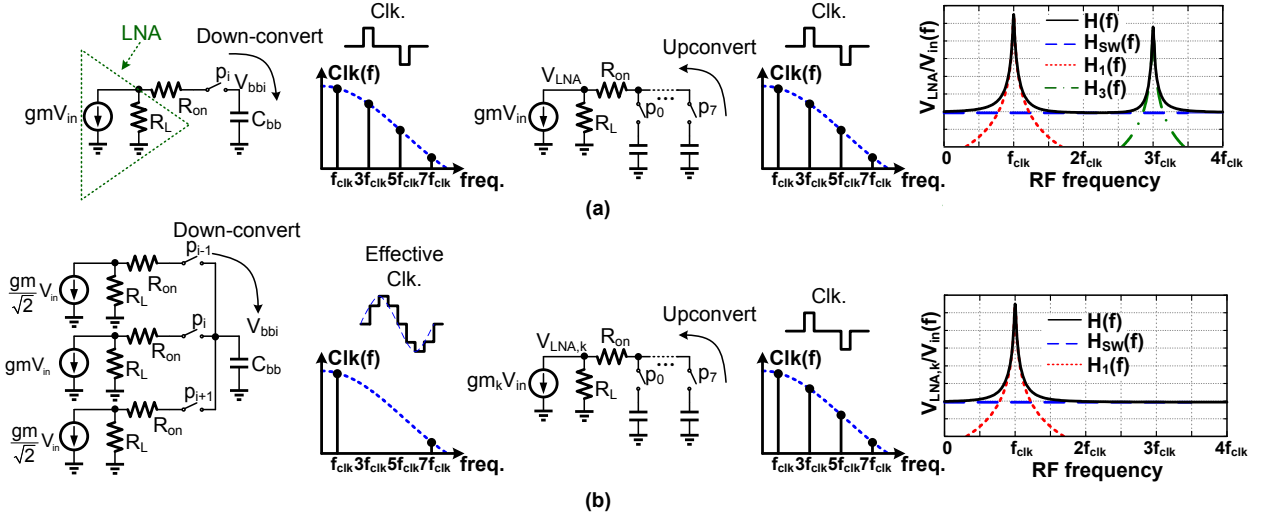


Figure 3.3: A simplified model for the harmonic response analysis for a differential NPF at the output of the LNA; the LNA is modeled with a Norton equivalent (a) For a conventional 8-path filter, the signals at f_{clk} and $3f_{\text{clk}}$ are down-converted then up-converted to RF input resulting in harmonic responses. (b) In the proposed harmonic-rejecting 8-path filter, the harmonic down-conversion from $3f_{\text{clk}}$ is rejected by the effective LO, and the harmonic responses are improved. (Note that the gain and bandwidth of the HR-8PF is different from conventional 8PF)

3.2.2 Analysis of the harmonic-rejecting N-path filter

Fig. 3.3 shows the simplified operation of the NPF and the proposed HR-NPF. In a conventional 8-path filter with an LNA, the RF signal is first down-converted to the baseband capacitors, then up-converted back to the LNA output as shown in Fig. 3.3(a). The total frequency response consists of transfer functions due to the fundamental of the clock $H_1(f)$, 3rd order harmonic of the clock $H_3(f)$, and finite on-resistance $H_{\text{SW}}(f)$. In the proposed HR-8-path filter, the 3rd order clock harmonic is rejected during down-conversion by combining the outputs of 3 LNAs with scaled transconductance (Fig. 3.3(b)). Thus the filter transfer function due to the 3rd order clock harmonic ($H_3(f)$) is removed, and the harmonic attenuation is limited only by switch R_{on} .

To calculate the transfer function of the HR-NPF, we use the similar approach in [26]. Fig. 3.4(a)

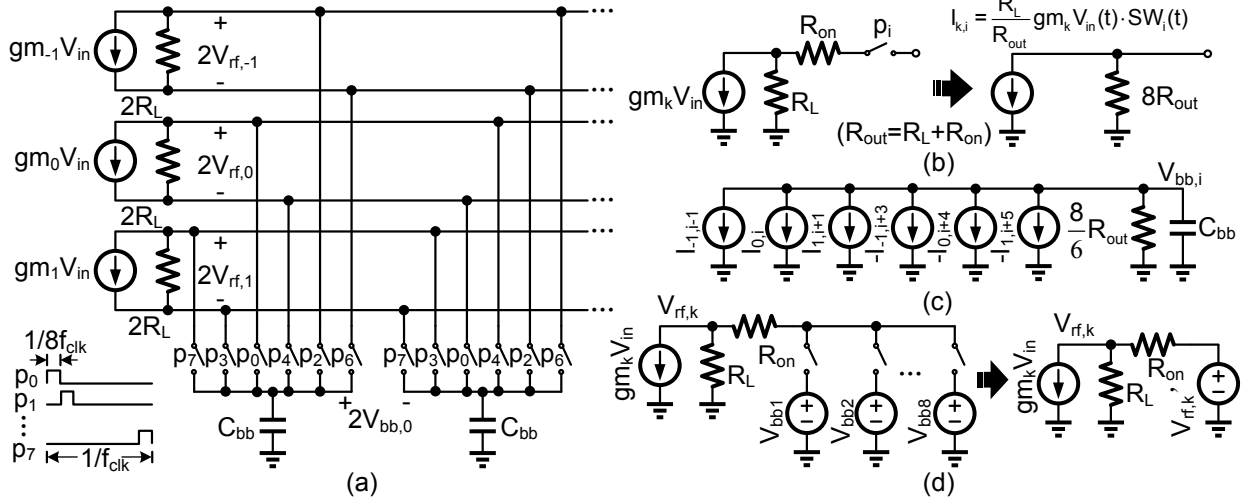


Figure 3.4: (a) A differential harmonic rejecting N-path filter with non-overlapping clocks. (b) An equivalent circuit of the LNA with a switch. (c) For one baseband capacitor, the currents from all the LNAs generate the baseband voltage $V_{bb,i}$. (d) All the baseband voltages are up-converted to the LNA output.

shows a differential harmonic-rejecting 8-path filter (HR-8PF). The switches driven by p_i and p_{i+4} share the same baseband capacitor to eliminate the even-order harmonic responses [24]. To analyze the transfer function $V_{rf,k}/V_{in}$, the LNAs are modeled as transconductors (Gms) with finite output impedance and $gm_k = gm \cdot \cos(k\pi/4)$ ($k = \{-1, 0, 1\}$), while the switches are modeled as ideal switches with finite on-resistance. We first find the baseband voltage on one capacitor C_{bb} , then calculate the LNA output voltage using the superposition of V_{in} and $V_{bb,k}$.

The Gm with one switch can be modeled as a time-varying Gm with finite output resistance as shown in Fig. 3.4(b) [26] since in each time slot only one switch is turned on for each Gm. Since the switching function SW_i is

$$SW_i(t) = \sum_{n=-\infty}^{+\infty} a_n e^{-j\frac{n\pi}{4}i} e^{jn\omega_{clk}t}, \quad (3.4)$$

where $a_n = \text{sinc}(n\pi/8)/8 \cdot \exp(-jn\pi/8)$, the equivalent Gm current with one switch (Fig.3.4(b)) in frequency domain can be written as

$$I_{k,i}(\omega) = \frac{R_L}{R_{out}} gm_k \sum_{n=-\infty}^{+\infty} a_n e^{-j\frac{n\pi}{4}i} V_{in}(\omega - n\omega_{clk}), \quad (3.5)$$

where $R_{out} = R_L + R_{on}$. The RF current is down-converted to the baseband by the n^{th} clock harmonic. The load resistor is $8 \cdot R_{out}$, since the duty cycle of the clock is $1/8$. For each C_{bb} , the current from 6 Gms are summed up and generate the baseband voltage $V_{bb,i}$ shown in Fig. 3.4(c). The load resistor is $8/6 \cdot R_{out}$. The baseband voltage is:

$$V_{bb,i}(\omega) = [I_{-1,i-1}(\omega) + I_{0,i}(\omega) + I_{1,i+1}(\omega) - I_{-1,i+3}(\omega) - I_{0,i+4}(\omega) - I_{1,i+5}(\omega)] \cdot Z_{bb}(\omega), \quad (3.6)$$

where Z_{bb} is the equivalent baseband impedance, which is $R_{bb}/(1 + j\omega R_{bb}C_{bb})$ ($R_{bb} = 4R_{out}/3$). The down-conversion from even order, 3rd, and 5th order clock harmonic frequencies are rejected since the Gms are scaled to the ratio of $0:1:\sqrt{2}:1:0:-1:-\sqrt{2}:-1$ in the different time intervals as in a harmonic rejection mixer. Since $gm_k = gm \cdot \cos(k\pi/4)$, the baseband voltage can be derived as:

$$V_{bb,i}(\omega) = \sum_{n=-\infty}^{+\infty} 4a_n e^{-j\frac{n\pi}{4}i} \frac{R_L}{R_{out}} gm V_{in}(\omega - n\omega_{clk}) Z_{bb}(\omega), \quad (n = 8l \pm 1, l \in \mathbf{Z}). \quad (3.7)$$

The output voltages of three LNAs can be considered as a superposition of the input Gm and the

up-converted $V_{bb,i}$ (Fig. 3.4(d)). The up-converted part $V'_{rf,k}$ is

$$V'_{rf,k}(\omega) = \sum_{m=-\infty}^{+\infty} \sum_{n=-\infty}^{+\infty} 32a_m a_n \frac{R_L}{R_{out}} gm V_{in}(\omega - (m+n)\omega_{clk}) Z_{bb}(\omega - m\omega_{clk}) e^{j\frac{n\pi}{4}k}, \quad (3.8)$$

$$(m+n = 8q, m = odd, n = 8l \pm 1, l, q \in \mathbf{Z}).$$

The desired signal frequency is $\omega_{clk} + \omega_{bb}$, so only the signals from $(1-8q)\omega_{clk} + \omega_{bb}$ will be folded into desired signal band. Since the 3rd and 5th clock harmonics are rejected during down-conversion, the HR-8PF doesn't have those harmonic responses. Ignoring the harmonic folding, the transfer functions for the k^{th} LNA can be written as:

$$\frac{V_{rf,k}(\omega)}{V_{in}(\omega)} = \cos\left(\frac{k\pi}{4}\right) gm R_{on} || R_L + \left(\frac{R_L}{R_{out}}\right)^2 \sum_{m=-\infty}^{+\infty} 32|a_m|^2 gm Z_{bb}(\omega - m\omega_{clk}) e^{-j\frac{m\pi}{4}k}, \quad (3.9)$$

$$(m = 8l \pm 1, l \in \mathbf{Z}).$$

The transfer function only has bandpass filtering around $(8l \pm 1)\omega_{clk}$; the 3rd and 5th clock harmonic responses are rejected. Assuming the LNA output resistance is much larger than the switch on-resistance ($R_L \gg R_{on}$), the bandwidth of the bandpass transfer function is $3/(2\pi R_L C_{bb})$, the in-band (IB) gain is $128/3 \cdot |a_1|^2 gm R_L$ and the OB gain is $\sin(k\pi/4) gm R_{on}$. Although the Gms in the three LNA branches are different, The IB gain of all the three branches are the same since the gain is determined by the up-converted voltage $V'_{rf,k}$ and for each branch the $V'_{rf,k}$ has the same amplitude but a different phase shift. Compared with an NPF directly connected to the RF input, to achieve the same baseband bandwidth with the LNA, a smaller capacitor can be used result-

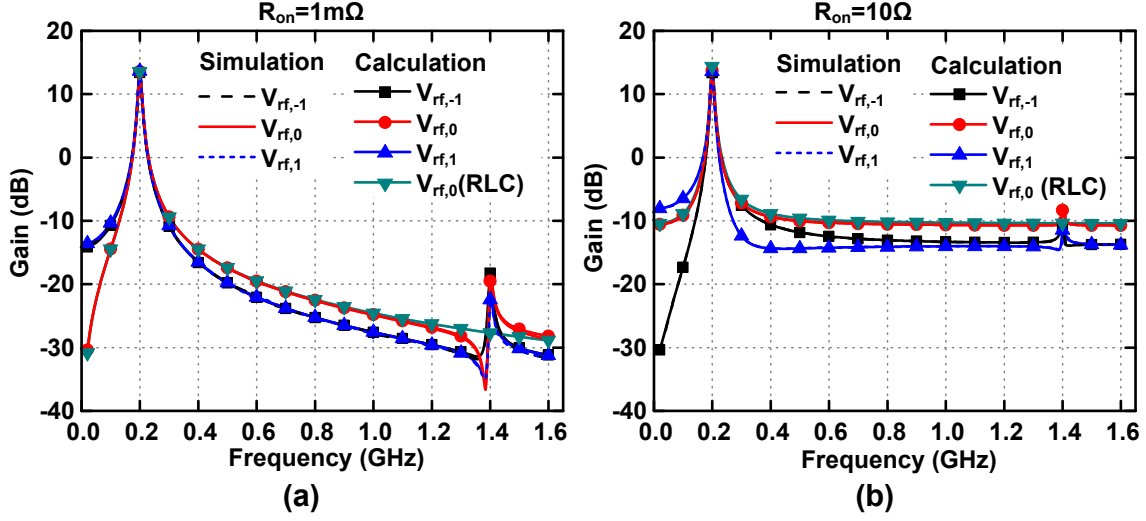


Figure 3.5: The calculated (using (3.9)) and simulated transfer function of the HR-8PF with an R_{on} of (a) $1 \text{ m}\Omega$ and (b) 10Ω .

ing in a smaller chip area, since the LNA R_L is much larger than the 50Ω RF source impedance. Additionally, larger OB attenuation can be achieved due to a larger R_L/R_{on} ratio.

The HR-NPF can be modeled as an RLC tank in series with R_{on} as conventional NPF [23]. The equivalent RLC values are: $R_m = 32|a_1|^2 R_{bb}$, $C_m = C_{bb}/64|a_1|^2$, $L_m = 1/(C_m \omega_{clk}^2)$. Fig. 3.5(a) shows the calculated and behavioral-level simulated transfer function of the three LNA outputs (Fig. 3.3(a)) as well as the RLC model for the middle LNA branch. The switches are driven by a 200MHz 8-phase non-overlapping clock, and $gm=30 \text{ mS}$, $R_L=250 \Omega$, $R_{on}=1 \text{ m}\Omega$, $C_{bb}=80 \text{ pF}$. The simulated transfer function matches the calculation using (3.9) very well. The frequency response of the HR-8PF is very close to an RLC filter and the center frequency is tunable. The difference of the different LNA outputs is caused by the phase shift in the up-converted voltage $V'_{rf,k}$.

To compare the HR-8PF (Fig. 3.1(c)) with a conventional 8PF (Fig. 3.1(b)), we assume that they have the same total LNA transconductance gm_{LNA} , that the LNA/sub-LNA load resistors of

8PF and HR-8PF are that $R_{L,LNA}$ and $3R_{L,LNA}$ respectively, that the baseband capacitors are C_{bb} , that the OB attenuation of the HR-8PF middle branch and 8PF are the same, and $R_{L,LNA} \gg R_{on}$. The sub-LNA in the middle branch of the HR-8PF has a gm of $gm_{LNA}/(1 + \sqrt{2})$, thus the gain and R_{on} of HR-8PF are $2/(1 + \sqrt{2})$ and $1/(1 + \sqrt{2})$ times that of the 8PF respectively. The bandwidth of the HR-8PF is the same as 8PF. The LNA power of the two filters are the same since they have the same gm. Assuming the clock generator power is proportional to the total switch capacitance and the capacitance of a switch is proportional to $1/R_{on}$, the clock generator power of the HR-NPF is $3/(1 + \sqrt{2})$ times that of the 8PF.

3.2.3 Second-order effects

Finite switch on-resistance

The finite switch on-resistance limits the OB attenuation of the HR-NPF. The HR-8PF OB attenuation can be derived as $20\log(128|a_1|^2 R_L / [3R_{on}\sin(k\pi/4)])$ for the k^{th} LNA branch from (3.9). Fig. 3.5(b) shows the calculated and simulated transfer function of the HR-8PF with $R_{on}=10\ \Omega$. The transfer curve of the LNA branch #-1 skews to the right while that of the LNA branch #1 skews to the left at low frequency offset due to the phase shift in the up-converted voltage V'_{rf} . At larger frequency offset, the OB attenuation of those two branches is limited by the switch R_{on} as expected.

Parasitic capacitors

In a real circuit, the LNA and switches have parasitic capacitors. The switch capacitor at the baseband side can be considered a part of C_{bb} . The parasitic capacitor at the output of the LNA will shift the filter center frequency and increase the in-band loss as discussed in [26].

Mismatch between the branches

In an ideal HR-8PF, no RF currents around the 3rd and 5th clock harmonics are down-converted to the baseband capacitors, and the harmonic responses are fully eliminated. However, in a real circuit, the cancellation of the harmonic components of the effective clock is limited by the gain and phase errors between the three branches. The finite R_{on} also limits the harmonic attenuation. Defining HA'_{HR} as the harmonic attenuation (1σ) of the HR-8PF due to harmonic mixing and using the derivation in [59], $HA3'_{HR}$ and $HA5'_{HR}$ of a HR-8PF can be written as:

$$\begin{aligned} HA3'_{HR} &= 3 \frac{\sin^2\left(\frac{\pi}{8}\right)}{\sin^2\left(\frac{3\pi}{8}\right)} \left[\left(\frac{\sigma_A}{12}\right)^2 + \left(\frac{\sigma_\phi}{4}\right)^2 \right]^{-1/2} \\ HA5'_{HR} &= 5 \frac{\sin^2\left(\frac{\pi}{8}\right)}{\sin^2\left(\frac{5\pi}{8}\right)} \left[\left(\frac{\sigma_A}{20}\right)^2 + \left(\frac{\sigma_\phi}{4}\right)^2 \right]^{-1/2} \end{aligned} \quad (3.10)$$

where σ_A and σ_ϕ are the standard deviations of gain and phase errors. The $HA3'_{HR}$ is 30 dB for a $\sigma_A = 10\%$ and $\sigma_\phi = 3^\circ$, which is better than the $HA3$ caused by a $10\ \Omega$ R_{on} and a $250\ \Omega$ R_L (around 25 dB). Thus, the OB attenuation at 3rd and 5th order clock harmonics is mainly limited by the finite switch R_{on} and can be as good as for other OB frequencies.

Clock leakage

Generally, for an RF receiver, the asymmetric baseband circuit DC offset and charge coupling mainly generate the clock leakage [65]. Considering the circuit in Fig. 3.1(b) as a differential RF receiver with an 8-phase mixer, for the receivers using baseband trans-impedance amplifier (TIA), the TIA input DC offset can be up-converted to $8f_{\text{clk}}$ and its harmonics by the switches. However, if the DC offsets of each V_{bb} are not symmetric or the clock signal has mismatch, the clock leakage will appear at f_{clk} . The clock charge injection is caused by the parasitic capacitor between the clock trace and the RF trace. It generates clock coupling due to the asymmetric parasitic capacitor or the clock signal mismatch.

In this work, the baseband capacitors are connected to the gate of Gm cells, and the Gm is biased by the LNA outputs. Thus, the DC offset of the Gm cell input is much smaller than TIA. To reduce the clock charge injection, the clock traces should not overlap with the RF traces in the layout, thereby reducing the parasitic capacitance.

The reverse isolation of the LNA also helps to reduce the clock leakage. For the receivers using feedback LNA, the clock leakage is limited to around -80 dBm [66], since the feedback path limits the LNA reverse isolation. In this work, noise canceling LNA is used, and a cascode device helps to improve the reverse isolation.

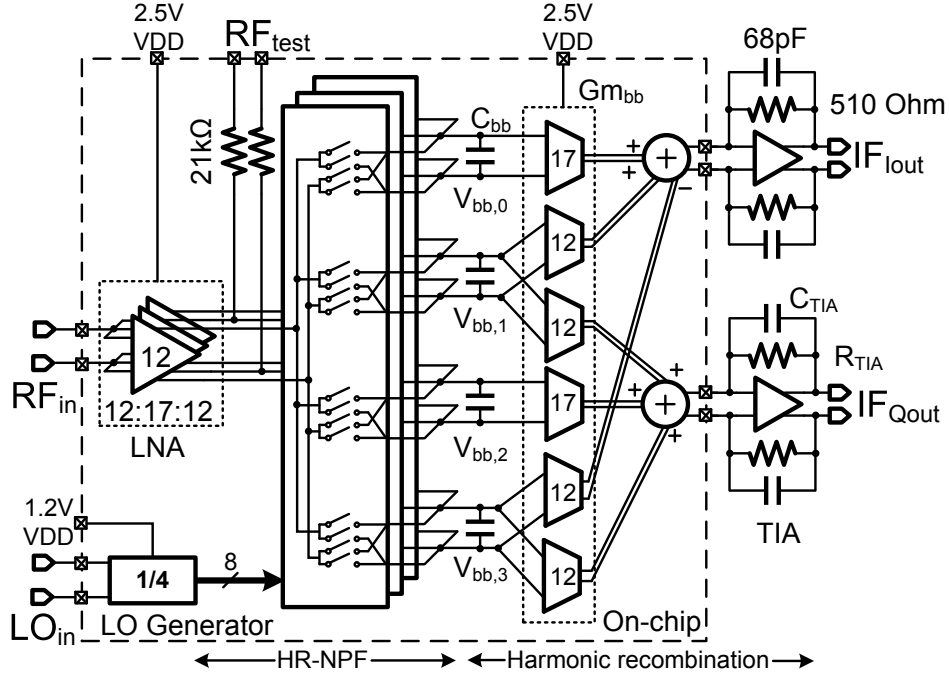


Figure 3.6: Architecture of the blocker tolerant RF receiver

3.3 RF receiver with harmonic rejecting N-path filter

3.3.1 RF front-end architecture

The architecture of the RF front-end prototype IC (Fig. 3.6) consists of a broadband LNA with HR-NPF, baseband Gms, and an LO generator. All the switches in the HR-NPF are driven by 8-phase nonoverlapping LO signals as the clock. The HR-NPF provides bandpass filtering with reduced harmonic responses at LNA outputs. Also, the RF signal is down-converted to the baseband capacitors in the HR-NPF with harmonic rejection. Since the down-converted voltage $V_{bb,i}$ has a phase shift $\exp(-jn\pi/4)$ for the n^{th} order LO down-conversion, the baseband Gms combine the baseband voltages with the gm factor of $\sin(i\pi/4)$ to realize a two-stage harmonic rejection architecture [59] and form in-phase and quadrature currents that drive off-chip TIAs. The conversion

gain of the receiver is

$$\begin{aligned}
 CG &= \frac{V_{IF}}{V_{in}} = \frac{\left(V_{bb,i-1}/\sqrt{2} + V_{bb,i} + V_{bb,i+1}/\sqrt{2} \right) gm_{bb} R_{TIA}}{V_{in}} \\
 &= \frac{4}{3} \text{sinc}\left(\frac{\pi}{8}\right) gm R_L gm_{bb} R_{TIA},
 \end{aligned} \tag{3.11}$$

where gm is the transconductance of the LNA and gm_{bb} is the transconductance of baseband Gm both with a gm factor of 1, R_L is the LNA load resistance, and R_{TIA} is the feedback resistance in the TIA. The ideal $1 : \sin(\pi/4)$ gm ratio is approximated as 17:12 in the LNA and baseband Gms. Generally the HRR of a receiver is limited by the gain error of the Gm and the LO phase error. In the two-stage harmonic rejection approach the overall relative gain error is the product of the relative errors for the LNA and baseband Gms [59]. The gain error is negligible and the HRR is limited by the LO phase error, so that a high HRR can be achieved. Compared with HRR calibration techniques [36], two-stage harmonic rejection can achieve high HR3 and HR5 simultaneously. The HRR further helps to reduce the mixer noise figure thanks to the reduction of noise folding.

3.3.2 Circuit implementation

Fig. 3.7(a) shows the schematic of the fully differential LNA which is split into 3 sections with relative sizes of 12:17:12. All sections are joined together at the inputs. $M_1 - M_4$ is a current-reuse common-gate (CG) stage and $M_5 - M_8$ is a current-reuse common-source (CS) stage. The total gm of the CG stage is 20 mS to achieve the 50Ω impedance matching at each input. Current re-use improves the current efficiency and the gm ratio of the CS and CG branches is 4:1 to achieve a low noise figure. The CG stages are biased with off-chip inductors to avoid the noise contribution

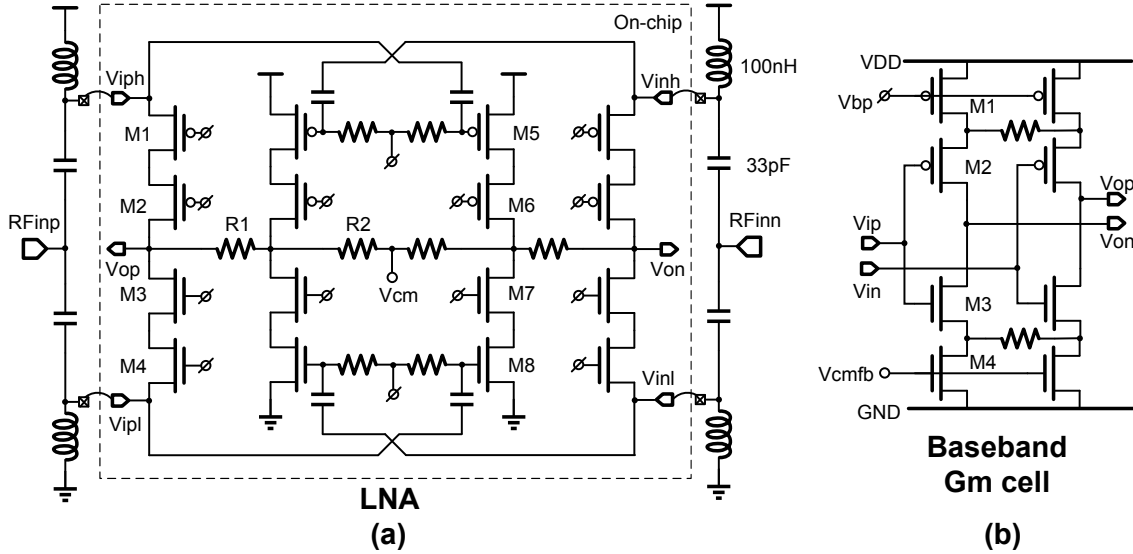


Figure 3.7: Schematic of (a) LNA and (b) baseband Gm cell

of an active current-source bias. The load resistor ratio is $R_1 : R_2 = 3 : 1$ and $R_1 + R_2$ is around 472Ω . The output common mode is maintained at $V_{DD}/2$ with an external regulator. The supply can vary from 1.8 V to 2.5 V and the cascode transistors guarantee a voltage drop smaller than 1V across each device at 2.5 V so that thin-oxide transistors can be used. The baseband capacitors C_{bb} (Fig. 3.6) have an effective 60 pF singled-ended capacitance and are realized with differential MIM capacitors and single-ended MOS capacitors.

The differential baseband Gm (Fig. 3.7(b)) also uses current-reuse and can operate from 1.8 V to 2.5 V. M_2 and M_3 are the input transistors with resistive source degeneration to improve linearity. M_1 is a PMOS current source, while a common-mode feedback (CMFB) circuit drives the NMOS current source transistor M_4 to maintain the output common mode voltage at $V_{DD}/2$. To ensure the common mode voltage tracks $V_{DD}/2$ during power up, a soft-start LDO is used, and the LDO output ramp speed is lower than the speed of the CMFB circuit.

The LNA, switches, and Gm cells are DC coupled ¹ (Fig. 3.6) to achieve higher OB linearity at low RF frequencies as in [36]. The DC coupling sets the source/drain voltage of the switch transistors to the LNA and Gm common mode, i.e. $V_{DD}/2$, which can be as high as 1.25 V. The NMOS switch transistors are placed in a deep N-well and their body and source are connected together to keep source, drain, and body at the same DC voltage. The 1.2 V_{pp} LO signal is AC coupled to the gates of the switches, and the gate bias voltage is $V_{DD}/2$. The voltage drop across all transistor terminal pairs is then not larger than the supply voltage (1.2 V) of the LO signal, and thin-oxide switch transistors can be used. The on-resistance of each switch is around 14 Ω .

3.3.3 Improvement of out-of-band linearity

The HR-NPF improves the OB linearity of the receiver since it has low OB gain before the baseband circuit and it reduces the voltage swing at the LNA output to improve the LNA linearity. The cascade IIP3 for a receiver is $1/A_{IIP3,tot}^2 = 1/A_{IIP3,LNA}^2 + G_{LNA}^2/A_{IIP3,BB}^2$ [67]. For the IB linearity, the baseband circuit is the bottleneck due to the large LNA gain. With the HR-NPF, the OB gain at the baseband capacitor is already reduced (Fig. 3.6), and the harmonic down-conversion from 3rd and 5th order LO harmonics is also rejected, thus the baseband circuit will not limit the OB linearity, so that the LNA linearity becomes the bottleneck. The low OB impedance of the HR-NPF also helps to improve the LNA output linearity. Fig. 3.8 shows the transistor-level simulated IIP3 and P1dB versus load impedance for the LNA in Fig. 3.7(a). The LNA is driven by a port with a $1 : \sqrt{2}$ balun, and the linearity is measured at the differential outputs of the LNA branch with a gm factor

¹However when using DC coupling, the LNA IM2 products and flicker noise may leak to into baseband circuits.

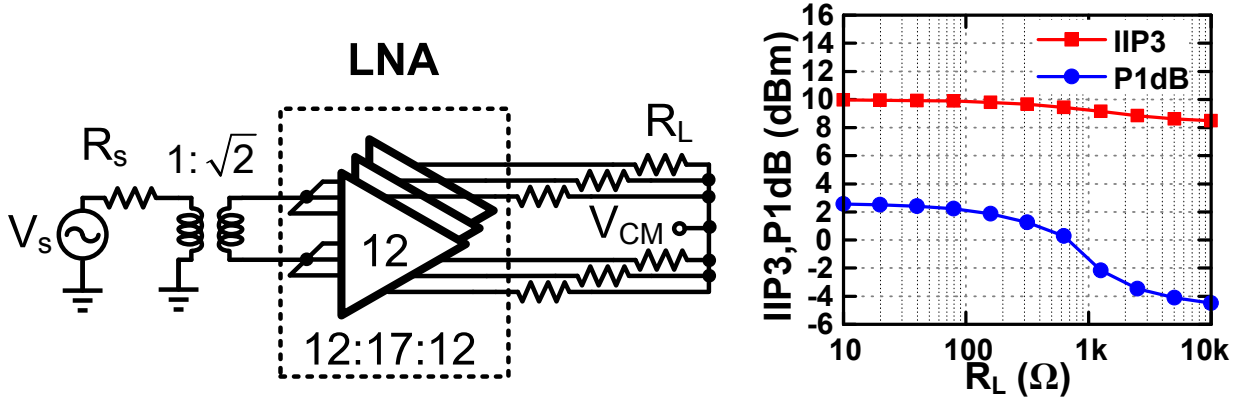


Figure 3.8: Transistor simulated IIP3 and B1dB versus LNA load impedance for the LNA with a gm factor of 17.

of 17. The small signal linearity (IIP3) and the large signal linearity (P1dB) are both improved with lower LNA load impedance as shown in Fig. 3.8(b). The P1dB improves more than the IIP3 with lower impedance since the LNA output will be clipped with a large input signal and high voltage.

3.3.4 Noise analysis

Noise-cancelling LNAs (NC-LNA) [19, 20] are widely used to achieve a low noise by cancelling the noise from their common-gate (CG) transistor. However, if we split the NC-LNA into several branches to achieve the harmonic rejection, the CG noise cannot be fully canceled. In this section we analyze the NC-LNA (Fig. 3.7(a)) in the harmonic rejection receiver (Fig. 3.6). The simplified circuit of the k^{th} branch of the LNA is shown as Fig. 3.9(a). $gm_{CG,k}$ and $gm_{CS,k}$ are the transconductances of the CG and common-source (CS) branches, and

$$gm_{CG,k} = \frac{gm_{CG} \cdot \cos(k\pi/4)}{\sum_{i=-1}^1 \cos(i\pi/4)}, gm_{CS,k} = \beta gm_{CG,k}. \quad (3.12)$$

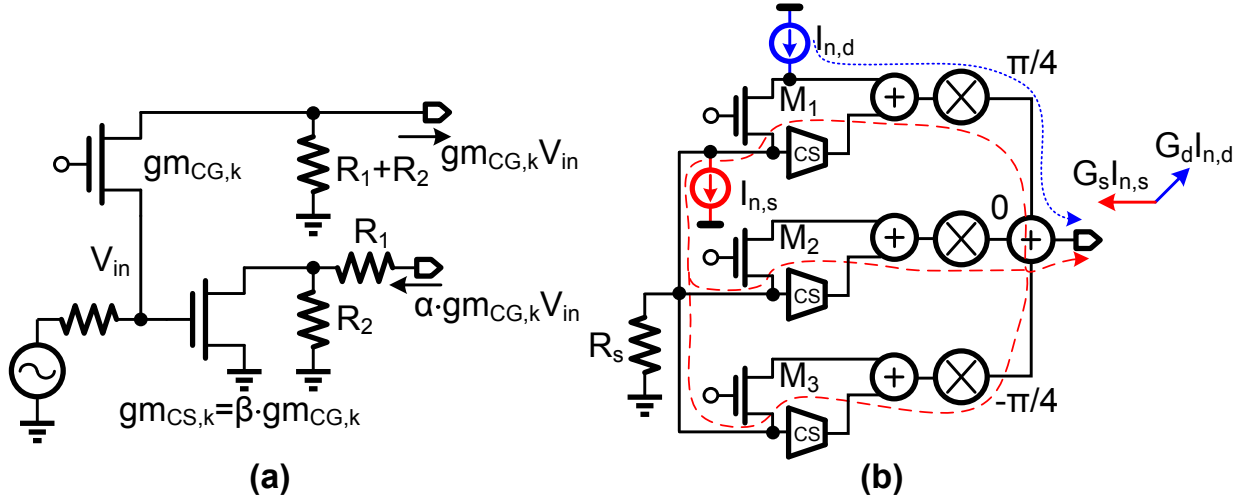


Figure 3.9: (a) Simplified model of the noise-cancelling LNA. (b) Noise cancelling in a harmonic rejection mixer.

The output currents of these two branches are $gm_{CG,k} V_{in}$ and $\alpha gm_{CG,k} V_{in}$, where $\alpha = \beta R_2 / (R_1 + R_2)$.

Thus, the conversion gain can be written as

$$CG = \frac{2}{3} \cdot \text{sinc}\left(\frac{\pi}{8}\right) (1 + \alpha) \eta_{gm} \cdot gm_{CG} R_L gm_{bb} R_{TIA}, \quad (3.13)$$

where η_{gm} indicates the Gm efficiency, and $\eta_{gm} = 2 / (1 + \sqrt{2})$, since all the gm_k s are combined as phasors after down-conversion, and $R_L = R_1 + R_2$.

The double-sideband (DSB) noise factor (F) due to R_s is $F_{R_s} = 1 / \text{sinc}^2(\pi/8)$, since the noise from $(8l \pm 1)^{\text{th}}$ LO harmonics are folded into desired signal band and $\sum_{i=-\infty}^{\infty} \text{sinc}^2(i\pi/8) = 2$ ($i = 8l \pm 1$). The CS transistor mean-square (MS) noise currents from different LNA branches are combined as scalars since those noise sources are independent, and the output noise due to the LNA only has the noise folding from the $(8l \pm 1)^{\text{th}}$ LO harmonics thanks to the baseband harmonic recombination. Since $\overline{V_{n,CS}^2} = 4kT\gamma gm_{CS} (\alpha/\beta)^2 (2/3 \cdot R_L gm_{bb} R_{TIA})^2 \cdot 2$, the additional DSB noise

factor due to the CS stage is

$$F_{CS} - 1 = \frac{1}{\beta} \left(\frac{2\alpha}{(1+\alpha)\eta_{gm}} \right)^2 \gamma_{\text{sinc}^2(\frac{\pi}{8})}. \quad (3.14)$$

The CS stage noise can be easily improved by increasing the gm ratio of CS and CG transistors β .

Using a similar analysis, the additional DSB noise factor due to the LNA load resistor is found to be $F_{RL} - 1 = [2/(1+\alpha)/\eta_{gm}]^2 3R_L/R_s/\text{sinc}^2(\pi/8)$. Assuming a given LNA gain, $A = (1+\alpha)gm_{CG}R_L$, the noise factor can be written as

$$F_{RL} - 1 = \frac{1}{A} \cdot \frac{12}{(1+\alpha)\eta_{gm}^2} \frac{1}{\text{sinc}^2(\frac{\pi}{8})}. \quad (3.15)$$

The load resistor noise can be improved by increasing the LNA gain.

To analyze the CG noise contribution, we split the noise source into two current sources ($I_{n,d}$, $I_{n,s}$) as shown in Fig. 3.9(b), then calculate the output noise voltage from these two sources. $I_{n,d}$ is only transferred to the output by the mixer in one LNA branch while $I_{n,s}$ is transferred to the output through all the branches. Thus, the output voltages $G_d I_{n,d}$ and $G_d I_{n,s}$ are not out-of-phase in the upper and lower LNA branches shown in Fig. 3.9(b), and the CG transistor noise cannot be fully canceled by tuning the gain of CS stage. The DSB noise factor due to CG transistors can be written as

$$F_{CG} - 1 = \left(\frac{2}{(1+\alpha)\eta_{gm}} \right)^2 \sum_{i=-1}^1 \xi_i \left| \eta_{gm} \frac{1+\alpha}{2} - e^{-j\frac{i\pi}{4}} \right|^2 \gamma_{\text{sinc}^2(\frac{\pi}{8})}, \quad (3.16)$$

where $\xi_i = \cos(i\pi/4) / [\sum_{i=-1}^1 \cos(i\pi/4)]$ is the ratio of the gm in the i^{th} CG branch to the total gm in the CG stage. Since the η_{gm} is also a constant, the NF due to CG stage (NF_{CG}) is only a

function of α which is the output current ratio of CS and CG stages. The NF_{CG} versus α is shown in Fig. 3.10. The optimal NF_{CG} is not 0 which indicates that the noise from CG stage cannot be fully canceled. However, compared with the NF_{CG} without noise cancellation ($\alpha = 0$), the NF_{CG} with noise cancellation ($\alpha = 1.9$) is improved by 4.6dB. To fully cancel the CG noise, we can remove M_1 and M_3 in Fig. 3.9(b) and only use M_2 to achieve the impedance matching; then re-scale the CS stages to achieve the harmonic rejection.

Considering $\eta_{gm} = 0.828$, the total DSB noise factor of the receiver due to R_s and NC-LNA can be written as:

$$F = \left(1 + \frac{1}{\beta} \cdot \frac{5.8\alpha^2\gamma}{(1+\alpha)^2} + \frac{5.8\sum_{i=-1}^1 \xi_i \left| 0.41(1+\alpha) - e^{-j\frac{i\pi}{4}} \right|^2 \gamma}{(1+\alpha)^2} + \frac{1}{A} \cdot \frac{17.5}{(1+\alpha)} \right) \frac{1}{\text{sinc}^2\left(\frac{\pi}{8}\right)}. \quad (3.17)$$

The NF lower limit is 1.4 dB, when $\beta = \infty$, $A = \infty$, and $\alpha = 1.9$. For a given LNA gain, the NF is a function of α and β . The calculated and behavioral-level simulated front-end noise figure (NF) versus α with different β for a noisy LNA is shown in Fig. 3.10 with $A = 19$ and $\gamma = 1$. The NF can be improved by increasing the ratio of the CS and CG stage (β). For the $\beta = 4$ condition, the optimal α is 1.4, and the minimum NF is 3.7 dB. In this work, $\alpha = 1$ is used resulting in a 3.8 dB NF which is close to the optimal value and 3.2 dB better than the NF without noise cancellation which is 7 dB. The transistor-level simulated noise figure of the receiver including the baseband Gm is 4.8 dB for a 0.4 GHz LO. The noise contribution breakdown for the simulation is shown in Table. 3.1.

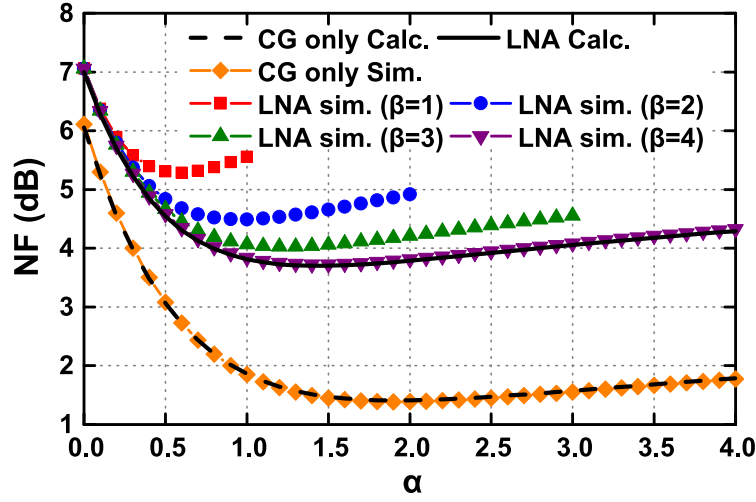


Figure 3.10: Calculated and behavioral-level simulated front-end noise figure with noisy LNA versus factor α .

Table 3.1: Breakdown of the transistor-level simulated noise contribution

	R_s	CS stage	CG stage	R_L	Baseband Gm	Others
Noise Contribution	34.3%	11.1%	15.8%	20.6%	15.6%	2.6%

3.4 Experimental Results and Comparison

The chip was fabricated in a 65nm CMOS process and the active area is $0.65 \times 0.45 \text{ mm}^2$ (Fig. 3.11). Typical measurements are done with a 2.5V analog/RF supply to achieve maximal linearity and a 1.2 V LO supply. The performance for different analog/RF V_{DD} s between 1.8 V and 2.5 V has also been measured. The measured S11 of each RF input is below -10 dB in the frequency range of 150 MHz-1.7 GHz. The remaining measurements have been done with an off-chip 180° hybrid driving the differential RF inputs and the hybrid loss was calibrated out. The LNA output can be measured through the RF test output shown in Fig. 3.6, the loss due to the resistor between LNA output and test output has been calibrated out in the measurement. The measured LNA transfer function (Fig. 3.12) shows the effect of the HR-NPF; the different traces are for LOs from 0.2 GHz

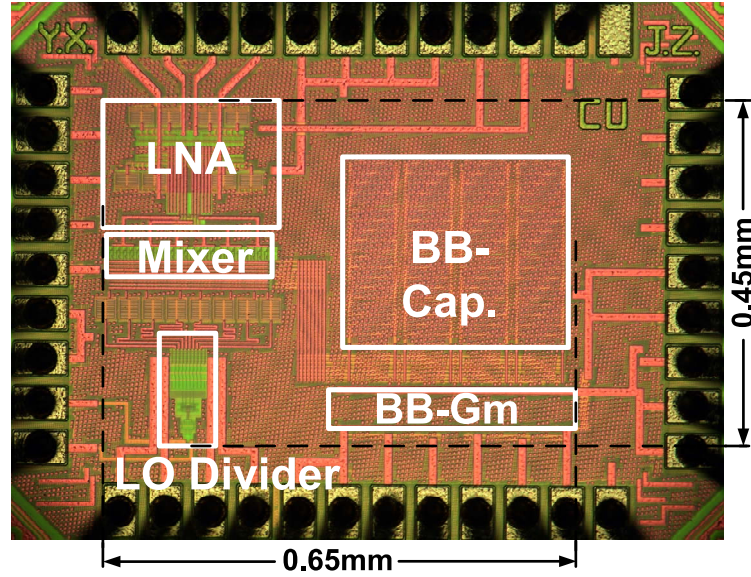


Figure 3.11: Chip photo

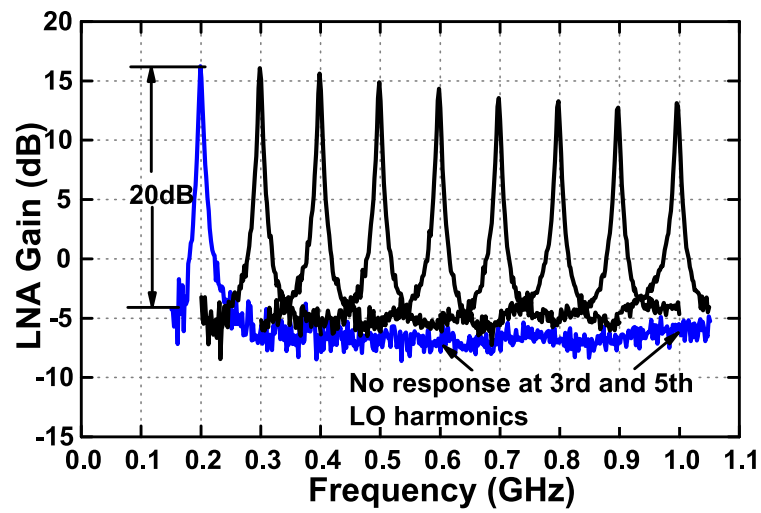


Figure 3.12: LNA transfer function measured at RFtest for LO frequencies swept from 0.2 to 1GHz with a 0.1GHz step

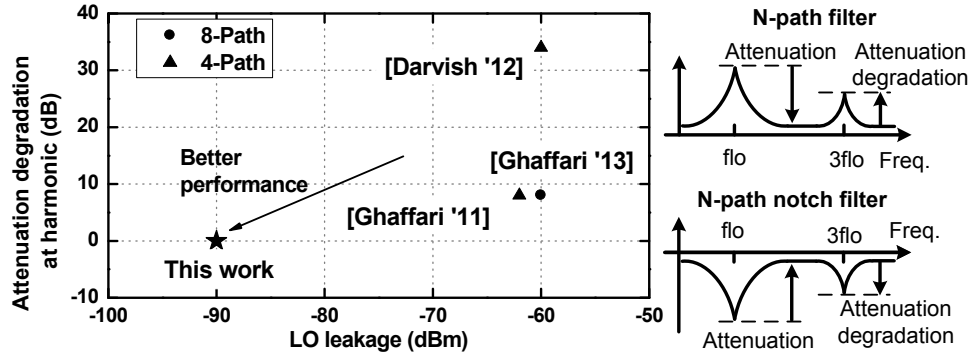


Figure 3.13: Harmonic attenuation performance compared with other N-path filters.

to 1 GHz, spaced at 0.1 GHz²; the trace for an LO of 0.2 GHz shows an OB attenuation of around 20 dB and illustrates that there are no harmonic responses at the 3rd and 5th LO harmonics which are 0.6 GHz and 1 GHz respectively. The LNA, baseband Gm, and LO generator consume 12 mA, 12 mA, and between 2 and 8 mA respectively.

Fig. 3.13 shows harmonic attenuation performance compared with various NPFs [23, 25, 68]. The attenuation degradation at the LO harmonics shows the difference between the attenuation at the 3rd order LO harmonic frequency and other OB frequencies. In contrast to earlier work, the presented HR-NPF achieves high harmonic attenuation with low LO leakage and has zero degradation which means the OB rejection is flat around the 3rd order LO harmonic.

The B1dB versus blocker frequency was measured with an LO frequency of 0.2 GHz and an in-band signal at 0.201 GHz as shown in Fig. 3.14(a), since the worst-case scenario for harmonic responses to blockers occurs for the lowest RF input frequency. For a blocker at a frequency offset of only 20 MHz, the B1dB is -2.4 dBm and the B1dB remains high at the 3rd and 5th LO harmonics. The B1dB also remains high beyond the 1 GHz RF bandwidth of the receiver. Only at the OB LO

²The LNA RF bandwidth is limited by the large LNA output impedance.

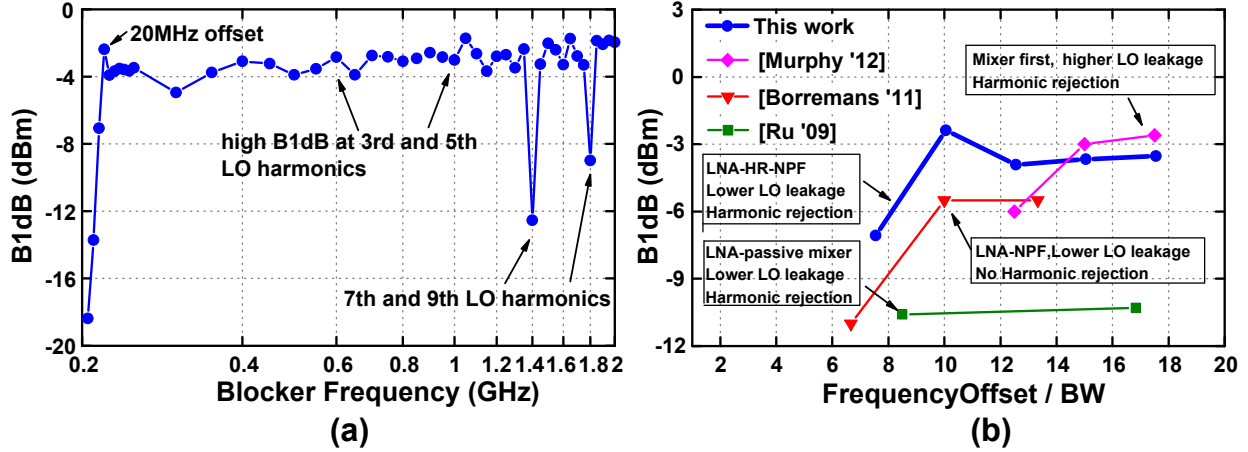


Figure 3.14: (a) Measured blocker 1dB compression point (B1dB) versus blocker frequency for an LO frequency of 0.2GHz. (b) B1dB versus relative blocker frequency offset compared with other blocker tolerant RXs.

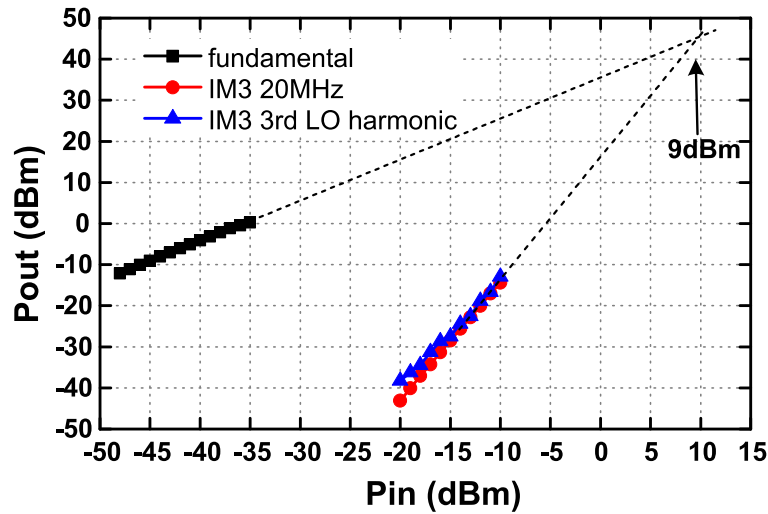


Figure 3.15: Measured out-of-band IIP3 for the OB signal located at 20MHz offset and 3rd order LO harmonic.

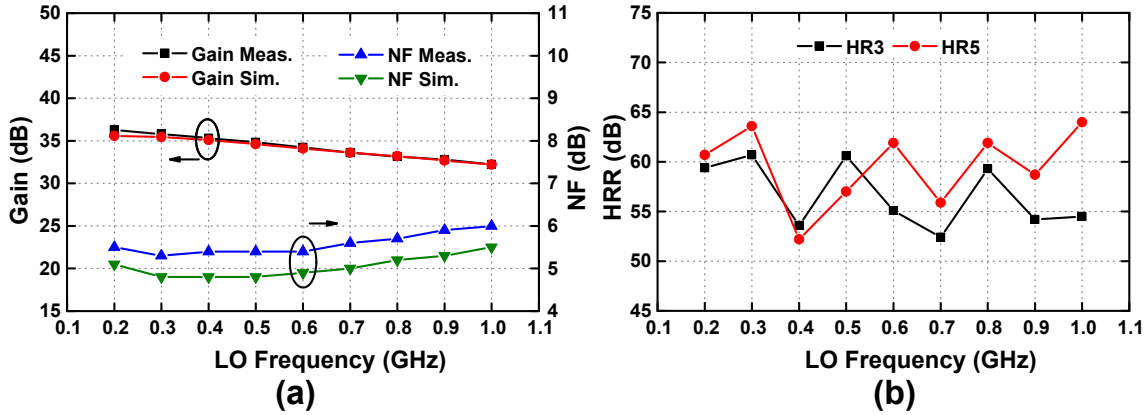


Figure 3.16: (a) Measured and simulated conversion gain and noise figure, (b) measured harmonic rejection ratio versus LO frequencies.

harmonics at 1.4 GHz (7th) and 1.8 GHz (9th) is the B1dB reduced but the interference from those harmonic frequencies can be filtered with an off-chip RF low-pass filter with fixed bandwidth. Fig. 3.14(b) shows the B1dB for low frequency offsets compared with other blocker tolerant receivers [29,35,59]. Frequency offset/IFBW is used as the x-axis to normalize the comparison since the receiver bandwidths are all different. For [35] the BW after LNA and B1dB at low gain have been plotted for best performance. Our work achieves a higher B1dB at low frequency offsets thanks to the HR-NPF and high V_{DD} . The OB-IIP3 (Fig. 3.15) is 9 dBm for an LO of 0.2 GHz. The OB-IIP3 at low frequency offset (two tones: 0.221 GHz and 0.241 GHz) and at LO harmonics (two tones: 0.401 GHz and 0.601 GHz) are nearly the same.

The gain, noise figure, and HR3 and HR5 versus LO frequency are shown in Fig. 3.16. The gain is 36 dB at 0.2 GHz and reduces to 32 dB at 1 GHz. The front-end noise figure is 5.5 dB at 0.2 GHz and 6 dB at 1 GHz. The measured HR3 and HR5 are both better than 51 dB at any LO frequency. The harmonic rejection of 10 samples was measured at 0.2GHz (Fig. 3.17); the minimum HR3 is 51 dB and minimum HR5 is 53 dB. Those HRRs are achieved without calibration. Fig. 3.17

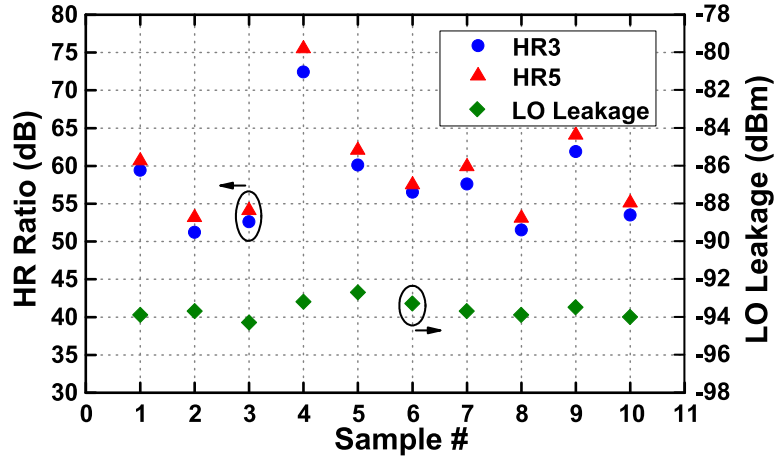


Figure 3.17: Measured harmonic rejection ratio with a 0.2 GHz LO and LO leakage with 1 GHz LO for 10 samples

also shows the LO leakage of 10 samples with 1 GHz LO, and the LO leakages are all lower than -90 dBm.

The gain, noise figure and HRR versus V_{DD} with a 0.2GHz LO are shown in Fig. 3.18(a). Those performances change only a little when V_{DD} is changed, since both the LNA and baseband Gm are current-biased. The linearity versus V_{DD} is shown in Fig. 3.18(b). With higher V_{DD} the OB linearity is improved, thanks to larger headroom at each amplifier output. The B1dB@20MHz is improved more, since at that frequency the blocker attenuation is limited by the filter order, though the clipping the at amplifier output still limits the large signal linearity when V_{DD} is low.

The comparison with the state of the art is shown in Table. 3.2. This work has lower LO leakage as compared with other works. The B1dB is -2.4 dBm at 20 MHz offset, and remains high at the LO harmonics. The receiver in [62] also achieves high B1dB at the LO harmonics but it doesn't have harmonic rejection at the RF input which makes the B1dB at the LO harmonics lower than at other OB frequencies.

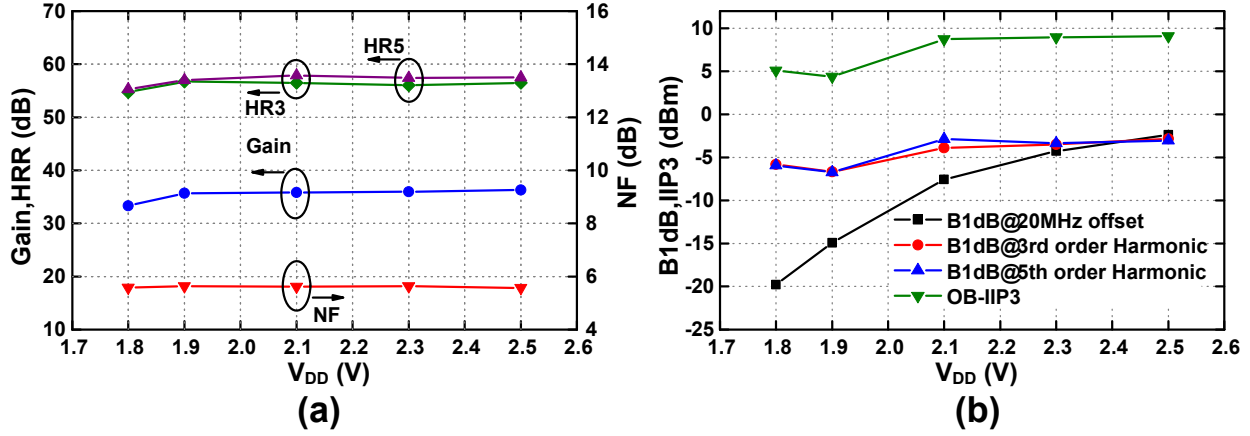


Figure 3.18: (a) Gain, noise figure, harmonic rejection ratio and (b) OB-IIP3, OB-B1dB versus V_{DD} measurement with a 0.2 GHz LO

Table 3.2: Comparison with the state of the art

	This work	N-path filter			Blocker tolerant RX				
		Darvishi JSSC '12	Ghaffari JSSC '13	Darvishi JSSC '13	Murphy JSSC '12	Borremans JSSC '11	Ru JSSC '09	Limpd JSSC '14	Murphy JSSC '15
Technology	65nm	65nm	65nm	65nm	40nm	40nm	65nm	28nm	28nm
RF Input	Differential	Single-ended	Differential	Differential	Single-ended	Differential	Differential	Differential	Differential
Offchip Inductor	4	0	0	0	0	2	2	2	0
Frequency (GHz)	0.2-1	0.4-1.2	0.1-1.2	0.1-1.2	0.08-2.7	0.4-6	0.4-0.9	0.4-6	0.1-3.3
LO leakage (dBm)	<-90	<-60	<-60	<-64	NR	NR	NR	NR	NR
B1dB(dBm)	-2.4@20MHz -2.8@3flo	NR	NR	7@50MHz	-6@25MHz	- 5.5@20MHz ^a	- 10@100MHz	- 12@80MHz	0.5@8MHz -6.5@3flo
OB-IIP3 (dBm)	9	29	NR	26	13.5	10	18	8	11.5
Gain (dB)	36	12	-1.4	25	70	70	34	70	NR
NF (dB)^e	5.4-6	10	1.6-2.5	2.7-3.1	1.4-2.4	3-8	3.5-4.4	1.8-3.1	1.7
BW (MHz)	2	21	NA	8	2	0.4-30	12	0.5-50	0.2-3
HA3 of NPF (dB)	20	20	14 ^b	NR	NA	NA	NA	NA	NA
HR3/5 (dB)	>51/>52	NA	NA	NA	42/45	NR	>60/>64	70/75 ^c	60/60
VDD (V)	1.2/2.5	1.2/2.5	NR	1.2	1.3	1.1/2.5	1.2	0.9	1
Power (mA)	26-32 ^d	15.6	3.5-30mW	15-48	27-60	30-55mW	41-50	44.4	36.8-62.4
Active area (mm²)	0.29	0.127	0.14	0.27	1.2	2	1	0.6	5.2

NR: not reported, NA: not applicable

a. RF filtering BW 15MHz, 6dB lower than max gain. b. For notch filter attenuation difference between fundamental and 3rd order harmonics is used as HA. c. with calibration.

d. Analog 24mA, Digital (clock) 2-8mA. e. 1-dB typical input balun loss should be included for RXs with differential inputs.

In the conventional receiver with NPF, it is hard to achieve a high OB linearity at LO harmonics due to the NPF harmonic response [23] [25] [26]. The harmonic rejection at baseband is achieved in [36] [69] [62], but those receivers have a harmonic response before the down-conversion, thus the OB linearity at LO harmonics is still not as good as at other OB frequencies. In this work, the HR-NPF rejects the harmonic down-conversion before the baseband Gm and reduces the LNA load impedance at LO harmonic frequencies, such that high OB-IIP3 and B1dB at 3rd and 5th order LO harmonics are achieved.

3.5 Conclusions

In this chapter an RF receiver with harmonic-rejecting N-path filtering is analyzed and implemented. The proposed HR-NPF achieves large OB attenuation and high harmonic attenuation at the LNA outputs, thus, the receiver achieves high B1dB at both low offset frequencies and the 3rd and 5th LO harmonics to make sure the receiver can tolerate an OB blocker at any frequency in the 0.2-1 GHz frequency range. This receiver also achieves <-90 dBm LO leakage and high HRR without calibration.

The HR-NPF offers a wideband OB interferer tolerance. However, the OB linearity is limited by active LNA. In the following chapters, high-order SC RF bandpass filters are presented to achieve much higher interferer tolerance especially for close-by blockers.

Chapter 4

Switched-Capacitor RF Receiver with Programmable High-Order Filtering

4.1 Introduction

As discussed in Chapter 1, wideband receivers (RX) are critical for the implementation of software-defined radio (SDR) and cognitive radio (CR) systems. In those systems, the goal is to replace the high-quality fixed off-chip radio-frequency (RF) filters with tunable RF filtering so that a blocker-tolerant RF receiver can be realized (Fig. 4.1(a)). RF MEMS filters have been proposed to achieve the off-chip high-quality tunable filters, but they suffer from limited tuning range, in-band loss and large size [32]. Switched-capacitor (SC) N-path RF filters implemented in CMOS realize the tunable high-quality filtering [22, 23, 26, 35–37, 64] to improve the out-of-band (OB) linearity. An NPF at the low-noise amplifier (LNA) output [35, 36, 64] reduces the OB-blocker voltage swing,

but the overall OB linearity remains limited by the nonlinear LNA. An NPF preceding the LNA as shown in Fig. 4.1(b) [37] attenuates RF input blockers, but the stop-band rejection is limited by the switch-on resistance (R_{on} ; Fig. 4.2). In [26], active circuits are used to realize a high-order N-path filter (NPF) with larger OB attenuation. However, before the first active amplifier, there is still a conventional NPF with limited OB attenuation. In mixer-first receivers [27–31], the active amplifiers are attached to capacitors (Fig. 4.1(c)) so that the stop-band rejection is not limited by R_{on} . But the filtering before the nonlinear active circuits is only first order so that the OB linearity for a close-by blocker is still not high enough (Fig. 4.2).

In our proposed SC RF receiver (SCRX) (Fig. 4.1(d)) [70], high-order filtering is achieved by linear passive SC circuits to highly attenuate the OB blockers before they reach the nonlinear active baseband amplifier (Fig. 4.2). Passive discrete-time (DT) SC circuits, which are easier to scale with process and have low process-voltage-temperature (PVT) variations, have been used as intermediate frequency (IF) filters in RF receivers [49–53]. In emerging CMOS processes, active circuits are more difficult to design due to the low voltage headroom and low intrinsic gain [71], while the passive SC circuits benefit from faster switches and higher clock speeds. Moreover, passive SC circuits have good linearity. However, in a conventional DT receiver [49–52, 69], those circuits are used after the LNA, thus the nonlinear active LNA still limits the OB-blocker tolerance. In our design, high-order linear SC filtering is achieved prior to the active amplifier to maximize the benefit of the filtering by the linear SC circuits.

The proposed SCRX not only achieves filtering, but also realizes RF impedance matching and harmonic-rejecting down conversion. A similar high-order SC filter is shown in [72]. How-

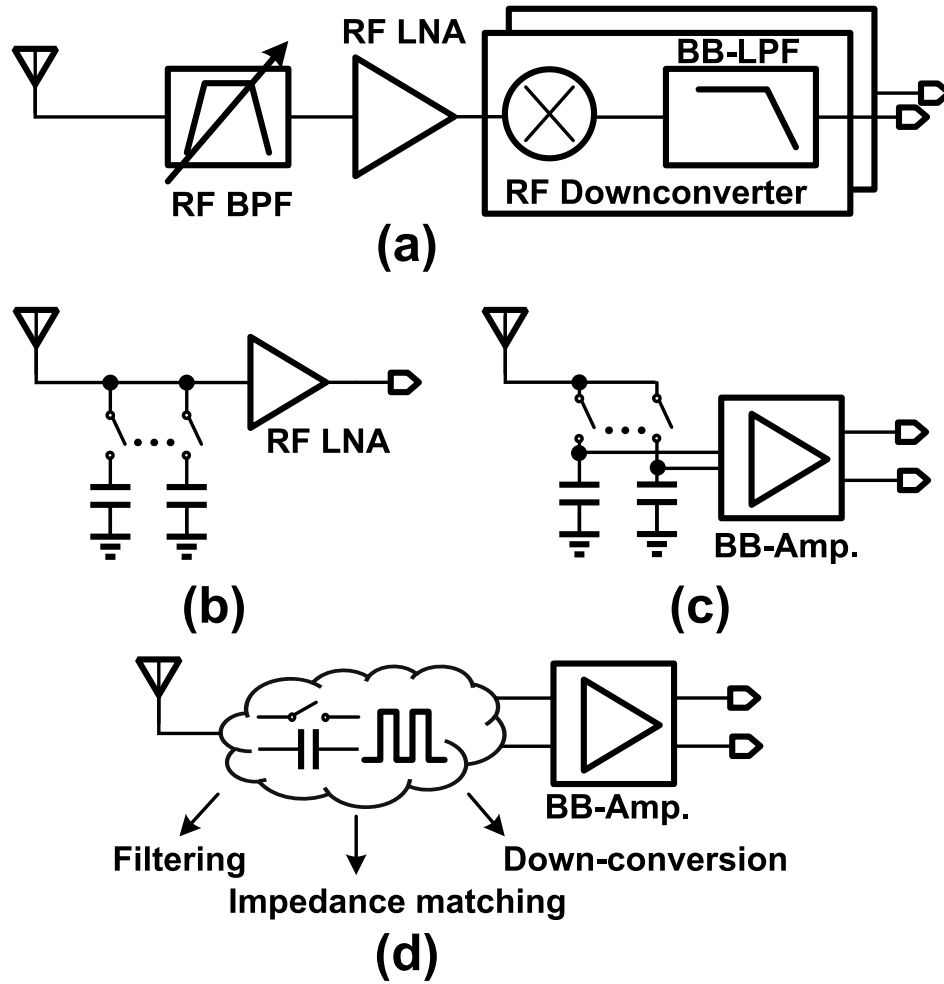


Figure 4.1: (a) Wideband receiver with an off-chip RF bandpass filter. (b) A wideband receiver with an N-path filter at the RF input. (c) A mixer-first receiver. (d) Proposed switched-capacitor receiver with filtering, impedance matching and down-conversion performed with switches and capacitors only.

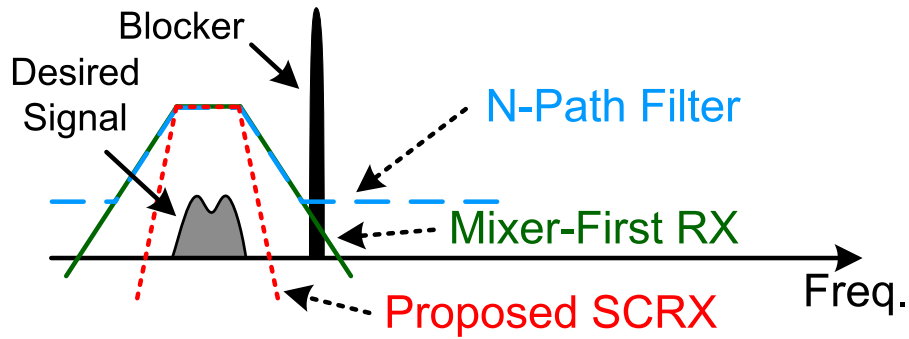


Figure 4.2: Equivalent RF filtering before the nonlinear active circuits of an N-path filter, a mixer-first receiver, and the proposed switched-capacitor receiver.

ever, it cannot achieve the impedance matching for the RF receiver, also the voltage-sampling approach would increase the noise figure (NF) due to noise folding. In [31], a SC circuit is used for impedance matching, but it can only provide first-order filtering as with other mixer-first designs.

The rest of this chapter is organized as follows. The concept and analysis of the SCRX are described in Section 4.2. The front-end architecture and circuit implementation are presented in Section 4.3. Section 4.4 provides the measurement results. The conclusions are presented in Section 4.5.

4.2 Switched-Capacitor RF Front End Concept and Analysis

4.2.1 Basic Concept

Fig. 4.3(a) shows the architecture of a single-ended version of the SC receiver. It is implemented with eight RF SC banks followed by baseband Gm cells and transimpedance amplifiers (TIAs). All the switches are driven by an eight-phase, nonoverlapping clock signal $p(i)$ as shown in Fig. 4.3(b).

The sampling frequency is f_s , and the equivalent LO frequency of this zero-IF receiver is $f_{lo} = f_s/8$. At the RF input, capacitors $C_{h0}\langle i \rangle$ with the $s_0\langle i \rangle$ switches in all eight banks realize an RF NPF to attenuate the OB signals. After that, a SC circuit is used for impedance matching, which is realized by capacitors $C_s\langle i \rangle$ with switches $s_1\langle i \rangle$ and $s_6\langle i \rangle$. Also, here the RF signal is sampled on $C_s\langle i \rangle$, and the continuous-time (CT) signal is converted to DT domain. After sampling, history capacitors $C_{h1}\langle i \rangle$ – $C_{h3}\langle i \rangle$ and the switches attached to those capacitors ($s_2\langle i \rangle$ – $s_4\langle i \rangle$) as well as $C_s\langle i \rangle$ and $s_6\langle i \rangle$ realize a high-order DT infinite-impulse-response (IIR) filter [57], and switches $s_5\langle i \rangle$ propagate the signal to the Gm input nodes. The Gm cells on the in-phase (I) and quadrature (Q) paths combine the signal from all eight SC banks and achieve the harmonic rejecting down-conversion [36]. Also, here the DT signal is converted back to the CT domain. A conventional RF receiver can be replaced by the proposed SCRX since the TIA output voltages are CT I/Q-baseband signals.

The SCRX achieves different circuit functions in sequential time intervals as shown in Fig. 4.3(c). For SC Bank #1, the RF signal is sampled on C_s in sampling phase p_1 , propagated to the Gm input node in p_5 , and dumped to ground in p_7 . From p_2 to p_4 , the signal is filtered with increasing order. The blank time intervals relax the timing constraints, and the eight banks operate in a time-interleaved fashion.

4.2.2 Core Switched-Capacitor RF Front End without Filtering

Fig. 4.4(a) shows the SCRX without filtering. The signal path can be modeled as in Fig. 4.4(b). Since the $s_1\langle i \rangle$ switches in the eight banks are turned on one after another, the input signal is consecutively sampled on $C_s\langle i \rangle$. Those sampled voltages, $V_{sp}[k]$ to $V_{sp}[k+7]$ ($k = 8 \cdot l, l \in \mathbb{Z}$), can

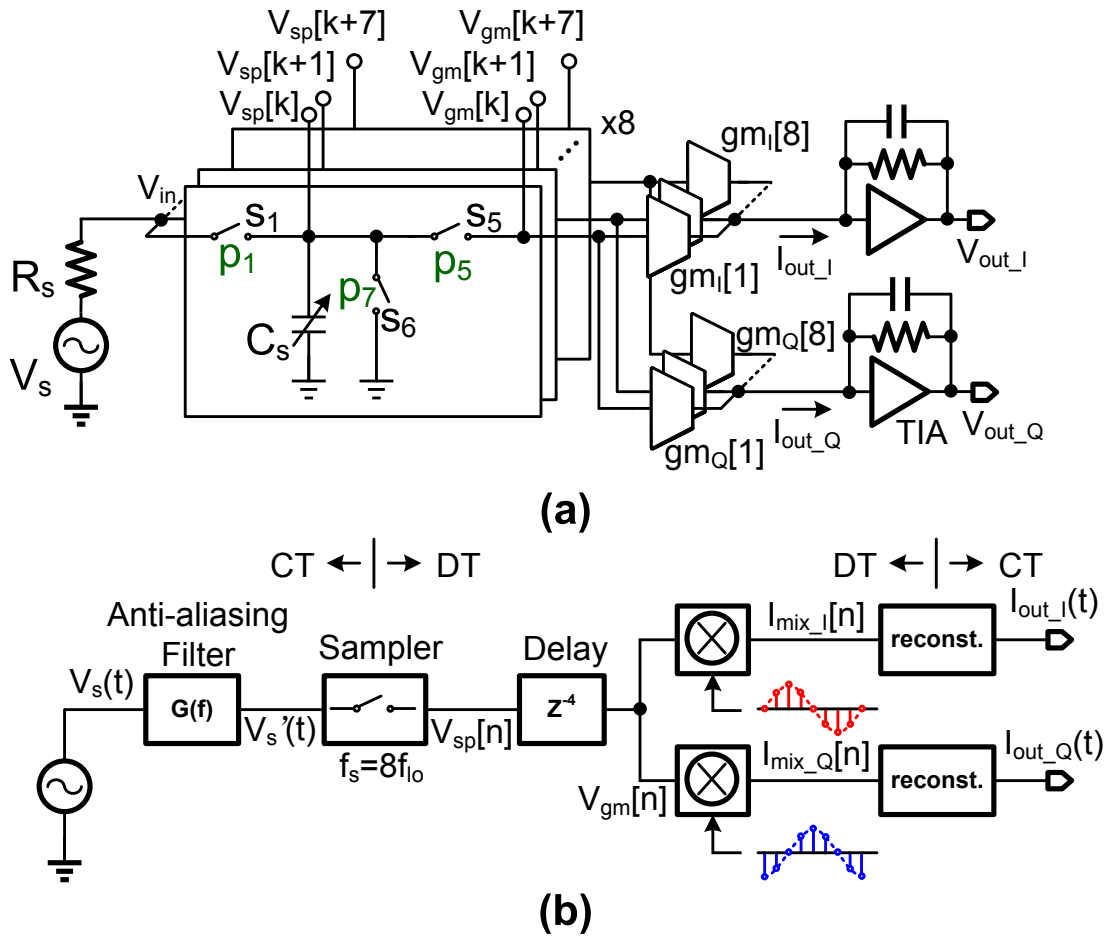


Figure 4.4: (a) Simplified RF SC receiver without filtering. (b) Model of the SC receiver.

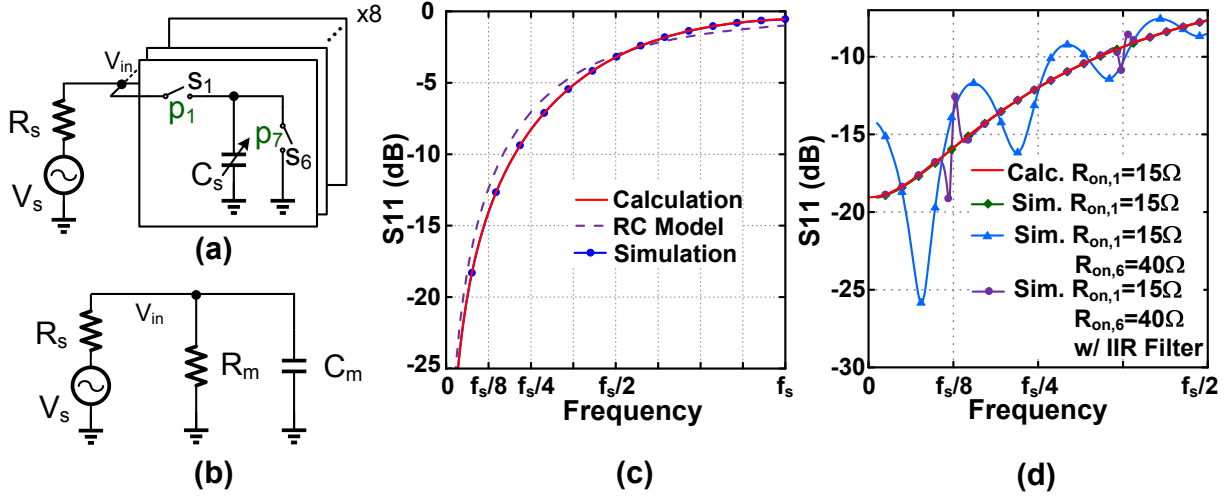


Figure 4.5: (a) Switched-capacitor impedance-matching circuit. (b) RC model of the impedance-matching circuit. (c) Calculated and simulated S_{11} with ideal switches. (d) Calculated and simulated S_{11} with finite R_{on} and the differential IIR filter loading the circuits.

be considered as one time-interleaved signal $V_{sp}[n]$ with sampling frequency f_s . The sampler with source resistor R_s can be mathematically modeled as an ideal sampler with a CT antialiasing filter $G(f)$ as discussed in a later subsection. The signal $V_{sp}[n]$ is propagated to the Gm inputs after a delay of $4/f_s$. The Gm cells are modeled as a DT mixer with a reconstruction circuit converting the DT voltage to a CT current.

Two key features of the SCR_X are the 50Ω input impedance matching with higher in-band gain than resistive matching and RF sampling with intrinsic antialiasing filtering.

RF Impedance Matching

The input impedance matching is achieved by charging and discharging $C_s\langle i \rangle$ (Fig. 4.5(a)) as discussed in [70]. Since $V_{in} = Z_{in}/(Z_{in} + R_s) \cdot V_s$, the input impedance can be calculated from V_{in} and V_s (Fig. 4.5(a)). The input impedance at a certain frequency f is defined as the input voltage

at f divided by the input current at the same frequency. To analyze V_{in} , a linear periodically time varying (LPTV) approach is required since the matching circuit is a CT SC system. In an LPTV system, the frequency domain input voltage $V_{in}(f)$ is a summation of filtered source voltage $V_s(f)$ with frequency shifts [67]:

$$V_{in}(f) = \sum_{n=-\infty}^{\infty} H_n(f) V_s(f - n f_s). \quad (4.1)$$

To calculate the input impedance $Z_{in}(f)$, we just need $H_0(f)$ in (4.1). The input impedance can be calculated by $Z_{in}(f) = H_0(f)/(1 - H_0(f)) \cdot R_s$. Using a similar approach as in [73,74], H_0 is derived in the appendix:

$$H_0(f) = \frac{1}{1 + jf/f_{rc}} \left[1 - \frac{f_s/2\pi f_{rc}}{1 + jf/f_{rc}} \left(1 - e^{-2\pi(f_{rc} + jf)/f_s} \right) \right], \quad (4.2)$$

where $f_{rc} = 1/(2\pi R_s C_s)$, and f_s is the sampling frequency. The input admittance ($Y_{in}(f) = 1/Z_{in}(f)$) can now be expressed as

$$Y_{in}(f) = \frac{jf/f_{rc} - (f/f_{rc})^2 + f_s/2\pi f_{rc} \left(1 - e^{-2\pi(f_{rc} + jf)/f_s} \right)}{1 + jf/f_{rc} - f_s/2\pi f_{rc} \left(1 - e^{-2\pi(f_{rc} + jf)/f_s} \right)} \cdot \frac{1}{R_s}. \quad (4.3)$$

The admittance is a function of f_{rc} . To match the DC input admittance to $1/R_s$, $Y_{in}(0) = 1/R_s$.

Evaluating (4.3) at DC and equating it to $1/R_s$, the equation for f_{rc} is

$$e^{-2\pi f_{rc}/f_s} + \frac{2\pi f_{rc}/f_s}{2} - 1 = 0. \quad (4.4)$$

Solving this transcendental equation, we obtain $f_{rc} \approx 0.25f_s$ and $C_s \approx 0.63/f_s R_s$, so the C_s needs to be tuned with different LO frequencies. Using (4.4) and given that $\exp(-2\pi f_{rc}/f_s)$ is small, the input admittance can now be simplified to

$$Y_{in}(f) = \left(\frac{1 + 2(f/f_{rc})^2}{1 + 4(f/f_{rc})^2} + j \frac{4(f/f_{rc})^3}{1 + 4(f/f_{rc})^2} \right) \cdot \frac{1}{R_s}. \quad (4.5)$$

At low frequencies ($f \ll f_{rc}$), the real part is dominant and equal to $1/R_s$. At high frequencies ($f \gg f_{rc}$), the imaginary part becomes larger, which can be modeled as a capacitor equal to C_s . The input impedance of the SCRX can thus be modeled as a resistor $R_m = R_s$ in parallel with a capacitor $C_m = C_s$ as shown in Fig. 4.5(b). Considering $f_{rc} \approx 0.25f_s$, $Y_{in}(f)$ can be normalized by f_s . Fig. 4.5(c) shows the S_{11} with ideal switches simulated with Spectre RF. The calculated S_{11} , using (4.3), and the RC model are also shown in Fig. 4.5(c) and match the simulation well. The S_{11} in the desired signal band around $f_{lo} = f_s/8$ is lower than -10 dB.

The S_{11} with finite switch R_{on} is shown in Fig. 4.5(d). $R_{on,1}$ is simply in series with Z_{in} of the SC circuit, and the calculated S_{11} with finite $R_{on,1}$ matches the simulation well. A non-zero $R_{on,6}$ however changes the shape of S_{11} since the C_s voltage is not fully reset in the resetting phase. The IIR filter (discussed in a later section) attenuates the OB signal before resetting, which makes the OB S_{11} close to the S_{11} with an ideal s_6 . The S_{11} in the signal band changes due to non-zero $R_{on,6}$.

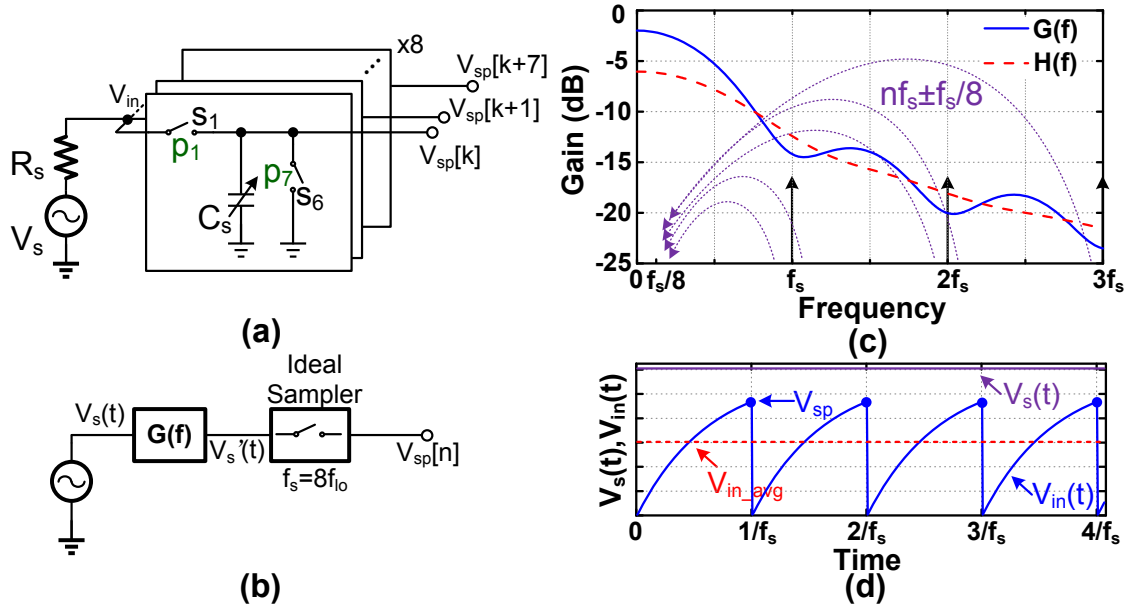


Figure 4.6: (a) Sampling circuit. (b) Model of the sampling circuit. (c) Calculated transfer function of the CT antialiasing filter $G(f)$. (d) Simulated input voltage transient wave form for a DC (0 Hz) source voltage.

RF Sampling

The RF sampler consists of s_1 , s_6 and C_s (4.6(a)). It can be modeled as a CT filter $G(f)$ and an ideal sampler as shown in Fig. 4.6(b). The $G(f)$ is derived in the appendix as

$$G(f) = \frac{1}{1 + jf/f_{rc}} \cdot \left[1 - e^{-2\pi(f_{rc} + jf)/f_s} \right]. \quad (4.6)$$

The first part of $G(f)$ is a first-order low-pass filter with a constant of $R_s C_s$, while the second part is a FIR filter with a delay of $1/f_s$. Considering $f_{rc} \approx 0.25f_s$, $G(f)$ can be normalized by f_s . Fig. 4.6(c) shows the $G(f)$ and $H(f)$ ($= V_{in}/V_s$) transfer curves. Since the input impedance is matched to R_s , the gain of $H(f)$ at the LO frequency ($f_s/8$) is -6 dB as in resistive matching, while $G(f)$ is -2.2 dB. This means the sampler provides a 3.8 dB passive gain (V'_s/V_{in}) because, when the switch

s_1 is turned on, the C_s voltage is charged from zero to V_{sp} , while V_{in} is the “average” voltage of the whole charging period as shown in the V_{in} transient wave form for a DC (0 Hz) source voltage V_s in Fig. 4.6(d).

The sampler operates between a voltage sampler and an integration sampler. In a voltage sampler, the C_s voltage follows the source voltage when the switch is turned on, and the high-frequency signals around the sampling frequency and its harmonics will be folded into the desired signal band. In an integration sampler, when the switch is turned on, the C_s voltage is the integral of the source current ($I_s = V_s/R_s$). The integration sampler has intrinsic antialiasing filtering with nulls at nf_s ($n \neq 0$) [75]. The key difference between the voltage and integration sampler is the FIR part in (4.6). The RC constant is relatively small ($R_s C_s \ll 1/f_s$) in a voltage sampler, and the FIR part in $G(f)$ can be ignored. In an integration sampler, the RC constant is large ($R_s C_s \gg 1/f_s$). Then the FIR filter generates deep nulls at the sampling frequency and its harmonics which reduces the aliasing. In this work, the RC constant is close to the sampling period, which makes it between a voltage and an integration sampler. Using $f_{rc} \approx 0.25f_s$, the bandwidth of the RC-filtering part in $G(f)$ is around $0.25f_s$. Also, the FIR filtering part in $G(f)$ provides more attenuation around the sampling frequency and its harmonics, although the attenuation is lower than in the integration sampler. The $G(f)$ transfer function is shown in Fig. 4.6(b). The $G(f)$ provides more than a 10 dB rejection to reduce the signal and noise folding from $nf_s \pm f_s/8$.

DT Down-conversion and Reconstruction

The Gm cells in Fig. 4.4(a) are modeled as a DT mixer with a reconstruction circuit. The DT mixing can be expressed as $I_{\text{mix-}\{I,Q\}}[n] = V_{\text{gm}}[n] \cdot \text{gm}_{\{I,Q\}}[\text{mod}(n,8) + 1]$, where $\text{mod}(\cdot)$ is the modulus function. By scaling $\text{gm}[i]$ as a DT sine wave, we obtain the down-converted $\{I, Q\}$ signal at the mixer output. The gm factors $\text{gm}[1]$ to $\text{gm}[8]$ in the I path need to be sized as $\sin((i-1) \cdot 4/\pi)$, which are 0, 1, $\sqrt{2}$, 1, 0, -1 , $-\sqrt{2}$, -1 , 0, while the gm factors in the Q path are $-\cos((i-1) \cdot 4/\pi)$ as in a harmonic rejecting mixer (HRM) [36]. So, only the signal around $f_s/8$ in the Nyquist bandwidth $f_s/2$ will be down-converted to baseband. Nonidealities like gain and phase mismatches will reduce the harmonic rejection ratio (HRR) as in other HRM [36].

Besides performing down-conversion, the Gm cells also convert the signal from the DT to the CT domain. The reconstruction is a zero-order hold with a hold time of $8T_s$ ($T_s = 1/f_s$); the output current can be expressed as $I_{\text{out-}\{I,Q\}}(t) = \sum_{n=-\infty}^{\infty} I_{\text{mix-}\{I,Q\}}[n] \cdot \text{rect}((t - 4T_s - nT_s)/8T_s)$, where $\text{rect}(\cdot)$ is the rectangular function.

Combining antialiasing filtering, sampling, DT mixing with harmonic rejection and reconstruction, the conversion gain of the receiver is

$$CG(f_{in}) = \frac{V_{out}(f_{in} - f_s/8)}{V_s(f_{in})} = G(f_{in}) \cdot \frac{1}{T_s} \cdot \frac{1}{2} \text{gm} \cdot 8T_s \text{sinc}\left(\pi \frac{f_{in} - f_s/8}{f_s/8}\right) \cdot R \approx 4G(f_{in}) \text{gm}R, \quad (4.7)$$

where f_{in} is the input RF frequency around LO frequency of $f_s/8$, gm is the transconductance of the Gm cell with a size of $\sqrt{2}$, and R is the feedback resistor in the TIA. The sinc function approximates to 1 for f_{in} close to $f_s/8$.

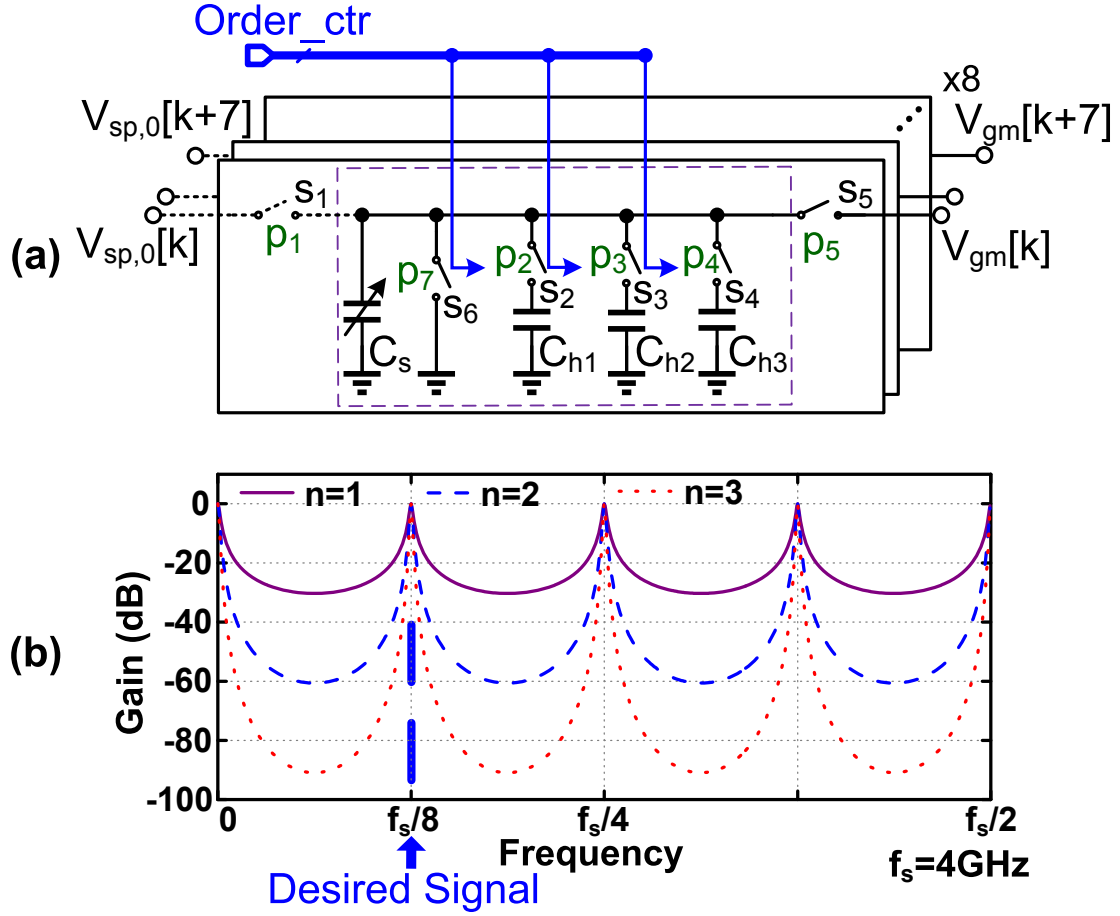


Figure 4.7: (a) Schematic of the IIR filter with programmable order. (b) Calculated transfer function of the IIR filter for $f_s = 4$ GHz, $C_s = 3.15$ pF, and $C_h = 50$ pF.

4.2.3 Programmable High-Order DT IIR Filter

The DT IIR filter consists of capacitors $C_s, C_{h1}-C_{h3}$ and switches s_2-s_4, s_6 as shown in Fig. 4.7(a). Instead of cascading first- or second-order filters as in [50, 51, 69], the high-order filter is implemented by charge rotating [57]. In each cycle of $8/f_s$, after C_s is charged to the finite state of sampling phase $V_{sp,0}$, it sequentially connects to C_{h1}, C_{h2}, C_{h3} , the gm input node, and ground.

When C_{hi} connects to C_s , the C_s voltage and C_{hi} voltage after charge sharing are

$$V_{sp,i}[n] = V_{h,i}[n] = \alpha V_{h,i}[n-8] + (1-\alpha)V_{sp,i-1}[n-1], \quad (4.8)$$

where $\alpha = C_{hi}/(C_{hi} + C_s)$, $i=\{1,2,3\}$, $V_{h,i}$ is the C_{hi} voltage, $V_{sp,i}$ is the C_s voltage after it connects to C_{hi} . Writing (4.8) in the z domain with $z = \exp(j2\pi f/f_s)$, the C_s voltage can be expressed as

$$V_{sp,i}(z) = \frac{1-\alpha}{1-\alpha z^{-8}} \cdot z^{-1} \cdot V_{sp,i-1}(z). \quad (4.9)$$

This shows that each C_{hi} provides a first-order IIR filtering. If C_{hi} is not connected, the transfer function (4.9) is just a delay (z^{-1}). The filter order can thus be tuned by enabling or disabling the clock signal for s_i connected to C_{hi} . When the clock signal is disabled, its clock driver can be turned off to save power providing a trade-off between filter order and power consumption.

Since $V_{gm}[n] = V_{sp,3}[n-1]$, the transfer function of the whole IIR filter is

$$\frac{V_{gm}(z)}{V_{sp}(z)} = \left(\frac{1-\alpha}{1-\alpha z^{-8}} \right)^n \cdot z^{-4}, \quad (4.10)$$

where $V_{sp} = V_{sp0}$, and n is the number of C_h being connected, $n=\{0,1,2,3\}$, which is also the IIR filter order. Fig. 4.7(b) shows the calculated IIR filter transfer curves in the Nyquist bandwidth for different filter orders with $f_s = 4$ GHz, $C_s \approx 0.63/f_s R_s$, and $C_h = 50$ pF. The DC and even-order LO harmonic responses will be removed using differential circuits as in a differential NPF [23].

In a DT IIR filter, the bandwidth changes with sampling frequency, since it is proportional

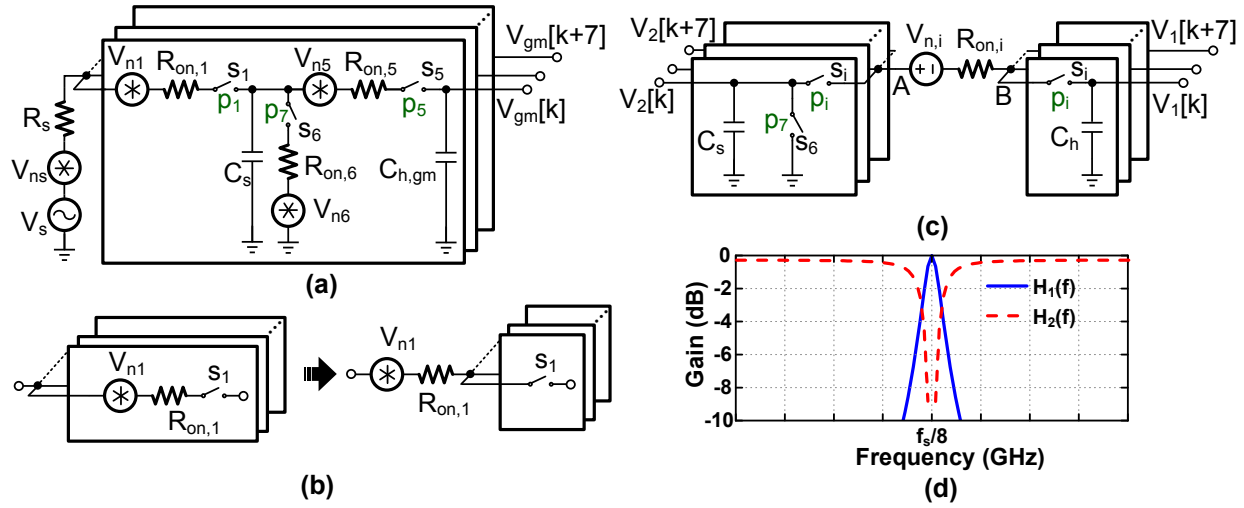


Figure 4.8: (a) Noise sources in the switched-capacitor receiver with filtering. (b) All the noise sources of the s_1 switches can be merged into a single noise source. (c) Simplified schematic for the noise analysis of s_2 to s_5 . (d) Calculated transfer function of voltage source $V_{n,i}$ in (c) to the capacitors C_h ($H_1(f)$) and C_s ($H_2(f)$).

to $f_s C_s / 8 C_h$. In this work, C_s is tuned to $0.63 / f_s R_s$ to achieve the impedance matching. So, the bandwidth is proportional to $0.63 / 8 (R_s C_h)$ and independent of f_s . So the filter bandwidth doesn't change when changing LO frequencies ($f_{lo} = f_s / 8$) and can be tuned by C_h . In this work, C_h is fixed.

4.2.4 Noise Analysis

In the SCRX, the added noise is mainly the thermal noise of the switches. Fig. 4.8(a) shows the noise sources of the SCRX without filtering (Fig. 4.4(a)). Switch s_i is modeled as an ideal switch in series with a parasitic resistor $R_{on,i}$ and a noise voltage V_{ni} . $C_{h,gm}$ is the parasitic capacitor of the Gm cell. Since there is no overlap between the clock signals driving $s_1(i)$ in the eight SC banks, all the white noise source $V_{n1}(i)$ can be merged into a single white noise source, V_{n1} ,

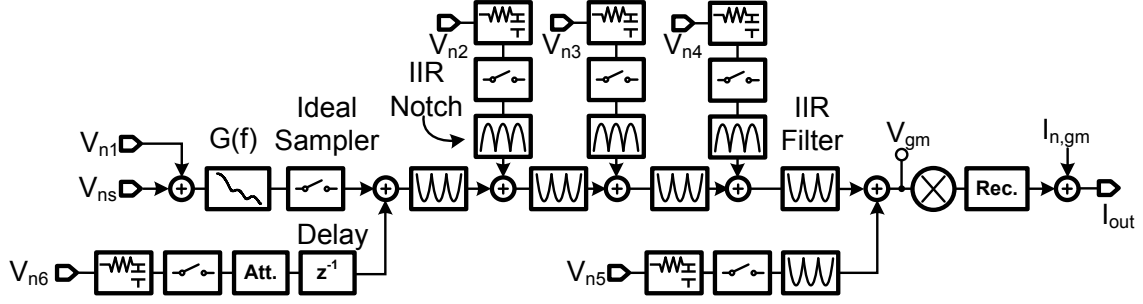


Figure 4.9: Model to calculate the propagation of the noise of the source and switches through the switched-capacitor receiver.

as shown in Fig. 4.8(b). The sampling switch, s_1 , noise is thus added to the source noise V_{ns} as shown in Fig. 4.9 since R_{on} is in series with R_s . The intrinsic antialiasing filter, $G(f)$, reduces the high-frequency noise folding.

The resetting-switch, s_6 , noise is first sampled on C_s . Together, C_s and s_6 are a voltage sampler ($R_{on,6}C_s \ll 1/f_s$) so that the high-frequency noise is folded into the signal band after sampling, resulting in a nearly white noise [76]. The noise spectral density is the total mean-square (MS) noise voltage, kT/C_s , divided by Nyquist bandwidth, $f_s/2$. Then, this sampled noise voltage is partially dumped by R_s when s_1 is turned on for a duration of $1/f_s$ and the noise voltage is reduced by a factor of $\exp(-2\pi f_{rf}/f_s)$. After that, the noise voltage is added to the desired signal as shown in Fig. 4.9. The noise spectral density at the Gm input node in the signal band due to V_{n6} is

$$\overline{V_{gm,n6}^2} = \frac{2kT}{C_s f_s} e^{-1/f_s C_s R_s} \cdot \Delta f. \quad (4.11)$$

Since the noise analyses of the switch s_5 and the switches in the IIR filter are related, we use the same equivalent schematic in Fig. 4.8(c) to analyze their noise transfer functions; $V_{n,i}$ is the noise voltage source of switch s_i , $i=\{2,3,4,5\}$; for the s_5 noise analysis, C_h is $C_{h,gm}$ and for the noise

analysis of the s_{j+1} in the IIR filter, C_h is C_{hj} , $j=\{1,2,3\}$. When s_i is turned on, $V_{n,i}$ is sampled on C_s in series with C_h . Let $V_{n,sp}$ be the sampled noise voltage between node A and B in Fig. 4.8(c) with an MS value of $kT/\alpha C_s$, where $\alpha = C_h/(C_h + C_s)$. The DT voltages on C_h and C_s are

$$V_I[n] = -(1 - \alpha)V_{n,sp}[n] + \alpha V_I[n - 1], \quad V_2[n] = \alpha V_{n,sp}[n] + \alpha V_I[n - 1], \quad (4.12)$$

Solving (4.12), we find

$$H_I(z) = \frac{V_I(z)}{V_{n,sp}(z)} = -\frac{1 - \alpha}{1 - \alpha z^{-8}}, \quad H_2(z) = \frac{V_2(z)}{V_{n,sp}(z)} = \alpha \frac{1 - z^{-8}}{1 - \alpha z^{-8}}. \quad (4.13)$$

H_1 is the s_5 noise transfer function and is an IIR bandpass filter with a 0 dB in-band gain. H_2 is the noise transfer function for the switches in the IIR filter and is a notch filter centered at the desired signal band. The calculated H_1 and H_2 , with $f_s = 4$ GHz and $C_h = 50$ pF, are shown in Fig. 4.8(d).

The s_5 noise is added to the desired signal at the G_m input node, as shown in Fig. 4.9 with an in-band-noise spectral density of

$$\overline{V_{gm,n5}^2} = \frac{2kT}{\alpha_{gm} C_s f_s} \cdot \Delta f, \quad (4.14)$$

calculated using (4.13) where $\alpha_{gm} = C_{h,gm}/(C_{h,gm} + C_s)$.

The switch noise from the IIR filter is added to the desired signal when being sampled on C_s with the transfer function H_2 . The in-band filter noise is first reduced by the IIR notch filtering H_2 ,

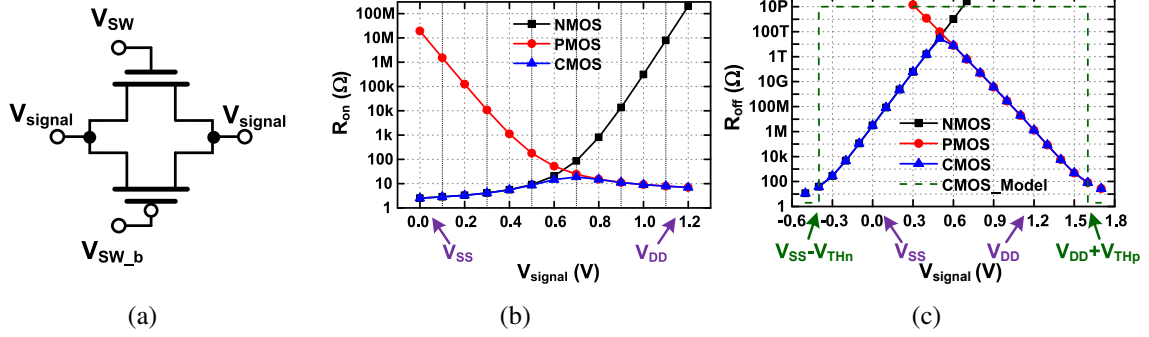


Figure 4.10: (a) Schematic of the CMOS switch, the sizes of the NMOS and PMOS transistors are the same ($W/L = 150 \mu\text{m}/40 \text{ nm}$). (b) Simulated R_{on} of NMOS, PMOS and CMOS switches versus signal voltage. (c) Simulated R_{off} of NMOS, PMOS and CMOS switches versus signal voltage.

then propagated to the output as shown in Fig. 4.9. It can thus be ignored, and the NF will remain almost the same when increasing filter order.

Including the Gm cell noise $\overline{I_{n,gm}^2} = 4kT\gamma(2 + 2\sqrt{2})gm$, the receiver's total double-sideband (DSB) noise factor at the target signal frequency ($f_{lo} = f_s/8$) is

$$F = 1 + \frac{R_{on,1}}{R_s} + \frac{1}{2R_s|G(f_s/8)|^2} \left[\frac{e^{-1/f_s R_s C_s}}{f_s C_s} + \frac{1}{\alpha_{gm} f_s C_s} + \frac{\gamma(1 + \sqrt{2})}{8gm} \right]. \quad (4.15)$$

Using $C_s \approx 0.63/f_s R_s$ and $G(f_s/8)$ from (4.6), (4.15) can be simplified as

$$F = 1 + \frac{R_{on,1}}{R_s} + 0.27 + 1.32/\alpha_{gm} + \frac{0.25\gamma}{gmR_s}. \quad (4.16)$$

Since $R_{on,1}$ is relatively small and $\alpha_{gm} < 1$, the receiver NF is dominated by fourth term i.e. the noise from s_5 . The NF lower limit is 4.13 dB when $R_{on,1} = 0$, $\alpha_{gm} = 1$, and $gm = +\infty$.

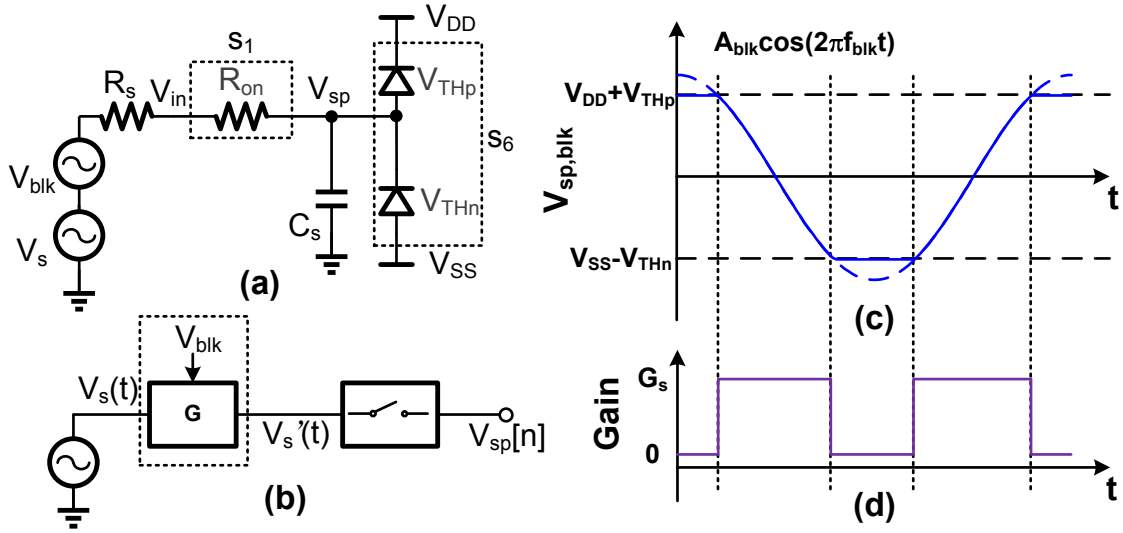


Figure 4.11: (a) Simplified sampler schematic when the input signal is sampled on C_s . (b) Sampler model with blocker. (c) Sampled blocker voltage versus time. (d) Small signal gain versus time.

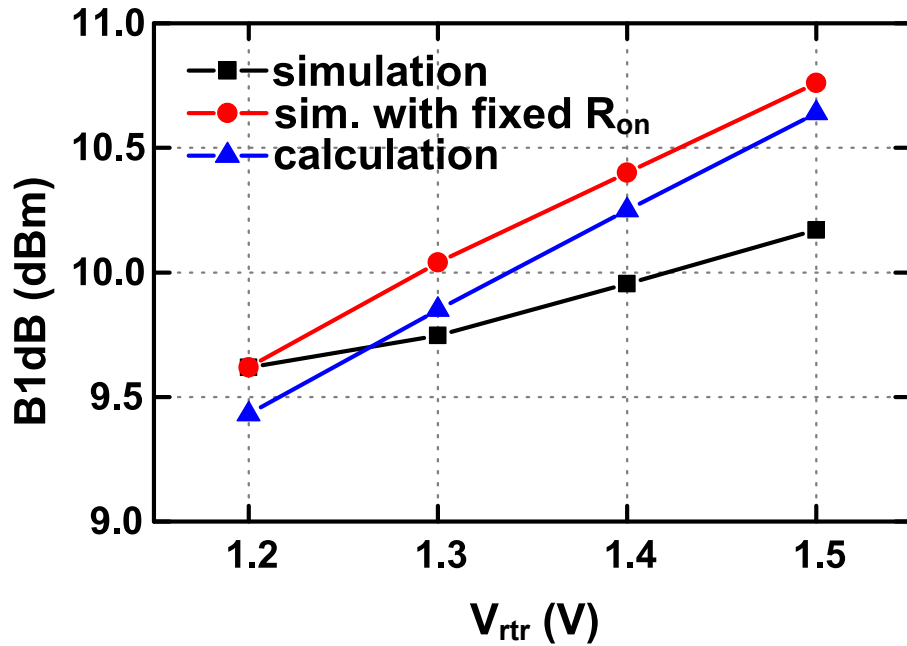


Figure 4.12: Calculated and simulated 1 dB compression point (B1dB) versus rail-to-rail voltage of the differential SCRX with a 100 MHz LO frequency and 30 MHz blocker frequency offset; real MOS transistors are used in the simulation and the input bias voltage is the midpoint of the rail-to-rail voltage.

4.2.5 Out-of-Band Blocker Linearity Analysis

The compression of the desired-signal gain due to the in-band blocker is mainly due to the nonlinear Gm cells (Fig. 4.3(a)). For an OB blocker, the Gm cells do not limit the blocker compression thanks to the SCRX's high-order filtering. The OB-blocker compression is thus limited by the sampler (Fig. 4.3(a)), which can tolerate more blocking than the Gm cells. In a SCRX without the NPF, the receiver's blocker compression approximates the compression of the sampler, which is limited by the nonlinearity of the switches. In this work, to improve blocker compression, CMOS switches (Fig. 4.10(a)) are used instead of the NMOS switches used in other blocker-tolerant receivers [26, 28, 29]. Fig. 4.10 shows the switch on and off resistance versus signal voltage. NMOS and PMOS transistors in the switch have the same size of $W/L = 150\mu\text{m}/40\text{ nm}$. $V_{SW} = V_{DD}$ and $V_{SWb} = V_{SS}$ when the switch is turned on; $V_{SW} = V_{SS}$ and $V_{SWb} = V_{DD}$ when the switch is turned off. In the simulation shown in Fig. 4.10, $V_{DD} = 1.2\text{ V}$ and $V_{SS} = 0\text{ V}$.

When the input signal is sampled on C_s (Fig. 4.6(a)), s_1 is turned on and s_6 is turned off. If s_1 is implemented by only NMOS, the R_{on} will increase with a large blocker signal (Fig. 4.10(b)), resulting in compression of the desired-signal gain. The R_{on} of the CMOS switch used in this work will not increase due to a large blocker. Thus, the R_{on} nonlinearity of s_1 will not compress the desired-signal gain. However, a large blocker will turn on s_6 , since the R_{off} of a switch decreases to tens of Ohms when the signal voltage is larger than $V_{DD} + V_{THp}$ or lower than $V_{SS} - V_{THn}$ as shown in Fig. 4.10(c), where V_{THp} and V_{THn} are the PMOS and NMOS threshold voltages, respectively. The model for the sampler in the sampling phase is shown in Fig. 4.11(a). s_1 is modeled as a resistor R_{on} , and s_6 is modeled as two ideal diodes with threshold voltage V_{THp} and V_{THn} .

Since the voltage on C_s will be clipped to $V_{DD} + V_{THp}$ and $V_{SS} - V_{THn}$ due to s_6 , the sampled blocker signal is as shown in Fig. 4.11(c). Since the desired signal will lose gain when V_{sp} is clipped (Fig. 4.11(d)), the sampler in the presence of a large blocker can be modeled as an LPTV system with a period of $T_{blk} = 1/f_{blk}$ as shown in Fig. 4.11(b). Assuming the NMOS and PMOS threshold voltages are the same ($V_{THp} = V_{THn} = V_{TH}$) and the input is biased at the midpoint of the rail-to-rail voltage ($V_{bias} = (V_{DD} + V_{SS})/2$), the desired-signal gain versus time is

$$G(t) = \begin{cases} G_s & |A_{blk} \cos(2\pi f_{blk} t)| \leq V_{RTR}/2 + V_{TH} \\ 0 & |A_{blk} \cos(2\pi f_{blk} t)| > V_{RTR}/2 + V_{TH}, \end{cases} \quad (4.17)$$

where G_s is the signal gain without the blocker and $V_{RTR} = V_{DD} - V_{SS}$ is the rail-to-rail voltage.

The desired signal gain without frequency shifting can be derived as [67]

$$G_{s,blk} = \frac{1}{T_{blk}} \int_0^{T_{blk}} G(t) dt = \frac{G_s}{\pi} \left(\pi - 2 \arccos \left(\frac{V_{RTR}/2 + V_{TH}}{A_{blk}} \right) \right). \quad (4.18)$$

The blocker amplitude resulting in a gain compression of 1 dB is

$$A_{blk,1dB} = \frac{V_{RTR}/2 + V_{TH}}{\cos(\pi/2 \cdot (1 - G_{s,blk}/G_s))} \approx 1.015(V_{RTR}/2 + V_{TH}). \quad (4.19)$$

For a differential SCRX without the NPF, considering 3 dB loss of the single-ended-to-differential converter and a $G_{blk} + 6$ dB blocker-signal gain of the sampler, the blocker B1dB is

$$B1dB_{woNPF} = 20 \log(1.015(V_{RTR}/2 + V_{TH})) + 10 - (G_{blk} + 6) + 3 \text{ (dBm)}, \quad (4.20)$$

where G_{blk} is around -2.2 dB as the desired-signal gain since compared with LO frequency, the blocker frequency offset is small. The B1dB depends mainly on the rail-to-rail voltage and the threshold voltage of the transistor.

Fig. 4.12 shows the calculated and simulated B1dB versus V_{RTR} of a differential SCRX without an NPF. For the calculation, transistor threshold voltage V_{TH} in (4.20) is set to 0.4 V. In the simulation, ideal Gm cells are used to show the B1dB of transistor-level SC circuits only. The LO frequency is 100 MHz and blocker frequency offset is 30 MHz. The simulated B1dB increases slightly less with V_{RTR} than the calculated value since the R_{on} is smaller when V_{RTR} increases, which increases the G_s . If we keep R_{on} fixed by fixing the V_{RTR} of the turn-on mode to 1.2 V, the simulated B1dB matches the calculation very well (second curve in Fig. 4.12).

4.2.6 Switched-Capacitor Front End with N-path filter

The NPF (Fig. 4.3(a)) has been extensively analyzed in [23, 24, 26, 68]. Its frequency-translation mechanism shifts the baseband low-pass impedance to the LO frequency resulting in a band-pass impedance. An OB blocker can be reduced at the RF input by the low OB NPF impedance. The NPF in this work can be turned off by disabling s_0 . With the NPF, the NF increases due to the filter insertion loss at the RF input. The behavioral-level simulated conversion gain and NF are shown in Fig. 4.21. The conversion gain and NF both degrade by 0.7 dB due to the NPF. The B1dB improves thanks to the OB attenuation before the sampler. Theoretically, the maximum B1dB improvement due to NPF is $(2R_{\text{on}} + R_s)/2R_{\text{on}}$, which is around 7 dB for $20\ \Omega$ switches.

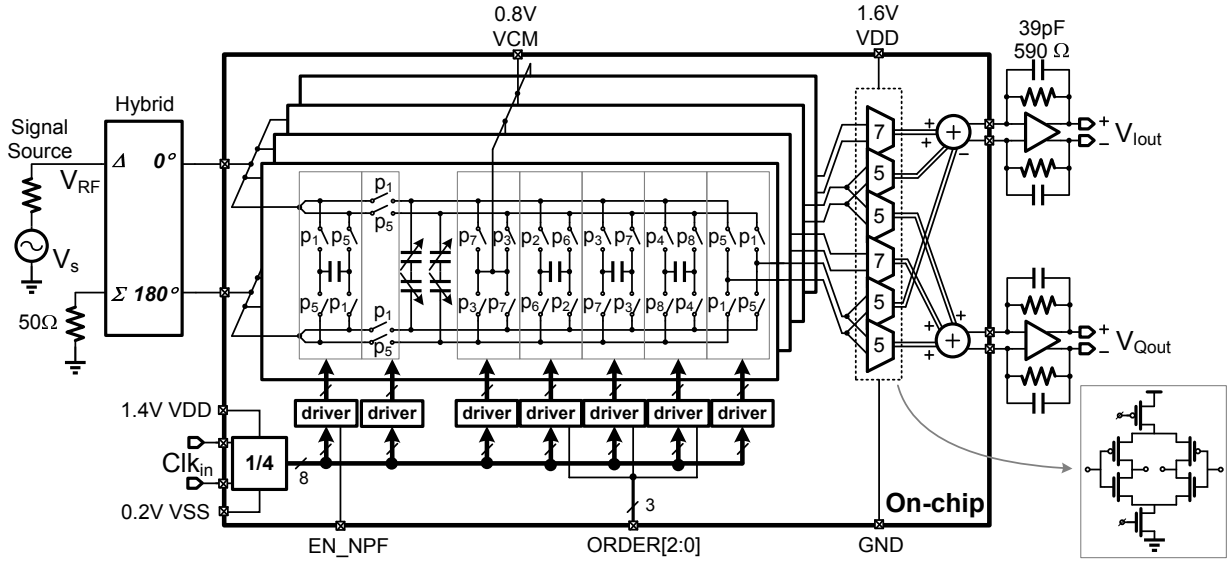


Figure 4.13: Schematic of the switched-capacitor RF receiver.

4.3 Implementation of the RF Front End

The schematic of the RF receiver prototype is shown in Fig. 4.13. It consists of the SC circuits, the baseband Gm cells, TIAs, and a clock generator. In the fully differential architecture, a differential NPF [23] is used at the RF input and the two C_s capacitors with opposite phases share the same C_h in the IIR filter to eliminate the DC and even-order LO harmonic responses. The corresponding two banks in Fig. 4.3(a) are merged into one bank in Fig. 4.13; as a result, we need eight capacitors for C_s and four capacitors for each C_h . The NMOS and PMOS in the CMOS switches are sized equally to reduce the charge injection and clock feedthrough. The R_{on} of the sampling switches s_1 and the output switches s_5 is $14\ \Omega$, while the other switches are sized for $20\ \Omega$. The C_s is implemented with a metal-oxide-metal (MoM) capacitor bank with switches to ground. The C_s tuning range is 1–16 pF with a 1 pF step. The C_h s are identical with an effective single-ended capacitance of 50 pF and are realized with a combination of differential MoM capacitors and MOS capacitors to ground.

The Gm cells combine the four-phase output signals from the SC circuits; each two C_s s with opposite phases share a single Gm cell which changes the hold time to $4T_s$ when converting the DT signal to CT. The Gm cells are realized by CMOS inverters with a tail current (Fig. 4.13) operating from a 1.6 V supply. The Gm input-common-mode voltage is set by V_{CM} in the reset phase. Common-mode feedback circuits set the output common-mode voltage to 0.8 V. A 5:7 size ratio is used to approximate the $1 : \sqrt{2}$ ratio for the harmonic recombination to eliminate the harmonic down-conversion. Dummy Gms are used to balance the load of the previous stage. The transconductance of the size-5 Gm cell is 40 mS. To reduce the flicker noise, a large transistor is used with $l=1\ \mu\text{m}$, resulting in 40 pF input-parasitic capacitance. Since the desired signal is already down-converted at the Gm input, this parasitic capacitor will not limit the receiver's frequency range. Each Gm cell can be tuned with a nine-bit control code to calibrate the harmonic rejection ratio (HRR) as in [36]. During the calibration, a harmonic signal is provided at the RF input and the Gm cells are externally tuned to minimize the baseband output power. This calibration cannot achieve high HRR for 3rd and 5th order LO harmonics simultaneously as explained in [36].

The clock divider generates eight nonoverlapping clock signals with a 1/8 duty cycle and drives the switch drivers. The drivers for the switches in the NPF and IIR filter can be turned on or off to change the filter order. The switch drivers are DC coupled to the switches. Since the receiver's V_{CM} is 0.8 V, and the rail-to-rail voltage is 1.2 V, the V_{DD} and V_{SS} of the clock generator are chosen to be 1.4 V and 0.2 V respectively to make sure $V_{CM} = (V_{DD} - V_{SS})/2$. Fig. 4.14(a) shows the block diagram of the clock divider. The latch-based counter generates an 8-phase 1/2-duty-cycle clock signal $X\langle 7:0 \rangle$. The latch output signals are combined by an array of AND gates to

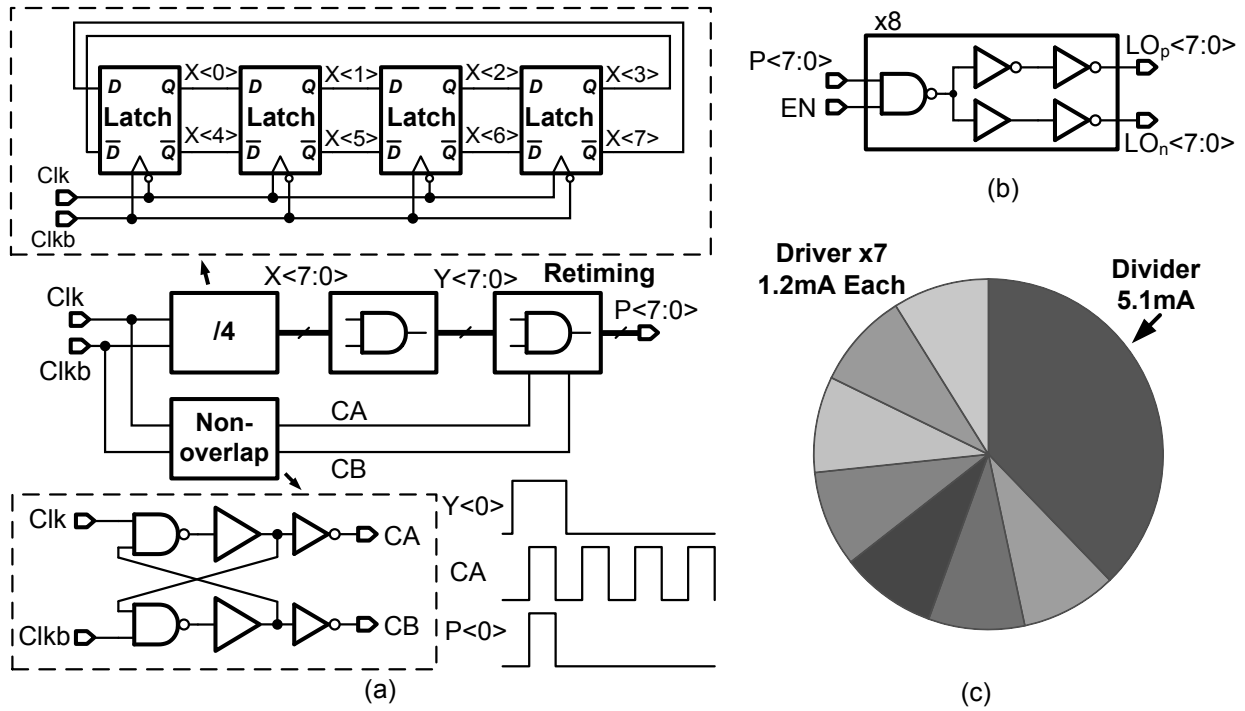


Figure 4.14: (a) Block diagram of (a) the clock divider and (b) the clock driver circuits. (c) Current consumption breakdown of the clock generator for a 0.2 GHz LO frequency.

generate a 1/4-duty-cycle clock $Y\langle 7:0 \rangle$ for the retiming circuit. After retiming by the 2-phase non-overlapping clocks CA and CB, the 8-phase 1/8-duty-cycle nonoverlapping clock $P\langle 7:0 \rangle$ is generated. The retiming scheme relaxes the noise requirements of the counter and the AND-gate array. The complementary clocks for CMOS switches are generated by clock drivers and can be enabled with the signal EN as shown in Fig. 4.14(b). LO_p and LO_n drive the PMOS and NMOS in the switch respectively. The digital buffer in the LO_n branch is used to equalize the delay of LO_p and LO_n , and the delay mismatch needs to be smaller than the gap between two non-overlapping clocks. The current consumption breakdown of the clock generator is shown in Fig. 4.14(c). For a 0.2 GHz LO frequency, the clock divider consumes 5.1 mA, while each clock driver consumes 1.2 mA, resulting in a total current of 13.5 mA when all the drivers are turned on.

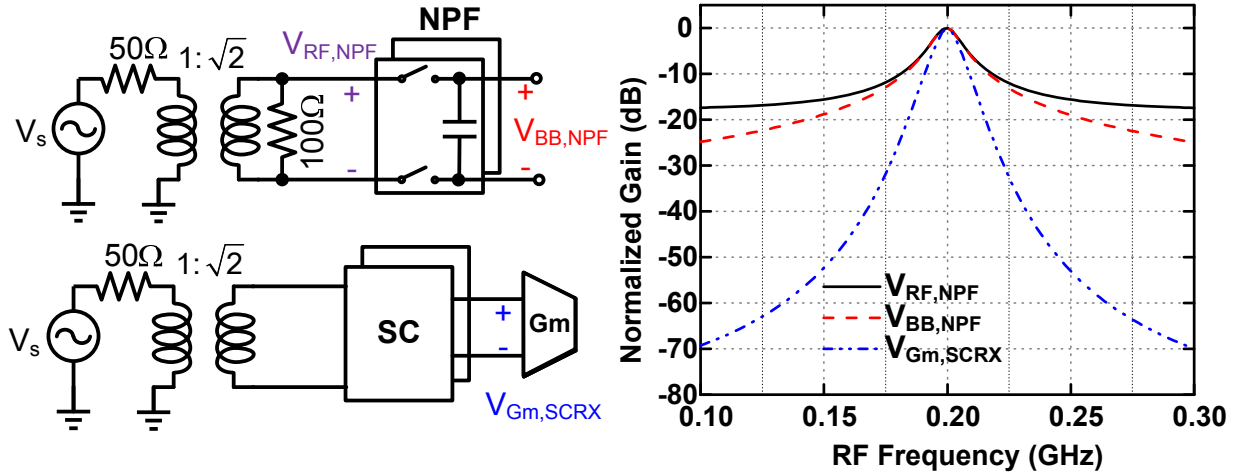


Figure 4.15: Transistor-level simulation of the gain/conversion gain at node $V_{RF,NPF}$, $V_{BB,NPF}$, $V_{Gm,SCRX}$ for a 0.2GHz LO frequency. All the transfer curves are normalized for equal in-band gain of 0 dB. $V_{RF,NPF}$, $V_{BB,NPF}$, and $V_{Gm,SCRX}$ are the nodes before non-linear active circuits in RF NPF, mixer-first receiver, and the proposed SCRX respectively as shown in Fig. 4.1(b)(c)(d).

Fig. 4.15 shows the transistor-level simulated gain or conversion gain of the proposed SCRX and a conventional NPF with the same total switch size ($R_{on} = 2.5\Omega$) and a same total history capacitance of 240 pF including the Gm input parasitic capacitance $C_{h,gm}$. The power consumption of the clock generator in the SCRX and in the NPF should be the same given they have the same total switch size. For the NPF, the OB attenuation at the RF input is limited by the finite R_{on} , and the attenuation at baseband is limited by the low-order filtering. In the proposed SCRX, when all of the filters are turned on, the SC circuits provide a 70 dB blocker attenuation at a 100 MHz frequency offset before the Gm cell which is 45 dB better than the NPF.

The calculated conversion gain ($V_{Iout}/(V_s/2)$) and DSB noise figure using the differential version of (4.7) and (4.15) are shown in Fig. 4.21 and match the behavioral-level simulation results. With NPF, the gain and NF degrade by 0.7 dB but don't change with LO frequency. In the transistor-level simulations, the gain is 41.3 dB, and the NF is 7 dB for a 0.1 Gz LO and both de-

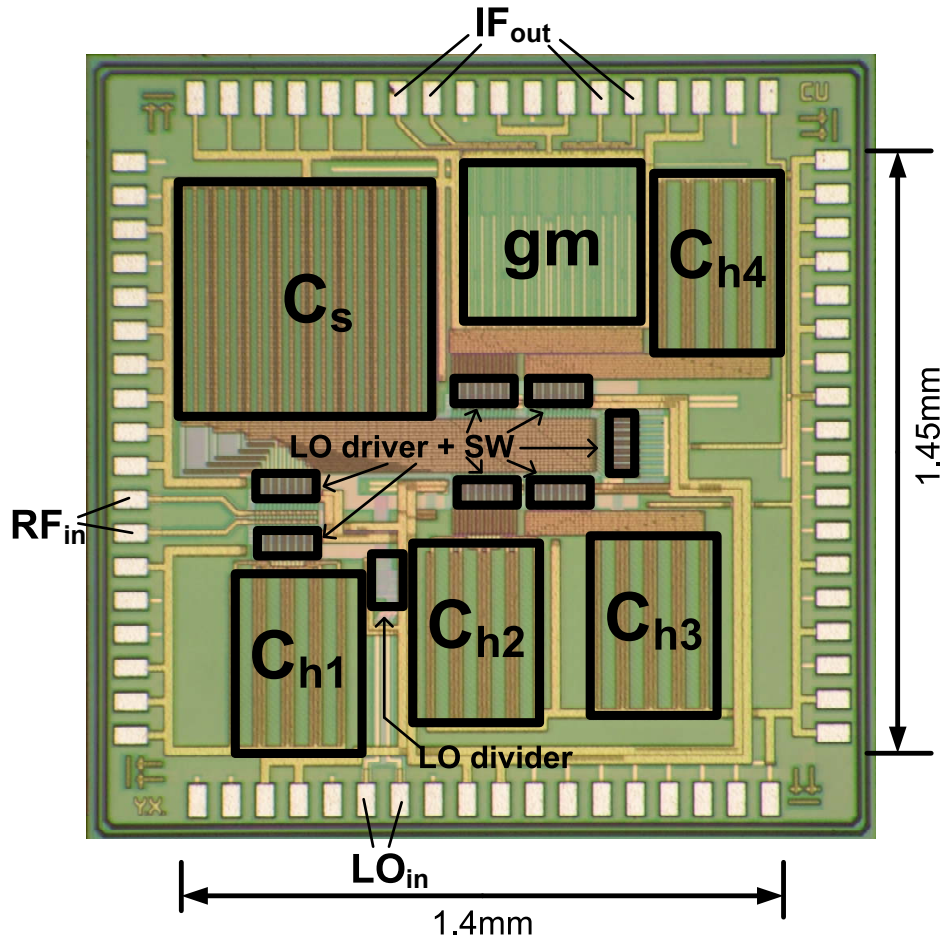


Figure 4.16: Chip photo.

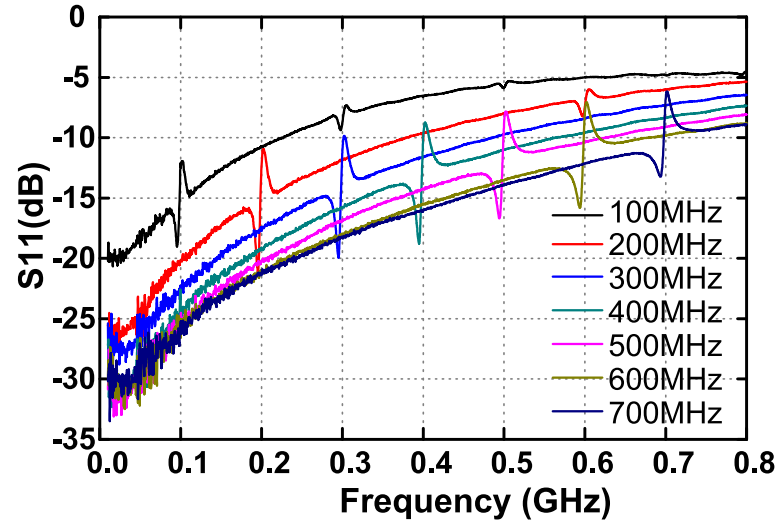
grade with LO frequency since the switches and routing have parasitic capacitance and the clock signals with a fixed rise/fall time and a fixed gap between the non-overlapping phases reduce the switch-turn-on-time to clock-cycle ratio at high LO frequencies. The gain and NF also degrade in the behavioral-level simulation (Fig. 4.21) when the parasitic capacitance and non-ideal clock are included.

4.4 Measurement Results

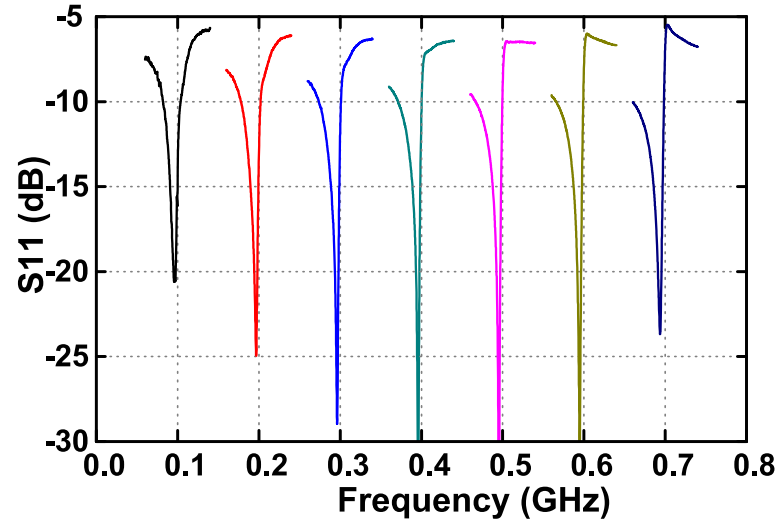
The chip prototype was fabricated in a 40 nm LP CMOS process and the active area is $1.4 \times 1.45 \text{ mm}^2$ (Fig. 4.16). Around 40% of chip area is occupied by MoM capacitors. The C_s value is set by the impedance matching requirements, and C_h value is set by the IF bandwidth requirements as discussed in section 4.2. The availability of higher capacitance density would directly reduce the chip size. In the measurements, an off-chip 180° hybrid drives the differential RF inputs as shown in Fig. 4.13 and the hybrid loss was calibrated out for all measurements.

The differential S_{11} s for LOs from 0.1 to 0.7 GHz are calculated from the measured two-port S parameters of the differential RF inputs. Fig. 4.17(a) shows the S_{11} of the receiver with third-order IIR filtering without the NPF. Wideband impedance matching is achieved; the bandwidth of S_{11} scales with the LO frequency. The wiggle around the LO frequency is caused by the finite switch resistance of s_6 (Fig. 4.4) as discussed in Section 4.2. The S_{11} of the receiver with the NPF is shown in Fig. 4.17(b). The OB S_{11} is higher due to the low OB impedance of the NPF. The slight deviation of the S_{11} notch and the LO frequency is caused by parasitic capacitance at the RF input [26]. The measured LO leakage to the RF input is less than -60 dBm across LO frequencies.

The conversion gain $V_{\text{Iout}}/(V_s/2)$ from the RF input to the TIA output with different filter configurations is measured for an LO frequency of 0.2 GHz in Fig. 4.18. The roll-off increases with higher filter order. The bandwidth changes from 4.8 to 3.2 MHz when the filter order increases. In Fig. 4.19 the B1dB versus blocker offset frequency is measured for a 0.2 GHz LO frequency and an in-band signal of 201 MHz. The blocker tolerance increases with filter order. The maximum B1dB without the NPF is limited to 10 dBm since the C_s voltage is clipped due to limited rail-to-rail

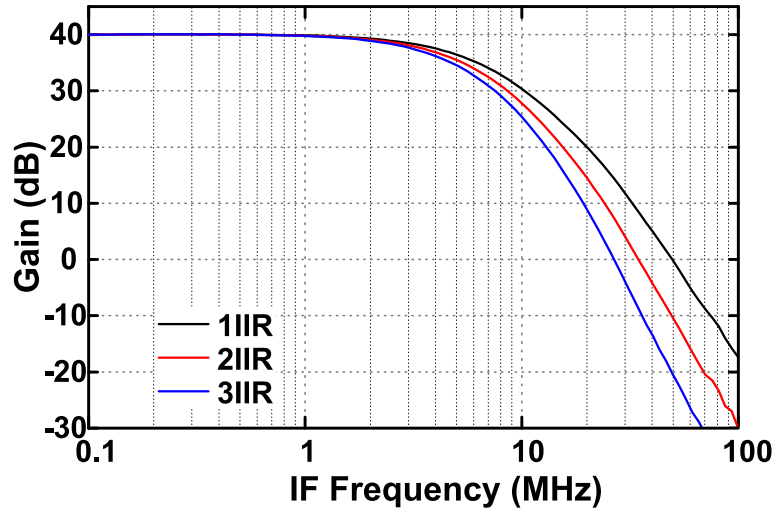


(a)

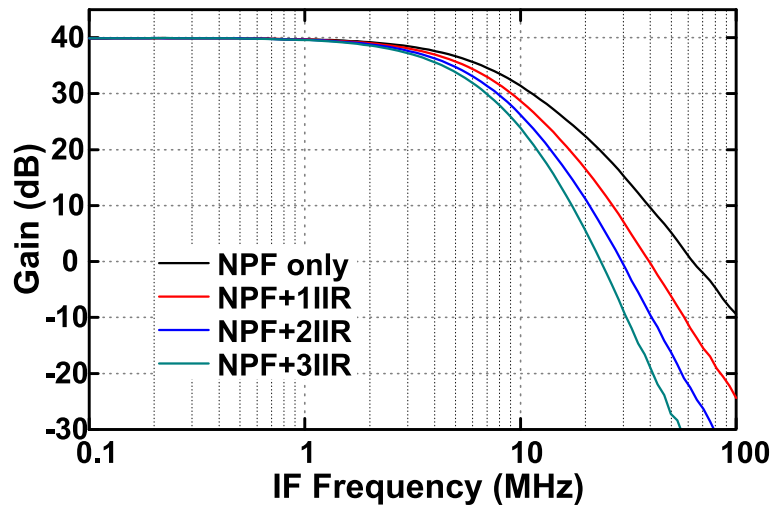


(b)

Figure 4.17: Measured differential-mode S_{11} for LO frequencies ranging from 0.1 to 0.7 GHz with a 0.1 GHz step: (a) S_{11} without the N-path filter; (b) S_{11} with the N-path filter.



(a)



(b)

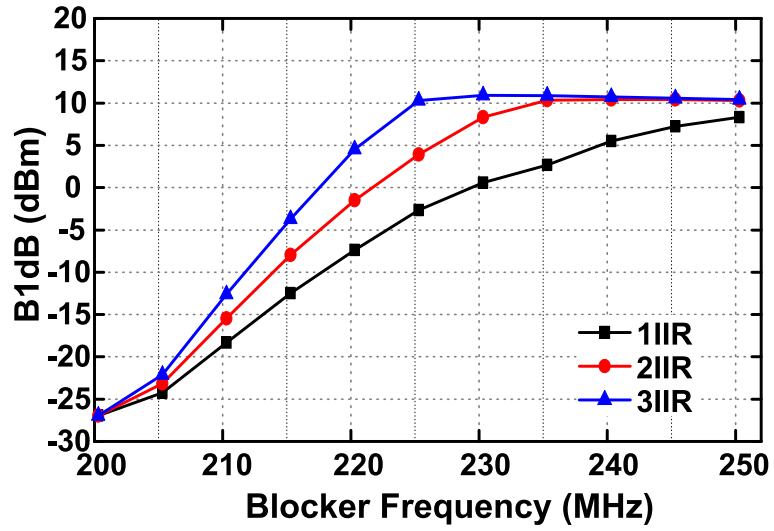
Figure 4.18: Measured conversion gain $V_{\text{Iout}}/V_{\text{RF}}$ with different filter configurations for an LO frequency of 0.2 GHz: (a) Conversion gain without the N-path filter; (b) Conversion gain with the N-path filter.

voltage as discussed in Section 4.2. With the NPF, the maximum B1dB is improved by 5 dB since the blocker is attenuated by the NPF before the sampler. With a third-order IIR filter and an NPF, the B1dB is as high as 14.7 dBm at a 30 MHz frequency offset. The OB third-order input intercept point (OB-IIP3) with the NPF and third-order IIR filter is 24 dBm with a LO frequency of 0.2 GHz and the two tones at 0.231 and 0.261 GHz.

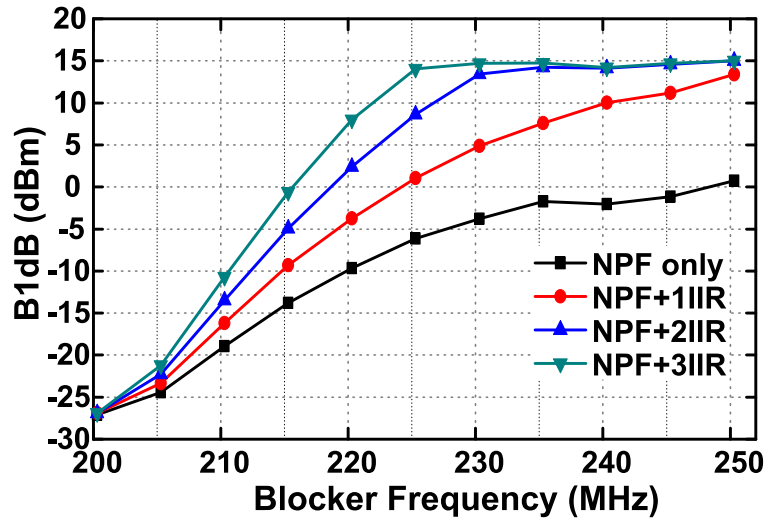
Fig. 4.20 shows the B1dB at a 30 MHz frequency offset, the NF and the LO current consumption for different IIR filter orders. With higher order filtering, the B1dB improves at the cost of a higher LO current, while the NF only increases by 0.2 dB. For a given IIR filter order, the NPF improves the B1dB but requires a larger LO current; the NF increases less than 0.2 dB due to the NPF's loss.

The measured gain, NF, B1dB and OB-IIP3 of the receiver with the NPF and third-order IIR filter versus LO frequency are shown in Fig. 4.21, which matches the transistor-level simulation results. The gain is 41 dB at 0.1 GHz and 38 dB at 0.7 GHz. The NF of the whole receiver is 6.8 dB at 0.1 GHz which is higher than the NF lower limit in Section 4.2 due to finite R_{on} , noisy Gm cells, and NPF's loss. The NF increases to 9.7 dB at 0.7 GHz due to the parasitic capacitance and non-ideal clock. The B1dB and OB-IIP3 change less than 2.5 dB and 4.5 dB respectively for the 0.1 to 0.7 GHz frequency range.

The B1dB versus relative blocker frequency offset is compared with other blocker-tolerant RF receivers [26, 29, 35] in Fig. 4.22. To normalize the comparison (frequency offset)/IFBW is used as the x-axis. For [26], the bandwidth of a single sideband is used since it is a RF bandpass filter.



(a)



(b)

Figure 4.19: Measured B1dB versus blocker frequency for an LO frequency of 0.2 GHz: (a) B1dB without the N-path filter; (b) B1dB with the N-path filter.

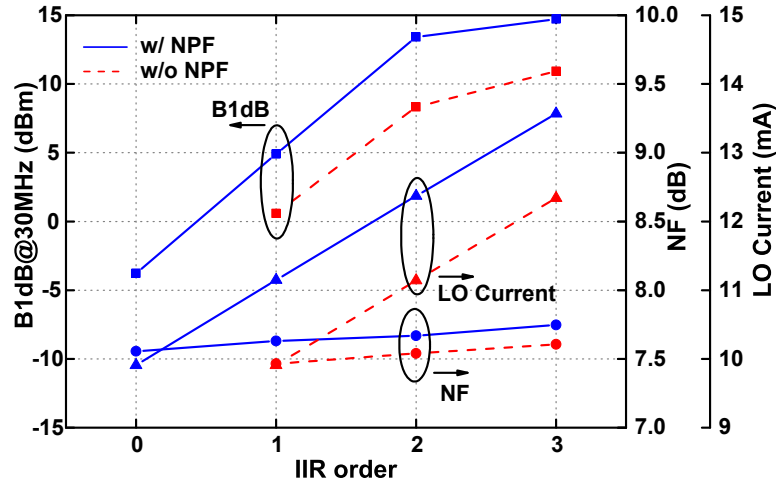


Figure 4.20: Measured B1dB at a 30 MHz frequency offset, noise figure, LO current consumption versus filter order for a LO frequency of 0.2 GHz.

With large blocker attenuation, this work achieves a higher maximum B1dB while the slope is also larger than in other work thanks to the high-order filtering.

Fig. 4.23 shows the measured NF versus blocker power with a 0.13GHz continuous-wave blocker for a 0.1GHz LO. In general, the NF increases due to gain compression or reciprocal mixing. Since in this work the gain compression is low given the +15dBm B1dB, the NF degradation is probably mainly caused by reciprocal mixing; in future work this can be improved with a low phase noise LO generator as discussed in [29].

The performance summary and comparison with the state of the art is shown in Table. 4.1. This work has higher-order filtering before active circuits and achieves the highest B1dB. The OB-IIP3 is as high as that of other work since the high-order filtering improves the large-blocker tolerance more than it improves the small-signal nonlinearity. The calibrated HR3 and HR5 are better than 66 and 73 dB, respectively, but they cannot be achieved with the same calibration code as explained in [36]. A moderate noise figure is achieved. However, if we add an appropriate resistive attenuator

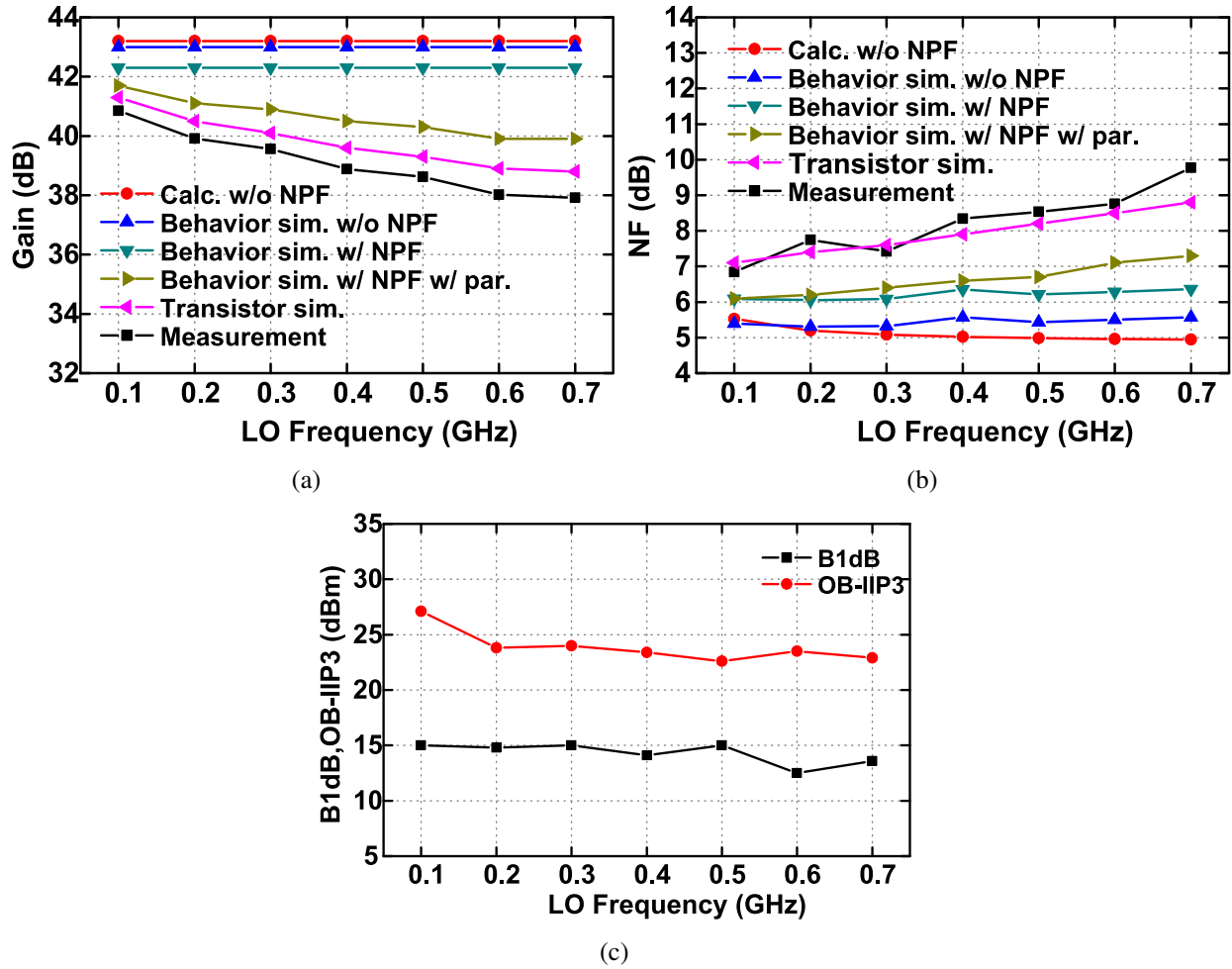


Figure 4.21: The (a) conversion gain $V_{\text{Iout}}/(V_s/2)$, (b) NF, and (c) B1dB and OB-IIP3 across LO frequency; in all cases 3rd-order IIR filtering is used; results are shown for calculations using the differential version of (4.7) and (4.15), behavioral-level simulations (without NPF; with NPF, with and without the parasitic capacitance and non-ideal clock), transistor-level simulations with NPF, and measurements with NPF.

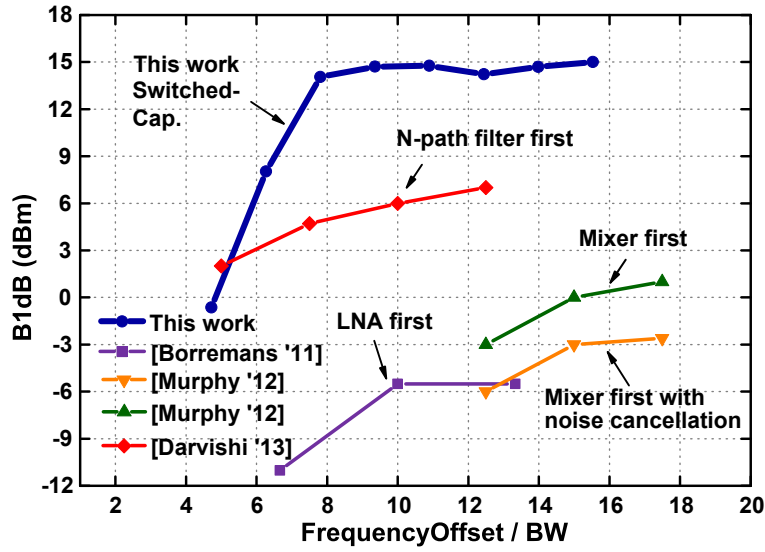


Figure 4.22: Comparison with other blocker-tolerant RF receivers of their B1dB versus relative blocker frequency offset.

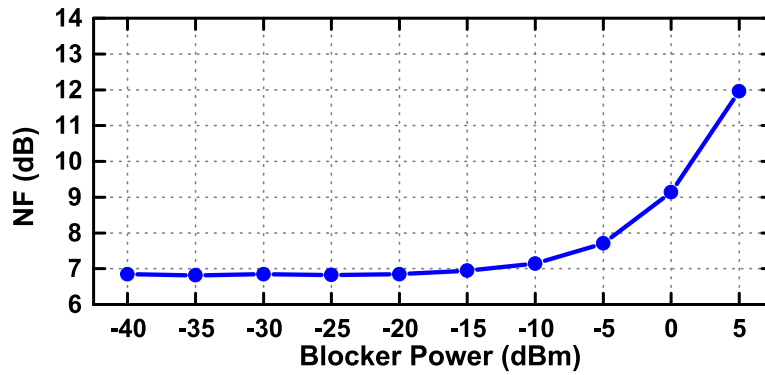


Figure 4.23: Measured noise figure versus blocker power with a 0.13GHz continuous-wave blocker for a LO frequency of 0.1GHz.

Table 4.1: Comparison with the state of the art

	This work	Borremans JSSC '11	Andrews JSSC '10	Mahrof JSSC '14	Murphy JSSC '12	Darvishi JSSC '13	Chen JSSC '14
Technology	40nm	40nm	65nm	65nm	40nm	65nm	65nm
Architecture	Switched-Cap.	LNA+NPF	Mixer first	Mixer first	FTNC	NPF	DT RX
Filter order before active circuits	1-4	0	1	1	1	1	NA
RF input frequency range (GHz)	0.1-0.7	0.4-6	0.1-2.4	0.2-2.6	0.08-2.7	0.1-1.2	0.5-3
Gain (dB)	40	70	70	26.5	72	25	35
Output BW (MHz)	3.2-4.8	0.4-30	<20	12	2	4 ²	10.5- 63.5 ³
NF (dB)	6.8-9.7	3-7	3-5	7.5	1.5-2.4 ¹ , 3.5-5	2.8	6.8-13.2
OB-IIP3 (dBm)	24@30MHz	10	25 @20MHz	18 @>450MHz	13@20MHz ¹ 17@20MHz	26 @50MHz	>11
Max. B1dB (dBm)	15	<-5	<6	NR	<0 ¹ , <5	7	-1
HR3/5 (dB)	>38/>35 >66/>73 (cal.)	NR	35.5/42.6	NR	>42/>45	NA	>46/>51
Power (mW)	Ana : 52(32.5mA) LO: 7-53 (6-44mA)	30-55	30-70	13.9	35-78	18-57.4	211-540 ⁴
Area(mm ²)	2.03	2	0.75	0.2	1.2	0.27	5.9
<i>Adding a resistive attenuator before the RXs to normalize all B1dB to 15dBm</i>							
Attenuation (dB)	0	20	9	NA	15 ¹ , 10	8	16
NF with normalized B1dB(dB)	6.8-9.7	23-27	12-12	NA	16.5-17.4 ¹ , 13.5-15	10.8	22.8-29.2

1. with noise cancellation 2. single side band 3. Bandwidth of DT RF signal processor, BW is proportional to LO frequency

4. without clock synthesizer and regulator 5. including pad frame

NA: not available, NR: not reported.

before the other receivers so that they achieve a B1dB of 15 dBm, the noise figure performance of the presented approach is excellent under these normalized operating conditions.

4.5 Conclusions

In this chapter, a switched-capacitor RF receiver with high-order embedded RF filtering is presented. A 0.1–0.7 GHz receiver prototype achieves as high as fourth-order filtering before the non-linear active baseband circuits. The HRR is higher than 66 dB with calibration. Thanks to the high-order passive SC RF filtering, the B1dB is as high as 14.7 dBm for a blocker offset as small as 30 MHz with only a moderate NF penalty.

The key drawback of the SC receiver is the noise performance is limited by the SC circuit and cannot be improved with better process. In the following chapters, several techniques are investigated to improve the noise performance.

4.6 Appendix

Using the same LPTV analysis as in [73, 74], the sampler (C_s with s_1 and s_6 in Fig. 4.4(a)) can be analyzed as follows. First, in one time interval, the V_s propagates to V_{in} (Fig. 4.4(a)) with a response of

$$\frac{d}{dt}V_{in}(t) = -\frac{1}{R_s C_s}V_{in}(t) + \frac{1}{R_s C_s}V_s(t), nT_s \leq t < (n+1)T_s. \quad (4.21)$$

Using (70) and (71) in [74], and considering there is only one time interval in the SC circuit with zero initial conditions, the response is

$$\frac{d}{dt}V_{in}(t) = -2\pi f_{rc}V_{in}(t) + 2\pi f_{rc}V_s(t) + \sum_{n=-\infty}^{\infty} [-V_{in}(t)\delta(t - (n+1)T_s)], \quad -\infty < t < \infty, \quad (4.22)$$

where $f_{rc} = 1/2\pi R_s C_s$, and $\delta(\cdot)$ is the Dirac function. The spectrum of input voltage is a combination of the frequency-shifted source signal as in (4.1) in Section 4.2. Using (77) and (78) in [74] and (4.22), the frequency domain transfer function is

$$H_n(f) = \frac{1}{j2\pi f + 2\pi f_{rc}} [2\pi f_{rc} - f_s G(f - nf_s)], \quad (4.23)$$

where $G(f)$ is a function that makes the voltage at switching moment $t = nT_s$ satisfy

$$\sum_{n=-\infty}^{\infty} \mathcal{F}(V_{in}(t)\delta(t - nT_s)) = \sum_{n=-\infty}^{\infty} [G(f) \cdot \mathcal{F}(V_s(t))] * \delta(f - nf_s) \cdot f_s. \quad (4.24)$$

We now calculate $G(f)$. In one time interval, the final condition with a sinusoidal source voltage ($V_s = \exp(j2\pi ft)$) and zero initial condition can be derived from (82) in [74]:

$$V_{in}((n+1)T_s) = \frac{1}{1 + jf/f_{rc}} \left[e^{j2\pi fT_s} - e^{-2\pi f_{rc}T_s} \right] e^{2\pi fnT_s}. \quad (4.25)$$

Since $V_{in}(nT_s) = G(f) \exp(2\pi fnT_s)$ and $f_s = 1/T_s$, $G(f)$ can be expressed as (4.6) in Section 4.2.

The $V_{in}(nT_s)$ is the final condition of one time interval which is the sampled voltage $V_{sp}[n]$ (Fig. 4.4(a)). The sampler can thus be modeled as an ideal sampler with $G(f)$ as shown in Fig. 4.4(b).

Using (4.6) and (4.23), the transfer function from the source voltage to the input node can be expressed as (4.2) in Section 4.2.

Chapter 5

Chopping Switched-Capacitor Receiver with Integrated Blocker Detection

5.1 Introduction

The switched-capacitor receiver (SCRX) presented in Chapter 4 uses SC circuits to realize high-order and high-linearity filtering to achieve high OB linearity even for a close-by blocker. The drawback of the SCRX is its relatively high noise figure (NF) and need for large-area baseband transconductors (Gms) to reduce RX in-channel flicker noise. In this chapter, a chopping SC receiver with integrated blocker detector (Fig. 5.1) is presented. It achieves input impedance matching, programmable high-order filtering, and mixing similar to the SCRX in Chapter 4. The RF SC front end has been modified to improve noise performance. A chopping technique is merged into the SC circuits to reduce the transconductor's (Gm) size and flicker noise. We use inverter-based

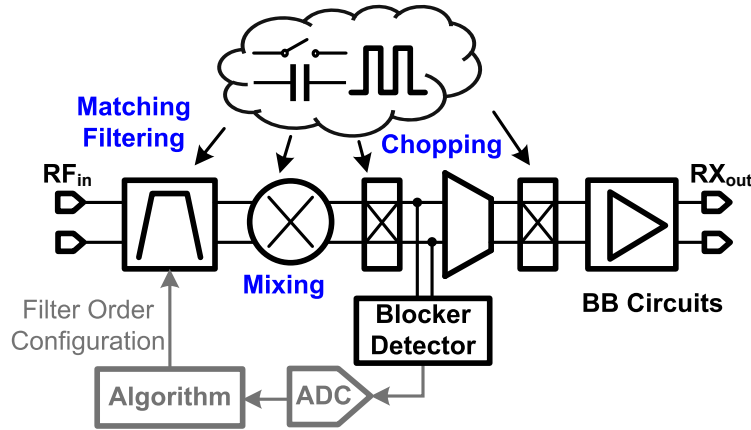


Figure 5.1: Proposed chopping switched-capacitor RF receiver with blocker detection.

Gm cells to reduce the supply voltage, and minimum-channel-length transistors to reduce Gm size. A blocker detector is integrated with the SC receiver to detect the OB RF blocker envelope with a short response time before the blocker is propagated to the Gm cells. The filter order can be increased with a feedback loop when a large blocker is detected to make the filter order adapt to the blocker power.

The chopping SC RF receiver is described in Section 5.2. Section 5.3 describes the blocker detection. The front-end architecture and circuit implementation are presented in Section 5.4. Measurement results are provided in Section 5.5, and Section 5.6 presents our conclusions.

5.2 Chopping Switched-Capacitor RF Receiver Design

The linear, passive SC RF circuit located in front of the receiver active baseband circuits provides high OB blocker tolerance, but receiver noise performance is limited by the switches. In this

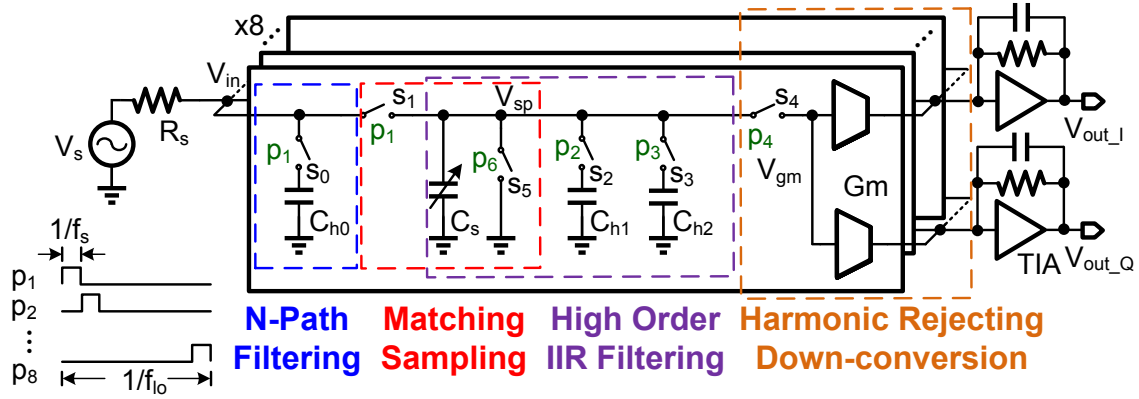


Figure 5.2: Simplified architecture of the switched-capacitor receiver.

chapter, a modified SCR_X is developed to improve noise performance. The chopping technique is incorporated into the modified SC receiver to solve the flicker noise problem [77].

5.2.1 Switched-Capacitor Receiver

Fig. 5.2 shows the simplified architecture of our earlier SCR_X with eight time-interleaved SC banks [5]. At the RF input, the NPF creates a bandpass input impedance to reduce the OB blocker, and the RF signal is sampled on C_s by s_1 with a sampling frequency of f_s . The input impedance matching is achieved by discharging the sampling capacitor C_s through switch s_5 . The high-order passive discrete time (DT) IIR filter [57] further attenuates the OB blocker before it propagates to the baseband G_m input. Each SC branch (e.g. C_{h1} with s_2) provides an additional order of filtering. Filter order programmability is realized by enabling and disabling the switches attached to the history capacitors C_{hi} . The G_m cells amplify the baseband signal and their transconductances are scaled in different banks to achieve harmonic rejecting down-conversion as in a harmonic rejection

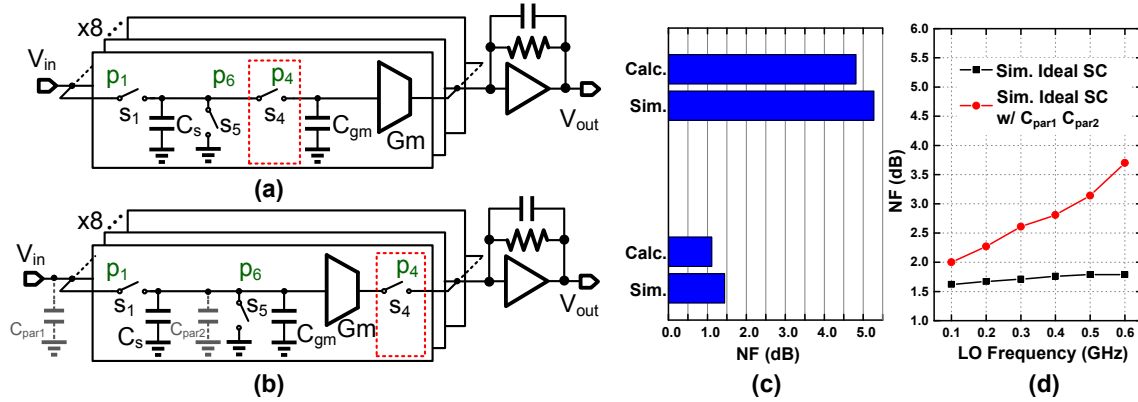


Figure 5.3: (a) Switched-capacitor RF receiver without filtering [5]. (b) Proposed approach to improve the noise figure by relocating output switch s_4 after the baseband transconductor G_m . (c) Calculated and behavioral-level simulated noise figure of both architectures. (d) Simulated noise figure versus LO frequency.

mixer [78]. The desired signal is located at the receiver LO frequency $f_{LO} = f_s/8$. The analysis of the SC receiver is described in [5].

5.2.2 Improving Noise Performance of the Passive Switched-Capacitor RF

Front End

Fig. 5.3(a) illustrates an SC RF receiver without filtering. To achieve RF input impedance matching to an RF source with impedance R_s at a sampling frequency f_s , the capacitance of C_s needs to be $C_s \approx 0.63/f_s R_s$. The noise factor F of the passive SC RF circuit is then

$$F = 1 + \frac{R_{on,1}}{R_s} + \frac{1}{2R_s |G(f_s/8)|^2} \left[\frac{e^{-1/f_s R_s C_s}}{f_s C_s} + \frac{1}{\alpha_{gm} f_s C_s} \right], \quad (5.1)$$

where $R_{on,1}$ is the on-resistance of switch s_1 , $\alpha_{gm} = C_{gm}/(C_{gm} + C_s)$, C_{gm} is the G_m input parasitic capacitance; $G(f)$ is the equivalent continuous-time (CT) transfer function before the CT signal is

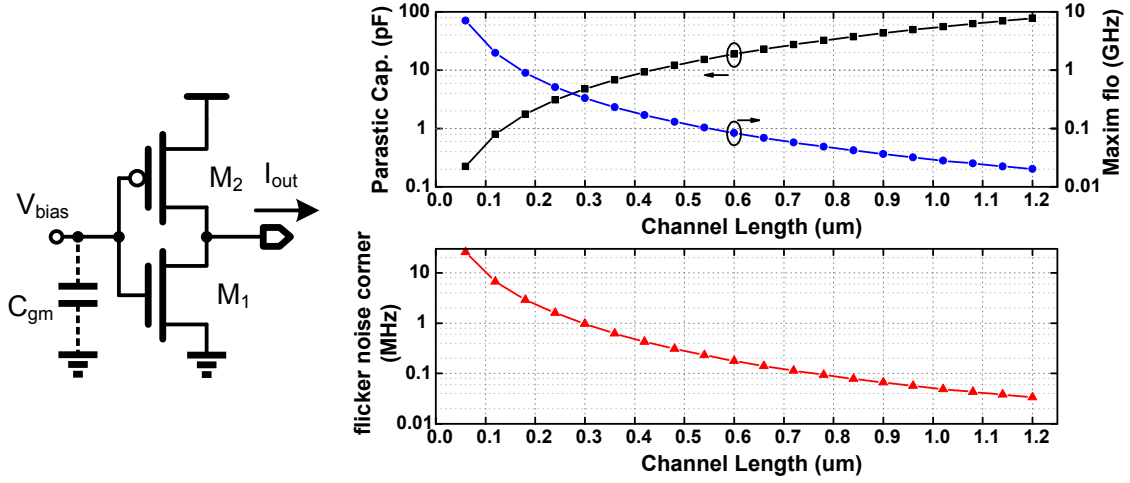


Figure 5.4: Simulated Gm parasitic capacitance, flicker-noise corner, and maximum f_{LO} of the switched-capacitor receiver versus transistor length for a 100 mS inverter-based Gm in 65 nm CMOS.

sampled by the sampler (C_s with s_1 and s_5):

$$G(f) = \frac{1}{1 + jf/f_{rc}} \cdot \left[1 - e^{-2\pi(f_{rc} + jf)/f_s} \right], \quad (5.2)$$

with $f_{rc} = 1/(2\pi R_s C_s)$. Using the RF input matching condition, the noise factor can be simplified to $F = 1 + R_{on,1}/R_s + 0.27 + 1.32/\alpha_{gm}$. The second, third, and fourth terms in the noise factor formula are caused by switches s_1 , s_5 , and s_4 respectively. The noise from s_1 can be reduced using switches with smaller R_{on} ; the noise from the IIR filter can be ignored [5, 57]; and the noise from Gm and other baseband circuits can be suppressed by using large transconductances. Output switch s_4 is the dominant noise source that limits noise performance and should be removed to improve the noise factor.

Moving switch s_4 to the Gm output (Fig. 5.3(b)) improves the SC receiver's noise performance. The noise from s_4 is suppressed by the Gm as in a conventional passive mixer [79]. Ignoring the

Gm noise, the noise factor of the modified SC receiver is $F = 1 + R_{on,1}/R_s + 0.27$. Fig. 5.3(c) shows the calculated and behavioral-level simulated noise figure (NF) of the conventional and modified SC receivers for a $1\ \Omega$ switch R_{on} . The Gm noise is ignored. By relocating s_4 , the NF is improved by 3.8 dB with the theoretical lower limit of the NF at 1 dB. In real circuits the NF will be higher than the lower limit due to non-idealities such as the non-zero switch R_{on} , clock non-ideality, and the parasitic capacitor especially at high LO frequency. Fig. 5.3(d) shows the simulated behavioral-level NF versus LO frequency with realistic circuit parameters. For a $10\ \Omega$ switch R_{on} , the NF is 1.6 dB at low frequencies and increases slightly at high frequencies due to the finite slope of the non-overlapping clock. Adding the parasitic capacitors at the RF input ($C_{par1} = 2\text{ pF}$) and the sampling node ($C_{par2} = 3\text{ pF}$) to the model (Fig. 5.3(a)), the NF is higher and increases even more at higher LO frequencies. Capacitor C_{par1} directly reduces the RF signal at high frequencies resulting in an increase in NF.

Taking into account the parasitic capacitance C_{par2} and C_{gm} (Fig. 5.3(b)), the receiver input impedance with NPF at an LO frequency f_{LO} is $0.63/[(C_s + C_{par2} + C_{gm})f_{LO}]/8$. The presence of C_{par2} and C_{gm} results in a maximum LO frequency $F_{lo,max}$ when C_s is set to 0. If the LO frequency is higher than $F_{lo,max}$, the receiver input resistance decreases which reduces the RF signal and increases the NF. Reducing the parasitic capacitance C_{par2} improves noise performance.

A drawback of the modified SC receiver is that the Gm parasitic capacitor (C_{gm}) limits the frequency range even if other non-idealities are ignored. For the inverter-based Gm cell shown in Fig. 5.4, the transconductance g_m is proportional to W/L and C_{gm} is proportional to WL for a given process and bias condition [80]. Using transistors with smaller length in the Gm cell reduces

C_{gm} while not changing g_m . However, small-size Gm cells increase the flicker-noise corner of the receiver since flicker noise corner frequency f_c is proportional to g_m/WL [80]. Fig. 5.4 shows the simulated Gm parasitic capacitance, flicker noise corner, and the calculated maximum f_{LO} versus the transistor length, assuming the total Gm transconductance in one SC bank in the modified SC receiver is 100 mS for both I and Q paths. We observe a trade-off between maximum f_{LO} and flicker noise corner. To achieve a 0.6 GHz maximum f_{LO} , the flicker noise corner is around 2 MHz, a value too high for a signal bandwidth of several MHz. It is therefore necessary to lower flicker noise while achieving high maximum f_{LO} .

5.2.3 The Chopping Switched-Capacitor RF Receiver Architecture

To break the trade-off between maximum f_{LO} and flicker-noise corner in the modified SC receiver, an SCRX with chopping is presented to remove the Gm flicker noise. Minimum-length transistors are used in the Gm cells to maximize the receive frequency range and reduce the Gm area.

The operation of our modified SC receiver is shown in Fig. 5.5(a). The sampling rate of the eight time-interleaved SC banks is f_s resulting in an f_{LO} of $f_s/8$. For SC band #i, both the desired signal at f_{LO} and the interference at the LO harmonics (e.g. 3rd and 5th LO harmonics) are down-converted to node $V_{sp}\langle i \rangle$. The Gm flicker noise is then added to the desired signal. The Gm output currents $I_{gm}\langle i \rangle$ s for all SC banks are combined before being amplified by the transimpedance amplifier (TIA) with phase shift $i\pi/4$. Since the Gm cells are scaled as a sine wave as in a harmonic rejection mixer [78], the down-conversion from 3rd and 5th order harmonics is rejected and the flicker noise remains in the desired signal band.

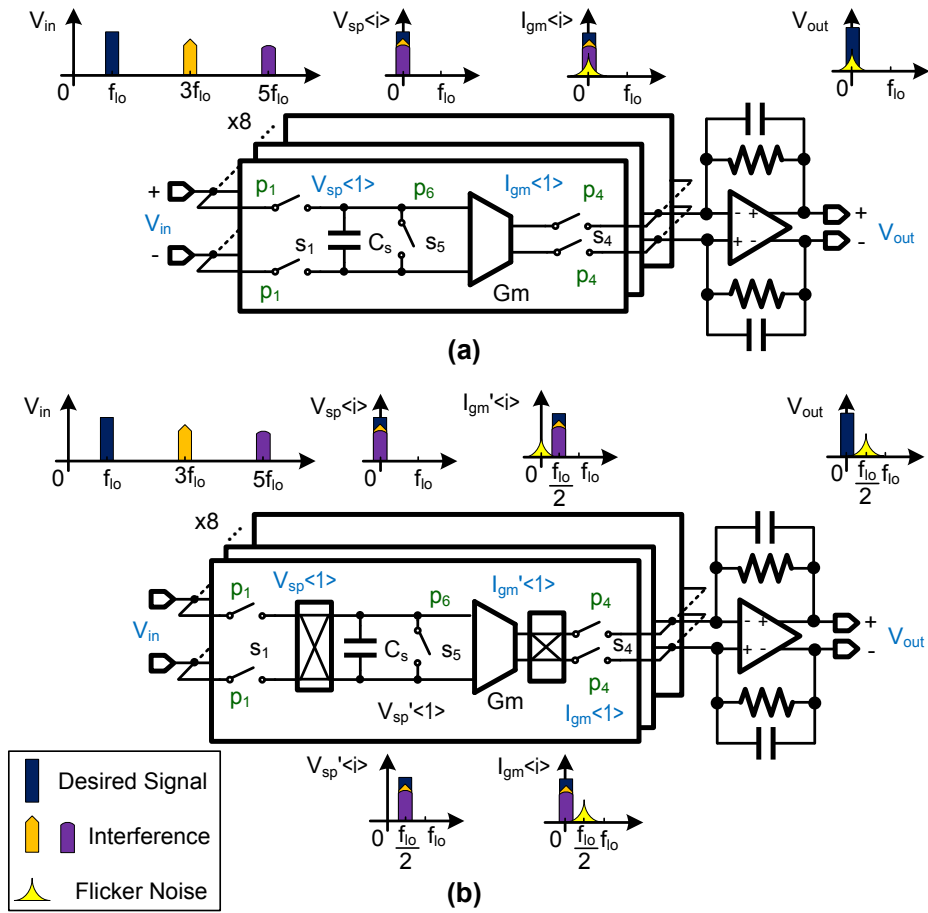


Figure 5.5: (a) Modified differential switched-capacitor receiver with improved noise performance; (b) proposed modified switched-capacitor receiver including chopping.

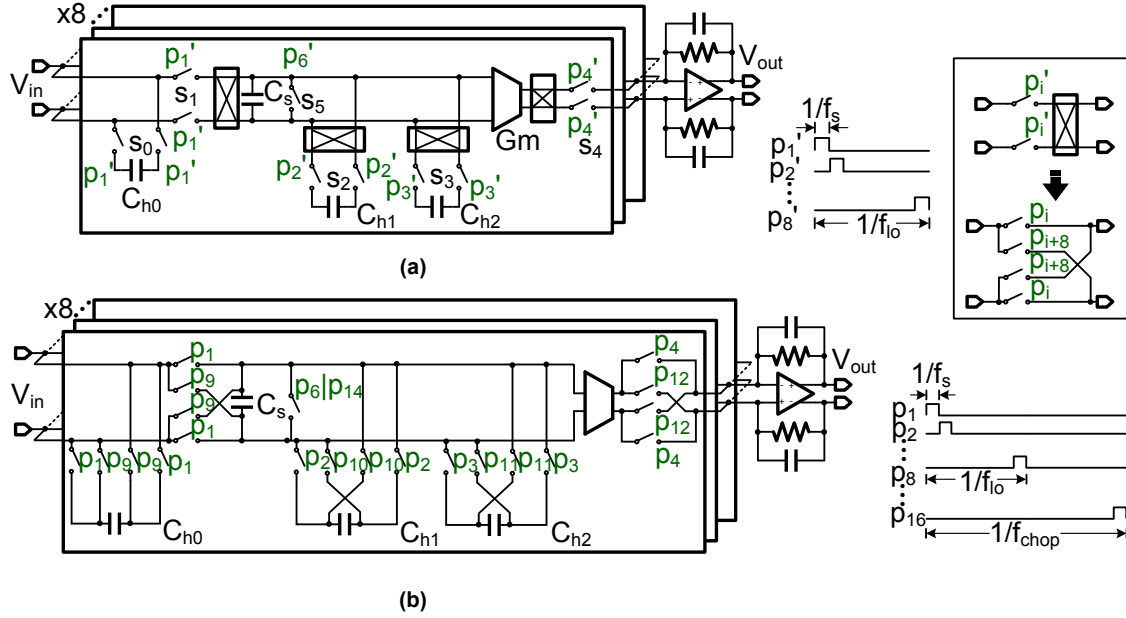


Figure 5.6: (a) Architecture of the proposed chopping switched-capacitor RF receiver with high-order filtering; (b) Implementation with the chopper merged into the switched-capacitor circuits.

By adding choppers before C_s and after G_m (Fig. 5.5(b)), the desired signal is up-converted to the chopping frequency $f_{chop} = f_{LO}/2$, before it reaches the G_m input. The desired signal is down-converted back to baseband before all G_m currents are combined, while the G_m flicker noise is up-converted to the chopping frequency. Fig. 5.6(a) shows the Chopping SCRX with high-order filtering. All switches are driven by eight-phase non-overlapping clock signals p_1' to p_8' . Choppers in series with the switches attached to C_{hi} are used to ensure that IIR filter transfer function is maintained while chopping. The chopper and the SC circuits can be merged while replacing the clock signals to a sixteen-phase non-overlapping clock p_1 to p_{16} (Fig. 5.6(b)). Switches driven by p_i' and the attached chopper are replaced by two cross-coupled switch pairs driven by p_i and p_{i+8} , so that $f_{chop} = f_s/16$. The sixteen time intervals can be equally divided into two groups. The sampling polarity is changed every eight time interval. At the end of each eight time interval, the C_s is reset,

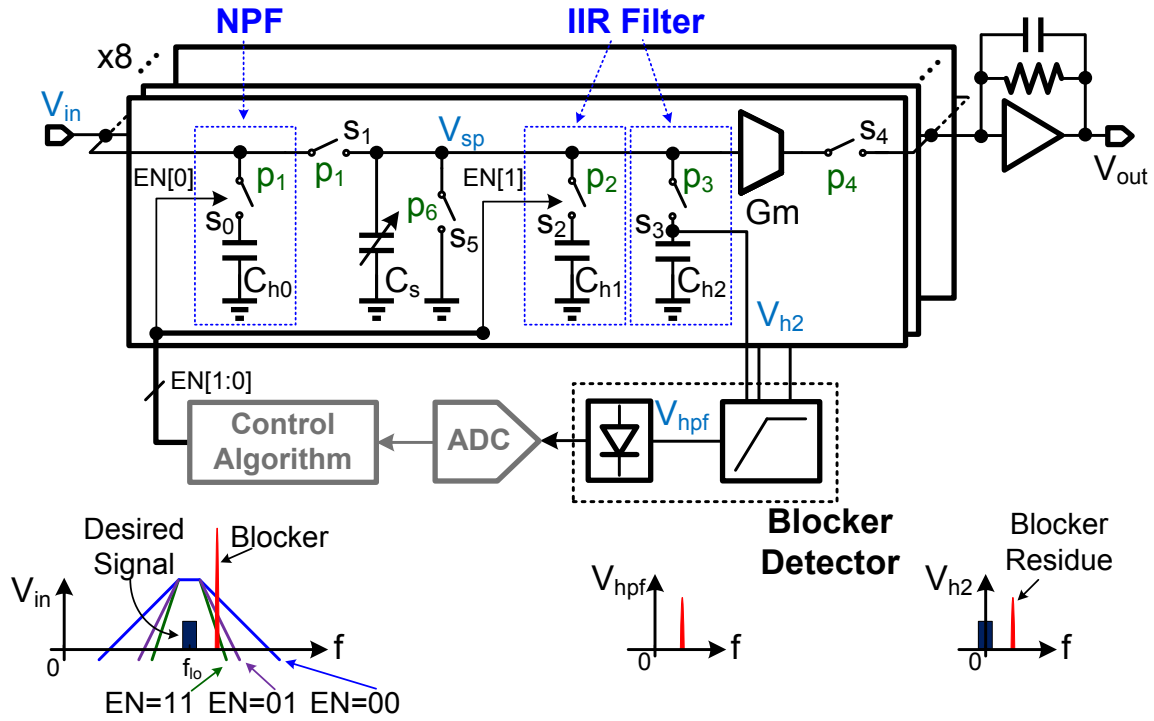


Figure 5.7: Block diagram of the switched-capacitor RF receiver with RF blocker power detector.

so the circuits between different choppers have no memory effect, resulting in a transfer function for the chopping receiver that is identical to the transfer function of a receiver without chopping. In addition, the noise source of each switch in our chopping receiver is independent, with one switch pair turned on in the chopper at each time interval. The noise performance from the SC receiver's thermal noise with chopping and without chopping should be the same.

5.3 Programmable Blocker Filtering and Blocker Detection

The SC receiver with programmable blocker filtering and blocker detection (Fig. 5.7) is shown for simplification with the singled-ended SC receiver driven eight-phase clock without chopping. The programmable filter is used to improve OB linearity. The SC circuits placed before the Gm

cells have very high linearity with blocker tolerance limited only by supply voltage and transistor threshold voltage to achieve the rail-to-rail blocker tolerance [5]. However, for the SC receiver without filtering (Fig. 5.3(b)), OB linearity is limited by active Gm cells. By introducing high-order filtering into the SC receiver, the OB blocker can be attenuated before it is amplified by the Gm. High-order filtering is achieved by the NPF (C_{h0} with s_0) at the RF input and the second-order IIR filter (C_{h1} with s_2 , and C_{h2} with s_3) after sampling, with filtering occurring sequentially. For SC bank #1, the filter attenuates the OB interferer in p_1 to p_3 . Since the signal is propagated only to the TIA in p_4 , during this time interval OB blocker amplitude at Gm input is already attenuated to reduce the distortion generated by the analog circuits. While higher-order filtering before Gm cells provides larger OB attenuation and better OB linearity, the high-order filter needs more clock power consumption to drive the SC filters. This power dissipation is unnecessary when OB interference does not exist or has lower power. The filter thus needs to be programmed to a lower-order filtering mode with a lower OB interference level.

We incorporate an integrated blocker detection before the non-linear Gm cells, so that the filter order can be tuned when a large blocker is detected. Since the blocker residue is available on the history capacitor C_{h2} , simple detector implementation can be achieved. In the SC receiver (Fig. 5.7), the last IIR filter is always turned on as a default configuration. After s_3 is turned on, C_s and C_{h2} have the same voltage, and C_s holds this voltage when s_4 is turned on. V_{h2} is thus a replica of the voltage amplified by the Gm, and holds the blocker residue after filtering. In the blocker detector, the high-pass filter attenuates the in-band signal and the envelope detector detects the blocker residue to configure the filter order. Because C_{h2} is tens of pF, detecting the blocker

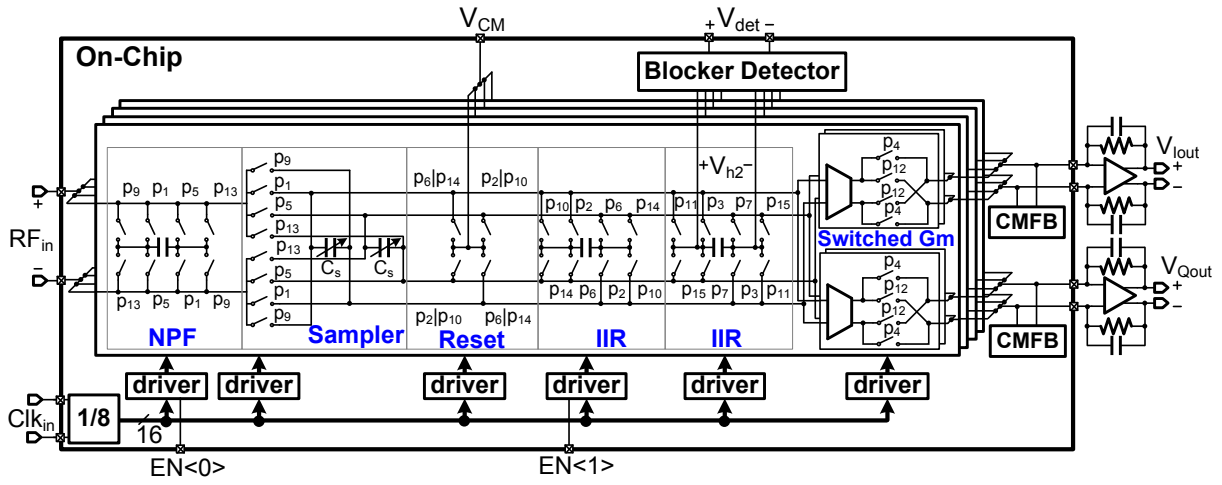


Figure 5.8: Schematic of the chopping switched-capacitor RF receiver.

at V_{h2} results in very low circuit overhead and performance penalty, so detector input capacitance can be ignored and does not affect the transfer function. If we try to detect the blocker directly at the Gm input node, the minimum capacitance at V_{sp} node will increase and limit the maximum f_{LO} as discussed in Section 5.2. Additionally, switches need to be added after the detector to ensure that only the voltage is amplified when s_4 is turned on. If we detect the blocker at Gm output, a large AC coupling capacitor must be used since the detector requires low input impedance due to the low TIA input impedance.

5.4 RF Receiver Circuit Implementation

5.4.1 RF Receiver Circuit Architecture

The architecture of the chopping SC receiver prototype IC (Fig. 5.8) consists of four SC banks, common-mode feedback (CMFB) circuits, a blocker detector, and a clock generator. Off-chip TIAs

convert Gm output currents to voltages in I and Q paths. In each SC bank, the C_s pairs with sampling phase p_i and p_{i+4} share the same C_h s in NPF and the IIR filters to reduce the DC and even-order LO harmonic response. The switches are implemented with CMOS transmission gates. The NMOS and PMOS in the switch have the same size $W/L = 100\mu\text{m}/60\text{nm}$. The Gm cells generate I and Q baseband currents. The Gms push current only to the TIAs when the output switches are turned on, which means the Gms need to be activated only in 1/8 duty cycle in one period $16T_s$. The Gms are therefore powered down in inactive time intervals to save power, achieved by the switched Gm. The on-chip LO divider generates the 16-phase non-overlapping clock signals, with filter order configured by the clock drivers as in [5].

Harmonic rejection is implemented by scaling the Gms in I and Q paths as cosine and sine waves. The two main Gm factors used in the I and Q paths are $gm \cdot \cos(i\pi/4)$, $gm \cdot \sin(i\pi/4)$ (factor #1) and $gm \cdot \cos(i\pi/4 + \pi/8)$, $gm \cdot \sin(i\pi/4 + \pi/8)$ (factor #2) [81], where gm is the effective transconductance in the DT mixing [5], and i is the SC bank index. Total Gm transconductance in these two cases is $4.8gm$ and $5.2gm$. Since the DC current is proportional to the transconductance, using factor #1 can save power consumption. However, because the switched Gm is used, total DC currents in the I and Q paths are not the same at different time intervals generating a ripple on the supply. Because of this effect factor #2 with a 5:12 size ratio is used to approximate the $\sin(\pi/8) : \sin(3\pi/8)$ ratio resulting in an effective gm of 114 mS. The harmonic rejection ratio (HRR) depends on the gain and phase mismatches [59], and can be improved using calibration [5, 36].

The gain of the receiver can be derived as in [5]. The samplers are modeled as a CT transfer

function $G(f)$ and ideal samplers with choppers, and the switched Gm cells are modeled as DT mixers with chopping followed by reconstruction circuits to convert the DT signals back to the CT domain. The conversion gain is

$$CG(f_{in}) = \frac{V_{out}(f_{in} - f_s/8)}{V_s(f_{in})} = G(f_{in}) \cdot \frac{1}{T_s} \cdot \frac{1}{2} gm \cdot T_s \text{sinc} \left(\pi \frac{f_{in} - f_s/8}{f_s} \right) \cdot R \approx \frac{1}{2} G(f_{in}) gm R, \quad (5.3)$$

where f_{in} is the input RF frequency close to an LO frequency of $f_s/8$, gm is the equivalent Gm transconductance for DT mixing, and R is the feedback resistor in the TIA. The sinc function approximates to 1 for f_{in} close to $f_s/8$. The noise factor of the receiver is

$$F = 1 + \frac{R_{on,l}}{R_s} + \frac{1}{|G(f_s/8)|^2} \left\{ \frac{e^{-1/f_s R_s C_s}}{2 f_s R_s C_s} + \frac{1}{gm R_s} \left[\gamma [\sin(\pi/8) + \sin(3\pi/8)] + \frac{2\gamma gm_{CMFB}}{gm} \right. \right. \\ \left. \left. + \frac{2}{gm R} + \frac{\overline{V_{n,op}^2} (1 + R/R_{o,gm})^2}{2kT gm R^2} \right] \right\}, \quad (5.4)$$

where $G(f)$ is the sampler gain shown in (5.2), gm_{CMFB} is the transconductance of the common-mode feedback (CMFB) circuit, $\overline{V_{n,op}^2}$ is the input referred voltage noise source of the op-amp in the TIA, and $R_{o,gm}$ is the Gm output resistance. In a transistor-level circuit the sampler gain decreases at higher LO frequencies since the parasitic capacitance of the switches and the routing wire limits the bandwidth at the RF input. In addition, the non-ideal non-overlapping clock with finite rise and fall time reduces the switch turn-on time in the sampling phase at higher LO frequency which also reduces the sampler gain. NF thus increases with LO frequency in a transistor-level circuit due to reduction in $G(f)$ in (5.4). Using a more scaled process with lower parasitic capacitance and a better clock generator improves the NF at high LO frequencies. The Gm-TIA circuit is

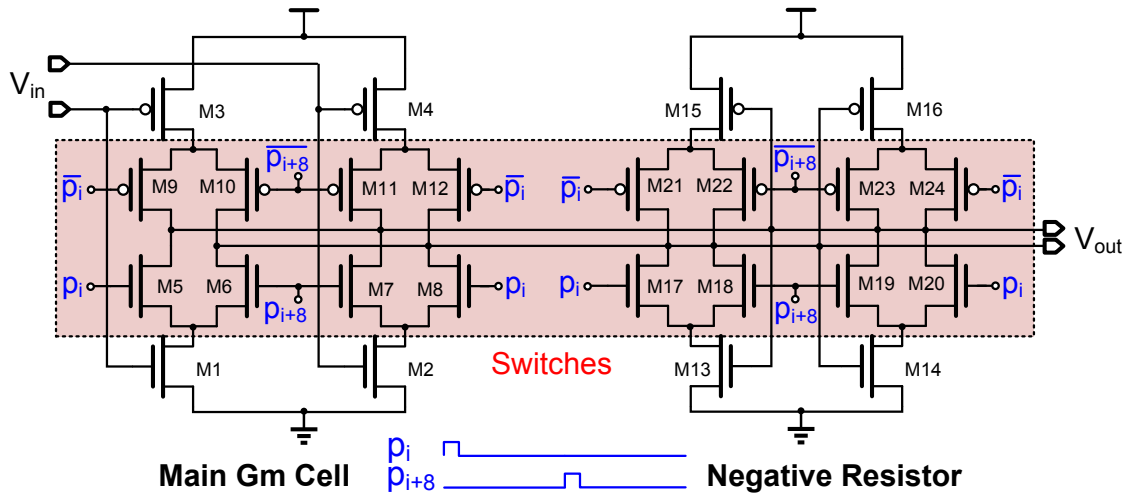


Figure 5.9: Schematic of the baseband switched Gm cell.

also a significant noise source in the chopping SCRX. The NF can be improved with larger gm value in (5.4). The finite gm output resistance increases the noise contribution of the TIA opamp. The output resistance of a 100 mS Gm with a minimum-channel-length transistor is only several hundred Ohms, To improve this value, the negative Gm at the Gm output is used (described in Section 5.4.2).

5.4.2 Baseband Circuit

Circuit implementation of the switched Gm (Fig.5.9) consists of a main Gm cell and a negative resistor. The input common mode voltage is set to V_{CM} in reset phase (Fig. 5.8) and the output common mode voltage is set by the CMFB circuit as in [29]. Inverter-based design [82] is adopted to improve power efficiency. In the main Gm cell, transistors M1-M4 provide transconductance, and the NMOS and PMOS are sized to achieve the same transconductance. Transistors M5-M12 are the switches that propagate the Gm output current to the TIA and achieve the chopping. The

DC current of the Gm is cut down when the switches are off to save power [83]. The minimum length transistors with low output impedance used in the main Gm cell increase the noise contribution of the TIA op-amp. A negative resistor [30] is adopted at the Gm output node to increase output impedance. Transistors M13-M16 generate negative resistance, and M17-M24 cut off the DC current as in the main Gm cell. All transistors in the switched Gm use minimum length thanks to the chopping technique. In the same way as we saw with the switches, the Gm area is scaled with the CMOS process. Compared with switch-Gm in [83], transistors M1-M4 and M13-M16 work in saturation region when the switches are on, and work in inversion mode when the switches are off to avoid build-up time of the inversion layer while the switches are turned on as well as to avoid the parametric loss at Gm input [84]. If M1-M4 work in depletion mode when the switches are off, a parametric loss of $(C_s + C_{gm,dep}) / (C_s + C_{gm,sat})$ is generated when the switches are turned on, where $C_{gm,dep}$ is Gm input capacitance in depletion mode and $C_{gm,sat}$ is the Gm input capacitance in saturation region, $C_{gm,dep} < C_{gm,sat}$.

The transistor-level simulated conversion gain of the SCRX without NPF is 36.3 dB which matches the calculated 37.4 dB conversion gain. The simulated NF of the behavioral-level receiver with only SC noise without NPF is 1.6 dB with $10\ \Omega$ switches R_{on} which does not change with LO frequency (Fig. 5.14(b)). With parasitic capacitance at RF input and clock non-idealities, NF increases with LO frequency. The simulated NF of the transistor-level receiver with parasitics and clock non-idealities is 3.9 dB for a 0.1 GHz LO with an increase to 8.5 dB when LO is 0.6 GHz. Compared to the NF with and without noise from the Gm-TIA circuit, we find Gm-TIA to be the main noise source.

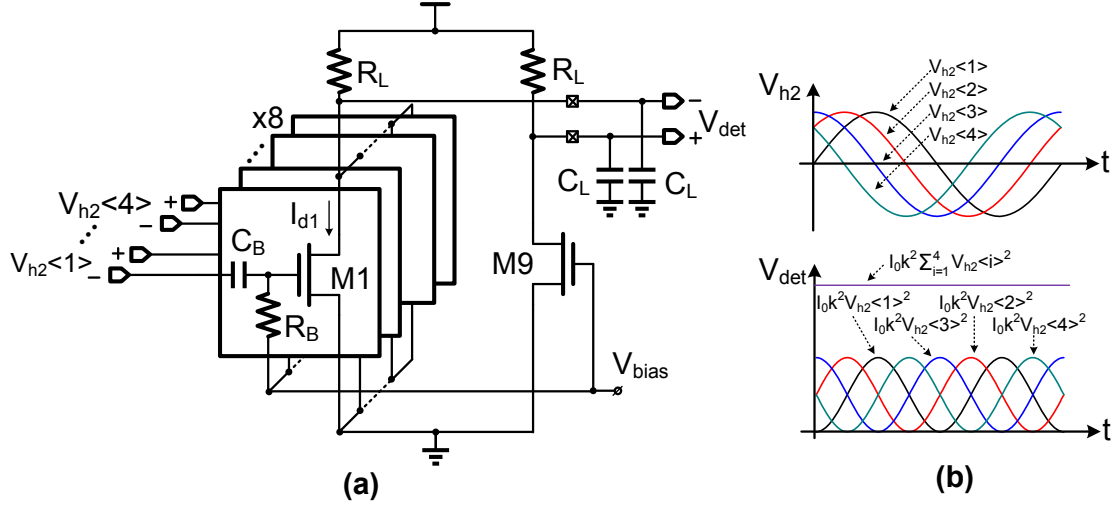


Figure 5.10: (a) Schematic of the blocker detector. (b) Input and output waveforms of the blocker detector.

5.4.3 Blocker detection circuit

The blocker detector (Fig. 5.10(a)) consists of eight AC coupled common-source transistors with resistor and off-chip capacitor loads and a replica. The $55\ \Omega$ R_B and $1.3\ \text{pF}$ C_B compose a high-pass filter to attenuate the in-band signal. All the transistors work in weak inversion mode. The output current of each transistor is $I_d = I_0 \cdot \exp(kV_{gs})$ [85]. For history capacitor voltage $V_{h2< i >}$, output current is $I_0[\exp(kV_{h2< i >}) + \exp(-kV_{h2< i >})] \approx 2I_0 + I_0 k^2 V_{h2< i >}^2$. Since each $V_{h2< i >}$ has a phase shift of $i\pi/4$ and the output current of the replica is $8I_0$, the detector output voltage is

$$V_{det} = I_0 k^2 \sum_{i=1}^4 [V_{h2,pk} \cos(\omega_{IF} t + i\pi/4)]^2 = 2I_0 k^2 V_{h2,pk}^2, \quad (5.5)$$

(Fig. 5.10(b)) with the blocker detector detecting the envelope of the IF blocker signal. The load resistor R_L is $15\ \text{k}\Omega$ and the load capacitor C_L is $10\ \text{pF}$ to achieve a small settling time.

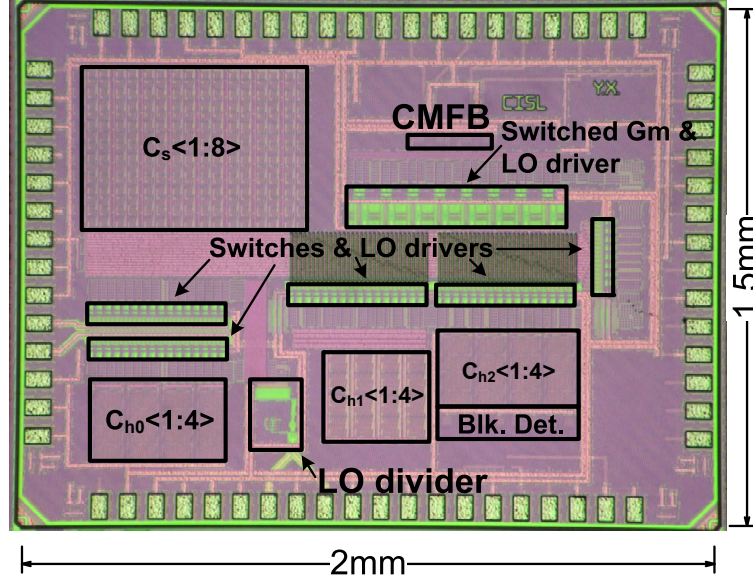


Figure 5.11: Chip photo.

5.5 Measurement Results

Our chip prototype was fabricated in a 65nm CMOS process with an active area of 1.63 mm^2 (Fig. 5.11). The supply voltage of the baseband circuit is 1.1 V and 1.25 V for the LO circuits.

Fig. 5.12 shows measured differential input reflection coefficient s_{11} . The receiver achieves a wideband impedance matching without NPF as in [5]. With NPF, the OB S_{11} is higher due to low NPF OB impedance, and the deviation of S_{11} center frequency and LO frequency is caused by RF input parasitic capacitance [26]. For the remainder of the measurements, an off-chip 180° hybrid drives the differential RF input, and the loss of the hybrid is calibrated out.

Fig. 5.13 shows the measured conversion gain $V_{\text{Iout}}/(V_s/2)$ and LO current for LO frequencies from 0.1 to 0.6 GHz for different filter orders. The conversion gain is lower for higher LO frequencies due to the parasitic capacitance and clock non-idealities. The OB attenuation and LO current increase with higher filter order.

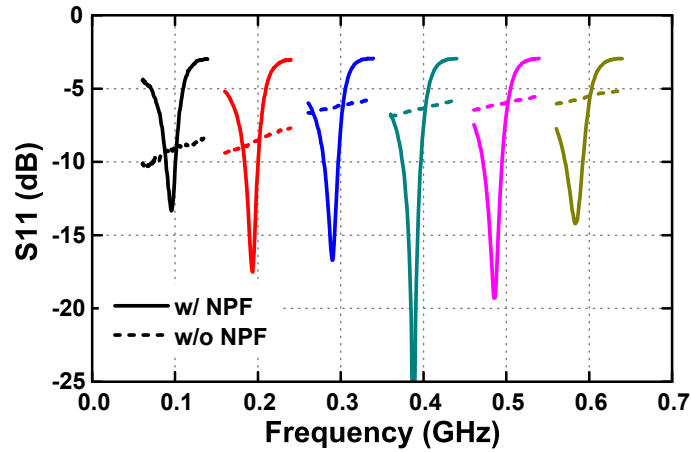


Figure 5.12: Measured differential-mode S_{11} for LO frequencies ranging from 0.1 to 0.6 GHz with a 0.1 GHz step with and without the N-path filter.

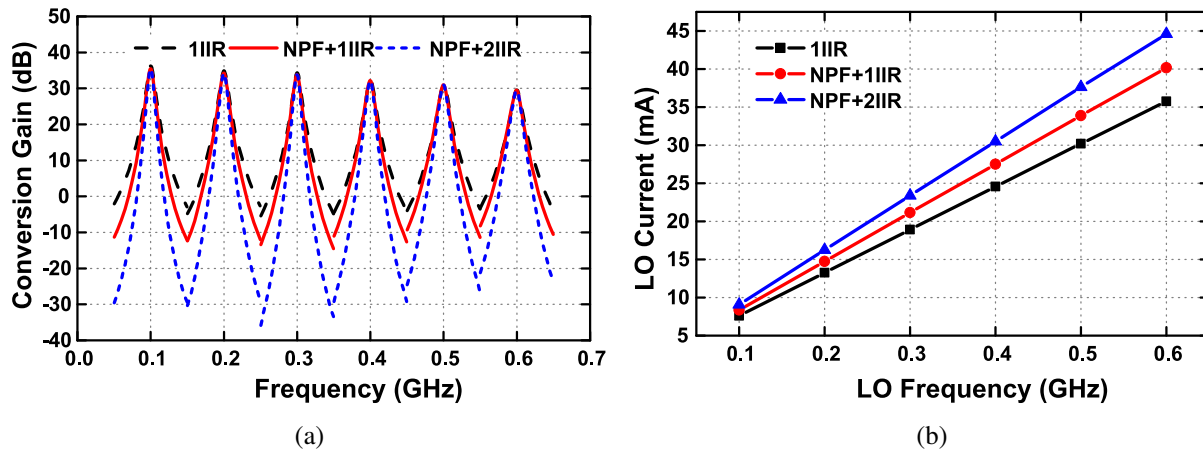


Figure 5.13: Measured (a) conversion gain V_{Iout}/V_{RF} ; (b) LO current versus RF frequency for LO frequencies ranging from 0.1 to 0.6 GHz with a 0.1 GHz step and for different filter configurations.

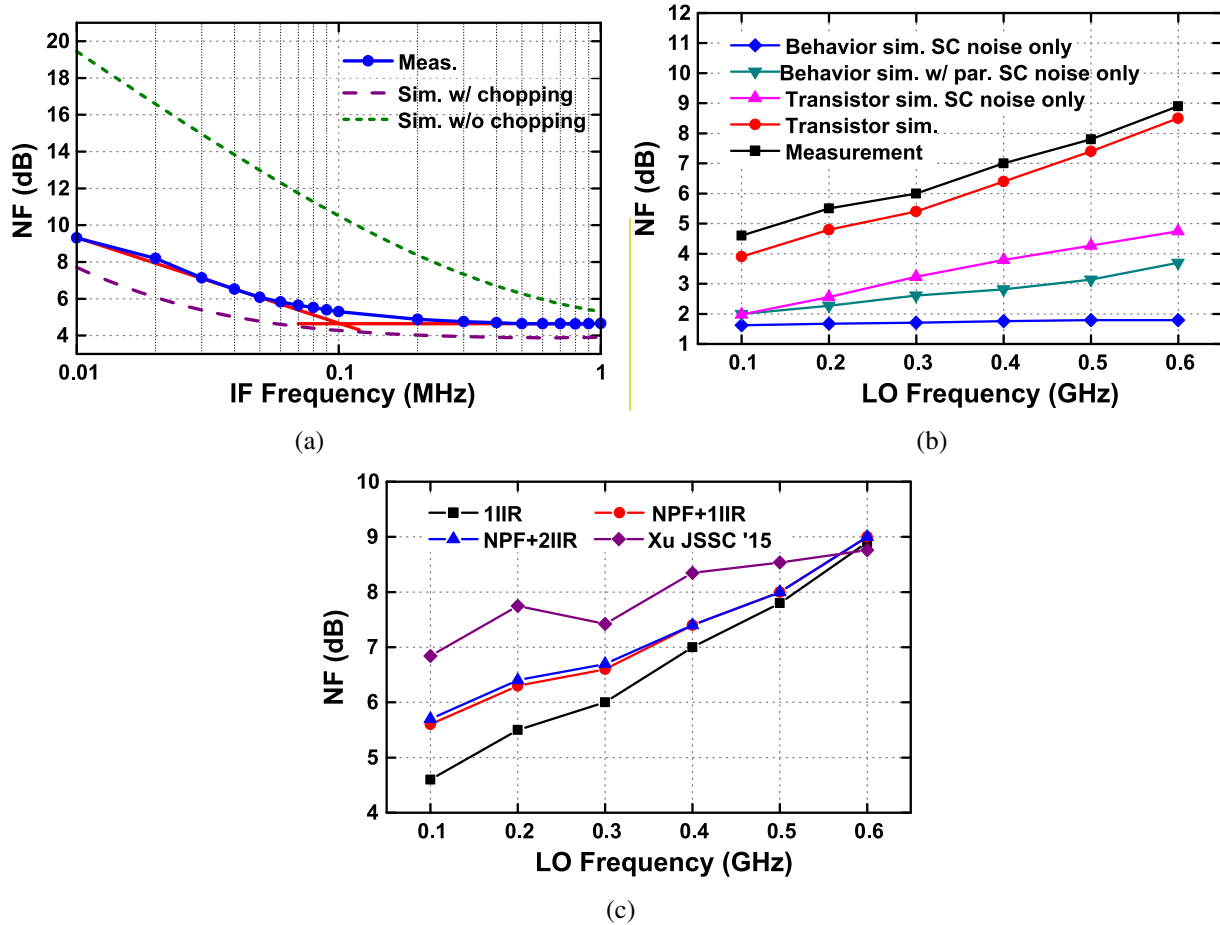


Figure 5.14: (a) Measured and simulated NF versus IF frequency for an LO frequency of 0.1 GHz with first-order IIR filtering; (b) Measured and simulated NF versus LO frequency for the receiver with first-order IIR filter; (c) Measured NF across LO frequency compared with earlier switched-capacitor receiver.

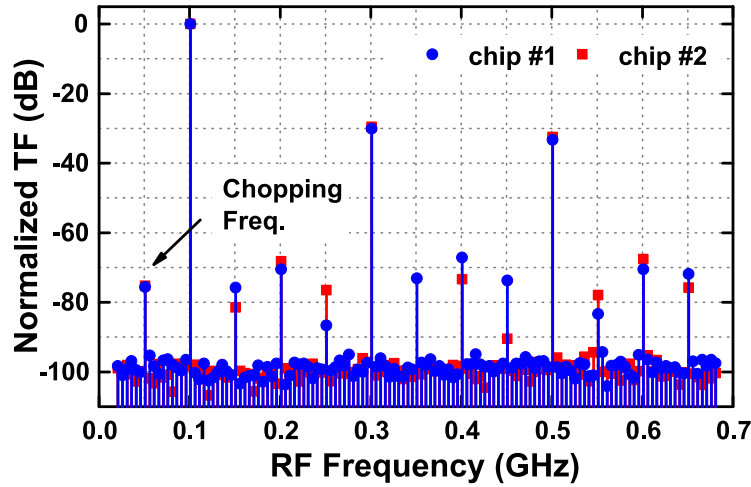


Figure 5.15: Measured wideband transfer function for an LO frequency of 0.1 GHz.

The measured and simulated NF versus IF frequencies with 0.1 GHz LO and first-order IIR filter are shown in Fig.5.14(a). The measured flicker noise corner is 100kHz with chopping while the simulated flicker noise corner without chopping is significantly higher. The simulated and measured NF versus LO frequency is shown in Fig. 5.14(b)(c). The noise degradation compared to ideal circuit is discussed in Section 5.4.2. The NF for a 0.1 GHz LO with first-order IIR filter is 4.6dB which is 2.2dB better compared with the earlier SCR_X [5]. With the NPF, the NF is higher due to NPF loss. The NF increases with LO frequency due to RF input parasitic capacitance and clock non-idealities.

The measured wideband transfer function for a 0.1 GHz LO is shown in Fig.5.15. The HRR for 3rd order is 30 dB and for 5th order LO harmonics is 33 dB. If better HRR is needed, the calibration method of [5, 36] can be applied. The chopping frequency for a 0.1 GHz receiver is 50 MHz. The spurious responses due to chopping are lower than -70 dB, and are not higher than the responses from LO even-order harmonics.

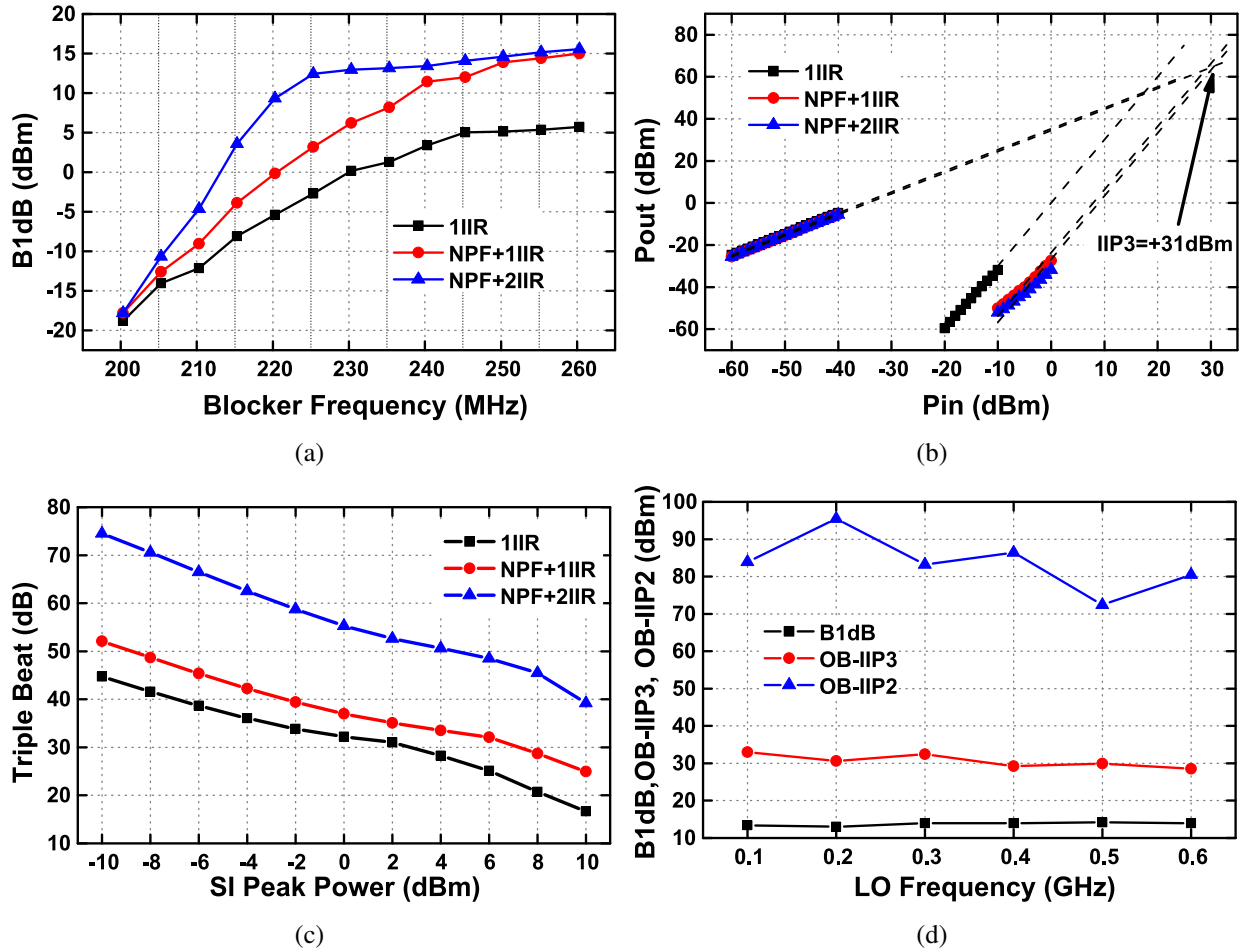


Figure 5.16: (a) Measured blocker 1dB compression point versus blocker frequency; (b) out-of-band IIP3; and (c) triple beat versus two-tone SI peak power for an LO frequency of 0.2 GHz with different filter configurations; (d) measured B1dB, OB-IIP3, OB-IIP2 for LO frequencies stepped between 0.1 and 0.6 GHz.

Fig.5.16(a) shows the measured blocker 1dB compression point (B1dB) versus blocker frequency for a 0.2 GHz LO. As expected the B1dB for a close-by blocker increases with filter order. When all filters are enabled, the B1dB for a 30 MHz blocker offset is 13 dBm and the maximum B1dB is larger than 15 dBm ($3.6 V_{pp}$ if referred to a 50Ω resistor). The OB-IIP3 (Fig. 5.16(b)) is measured with a two-tone signal at 0.231GHz and 0.261GHz for a 0.2 GHz LO. When all filters are turned on, the OB-IIP3 is 31dBm. The triple beat (TB) (Fig. 5.16(c)) for a 0.2 GHz LO versus self-interferer (SI) peak power is measured with a -30 dBm adjacent-channel jammer and two-tone SI signals with a frequency offset as small as -30 MHz and a 5 MHz frequency spacing. The TB for a -4 dBm SI peak power is 62.5 dB with highest-order filtering, and the receiver can handle larger than 10 dBm SI peak power. The high order filtering improves B1dB, OB-IIP3, and TB compared with a first-order IIR filter. With NPF and second-order IIR filters, B1dB for a 30 MHz blocker offset is improved by 12.8 dB, OB-IIP3 is improved by 13/dB, and TB for a -4 dBm SI peak power is improved by 26.5 dB. In an FDD or co-existence application, the filter order can be tuned with SI power level information available in the same device.

We measured the blocker NF for 0.1 GHz LO frequency and a blocker at 30 MHz frequency offset with NPF and second-order IIR filter (Fig. 5.17). The NF matches the simulation result with an LO phase noise of -150 dBc/Hz at 30 MHz offset for a 1/16-duty-cycle LO. The simulated blocker NF without LO phase noise does not change with blocker power. We find that reciprocal mixing mainly increases the blocker noise figure. In future work, this can be further improved using a better clock generator. Compared to other blocker-tolerant receivers, our receiver achieves a better blocker NF for a large blocker (5dBm) thanks to its low gain compression.

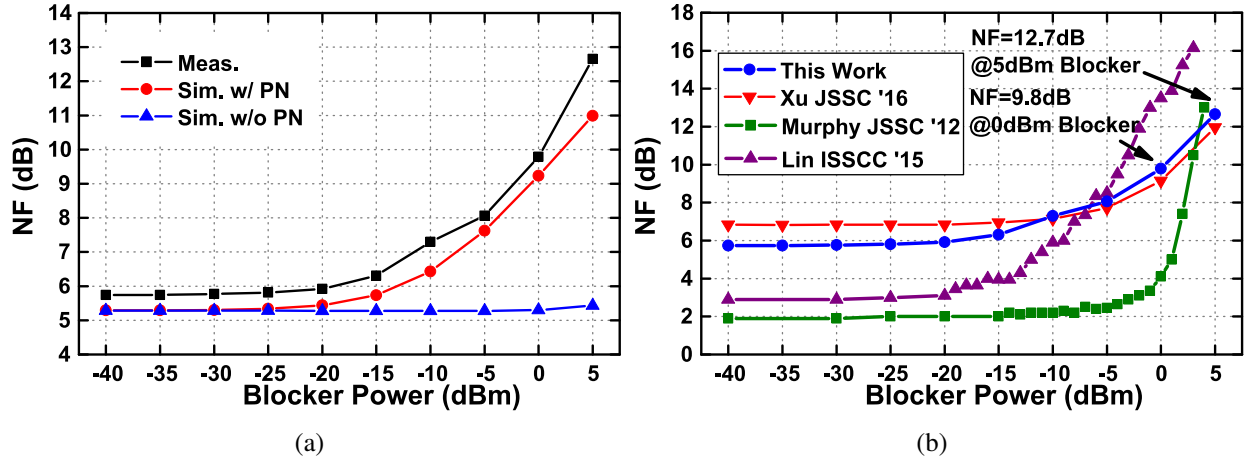


Figure 5.17: (a) Measured and simulated blocker noise with blocker at 30MHz for a 0.1 GHz LO. (b) Measured blocker noise figure compared with other blocker tolerant receivers.

For an unknown CW OB blocker, the blocker detector can be used to adapt the filter order to the blocker power between two communication packets. Fig.5.18 shows the filter adaptation using the integrated blocker detector. The Gm input-referred blocker power (Fig.5.18(a)) is the blocker power level at the input of the (nonlinear) Gm and is calculated by subtracting the normalized measured RF filtering transfer function from the applied blocker input power. The detector output voltage is a linear function of the Gm input referred blocker power. Fig. 5.18 shows the measured conversion versus blocker power with adaptive filter order for a 0.2 GHz LO and 30MHz blocker offset. The detector output voltage increases with blocker power; when the voltage is higher than a threshold (50mV), the filter order is increased and improves gain compression. The blocker detector transient response (Fig.5.18(c)) settles at less than 1us; after increasing the filter order, the Vdet stabilizes again in 1us. The detector consumes only 0.2mW (including 0.1mW from bias circuits).

When compared with the state of the art (Table 5.1), our receiver achieves the highest OB

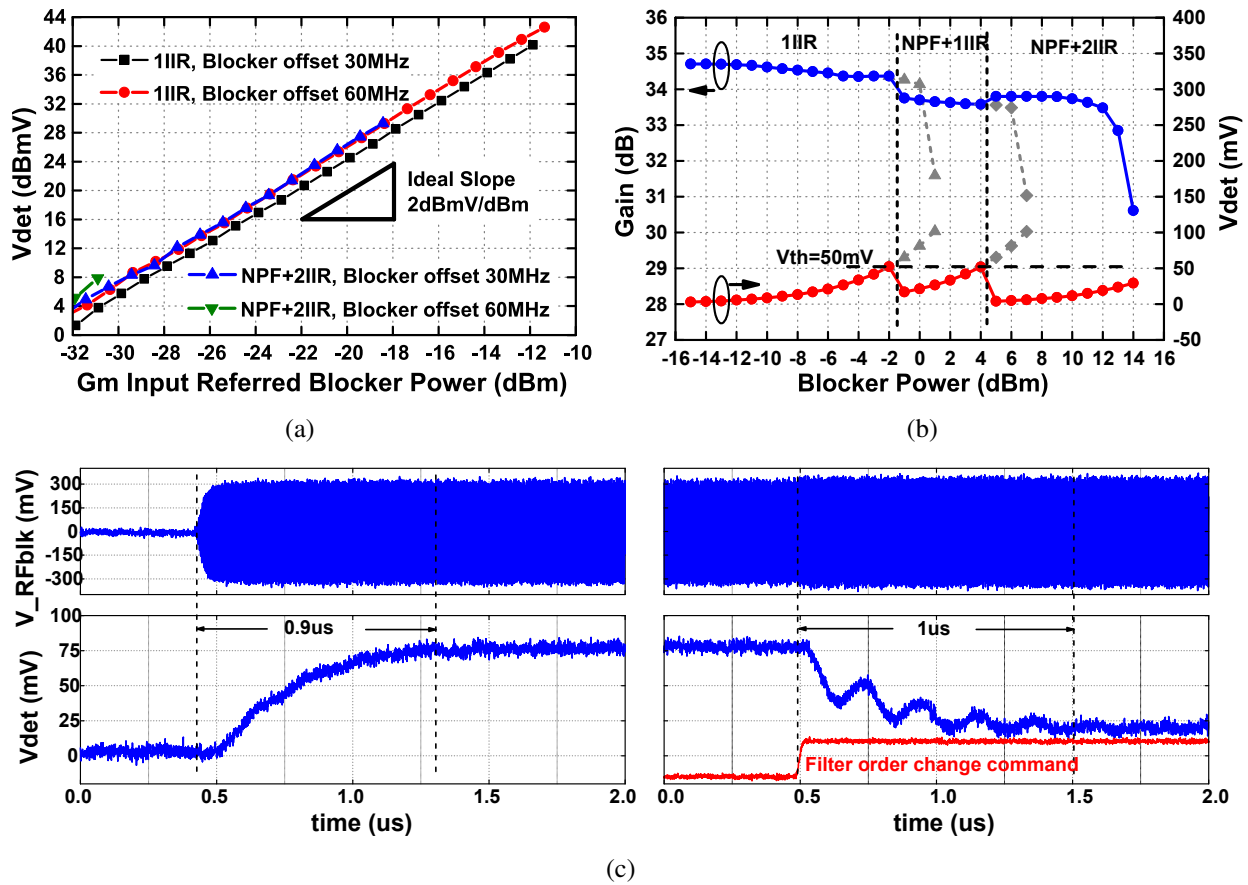


Figure 5.18: (a) Measured blocker-detector output voltage versus Gm input-referred blocker power for different filter orders and blocker offset frequencies. (b) Measured conversion gain versus blocker power with adaptive filter order for a 0.2 GHz LO and 30 MHz blocker offset. (c) The blocker-detector transient response.

Table 5.1: Comparison with the state of the art

	This work	Xu JSSC '16	Murphy JSSC '12	Zhou ISSCC '15	Darvishi JSSC '13	Lin ISSCC '15
Technology	65nm	40nm	40nm	65nm	65nm	
Architecture	Chop. SC	SC	FTNC	SI Canc.	NPF	Mixer-first
Blocker detector	Yes	No	No	No	No	No
RF freq. (GHz)	0.1-0.6	0.1-0.7	0.08-2.7	0.8-1.4	0.1-1.2	0.1-1.5
NF (dB)	4.6-9	6.8-9.7	1.5-2.4 ^a 3.5-5	4.8, 5.3 ^b	2.8	1.5-2.9
OB-IIP3 (dBm)	31	24	13 ^a , 17	17	26	13
B1dB (dBm)	15	15	<0 ^a , <5	4	7	13.5
TB _{-4dBm} ^c (dB)	63	NR	NR	48, 64 ^b	NR	NR
Max Handled Peak SI Power (dBm)	>10	NR	NR	NR, -4 ^b	NR	NR
OB-SFDR ^d (dB)	92.9	87.5	83.7 ^a , 85	84.1	91.5	83.7
Power (mW)	Ana: 24 LO: 9.5-55.8 Detector: 0.2	Ana: 52 LO: 7-53	35-78	63-69, 107-160 ^b	18-57.4	11

NR = not reported; a: with noise cancellation b: with self interference cancellation, calibration is required c: Triple beat at a -4dBm SI peak power d: OB-SFDR = $2/3(\text{OB_IIP3} - (-174\text{dBm/Hz}) - 10\log(1\text{MHz}) - \text{NF})$

spurious-free dynamic range (SFDR) [86]. The NF and power consumption are better than in [5] and our receiver supports fast blocker detection. For FDD and the co-existence application, compared with an SI cancellation method [87], our receiver provides similar TB performance and has larger power handling. The NF increases at higher LO frequencies which is limited by parasitic capacitance. This limitation can be improved with process scaling.

5.6 Conclusions

In this chapter, a chopping switched-capacitor RF receiver with high OB linearity is presented to improve OB interference tolerance. The highly linear passive SC RF circuit placed before nonlinear baseband Gm cells provides high-order filtering and improves OB linearity. By using chopping, a key noise source in the earlier SCRX is eliminated and the NF is improved. Our blocker detector detects the blocker residue on the history capacitor before the Gm cells and does not affect receiver performance and makes it possible for the filter order to adapt quickly to blocker power. These techniques provide a more efficient way to make tunable receivers survive the limiting effects of OB interference.

Chapter 6

Analysis of Passive Gain Techniques for Switched-Capacitor Receivers

6.1 Introduction

The passive SC receiver (SCRX) described in Chapter 4 achieves programmable high-order and high-linearity filtering before the active circuits, resulting in a high OB linearity even for a close-by blocker. However, its noise figure (NF) is relatively high. Since introducing signal gain can potentially improve the NF, this chapter reviews two SCRX architectures with passive gain. The first is a capacitor-stacking SCRX (CS-SCRX). The capacitor-stacking circuits [88] amplify the desired signal before the active transconductor (G_m) by stacking sampling capacitors. The second is a parametric SCRX (P-SCRX). In this approach, MOS transistors serve as the sampling capacitor;

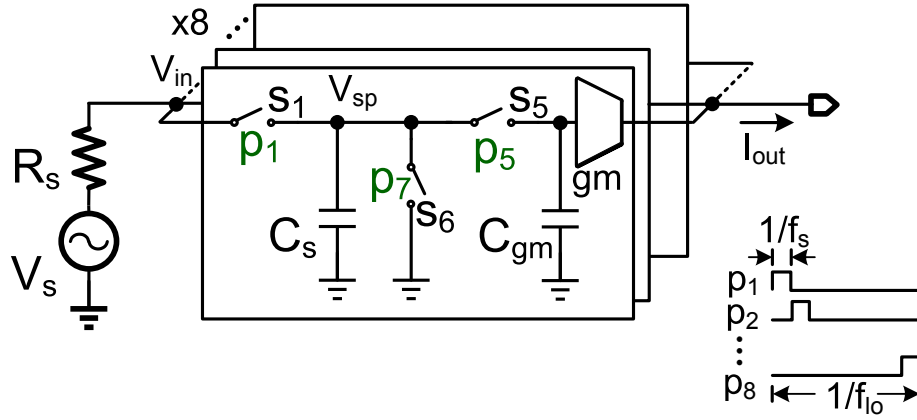


Figure 6.1: Core circuits of a switched-capacitor receiver.

the amplification is achieved by changing the transistor from inversion mode to depletion mode [89]. We propose a linearized MOS capacitor to improve the linearity of the P-SCRX.

As shown in Fig. 6.1, the core circuits of the SCRX proposed in Chapter 4 consists of eight time-interleaved SC banks. All the switches are driven by eight-phase nonoverlapping clock signals. For SC bank #1, the RF signal is sampled in p_1 , propagated to the G_m input node in p_5 and dumped to ground in p_7 . High-order SC filtering can be added to this core circuitry to achieve high OB linearity and a large OB attenuation before the nonlinear G_m cells. As described in Section 4.2, the NF lower limit of the SCRX is 4.13 dB which is relatively high.

6.2 Capacitor-Stacking Switched-Capacitor Receiver

6.2.1 Capacitor-Stacking Concept

The schematic of the CS-SCRX core circuits is shown in Fig. 6.2. To simplify the diagram, only SC bank #1 is shown in this figure. In contrast to the earlier SCRX (Fig. 6.1), the sampling capacitor

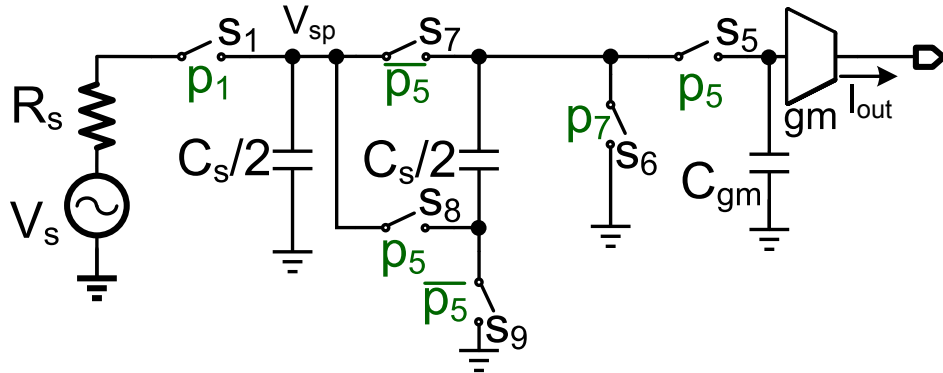


Figure 6.2: SC bank #1 of the capacitor-stacking SCRX core circuits.

is separated into two capacitors, each with half the capacitance of the conventional value. Switches s_7 – s_9 are added for capacitor stacking. s_8 is driven by clock signal p_5 , while s_7 and s_9 are driven by the inverted p_5 clock.

Fig. 6.3 shows the operation of the CS-SCRX. In the sampling phase (p_1), the RF signal is sampled on two sampling capacitors. The sampled voltage is V_{sp} . In the passive-gain phase (p_5), the two capacitors are stacked, doubling the signal. The voltage propagated to the G_m input node is $2V_{sp}$. In the reset phase (p_7), the sampling-capacitor voltage is reset to ground. When SC filters are added into this architecture, the high-order filtering phases need to be inserted before the passive-gain phase so that the capacitor stacking does not amplify the OB interference to maintain the SCRX's OB linearity.

6.2.2 Noise Limitation

The SC circuits' passive gain reduces the noise contribution of the succeeding stages. However, noise from the dominant noise source, s_5 , cannot be reduced, which limits the noise performance.

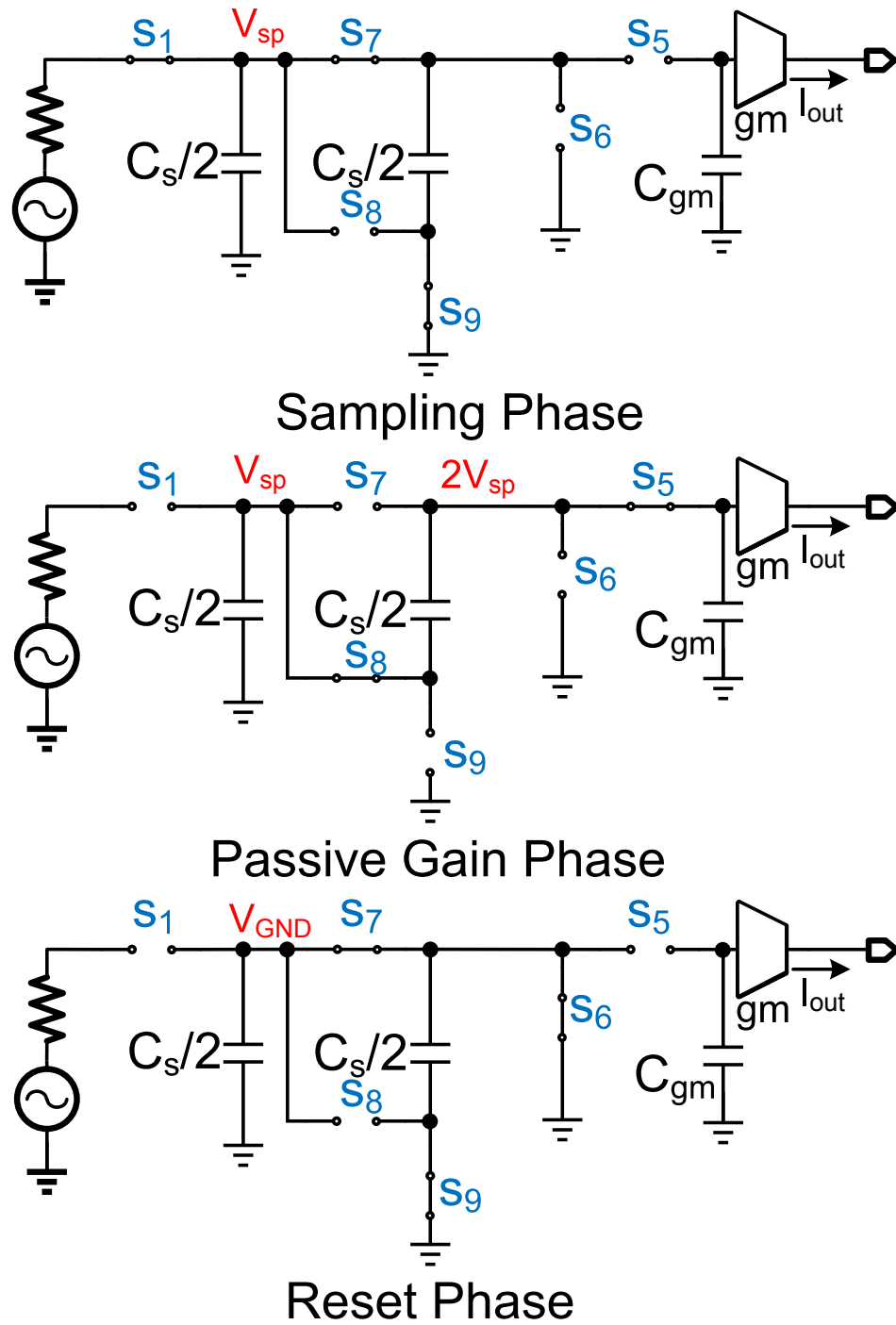


Figure 6.3: Operation of a capacitor-stacking SCRX.

For the SCRX, the s_5 noise at the G_m input is

$$\overline{V_{s_5}^2} = \frac{2kT}{C_s f_s} \cdot \Delta f, \quad (6.1)$$

assuming C_{gm} is much larger than C_s . Since the source noise at the G_m input is

$$\overline{V_{R_s}^2} = 4kTR_s \left| G \left(\frac{f_s}{8} \right) \right|^2 \cdot \Delta f, \quad (6.2)$$

the noise factor due to s_5 can be written as

$$F_{s_5} - 1 = \frac{1}{2R_s C_s f_s \left| G \left(\frac{f_s}{8} \right) \right|^2}. \quad (6.3)$$

In the CS-SCRX, the source noise is amplified by passive gain, however, the s_5 noise is also larger due to the C_s reduction in passive-gain phase. Assuming C_s consists of N capacitors, each capacitor is C_s/N and the switches are ideal. These N capacitors provide a passive gain of N in the capacitor-stacking phase. The source noise amplified by the passive gain is

$$\overline{V_{R_s,CS}^2} = 4kTR_s \left| G \left(\frac{f_s}{8} \right) \right|^2 \cdot N^2 \cdot \Delta f. \quad (6.4)$$

Since the equivalent sampling capacitance after capacitor stacking is C_s/N^2 , The s_5 noise is

$$\overline{V_{s_5,CS}^2} = \frac{2kT}{C_s f_s} \cdot N^2 \cdot \Delta f. \quad (6.5)$$

Table 6.1: Comparison of SCRX without and with capacitor stacking.

	SCRX	CS-SCRX
Gain (dB)	5.9	11.5
NF (dB)	4.9	4.7

Since both of the noise values increase by N^2 , the noise factor due to s_5 is the same as that of the earlier SCRX.

6.2.3 Simulation Results

The simulated conversion gain and NF for a SCRX with and without capacitor stacking is shown in Table 6.1. The simulation uses ideal switches with $10\ \Omega$ on-resistance. The G_m is ideal and noiseless with an input capacitance of 50 pF. The conversion gain is simulated at the G_m input node. With capacitor stacking, the conversion gain is doubled, however the NF is almost not improved.

Therefore, capacitor stacking is not a good solution to improve the SCRX noise performance since it cannot fundamentally improve the SC circuits' noise, and the noise from the succeeding stages can be improved by increasing the G_m gain instead of the passive gain. Also, the parasitic capacitance of the switches limits the SCRX frequency range and reduces the passive gain.

6.3 Switched-Capacitor Receiver with Parametric Amplification

To reduce the s_5 noise, we next study parametric amplification. SC bank #1 of P-SCRX is shown in Fig. 6.4. Compared with earlier SCRX core circuits (Fig. 6.1), the sampling capacitor is im-

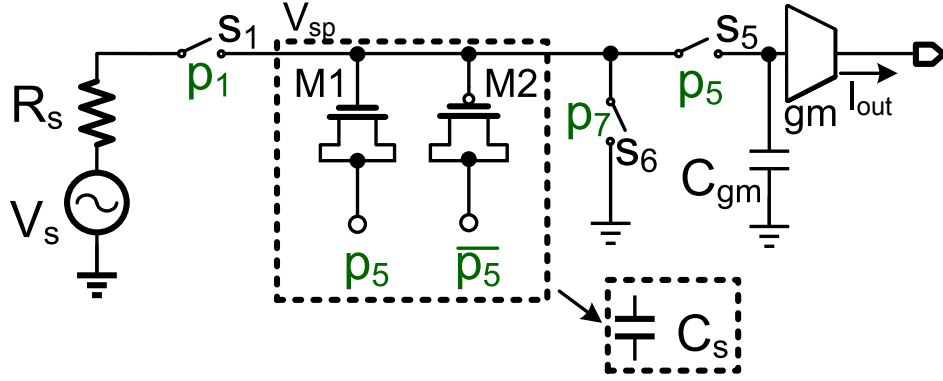


Figure 6.4: SC bank #1 of the parametric SCRX core circuits.

plemented by MOS transistors. The capacitance of the MOS capacitor is tuned by the transistor source–drain voltage, V_{SD} , to achieve the parametric amplification [84,89]. Both NMOS and PMOS are used to ensure the common mode voltage does not change when changing V_{SD} . The source–drain node of the NMOS M1 are connected to clock signal p_5 , and the source–drain node of the PMOS M2 is connected to inverted p_5 .

Fig. 6.5 shows the operation of the P-SCRX. In the sampling phase (p_1), the V_{SD} of M1 is V_{gnd} , while the V_{SD} of M2 is V_{DD} . Both MOS transistors are in inversion. The capacitance is C_s . The RF signal is sampled on the MOS capacitor, and the sampled voltage is V_{sp} . In parametric-gain phase (p_5), the V_{SD} s of M1 and M2 are switched to V_{DD} and V_{gnd} , respectively. The MOS transistors work in depletion mode, and the capacitance reduces to C_s/a ($a > 0$). Since the charge on the sampling capacitor does not change, the voltage propagated to the G_m input is $a \cdot V_{sp}$.

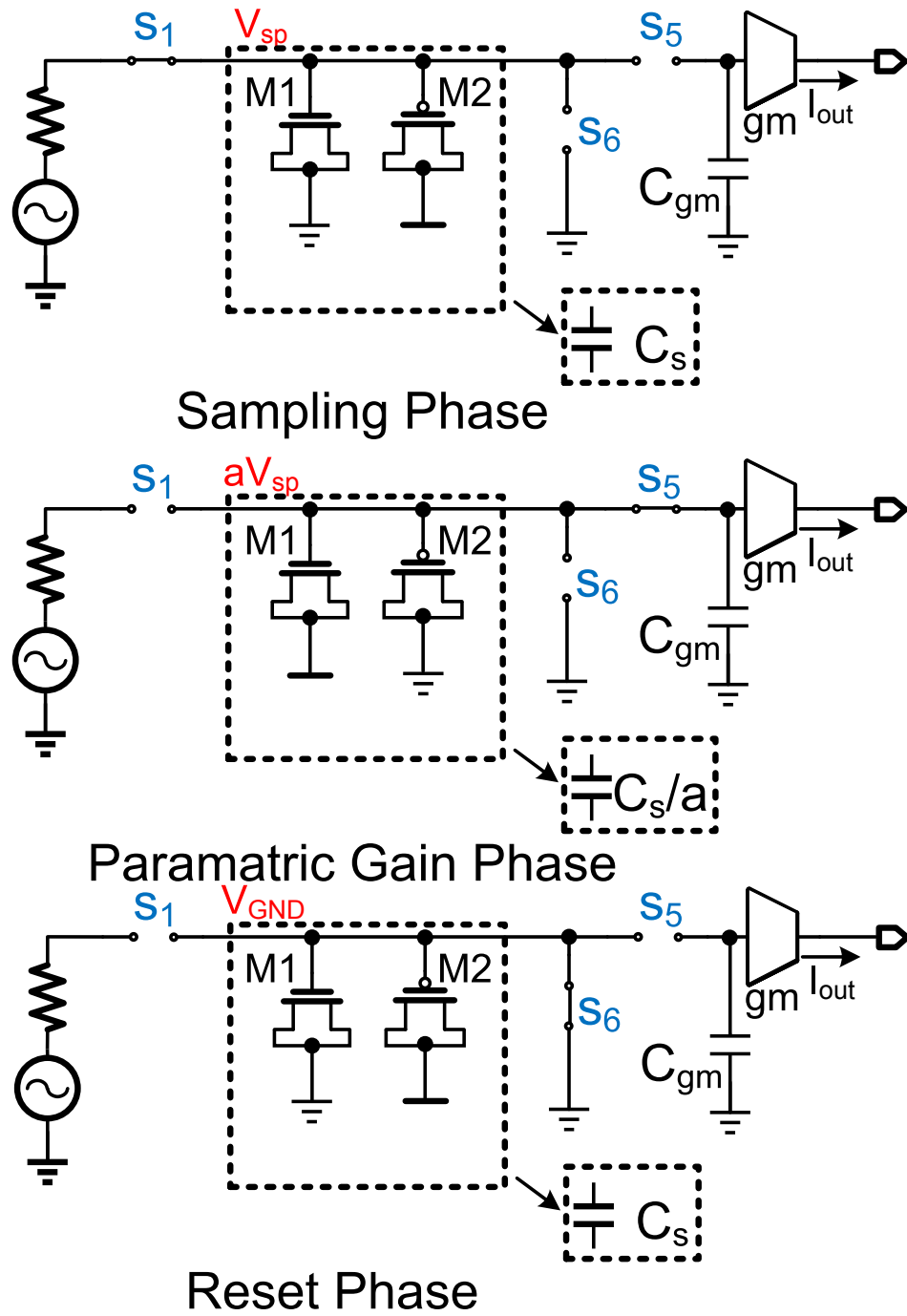


Figure 6.5: Operation of the parametric SCRX.

6.3.1 Noise Analysis

Capacitor stacking and parametric amplification both provide passive gain before the G_m cells to suppress the noise of the succeeding stages. The key difference is that parametric amplification reduces switch s_5 's noise contribution. The source noise after parametric amplification is

$$\overline{V_{R_s,P}^2} = 4kTR_s \left| G \left(\frac{f_s}{8} \right) \right|^2 \cdot a^2 \cdot \Delta f. \quad (6.6)$$

Since the sampling capacitance after capacitor stacking is C_s/a , The s_5 noise is

$$\overline{V_{s_5,P}^2} = \frac{2kT}{C_s f_s} \cdot a \cdot \Delta f, \quad (6.7)$$

and the noise factor due to s_5 is

$$F_{s_5,P} - 1 = \frac{1}{2R_s C_s f_s \left| G \left(\frac{f_s}{8} \right) \right|^2 \cdot a}. \quad (6.8)$$

The dominant noise source, s_5 , is reduced by the parametric amplification, and the noise of the succeeding stages can also be improved. Parametric amplification achieves better noise performance compared with capacitor stacking. However, the MOS capacitor has limited linearity.

6.3.2 Sampling Capacitor Linearization

One of the drawbacks of the parametric amplification is the MOS capacitors' relatively low linearity. For the earlier SCRX (Fig. 6.1) and the capacitor-stacking SCRX (Fig. 6.2), linear MoM and

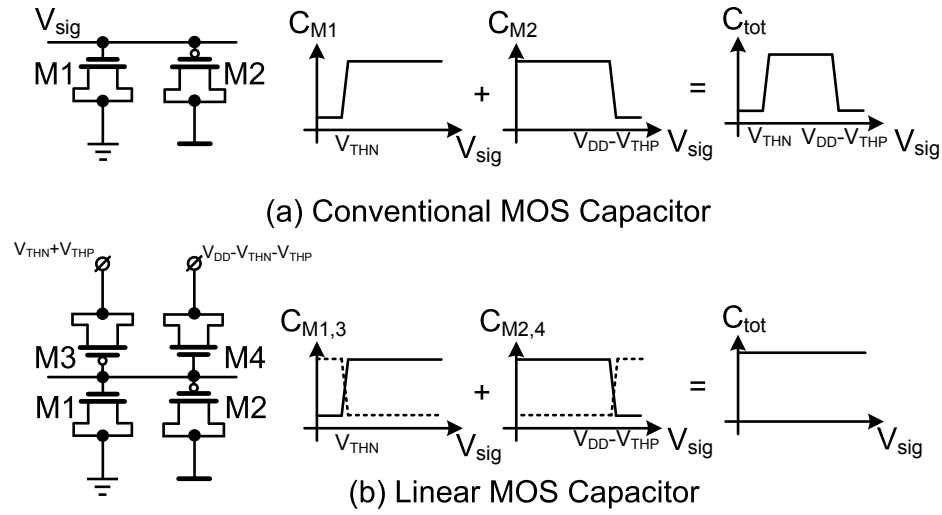
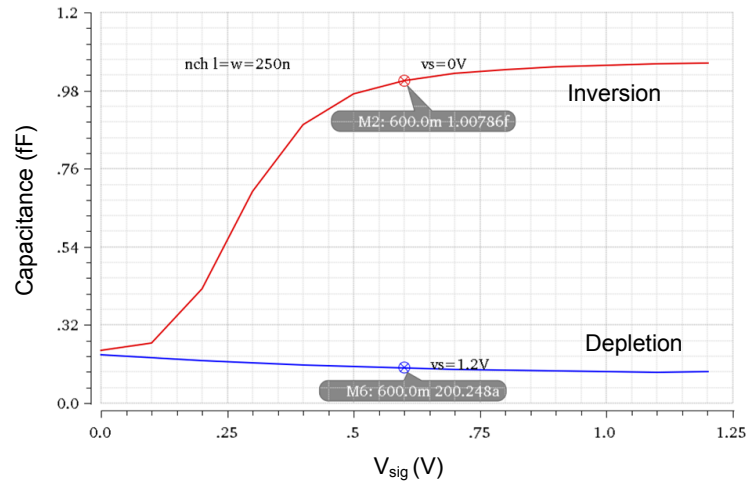
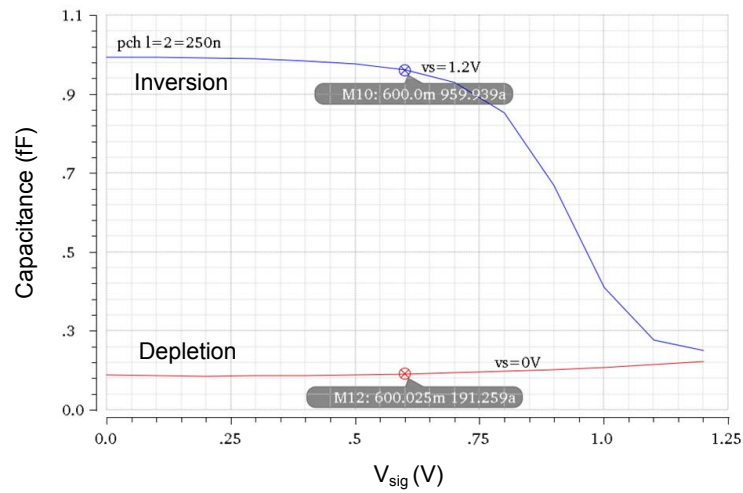


Figure 6.6: Linearization of sampling capacitance in parametric amplification.

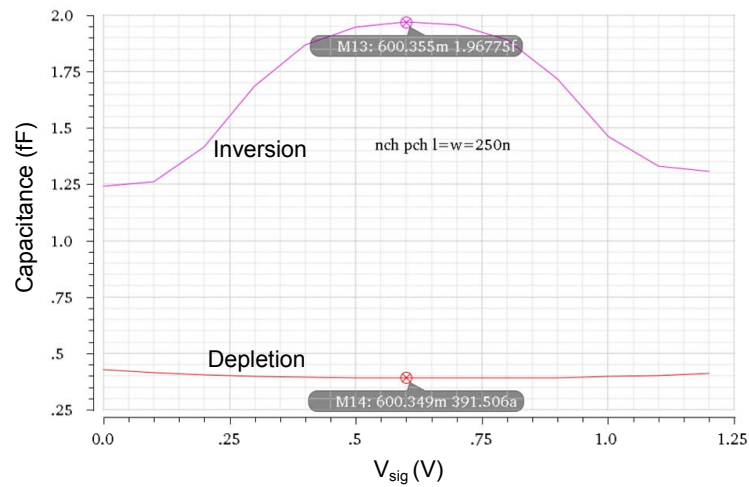
MiM capacitors can be used as sampling capacitors. When using MOS capacitors, the sampling capacitance depends on the signal voltage, as shown in Fig. 6.6. This dependence is because, for a NMOS transistor, if the signal voltage (V_{sig}) is lower than threshold voltage (V_{THN}), the transistor works in depletion mode with a lower capacitance. PMOS capacitors have the same issue. To improve the linearity of the NMOS capacitor, a PMOS M3 is added in parallel with M1. V_{SD} is $V_{THN} + V_{THP}$ to compensate for the nonlinearity of M1 (Fig. 6.6). Also, an NMOS M4 is used to compensate for the nonlinearity of M2. All the source-drain nodes of the NMOS transistors are connected to V_{gnd} and the source-drain nodes of the PMOS transistors are connected to V_{DD} in the parametric-gain phase.



(a)



(b)



(c)

Figure 6.7: Simulated capacitance of (a) NMOS, (b) PMOS, and (c) CMOS capacitors versus input voltage.

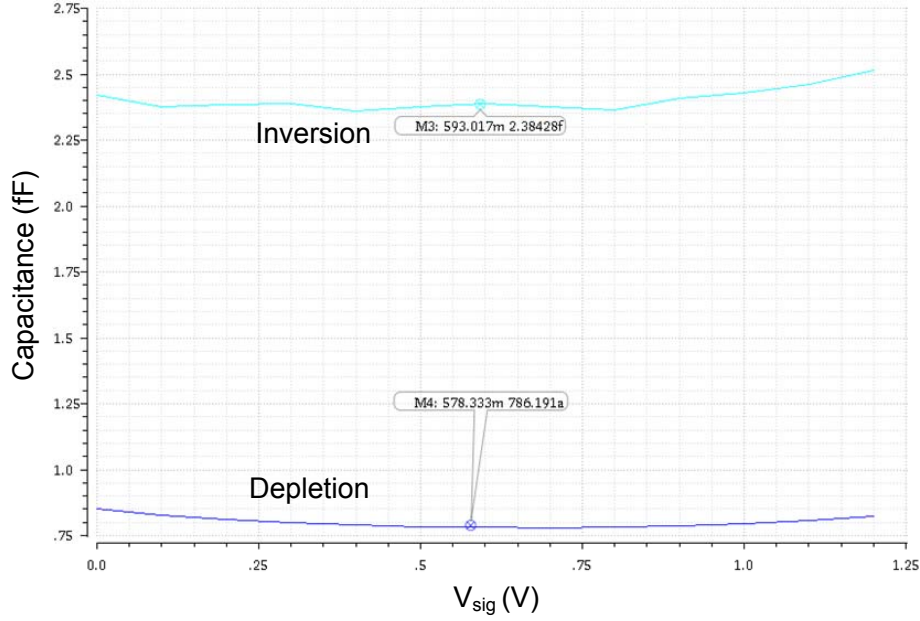


Figure 6.8: Simulated capacitance of the linearized CMOS capacitor versus input voltage.

6.4 Simulation Results

The SCRX with parametric amplification is simulated in 65 nm CMOS process with a supply voltage of 1.2 V. The capacitance of the MOS capacitors (Fig. 6.6(a)) versus input DC voltage V_{sig} is shown in Fig. 6.7. The NMOS and PMOS transistors have the same size of $w, l = 250$ nm. For an NMOS or PMOS capacitor, the capacitance in the depletion region (C_{dep}) is almost constant while the capacitance in the inversion region (C_{inv}) depends strongly on the input DC voltage. Thus, the depletion capacitance of a CMOS capacitor changes little with V_{sig} , but the inversion capacitance is larger when V_{sig} is around $V_{DD}/2$ as shown in Fig. 6.7(c). Since the gain of the parametric amplification is C_{inv}/C_{dep} , the gain of the CMOS capacitor is nonlinear when the input voltage swing is large. For the linearized CMOS capacitor, M3 and M4 (the same size as M1 and M2) are added as shown in Fig. 6.6(b), and V_{SDS} of M3 and M4 are both $V_{DD}/2$ in the inversion region. Compared

Table 6.2: Comparison of SCRX with CMOS capacitor and linearized CMOS capacitor.

	CMOS Capacitor	Linearized CMOS Capacitor
S11 (dB)	−19	−19
Gain (dB)	12	10
NF (dB)	3.7	4.0
IIP3 (dB)	20	22
B1dB (dB)	1.8	5.3
Power (mW)	26	23

with the CMOS capacitor (Fig. 6.7(c)), the C_{inv} of the linearized CMOS capacitor depends less on V_{sig} as shown in Fig. 6.8, but the parametric gain is smaller.

Table 6.2 compares the SCRX with the CMOS capacitor and with the linearized CMOS capacitor. The switches and G_m s are ideal, and the MOS capacitors are implemented by transistors. The LO frequency is 500 MHz. The conversion gain is simulated at the input of the node G_m s. The P-SCRX with the linearized CMOS capacitor provides better linearity but less gain and higher NF.

6.5 Conclusions

In this chapter, we study capacitor stacking and parametric amplification to improve the SCRX noise performance. Capacitor stacking provides passive gain to reduce the noise of succeeding stages. However, it cannot improve the dominant noise source of the SC circuits, which makes this technique inadequate to significantly improve the SCRX noise performance. Parametric amplification reduces the dominant noise source. However, the passive gain is limited by the MOS transistor's $C_{\text{inv}}/C_{\text{dep}}$. Also, the MOS capacitor in the P-SCRX is not as linear as the MoM and MiM capacitors used in the earlier SCRX, which costs it the key advantage of high linearity.

Chapter 7

Conclusions

Dynamic spectrum access provides better spectrum efficiency for wireless communication but requires a wideband receiver. High interferer tolerance with wide tuning range is one of the key challenges for wideband-receiver design. This thesis focuses on improving the performance of passive SC bandpass filters for high interferer tolerance. The passive SC bandpass filters have high selectivity, wide tuning range, and good linearity and benefit from process scaling.

Chapter 3 presents an RF receiver with a harmonic-rejecting N-path filter (HR-NPF). In the conventional N-path filter, the harmonic responses reduce the interferer tolerance at LO harmonics. The HR-NPF achieves tunable narrow band filtering and high attenuation at the third- and fifth-order LO harmonics, resulting in high linearity for a very wide band. With the HR-NPF, a 0.2–1 GHz RF receiver is implemented in a 65 nm CMOS process. The blocker B1dB is -2.4 dBm at a 20 MHz offset, and remains high at the third- and fifth-order LO harmonics. The HR-NPF also offers additional harmonic rejection for the down-conversion. With a baseband harmonic recomb-

nation stage, the two-stage harmonic rejection approach offers a > 51 dB harmonic rejection ratio at the third- and fifth-order LO harmonics without calibration. the LO emission of the receiver is below -90 dBm, thanks to the LNA's reverse isolation.

Chapter 4 focuses on improving the interferer tolerance at close-by frequencies. A high-order passive RF SC filter is presented to achieve rail-to-rail blocker tolerance. The high-order filtering is implemented with N-path and DT IIR filters. RF input-impedance matching and down-conversion are also achieved with passive a SC circuit to make it a fully functional RF receiver front end. The 0.1–0.7 GHz 40 nm CMOS SC receiver (SCRX) consumes 38.5–76.5 mA, achieves 40 dB gain, 24 dBm OB IIP3, 14.7 dBm B1dB for a 30 MHz blocker offset, and a 6.8–9.7 dB noise figure. The key drawback of the SCRX is the relatively high theoretical noise figure lower limit.

Chapters 5 and 6 investigate how to improve the noise performance of the SCRX. The chopping SCRX presented in Chapter 5 improves the noise performance by relocating the key noise source to the active G_m output. The chopping technique eliminates the G_m flicker noise so that a minimum-length G_m can be used for lower parasitic capacitance and smaller G_m size. Blocker detector is integrated with the SC circuit so that the filter order can be adapted to blocker power. The 34–80 mW 65 nm receiver prototype achieves 35 dB gain, 31 dBm OB-IIP3, 15 dBm B1dB, and 4.6–9 dB NF. The 0.2 mW integrated blocker detector detects large OB blockers with a 1 μ s response.

An SCRX with passive gain is studied in Chapter 6. Capacitor stacking can provide signal gain before the active baseband circuits. However, it cannot improve the SCRX NF lower limit. By replacing the sampling capacitor with MOS capacitors, parametric amplification improves the NF lower limit. However, the receiver linearity is limited by the MOS capacitors. Also, signal gain

is limited by the capacitance ratio of the transistor's inversion and depletion modes. These two techniques are therefore not implemented in the prototype IC.

This thesis offers five original contributions:

1. The analysis, design, and implementation of a harmonic-rejecting N-path filter.
2. Design and implementation of high-order SC filtering at RF input to improve receiver OB linearity.
3. Analysis of impedance matching, conversion gain, noise performance, and linearity for the SC receiver.
4. Analysis, design, and implementation of a chopping SC receiver to break the noise limitation of the earlier circuit.
5. Analysis and evaluation of the passive gain of the SC receiver.

Process improvement and circuit innovation are two main engines driving the evolution of RF receivers. The 7 nm CMOS process was on the horizon at the time this thesis was written, while the circuit designers keep pushing receiver performance toward the device physical limits. SC circuits feature high linearity and process scaling. IC designers should keep investigating SC RF techniques in future work:

1. For the receiver with HR-NPF, the noise performance is limited by the partial noise canceling because the noise from the LNA common-gate stage cannot be fully canceled. It can be improved by redesigning the common-gate stage to achieve full noise cancellation.

2. For the SCRX, the in-band linearity is limited by the baseband G_m . This can be improved by linearizing the G_m cells. Linearized G_m can further improve close-by linearity.
3. The SCRX has a very high gain-compression point. However, the blocker noise figure (NF) is limited by the reciprocal mixing as discussed in Chapter 5. Lowering the phase noise of the clock generator reduces the blocker NF; however, the power consumption will be higher. Using better process, a low-noise clock generator might be achievable with reasonable power margin. Phase-noise cancellation techniques [90] can also be considered to cancel the phase noise at baseband to improve the blocker NF.
4. The parasitic capacitor at the RF input and the C_s nodes limit the SCRX frequency range. The parasitic capacitance in parallel with C_s can be improved with better CMOS process because the switches' parasitic capacitance is lower and routing can be shorter due to the smaller switch size. The parasitic capacitance at RF input can also be improved with process scaling since the NFP and sampling switches can be smaller. However, at the RF node, the parasitic may be limited by ESD circuits and bonding pads. An off-chip inductor can be used to improve high-frequency performance.
5. SC circuits can be used as the output stage of a transmitter without PA [48]. The concept of higher order filtering in this work can also be used to achieve better transmitter noise filtering.
6. The passive SC circuits reduce the OB self-interferer tolerance for the receiver in a frequency-division duplex (FDD) system. Replacing the rectangular wave clock signal driving the SC

circuits with a coded clock signal (e.g., pseudo noise code) can achieve self-interferer reduction in a code division duplex (CDD) system [91].

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