Architectures and Circuit Techniques for High-Performance Field-Programmable CMOS Software Defined Radios

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Abstract

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Next-generation wireless communication systems put more stringent performance requirements on the wireless RF receiver circuits. Sensitivity, linearity, bandwidth and power consumption are some of the most important specifications that often face tightly coupled tradeoffs between them. To increase the data throughput, a large number of fragmented spectrums are being introduced to the wireless communication standards. Carrier aggregation technology needs concurrent communication across several non-contiguous frequency bands, which results in a rapidly growing number of band combinations. Supporting all the frequency bands and their aggregation combinations increases the complexity of the RF receivers. Highly flexible software defined radio (SDR) is a promising technology to address these applications scenarios with lower complexity by relaxing the specifications of the RF filters or eliminating them. However, there are still many technology challenges with both the receiver architecture and the circuit implementations. The performance requirements of the receivers can also vary across different application scenario and RF environments. Field-programmable dynamic performance tradeoff can potentially reduce the power consumption of the receiver.

In this dissertation, we address the performance enhancement challenges in the wideband SDRs by innovations at both the circuit building block level and the receiver architecture level. A series of research projects are conducted to push the state-of-the-art performance envelope and add features such as field-programmable performance tradeoff and concurrent reception. The projects originate from the concept of thermal noise canceling techniques and further enhance the RF performance and add features for more capable SDR receivers. Four generations of prototype LNA or receiver chips are designed, and each of them pushes at least one aspect of the RF performance such as bandwidth, linearity, and NF.

A noise-canceling distributed LNA breaks the tradeoff between NF and RF bandwidth by introducing microwave circuit techniques from the distributed amplifiers. The LNA architecture uniquely provides ultra high bandwidth and low NF at low frequencies. A family of field-programmable LNA realized field-programmable performance tradeoff with current-reuse programmable transconductance cells. Interferer-reflecting loops can be applied around the LNAs to improve their input linearity by rejecting the out-of-band interferers with a wideband low input impedance. A low noise transconductance amplifier (LNTA) that operates in class-AB-C is invented to can handle rail-to-rail out-of-band blocker without saturation. Class-AB and class-C transconductors form a composite amplifier to increase the linear range of the input voltage. A new antenna interface named frequency-translational quadrature-hybrid (FTQH) breaks the input impedance matching requirement of the LNAs by introducing quadrature hybrid couplers to the CMOS RFIC design. The FTQH receiver achieves wideband sub-1dB NF and supports scalable massive frequency-agile concurrent reception.

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Chapter 1

Introduction

1.1 Technology Trends of Wireless Communications

The wireless communication technologies have seen rapid growth over the past two decades in terms of the number of devices, the overage of the network, and the quality of the service. In particular, mobile wireless communication systems evolved from the simple radio pagers to the modern broadband 4G LTE cellular networks and will continue to evolve into the next-generation (5G) systems. The data throughput of the networks have grown by several orders of magnitude and the service types have evolved from basic voice and text messages into broadband Internet access and content-rich multimedia applications. These applications further diversify into multiple categories each emphasize different aspects of the wireless link performance (Fig. 1.1). For example, enhanced mobile devices such as next-generation smartphones need higher data throughput for multimedia contents such as file sharing, video streaming, and real-time video chatting. Mission

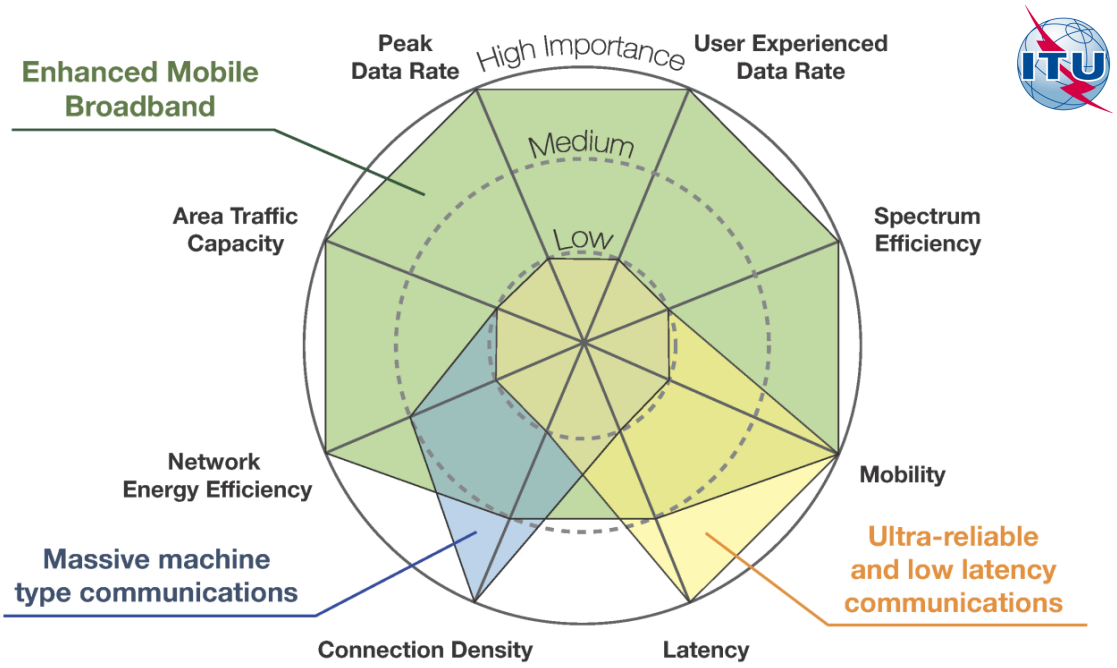


Figure 1.1: 5G capability perspectives from the ITU-R IMT-2020 vision recommendation; different sets of parameters will to be adopted depending on use cases [1].

critical systems, such as those for public safety, autonomous vehicles, and drones, must guarantee ultra-low latency and ultra-high reliability. The machine type communications (also known as the Internet of Things) need to support a massive number of devices with lower power and cost.

To accommodate the proliferation of wireless devices and the ever-increasing data throughput, more RF spectrums are also being introduced, especially for mobile communications. However, due to legacy issues and different regional spectrum allocation policies, the available spectrums are highly fragmented and are not always compatible between geological regions. For example, the frequency bands for mobile communications have increased from the 4 bands in the GSM system to more than 50 bands in the latest LTE standards scattered between 450MHz and 5GHz [3]. On top of the large number of frequency bands, utilizing the fragmented spectrums is also very

challenging in terms of radio implementations. Technologies such as carrier aggregation (CA) are being developed to stitch together multiple segments of contiguous or non-contiguous spectrums to achieve a broader system bandwidth[1]. Furthermore, next-generation flexible spectrum sharing paradigms for both licensed and unlicensed spectrums might allow multi-tier opportunistic spectrum utilization and need flexible cognitive radios (CR) that are able to sense and adapt to the RF environment [4].

These seemingly conflicting requirements impose both great challenges and opportunities for the wireless communication systems. To address these challenges, software defined radios (SDR) are actively researched as promising candidates for the next-generation wireless radios in both the academia and the industry. The original SDR concept [5] proposed to interface the analog to digital converters (ADCs) and digital to analog converters (DACs) directly with the antennas to digitize the entire spectrum of interest. The processing of the information can be performed by software and easily reprogrammed. Such strategies are starting to be adopted in some special application scenarios where either the carrier frequency is very low (AM radios) or the spectrum utilization is relatively predictable and controllable with lower dynamic range requirements (digital cable TV, DOCSIS). However, for other types of wireless communications, especially cellular communication system, over 100dB of dynamic range is often needed at several GHz of carrier frequencies. A single data converter that is able to handle such high dynamic range either has extremely high power consumption or does not exist at all [6]. As a compromise between the power consumption, cost, computation complexity, and flexiblity, practical modern SDRs are typically

[1]Carrier aggregation technologies are discussed with further details in Chapter 6.

implemented with programmable multi-mode multi-band (MMMB) RF front ends and wideband data converters.

1.2 Challenges in Multi-Band Multi-Mode RF Front Ends

Historically, high-performance narrowband receiver front ends often make use of external filters such as band-selection filters, image-reject filters, and intermediate frequency (IF) filters to protect the receiver from out-of-band interferers and to suppress spurious responses. These filters are usually implemented with high quality microwave resonators such as transmission lines and cavities, or with acoustic resonators of surface acoustic wave (SAW), bulk acoustic wave (BAW) or film bulk acoustic resonator (FBAR) technologies. These filters are often bulky, costly and difficult to integrate with CMOS RFICs. Furthermore, they are often not tunable nor programmable in operating frequencies due to technology limitations. To reduce the cost and the form factor of receiver front ends and to improve flexibility at the same time, the off-chip filters should be eliminated as much as possible. The widely adopted zero-IF (direct-conversion) and low-IF receivers eliminate the use of external image-rejection filters and IF filters. Challenges such as IIP_2 and self-mixing DC offsets can now be addressed with digital-assisted calibrations []. The band-selection filters, however, are still critical components to protect the receiver from out-of-band interferers.

Multi-mode multi-band (MMMB) radios often adopt multiple band-selection filters and duplexers to support the different operation modes and different frequency bands. Fig. 1.2 shows a typical block diagram of an RF front end of a modern mobile phone [7] that supports three generations of standards including GSM, WCDMA and LTE. These standards have different frequency

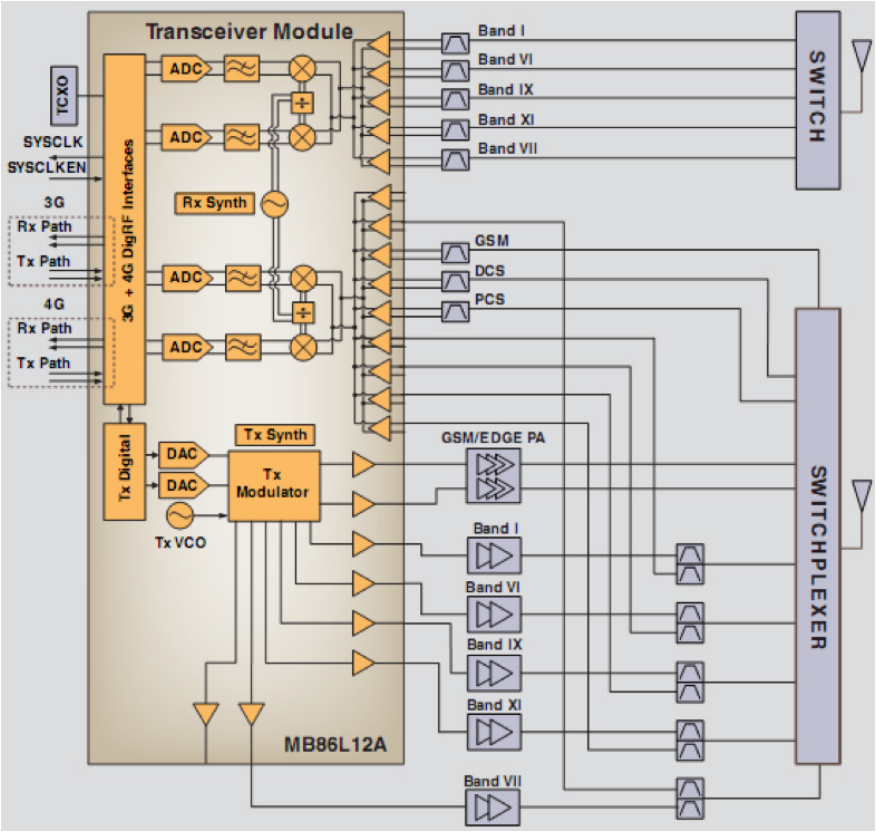


Figure 1.2: The block diagram of a modern multi-mode multi-band RF front end.

bands of operation, duplexing methods, and RF performance requirements such as sensitivity and linearity. In order to meet the stringent RF requirements, a dedicated RF filter is often used for each frequency band. As can be seen in Fig. 1.2, many RF filters and LNAs are connected to the antennas with high-fanout RF switches. With an increasing number of bands and emerging carrier aggregation band combinations [3], the RF front end complexity grows rapidly and it inevitably increases the cost and the form factor of the radio solutions.

Wideband SDR receiver front ends with eliminated RF filters[2] are possible substitutes for the MMMB receivers. However, due to the stringent RF performance requirements, designing wide-band receivers that have comparable performance to the traditional narrow-band receivers still remain one of the major technical challenges.

1.3 Challenges of High-Performance Field-Programmable Wide-band SDR Receivers

1.3.1 Wideband SDR Receivers Need Uncompromised RF Performance

Substituting the traditional narrow-band receivers with field-programmable wideband receivers is very challenging due to the absence of the band-selection RF filters. The performance of the wideband receiver must be significantly enhanced to match that of the narrow band receivers.

Wideband LNAs, such as the common-gate LNAs and the resistive feedback LNAs, typically have higher NFs than the narrowband inductively degenerated LNAs. The requirement of main-

[2]Such receivers are referred to as SAW-less receivers in the rest of the dissertation.

taining a matched input impedance often conflicts with the effort of reducing the NF with more power consumption[3].

Wideband receivers and LNAs need to have higher out-of-band blocker and interferer tolerance without the protection of the RF filters. The out-of-band blocking mask specifications vary across different wireless standards. For example, the wideband LTE receivers need to handle at least -15dBm out-of-band blockers, the GSM receivers need to tolerate 0dBm blockers, and co-located base stations, in the worse scenarios, can suffer from blocker levels as high as +10dBm [3]. Large out-of-band blockers can cause gain compression due to the nonlinearities in the signal path of the receiver. The linearity problems are especially prominent for wideband LNAs as they often apply significant voltage gains to reduce the NF of the LNAs and to suppress the noise contributions of the successive stages in the signal chain. However, undiscriminated amplification of the desired signal and the interferers without filtering can desensitize the receiver through various distortion mechanisms.

Without the band-selection filters, the wideband SDR receiver is also suspect to interferers across a very wide frequency range. Mixers in the SDR receiver can pickup spurious interferers at harmonics of the local oscillator (LO) frequency and corrupts the desired in-band signals. Thus, wideband receivers need harmonic-rejecting techniques such as harmonic rejecting mixers (HRM) or programmable RF anti-aliasing filters.

Finally, reciprocal mixing can be a very challenging issue in wideband SDR receivers [8]. Reciprocal mixing is caused by the mixing of out-of-band interferers and the phase noise of the local oscillator (LO) signals at the corresponding offset frequencies. The mixing corrupts the in-

[3]This will be discussed in more details in Chapter 2.

band desired signal with an additive noise proportional to the amplitude of the interferer. Thus, the LO signals need to have lower phase noise comparing to the narrow band receivers.

1.3.2 SDR Receivers Need Programmability for Dynamic Performance Trade-off

As Discussed above, achieving uncompromised RF performance with wideband SDR receivers is a very challenging circuit design task. A multi-mode SDR receiver is often deployed to cover several different standards, and it needs to meet the most stringent RF requirements among all the supported standards.

A fixed SDR receiver that is designed to address the performance requirements of the worst-case operation scenario often have penalties in some other aspects, usually in the power consumption. For instance, receiver NF improvement is usually directly associated with an increased power; linearity enhancement circuits can consume additional power. Apart from the power penalty, linearity enhancement techniques often incur NF panelty on the receiver.

However, not all the standards have equally stringent performance requirements. For example, GSM handset receivers need to tolerate larger out-of-band blocker than the UMTS and LTE receivers, but the UMTS and LTE receivers have higher sensitivity requirements even they have larger carrier bandwidth. Other short-range broadband wireless standards such Bluetooth and 802.11 have large carrier bandwidth but relatively relaxed requirements on sensitivity. Even within the one standard, the RF performance requirements can vary depending on the operation scenarios and the RF environments. Shown in Fig. 1.3 are the transmit power statistics of UMTS mobile

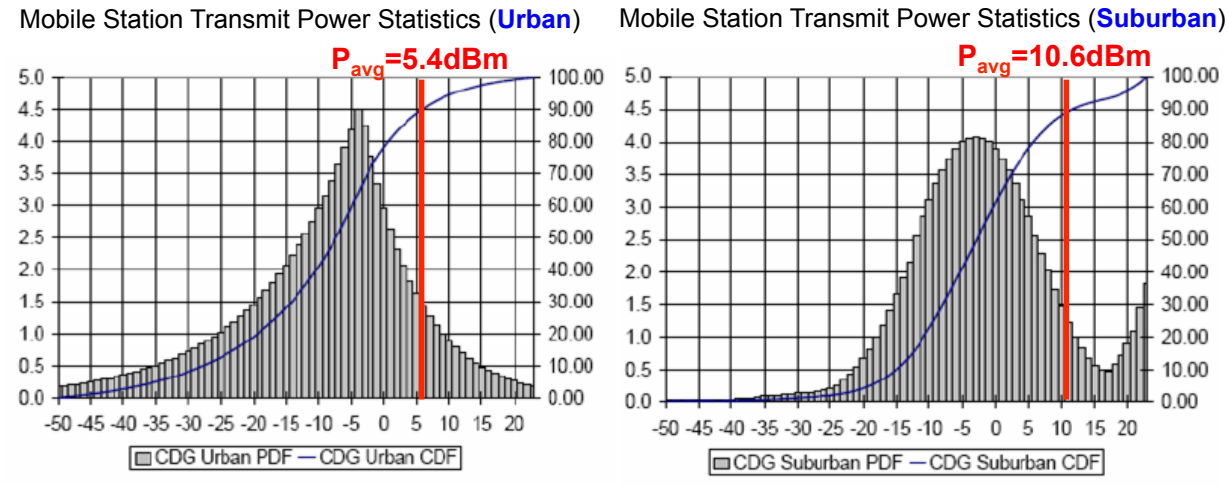


Figure 1.3: Statistic distributions of the UMTS mobile station (handset) transmit power under different depolyment scenarios.

handsets in the urban and the suburban areas. Suburban deployments have significantly more probability to transmit at its maximum power for an extreme coverage reach. The average transmit power in the suburban area is 10.6dBm comparing to the 5.4dBm in the urban area. Thus, in situations where the handset is close to the basestation with favorable channel conditions, both the transmitter power and receiver sensitivity can be relaxed to save power consumption. The presence of the blocker signals also depends on the proximity of the handset to the source of the interferer and its transmit behaviors. Thus, flexible and field-programmable RF circuits are desirable building blocks for SDR receivers. The performance of the receiver, such as the linearity, NF and power consumption, can be dynamically traded off depending on the operation scenario and RF environments to optimize power consumption of the receiver.

Though an attractive concept, field-programmable RF circuits are not easy to design. Many of the circuit parameters are strongly coupled with each other, and independent adjustments of each performance aspect are not always possible. Also, adding programmability to the circuits can intro-

duce additional parasitic resistance and capacitance, which can degrade the receiver and LNA performance such as the bandwidth and NF. With the deeply scaled CMOS transistors, low-parasitic RF switches are becoming feasible and create new opportunities for wideband programmable RF circuits implementations.

1.4 CMOS Technology Scaling Enables New RF Techniques

Traditional RF and microwave circuit designs often work with discrete and distributed components that are integrated on printed circuit boards (PCB). As the dimensions of the circuits and interconnections are comparable to the wavelength of the signals, distributed element models are used. Signals are represented as power or voltage waves and maximum RF power transfer is often desired due to the difficulty of obtaining RF gains from low f_T devices. The 50Ω system impedance convention is widely adopted to facilitate the integration of different components such as antennas, filters, amplifiers and mixers.

The development of modern CMOS RFIC shifts drastically from the traditional RF design paradigm. Thanks to the technology scaling, modern CMOS devices have very high speed and yet can be manufactured with very low cost and profile. CMOS RFICs are able to integrate most of the transceiver circuits onto a monolithic substrate. At this scale, the dimensions of the devices and interconnections are reduced from centimeters to micrometers, which is now much shorter than the signal wavelength of the low-GHz signals. As a result, signal representations shift from waves to currents and voltages, maximum power transfer becomes less critical, and the 50Ω convention is no longer followed for the on-chip interconnections and interfaces.

Modern commercial wireless radios are often integrated into a system-on-chip (SoC) platform with massive digital signal processing (DSP) circuit and microprocessors. In these SoC implementations, highly scaled CMOS technologies are often favored for the intensive digital circuits. The availability of of these fast devices dramatically changes the fashion of RF circuit design.

Traditional analog circuit techniques are being introduced into the low-GHz RF circuit designs. The lower parasitic capacitance of the scaled CMOS devices makes the implementation of inductorless wideband RF circuits possible. Traditionally, inductively source-degenerated LNAs are the dominating topology for integrated CMOS LNAs, and a classical implementation can use up to three inductors. The LNA is narrow band and and can hardly be tuned across different operating frequencies. Recently, wideband inductorless LNAs using resistive feedback, g_m boosting, and noise canceling techniques become increasingly popular. Linearization techniques such as feedback and resistive degeneration are not uncommon for wideband RF receivers.

However, the lower breakdown voltage of scaled CMOS transistors eats into the voltage headroom of the RF circuits. In conventional voltage-mode LNAs, the out-of-band interferers are also amplified and the low output voltage headroom limits the linearity of the LNAs. This becomes a more challenging problem with the low power supply voltage of the scaled technology. One possible solution is to operate the LNA at a higher supply voltage and carefully bias the circuits for reliable operations and a startup [9]. Another solution is to process the received signals in the current domain with low noise transconductance amplifiers (LNTA) and avoid voltage gain before filtering. These LNTAs can be co-designed with the current driven passive mixers as current sink loads. Receivers using such circuit topologies have demonstrated higher than 0dBm out-of-band

blocker tolerance [10]. Inverter-based RF and baseband circuits are also becoming more popular due to the lower power supply voltage [11]. They are starting to be used as compact yet power efficient transconductors.

CMOS transistors are being extensively used as switches in the RF circuits. In older technologies, the device parasitic capacitance often loads the circuits significantly and incur a large penalty on the circuit bandwidth. With scaled transistors, low-resistance switches can be easily implemented with much lower parasitics. Programmable circuits building blocks such as programmable LNAs can have multiple sliced unit circuits and digitally controlled configuration switches. High-speed switches are also used in the multi-phase harmonic-rejection passive mixers for frequency conversion and in the high-Q N-path filters whose center frequency can be conveniently set by its clock frequency.

Although most parts of a receiver front end can now be integrated into a single CMOS RFIC, the antenna interface still has to follows the 50Ω system impedance convention due to the distributed nature of the antennas and their feed lines. In situations where band-selection filters are needed, the 50Ω interface is also necessary to maintain the transfer function and the specifications of the RF filters. This input impedance matching requirement is one of biggest constraints on the LNA and receiver design. We address the antenna interface challenge with multiple research projects conducted in the scope of this dissertation.

1.5 Pushing for High-Performance Field-Programmable SDR Receivers

The objectives of this dissertation are to invent and investigate new SDR receivers architectures and circuit building blocks for the next generation wireless communication systems. The conducted research strives to advance SDR receivers technologies in three aspects: pushing the state-of-the-art performance through circuit and radio architecture innovations, adding new features such as concurrent reception, and introducing field programmability for dynamic performance tradeoff and power optimization.

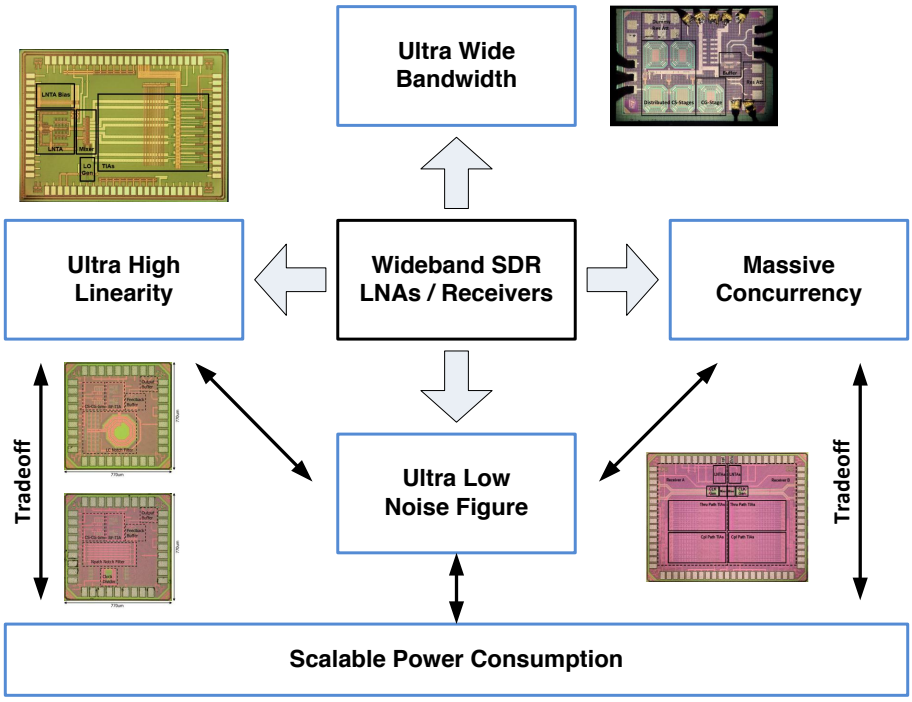


Figure 1.4: Performance enhancements to the wideband SDR receivers and the field-programmable dynamic performance tradeoffs, annotated with prototype chips covered in this dissertation.

Fig. 1.4 illustrates the key research directions to push the performance and features of the SDR receivers and the dynamic tradeoffs between different performance aspects. The aims are to push for ultra high linearity, ultra low noise figure, ultra wide bandwidth and massive concurrent reception. Shown in double arrows are the relationships between the performance aspects and features that can be dynamically traded off.

Thermal noise canceling is a family of circuit techniques that are suitable for wideband antenna interfaces. The noise canceling techniques can maintain a wideband RF input impedance matching and achieve a low NF at the same time. In Chapter 2, we review the principle of the noise canceling techniques, the existing circuit architectures, and their limitations and challenges.

In this dissertation, innovations at both the circuit and the receiver architecture level push the capabilities of noise canceling techniques. Several modifications to the core idea of noise cancellation are made to break the performance bottlenecks and fundamental tradeoffs. As a result, we can enhance the RF performance and incorporate field programmability into the receivers. Research conducted in these directions leads to four independent tapeouts of proof-of-principle CMOS LNA and receiver chips for technology validation.

Pushing a wideband LNA antenna interface to the multi-GHz range while maintaining a low NF across the whole operating frequency range is very challenging. Using larger devices for a lower NF introduces more parasitic capacitance and inevitably reduces the RF bandwidth. Thus, a tradeoff between the NF and the bandwidth must be made. We combine the architecture of the common-source common-gate noise-canceling LNA with the distributed amplifier to uniquely break this tradeoff. A CMOS noise canceling distributed LNA designed in 65nm CMOS technol-

ogy is demonstrated in Chapter 3. The LNA operates from DC up to 9.5GHz and still maintains a low noise figure at low frequencies.

To push the input linearity of the LNAs and introduce field programmability, a family of LNAs with interferer-reflecting loops (IR-Loop) was designed. IR-Loop is a technology that applies frequency-selective feedback loops around wideband LNAs to reduce the out-of-band input impedance and to suppress the input voltage swing created by the blockers. Notch filters tuned to the operation frequency create selectivity in the feedback loop. The filters can be implemented with on-chip inductors and capacitors, bondwire inductors and on-chip capacitors, or switched-capacitor N-path notch filters. Current-reuse CS and CG LNA cores are designed with programability in the gain, NF, linearity and power consumption for dynamic power optimization. Two prototype chips are designed and fabricated with a 65nm CMOS technology. Different filter technologies are used and two different packaging configurations are used to program the bondwire inductance during packaging time. Chapter 4 discusses the analysis, design and validation of the IR-LNAs in details.

The input linearity of an SDR receiver can be further pushed with the use of low noise transconductance amplifiers (LNTA) and current-mode passive mixers. Chapter 5 introduces the field-programmable LNTAs with ultra-high linearity. The innovative class-AB-C LNTAs use class-AB and class-C cells to complement and extend their linear operation range. The biasing circuits maintain the linearity performance robustly across PVT variations. When connected to a noise canceling receiver, the class-AB-C LNTAs can tolerate a maximum out-of-band B_{1dB} of +11dBm in the best case, which corresponds to a 2.24V peak-peak voltage swing at the input of the receiver

without any RF filtering. In addition to the ultra-high linearity, the full receiver can be programmed in different modes of operation to dynamically trade off the NF, linearity and power consumption.

To realize a sub-1dB NF and enable massive concurrent reception, we invented the frequency-translational quadrature-hybrid (FTQH) technique. By combining quadrature hybrid couplers with RFICs, the FTQH architecture breaks the tradeoff between the receiver input impedance matching requirements and the actual input impedance used by the LNAs or LNTAs. The freedom to use an arbitrary input impedance opens up many opportunities to minimize the NF and to support massive concurrency. In chapter 6 we discuss the operation principle of the FTQH technique and its circuit implementation to achieve an ultra-low NF and massively scalable concurrency from a single wideband antenna. A 65nm CMOS prototype chip is demonstrated with a sub-1dB minimum NF for signle-channel operation and up to 4 channel concurrent reception between 600MHz and 2.1GHz.

Chapter 7 summarizes this dissertation and provides avenues for future work and potential improvements.

Chapter 2

Review of Noise Cancelling Techniques for Wideband SDR Antenna Interface

2.1 Impedance Matching Requirements of Receiver Antenna Interfaces

Traditional RF and microwave circuit often use a 50Ω system impedance to interface various building blocks. These designs work with discrete components that are either interconnected with RF cable assemblies or integrated onto a single RF PCB. The dimensions of the components and interconnections are comparable to the wavelength of the signals, and the analysis and design of such RF circuits often use distributed element models and S-parameters. Signals are typically represented as voltage or power waves normalized to a system impedance, which facilitates the integration of cables and separately designed components such as antennas, filters, couplers, amplifiers,

and mixers. The 50Ω system impedance is a commonly accepted convention as a compromise between loss and power handling.

The modern CMOS RFIC design makes a drastic shift in the analysis and design methodologies. Thanks to CMOS technology scaling and fast devices with an f_T exceeding 200GHz, RFICs can integrate most of the active circuits onto a single substrate. The dimensions of the devices and interconnections decrease to micrometers and are much shorter than the signal wavelength at several GHz. As a result, signals can now be presented as currents and voltages, and lumped element models can be used. With the ability to co-design all the active circuits, on-chip RF circuit interfaces no longer follow the 50Ω convention.

Even with highly integrated receivers, the antenna interface still needs to follow the 50Ω system impedance convention due to the separately designed antennas and their distributed feed lines. Also, band-selection filters need terminated 50Ω interface at all the ports to maintain their transfer functions and specifications.

2.2 Noise Scaling in Analog Amplifiers

In traditional analog circuit designs, there is often a strong tradeoff between the noise performance and the power consumption of a circuit. For example, considering an analog amplifier shown in Fig. 2.1(a), the voltage-mode amplifier is driven with a input voltage signal composed of the desired signal V_s and its noise $\overline{V_{n,s}^2}$. The noise of the amplifier can be represented as an equivalent input referred noise voltage $\overline{V_{n1}^2}$. One of the possible implementations of the amplifier is a simple common-source MOSFET with a transconductance g_m driving a resistive load R_L. The noise factor

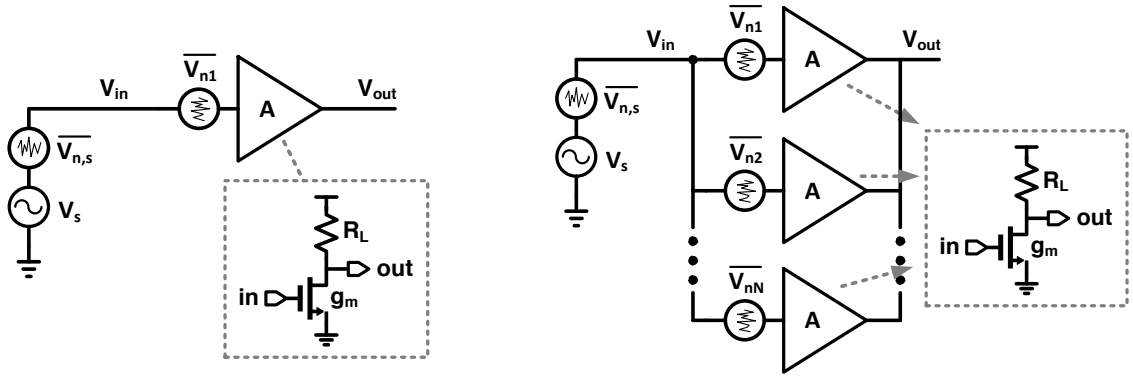
of the circuit shown in Fig. 2.1(a) is:

$$F = \frac{A^2\overline{V_{n,s}^2} + A^2\overline{V_{n1}^2}}{A^2\overline{V_{n,s}^2}} = 1 + \frac{\overline{V_{n1}^2}}{\overline{V_{n,s}^2}} \tag{2.1}$$

When multiple such amplifiers are put in parallel, the overall equivalent input and output impedances both become N times lower and the voltage gain of each amplifier slice is reduced by N times. As the signal and the noise from the source are amplified coherently by each amplifier slice, they add up in magnitude at the output and the voltage gain from V_{in} to V_{out} stays the same as a single amplifier slice. The noise contributions from the amplifier slices, however, are often independent with each other. Assuming that they are independent Gaussian white noise sources, the noise components add up in power at the output instead of in magnitude. The noise factor can now be calculated as:

$$F_{scaled} = \frac{(NA)^2\frac{\overline{V_{n,s}^2}}{N^2} + \sum_{i=1}^{N}\frac{\overline{V_{n,i}^2}}{N^2}}{(NA)^2\frac{\overline{V_{n,s}^2}}{N^2}} = 1 + \frac{\overline{V_{n1}^2}}{N \times \overline{V_{n,s}^2}} \tag{2.2}$$

It can be observed that the noise factor of the amplifier can be improved by scaling up the circuit at the cost of an N times larger power consumption and device area. The gain, linearity and bandwidth do not change with such scaling, but both the input and output impedances become smaller. Such impedance change is usually not critical for low-frequency analog circuits as they often have high-impedance MOSFET gates at their inputs and the input impedance is largely capacitive. Scaling up the circuits simply presents more load capacitance to the previous stage and may reduce the analog bandwidth of the signal chain. In the case of RF LNAs, however, noise scaling cannot be easily achieved by simply putting more LNA circuits in parallel. The RF interface of the LNA



(a) (b)

Figure 2.1: Noise scaling of an analog amplifier: (a) a unit voltage-mode amplifier (b) improving the SNR with noise scaling at the cost of multiple devices and a higher power consumption.

often requires a 50Ω matched impedance, but the direct noise scaling method is not able to keep the input impedance constant.

2.3 Thermal Noise Cancelling Techniques

Thermal noise cancelling is a family of circuit techniques that breaks the tradeoff between the input impedance matching requirement and the noise scaling techniques. The key idea behind the techniques is to measure the thermal noise created by the input matching circuit and to subtract it from the desired signals to mitigate its noise contribution. A conceptual block diagram of the noise cancelling RF interface is shown in Fig. 2.2. In order to separate the signal from the source (denoted by s) and the noise from the matching circuit (denoted by n), two separate low-noise measurements (denoted by m_1 and m_2) need to be performed around the matching circuit. Assuming that the noise contributions from the matching circuits to the two measurements are fully correlated,

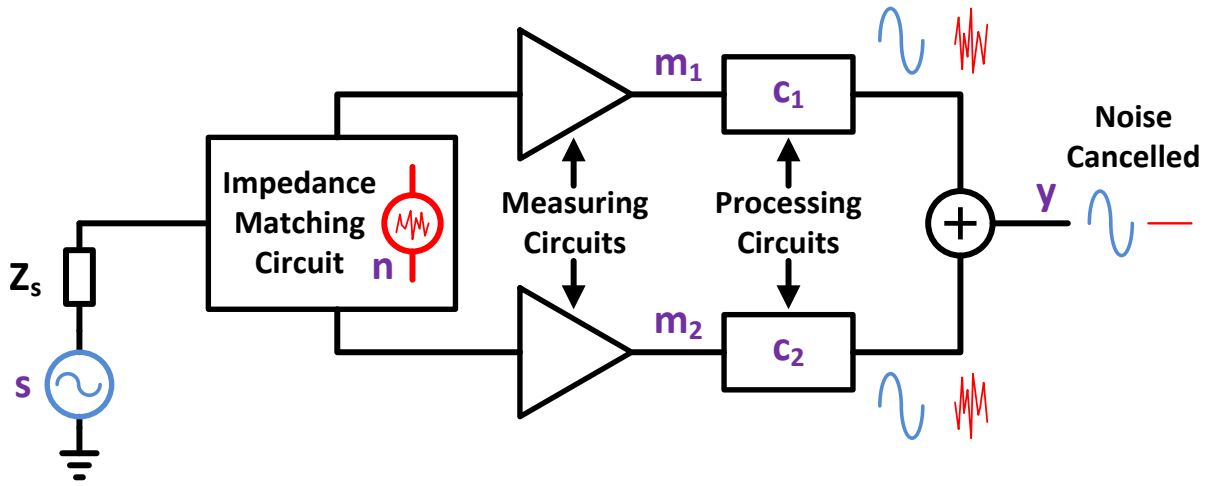


Figure 2.2: Conceptual block diagram of a noise-cancelling RF interface.

the two measurements can be described mathematically with the following matrix equation:

$$\begin{bmatrix} m_1 \\ m_2 \end{bmatrix} = \begin{bmatrix} k_{11} & k_{12} \\ k_{21} & k_{22} \end{bmatrix} \begin{bmatrix} s \\ n \end{bmatrix} + \begin{bmatrix} n_1 \\ n_2 \end{bmatrix} \tag{2.3}$$

The matrix K denotes the transfer coefficients from s and n to m_1 and m_2. n_1 and n_2 denotes the additive noise introduced by the two measurement circuits.

The two measurements are further processed with two coefficients c_1 and c_2 and summed as the final output y.

$$y = \begin{bmatrix} c_1 & c_2 \end{bmatrix} \begin{bmatrix} m_1 \\ m_2 \end{bmatrix} = \begin{bmatrix} c_1 & c_2 \end{bmatrix} \begin{bmatrix} k_{11} & k_{12} \\ k_{21} & k_{22} \end{bmatrix} \begin{bmatrix} s \\ n \end{bmatrix} + \begin{bmatrix} c_1 & c_2 \end{bmatrix} \begin{bmatrix} n_1 \\ n_2 \end{bmatrix} \tag{2.4}$$

If we can design the matrix C and K to satisfy the criteria such that:

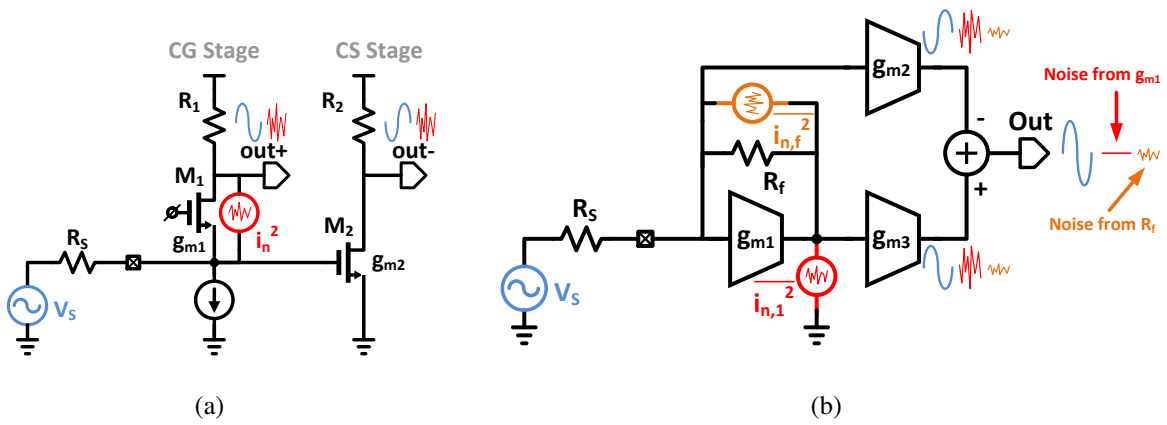
$$\begin{bmatrix} c_1 & c_2 \end{bmatrix} \begin{bmatrix} k_{11} & k_{12} \\ k_{21} & k_{22} \end{bmatrix} = \begin{bmatrix} a_1 & 0 \end{bmatrix} \tag{2.5}$$

The final out now becomes:

$$y = a_1 s + c_1 n_1 + c_2 n_2 \tag{2.6}$$

The contribution from the matching circuit (n) is completely cancelled out at the final output. The signal from the source is amplified by a gain of a_1 and the noise from the matching circuits is completely cancelled. The only noise contributions now comes from the two measurement circuits. If we can apply noise scaling to these measurement circuits, then the overall noise figure can be reduced by increasing the power consumption.

Notice that the variables used in the above analysis are all abstract and in practical implementations can be mapped to physical parameters such as voltage, current or even guided waves. c_1 and c_2 are also generalized gains that can be either real coefficients for broadband real signals, complex coefficients for band-limited signals, or even complex conversion gains across different frequency domains.



(a) (b)

Figure 2.3: The operation principle of two example wideband noise canceling LNAs: (a) a CS-CG noise canceling LNA; (b) a noise canceling LNA with a resistive feedback matching circuit.

2.4 Practical Implementations of Noise-Canceling LNAs and Receivers

Since the invention of the initial noise cancelling technique, many noise cancelling topologies have been explored by both the academia and the industry [12]. In this section, we discuss several suitable architectures for practical implementations. The input impedance matching circuit can have different topologies and there are different implementations of the low-noise measuring circuits and the combination circuits. Furthermore, the combination can be done at different signal domains such as voltages and currents, and across the same or different frequencies.

Fig. 2.3(a) shows a simple common-source common-gate (CG) noise canceling LNA [13]. The transconductance of the CG transistor M_1 (g_{m1}) is $20mS$ and provides a wideband input impedance of 50Ω. It also converts the voltage signal at the input into a current signal as the first measurement. The CS transistor has a transconductance of g_{m2}. It takes the voltage signal at the input node and also converts it into a current signal as the second measurement. The CG stage has a non-inverting

voltage gain and the CS stage has an inverting voltage gain for the signal from the input. The channel thermal noise from the CG stage (M_1), however, propogate to the CS and CG output current with the same polarity. By scaling the two load resistors (R_1 and R_2) properly, the two measured signal currents are converted into voltages, with the signal from the source appearing in the differential mode and the thermal noise from M_1 appearing in the common mode. If the next stage takes the output signal from the LNA differentially, the noise from the termination resistor is cancelled. Thus, the CS-CG noise canceling LNA provides wideband input impedance matching, noise cancellation and single-ended to differential conversion (balun) at the same time. As discussed in Section 2.3, after the noise from the termination circuit is cancelled, the NF is limited by the excess noise from the measurement circuits. In this particular case, the excess noise from the CS stage can be reduced with the noise scaling at a cost of increased power consumption (Section 2.2). The excess noise from the CG load resistor (R_1) is not cancelled and can only be reduced by increasing the value of the resistor. As g_{m1} is fixed due to the input matching requirement, R_1 is directly proportional to the voltage gain of the LNA. In the absence of RF filtering, R_1 cannot be increased without degrading the linearity of the LNA.

Another common implementation of the noise cancelling LNA is to use a resistive feedback stage as the input impedance matching circuit (shown in Fig. 2.3(b)) [12, 14]. The impedance matching is achieved by designing the feedback amplifier with a transconductance of $g_{m1} = 1/R_s$. The noise contribution of the transconductor can be modeled as a shunt current source ($\overline{i_{n,1}^2}$) from its output to the ground. The noise current flows through R_f and R_s and creates noise voltages at the input and output nodes of the matching amplifier with the same polarity. The signal from the

source (V_s), on the other hand, creates signal voltages at these two nodes with opposite polarities. The voltages on these nodes can be sensed and combined with properly weighted transconductors (g_{m2} and g_{m3}) and summed with opposite polarity to cancel the noise contribution of the matching amplifier. However, the noise contribution of R_f ($\overline{i^2_{n,f}}$) cannot be modeled in the same way as $\overline{i^2_{n,1}}$ and cannot be canceled. Increasing R_f can improve the minimum achievable NF and increase the voltage gain at a cost of the linearity of the LNA. The two sensed voltages can be combined either in voltage domain or in current domain. The current domain operation facilitates the use of current-driven passive mixers for their higher blocker handling capabilities. However, the matching amplifier still have a wideband voltage gain and has limited out-of-band linearity.

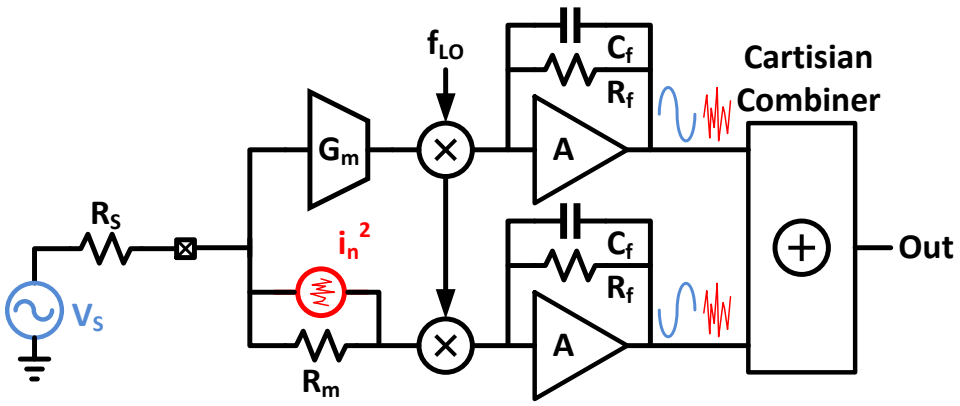


Figure 2.4: Operation principle of the frequency-translational noise-canceling (FTNC) receiver.

Both the noise canceling LNAs shown in Fig. 2.3 have wideband RF voltage gains and have limited blocker tolerance without RF filters. The NF of these LNAs are also tied to their voltage gains and impose a linearity-NF tradeoff. Furthermore, as the combining circuits have fixed real weights, an antenna impedance that deviates from 50Ω in both magnitude and phase can have negative impacts on the NF of the LNAs.

The frequency-translational noise-canceling (FTNC) receiver [10] addressed these challenges by inserting frequency downconverters between the two low-noise RF signal measurements and the noise-canceling combining circuits. Shown in Fig 2.4 is a simplified block diagram of an FTNC receiver. The input impedance matching is achieved with a matching resistor (R_m) together with the low input impedance of the passive mixer. The noise current generated by R_m generates a noise voltage at the input node and also flows through the main passive mixer and is downconverted to the I-Q baseband, which makes the first low noise measurement. A common-source transconductor (G_m) measures the voltage at the RF input node, converts it into a current signal, and downconverts it to the I-Q baseband with the auxiliary downconverter. With an ideal source impedance of 50Ω, the signal from the source appear at the main and auxiliary I-Q basebands out of phase and the noise from R_m appears at the two I-Q basebands in phase. A Cartesian combiner with complex weights can be used to sum the two complex baseband signals and to cancel the noise from R_m.

The FTNC technique has several benefits comparing to the wideband NC LNAs. First, no wideband voltage gains are applied to the RF input signals. RF signals are processed in current domain and are only converted to voltages after baseband filtering. Second, relatively higher load impedances can be used for lower NF. Similar to R_1 in Fig. 2.3(a), R_{f1} in Fig. 2.4 contributes thermal noise that cannot be cancelled and limits the minimum achievable NF of the receiver. With the filtering of the baseband transimpedance amplifiers (TIA), higher baseband load resistors can be used to achieve conversion gains in the range of 40 to 50dB instead of a typical RF voltage gain of 15 to 25dB in the wideband NC LNAs. Third, the complex signal combining at the I-Q basebands improves robustness of the noise canceling when the source impedance deviates from the 50Ω

system impedance. By injecting a test signal from the main path and nulling it at the combiner output, the noise canceling coefficients can be optimized. With these advantages, FTNC receiver architecture is able to achieve sub 2dB wideband NF and tolerate 0dBm out-of-band blocker at the same time.

2.5 Limitations and Further Improvements of Noise Canceling Techniques

Noise canceling technique is a very promising circuit technique for wideband SDR receiver implementations. However, it still has several performance limitations and needs further improvements. This dissertation pushes these limitations by breaking the tradeoff and constraints with circuit innovations.

Wideband noise canceling LNAs have tradeoffs between the NF and the RF bandwidth. As discussed earlier, noise canceling technique can eliminate the noise contribution from the impedance matching circuit and achieve a low NF by scaling up the low noise sensing circuits. Such noise scaling not only increases power consumption of the receiver, but also introduces more parasitic capacitance to the antenna interface and limits the maximum operation frequency of the receiver. This tradeoff between the NF and the RF bandwidth can be broken by combining the noise canceling techniques with microwave circuit techniques such as the distributed amplifier [15]. Chapter 3 will discuss this topic in more details.

Noise canceling techniques need low-noise high-linearity RF signal sensing circuit. The

FTNC receiver architecture have shown that the bottleneck of the linearity of the receiver is the auxiliary low-noise sensing circuits for the noise cancellation. Specifically, low noise transconductance amplifiers (LNTAs) are desired for their high-linearity current-mode operation. Chapter 5 discusses the design and implementation of ultra-high-linearity LNTAs that are resilient to rail-to-rail blockers.

New topologies are needed for the impedance matching circuits. Most of the practical implementations of the noise canceling antenna interface synthesize the 50Ω input impedance with analog techniques. In most of the cases, the two low-noise measurement circuits have different implementations and are intrinsically asymmetric.

The measurement with a lower gain often limits the minimum achievable NF. For example, in the CS-CG NC LNA, the CG stage has only a unit current gain and limits the NF of the LNA. New impedance matching circuits can be realized with distributed microwave components. Quadrature hybrid couplers is a widely used microwave component that is able to achieve input impedance matching and enable two symmetric low noise measurements such as the case in the balanced amplifier [15]. This technique is discussed in Chapter 6 as the frequency-translational quadrature hybrid (FTQH) receivers.

CMOS noise canceling receivers need ultra-low NF comparable to that of the III-V compound devices. An ultra-low NF is always desired in wireless communications as it directly improves the receiver sensitivity. III-V compound devices dominate the ultra-low-noise sub-1dB NF LNAs due to their high electron mobility. However, these III-V devices are costly and cannot be

integrated with monolithic CMOS RFICs. With the FTQH techniques to be discussed in Chapter 6, a first CMOS sub-1dB wideband receiver is realized with only one external passive component.

Existing noise canceling techniques cannot support concurrent receptions. Next-generation wireless communications need concurrent wireless links to maximize the utilization of the fragmented spectrum in systems such as LTE Advanced. The implementation of concurrent wideband receivers is very challenging and have either significant linearity and NF penalty. Thus, low-penalty RF signal splitting circuit techniques are highly desired. FTQH receivers (Chapter 6) can be scaled up to realize a concurrent receiver array with its unique antenna interface.

Field programmability is desired for the dynamic performance tradeoffs and the power consumption optimization. As discussed in Section 1.3.2, the field-programmable tradeoffs are essential to optimize the power consumption of an SDR receiver without operating for the worst-case scenarios in all RF environments. The field programmability is a theme that is consistently followed in all the prototype chip designs throughout Chapter 4 to Chapter 6.

Chapter 3

Antenna Interface Bandwidth Enhancement with Noise Cancelling Distributed Amplifier

3.1 Introduction

Common-source common-gate noise-canceling LNAs (CS-CG NC-LNA) [16] [17] are promising for wideband SDR receiver front ends. But in a typical 65nm technology, it is difficult to obtain sufficient input matching beyond 6GHz with an inductor-less design [16]. Resonated designs can extend the input matching beyond 10GHz [17], but due to the resonated nature the amplifier has low gain at sub-GHz bands, and is not suitable for lower frequency RF operation. Other noise-canceling LNA designs also have similar issues [18].

Distributed amplifiers (DA) are capable of operating from DC up to very high frequencies. CMOS DAs that have bandwidth larger than 10GHz are reported e.g., in [19–21]. DAs typically

have relatively low gains due to the need of a matched impedance for the drain line. A second fundamental draw-back of a conventional DA design is the noise contribution from the gate line termination resistor at low frequencies. The noise figure usually increases rapidly when operating below 1GHz which makes the distributed amplifier less suitable for SDR or CR applications where there is a strong interest in low and high frequeny bands.

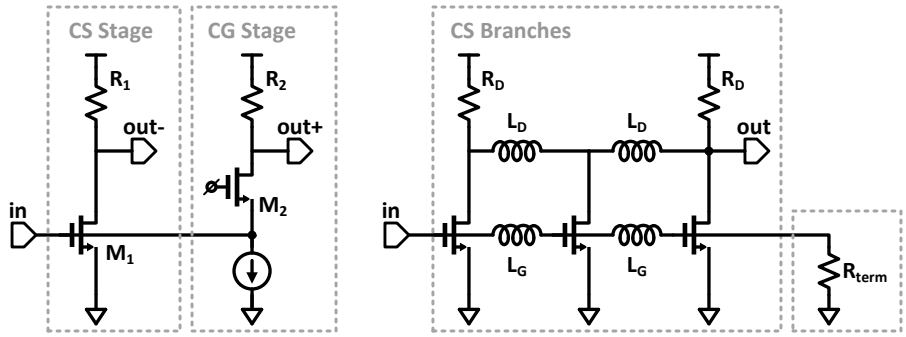
In this chapter, we introduce a hybrid topology that combines the features of a noise-canceling LNA and a distributed LNA: the Noise Canceling Distributed LNA (NCDA). The physical 50Ω gate line termination resistor of a classical DA is replaced by a common gate amplifier with a 50Ω input impedance, and its noise is canceled at the differential output.

3.2 Noise Canceling Distributed LNA

3.2.1 Limitations of CS-CG NC-LNA and DA

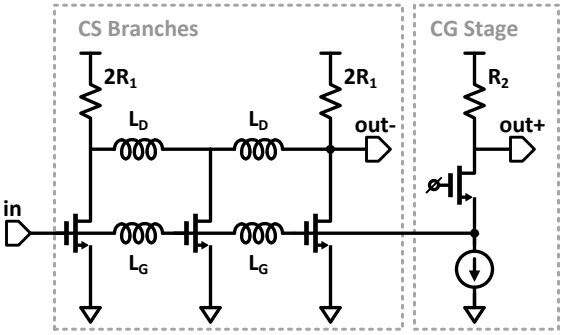
A conventional CS-CG noise canceling LNA usually consists of a CS stage and a CG stage, as illustrated in Fig. 3.1(a). The CG stage enables wide-band input impedance matching, and the thermal noise associated with M_2 is sensed by M_1 and appears as common mode at the differential output voltage [16]. The excess thermal noise is thus mainly contributed by M_1 and load resistors. By putting more CS branches in parallel, noise figure of the NC-LNA can be improved.

However, sizing up the CS stage inevitably increases the parasitic capacitance at the LNA input. In combination with the capacitance from the bond pad and ESD diodes, input matching bandwidth is eventually limited. The NC-LNA demonstrated in [16] has a -10dB S_{11} bandwidth of



(a) CS-CG noise-canceling LNA

(b) 3-branch Distributed LNA



(c) 3-branch Noise-canceling distributed LNA

Figure 3.1: Simplified schematics of NC-LNA, DA and NCDA

no more than 6GHz. The work in [17] uses an inductor to resonate out the input capacitance. This LNA achieves broad-band input matching up to 14GHz, at the expense of not being able to operate below 1GHz.

Distributed amplifiers address the wide-band input matching problem in a different way. The simplified schematic of a conventional DA is shown in Fig. 3.1(b). Two artificial transmission lines (T-lines) are formed by inserting inductors (L_G and L_D) between CS branches. The parasitic capacitors are absorbed into the T-line design. The input signal propagates along the gate T-line, amplified by each branch and combined coherently in the drain T-line. As a result a very wide-band operation is achieved (see e.g. [19–21]).

The disadvantage of using distributed amplifiers as an LNA is the high noise figure at low frequencies. The gate T-line of a DA is usually terminated with a physical resistor R_{term} (Fig. 3.1(b)). The noise transfer function from R_{term} towards output is bandstop [19], thus the midband noise performance is acceptable. However, at low frequencies, R_{term} will add significant noise and impose a minimum noise figure of 3dB due to the termination alone.

3.2.2 Design of a Noise-Canceling Distributed LNA

Considering the limitations of NC-LNA and DA, we propose a Noise-Canceling Distributed LNA that combines desirable features of the two topologies. A simplified schematic is shown in Fig. 3.1(c) to compare with an NC-LNA and DA.

The NCDA distributes the CS stage into multiple branches and inserts inductors in-between. The input capacitance of the CS is absorbed into an artificial transmission line as in a distributed LNA, which improves the operating bandwidth. At low frequencies, the inductors practically become shorts, and the NCDA operates like a conventional NC-LNA and offers cancellation of the noise from the gate T-line termination.

ESD protection at the LNA input is essential as the LNA is directly connected to a pad. The large parasitic capacitance associated with the ESD diodes is substantial, but thanks to the distributed nature of the NCDA, these ESD diodes can also be divided into smaller parts and distributed to each CS branch [20].

The pad capacitance is lumped into capacitance of the first CS branch, and the parasitic of the CG stage is lumped into the third CS branch. The total capacitance associated with each branch is

designed as follows:

$$2C_{1G} = C_{2G} = 2C_{3G} = C_G. \tag{3.1}$$

The capacitance of the three branches and two inductors of value L_G form a two stage π network. This approximates a transmission line with characteristic impedance of:

$$Z_{0G} = \sqrt{L_G/C_G} = 50\Omega. \tag{3.2}$$

Similarly, the drain capacitance of the three branches and two inductors L_D form the drain T-line. To save power, the drain T-line uses a higher characteristic impedance of $Z_{0D} = 75\Omega$. Also, to equalize the phase velocity in the gate T-line and drain T-line, The following constraints need to be satisfied:

$$\beta = \omega\sqrt{L_G C_G} = \omega\sqrt{L_D C_D}. \tag{3.3}$$

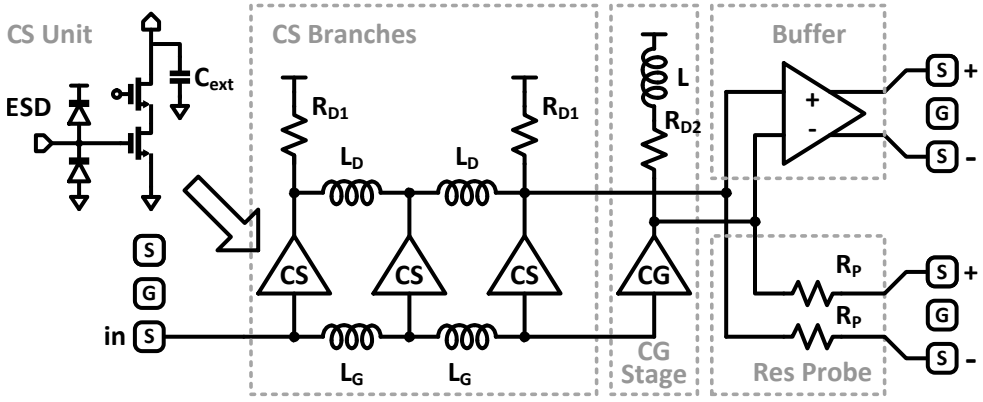


Figure 3.2: Simplified schematic of the NCDA prototype chip

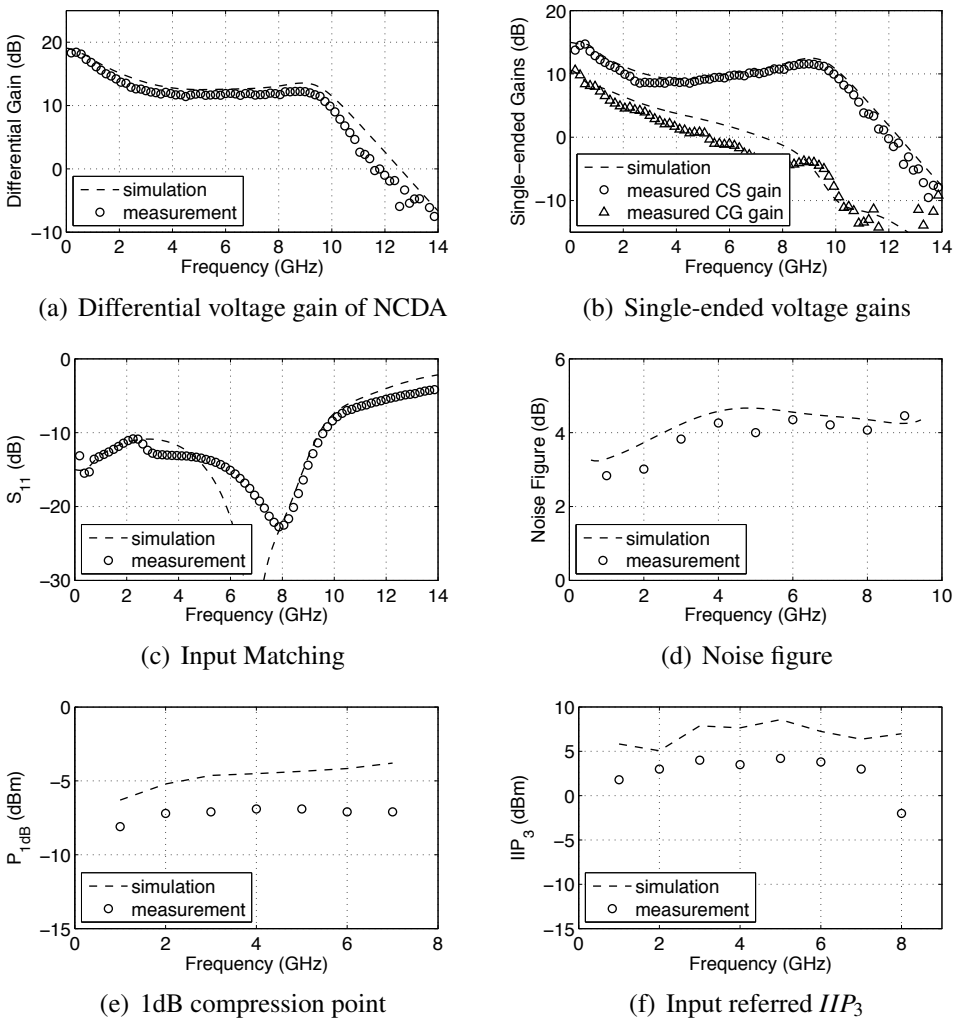
3.2.3 Proof-of-principle Prototype

A complete block diagram of the NCDA prototype chip is shown in Fig. 3.2. Each CS branch consists of a common-source cascode amplifier. ESD diodes are put close to the transistor to protect the gates. Some extra capacitance C_{ext} is appropriately added to equalize impedance and phase velocity of the drain T-line. In addition to the basic NCDA topology, an inductive peaking inductor L has been put in series with R_{D2}. This NCDA is initially designed for integration into a complete receiver, so the LNA is not suitable to directly drive a 50Ω load. To compensate the insertion loss of the test fixtures, an on-chip differential buffer has been included to drive the signals off-chip so that noise figure can be more accurately measured. To measure the frequency response and linearity of the NCDA without being limited by the buffer linearity, a pair of resistive attenuators are used to tap out RF signals without overly loading the NCDA with pad parasitics [22]. A pair of dummy resistive attenuators has also been included on the chip so that the attenuator response can be characterized and de-embedded.

3.3 Simulation and Measurement Results

Extensive post-layout simulations have been used to verify the prototype NCDA design. Small circuit cells are extracted with Calibre PEX. Larger passive structures such as custom probe pads, inductors and long interconnections are modeled with EM simulations with EMX. Multi-port S-parameter models are used to ensure the best accuracy.

The prototype chip has been directly bonded to a printed circuit board (PCB) that provides all



(a) Differential voltage gain of NCDA

(b) Single-ended voltage gains

(c) Input Matching

(d) Noise figure

(e) 1dB compression point

(f) Input referred IIP_3

Figure 3.3: Comparison of measurement results to post-layout simulations

power supplies and bias currents. The RF signals are provided and measured with Cascade 40GHz SGS differential RF probes. The microphotograph of the bonded die with RF probes landed on the RF input and output pads is shown in Fig. 6.11(a). The dummy resistive attenuators have first been characterized so that they can be de-embedded from the amplifier's S-parameter measurements taken with a 4-port Agilent N5230A vector network analyzer.

The amplifier's small signal parameters are shown in Fig. 3.3(a) and Fig. 3.3(b). The NCDA

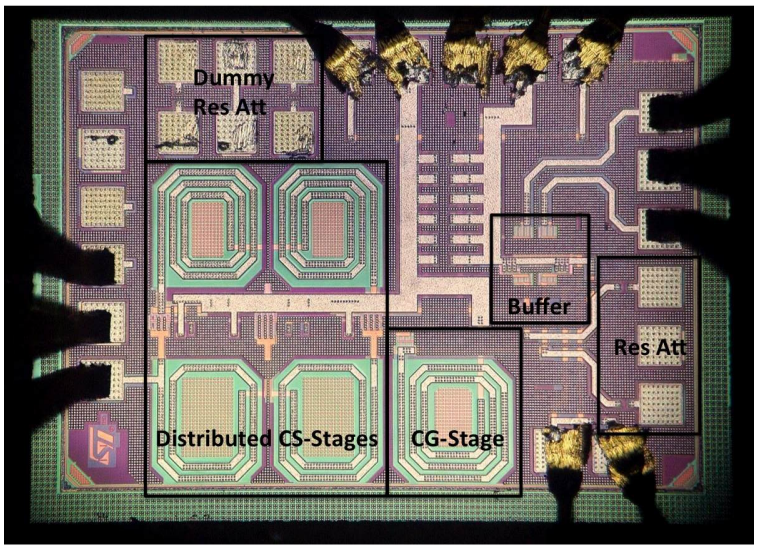


Figure 3.4: Die photo of the distributed noise canceling LNA

Table 3.1: Performance summary of wide-band CMOS LNAs

	[16]	[23]	[17]	[18]	[19]	[20]	[21]	[24]	[25]	[26]	This work
Topology	NC-LNA	NC-LNA	NC-LNA	NC-LNA	DA	DA	DA	Res FB	Res FB	Active FB	**NCDA**
CMOS Tech.	65nm	65nm	180nm	90nm	180nm	130nm	130	90nm	90nm	65nm	**65nm**
Gain (dB)	13	10.7	9.7	7.8-12.3	8	15	20.47	22	25	13	**12**
BW (GHz)	0.2-5.2	DC-10	1.2-11.9	3.1-13.9	0.04-7	DC-12	0.4-10.5	0.5-7.0	0.5-8.2	DC-10	**DC-9.5**
NF min (dB)	3	2.9	4.5	2.7	4.2	2.5	3.29	2.3	1.9	4	**2.8**
IIP_3 (dBm)	0	-3.5	-6.2	-6.4	3	0	-11.5	-10.5	-4	-1.5	**4**
V_{DD} (V)	1.2	1	1.8	1	1.3	1	1.5	1.8	2.7	1.2	**1.4**
P_{DC} (mW)	14	13.7	20	2.5	9	26	37.8	12	42	N/A	**18**
Area(mm^2)	0.009	0.02	0.1	0.59	1.16	0.435	0.616	0.012	0.025	N/A	**0.4**
FoM	0.32	0.12	0.02	0.26	0.34	0.28	0.02	0.13	0.31	N/A	**0.61**

provides more than 12dB gain up to 9.5GHz. The single-ended gain of the CG stage rolls off relatively quick, but is compensated by high frequency gain peaking of the CS stages. The measurement results match well to the post-layout simulations. The measured input matching S_{11} of the NCDA is shown in Fig. 3.3(c). The S_{11} is better than -10dB up to 9.5GHz.

The noise figure (NF) of the LNA is measured using the noise figure personality on an Agilent E4446A spectrum analyzer with an NC436B noise source from Noisecom. In order to obtain

accurate NF measurement results, the whole circuit is powered with batteries and all bias controls are properly shielded. The differential output from the on-chip buffer is converted into singled-ended signal with a wide-band hybrid. Insertion loss of the input cable, adaptors and probes are carefully characterized and de-embedded from the raw data. The measured NF is slightly lower than simulation results, but is within tolerance of the device model and measurement uncertainty.

All linearity measurements are conducted using the resistive attenuator interface. The differential output signal is converted to single-ended for the spectrum analyzer. 1dB compression point (P_{1dB}) of the NCDA is around -7dBm across frequencies (Fig. 3.3(e)). Two-tone intermodulation tests are conducted at multiple frequencies with the two tones placed 5MHz above and below the center frequency. The average IIP_3 across frequencies is +4dBm (Fig. 3.3(f)).

3.4 Comparison to the State of the Art

In this section, we compare the NCDA prototype with state-of-art wide-band CMOS LNA designs. Several representative publications have been collected, including noise canceling LNAs, distributed LNAs and resistive feedback LNAs. Their specifications are summarized in Table 3.1.

The following figure of merit (FoM) [19] has been used to compare LNA designs of different topologies and specifications; it combines gain, linearity, NF and power:

$$FoM = \frac{G \times IIP_3}{(F-1)P_{DC}}. \tag{3.4}$$

Variables and their units are defined as follows. The IIP_3 quantifies the linearity of the LNA and

has a linear unit of mW. F is the linear noise factor of the LNA, and $F-1$ quantifies its excess noise contribution. P_{DC} is the quiescent power consumption and uses unit of mW. G denotes voltage gain of the LNA and uses dimensionless linear scale. This unitless FoM appropriately approximates the physical interdependence of an LNA's specifications and provides a valid evaluation standard across different designs and topologies.

Looking at Table 3.1, it can be observed that this NCDA prototype has the highest FoM amongst comparable state-of-the-art designs. This indicates that the NCDA topology strikes a good balance between all the specifications mentioned in the FoM.

Resistive feedback LNAs [24] [25] generally have high voltage gain, and good noise performance compared to other topologies. However, their linearities are relatively low.Distributed LNAs like [19] and [20] have a good FoMs due to low power consumption. [21] has good gain, but linearity is significantly degraded. The NC-LNAs in [16] and [18] achieve decent FoMs, but [16] has low bandwidth and [18] is not able to operate below 3GHz. [23] and [17] are very area efficient, but only have moderate gain and linearity. [26] is comparable to this work if its power is lower than 3.5mW.

In conclusion, the noise-canceling distributed LNA is a good candidate when high bandwidth operation and high linearity are desirable. Moreover, the NCDA is usable as LNA across the entire operating band, for instance for software defined or cognitive radio applications.

Chapter 4

Input Linearity Enhancement of Field-Programmable LNAs with Interferer-Reflecting Loop

4.1 Introduction

The growth of wireless communications has resulted in a large number of different standards operating in different portions of the spectrum. Software defined radios (SDRs) have been proposed so a single device can operate with different standards or frequencies [27, 28]. Their implementation remains an active area of research given the challenging performance requirements in terms of noise figure (NF), linearity and power dissipation. Multi-standard receivers are often designed to meet the worst-case combination of requirements which leads to increased power dissipation.

Given the continued growth in usage and data rates of wireless devices, the amount of interference that receivers need to tolerate keeps increasing, while the spectral conditions can also vary significantly from location to location and from time to time [29]. Therefore it is becoming more and more desirable to design RF front ends that can dynamically adjust to the specific spectral operating conditions and standards [27].

To address these needs, we are investigating field-programmable (FP) low-noise amplifiers (LNAs) with input-linearity-enhancement interferer-reflecting (IR) loops. The operating frequency as well as the noise-linearity-power performance envelope can be changed by the user in the field. The LNA is the first building block in a receiver and often dictates the receiver NF and out-of-band linearity; it is thus a key block to study for how to enable FP performance trade-offs.

We propose a FP interferer-reflecting LNA (IR-LNA) that is designed with a high degree of programmability in terms of gain, NF, linearity and power consumption. In addition, a negative feedback interferer-reflecting loop is introduced to improve the out-of-band input linearity of the LNA and to enhance the performance of programmable filters. The combination of high programmability and linearity enhancement makes the FP IR-LNA a promising solution for SDR front ends.

The related art of FP LNAs and LNA/receiver linearization techniques is reviewed in Section 4.2, and the concept of wideband interferer reflection is presented and analyzed in Section 4.3. Section 4.4 discusses the design of the FP LNA core and the circuit realization of the IR-LNA prototypes with different filter implementations. Experimental results are presented in Section 4.5 and conclusions are provided in Section 6.8.

4.2 Field Programmable LNAs and LNA Linearization Techniques

We briefly review prior research on FP LNA topologies. In cellular communication systems, the out-of-band blockers are often only a few tens of MHz away from the desired signal. To reject these blockers, high Q off-chip filters are typically used, but they are bulky, expensive and cannot be tuned. We also review recent research on realizing integrated on-chip narrowband filtering or providing equivalent linearity enhancements with linearization loops.

4.2.1 Field-Programmable LNA Architectures

Programmable LNAs can be implemented based on conventional topologies such as the common-gate (CG) [30], resistive feedback [31, 32] or inductive degeneration [33] LNAs. In CG LNAs the programming is limited to resistive load switching or a programmable input attenuator [30] due the strict coupling between input matching and the transistor transconductance (G_m); this has drastic NF penalties and does not improve the dynamic range. In resistive shunt-shunt feedback LNAs the NF can be reduced by increasing G_m but the feedback and load resistor need to be changed in tandem to maintain input matching [31, 32, 34]. Similar approaches can be used when the feedback is through a translational loop [35]. A variant of the resistive feedback LNA with orthogonal gain and linearity programmability was demonstrated in [36], but the linearity is relatively low ($OB\text{-}IIP_3$ of -16.3dBm [36]). The operating frequency of inductively degenerated LNAs can be programmed by

switching in and out the common source devices [33] and the gain can be programmed by current steering techniques [37]. However, realizing a programmable NF-power trade-off is difficult.

4.2.2 LNA and Receiver Linearization Techniques

Receivers for SDR applications need to operate with broadband RF selection filters or tunable RF filters which often offer less blocker rejection. Recently, a variety of interferer filtering and rejecting techniques have been explored to enhance the linearity of LNAs or receivers for SDR applications.

N-path bandpass filters [38, 39] can be inserted between the antenna and the LNA to reject out-of-band interferers. Due to the low impedance level at LNA input, large capacitors (e.g., 40pF to 70pF [38, 39]) need to be used which take up a lot of chip area [1]. They further require low ohmic (e.g., 5Ω [38] to 10Ω [39]) and thus large switches which increases the clock power dissipation. Mixer-first receivers [41, 42] similarly use the impedance frequency translation technique of passive mixers to realize highly selective RF input matching with high linearity ($OB\text{-}IIP_3$ of +25dBm [41]) but have a higher flicker noise corner (200kHz [41]) due to the absence of RF gain before downconversion. In [43] an N-path notch filter is implemented to reject a blocker at a specific frequency. However, in this case, the blocker frequency needs to be known.

Translational loops down convert RF signals to baseband, perform filtering with low frequency filters and upconvert the filtered signals back to RF to reject out-of-band interferers. In the feed-forward interferer cancellation loop [44–46] (Fig. 4.1(a)) the auxiliary path inserts the out-of-band

[1] Passive impedance transformation such as baluns/transformers [40] can be used to increase the impedance level at the LNA input, but these techniques come with linearity penalties.

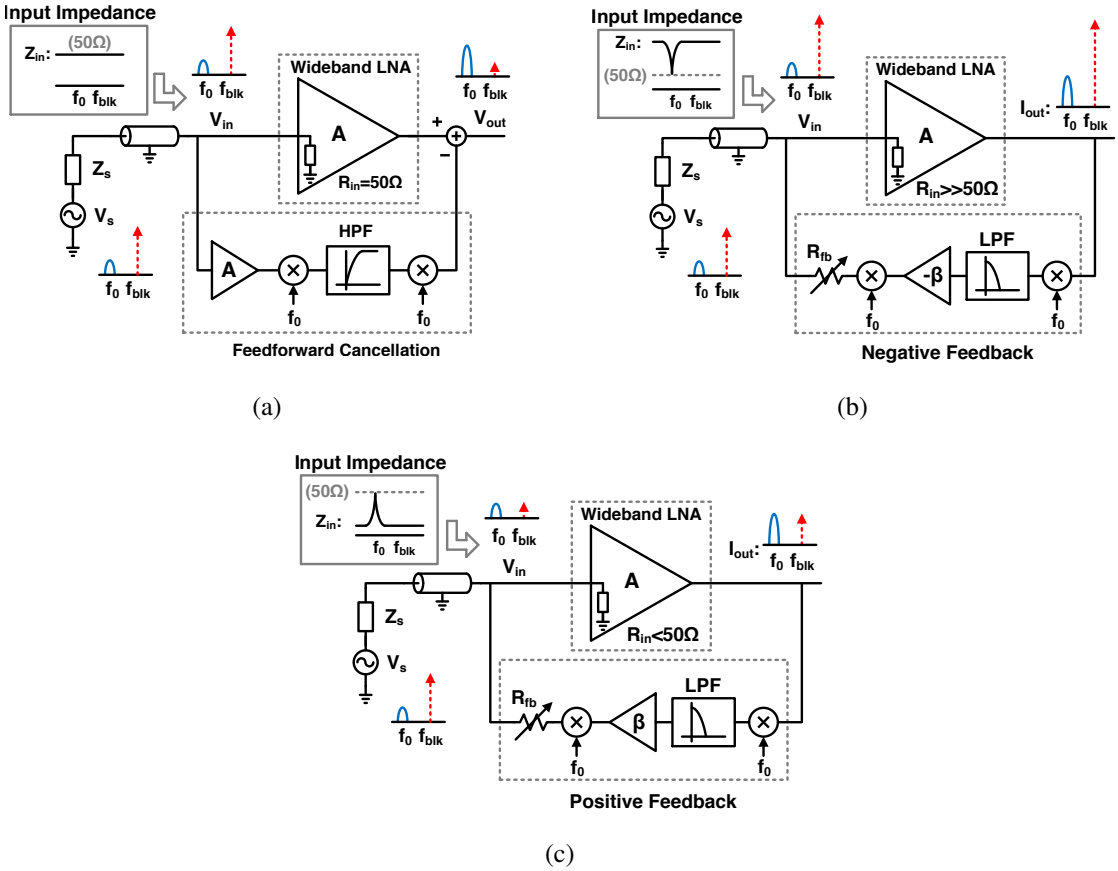
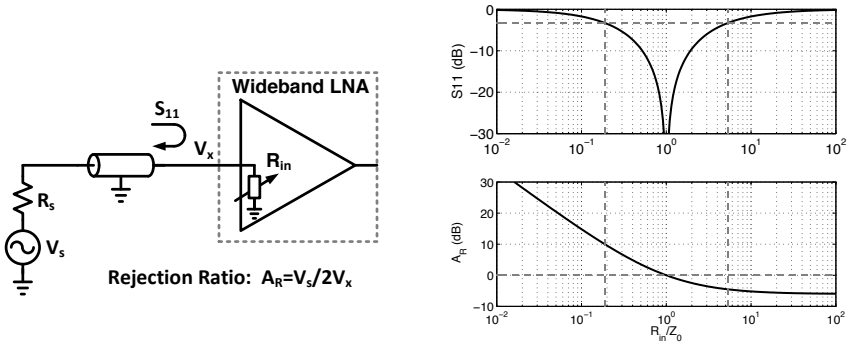


Figure 4.1: Review of translational loop techniques for interferer cancellation or impedance matching; (a) feedforward loop that cancels out-of-band blockers at the output of a matched LNA but not at the input; (b) negative feedback translational loop to realize in-band impedance matching for a high input impedance LNA while out-of-band blockers see a high impedance and create large unwanted voltage swings; (c) positive feedback translational loop to realize in-band impedance matching with a low input impedance wideband LNA.

interferers with opposite phase at the LNA output to do interferer cancellation. This only improves the LNA output linearity. Due to the frequency dependent phase shift in the high-pass filters in the aux. path the cancellation is also only effective for signals close to the band of operation.

Negative feedback translational loops (Fig. 4.1(b)) [28, 35] create an input impedance match in the signal band for LNA circuits like G_m cells that have a high input impedance. The wanted RF signals are downconverted to baseband, low-pass filtered and then up converted back to the LNA input. However, for out-of-band signals, the loop gain is low and the input impedance is high (see Section 4.3.1). As a result, the LNA input linearity and the out-of-band blocker tolerance are degraded. Other negative feedback translational loops, e.g. in [47–50], suppress out-of-band interferers at the LNA output but do not improve input linearity. Again, due to the limited baseband bandwidth and phase matching, these loops only reject blockers close to the frequency of operation. Negative feedback translational loops can also be combined with high-pass IF filters across an input matched LNA to reduce the out-of-band input impedance and suppress blocker signals [51, 52].

In translational loops with positive feedback (Fig. 4.1(c)) [53] a wideband LNA is used with a low input impedance (e.g., 20Ω), and the feedback increases the input impedance to 50Ω for the desired signals. This enables wideband blocker rejection to the extent that a wideband low input impedance can be realized, but this can require a substantial power dissipation. G_m boosting techniques [53, 54] can reduce power dissipation but degrade the linearity. The positive feedback gain further needs to be accurately adjusted to achieve the matched impedance [55]. Such RF calibration is challenging and needs to be performed every time the gain code is changed.



(a) (b)

Figure 4.2: (a) illustration of rf reflection at an lna input with an input impedance r_{in}; (b) reflection coefficient s_{11} and voltage rejection ratio a_r for varying input impedance; a_r quantifies the voltage swing in the reflected configuration compared to the matched configuration; for the same s_{11}, low impedance reflection provides high a_r and small voltage swings, while high impedance reflection results in low a_r and high voltage swings.

4.3 The Interferer-reflecting LNA

4.3.1 The Operation Principle of the Interferer-Reflecting Loop

Our goal is to improve the LNA *input* linearity by making sure that input blocking signals do not create large voltage swings at the LNA input. LNAs are most often operating in an impedance-matched RF environment receiving their input signals from the antenna through RF switches, filters, duplexers and transmission lines. For the desired signals, an impedance match is required to make sure signals do not undergo unnecessary attenuation or dispersion through the RF components. However, for unwanted signals we can choose to use a mismatched termination. Fig. 4.2(a) shows an LNA with an input impedance R_{in} connected to an RF signal source with a source impedance R_S through a transmission line with a characteristic impedance R_S. For an impedance match ($R_{in} = R_S$), S_{11} [56] is low and the voltage rejection ratio $A_R = (V_S/2)/V_X$ is

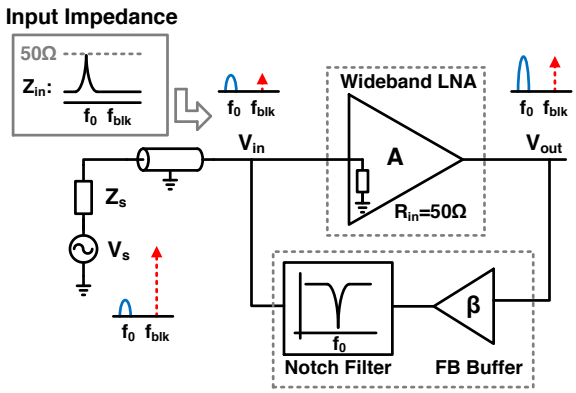


Figure 4.3: The proposed interferer-reflecting LNA topology. A frequency selective negative feedback around a wideband matched LNA results in a bandpass profile for the input impedance with a matched input impedance for the wanted signal and a low input impedance for unwanted signals. As a result, the out-of-band blocker voltage swings are reduced.

0dB (Fig. 4.2(b)); V_S is the source voltage and V_X is the LNA input voltage. Assuming a matched source impedance (R_S), for large R_{in}, A_R becomes as low as -6dB, and the signal can undergo up to a 2x voltage gain compared to the matched condition. But for small R_{in}, A_R can become arbitrarily large and the voltage swing at the LNA input can be strongly suppressed. E.g., in a 50Ω system an S_{11} of -3.3dB occurs for a low impedance reflection with an R_{in} of 9.4Ω, and voltage attenuation of 10dB (3.2x) compared to a matched case, or for a high impedance reflection with an R_{in} of 266Ω but then the voltage swing is 4.5dB (1.7x) higher than the matched case.

A wideband input-matched LNA with a frequency-selective shunt-shunt feedback can realize the desired frequency dependent input impedance (Fig. 4.3). A notch filter tuned at the desired signal frequency is used in the feedback path. For the in-band signals, the feedback loop gain is very small and the presence of the loop can be ignored. The input impedance is set by the LNA input impedance which is designed to be R_S. For out-of-band interferers, the loop gain is large. The input impedance is then strongly reduced and low impedance signal reflection is obtained. To

the first order, the voltage swings at the LNA input are dominated by the in-band signals. Out-of-band signals are shorted through the notch filter and its low impedance driver and the interferer power is reflected back to the antenna. This approach has the following key advantages. First, a *broadband* interferer rejection is realized that is only limited by the RF bandwidth of the loop which improves with CMOS process scaling. In contrast, in a translational loop the bandwidth is set by the baseband or IF amplifier and is much smaller. Second, the interferer rejection is *frequency agnostic.* No prior information is needed about the interferer's frequency in contrast to several other approaches (e.g., [43, 46, 57]). Finally, *no calibration* is required. Finite suppression in the notch filter only leads to relatively small impedance matching errors in the LNA at the desired frequencies.

4.3.2 The IR Loop Enhances the Loaded Q of Passive Filters

An additional key feature is that the IR loop enhances the loaded Q factor of the notch filter, which we illustrate with the following example. Let's assume a parallel LC tank is available with a given Q factor and tuned to the desired frequency. The first design option is to place the tank at the input of a wideband LNA to create a bandpass response so that out-of-band interferers are attenuated (Fig. 4.4(a)). At the input of the LNA, the impedance level is only 25Ω—R_S // R_{in}, both 50Ω—which results in a low loaded-Q and a broad filter passband. Alternatively, we can use the same tank as a notch filter in an IR-Loop around the wideband LNA with inverting gain α_1 (Fig. 4.4(b)). At resonance, the parallel tank has high impedance which strongly reduces the loop gain, while at out-of-band frequencies, the tank has low impedance and the loop gain is high. The

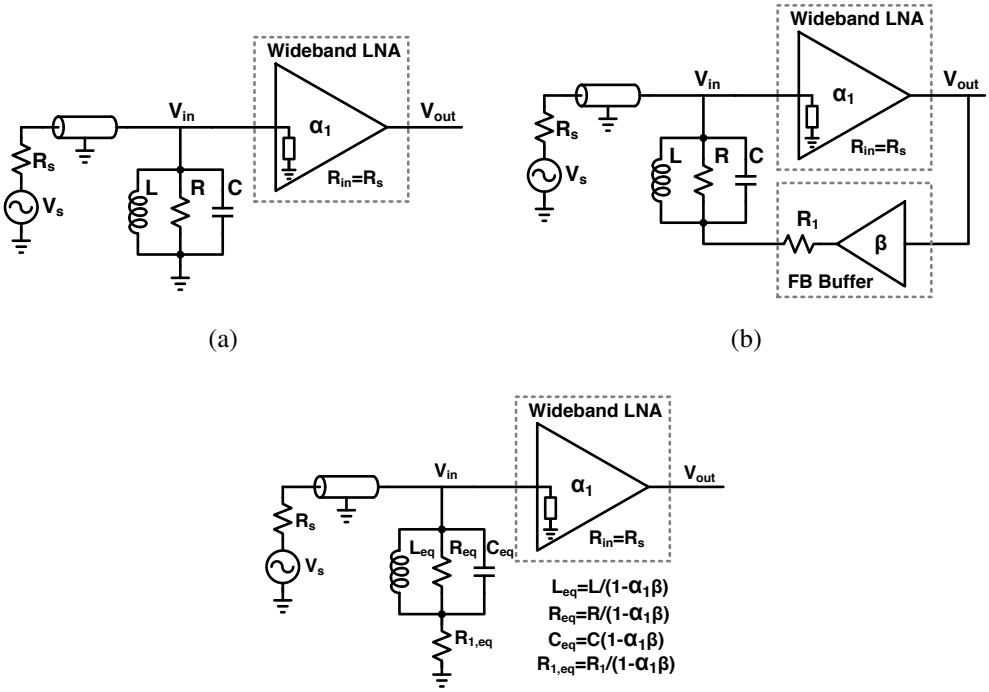
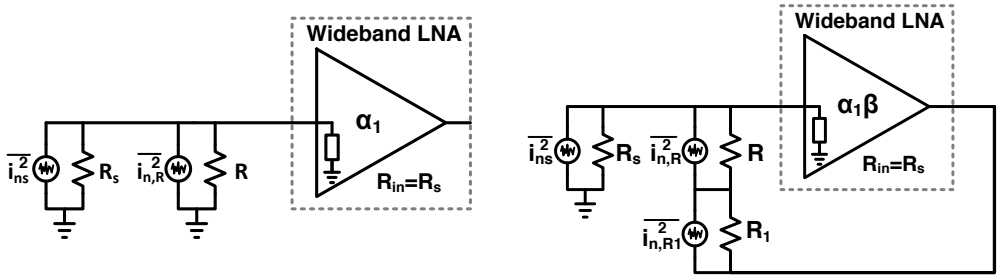


Figure 4.4: Example to illustrate the loaded Q-factor enhancement by the interferer-reflecting loop; (a) a parallel RLC tank is put directly at the input of the LNA as a bandpass filter; the LNA is modeled as a broadband negative voltage gain α_1 with a matched input impedance R_{in};(b) the same RLC tank placed in an IR-Loop as a notch filter; (c) equivalent circuit of (b), showing that the impedance of the tank is reduced by the loop gain.



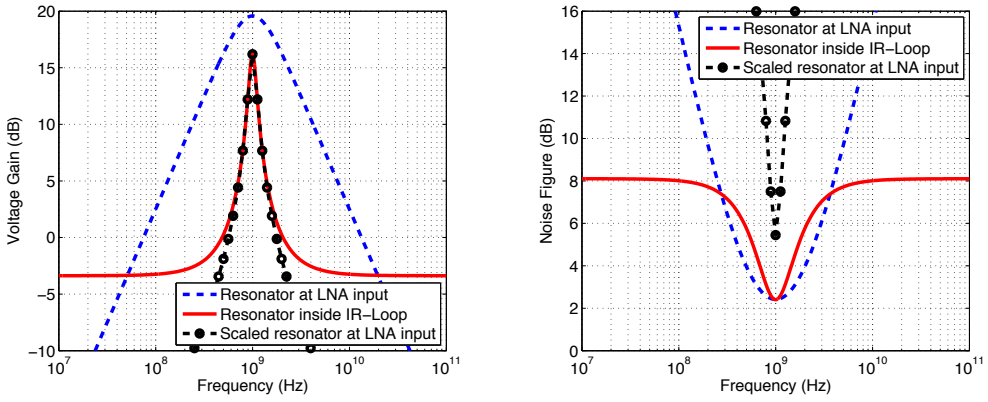
(a) (b)

Figure 4.5: Comparison of the noise performance of the two LNA designs of Fig. 4.4; (a) in-band noise model of the LNA with input filter (Fig. 4.4(a)); (b) in-band noise model of the LNA with a filter in an IR loop (Fig. 4.4(b)).

equivalent circuit of the IR-Loop is shown in Fig. 4.4(c) using a Thevenin-equivalent model for the feedback buffer with voltage gain of β and an output impedance of R_1. Due to the negative feedback the equivalent tank impedance is lowered $(1-\alpha_1\beta)$ times while the resonant frequency stays unchanged. The loaded filter Q is now set by the 25Ω impedance of R_s // R_{in} and a smaller equivalent inductance and larger equivalent capacitance. The resulting loaded Q is higher and the filter response has a narrower bandwidth by a factor of $1-\alpha_1\beta$ as long as the equivalent parallel resistance $R_{eq} = R/(1-\alpha_1\beta)$ is $\gg R_s$. However, due to the non-zero driver output impedance R_1 only a finite out-of-band rejection can be achieved. Also, due to the finite R_{eq} the insertion loss at the LNA input is slightly increased but we will show next that the associated noise penalty is negligible.

4.3.3 The IR Loop Breaks the Trade-off between Bandwidth and Noise Penalty

The equivalent noise models for the two filtering alternatives of Fig. 4.4 are given in Fig. 4.5. To model the in-band noise performance of the LNA, we can assume that all the reactive components



(a) (b)

Figure 4.6: (a) Simulated voltage gain from the source to the output ($A_v = 2V_{out}/V_s$) of the circuits in Fig. 4.4(a)(- -), Fig. 4.4(b)(–) with the same resonator and the circuit in Fig. 4.4(a) with a scaled resonator (-o-) to match the bandwidth of the circuit in Fig. 4.4(b) with the original resonator; (b) simulated noise figures for the same circuits.

are resonated out and that $R_{in} = R_s$. The subsequent analysis only focuses on the noise contribution due to the filtering, since the LNA contribution is the same in both cases. For the filter placed at the input (Fig. 4.5(a)) we easily obtain the noise factor as: $F = 1 + \frac{R_S}{R}$. With the filter in the IR loop (Fig. 4.5(b)) the effect of the negative feedback and the noise contribution from the feedback buffer needs to be taken into account. The buffer noise is assumed proportional to the output resistance R_1 by a factor of γ as is the case in a source-follower-type buffer. The noise factor is then:

$$F = 1 + \frac{R_S(R+\gamma R_1)}{(R+\gamma R_1 + R_S/2)^2} \approx 1 + \frac{R_S}{R} \text{ when } R \gg \gamma R_1 \text{ and } R \gg R_S \tag{4.1}$$

Assuming that R_1 is made sufficiently small, the noise factors are approximately identical. Placing the filter in the IR loop thus yields a sharper response without the noise penalty typically associated with increased selectivity.

To verify the theoretical analysis, the circuits in Figs 4.4(a) and 4.4(b) are simulated for a

wideband 20dB LNA with 2dB noise figure, a unity-gain buffer with $R_1 = 20\Omega$, and an on-chip tank resonant at 1GHz with a Q of 15 ($R = 500\Omega,\ L = 5.3nH,\ C = 4.8pF$). Fig. 4.6(a) shows the voltage gain over frequency; as expected the IR-Loop reduces the 3dB bandwidth from 1.4GHz to 182MHz, but causes around 3dB gain loss. The NF remains the same as shown in Fig. 4.6(b). Simulations were also performed for a scaled tank at the input of the LNA that offers the same selectivity; however, it has a 3dB noise penalty compared to the IR loop.

Due to the non-zero output impedance R_1 of the feedback buffer (see Fig. 4.4(c)), the out-of-band rejection for the IR loop is finite and as a result the voltage rejection ratio A_R is limited to:

$$A_R = \frac{\frac{2}{R_s} + \frac{1-\alpha_1\beta}{R_1}}{\frac{2}{R_s}} \tag{4.2}$$

which is 23.4dB in this example.

4.3.4 The IR Loop Improves the LNA Input Linearity

The improved filter sharpness thanks to the IR loop reduces the voltage swing at the LNA input even for close out-of-band interferers; we now evaluate how this improves LNA input linearity using the circuit models in Fig. 4.7.

Effect of the Non-Linearities of the LNA Core

We first assume distortion is mainly generated in the LNA core whose transfer characteristic $v_{out}-v_{in}$ is modeled as a third order memoryless[2] non-linearity: $v_{out} = \alpha_1 v_{in} + \alpha_3 v_{in}^3$. For analysis of intermodulation distortion V_s is $A_0 cos(\omega_1 t) + A_0 cos(\omega_2 t)$. We write the spectral component of a voltage signal V at frequency $a\omega_1 + b\omega_2$ as $V_{(a,b)}$; so $V_{(1,0)}$ and $V_{(0,1)}$ are the test tones and $V_{(2,-1)}$ and $V_{(-1,2)}$ are the closeby IM3 components. Without loss of generality, we assume test tones at frequencies higher than the operation band with $2\omega_1 - \omega_2 = f_0$, so $V_{out,(2,-1)}$ is the IM3 component that needs to be minimized.

Without the IR Loop (Fig. 4.7(a)), the LNA presents a wideband matched 50Ω impedance and the LNA input voltage is $V_{in,noIR(1,0)} = \frac{1}{2} V_{s(1,0)}$; the IM_3 component of the output voltage is [8]:

$$V_{out,noIR(2,-1)} = \frac{3}{4}\alpha_3 \left(\frac{1}{2}A_0\right)^3. \tag{4.3}$$

We now analyze the out-of-band IIP_3 (OB-IIP_3) of the LNA with the IR-Loop engaged (Fig. 4.7(b)). R_{sw} models the parasitic series resistance[3] between the feedback buffer and the filter. The feedback buffer is assumed linear and modeled with a linear transconductor representing the transistor in a source follower. When the IR-Loop is engaged (Fig. 4.7(b)), the effect of the feedback loop is analyzed using harmonic balance. Assuming ω_1 and ω_2 are out of band, the two-tone signals see a largely resistive impedance (see Section 4.3.2). Applying KCL at the input node for the

[2]In wideband RF circuits a memoryless assumption is typically sufficient for the purpose of hand analysis. The effect of second order non-linearities can be neglected due to low impedance at the LNA input at low frequencies and the differential output signal.

[3]When using a discretely programmable L-C filter, this is the on resistance of the bank selection switches, and in the case of an N-path filter, this is the on resistance of the switch transistors.

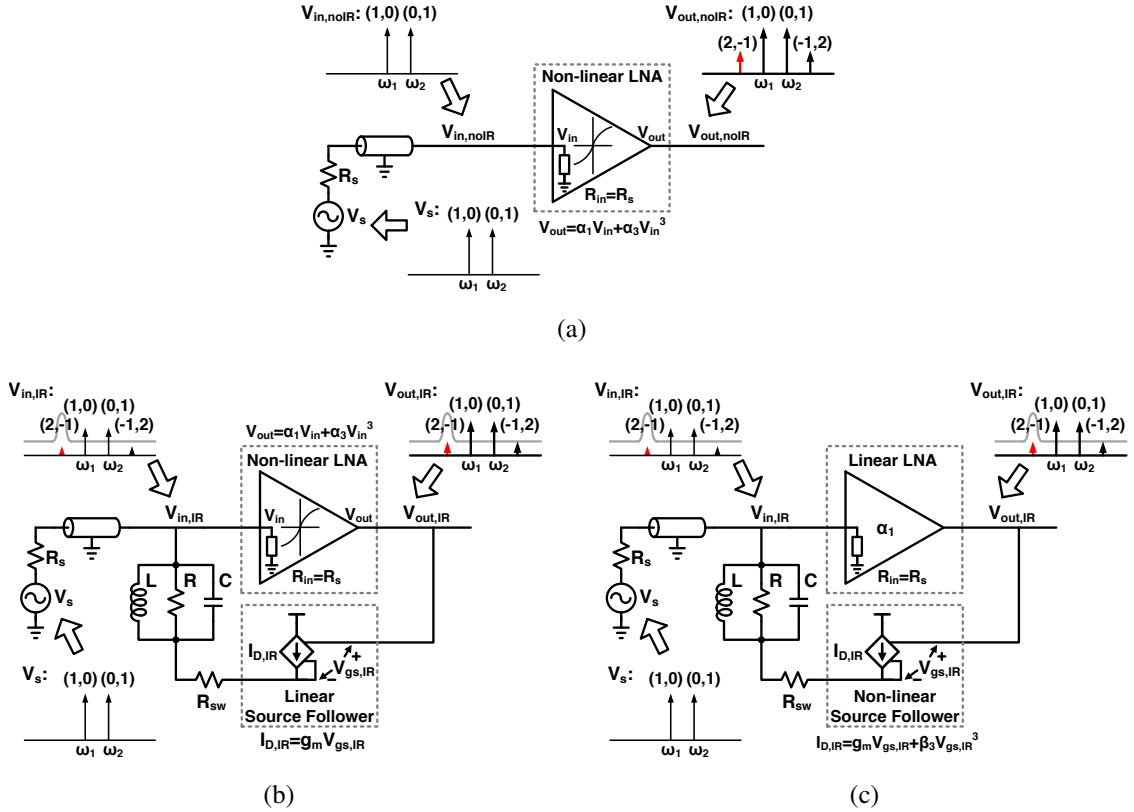


Figure 4.7: Analysis of the two-tone intermodulation linearity of (a) a non-linear LNA without the IR loop; (b) a non-linear LNA with the linear IR loop; (c) a linear LNA with non-linear feedback buffer in the IR loop.

out-of-band (1,0) test tone gives:

$$\frac{V_{in,IR(1,0)} - V_{s(1,0)}}{R_s} + \frac{V_{in,IR(1,0)}}{R_s} = I_{D,IR(1,0)}. \tag{4.4}$$

with $V_{s(1,0)} = A_0$. KVL for the feedback path gives:

$$V_{in,IR(1,0)} + I_{D,IR(1,0)} \cdot R_{sw} + V_{gs,IR(1,0)} = V_{out,IR(1,0)}. \tag{4.5}$$

For the (0,1) components similar relations are obtained. Assuming the LNA is operating without gain compression, $V_{out,IR(1,0)} = \alpha_1 V_{in,IR(1,0)}$, and using $I_{D,IR(1,0)} = \beta_1 V_{gs,IR(1,0)}$, the fundamental components of the input voltage can be calculated:

$$V_{in,IR(1,0)} = V_{in,IR(0,1)} = \frac{A_0}{2} \frac{\frac{2}{R_s}}{\frac{2}{R_s} + \frac{1-\alpha_1}{(R_{sw}+1/g_m)}} = \frac{1}{2} \frac{A_0}{A_R}; \tag{4.6}$$

note that A_R is given by (4.2) with $\beta = 1$ and $R_1 = R_{sw} + 1/g_m$. For the in-band components (2,-1), $V_{s(2,-1)} = 0$; applying KCL and KVL and the non-linear LNA and linear feedback buffer characteristics yields:

$$\frac{2}{R_s} V_{in,IR(2,-1)} = I_{D,IR(2,-1)}, \tag{4.7}$$

$$V_{in,IR(2,-1)} + (R + R_{sw}) I_{D,IR(2,-1)} + V_{gs,IR(2,-1)} = V_{out,IR(2,-1)}, \tag{4.8}$$

$$V_{out,IR(2,-1)} = \alpha_1 V_{in,IR(2,-1)} + \frac{3}{4} \alpha_3 (V_{in,IR(1,0)})^2 V_{in,IR(0,1)}, \tag{4.9}$$

$$I_{D,IR(2,-1)} = g_m V_{gs,IR(2,-1)}. \tag{4.10}$$

The output IM_3 component can now be calculated as:

$$V_{out,IR(2,-1)} = \left(\frac{\frac{2}{R_s} + \frac{1}{R+R_{sw}+1/g_m}}{\frac{2}{R_s} + (1-\alpha_1)\frac{1}{R+R_{sw}+1/g_m}} \right) \frac{3}{4}\alpha_3 (V_{in,IR(1,0)})^3 \tag{4.11}$$

For typical circuit parameters[4] ($R_S = 50\Omega$, $R \approx 1k\Omega$, $\alpha_1 \approx 7$, $R_{sw} \approx 30\Omega$ and $g_m \approx 26mS$), α_1 is sufficiently small and $R \gg R_s$, so that $R/\alpha_1 \gg R_s$, and

$$V_{out,IR(2,-1)} \approx \frac{3}{4}\alpha_3 (V_{in,IR(1,0)})^3 = \frac{3}{4}\alpha_3 (\frac{1}{2}\frac{A_0}{A_R})^3. \tag{4.12}$$

Assuming the in-band gain is similar for both cases, the out-of-band IIP_3 with and without IR loop can now be evaluated using (4.3) and (4.12):

$$OB\text{-}IIP_{3,IR,dBm} - OB\text{-}IIP_{3,noIR,dBm} = \frac{1}{2} \cdot 20\log \left(\frac{V_{out,noIR(2,-1)}}{V_{out,IR(2,-1)}} \right) \approx \frac{1}{2} \cdot 20\log(A_R^3) = \frac{3}{2} \cdot A_{R,dB} \tag{4.13}$$

Another important linearity measure is the B_{1dB}, i.e. the out-of-band blocker power level for which the in-band signal gain is compressed by 1dB. The IR loop will similarly reduce the voltage due to this blocker at the input of the LNA by A_R. Given that every 1dB rejection of the blocker voltage swing at the LNA input translates into 1dB of B_{1dB} improvement, we obtain:

$$B_{1dB,IR,dBm} = B_{1dB,noIR,dBm} + A_{R,dB} \tag{4.14}$$

[4] E.g., based on the N-path IR loop prototype presented later.

Effect of the Non-Linearities of the Feedback Buffer

Next, we analyze the impact of a non-linear feedback buffer on the *OB-IIP$_3$* (Fig. 4.7(c)). Now we assume the LNA is linear with voltage gain α_1 and all distortions come from the nonlinear G_m of the buffer, modeled with a third order memoryless non-linearity $I_D = g_m V_{gs} + \beta_3 V_{gs}^3$.Equations (4.4) to (4.8) still hold and we can also write:

$$V_{out,IR(2,-1)} = \alpha_1 V_{in,IR(2,-1)}, \tag{4.15}$$

$$I_{D,IR(2,-1)} = g_m V_{gs,IR(2,-1)} + \frac{3}{4}\beta_3 V_{gs,IR(1,0)}^2 V_{gs,IR(0,1)}. \tag{4.16}$$

Solving (4.4) to (4.6) for $V_{gs,IR(1,0)}$ gives:

$$V_{gs,IR(1,0)} = \frac{\alpha_1 - 1}{1 + g_m R_{sw}} V_{in,IR(1,0)} = \frac{\alpha_1 - 1}{1 + g_m R_{sw}} \left(\frac{1}{2}\ \frac{A_0}{A_R}\right) \tag{4.17}$$

Given $V_{gs,IR(1,0)} = V_{gs,IR(0,1)}$, and solving for $V_{out,IR(2,-1)}$:

$$V_{out,IR(2,-1)} = \alpha_1 \frac{3\beta_3}{4 g_m} \left(\frac{A_0}{2}\right)^3 \left(\frac{\alpha_1 - 1}{1 + g_m R_{sw}} \frac{1}{A_R}\right)^3 \left(\frac{1}{1 + \frac{2(R+R_{sw})}{R_s} + \frac{2}{\alpha_1 R_s} - \alpha_1}\right) \tag{4.18}$$

OB-IIP$_3$ is the value of $A_0/2$ when $|V_{out,IR(2,-1)}| = \alpha_1 A_0/2$, so

$$OB\text{-}IIP_3 = IIP_{3,G_m} \cdot \sqrt{\left| \left(1 + 2\frac{R + R_{sw}}{R_s} + \frac{2}{g_m R_s} - \alpha_1\right) \left(\frac{1 + g_m R_{sw}}{\alpha_1 - 1} A_R\right)^3 \right|}. \tag{4.19}$$

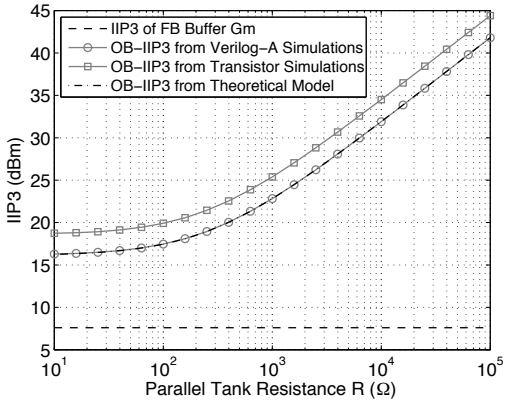


Figure 4.8: Comparison between the theoretical model (4.19) and the simulations of LNA's $OB\text{-}IIP_3$ due to feedback buffer non-linearities only. As the equivalent parallel resistance R of the notch filter increases, and its attenuation improves, the $OB\text{-}IIP_3$ is improved.

where $IIP_{3,G_m} = \sqrt{\frac{4}{3}|g_m/\beta_3|}$ is the IIP_3 of the feedback buffer when driving an AC short. Using the expression of A_R obtained from (4.6) with $\beta = 1$ and $R_1 = R_{sw} + 1/g_m$, and using the same typical circuit parameter as above, we obtain:

$$OB\text{-}IIP_3 \approx IIP_{3,G_m} \cdot \sqrt{Att_{notch}} \tag{4.20}$$

with Att_{notch} the in-band attenuation of the L-C notch filter when driving an $R_s/2$ load given by $2R/R_s$.

Simulations (Fig. 4.8) with a transistor-level and a third order polynomial Verilog-A transconductor model shown in Fig. 4.7(c) for the feedback buffer validated the theoretical model in (4.19); the simulation parameters are derived from the circuits presented in Section 4.4: $\alpha_1 = 7$, $g_m = 26mS$, $\beta_3 = -60mA/V^3$, $R_{sw} = 30\Omega$ and $R_s = 50\Omega$; g_m and β_3 are extracted from linearity simulations when the buffer drives an AC short. The theoretical analysis (4.19) matches well with

the Verilog-A simulations; the discrepancy between the model and the transistor-level simulations is likely due to the non-linear transistor output impedance r_o. For large R, $OB\text{-}IIP_3$ improves with a 10dB/dec slope, as in (4.20).

The IR-LNA design targets $OB\text{-}IIP_3$ of +15dBm. Typical R values for the on-chip filters that will be used (see Section 4.4.3) range from 200Ω to $1k\Omega$ resulting in an LNA $OB\text{-}IIP_3 > +19dBm$ for an IIP_{3,G_m} of +7.5dBm Assuming the buffer is designed with this linearity (see section 4.4.2), it will not be the limiting factor for the linearity of the IR-LNA.

4.3.5 IR Loop Analysis Summary

We conclude that the IR-loop technique can improve the trade-off between filter bandwidth and insertion loss for passive filters with finite Q. It reduces the equivalent tank impedance and improves the loaded Q resulting in a sharper response, however without any additional noise penalty when compared to placing the passive filter directly at the input of the LNA. The IR loop performs narrowband filtering at the LNA input and suppresses the voltage swing due to unwanted out-of-band signals resulting in significant input linearity improvements.

4.4 Field-Programmable Interferer-Reflecting LNA Circuit Realization

The IR-LNA prototype chip (Fig. 4.9) is composed of a field programmable LNA core and an IR loop with a feedback buffer driving tunable notch filters.

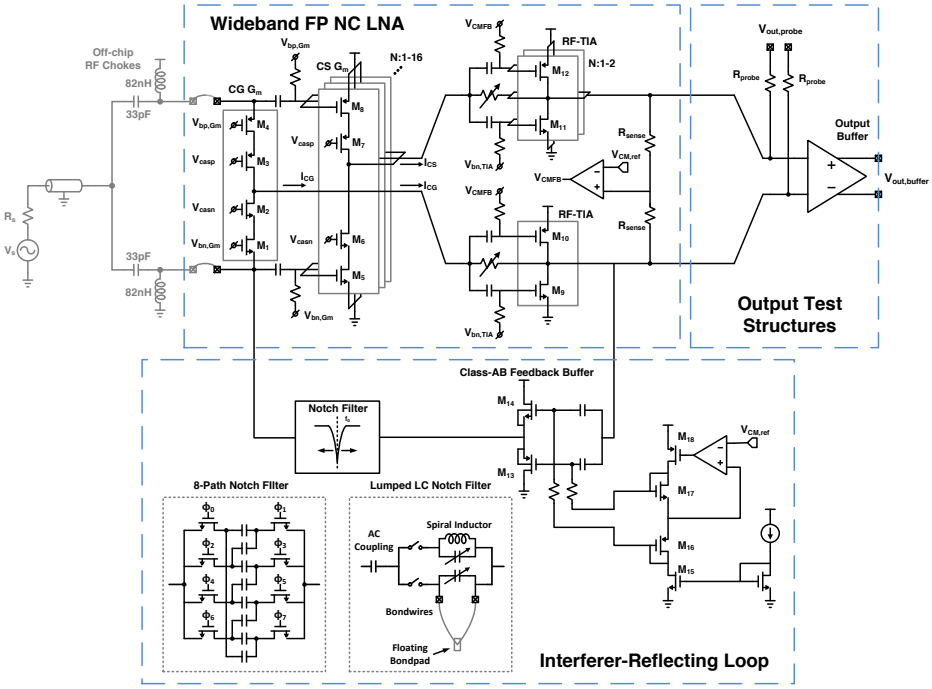


Figure 4.9: Circuit schematic of the field-programmable interferer-reflecting LNA with an 8-path notch filter.

4.4.1 The Field-Programmable Wideband Noise-Canceling LNA Core

The common-source common-gate (CS-CG) noise canceling LNA [13] is a wideband LNA topology that breaks the tradeoff between input matching and NF; by scaling the G_m of the CS stage, power consumption can be traded off with NF largely independent of input matching. In [13] this tradeoff is performed at design time, we propose a more flexible topology whose performance envelope can be adjusted in the field. If we were to program the gain by changing the load resistors in the standard NC LNA [13], the output common mode voltage would change substantially making the interface to the next stage challenging. The complementary current reusing topology shown in Fig. 4.9 overcomes this problem and has two key advantages. All the bias current flows through the G_m cell itself, only the signal current flows through the loads; the output DC operation point is

now largely independent of the G_m scaling. Current reuse further approximately doubles the G_m for the same current consumption with a small penalty in input bandwidth.

The cascode CS G_m stage is split into 16 slices that can be individually turned off by pulling the respective V_{casn} to V_{SS} and V_{casp} to V_{DD}. This allows to reduce the LNA power consumption in the field at the expense of a higher NF. The signal currents from the complementary CS and CG stages are pushed into trans-impedance amplifiers to improve the output bandwidth like in the Cherry-Hooper wideband amplifier [58]. These RF-TIAs have resistive shunt-shunt feedback with digitally programmable resistors. This allows to independently program the LNA gain and to adjust the weighted combination of the CS and CG signals.

4.4.2 Feedback Buffer

The feedback buffer is implemented as a class-AB complementary source follower (M_{13} and M_{14} in Fig. 4.9). The source follower topology ensures a low output impedance. The complementary structure can be biased with a low quiescent current (1.1mA) to save DC power, but when large blockers are present, it can sink large currents. To minimize the body effect, triple-well transistors are used. In the bias circuit the signal transistors are replicated as diodes while the DC bias current and the output DC voltage $V_{cm,ref}$ are controlled with feedback. The user can disable the IR loop around the LNA by putting the feedback buffer in a high impedance state by appropriately pulling the gate biases to V_{SS} and V_{DD}. The feedback buffer has been designed with a g_m of 26mS and an IIP_{3,G_m} of +7.5dBm. Analyses and simulations presented in Section 4.3.4 show that this performance is sufficient so that the buffer does not limit the LNA's overall $OB\text{-}IIP_3$.

4.4.3 Tunable Notch Filter Implementations

In this work, we demonstrate three implementations for the tunable notch filter in the IR loop: an LC filter with on-chip switchable capacitors and a spiral inductor, an LC filter with on-chip switchable capacitors with bondwires as high Q inductors, and a low power switched-capacitor N-path notch filter.

Compact, Low-Power N-path Notch Filter: N-path filters translate[5] a baseband impedance to RF frequencies realizing RF filters with high selectivity and tunable center frequency. An 8-path switched capacitor filter is equivalent to a high-Q RLC resonator [43] (where $R > 1k\Omega$ when loaded with 25Ω) and can be used directly in the IR-Loop to realize a narrowband filtering characteristic that is tunable with the clock frequency. As analyzed in Section 4.3.2, the IR-Loop improves the selectivity of the N-path notch filter and smaller capacitors can thus be used to achieve the same bandwidth compared to the case where an N-path BPF is placed before the LNA input (see Fig. 4.10). This saves chip area occupied by the capacitors. The N-path notch filter in this design uses 4pF MiM capacitors for each path, which is much smaller than the capacitance needed for a bandpass N-path filter in [38] or [39]. The effect of ON resistance R_{ON} of the switches is also reduced by the loop, so smaller switches (50um/65nm) with an $R_{ON} = 15\Omega$ achieve the same out-of-band rejection. This saves significant power in the switch clock drivers. Additional power savings have been achieved by improving the N-path notch filter topology and clocking scheme (Fig. 4.11). To overcome the significant loading to the input due to the combined bottom-plate

[5] In principle, the IR-LNA with an N-path filter could also be considered as a frequency translational loop. However, here we will model the N-path filter with an equivalent notch filter response [43] in order to analyze the IR-LNA performance based on Section 4.3.2.

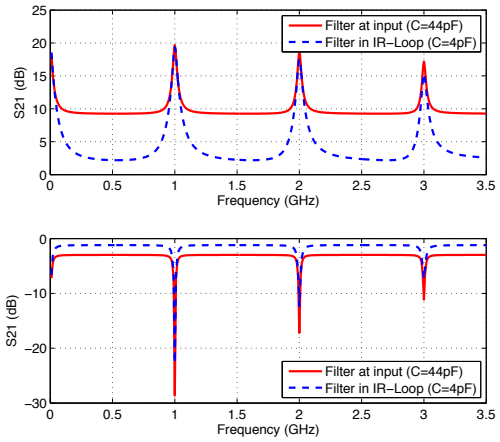


Figure 4.10: Comparison of the performance obtained with an N-path filter placed in the IR-LNA topology vs. an N-path bandpass filter at LNA input. Switch sizes are kept unchanged, while the capacitors are scaled by a factor of 11. The IR-Loop significantly reduces the capacitor size and improves the out-of-band rejection of the filter.

capacitance of all the branches in the conventional single-ended N-path notch filter [43], we use switches on both sides of the capacitor (Fig. 4.11). Each switch is shared by two capacitors to avoid the power penalty associated with driving extra switches. A set of 8-phase 25% duty cycle overlapping clocks are used instead of the conventional 8-phase 12.5% duty cycle clocks. The eight capacitors are sequentially selected by the overlapping phases of the two switches on either side of each capacitor. The clock signals on the same side of the filter still need to be non-overlapping to prevent discharging the capacitors during switch over time. The 25% duty cycle clock pulses are twice as wide and easier to distribute and enable the operation at higher frequencies. Instead of the conventional divide-by-8 ring counter [43], a lower power divide-by-4 dual-edge-triggered latch divider operating at half the frequency is used for clock generation. The state machine of the divider feedback guarantees a unique dividing mode, so flip-flop start-up reset is not required. The clock frequency can be tuned between 0.8GHz to 6.4GHz corresponding to a 0.2GHz to 1.6GHz

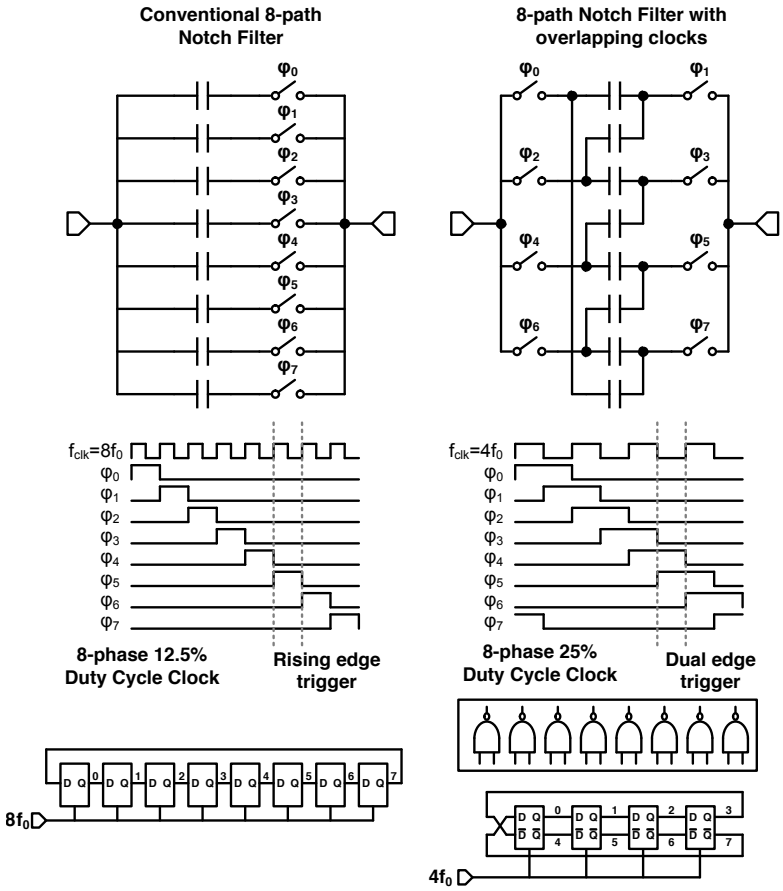


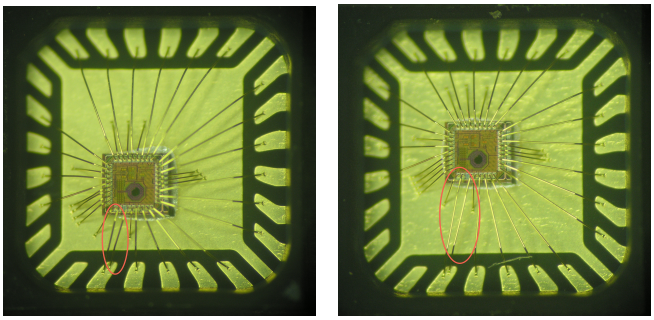
Figure 4.11: Comparison between (left) a conventional 8-path notch filter at f_0 with 12.5% duty-cycle clocks requiring a clock generator at $8f_0$ and (right) the proposed 8-path notch filter at f_0 with dual-edge triggered 8-phase 25% duty-cycle clocks only needing a clock generator at $4f_0$.

frequency tuning range for the notch filter. By employing these techniques, the measured power consumption of the N-path filter is reduced to only 1mA at 200MHz and 5.5mA at 1.6GHz from V_{DD} of 1V.

The analysis of the proposed N-path notch filter is similar as for the conventional topology. Non-idealities such as phase mismatch among different clock phases will cause clock emission and harmonic folding and phase noise of the clock will cause reciprocal mixing [43]. In contrast to the conventional N-path notch filter where the blocker to be rejected is at the same frequency of the clock, in the IR-LNA the blockers are in the passband of the notch filter. This makes the reciprocal mixing less an issue [43].

On-Chip LC Filter: An alternate solution is to realize the notch filter with on-chip spiral inductor (1.1nH) and a switchable array of MiM capacitors (4.2pF to 6pF). This is a fully integrated solution but has lower Qs (< 15) and thus poorer selectivity ($R \approx 250\Omega$, loaded $Q \approx 1.3$ without IR-Loop). However, there are no concerns about clock leakage.

Bondwire LC Filter: Bondwires can offer a high Q alternative ($Q > 20$ [59]) to realize the inductors. At packaging time the wire length can also be altered to program the frequency while the on-chip capacitors can be programmed in the field from 4.2pF to 6pF for fine tuning. Fig. 4.12 illustrates the approach for a QFN package where a floating pin is used as an intermediate landing point.



(a) (b)

Figure 4.12: Different bonding options enables filter frequency programmability at packaging time: (a) low inductance with short bond wires (approximately 1nH) (b) high inductance with longer bondwires (approximately 1.5nH).

4.4.4 Stability Analysis

The uncertain antenna impedance complicates the stability analysis of the LNA with IR loop substantially. Whereas in-band a matched source impedance can typically be assumed, the out-of-band impedance can vary widely. Stability factors or source and load stability circles [56] are used to evaluate amplifiers with uncertain source *and* load impedance. In the IR-LNA the load impedance is well defined since it is intended to be used with an on-chip downconverter[6]. The LNA can thus be analyzed as a one-port network with varying source impedance. As long as the real part of the LNA input impedance remains strictly positive across a wide frequency range, the amplifier will be stable for any arbitrary passive source impedance. However, for the N-path filter case, the LNA input impedance depends on the source impedance and we have to resort to simulation to evaluate the LNA input impedance for varying source impedances.

A set of periodic steady-state AC simulations are run with 45 different complex source impedance values (Fig. 4.13(a)). Each simulation spans from 10MHz to 10GHz with linear 10MHz steps. At

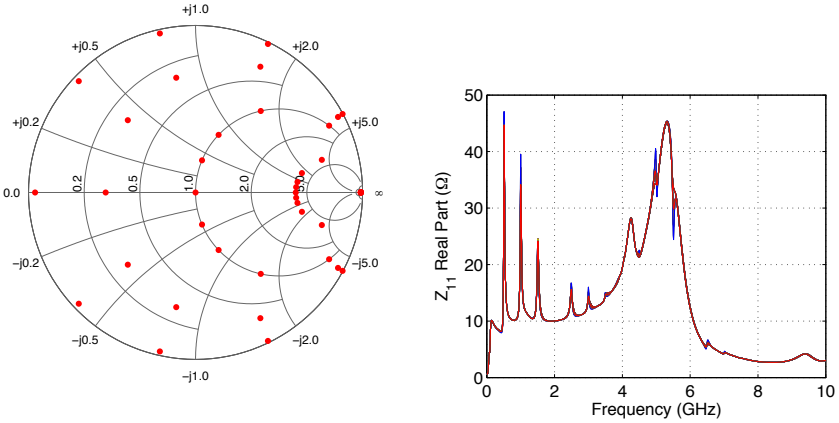
[6]In our proof-of-principle prototype an on-chip buffer or resistive probe are used; both also have a well defined impedance subject to minor process variations.

frequency below 10MHz, the source impedance is shorted out by the RF choke for the CG stage biasing and the circuit does not have enough loop gain to oscillate. Beyond 10GHz, the LNA has little gain limited by finite circuit bandwidth. The input impedance Z_{11} of the LNA is calculated as the ratio of the AC LNA input voltage and the AC current flowing into the LNA. The real part of Z_{11} is plotted in Fig. 4.13(b) across 45 simulations with the N-path notch filter operating frequency set to 500MHz. The spikes at low frequencies come from the fundamental and harmonic responses of the N-path notch filter in combination with the effect of the IR-Loop. The simulations show an in-band impedance close to 50Ω and low out-of-band impedance, as is expected from the analysis of the IR-Loop operation. The high impedance around 5GHz is an artifact when operating close to the bandwidth of the feedback loop. Other spurious responses are due to package parasitics.

The changes in source impedance only marginally change the impedance profile around the in-band responses of the N-path filter. All the input impedance profiles have a strictly positive real part, which guarantees stability for sources with passive impedance.

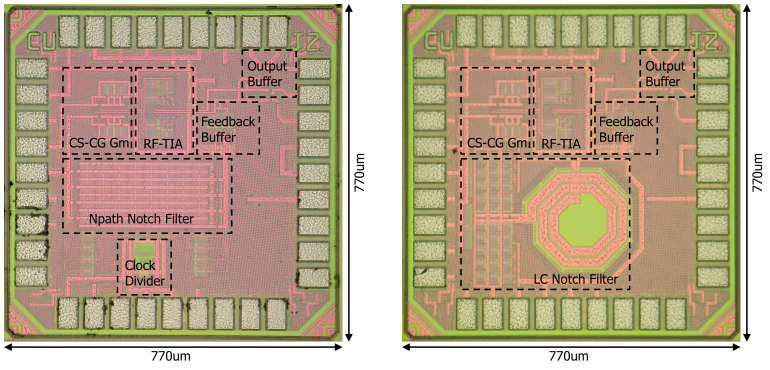
4.5 Experimental Results

A family of FP LNAs with IR-Loop linearity enhancement have been implemented in 65nm CMOS using an identical LNA core but with different notch filters; the first prototype (Fig. 4.14(a)) uses an 8-path tunable notch filter and the second prototype with passive LC notch filters (Fig. 4.14(b)) can be used with an on-chip capacitor array and an on-chip inductor or a bondwire inductor. For noise figure measurements the LNA drives a differential output buffer that rejects the common-mode noise; a pair of resistive probes are used for the linearity measurements (Fig. 4.9).



(a) (b)

Figure 4.13: Forty five different source impedance values have been used in simulation to verify the stability of the IR-Loop against source impedance variations. (a) The 45 source impedance points chosen to evaluate the stability of the IR-Loop cover the Smith chart. (b) The real part of Z_{I1} simulation results from 10MHz to 10GHz under the 45 source impedance values. The input impedance of the IR-LNA is marginally affected by the source impedance variation and the strictly positive input impedance guarantees stable operation.



(a) (b)

Figure 4.14: (a) IR-LNA 65nm CMOS prototype using an 8-path notch filter; (b) IR-LNA prototype using on-chip LC filter or bondwire-L-C filter; both prototypes have an active area of 0.2mm^2.

4.5.1 Characterization of the Field-Programmable Noise-Canceling LNA Core

Fig. 4.15(a) shows the single-ended to differential small signal gain of the core wideband noise-canceling LNA with the IR loop disabled. The amplifier operates with programmable gain from 200MHz to 2GHz; e.g., at 1GHz, the gain is programmable from 14dB to 22dB. The gain imbalance (Fig. 4.15(b)) is within $\pm$1dB and the phase imbalance (Fig. 4.15(c)) is around 2° at 0.2GHz and gradually degrades to 15° as frequency increases to 2GHz. Fig. 4.16(a) shows open-loop NF measurements with different numbers of CS G_m cells enabled; the feedback resistors in the transimpedance stage are adjusted in tandem so that the gain remains balanced. Decreasing the number of active CS G_m elements reduces the power consumption but degrades the NF (Fig. 4.16(b)); e.g., at 800MHz, 2.2mA of DC current can be saved at the cost of a 2.4dB NF penalty. A user can thus dynamically trade power vs. sensitivity depending on operating conditions in the field.

4.5.2 Characterization of the FP IR-LNA with 8-Path Notch Filter

The measured gain and input matching of the N-path filter chip with the IR loop active and inactive is shown in Fig. 4.17(a); the operation-band center frequency can be tuned from 200MHz to 1.6GHz while the 3dB bandwidth remains constant at 20MHz; the second order response of the N-path filter can be clearly observed. The in-band S_{11} is lower than -10dB for operating frequencies below 1GHz and degrades for higher operating frequencies bands due to the pulling by the parasitic capacitance at the LNA input. Fig. 4.17(b) shows the operation at 800MHz for varying gain codes; as the gain is reduced, the loop gain reduces and the out-of-band S_{11} reduces, but in-band matching is not affected by the gain tuning. The measured NF with and without the IR-Loop is

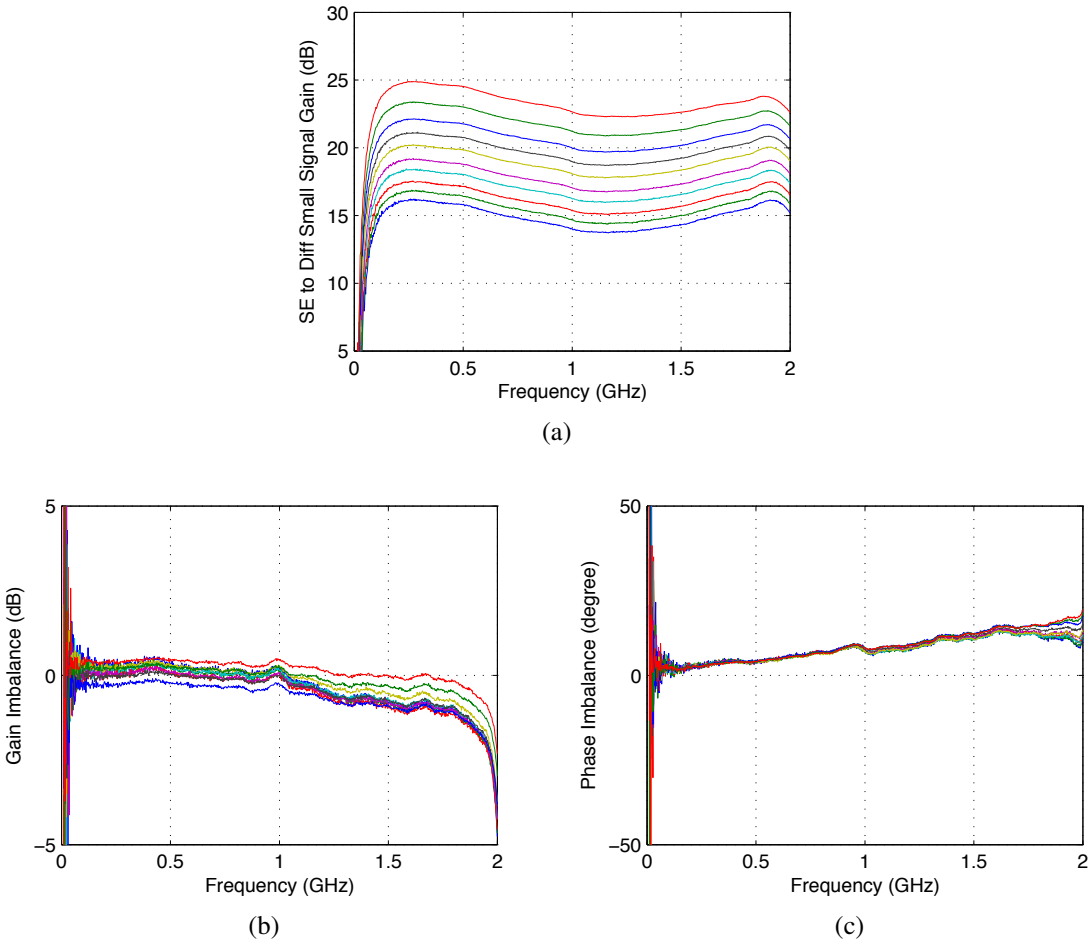
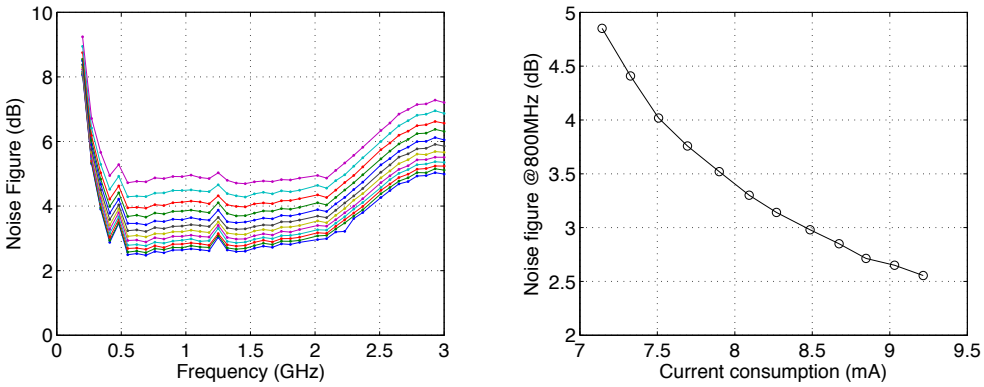
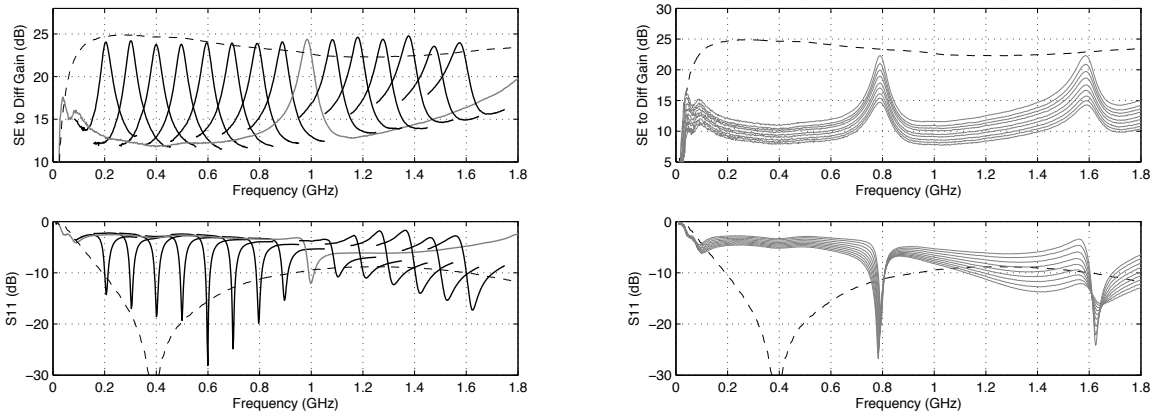


Figure 4.15: (a) Measured single-ended to differential small-signal gain across different gain codes and without the IR-Loop active; (b) gain imbalance of CS and CG outputs; (c) phase imbalance of the CS and CG outputs.



(a) (b)

Figure 4.16: (a) Measured NF without IR-loop for different common-source stage configuration codes; (b) NF at 800MHz without IR-loop vs. total LNA DC current consumption for the different common-source stage configurations.



(a) (b)

Figure 4.17: (a) Measured programmable operation at different frequencies of the IR-LNA with the N-path notch filter programmed by the clock frequency; (b) programmable operation at a given frequency with varying gain.

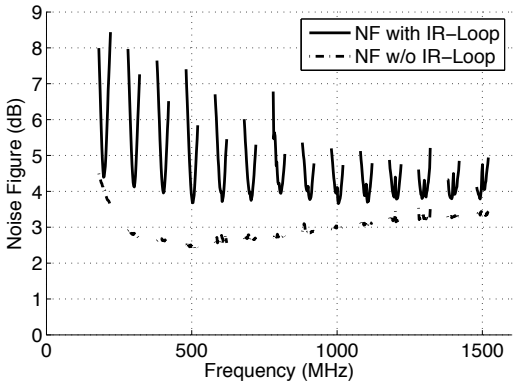


Figure 4.18: NF of the IR-LNA with N-path notch filter with and without the IR-Loop.

shown in Fig. 4.18; engaging the IR-Loop[7] degrades the NF by approximately 1.1dB. The 8-path filter inherently introduces >0.35dB noise folding from high-order harmonics [38]; the additional NF degradation might come from flicker noise of the LO divider and switch drivers [42]. The IR-Loop suppresses interferers at the input of the LNA and improves the linearity. For an out-of-band signal at an 80MHz offset S_{11} is -3.3dB so the IR-Loop has an A_R of 10dB (Fig. 4.17), and the B_{1dB} improves from -15dBm to -4dBm (Fig. 4.19(a)) close to the 10dB predicted by (4.14). Engaging the IR-Loop improves the $OOB\text{-}IIP_3$ from +2.5dBm to +14.5dBm at an 75MHz offset (Fig. 4.19(b)), which is close to the value predicted by (4.13); Fig. 4.19(c) shows the B_{1dB} and $OOB\text{-}IIP_3$ improvements vs. offset frequency. The in-band LO emission is measured to be -69dBm at low operating frequencies and gradually increases to -50dBm at 2GHz. This is mainly due to phase mismatches in the N-path filter.

[7]The in-band variation of the NF is due to the parasitic capacitor at the LNA input which pulls the LNA gain response peak slightly lower than the N-path filter center frequency. The gain minimizes noise contribution from the load resistors, whereas the feedback buffer noise is minimized the N-path notch filter. The combination of these two effects explains the in-band NF variation.

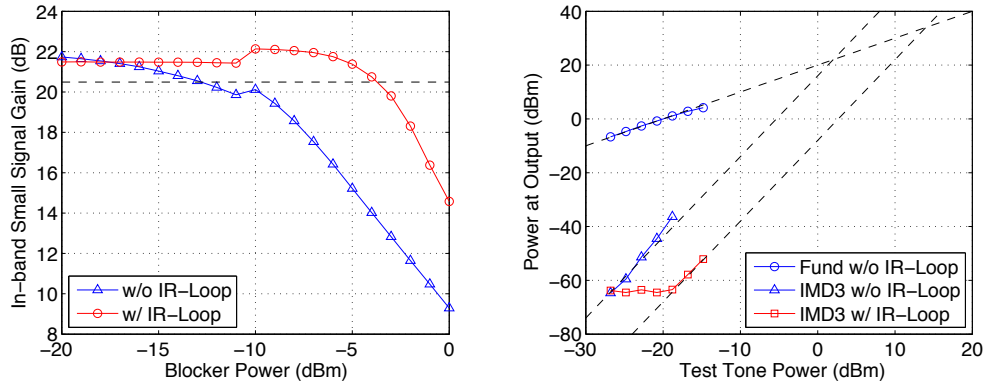
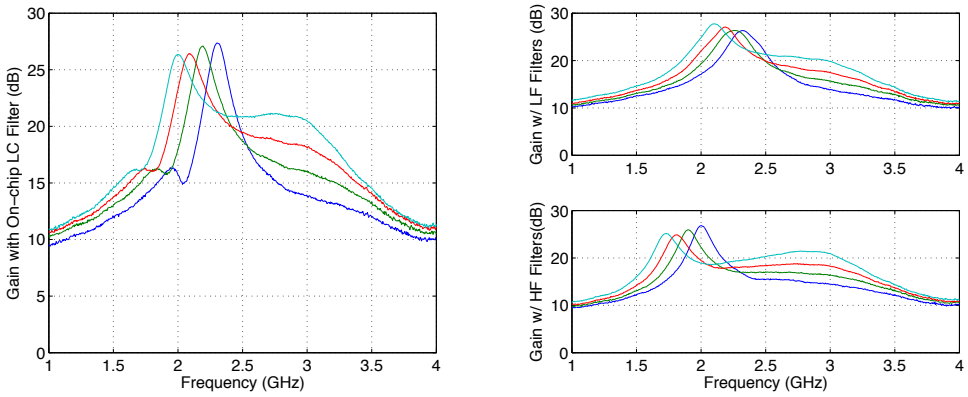


Figure 4.19: Linearity measurements for the IR-LNA with N-path notch filter: (a) B_{1dB} improvement at 80MHz offset; (b) out-of-band IIP_3 improvement at 75MHz offset; (c) B_{1dB} and IIP_3 improvement vs. offset frequency



(a) (b)

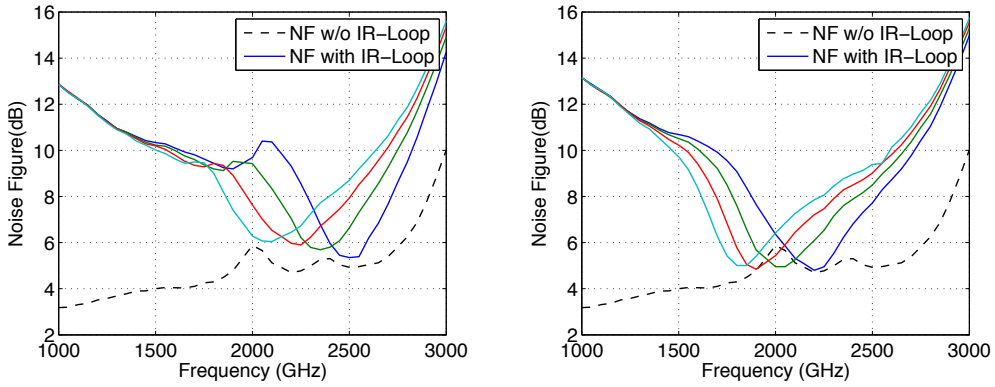
Figure 4.20: (a) Single-ended to differential small-signal gain for the IR LNA with on-chip LC tank; (b) single-ended to differential small-signal gain for the IR-LNA with bondwire LC tanks: (top) short bondwires and (bottom) long bondwires.

4.5.3 Characterization of the FP IR-LNAs with Passive LC Notch Filters

By tuning the capacitor in the on-chip LC filter in the IR loop, the LNA can operate[8] from 2GHz to 2.4GHz (Fig. 4.20(a)); at lower frequencies the tank Q degrades due to lower inductor Q and more switch loss in the capacitor arrays as more capacitors are switched in; the LNA gain code has been adjusted to overcome the gain degradation. Fig. 4.20(b) shows the operation of the IR-LNA with the bondwire LC notch filter; two sets of chips were packaged with different bondwire lengths, demonstrating coarse programming at packaging time. Further programming is achieved with the on-chip programmable capacitor bank. Fig. 4.21(a) and Fig. 4.21(b) show the NF measurements with the IR loop active and inactive for the on-chip LC filter and bondwire LC filter. These IR-LNAs operate close to the upper bandwidth of the core LNA which results in a higher NF for the IR-LNA[9]; more pronounced phase mismatches at higher frequencies in the CG branch also result

[8]The small notch on the left side of the peak response is due to the interaction with the bondwire based filter tank. This can be avoided in future implementions.

[9]The bumps around 2GHz and 2.4GHz in the NF measurement without the IR loop are measurement artifacts.



(a) (b)

Figure 4.21: Measured NF of the IR-LNA with (a) on-chip LC filter and (b) bondwire LC filter with and without the IR loop active.

in poorer noise canceling. The on-chip LC version has a higher NF due to a poorer filter quality factor compared to the bondwire LC. Activating the IR loop (Fig. 4.22) improves the B_{1dB} from -9dBm to -5dBm in the on-chip LC case and -2dBm in the bondwire LC case [10]. The LC notch filter LNAs operate with a lower gain for improved stability because the notch filters operate close to the corner frequency of the LNA. As a result, A_R is limited to 5dB.

4.5.4 Discussion

The performance of the FP-IR-LNAs is summarized in Table 4.1 and is compared to state-of-the-art programmable LNAs in Table 4.2. The IR-LNAs offer more programmability features than the state-of-art programmable LNAs [30, 32, 33, 36, 48]. Also, comparing to these LNAs at maximum gain, the IR-LNA has much higher out-of-band linearity with the IR loop activated. The N-path filter based IR-LNA is further compared with state-of-the-art linearity enhancement techniques

[10] The larger B_{1dB} might be caused by the interaction between the parasitics in the bondwire filter and the feedback buffer.

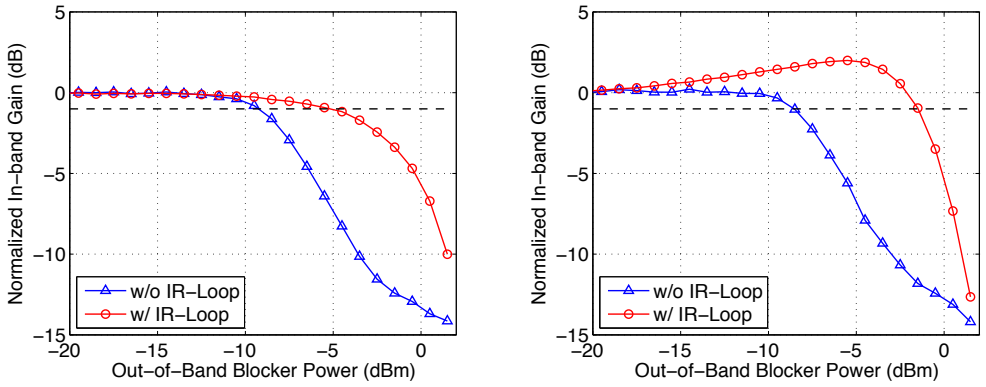


Figure 4.22: Measured B_{1dB} improvement for the IR-LNA with a 900MHz blocker (a) on-chip LC filter tuned to 2GHz and (b) short bondwire filter tuned to 2.1GHz.

Table 4.1: Performance Summary

	Open Loop	N-path Filter IR Loop	On-chip LC IR Loop	Bondwire LC IR Loop
Frequency (GHz)	0.1-2.1	0.2-1.6	2-2.4	1.7-2 / 2.1-2.4*
Gain (dB)	14-22	14-24	16-27	16-28
NF (dB)	2.4	3.6	5.4	4.9
B1dB-CP (dBm)	-15	-4	-5	-2
Analog Current (mA)	8.1	9.2	9.2	9.2
LO Current (mA)	0	1.1-5.5	0	0
Power Supply (V)	1.6 (Analog)	1.6 (Analog) / 1.0 (LO)	1.6 (Analog)	1.6 (Analog)
Power Consumption (mW)	13	15.8 - 20.2	14.7	14.7

* Long bondwire / short bondwire

in LNAs, receiver front ends and bandpass N-path filters in Table 4.3. Note that these designs do not have, or have much more limited programmable NF, gain, operating frequency or linearity. Compared to translational loop techniques [35,45,48,51,53], the IR-LNA has superior out-of-band IIP_3 performance. Due to the finite wideband loop gain adopted for agnostic blocker rejection, the B_{1dB} performance of the current IR-LNA prototype is not as high as [10, 39, 42, 45]. But the IR-LNA consumes more than three times less clock power. In future versions, more power can be

Table 4.2: Comparison of the FP-IR-LNA to other state-of-the-art Programmable LNAs

	This Work	[29]	[31]	[32]	[35]	[47]
Topology	Noise Canceling	Common Gate	Resistive Feedback	Resistive Feedback	Inductive Degeneration	Inductive Degeneration
Programmable Gain	✔	✔	✔	✔	✖	✖
Programmable Frequency	✔	✖	✔	✖	✔	✔
Programmable RF Selectivity*	✔	✖	✖	✖	✖	✔
NF - Power Scalable	✔	✖	✖	✔	✖	✖
Linearity - Power Scalable	✔	✖	✔	✔	✖	✔

*The ability to activate/deactivate RF filtering

Table 4.3: Comparison of the N-path IR-LNA to other state-of-the-art LNAs and receivers

Design Type	LNA									Receiver								N-path Filter	
Reference	This Work		[29]		[31]	[32]	[35]	[47]		[9]		[34]	[41]	[44]		[50]	[52]	[38]	[42]
Topology	FP Noise-Canceling LNA		Common Gate		Resistive Feedback	Resistive Feedback	Inductive Degen.	Feedback Trans. Loop		Feedforward Cancellation		Feedback Trans. Loop	Feedback Tran. Loop	Feedback Tran. Loop		Mixer First	Freq Trans Noise Canceling	6th-order Bandpass	2nd-order Notch
CMOS Technology	65nm		130nm		90nm	180nm	90nm	65nm		65nm		45nm	65nm	65nm		65nm	40nm	65nm	65nm
Linearity Enhancement	Off	On	Min	Max*				Off	On	Off	On			Off	On				
Frequency (GHz)	0.1-2.1	0.2-1.6	0.048-0.86		0.1-6	0.1-1	2.1-6	1.9		1.9		0.9-2.1	1.3-2.85	2-6		0.05-2.4	0.08-2.7	0.1-1.2	0.1-1.2
Gain (dB)	13-22	14-24	19.8	-35.4	0-21.5	12.8	16.9	24.7	22.5	23.4	20.9	37	48-52	43	41	80	70	25	-1.4
NF (dB)	2.4	3.6	1.9	51	2.7	1.88	2.16	7	7.2	3.9	6.8	2.7	5-6.5	3.2	5.7	5.5	2	2.8	1.2
OB IIP3 (dBm)	+2.5	+14.5	+9.1	+28	-8.6	-16.3	0.5	N/R	N/R	+2.6	N/R	+1.5	-2.3	-13	-5	+27	+13.5	+26	+18
B1dB-CP (dBm)	-15	-4	N/R	N/R	N/R	N/R	N/R	-30**	-18**	N/R	0	N/R	N/R	-23	-16	+5**	0	+7	+6
Analog Current (mA)	8.1	9.2	3	5	10-26.8	12.6	3-20.3	N/R	150	8	8	7.3	25	26	26	12	24	11.7	N/A
LO Current (mA)	0	1.1-5.5	N/A	N/A	N/A	N/A	N/A	N/R	N/R	0	21	N/R	N/R	0	31	6-33	3-36	3-36	2-16
Power Supply (V)	1.6 (Analog) / 1.0 (LO)		1.8		1.2	1.8	1.2	2.5		2.5(Analog) / 1.2(LO)		1.3	1.2	1.2		1.2(RF) / 2.5(BB)	1.3	1.2	1**
Power Consumption (mW)	13	15.8-20.2	5.4	9	12-32.2	22.7	3.6-24.3	N/R	375	20	45.2	9.5	30	31.2	68	37-70	35.1-78	18-57.4	2-16

N/R = Not Reported, N/A = Not Applicable

*Bypass Attenuation Mode **Estimated

used in the feedback buffer and switches to further improve out-of-band linearity. The IR-LNA also performs broadband blocker rejection without needing to know the blocker frequency as in [43].

4.6 Conclusions

In this chapter, a family of field-programmable interferer-reflecting LNAs are analyzed, implemented and measured. The proposed LNA architecture is highly programmable in terms of gain, NF and linearity. An LNA input linearity enhancement technique named interferer reflection is further proposed and delivers blocker agnostic linearity improvement. The technique can be im-

plemented with N-path notch filters when wide tuning range and high Q filtering are required. If clock emission or harmonic folding are of concern, LTI notch filters such as on-chip LC or bondwire-LC filters can be used The selectivity of the notch filters is improved with the IR-Loop without a significant noise penalty.

Chapter 5

Achieving Rail-to-Rail Blocker Resilience with Field-Programmable Hybrid Class-AB-C LNTAs

5.1 Introduction

Modern wireless communication systems need to support multiple wireless standards and an increasing number of frequency bands. As the wireless spectrum become more congested, interference management and mitigation becomes very challenging. Traditional receiver solutions often use high quality SAW filters at the RF input to reduce the level of out-of-band interferers. Such filters are usually not tunable in terms of their center frequency and bandwidth and are not suitable for wideband software defined radios (SDR). State-of-the-art wideband SAW-less SDR receivers

often use low noise transconductance amplifiers (LNTAs) combined with current-driven passive downconversion mixers and/or N-path filters to avoid voltage-domain amplification of the blockers at RF frequencies. Such current-mode operation improves the out-of-band linearity such as $OB\text{-}IIP_3$ and B_{1dB}.

One of the challenges of using LNTAs for SDRs is the receiver input impedance matching requirement. Various circuit techniques have been demonstrated to achieve impedance matching with NF penalties as low as possible. Fig. 5.1 shows several existing antenna interface solutions with LNTAs. Some receivers use g_m-boosted common-gate (CG) LNTAs for a wideband 50Ω input impedance [9]. Frequency-translational noise cancellation (FTNC) receivers [10] use a mixer-first receiver path or an CG LNTA path for input impedance matching and a common-source (CS) LNTA path for noise cancellation. Frequency-translational quadrature hybrid (FTQH) receiver (see Chapter 6) addresses the problem with a quadrature hybrid (QH) coupler and two identical CS LNTAs. Input impedance matching is guaranteed with balanced operation and the thermal noise from the termination resistor is cancelled at the baseband. CS LNTAs can also pair with translation loops (see Chapter 4) to maintain in-band RF input impedance matching [35] [60]. For voltage mode resistive feedback LNAs loaded with N-path filters [61] [62], the LNAs do not benefit from the feedback loop due to the low loop gain at out-of-band frequencies. At these frequencies, the linearity of the LNA approaches to that of the transconductor (G_m) cells used to implement the LNA.

The out-of-band linearity of these circuits is often limited by the linearity of the LNTAs as the rest of the signal chain are protected by filters before applying voltage gains to the out-of-band

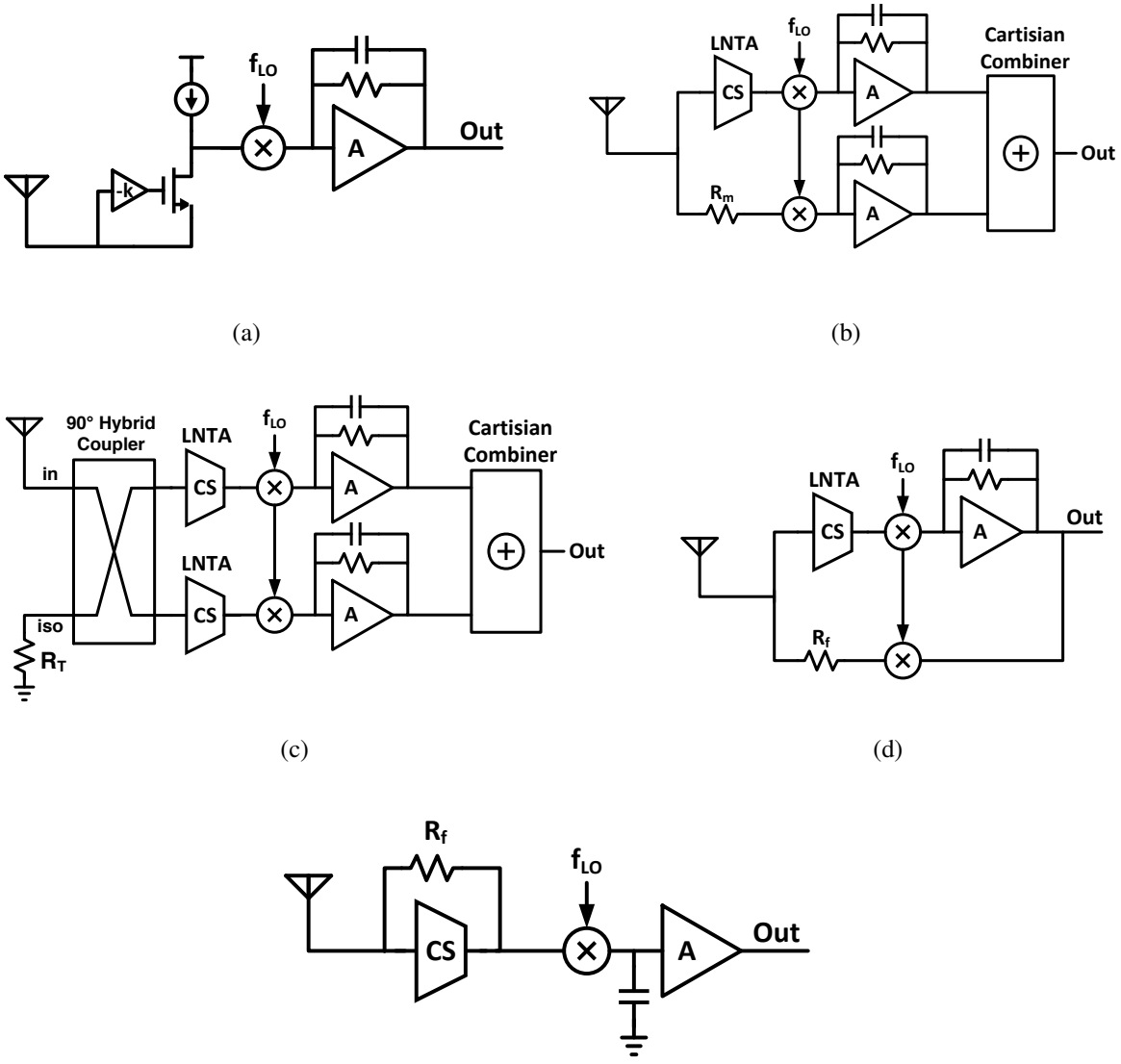


Figure 5.1: Existing antenna impedance matching solutions for LNTA based wideband receivers: (a) G_m boosted common gate LNTA; (b) frequency-translational noise-canceling (FTNC) receiver; (c) frequency-translational quadrature hybrid (FTQH) receiver; (d) negative feedback translation loop; (e) resistive feedback LNA with an N-path filter mixer.

interferers. As discussed in Chapter 1, field programmability for dynamic performance tradeoff between NF, linearity and power can help to optimize the power consumption of the receiver when extreme performance is not needed. Thus, field-programmable high-performance RF LNTAs are critical building blocks for next-generation high-performance SDR receivers. In this chapter, we present a family of noise canceling LNTAs with robust biasing circuits and demonstrate their resilience to extremely large blockers with rail-to-rail swings. The LNTAs are integrated into a wideband SAW-less receiver front end to evaluate their performance.

5.2 RF Transconductor Linearization Techniques

RF transconductors (G_m) cells are the basic building components for LNTAs and their linearity directly impacts the out-of-band linearity of the full receiver signal chain. In this section, we briefly review the existing RF G_m cell linearization techniques and discuss their advantages and limitations.

5.2.1 Large Signal Linearity vs. Small Signal Linearity

The linearity of a G_m cell can often be characterized by its small-signal linearity and large-signal linearity, and they affect the performance of the receiver in different ways.

When multiple interferers are seen by the circuit, the finite small-signal linearity of the G_m cell can generate undesired distortion signals through mechanisms such as intermodulation or cross modulation. With certain frequency location relationships between interferers and the desired signal, the distortion product can fall on top of the desired signal and corrupt its SNR. The small-

signal linearity is usually quantified by specifications such as the second-order and third-order intercept point (IIP_2, IIP_3) for intermodulation distortions and the third-order triple-beat (TB_3) for the cross modulation.

To analyze the small signal linearity, an wideband G_m cell is often modeled with a memoryless weak distortion. The I-V transfer characteristic of the G_m cell can be represented by a third-order polynomial in the form of:

$$I_{out} = a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3. \tag{5.1}$$

And IIP_3, IIP_2, and TB_3 can be calculated with ratios of the polynomial coefficients. The memoryless assumption is typically valid if the bandwidth of the signals are much lower than the analog bandwidth of the G_m cell. The polynomial is often obtained from a truncated Taylor series where the high-order terms are negligible. This assumption is only valid when the excursion of the input voltage stays within the confidence interval of the Taylor series. This is a versatile model for circuits with weak distortions. However, if the interferer signals are large enough and the G_m cell starts to see hard nonlinearities such as clipping, the higher order terms in the Taylor series quickly grows to significant levels and cannot be neglected. In the presence of clipping behaviors, increasing the number of terms in the polynomial cannot effectively extend the confidence interval of the model.

The large signal linearity mainly affects the performance of the receiver through the mechanism of blocking. Very large interferer can cause receiver saturation where the gain of desired signal is severely compressed and the SNR is degraded. The large signal linearity is usually quantified by specifications such as the 1dB compression point (P_{1dB}) and 1dB blocking point (B_{1dB}). P_{1dB} is

defined as the interferer power level where the *gain of the interferer* is compressed by 1dB. B_{1dB} is defined as the power level of an out-of-band interferer where the gain of an in-band small signal is compressed by 1dB.

The large signal linearity is often limited by the hard clippings in the transfer curve of the device where the device is cut off or goes into the triode region. The linear input range without compression can often be estimated by inspecting the bias point and the swing limits on the transfer curve.

Both the small-signal and large-signal linearity are both important metrics that determines the receiver's resilience to interferers. LNTA linearization techniques should consider both types of linearity depending on the application scenarios.

5.2.2 LNTA Linearity Enhancement with Derivative Superposition

The I-V transfer curve of a MOS transistor in the weak-inversion region has expanding nonlinearity due to the exponential I-V relation ($a_3 > 0$). In strong inversion, it has compressing nonlinearity due to velocity saturation and eventually goes into the triode region ($a_3 < 0$). The linearity of the LNTA can be improved with the derivative superposition (DS) technique where multiple transistors are used in parallel with different bias voltages. The third order small signal distortion products from the weak-inversion biased transistors and the strong-inversion biased transistors cancel out with each other and IIP_3 is improved as a result. The cancellation is optimum when the combined transfer curve has a zero third order derivative at the bias point and thus such methods are named

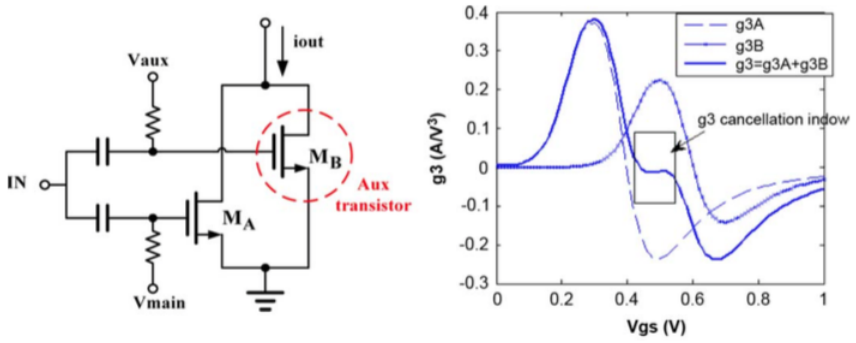


Figure 5.2: The derivative superposition technique with two NMOS transistors biased in weak and strong inversions respectively [2]. The third order derivatives cancel out with each other around a V_{gs} of 0.45V.

derivative superposition (DS). Fig. 5.2 ([2]) shows an example of two NMOS transistors combined with the DS method.

The DS method can effectively improve the small signal linearity in principle, but it still has several drawbacks with practical implementation. First, the region where the cancellation happens is limited and can only work with relatively small signal swings. In cases such as third-order triple beat (TB_3), where a strong modulated interferer is involved, the input voltage excursion can go beyond the small cancellation region and the simple third-order polynomial model is no longer valid. For a similar reason, simple DS methods do not improve the large-signal linearity. Second, the DS technique requires carefully tuned device size ratios and biasing schemes to align the devices with opposite derivative signs. The device sizing and biasing are sensitive to process, voltage and temperature (PVT) variations. And the design is at the mercy of the accuracy of the device model.

5.2.3 Resistive Source Degeneration

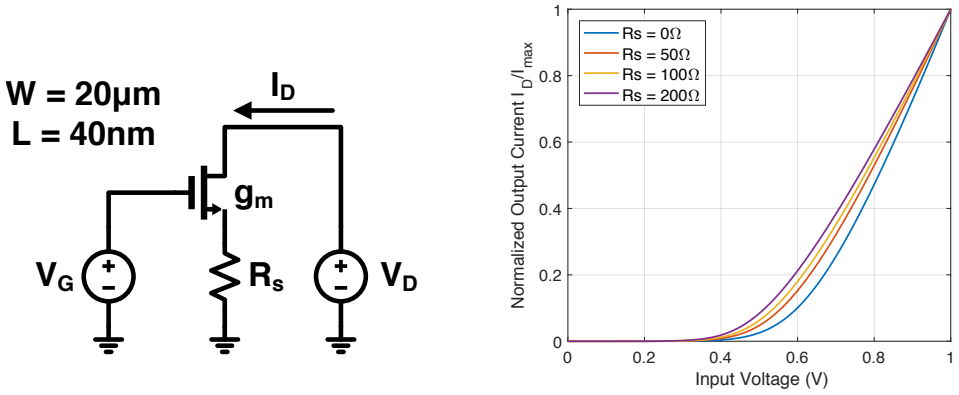
Resistive source degeneration is a transconductor linearization technique widely used in analog circuits [8]. It can be considered as a series-series feedback with the degeneration resistor as the feedback network. Take a source-degenerated common-source transconductance amplifier for example (Fig. 5.3(a)), the degeneration resistor R_s reduces the overall transconductance gain (G_m) but linearizes the transfer curve of the amplifier. The G_m of the amplifier at a specific bias point can be expressed as:

$$G_m = \frac{g_m}{1 + g_m R_s}. \tag{5.2}$$

Where g_m is the transconductance of the NMOS. It can be observed that when the loop gain $g_m R_s$ becomes much larger than 1, G_m will be determined by the feedback component as $1/R_s$. Consider different biasing conditions of the NMOS. When biased in weak inversion, $g_m R_s$ is small and $G_m \approx g_m$, and we still see the exponential behavior. When biased in strong inversion, $g_m R_s$ is large and the transfer curve is linearized by the feedback.

Shown in Fig. 5.3(b) are the simulated transfer curves of a resistive degenerated transconductance cell with different R_s values. The transfer curves are normalized with their maximum drain current at a 1V input voltage (V_G). It can be observed that the transfer curve in strong inversion regions become more linear as R_s inceases Fig. 5.3(b).

Fig. 5.4 shows the third order derivative (g_3) of the simulated transfer curves (Fig. 5.3). The increasing the resistive degeneration does not fundamentally change the overall profile of the third order derivatives but rather shift the profile curve to lower voltages. When biased at a fixed V_G, for



(a) (b)

Figure 5.3: Simulated DC transfer curves of (a) an NMOS transconductor with resistive source degeneration; (b) normalized DC transfer curves with a progressively larger degeneration resistor.

example 0.65V, g_3 reduces as R_s increases, which translates into better small-signal linearity such as IIP_3.

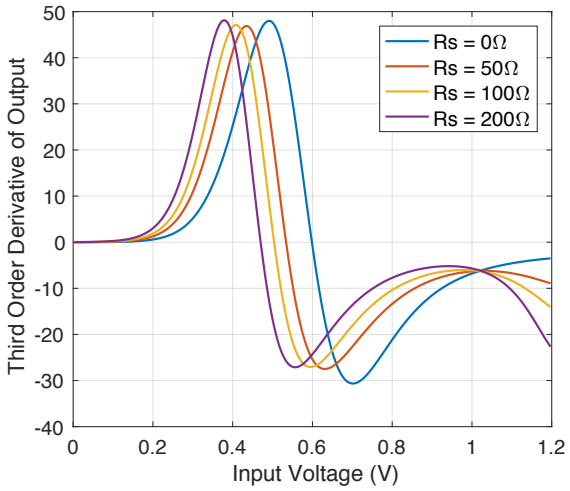


Figure 5.4: The third order derivative of the transfer curves shown in Fig. 5.3. The profile is shifted to the left with a progressively higher degeneration resistor.

As for large signal linearity, the source degeneration has improvements on the cut off voltage, but has a penalty on the output headroom where the transistor goes into linear region. The source

degeneration reduces the voltage swing across the transistors. This can reduce the stress on the gate oxide of the MOS transistor and improve reliability under extremely large interferers.

The main penalty of resistive degeneration is the reduction in the equivalent transconductance comparing to a standalone device. This translates into a direct penalty in the f_T of the device.

5.3 Operation Principles of the Hybrid Class-AB-C LNTAs

The conventional transconductor linearization methods reviewed in the previous section can increase the small-signal linearity but have limited improvements on the large-signal linearity. In this section, we introduce a new LNTA topology that offers improvements on both the small-signal and large-signal linearity.

5.3.1 The Class-AB-C Transconductor

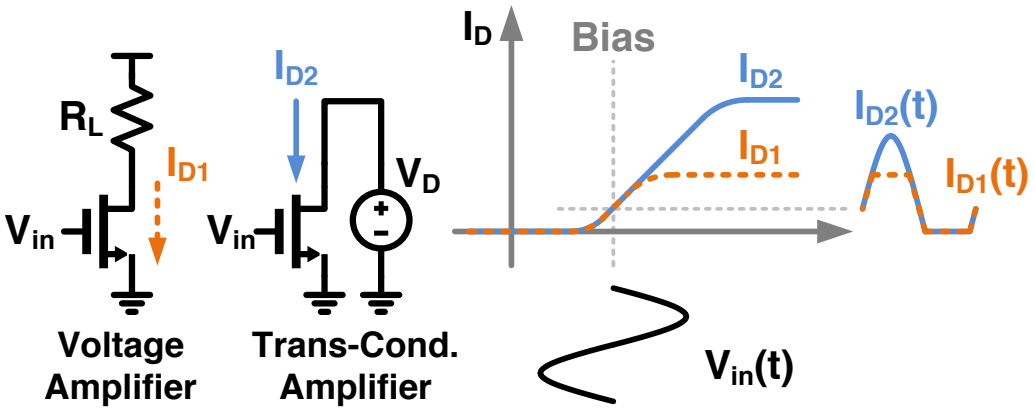
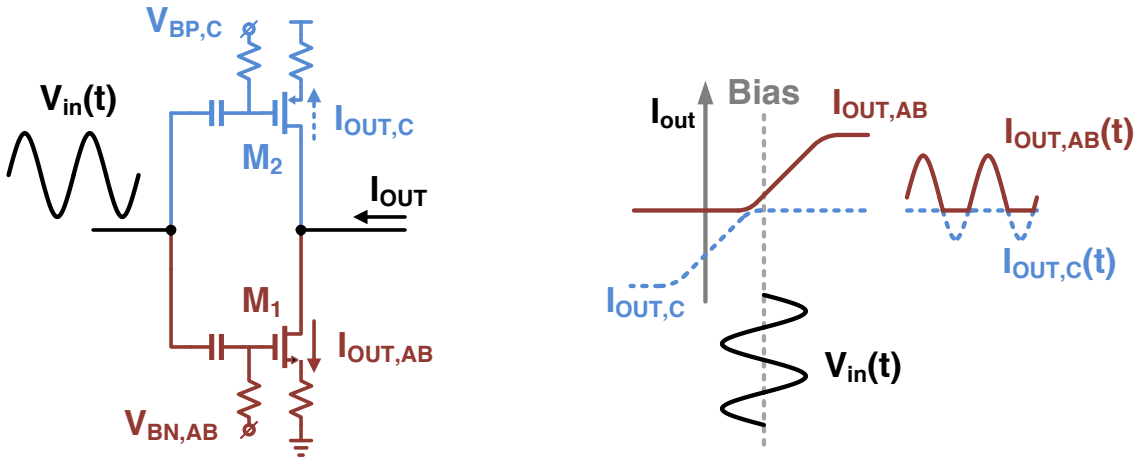


Figure 5.5: Compression mechanisms in a wideband voltage-mode amplifier and a wideband transconductance amplfiier.

Fig. 5.5 shows the DC I-V transfer curve of an NMOS CS transconductor (g_m cell) under different load configurations. In the first case, the g_m cell drives a load resistor and operates as a voltage amplifier, whereas in the second case, the g_m cell drives an idea current sink and operates as a transconductance amplifier. As the input voltage increases, the voltage amplifier goes into the triode region earlier than the transconductance amplifier due to the lower output voltage headroom. In common design practices, the NMOS transistors are often biased in the saturation region with an overdrive voltage of 150mV to 200mV to guarantee strong inversion operation. When a large voltage signal is applied to the NMOS input, the voltage amplifier suffers from clipping in both the cutoff region and the triode region, and the transconductance amplifier only suffers from cutoff clipping due to the extended saturation region thanks to the current-mode operation. The transconductance amplifier operates in class-AB mode under large input blockers. If class-A mode operation is desired to maximize the input voltage swing, the transistor must be biased at a higher overdrive voltage. However, such biasing schemes are often discouraged due to the increased power consumption.

In order to extend the input voltage swing of a NMOS g_m cell, we can introduce a complementary class-C biased PMOS device (Fig. 5.6). The PMOS device stays cutoff in quiescent and only pushes out current when a large input blocker is present. Its output current compliments the current from the class-AB NMOS device and the combined transfer curve of the two devices has a much larger linear operation range compare to the standalone class-AB transconductor. Due to the composite operation of class-AB and class-C, we name this type of amplifier a hybrid class-AB-C transconductor.



(a) (b)

Figure 5.6: The operation principle of the class-AB-C transconductance cell: (a) the simplified schematic; (b) the combined transfer curve extends the linear input voltage range and prevents clipping in the output current.

The input blocking point of this LNTA cell is no longer limited by the input linearity. The compression limit is now at the output voltage swing of the LNTA, which depends on the load impedance seen by the LNTA and the output swing headroom. With current-steering passive mixers, the output linearity can be maximized.

5.3.2 Class-AB-C Transfer Curve Alignment Non-idealities

The transfer curves of the class-AB and class-C devices need to be properly aligned to effectively improve the linear input swing range. The slope of the class-AB and class-C cells in their saturation regions need to be the same. The threshold voltage of the class-AB and class-C cells need to be aligned to prevent crossover distortion. And ideally, the shapes of the transition areas around the

thresholds need to match with each other. In this section, we discuss these non-idealities and their impact on the linearity performance of the LNTA.

In order to simplify the discussion of the transfer curve alignment, we use an empirical I-V model to capture the key aspects of the behavior of the MOS g_m cells. A two-region piece-wise linear model is used where the transfer curve is divided into the cutoff region and the saturation region. The output current is zero in the cutoff region and the slope of the curve equals g_{m0}. This simplified model does not capture the output compression of the transistors as it is not affected by the alignment non-idealities of the class-AB-C cells.

The impact of the transfer curve misalignment can be modeled as an error transfer curve superimposed onto a linear transfer curve that is expected for an ideal alignment. Fig. 5.7 demonstrates the non-idealities in the alignment and the corresponding error curves. When an interferer signal is applied, the error curve generates an error current in addition to the linear output. The error current can be expanded into harmonic components that affect the large-signal and small-signal linearities of the LNTA. The fundamental term of the error current creates compression to the signal, and the second and third-order harmonics affect the level of the intermodulation products.

Slope Mismatch

Slope mismatch between the class-AB and class-C cells results in an error transfer curve that has a even symmetry (Fig. 5.7(d)). It is equivalent to the distortion created by a device whose size equals the large signal g_m difference between the class-AB and class-C cells. The ratio of the slopes between the linear transfer curve and the error transfer curve (Fig. **??**) determines the

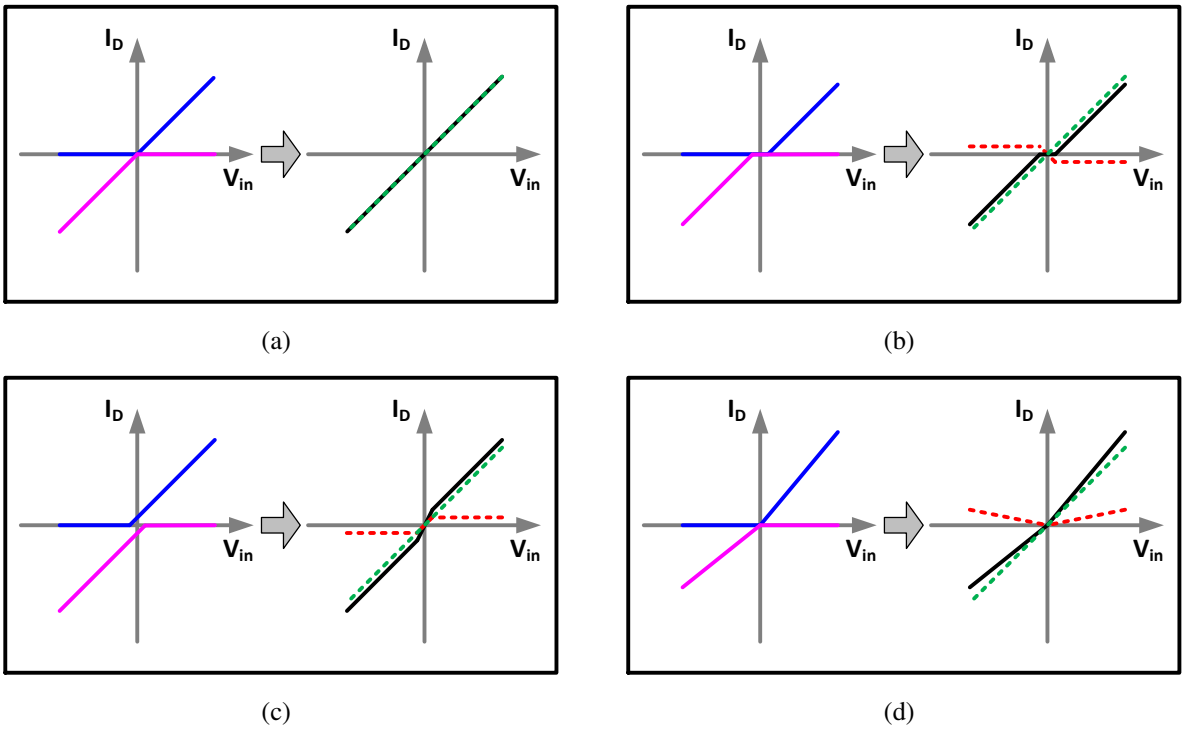


Figure 5.7: Illustration of the class-AB-C alignment non-idealities: (a) perfect alignment, (b) positive V_{th} misalignment with cross over distortion, (c) negative V_{th} misalignment (d) large signal slope mismatch.

maximum amount of gain compression when a large blocker is applied. IIP_2 is especially prone to the slope mismatch.

V_{th} alignment error

Another source of alignment error comes from the misalignment of the V_{th} of the class-AB and class-C G_m cells. In the presence of V_{th} misalignments (Fig. 5.7(b), Fig. 5.7(c)), the error curve only creates output currents when the signal crosses the alignment gap. If the signal swing is large enough, the error curve acts as a limiter and the error current is approximately a duty-cycled

square wave and does not increase with the input signal level. Thus, when the signal becomes large enough, the error term becomes relatively less prominent.

Transition Region Mismatch

The characteristics of the transition regions in the transfer curves need to meet certain criteria to realize perfect alignment that minimize both large-signal and small-signal nonlinearities. All high-order derivatives need to have symmetric profiles around V_{th} to achieve a perfect alignment. However, for physical MOS devices, the derivative profiles are typically asymmetric and cannot realize perfect derivative cancellation across all the operation region (Fig. 5.4). Thus, it is advised to avoid biasing the G_m cell near the V_th so that the small signal linearity is less sensitive to the alignment error.

5.4 Circuit Implementation

To validate the performance of the class-AB-C LNTAs, we designed and sent a prototype receiver chip out for fabrication in a 40nm CMOS LP technology. In this section, we discuss the architecture of the receiver prototype and the implementation of the circuit building blocks.

5.4.1 Receiver Architecture

The prototype receiver (Fig. 5.8) has an architecture similar to the FTNC receiver [10]. The mixer-first receiver in the main downconversion path is replaced with a CG LNTA to achieve a wideband input-impedance matching. The reverse isolation of the CG LNTA reduces the LO leakage to the

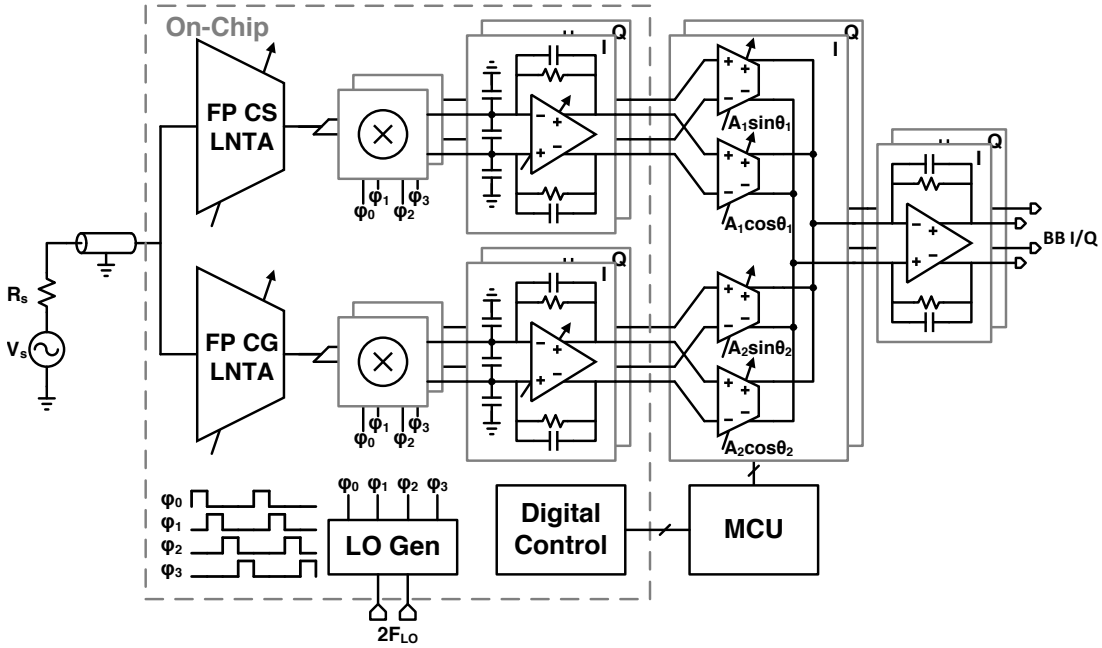


Figure 5.8: Block diagram of the wideband field-programmable prototype receiver with CS and CG class-AB-C LNTAs.

antenna. The noise of the CG LNTA is sensed by the CS LNTA and canceled in the complex baseband, and the receiver NF is dominated by the CS LNTA [10]. The programmable CS and CG LNTAs are followed by I/Q single balanced current-driven 4-phase passive mixers. The down-converted current signals are filtered and amplified by baseband transimpedance amplifiers (TIA) and then combined with appropriate phase and gain adjustments in the complex basebands[1]. The I/Q downconversion mixers use 4-phase 25%-duty-cycle clocks generated with a divide-by-2 circuit. The LNTAs are DC coupled to the passive mixers to reduce the load impedance seen by the LNTAs.

[1] In our prototype the baseband combiners are realized off-chip for testing flexibility.

5.4.2 Hybrid Class-AB-C LNTAs

Fig. 5.15(c) shows the detailed schematics of the class-AB-C CS and CG LNTAs. Both the CS and CG LNTAs are composed of cascode NMOS and PMOS G_m cells. The G_m cells have multiple source-degenerated slices and the bias voltage of each slice can be individually programmed. Multiple G_m slices share a single cascode device as shown in the schematic. Each CG LNTA G_m slice has a large signal transconductance of 30mS, and each CS LNTA G_m slice has a transconductance of 20mS. Each individual bias voltage can be programmed with an analog MUX into three different modes: class-AB, class-C and OFF. In class-AB mode the transistor is biased in strong inversion, in class-C mode the transistor is biased in deep weak inversion, and in the OFF mode the $|V_{GS}|$ is set to 0V.

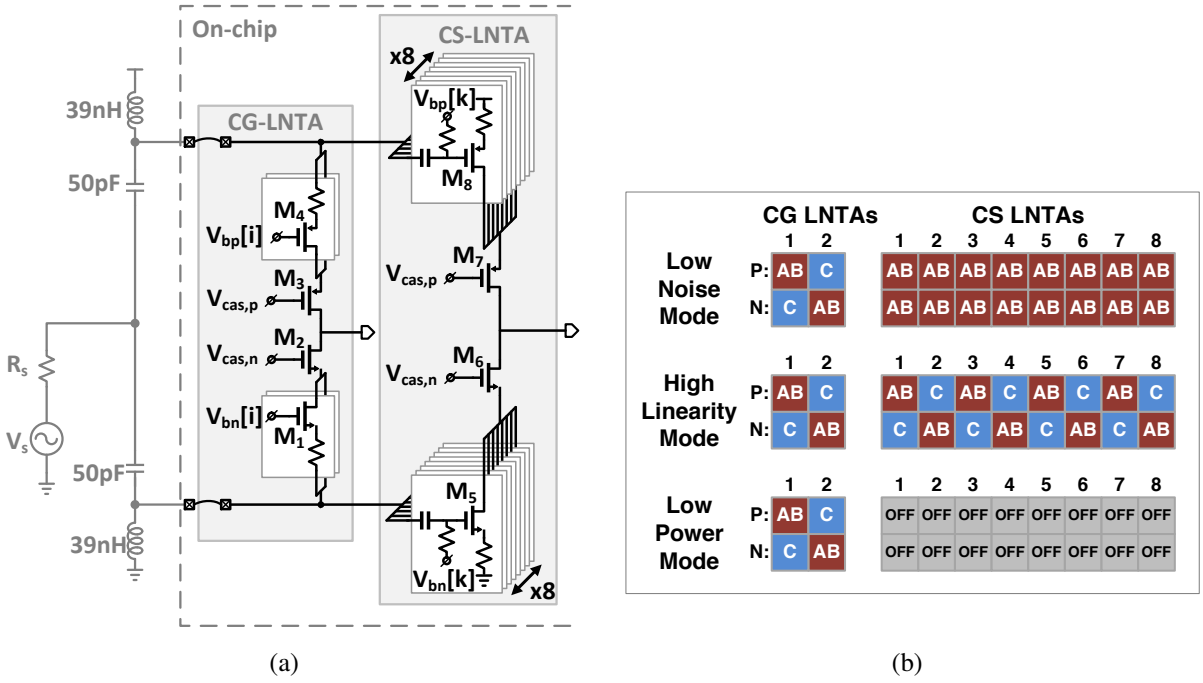


Figure 5.9: (a) Schematics of the CS and CG field-programmable noise canceling LNTAs (bias not shown); (b) three example operation mode of the noise canceling LNTAs.

Both the CS and CG LNTAs are designed with a current-reuse topology (Fig. 6.9), where both the NMOS and PMOS G_m cells contribute to the transconductance of the LNTA. The complementary topology offers lower noise than a single-transistor transconductor with a current-source load, where the load noise can contribute excess thermal noise and degrade the NF. This is particularly important for the CG LNTA since it does not have a high current gain. The CG LNTA uses two off-chip choke inductors to provide the DC bias currents with low noise penalty.

The flexible LNTA architecture has a large number of possible biasing combinations which makes a dynamic trade-off between LNTA noise and linearity performance and power consumption possible in the field. To maintain balance in the DC bias current of the NMOS and PMOS G_m cells, the number of class-AB NMOS cells needs to match the number of class-AB PMOS cells. Additionally, the class-AB cells needs to be matched with an equal number of class-C cells for the class-AB-C operation. In this section, we focus on three typical modes of operation shown in Fig. 5.9(b). The CG G_m cells are always kept in the class-AB-C mode, while the configuration of the CS cells is changed.

Low Noise Mode: When there are no extremely large blockers present and the highest sensitivity is desired for the receiver, all 8 cells of the CS LNTA are programmed with class-AB bias to maximize the CS branch G_m at the expenses of increased power dissipation.

High Linearity Mode: When large out-of-band blockers appear at the input, the CS LNTA is programmed into a high-linearity mode with half the cells biased in Class-AB and the other half in Class-C to handle the large blocker without compression. The NF degrades slightly due to lower G_m and conversion gain comparing to the low noise mode.

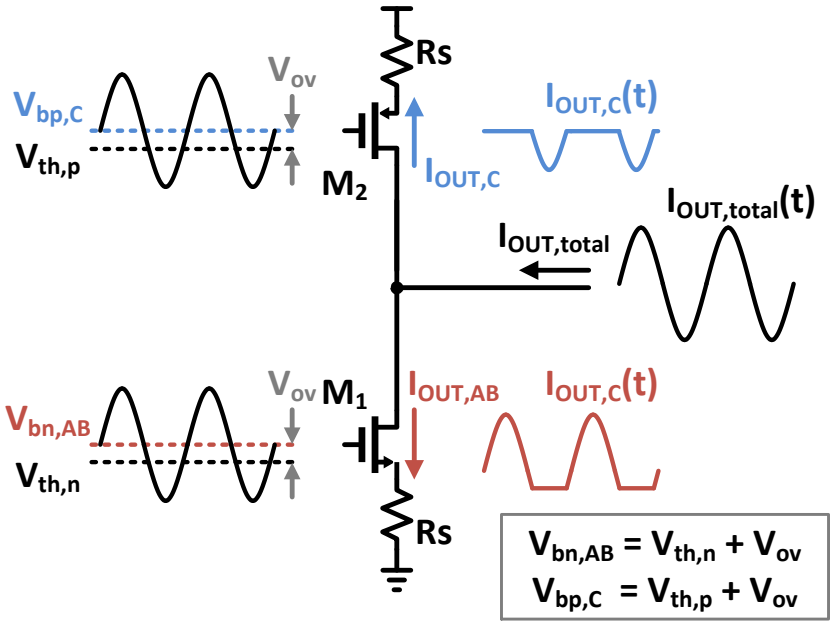


Figure 5.10: The bias voltage alignment criteria of the class-AB-C G_m cells.

Low Power Mode: In a benign RF environment with moderate blockers and a strong desired signal, the CS path can be shut down completely to save power at the cost of an increased NF; in the current implementation the CG path remains configured in the hybrid class-AB-C mode and the receiver linearity remains excellent.

5.4.3 Robust Biasing Scheme

The discussions in Section 5.3.2 indicate that the process, supply voltage, and temperature variations can all impact the transfer curve alignment robustness and adversely affect the linearity of the class-AB-C transconductor. Thus, it is critical to have properly designed G_m cells and biasing circuits that can accommodate the PVT variations and robustly maintain the alignment accuracy.

Resistive degenerated G_m cells are used instead of stand-alone MOSFET devices to reduce

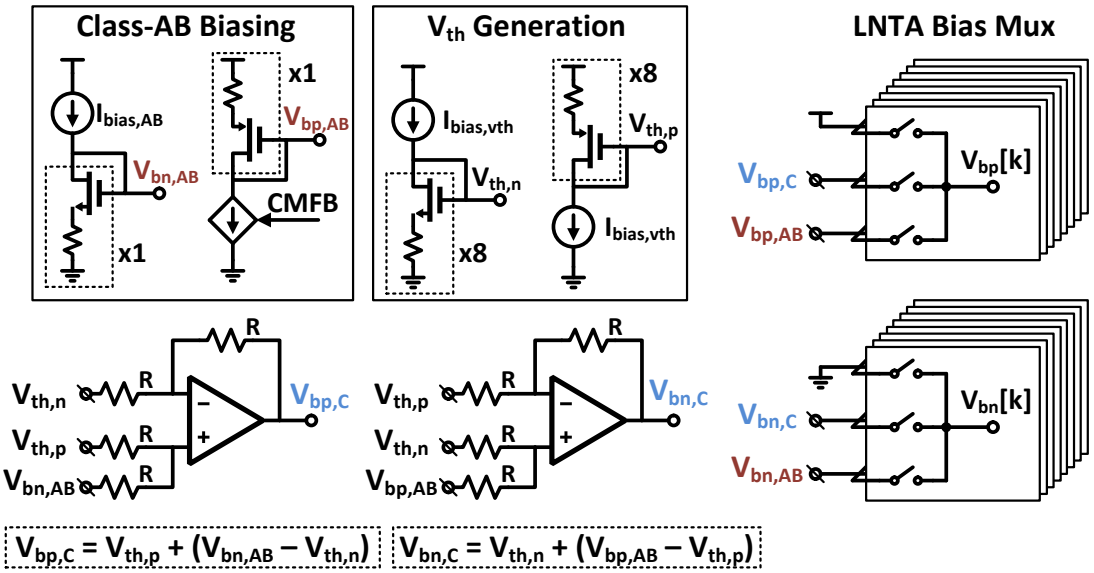


Figure 5.11: The LNTA bias generation and configuration circuits that are robust against PVT variations.

the slope mismatch. The large signal slopes of the short channel devices are often dominated by velocity saturation, which is a strong function of the temperature and process variations. The NMOS and PMOS devices can have relatively independent process corners and create P-N slope mismatch between the NMOS and PMOS G_m cells in the class-AB-C mode. The large signal slope of the resistively degenerated G_m cells are largely determined by the resistor value (see Equation 5.2). By using matched resistors of a same value for the NMOS and PMOS degeneration, the P-N slope mismatch becomes less sensitive to process variations. And as the resistors have closely matched temperatures and temperature coefficients, the slope mismatch also becomes less sensitive to temperature variations.

Fig. 5.10 illustrate the alignment criteria for the bias voltages of a class-AB NMOS G_m and a class-C PMOS G_m. The bias voltage of the class-AB NMOS cell ($V_{bn,ab}$) needs to be higher than

the threshold voltage of the NMOS cell ($V_{th,n}$) by V_{ov}. To ensure that the PMOS starts pushing out current as soon as the NMOS is turned off, the absolute bias voltage of the PMOS cell needs to be V_{ov} higher than its absolute threshold voltage. This puts the PMOS into deep weak inversion and it operates in class-C mode. Fig. 5.11 shows the bias voltage generation circuits for the LNTAs. The class-AB bias voltages are generated by pushing a constant current into a unit G_m cell. A DC feedback loop guarantees that the output DC voltage of the LNTA stays at half V_{DD}. The threshold voltages of the NMOS and PMOS G_m cells are found by pushing a small current into large unit G_m cells. Two simple DC opamps calculate the overdrive voltages of the NMOS and PMOS class-AB cells and adjust the threshold voltages accordingly to create the class-C bias voltages. Since the bias voltages are generated with V_{th} as references, the V_{th} alignment tracks the PVT variations and the errors are significantly reduced. Fig. 5.12 shows the simulation results of the P_{1dB} and the IIP_3 of the CS and CG LNTAs operating in class-AB-C mode. It can be seen that the linearity remains excellent and consistent across PVT variations. The linearity of the CS LNTA reduces slightly with the lower power supply, which is due to the lower output headroom, not due to the alignment non-idealities.

5.4.4 Baseband Trans-Impedance Amplifiers

The baseband trans-impedance amplifiers (TIAs) are also important building blocks. To accommodate the programmability in the LNTA, the TIAs are also designed with capability to back off in power when lowest noise is not required. Fig. 5.13 shows the simplified schematic of the programmable operational transconductance amplifier (OTA) used in the TIAs. The amplifier is a

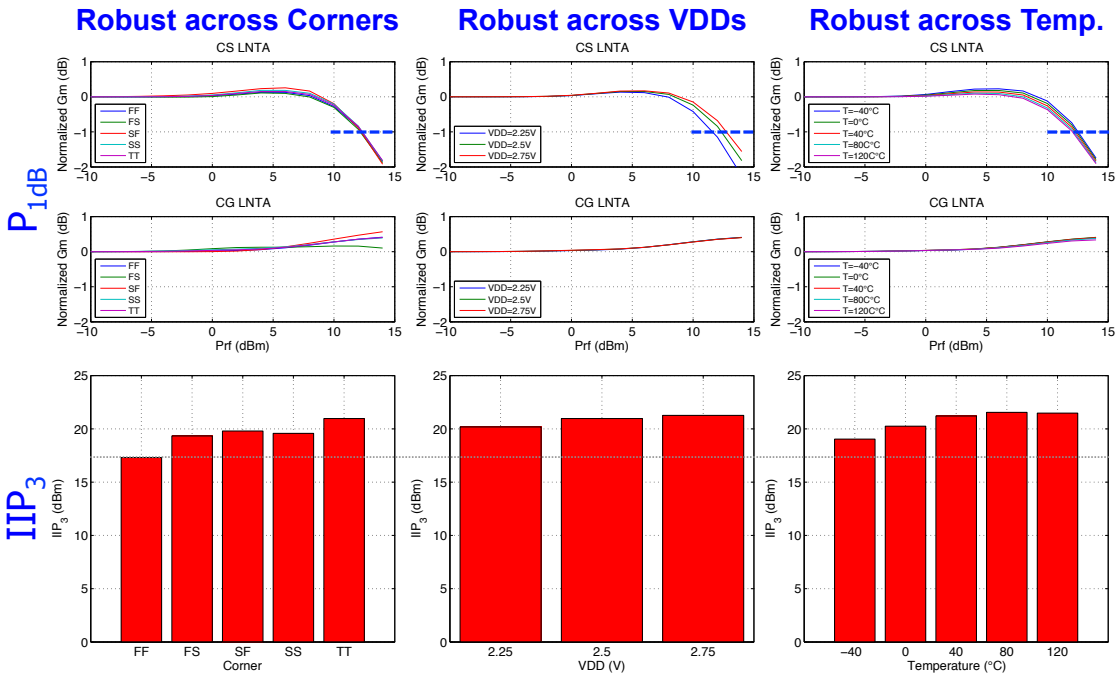


Figure 5.12: Linearity simulation results of the CS and CG LNTAs configured in the class-AB-C mode across different process corners, supply voltages, and operation temperatures.

traditional two-stage folded cascode fully differential OTA with Miller compensation. As the noise of the TIA is dominated by the input stage, it is designed with three slices that can be switched in and out. Programming the g_m of the input stage changes the phase margin, and a pair of programmable compensation capacitors (C_1 and C_2) are needed to maintain stability. The OTA is designed to operated with a 2.5V V_{DD} and a 1.25V common voltage. 2.5V thick-oxide I/O transistors are used for reliability considerations. Degeneration resistors (R_1 and R_2) are added to the output stage to shift the bias voltages of M_{15} and M_{16} and increase the headroom of M_9 and M_{10}. The degeneration resistors further linearize the output stage.

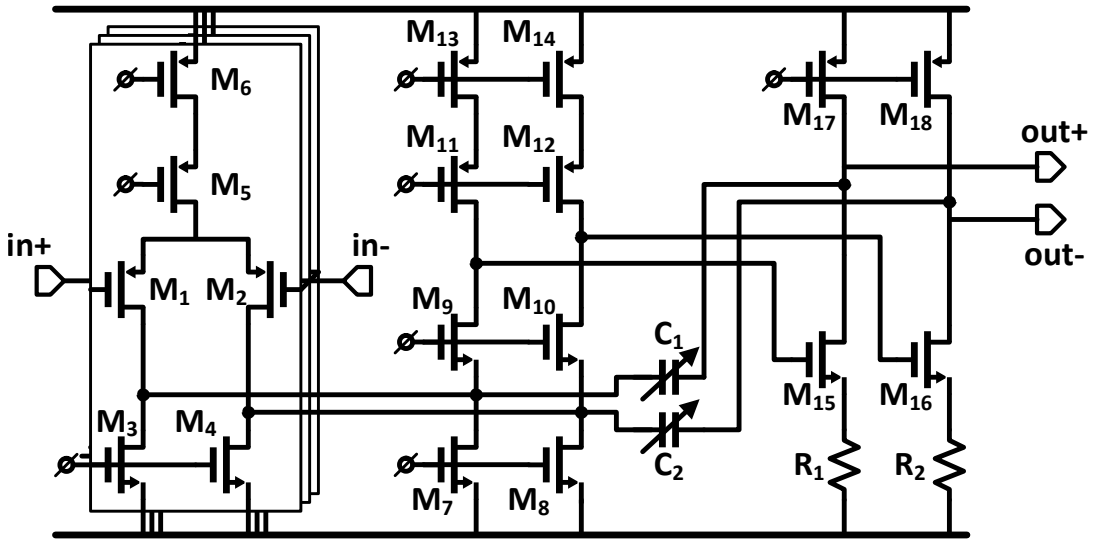


Figure 5.13: Simplified schematic of the programmable base-band OTA.

5.5 Experimental Results

The 40nm CMOS LP receiver chip has an active area of 1.6mm^2 (Fig. 6.11(a)). Fig. 5.15 shows the measured NF, out-of-band IIP$_3$ and B$_{1dB}$ for a 900MHz LO frequency across the three operating modes. The low noise mode has a 2.2dB NF, +15dBm OB-IIP$_3$ and +5dBm B$_{1dB}$ while consuming 49mA. The high linearity mode has a slightly degraded NF of 3dB, but the OB-IIP$_3$ improves to +21dBm, B$_{1dB}$ improves to +8.5dBm and current reduces to 42mA. The low power mode has a higher NF of 5.5dB and a moderate OB-IIP$_3$ of +17dBm; the B$_{1dB}$ of +11dBm is the highest due to the higher blocker tolerance of the CG LNTA. Assuming the CS downconversion path is powered

down[2], current consumption reduces to 20mA. The LO path power dissipation depends on LO frequency and is the same for low noise and high linearity modes, but is half for low power mode.

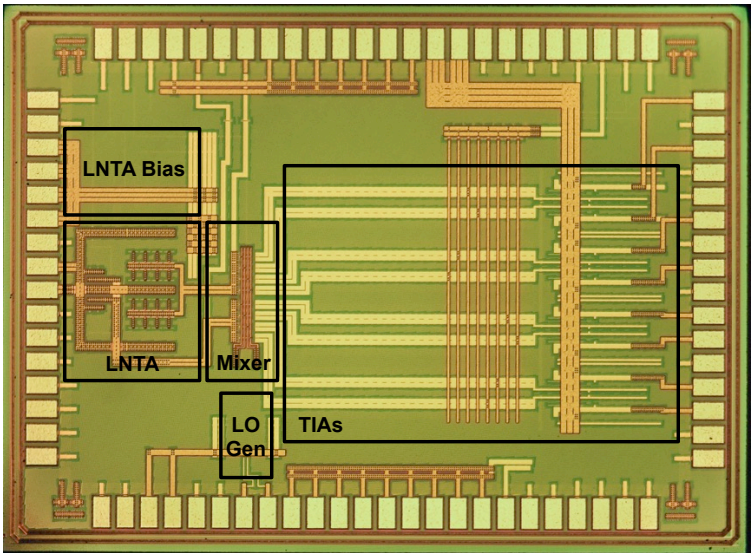


Figure 5.14: Die photo of the 40nm LP CMOS receiver prototype.

OB-IIP_3 measurements have been performed across the 3 modes and exhibit clean 3dB/dB slopes indicating that the linearity improvement is largely independent of signal power and that the IIP_3 can be reliably obtained by extrapolation. Fig. 6.16(b) and Fig. 5.17 show the linearity measurements for the high linearity mode and the NF and conversion gain measurements for the low noise mode across LO frequencies. The baseband complex combiner is reconfigured at each LO frequency for noise cancellation [10] whereas the LNTA biasing does not require calibration.

A key advantage of using a CG impedance matching path instead of a mixer-first path is the significantly reduced LO leakage. The measured LO leakage of our prototype is as low as -84dBm.

Table 5.1 summarizes the measured performance, which matches well with the simulated per-

[2]Our prototype chip does not include the TIA and LO power down circuits, but they can be easily added; current consumption of the low noise mode has been estimated based on the measured TIA and LO path current consumption.

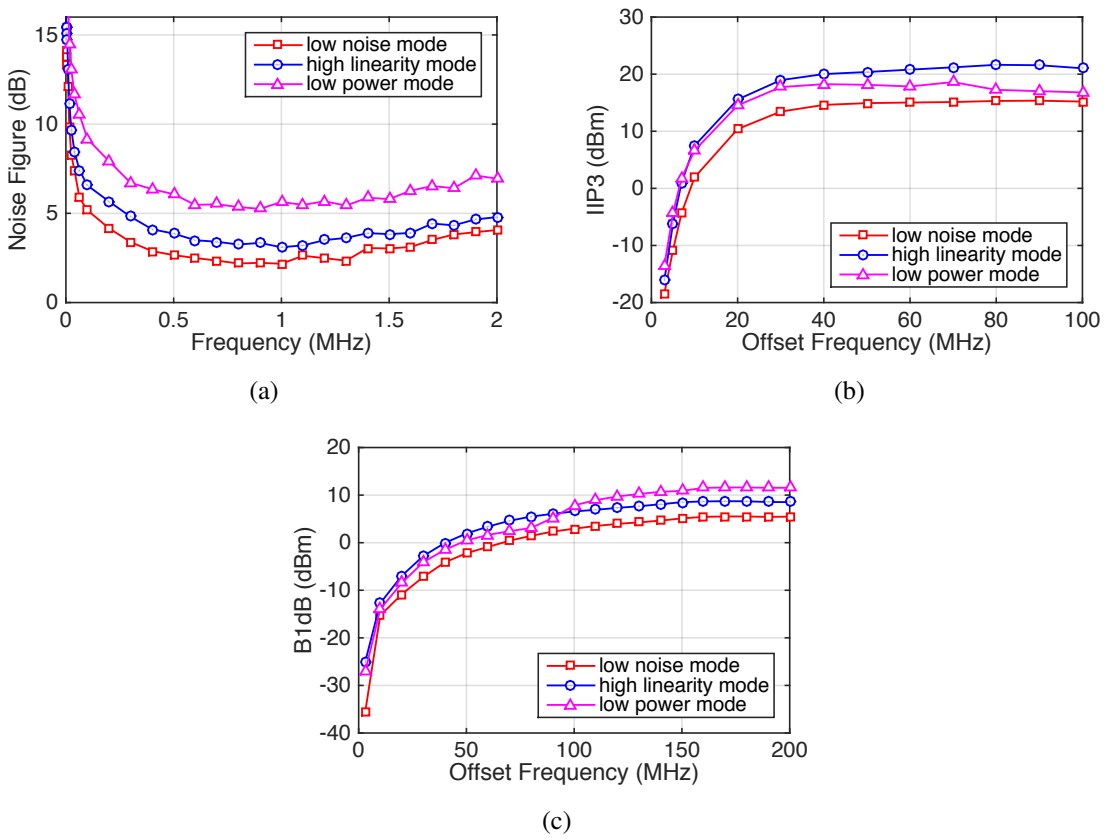


Figure 5.15: The receiver performance measured with a 900MHz LO for different operation modes: (a) noise figure vs. IF frequency (b) OB-IIP$_3$ vs. two-tone offset frequency (c) B$_{1dB}$ vs. blocker offset frequency.

formance in the TT corner, and provides a comparison with the state of the art in wideband receivers and LNTAs. The presented design has comparable linearity to [42] but better NF. The designs in [10, 63, 64] have slightly better NF, but this work has much higher blocker tolerance and IIP$_3$. The LNTA in [65] has a very high measured blocker tolerance, but the LNTA presented here demonstrates similar linearity with much lower NF. This prototype is designed in a CMOS LP technology and a high V_{DD} is used to provide more headroom over the large V_{th}.

Note that the other designs are fixed whereas the field-programmability of the presented design

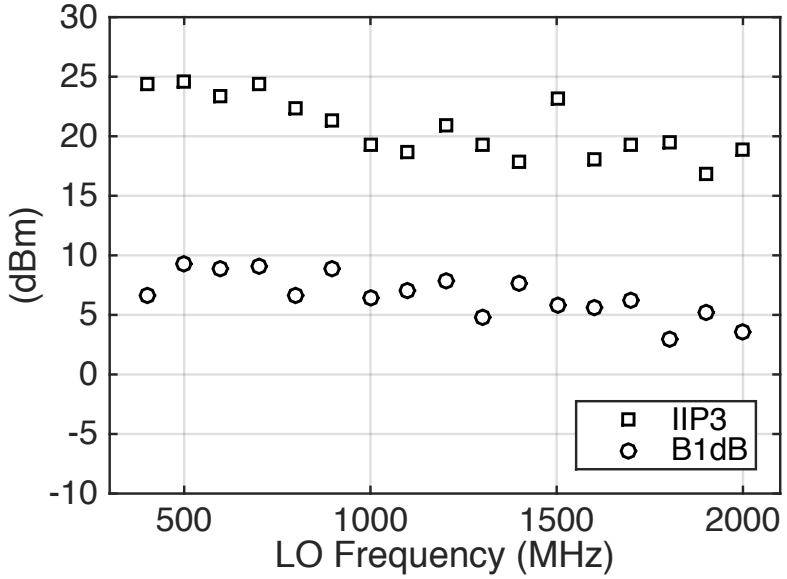


Figure 5.16: OB-IIP$_3$ and B$_{1dB}$ at different LO frequencies, OB-IIP$_3$ measured at 80MHz offset and spacing and B$_{1dB}$ measured for a 200MHz offset.

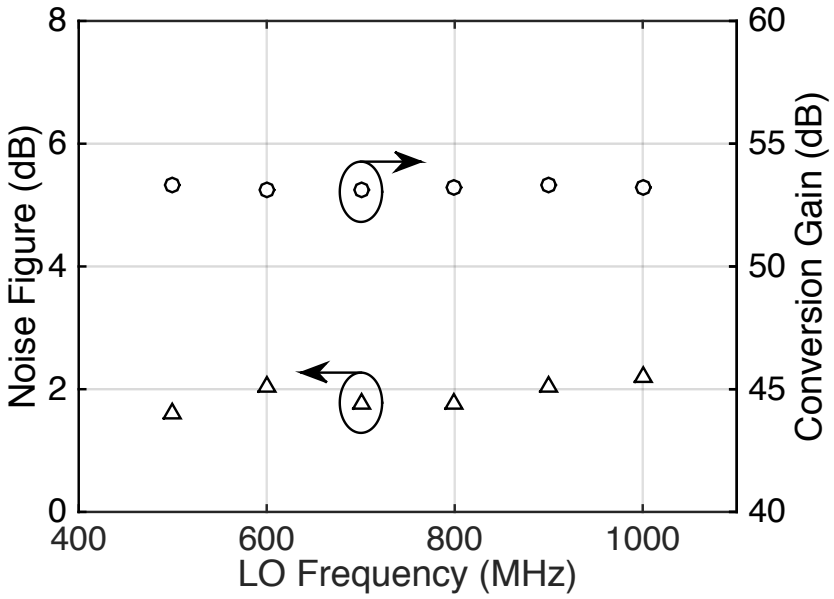


Figure 5.17: DSB NF and conversion gain for LOs from 0.5 to 1GHz.

Table 5.1: Measurement Summary and Comparison to the State of the Art

Design Type	Field-Programmable RX			Wideband RX				LNTA
Reference	This Work			[41]	[9]	[63]	[64]	[65]
	Low Noise	High Linearity	Low Power					
CMOS Technology	40nm			65nm	40nm	28nm	40nm	65nm
Frequency (GHz)	0.4-2.0			0.05-2.4	0.3-2.9	0.4-6	0.1-2.8	1.5-2.0
Max Gain (dB)	53	47	47	80	58	70	50	100mS
NF (dB)	2.2	3	5.5	5.5	1.9-2.1	1.8	1.8	6.5
OB IIP3 (dBm)	+15	+21	+17	+27	+12	+5	+3	+20
B1dB-CP (dBm)	+5	+8.5	+11	+5**	0	0	N/R	+8
LO Leakage (dBm)	-84.6	-85.6	-84.2	N/R	N/R	N/R	-82	N/R
Analog Current (mA)	39.9	32.8	15.0	12	24	20.4	24	7.5
LO Current (mA)	4.4-20	4.4-20	2.2-10	6-33	3-36	1.6-23.6	0.5-12.2	N/R
Power Supply (V)	2.5(Analog)/1.1(LO)			1.2(LO) / 2.5(BB)	1.3	0.9	1.1	1.5

N/R = Not Reported **Estimated

further allows to adapt to the RF signal environment, and switch to a low power mode when extreme noise or linearity performance is not needed.

5.6 Conclusions

The proposed field-programmable wide-band noise-canceling receiver achieves a minimum NF of 2.2dB, a maximum B_{1dB} of +11dBm, max OB-IIP_3 of +21dBm while keeping LO leakage below -84dBm. The high linearity stems from the use of the hybrid class-AB-C CG and CS LNTAs. The ability to dynamically trade noise and linearity performance off with power consumption in the field makes it a promising candidate for multi-standard software-defined radios.

Chapter 6

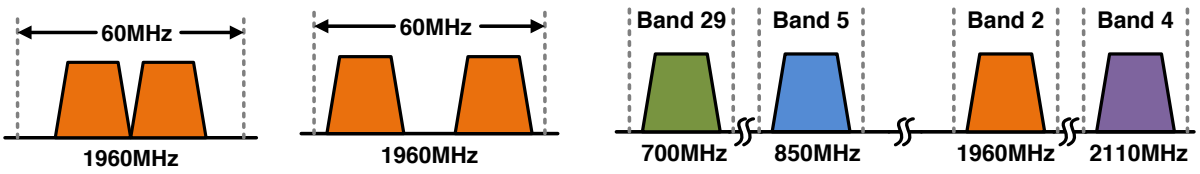
Achieving Ultra-Low Noise Figure and Massive Frequency-Agile Concurrency with Field-Programmable Frequency-Translational Quadrature-Hybrid Receiver Array

6.1 Introduction

Given the exponentially growing demands on data throughput, next generation wireless communication systems are expected to support 1000 times more traffic than today [66]. This will require

opening up bandwidth for the radio access network. However, due to diverse regional policies, it is challenging to find unified and contiguous wireless spectrum for global network deployments. In LTE systems, for example, the spectrum is fragmented across now nearly 50 frequency bands covering licensed and unlicensed spectrum [3].

The carrier aggregation (CA) technology utilizes the fragmented spectrum effectively by concurrently communicating on multiple carriers from either the same band or different bands, called intra-band and inter-band CA respectively (Fig. 6.1). Intra-band carriers are usually within several tens of MHz in a single frequency band. Intra-band CA receiver architectures have been demonstrated using two-step down-conversion [67], baseband complex filtering [60], or block down-conversion assisted with digital image-rejection calibration [68, 69]. Inter-band carriers, however, are usually hundreds of MHz apart making a single wideband receiver with sufficient dynamic range impractical. Conventional solutions split carriers from different bands into independent RF receivers with dedicated low-noise amplifiers (LNAs) and down-conversion signal paths [67], [60]. The RF signal splitting for these inter-band CA can be achieved with separate antennas or off-chip low-loss diplexer or duplexer filter banks. A multi-antenna approach needs as many antennas as the number of carriers, which is incompatible with the form factor of modern handheld devices. The diplexer or duplexer approach needs high-quality filters co-optimized for each band combination. Given the demands for more than four inter-band carriers and the exponentially growing band combinations (> 200) [3], neither of these signal splitting approaches scales well in terms of system complexity for the aggregation beyond more than 2 carriers. The alternative is to split the RF signal into separate down-conversion paths after a wideband LNA. However, this imposes too



(a) (b) (c)

Figure 6.1: Operation scenario examples for LTE carrier aggregation: (a) intra-band contiguous CA (Band 2), (b) intra-band non-contiguous CA (Band 2), (c) inter-band CA (4-band case) [3].

large a penalty on the receiver linearity since all interferers are also amplified without filtering [10]. State-of-the-art high linearity software-defined radio (SDR) receivers are realized with LNTAs and passive down-conversion mixers to avoid RF voltage gain [10, 70, 71]. Thus, a frequency-agile, scalable, RF-signal splitting technique using independent LNTAs is highly desired for inter-band CA applications.

In addition, receivers with low noise figure (NF) are always desirable since they offer better signal-to-noise ratios (SNRs), which improves receiver sensitivity for better network coverage and can support higher order modulation schemes for larger data throughput.

We introduce the frequency-translational quadrature-hybrid (FTQH) receiver architecture [72] that combines microwave techniques with modern CMOS RFIC and digital-assisted calibration circuits to achieve superior performance in terms of noise figure and massive reception concurrency. Section 6.2 introduces the operation principle of FTQH receivers. Section 6.3 discusses opportunities of adopting FTQH receivers in ultra-low-noise applications. Section 6.4 shows how FTQH technology enables frequency-agile, scalable carrier aggregation. The prototype circuit realization and the measurement results are presented in Section 6.5 and 6.6 respectively. And finally,

the FTQH receiver architecture is compared with the state of the art in Section 6.7 followed by conclusions in Section 6.8.

6.2 FTQH Receiver Architecture

6.2.1 Tradeoff Between Input Impedance Matching and NF for LNAs and Receivers

In conventional RF LNA designs, the optimum noise matching and the input power matching usually cannot be achieved simultaneously and there is a tradeoff between the noise figure (NF) and input impedance matching [15]. LNA and receiver design techniques such as active gate termination [73], common-gate G_m boosting [9, 74], resistive feedback [8, 35, 53, 60], and thermal noise cancellation [10, 13, 75] all create a matched input impedance while trying to minimize its impact on the NF. However, these techniques cannot be easily applied to RF signal splitting without significant NF penalty from reduced signal gain or less effective noise cancellation.

6.2.2 Traditional Balanced LNAs

In the balanced[1] amplifier architecture, there is no linkage between the RF input impedance matching constraint and NF optimization of the LNA [15, 76]. It is widely used in high-performance ultra-low-noise amplifiers and power amplifiers and uses quadrature hybrid couplers (QH) to achieve input matching. The QH [15] is a symmetric 4-port microwave device that splits the

[1] Note that the "balanced" is used here with its meaning from the microwave field and is not used with the meaning of "differential" as is more common in IC publications.

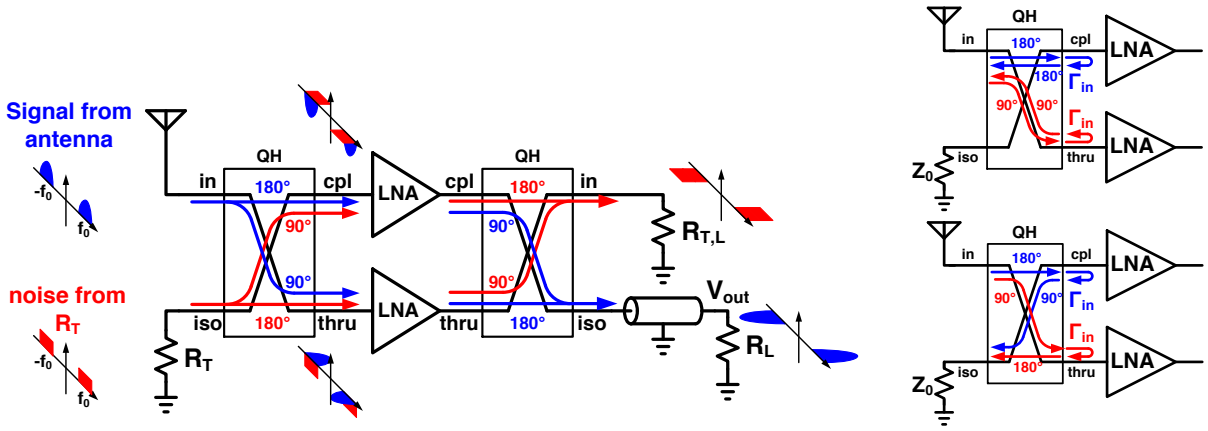
RF input signal equally in power to the through (*thru*) and coupled (*cpl*) ports with a 90° phase difference, and isolates the input (*in*) port from the isolated (*iso*) port. A wideband QH is usually implemented with coupled transmission lines and a multi-section design can cover several octaves of operation frequency range [15].

In a balanced LNA (Fig. 6.2(a)), two identical LNAs are connected to a QH at their inputs and a QH at their outputs. The input QH provides RF input impedance matching with poorly matched but identical loads (i.e. identical LNA input impedances). The waves reflected at the load cancel each other out at the input port and input matching is achieved, while the reflected power propagates to the *iso* port (Fig. 6.2(b)). If the QH's load impedance is purely reactive ($|\Gamma_L| = 1$) and the QH has low loss, then almost all of the incident power is redirected to the *iso* port[2]. The LNAs can still amplify the voltage signals without taking power from the incident signal. This is an important feature that we will revisit in Section 6.4.2 to enable RF daisy chaining for scalable CA.

6.2.3 Operation Principle of an FTQH Receiver

Balanced LNAs are designed as stand-alone amplifiers with wideband voltage gain, which incurs a linearity penalty on the receiver chain following the LNA. Using highly integrated CMOS RFIC designs, we can use two sets of LNTAs and passive mixers to down-convert the *thru* and *cpl* signals to the complex baseband and combine them in quadrature as shown in Fig. 6.3. Instead of performing the 90° phase shift at RF with an external output QH, it is implemented easily at

[2]The principle is much like that of a reflection phase shifter [15].



(a) (b)

Figure 6.2: Balanced LNA and its signal flow: (a) the desired signal from the antenna is amplified and the noise from R_T is cancelled; (b) the reflected signals from the LNTAs cancel at the *in* port and are redirected to the *iso* port when $|\Gamma_L| \approx 1$.

the complex baseband. Similar to the balanced LNA, the phase shifts are configured such that signals from the input port are amplified and combined in-phase in the baseband, while noise from the termination resistor R_T is canceled. With its quadrature operation across RF and baseband, we name this receiver architecture a frequency-translational quadrature hybrid (FTQH) receiver. Thanks to the input matching mechanism of the input QH, we can now use any type of LNTA without any constraints on its input impedance.

6.2.4 Calibration of the Impairments in a FTQH Receiver

The main sources of the RF impairments (Fig. 6.4) are the QH gain and phase imbalance, the imbalance between *cpl* and *thru* LNTA input reflections, the non-zero source or antenna reflection coefficient (Γ_s), the non-zero reflection coefficient (Γ_T) of the termination resistor R_T, and the gain and phase mismatch between the two down-conversion paths on the RFIC. These impairments

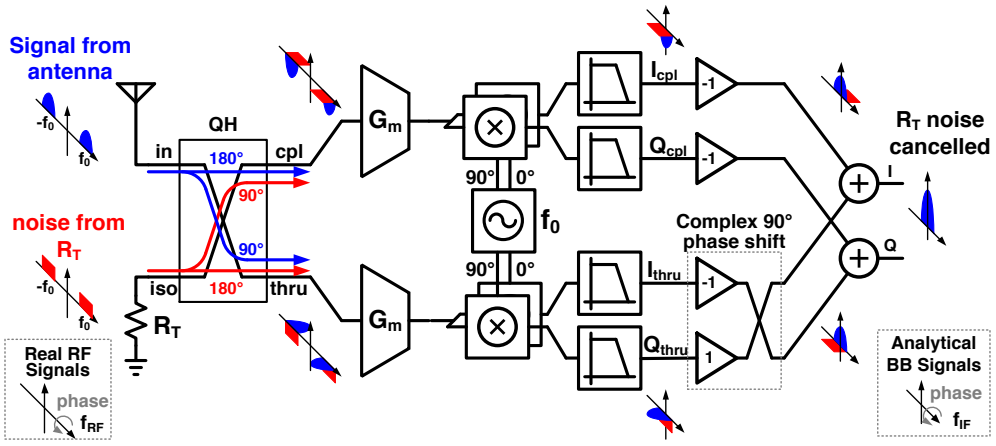


Figure 6.3: Architecture of the frequency-translational quadrature-hybrid receiver and its termination-resistor noise-cancelling mechanism.

cause non-perfect signal cancellation and result in finite input S_{11} and NF degradation due to the residual noise from R_T.

Finite RF Input Return Loss

Assuming $R_T = Z_0$ and a lossless QH with perfect isolation ($S_{41} = 0$), the finite S_{11} is mainly caused by imbalances of the QH, imbalances in the LNTA input reflection coefficients $\Gamma_{L,cpl}$ and $\Gamma_{L,thru}$, and the non-zero termination reflection coefficient Γ_T. The *cpl* and *thru* QH S-parameters have ideal values of $S_{21,nom} = -\frac{1}{\sqrt{2}}$ and $S_{31,nom} = \frac{j}{\sqrt{2}}$. Assuming a gain and phase imbalance while maintaining the lossless condition $|S_{21}|^2 + |S_{31}|^2 = 1$, we have:

$$S_{21} = -\frac{1}{\sqrt{2}}\sqrt{1+\alpha} \times e^{j(\frac{1}{2}\Delta\phi)}, S_{31} = \frac{j}{\sqrt{2}}\sqrt{1-\alpha} \times e^{j(-\frac{1}{2}\Delta\phi)}, \tag{6.1}$$

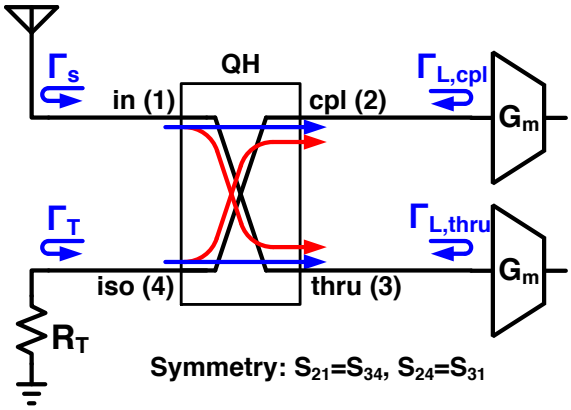


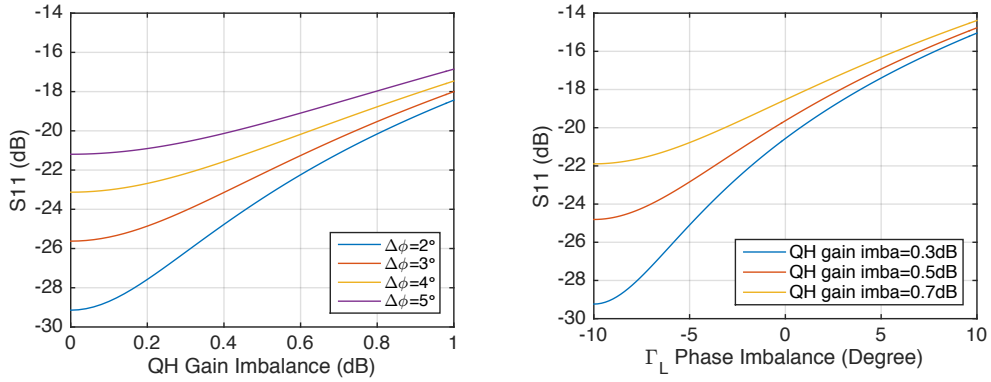
Figure 6.4: Possible RF impairments of the FTQH antenna interface, where the imbalanced QH S-parameters, the imbalanced LNTA input reflection coefficients, and the non-zero reflection coefficients of the antenna and the R_T all introduce cancellation errors which can possibly degrade the RF performance.

where $\sqrt{1+\alpha}/\sqrt{1-\alpha}$ is the gain imbalance ratio of the QH, and $\Delta\phi$ is its phase imbalance in radians. When highly reflective LNTAs are used, the main imbalances in $\Gamma_{L,cpl}$ and $\Gamma_{L,thru}$ are the phase error $\Delta\theta$ caused by imbalances in parasitic capacitors and inductors. The imbalanced LNTA input reflections are modeled as small phase shifts on the ideal Γ_L:

$$\Gamma_{L,thru} = \Gamma_L e^{j\frac{1}{2}\Delta\theta}, \Gamma_{L,cpl} = \Gamma_L e^{-j\frac{1}{2}\Delta\theta}. \tag{6.2}$$

Due to reciprocity, $S_{12} = S_{21}$ and $S_{13} = S_{31}$. The input return loss of the FTQH receiver now becomes

$$\begin{aligned} S_{11,Rx} &= S_{21}\Gamma_{L,cpl}S_{12} + S_{31}\Gamma_{L,thru}S_{13} + (S_{21}\Gamma_{L,cpl}S_{42} + S_{31}\Gamma_{L,thru}S_{43})^2 \\ &\approx (\alpha + j(\Delta\phi + \Delta\theta))\Gamma_L + \Gamma_L^2\Gamma_T. \end{aligned} \tag{6.3}$$



(a) (b)

Figure 6.5: Achievable S_{11} under RF impairments: (a) S_{11} with QH imbalance errors only; (b) S_{11} with Γ_L phase imbalance with the phase imbalance of the QH kept at 5°.

The achievable S_{11} with these non-idealities is shown in Fig. 6.5 with the QH gain imbalance expressed in dB as $20log(\sqrt{1+\alpha}/\sqrt{1-\alpha})$ and the phase imbalance $\Delta\phi$ expressed in degrees. According to [77], the QH gain and phase imbalance can be controlled within $\pm$0.5dB and $\pm5^\circ$ respectively across its operation frequency band. The input return loss S_{11} can then be kept well under -15dB without calibration, which is acceptable for most wideband wireless receivers.

Termination Resistor Noise Residue

As shown in Fig. 6.3, the noise from R_T should be completely canceled with a 90° baseband combiner. However, the noise cancellation with a fixed baseband combiner can be limited by the QH imbalance, and the residual noise directly degrades the FTQH receiver NF. The noise signals at the baseband output due to the signal source noise $\overline{V_{n,s}^2}$ and the termination noise $\overline{V_{n,R_T}^2}$ are:

$$\overline{V_{n,BB,s}^2} = \overline{V_{n,s}^2}(S_{21}A_{conv}e^{j\frac{\pi}{2}} + S_{31}A_{conv}e^{j\pi})^2,\ \overline{V_{n,BB,R_T}^2} = \overline{V_{n,R_T}^2}(S_{24}A_{conv}e^{j\frac{\pi}{2}} + S_{34}A_{conv}e^{j\pi})^2, \quad (6.4)$$

where A_{conv} is the conversion gain of each receiver path. Considering only QH imbalance and assuming $S_{21} = S_{34}$, $S_{31} = S_{24}$, the impact of the noise residue at baseband due to non-ideal cancellation can be quantified by its power ratio to the noise from the signal source:

$$\frac{\overline{V_{n,BB,R_T}^2}}{\overline{V_{n,BB,s}^2}} = \frac{\overline{V_{n,R_T}^2}}{\overline{V_{n,s}^2}} \left(\frac{\frac{\sqrt{1+\alpha}}{\sqrt{2}} e^{(\pi - \frac{1}{2}\Delta\phi)} + \frac{\sqrt{1-\alpha}}{\sqrt{2}} e^{(2\pi + \frac{1}{2}\Delta\phi)}}{\frac{\sqrt{1+\alpha}}{\sqrt{2}} e^{(\frac{3}{2}\pi + \frac{1}{2}\Delta\phi)} + \frac{\sqrt{1-\alpha}}{\sqrt{2}} e^{(\frac{3}{2}\pi - \frac{1}{2}\Delta\phi)}} \right)^2 \approx \frac{\alpha^2 + \Delta\phi^2}{4}. \tag{6.5}$$

Even with noiseless receiver circuits, the noise factor of the FTQH receiver will then be limited to

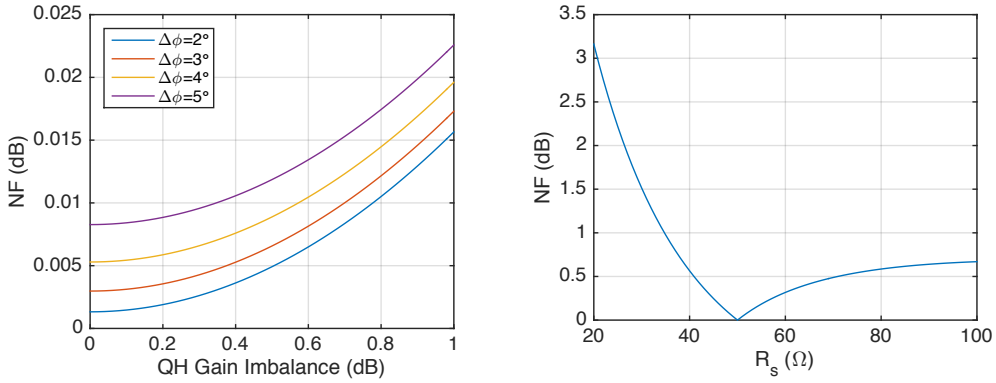
$$F \approx 1 + \frac{\alpha^2 + \Delta\phi^2}{4} \tag{6.6}$$

Fig. 6.6(a) shows the minimum achievable NF with noiseless receiver circuits under QH imbalance. The NF penalty is less than 0.03dB for typical QH impairments, which can be neglected for most systems.

The non-zero source or antenna reflection coefficient Γ_s has a much larger impact on the NF, especially when highly reflective LNTAs are used [78]. The noise from R_T is redirected to the input and reflected back by Γ_s. This portion of the noise overlays on the input signal and degrades the NF. To quantify the problem, we evaluate the minimum achievable NF with non-zero Γ_s. The source noise signal power depends on the magnitude and the phase of Γ_s, which complicates the analysis. Thus, we analyze a simplified scenario where the source is purely resistive. The noise factor is:

$$F = 1 + \frac{\frac{1}{4}\overline{V_{n,R_T}^2}(S_{24}\Gamma_L S_{12} + S_{34}\Gamma_L S_{13})\Gamma_s}{\frac{1}{4}\overline{V_{n,s}^2}} = 1 + \frac{R_T}{R_s}\left|\frac{R_s - Z_0}{R_s + Z_0}\right|. \tag{6.7}$$

Fig. 6.6(b) shows the NF penalty due to source mismatch. A purely real antenna impedance of $R_s = 26\Omega$ gives a moderate return loss of -10dB but introduces up to 2.06dB of NF penalty.



(a) (b)

Figure 6.6: Minimum achievable NF with RF impairments: (a) NF with QH imbalance errors only; (b) NF with non-50Ω R_s (i.e. non-zero Γ_s).

Termination Noise Cancellation Calibration

The R_T noise residue can be significantly reduced with digitally assisted calibration and replacing the baseband fixed 90° combiner with a programmable, complex Cartesian combiner implemented either in baseband analog circuits, or in the DSP after digitization (Fig. 6.7). A calibration RF test signal is injected at the termination resistor R_T and an adaptive algorithm controlling the combiner is used to minimize the resulting baseband test signal power at the combiner output. The test signal can be a small tone or a noise-like modulated signal; in our experiments, a -80dBm tone has been used. The effectiveness of the noise cancellation depends on the total cancellation across the receiver IF bandwidth (tens of MHz). For a receiver with an NF of 1dB with perfect noise cancellation, a moderate cancellation of -20dB, which can relatively easily be achieved, gives an NF penalty of only 0.03dB. When canceling the noise from R_T, there is a possibility of a slight

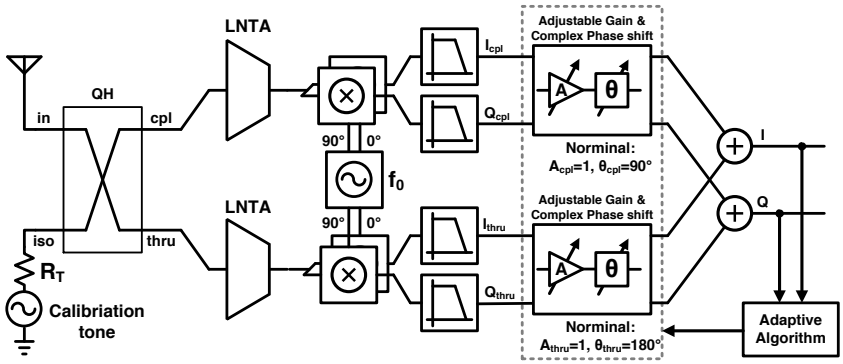


Figure 6.7: Calibration of the FTQH baseband Cartesian combiner for optimum noise cancelation.

noise figure penalty due to the reduced gain of the desired input signals, as the combiner might not combine them completely in-phase. This noise figure penalty is usually less than 0.1dB if the errors are small.

6.3 FTQH for the Realization of Wideband, Ultra-Low-Noise Receivers

The FTQH receiver allows using an arbitrary LNTA input impedance, which opens opportunities for ultra-low-noise front-end amplifiers with non-conventional topologies.

6.3.1 Prior Art in Ultra-Low-Noise Amplifiers

Traditionally, ultra-low-noise amplifiers with sub-1dB NF at room temperature are realized with III-V devices in either single [79] or balanced mode [80]. Although these LNAs have excellent NF and linearity, their power consumption is often too high for mobile terminals. They can currently

also not be integrated with the CMOS RFIC to lower cost. CMOS ultra-low-noise amplifiers are either narrow band [81], assume a non-50Ω system impedance [82, 83], or compromise the input impedance matching requirements [83].

6.3.2 Ultra-Low-Noise CMOS Common-Source Transconductance Amplifier

A common-source (CS) MOSFET can be used to achieve a sub-1dB NF if input impedance matching is not required [83]. Driving a CS transconductor with a sufficiently small input capacitance from a 50Ω R_s makes a wideband LNTA with a 6dB passive voltage gain [83] compared to an impedance-matched LNA. Assuming the input capacitance is dominated by the C_{gs} of the MOSFET and operating at a frequency f which is much lower than the transit frequency f_T of the MOSFET, so that gate-induced noise can be neglected [84], the noise factor can be approximated as:

$$F \approx 1 + \frac{\gamma}{g_m R_s} + \gamma \left(\frac{f}{f_T} \right)^2 g_m R_s, \tag{6.8}$$

where γ is the channel-noise constant of the MOSFET and g_m is the device transconductance. When we scale up the size of the CS transistor and keep the current density unchanged (fixed g_m/I_D and f_T), the g_m increases and the NF of the LNTA improves (Fig. 6.8). However, the rate of improvement quickly reduces and spending more power only reduces NF marginally. For very large device sizes, the higher parasitic capacitance causes a reduction in the input RF bandwidth

resulting in a noise factor increase. Thus, for a given device f_T, there is a direct tradeoff between the NF, power consumption, and the RF bandwidth of a CS LNTA.

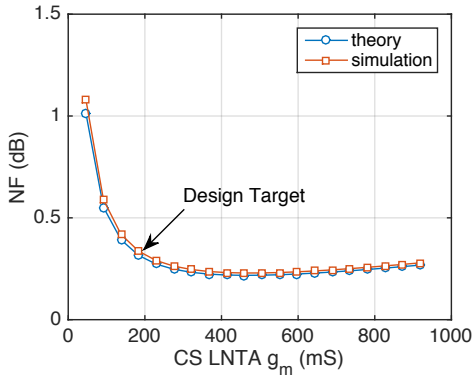


Figure 6.8: Theoretical calculation (Equation 6.8) and schematic simulations of the NF of a 65nm CMOS LNTA at 1GHz vs. g_m scaling, with a device f_T of 90GHz.

When driving an ideal current-sink load, the distortion of the LNTA is dominated by its input nonlinearity and depends on the device's (g_m/I_D) or overdrive ($V_{gs} - V_{th}$). The input linearity can also be improved with circuit techniques such as resistive degeneration and/or derivative superposition [2, 70]. However, improving the linearity will typically come at the cost of a reduced effective device f_T which directly impacts the NF-power-BW tradeoff.

Properly sized and biased inverters can be used as wideband transconductors for both analog and RF applications [10, 11] with good noise and linearity performance. Fig. 6.9 shows the block diagram and schematic of the inverter-based CS LNTA. The two-branch LNTA takes one single-ended voltage input and generates two separate current outputs, which drive two independent passive down-conversion mixers for concurrent reception. The two branches each have a maximum g_m of 100mS and are composed of four binary-weighted inverter G_m slices with a unit weight g_m of 6.6mS. The inverter PMOS and NMOS transistors are sized with a ratio of 2:1. Each G_m slice

can be powered on and off with source switching which offers better output voltage swing for out-of-band blocker tolerance than drain switching. Using this field programmability, the LNTA g_m can be reduced to save power when high sensitivity is not needed. The LNTAs have DC coupled inputs to avoid having to use a large capacitor array to couple to the multi-slice G_m core, as this would degrade the NF by approximately 0.1dB. The AC coupling capacitors can be placed off-chip if needed. The two LNTA branches have 200kΩ self-biasing feedback resistors which do not degrade the NF. The two-channel LNTA operates with a VDD of 1.1V and a total power consumption of 20mW, with a simulated NF[3] of 0.32dB at 900MHz in the two-channel aggregated high-sensitivity mode (Section 6.5).

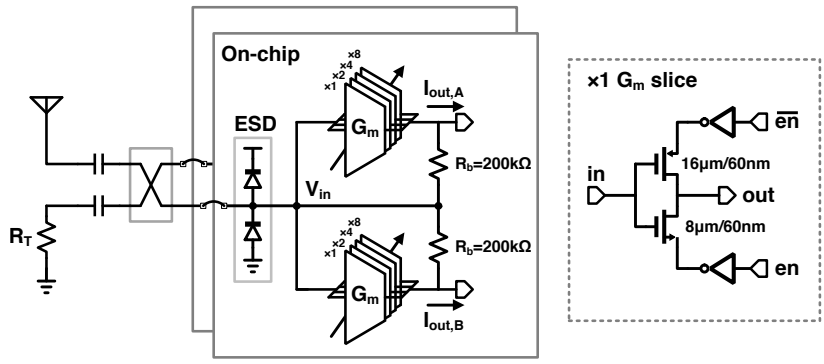


Figure 6.9: The schematic of a two-channel common-source LNTA that enables wideband voltage domain RF signal splitting.

Due to the high g_m values (100mS each branch) used in the LNTA, and relatively high load impedance from the mixer R_{on} (10Ω) and TIA out-of-band input impedance (30Ω at a 200MHz offset freq.) the LNTAs still have an out-of-band voltage gain larger than 1. With a 0.8V peak-to-peak LNTA output voltage swing, the input referred out-of-band 1dB compression point ($OB\text{-}P_{1dB}$)

[3]The NF was simulated on the stand-alone LNTA without the QH. It is then used as a baseline to estimate the NF of the LNTA in the balanced mode with the QH.

at which the gain of the blocker is compressed by 1dB is around -10dBm. The out-of-band 1dB blocking point ($OB\text{-}B_{1dB}$) is the blocker power level for which the gain of an in-band desired signal is compressed by 1dB. This is expected to be 3dB lower than $OB\text{-}P_{1dB}$ and is -13dBm. The linearity of the full FTQH receiver is 3dB better than that of a single receiver path thanks to the division of the input power by the QH over its two output branches. Thus, the estimated input referred $OB\text{-}B_{1dB}$ of the full receiver is around -10dBm, which matches with measurements shown in Section 6.6.

6.3.3 FTQH Receiver Noise Budget

The main contributors to the overall receiver NF are: the insertion loss of the QH, the thermal noise of the LNTA, the mixer noise folding from higher harmonics, and the thermal noise from baseband amplifiers and resistors. Our design target is to achieve a sub-1dB receiver NF for a 900MHz operating frequency including the noise penalty from the QH. In this design we use a low loss off-chip coupler that operates between 0.7-2.7GHz with a $< 0.3dB$ insertion loss below 2GHz and a $< 0.15dB$ insertion loss below 1GHz [77]. The QH insertion loss directly affects the receiver NF and does not scale with the receivers's power consumption. The LNTA has a simulated NF of 0.32dB at 900MHz, which can be improved by spending more power at the cost of reduced RF bandwidth. The harmonic folding of noise in the down-conversion mixer also increases the NF of the receiver. Assuming that the RF source and the LNTAs are wideband, noise folding increases the output noise by a fixed ratio. A 4-phase mixer will have 0.81dB of noise penalty and the 8-

phase harmonic rejection mixer (HRM) used in this work has a 0.17dB noise penalty [10]. This noise folding cannot be improved with power scaling.

These three noise contributors limit the minimum NF of the receiver to 0.64dB. Although the LNTA has substantial transconductance gain, the noise from the baseband trans-impedance amplifiers (BB TIA) still contributes to the overall noise figure by about 0.15dB in the maximum gain setting, where $R_1 = 0\Omega$, $R_2 = 4.8k\Omega$, $R = 100\Omega$ and $G_{m,TIA} = 25mS$ (Fig. 6.14). This gives an overall minimum NF of around 0.8dB, which is confirmed with full-signal-chain simulations where the QH is modeled with measured S-Parameters [77]. Considering the possible additional losses in the package or the PCB there is 0.2dB design margin to achieve sub-1dB NF at 900MHz.

6.4 FTQH for Scalable Inter-Band Carrier-Aggregation Receivers

An FTQH receiver array offers a versatile solution for inter-band carrier aggregation. The maximum number of concurrent channels can be scaled in two ways: we can attach M receivers in parallel to a single QH and we can further daisy chain N QHs to support up to $M \times N$ channels (Fig. 6.10).

6.4.1 Paralleling CS LNTAs with a Single QH

The CS LNTAs not only have ultra-low NF, but are also suitable for concurrent operation. Their high input impedance enables voltage domain RF signal splitting, and their reverse isolation of the LNTAs improves channel-to-channel isolation. For balanced operation, the same number of

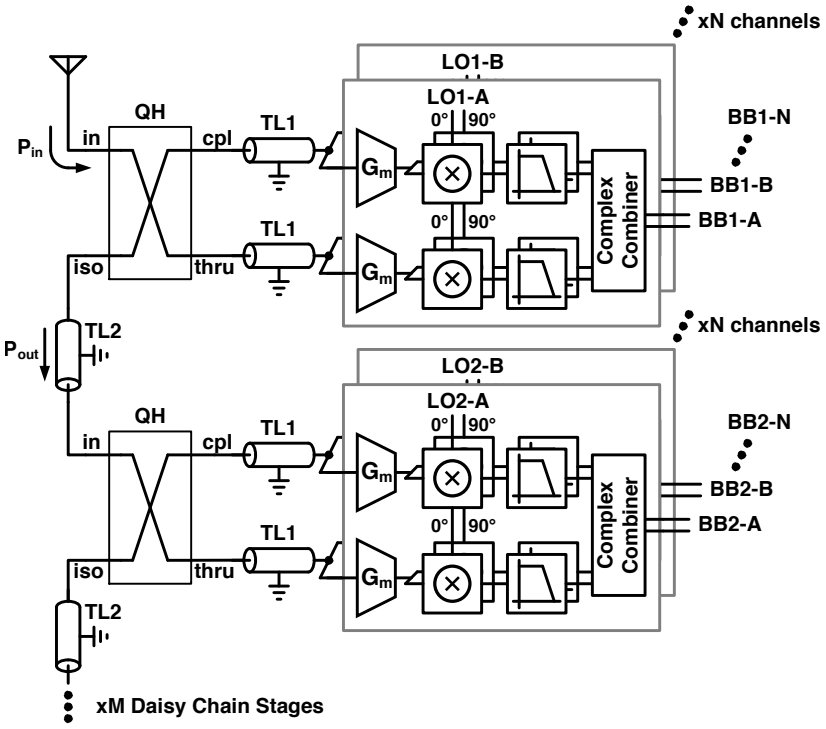


Figure 6.10: An FTQH carrier aggregation receiver array can be scaled by adding more parallel receivers per QH and by daisy chaining QHs with parallel receivers.

LNTA branches should be attached to both the *cpl* port and the *thru* port to meet the input matching condition.

As discussed in Section 6.3.2, there is a tradeoff between NF, power consumption, RF bandwidth, and linearity. When putting LNTAs in parallel, the total parasitic capacitance at the LNTA input is increased. Given a required RF bandwidth, the maximum acceptable amount of input capacitance is fixed, and the corresponding total maximum g_m of all the LNTA branches can be determined from the technology device f_T. Given this max. total g_m, there is a tradeoff between the number of supported concurrent channels and the NF of each channel. NF of each channel increases as we distribute the total g_m into more channels. The tradeoff can be improved by using a more advanced CMOS technology node with higher device f_T.

6.4.2 Daisy Chaining FTQH Receivers

As discussed in Section 6.2.2, the incident RF signal power is redirected to the *iso* port when highly reflective LNTAs are used. The redirected signal can now be fed into another FTQH receiver. Repeating this connection results in a cascaded receiver daisy chain. The daisy chaining works with any amount of lossless parasitic capacitance attached to the *thru* and *cpl* ports as they only affect the phase shift from the *in* port to the *iso* port, not the insertion loss.

The total insertion loss introduced by one stage of the FTQH daisy chain can be expressed as:

$$IL = 2 \times (IL_{hybrid} + IL_{TL1}) + RL_{LNTA} + IL_{TL2}, \tag{6.9}$$

where IL_{hybrid} is the insertion loss of the hybrid coupler, IL_{TL1} is the loss of the transmission line

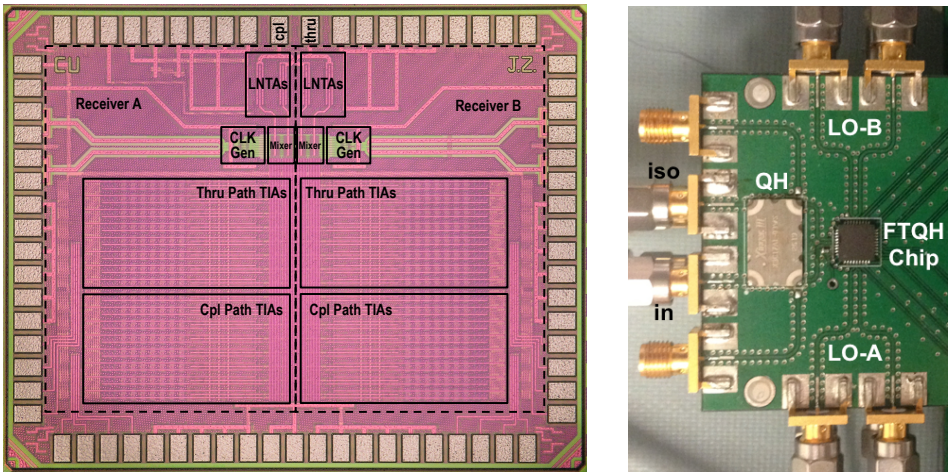
connecting the hybrid and the receiver chip, RL_{LNTA} is the return loss of the LNTA input, and IL_{TL2} is the insertion loss of the transmission line connecting one FTQH stage to the next (Fig. 6.10). For a typical implementation, the insertion loss at 1GHz is around 1dB. The NF of the receiver increases at higher frequencies, so assigning the high-frequency bands to the earlier FTQH stages helps equalize the sensitivity accross all concurrent channels; alternatively, if the low-frequency bands are allocated to the earlier stages, the best sensitivity for these bands can be achieved.

6.4.3 Supporting Intra-Band CA

The FTQH receivers split the carrier signals at the input of the LNTAs with arbitrary frequency combinations. Thus, the FTQH architecture is compatible with existing receiver techniques that use current driven passive mixers. Techniques demonstrated in [68] and [60] can possibly be adopted by the FTQH design to support intra-band CA. Our prototype chip supports up to 70MHz of RF bandwidth, where block down-conversion techniques [68] can be applied in the digital domain.

6.5 FTQH Receiver Prototype Circuit Realization

To validate the proposed FTQH receiver architecture, we designed a prototype chip in a standard 65nm CMOS GP technology with a size of 1.2mm$\times$1.5mm and an active area of 1.1mm^2 (Fig. 6.11(a)). Fig. 6.12 shows the block diagram of the prototype chip. Dual-branch CS LNTAs are connected to the *thru* and *cpl* inputs for two independent FTQH receiver channels (A and B) sharing the same off-chip wideband QH. The on-chip input interconnections of the LNTAs need



(a) (b)

Figure 6.11: The FTQH 65nm prototype receiver: (a) Die photo of the dual-channel FTQH prototype chip showing two symmetric receiver channels on the left and right; (b) RF section of the test PCB showing the wideband QH and the FTQH receiver chip; the transmission lines are kept short and symmetric.

careful layout to minimize the insertion loss. An M1-M2 metal ground shield is used to isolate the input from the lossy substrate. Each output of the LNTAs is connected to a down-conversion chain consisting of 8-phase passive harmonic down-converters followed by programmable BB TIAs and resistive harmonic combination networks.

As discussed in Section 6.3.3, harmonic-rejecting mixers (HRM) are used to reduce folding of the broadband noise from the antenna and the LNTA. The HRMs are realized with eight switching paths driven by 8-phase 12.5% duty-cycle non-overlapping LO signals (Fig. 6.13). The 8-phase LO signals are generated by a divide-by-4 divider realized with 4-stage differential CMOS latch [10]. The eight output signals are single-ended with a 50% duty cycle and with equally spaced phase differences. This assumes that the divider is driven by a 50% duty cycle clock signal at $4f_{lo}$. To reduce the power dissipation in the clock distribution, the LO signals are sent to the mixers with a 50% duty cycle, and the local logics of each mixer switch select the proper phases to generate

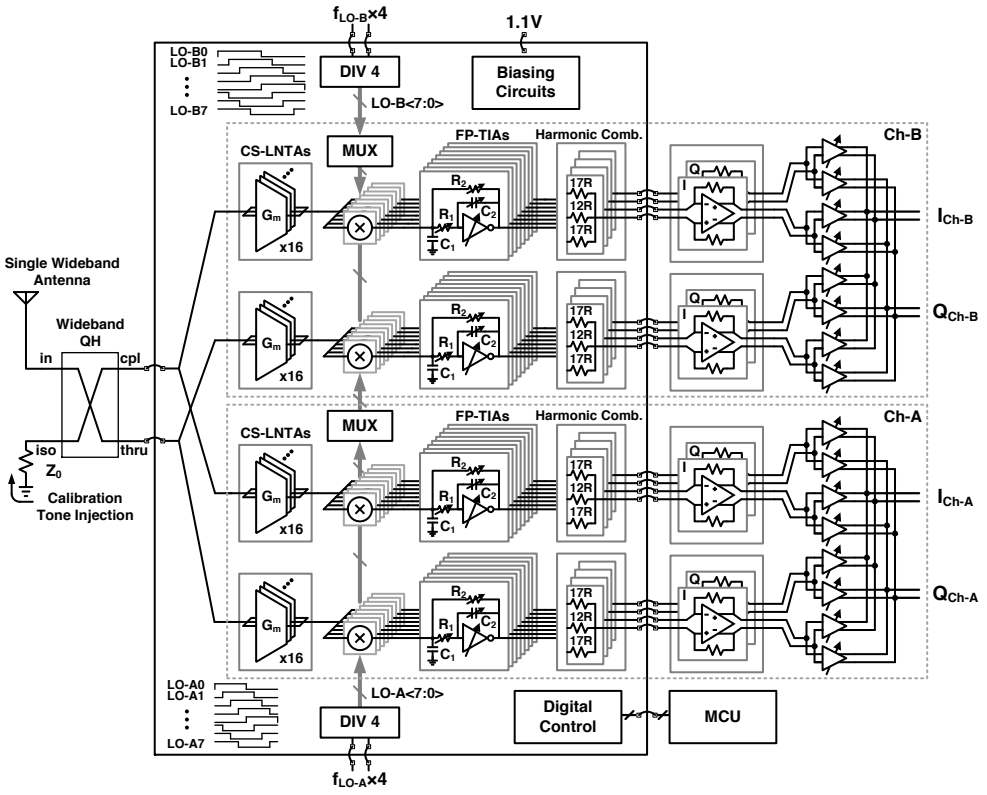


Figure 6.12: The system block diagram of the two-channel FTQH receiver prototype chip.

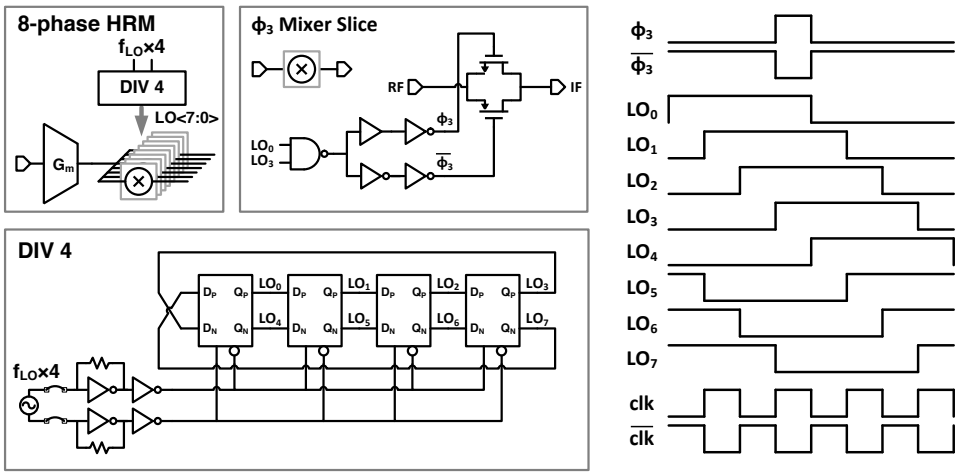


Figure 6.13: The schematic of the 8-phase passive mixer and the LO signal generator; each prototype chip has two sets of LO generators.

the 12.5% duty cycle non-overlapping signals. A digital balun [85] (shown in Fig. 6.13) is used to convert the single-ended LO signals to differential before driving the transmission gate switches. The balun has less than 10ps of systematic clock skew and does not have significant impact on the system performance. The inverter-based LNTAs can support an almost rail-to-rail output voltage swing. Thus, we use transmission-gate mixer switches for their wide input-voltage range. The on-resistance of the switches is designed to be less than 10Ω.

The down-converted signals are then amplified and filtered by eight programmable transimpedance amplifiers (TIA) and combined with weighted-resistor networks (Fig. 6.14). A resistor ratio of 17:12:17 is used to approximate the desired conductance ratio of $1:\sqrt{2}:1$ for harmonic rejection [8]. Unit resistor cells are used to realize the integer ratios for optimum resistor matching. Dummy resistors are attached where necessary to the TIA branches to maintain the same amount of resistive load for each TIA branch to mitigate systematic gain errors. The programmable TIAs are also realized with inverter-based transconductor slices. The channel length of the transistors

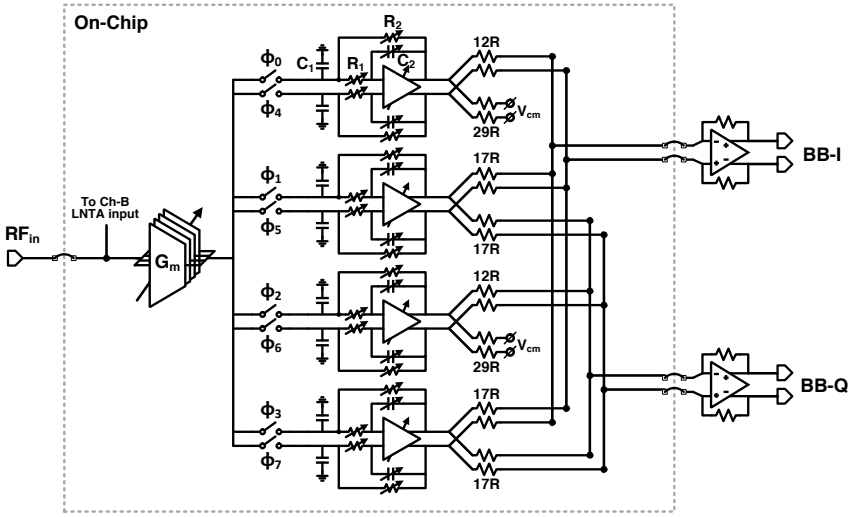


Figure 6.14: The schematic of a single down-conversion signal chain with CS LNTA driven 8-phase HRM; each prototype chip has four such signal chains.

is increased to 500nm to reduce their flicker-noise. The TIAs are realized in pseudo-differential Rauch Biquad [71] configuration with the bandwidth programmable from 6MHz to 35MHz. Capacitor C_1 is realized as an NMOS capacitor [4] and C_2 is realized with a switched, 2fF/μm^2-MiM capacitor array. In the current prototype chip, part of the harmonic rejection circuits and the baseband Cartesian combiners for noise cancellation are implemented off-chip for maximum testing flexibility. In the future, the combiners can be easily integrated on chip using techniques as in [10].

The FTQH receiver prototype is realized with highly programmable circuits that enable dynamic, in-the-field performance tradeoffs between noise, power, linearity and operation modes. The g_m of the LNTAs can be programmed to obtain different signal gains. The bottleneck of the out-of-band blocker tolerance is at the output of the LNTAs, so backing off the gain improves linearity and saves power at the cost of a worse NF. The baseband TIAs have programmable gain,

[4] We find that the linearity of C_1 is not the bottleneck of the receiver linearity performance.

bandwidth and power consumption by programming the values of resistors and capacitors and the number of active slices in the TIAs.

The two FTQH channels can be driven with different LO frequencies for dual-band concurrent reception mode. If very high sensitivity is needed, the two channels can be driven coherently with LO signals from the channel-A divider, and the baseband signals of the two channels can be combined to further reduce the NF. This is achieved by programming the LO multiplexers for the channel-B mixer.

Due to the independent operation of each receiver channel, the linearity of the receiver does not change between the low noise mode and the concurrent reception mode. Backing off in LNTA gain does improve the out-of-band linearity as the bottleneck is at the LNTA outputs.

6.6 Experimental Results

The FTQH receiver prototype chip is packaged in an open cavity 6mm$\times$6mm 36pin QFN package and soldered onto a 4-layer FR-4 PCB for testing. To obtain good symmetry, the PCB transmission lines for the receiver inputs are designed as short as possible for lower loss and the layouts between the hybrid coupler and the receiver chip are kept symmetric to ensure consistency between the reflection coefficients of the *thru* and *cpl* paths to improve the achievable S_{11}. For packaging, the chip is placed at the center of the QFN package cavity so that the bond wires of the *thru* and *cpl* inputs introduce the same amount of parasitics. A grounded pin is placed between these two inputs to improve the isolation between them. The programmable baseband combiners are

implemented in the analog baseband domain with variable-gain amplifiers[5] (VGA) and opamp based combiners as shown in Fig. 6.12. The prototype chip has been characterized with extensive system performance measurements. Since the receiver features ultra-low NF and scalable carrier-aggregation operation, the measurements also fall into these two categories.

6.6.1 Ultra-Low NF FTQH Operation

The NF of the receiver is measured with a NoiseCom NC346A noise source and an Agilent E4446A spectrum analyzer with the NF measurement personality. All the noise measurements include insertion loss of the QH and of the FR4 PCB transmission line between the QH and the chip input. The loss of the feed line to the QH input has been de-embedded. Before each NF measurement, the noise cancellation calibration described in Section 6.2.4 is performed by injecting a -80dBm test tone into the *iso* port and monitoring the down-converted tone at the baseband with the spectrum analyzer. The amplitude of the tone is minimized by adaptively tuning the VGA gains with an automated measurement setup. After calibration, the analog outputs of the two channels on the same chip can be directly combined to improve the SNR as their phase difference is typically less than 10°.

Fig. 6.15(a) shows the measured NF at 900MHz under different configurations. The channel-A *thru* branch alone has a 5dB NF. Combining the channel-A *thru* and *cpl* branches cancels the noise from the termination resistor and using the calibration shown in Fig. 6.7 reduces the NF to 1.8dB. Combining the A and B channels coherently further reduces the NF to 1dB. The 0.2dB increase

[5]The VGAs are AD8330 [86] controlled by MCP4728 [87] 4-channel DACs.

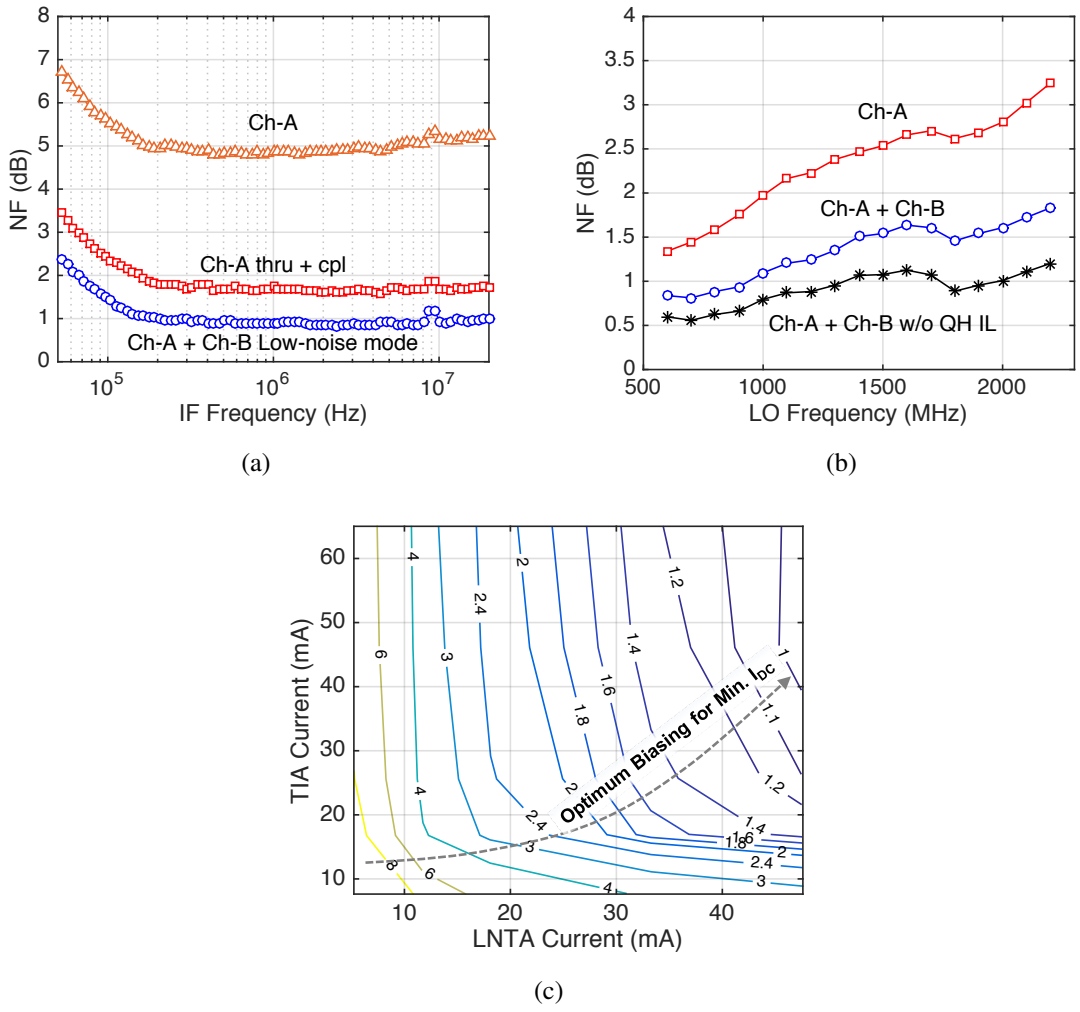


Figure 6.15: Noise-figure measurements of the FTQH prototype as a field-programable wideband SDR: (a) NF measurements at 900MHz across a 20MHz IF bandwidth under different operation modes; (b) NF measurements across different LO frequencies under different operation modes; (c) NF measurements at 900MHz showing in-field NF-power tradeoff.

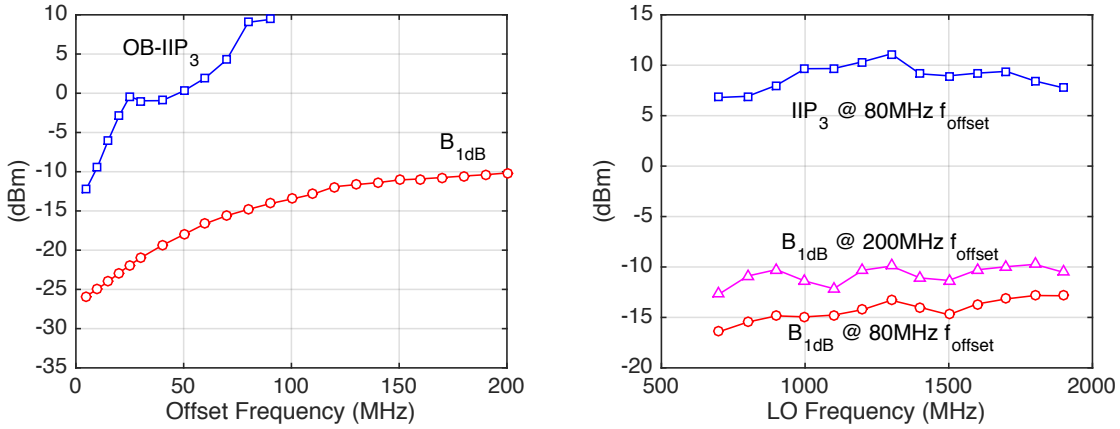
compared to the simulated results is attributed to PCB losses between the hybrid and the chip input. Also, the typical measurement uncertainty for the ENR of the noise source is $\pm$0.1dB [88].

Fig. 6.15(b) shows the measured NF of the FTQH receiver for different LO frequencies. The NF degradation at higher frequencies is caused by two factors: the hybrid coupler and transmission lines have higher insertion loss at higher frequencies; the parasitic capacitance at the input of the LNTA (approx. 1.5pF in total) limits the RF bandwidth to 2.2GHz and causes signal attenuation at high frequencies. The NF for channel A and B combined stays below 1dB up to 900MHz and well below 2dB up to 2.2GHz. After de-embedding the insertion loss of the QH and the transmission line, the NF of the receiver chip is below 1.2dB all the way up to 2.2GHz.

The contour plot in Fig. 6.15(c) shows power-NF tradeoff when the current consumption in the LNTAs and baseband TIAs are reprogrammed by turning on and off G_m slices in both blocks. In the top part of the plot, the contour lines are mostly vertical, and the NF is dominated by the noise of the LNTA. And we can reduce the bias of the TIA while maintaining the same NF. The dashed line in the lower part of the plot indicates the optimum biasing configuration for minimum current consumption for a certain receiver NF.

6.6.2 Linearity Measurements

The out-of-band linearity measurements of the receiver are shown in Fig. 6.16. Thanks to the high isolation and symmetry between the two receiver channels, the linearity of channels A and B are very close, and combining the two channels together does not affect the linearity. Thus, we only report the linearity of channel A for maximum gain and with a 3dB IF bandwidth of 10MHz. Shown



(a) (b)

Figure 6.16: Linearity measurements of on channel A of the FTQH receiver with the IF bandwidth programmed to 20MHz: (a) IIP_3 and B_{1dB} vs offset frequency; for $OB\text{-}IIP_3$ the two tones are placed at around $f_{LO}+f_{offset}$ and $f_{LO}+2f_{offset}$; (b) Linearity measurements across LO frequencies; B_{1dB} improves with 6dB LNTA gain backoff.

in Fig. 6.16(a), both the B_{1dB} and $OB\text{-}IIP_3$ improve as the offset frequency increases. At 80MHz offset frequency, the receiver has +8dBm $OB\text{-}IIP_3$ and -15dBm B_{1dB} respectively Fig. 6.16(b) shows uniform linearity across different LO frequencies.

6.6.3 Concurrency and Carrier Aggregation Measurements

We validate the two proposed aggregation solutions with a concurrent receiver setup where two FTQH chips are daisy-chained so that a total of 4 carriers can be received concurrently (Fig. 6.17(a)). Channels A and B are configured to receive high-frequency carriers at 1900MHz and 2100MHz, channels C and D receive carriers at 690MHz and 900MHz. Fig. 6.17(b) shows the measured conversion gain of the four receiver channels. For NF calibration, a test tone of -80dBm is injected into the daisy chain from the final stage termination resistor (Fig. 6.17(a)) and propagates along the daisy chain to calibrate each receiver channel sequentially before the NF measurements.

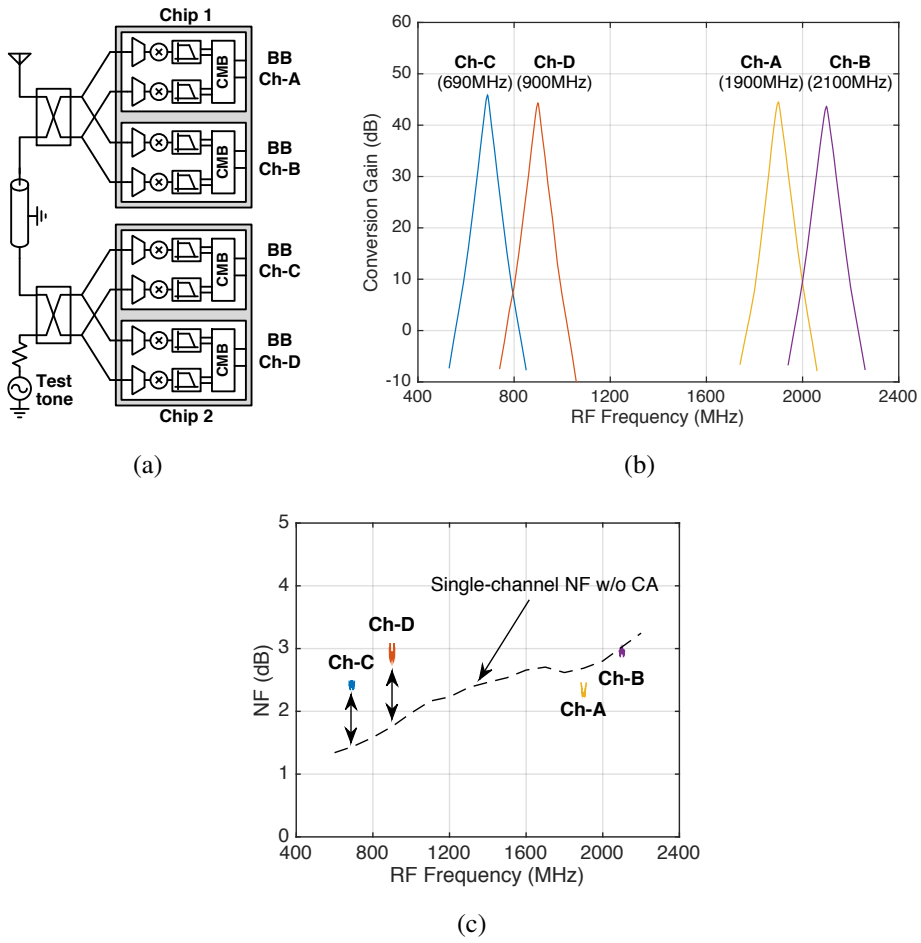
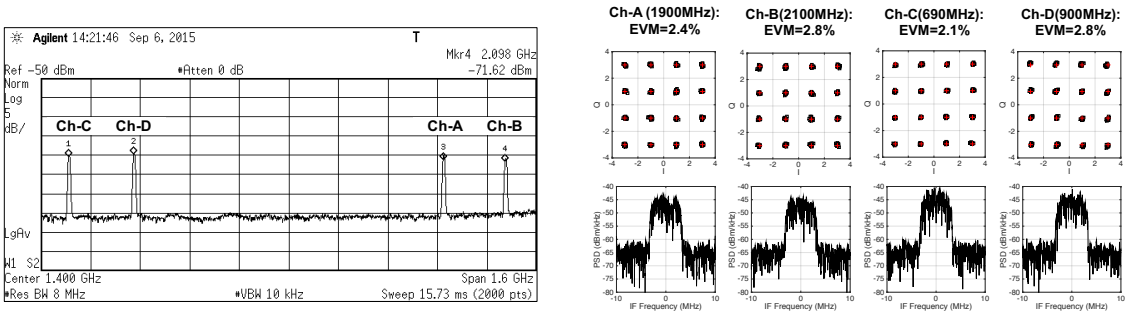


Figure 6.17: Four-channel inter-band CA measurements: (a) Block diagram of the two-chip 4-channel CA setup; (b) Measured conversion gains of the four concurrent channel; (c) NF measurement of each channel, the two low-frequency channels (C and D) have 1dB NF penalty from the insertion loss of the first QH daisy chain stage.

Fig. 6.17(c) shows the measured NF of each channel, and the measured NF of a single channel is overlaid as a comparison baseline for the CA case. It can be seen that the channels A and B on chip 1 have similar NF, within measurement tolerances, compared to the single channel measurements. Channels C and D on chip 2 suffer a 1dB NF penalty from the insertion loss of the hybrid coupler and the cables.

The 4-channel CA receivers are further evaluated with concurrent error vector magnitude



(a) (b)

Figure 6.18: EVM measurements of the 4-channel CA setup: (a) Measured spectrum of the four modulated input carriers each has approximately -70dBm integrated power; (b) Demodulated constellations of the four carriers with a worst-case EVM of 2.8%.

(EVM) measurements. Four modulated carriers are generated, combined, attenuated and fed into the single antenna connector of the CA receivers. Each carrier is modulated with 5MSps 16QAM with $\alpha = 0.35$ with better than 1% EVM with Agilent E4438C. The power of each carrier is controlled to approximately -70dBm at the input of the receiver array. The measured RF input spectrum is shown in Fig. 6.18(a). The 4 baseband IQ signals are then captured concurrently with two 4-channel oscilloscopes and analyzed with the Keysight 89600 VSA software. The demodulated constellations are shown in Fig. 6.18(b). All carriers have lower than 2.8%rms EVM. These receivers measurements were performed without IQ error calibration.

6.7 Discussion and Comparison to the State of the Art

6.7.1 Comparison to Low Noise SDRs and Wideband LNAs

In low-noise combined-mode the FTQH receiver has the best NF among the comparable wideband CMOS SDR receivers as shown in Table 6.1. This does come at the price of increased power

Table 6.1: Comparison to the state-of-the-art high-performance SDR receivers and LNAs.

Design Type	Low Noise SDR Receivers			Balanced LNA
Reference	This Work	[9]	[61]	[80]
Technology	CMOS 65nm	CMOS 40nm	CMOS 28nm	pHEMT
Frequency (GHz)	0.6-2.2	0.08-2.7	0.4-6	0.6-1.2
Max Gain (dB)	48	72	70	14-19
BB Bandwidth(MHz)	6-35	2	0.5-50	N/A
NF w/o Balun/Hybrid (dB)	0.6-1.2	1.5-2.1	1.8-2.4	0.4
NF w/ Balun/Hybrid (dB)	0.9-1.8	N/A	N/R	0.56
Matched RF Input	Yes	Yes	Yes	Yes
OB IIP3 (dBm)	8	13.5	8	16*
B1dB-CP (dBm)	-15 / -10	0	-13	1**
Analog Power (mW)	95	35.1-78	<40	250
LO Power (mW)	2.2-19	N/R	N/R	N/A (LNA only)
Power Supply (V)	1.1	1.3	0.9	5

N/R = Not Reported N/A = Not Applicable * In-band IIP3 **Estimated

consumption comparing to [10] and [62]. The out-of-band linearity is lower than [10] but the presented work has more than 10 times higher IF bandwidth. Comparing to receivers with similar IF bandwidth and power supply [62], the linearity is acceptable. Note that the NF of the FTQH receiver is measured with the loss of the hybrid coupler included and operates with a single-ended antenna interface. For some of the designs with differential RF input [62], the NF should be compared incorporating the loss of the balun. The ultra-low NF of the FTQH receiver is further compared to III-V pHEMT balanced LNAs [80]. Considering that the FTQH implements a full receiver, the CMOS LNTA indeed has comparable NF to the III-V LNAs with much lower power consumption. The linearity falls short due to the much lower available voltage headroom of CMOS technologies.

Table 6.2: Comparison to the state-of-the-art CA receivers.

Design Type	Carrier Aggregation Receivers					
Reference	This Work		[59]		[67]	[68]
	2-Channel	2-Chip, 4-Ch				
Technology	CMOS 65nm		CMOS 65nm		CMOS 65nm	CMOS 45nm
Frequency (GHz)	0.6-2.2	0.6-2.2	0.5-3	0.5-3	1.96	2
CA Bands	2 inter-band	4 inter-band	2 inter-band	2 intra-band	1 inter-band 2 intra-band	2 intra-band
Number of Antennas	1	1	2	1	2	1
Max Gain (dB)	42	42	50	50	45	37
BB Bandwidth(MHz)	6-35	6-35	1-30	N/R	N/R	35
NF (dB)	1.3-3.2/Ch	< 3.2/Ch*	3.8/4.7	4.8	4.5	3.9
OB IIP3 (dBm)	8	8	10	N/R	2.4	2.75
B1dB-CP (dBm)	-15 / 10	-15 / 10	-1	N/R	-15.5	NR
Harmonic Rejection	46/46	-	35/42	N/R	>80	N/R
Analog Power (mW)	96	192	192**	168	155/435***	15
LO Power (mW)	2.2-19	4.4-38	54-194***	54-194***	N/R	NR
Power Supply (V)	1.1	1.1	1.2/2.5	1.2/2.5	1.45/1.8	1

N/R = Not Reported N/A = Not Applicable

*Measured with band combination in Fig. 4 **Estimated from single channel data ***Include PLL

6.7.2 Comparison to Carrier Aggregation Receivers

The FTQH receiver array is a unique single-antenna solution that delivers frequency-agile, inter-band CA. It further delivers an NF comparable with state-of-the-art single-channel receivers while offering up to 4-band CA (Table 6.2). The power consumption is lower than [60] and [67], but these designs have integrated PLLs and/or ADCs, which makes a power comparison hard. The prototype receiver has a programmable IF bandwidth from 6MHz to 35MHz, which is comparable to the other CA receivers. The linearity of the FTQH receiver is lower than that of [60] due to lower filter order[6] and higher LNTA gain. The linearity is comparable to that of [67]. As for intra-band CA, each FTQH channel can cover up to 70MHz of RF bandwidth, so that block down-conversion

[6] R_1 in Fig. 6.14 is bypassed during the linearity measurements for consistency with the NF measurements. We then effectively have a first-order IF filter.

techniques [68] can easily be adopted in future work to support intra-band CA. The current receiver prototype serves as a demonstration of the FTQH concept and is not claimed to be compliant to specific communication standards. The challenge of interfacing with transmitters and RF front-end filters remains the topic of further research.

6.8 Conclusions

In conclusion, the proposed FTQH receiver architecture gives the RF designer the freedom to optimize the LNA/LNTA input impedance independent of RF input matching requirements. Combined with frequency translational signal processing and calibration, FTQH receivers can achieve exceptional noise figure with a wide operation frequency range. The FTQH receiver array also demonstrates support for as high as 4 band inter-band carrier aggregation, which can be further scaled with more parallel receivers or hybrid coupler daisy chains.

Chapter 7

Conclusions

The next-generation wireless communication technology will advance the performance and features of the wireless systems in many aspects such as data rate, spectrum efficiency, energy efficiency, latency, and connection density. Although a unified framework is proposed to accommodate all kinds of wireless devices, they can have vastly different RF specification requirements depending on the deployment scenarios and the RF environment during operation.

One of the major challenges faced by the next-generation wireless system is the ever-increasing number of frequency bands as more RF spectrums are being introduced for a larger system bandwidth. For mobile communication alone there are more than 50 different frequency bands spanning a frequency range of 400MHz to 6GHz, including licensed and unlicensed bands, FDD and TDD bands. These bands are highly fragmented due to legacy issues and often have overlap and conflicts across geological regions. Traditionally, this challenge have to be addressed with RF filters customized for each frequency band. An array of such filters is often needed to support devices for

a global deployment. The emerging carrier aggregation technology needs concurrent transmission and reception from a single antenna and makes the filter band design extremely challenging.

High performance wideband software defined radios are promising candidates to relax the specifications of the RF filters or to completely eliminate them. However, several technology challenges still need to be addressed. The SDRs need to have un-compromised performance comparing to the existing narrow band solutions with RF filters, and significant performance improvements in terms of sensitivity and linearity need to be realized. The SDRs also need to have field programmability for dynamic tradeoffs of their RF performances, and to adjust them to suitable levels for optimum power consumption under different operation scenarios. With the requirement of carrier aggregation, scalable and massive concurrency must be supported with low RF performance penalty and complexity overhead.

7.1 Summary

This dissertation starts with a brief review of the thermal noise canceling technique and its existing practical implementations as wideband LNAs and receiver front ends. The advantages and limitations of the existing noise canceling techniques are identified and discussed. The technique is suitable for high performance SDR receiver front end, but still need further improvement at both the circuit level and the receiver architecture level. In this dissertation, four prototype LNA or receiver chips are designed and each of them pushes at least one aspect of the performance such as bandwidth, linearity, and NF.

The traditional wideband noise canceling LNAs improve the NF at the cost of a higher power

consumption and larger parasitic capacitance, which limits the RF bandwidth of the antenna interface. This bottleneck and fundamental tradeoff is identified and alleviated with the introduction of distributed techniques (Chapter 3). The combination of a noise canceling LNA and a distributed amplifier has a greatly improved bandwidth comparing to a conventional noise canceling LNA and uniquely achieve low NF at both the low frequency and high frequency comparing to a distributed amplifier.

Out-of-band linearity of the SDR receiver is critical to avoid desensitization by large blockers, especially when the RF filter is eliminated. The linearity improvement can be improved either by adopting high-Q programmable RF filters, or by improving the linearity and blocker tolerance of the receiver circuits. We introduced the interferer-reflecting loop (IR-Loop) technique (Chapter 4) to improve the input linearity of the LNA. Multiple programmable filter implementation are demonstrated to have an enhanced loaded Q and lower NF penalty comparing to directly applying the filters at the RF input. We also introduced the hybrid class-AB-C LNTAs for rail-to-rail blocker tolerance (Chapter 5). Transconductor cells that operate in different modes are combined and aligned to extend the linearity operation range of the LNTA. Biasing circuits are designed properly to guarantee robust operation across PVT variations.

The NF of the receiver directly affects the sensitivity of the wireless communication link. The NF optimization in wideband LNA and LNTA design is often limited by the input impedance matching requirements. We introduced the FTQH technology that adopts an quadrature hybrid coupler at the inputs of the receiver for wideband input impedance matching (Chapter 6). This technique completely alleviates the input matching constraint on the LNAs and LNTAs and an

arbitrary impedance can be used to optimized the NF. With the use of current-reuse CS LNTAs, wideband sub-1dB NF is achieved with a full-CMOS SDR receiver with only one external passive components.

In addition to the performance enhancements of the SDR, more advanced features such as concurrent reception are needed for flexible aggregation of the fragmented spectrum. We introduced the FTQH receiver array as a scalable solution to wideband frequency-agile inter-band carrier aggregation. The unique antenna interface facilitates the use of high-input-impedance LNTAs and enables voltage domain voltage splitting directly at the LNTA input nodes. In addition to the voltage domain RF signal splitting, the FTQH receivers can also be daisy-chained as most of the power from the antenna is reflected and redirected to the isolation port. The number of concurrent reception channels can be scaled in two dimensions and forms a highly flexible receiver array.

Finally, field programmability is also featured in these designs to enable dynamic performance tradeoff between the NF, linearity, power consumption and concurrency. For the IR-LNAs and the FTQH LNTAs, the RF g_m cells are implemented with multiple unit slices, each of which can be digitally turned on and off for a dynamic tradeoff between the NF and power consumption. In the class-AB-C LNTA design, each of the g_m slice can be individually biased into a different operation mode for a tradeoff between the NF, power, and linearity. The IR-Loop can be dis-engaged when large blocker is absent to save power and improve NF. In the FTQH receivers, the parallel receiver channels can be programmed to receiver multiple carriers concurrently or to receive the same carrier coherently for an ultra-low NF.

7.2 Future Research

The study presented in this dissertation leads to several topics for future research.

Some of the techniques demonstrated in this dissertation are compatible with each other and can be combined to further push the performance of wideband SDRs. For example, the class-AB-C LNTAs can be easily combined with the FTQH receiver architectures for an ultra-low-noise, ultra-high-linearity receiver.

Modern receivers need to open up the IF bandwidth to accommodate a wideband carrier or multiple adjacent carriers, and this makes the receiver more susceptible to close-by interferers. As the duplexing frequency spacing of the transceiver becomes smaller, and the spectrum becomes more crowded, the requirements on both the RF and IF filters become more stringent. In addition to the blocker tolerance challenges, multiple out-of-band interferers can create intermodulation products that corrupt the desired in-band signals. For close-by interferers, the filters offer limited protection for the receiver. There are opportunities for digital-assisted intermodulation cancellation schemes to improve the linearity of wideband SDRs for close-by interferers. If each interferer can be measured with a sufficient SNR, their intermodulation product can also be reproduced with high SNR. Thus digital cancellation of the intermodulation product will not impose significant noise penalty on the desired signal.

The FTQH receiver array addresses the challenge of scalable concurrent reception. However, scalable concurrent transmission and RF multiplexing circuits still remain a very challenging problem. Due to the various limitations of the current wideband duplexing methods, RF filters and duplexers still cannot be completely eliminated. If multiple carriers need to be received and trans-

mitted concurrently, an RF multiplexer needs to be specially designed for the specific frequency band combination. Due to the large number of band combinations, the complexity of such antenna interfaces grows rapidly. The FTQH technology has the potential to incorporate RF filters into the RF daisy chain. As most RF filters are realized with high-Q resonators that have reflective out-of-band impedances, they can be combined with quadrature hybrid couplers to realize a flexible and modular antenna interface for concurrent transmission and reception.

The impedance and performance of the antennas on handset devices are susceptible to the RF environments and the proximity of nearby objects. As a result, antenna impedance tuners are often introduced to fight against such RF impairments and to adjust the antenna impedance closer to the system impedance of 50Ω. Such impedance tuning circuit work best with a closed-loop control system. The antenna impedance or VSWR is sensed and used to assist the control algorithm for the impedance tuner. FTQH receiver needs a calibration process for optimum noise cancellation, the coefficients obtained during the calibration process contain full information of the antenna impedance. With proper calibration and de-embedding, the FTQH receiver can serve as a single-port vector network analyzer and sense the antenna impedance with both the magnitude and the phase information. The antenna impedance sensing can be performed at the frequency of each carrier to be concurrently received. Designing impedance tuning circuits that can optimize the antenna VSWR at several frequencies is also a challenging and valuable problem that is yet to be solved.

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