Monolithically Integrated Acoustic Resonators on CMOS for Radio-Frequency Circuit Applications

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ABSTRACT

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Wireless communication circuits rely on the use of high-quality passive elements (inductor-capacitor resonant tanks) for the implementation of selective filters and high-purity frequency references (oscillators). Typically available CMOS, on-chip passives suffer from high losses, primarily inductors, and consume large areas that cannot be populated by transistors leading to a significant area penalty. Mechanical resonators exhibit significantly lower losses than their electrical counterparts due to the reduced parasitic loss mechanisms in the mechanical domain. Efficient transduction schemes such as the piezoelectric effect allow for simple electrical actuation and read-out of such mechanical resonators. Piezoelectric thin-film bulk acoustic resonators (FBARs) are currently among the most promising and widely used mechanical resonator structures. However, FBARs are currently only available as off-chip components, which must be connected to CMOS circuitry through wire-bonding and flip-chip schemes. The use of off-chip interfaces introduces considerable parasitics and significant limitations on integration density. Monolithic integration with CMOS substrates alleviates interconnect parasitics, increases integration density and allows for area sharing whereby FBARs reside atop active CMOS circuitry. Close integration of FBARs and CMOS transistors can also enable new circuit paradigms, which simultaneously leverage the strengths of both components.

Described here, is a body of work conducted to integrate FBAR resonators with ac-

tive CMOS substrates (180nm and 65nm processes). A monolithic fabrication method is described which allows for FBAR devices to be constructed atop the backend small CMOS dies through low thermal-budget ($< 300°C$) post-processing. Stand-alone fabricated devices are characterized and the extracted electrical model is used to design two oscillator chips. The chips comprise amplifier circuitry that functions along with the integrated FBARs to achieve oscillation in the 0.8-2GHz range. The chips also include test structures to assess the performance of the underlying CMOS transistors before and after the resonator post-processing. A successful FBAR-CMOS oscillator is demonstrated in 65nm CMOS along with characterization of FBARs built on CMOS. The approach presented here can be used for experimenting with more complex circuits leveraging the co-integration of piezoelectric resonators and CMOS transistors.

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Chapter 1

Introduction

1.1 Background and Motivation

Silicon transistor integrated circuit (IC) technology has led to very profound improvements in the performance of electronic devices, reduction in power consumption and drastic reductions in size. This has been coupled with a dramatic increase in the reliance on digital circuits which operate with binary signals quantized in time. Digital circuits are contrasted with their analog counterparts which process signals with continuously varying signal levels. Digital circuits highly programmable and more robust to signal noise than analog circuits. Electronics in mobile communications systems are no exception to this trend. With the huge increase in the number of transistors per square mm of silicon, digital transistor circuits are being recruited to perform and more of a radio transceiver system′s functionalities. As a result, the natural evolution of radios is towards the software defined radio paradigm [1], whereby most of the radio functions and operation are performed digitally and can easily be modified in software. However, the communication medium, i.e. the wireless spectrum, is analog in nature and thus it is necessary to digitize inputs and outputs in a manner that allows interfacing with the digital radio core. Conceptually, a purely digital, software defined radio requires an analog-to-digital converter (ADC) to digitize

the analog wireless signals picked up by the radio antenna and relay them onto the digital section of the radio (Figure 1.1). Analogously, a digital-to-analog converter (DAC) would be needed for transmission in the opposite direction. In practice, such an ADC/DAC would have to operate at high sampling rates leading to prohibitively large power dissipation [2, 3].

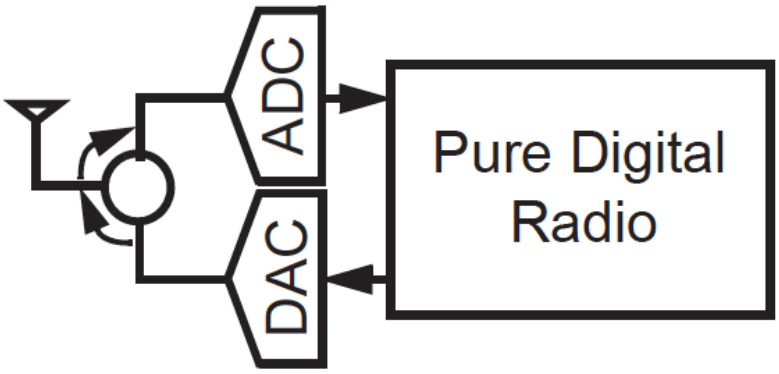


Figure 1.1: The Pure Digital, Software Defined Radio [3].

In practice, it is the RF front-end portion of the receiver that serves as in intermediary between the antenna and the digital base-band unit. The RF front-end achieves this by performing a number of analog signal processing functions namely, frequency translation (mixing), filtering and amplification (gain) that condition the wireless signals from the antenna to a form that is usable by low-cost, low-power digital circuitry. Amplification is most commonly performed using transistor amplifier circuits whereas filtering and amplification almost invariably rely on the use of electrical passive components i.e. inductors and capacitors.

Leveraging the significant advances in silicon manufacturing technology motivated by what is known as Moore′s law and the dimension-scaling of digital circuits, modern digital CMOS processes provide designers with high-speed transistors (unity gain frequency >210GHz [4]) in large numbers and reasonable device-to-device variability. Unfortunately, the same does not apply to the selection of passive components

available in modern digital CMOS processes. There is an increasing move towards system-on-chip (SoC) solutions where all of a system's functions are crammed into a single integrated circuit [5] and the SoC areas are dominated by the digital blocks. Consequently, RF front-end and analog designers are increasingly prohibited from using CMOS technologies with improved passives optimized for analog circuit design as opposed to digital design.

1.2 Mechanical vs. LC Passives

Whereas most CMOS processes provide reasonable performance capacitors (quality factors around 100), these capacitors introduce significant area penalties whether implemented in the front-end (MOS capacitors and deep trench capacitors) or the back-end (Metal-insulator-metal caps), which reduces available area for transistors and interconnect routing layers.

On-chip inductors are far inferior to their off-chip counterparts due to their very high loss factors and large areas. Magnetic fields generated by current flow in the inductor will induce eddy currents in the silicon [6–8]. This leads to very low quality factors (< 30). Another significant limitation of inductors is the large area penalty they incur. Due to eddy currents developed in the underlying substrate, in general, active and passive components cannot be placed underneath inductors, rendering the silicon and interconnect area dead. Using silicon-on-insulator technologies (SOI) can reduce losses, but SOI technologies are generally more costly than bulk technologies and it is still unclear if this situation will change in the near future [9]

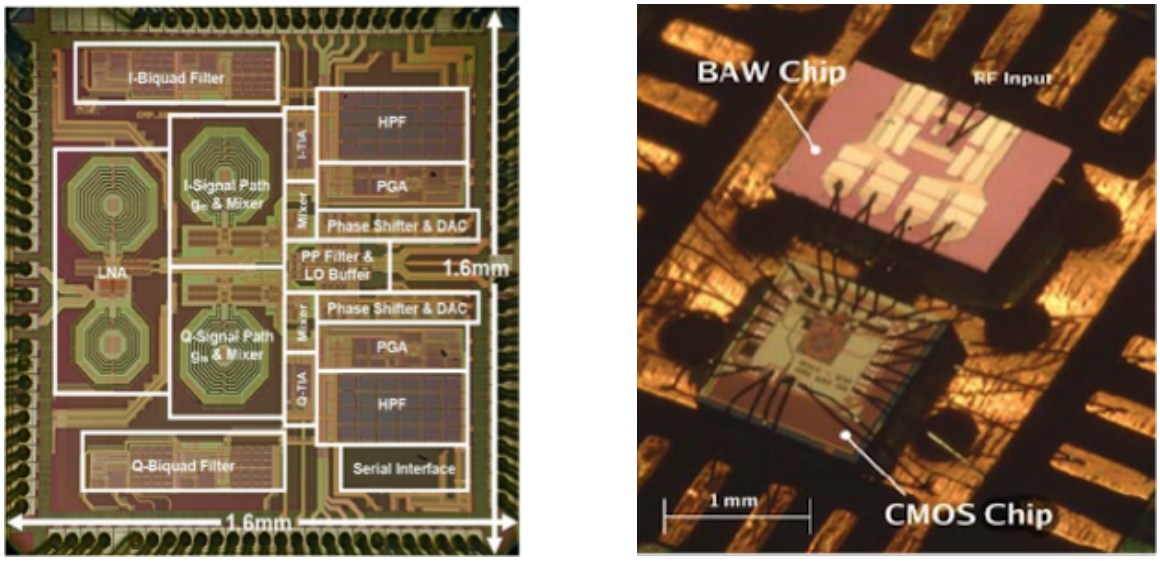
For the most demanding applications, such as timing references, and selective front-end filters and antenna duplexers, there has been near unanimous adoption of mechanical resonant devices [10–13]. In mechanical resonant devices, an electrical signal is converted into an acoustic wave in the mechanical domain through a specific

transduction mechanism (e.g. electrostatic, piezoelectric). Depending on the physical dimensions of the device, a high quality mechanical resonance will occur at a specific frequency. Reduced loss pathways and efficient transduction mechanisms are leveraged to enable higher quality factors (orders of magnitude) than those attainable using standard LC passives. Mechanical crystal filters based on exotic ceramics have long been used for filtering applications [14] and the venerable quartz crystal oscillator, also based on mechanical resonance, enjoys near universal application as an oscillator source in phase-locked loop circuits [15, 16]. Due to their operation at radio-frequencies (RF), mechanical resonant devices typically have dimensions on the order of micrometers, therefore the terms mechanical resonator and micro-electro-mechanical (MEMS) resonators are often used interchangeably.

Despite their excellent electrical performance, mechanical resonant devices are typically fabricated using manufacturing processes not easily merged with silicon CMOS manufacturing [17] or ones that occupy too much silicon area that could instead be used for transistors [18]. As a result, mechanical passives are almost invariably used as external components that need to be integrated with CMOS transistor circuitry using heterogeneous integration schemes such as wire-bonding and flip-chip interconnection. At RF and microwave frequencies, bond-wires introduce significant inductive parasitics that complicate circuit design [19]. Moreover, off-chip components are designed with very specific port impedances (typically 50Ω) to enable standardized coupling of off-chip modules. Whereas the standardized impedances help from a component modularization standpoint, the designer loses flexibility in impedance selection, which limits freedom in terms of where the mechanical passive can be used within the circuit. Relegating mechanical passives to off-chip placement also greatly reduces any possibility of programmability/trimming that can be introduced by re-organizing CMOS transistors around the mechanical passives.

As a result, the current RF designer′s toolkit is as follows; On-chip LC passives

are available in most CMOS processes but with considerable performance and area penalties. For applications where on-chip LCs cannot reasonably meet required performance specifications (Duplexers,front-end,etc...)mechanical resonators can be used, but in very limited numbers and with virtually no tunability/reconfigurability due to their off-chip form factor. Figures 1.2a and 1.2b put into perspective the possible form factors for RF design in current technology.



(a) (b)

Figure 1.2: Current RF design options: (a) Integrated LC receiver with large inductors visible [20] (b) CMOS chip integrated with BAW mechanical filter chip using wirebonding [21].

Amidst this technological landscape, two key challenges are arising: The explosive increase in demand for high data rates and communication bandwidths in the past years has resulted in a large number of different communications standards assigned to different portions of the electromagnetic spectrum, each with its own frequency planning specifications. Software defined radios are seen as a flexible hardware solution that can that can function with multiple different standards by merely adjusting

adjusting the baseband software. However, a flexible RF front-end is required in order to cope with the different standards. Figure 1.3 shows a multi-band radio module from Triquint semiconductor. The image shows a dedicated BAW or SAW filter, both mechanical resonant devices, dedicated for each frequency band. With the increasing number of communication bands and standards, more and more of filters will be required. Therefore component designers are left with the challenge of trying to integrate more and filters without increasing size and cost. This is an active area of industrial development and research [22–24]. However, it appears that future solutions will continue along the lines of heterogenous integration such as wire-bonding and flip-chip.

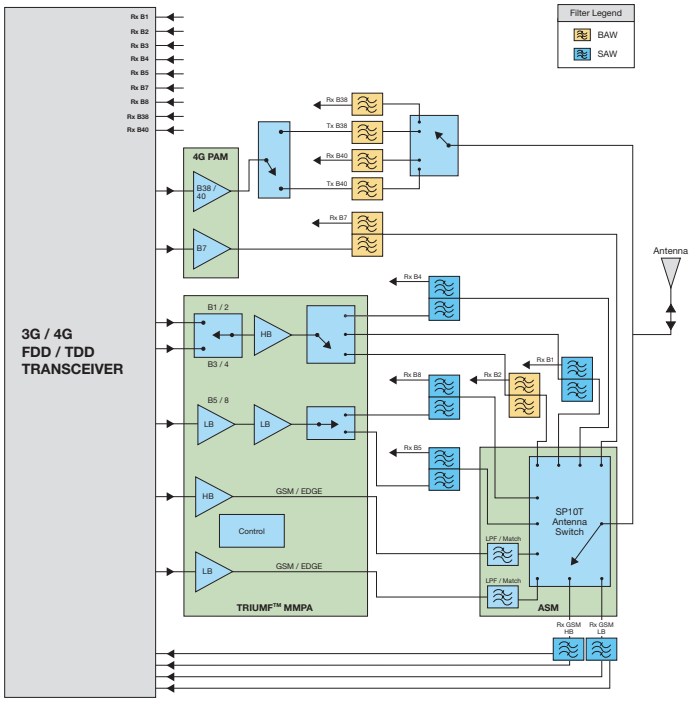


Figure 1.3: Block diagram of a 3G/4G multi-band radio module from Triquint Seminconductor [25].

Another more difficult problem is that of frequency diversity [26]. The wireless

spectrum consists of a finite set of frequencies that are usable for communication applications. Each communication standard is assigned a fixed set of frequencies over which data transmission may take place. The frequency allocation is fixed. Furthermore, the individual frequency bands are separated by empty guard bands. The guard bands are a "spectral no-man's land" where communication is not allowed in order to avoid power leakage between adjacent communication bands. If the assigned user is not using their designated portion of spectrum, it will remain unused since no other user is allowed access to this portion. For bursty, non-constant communication, this is clearly wasteful of the spectrum. A solution is what is known as the cognitive radio [26]. A cognitive radio is aware of its spectral surroundings and can dynamically adjust communication bands to use currently unoccupied frequencies and achieve more efficient spectral utilization as shown in Figure 1.4. A cognitive radio monitors large swathes of the electromagnetic spectrum with signals varying substantially in power levels. In the more dynamic spectral environment observed by a cognitive radio, frequency planning alone is not sufficient to avoid interference between different users since the frequency planning is no longer static, but evolving depending the number of users transmitting at any instant in time. Selective filters are necessary in order to prevent strong interferers from corrupting nearby weak desired signals. Once again, such performance is generally not achievable with standard CMOS circuitry (without unacceptable power consumption) and mechanical filters are need in this case.

In summary, it is clear that demand for high-quality RF-MEMS components will only increase with the continuing evolution of new communication hardware. Closer integration between these devices and transistor circuits is continuing target.

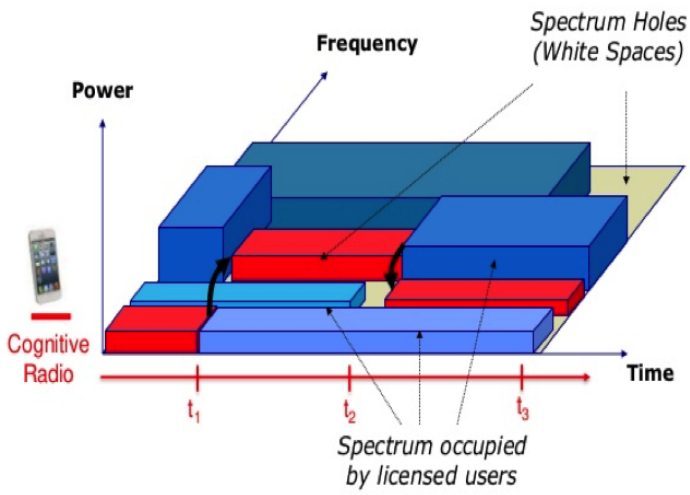
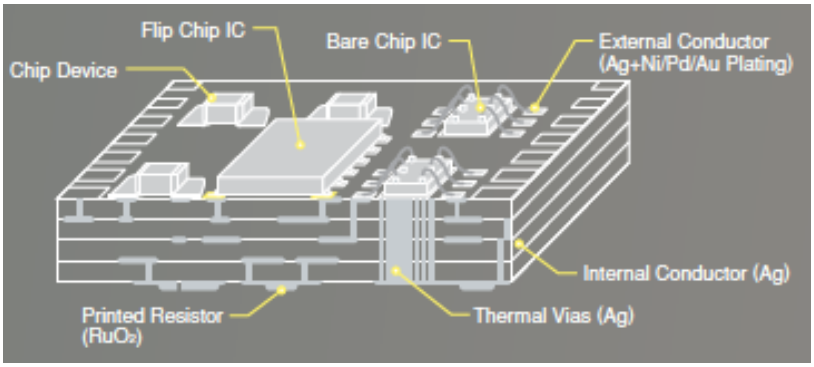


Figure 1.4: Cognitive radio concept [26].

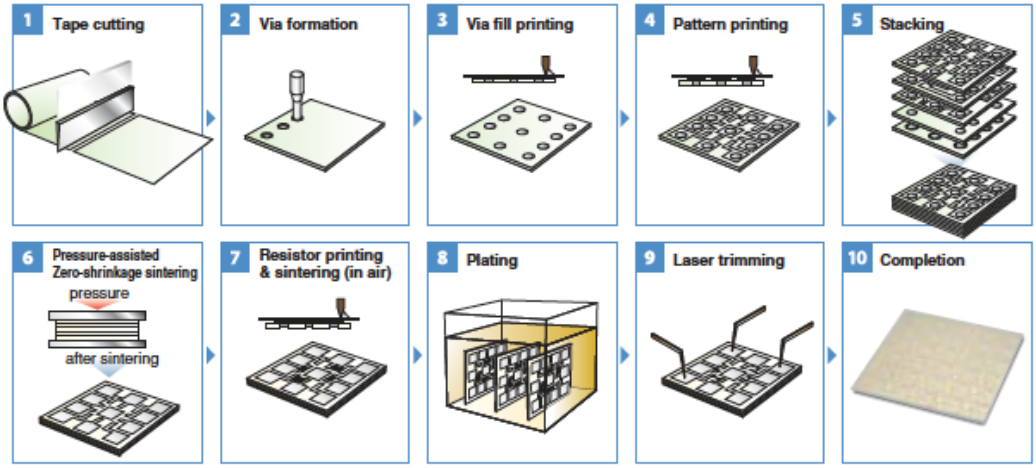
1.3 SoC vs. SiP

To date, the majority of wireless design for mobile communications follows the system-in-package (SiP) paradigm. Here the different components required, each already individually packaged, are brought together onto a carrier substrate and interconnected together and the whole assembly is collectively packaged. The interconnection can be made through wire-bonding, flip-chip techniques or a combination of both. The components are combined using polymer bonding or low temperature co-fired ceramic (LTCC) techniques [27]. LTCC supports a variety of compoennts including integrated circuits (ICs), passives and printed resistors. In LTCC, Ceramic tape is used as a substrate on which the different components are placed. Conductive copper or silver traces are printed on the ceramic tape for electrical interconnection of the different components. The component-populated ceramic tapes can be stacked vertically to reduce overall size. This is achieved using holes known as "vias" that enable vertical interconnection. Finally, The whole assembly is sintered or fired at temperatures below 1000C to bond all the components together into one solid assembly [28]. A LTCC

assembly is shown in Figure 1.5a with the fabrication process depicted in Figure 1.5b.



(a)



(b)

Figure 1.5: LTCC module structure and fabrication: (a) Schematic of a LTCC module [28] (b) LTCC module fabrication [28].

LTCC and similar techniques have led a dramatic reduction in size for mobile communication electronics. And there is ongoing industrial research and development to achieve further reductions in size [13]. The main advantage of LTCC techniques is reduced cost and ease of assembly. Here, each component is fabricated separately the integration is only done at the end. Therefore, fabrication of each component can be optimized independent of other components.

However, a more aggressive integration scheme can provide advantages unattainable by LTCC and similar heterogenous integration schemes. First, direct system-on-chip (SoC) integration where all the circuitry and MEMS devices are fabricated atop each other, in a monolithic layer by layer fashion can enable drastic reductions in size beyond what is attainable with heterogenous schemes. Monolithic integration would also save space by sharing component packaging across multiple components. In addition to size reduction, parasitics would be be greatly reduced since the MEMS components are in close-proximity to the transistor circuitry alleviating the need for long wiring. Reduced parasitics can simplify system design and enhance performance . Beyond size and parasitic reduction, more fundamental advantages emerge. Typically RF components in wireless system design are designed with strictly define impedance levels (commonly 50Ω) for their input and output ports. Whereas, standardized impedances are advantageous from a system modularization perspective, the designer is denied the freedom of adjusting impedances; a standard impedance such as 50Ω is not always the best choice for different circuit blocks. Monolithic integration, where transistors and brought in close proximity, can enable co-design of both components to achieve best performance [13, 19].

Finally, monolithic integration can enable paradigm shifts in RF system design whereby large numbers of transistors are "wrapped around" the MEMS devices. Transistor switches can enable dynamic reconfigurability of a MEMS based circuit where large banks of MEMS devices are controlled by sophisticated transistor circuitry. There is growing interest in tunable filters [29] which combine acoustic MEMS devices with variable capacitors to achieve tunability (Figure 1.6). Transistor-MEMS integration would provide new avenues for extending this concept. Such opportunities would not be available in heterogenous integration schemes where large component size and increased parasitics limit applicability.

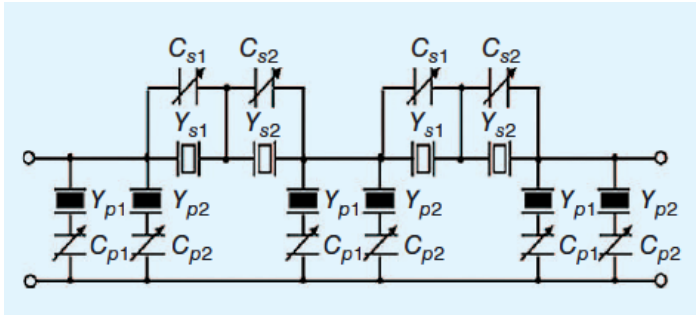


Figure 1.6: Tunable BAW filter structure with variable capacitors [29].

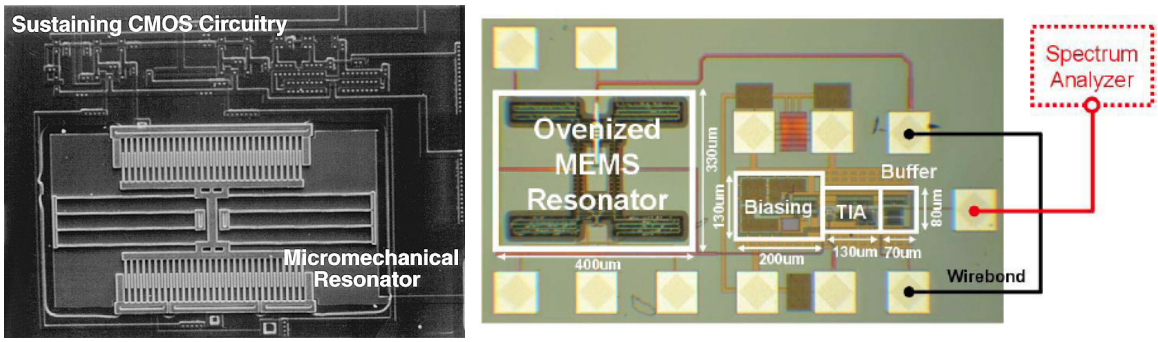
1.4 Mechanical Resonator Types

A key differentiator of different mechanical resonator technologies pertains to their mechanism of transduction, namely how the input signal is coupled from the electrical domain to the mechanical domain, where the resonance takes place, and consequently back to the electrical domain for output detection. The two most popular mechanical transduction mechanisms are electrostatic and piezoelectric. Piezoelectricity refers to a mechanism by which certain crystal structures generate charge (i.e. electric field) in response to a mechanical deformation and vice-versa. In capacitive resonators, transduction takes place through electrostatic attraction and charge conservation. Piezoelectric transduction is usually orders of magnitude more efficient than electrostatic transduction [30,31]. The majority of commercially successful MEMS resonator devices are piezoelectric. Higher piezoelectric transduction efficiencies result in lower impedance values ($1-300\Omega$) which are more compatible with RF system design techniques than the higher impedances ($\sim 1\text{M}\Omega$) of electrostatically transduced devices. Consequently, here will be more focus on piezoelectric devices in the coming sections.

1.5 Current Integration demonstrations

Motivated by the possible advantages, there have been a number of demonstrations of MEMS resonators monolithically integrated with CMOS circuits. These are distinguished by the fabrication of the MEMS device directly on the same piece of silicon as the CMOS transistors as opposed to heterogenous integration such as wire-bonding where the CMOS and MEMS devices are located in separate packages or modules. These can be split into two classes: those with electrostatically transduced MEMS and those with piezoelectric MEMS. In the first class, the demonstrations either rely on fabricating the *MEMS first* on specific area of a silicon wafer and later fabricate the CMOS transistors in different area [18] *or* the CMOS transistors are first fabricated using standard silicon processing techniques and the MEMS is built in the CMOS wiring layers using subtractive patterning or etching [32–34]. The first technique allows custom tailoring of the MEMS device properties since the CMOS and MEMS fabrication is decoupled but it technically complex. Whereas the second approach allows for simpler processing, however since the MEMS is built at the end, only materials compatible with the thermal properties of the CMOS transistors are allowed thereby limiting the flexibility with which the MEMS can be fabricated. Typically the thermal limit for CMOS processes is $300C$ beyond which metal wiring layers (typically aluminum or copper) significantly deteriorate [32]. All the above approaches lead to trade-off between the area used by the MEMS structure and that for transistors since these areas cannot be shared. Furthermore, such MEMS devices require vacuum packaging to operate properly and exhibit large impedances ($\sim$1MΩ) which are not compatible with 50Ω impedance levels customarily found in RF systems. Shown in Figure 1.7 are MEMS-CMOS oscillator systems presented in [32] and [34].

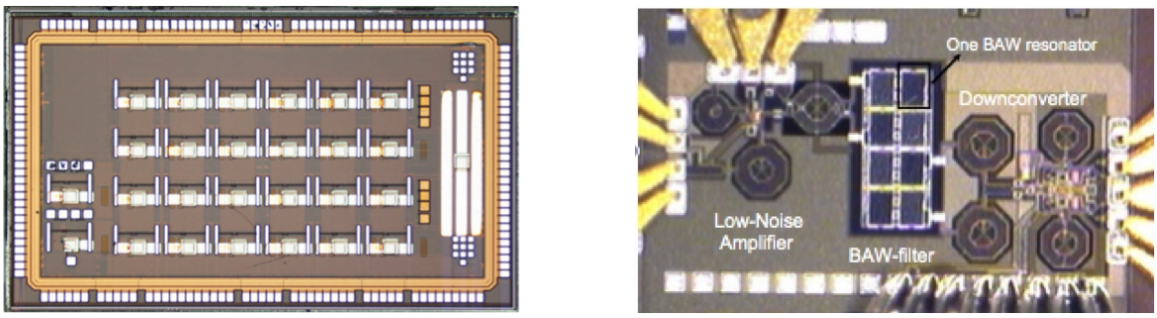
There have also been a number of demonstrations of monolithic MEMS-CMOS integration based on piezoelectric MEMS devices. These invariably rely on a MEMS-



(a) (b)

Figure 1.7: CMOS integrated electrostatic MEMS oscillators: (a) CMOS comb-drive resonator integrated oscillator [32] (b) Integrated monolithic CMOS-MEMS oscillator [34].

last approach where the piezoelectric MEMS is built atop the completed CMOS transistor wafer or die. Monolithically integrated MEMS oscillators and filters have been applied to biological sensing applications [35] and RF receivers [19] The piezoelectric MEMS devices exhibit lower quality factors than their electrostatic counterparts in return for much lower impedance levels compatible with 50Ω systems.



(a) (b)

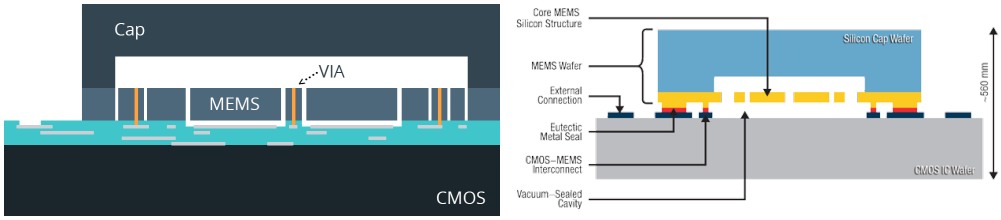
Figure 1.8: Demonstrations of monolithically integrated piezoelectric MEMS resonators on CMOS: (a) Monolithic MEMS resonator array on 180nm CMOS [35] (b) RF front-end based on CMOS-integrated MEMS resonator-filters [19].

1.6 Challenges of SoC Integration

Despite the basic feasibility of CMOS-Mechanical resonator integration, concerns have been raised regarding the yield of such integration [17]. The most feasible integration schemes involve completion of the CMOS followed by fabricating of the MEMS portion. Since the yields of the two process are multiplicative, the yield of the combined process will generally be lower than the yields of each individual process which can further drive up costs. Moreover, MEMS technology typically involves less layers and much more relaxed tolerances on lithography resolution and fabrication tool specifications than CMOS transistor technology.

Once additional concern that has been raised with CMOS-MEMS integration is the need for complicated packaging [13]. A MEMS device involves mechanically vibrating structures that may often be free-standing. Dust and moisture can potentially lead to significant MEMS device degradation. Therefore, specialized packaging schemes involving hermetic sealing. This is to be contrasted with CMOS ICs, packaging merely involves simple moisture barrier schemes that are significantly cheaper than their MEMS counterparts. In recent years, there have been significant technological advances and cost-reductions in packaging technologies [36], with several commercially successful MEMS products on the market [37]. New packaging technologies provide monolithic MEMS-CMOS integration in a fabless fashion that is agnostic to the particular CMOS transistor process being used [38]. As a result, MEMS packaging is becoming a much less of a hurdle for MEMS-CMOS integration.

In summary, monolithic integration provides a number of unique design advantages However, technological complexity and corresponding costs have understandably lead to a prevalence of the SiP approach. Silicon IC foundries exclusively fabricate transistors on silicon wafers ranging in size from 4-12 inches in diameter [39]. With the prohibitively large cost of producing a silicon transistor wafer, foundries are not inclined to experiment with the challenges MEMS-CMOS integration unless



(a) (b)

Figure 1.9: Commercial CMOS-MEMS products: (a) mCube^{TM} Monolithic MEMS platform [38] (b) Invesense$_R$ CMOS-MEMS platform [37].

there are economic incentives. Here, it is worth pointing out that a number of highly complicated transistor technologies [40], involving radical changes in fabrication processes have made the leap from concept to high-volume, high-yield production [41]. Therefore, with sufficient demand for integrated CMOS-MEMS platforms, there will be sufficient financial motivation for foundries to solve the yield issues necessary for high-volume manufacturing

What is needed, is a low-cost, low-risk approach for experimenting with MEMS-CMOS integration and exploring the new design approaches enabled by the integration. The use of multi project wafer (MPW) services [42] has long been a common practice for industrial and academic research groups for obtaining high-quality silicon transistor ICs in an economical fashion. MPW services combine designs from multiple users and are integrated onto a single wafer that can be produced by a dedicated silicon IC foundry. All the technological complexity of producing a wafer is handled by the foundry with no user involvement. The foundry dices the wafer into multiple dies that can be packaged and use by the end-user. Fabricating MEMS devices directly on MPW dies would provide the end-user with the sought after, low-risk and low-cost approach to experimenting with MEMS-CMOS integration. To date, the vast majority of monolithic integration of MEMS on CMOS has been performed on wafers with the exception of [35] which utilized CMOS dies. However, this work was

targeted towards sensing. Extending die-level techniques to RF circuit applications would be advantageous and is the main thrust of this thesis.

1.7 Thesis Goal

The goal of this thesis is to help in providing RF designers with platforms enabling experimentation with new circuit topologies leveraging the combined advantages of CMOS transistors and MEMS passives. To achieve this goal, die-level processing techniques have been developed which enable robust fabrication of piezoelectric MEMS resonators directly above foundry-sourced CMOS dies. The design and implementation of CMOS-MEMS oscillators is discussed in detail in the following sections. The process described here-in starts from the fabrication of stand-alone MEMS devices on low-cost passive glass substrates, followed by the electrical characterization and modeling of said devices and ultimately leading to the successful co-integration of the MEMS device and CMOS transistors.

1.8 Thesis Organization

Chapter 2 presents relevant background on acoustic devices and piezoelectricity, leading to the development of electrical models that can be used for subsequent circuit design. The basic elements of the film-bulk acoustic resonator (FBAR) resonator structure are outlined along with a discussion of necessary properties of materials used in the structure. The FBAR is the primary structure that will be used through this thesis. Chapter 3 relates the electrical model of the FBAR to the physical structure and delves into the fabrication techniques employed in FBAR fabrication. Lithographic patterning and thin-film deposition techniques used in the FBAR fabrication along with corresponding optimizations to improve FBAR performance. The

measurements of the fabricated FBAR devices are fit to a lumped model which is used to demonstrate basic filter structures. Chapter 4 starts off with the discussion of two RF IC designs in 65nm and 180nm CMOS for demonstrating FBAR-CMOS co-integration. The electrical models from chapter 3 form the basis of these designs. The second portion of chapter 4 goes into the details of a specially developed post-process for integrating FBARs on small CMOS dies. The chapter is concluded with a discussion of results for an FBAR-CMOS oscillator operating at 1.75GHz along with direct measurements of FBARs fabricated on CMOS.

Chapter 2

Acoustic Resonator Background

2.1 Introduction

This chapter provides a brief overview of the fundamentals of acoustic devices with an emphasis on resonators. First, the basics of acoustic wave propagation are discussed. Following this, the piezoelectric effect is introduced and combined with acoustic wave formalism to present the Mason and Butterworth-Van Dyke electrical models for an acoustic resonator. These models will be the basis of subsequent circuit design using such resonators. Finally, the film-bulk acoustic resonator (FBAR) structure is presented, which is the primary resonator structure that will be used in the rest of the thesis.

2.2 FBAR Background

A thin-film bulk acoustic resonator (FBAR) consists of a metal-piezo-metal sandwich as shown in Figure 2.1 [43]. Applying an electrical signal to the metal electrodes triggers and acoustic excitation in the structure through the piezoelectric effect. The resonator presents an "acoustic transfer function" to the incoming acoustic excitation,

determined by the geometry and constituent materials of the resonator structure. In a properly designed resonator, the structure will present a sharp mechanical resonance around its natural vibration frequency. The resulting acoustic signal can then be picked up electrically through the inverse piezoelectric effect. Consequently, an FBAR provides an electrical input, electrical output resonator with typically smaller sizes than an electromagnetic resonator since the velocity of acoustic waves in the FBAR is much lower than the phase velocity of waves in an electromagnetic resonator. FBARs have been demonstrated up to 8 GHz resonance frequency with high quality factors [44]. The following sections will be dedicated to developing an electrical model of the FBAR and outlining the practical details of the structure.

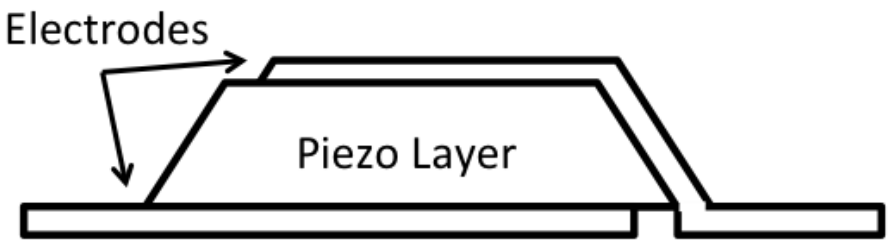


Figure 2.1: Basic FBAR structure.

2.3 Wave Propagation and Thin-Film Resonance

2.3.1 Wave Propagation

Acoustic devices are based on the propagation of acoustic devices through solid media. In a solid, small, localized particle displacements form their equilibrium position collectively lead to a much larger motion across the solid which constitutes an acoustic wave. The solid medium can be viewed as a distributed spring-mass stem where particles are confined to their local positions by local restoring forces behaving similarly

to an ideal spring whose deformation is governed by Hooke's law

$$F = -kx \tag{2.1}$$

In a solid material under deformation, Hooke's law can be rephrased in terms of stress and strain. Stress (T) is a measure of internal restoring forces and is computed as applied force per unit area. Strain (S) corresponds to the deformation of a volume as a fraction of its original dimensions. In the most general case of a non-piezoelectric material, Hooke's law now becomes:

$$T = cS \tag{2.2}$$

where c corresponds to the stiffness of the material, analogous to the spring constant k in the above equation.

Observing a unit material volume of area A, thickness ∂z and density ρ, Netwon's second law of motion $F = ma$ can be rephrased in terms of stress and strain as

$$\frac{\partial T}{\partial z} = \rho \cdot \frac{\partial^2 u}{\partial t^2} \tag{2.3}$$

where $F = \frac{\partial T}{\partial z} \cdot \Delta V$ and $ma = (\rho \cdot \Delta V) \cdot \frac{\partial^2 u}{\partial t^2}$ and u corresponds to the particle dipslacement.

Using Hooke's law and combining with the definition of strain:

$$S = \frac{\partial u}{\partial z} \tag{2.4}$$

a wave equation is obtained:

$$\frac{\partial^2 u}{\partial t^2} = \frac{c}{\rho} \cdot \frac{\partial^2 u}{\partial z^2} \tag{2.5}$$

this corresponds to a wave propagating with phase velocity

$$v = \sqrt{\frac{c}{\rho}} \tag{2.6}$$

In this case, the displacement can be assumed to be of the form

$$u(z,t) = [a \cdot sin(kz) + b \cdot cos(kz)] \cdot e^{j\omega t} \tag{2.7}$$

where the wave number is k is defined as

$$k = \frac{\omega}{v} = \frac{2\pi}{\lambda} \tag{2.8}$$

2.3.2 Types of Acoustic Waves

Acoustic waves in a solid are generally separated into bulk acoustic waves (BAW) and surface acoustic waves (SAW) [45]. Bulk waves consist of a series of alternating compressions and dilations traveling throughout the entire volume of a solid. Surface waves on the other hand comprise displacements primarily localized to the surface of the solid with minimal to no penetration into the volume of the structure. The figures below graphically illustrate the difference between bulk and and surface waves.

An example of a surface wave is the Rayleigh wave [46]. Here, particles at the surface move in an elliptic fashion in planes perpendicular of the surface and parallel to the direction of travel as shown in Figure 2.2. The particle displacement penetrates to a depth of about one wavelength.

Bulk waves (BAW) on the other hand, propagate throughout the volume of a solid material in contrast with the surface localization of SAWs. There are two general classes of bulk waves, namely longitudinal and shear or transverse waves. In a longitudinal wave, particle motion takes place in the direction of travel of the wave front (Figure 2.3).On the other hand, a shear or transverse wave comprises particle oscillations in a direction perpendicular to the direction of propagation of the wavefront as seen in Figure 2.4.

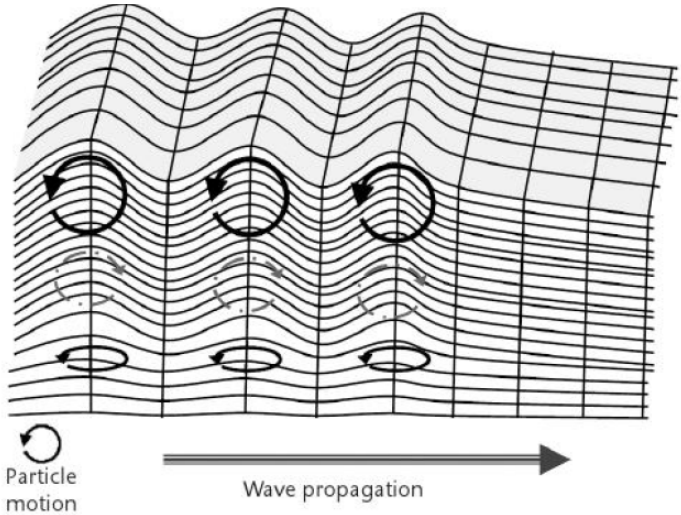


Figure 2.2: Rayleigh surface wave [46].

A practical acoustic device can incorporate any number of the above wave types, usually acoustic structures are usually engineered to favor certain propagation type. Each different wave type can setup standing waves and corresponding resonances at different frequencies, some of which maybe considered undesired or spurious for the target application.

2.3.3 Practical Considerations for Bulk and Surface Waves

Surface and bulk waves each provide a number of advantages and corresponding disadvantages. SAW devices are simpler in construction. Since acoustic waves propagation is confined to the surface, transduction electrodes are only required on one surface of the resonator structure. Furthermore, the thickness dimension of the resonator is of little concern since it plays no role in the acoustic propagation characteristics as long as it is more than one wavelength thick.

Bulk waves require more complex fabrication processes due to acoustic energy being stored across the volume of the structure. Transduction electrodes must usually

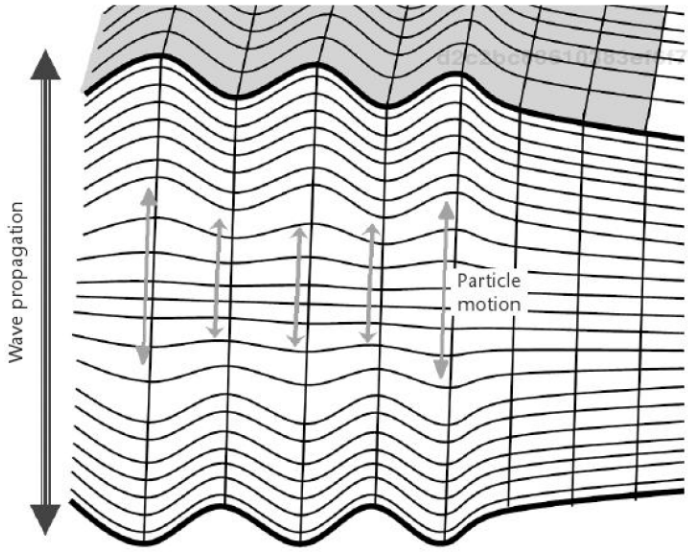


Figure 2.3: Longitudinal bulk wave [46].

be patterned on multiple surfaces of the resonant structure. In this case, the thickness of the structure must be properly controlled since it can impact the resonant frequency of the structure among other properties. Additionally, a BAW device must be acoustically decoupled from its carrier substrate to avoid energy leakage. The finite depth of acoustic wave penetration in SAWs avoids this problem

However, BAW devices exhibit a number of advantages compared with SAW devices. The distribution of acoustic energy across the volume enables BAW devices to handle higher power levels than their SAW counterparts. Secondly, BAW devices generally exhibit higher quality factors than SAW structures. Finally, BAW devices enable higher operation frequencies than their SAW counterparts and with smaller device size [13].

Historically, SAW devices emerged first due to their simpler technological complexity. However, since the early 2000s, BAW technology has matured rapidly and competes with SAW technology in several applications owing to its higher performance potential. In this work, the focus is mainly on bulk wave devices since they exhibit

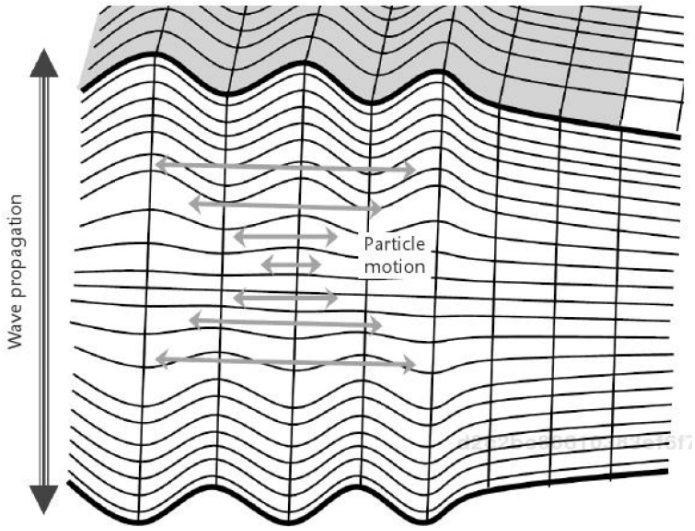


Figure 2.4: Shear acoustic wave [46].

more favorable properties for implementing high quality RF resonators [10, 12, 13].

2.4 Piezoelectric Effect

The previous discussion on acoustic wave propagation applies to any solid material supporting an acoustic vibration. However, a transduction mechanism is needed to provide the source for such acoustic displacements and subsequently provide a detection pathway. A frequently used transduction scheme used in many commercial devices relies on use of the piezoelectricity. As mentioned previously, piezoelectric transduction is usually preferred over other transduction schemes such as capacitive owing the much higher efficiency of piezoelectric transduction [31].

In a special class of materials lacking inversion symmetry i.e. the internal atomic structure is not symmetric about its central axis, electric fields and mechanical deformations become coupled. The lack of inversion symmetry implies that a compressive deformation of the piezoelectric material will lead to equal and opposite displacements of the positive and negative charge centers. As a result, a dipole and corresponding electric field are setup across the material compared with the normal case with no deformation. Applying tension to the material will setup a similar electric field of opposite polarity as shown in Figure 2.9. This is the essential principle of the piezoelectric effect.

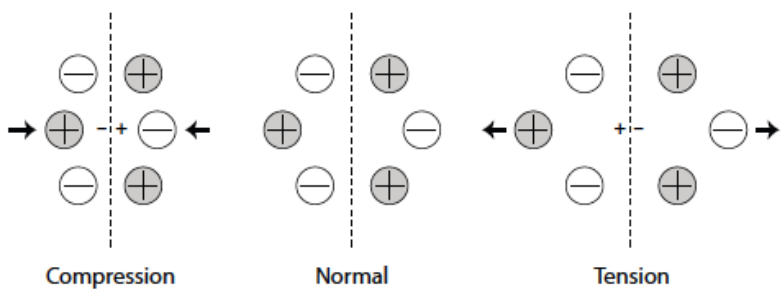


Figure 2.5: The piezoelectric effect [47].

Piezoelectricity also operates in the reverse fashion. Applying an electric field to a piezoelectric material will lead to a separation of the positive and negative charge

centers with an accompanying deformation dependent on the polarity of the applied field. This is referred to as the reverse piezoelectric effect shown in Figure 2.10.

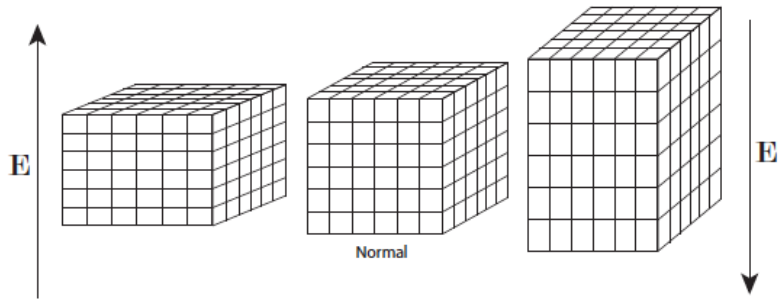


Figure 2.6: The inverse piezoelectric effect [47].

Piezoelectricity provides more efficient transduction, quantified as mechanical displacement in response to an applied electric field, than electrostatic transduction. This has lead to the dominance of piezoelectric acoustic resonators over their electrostatic counterparts.

2.5 Piezoelectric Resonator Operation

2.5.1 Electrical Modelling

Acoustic resonators and transducers are based on the propagation of acoustic waves through solid media. As such wave mechanics formalism are the natural starting point for anlaysis of such structures. However, in multi-layerd resonator structures (electrodes, piezo, bragg reflector, etc....), where electrical and mechanical fields are coupled through the piezoelectric effect, analytical solutions of the wave equation can be quite cumbersome to derive in all but a few special cases [48]. Furthermore, since the devices are typically used as electronic components, it is naturally desired to have a simple model with both electrical inputs and outputs which the designer can apply

without the complications of dealing with the mechanical domain. By leveraging the techniques of network theory, Mason [49], has developed an exact equivalent circuit that separates the piezoelectric materials into mechanical and electrical ports and acoustic ports through the use of an ideal "electro-mechanical transformer". The derivation presented here follows that in [13, 48, 50]

In a piezoelectric material, Hooke's law in eq.2.2 is modified to include transduction through the piezoelectric effect and inverse piezoelectric effect. This leads to the so-called piezoelectric constitutive relations below

$$T = cS - eE \tag{2.9}$$

$$D = eS + \epsilon E \tag{2.10}$$

where T is the stress, S corresponds to strain, e is the piezoelectric coefficient of the material under question, c the mechanical stiffness, ϵ the material permittivity and E is the electric field. This equation corresponds to Hooke's law. Now, the stress is T becomes:

$$T = c^E\left(1 + \frac{e^2}{c^E\epsilon^S}\right)S - \frac{e}{\epsilon^S}D = c^D S - \frac{e}{\epsilon^S}D \tag{2.11}$$

combining this result with eq.2.3 and eq.2.5, a wave equation is obtained with a new phase velocity given by

$$v^D = \sqrt{\frac{c^D}{\rho}} = \sqrt{\frac{c^E}{\rho}} \cdot \sqrt{1 + K^2} = v.\sqrt{1 + K^2} \tag{2.12}$$

the electromechanical coupling factor K^2 is given by

$$K^2 = \frac{e^2}{c^E\epsilon^S} \tag{2.13}$$

In the above analysis, the superscripts E and S denote the calculation of the material constants under constant electric field and strain respectively.

We now consider the case of an ideal FBAR which consists of a piezoelectric layer of thickness $2d = z_2 - z_1$ sandwiched between infinitesimally thin electrodes. The top face of the resonator is located at $z = z_1$ with the bottom face being located at $z = z_2$ Using eq.2.9 and eq.2.10 with the definition of strain in eq.2.4, the electric field is found to be

$$E = \frac{1}{\epsilon^S} \cdot D - \frac{e}{\epsilon^S} \cdot S = \frac{1}{\epsilon^S} \cdot D - \frac{e}{\epsilon^S} \cdot \frac{\partial u}{\partial z} \tag{2.14}$$

subsequently, the voltage across the piezoelectric layer is found to be

$$V = \int_{z_1}^{z_s} E(z)dz = \frac{2dD}{\epsilon^S} - \frac{e}{\epsilon^S}[u(z_1) - u(z_2)] \tag{2.15}$$

where $2d = z_2 - z_1$ corresponds to the thickness of the plate. Substituting $v = \frac{\partial u}{\partial t} = j\omega$ and noting that the current $I = j\omega A \cdot D$ the voltage takes the form

In an ideal piezoelectric, the only current conduction is through a displacement current given by $J = \frac{\partial D}{\partial t}$. The current through the resonator electrodes is computed as $I = j\omega A \cdot D$ where A is the area of the resonator. With this definition of current, the voltage becomes:

$$V = \frac{2d}{\epsilon^S} \cdot \frac{I}{j\omega A} + \frac{e}{j\omega\epsilon^S} \cdot [v(z_2) - v(z_1)] \tag{2.16}$$

and

$$I = j\omega C_o V + \frac{eC_0}{\epsilon^S}[v(z_2) - v(z_1)] \tag{2.17}$$

Now, the constants a and b in the expression for the particle displacement $u(z)$ in eq.2.7

$$a = \frac{1}{sin(2kd)} \cdot [u(z_2)cos(kz_1) - u(z_1)cos(kz_2)] \tag{2.18}$$

$$b = \frac{1}{sin(2kd)} \cdot [u(z_1)cos(kz_2) - u(z_2)cos(kz_1)] \tag{2.19}$$

The mechanical force at the resonator faces is computed as a product of the force and face area

$$F = -TA = -\left(c^D S - \frac{e}{\epsilon^S} D\right) \cdot A \tag{2.20}$$

inserting the expressions for a and b into the strain S equation, the force at the top face of the FBAR is found to be:

$$F_1 = \frac{kc^D A}{sin(2kd) \cdot [u(z_2) - u(z_1)]} - kc^D A \cdot tan(kd) \cdot u(z_1) + \frac{eD}{\epsilon^S} \cdot A \tag{2.21}$$

this can be further simplified by defining an acoustic impedance $kc^D = \omega Z$ combined with current and particle velocity expressions $I = j\omega A.D$ and $v = j\omega u$

$$F_1 = \frac{ZA}{jsin(2kd) \cdot [v(z_2) - v(z_1)]} + jZA \cdot tan(kd).v(z_1) + \frac{e}{j\omega\epsilon^S}.I \tag{2.22}$$

analogously, the force on the bottom face of the FBAR is found to be:

$$F_2 = \frac{ZA}{jsin(2kd) \cdot [v(z_2) - v(z_1)]} + jZA \cdot tan(kd).v(z_1) + \frac{e}{j\omega\epsilon^S}.I \tag{2.23}$$

By incorporating an ideal electromechanical transformer to model the piezoelectric transduction, Mason developed an equivalent circuit that satisfies the previous set of equations as shown in Figure 2.7.The mason equivalent consists of two acoustic ports corresponding to the two faces of the resonator which are described by force F and face velocity v and an electrical port with voltage V and current I. The electromechanical transformers couples the electrical and mechanical ports through the piezoelectric and inverse piezoelectric effect.

In the case of an ideal resonator, both ends are free with force $F = 0$. This corresponds to shorting of the acoustic ports. Shorting port 1 leads to the circuit in Figure 2.8.

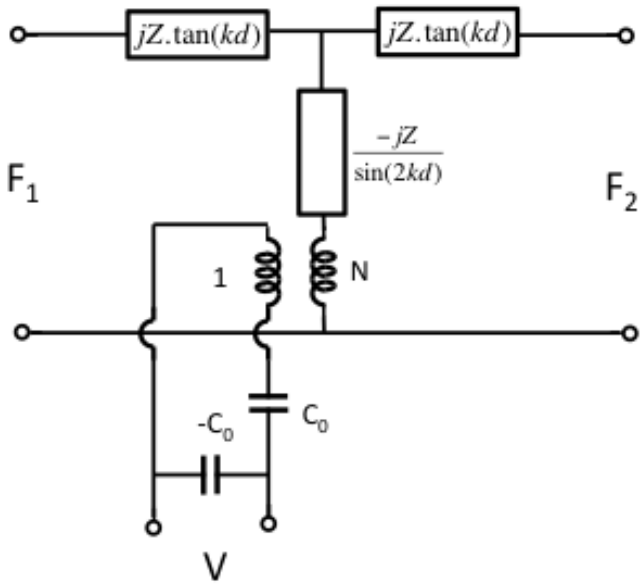


Figure 2.7: Mason model of piezoelectric layer.

By applying the simplification developed by Norton [50] (Figure 2.9, the previous circuit can be transformed to that of Figure 2.10

where

$$Z_a = \frac{Z_1(Z_1 + Z_2)}{Z_2}, \quad Z_b = Z_1 + Z_2, \quad N = \frac{Z_1 + Z_2}{Z_2} \tag{2.24}$$

this ultimately leads to the following circuit

Near resonance frequency $\omega_0 = \frac{\pi \cdot v}{d}$, the impedance $\frac{2Z_0}{jtan\frac{\pi}{2}\frac{\omega}{\omega_0}}$ in Figure 2.10 can be expanded as

$$\frac{2Z_0}{jtan\frac{\pi}{2}\frac{\omega}{\omega_0}} = \frac{2Z_0}{jtan\frac{\pi}{2}(1+\frac{\delta}{\omega_0})} = j_1 Z_0\left(\frac{\delta}{\omega_0} + \frac{\pi^2}{12}\frac{\delta^3}{\omega_0^3} + \dots\right) \tag{2.25}$$

comparing this with the impedance of a series L,C circuit expanded around its resonance frequency $\omega_0 = \sqrt{\frac{1}{LC}}$

$$Z = j\left(\omega L - \frac{1}{\omega C}\right) = \frac{2j}{\omega_0 C}\left(\frac{\delta}{\omega_0} + \frac{\delta^2}{2\omega^2}\right)\left(1 - \frac{\delta}{\omega_0} + \dots\right) \tag{2.26}$$

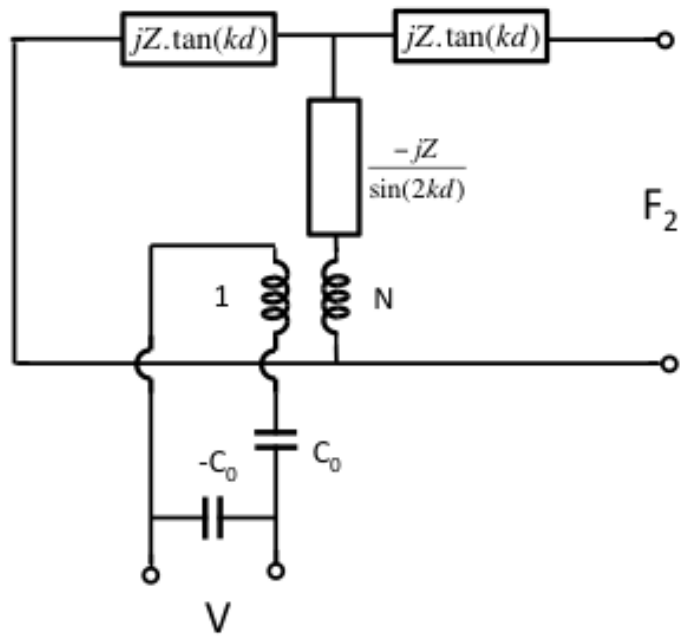


Figure 2.8: Shorting of acoustic port.

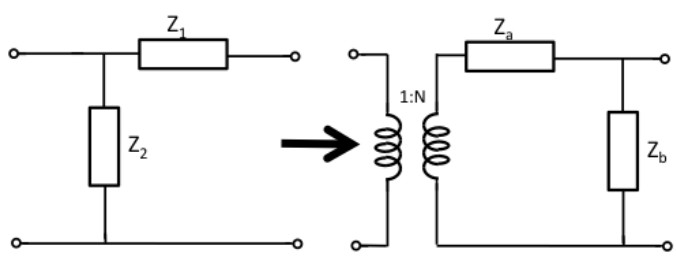


Figure 2.9: Norton transformation of previous circuit.

This leads to a a lumped circuit representation in Figure 2.11(a) where

$$C = \frac{2}{\pi \omega_0 Z} \tag{2.27}$$

$$L = \frac{1}{\omega_0^2 C_1} \tag{2.28}$$

By reflecting the LC elements across the mechanical transformer and adding a

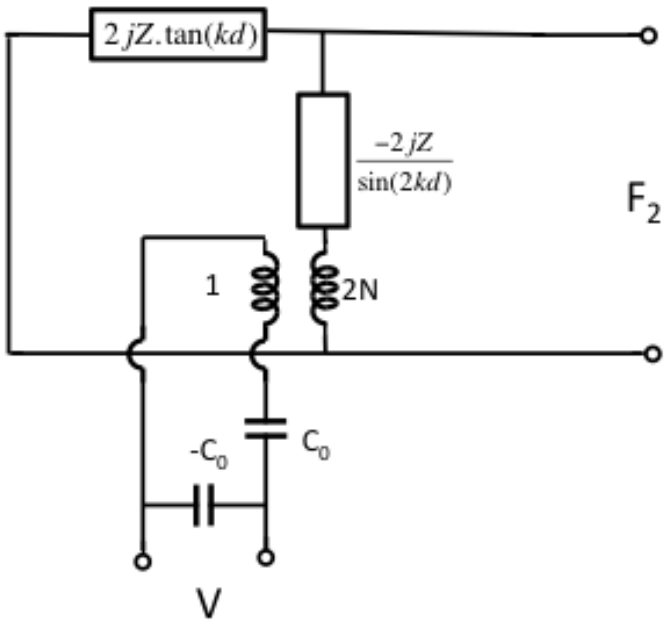


Figure 2.10: Simplified circuit after Norton transformation.

mechanical loss factor R_m, the circuit in Figure 2.11(b) is obtained

This is the essence of the Butterworth-Van Dyke model (BVD) [51–53]. The BVD model abstracts the mechanical aspects of the resonator and provides a simple, compact model that can be used for designing circuits operating near resonance.

2.5.2 Modified Butterworth Van-Dyke Model and Added Parasitics

The BVD model circuit is split into two main branches, the electrical and mechanical. The electrical branch consists of a "static" capacitor corresponding to the parallel-plate capacitance of the resonator as given by $C_0 = \frac{\epsilon A}{d}$. This is a purely electrical element with no transduction component. The motional branch consists of the *motional* components R_m, C_m, L_m which are a lumped electrical representation of the mechanical resonance behavior in the vicinity of the resonant frequency $\omega_0 = \frac{1}{L_m C_m}$.

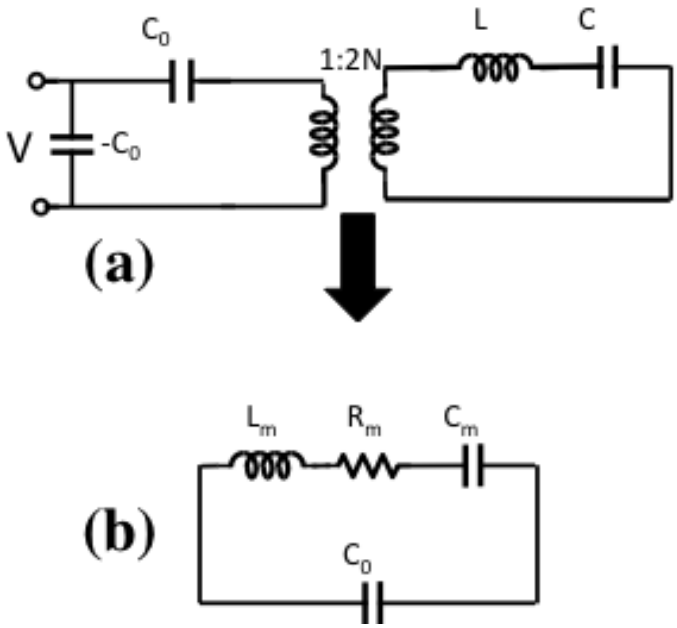


Figure 2.11: Reflecting mechanical elements across electromechanical transformer leads to the Butterworth-Van Dyke model.

The modified Butterowrth-Van Dyke model [54] incorporates an additional resistance in series with the parallel capacitance. This is found to improve the fitting of the BVD model to measured resonator responses. Additionally, the core BVD model only captures the intrinsic core of the resonator behavior. A practical resonator will incorporate additional parasitic elements due to the electrical resistance of the electrodes ,which presents itself as a series resistance contribution R_{series}, in addition to parasitic coupling capacitances to the substrate $C_{substrate}$).

The response of the core BVD model shows a pair of resonances, namely a series resonance ω_s corresponding to the resonance of the L_m and C_m and a higher frequencie parallel resonance ω_p due to the resonance of L_m and series combination of C_m and C_0. Series resonance presents a minimum of impedance whereas parallel resonance presents an impedance maximum. This is shown schematically in Figure 2.14

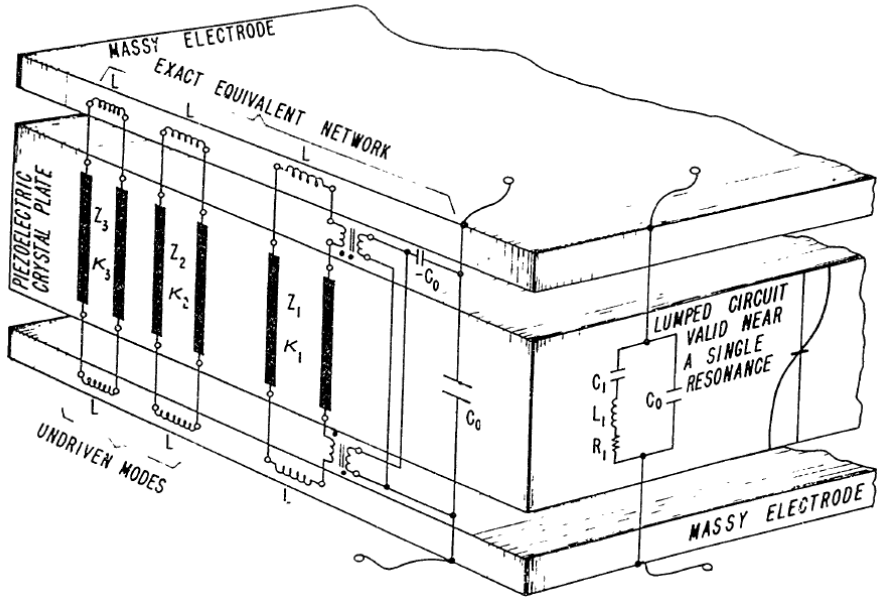


Figure 2.12: Exploded view of FBAR showing simplified BVD model around resonance and more general Mason model [48].

A widely used transduction parameter is what's known as the electromechanical coupling coefficient or k_t^2 which corresponds to the ratio of the electrical energy input into the structure to that of the mechanical energy that is output as a result of the specific transduction mechanism in question. The magnitude of k_t^2 [55] i.e. the transduction efficiency of the mechanical resonators is governed by the material properties of the resonant structure and the mechanical design of the structure. The transduction k_t^2 cannot exceed the material value k_{max}^2, but the overall device coupling coefficient can be and is almost invariably smaller than the material value due to a number of constraints imposed by the mechanical structure of the device. From [55], the electromechanical coupling can be computed from the spacing of the series resonance f_s and parallel resonance f_p frequencies as:

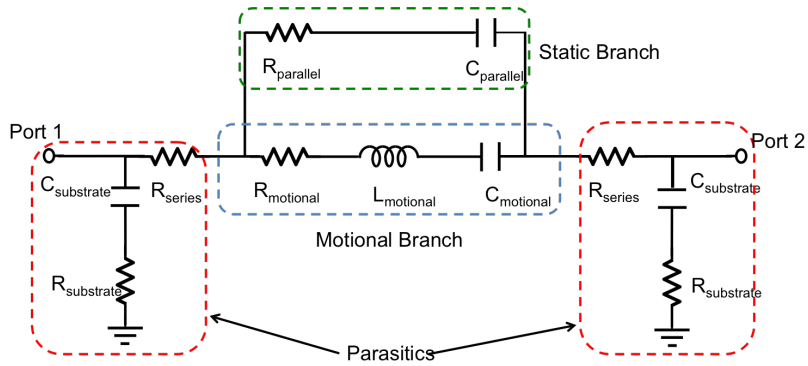


Figure 2.13: Modified Butterworth-Van Dyke Model (mBVD).

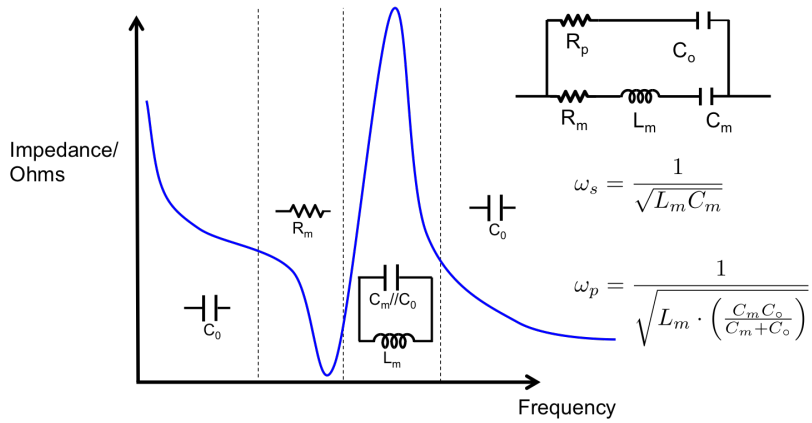
$$k_t^2 = \frac{\pi}{2} \frac{1}{\left[tan(\frac{\pi}{2} \frac{f_s}{f_p}) \right]} \tag{2.29}$$

The quality factor of the resonator, which quantifies it's loss properties, is computed as:

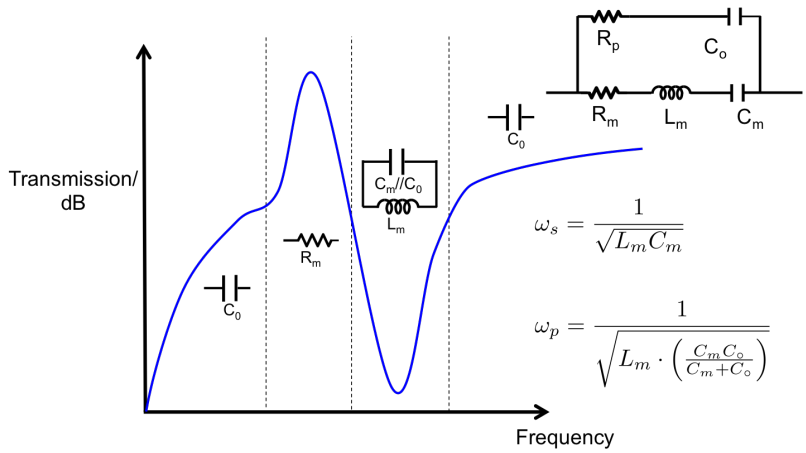
$$Q = \frac{w_r L_m}{R_m} \tag{2.30}$$

The motional resistance R_m is inversely proportional the k_t^2, Q and area A

$$R_m \propto \frac{1}{k_t^2 \times Q \times A} \tag{2.31}$$



(a)



(b)

Figure 2.14: Resonator BVD electrical response: (a) Impedance vs. frequency (b) Transmission response vs. frequency.

2.6 Vertical vs. Lateral Structures

Due to the anisotropy of piezoelectric materials, an electric excitation applied in a particular axis can trigger acoustic vibration in an orthogonal axis. The converse is also true where a deformation in one axis can generate an electric field in an orthogonal axis. Therefore, by appropriate placement of the actuating electrodes a variety of different vibration "modes" can be generated. The vibration modes can also be

tailored by adjusting the geometry of the piezoelectric layer. Shown in Figure 2.15 are a number of different acoustic modes. Here, the integers the X,Y,Z coordinate axes are designated the integers 1,2,3 respectively. The FBARs used in this work, use the longitudinal "33" mode where the electric excitation is applied in the vertical direction and the acoustic deformation takes place in the same direction. This structure was chosen for its simplicity and because it presents the highest k_t^2 of the different geometries. A lateral-extensional "31" mode exhibits lower k_t^2 values but allows for lateral definition of resonant frequency [13]. This is in contrast to the longitudinal mode where the frequency is determined by the vertical dimension or thickness of the piezoelectric layer. Therefore, lateral-extensional resonators can enable multiple frequencies using the same thickness of piezoelectric which is not possible with longitudinal resonators [56]. This is a significant advantage of lateral-extensional modes towards enabling frequency reconfigurable circuits [57]. The technological operations required to fabricate lateral and longitudinal mode devices are nearly identical, therefore the fabrication approaches that will be developed in this thesis for longitudinal FBARs can easily be applied to lateral devices in the future. Longitudinal FBARs were merely chosen in this work for their higher k_t^2 and consequently lower R_m values that simplify subsequent CMOS circuit design.

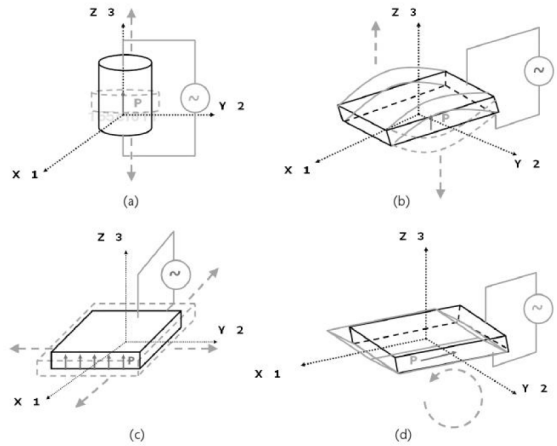


Figure 2.15: Excitation of different modes in piezoelectric resonators: (a) Longitudinal mode, (b) Flexural mode, (c) Thickness shear mode, (d) Lateral shear mode [46].

2.7 Acoustic Decoupling

The quality factor of an acoustic resonator is ultimately determined by material properties, which dictate the magnitude of internal losses and damping in the material, and by the various pathways of mechanical energy leakage from the resonator into the surrounding environment. In practice, the quality factor is almost invariably limited by the latter of the above two mechanisms. This follows intuitively from the definition of quality factor as the ratio of the energy retained to that lost by the structure where energy leakage corresponds to degradation in quality factor.

The primary energy leakage route is through the substrate on which the resonator is built. There are two key ways of eliminating energy leakage from a mechanical resonator, namely acoustic bragg reflectors and release/suspension of the resonant structure. In the case of released structures, the resonator comprises a membrane is suspended above an air cavity. This can be achieved through surface micromachinIng techniques whereby the resonator is built atop a thin sacrificial layer that is subsequently etched to release the structure of through the use of bulk microma-

chining techniques where the substrate itself is hollowed out to effectively release the resonant structure.

2.7.1 Membrane Isolation

The air cavity exhibits a large acoustic impedance mismatch to the materials in the resonant structure leading to a strong reflection of leaked energy back into the resonant structure. At low frequencies, there maybe some non-negligible coupling of energy from the resonator into the air cavity through squeeze damping which necessitates operation in vacuum [31]. However, piezoelectric resonators generally do not suffer any appreciable degree of squeeze damping since they do not relay on small gaps as in the case of electrostatically transduced resonators and squeeze damping does not contribute to energy loss.

Etching of the air cavity can be performed using wet or dry etching techniques. A key drawback of suspended structures is their mechanical fragility. Stress management is critical in the fabrication of such structures otherwise the membrane my warp and ultimately buckle leading to disintegration of the structure. This process is further complicated by the fact that the membrane is typically a heterogeneous stack of materials comprising the electrodes, piezoelectric layer and temperature compensation layers that all have different material properties and different stress profiles. Achieving zero or low stress in the structure can be quite challenging. In fact, achieving low stress membranes was one of the primary technical hurdles to the implementation of released FBAR technology [13]. The membranes are typically only a few 100nm to a few 100μm's thick, mechanical stresses during dicing, and subsequent fabrication operations can result in buckling and cracking of the membranes. Furthermore, the release etch is performed as the last step of the fabrication process, an appropriate release etch must be chosen which exhibits enough selectivity to the other materials in the resonator stack to prevent undesired etching. Recent work on the use of

xenon-difluoride (XeF_2) release etching has demonstrated promise towards addressing selectivity issues [58]. XeF_2 can be used for rapid etching of silicon ($10\mu m$ per min) with extremely high selectivity to most other materials.

2.7.2 Bragg Reflector Isolation

A mechanically robust acoustic decoupling alternative relies on the sue of acoustic bragg reflectors. In this incarnation, the resonator is built atop a stack of carefully selected materials whereby each layer is fully anchored to the substrate that is mechanically stable and robust [59], [60]. An acoustic mirror is the acoustic analog of the optical bragg reflector which is formed by the alternating layering of materials with high and low-acoustic impedance. If the acoustic impedance mismatch between layers is high enough and the layer thicknesses are selected appropriately, the acoustic mirror will behave has a very high impedance or very low impedance boundary (such as air) in a specific frequency bandwidth determined by the mirror design [61].

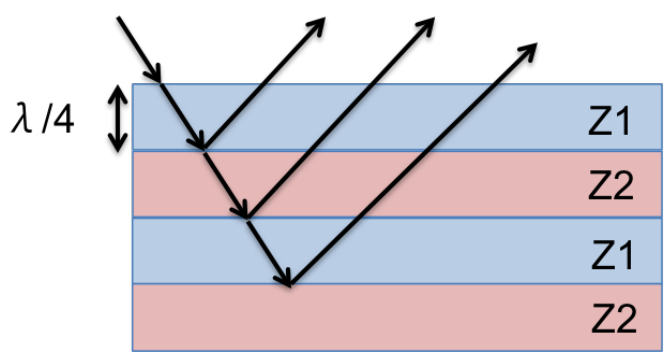


Figure 2.16: Bragg reflector operation.

The operation of a bragg reflector is based on the propagation and reflection of acoustic waves at the interface between dissimilar materials. Due to the underlying similarity between acoustic wave mechanics and transmission line theory, the structure can be modeled as a transmission line network [62]. Here, each layer is quantified

by a length (i.e. layer thickness) and characteristic impedance corresponding to the acoustic impedance of the material. Acoustic impedance is calculated as the product of material density and the velocity of sound in the material. As explained earlier, the Mason model allows for the modeling of acoustic layers as transmission lines. Therefore, the impedance of the bragg reflector can be calculated by cascading the impedances of the different layers where each layer presents an impedance determined by its length, characteristic impedance and neighboring layers [63] :

$$Z_{in} = Z_0 \left[\frac{Z_l cos(\beta l + j Z_0 sin(\beta l)}{Z_0 cos(\beta l) + j Z_l sin(\beta l)} \right] \tag{2.32}$$

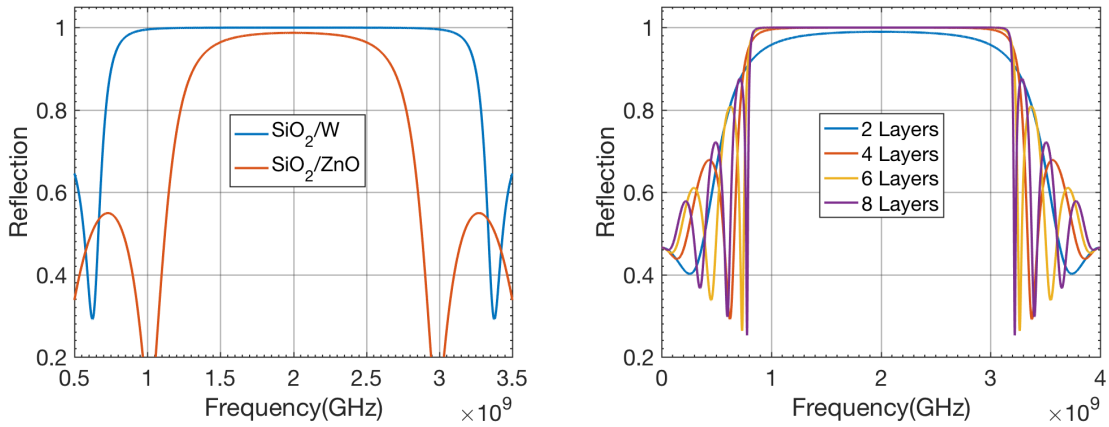
where l is the thickness or acoustic path length of the layer, $\beta = \frac{2\pi}{\lambda}$ is the propagation constant in the layer and Z_0 is the acoustic impedance of the layer.

Assuming thin electrodes, the product βl becomes small and the piezoelectric layer dominates the acoustic impedance of the resonator. Therefore, a reflection coefficient $\Gamma = \frac{Z_{mirror} - Z_{piezo}}{Z_{mirror} + Z_{piezo}}$ is observed looking into the mirror.

Using the above equations, the response of the bragg reflector can be computed. As shown in Figure 2.17 a higher acoustic-impedance mismatch between the alternating layers leads to a larger reflector bandwidth. Increasing the number of layer pairs leads to a higher reflection coefficient. With quality factor inversely proportional to energy loss $Q = \frac{1}{T}$ with T corresponding to the energy leakage through the resonator. Therefore, a reflection of 99 limits the maximum quality factor to 100. Consequently, a reflectance value greater than 99.99% is required to achieve quality factors greater than 100.

2.7.3 Bragg reflector construction and material selection

A practical bragg reflector should require a minimum number of layers to simplify fabrication. As discussed above, the reflectivity of a Bragg reflector id correlated with the acoustic impedance mismatch between the constituent layers of the reflector. Shown



(a) (b)

Figure 2.17: Bragg reflector dependence on number of layers and acoustic impedance mismatch: (a) Bragg reflector bandwidth increases with acoustic impedance mismatch (b) Reflectance magnitude increases with number of layers.

below (table.2.1) is a table of commonly used thin-film materials and their corresponding acoustic impedances [64]. It is generally observed that amorphous solids exhibit relatively low acoustic impedances whereas metal thin films exhibit higher acoustic impedances. This is generally to the higher density of metallic films and their tendency to crystallize at low temperatures. Consequently, a metallic thin film will be in a higher state of crystallinity or structural ordering than a dielectric film. Therefore, for this work Tungsten was chosen as the high acoustic impedance material and silicon dioxide as the low acoustic impedance material. Once notable exceptions are silicon-carbide (SiC) and silicon-oxycarbide (SiOC) [65, 66] which exhibit high and very low acoustic impedances. Silicon oxycarbide/Silicon nitride membranes have been previously demonstrated with high reflectivities. However, a fundamental issue with silicon oxycarbide is its high loss in the GHz range and the extreme sensitivity of its acoustic impedance to stoichiometry of the deposited film which limits their practical utility.

Material	Acoustic Impedance
	Z_α $[W/m^2/(m/s)^2]$
Zinc Oxide (ZnO)	34.5×10^6
Aluminum (Al)	36.0×10^6
Gold (Au)	17.3×10^6
Tungsten (W)	63.2×10^6
Silicon (Si)	106×10^6
Silicon (Si)	19.7×10^6
Silicon Oxide (SiO_2)	12.6×10^6
Silicon (Si)	25.7×10^6
Silicon Nitride (Si_3N_4)	3.6×10^6
Silicon Carbide (SiC)	38.92×10^6
Silicon Nitride (SiOC)	3.6×10^6

Table 2.1: Acoustic impedances of different materials.

Therefore, the decision was made to use W/SiO_2 mirrors despite the parasitics introduced by having metallic reflector layers. The following sections describe a specific reflector layout designed to reduce such parasitics.

2.8 Chapter Summary

In this chapter, the basics of acoustic wave propagation were outlined. This was followed a brief derivation of the Mason and Butterworth-Van Dyke electrical models for FBARs. The chapter concluded with a discussion of different vibration modes and methods for acoustic decoupling in FBARs.

Chapter 3

Fabrication of Stand Alone FBARs and Filters

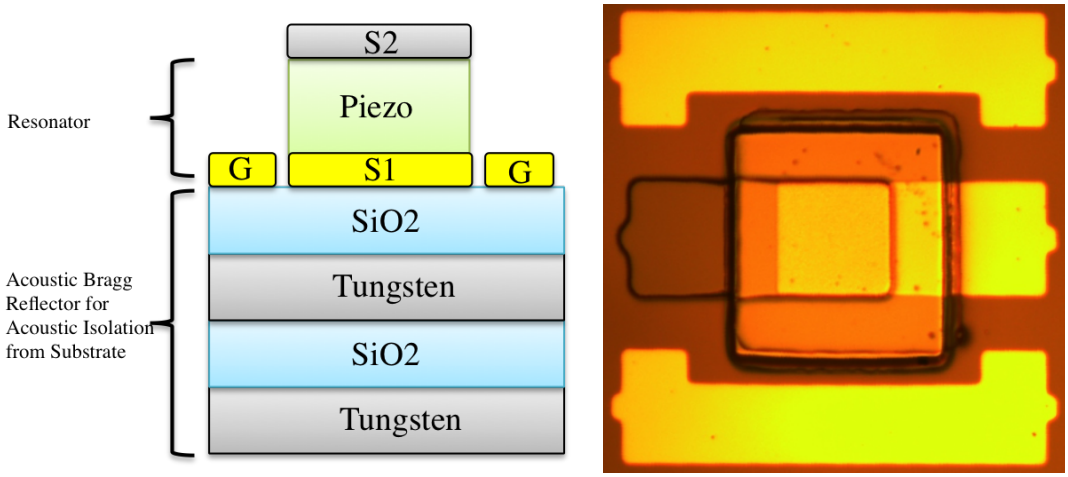
3.1 Introduction

In this chapter, the practical implementation of stand-alone FBAR resonators and filters on glass substrates is discussed. The discussion commences by outlining the utility of the BVD electrical model as a diagnostic tool for assessing and improving resonator performance. Following this, practical fabrication details of the resonators are presented. Finally, the chapter concludes with an overview of fabricated device progression and assessment of their application RF ftilers.

3.2 Fabricated FBAR Structure

The basic device used in this work is a Zinc-Oxide (ZnO) based FBAR built on a 4-layer W/SiO_2 bragg reflector shown in Figure 3.1. The thickness of the piezoelectric layer used in the different FBAR devices was chosen to provide devices operating between 1.5-1.8 GHz The electrodes are arranged in a two-port, 150μm pitch ground-

signal-ground layout compatible with RF coplanar probe measurement using a vector network analyzer (VNA). The VNA provides S-parameter measurements which are subsequently converted to admittance (Y) and impedance (Z) parameters that can be fit to the BVD lumped model.



(a) (b)

Figure 3.1: FBAR structure: (a) FBAR Device Layers (b) Microscope image of fabricated $100\mu m \times 100\mu m$ FBAR.

3.3 BVD Model as a Diagnostic Tool

In addition to its use in the eventual design of FBAR-CMOS circuits, the BVD model serves as an important diagnostic tool for characterizing FBAR performance and pinpointing of device fabrication defects. An FBAR and its corresponding bragg reflector comprise a complicated multi-layer structure. Material characterization techniques such XRD and sheet resistance measurements can not be used to assess the properties of the individual devices due to the small area of a completed device ($\sim 100\mu m \times 100\mu m$). Therefore, electrical measurement using a VNA is typically the only way to interrogate the properties of a completed FBAR device.

Shown below is a schematic mapping of the the FBAR structure to the different elements of the BVD model (Figure 3.2). As shown in (a), the motional elements (R_m, L_m, C_m) encompass the mechanical loss mechanisms such as leakage through the bragg reflector. The motional elements also factor in the efficiency of the transduction as quantified by the electromechanical coupling coefficient k_t^2. Parasitic capacitive coupling to the substrate typically occurs through the top layer of the bragg reflector and to the top-most tungsten layer. Excessive substrate capacitance can lead to an apparent reduction in resonator k_t^2 by "shunting" away a portion of the input signal to ground as opposed to being applied to the piezoelectric portion of the device. Fitting to the mBVD model can allow for decoupling this effect from a genuinely poor k_t^2 value. The same applies to de-embedding a high R_m value from excessive contact resistance in series with the resonator terminals as shown in (d).

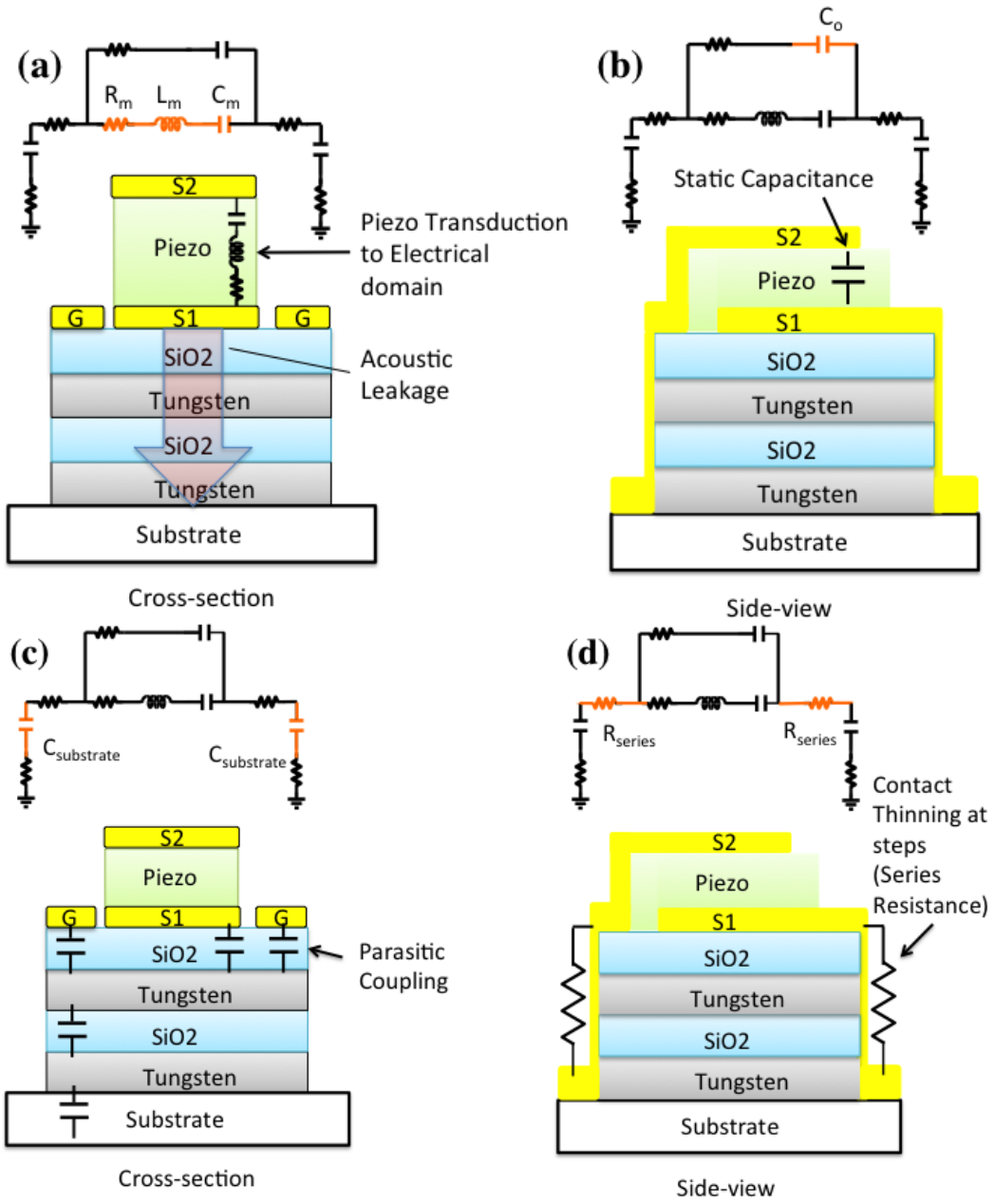


Figure 3.2: Mapping FBAR structure to BVD model elements: (a) Motional elements are primarily determined by piezoelectric layer and acoustic decoupling (b) Resonator static capacitance (c) Parasitic coupling to conductive mirror layers (d) Parasitics series resistance from electrodes.

3.4 Fabrication Basics

3.4.1 Lift-off Patterning of Device Layers

To pattern the different FBAR layers, ultra-violet (UV) contact lithography was used. In contact lithography, the sample is coated in a photosensitive compound known as photo-resist (PR). The resist is usually applied in liquid form and then baked to form a solid layer. The photoresist is exposed to UV illumination through a patterned chromium on glass photomask. Due to chromium's opacity to UV light, the photoresist is exposed in the mask pattern. Exposure results in a chemical reaction which structurally weakens the exposed photoresist rendering the resist much more soluble in a special developer solution than the non-exposed resist. This pattern can then be transferred to an underlying substrate in subtractive fashion (etching) where the resist serves as mask for etching away the substrate, *or* in additive fashion where the mask serves as a stencil for selective deposition on the substrate (lift-off) [39]. For most layers in the FBAR, lift-off was the patterning method of choice. Lift-off is useful for depositing layers which are difficult to etch. This maybe due to to poor etching selectivity where the etchant equally etches the desired material to be patterned as well as other materials in the structure. A special bi-layer lift-off technique was used to ensure proper patterning. In this scheme, a lift-off resist (LOR) is first applied to the sample followed by a coating of photoresist. The structure is then exposed and developed to yield the desired pattern. However, the LOR is designed to etch faster in developer than the photoresist. Consequently, an overhang or undercut will form with a resist "shelf" protruding beyond the edges of the LOR. During deposition, the resist shelf prevents deposited material on the resist from bridging with that deposited on the substrate. The resist and LOR are then removed in a solvent solution leading thereby "lifting-off" the undesired material and leaving material in the desired pattern on the substrate. The LOR undercut can be optimized by carefully controlling the

develop and bake times. Improper undercut, or collapse of the shelf can lead to the bridging of the deposited film on the resist and substrate leading to poor lift-off and the formation of "wings" or sharp edges where the deposited film tears following lift-off. Figure 3.3 depicts the operation of the bi-layer lift-off process on a glass substrate.

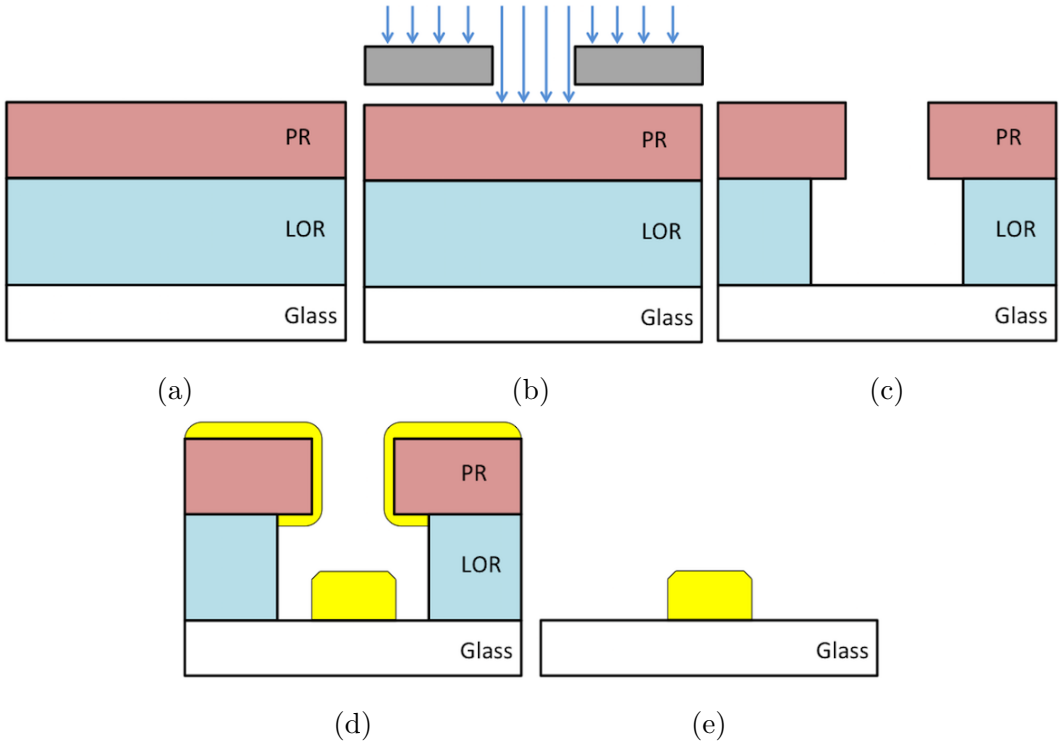


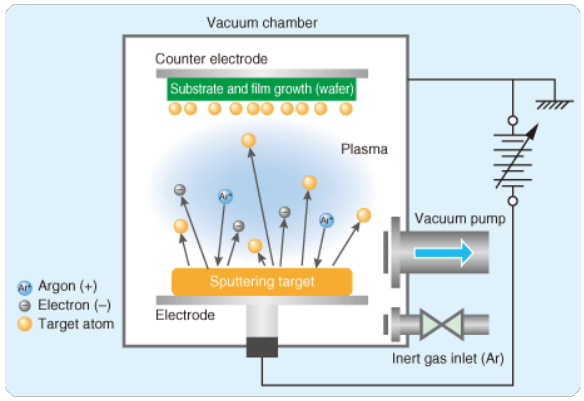
Figure 3.3: LOR lift-off process: (a) Spinning photoresist and LOR on substrate (b) UV exposure through photomask (c) Developing and LOR undercut (d) Material deposition (e) Clean lift-off following resist stripping.

In some cases, such as high-temperature deposition, lift-off can be problematic and etching maybe a more appropriate solution as will be discussed on the section on tungsten deposition.

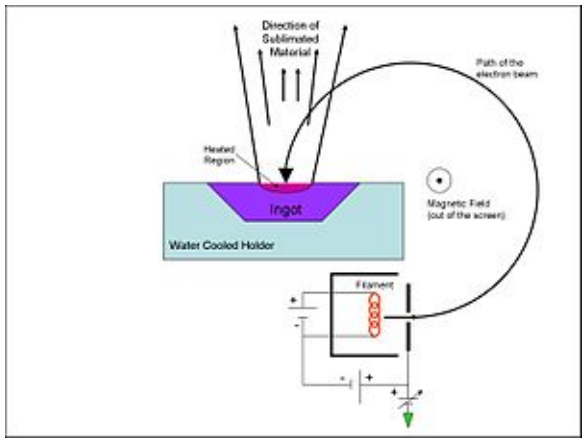
3.4.2 Thin-film Deposition

For depositing the the constituent thin-film layers of the FBAR structure, two techniques were used: RF magnetron sputtering and e-beam evaporation. In sputtering, a radio-frequency (RF) plasma is generated in a low pressure gas such as argon. As shown in Figure 3.4, ionized argon ions in the plasma are accelerated by the RF field and collide with a target made of the desired deposition materials and eject atoms from the target. These atoms then re-deposit on the substrate surface and grow into a thin-film. Argon is utilized due to its large mass which allows for easier ejection of target atoms by momentum transfer. Additional gases such as oxygen can also be flown into the sputtering chamber to compensate for any stoichiometric deficiencies arising when the target consists of multi-element compound (such as zinc-oxide) where the constituent elements sputter at different rates [67]. Sputtering is typically used for growing thick films and in cases where the target materials with high melting temperatures that are difficult to practically melt. Sputtering was used for depositing all the FBAR layers with the exception of the gold electrodes.

The gold electrodes were deposited using e-beam evaporation. Here, a beam of electrons is directed, using magnetic fields, into a crucible containing the desired deposition material. The energy from the electron beam melts the crucible which is then vaporized and travels towards the substrate. The material condenses to form a solid film. E-beam evaporation is schematically depicted in Figure 3.4.



(a)



(b)

Figure 3.4: Thin-film deposition methods: (a) RF sputtering (b) E-beam evaporation.

3.5 Bragg Reflector

As described before, a tungsten (W) and silicon dioxide (SiO_2) bragg reflector was chosen due to the high acoustic impedance mismatch of the two materials which provides a large reflector bandwidth and high reflectivity with a minimum number of layers. The SiO_2 is the low-acoustic impedance material with the W as the high-acoustic impedance material. Both layers were deposited using RF-magnetron sputtering in a pure argon plasma. The layer thicknesses of the reflector layers were selected to target

Material	RF Power[Watts]	Argon Pressure[mTorr]	Thickness[nm]	Deposition Rate[Å\s]
W	150	2	650	1.5
SiO_2	200	10	680	1

Table 3.1: Acoustic bragg reflector layer thicknesses and deposition conditions.

a reflector center frequency of 1GHz. Shown in table.3.1 are the layer thicknesses and the deposition conditions for each layer.

In depositing the bragg reflector layers, the W layer presented a number of challenges due to its physical properties. The optimization of W deposition is discussed in the next section.

3.5.1 Tungsten Deposition

A key challenge in the development of the resonator fabrication process was controlling the stress in the sputter-deposited tungsten layers of the acoustic bragg reflector. As discussed before, the use of Tungsten was chosen due to its very large acoustic impedance mismatch with SiO_2. In this work, tungsten is deposited via sputtering whereby an energetic plasma of argon ions ejects material from a tungsten target which later condenses and deposits on a substrate placed some distance from the target [67]. Due to the high energy imparted to sputtered tungsten atoms, sputter deposited tungsten is deposited in a crystalline form where the atoms arrange into in an orderly fashion over a long-range. A region of ordered atoms is referred to as a "grain" or crystallite [68].

Sputtered tungsten deposits in two key crystal structures, namely body-centered-cubic structure (BCC) designated alpha (α), and the A15 crystal structure referred to as beta (β). The alpha is a body-centered cubic structure with dense columnar growth. On the other hand, the beta is an A15 crystal structure with loose packing of

grains and exhibits lower density than the alpha phase. As mentioned above, acoustic impedance is a product of the sounds velocity and density of a material, therefore the alpha phase is preferred for bragg reflector fabrication where the higher tungsten film density corresponds to a higher acoustic impedance and thus a higher acoustic impedance mismatch between the bragg reflector layers. Furthermore, the beta phase structure is thermodynamically unstable and spontaneously transforms into alpha phase even at room temperature. The process is accelerated by the addition of higher than ambient temperatures [69, 70].

The relative ratio of alpha and beta phase crystallites in a tungsten film is strongly influenced by the temperature and pressure at which the sputtering takes place. Several works have observed the predominance of alpha phase tungsten at lower pressures ($< 5mTorr$) with the proportion of beta-phase crystallites increasing at higher pressures ($> 10mTorr$). XRD measurements of tungsten films deposited at different pressures (Figure 3.6) show stronger A15 peaks with increasing sputtering pressure with a corresponding reduction in the beta peak strength .

However, lower pressure deposition yields highly compressive tungsten films. Large values of stress in the tungsten films can lead to cracking and delamination of the deposited tungsten films [72]. Therefore a trade-off must be achieved between attaining high-density alpha tungsten for high quality factor and managing stress in the deposited films. It is also desired that the film be comprised predominantly of alpha crystallites since the spontaneous transformation of beta phase crystallites to the alpha phase can lead to significant cracking as the crystallites change structure within a fixed volume.

The deposition of tungsten is further complicated by the fact that lift-off has been employed in the patterning of the tungsten layers. Photoresists used in this process typically cannot tolerate temperatures higher than 120°C without reflow/deformation and charring. Reflow becomes critical with liftoff processes, since the resist shelf is

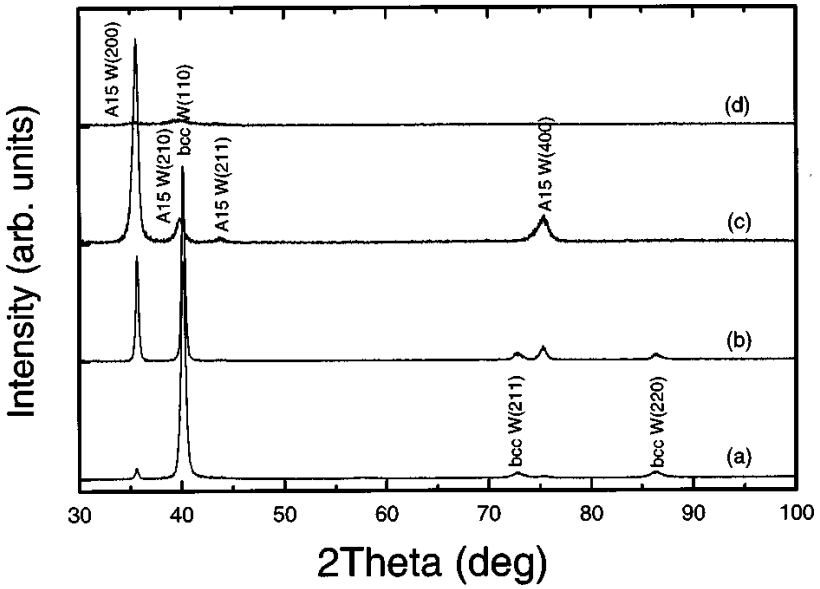


Figure 3.5: Sputtered tungsten XRD scans at (a) 3mTorr (b) 12mTorr (c) 26mTorr (d) 60mTorr [71].

specifically engineered to prevent bridging of the growing film with deposits on the resist surface. Shelf-collapse (3.7) due to high temperatures and excessive stress in the deposited film leads to film bridging and consequent tearing of the film resulting rough edges that contribute to shorting and faulty contact between the top and bottom of the film. The problem is exacerbated by the need for thick films (up to $0.68\mu m$ per single deposition). Figure3.8 shows shorting of the tungsten layers of a reflector with tungsten layers deposited at high temperature.

In order to reduce the warping of the resist and potential electrode shorting, a lower power deposition was utilized. Whereas the lower power reduced deposition temperature and had the effect of eliminating shorting across the mirror. However, pristinely deposited low-power mirrors rapidly cracked and shattered within a few hours at room temperature (Figure 3.9) likely due to the transformation of alpha crystallites into the beta-form.

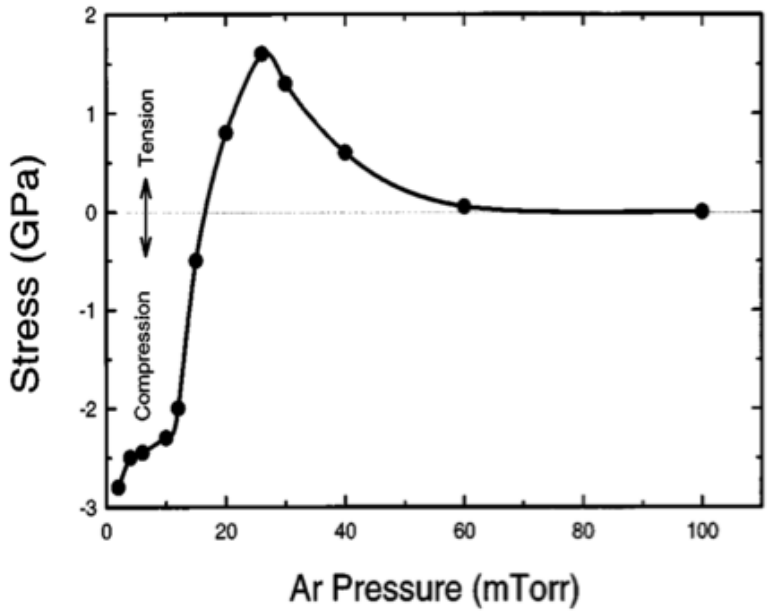
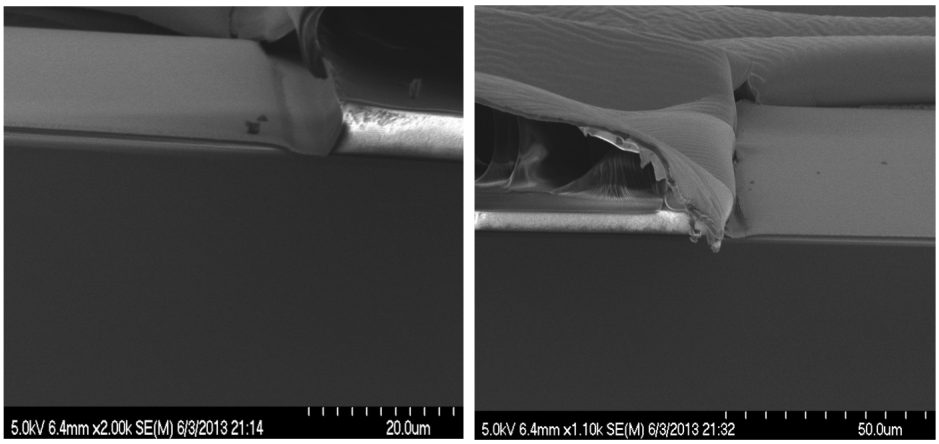


Figure 3.6: Tungsten stress as a function of sputtering pressure [71].



(a) (b)

Figure 3.7: Tungsten lift-off: (a) Warping of resist shelf (b) Collapse of resist shelf.

To ultimately achieve stable, low-stress a mirrors a scheme of alternating low-pressure and high-pressure tungsten depositions [73]. Shown below in Figure 3.10.

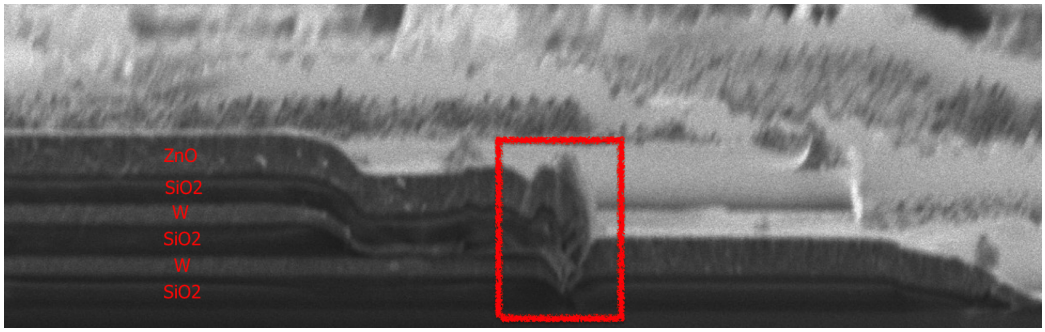
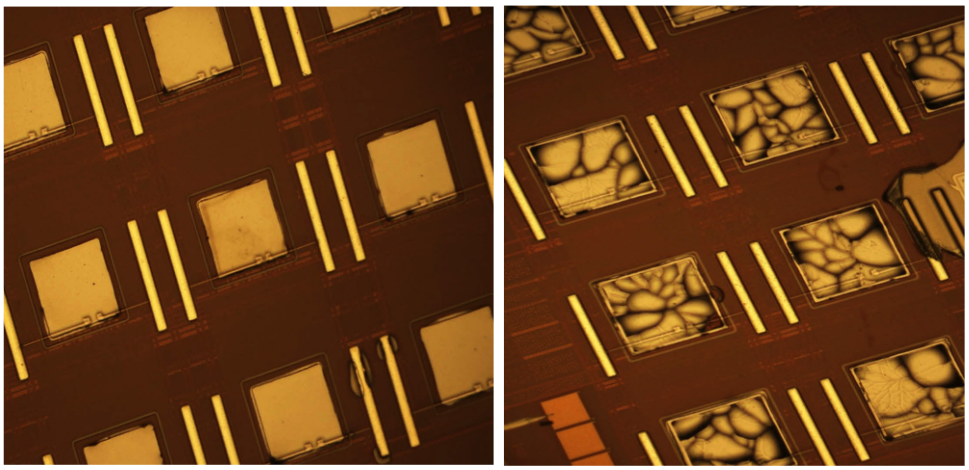


Figure 3.8: Shorting of tungsten mirror layers deposited at high temperature.

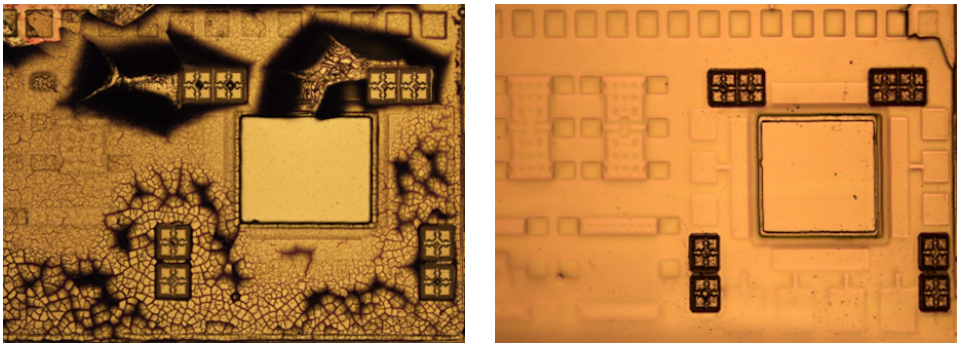


(a) (b)

Figure 3.9: Mirror Cracking due to Transformation from Beta to Alpha Tungsten: (a) Uncracked, as-deposited mirrors (b) Mirror cracking.

3.5.2 Etch Based Patterning

In parallel with the development of lift-off based mirrors, dry etching was explored as an alternative for mirror patterning. As shown in this case, an etch-based approach would involve depositing all the mirror layers in blanket fashion and then deposit a patterned, metallic hard mask to pattern the blanket layers into the desired pattern. Finally, the patterned mirror would be blanketed with an SiO_2 layer that serves as



(a) (b)

Figure 3.10: Optimization of sputtered tungsten stress: (a) Single pressure tungsten Deposition (b) NCL deposited tungsten.

the topmost mirror layer and prevents shorting between mirror layers. The blanket deposition approach would not suffer the temperature limitations of the lift-off approach which is limited by resist reflow and warping. Furthermore, processing is simplified since only to patterning steps are required, namely the patterning of the hardmask followed by dry etching and the patterning and deposition of the blanket SiO_2 layer. The goal was to attain and etch recipe that was isotropic in nature leading to a tapered or mesa profile that can ease electrical contact between layers at the top and at the base of the mirror.

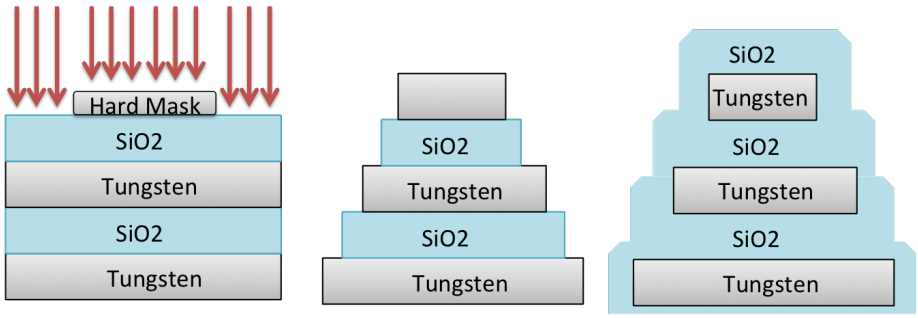


Figure 3.11: FBAR mirror etching.

Fluorine based plasmas have previously been reported for etching of the constituent materials of the of the reflector (chromium, tungsten and silicon Dioxide). Pan et. al Have studied both CHF_3/O_2 and SF_6/O_2 plasmas for etching of tungsten and SiO_2 [74]. A CHF_3/O_2 plasma was chosen in this work since it demonstrates comparable etch rates for both W and SiO_2. One concern with etching of the mirror layers is differential under-cutting whereby a layer etches faster than the layer right above it. This leads to staggered protrusions that can prevent good electrical contact across the sides of the mirror. Shown in Figure 3.12 is noticeable differential undercutting when etching at 60mTorr. Significant protrusions of the SIO_2 layers are observed.

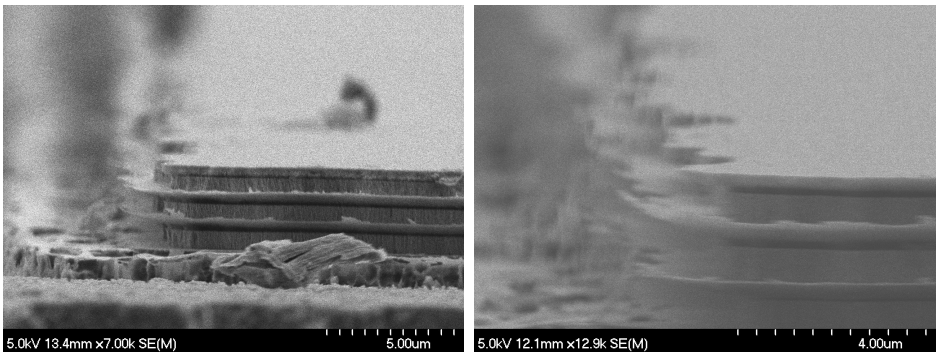


Figure 3.12: Staggered protrusions due to differential undercutting at 60mTorr pressure.

In order to minimize differential undercutting, the etching parameters were optimized based on the findings in [74] to decrease the etch rate of SIO_2 relative to W. Indeed, adjusting the gas pressure to 20mTorr led to a much improved profile as shown in Figure 3.13

With appropriately patterned mirrors, the etching technique was applied to fabrication of FBAR devices. Initial devices fabricated using etched-mirrors exhibited very poor resonant characteristics. Upon closer optical inspection of the etched mirrors, pitting was observed in the mirror structures. This was believed to be due to

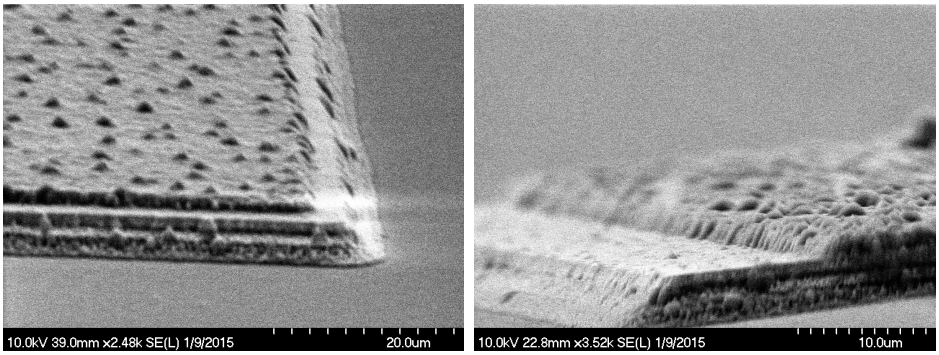


Figure 3.13: Mirror etching profile at 20mTorr etching pressure.

increased stress in the blanket deposited mirror layers. Whereas the lift-off patterned mirrors showed no pitting, the much larger area of the blanket mirrors leads to an aggregation of stress across the sample area leading to increased stress values. In order to relieve the large stress, the film will typically buckle or delaminate at the points of maximum stress concentration. This is especially the case with materials such Tugnsten that possess a high Young's modulus or stiffness [75]. It was believed that the stress-induced delamination lead to high surface roughness which in turn reduced the quality of the ZnO piezoelectric film. This was observed as low k_t^2 values less than 1%

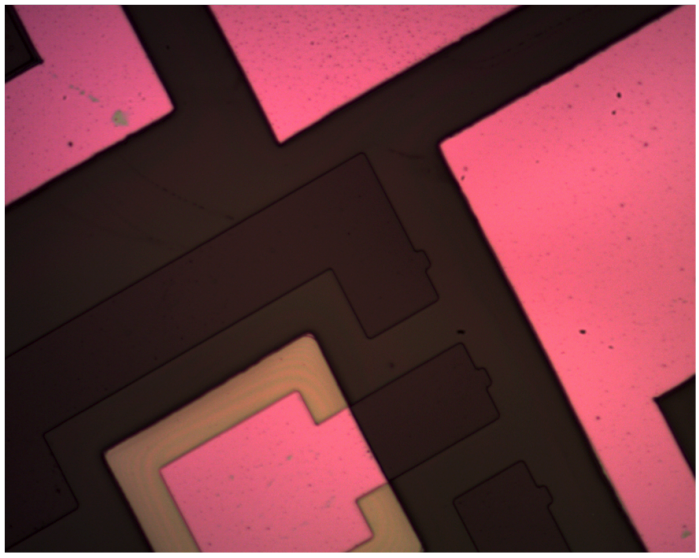


Figure 3.14: Stress-induced mirror pitting.

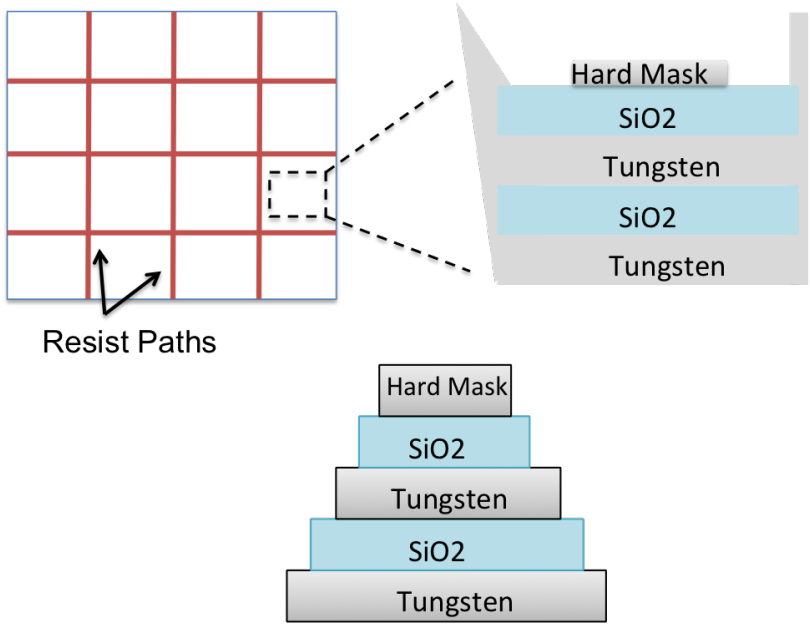
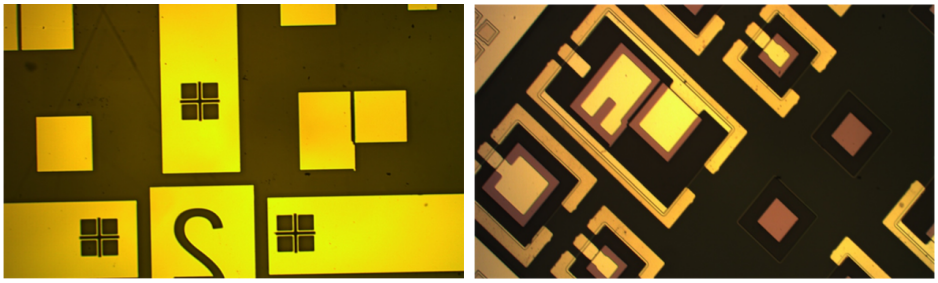


Figure 3.15: Mirror pre-patterning process.



(a) (b)

Figure 3.16: Optimized etched mirrors: (a) Blank etched mirrors before contact deposition (b) Etched mirrors with piezo and contacts deposited.

3.6 Piezoelectric layer growth

The piezoelectric layer is the core of the FBAR. A high-quality piezoelectric layer is crucial to attaining efficient transduction (high k_t^2) and high quality factor (Q). A number of piezoelectric materials have historically been used. Quartz has long been used in crystal oscillators and exhibits high material quality factors ($\sim 10,000$), however it is grown in cylinders or bools and is difficult to grow on an a foreign substrate such as glass or a CMOS die. Lead-Zirconium-Titanate (PZT), is also a frequently used piezoelectric material with large k_t^2 up to 50%, however it exhibits very high losses at RF frequencies and is difficult to deposit at low temperatures compatible with CMOS processing ($< 300C$). Consequently, thin-film piezoelectric materials such as Zinc-Oxide(ZnO) and Aluminum-Nitride(AlN) have gained significant popularity for FBAR fabrication. Both these materials can be deposited in thin films ($\sim 1 - 5\mu$ m) for operation in the RF frequency range. Furthermore, they can be deposited at CMOS compatible temperatures [13]. Both materials are usually deposited by RF sputtering.

In this work, ZnO was the chosen piezoelectric material due its availability. In order to achieve high k_t^2, the ZnO should be grown in a crystalline well-oriented

fashion [76]. ZnO crystallinity is strongly dependent on the deposition conditions such as the sputtering pressure, the gas environment during sputtering, substrate, and the substrate material on which the ZnO film is deposited [77]. The film was grown on 75 nm gold (Au) electrodes, which are in turn grown on a 20 nm titanium (Ti) layer. Au/Ti electrodes have been observed to promote the crystallinity of ZnO significantly in comparison with other materials [78]. A number of experiments were performed to obtain the optimal ZnO growth conditions. In order to assess film quality, XRD measurements were used to measure the strength of the 34.2°peak which corresponds to the piezoelectric crystal orientation (002) of ZnO. Substrate heating was also observed to significantly improve ZnO crystallinity. Substrate temperature during deposition was limited to 150°C to avoid degradation of photoresists used for lift-off patterning. Shown in Figure 3.17 is the improvement in ZnO peak strength with substrate heating to 150°C. The highest crystallinity (as quantified by XRD peak strength) was obtained for sputtering at 2 mTorr pressure, in an argon/oxygen environment (90%/10%) and at a power of 200 W applied to a 4inch ceramic ZnO target. Both tungsten and gold/titanium and tungsten electrodes were tested and the gold/titanium combination yielded the better results

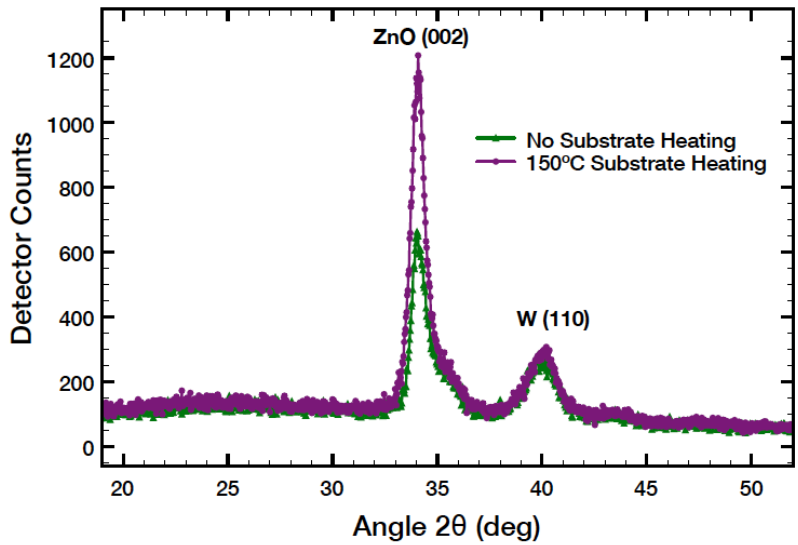
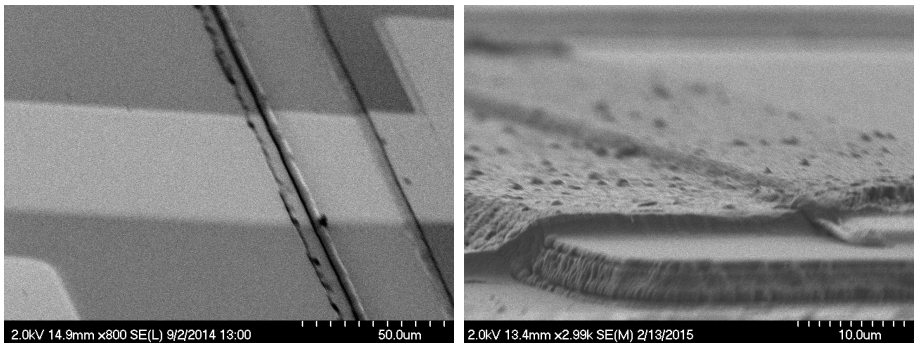


Figure 3.17: XRD measurement of ZnO on W with and without substrate heating at 150°C.

3.7 FBAR Resonator Results

The fabrication of FBAR devices went through a number of iterations with different structural optimizations performed at different device generations. Initially, the FBARs were built on blanket acoustic reflectors (Gen1) which lead to large substrate parasitics. To address the capacitive parasitics, Gen2 devices were fabricated on patterned acoustic reflectors where the reflector is present only beneath the FBAR signal electrodes and not the ground electrodes. Indeed, the capacitive parasitics were reduced, however the patterned mirror lead to an increase in series resistance. This is likely due to thinning of the gold electrodes (75 nm thick) as they climb the sides of the reflector which is $\sim 3\mu$m in thickness. All devices fabricated so far were build on silicon wafers with a 300 nm thick SiO_2 layer. Migration to insulating glass substrates lead to further reduction in capacitive parasitics (Gen3). Adopting a staggered or pyramidal geometry and adding thick aluminum contact extensions ($\sim 2\mu$m) led a

significant reduction in contact resistance (Gen4). The thick contact extensions are demonstrated in Figure 3.18. Devices with etched mirrors exhibited similar performance with the exception of increased contact resistance. Further optimization of the mirror etching profile to reduce contact resistance will be an item of future work. Figure 3.19 graphically demosntrates the evolution of the FBAR structure from Gen1 to Gen4. Figure 3.20 shows the corresponding improvement in measured S-parameters.



(a) (b)

Figure 3.18: Improving FBAR contact resistance: (a) No contact extension (b) Thick aluminum contact extension.

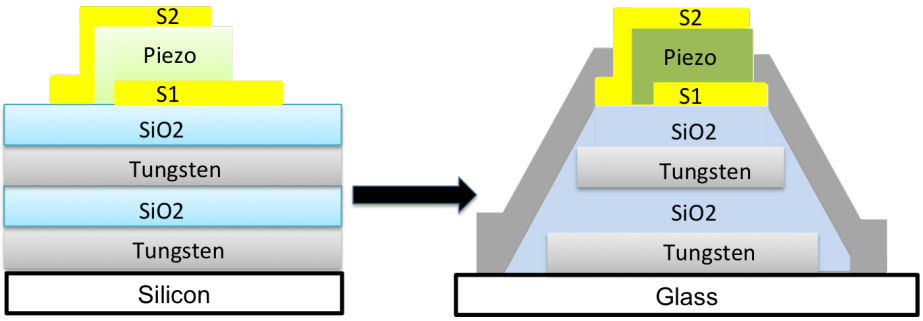


Figure 3.19: FBAR structure evolution: (a) Initial FBAR on blanket mirror (b) Pyramidal mirror with contact extensions and improved piezoelectric layer.

	Gen1	Gen2	Gen3	Gen4	Gen5
Q	~ 350	~ 400	~ 700	~ 500	~ 500
k_t^2	1%	3.1%	3.5%	4.5%	4.5%
$R_s(\Omega)$	1	6	4	0.3	5
$C_{sub}(fF)$	3000	700	10	10	10
R_m	400	15	5	5	5.3
Process	Blanket mirrors	Patterned mirrors and improved piezo growth	Insulating substrate	Pyramidal mirror and thick contact extension	Etched Mirror

Table 3.2: FBAR performance progression.

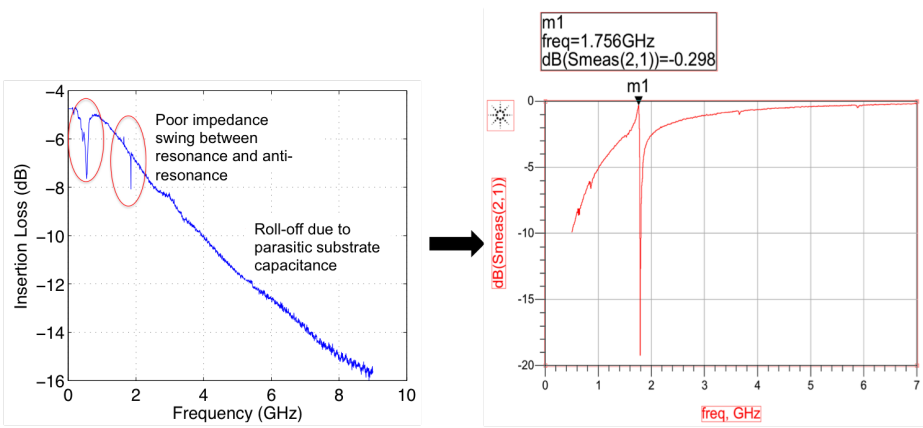


Figure 3.20: Performance evolution of 100μ m $\times$100μ m FBAR.

3.8 FBAR Filters

With working resonators now available, experiments were performed to assess their applicability to filters. A large number of filter topologies have been developed for use with acoustic and non-acoustic resonators by interconnecting the resonators into a

coupled resonator system with a filter transfer function. The inter-resonator coupling can be performed mechanically or electrically. Mechanical coupling exhibits much higher coupling enabling filter bandwidths well in excess of the resonator k_t^2 separation, however mechanical coupling is challenging due the generation of spurious modes. Acoustic resonators generally exhibit multiple degrees of freedom, each with their corresponding resonant frequency, depending on how they have been anchored to the substrate. In a mechanically coupled filter, the different modes can couple to produce spurs at undesired frequencies. Therefore, despite the lower coupling factor, and subsequently lower bandwidths, electrical coupling schemes are the more commonly used ones in GHz, commercial, high-performance acoustic resonators. As such, filters in this work were restricted to electrically coupled topologies.

The ladder and lattice structures are the most frequently used electrically coupled FBAR filter topologies. Shown in Figure 3.21 the schematics of the ladder and lattice filter structures.

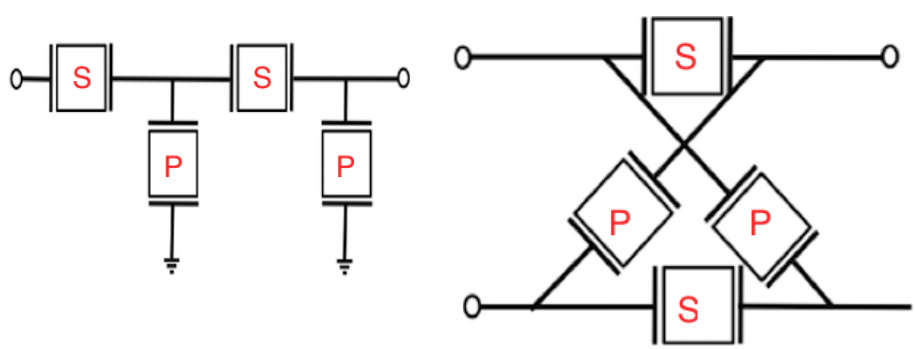


Figure 3.21: Resonator-based filter structures: (a) Ladder filter structure (b) Lattice filter structure.

Ladder filters are composed of "sections" consisting of a series resonator of resonant frequency f_s and a shunt resonator of resonant frequency f_p which slightly lower than f_s. The operation of a ladder filter is described below in Figure 3.22.

At low frequencies, far from both fp and fs, both resonators appear mainly capac-

itive yielding a capacitive voltage divider. The ratio of the capacitances (i.e. areas) of both resonators determined the passive gain of the divider and consequently the out-of-band insertion loss.

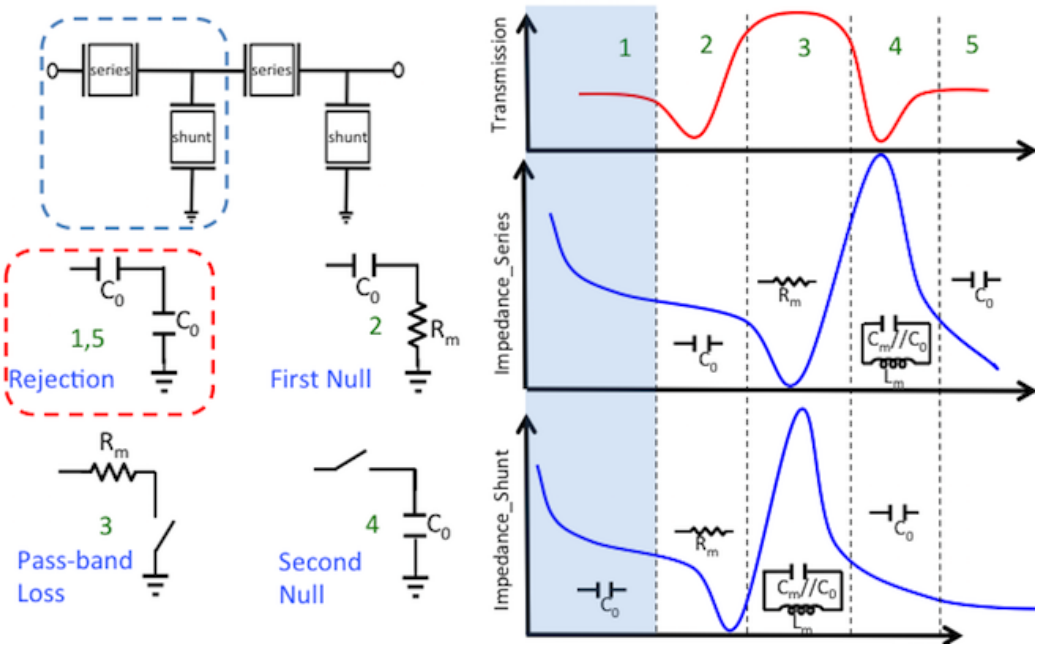


Figure 3.22: Ladder filter operation out-of-band.

Around f_p, the shunt resonator goes into its series resonance and presents a low-impedance equal to R_m between its terminals. As a result, the input of the filter is "shunted" to ground through the low-impedance path provided by R_m, leading to a sharp notch in the filter response.

At a slightly higher frequency, the shunt resonator enters its parallel resonance while the series resonance is in series resonance. The much larger impedance of the shunt path through the shunt resonator results in increased transmission between the input and output terminals of the filter. This region forms the filter pass-band

Further up in frequency, the shunt resonator has returned to its capacitive regime away from resonance and the series resonator is in anti-resonance leading to transmission zero between the filter terminals which appears as a second notch in the filter

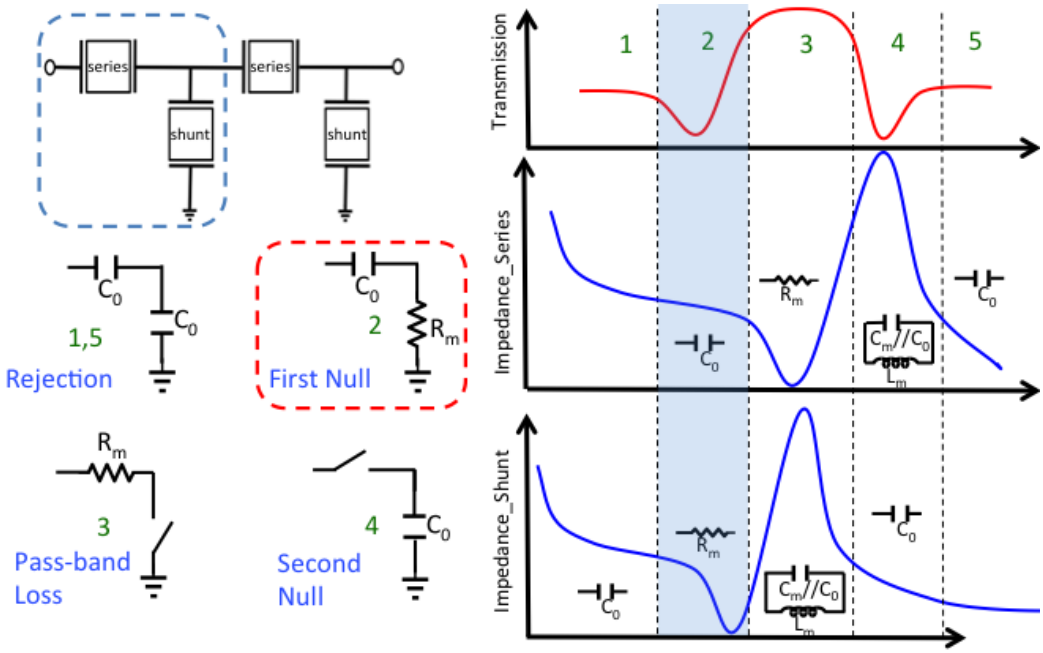


Figure 3.23: Ladder filter operation at low-frequency null.

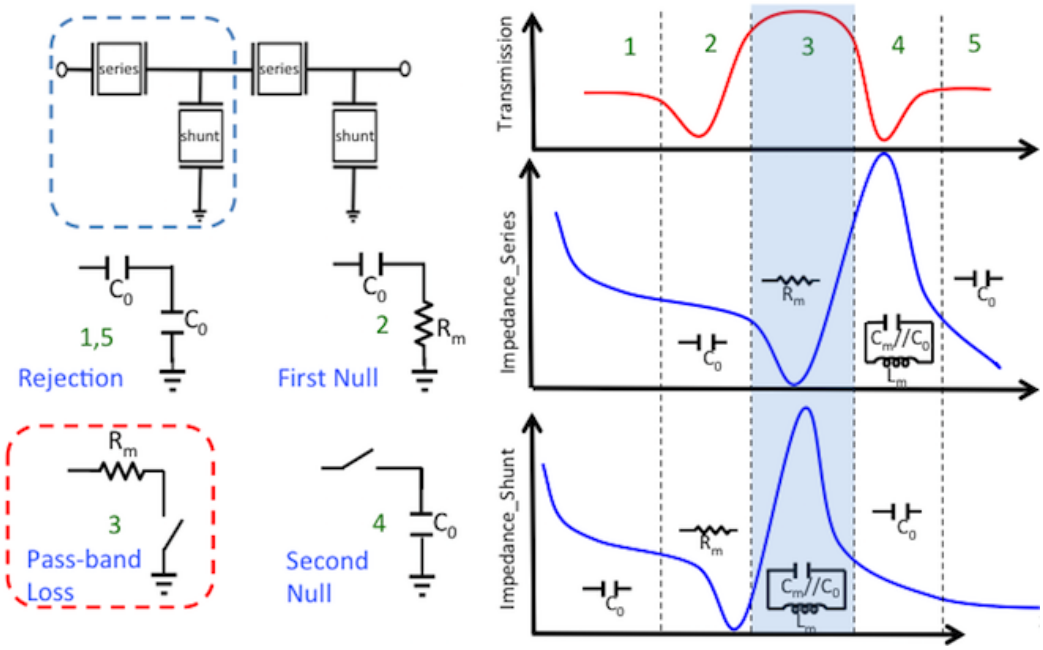


Figure 3.24: Ladder filter operation in pass-band.

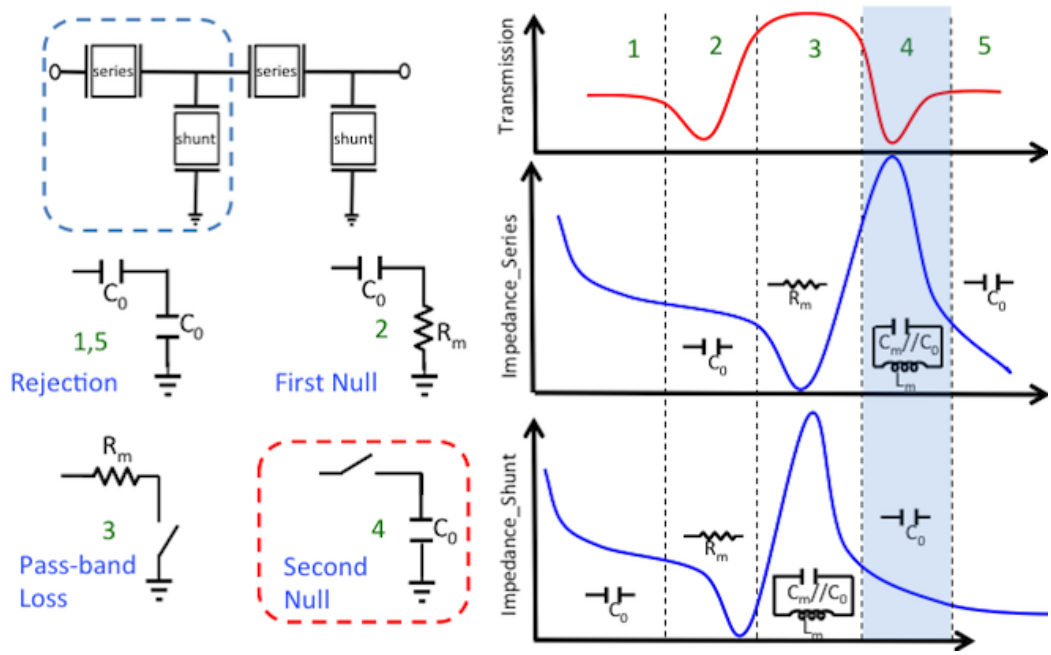


Figure 3.25: Ladder filter operation in pass-band

response. Finally, far from f_p, the filter once again behaves as a capacitive divider.

Based on the operation described above, it is worth noting how the electrical behavior of the individual resonators impacts the overall filter response. The passband insertion loss is primarily limited by the motional resistance of the resonators. A low R_m is desired for the series resonators to provide high signal transmission between input and output and likewise a low R_m in the shunt resonator leads to reduced signal shunting by the shunt resonators in the passband region. The bandwidth of the ladder filter is determined by the separation of the resonance and anti-resonance frequencies of the consitutent resonators. Therefore, a high k_t^2 is desired to achieve a wide-bandwidth filter. With a large k_t^2 value, it is straightforward to reduce the filter bandwidth by adding additional capacitance in parallel with the resonators. Since the out of band rejection is set by the capacitance ratio of the series resonator to the shunt resonator, it is necessary to strike a balance between having a large series resonator to achieve low R_m, and having a small enough area for the series resonator

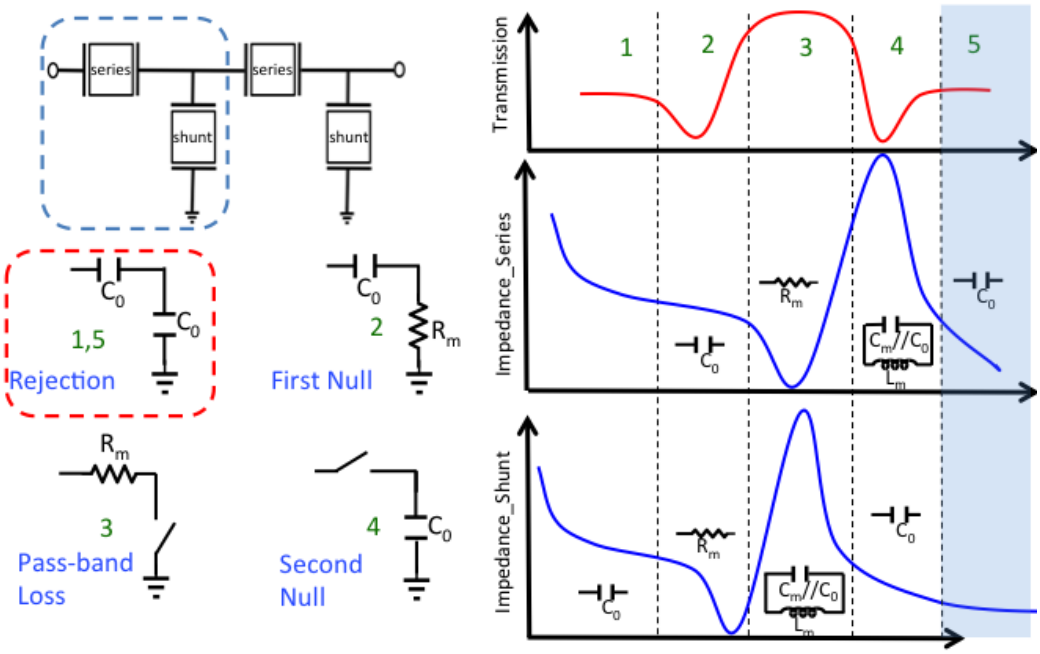


Figure 3.26: Ladder filter operation at high-frequency null.

relative to the shunt resonator to achieve a large out of band rejection.

Shown below are the results of the first fabricated ladder filter. The filter was built on glass by interconnecting previously fabricated 6-layer mirror FBARs. The frequency of the shunt resonators was de-tuned relative by depositing approximately 75nm of sputtered silicon dioxide on the shunt branch resonators. The filter consisted of two cascaded L-sections each consisting of a 100μ m $\times$100μ m shunt resonator and a 300μ m $\times$300μ m series resonator.

As shown in Figure 3.27, the filter exhibits moderate insertion loss in the pass-band, but very low out of band rejection. This is was due to the improper sizing of the resonators whereby the series resonator area was much larger (9times) larger than the shunt resonator area.

In order to improve the out of band rejection of the filter, the filter structure was redesigned with 120μm $\times$120μ m series resonators and 300μm $\times$ 300μm resonators.

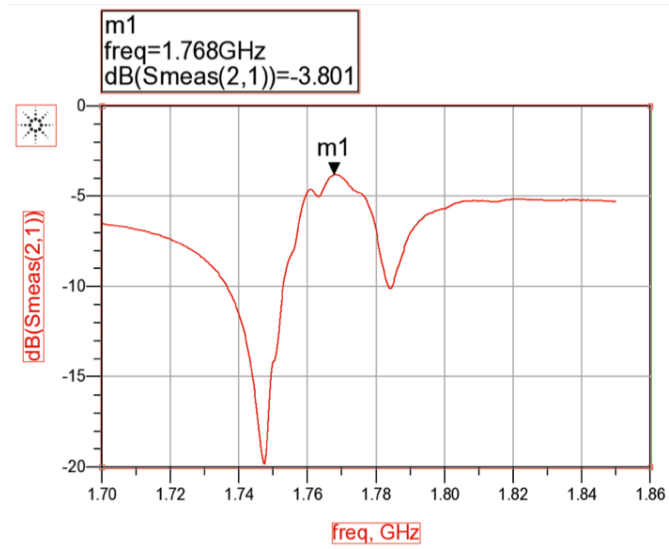


Figure 3.27: Initial ladder filter results.

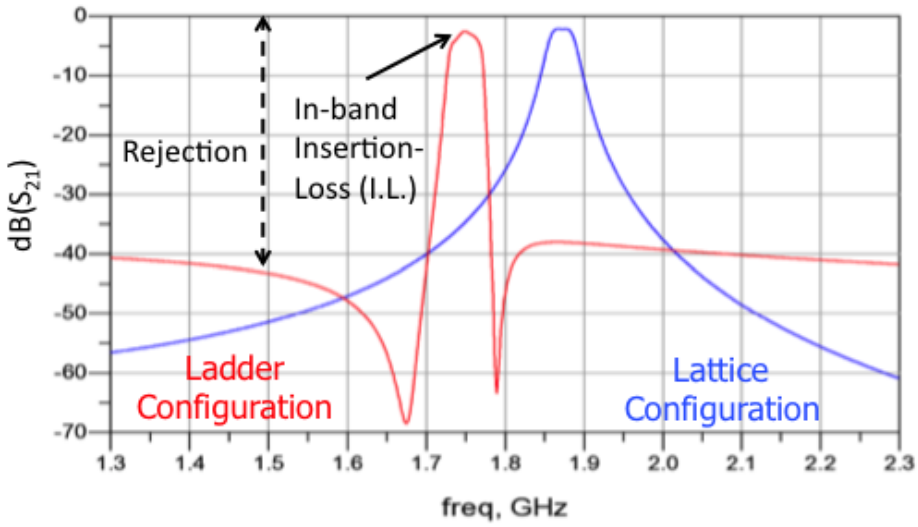
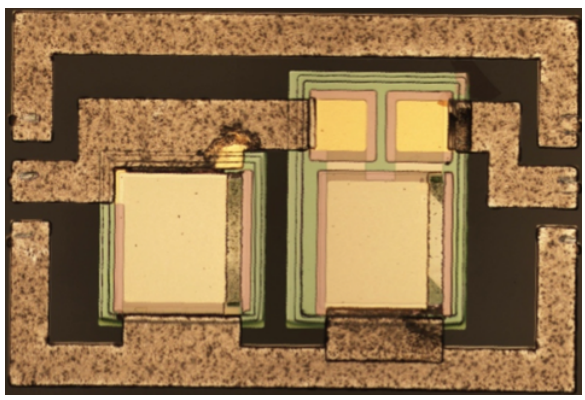


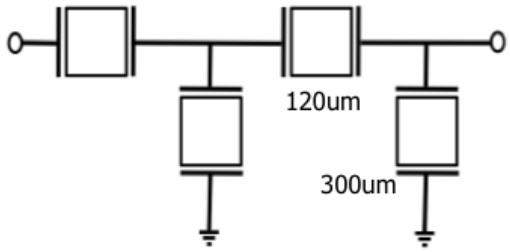
Figure 3.28: Simulated ladder and lattice filter responses based on measured resonator parameters.

The resonator areas were optimized through simulation of two-stage ladder filter using the extracted models for the fabricated resonators. The interconnect between

the resonators was assumed to provide a maximum resistance of 0.3Ω based on the dimensions of the longest aluminum interconnect trace in the filter layout (100μ m $\times$2μ m $\times$30μ m). In order to shift the frequency of the shunt resonator, the L_m value for the shunt resonator was slightly increased. The L_m value was tuned by only ($< 1\%$ of initial value) which leads to a practically insignificant change in the resonator Q from the extracted model values. Shown below in Figure 3.3 is the measured response of the filter along with lumped model fit. Since the filter measurements only allow for measurement of the completed filter, the fit was obtained by the tuning the individual resonator parameters in the filter model to match the measured response.



(a)



(b)

Figure 3.29: Second generation ladder filter: (a) Fabricated ladder filter (b) ladder filter schematic showing resonator sizes.

The filter exhibited much improved insertion loss due to the proper sizing of the

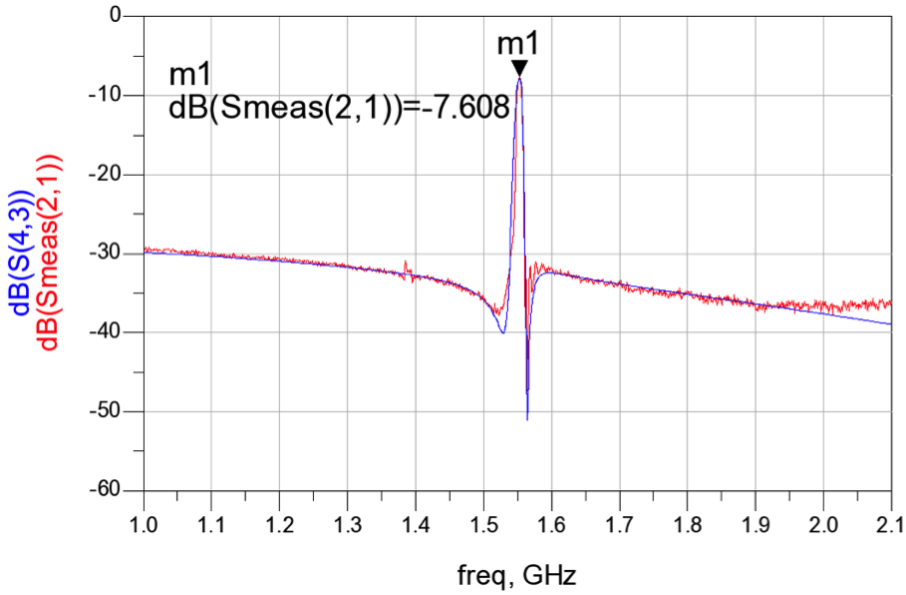


Figure 3.30: Second generation ladder filter response and fitting.

resonators, however the insertion loss was poor. The extracted value of the resonator k_t^2 values across the substrate were found to be between $2 - 2.8\%$. This value is significantly lower than the previously measured value of 8.8%. The poor k_t^2 is clearly reflected in the high values of R_m, namely 9.34 and 3. There is also a significant increase in the series resistance of the 300μm resonator. As mentioned before, the k_t^2 of the zinc oxide piezoelectric layer is strongly influenced by its crystallinity. The crystallinity of the zinc oxide is in turn strongly influenced by the texture of the underlying metallic seed layer (gold in this case). As shown in Figure 3.31, optical inspection shows a noticeable difference between the gold film of the top electrode layer and the bottom electrode layer. The bottom layer appears to be dimmer and more dull indicating a possible increase in roughness value compared with standard gold deposited films. The increased roughness could likely lead to a degradation in the grown zinc oxide film and thus the poor electrical parameters of the resonatores.

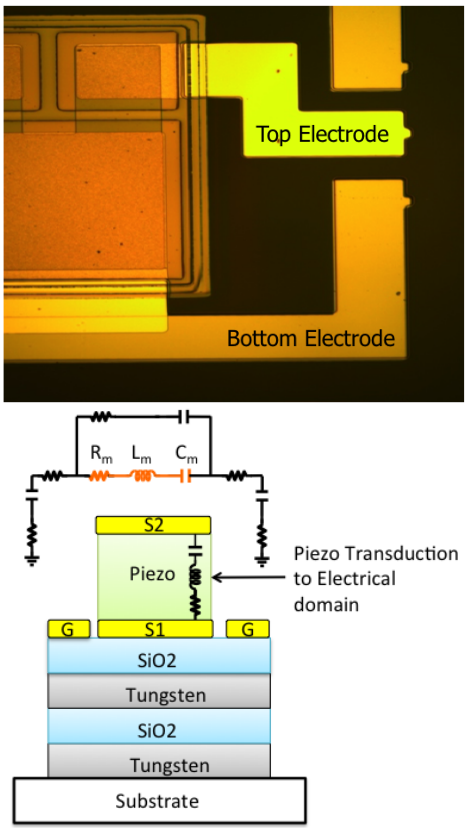


Figure 3.31: Differing gold texture between top and bottom electrodes.

Parameter	Measured Resonators		Resonators Estimated from Filter Fitting	
Size	120μm	300μ m	120μ m	300μ m
$R_m[\Omega]$	9.12	2.30	9.34	3
$L_m[nH]$	533	90.50	530	89.60
$C_m[fF]$	20	117.9	19.83	119.30
$C_0[fF]$	1,165	6,050	1,430	7,166
$R_s[\Omega]$	3	8	0.20	3.20
Q	566	302	550	289

Table 3.3: Lumped model parameters of measured 120μm and 300μm resonators compared with resonator models extracted from fitting of measured filter response.

3.9 Note on Inkjet Mass-loading

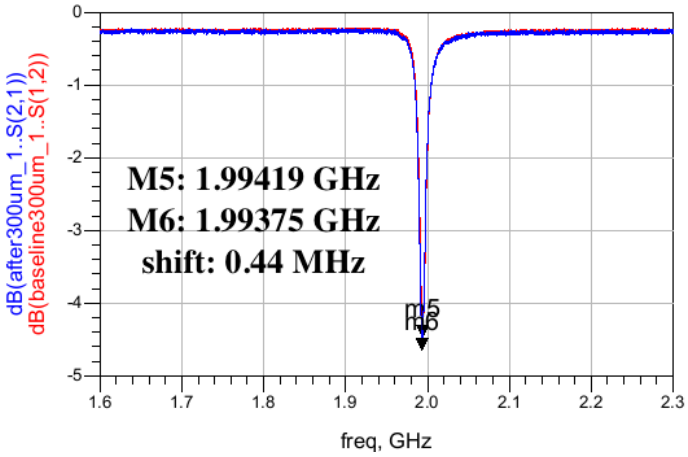
One significant difficulty with fabricating filters is in accurately and reproducibly shifting the frequencies of the shunt resonators. The vacuum deposition and lithographic patterning involved with SiO_2 massloading is complex and time-consuming. A possible, and as of yet unexplored, mass-loading alternative is the use of inkjet-printing. Inkjet printing is a mature commercial technology capable of attaining high throughputs and depositing very small volume and well controlled droplets of a variety of different inks [79]. Here, the inkjet printing of nano-silver ink was explored for filter mass-loading. The silver can be deposited and then induced to reflow to a form a continuous film by low temperature heating (140C). The ink was provided by Advanced Nano Products [80]. In order to attain fine control over the attained frequency shifts, the silver ink was diluted in ethanol. Shown below are initial results of mass-loading and corresponding resonant frequency shit of 300μm resonators using a 1:10,000 silver ink\ethanol mixture.

The results demonstrate the ability to attain frequency shifts smaller than 0.5MHz. A typical FBAR filter will have a bandwidth between 10 MHz-60 MHz [13]. The bandwidth also corresponds to the frequency shift that is needed in the shunt resonators to form a filter. It is clear that technique exhibits sufficient accuracy to adjust two resonators of the same initial frequency to produce a filter response.

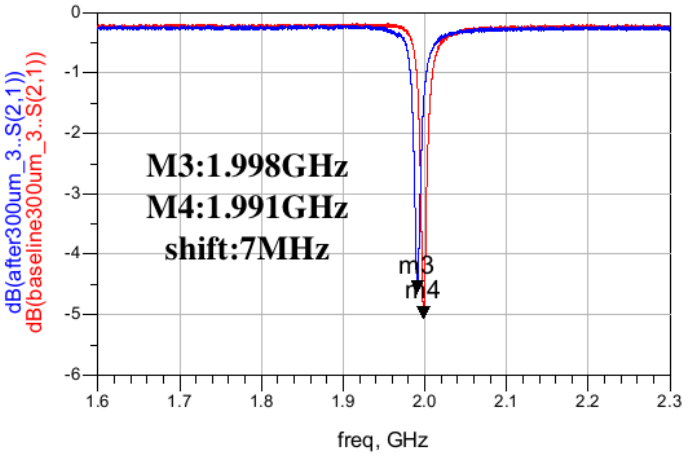
The greater potential of this technique lies in its potential for shifting the response of entire filters to convert a bank of similar center-frequency filters to a bank of staggered, non-overlapping filters. In this case, both resonators in the filter must be shifted in unison. Shown in Figure 3.33 are results for shifting a ladder filter by approximately 2MHz downwards in frequency.

The filter shape is preserved after shifting with only 0.1dB increase in pass-band insertion loss. The technique shows promise with regards to frequency shifting precision. However, more work is necessary to assess the degradation induced by the

silver-ink loading of the individual resonators. Future work will involve fitting the initial and shifted responses to a lumped electrical model and comparing before and after parameters. Additionally, the initial filter used here exhibits high insertion loss. A filter with lower starting insertion loss must be used in future work to establish the validity of the technique for producing contiguous filter banks.



(a)



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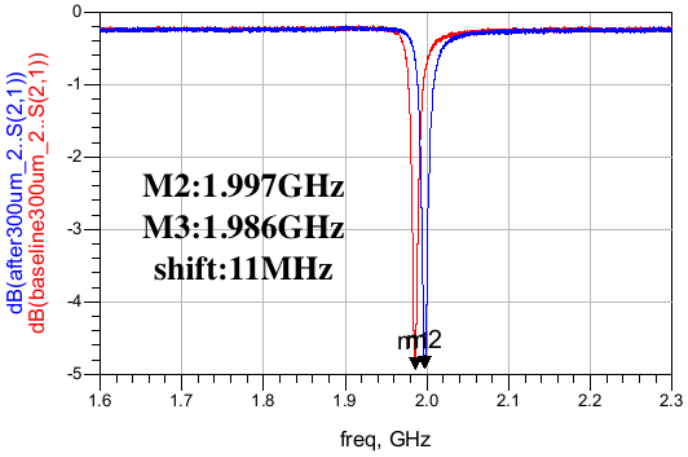


(c)

Figure 3.32: Resonance frequency shifting with different silver ink droplet loadings: (a) 1,000 droplets (b) 3,000 droplets (c) 5,000 droplets.

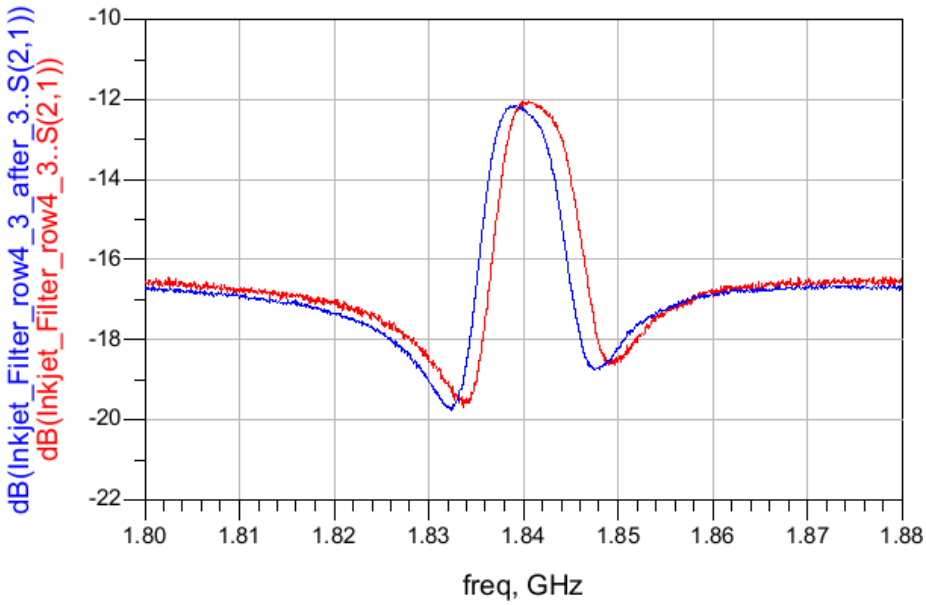


Figure 3.33: Ladder filter shifting with inkjet mass-loading.

3.10 Chapter Summary

In this chapter, practical details of FBAR fabrication and subsequent electrical modeling of FBARs fabricated on glass. Structural optimizations of FBARs are presented along with corresponding improvements in device performance. The fabricated FBARs are then used for implementing bandpass filters. The chapter concludes with a brief discussion of inkjet printing as a technique for shifting resonator frequency to implement filters. Preliminary measurements of the frequency shifting precision are presented.

Chapter 4

CMOS ICs

4.1 Introduction

With electrical models for resonators and preliminary filter results in hand, the next step was the design and tape-out of integrated circuit demonstrator vehicles. The ultimate goal of the project is the demonstration of integration and close interconnection between piezoelectric FBARs and CMOS circuitry with the goal of enabling the implementation of RF transceiver systems with increased frequency agility and reconfigurability. Whereas filters on CMOS are the ultimate goal of the project, a filter is a complicated multi-resonator structure. In the case of failures, inevitable in initial development efforts such as this one, debugging the filter can be very challenging. Moreover, the limited available CMOS die area would not allow for sufficient test-structures and testing points to assess the filter performance. Therefore, the decision was made to use oscillator circuits as the demonstrator platform for the FBAR-CMOS integration

4.2 CMOS IC Demonstrators

For this project two, technologies were available for an IC design, namely TSMC′s bulk CMOS 65nm process and the IBM CMOS7RF, 180nm bulk CMOS process. The IC design proceeded with 3 key goals:

- Testing out new layout strategies to simplify the lithography and fabrication of high quality FBARs directly on CMOS. Emphasis was on simplicity of the post-process and ease of implementation on CMOS dies of different sizes and from different technologies.
- The successful co-integration of FBARs built on the CMOS back-end and underlying CMOS circuitry.
- Implementaiton of CMOS test structures to study the impact of the CMOS post-process on the underlying CMOS transistor circuitry.

The availability of two CMOS processes provided an opportunity to test out the integration on different CMOS technologies with different back-end structures. Based on space availability in the 65nm process ($680\mu m \times 760\mu m$), the decision was made to implement a single oscillator in the 65nm process with minimal test structures and to relegate the bulk of testing structures to the 180nm design which had a larger available area of $1.5mm \times 1.5mm$. What follows is a brief account of the planning and design of each of these ICs. The CMOS IC design portion of the project was led by Daniel Peixoto for the 65nm IC and Aida Cólon-Berrios for the 180nm IC.

4.3 Oscillator Fundamentals

If an ideal LC resonant tank is imparted with a jolt of energy from a current or voltage spike, it will theoretically continue to ring indefinitely at the resonance frequency of

the tank. However, a practical resonator will present a decaying sinusoidal response when excited. If the resonator is periodically kicked with sufficient frequency, the oscillations will no longer decay, but can be made to increase until they stabilize at a level determined by the circuit non-linearities (such as the supply voltage range). This is the essential operating principle of an oscillator, where a sustaining amplifier imparts enough energy to counteract the losses in the resonant tank and enable sustained oscillation [81]. Quantitatively, the necessary conditions for the sustaining amplifier are provided by the Barkhausen criterion which describes an amplifier in feedback with a resonant tank as shown in Figure 4.1 [82].

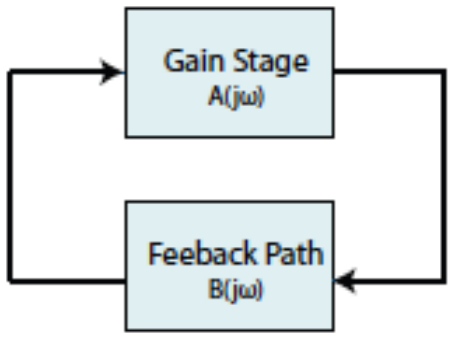


Figure 4.1: Basic feedback circuit describing Barkhausen criterion.

The Barkhausen criterion dictates:

- The loop gain given by the product of the amplifier gain and feedback factor must equal unity $|\beta A| = 1$
- The phase shift around the loop must be zero or an integer multiple of $2\pi, \beta A = 2\pi n, n \in 0, 1, 2, \ldots$

In the case of an oscillator, the gain is usually provided by a transistor amplifier of gain A and the resonant tank forms the feedback element β. A variety of oscillator circuit topologies have been developed for use with acoustic resonators. In this work,

the Pierce oscillator topology was selected [83]. In this circuit, an inverting amplifier provides the sustaining gain while two shunt capacitances(C_1, C_2) work in concert with the resonant tank to the phase shift necessary to meet the Barkhausen criterion as shown in Figure 4.2(a). Please note, biasing details are not shown in the figure. This topology is selected for its simplicity and avoidance of inductors.

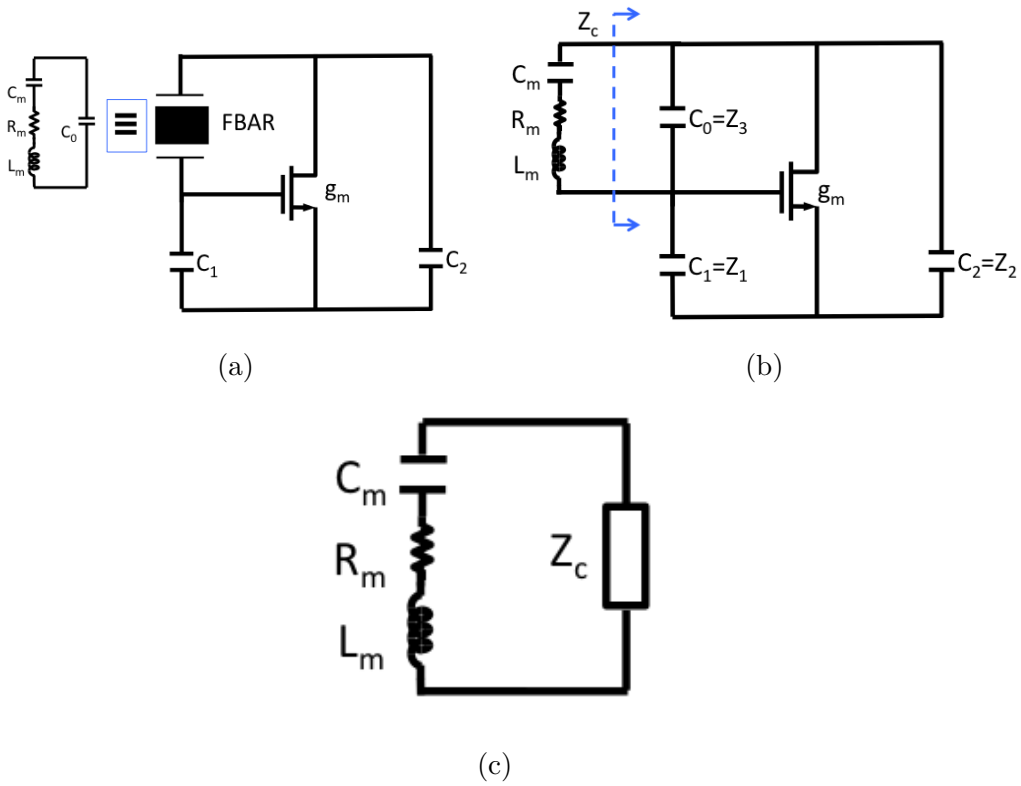


Figure 4.2: Pierce oscillator analysis: (a) Basic Pierce oscillator circuit (b) Simplification of Pierce oscillator (c) Equivalent circuit for for resonant tank and sustaining amplifier.

Following the analysis in [15], the Pierce oscillator can be understood as follows. Assuming linear operation, which is applicable to small oscillation amplitude, the circuit can be simplified by segmenting into a sustaining amplifier portion with equivalent impedance Z_c and a series RLC circuit consisting of the motional elements

R_m, L_m, C_m as shown in Figure 4.2(b). Denoting the different capacitors as general impedances $Z_1 = \frac{1}{j\omega C_1}, Z_2 = \frac{1}{j\omega C_2}, Z_3 = \frac{1}{j\omega C_0}$, the impedance of the sustaining amplifier can be written as :

$$Z_c = \frac{Z_1 Z_3 + Z_2 Z_3 + g_m Z_1 Z_2 Z_3}{Z_1 + Z_2 + Z_3 + g_m Z_1 Z_2} \tag{4.1}$$

By substituting the appropriate capacitor values in in the above eq.4.1, the real and imaginary components of Z_c are found to be :

$$Re(Z_c) = -\frac{g_m C_1 C_2}{(g_m C_0)^2 + \omega^2 (C_1 C_2 + C_2 C_0 + C_0 C_1)^2} \tag{4.2}$$

$$Im(Z_c) = -\frac{g_m^2 C_0 + \omega^3 (C_1 + C_2)(C_1 C_2 + C_2 C_0 + C_0 C_1)}{\omega[(g_m C_0)^2 + \omega^2 (C_1 C_2 + C_2 C_0 + C_0 C_1)^2]} \tag{4.3}$$

The above analysis yields a "negative resistance" element, provided by the sustaining amplifier, which combines with the resonant tank. If the negative resistance is made larger than R_m by proper selection of g_m and capacitor values, the losses in the resonant tank are compensated and the circuit will oscillate at the tank's resonant frequency. Based on the form of the negative resistance in eq.4.2, a few important observations can be made :

- Increasing g_m arbitrarily does not increase the negative resistance. As $g_m \to \infty$, the real part of the negative resistance reaches zero and no oscillation can be attained. Therefore, care is necessary in selecting the value of g_m that maximizes resistance.

- The denominator of $Re(Z_c)$ grows as the square of C_0. Therefore, whereas increasing the area of the resonator by ΔA leads to a corresponding reduction in R_m, the attainable negative resistance for a given g_m reduces by a factor proportional to ΔA^2. Therefore, arbitrarily increasing resonator size is not a feasible solution to increasing negative resistance margin $Re(Z_c) - R_m$

4.4 65nm IC

4.4.1 Oscillator Circuit Design

A single transistor Pierce oscillator was selected for its simplicity. Back-end Metal-Insulator-Metal (MIM) capacitors were used to implement the shunt capacitors of the Pierce topology. The increased surface roughness of the CMOS back-end was expected to cause noticeable degradation of FBAR performance compared with glass devices due to increased scattering and mechanical losses [84]. At the time of design, it was not clear how much the CMOS surface roughness could be reduced. As described in literature, increased build surface roughness can impact both resonator quality factor (Q) and crystallinity and piezoelectric strength of the piezoelectric layer k_t^2. Both of these effects manifest as an increase in the motional resistance value (R_m) of the resonator. Therefore, the Pierce oscillator was designed with a large margin of additional negative resistance to counteract possible increase in R_m.

Shown in Figure 4.3 is the schematic of the 65nm oscillator circuit. The circuit consists of a single nFET transistor as the gain stage. FB1 and FB2 denote the electrodes through which the FBAR top and bottom electrodes contact the circuit. The gain stage is biased through a PMOS current mirror with programming current IBIAS and resistive feedback between the drain and gate sets the DC voltage level at the gate. The output of the gain stage exhibits a swing of 300 mV peak-to-peak centered around 0.2. Therefore, the output capacitively coupled into a level-shifter circuit that translates the DC voltage of the output signal to 0.6 V. This allows the the circuit to properly drive an two-stage inverter-based 50Ω buffer circuit that is used to minimize capacitive loading on the resonant tank and provide a larger output swing that can be measured with 50Ω RF coplanar probes.

The negative resistance of the circuit shows strong dependent on the size of the resonator static capacitance. Therefore, a reduction in resonator R_m through area

scaling will lead to a corresponding increase in the resonator static capacitance which will in turn degrade the effective negative resistance of the oscillator circuit. Therefore, merely increasing resonator size is not a feasible approach to improving oscillator functionality. To this end, two Pierce oscillator topologies were designed based on optimization of transistor size and MIM capacitor value in relation the static capacitances of $100\mu m \times 100\mu m$ and $200\mu m \times 200\mu m$ resonator sizes respectively. Shown below in Figure 4.4 is a plot of the negative resistance of the Pierce oscillator circuit under different bias currents. The simulation was performed under full parasitic extraction of resistive and capacitive parasitics. Based on measured glass FBAR data a $100\mu m$ FBAR presents an $\mathrm{R_m}$ of 5.3Ω whereas a $200\mu m$ FBAR would present an R_m of 0.72Ω at 1.8 GHz. Therefore, the circuit as designed provides 125% percent additional negative resistance for the $100\mu m$ case and 730% additional negative resistance for the $200\mu m$ resonator case.

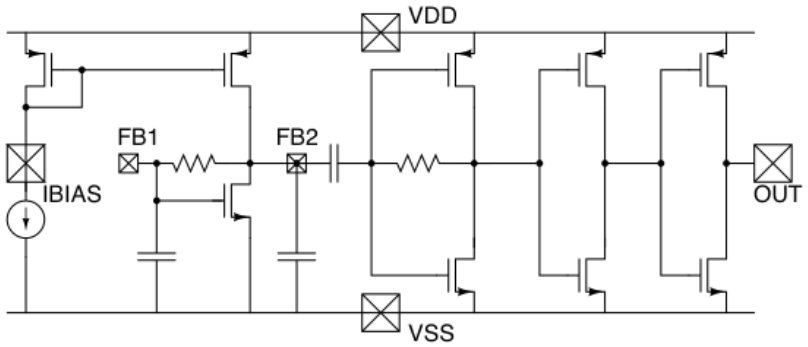


Figure 4.3: 65nm oscillator schematic.

4.4.2 Layout Techniques for FBAR Fabrication

In addition to the pre-emptive design of the Pierce oscillator circuit, the top-level layout was designed to simplify fabrication and potentially allow for the reduction of surface roughness. Special lithographic alignment marks were included in the CMOS

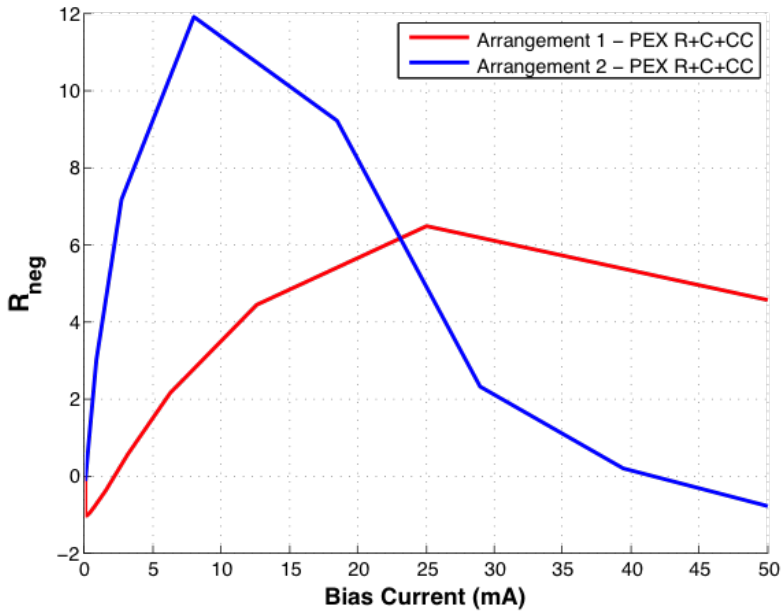
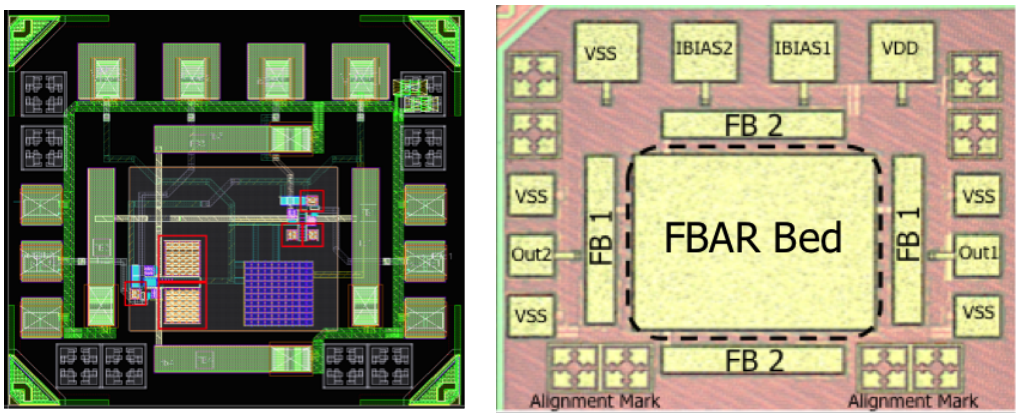


Figure 4.4: Attainable negative resistance with 65nm Circuit.

top metal layer to facilitate contact alignment of sub-10μm features. Furthermore, the native foundry passivation was retained over the bond pads. Typically, the whole chip-back end is coated in a passivation coating, which is selectively removed from the bondpads prior to shipping to the customer. These openings in the passivation are referred to as *glass-cuts*. To prevent bondpad damage during processing, the passivation was retained over the bondpads through manipulation of the CAD layers during bondpad layout.

Finally, a portion of the top metal layer, designated the *FBAR-Bed* was laid out to be used as the FBAR build surface as shown in Figure 4.5. This metal layer serves two purposes. The first is to mask the underlying CMOS circuitry from harsh chemicals and plasma etching experienced during the microfabrication process. The metal of the bed area serves no electrical purpose and could be discarded later if necessary. The second and more important purpose was to explore a new technique

for achieving a low-roughness FBAR build surface. The technique covered in more detail in the next chapter entails removing the top most CMOS passivation layer and subsequently removing the metal of the bed layer to access the underlying planarized dielectric surface. Foundry planarization is adopted in most modern CMOS processes, therefore it is reasonable to assume the CMOS dielectric layer beneath the bed top metal would indeed by planarized.



(a) (b)

Figure 4.5: 65nm IC: (a) IC layout showing circuit directly underneath FBAR bed (b) Die photo showing alignment marks and FBAR bed.

In order to allow rapid measurements of the oscillators following FBAR fabrication, the bondpad layout was optimized to enable on-chip probing using a combination of RF coplanar probes and DC eye-pass probes for biasing. Contact pads measuring ($200\mu m \times 25\mu m$) were designed to connect the microfabricated FBAR to the underlying oscillator circuit. The contact pads for the two oscillator circuits were placed at orthogonal positions around the FBAR bed. In Figure 4.5, the two sets of contact pads are designated FB1 and FB2 for the $100\mu m$ and $200\mu m$ circuits respectively. Shown in Figure 4.6 below is the probing arrangement for the FBAR oscillator circuits.

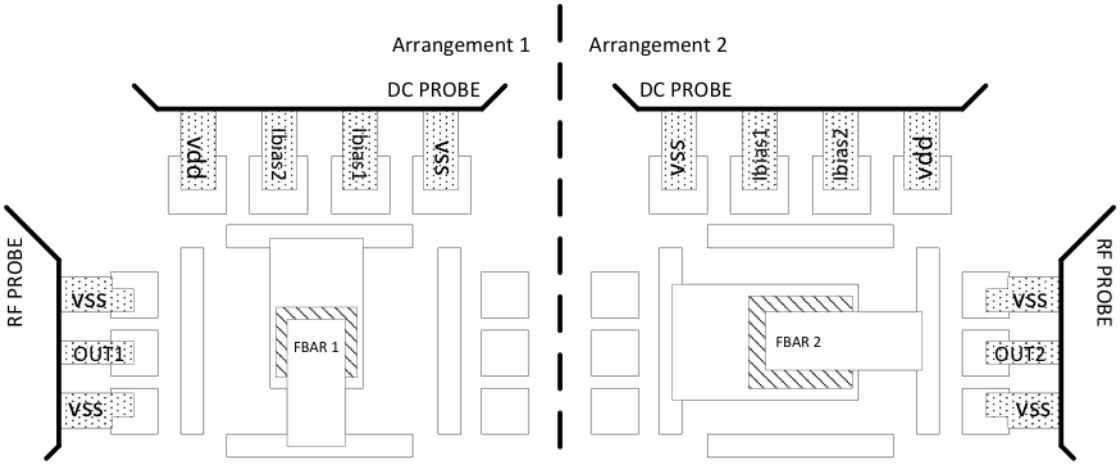


Figure 4.6: 65nm IC testing schematic showing biasing input and RF output configurations for both oscillator arrangements.

4.5 180nm IC

4.5.1 Oscillator and Test Circuits

Given the increased die area ($1.5mm \times 1.5mm$) available in the 180nm process, amore testing structures and oscillator topologies were added than the 65nm IC. The design included the following features will be discussed below

- A single transistor FBAR Pierce oscillator
- A Three inverter FBAR Pierce oscillator
- A probe-able FBAR for measuring with RF probes
- A variety of DC and RF test structures

Once again a single transistor Pierce oscillator was included in the design. The design followed along similar lines to the 65nm single transistor Pierce oscillator using the negative resistance methodology. A probe-able FBAR was also included

which could be measured with RF coplanar probes. This structure can be used to obtain the electrical model of devices built on CMOS compared with their glass-based counterparts. Additionally, a 3-inverter Pierce oscillator topology was added to the design. Understandably, the 3-inverter topology provides significantly higher negative resistance than the single inverter version; exponentially higher. This additional gain practically translates to higher negative resistance. The topology is generally avoided due difficulty in analysis and parasitic oscillations that can be triggered due to the large gain of the circuit [85]. Despite this drawback, the circuit provides a number of advantages for FBAR resonators that render it interesting for experimentation. As shown in previous works [35], GHz frequency FBAR oscillators can be used as highly sensitive mass sensors, by monitoring shifts in their resonance frequency in response to adsorbed material on the resonator surface. The resonant frequency shift is due to a change in the acoustic path length after the mass addition. Frequency shift is the only observed effect if the adsorbed film is solid. However, in biological sensing applications, the adsorbed films are often soft films and the sensing frequently takes place in aqueous media that introduce significant damping and consequent increase of the resonator motional resistance R_m [86]. The high gain of the 3-inverter circuit can be advantageous in such cases. The work in [35] successfully applied the 3-inverter topology in a 0.86 GHz integrated CMOS-FBAR oscillator for sensing applications. An additional application of the high gain of the 3-inverter circuit is in testing different resonator topologies which may still have high Q′s similar to FBARs but larger R_m values [57]. Finally, large negative resistance can be used for exploring the scaling limits of FBAR-CMOS oscillators operating with ultra-small resonators ($< 25\mu m$) and large R_m values.

With regards to test structures, both DC and RF devices were added. The biasing circuitry of the single transistor Pierce oscillator includes diode-connected transistors that can both be used to assess transistor threshold-voltage shifts before and after

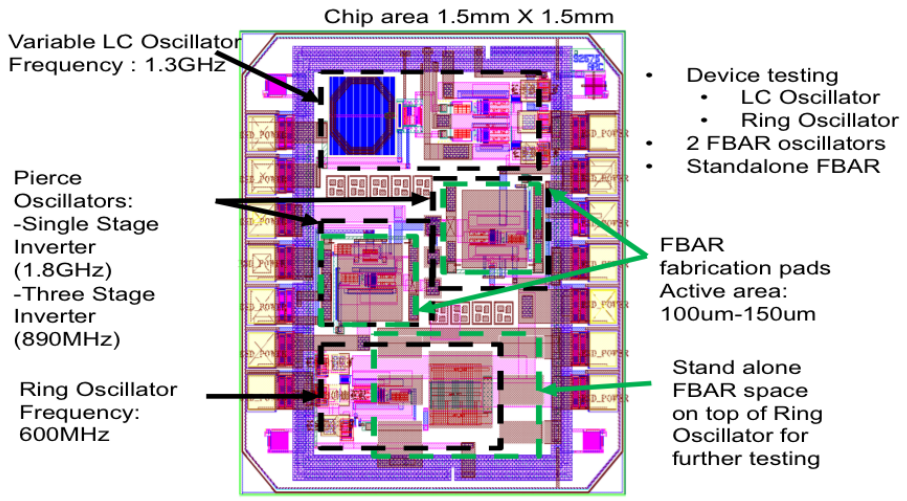
the post-process. Of the few demonstrations of monolithic FBARs on CMOS, the majority have not included FBARs fabricated directly above CMOS transistors but rather relegated to *dead* areas of the silicon with no transistors [19]. Other demonstrations have not assessed coupling and interaction between the FBAR and circuit. Therefore, the 180nm design discussed here incorporates a 31 stage ring oscillator directly beneath the probe-able FBAR. This will allow simultaneous interrogation of the FBAR and ring oscillator circuits and observe any mechanical/electrical cross coupling or frequency pulling. To the author′s knowledge, this demonstration had not been attempted at the time of the IC design.

Finally, a differential LC oscillator was added to the circuit. This allows direct comparison of an LC and FBAR oscillator built directly on the same CMOS die with regards to phase noise performance. More importantly, this would allow experimentation with building of FBARs directly atop the inductor using specially designed, slotted FBAR electrodes. The inductor can be probed directly using on-wafer probes to ascertain a detailed electrical model before and after fabricating the FBAR by exposing the inductor terminals. The oscillator can then be tested in a similar fashion to the FBAR/ring oscillator system to observe any cross-talk and coupling between the FBAR and LC oscillator circuit.

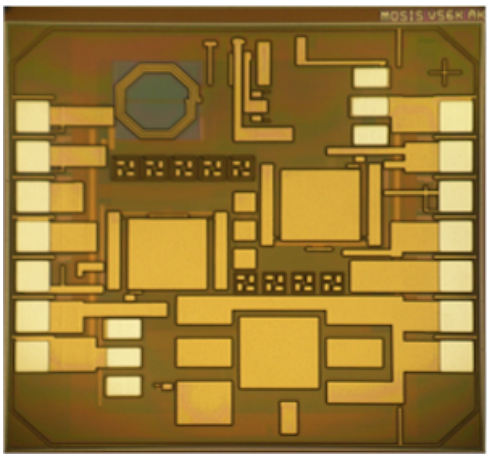
4.5.2 180nm IC Layout

The 180nm IC layout adopted similar approaches to the 65nm chip including protection of the FBAR contact pads and a designated FBAR bed for experimenting with planarization. However, due to the variety of test structures on the chip, it was necessary to be allow bondpad access for electrical testing prior to the FBAR post process. Therefore, the bondpad layout cells were not modified and incorporated the customary glass-cut from foundry. Due to the large number of circuits involved and the limited area on chip, the Vdd ring of the pad-frame was segmented at multiple

points to yield 4 isolated Vdd domains. Additionally, the pad-frame was modified from the standard square pattern with bondpads on all four sides to a more rectangular form with bondpads on only two sides to provide more space for the test circuits and top metal probing pads. The overall die area was $1.5mm \times 1.5mm$. As opposed to the 65nm design, the whole 180nm die was dedicated to FBAR circuits and was not shared with other designs. The layout and test circuit arrangement is shown in Figure 4.7



(a)



(b)

Figure 4.7: 180nm IC: (a) Layout of the 180nm IC showing the different Circuits (b) 180nm die photo.

4.6 Fabrication on CMOS

As discussed previously, a key thrust of this project was the development of techniques and procedures to allow for the integration of acoustic resonators on CMOS dies for implementing hybrid CMOS-acoustic circuits. CMOS circuits and other technolo-

gies are invariably fabricated using wafer level operations whereby circuits are fabricated using photolithography based processes on large wafers ranging from 200mm to 300mm in diameter. A typical IC design will not exceed a few mm to a cm in size. Therefore, a single wafer can host multiple copies of a single design with the wafer subsequently diced to separate the individual copies of the design known as *dies*. The manufacturing cost of a single wafer is quite high, in the range of 10's of thousands of dollars, and researching new designs typically does not require a full wafer's worth(100s-1000s) of dies.

This lead to the birth of the multi-project wafer (MPW) concept whereby multiple designs, usually from unaffiliated groups, are combined and placed onto a single wafer. As a result, dramatic costs reductions are achieved by leveraging the parallel processing nature of wafer manufacturing and integrated circuit prototyping is made available to a larger customer base. MPW services such as MOSIS (Metal Oxide Silicon Implementation Service) provide several MPW fabrication runs every year in a number of different technologies available to university and commercial users [42]. The MPW concept lead to the emergence of the *fabless* semiconductor model whereby designers can focus their efforts on IC design at the computer-aided-design (CAD) level and outsource the actual semiconductor fabrication to an MPW foundry which compiles designs from multiple fabless designers.

While MPW runs significantly reduce costs, the MPW form factor introduces a number of challenges to further processing using micro/nano-fabrication techniques. This is not surprising given that MPW dies are typically viewed as a final, packaged module to be inserted into a chip package and probed externally as opposed to a substrate to be used for micro-fabrication. As CMOS silicon real-estate is costly (at least thousands of dollars for $40mm \times 40mm$ area in a mature CMOS technology such as 180nm), designers attempt to cram as much transistors as possible into a small area. Therefore, dies can easily be as small as 1mm x 1mm and incorporate a large

number circuit functionalities [87,88]. The small die form factor introduces a number of significant challenges with regards to micro-fabrication.

4.6.1 Die Handling And Resist Spinning

Small die sizes necessitate careful handling to prevent damage to the die. Techniques used to handle dies for wire-bonding or packaging cannot be applied in this case. Such techniques generally involve contacting the top surface of the die and can lead to damage of any structures micro-fabricated atop the die surface in addition to causing surface contamination. Therefore, it becomes necessary to mechanically attach the die to a larger, sacrificial carrier substrate that can be handled with ease. The carrier substrate and the means of bonding the die to such substrate must be chemically stable towards the various chemicals used in the micro-fabrication process.

The vast majority of fabrication process flows rely on optical/electron lithography to pattern desired structures on an underlying substrate. A lithography process relies on transferring a pattern to an imageable resist material (photoresist) that can be subsequently transferred to an underlying thin-film using subtractive (etching) or additive (lift-off) patterning as explained in chapter 2.

Spin-deposition provides an efficient and reproducible method for depositing photoresist over a substrate's surface. Here, liquid-form resist is dispensed onto a spinning substrate. The centrifugal force from the rotation leads to the formation of a thin, uniform coating that can be controlled by adjusting spin speed, duration and acceleration. In addition to the circular perimeter that allows for even flow of resist towards the edges, wafers typically have beveled edges that ease the flow of resist off the wafer edges. However, rectangular/square substrates with edge sizes on the order of mm′s provide an unfavorable surface for resist spinning whereby the centrifugal force induced by the spinning is not sufficient to flow resist off the edges of the sample. The result is aggregation of resist at the edges of the chip leading to an *edge-bead* as

shown in Figure 4.8.

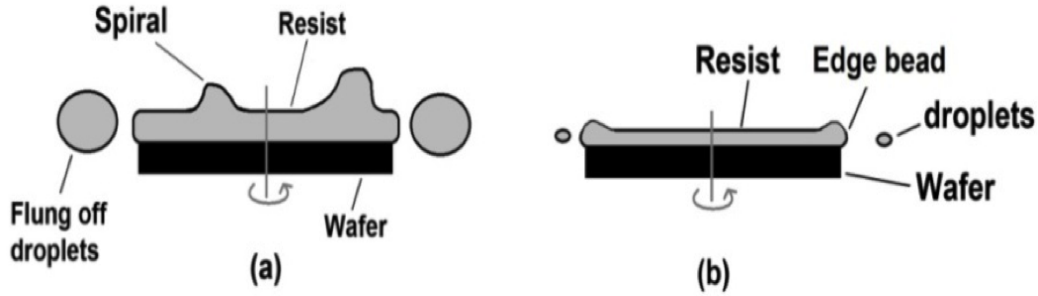


Figure 4.8: Edge-bead formation during resist spinning.

For mm sized dies, this situation leads to edge-beading of size comparable to the die area. Moreover the photoresist bead generally exhibits non-uniform thickness across the die area. Consequently, in-place of a resist film that should nominally be $1 - 10\mu m$ in thickness with less $100nm$ of variation across its surface, one is left with a non-uniform, beaded resist film that can vary from single microns to 100's of microns in thickness across the die surface. During lithography exposure, the thickness variation leads to non-uniform exposure of the resist film with the thicker areas experiencing higher dosages than the thinner ones. Moreover, UV exposure light has a finite depth of focus (Figure 4.9) within which the exposing pattern is in acceptable focus. The edgebead will generally be far thicker than the depth of focus (> 10) and lead to distorted feature transfer to the resist coated-substrate. Finally, the majority of lithography systems in use in research environments are contact lighoraphy setups which bring the photomask into physical contact with the resist-coated substrate. Even soft-contact between mask and substrate will most likely lead to resist cracking that can expose the underlying substrate and lead to erroneous lithographic patterning.

A related problem is that of resist bubbling. A CMOS die typically has non-planar surface topography with up to $5\mu m$ of thickness variation between thick aluminum

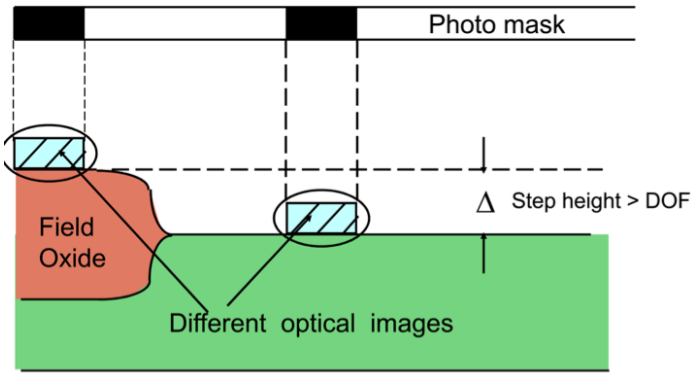
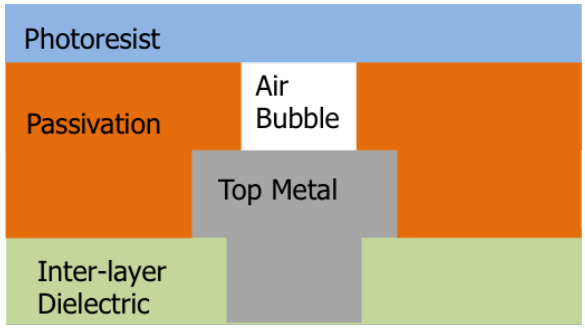


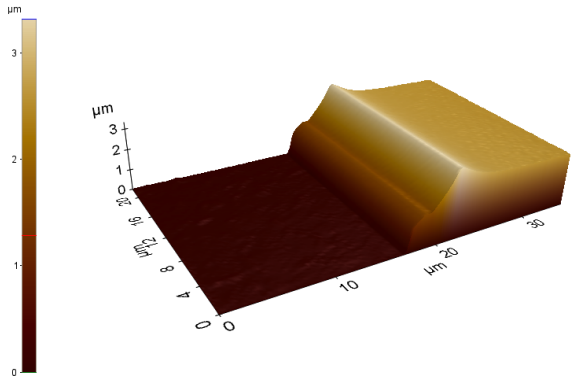
Figure 4.9: Depth of focus during lithography.

contacts and dielectric coated regions of the die surface. This the situation observed with glass-cut openings or vias. The thickness variation in addition to the vastly different thermal conductivities between the metal pad regions and the dielectric coated regions can lead to significant bubble formation during resist baking as opposed to baking on a flat wafer surface. Shown in Figure 4.10 is the schematic of a CMOS passivation opening above a metal-pad. Improper resist baking can leads to bubble formation between the resist and metal-pad. The bubbling effect is exacerbated by the use of thick photoresists which are commonly used for etching and lift-off of thick layers in MEMS devices. Thick resists will generally incorporate more bubbles during spinning and baking than their thinner counterparts.

Bubbles cause the same problems of cracking and de-focusing resulting from edge-bead formation. Bubbling above metal-pads is evident in Figure 4.11 showing a 180nm CMOS die following baking of resist. It is worth observing that bubbles concentrate around pad areas likely due to the thermal mismatch between metal and dielectric layers. Typically all the above-mentioned fabrication problems occur in concert as shown in Figure 4.12. Spinning of a $3\mu m$ thick resist (Microchem LOR 30B) leads to significant beading at the chip edges (Figure 4.12 (b)) with subsequent resist baking leading to resist bubbling around the metal-pads in the chip periphery. Contact with



(a)



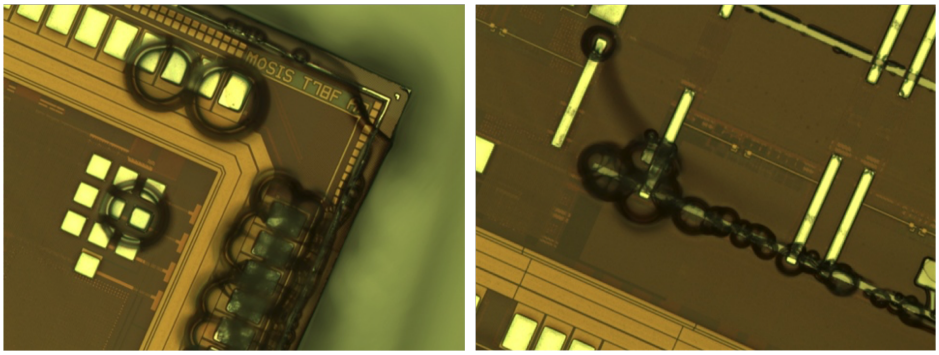
(b)

Figure 4.10: Formation of resist bubbles in CMOS pads: (a) Schematic of bubble formation in a CMOS pad (b) Measurement of pad via thickness.

the the photomask during alignment leads to resist cracking (Figure 4.12 (c)) which exposes the underlying die surface in undesired areas (ones that should nominally be masked by resist) and can lead to the formation of erratic vein patterns during photoresist developing.

4.6.2 Bondpad Damage

Another challenge with die processing is that of protecting bondpads. In most CMOS processes, aluminum is used as the top most metal layer for bondpads that connect the chip to the external world. Even tecnologies based on copper metallization will



(a) (b)

Figure 4.11: Bubbling in CMOS pads with improper Baking: (a) Bubbling near die periphery (b) Bubbling near center of die.

generally have a coating of aluminum on the top layer to enable wirebonding. Any device fabricated atop a CMOS die will need to electrically access underlying circuitry though this layer. While aluminum exhibits favorable electrical properties, it is easily etched by chemicals commonly used in microfabrication operations such as photoresist developer containing Tetra-Methyl-Ammonium-Hydroxide (TMAH) and Potassium-Hydroxide (KOH). Therefore, care must be applied when processing CMOS dies in order to avoid damage to aluminum pads which could complicate subsequent chip bonding after. If aluminum bondpads are etched, it becomes increasingly difficult to access the circuit connected to the bondpad without complicated etching and the possibility of damage to the CMOS die. As an illustration of the above, a short, 4 minute exposure to aluminum etchant (frequently used to pattern aluminum layers) leads to almost complete etching of the thick aluminum contact pads in the periphery of a 180nm CMOS die as shown in Figure 4.13.

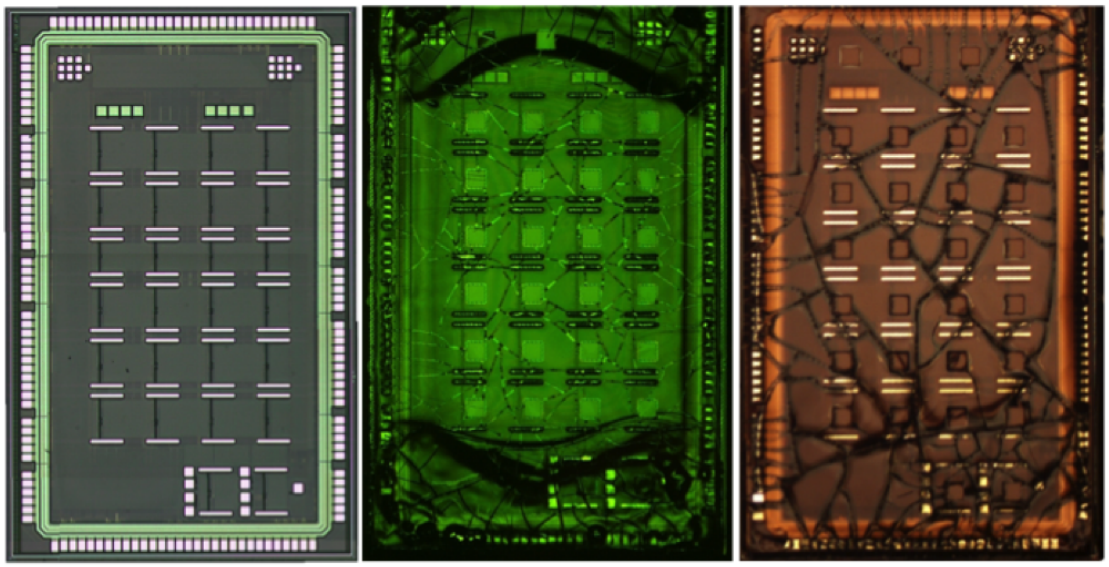
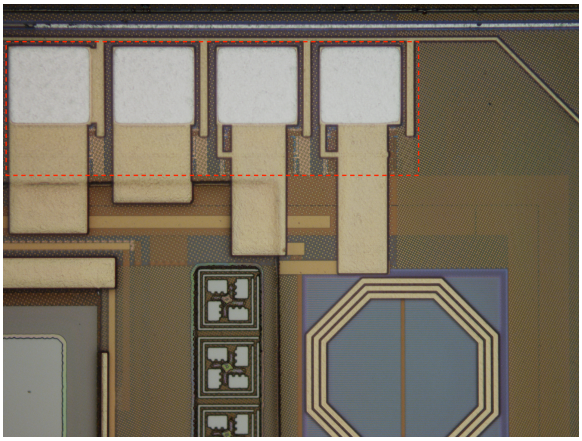


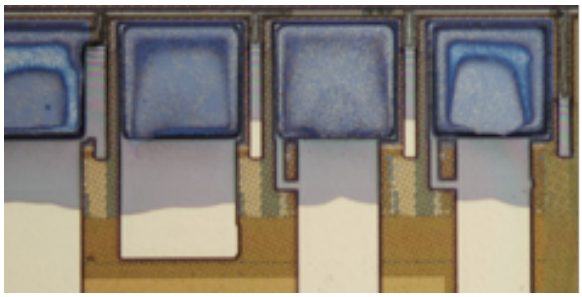
Figure 4.12: Resist cracking: (a) CMOS die before processing (b) CMOS die showing resist beading at edges (c) Resist cracks emanating from bondpad ring.

4.6.3 Surface Roughness

For acoustic devices, surface roughness is a very important consideration. As noted in [84], the degree of roughness of the substrate on which an acoustic resonator is built, can have a profound effect on the performance of the resonator. In [84], a 3-fold reduction in acoustic resonator quality factor was observed, as roughness of the build substrate was increase from 2nm to 6nm. This result is significant since the top surface of CMOS dies is not customarily planarized. In addition to the micron-range thickness variation between different regions of the surface (glass-cuts are several μm deep), the local surface roughness over small areas ($5\mu m \times 5\mu m$) can be as high as 20 nm which can lead to poor performance of acoustic resonators built on such a surface.



(a)



(b)

Figure 4.13: Etching of CMOS Pads: (a) Pads as received from foundry (b) Pad etching following short exposure to etchant.

4.6.4 Thermal Budget

Finally, thermal budget is a critical consideration in fabricating any structures on a CMOS MPW die. As received from foundry, the CMOS die consists of a complicated stack of transistors and corresponding interconnect layers. It is necessary that any subsequent processing operations take place within a temperature envelope (typically <300°C for foundry CMOS) that does not lead to damage of interconnect layer (due to thermal expansion mismatch) or damage transistors (e.g. dopant diffusion). Therefore, provisions must be made to keep processing temperatures low enough.

4.7 Development of Die-level Processing Techniques

In order to address the challenges above, a number of processing techniques were developed. This will be outlined in the following sections and will be ultimately applied to the fabrication of FBARs on 180nm and 65nm CMOS dies.

4.7.1 Resist spinning

In this work, processing of CMOS dies commenced by bonding the dies to a silicon carrier wafer. A number of bonding agents were explored. The key attributes desired were thermal stability during processing (incurred during resist baking $\sim$ 180°C). Secondly, the bonding agent should be chemically stable in N-methyl pyrrilodine (NMP), which is a solvent used for lift-off and stable in TMAH-based photoresist developer.

NMP is a very aggressive solvent and its use rules out most photoresists and epoxies as bonding agents. Furthermore, standard solvents such as acetone and isopropyl alcohol (IPA), which are used for surface cleaning, will generally dissolve most epoxides. Wafer-bonding epoxies such as CR-200 [89] exhibit temporary stability to NMP exposure ($\sim$ 1 hour in NMP), however the number of lithography steps involved in FBAR fabrication in this work can be as high as 12steps with multiple hour-long soaks in NMP.

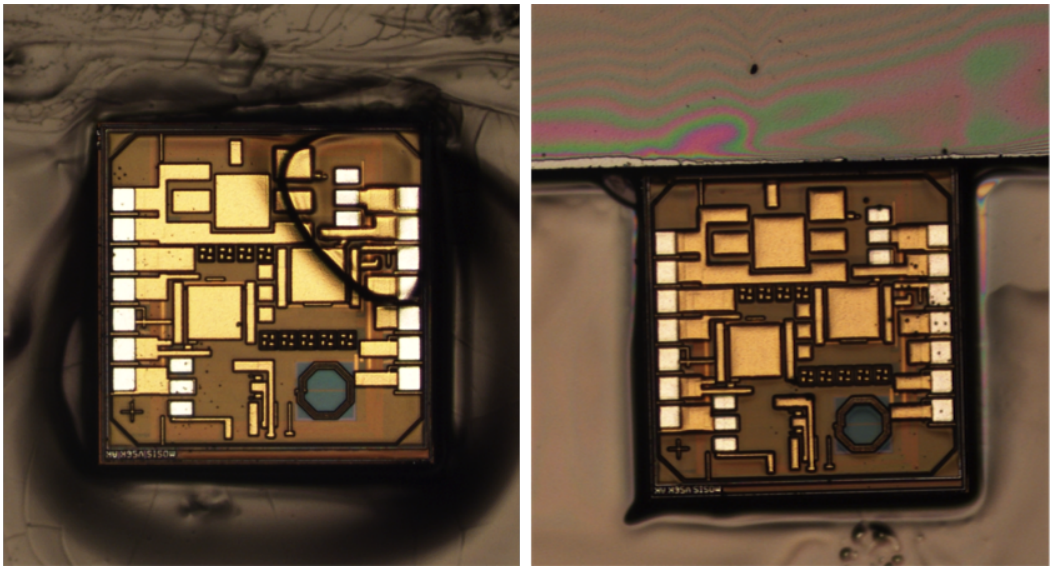
The decision was made to use the SU-8 family of negative epoxies [90]. SU-8 is a photo-imageable epoxy that exhibits high temperature stability (up to 300°C) and resistance to chemical etching in NMP after cross-linking by baking at temperatures above 150°C. Furthermore, SU-8 resists exhibit some degree of reflow which allows during baking which allows them to more easily fill voids and imperfections in a CMOS die surface [91] .

To mitigate edge-bead formation, two process additions were introduced. First,

$6mm \times 6mm$ bare silicon dies were thinned to the same thickness as the MPW CMOS dies ($300\mu m \pm 10\mu m$) by etching in an SF_6/O_2 plasma using an OXFORD plasmalab 80+ etching system. The etch was performed at 20 mTorr with 10 sccm and 10 sccm SF_6 and O_2 flow rates respectively. An ICP power of 50 W was used with an RF power of 250 W. The thinned silicon dies are first bonded to the carrier wafer, and subsequently the MPW dies are abutted to the silicon dies using SU8 3005 with the abutted assembly baked at 150°C for 5 hours to set both dies in place. The SU-8 bonding layer is spun at 3000 rpm for 45s at an acceleration of 10,000 rpm/s.

The abutting die effectively extends the surface of the CMOS die and increases its area leading to much reduced edge-bead formation. Furthermore, any resulting edge-bead forms far away from the area of the MPW die and can be easily removed by wiping with solvents. In order to avoid the need for abutting on every corner of the CMOS die, the assembled carrier wafer is mounted such that the CMOS die is positioned approximately 0.5 inches off-center from the center of the spinner chuck leading to resist flow effectively in a single direction over the surface of the CMOS die. As shown in Figure 4.14, the abutting technique leads to a significant improvement in resist coating and reduction of edge beading even with the 180nm dies which measure only $1.5mm \times 1.5mm$.

Previous work on CMOS dies involved the use of dry-film resist [92]; whereby instead of spinning, the resist is applied by laminating a solid resist film to the substrate and baking to adhere to the substrate. In comparison to dry film resists, the approach outlined here allows for a wider selection of resists to be used, since most resists are not available in dry-film form. Moreover, the approached presented allows processing of smaller die sizes than can be used with dry-film resists.

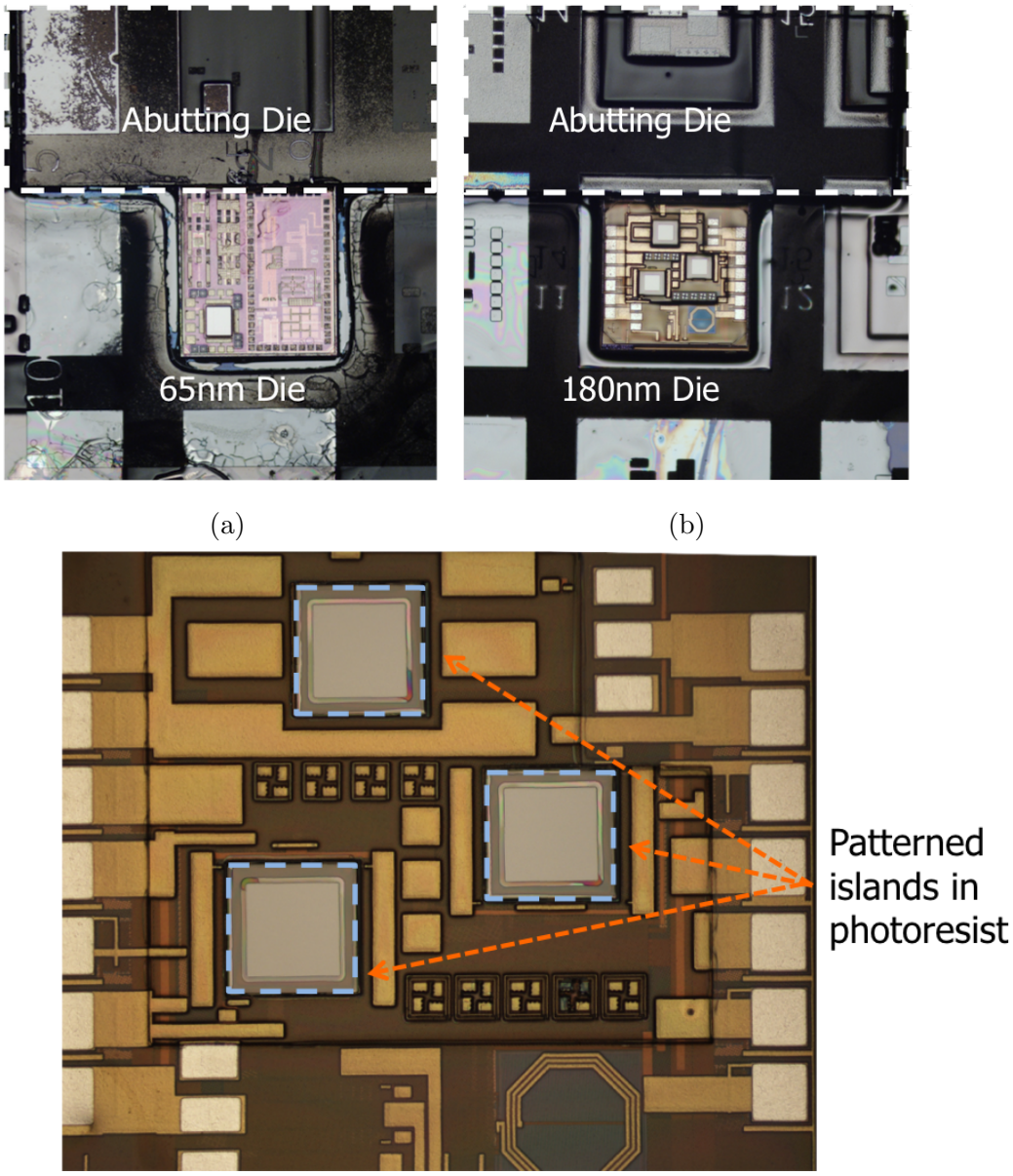


(a) (b)

Figure 4.14: Resist spinning on 180nm die: (a) Beading without abutting die (b) Reduced edged beading with abutting and off-center spinning.

4.7.2 Ramped Resist Bake

Resist spinning is only the first part of successful resist application to the MPW dies. In order to harden the resist, a soft-bake is required. Whereas CMOS processes employ sophisticated layer planarization schemes to allow lithography of fine features and improve fabrication yield, the top-most layer of a CMOS die is typically not planarized. From the foundry′s perspective, this would add unnecessary processing steps and costs for a surface that is not originally intended as a substrate for micro fabrication. This leads to a surface with large topology variation (∼microns). Coupled with the fact that the thicker layers are typically very thermally conductive copper or aluminum and the lower portions are insulating polyimide and nitride coatings, a large thermal gradient with abrupt interfaces results across the die surface. The thermal gradient is exacerbated in the vicinity of features with sharp edges. When using viscous resist such as polydimethylglutarimide (PMGI) based lift-off resists,

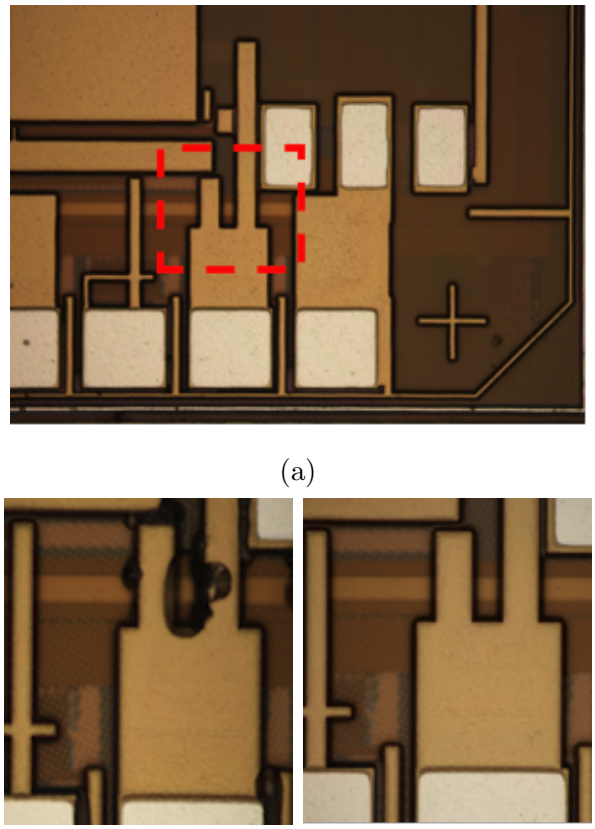


(a) (b) (c)

Figure 4.15: Die-abutting: (a) Abutted 65nm die (b) Abutted 180nm die (c) Successful lithographic patterning on 180nm die with no damage to bondpads.

bubbles will readily form during baking. To confront resist bubbling, a multi-stage, ramped soft-bake is employed during the resist baking step. It is necessary to provide

a gradual heating of the resist, since a number of thermal interfaces are now present compared with the case of resist spinning directly on glass or a silicon wafer: Heat must first travel through the bonding adhesive (SU-8) and into the base of the CMOS die. Following this, the thermal flux must travel through the complicated CMOS stack of transistors and back-end interconnect layers. Finally, the heat makes its way through the passivation coating on the die surface and into the resist film. Applying a 3-stage ramped bake (115°C, 150°C, 170°C) to the baking of a $3\mu m$ LOR 30B resist layer [93] eliminates bubbles compared with a single-step bake at 170°C for the same duration (Figure 4.16).



(a)

(b) (c)

Figure 4.16: Resist bubbling during bake: (a) Area observed on die surface (b) Resist bubbling with single step bake (c) Bubbling eliminated with multi-step resist bake.

4.7.3 Passivation Etching

As mentioned before, aluminum or aluminum/copper combinations are typically employed as the top metal layer in CMOS processes. The challenge in fabricating on such dies is the ease with which aluminum etches in standard photo-resist developers, which are either potassium hydroxide or Tetra-methyl-ammonium hydroxide, based. Since, the proposed fabrication involves up to 12 layers of lithography and each lithography layer requires a resist developing step, it is absolutely critical that any exposed aluminum in the bondpad layer be protected from developer. To this end, two approaches are adopted.

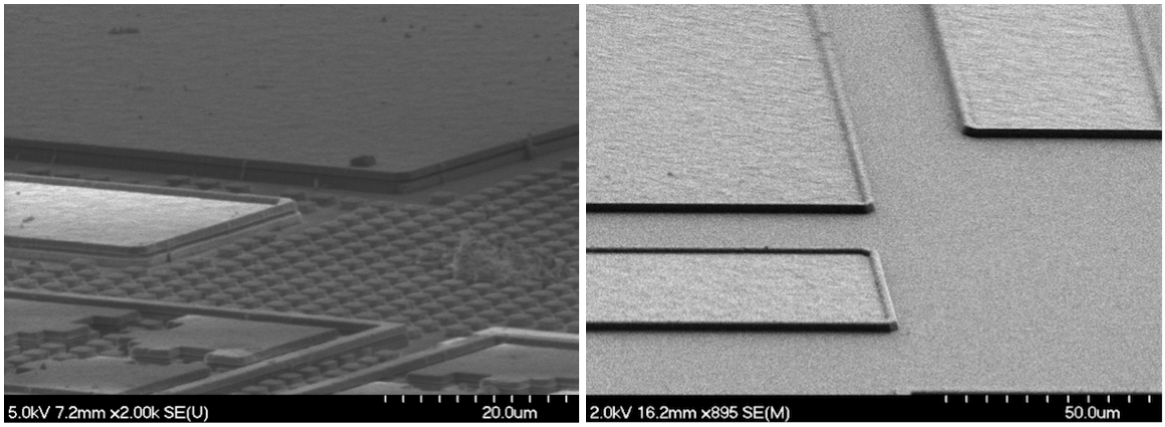
4.7.3.1 65nm Bondpad Passivation

In the 65nm chip, the native, foundry polyimide passivation was retained through customized layout techniques. In IC fabrication at a silicon foundry, the final step of chip fabrication is the etching of the polyimide passivation layer to expose the underlying bondpad metal in what is known as a glass-cut. During IC layout, the glass-cut layer was deliberately removed so that the bondpads would remain passivated. The passivation layer would be retained throughout the fabrication process, only to be removed at the very end of the process flow using an in-house glass cut etch.

The etching took place with using an SF_6/O_2 chemistry in an ICP reactor [94]. The polyimide (typically applied via spin coating at foundry) is primarily etched by oxygen whereas SF_6 is incorporated to ensure removal of any silicon-based adhesion promoters used to enhance polyimide adhesion to the die surface. In most CMOS processes, the interconnect back-end stack is terminated in layers of silicon oxide and silicon nitrides which is subsequently coated in the spinnable polyimide coating described above [95]. Any metal pads that have not undergone glass-cut etching are embedded in this nitride/oxide/polyimide stack. The exact thicknesses and layer compositions of this backend passivation is proprietary and varies by technology and

from foundry to foundry.

Compared with its poor resistance to wet-chemical etching, aluminum is very stable to dry etching in fluorine and oxygen due to the formation of a protective coating of aluminum oxide [96]. Therefore, the polyimide/back-end etching can easily be terminated at aluminum layers. However, the same cannot be said for the nitride and oxide layers since nitrides and oxides do exhibit non-negligible etching in fluorine containing plasmas. Therefore, it is necessary to optimize the back-end etching duration in order to avoid over-etching of the passivation stack and lead to undesired exposure of the underlying interconnect layers. Shown in Figure 4.17 (a) is an over-etched 65nm chip showing significant passivation etching to the point of exposing underlying metal-fill layers. This could lead to shorting across the die and expose chemically fragile back-end metal layers to chemical etching during the microfabrication processes.



(a) (b)

Figure 4.17: 65nm passivation etching: (a) Over-etched 65nm die showing dummy metal-fill squares (b) Optimized passivation etching.

In order to optimize the passivation etching, two indicators were used to detect etching end point. First, energy-dispersive X-ray (EDX) measurements were performed at different stages of etching to detect the removal of the polyimide and

(a) (b)

Figure 4.18: Multi-layer via strategy: (a) Pads as received (b) Even though top metal is etched, vias remain. This allows contacting the underlying circuit despite the etching.

nitride/oxide coatings. EDX is based on the interaction of X-ray excitation and the material under testing [97]. Due to the unique atomic structure of each element, a distinct peak appears in the EDX spectrum corresponding to each element present in the sample under examination.

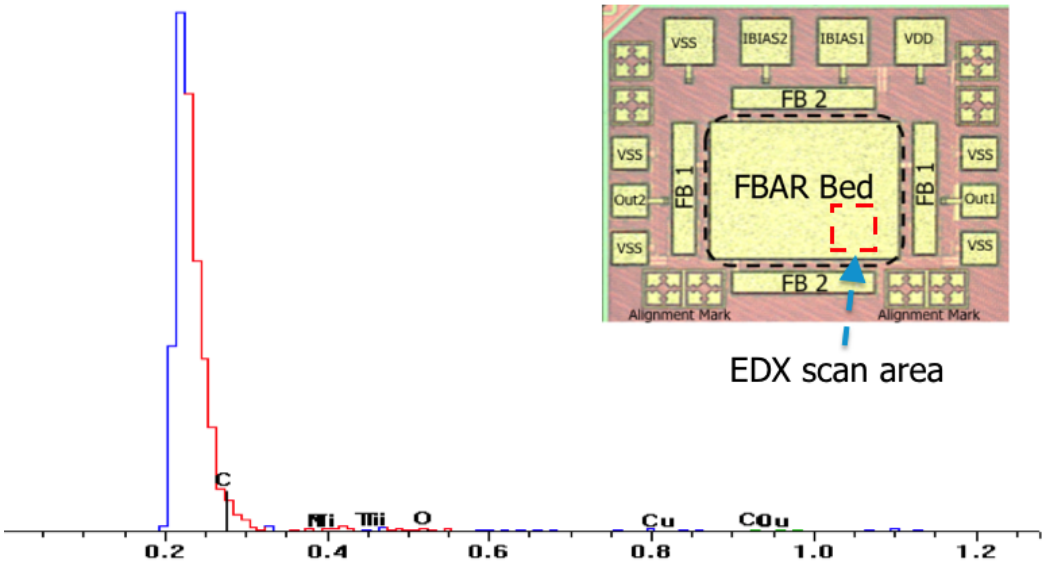
Shown in Figure 4.19 (a) is an EDX scan of an area top metal on the 65nm die as received from foundries. The EDX spectrum shows peaks corresponding to the aluminum (Al) /copper (Cu) metallization silicon (Si), nitrogen (N) and oxygen (O) peaks corresponding to the polyimide and oxide/nitride coatings. The polyimide is primarily a polymeric, carbon (C) based compound, however, the intensity of the carbon peak is not a reliable indicator since there is an abundance of carbon adhesive tape in the EDX measurement system and moreover, due to the X-ray energies available in the measurement system used, carbon and lighter atoms are difficult to detect accurately. Furthermore, the entire EDX spectrum only gives a qualitative assessment of the layer composition since the X-rays have non-negligible penetration (even at low beam energies) into the underlying back-end layers. As a result, the measured spectrum is a composite plot of the signals from several microns of CMOS

back-end. Nonetheless, EDX provides a valuable tool to assess the progression of the polyimide etching. With continued etching of the polyimide, a very prominent copper (Cu) peak is observed in Figure 4.19 (b). This corresponds to removal of the polyimide and exposing of the copper top metal.

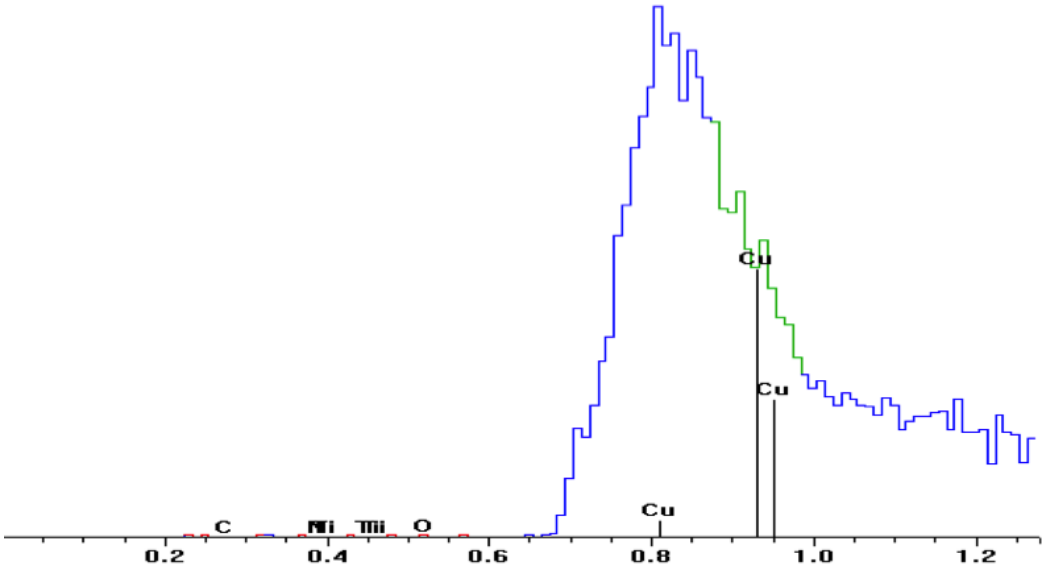
To conclusively rule out the removal of polyimide coating, wet etching of the copper top metal layer was applied to the chips. If the polyimide coating was indeed appropriately etched, the top metal would be easily removed when the chip is dipped into a wet etchant bath. Regions still coated in polyimide showed negligible etching even after long durations in the etchant bath. Wet etching of top metal will be discussed in more detail in the next section.

In addition to using foundry passivation bondpads, passivation etching is also required to gain access to large sections of top metal. Typically foundry design rules prevent the designer from requesting glass-cuts for traces much large than the bondpad area. Therefore, large metal traces will arrive form foundry coated with the full passivation stack. Such large traces maybe include contact pads used to connect the fabricated resonator ot the underlying CMOS circuitry. The same applies to the FBAR-bed area which is $> 200\mu m \times 200\mu m$ which is too large for a foudnry glass cut.

The two CMOS dies used in this work presented very different back-end topologies. As a result, two different passivation etches were developed. One for the thinner passivation coating ont eh 65nm chip and a more aggressive multi-stage etch process for the 180nm chip due to its thicker passivation coating. The recipe contained SF_6/O_2 in a ratio of 25% : 75% with etching taking place in 30 second intervals at 20 mTorr separated by 1 minute cooling cycles in an argon atmosphere at 60 mTorr. In order to prevent charge-induced damage to the underlying CMOS circuitry, the final several 100nm of passivation are etched in a slow manner with low RF power supplied to the plasma. The low plasma power reduces the amount of ions and electrons generated in



(a)



(b)

Figure 4.19: Passivation etching of 65nm IC: (a) EDX scan before passivation etching showing strong carbon peak (b) EDX scan after passivation etching showing strong copper peak due from top metal.

the plasma and also reduces the energy with which ions and electrons are accelerated towards the die surface under etching.

4.7.3.2 180nm Bondpad Passivation

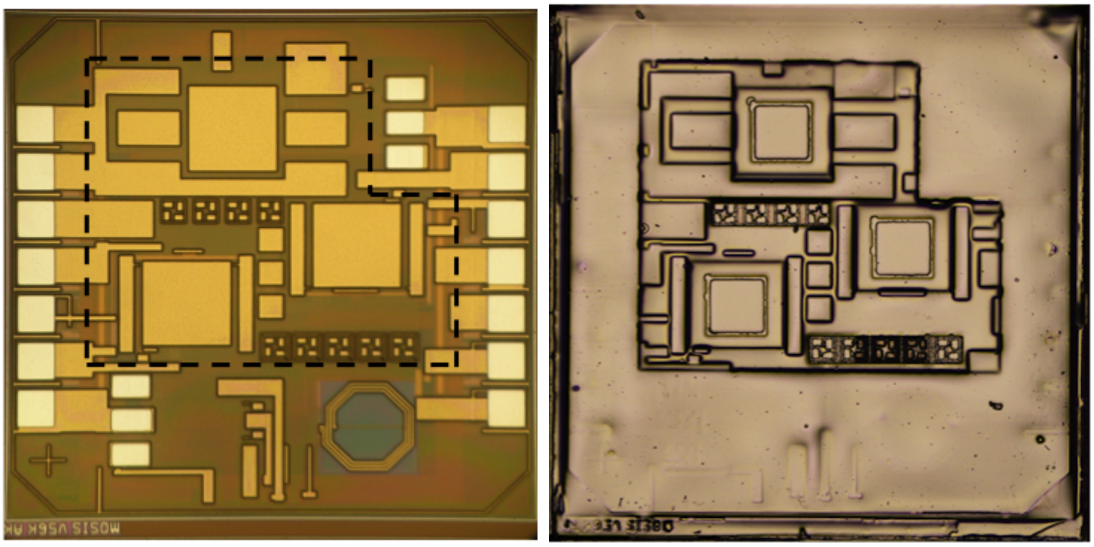
As mentioned before, the bondpads of the 180nm IC were exposed using foudnry glass-cuts to enable teseting upon receipt from foundry. Therefore, as opposed to the 65nm IC, it was necessary to deposit a passivation coating on the bondpads prior to fabrication. Once again, the choice was made to use SU-8 3005 as a protective coating. SU-8 can resist developer and etchants and can be etched easily, after FBAR fabrication, using the recipe developed for polyimide passivation etching. Equally important is the ability to lithographically pattern SU-8 Shown in Figure 4.20 (a) is a die photo prior to passivation. In Figure 4.20 (b), the SU-8 passivated die is shown. Due to the optical transparency of SU-8, the die is coated in blanket aluminum to increase the contrast between the die surface and SU-8 passivation. As can be observed, the outline of the inductor and bondpads are no longer visible due to the successful reflow of the SU-8 into the bondpad cavities and glass-cuts.

Once again, EDX was used to optimize the passivation etch. Figure 4.21 shows EDX scans before and after successful passivation etches. Here, aluminumis the top metal material. Therefore, the etching of the polyimdie passivaiton is accompanied with a strong increase in the aluminum (Al) peak relative to the carbon (C) peak intensity.

4.7.4 Bed Etch

4.7.4.1 65nm Bed Etch

As mentioned previously, low surface roughness ($< 6nm$) is crucial to fabricating high quality factor acoustic resonators. As received dies exhibit poor surface roughness



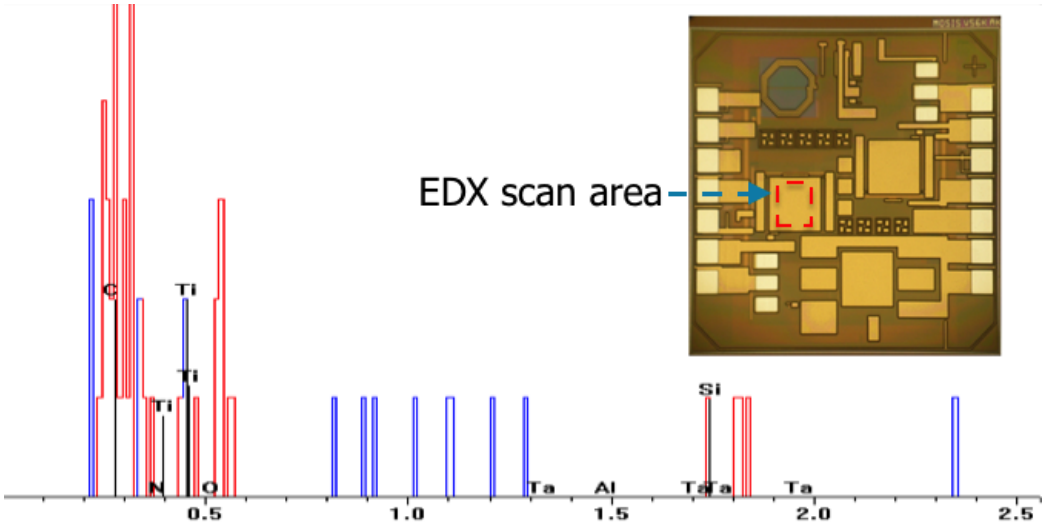
(a) (b)

Figure 4.20: 180nm pad protection: (a) Die before pad protection showing area to be coated in SU-8 (b) Die following SU-8 pad protection. The die is coated in blanket aluminum to allow observation of pad protection ring.

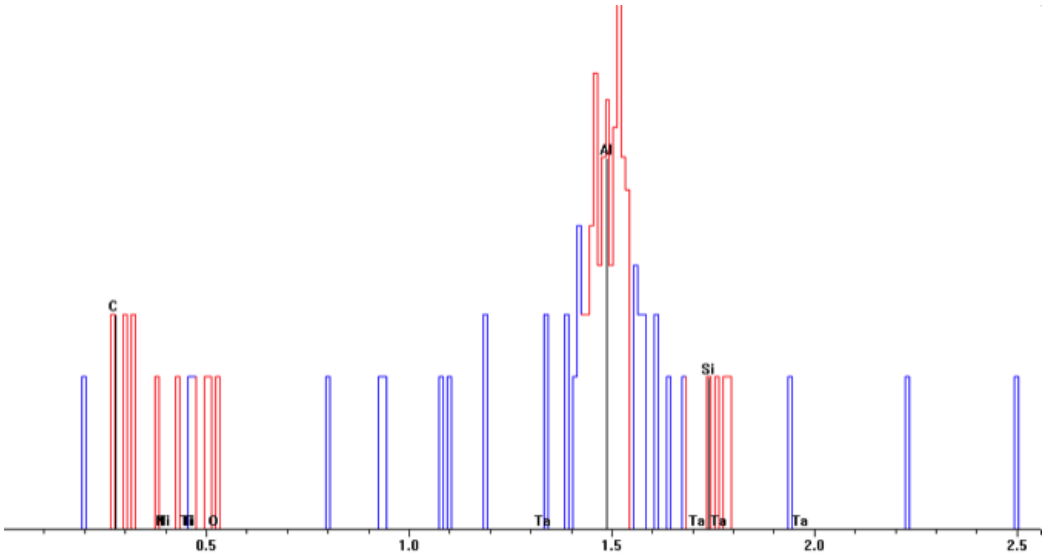
in the range of 12-20 nm. Shown below are atomic force microscopy scans of a $15\mu m \times 15\mu m$ area on the back-end passivation layer of both the 180nm die and the 65nm with corresponding RMS roughnesses of 20 nm and 12.4 nm respectively.

A possible solution to reduce surface roughness is to leverage the high-quality planarization that is applied in most modern CMOS processes. Chemical mechanical planarization (CMP) is crucial in the patterning of copper interconnect layers and is applied to the planarization of inter-metal dielectrics in order to improve lithography yield and eliminate large step heights that can lead to poor electrical contact and shorting across the step [39].

All but the top most metal and dielectric layer of a CMOS die is planarized via CMP. Therefore, the target was to build FBARs on the planarized dielectric layer directly underneath the top most CMOS metal layer. In order to preserve the



(a)



(b)

Figure 4.21: Passivation etching of 180nm IC: (a) EDX scan before passivation etching showing prominent carbon peak (b) EDX scan after passivation etching showing higher aluminum peak strength compared with carbon. This corresponds to the aluminum top metal.

pristine quality of this build surface, it is necessary to mask the layer from dry and wet etching. The approach adopted was to design the layout with an electrically isolated perimeter of top metal to demarcate the build area for the FBAR resonators. The top metal mask is exposed by passivation etching and subsequently removed using a wet-chemical-etch to expose the underlying planarized dielectric layer. This approach is superior to that where the build area is directly underneath the back-end passivation without being interrupted with the top metal. Dry etching-etching techniques, despite their high precision and feature transfer fidelity, generally exhibit moderate to poor etch selectivity for different materials. Moreover, the energetic "soup" of ions and electrons present in plasma dry etching leads to roughening of underlying surfaces that could degrade the quality of the resonator build surface. Wet chemical etchants however, exhibit very high selectivity and impart negligible roughness degradation on surfaces to which they are selective. It is worth noting that wet-etches of CMOS back-end passivation require the use of a number of harsh chemicals such as hydrofluoric acid and hydrogen peroxide require. Therefore, a dry etch was preferred for the back-end passivation etching.

The 65nm die uses copper for the top metal. As per the foundry informtion, the top metal is directly coated with passivation coating. However, in practice, there is a thin diffusion barrier layer separating the passivation and metal layers. Aluminum and copper, by virtue of their physical properties, tend to diffuse into surrounding dielectric and semiconducting layers. In the worst of cases, this can leads to electrical shorts as the metal layers "spike" into the dielectric/semiconducting layers. To address metal diffusion, a thin conducting layer with low diffusivity is wrapped around the copper and aluminum metal layers to prevent diffusion into the surrounding structures [98]. The most commonly used diffusion barriers in CMOS processes are titanium-nitride (TiN) and tantalum-nitride (TaN) [99].

The diffusion barrier prevents wet etchants from accessing the top metal layers to

remove the metal and expose the underlying planar dielectric. This leads to a drastic reduction in the etch rate of the metal etchant requiring hours instead of minutes to perform any appreciable etching of the metal. Even then, the etch proceeds non-uniformly as shown below, etching primarily in the large open feature areas and leaving behind "tents" near the feature edges whereby the etchant undercuts the metal layer leaving behind a diffusion barrier film as shown in Figure 4.22.

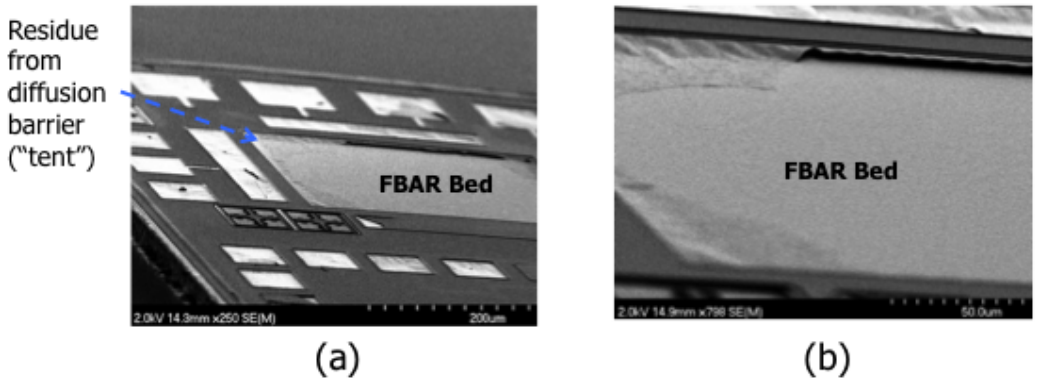
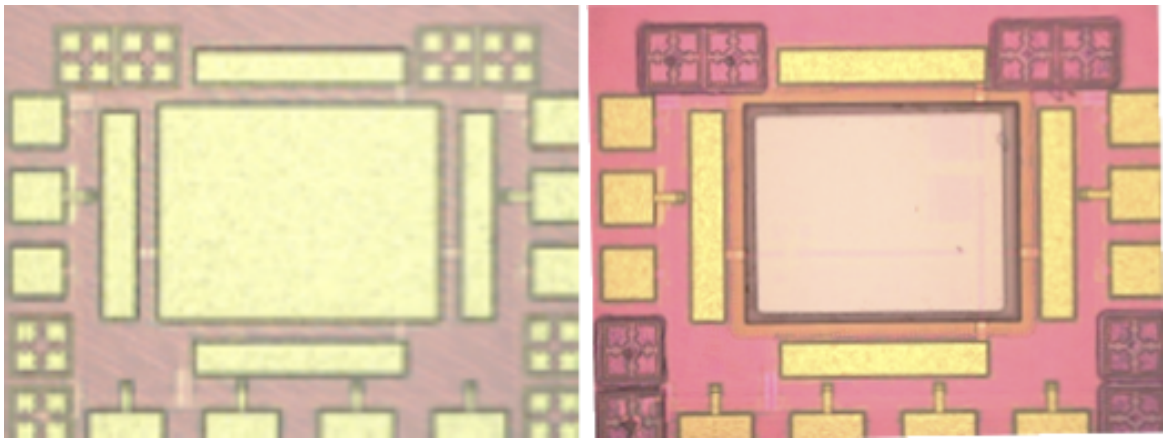


Figure 4.22: Resist cracking: (a) SEM of diffusion barrier tent after wet-etching (b) Zoomed-in SEM of diffusion barrier tent (c) Optiacl image of poor top metal etching due to diffusion barrier.

A number of approaches were adopted to remove the diffusion barrier. At the time of first experimentation, there was no access to EDX measurements and the exact chemical nature of the diffusion barrier was unknown. Since diffusion barriers are typically 10's of nm in thickness, ion milling was used in an attempt to etch the barrier layer. Ion milling utilizes inert plasma containing heavy ions, argon in this case, to bombard the surface to be etched and physically remove material by momentum transfer to the surface. As such, ion milling does not involve a chemical component and can be used to etch a variety of different materials regardless of their chemical structure. However, ion milling was found to be ineffective since it leads to damage of the underlying dielectric layers and also leads to re-deposition of "milled"

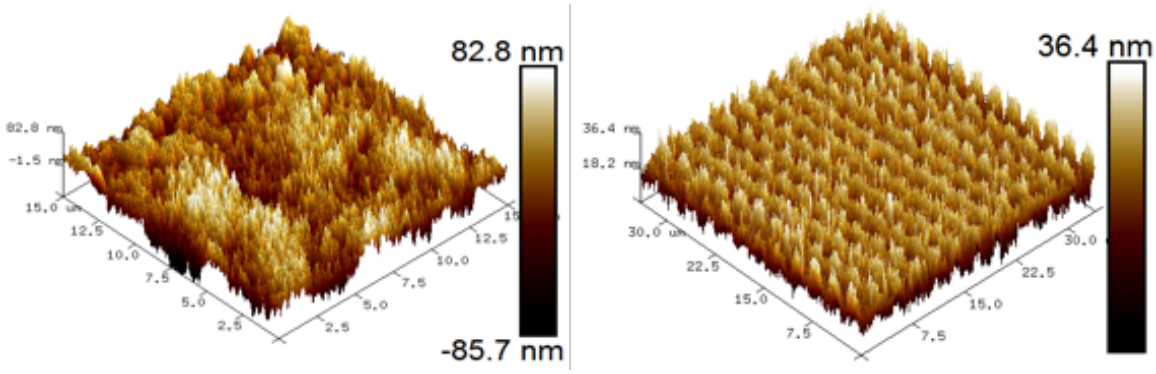
material onto other areas of the substrate.

Successful etching of the diffusion barrier was achieved by using short chlorine plasma etch. Chlorine plasma s have been demosntrated to etch TiN and TaN films in an "ion-enhanced" chemical etch [100, 101]. Here the etch is mainly chemical with the chlorine reacting with the TiN and TaN to form volatile byproducts. For the 65nm IC, the diffusion barrier was fully removed through a 2min ICP etch in pure chlorine (Cl_2). The etch was performed at 12 mTorr in an Oxford PlasmaPro System 100 Cobra etching system in 30s etching cycles followed by 30s of cooling in pure argon at 20 mTorr. Following diffusion barrier etching, the copper top metal is removed by immersion in Transene APS-100 copper etchant for 4mins at 60°C. Shown in Figure 4.23 is the successful etching of the diffusion barrier and subsequent top metal etching of the FBAR bed in a 65nm die. This is accompanied with a corresponding reduction in root-mean-square (r.m.s) roughness of the die surface from 20 nm to 5.2 nm as shown in Figure 4.24. This corresponds to a significant improvement which will exhibit a strong influence on the ability to fabricate FBARs with performance comparable to glass-based devices.



(a) (b)

Figure 4.23: (a) Chip as received (b) Top metal removed in planarization etch



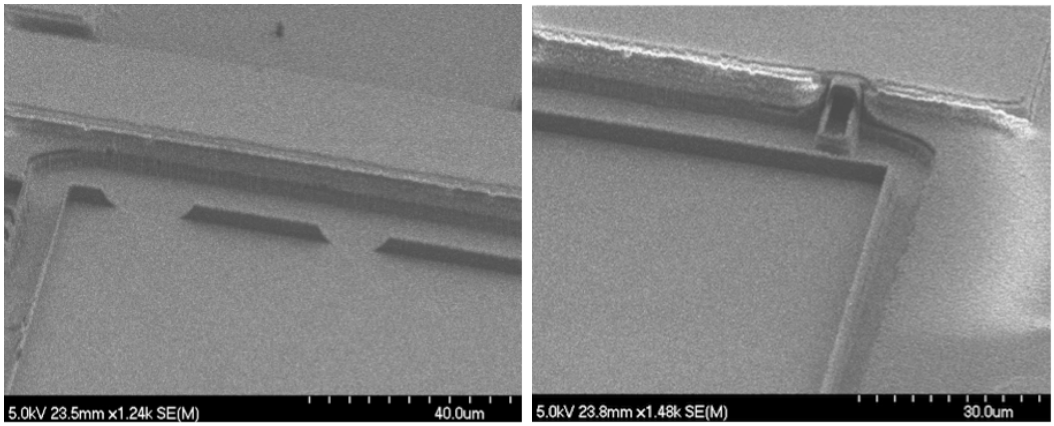
(a) (b)

Figure 4.24: 65nm die surface planarization: (a) AFM scan of die surface before planarization etch with r.m.s roughness of 20nm (b) AFM scan of die surface after planarization with r.m.s roughness of 5.2 nm.

4.7.4.2 180nm Bed Etch

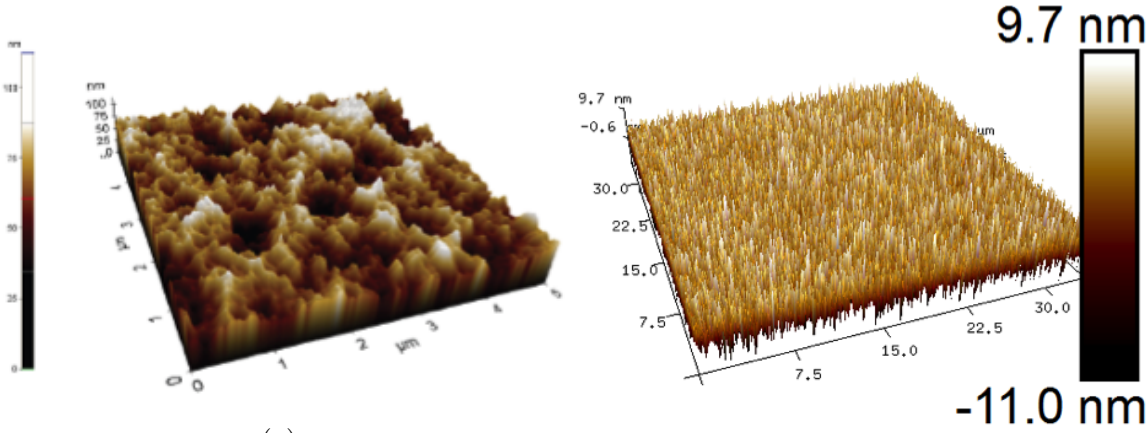
Bed etching the top metal of the 180nm IC differed in the use of aluminum etchant (Transene TFA etchant) to remove the aluminum top metal as opposed to the copper metalization of the 65nm IC. Furtheremore, there appeared to be no diffusion barrier above the 180nm top metal which simplified the etching. However, SEM analysis following aluminum etching revealed the presence of a "fence" of TiN surrounding the periphery of the FBAR bed (Figure 4.26. This fence complicates reist spinning and can lead to shorting of the FBAR electrodes. The fence did not exhibit any noticeable etching in aluminum etchant. Chlorine dry etching of the TiN fence prior to removal of the aluminum was not successful. This is likely due to the narrow width of the fence ($\sim 2\mu m$) which presents a very small cross-section for the chlorine etching plasma. An alternative approach that was utilized involved ultrasonic sonication of the 180nm dies following aluminum etching. The sonication resulted in collapse of the fence which allowed for successful resist spinnng. Bed etching of top metal in the 180nm die led a reduction in r.m.s surface rougness from 12.4nm to 2.3nm which is

considerably smaller than the surface roughness of the 65nm IC.



(a) (b)

Figure 4.25: 180nm bed etching showing "fence" remaining after etching.

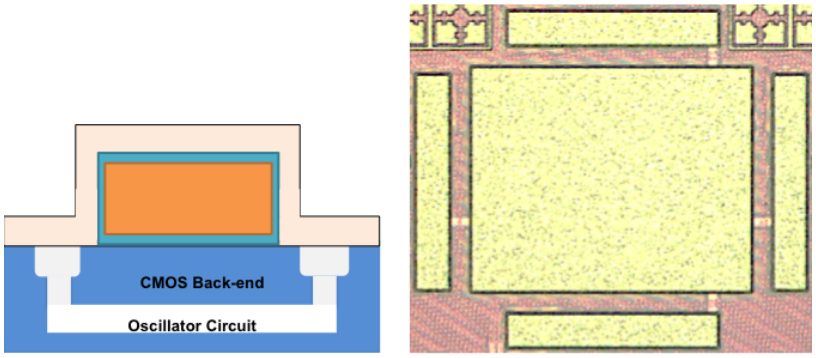


(a) (b)

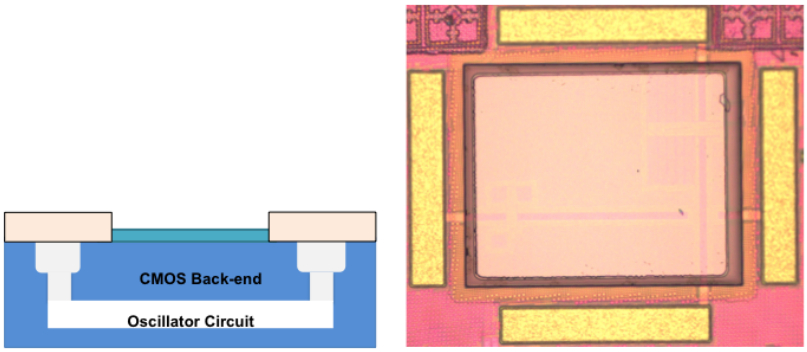
Figure 4.26: 180nm die surface planarization: (a) AFM scan of die surface before planarization etch with r.m.s roughness of 12.4 nm (b) AFM scan of die surface after planarization with r.m.s roughness of 2.3 nm.

4.8 Overall Process Flow

With smooth build surfaces attained, FBARs were fabricated on the CMOS dies. Process flow for the 65nm FBAR fabrication is as shown below in Figure 4.29. After bonding the foundry die (a) to the carrier substrate, the fabrication commences with etching of the polyimide passivation, followed by diffusion barrier and FBAR bed etching (b). WIth a planarized build surface, The first set of mirror layers is sputtered and patterned (c). Now, the mirror is blanketed with SiO_2 as the final mirror layer. This also prevents shorting of conductive mirror layers with the FBAR electrodes in subsequent depositions. Now, the bottom gold electrode is deposited which serves as the seeing layer for the ZnO piezoelectric layer (e). The FBAR structure is completed with deposition of the gold top electrode. All that is left, is to access the top metal contacts to the oscillator circuit using passivation etching (a), and to deposit thick aluminum contacts which connect the FBAR to the circuit. At this point, the CMOS-FBAR structure is completed and ready for measurment. The 180nm process flow follows similar lines with the addition of an SU-8 patterning step at the beginning of the process for protecting the bondpads.



(a)



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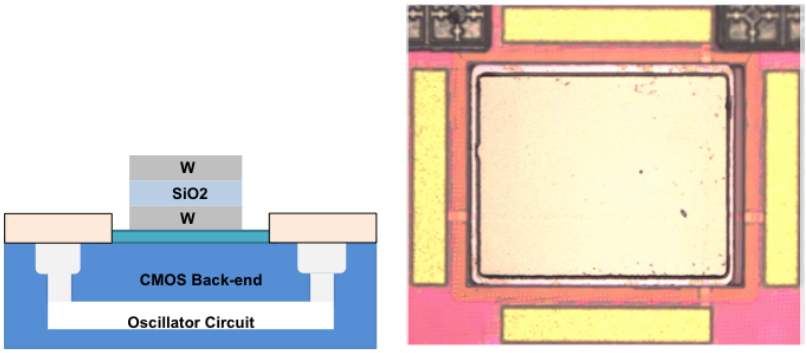


(c)

Figure 4.27: 65nm FBAR Fabrication Process Flow: (a) Die before processing (b) Bed etching (c) Deposition of first mirror layers.

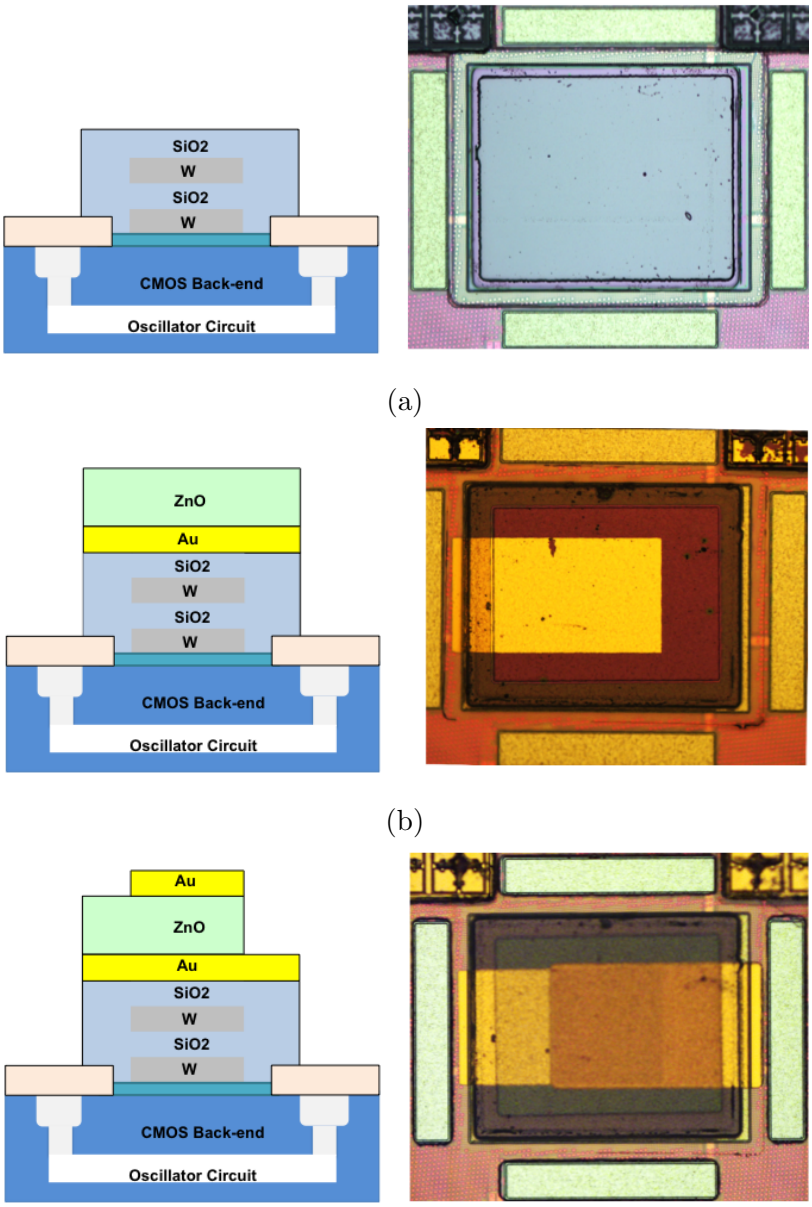
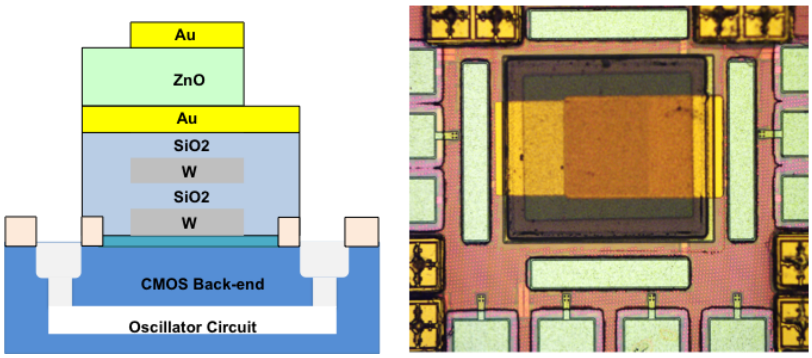
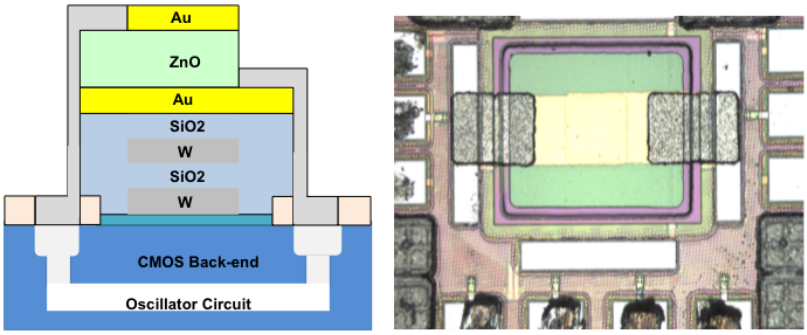


Figure 4.28: 65nm FBAR Fabrication Process Flow: (d) Blanket SiO_2 to prevent electrode shorting (e) Deposition and patterning of gold bottom electrode and ZnO piezoelectric layer (f) Deposition and patterning of gold top electrode.



(e)



(f)

Figure 4.29: 65nm FBAR Fabrication Process Flow: (g) Passivation etch to access underlying metal pads (h) Deposition of aluminum contact extension for connecting FBAR to CMOS circuit.

4.9 65nm Results

4.9.1 Measurements

As mentioned in previous sections, both ICs were designed to be tested using RF coplanar probing. The 65nm IC requires 150μm RF coplanar probes (Cascade Microtech) for measuring the oscillator output and A 4-pin DC eye-pass probe (Cascade Microtech) for applying the supply voltage and biasing signals. Shown in Figure 4.30 is the IC during probing of the 100$\mu m \times 100\mu m$ FBAR oscillator.

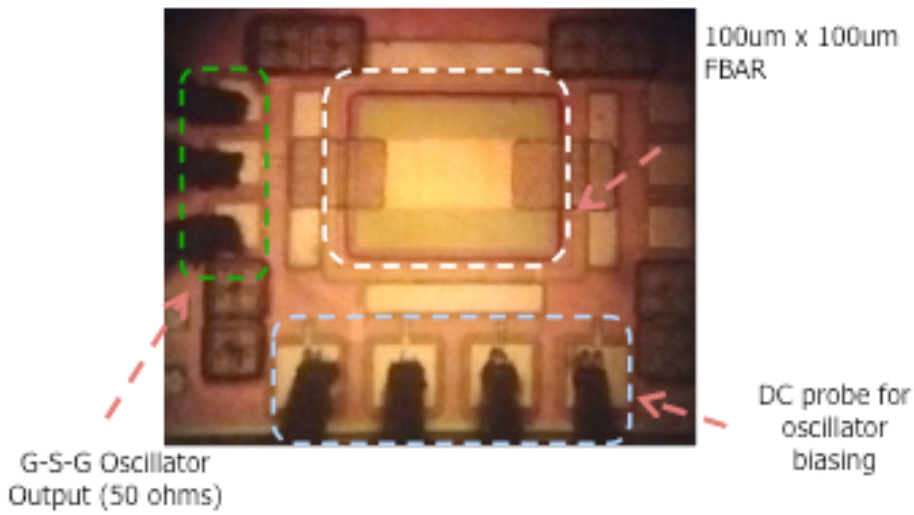
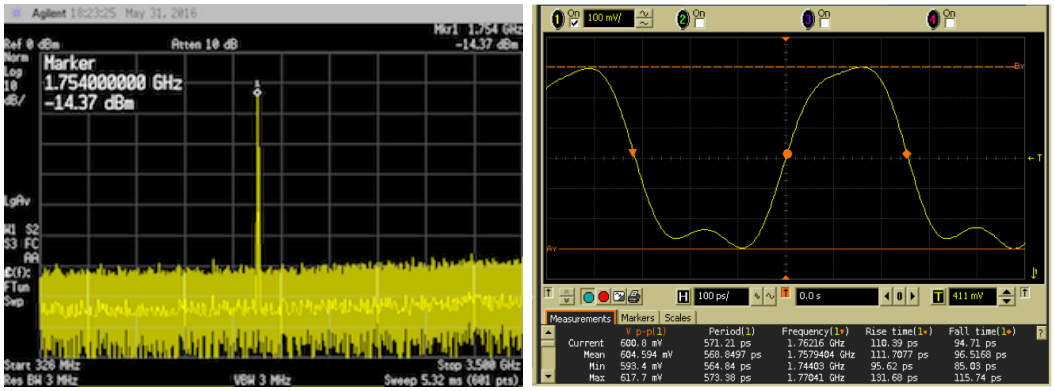


Figure 4.30: RF probing of 65nm IC with monolithically fabricated 100$\mu m \times 100\mu m$ FBAR.

The oscillator output was measured using an Agilent spectrum analyzer. The measurement indicated an oscillation at 1.754 GHz. The measured output swing at 1.2 V supply voltage and a 9 mA bias current was 900 mV. The results are shown below in Figure 4.31.

The stability of the oscillator was assessed using phase noise measurements. Shown in Figure 4.32 is the phase noise plot of the 100μm oscillator output at a supply voltage



(a) (b)

Figure 4.31: FBAR oscillator measurements for $100\mu m \times 100\mu m$ FBAR: (a) Spectrum analyzer output (b)High-speed oscilloscope output.

of 1.1V and a bias current of 9mA.

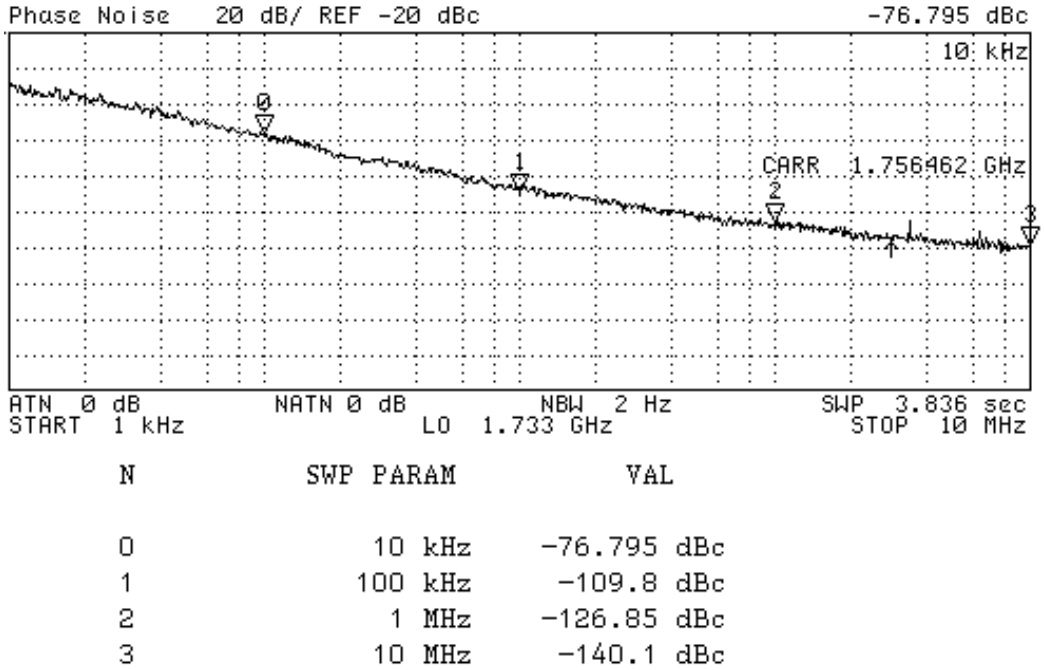
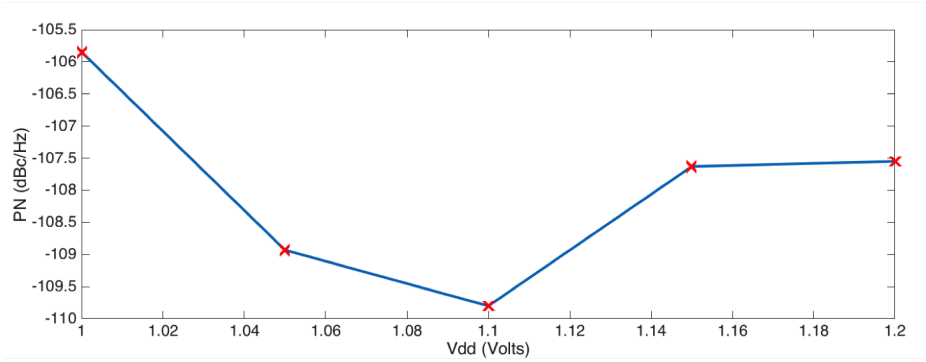
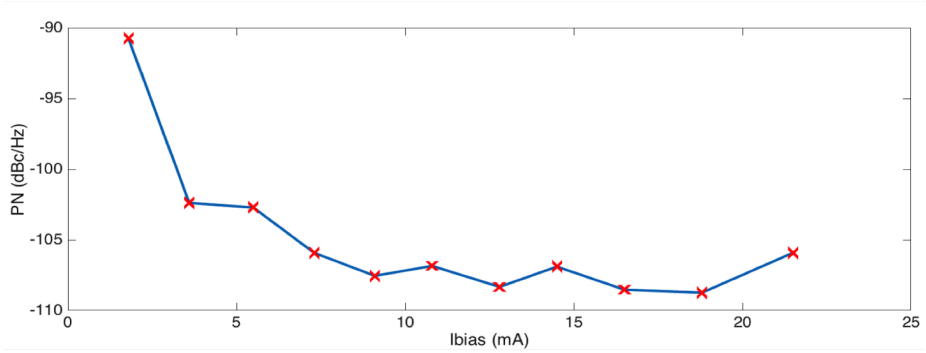


Figure 4.32: Phase noise of $100\mu m \times 100\mu m$ FBAR oscillator. This measurement was performed at a Vdd of 1.1 V and a bias current. $Ibias = 9mA$



(a)



(b)

Figure 4.33: Phase noise variation with bias: (a) Sweeping Vdd, (b) Sweeping Ibias.

4.9.2 FOM

Different oscillator circuits can be compared by computing a figure-of-merit (FOM) dependent on power consumption and phase noise at a particular carrier offset frequency. Lower the phase noise, lower the power consumption and the higher the operating frequency lead to higher FOM values corresponding to a higher perofmrnace oscillator. A comparison of the FOM of the 65nm-FBAR oscillator shown here with comparable oscillators in literature is shown in table.4.1. The FOM [102] is

Reference	f_{osc}	Power	PN(100 kHz)	FBAR	FOM
	GHz	mW	dBc/Hz		dB
[103]	1.9	0.3	-120	Off-chip	210.8
[104]	2.145	12	-124	Flip-chip	199.8
[105]	2.1	58.3	-120	Monolithic	188.8
[106]	5.46	4.59	-117.7	Monolithic	205.8
This Work	1.75	9.9	-109.8	Monolithic	184.7

Table 4.1: Comparison with other FBAR-based oscillators.

defined as:

$$FOM = 10log\left(\left(\frac{f_o}{\Delta f}\right)^2 \frac{1}{L\{\Delta f\}P}\right) \tag{4.4}$$

4.9.3 65nm Results Discussion

As shown in table.4.1, the oscillator demonstrates a lower figure of merit than off-chip FBAR based oscillators due to its high power consumption and approximately 10 dB higher phase noise than comparable FBAR oscillators at a $100kHz$ carrier offset. The large power consumption is to be expected based on the conservative design of the oscillator circuit (Figure 4.4). The lower phase noise compared with other FBAR oscillators can explained by observing the form of the phase noise in the $\frac{1}{f^2}$ region shown below [82]:

$$L\{\Delta\omega\} = 10log\left[\frac{2kT}{P_{sig}}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] \tag{4.5}$$

In [103], an output power of 6 dB corresponding to approximately 1.2 V peak-peak oscillation at 1.917 GHz was measured. With a phase-noise of 120 dBc/Hz at 100 kHz carrier offset. An external resonator of quality factor 1200 is used. Contrasting these

numbers with the 900 mV peak-peak swing of the 65nm FBAR-oscillator at 1.754 GHz and assuming a quality factor of 450 (based on glass device measurements), eq.4.5 yields a difference of 10.18 dB. This value agrees with the observed phase noise discrepancy. Therefore, it is clear that an increase in resonator quality factor can improve phase noise. In this work, the emphasis was on simplicity of the demonstration structure. However, a number of industrially prevalent structural optimizations [107] have been shown to improve the quality factor by up 200% and these can be applied to the FBAR-CMOS platform. Furthermore, a move to membranes devices [13] can lead to even larger improvements in resonator quality factor. Appendix A discusses work conducted towards enabling released devices on CMOS.

4.10 180nm Results

The limited die area of the 65nm IC did not allow for fabricating a probe-able FBAR on the same die to quantify the FBAR performance on its own. Therefore the oscillator results are used to assess the performance of the on-chip FBARs. A commonly used figure-of-merit (FOM) for comparing different oscillators is shown in eq.4.4. The FOM is calculated from the oscillation frequency f_{osc}, the DC power consumed in mW, and the phase-noise at a specified offset from the oscillation frequency. A higher FOM corresponds to a superior oscillator. Table4.1 compares the FOM of the 65nm CMOS oscillator with other FBAR oscillators published in literature.

As with the 65nm IC, FBARs were fabricated on both oscillator sites on the 180nm. Additionally, a probe-able FBAR was also fabricated on the die surface. Shown in Figure 4.34 is a microscope image of the processed chip just prior to etching the SU-8 protective ring on the bondpads.

Measurement indicated failure of the single transistor Pierce oscillator to start-up. The oscillator was primarily outputting a tone around 2 MHz which shifted signifi-

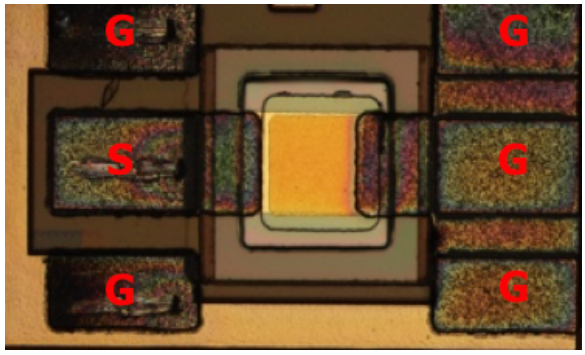


Figure 4.34: Microscope image of completed 180nm die prior to removing SU-8 protection on bondpad ring.

cantly in response to supply voltage tuning. The 3-inverter Pierce oscillator showed the same, supply sensitive tone around 2 MHz. However, there was an additional, much weaker tone around the target resonance frequency of 1.784 GHz as shown in Figure 4.35. This tone appeared to be independent of supply tuning as in Figure 4.36.

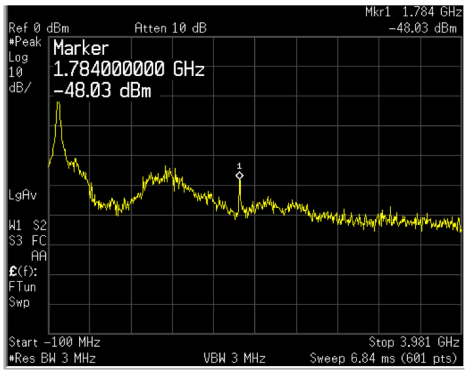
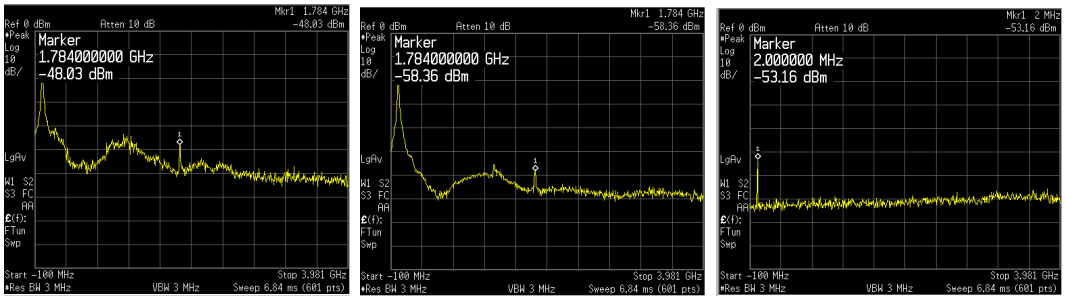


Figure 4.35: Output spectrum of 3-inverter oscillator at Vdd=1.2V.

In order to debug the oscillator fault, the probe-able FBAR was measured and fit to an electrical model to assess the integrity of the on-chip resonators. The resonator was fit to a lumped BVD model as shown in Figure 4.37. The lumped fitting indicated



(a) (b) (c)

Figure 4.36: Spectrum analyzer output of 3-inverter Pierce oscillator at: (a) Vdd=1.2 V (b) Vdd= 1 V (c) Vdd=0.8 V.

Q values comparable to those measured for resonators on glass and and somewhat lower and k_t^2 values as shown in table.4.2.

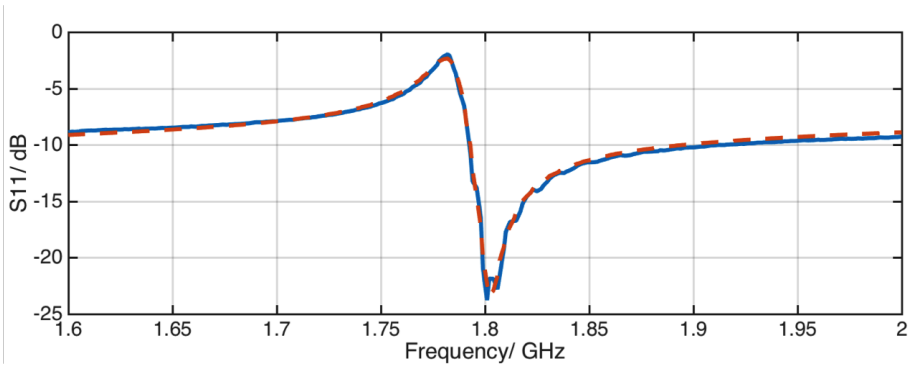


Figure 4.37: Fitting of 180nm probeable 100μ m$\times 100\mu m$ resonator to lumped model.

However, one peculiar observation from the lumped model fitting was the presence of a low-resistance shunt around 45Ω between the resonator terminals. The shunt manifested as an apparent hard-limit that prevents the resonator's impedance characteristic form exceeding 45Ω during anti-resonance. However, the behavior around series resonance appeared consistent with a properly functioning resonator of $R_m = 4.7\Omega$. This shunt resistance appears to interfere with the sustaining ampli-

	Gen4	Gen5	Gen10
Q	~ 500	~ 500	460
k_t^2	4.5%	4.5%	3.3%
$R_s(\Omega)$	0.3	5	0.4
$C_{sub}(fF)$	10	10	300
Q	5	5.3	4.7
Process	Pyramidal mirror and thick contact extension	Etched Mirror	On CMOS

Table 4.2: FBAR performance progression.

fier circuit and leads to a significant reduction in the negative resistance. This follows from the negative resistance equation in eq.4.1. This is the likely reason for the weak tone observed in the spectrum analyzer output of the 3-inverter Pierce oscillator.

Additionally, excessive parasitic capacitance to the substrate was found in the range of $300fF$. Shown in Figure 4.38 is the lumped model highlighting the parasitic substrate capacitance and shunt resistance. By reducing the parasitic substrate capacitance in the lumped model to $50fF$, the k_t^2 value was found to increase from 3.3% to 4.3%. The source of this parasitic is capacitive coupling through the topmost tungsten layer of the bragg reflector. More aggressive layout with shorter electrodes (and thus smaller electrode-mirror overlap area) can feasibly reduce the parasitic capacitance to the $50fF$ range. The probe-able FBAR requires large contact pads ($100\mu m \times 275\mu m$) for proving with RF coplanar probes. On the other hand, an FBAR contacting the underlying circuitry only requires small electrodes on the order of $50\mu m \times 10\mu m$) since no RF probes are immediately contacting the FBAR.

Therefore, it is reasonable to expect a significant reduction in parasitic capacitance in FBARs used for oscillators compared with the probe-able FBAR.

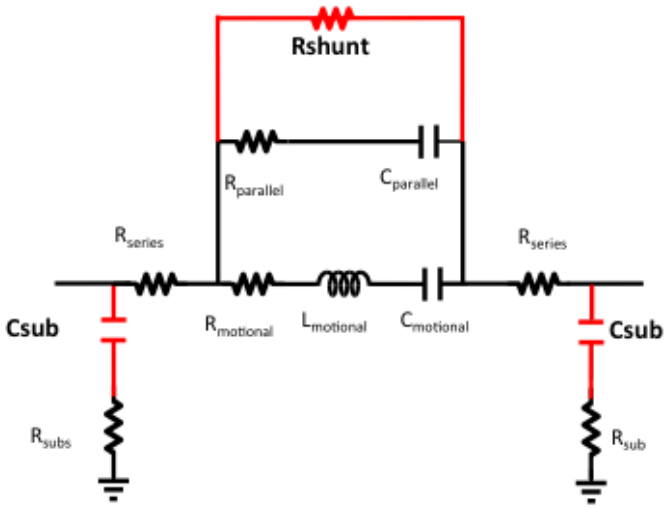


Figure 4.38: Highlighting of parasitic elements impacting resonator performance.

In an attempt to determine the source of the low-resistance shunt, the processed die was subject to scanning electron microscopy as shown below in Figure 4.39. Upon careful examination of the aluminum contact strap that bridges the FBAR to the underlying CMOS circuit (Figure 4.40(a)), a rough, jagged strip was found piercing the aluminum layer as seen in Figure 4.40(b). Based on the position of the rough features, it appears to be residue from incomplete removal of the diffusion barrier fence. Further optimization of the fence etch is necessary to achieve working oscillators in the 180nm design.

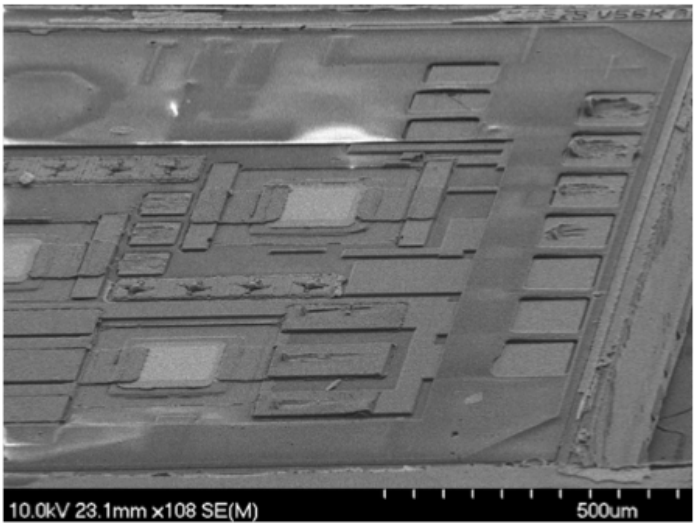
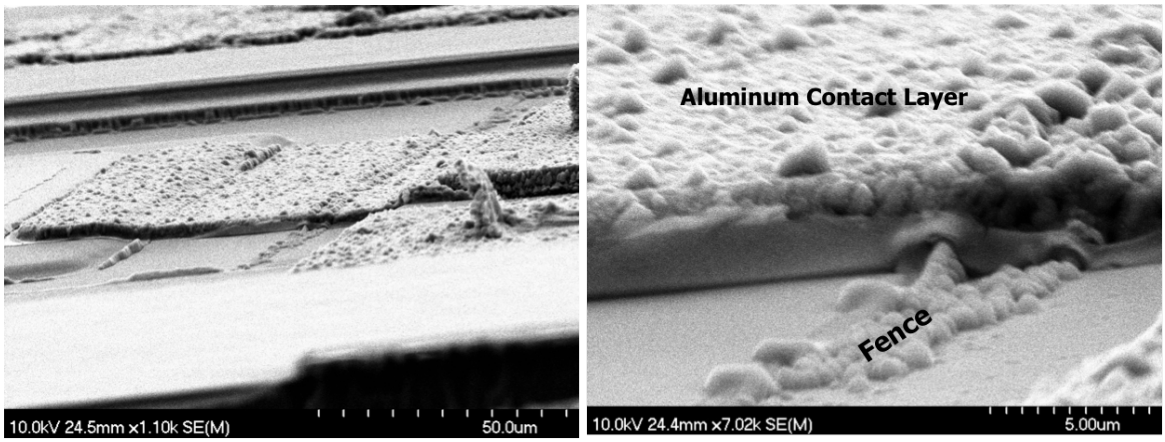


Figure 4.39: Scanning electron microscope (SEM) image of processed 180nm die showing fence.



(a) (b)

Figure 4.40: SEM images of fence.

4.11 Chapter Summary

This chapter outlined the design and implementation of FBAR-based oscillators using 65nm and 180nm CMOS IC dies. Design of the CMOS oscillator circuits was discussed

along with a description of layout-level techniques to simplify subsequent fabrication of FBARs on the CMOS surface. Among these was a specially developed technique for reducing surface roughness of CMOS die surfaces was presented. Additionally, processes were described to enable fabrication on small size CMOS dies ($2mm \times 1.7mm$ and $1.5mm \times 1.5mm$).

Electrical measurements of a working 65nm CMOS-FBAR oscillator were presented along with a discussion of the phase noise performance of the oscillator. Finally, electrical measurements of a stand-alone resonator fabricated on 180nm CMOS were fit to a lumped circuit model. The model was used to compare performance with a similar resonator fabricated on glass and outline possible sources of performance discrepancy.

Chapter 5

Conclusion

5.1 Summary of Results and Contributions

This thesis describes efforts to develop and implement a fabrication post-process for fabricating piezoelectric FBAR resonators in a monolithic fashion directly above foundry-sourced, small sized CMOS IC dies. The process commenced with the fabrication and characterization of stand-alone devices on glass substrates, followed by subsequent design of custom ICs in standard 65nm and 180nm CMOS processes and culminating in the demonstration of a working FBAR-CMOS oscillator.

Contributions of this work include :

- Development of techniques for handling and performing multi-layer photolithography on CMOS dies smaller than $2mm \times 2mm$. This die area is more than 400% smaller than that of previous die-based MEMS-CMOS integration efforts [35].
- A simple technique for significantly reducing the roughness of CMOS die surfaces for fabricating high-quality FBARs.
- The first demonstration of a monolithically integrated FBAR-CMOS oscillator in a 65nm CMOS process.

- Demonstration of the smallest size monolithically integrated FBAR-CMOS oscillator. The size denotes the combined area of the FBAR and CMOS core.

5.2 Future Work

Studying FBAR-CMOS Coupling

Due to time limitations, a thorough investigation of the coupling between the monolithically-fabricated FBARs and the underlying CMOS circuitry was not completed. This can be a subject of future work whereby the FBAR-CMOS coupling is interrogated by assessing the phase-noise and spectral content of the oscillators in the 180nm IC demonstrator with the FBARs simultaneously activated and de-activated.

Oscillator Design

For practical reasons, the oscillator designs used in this work were conservative to ensure a successful FBAR-CMOS integration demonstration. There is a large body of work relating to the design of low-power and low phase noise oscillators with several works focusing on the unique aspects of FBAR oscillator design [108]. Future work can leverage these techniques to improve oscillator performance.

Membrane Devices

Extending the processing techniques described here to membrane-based FBARs can allow the fabrication of higher Q resonators and more importantly enable use of lateral structures with lithographically defined frequencies. The adoption of lateral structures will provide frequency diversity to enable applications such as switchable filters and integrated reconfigurable oscillators [57] where each resonator or set of resonators operate at a different frequency. Current work in the same research group

is being conducted towards this goal and appendix A provides an account of successful attempts for fabricating low-stress membranes.

Tunable Filters

There is currently increasing interest in tunable SAW and BAW wave filters [29]. The most successful demonstrations of tunable filters have relied on the use of external tunable capacitors based on ferroelectric dielectrics. However, monolithic integration of BAW devices with CMOS circuitry as demonstrated in this thesis can allow for the use of large CMOS switched-capacitor banks, an as of yet unexplored approach, which can provide a larger degree of tunability and control of filter response.

5.3 Concluding Remarks

It is the hope of the author that the techniques presented in this thesis can lead to wider demonstrations of CMOS-MEMS resonator integration to enable experimentation with new circuit architectures that can simultaneously leverage the advantages of CMOS transistors and MEMS resonators.

Appendix A

Zinc-Oxide Stress Compensation for Released FBAR Fabrication

A.1 Introduction

The FBAR devices demosntrated in this thesis were all solidly mounted and fabricated on an acoustic bragg reflector. However, moving to a released structure whereby the FBAR is fabricated on a membrane can provide higher quality factors and k_t^2 values than attainable with a solidly mounted device. Furthermore, a released device would involve a smaller number of layers during fabrication and can provide a wider bandwidth , since the air cavity provides a much broader response in frequency compared with a bragg reflector which is band-limited as dictated by thicknesses and material properties of the reflector layers [12], [10]. The key challenge with released devices is compensation of membrane stress. Since a membrane is not fully anchored, any excess stress will lead to a compensatory deformation of the membrane in order to release the stress. If the magnitude of the stress is too large, the membrane can buckle and crack. In fact, stress control in membranes was one of the challenges that plagued early development of FBAR devices in the late 90s [13].

A.2 Origins of Thin-film Stress

Nearly all thin films possess some degree of residual stress due to the mismatched thermal expansion coefficients between the film and underlying substrate, lattice mismatch whereby there are defects in the crystal structure of the material whereby an atom can out of place or due to stress induced by the growth process itself. Thermal expansion mismatch is an example of extrinsic stress which results from factors external to the film. Crystal defects are an example of intrinsic stress contributors which reflect the internal structure of the growing film. In most cases, thermal stress is uniform throughout the film whereas intrinsic stress is non-uniform and leads to a stress gradient across the thickness of the film. One common way of reducing intrinsic-stress effects involves thermal annealing at high temperatures (600C) [109]. However, this method cannot be applied in this work since the thermal budget limits processing temperatures Furthermore, the stress can be tensile (positive) where the film is the particles in the film are under tension, or compressive (negative) where the stress leads to bunching of the film particles. Shown below is a graphic representation of film stress induced by thermal expansion mismatch between and substrate. In (a), the growing film shrinks relative to the substrate. This leads to a bending moment or torque on the substrate which results in strain. If the substrate is free to move, and since the film is anchored to the substrate, the structure will bow upwards to counteract the bending moment. Analogously, the film will bow downwards if the film is under compressive stress. [110], [111], [39]

In a released FBAR, the piezoelectric layer is usually the thickest layer and consequently the main contributor to residual stress in the completed stack. RF sputtered Zinc Oxide, which is the piezoelectric used in this work, generally exhibits very large stress values ($1GPa$) which are not compatible with MEMS device and membrane fabrication [112]. The intrinsic stress of ZnO is primarily due to oxygen deficincies in the film whereby a stoichiometric imbalance results from having more zinc atoms

than oxygen atoms. [113], [114], [115]. An increase in sputtering pressure in an oxygen environment tends to reduce the film stress due to the incorporation of oxygen atoms that compensate the oxygen deficiencies.

Film stress is usually measured quantitatively by depositing the desired film on a silicon wafer and measuring the change in wafer curvature before and after film deposition. At the time of this work, such an instrument was not available. Furthermore, wafer curvature measurement only provides a large area, averaged measurement of stress of the enitre wafer and does not consider local fluctuations across the sample. The average stress measurement also does not allow discerning of stress gradients across the film. Therefore, as a tool for stress-assessment, released cantilever beams were used as shown in Figure A.1. The film under test is deposited and patterned in the shape of a cantilever. Following release of the cantilever, the film will then either bend upwards or downwards to release the stress gradient across the film.

The RF sputtered films in this project exhibit a compressive stress gradient with the film becoming less compressive with thickness. As a result, ZnO cantilevers tend to curl upwards. Shown below are ZnO cantilevers deposited at 2mTorr and 20mTorr. It is clear from the beam deflections that the higher pressure case exhibits lower overall stress. However, the resulting stress value was still too large and led to cracking of clamped beam structures fabricated using these ZnO conditions.

Ruling out high temperature anneals due to thermal budget constraints, an alternative approach was chosen to compensate the stress in the ZnO films. Here, the ZnO would be deposited above silicon nitride (nitride) films deposited using plasma-enhanced-chemical-vapor-deposition (PECVD). PECVD nitride films are generally tensile in nature. Stacking a compressive zinc oxide film atop a tensile nitride film of comparable stress magnitude can lead to composite film that is low-stress or even stress-neutral. Moreover, PECVD provides a number of different process parameters that can be tuned to engineer the nitride stress to the desired value. As shown in

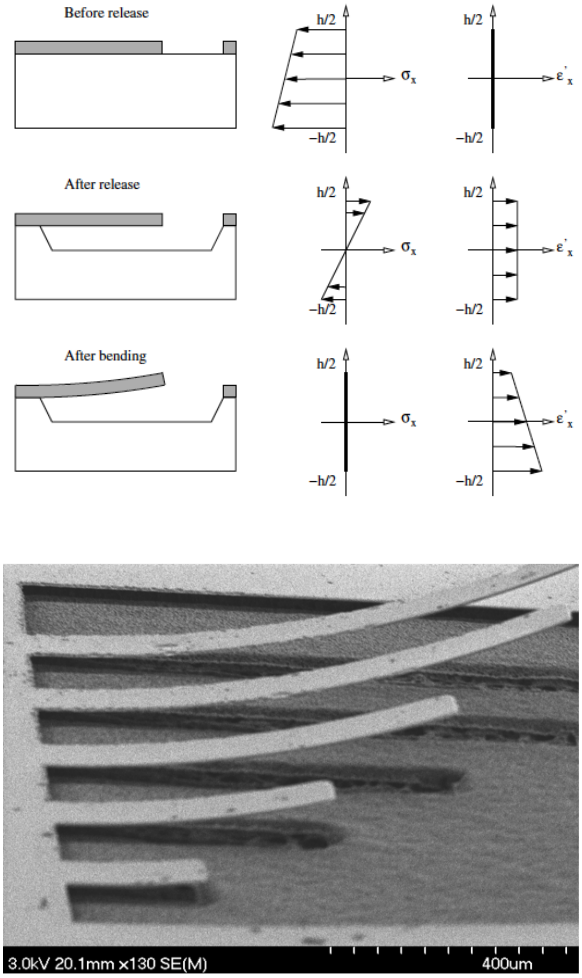
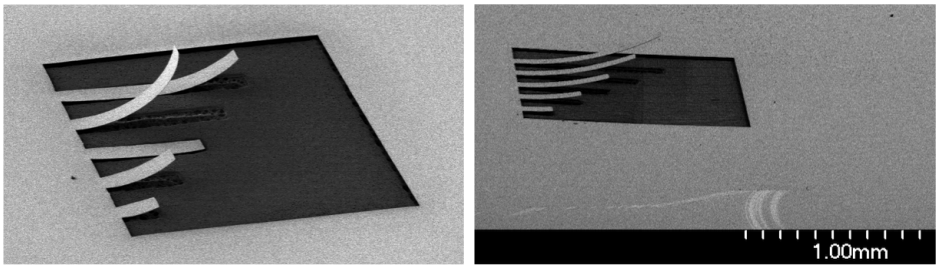


Figure A.1: Cantilever fingers for measuring film stress

the Figure A.3, the stress of PECVD nitride films exhibits a strong, almost linear dependence on the deposition pressure and the duty-cycle of the high-frequency plasma source [116]. Furthermore, the thickness of the nitride film serves as an additional control parameter.

Initial ZnO/Nitride stacks exhibited very high tensile stress overall leading significant upwards bending of the cantilever beams.

By adjusting deposition parameters to 100% high-frequency duty cycle and a deposition pressure of 900mTorr, the direction of finger curvature was reversed with

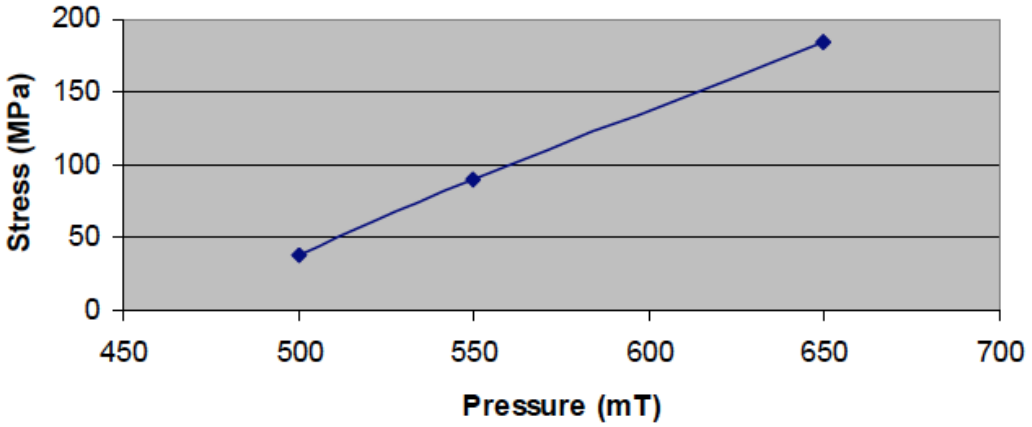


(a) (b)

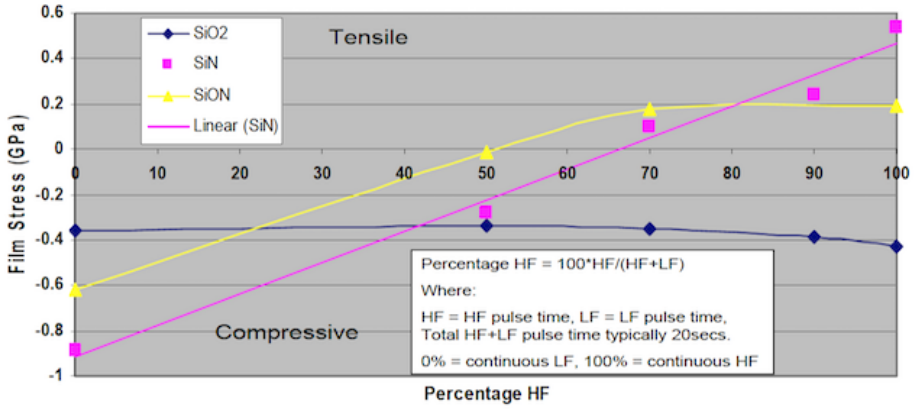
Figure A.2: ZnO stress at different deposition pressures: (a) 2 mTorr (b) 20 mTorr.

a noteicably smaller deflection than in preivous cases.

Future work will involve further optimization of the PECVD nitride thickness to obtain even lower stress layers for implementing membrane devices. This can enable the fabrication of membrane-based FBARs with higher performance than the Bragg reflector devices.



(a)



(b)

Figure A.3: Controlling nitride stress: (a) PECVD nitride depends linearly on deposition pressure (b) PECVD nitride stress becomes more tensile with increasing high-frequency pulse time [116].

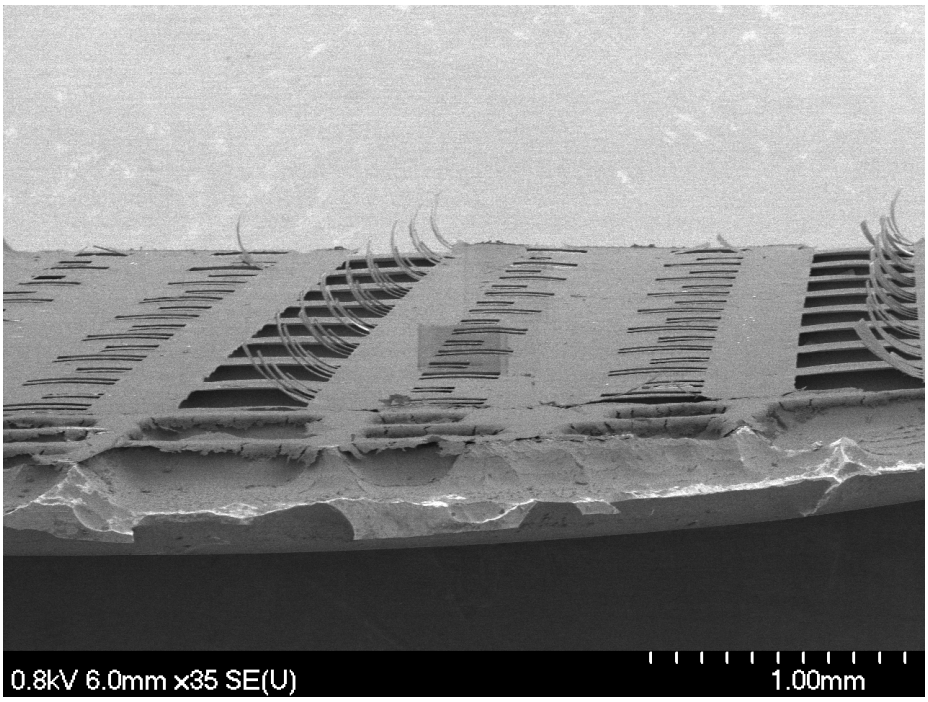
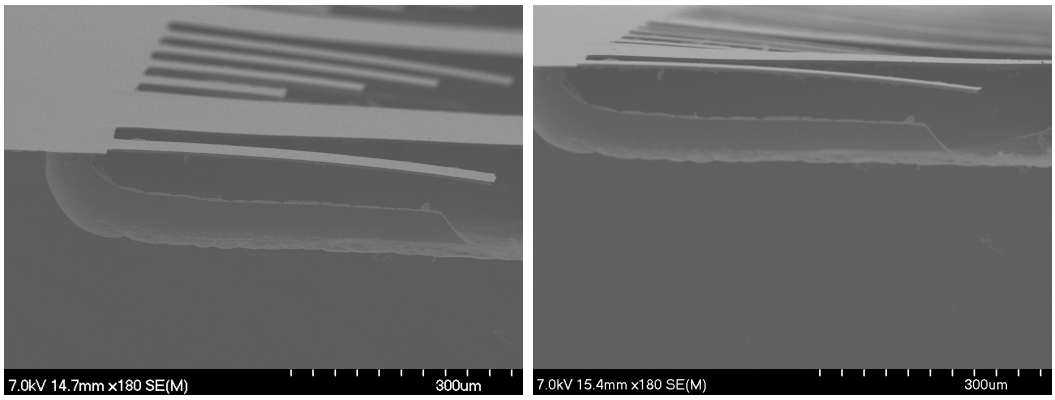


Figure A.4: Released nitride fingers showing large tensile stress



(a) (b)

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U. Seckin, H. Firouzkouhi, B. Saeidi, H. Akyol, Y. Choi, A. Mahjoob, S. D'Souza, C.-Y. Hsieh, D. Guss, D. Shum, D. Badillo, I. Ron, D. Ching, F. Shi, Y. He, J. Komaili, A. Loke, R. Pullela, E. Pehlivanoglu, H. Zarei, S. Tadjpour, D. Agahi, D. Rozenblit, W. Domino, G. Williams, N. Damavandi, S. Wloczysiak, S. Rajendra, A. Paff, and T. Valencia, "Single-chip multiband wcdma/hsdpa/hsupa/egprs transceiver with diversity receiver and 3g digrf interface without saw filters in transmitter / 3g receiver paths," in *Solid-State Circuits Conference - Digest of Technical Papers, 2009. ISSCC 2009. IEEE International*, pp. 116–117,117a, 2009.

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