Optimization of Printed Electronics

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ABSTRACT

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Solution processed circuitries are expected to be the main components to achieve low cost, large area, flexible electronics. However, the commercialization of solution processed flexible electronics face several challenges. The passive component such as capacitors are limited in frequency range and operating voltage. The active component such as transistors suffer from low mobility ultimately leading to limited current-carrying capacity. Just as in traditional silicon technology, the fabrication process and material choices significantly impact the performance of the fabricated devices. My thesis focuses on the optimization of the performance of printed capacitors and transistors through investigation of several aspects of the device structure and fabrication process.

The first part of this work focuses on the optimization of printed nanoparticle/polymer composite capacitors. Thin film metal oxide nanoparticle/polymer composites have enormous potential to achieve printable high-k dielectrics. The combination of high-k ceramic nanoparticle and polymer enables room temperature deposition of high dielectric constant film without the need of high temperature sintering process. The polymer matrix host fills the packing voids left behind by the nanoparticles resulting to higher effective dielectric permittivity as a system and suppresses surface states leading to reduced dielectric loss. Such composite systems have been employed in a number of flexible electronic applications such as the dielectrics in capacitors and thin film transistors. One of the most important properties of thin film capacitors is the breakdown field. In a typical capacitor system, the breakdown process

leads to catastrophic failure that destroys the capacitor; however, in a nanoparticle/polymer composite system with self-healing property, the point of breakdown is not well-defined. The breakdown of the dielectric or electrodes in the system limits the leakage observed. It is possible, however, to define a voltage/field tolerance. Field tolerance is defined as the highest practical field at which the device stays operational with low failure rate by qualifying the devices with defined leakage current density. In my work, the optimization of the field tolerance of $(Ba,Sr)TiO_3(BST)$/parylene-C composite capacitors is achieved by studying the influence of the electromigration parameter on leakage and field strength through the inherit asymmetrical structure of the fabricated capacitors.

One approach to creating these composites is to use a spin-coated nanoparticle film together with vapour deposited polymers, which can yield high performance, but also forms a structurally asymmetric device. The performance of a nanoparticle BST/parylene-C composite capacitor is compared to that of a nanoparticle BST capacitor without the polymer layer under both directions of bias. The composite device shows a five orders of magnitude improvement in the leakage current under positive bias of the bottom electrode relative to the pure-particle device, and four orders of magnitude improvement when the top electrode is positively biased. The voltage tolerance of the device is also improved, and it is asymmetric (44 V vs. 28 V in bottom and top positive bias, respectively). This study demonstrates the advantage of this class of composite device construction, but also shows that proper application of the device bias in this type of asymmetrical system can yield an additional benefit.

The dependence of the field tolerance of nanoparticle/polymer composite capacitors on the electromigration parameter of the electrodes is investigated using the symmetrical dielectric system. The breakdown is suppressed by selecting the polarity used in nanoparticle $(Ba,Sr)TiO_3$/parylene-C composite film-based capacitors. Metals including gold, silver, copper, chromium, and aluminum with comparable surface conditions were examined as the electrodes. The asymmetric silver, aluminum, gold,

copper, and chromium electrode devices show a 64 %, 29 %, 28 %, 17 %, 33 %, improvement in the effective maximum operating field, respectively, when comparing bias polarity. The field at which filament formation is observed shows a clear dependence on the electromigration properties of the electrode material and demonstrates that use of electromigration resistant metal electrodes offers an additional route to improving the performance of capacitors using this nanoparticle/polymer composite architecture.

The second part of my thesis focuses on the novel pneumatic printing process that enables manipulation of the crystal growth of the organic semiconductors to achieve oriented crystal with high mobility. Small molecule organic semiconductors are attracting immense attention as the active material for the large-area flexible electronics due to their solution processability, mechanical flexibility, and potential for high performance. However, the ability to rapidly pattern and deposit multiple materials and control the thin-film morphology are significant challenges facing industrial scale production. A novel and simple pneumatic nozzle printing approach is developed to control the crystallization of organic thin-films and deposit multiple materials with wide range of viscosity including on the same substrate. Pneumatic printing uses capillary action between the nozzle and substrate combined with control of air pressure to dispense the solution from a dispense tip with a reservoir. Orientation and size of the crystals is controlled by tuning the printing direction, speed, and the temperature of the substrate.

The main advantages of pneumatic printing technique are 1) simple setup and process, 2) multi-material layered deposition applicable to wide range of solution viscosity, 3) control over crystal growth. The manipulation of crystal growth will be discussed in the next chapter. This method for performance optimization and patterning has great potential for advancing printed electronics.

The dependence of the mobility of printed thin film 6,13-bis(triisopropylsilylethynyl) pentacene [TIPS-pentacene] and C8-BTBT on printing conditions is investigated, and

the result indicates that the formation of well-ordered crystals occurs at an optimal head translation speed. A maximum mobility of 0.75 cm^2/(Vs) is achieved with 0.3 mm/s printing speed and 1.3 cm^2/(Vs) with 0.3 mm/s printing speed at 50 °C for TIPS-pentacene and C8-BTBT respectively. In summary, pneumatic printing technique can be an attractive route to industrial scale large area flexible electronics fabrication.

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To my family

Chapter 1

Introduction

1.1   Background and Motivation

Solution processed electronics are expected to be pave the way to enable low cost, large area, flexible circuitries and allow for wide range of applications space not possible with traditional silicon based electronics. The applications such as flexible and conformal display, large area sensing including electronic skin, and ultra low cost/disposable electronics are becoming a reality as the technology matures. [1][2][3][4][5][6][7]

However, the commercialization of solution processed flexible electronics faces several challenges. The passive components such as capacitors are limited in frequency range and operating voltage or require high temperature treatment (> 600 °C), which is not suitable for fabrication on plastic substrate.[8] On the other hand, the printed active components such as organic semiconductor based transistors suffer from low mobility, and ultimately, leading to limited current-carrying capacity. Just as in traditional silicon technology, the fabrication process and material choices significantly impacts the performance of the fabricated devices. Therefore, improving the performance through optimization of material and structure consideration as well as fabrication process is desirable.

Ceramic nanoparticle and polymer composite dielectrics offer a promising route to

achieve high performance printed capacitors. The filler-matrix system with ceramic fillers hosted with polymer matrix combines the high dielectric constant of the ceramic materials and the low loss of the polymer materials.[9][10][11] In particular, the high-κ dielectric nanocrystals based peroskite oxides in paraelectric or potentially super paraelectric state is an attractive candidate as the ceramic filler. It has been shown that parylene can be used as the host matrix polymer that passivates the surface and suppressed the loss due to leakage in such composite system.[8] Understanding of the failure mechanism of such system can lead to optimization of bias conditions and electrode material selection that can provide additional knob to tuning the performance of the device.

Solution processable small molecule semiconductors are strong candidates as the active materials for field transistor for the flexible electronics applications due to their high mobility with potential for further improvement.[12][13][14] The mobility of the small organic molecule semiconductors are strongly depending on its crystal orientation.[15][16][17] Hydrodynamics flow significantly influences the molecular assemblies, and the highest mobility is achieved when the direction of the current flow is aligned with the direction of molecular packing.[18][15][19][20][21][22] Many methods have been developed to control the orientation of the crystal growth including dip coating, zone casting, hollow pen writing, solution shearing, and off-centre spincoating technique.[22][23][16][24] However, these techniques have challenges in patterning, or practical implementation due to complex equipment requirements. Therefore, the development of simple printing method that can manipulate the crystal growth to achieve high performance and deposit multiple materials at the simultaneously is desirable. With such technique, the solution processable organic semiconductor transistors are one step closer to commercial implementation.

1.2 Capacitor

This section presents an introduction to the theory of the capacitor operation and general discussion of the dielectric materials. The parallel plate capacitor is the simplest structure to investigate the electrical properties of the dielectric materials, and it is the preferred structure for the experiments discussed in this thesis. We will introduce the basics of the material of interest, $BaSrTiO_3$/parylene composite dielectric, later in this section as well.

1.2.1 Parallel Plate Capacitor Structure

Many materials can be used as the dielectric material, and the electrical characteristics of the capacitor depend on the material employed. The electrical properties of a given material can be characterized through a simple parallel plate structure. The operation theory and the basic characteristics of parallel plate capacitor structure are described in this section.

The 3D cross sectional view of a parallel plate capacitor structure is shown in Fig. 1.1. The capacitor is made of two metal electrodes with the same area, A, separated by the dielectric material of interest with thickness of d. Note that the overlapping area of the two electrodes defines the active area of the capacitor. In this case, it is assumed that the electrodes are perfectly aligned so that the active area is equal to the electrode area A. When a voltage source is connect to the capacitor as shown in the Figure, the electric force will move the electron towards the positive terminal of the voltage source. An electron deficiency occurs on the positive side which can be describe as plus charge, +q, will accumulate on the (+) electrode and negative charge, -q, will accumulate on the (-) negative electrode. The movement of the electron continues until the potential between the two electrodes are equal to the potential of the voltage source. The is the charging of the capacitor. The equation describing the total capacitance are:

$$Q = CV \tag{1.1}$$

$$C = \frac{\epsilon A}{d} \tag{1.2}$$

$$\epsilon = \epsilon_0 * \epsilon_r \tag{1.3}$$

Where C (Farad) is the total capacitance, ϵ the dielectric constant, A (cm^2) the surface area, and d (cm) the thickness of the dielectric layer. The dielectric constant is given by the product of permittivity of vacuum ($\epsilon_0 = 8.854 * 10^{-12}$ F/m) and the relative permittivity (ϵ_r).[25]
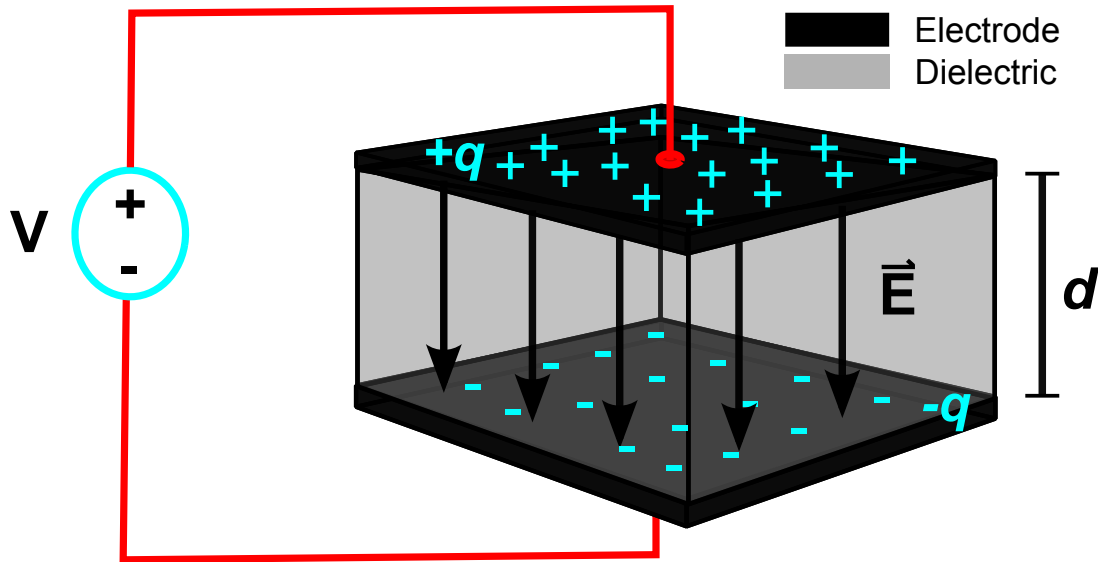
Figure 1.1: Parallel plate capacitor structure illustrated with dielectric material with dielectric constant, ϵ. The two identical electrodes, with area A, are separated by dielectric layer with thickness of d. The total capacitance of the parallel plate capacitor is given by $C = \frac{\epsilon A}{d}$.

1.2.2 High-κ BaSrTiO$_3$/Parylene Composite Dielectric

Dielectric material properties determine the performance of the capacitors. Thin film materials with high dielectric constant are attracting immense attention due to the ability to enhance the field effect or energy storage density. Such high performance film have a wide range of applications including memory, embedded capacitor, gate dielectric for TFT, and power storage devices.[26][27][28][29][30] Improving the property of the dielectric media through nanofabrication techniques and nanoscale material engineering can enable increased efficiency and range of operation.[31]

A number of approaches have been proposed to achieve high capacitance density in a thin film system including deposition of high-κ inorganic dielectric with high temperature post annealing and the development of high-κ polymer dielectrics.[32][33][34][35] [36] However, these approaches introduce several fabrication complications and face some performance limitations. The use of inorganic dielectric requiring high temperature process ($> 600°$C) prevents fabrications on flexible substrates. The polymer dielectrics typically have lower dielectric constant (< 15) and limited frequency range. Combining both advantages, the high dielectric constant of inorganic dielectrics and the low processing temperature of the polymer dielectrics, appears to be possible through the use of ceramic-nanoparticle/polymer composite dielectrics.

Low temperature processed, aggregate-free, highly crystalline ceramic nanoparticle are strong candidates as the next generation dielectric materials. Previous work have shown the size tunability and solvent dispersion uniformity of the BaSrTiO$_3$ (BST) nanoparticle.[37][38][39] The size of the BST particle can be tuned from 5 to 100 nm with 90 % yield and narrow size distribution.[8] However, pure BST films exhibit lower dielectric constant (15) due to limitation in packing ratio of the spherical structure. It has been shown that by filling the voids (initially air) with polymer matrix, the performance of the composite system increases significantly.[31] Furthermore, the dielectric loss is reduced by an order of magnitude. The performance and optimization of the composite dielectric capacitor formulated by combining the BST

nanoparticles and the polymer matrix will be discussed in detail in the fist part of this thesis.

1.3 Organic Thin Film Transistor

This section presents an introduction to basic theory and operation principles of organic semiconductors. The correlation between the chemical structures and electronics properties is discussed. TIPS-pentacene and C8-BTBT are two promising organic semiconductor materials that exhibit high mobility with potential in organic thin film transistor applications.

1.3.1 Basics of Organic Semiconductor - Pentacene

Organic semiconductors are carbon-based materials with electrical conductivity in between that of the insulator and conductor. This class of materials have delocalized charge carrier resulting from their conjugated bonds. [40] The alternating single and double bonds in the molecule, illustrated in Fig. 1.2, indicate that the carbon atoms in the molecule are *sp2* hybridized. The neighbouring sp^2 hybridized carbon atoms forms delocalized clouds of π electrons called conjugated bonds. This conjugated network gives rise to the energy-gap (E_g) which is defined as the difference between the highest-occupied-molecular-orbital (HOMO) and lowest-unoccupied-molecular-level (LUMO).[41] The presence of HOMO-LUMO gap results in the semiconductor characteristics where charge transport can be controlled by external stimulation including electric field and light. The material characteristic of the organic semiconductor can be modified by changing its chemical structure. For example, increasing the length and branching position of the side chains and changing the length of the fused benzene ring backbone can greatly influence the material properties of the organic semiconductors.[41][42]

Pentacene is a p-type semiconductor consists of five benzene rings, and it is one of
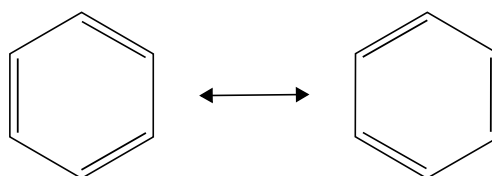
Figure 1.2: Resonanace forms of benzene

the most popular small molecule organic semiconductor due to its potential for high mobility. The chemical structure of the pentacene is shown in Fig 1.3. The HOMO-LUMO gap for pentacene is about 2.1 eV.[43] Pentacene is a p-type semiconductor meaning the holes are the majority charge carriers, and the positive charge transport is the dominant carrier transport. The electron rich pentacene molecule can easily lose an electron, but it is energetically difficult to accept one. The highest mobility reported exceeds 5 cm^2/Vs which is larger than that of amorphous silicon.[44][45]
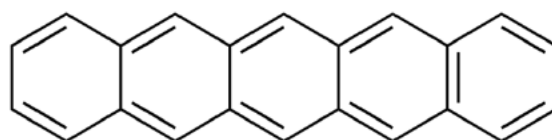
Figure 1.3: Chemical structure of pentacene

However, pentacene is not ideal for large area electronics application for several reason. First reason is that pentacene can only be deposited through vacuum because it is not soluble to the degree where solution process can be employed. Second, pentacene oxidises easily, which leads to disruption of transport and performance degradation. Lastly, the pentacene forms two crystal phases that are not perfectly matched. The presence of both crystal phases leads to grain mismatch and reduces electrical performance. One approach to solve all three short comings is to engineer pentacene derivative by functionalizing it. The most promising pentacene derivative that posses both air-stability and high performance is TIPS-pentacene.

1.3.2   TIPS-pentacene

The 6th and 13th position of the pentacene is susceptible to reaction to water and oxygen resulting in performance degradation. A pentacene derivative, 6,13-Bis(triiso-propylsilylethynyl)pentacene [TIPS-pentacene], is engineered to synthetically attach two Si-$(CH_3)_3$ to the 6th and 13th position on the molecule. The attached functional groups are carefully selected to achieve passivation of the most reactive sites and improves solubility. Furthermore, the functionalization leads to single phase crystallization.[41][46] The molecular structure of the TIPS-pentacene is shown in the Fig. 1.4. TIPS-pentacene can be deposited through both thermal evaporation and solution process. The performance of the evaporated TIPS-pentacene is better than that of the regular pentacene; however, solution processed TIPS-pentacene shows potential for high performance because its strong tendency to crystallizes. Solution process TIPS-pentacene has attracted many attention over the last decade due to its superior mobility. In the second part of this thesis, we will explore a novel printing method to achieve well aligned crystal growth and improved mobility in TIPS-pentacene based transistors.
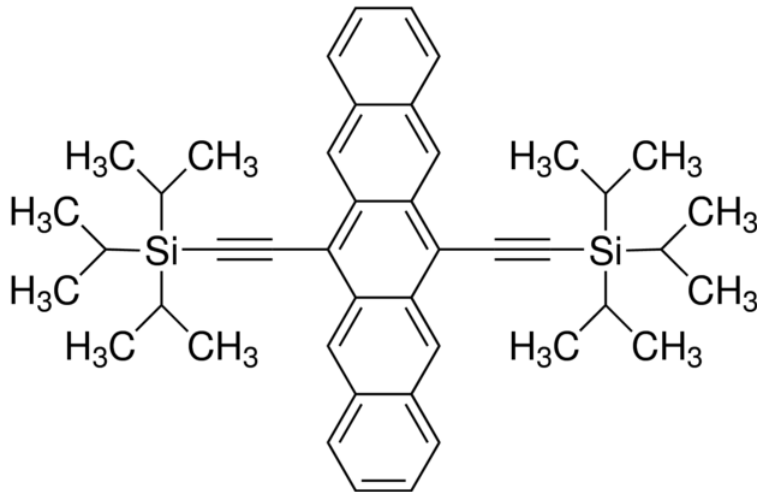
Figure 1.4: Chemical structure of TIPS-pentacene

1.3.3   C8-BTBT

Another small molecule that exhibit high mobility is 2,7-dioctyl[1]benzothieno[3,2-b][1]benzothiophene (C8-BTBT). The molecular structure of C8-BTBT is shown in Fig. 1.5. The crystal stacking of C8-BTBT is characterized by herring-bone arrangement in the intra-layer plane which facilitates almost isotropic carrier transport in two-dimension.[47] The highest reported mobility for C8-BTBT is 43 cm^2/Vs by Yuan et al. The extra ordinary mobility is achieved by an novel off-centre spin-coating method to form a meta-stable crystal structure.[24] Other groups have employed various printing technique including solvent/antisolvent inkjet printing, spin-coating with solvent vapour annealing, dip-coating process to fabricate transistor devices that exhibit mobility in the range of 3 - 16 cm^2/Vs. [20][48][49]
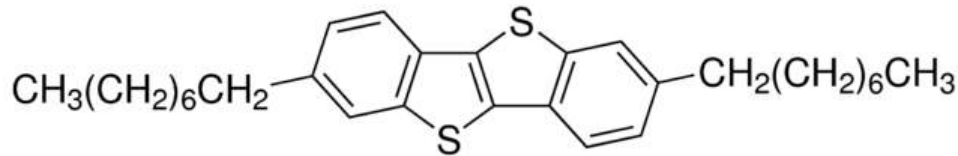
Figure 1.5: Chemical structure of C8-BTBT

1.3.4   OFET Operation and Model

The carrier transport in organic semiconductor is still under-debate, but, in general, the conduction occurs due to hopping of charges between localized states on the individual molecules. The transport in an organic semiconductor is typically single carrier dominant. The formation of one or the other charge carrier type would require overcoming significantly larger barrier due to the asymmetry in the density of states in the disordered system like the organic semiconductor material. Therefore, the amorphous or polycrystalline organic semiconductors excursively allow electron or hole transport but not both.[41] Typical transfer and output characteristic of printed TIPS-pentacene is shown in Fig 1.6 a) and b) respectively.

Even though organic semiconductor based TFTs (OFETs) operate under different conduction mechanism, the electrical characteristic of the organic thin film transistor can be modelled using the formula similar to the ones used for the classic MOSFETs to the first order. The basic capacitor structure that dictates the charge density in the channel through the relationships $Q_C = C_i(V_{GS} - V_T)$ holds true for OFET as well. C_i is the gate dielectric capacitance, and the $V_{GS} - V_T$ is voltage applied in the channel through the gate electrode above the threshold voltage. The regions of operation can be separated into three regions: cut-off, linear and saturation.

The OFET regions of operations are organized in Table 1.1. Under bias condition where $V_{GS} < V_T$, the channel is depleted, and there are very few mobile charges and almost no current flows. When small V_{DS} and larger V_{GS} is applied with the bias conditions $V_{GS} > V_T$ and $V_{DS} < V_{GS} - V_T$, the device enters linear region where the current is determined by the charge induced by the gate voltage above threshold and the geometrical factor. The bias condition and current equation in the linear region is shown in row 2 of the Table 1.1. As the V_{DS} is increased until $V_{DS} > V_{GS} - V_T$, pinch-off occurs, and the device is under saturation. The bias condition and current equation in the saturation region is shown in row 3 of the Table 1.1. The schematic illustrations of the organic thin film transistor cross-sectional structure and operation regions are shown in Fig. 1.7.

Fundamentally, mobility is the relationship describing how fast carriers can move through a given material under an applied electric field, and it is the most frequently-reported figure of merit to evaluate the performance of the fabricated OFETs. The mobility in an organic semiconductor is significantly dependent on the dielectric/semiconductor interface properties and the structure and alignment of the semiconductor crystals. The effective mobility of the fabricated OFETs can be determined by measuring the I_D vs V_G characteristic in the saturation region. To eliminate the dependency on the ambiguity of the threshold voltage, the effective mobility can be extracted by plotting the $\sqrt{|I_D|}$ vs V_G and calculating the slope. The equation for mobility extraction is

Table 1.1: OFET regions of operation and equations

Region	Bias condition	Equation
Cutoff	$\mid V_{GS} \mid < \mid V_T \mid$	$I_D \approx 0A$
Linear	$\mid V_{DS} \mid < \mid V_{GS} - V_T \mid$	$I_D = \dfrac{W}{L} \mu C_{OX}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS}$
Saturation	$\mid V_{DS} \mid > \mid V_{GS} - V_T \mid$	$I_D = \dfrac{W}{2L} \mu_{sat} C_{OX}(V_{GS} - V_T)^2$

shown in Eqn. 1.4.

$$\mu = \frac{2L}{W}\frac{1}{C_i}\left(\frac{\partial\sqrt{I_D}}{\partial V_G}\right)^2 \tag{1.4}$$

1.4 Objective and Approach

1.4.1 Printed BaSrTiO$_3$/Parylene Capacitor

Nanoparticle (Ba, Sr)TiO3 (BST)-based films exhibit a high effective dielectric constant. Incorporation of polymer host, parylene, improves the dielectric strength and high loss by reducing the leakage current. The composite system combines the favourable dielectric constant of the nanoparticles with the superior dielectric strength of the polymer host to offer a high performance, printable dielectric material. We have previously shown that depositing a parylene-C film via chemical vapour deposition after printing a film of inorganic nanoparticles improves surface roughness and suppresses leakage while maintaining reasonably high effective dielectric constant. The introduction of parylene-C as a passivation layer results in a physically asymmetric capacitor, and this asymmetric system is well suited for investigating the electrical consequences of the bias polarization. Furthermore, the asymmetric structure of the

BST/parylene-C capacitor is an ideal system to study the effect of the electrodes' electromigration parameter on capacitor performance. The top and bottom electrodes interface with different physical barriers, providing a controlled experimental environment in which to compare the same electric field on the dielectric with a passivated (parylene-C coated) surface, and a free (porous BST) electrode interface. We use this asymmetrical relationship to investigate the correlation between voltage tolerance and electromigration susceptibility. The favourable bias condition and the selection of electrode material will lead to optimization of the field strength of the printed capacitors.

1.4.2 Printed Organic Semiconductor

The simplest way to print organic semiconductor solution is to use a needle syringe interfaced with 3D stage and a EFD to control the back and forward pressure applied to the syringe. I demonstrate that this simple and novel pneumatic nozzle printing approach to fabricating organic semiconductor can achieve control over the crystallization of thin-films and deposition of multiple materials on the same substrate. Pneumatic printing uses capillary action between the nozzle and substrate combined with control of air pressure to dispense the solution from a dispense tip with a reservoir. We can control the orientation and size of the crystals by tuning the printing direction, speed, and the temperature of the substrate. Pneumatic printing technique can be an attractive route to industrial scale large area flexible electronics fabrication.
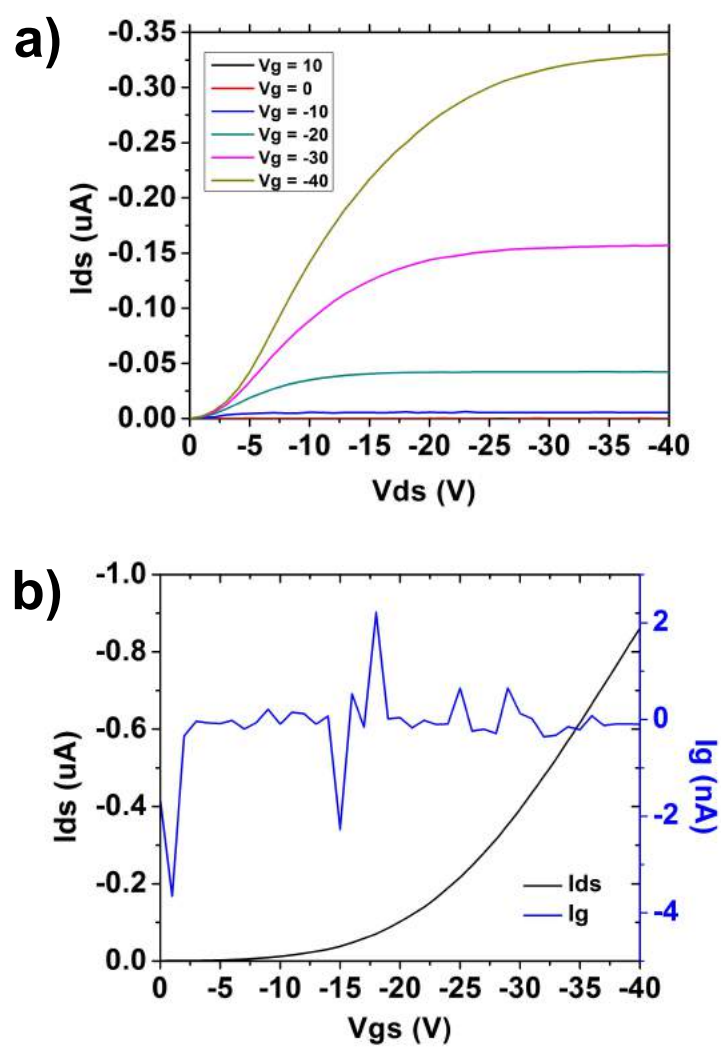
Figure 1.6: IV characteristic of printed TIPS-pentacene. a) I_{DS} vs V_{DS} under different V_G b) I_{DS} vs V_{GS} with V_{DS} = -40 V

Cross section of OFET structure

Semiconductor
Source
Drain
Substrate
Gate
Gate dielectric

**Cutoff
(Depleted)**

0 V   0 V
0 V

**Linear region
(Accumulated)**

0 V   - 0.1 V
- 5 V

**Saturation region
(Accumulated)**

0 V   - 40 V
- 40 V

Organic Semiconductor   Gate electrode

Source/drain electrode   Substrate

Gate dielectric   Accumulated charges
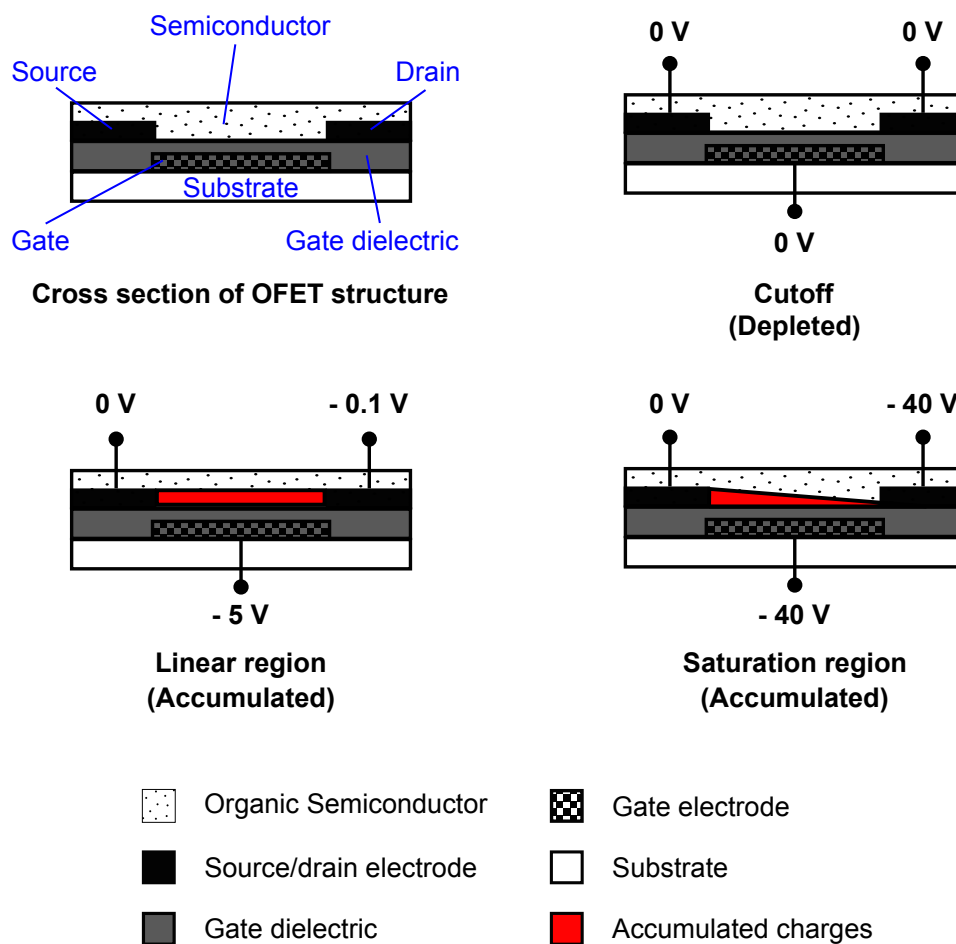
Figure 1.7: A schematic illustration of the organic thin film transistor cross-sectional structure and operation regions.

Part I

Printed Capacitor Optimization

Chapter 2

BaSrTiO$_3$/Polymer composite Capacitor - Asymmetric Structure and Field Tolerance Optimization

2.1 Introduction

Polymer/metal oxide nano-composites are attractive as solution processable high permittivity materials for dielectric layers in a variety of electronic devices including transistors and energy storage devices.[8][50][51][52][53][54][55] The solution processability of these nano-composites enables roll-to-roll fabrication on flexible substrates at room temperature under ambient conditions, which has the potential for large-scale, low cost manufacturing.[56] Printable ceramic capacitors offer performance competitive with high temperature fired multi-layer ceramic capacitors, and they exhibit potential for high operating frequency performance, making them competitive with polymer film capacitors.[8][54][57][58]

Nanoparticle (Ba, Sr)TiO3 (BST)-based films have been shown to exhibit a high effective dielectric constant.[8][54][57][59] Without surface modification or incorporation of a polymer host, however, a high leakage current in the film leads to poor

dielectric strength. The incorporation of a polymer host combines the favorable dielectric constant of the nanoparticles with the superior dielectric strength of the polymer host to offer a high performance, printable dielectric material.[8][54][57][60][61][62]

We have previously shown that depositing a parylene-C film via chemical vapor deposition after printing a film of inorganic nanoparticles improves surface roughness and suppresses leakage while maintaining reasonably effective high dielectric constant.[8] Forming the composite in this way offers several advantages: there is no interaction of the polymer component with the particles in the suspension, the polymer penetrates and condenses in the film without disrupting its packing, and a higher effective fill factor can be achieved in the solid film.[63][64] Parylene deposition has also been shown to passivate surface states that lead to leakage and dielectric loss in nanoparticle and thin film systems.[8][54][57]

The introduction of parylene-C as a passivation layer results in a physically asymmetric capacitor. The bottom electrode is directly in contact with the nanoparticle material, whereas the top electrode is deposited on a thin parylene layer. The parylene also does not penetrate the entire body of a 280 nm thick nanoparticle film, which is confirmed by both microscopy and examination of thickness. As the reactive monomer condenses in the BST voids, it forms a polymer layer that prevents further penetration of monomer material deeper into the structure. In this work, we investigate the electrical consequences of this asymmetry, with a particular emphasis on the effect this asymmetry has on the use of these capacitors in energy conversion applications. We show that the difference in electromigration characteristics between the bottom and top interface leads to reduced leakage and superior dielectric strength when the device is biased with the bottom electrode as the positive electrode.

2.2   Fabrication Method

The device tested is a 3 mm x 3 mm parallel plate capacitor with the composite
material as the dielectric. The capacitors were made using the following process
(illustrated in Fig. 2.1): First, 5 nm of chrome and 40 nm of gold are deposited onto
a clean bare glass substrate by thermal evaporation. These electrodes, which are
the bottom electrodes of the structure, are photolithograhically patterned and wet
etched. The nanoparticle solution is composed of B0.7S0.3TiO3 nanoparticles, 8 to
12- nm diameter, dispersed in ethanol with no surfactant at a concentration of 20
mg/ml.[8] The nanoparticles are synthesized using wet chemistry techniques yielding
a high degree of monodispersity.[8] A film is formed by spin-casting the solution onto
the bottom electrode using a two-step dynamic coating process. The first spin step
is 15 seconds at 500 rpm, and the solution is dispensed on the substrate during this
step. The second spin step is 45 seconds at 1000 rpm. The spin-coating process is
repeated 4 times to achieve the desired thickness of 280 nm 20 nm. After a 12-hour
dehydration bake at 80 C, parylene-C is deposited on top of the BST film by chemical
vapor deposition. This process forms a BST/parylene-C composite layer of around
80 nm. Finally, 40 nm of gold is thermally evaporated with a metal stencil shadow
mask to form a patterned top electrode. The cross section of the device is shown in
Fig. 2.2. Capacitors with 1 mm x 1 mm active area are also fabricated to test for
frequency response.

2.3   Testing Method and Field Tolerance

The capacitance and loss of the device was measured using an Agilent 4294 impedance
analyzer with 42941A impedance probe.

It is known that the polymer film capacitors show a self-healing behavior, whereby
local degradation of the electrode leads to recovery of the capacitor after a local failure.
As a result, defining a single breakdown voltage for these devices is difficult.[65] We

instead use a voltage tolerance test that measures the leakage current and sets an acceptable range for leakage in each application. In this test, the voltage is swept from 0 V to 80 V and the current is measured. The top electrode is grounded and the bias is applied to the bottom electrode. For the forward bias case, a positive voltage is applied to the bottom electrode, and for reverse bias, a negative voltage is applied to the bottom electrode. The effect of the asymmetry introduced by the parylene-C composite layer is quantified by measuring the voltage tolerance, which is the voltage at which the device leakage current exceeds a defined current density. The leakage current is chosen so that the device is stressed below the level of catastrophic failure of the electrode. Fig. 2.3 illustrates the voltage tolerance qualification. The chosen leakage current density in this experiment is 10 A/cm^2. This voltage tolerance test is performed on 32 devices per substrate using a switch matrix system (Keithley 7001) and source meter (Keithley 2400) with automated computer control.

Testing is performed on BST devices and BST/parylene-C composite devices. The BST device is symmetric in structure and serves as the control device. Comparison between the performance of the BST device and the BST/parylene-C composite device indicates the impact of the composite film.

2.4   Failure Mechanism

In many capacitor systems, the breakdown process leads to runaway damage that destroys the capacitors. In self-healing systems, such as polymer film and ceramic nanoparticle/polymer composites, the point of breakdown is not well-defined. The breakdown process is typically self-limiting, and destruction of the dielectric or electrodes limits the leakage observed in the device. Fig. 2.4 a) shows the IV characteristic of a self-healing device. The characteristic partial breakdown on the electrode is shown in Fig. 2.3 b). The leakage current in self-healing systems, which typically exhibit filamentary defects, follows a Fowler-Nordheim tunneling characteristic.[66][67]

Surface modification can suppress the leakage current in filament-forming capacitor
systems and is one accepted approach to improving the voltage tolerance.[8][61][60][62]
However, the two major factors that have been demonstrated to have major impact
on the Fowler-Nordheim emission type leakage are the surface roughness and the
work function. It has been shown, for example, that the surface roughness plays a
significant role in the leakage characteristic, and that rougher electrode surfaces re-
duce the voltage at which the leakage occurs due to the formation of field enhancing
asperities.[68] The tunneling current, which is caused by field emission from the elec-
trode surface, is barrier dependent. The work function of the electrodes therefore also
influences the leakage and breakdown field strength of the device.[69][70][71]

2.4.1 Fowler-Nordheim Emission

The Fowler-Nordheim emission equation is shown in equation 2.1 where the leakage
current shows dependence on barrier heigh (ϕ) and applied electric field (E). It is clear
that work function and surface roughness will play a role in this high field leakage
regime. The work function will define the barrier height and the surface roughness
(defining the effective distance between the electrode, d) will influence the effective
applied field as shown in the equation 2.2. The measured leakage data can be fitted
with the Fowler-Nordheim equation as shown in Fig. 2.5.

$$I_{leakage} = \frac{AE^2}{\phi} exp(\frac{-B\phi^{3/2}}{E}) \tag{2.1}$$

$$E = \frac{V}{d} \tag{2.2}$$

In devices that exhibit filamentary failure mechanism, the electromigration pa-
rameter of the electrode material is a factor that can affect the field strength of the
capacitor.[51] The electromigration parameter will determine the susceptibility of the

electrode to filament formation. Once the filaments are formed, the leakage current increase from the field enhancement at the apex of the wire, and will continue to draw the metal out. As the filament grows, the field and current increase,and it will ultimately lead to a runaway leakage process until Joule heating destroys the metal wire and heals the capacitor. The competing proposed mechanism is the formation of conducting paths in the dielectric, resulting in dielectric breakdown. In this situation, the conducting path is generally proposed to be formed by a change in the molecular structure of the dielectric associated with an interaction with the leakage current. In both cases, the work function is a crucial parameter in determining the breakdown field strength because the charge injection is directly associated with the barrier height. In the filamentary mechanism, the electromigration parameter also plays a significant role in determining the field tolerance, and understanding the influence of the electromigration parameter on leakage and field strength will provide an additional path to device optimization.

The asymmetric structure of the BST/parylene-C capacitor is an ideal system with which to study the effect of the electrodes' electromigration parameter on capacitor performance. The top and bottom electrodes interface with different physical barriers, providing a controlled experimental environment in which to compare the same electric field on the dielectric with a passivated (parylene-C coated) surface, and a free (porous BST) electrode interface.[72] In the next chapter, we use this asymmetrical relationship introduced in this chapter to investigate the correlation between voltage tolerance and electromigration susceptibility, while also examining the work function and the surface roughness contribution of the electrodes to the field tolerance of the device.

2.5   Electrical Properties and Discussion

The dielectric characteristics of the BST/parylene-C composite capacitor are summarized in Table 2.1. The dielectric layer is about 280 nm in thickness, and exhibits a relatively high k of 22 at 1 kHz and 17 at 1 MHz. The capacitance density is around 71 nF/cm^2 at 1 kHz and 55 nF/cm^2 at 1 MHz. The loss tangent is less than 0.05 at 1 MHz. Typical capacitance density data of 1 mm x 1 mm devices are shown in Fig. 2.6. The capacitance density measured from 1 mm x 1 mm devices and the 3 mm x 3 mm devices are consistent indicating good uniformity. The frequency dependent relative dielectric constant and loss tangent of the nanoparticle BST/parylene-C composite capacitor is shown in Fig. 2.7 2. Our data shows higher k and similar loss to our previously reported devices.[8]

The capacitor leakage is roughly exponential with voltage as shown in 2.8(a) for the nanoparticle BST device and Fig. 2.8(b) for the nanoparticle BST/parylene-C composite device. We suspect that filamentary conduction is the primary cause of this non-ohmic transport. Direct tunneling between two electrodes is unlikely at this dielectric thickness, and other groups have reached the same conclusion, showing Fowler-Nordheim tunneling from electrode filaments.[73][74][75] From AFM data, our gold bottom electrode shows a roughness of 11 nm with spikes as large as 78 nm. It has been shown that the roughness of the electrode contributes to the enhancement of Fowler-Nordheim tunneling.[66][67] When the conduction mechanism is filamentary in nature, the asymmetry in the structure leads to asymmetry in the leakage current and voltage tolerance due to the surface passivation provided by the parylene layer. The I-V plot for a nanoparticle BST capacitor is shown in 2.8(a). As expected, there is no asymmetry present between the two bias conditions. The measurement variation due to the high leakage of the pure BST film in the low field region is shown with two pairs of curves in 2.8(a). A typical I-V characteristic for a nanoparticle BST/parylene-C composite capacitor under forward and reverse bias condition is shown in 2.8(b). While the leakage current still appears exponential in shape, the

reverse-biased leakage current is roughly thirty times larger than the forward bias leakage current at 20 V shown in Table 2.1. The effect of the parylene-C layer can further be quantified by binning the leakage current density and voltage tolerance under forward and reverse bias conditions.

The voltage tolerance is investigated at a leakage current density of 10 A/cm^2 under different bias conditions. The voltage tolerance data is shown in 2.8(c). The voltage tolerance is comparable for nanoparticle BST devices under forward and reverse bias conditions. The capacitors with a nanoparticle BST/parylene-C composite dielectric layer, however, show a different voltage tolerance under varying bias polarity. All of the composite devices have a voltage tolerance less than 40 V under reverse bias. In comparison, under forward bias, 16% of the composite devices have a voltage tolerance below 40 V.

The leakage current density is investigated at 20 V under both bias conditions. The leakage current density data is shown in 2.8(d). The data for the capacitors without parylene-C shows no asymmetry with bias polarity; the leakage current is in the mA/cm^2 range at 20 V for both bias conditions. The capacitors with parylene-C composite exhibit asymmetry under different bias condition, as expected. A majority of the composite devices have a leakage current of approximately 1 A/cm^2 under reverse bias, and roughly 10 nA/cm^2 leakage under forward bias. The data demonstrates that the parylene-C rich interface to the top electrode is likely resisting filament formation.

2.6 Conclusion

We have investigated the electrical characteristic of capacitors made using BST nanoparticle films and nanoparticle BST/parylene-C composite films. The failure mechanism of such composite materials are also discussed. The capacitor with the composite film dielectric demonstrates a significant improvement in its electrical properties,

with leakage current reduced by about 4 orders of magnitude when compared with the nanoparticle BST film capacitor. We have further demonstrated significant benefit from forward biasing the particle/polymer composite device. Forward biasing the capacitor results in a 27x reduction in the device leakage current and a 16 V improvement in voltage tolerance when compared with identical capacitors under reverse bias. This work demonstrates a previously unrecognised sensitivity to bias direction in these composite devices, and that these systems will exhibit a higher voltage tolerance and lower leakage under forward bias polarization.
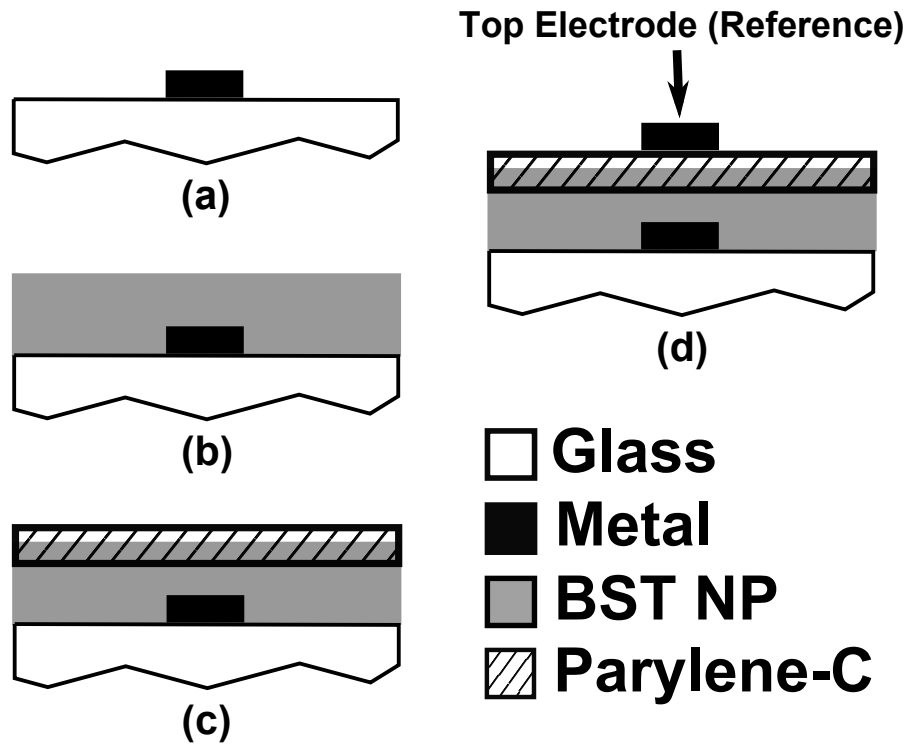
Figure 2.1: Process flow of the nanoparticle BST/parylene-C composite layer: (a) 5 nm of chrome and 40 nm of gold are deposited onto a clean bare glass substrate by thermal evaporation and photolithographically patterned. (b) BST film (280nm) is deposited by spin-casting the solution onto the bottom electrode using a two-step dynamic coating process followed by dehydration bake at 80 C for 12 hours. (c) Parylene-C is deposited on top of the BST film by chemical vapor deposition. This process forms a BST/parylene-C composite layer of around 80 nm. (d)40 nm of gold is thermally evaporated with a metal stencil shadow mask to form a patterned top electrode.
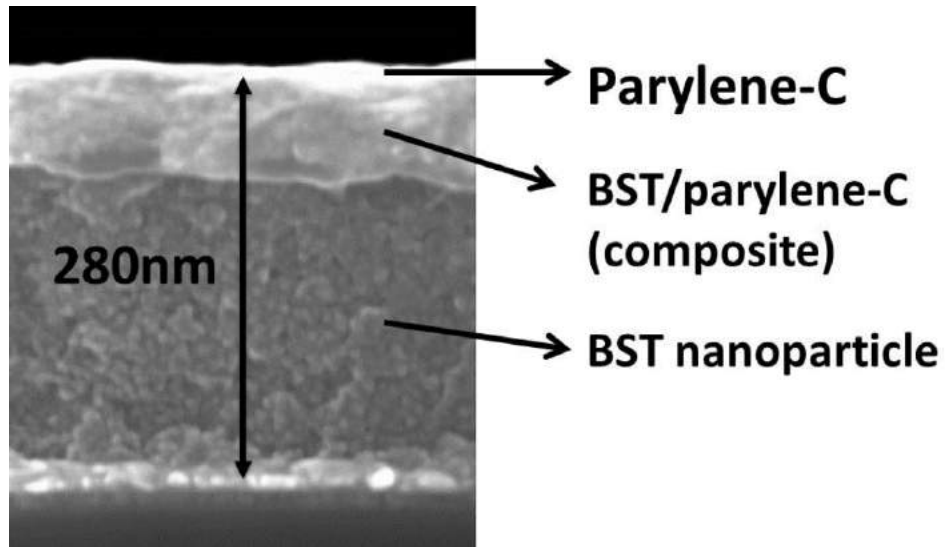
Figure 2.2: Cross section SEM image of the nanoparticle BST/parylene-C composite layer
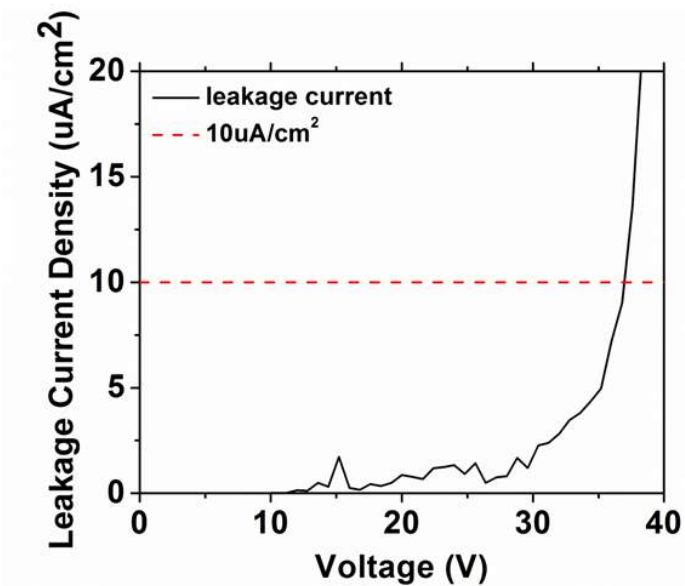
Figure 2.3: Illustration of quantifying voltage tolerance by qualifying at a set leakage current density.
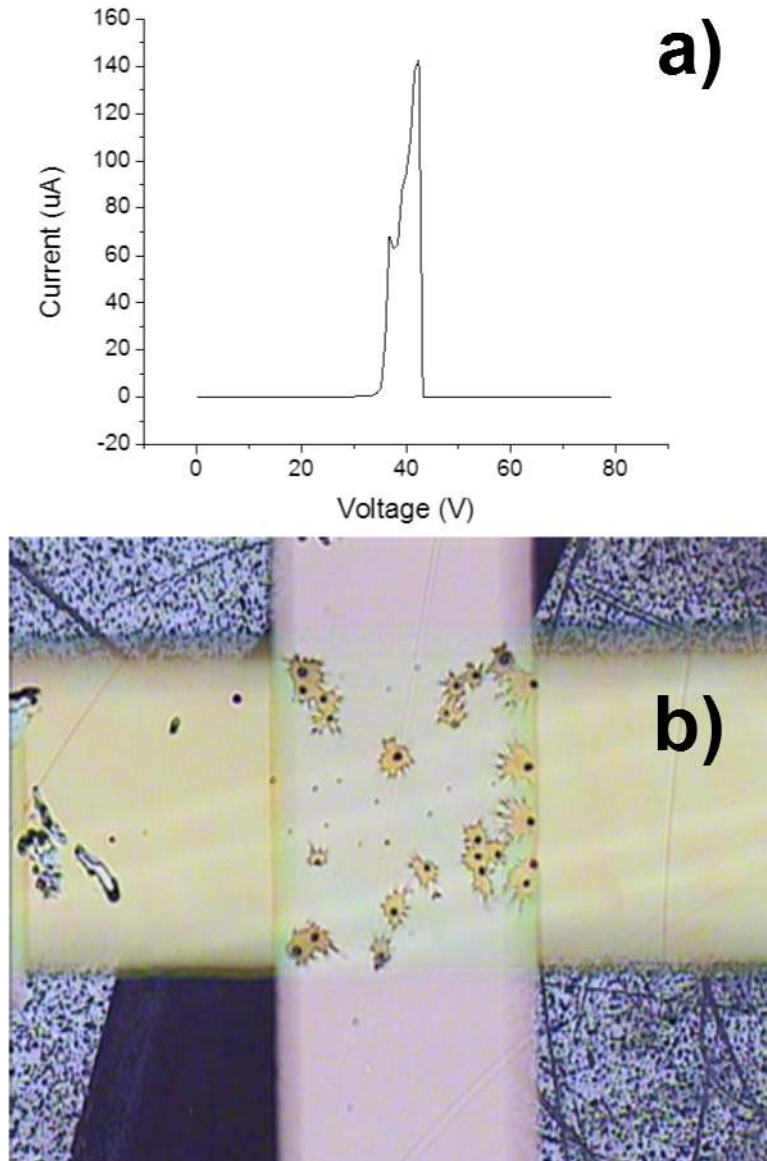
Figure 2.4: Characteristic of a self-healing device (a) I-V characteristic device with self-healing property. The leakage current is significantly reduced after the partial breakdown (b) Top view of the self-healing capacitor after partial breakdown.

Leakage Current (uA) vs **Applied Voltage**

Experimental data
Fitted data

Barrier height = 0.68 eV
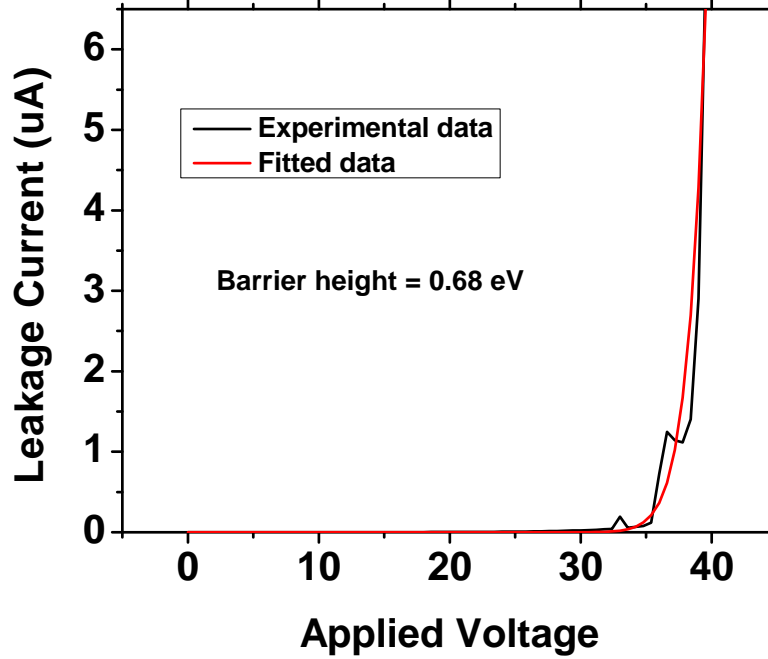
Figure 2.5: Experimental data and Fowler-Nordheim equation fitted data

Table 2.1: Dielectric characteristic of BST/parylene-C composite films

	Reverse Bias	Forward Bias
Film thickness (nm)	280 ± 20	400 ± 20
Effective dielectric constant	$17 \pm 1.5^a \ 22 \pm 2^b$	$17 \pm 1.5^a \ 22 \pm 2^b$
Capacitance density (nF/cm^2)	$55 \pm 5^a \ 71 \pm 6^b$	$55 \pm 5^a \ 71 \pm 6^b$
Dielectric loss (at 1 MHz)	< 0.05	< 0.05
Voltage tolerance (V)	28 ± 5^c	44 ± 4^c
Leakage current density (A/cm^2)	$3.20*10^{-6d}$	$1.19*10^{-7d}$

^{a}Measured at 1 MHz

^{b}Measured at 1 kHz

^{c}Voltage tolerance at 10 μA/cm^2

^{d}Current density at 20 V
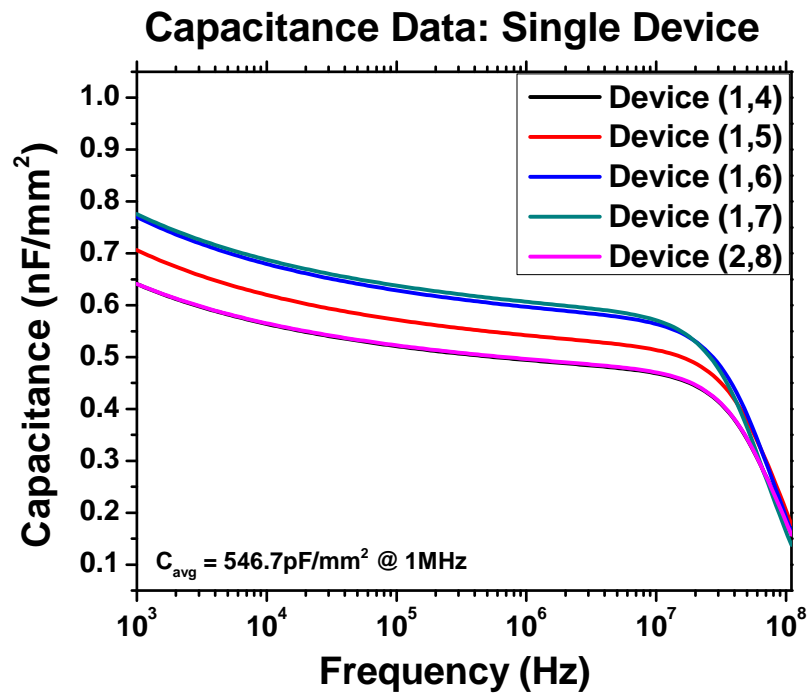
Figure 2.6: Frequency dependent capacitance plot
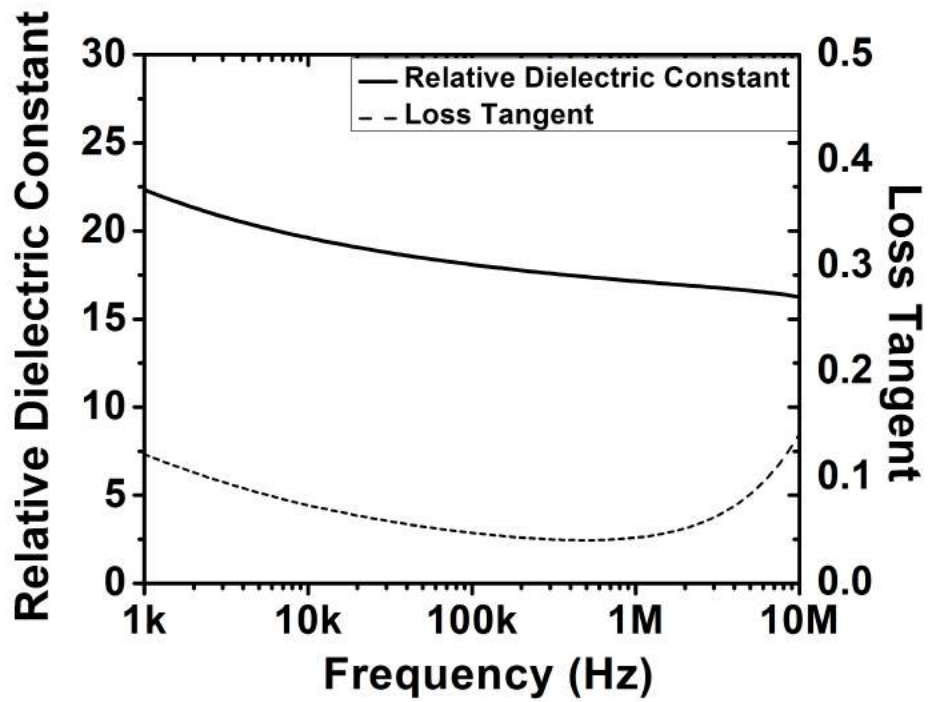
Figure 2.7: Frequency dependent relative dielectric constant and loss tangent
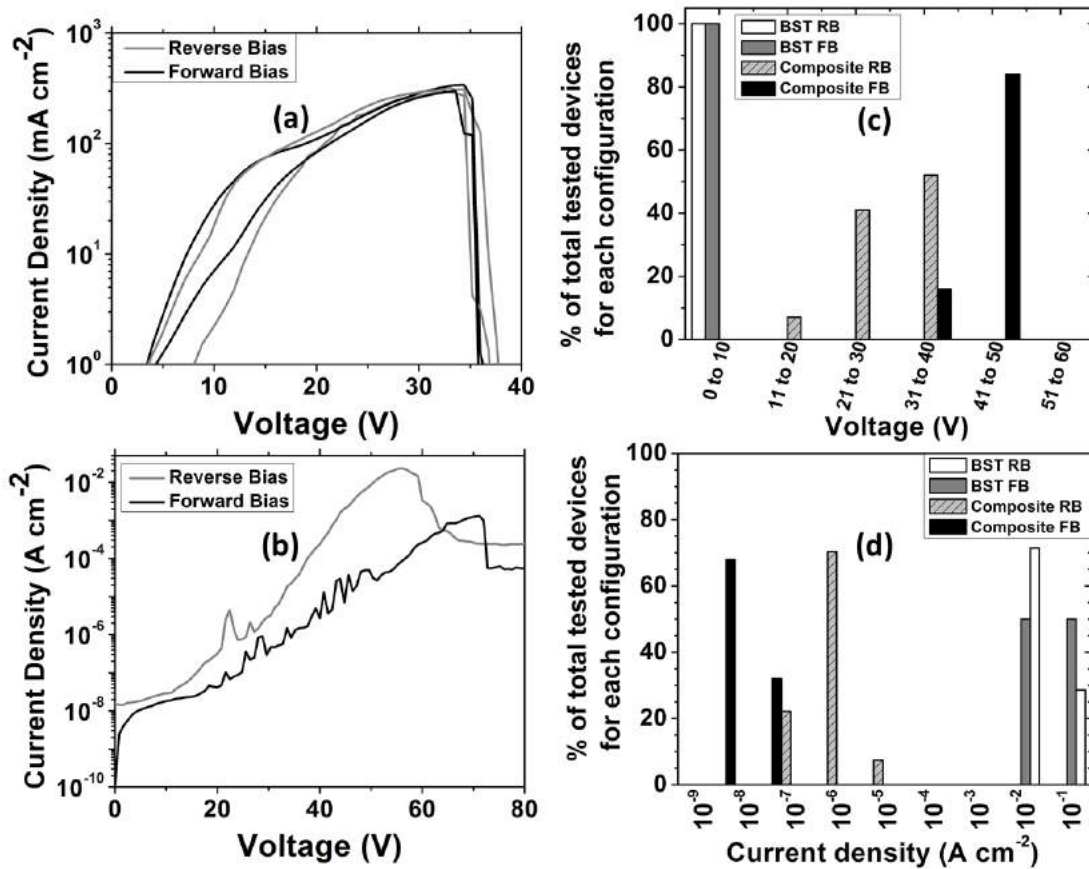
Figure 2.8:   (a) I-V characteristic of BST device (b) I-V characteristic of
BST/parylene-C composite device (c) Voltage binning data at 10 A/cm2 (d) Current binning data at 20V

Chapter 3

Electromigration and its Effect on Field Tolerance

3.1 Introduction

Thin film metal oxide nanoparticle/polymer composites have been extensively examined as an attractive solution for printable and solution-deposited high-k dielectrics. The use of high-k ceramic nanoparticles allows for the formation of a room temperature deposited, solution processed high dielectric constant film without the need for chemical conversion or high temperature sintering. The polymer matrix used in such systems fills the interstitial voids, leading to a higher effective dielectric permittivity, and also passivates the surface states of the nanoparticles, reducing the dielectric loss.[54] These materials have been applied to a number of large area and flexible electronic devices including use as gate dielectrics in thin film transistors, dielectric films in thin film capacitors, and integration into energy storage devices.[51][52][53][55][76][77]

The solution processability and low temperature processing conditions used to create these composites are especially well suited for large area roll-to-roll fabrication, and are of particular interest for large capacitance, high frequency power management

devices.[56] Printable $(Ba,Sr)TiO_3(BST)$/parylene-C polymer/metal oxide composite capacitors exhibit a field strength, frequency, and loss performance competitive with multilayer ceramic capacitors (MLCCs), while offering a low temperature fabrication process and higher total capacitance values than available in MLCCs.[8] These composites also offer performance superior to the competing high-frequency/high capacitance technology, metallized polypropylene polymer film capacitors, including a higher operating frequency, greater dielectric constant, and higher temperature capability.[54][58]

In many capacitor systems, (e.g. ceramic and electrolytic capacitors) the breakdown process leads to runaway damage that destroys the capacitor. In self-healing systems, such as polymer film and ceramic nanoparticle/polymer composites, the point of breakdown is not well-defined. The breakdown process is typically self-limiting, and destruction of the dielectric or electrodes limits the leakage observed in the device. Despite this uncertainty, however, it is possible to determine a voltage tolerance (i.e. the highest practical voltage at which the device can be operated with some low failure rate) by qualifying device samples according to leakage current density.[72] The leakage current in self-healing systems, which typically exhibit filamentary defects, follows a Fowler-Nordheim tunneling characteristic.[66][67] Surface modification can suppress the leakage current in filament-forming capacitor systems and is one accepted approach to improving the voltage tolerance.[8][61][60][62]

The composition and surface condition of the electrodes influence the electrical properties of the capacitors.[78][66][67][69][79] The two major factors that have been demonstrated to have major impact on the Fowler-Nordheim emission type leakage are the surface roughness and the work function. It has been shown, for example, that the surface roughness plays a significant role in the leakage characteristic, and that rougher electrode surfaces reduce the voltage at which the leakage occurs due to the formation of field enhancing asperities.[68] The tunneling current, which is caused by field emission from the electrode surface, is barrier dependent. The work function

of the electrodes therefore also influences the leakage and breakdown field strength of the device.[69][70][71]

Two major classes of failure mechanisms have been proposed for thin film capacitors: filament formation [80] and local conversion of the dielectric to a conducting form.[81]. In bulk BT dielectrics, failure due to both mechanisms has been observed. Failure at fields and temperatures much lower than the electrical or thermal breakdown value of the bulk material has been observed due to oxygen vacancy diffusion. The presence of oxygen vacancies in significant concentration in the bulk BT can cause additional electron injection to compensate for the accumulation of vacancies at the cathode under an applied DC electric field.[82] Other possible alternative failure mechanisms include the formation conducting paths due to surface charge, free charge absorption from humidity, or pinholes.

In devices that exhibit a filamentary failure mechanism, the electromigration parameter of the electrode material is a factor that can affect the field strength tolerance of the capacitor.[51] The electromigration parameter will determine the susceptibility of the electrode to filament formation. Once the filaments are formed, the leakage current increase from the field enhancement at the apex of the wire, and will continue to draw the metal out. The filament grows, increasing the field and current, ultimately leading to a runaway leakage process until Joule heating destroys the metal wire and heals the capacitor. The competing proposed mechanism is the formation of conducting paths in the dielectric, resulting in dielectric breakdown. In this situation, the conducting path is generally proposed to be formed by a change in the molecular structure of the dielectric associated with an interaction with the leakage current. In both cases, the work function is a crucial parameter in determining the breakdown field strength because the charge injection is directly associated with the barrier height. In the filamentary mechanism, the electromigration parameter also plays a significant role in determining the field tolerance, and understanding the influence of the electromigration parameter on leakage and field strength will provide

an additional path to device optimization.

The asymmetric structure of the BST/parylene-C capacitor is an ideal system with which to study the effect of the electrodes' electromigration parameter on capacitor performance. The top and bottom electrodes interface with different physical barriers, providing a controlled experimental environment in which to compare the same electric field on the dielectric with a passivated (parylene-C coated) surface, and a free (porous BST) electrode interface.[72] In this work, we use this asymmetrical relationship to investigate the correlation between voltage tolerance and electromigration susceptibility, while also examining the work function and the surface roughness contribution of the electrodes to the field tolerance of the device.

3.2 Structure and Fabrication Method

The capacitor tested is a 3 mm x 3 mm parallel plate structure with the composite $B_{0.7}S_{0.3}TiO_3$/parylene-C material as the dielectric layer. The top and bottom electrodes are composed of the same metal in all cases. Gold, copper, chromium, aluminum, and silver were used as the electrode materials. Starting with a glass substrate, we thermally evaporated 5 nm of chromium as a wetting/adhesion layer and 40 nm of the electrode metal being investigated. The deposition conditions were tuned for each electrode material to provide a similar surface condition. We patterned the bottom electrodes via photolithography and wet etching. The nanoparticle solution consisted of 8 to 12 nm diameter $B_{0.7}S_{0.3}TiO_3$ nanoparticles uniformly dispersed in ethyl alcohol at a concentration of 20 mg/ml without surfactant.[8] We spin-coated the nanoparticle solution on top of the bottom electrodes to form the dielectric layer using a two-step dynamic spinning process. The solution is dispensed during the first spin step at 500 rpm for 15 seconds, and the second spin step was run at 1000 rpm for 45 seconds. After drying each layer, the spin-coat process was repeated four times to compose the desired thickness of the dielectric. Parylene-C was vapor deposited on

top of the BST film via chemical vapor deposition after a 12 hour bake at 80 °C to re-
move residual solvents.[72][83] This process results in an overlapping BST/parylene-C
composite layer, with a total thickness of approximately 300 nm. The top electrode
is thermally deposited with a shadow mask to complete the device. The complete
device stack and the cross section of a single device are shown in Fig. 6.1.

3.3   Testing Method

The capacitance and loss of the device were measured using an Agilent 4294 impedance
analyzer with a 42941A active impedance probe. The polymer film capacitors exhibit
a self-healing behavior, where the local degradation of electrodes occurs during a lo-
cal failure that results in the recovery of the capacitor. A definite breakdown voltage
is therefore difficult to define.[65] As an alternative, voltage tolerance is established
using a threshold leakage current density above which the device is considered to
fail. A safety factor (typically between 1/2 and 1/5th the maximum voltage) is then
applied to define a safe operating voltage. This leakage current density corresponds
to a current density greater than acceptable for the application, but less than the
current density associated with the healing process. In our test, we measure the I-V
characteristic of each capacitor from 0 V to 80 V. The step size is 0.8 V and the
integration time is 250 ms. A positive bias is defined as applying positive voltage on
the bottom electrode, using the top electrode as the ground reference. The leakage
current density is chosen so that the device is biased well below the level of catas-
trophic failure or healing action of the electrodes. In this experiment 10 μA/cm^2 is
used. The voltage tolerance test is performed on 32 devices per substrate via a switch
matrix system (Keithley 7001) and source measurement unit (Keithley 2400) with an
automated LabView program. The capacitors are connected to the switch matrix
system via flex circuit which eliminates damage to the capacitors due to probing.
Previous studies have shown that the metal ion migration process can be enhanced

due to high humidity [84] [85]; therefore, all of our electrical tests were conducted under ambient conditions.

The thickness of the dielectric layer varies slightly due to both process variation and the surface energy of each electrode material, which affects the wetting of the nanoparticles; therefore, the voltage tolerance is normalized with the thickness of the dielectric film to obtain the field tolerance. The dielectric thickness and the surface roughness are measured using contact profilometry and atomic force microscopy.

3.4   Result and Discussion

The dielectric and electrode characteristics of the BST/parylene-C composite capacitor with different metal electrodes are summarized in Table 3.1. The dielectric thickness varies between 300 - 400 nm, and the effective composite relative dielectric constant k is approximately 13 at 10 kHz for each case. The frequency dependent relative dielectric constant is shown in Fig. 3.2. Our data show similar k values and frequency stability to previously reported devices fabricated using the same approach.[8][72] The pure parylene-C dielectric devices have higher breakdown field ranging from 500 to 2500 MV/m depending on the thickness of the film.[86][87] This is higher than our composite film; the dielectric constant of the parylene-C capacitor, however, is much lower leading to a smaller overall energy density for the system.

The field tolerance is investigated at a leakage current density of 10 μA/cm^2 under positive and negative bias conditions. The positive bias field tolerance is higher than the negative bias field tolerance, consistent with previous results.[72] The silver, aluminum, gold, copper, and chromium electrode devices show 64 %, 29 %, 28 %, 17 %, 33 %, improvement in field tolerance, respectively when comparing the positive biased condition to the negative biased condition. This result demonstrates that the different physical barrier resulting from the two dielectric/electrode interfaces plays a significant role in the field tolerance.

Field tolerance is plotted against electrode metal and its electromigration parameter in Fig. 3.3. A larger magnitude of the electromigration parameter, an indication of higher susceptibility to electromigration effects, results in lower field tolerance. The plot shows a similar trend for both positive and negative bias conditions. The bias polarity dependence indicates that the parylene-C interface to the top electrode has a higher resistance to filament formation than the free surface at the bottom interface. Once the filament is formed, the enhanced field leads to larger leakage. The increased leakage current continues to draw out the filament which, if continued, ultimately leads to local failure from Joule heating. The field tolerance of the capacitor exhibits an 89 % (31.7 MV/m) increase for positive bias condition and 350 % (44.5 MV/m) increase for negative bias condition when employing copper instead of silver as the electrode. The magnitude of the electromigration parameter of copper is lower than that of silver by 15.5. An additional 3.4 MV/m increase in the field tolerance under positive bias is observed when chromium, which is even less susceptible to electromigration, is used instead of copper as the electrode material.

It is possible that the movement of oxygen vacancies also contributes to the observed breakdown in these devices.[82] The BST nanoparticles used are synthesized by a solvothermal method at low temperature under an -OH rich environment and the native presence of oxygen vacancies, which is essential for this failure mode, is expected to be low.[89] The introduction of the polymer layer into the dielectric also passivates the surface states and has been demonstrated to reduce the contribution due to surface conduction, pinholes, and moisture ingress.[8]

The capacitor leakage is non-ohmic in nature and dominated by Fowler-Nordheim tunneling.[74][73][75] Two other possible contributing characteristics of the electrodes, the work function and surface roughness, were also examined. Other groups have shown a significant work function dependence on capacitor leakage and breakdown.[70] The magnitude of the tunneling current in a Fowler-Nordheim system is dependent both on the barrier height of the system and the strength of the field applied. The

field tolerance and the work function are shown in Fig. 3.4a. The field tolerance of the devices examined appear to have little or no correlation with the work function. The thick dielectric layer in our system may reduce the field away from the filament, leading to a smaller contribution of the work function to current transport. The electrodes in our system are relatively smooth and are deposited using a wetting layer and thermal evaporation. This yields a similar surface characteristic among samples and minimizes the surface roughness contribution. The RMS and Rmax values of each electrode are shown in Table 3.1. The plot of field tolerance and surface roughness is shown in Fig. 3.4b. The plots show a slight positive correlation between the surface roughness and the field tolerance.[66][67][68] Electrode asperities associated with surface roughness can also form the initial sites for filament formation.

3.5 Conclusion

We investigated the effect of the electromigration parameter on the field tolerance of nanoparticle BST/parylene-C composite capacitors. The fabrication process is tuned to yield similar surface conditions to ensure that the contribution of surface roughness is as similar as possible from each electrode. The influence of work function is also investigated to verify that the electromigration parameter is the dominant contributing factor. This correlation holds for both the free electrode interface and surfaces that have been coated with the composite polymer filler. This work demonstrates that tuning the electromigration parameter is a crucial consideration for improving voltage tolerance, and should be considered together with the traditional approaches to improving breakdown performance by engineering the work function and reducing surface roughness. This observation offers an additional route to performance optimization for thin film inorganic/organic composite capacitors.
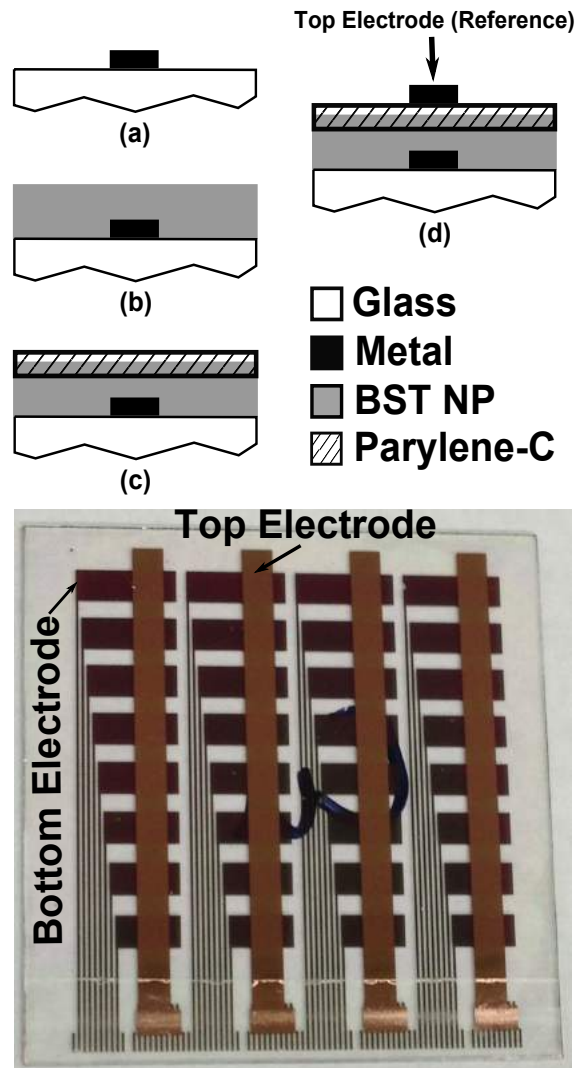
Figure 3.1: Schematic cross section of the BST/parylene-C composite capacitor on a glass substrate (top). The dielectric thickness is approximately 300 nm, and the top electrode serves as the reference electrode. The same metal is used for the top and bottom electrodes, with the exception of a thin chromium adhesion/wetting layer applied to the glass prior to deposition of the bottom electrode. The parylene coating partially penetrates the nanoparticle film. The deposition is self-limiting; parylene initially fills the voids between the nanoparticles until a solid composite is formed and deposition proceeds on the surface. The fabricated capacitor array is also shown on the bottom. The electrodes are outside of the active region which minimizes the damage during the testing.
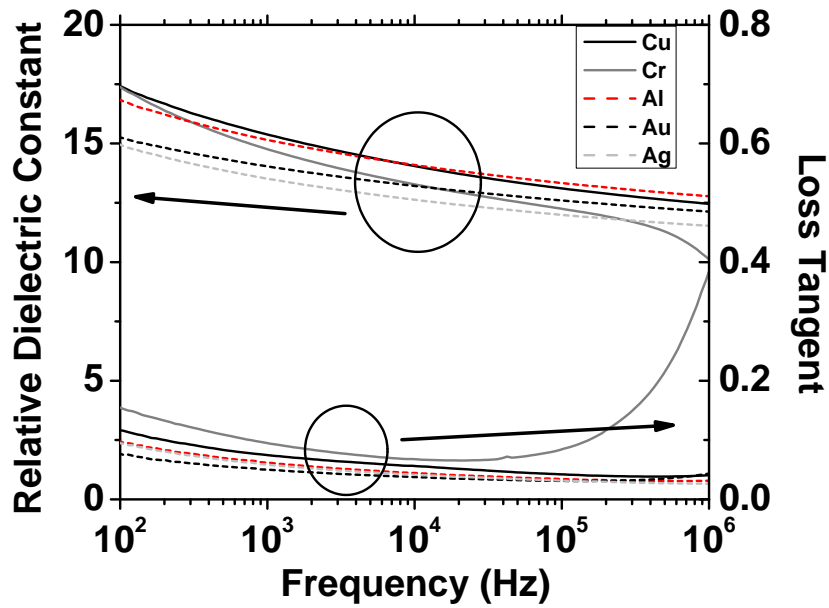
Figure 3.2:   This figure shows the frequency dependent relative dielectric constant
(top group) and the loss tangent (bottom group) of the BST/parylene-C capacitors
with silver, aluminum, gold, copper, and chromium electrodes. The high resistivity of
the chromium electrodes leads to an unusually large effective series resistance (ESR),
leading to an electrode-limited frequency response. In general, the electrode material
has minimal influence on the dielectric property.

Table 3.1: Dielectric and Electrode Properties

	Ag	Al	Au	Cu	Cr
Delectric Material	BST/Pary-C	BST/Pary-C	BST/Pary-C	BST/Pary-C	BST/Pary-C
Delectric Thickness (nm)	340 ± 20	400 ± 20	380 ± 20	380 ± 20	300 ± 20
k[a]	12.6	14.1	13.2	14	13.3
Capacitance[a] Density (nF/cm^2)	32.5	31.1	30.9	32.7	39.1
Field Tolerance (MV/m)[b]	35.5[c] 12.7[d]	51.8[c] 40.3[d]	54.1[c] 42.3[d]	67.2[c] 57.2[d]	70.6[c] 47.1[d]
Electromigration Parameter[88]	-21	-12	-8	-5.5	–[e]
Work Function (eV)	4.52	4.06	5.1	4.53	4.5
Electrode Thickness (nm)	40	40	40	40	40
Electrode Roughness (nm)	RMS: 3.94 Rmax: 26.6	RMS: 4.42 Rmax: 12.6	RMS: 3.24 Rmax: 20.7	RMS: 2.81 Rmax: 20.9	RMS: 3.05 Rmax: 17.3

[a]Measured at 10 kHz

[b]Field Tolerance at 10 μA/cm^2

[c]Forward Bias

[d]Reverse Bias

[e]The electromigration parameter for chromium does not appear to be reported in the literature.
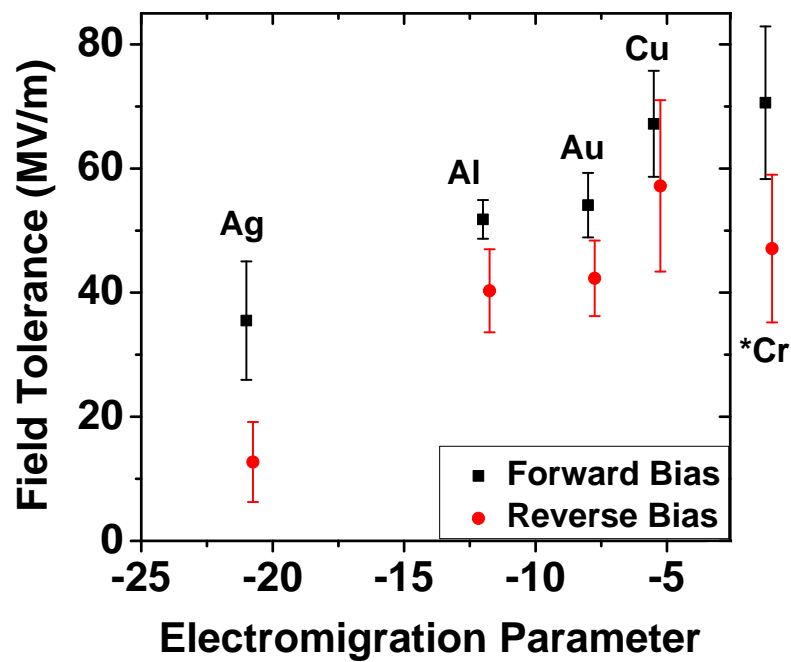
Figure 3.3: The field tolerance of BST/parylene-C composite capacitors plotted against the electromigration parameter of the silver, aluminum, gold, and copper electrodes. The electromigration parameter for chromium does not appear to be reported in the literature and is plotted outside the group.
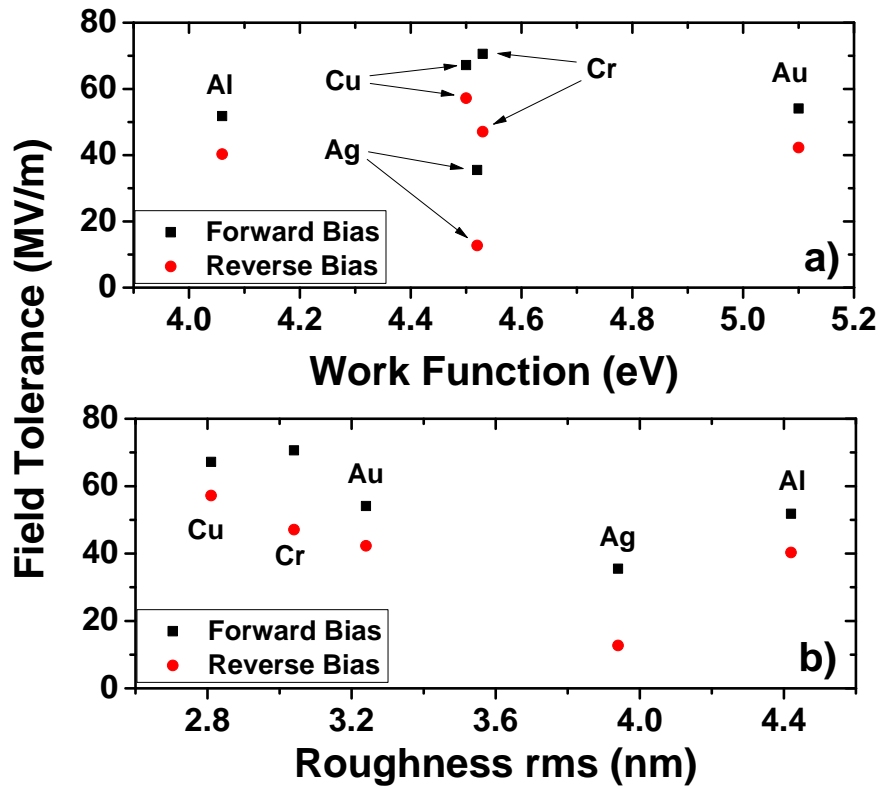
Figure 3.4: Field Tolerance of the BST/parylene-C composite capacitors plotted against a) Work Function and b) Surface Roughness of the silver, aluminum, gold, copper, and chromium electrodes.

Chapter 4

Mechanical Properties and Reliability

Understanding the mechanical properties are vital for flexible electronic devices as the devices may be subjected certain physical condition during roll-to-roll fabrication process and also during operation. The mechanical properties of the device indicate the physical conditions which the device can tolerate. In this section, we present the test result for fracture toughness, hardness (Youngs modulus), and adhesion of the fabricated capacitors. We will also demonstrate the reliability of the fabricated capacitors through age and elevated tests.

4.1 Fracture Toughness Test

The fracture toughness test determines the amount of strain the meta-capacitor can withstand before cracking occur either in the electrode or the dielectric layer. The cracking of the metal leads to dramatic decrease in the capacitance, and the cracking of the dielectric leads to shorting of the device. Hence, the change in resistance and/or capacitance before and after applying the strain indicates the failure. The device was subjected to strain by bending the sample around the cylinders with the radius of 2

cm, 5 cm, 10 cm, and 50 cm which correspond to strain of 0.438 %, 0.175 %, 0.0872 %, and 0.0174 % respectively. The test setup and method is shown in Fig. 4.1. The result of a single device is shown in the table below (Table 4.1). Multiple devices were tested, and the meta-capacitors show no sign of failure after applying up to 0.438 % of strain.
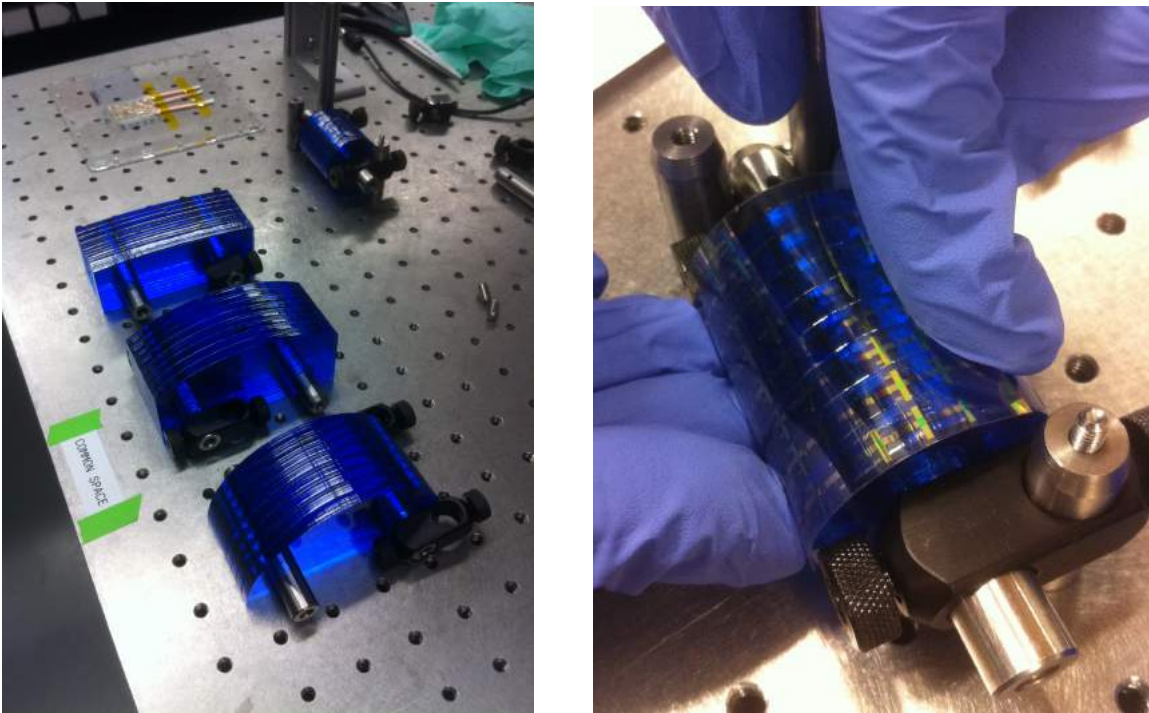
Figure 4.1: Test setup and method for fracture toughness

4.2 Hardness and Youngs Modulus

The hardness and Youngs modulus test determines the elastic property of the dielectric films. The hardness and Youngs modulus measurements are taken using a nanoindenter. The data taken for the meta-capacitor dielectric layer is shown in Fig. 4.2. The nanoindentation test consists of three parts. First part is the indentation, and the hardness is recorded at the peak load on sample. The second part is the

Table 4.1: Result for fracture toughness test

Bending radius (cm)	Strain	Capacitance (nF)	Resistance (ohm)
-	0	380	O.L.
50	0.0174 %	380	O.L.
10	0.0872 %	380	O.L.
5	0.175 %	380	O.L.
2	0.438 %	380	O.L.

10 sec hold at peak load on sample which indicates the elastic deformation of the dielectric film. The last part is the elastic recovery in which the youngs modulus is extracted. The hardness of our dielectric film is 0.352 GPa, and the youngs modulus is 32.9 GPa. The results are shown in Table 4.2 in comparison to the silica standard. This result shows that our materials is much softer and more elastic than silica.

Table 4.2: Nano-indentation result

	Composite film	Silica
Hardness (GPa)	0.352	6.65
Young's Modulus (GPa)	32.9	70.9

4.3 Adhesion Test

The adhesion test measures the resistance of the thin film capacitor to separation from the substrate. The test method is based on ASTM 3359 method B for thin films with thickness less than 250 μm. The capacitor is scribed to form a 5 x 5 square grid with line separation of 1 mm, shown in Fig. 4.3, and the adhesion is tested by pulling the grid area with 3M magic tape (shown in Fig. 4.4). The device exhibits class 5B adhesion as almost none of the grid area was removed during the test. The
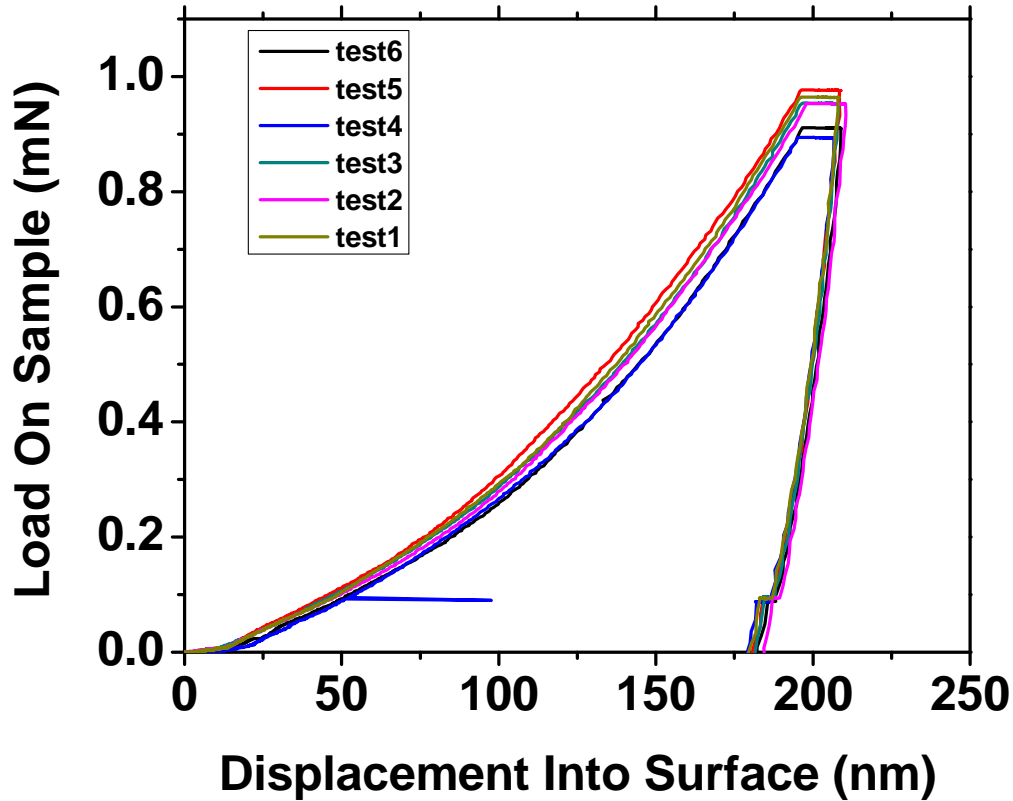
Figure 4.2: The data for hardness test on BST + parylene film

classification table is shown in Table 4.6[90], and the zoomed in grid before and after the tape test is shown in Fig. 4.5.

4.4 Age Test and Reliability

Aging tests were conducted on metacapacitors fabricated on flexible substrates under 50 V bias at 125 C. The capacitors were fabricated using the spray-coating process with thermally evaporated copper electrodes. The electrodes are 400 nm thick. The bottom electrodes are lithographically patterned, and the top electrodes are patterned using a shadow mask. This switch matrix structure, shown in Fig. 4.7, enabled
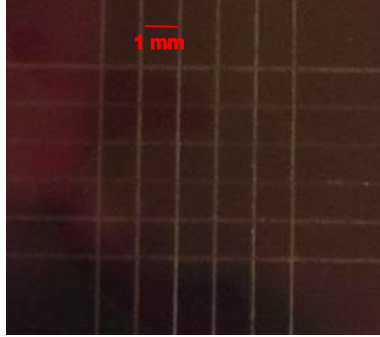
Figure 4.3: Grid for Adhesion test

statistical analysis of the sample. The fabricated capacitors were pre-conditioned with a slow ramp at 1 V/s up to 50 V and held at 50 V for the age test at 125 C for 1100 hours. The capacitances of both the biased and unbiased devices were measured every 100 hours at room temperature to determine the condition of the capacitors.

The complete 1100 hour test is shown in Fig. 4.8. There is a 43 % drop in capacitance during the first 100 hours of the age test for both the biased and the unbiased capacitors. The fact that the capacitance drop occurred in both the biased and unbiased capacitors suggests that the FA continues to polymerize in the dielectric layer. The capacitance is stabilized after the first 100 hours. The capacitances for both the biased and unbiased devices exhibit less than 5 % variation during the subsequent 1000h test. The initial leakage of the capacitors is 800 nA/cm2. However, the leakage decreases during the first 400 hours of the age test. The leakage is 160 nA/cm^2 at the end of the first 400 hours and stabilizes thereafter.

4.5 Conclusion

Mechanical properties are vital for flexible electronic devices as the devices may be subjected certain physical condition during roll-to-roll fabrication process and also during operation. The mechanical properties of the device indicate the physical conditions which the device can tolerate. We have demonstrated that the fabricated
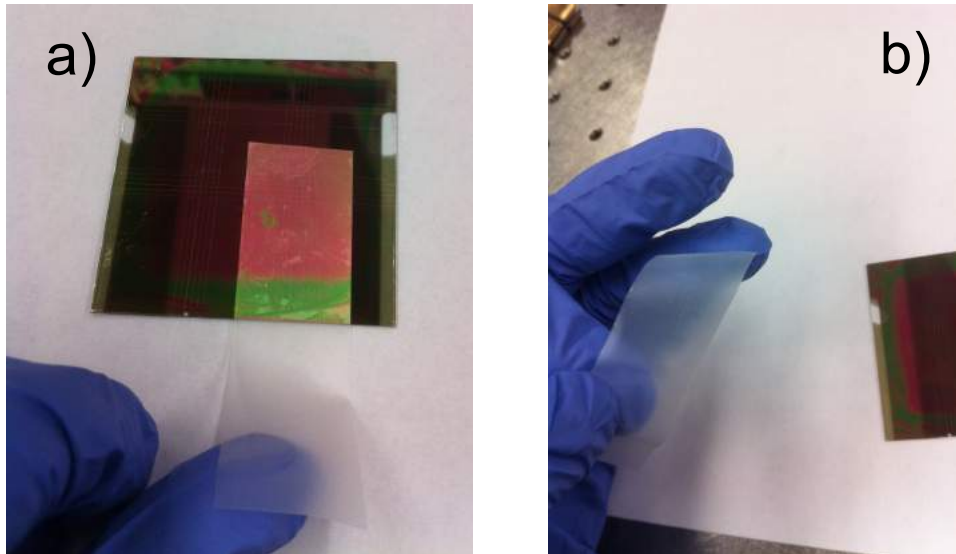
Figure 4.4: The tape test method
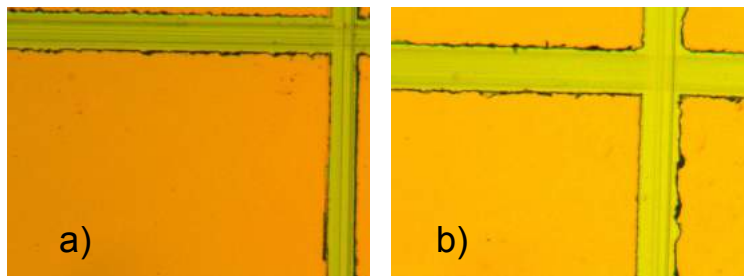
Figure 4.5: Adhesion test result

devices can tolerate more than 0.4 % strain with superior adhesion to flexible substrate. In addition, the fabricated capacitor exhibits less than 1 % delta in capacitance during the 100 hour age test and does not go though a phase transition that leads to significant capacitance change with in the temperature range of interest.
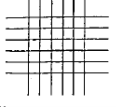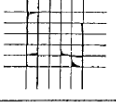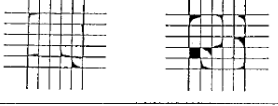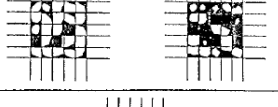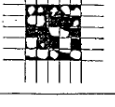
CLASSIFICATION OF ADHESION TEST RESULTS		
CLASSIFICATION	PERCENT AREA REMOVED	SURFACE OF CROSS-CUT AREA FROM WHICH FLAKING HAS OCCURRED FOR SIX PARALLEL CUTS AND ADHESION RANGE BY PERCENT
5B	0% None	
4B	Less than 5%	
3B	5 - 15%	
2B	15 - 35%	
1B	35 - 65%	
0B	Greater than 65%	

Figure 4.6: ASTM 3359 Table
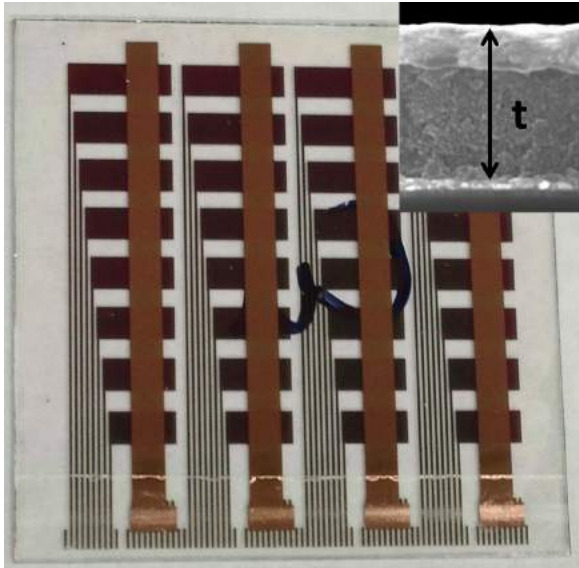
Figure 4.7: Age test sample designed to be interfaced with 7001 switch matrix system to obtain statistical data.
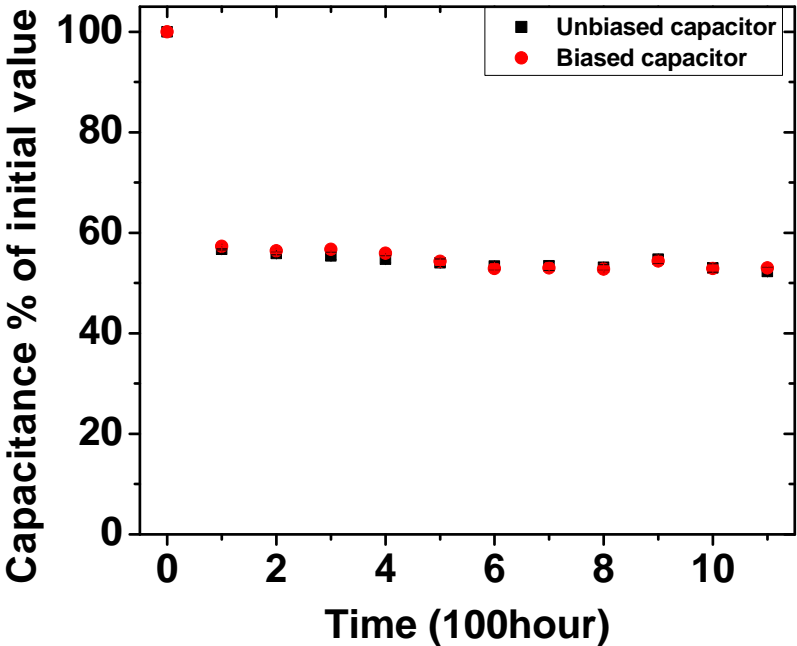
Figure 4.8: Age test conducted at elevated temperature over 1100 hours.

Part II

Printed OTFT Optimization

Chapter 5

Pneumatic Printing Method

5.1 Introduction

Pneumatic printing process simultaneously enables patterning and deposition of multiple materials. This approach has particular application to the fabrication of organic thin film transistors with high performance and yield, but can also be applied to other material systems that are printed including insulators, metals, and active elements. The technique is also capable of depositing multiple materials on the same substrate.

There are many other printing techniques that have been studied extensively for printing electronic such as inkjet printing, screen printing, and gravure printing. Inkjet printing utilizes a printhead with piezoelectric crystals to deposit desired materials on a substrate via droplets.[91] The solution forms meniscus at the end of the printhead, and with precise control over the mechanical movement of the piezoelectric material through electrical signal (usually periodic), the droplets form and ejected from the printhead tip. The advantage of using inkjet printing method is precise control over the droplet formation and deposition. The droplet size is determined by the printhead nozzle diameter and the waveform. The thickness of the deposited materials depends on the printing conditions and the solution concentration. Inkjet printing method enables the ability to achieve moderately hight resolution (5 - 20

um) and thickness control down to around 100 nm. The disadvantage of the inkjet printing methods are 1) nozzle clogging tend to occur when printing high viscosity materials such as organic dielectrics due to deposition via droplets, 2) the thickness and uniformity of the printed film is difficult to control due to coffee ring effect (complicated method can be used ie solvent and anti-solvent to improve uniformity), 3) aligned crystal growth is not possible. Screen printing offers patterned deposition through openings on the printing screens. Thick layer (> 10 um) deposition can be achieved through screen printing with good uniformity. Additionally, solution wide range of viscosity can be deposited. The main limitations of the screen printing method are low resolution (> 100 um), and inability to control crystal growth for organic semiconductor. Therefore, the screen printing method is suitable technique for printing electrode materials and dielectrics due to its ability to deposit highly viscous materials and pattern. (citation for screen printing). Gravure printing can achieve patterning with recesses and surface relief on the surface of the master, and this printing technique allows for thickness control over wider range (1 to 8 um) with high resolution less than 20 um. The main advantage of using gravure printing is the high quality layer, superior reproducibility and throughput. However, there are a few disadvantages associated with gravure printing as well. First, the initial cost is high due to patterned cylinder manufacturing, and each customization or alteration of design require additional master. Second, the multi-material deposition require material-solvent compatibility consideration as the new solution can contact the previously deposited patterns. Third, as with inkjet and screen printing methods, the control over crystal growth such as alignment is not possible. Some of the solution-based deposition techniques to achieve aligned crystal growth for organic semiconductor will be discussed in detail in the next chapter.

The main advantages of pneumatic printing technique over the other printing techniques such as inkjet, screen printing, and gravure printing, therefore, are 1) simple set-up and process, 2) multi-material layered deposition applicable to wide range of

solution viscosity, 3) control over crystal growth. The manipulation of crystal growth will be discussed in the next chapter. This method for performance optimization and patterning has great potential for advancing printed electronics.

5.2   Pneumatic Printing Process

Fig.   5.1 shows the set-up for the pneumatic printing process. The syringe and the needle serve as the solution reservoir and the printing nozzle. The reservoir is interfaced with EFD pressure controller to provide vacuum and forward pressure. The Bluefox camera is there to enable alignment of different deposition layers. Spring-loaded sample holder allows for levelling of the sample, and it is equipped with a thin film heater not shown) for substrate temperature control. The camera, sample holder, and the syringe are interfaced with a 3D stage to control the position and printing motion. Custom LabView program was written to navigate the printing process. Fig. 5.2 illustrates the pneumatic printing steps. The printing process starts of with positioning the nozzle to the desired position with 3D stage, and lowering the nozzle to specific printing height, h, shown in Fig. 5.2 (1). An appropriate level of vacuum is applied to the reservoir to both keep the solution from dripping out, and to suspend the meniscus. A forward pressure is then applied for a short period of time, typically 10 - 20 ms, to contact the meniscus to the substrate surface shown in Fig. 5.2 (2). At this moment the capillary force keeps the meniscus attach to the surface even after applying the forward pressure and same level of vacuum is applied as before. The nozzle starts the printing with defined direction with defined printing speed, and the solution is drawn out of the nozzle via capillary action as shown in Fig.   5.2 (3). Once the desired printing is done, the nozzle is raised to a height greater than the printing height, h, to separate the meniscus contact with the substrate. A trace of desired material has been drawn on the substrate. The key parameter such as the vacuum, forward pressure, printing height, substrate temperature and printing height

will dictate the morphology and pattern of the printed material.

5.3   Printing Electrode

Silver electrodes were printed to demonstrate the applicability of pneumatic printing process for printing conductive materials. The 3D illustration of the silver electrode printing process is shown in Fig. 5.3 (a) - (d). The printing process is as described in previous section - (a) Lower the nozzle to printing heigh,h. (b) A forward pressure is then applied for 10 ms to establish contact between the meniscus and the substrate surface. (c) The 3D stage initiates printing with defined direction at specified printing speed. (d) Once the desired printing is done, the nozzle is raised to a height greater than the printing height, h, to separate the meniscus contact with the substrate. The width of the printed electrodes are determined by the gauge/diameter of the nozzle. In our case, the printed electrode width is around 300 um. The smallest line spacing achieved is 30 - 45 um, and this is limited by the step size of the 3D stage. Continuous conductive silver film with smooth edge can be printed as shown in Fig. 5.4. The smooth edge of the printed electrodes is particularly advantageous in printed thin film transistor application as it results in well defined channel width and length. Fifteen devices were fabricated to study the repeatability and control of the printed silver electrodes. The fabricated source, drain, gate device, shown in Fig. 5.5, have average channel length of 100 ± 11 um.

5.4   Printed Inverter

The performance of the organic semiconductor based printed thin film transistors has increased dramatically in the past few years, and their potential in integrated circuits and flat-panel display is apparent. One of the most basic and essential building blocks in those complementary digital circuit applications is the inverter. Therefore,

fully-printed organic TFT inverters with pneumatically printed source, drain and gate electrodes, and drop-casted organic semiconductor are fabricated to demonstrate the feasibility of employing the pneumatic printing technique for advancing printed electronics.

5.5 Fabrication Method

For sample preparation, the PET substrates were cut into 5 cm x 5 cm size. The square PET samples are cleaned with acetone, IPA, and DI water. The gate electrodes are printed using the pneumatic printing method described from the section earlier followed by an hour post bake at 100 ∘C. Then 1 um of parylene is deposited on the samples as the gate dielectric. HMDS spin-coated on the parylene to increase pinning of the silver ink. The source and drain electrodes are printed using the pneumatic printing method followed by an hour post bake at 100 °C. TIPS-pentacene (10mg/ml in Tetralin) and DPP-CN (10mg/ml in chlorobenzene) are then drop-casted on their respective S/D area followed by 15 min bake at 90 °C. The channel length is 100 μm and the channel widths are 2000 μm and 4000 μm for p-type and n-type channel respectively. The cross-section of the printed TFT is shown in Fig. 5.6 a). The microscope image of the printed S/D/G electrodes for the p-type and the n-type devices are shown in Fig. 5.6 b) and c) respectively. The p-type 2000 μm channel width devices have average channel length of 104.4 $\pm$ 12.5 μm, and the n-type 4000 μm channel width devices have average channel length of 97 $\pm$ 8 μm. The top-view of the complete inverter is shown in Fig. 5.6 d).

All the electrical characterizations were conducted in ambient environment using Keithley 2400 source measuring unit interfaced with Labview.

5.6 Result and Discussion

The inverter structure in shown in Fig. 5.7. In order to have a symmetric transition between the on and off state, the on-current of the p- and the n- type transistor needs to be matched. Diketopyrrolopyrrole-cyanovinylene-4-nitrophenyl (DPP-CN) and TIPS-pentacene are chosen to be the n-type and p-type material respectively. The typical transfer characteristics of the printed electrode TFT with drop-casted organic semiconductor for both p- and n-type devices are shown in Fig. 5.8. As we can see from the IV plot, the on-current of the TIPS-pentacene transistor is about 2x of that of the DPP-CN device. Therefore, the optimal channel width ratio for the inverter is 2:1 (width of the n-type channel to that of the p-type).

In an ideal inverter, the high and low V_{out} should be close to Vdd and ground respectively. The transfer characteristic of the fabricated inverter is shown in Fig. 5.9 a). The Vdd is 40 V in this case. When input voltage is low (< 15 V) the output voltage of 40 V is obtained. The output voltage is decreased to 0 V when the input voltage increased above 15 V. The maximum gain, which is the steepness of the transition region of the inverter characteristic, we obtained was 15.9, and V_M, the voltage midpoint, is about 15 V. The transfer characteristics of 7 inverters are shown in Fig. 5.9 b) to illustrate the process variation in the inverter fabrication. The average gain and standard deviation of the devices are summarized in Table 5.1. The average gain is 10 and the standard deviation is 1.24. The results show that the pneumatic printing technique can be employed to fabricate inverter with fairly uniform characteristics.

Table 5.1: Average gain and V_m of the printed inverter

	Gain	V_m (@ max gain)
Average	10.03	24.4
ST Dev	1.24	2.87
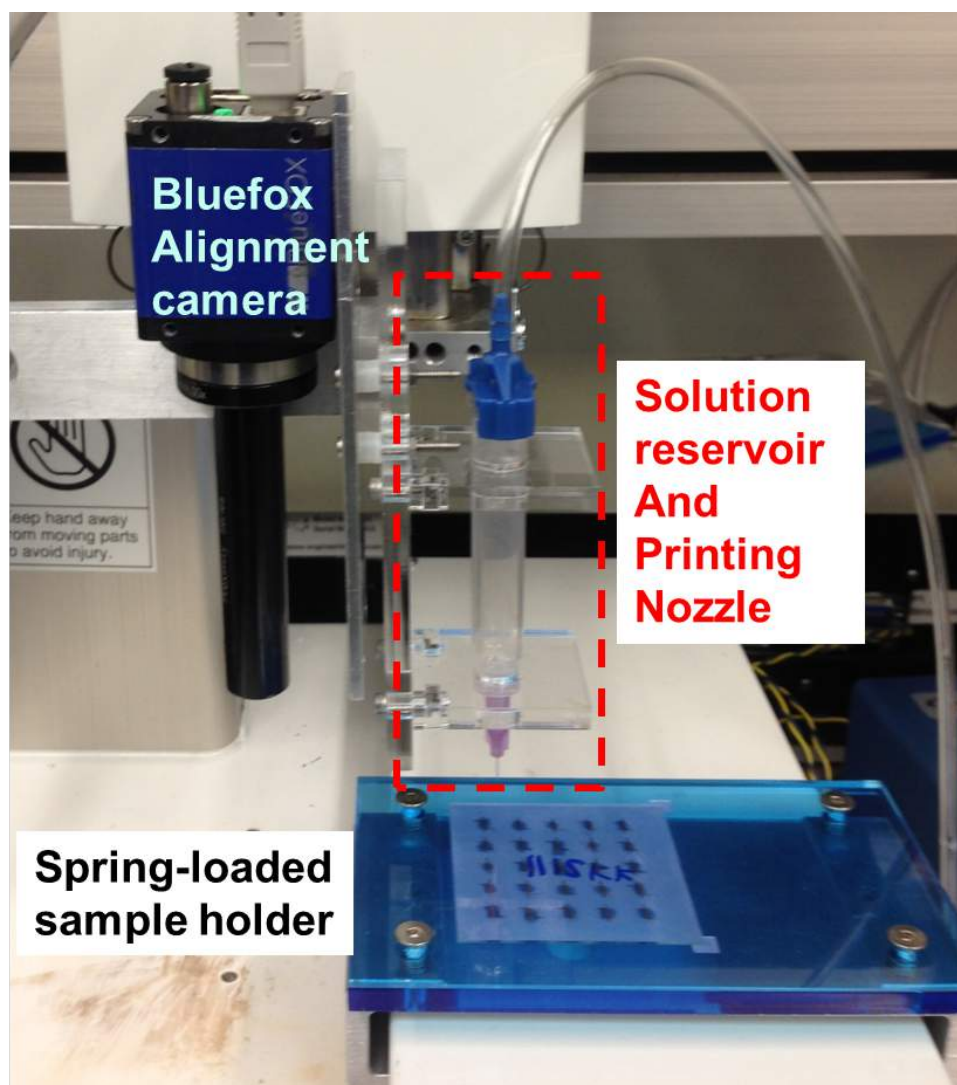
Figure 5.1: Pneumatic printer set-up. The syringe and the needle serve as the solution reservoir and the printing nozzle. The reservoir is interfaced with EFD pressure controller to provide vacuum and forward pressure. The Bluefox camera is there to enable alignment of different deposition layers. Spring-loaded sample holder allows for levelling of the sample, and it is equipped with a thin film heater (not shown) for substrate temperature control. The camera, sample holder, and the syringe are interfaced with a 3D stage to control the position and printing motion.
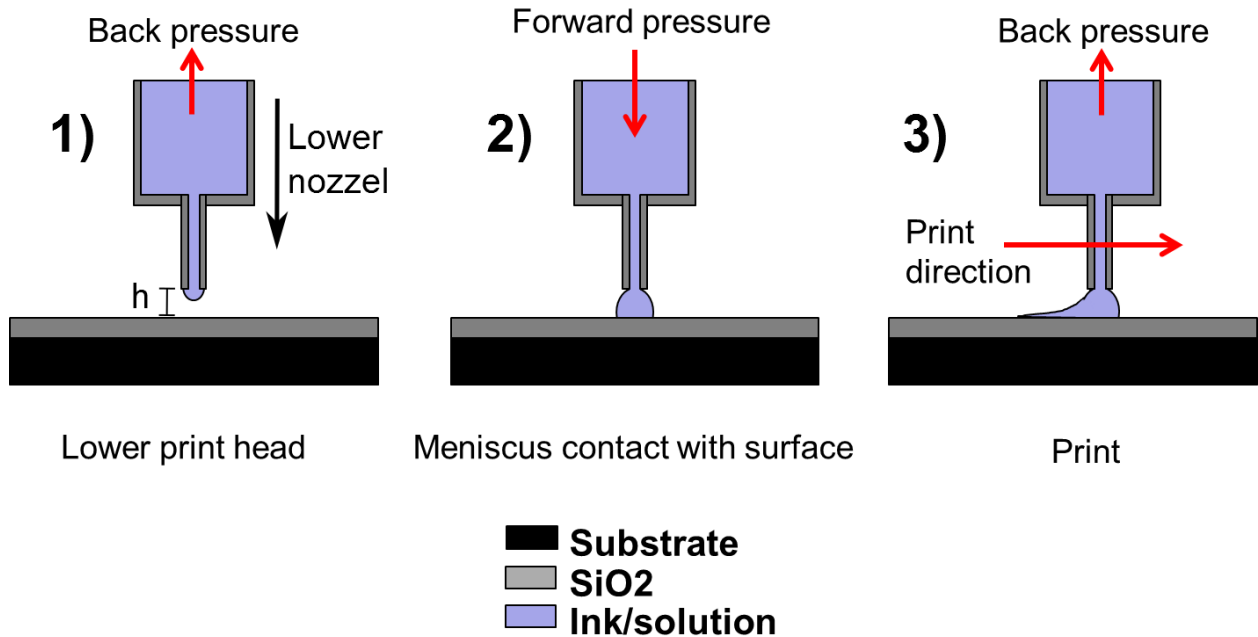
Figure 5.2: Illustration of the pneumatic printing process. **1)**. An appropriate level of vacuum is applied to the reservoir to both keep the solution from dripping out, and to suspend the meniscus. **2)** A forward pressure is then applied for a short period of time, typically 10 - 20 ms, to contact the meniscus to the substrate surface. At this moment the capillary force keeps the meniscus attach to the surface even after applying the forward pressure and same level of vacuum is applied as before. **3)** The nozzle starts the printing with defined direction with defined printing speed, and the solution is drawn out of the nozzle via capillary action. Once the desired printing is done, the nozzle is raised to a height greater than the printing height, h, to separate the meniscus contact with the substrate. A trace of desired material has been drawn on the substrate.
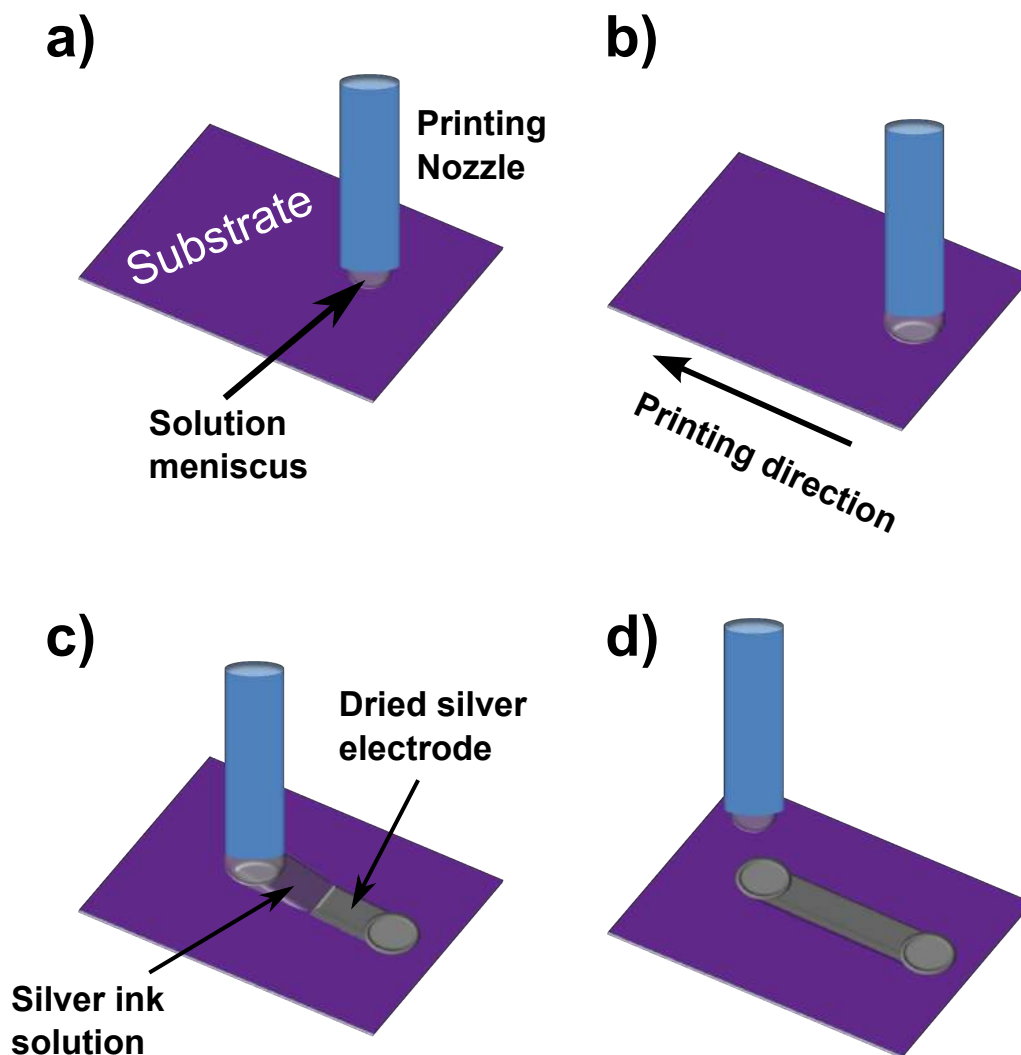
Figure 5.3: Printing process of silver electrode. a) Lower the nozzle to printing heigh,h. b) A forward pressure is then applied for 10 ms to establish contact between the meniscus and the substrate surface. c) The 3D stage initiates printing with defined direction at specified printing speed. d) Once the desired printing is done, the nozzle is raised to a height greater than the printing height, h, to separate the meniscus contact with the substrate.
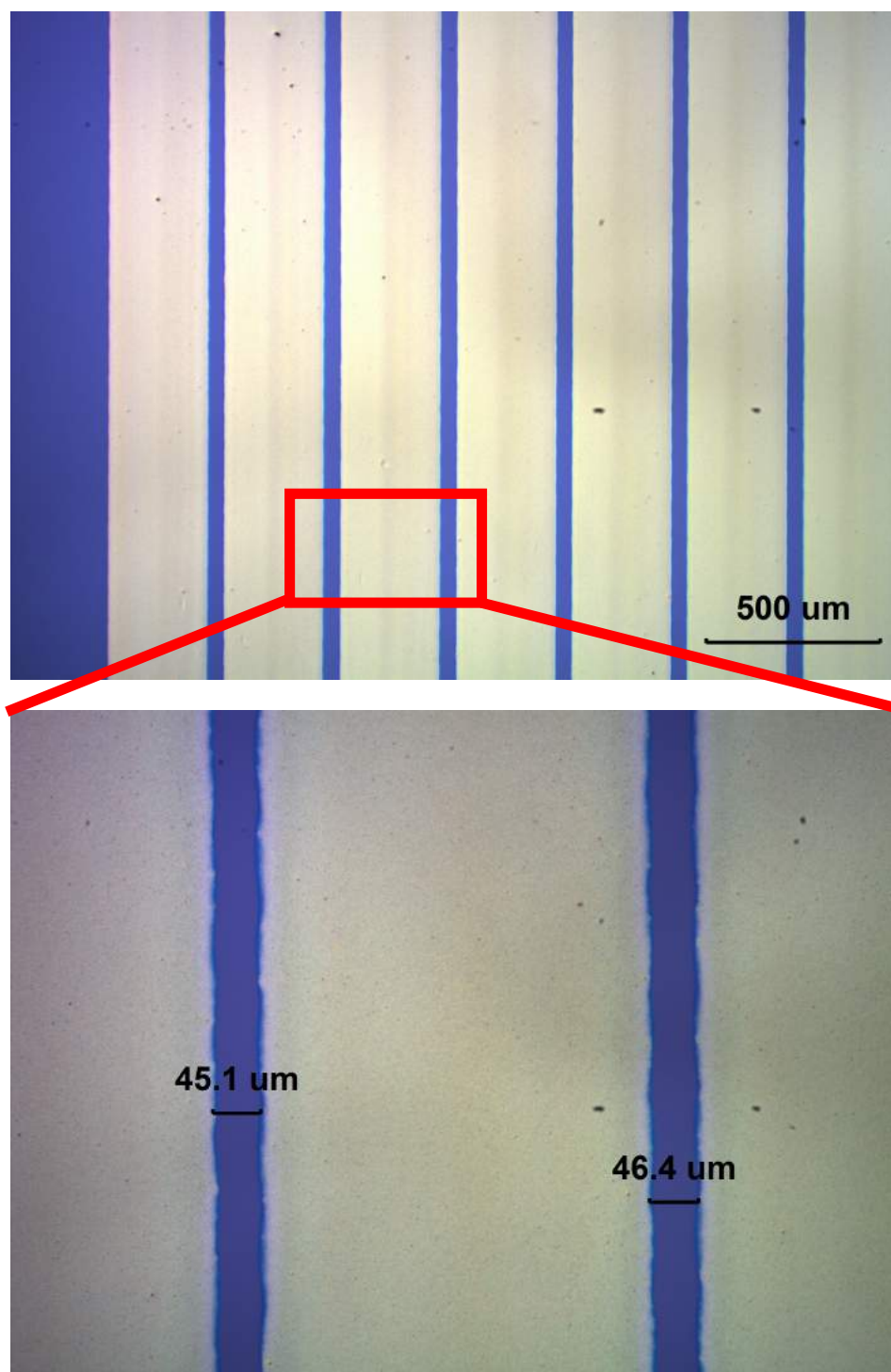
Figure 5.4: Printed silver electrode. Repeated pattern with 300 μm electrode width and 45 μm spacing
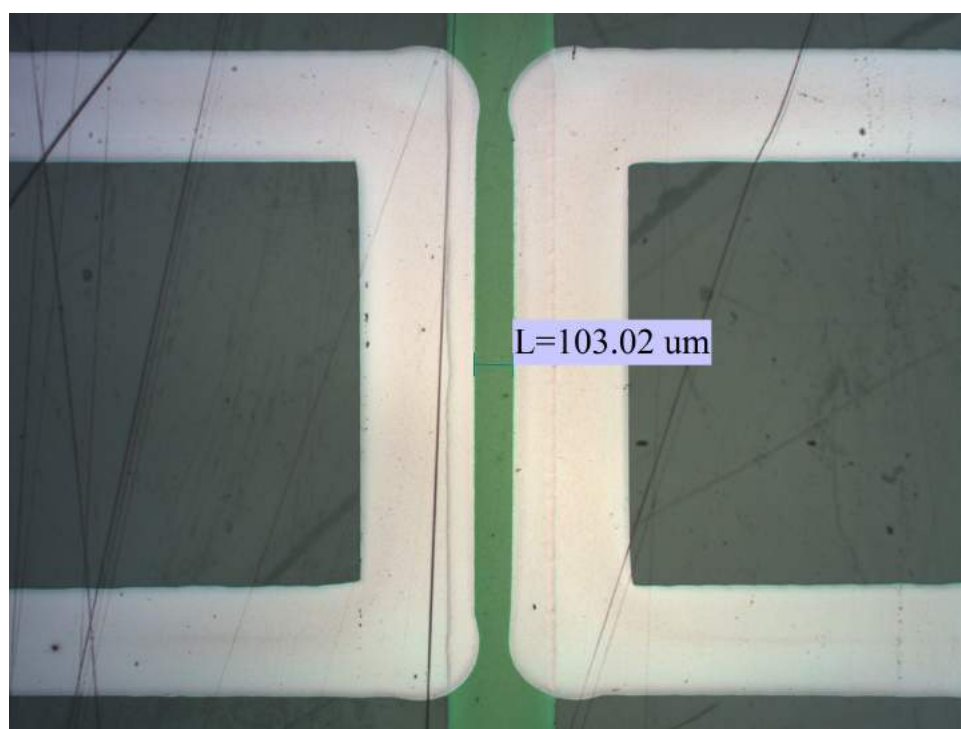
Figure 5.5: Printed silver SD and G electrode with average channel length of 100 $\pm$ 11 um.
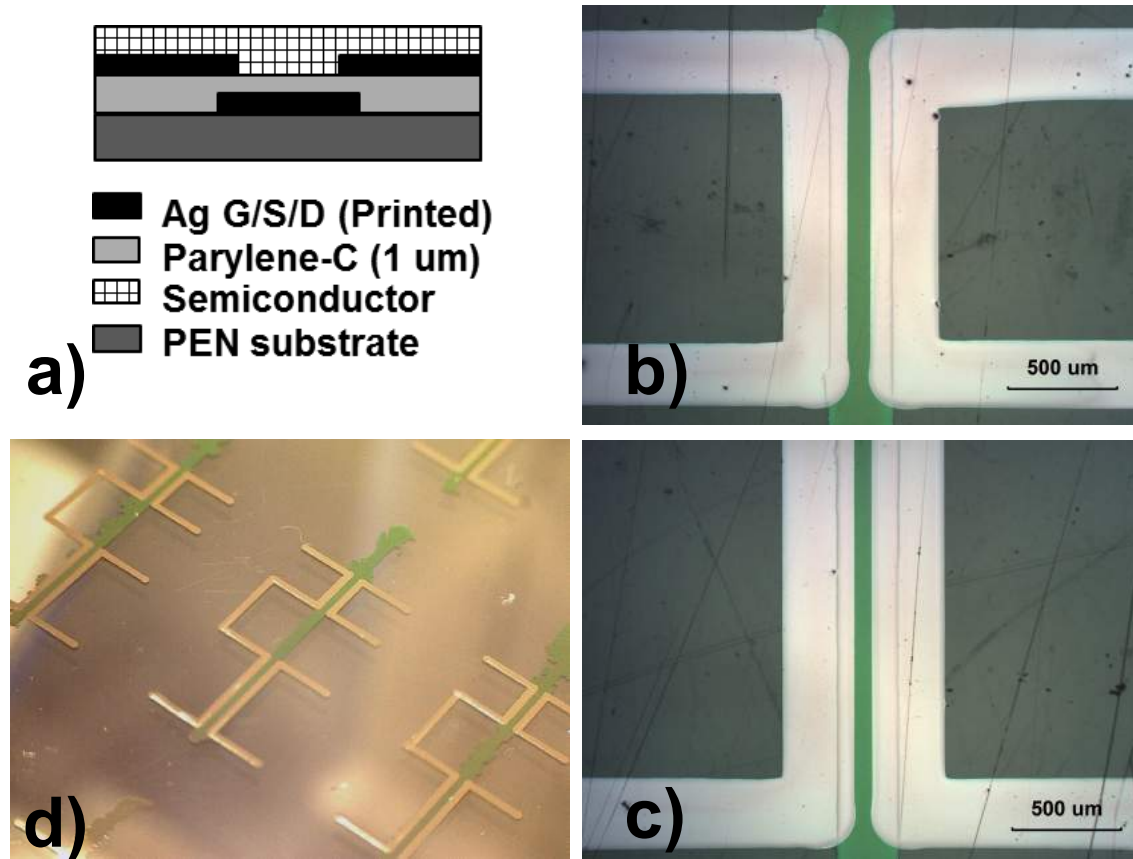
Figure 5.6: Structure of the printed TFT. a) Cross-section of the TFT b) Top view of fabricated SDG structure with dielectric before p-type semiconductor deposition c) Top view of fabricated SDG structure with dielectric before n-type semiconductor deposition d) Top view of the complete inverter structure
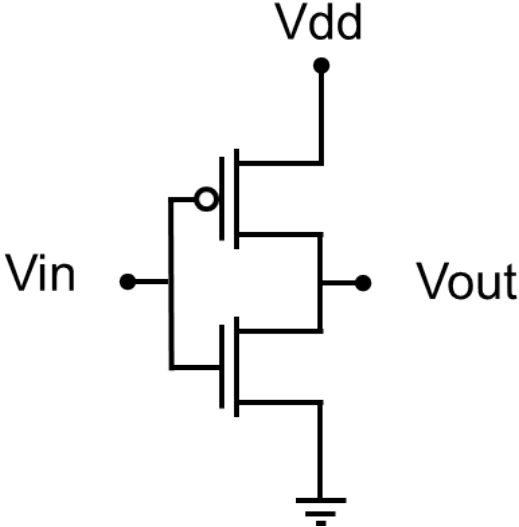
Figure 5.7: Circuit diagram of the inverter
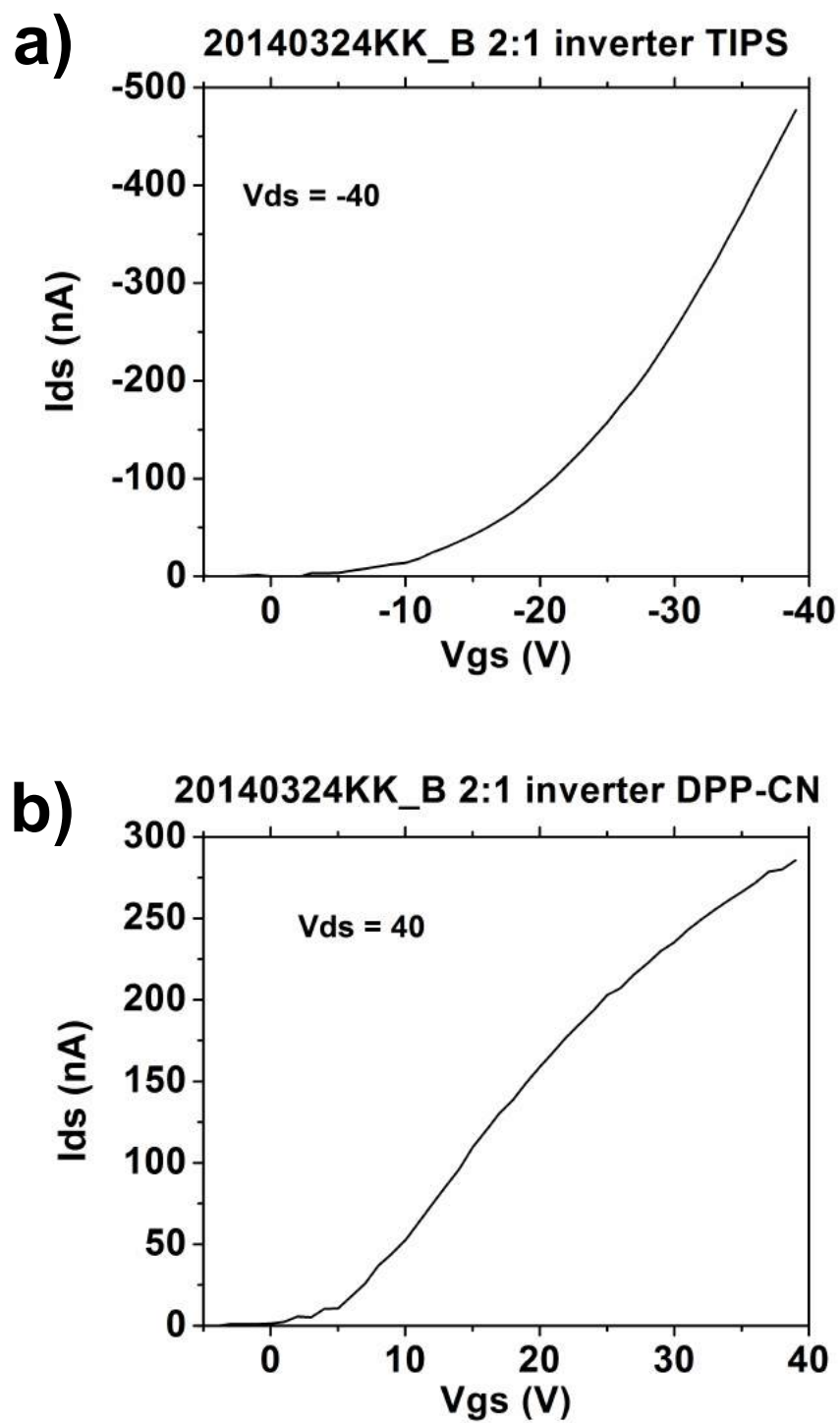
Figure 5.8: Output characteristic of the printed TFT. a) p-type TIPS-pentacene b) n-type DPP-CN
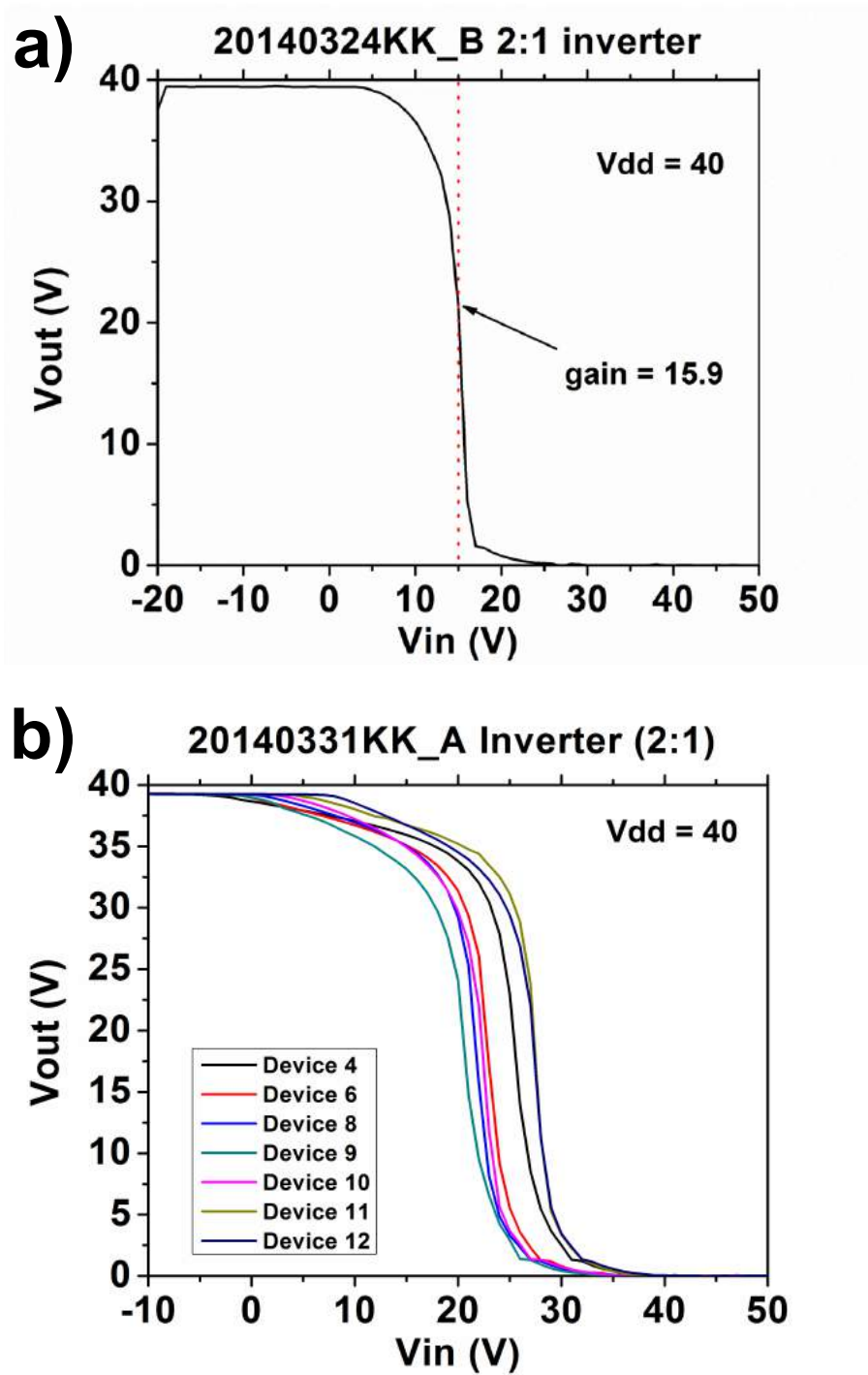
Figure 5.9: Output characteristic of the printed 2:1 inverter. a) Transfer curve of inverter with gain of 15.9 b) Transfer curve of 7 devices.

Chapter 6

Small Molecule Semiconductor Crystal Growth Manipulation via Pneumatic Printing Process

6.1 Introduction

While the classical inorganic semiconductors are the main steam materials for current technology platform due to their superior transport characteristics, the performance of the transistors incorporating solution-processed organic semiconductor materials have improved significantly over the last few years. Solution printing techniques employed to deposit organic semiconductors such as inkjet printing and blade coating can be extend to roll-to-roll fabrications to achieve near ambient condition process. The large-area and potentially high through-put deposition enable by solution printing can pave the way to realize more energy-efficient and cost-effective production of flexible electronics.[92] The main challenge to achieve high performance is the ability to control the thin film morphology is a precise manner. The solution-processed organics semiconductor thin film morphology is strongly dependent on the deposition process, and, in turn, significantly impacts the device performance. In this chapter,

the details of how the pneumatic printing process can be employed to control the organic semiconductor crystal growth will be discussed.

The parameter that is widely regarded as the metric or standard defining the high performance of a given electronics devices, such as organic FETs, is the charge carrier mobility. The mobility is the measure of how fast the electrons or holes (carriers) can travel through the media under applied electric field. The mobility dictates the rate of transport in the active layer, and thus, is responsible of the current conduction characteristics. Many factors can influence the charge carriers transport characteristics. Marcus theory, shown in equation 6.1, is a widely used theory to describe the charge transport in the organic semiconductors.[93] Where k_{ET} is the charge carrier transfer, T is the temperature, t is the transfer integral, λ is the reorganization energy, h and k_B are the Planck and Boltzmann constants respectively. The theory predicts that the orbital overlap (transfer integral) and the reorganization energy are vital to determining the carrier mobility. Therefore, any process that can modify the crystal structure and packing of the organic semiconductor layer will influence the orbital overlap and, thus, the mobility.[94][93][95] While there are many types of printing technique employed to enhance charge transport in the solution-process organic semiconductors, there are two main strategies to control the deposited thin film morphology, as described by Diao at el[92], 1) Control of nucleation and 2) Control of crystal growth.

$$k_{ET} = \frac{4\pi^2}{h}\frac{1}{\sqrt{4\pi k_B T}}t^2 exp(-\frac{\lambda}{4k_B T}) \tag{6.1}$$

Nucleation and crystal growth are, fundamentally, the two steps involved in the crystallization of organic semiconductor materials. Nucleation requires overcoming an intrinsically stochastic free energy barrier.[96] Therefore, without controlled nucleation, the crystals obtained will have random distribution of size and boundaries.

The crystal structure integrity, level of crystallinity, and basic qualities of the crystal
are dictated by the crystal growth. The crystal quality have a direct impact on the
transport property; therefore, controlling the crystal growth is the key to improve
charge carrier mobility.

Minemawari et al. have shown that both nucleation and crystal control can be
realized by using the inkjet printed platform.[20] The solvent and antisovent method
in which anitisovent was deposited in a defined area prior to the deposition of the
semiconductor solution. The crystallization initiates on the surface first and covers
the entire surface of the droplet. As the solvent evaporates the crystal remains.
This deposition method combined with nucleation control by asymmetry in solution
volume, where the differential volume resulting from asymmetrical pattern is used
to induce nucleation at the lower solution volume area, high mobility (30 cm^2/Vs)
with C8-BTBT is achieved. The disadvantage of this method is that, even though
single crystal can be obtained with relatively high yield (50 %), the orientation of the
crystal can not be precisely controlled.

Hallow pen printing and hallow capillary printing method developed by Headrick
et al. and Wo et al. utilizes meniscus-guided coating technique to achieve aligned
crystal growth.[97][98] The meniscus-guided coating process employs linear transla-
tion of substrate or coating tool to induce oriented crystal growth. Headrick et al.
and Wo et al. used hallow glass stylus to deposit TIPS-pentacene solution, and
were able to show grain size dependency on writing speed and substrate temperature.
The highest mobility achieved with this method with TIPS-pentacene is around 0.8
cm^2/Vs. The disadvantages of utilizing this method is that deposition of high and
low viscosity solution is difficult due to lack of pressure control. The control over
printing height is also not possible as it requires some control over the meniscus size.

Solution shearing is another meniscus-guided coating that can simultaneously con-
trol nucleation and crystal growth.[99][100] This printing process utilizes a tilted
shearing blade to sandwich the organic semiconductor solution between the heated

substrate to prevent exposure of the whole solution to air. This topology limits the air-solution interface to confine the solvent evaporation region. The shearing blade is then moved at a constant speed exposing the meniscus to allow deposition of aligned thin film. The technique developed by Diao et al.[16] demonstrated printed single crystal TIPS-pentacene with mobility greater than 10 cm^2/Vs by further combining the patterned feature to both induce nucleation and eliminate undesired crystal growth and the flow-assisted crystallization . The flow-assisted crystallization employs patterned shearing blade to increase the mass transport via fluid re-flow to eliminate the void formation during crystal growth. The limitation of the solution shearing is difficulty in the multi-material deposition. The process spreads the solution over the whole substrate; therefore, deposition of subsequent material, i.e. different type of semiconductor for example, require consideration for solvent compatibility in addition to potential mechanical damage to the previously deposited film.

Pneumatic printing technique can potentially achieve seeding and crystal growth simultaneously when used to print organic semiconductor. The printing process is analogous to seeded super lateral growth in laser recrystallization technique used in silicon technology. The seeding is achieved due to the differential volume of the contact meniscus, and the aligned crystal growth is achieved by matching the crystal growth rate and defining the printing direction. The resulted printed crystals have highly aligned polycrystalline structure that are millimetre long. Furthermore since the solution is confined in deposition area, patterned deposition and multi-material (both n- and p-type semiconductor for instance) can be realized.

In summary, the main advantages of employing pneumatic printing technique for printing organic semiconductors over the other printing techniques, therefore, are 1) simple setup and process, 2) multi-material layered deposition applicable to wide range of solution viscosity, 3) control over crystal seeding and growth. This method for performance optimization and patterning has great potential for advancing printed electronics. In this study, the crystal growth manipulation achieved by pneumatic

printing technique is the primary focus and is discussed in detail. Preliminary results for seeding is presented, but will require further study in the future.

6.2 Experimental

6.2.1 Materials

The TIPS-pentacene and C8-BTBT were used as received from Sigma-Aldrich without further purification. Phenyltrichlorosilane (PTS), (tridecafluoro-1, 1, 2, 2-tetrahydrooctyl) trichorosilane (TTT) and anhydrous-toluene were purchased from Sigma-Aldrich as well. Hihgly doped n-type silicon wafers with 300 nm thermal silicon oxide from SQI were used as the substrate.

6.2.2 Sample Preparation and Patterning

The cross-section of the printed TFT device is shown in Fig. 6.1. The Si/SiO_2 wafers were treated with PTS (immersing in 3 wt% in anhydrous-toluene) for 15 hours at 90 °C to ensure proper wetting of the organic semiconductor solution. The wafers were cleaned with toluene, acetone, and Isopropyl alcohol after the PTS treatment. Desired patterns on the surface were generated using photo-lithography. The PTS in the unwanted regions were removed by exposing the substrate to oxygen plasma (250 mmHg O_2, 100W) for 60 seconds after photo-resist development. The de-wetting surfaces were then formed by placing the substrate into a vacuum sealed dessicater with 15 μl of TTT in a glass vial for 3 hours. The remaining photo-resist were removed by sonicating the substrate in acetone for 5 min.

6.2.3 Printing and Characterization

TIPS-pentacence solution was prepared at a concentration of 16 mg/ml in anhydrous-toluene. The substrate was heated to desired temperature by the resistively heated

stage on the 3D XYZ robot (Janome JR 2200N mini). The TIPS-pentacene solution
were loaded into the syringe, and 0.7 psi of vacuum was applied to avoid the solution
from dripping. The printing height was controlled to be 80 μm, and 0.7 psi forward
pressure is applied before the printing to create meniscus contact between the nozzle
and the substrate. The vacuum and forward pressure values were optimised based on
the TIPS-pentacene solution concentration and solvent. The printing speed varied
between 0.1 - 1.5 mm/s. During the printing, the meniscus stayed in contact with
the substrate. The printing length varied from 2 - 4 mm depending on the device
structure. The printed films were characterized using a cross-polarized optical mi-
croscope. The thickness and surface characterization were performed using tapping
mode atomic force microscopy (AFM). The source and drain electrodes were pat-
terned by metal stencil shadow mask and thermally evaporating 60 nm of gold. The
channel length and width of our mask design is 100 μm and 3000μm, respectively;
however, the actual w of the device is 300 μm due to the nozzle width. All the elec-
trical characterizations were conducted in ambient environment using Keithley 2400
source measuring unit interfaced with Labview.
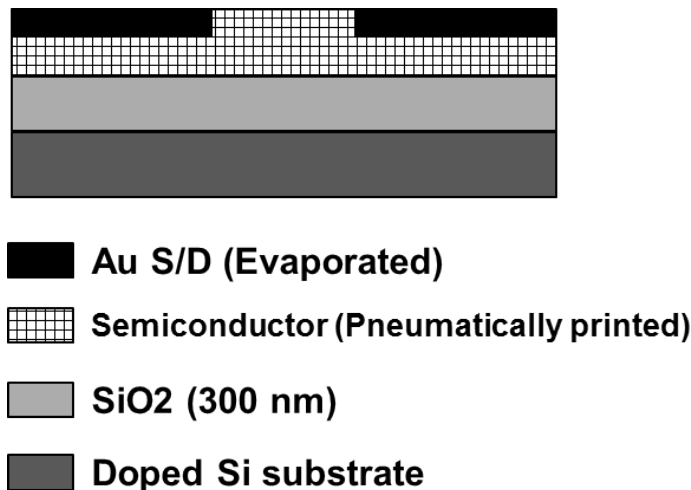
Figure 6.1: Cross-section of the printed TFT structure.

6.3   Printing Parameters

Pneumatic printing technique can achieve seeding and crystal growth simultaneously.
The printing process for organic semiconductor is shown in Fig. 6.2. The pneumatic
printing process is as described in section 5.2 in Chapter 5. **a)**. An appropriate level
of vacuum is applied to the reservoir to both keep the solution from dripping out, and
to suspend the meniscus. **b)** A forward pressure is then applied for a short period
of time, typically 10 - 20 ms, to contact the meniscus to the substrate surface. At
this moment the capillary force keeps the meniscus attach to the surface even after
applying the forward pressure and same level of vacuum is applied as before. **c)** The
nozzle starts the printing with defined direction with defined printing speed, and the
solution is drawn out of the nozzle via capillary action. **d)** Once the desired printing
is done, the nozzle is raised to a height greater than the printing height, h, to separate
the meniscus contact with the substrate.

All the key parameters that can influence the printing characteristics are shown
in Table 6.1. The printed height is dependent on the viscosity of the solution, which
is determined from the solvent used and the concentration, and the surface of the
substrate. In this experiment, the printing height is fixed at 80 μm as larger distance
result in meniscus separation before the completion of printing. The vacuum and
forward pressure is critical for the pneumatic printing process. The control over the
meniscus is fundamentally dictated by the pressure applied. The differential pressure
gives rise to the seeding for crystal growth, and the forward pressure and vacuum are
both fixed at 0.7 psi which will give the differential pressure of 1.4 psi. The solution
concentration depends on the solubility of the organic semiconductor used. The con-
centration is fixed at saturation which is 16 mg/ml for TIPS-pentacene in toluene.
Saturated solution is used because in order to achieve well ordered alignment, high
solution concentration (high nuclei density) is desirable.[92] The substrate tempera-
ture is dependent on the solvent used as it will dictate the solvent evaporation rate
and in turn influence the formation of the supersaturation that results in solute pre-

cipitation. The temperature is fixed at 50 °C. The detailed analysis of the substrate temperature is discussed later in the chapter. The self-assembled monolayer (SAM) forms a wetting surface for the TIPS-pentacene solution and it is determined by the solvent used. Since toluene is used as the solvent, phenyl trichlorosilane (PTS) is used to ensure proper wetting. All of the above parameter will influence the optimal printing speed in which the highest mobility is achieved. The printing speed is varied to study the dependency of mobility on the printing speed with all other parameter kept at constant.

Table 6.1: Key parameters for pneumatic printing of TIPS-pentacene

Parameter	Dependance	Optimal value
Printing height	viscosity/surface	80 μm
Pressure	Solvent/concentration	Fixed
Concentration	solubility	16 mg/ml
Temperature	Solvent	50 °C
SAM	Solvent	PTS
Printing speed	All of the above	Varied

6.4 Self-Assembled Monolayer Surface Treatment

The self-assembled monolayer (SAM) forms a wetting surface for the TIPS-pentacene solution and reduce surface traps.[15] Therefore, the quality of the SAM layer can have a significant impact on the crystal formed. The AFM image of good quality and poor quality SAM layers are shown in FIg. 6.3. The good quality SAM has surface roughness of 1.6 nm which is roughly the same as the substrate surface roughness. As expected, the crystal structures are significantly different depending on the quality of the underline SAM layer. The crystal grown on the poor quality SAM layer is shown in Fig. 6.4. The crystal structure is irregular with rough surface and zigzagged edge.

The crystal grown on the good quality SAM layer is shown in Fig. 6.5. The crystal structure is well defined with smooth surface and straight edge. The crystals formed on poor quality SAM are also much thinner. The thickness of the crystal on poor quality SAM is 76 nm compared to 190 nm on the good quality SAM. The crystal quality in turn dictates the electrical property. The Id vs Vg characteristics of TFTs made with both good and bad quality SAM are shown in FIg. 6.6. The carrier transport is much better with well defined crystal structure. Table 6.2 summarises the mobilities extracted from both SAM conditions. The mobility is about 2x higher with good quality SAM; therefore, it is important to ensure the quality of SAM layer to achieve high performance.

Table 6.2: Comparison of mobility with good and poor quality SAM layer

SAM condition	Max mobility	Avg mobility	stdev
Poor	0.16	0.13	0.03
Good	0.4	0.25	0.13

6.5 Printing Temperature

Substrate temperature is one of the most vital parameter that can influence the crystal growth when using a meniscus-guided deposition method. As the linear transition of the substrate or the nozzle initiates, the evolution and reshape of the solution-air interface or meniscus occurs. The Solvent evaporation occurs at this reshaped tail interface. The solution concentration increases as the solvent evaporates in this region, and the solute precipitates and deposits as crystal film when supersaturation in the solution is reached. The evaporation rate plays a pivotal role in establishing this supersaturation regime. The substrate temperature with respect to the solvent boiling point needs to be considered for optimal printing temperature. Fig. 6.7 shows the effect of substrate temperature have on the resulting crystal structure. At

40 °C, the supersaturated regime is not established as the boiling point of toluene is 120 °C. Therefore, the crystallization occurs after the drawing is completed. This similar to drop-casted method, and spherulitic crystal structures are formed. At 70 °C, the supersaturation regime and precipitation occur faster than the printing speed; therefore, discontinuous wave-front crystal structures are formed. It turns out that 50 °C is the optimal printing speed at which the supersaturation and crystallization can occur at a rate that matches our printing speed. The printing of TIPS-pentacene will be carried out at a fixed substrate temperature at 50 °C.

6.6 Solution Concentration

Another important parameter to consider is the solution concentration because the concentration will determine the nuclei density. The nuclei density can have a impact on nucleation site formation and also crystal growth from supersaturation of the solution. Saturated solution is used because in order to achieve well ordered alignment, high solution concentration (high nuclei density) is desirable.[92] Fig 6.8 shows the variation of crystal structures due to varied solution concentrations. As shown in Fig. 6.8 a), when solution concentration is lower, the decreased nuclei density leads reduced nucleation and seeding. Furthermore, supersaturation regime is more difficult to establish due to higher solvent ratio. Hence,spherulitic crystal structures are formed. Fig. 6.8 b) shows the polycrystalline crystal structure formed when saturated solution is used.

6.7   Result and Discussion

6.7.1   TIPS-pentacene Nucleation and Crystal Growth Manipulation

The nucleation of the seeds are formed due to the differential volume of the contact meniscus. The nucleation inducing process is composed of two steps: 1) Initial meniscus contact is formed during the period when forward pressure is applied for 10 ms. 2) Then vacuum is applied immediately, as described before, after the forward pressure. This difference in pressure results in differential volume of the initial contact meniscus and the contact meniscus when vacuum is applied. As a result, the contact area becomes smaller, and this retraction of meniscus creates nucleation and spherically oriented crystal growth that will serve as the seeds for further crystal growth. The exaggerated seeding feature, due to purposely increased forward pressure, is shown in Fig. 6.9. This result shows promising potential that the seeded nucleation can be achieved, but further study is needed to optimize and quantify the nucleation process.

Once the seeding is achieved, the guided-meniscus will facilitate the crystal growth in the printing direction. As mentioned before, after the linear transition of the substrate or the nozzle initiates, the evolution of the solution-air interface or meniscus occurs. The Solvent evaporation occurs at this reshaped tail interface. The solution concentration increases as the solvent evaporates in this region, and the solute precipitates and deposits as crystal film when supersaturation in the solution is reached. The alignment in the crystal growth is achieved by the inherent directionality of the linear motion guiding the meniscus.

Contrasted crystal structure image can be observed under the cross polarized optical microscope (CPOM). Fig 6.10 shows the cross polarized image of the printed TIPS-pentacene crystal via pneumatic method. Well aligned crystal structure is observed. When looking at the crystal domain in the boxed region in Fig. 6.10 a), the crystal domain extinguished polarized light almost completely when rotated about

45° shown in Fig 6.10 b). The intensity change indicates that the crystal domain formed is well aligned.

6.7.2   Printed TIPS-pentacene Mobility

During the TIPS-pentacene pneumatic printing process, the dragged meniscus exposes the solution front, and the printing speed dictates the shape of the exposed solution-air interface. The shape of the interface depends on the printing speed, and the printing speed have significant impact on the structure of the crystal formed. As discussed in the earlier section, the charged carrier transport is largely dictated by the structure and quality of the crystal film. Therefore, the mobility of the printed film will strongly depend on the printing speed. Fig. 6.11 a) - f) shows the cross-polarized optical microscope images demonstrating the thin film crystal structure and thin film texture dependency on the printing speed, varying from 1 mm/s to 0.1 mm/s. At high printing speed (1 mm/s and 0.8 mm/s), the oriented micrometer wide needle like TIPS-pentacene domains are obtained with length of few hundreds of micrometers. When printing speed is significantly lower (less than 0.2 mm/s), the crystal domains becomes thicker but discontinued. This is because the supersaturation regime and precipitation occur faster than the printing speed; therefore, discontinuous piece-wise crystal domains are formed. Between printing speed of 0.6 mm/s and 0.2 mm/s, the tens of micrometer wide TIPS-pentacene domains with length in the hundreds of micrometer to millimetre range are formed. The mobility of the fabricated devices are extracted and plotted against the printing speed to evaluate the crystal quality. The top-view of the fabricated TFTs are shown in Fig. 6.12. The mobility against printing speed plot is shown in Fig. 6.13 a). The optimal printing speed at 0.2 mm/s resulted in highest average mobility of above 0.25 cm^2/Vs. The maximum mobility of 0.75 cm^2/Vs is obtained at a printing speed of 0.3 mm/s, and the top-view of this device is shown in Fig. 6.13 b). The device carrier mobility indeed shows a strong correlation with printing speed. The spin-coated TIPS-pentacene device have mobil-

ity of around 0.007 cm^2/Vs; therefore, a 100x improvement in mobility is achieved
with pneumatic printing process.

6.8   C8-BTBT

Another small molecule organic semiconductor material printed using the pneumatic
printing process is C8-BTBT. The printing condition was exactly the same as the
TIPS-pentacene solution. The C8-BTBT was dissolved in toluene at a concentration
of 16 mg/ml. Fig. 6.14 a) - f) shows the cross-polarized optical microscope images
demonstrating the thin film crystal structure and thin film texture dependency on
the printing speed, varying from 1 mm/s to 0.1 mm/s. The crystal stacking of C8-
BTBT is characterized herring-bone arrangement in the intra-layer plane which seems
to facilitates isotropic growth of the crystal domain. The crystal domian obtained
is much wider than that of TIPS-pentacene. Fig. 6.15 shows the top-view of the
fabricated TFTs with printed C8-BTBT thin film as the active layer. The printed C8-
BTBT domain can be larger than hundred micrometer wide with millimetre length.
The mobility against printing speed plot is shown in Fig. 6.15 a). The optimal
printing speed at 0.3 mm/s resulted in highest average mobility of close to 0.4 cm^2/Vs
and maximum mobility of 1.3 cm^2/Vs. The top-view of this device is shown in Fig.
6.15 b). The spin-coated C8-BTBT device have mobility of around 0.13 cm^2/Vs;
therefore, a 10x improvement in mobility is achieved with pneumatic printing process.
The printing process needs further optimization, and there is potential for isotropic
conduction in the active layer.

6.9   Conclusion

Printing organic semiconductors is a promising approach to achieve low-cost fabri-
cation of large area flexible electronics. The ability to rapidly pattern and deposit

multiple materials and control the thin-film morphology are significant challenges facing industrial scale production. The morphology of the printed organic semiconductor thin film is strongly dependent on the printing process and its parameter. We demonstrated a novel pneumatic nozzle printing approach to control the both the seeding and crystallization of organic thin-films and deposit multiple materials on the same substrate. Pneumatic printing uses capillary action between the nozzle and substrate combined with control of air pressure to dispense the solution from a dispense tip with a reservoir. We achieved seeding by applying differential pressure before the linear translation of the substrate. We can control the orientation and size of the crystals by tuning the printing direction, speed, and the temperature of the substrate. We demonstrate the dependence of the mobility of printed thin film 6,13-bis(triisopropylsilylethynyl) pentacene [TIPS-pentacene] and C8-BTBT on printing conditions; formation of well-ordered crystals occurs at an optimal head translation speed. A maximum mobility of 0.75 $cm^2/(Vs)$ is achieved with 0.3 mm/s printing speed and 1.3 $cm^2/(Vs)$ with 0.3 mm/s printing speed at 50 °C for TIPS-pentacene and C8-BTBT respectively. When compared to the spin coated method, pneumatically printed TFTs exhibit 100x and 10x improvements in mobility for TIPS-pentacene and C8-BTBT respectively. Pneumatic printing technique can be an attractive route to industrial scale large area flexible electronics fabrication.
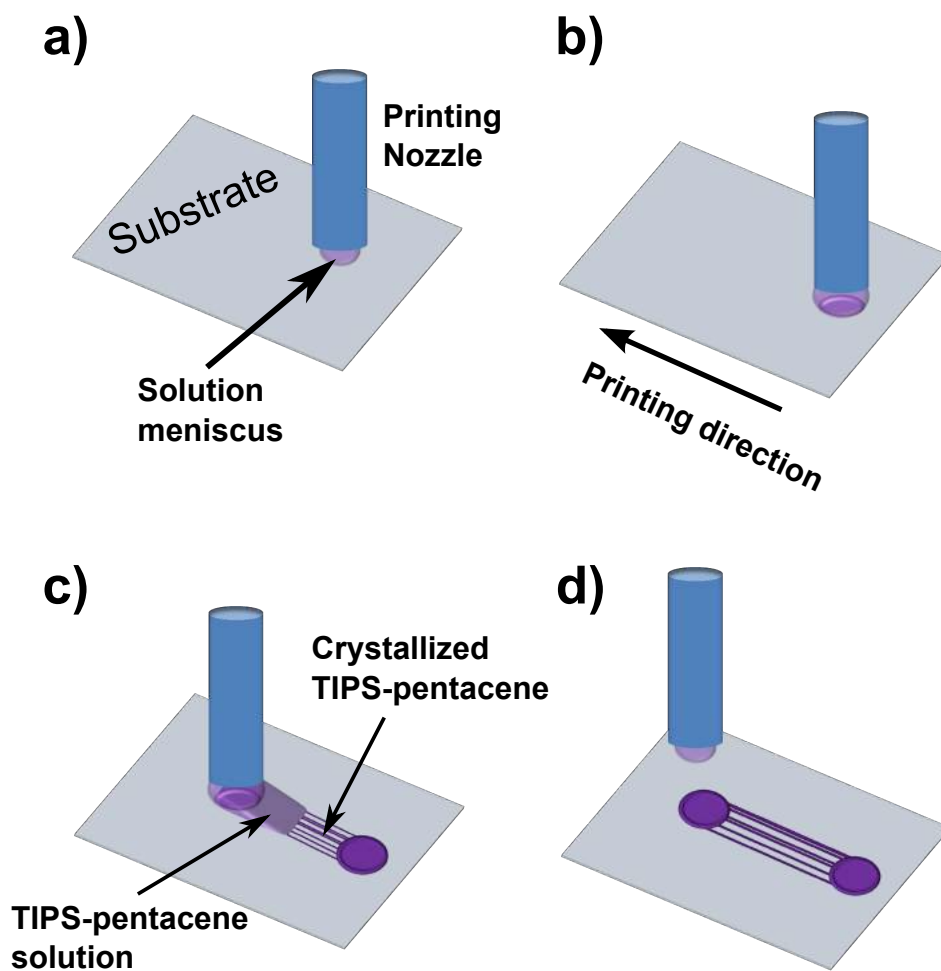
Figure 6.2: Printing process of TIPS-pentacene. **a)**. An appropriate level of vacuum is applied to the reservoir to both keep the solution from dripping out, and to suspend the meniscus. **b)** A forward pressure is then applied for a short period of time, typically 10 - 20 ms, to contact the meniscus to the substrate surface. At this moment the capillary force keeps the meniscus attach to the surface even after applying the forward pressure and same level of vacuum is applied as before. **c)** The nozzle starts the printing with defined direction with defined printing speed, and the solution is drawn out of the nozzle via capillary action. **d)**Once the desired printing is done, the nozzle is raised to a height greater than the printing height, h, to separate the meniscus contact with the substrate.

Figure 6.3: AFM image of the SAM layer. a) Good quality SAM layer that has surface roughness of 1.6 nm which is close to that of the substrate. b) Poor quality SAM laye with surface roughness several times larger at 6.74 nm.
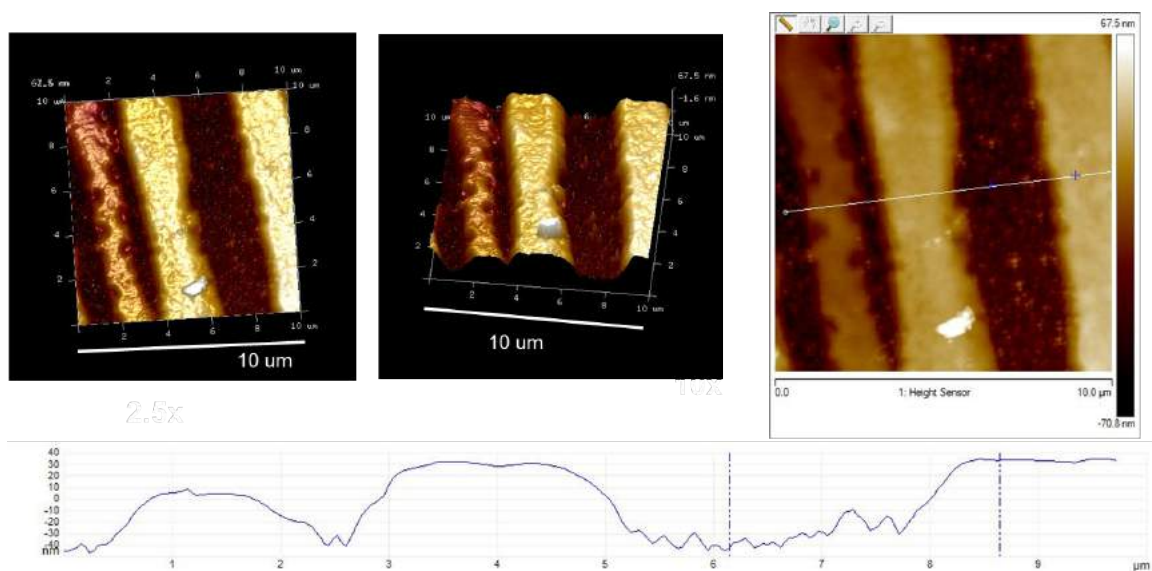
Figure 6.4: AFM image of the printed TIPS-pentacene on top a poor quality PTS SAM layer. The crystal quality is poor with rough edges and uneven surface. The thickness of the film is about 76 nm.
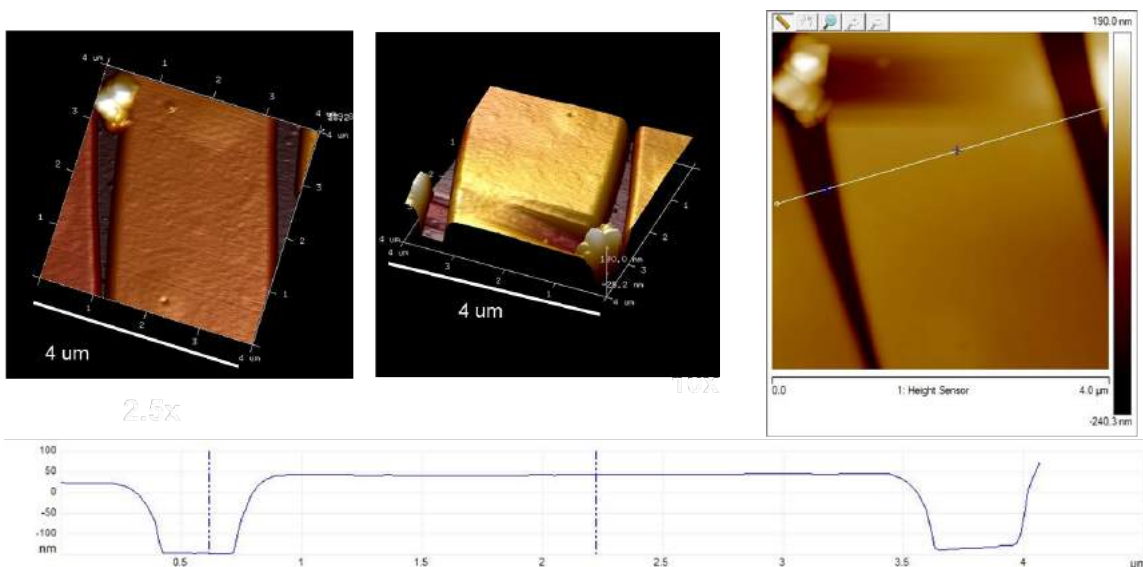
Figure 6.5: AFM image of the printed TIPS-pentacene on top a good quality PTS SAM layer. The crystal quality is much better with sharp edge and smooth surface. The thickness of the crystal is about 190 nm.
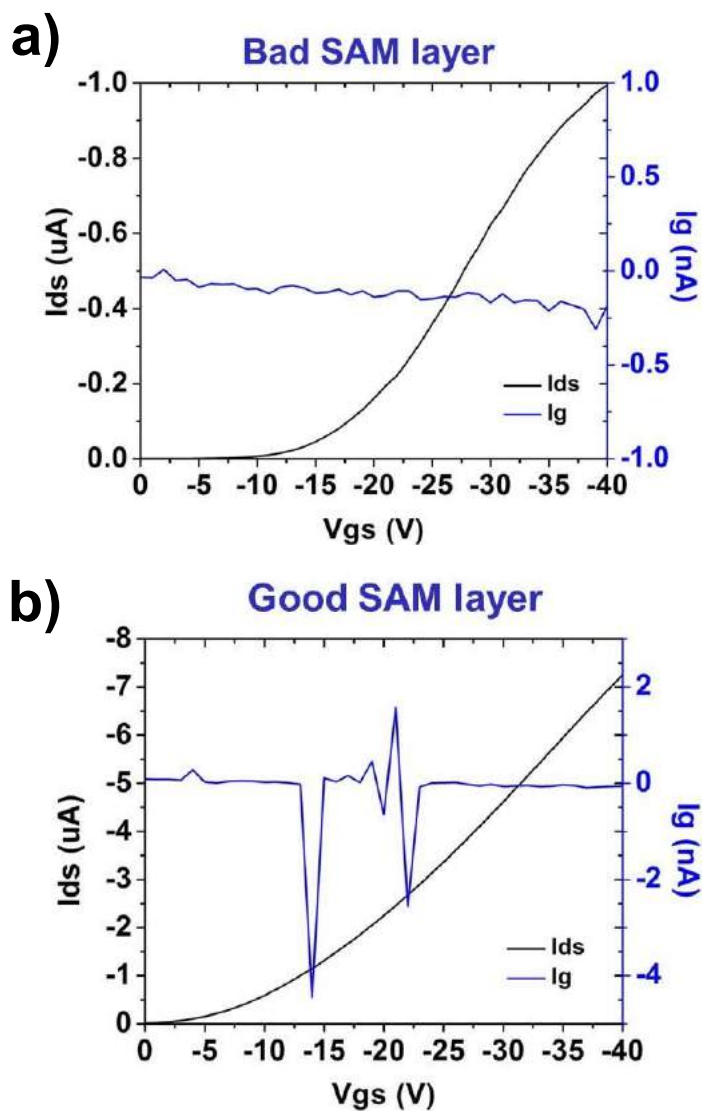
Figure 6.6: IV characteristic of the fabricated TFT. a) Output of TFT with poor quality SAM with lower current than expected. b) Output of the TFT with good quality SAM with much higher current level and smoother curve.
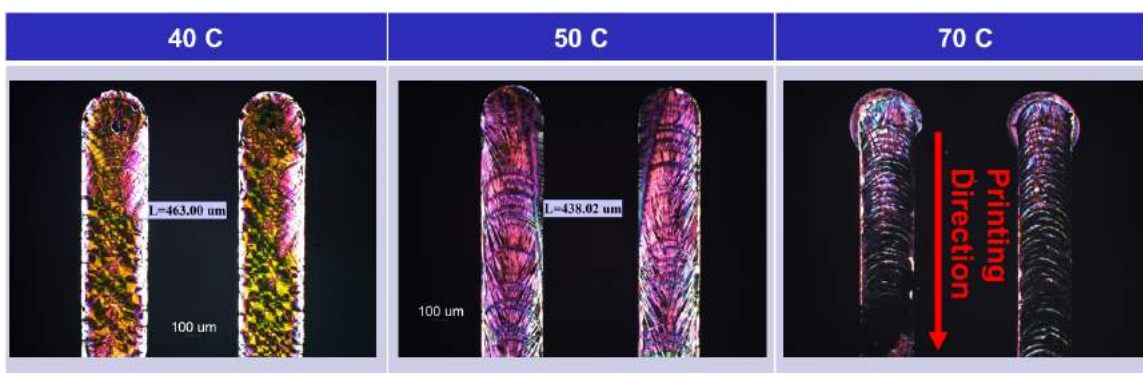
Figure 6.7: Crystal structure dependency on substrate temperature. At 40 °C, the supersaturated regime is not established as the boiling point of toluene is 120 °C. Therefore, the crystallization occurs after the drawing is completed. This similar to drop-casted method, and spherulitic crystal structures are formed. At 70 °C, the supersaturation regime and precipitation occur faster than the printing speed; therefore, discontinuous wave-front crystal structures are formed. It turns out that 50 °C is the optimal printing speed at which the supersaturation and crystallization can occur at a rate that matches our printing speed.
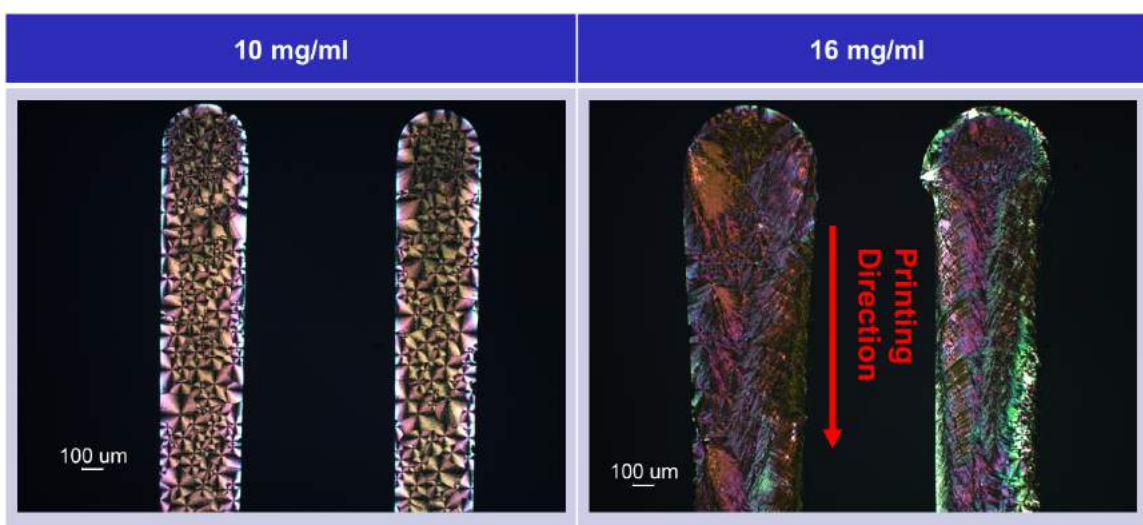
Figure 6.8: Crystal structure dependency on solution concentration a) When solution concentration is lower, the decreased nuclei density leads reduced nucleation and seeding. Furthermore, supersaturation regime is more difficult to establish due to higher solvent ratio. Hence,spherulitic crystal structures are formed. b) Polycrystalline crystal structures are formed when saturated solution is used.
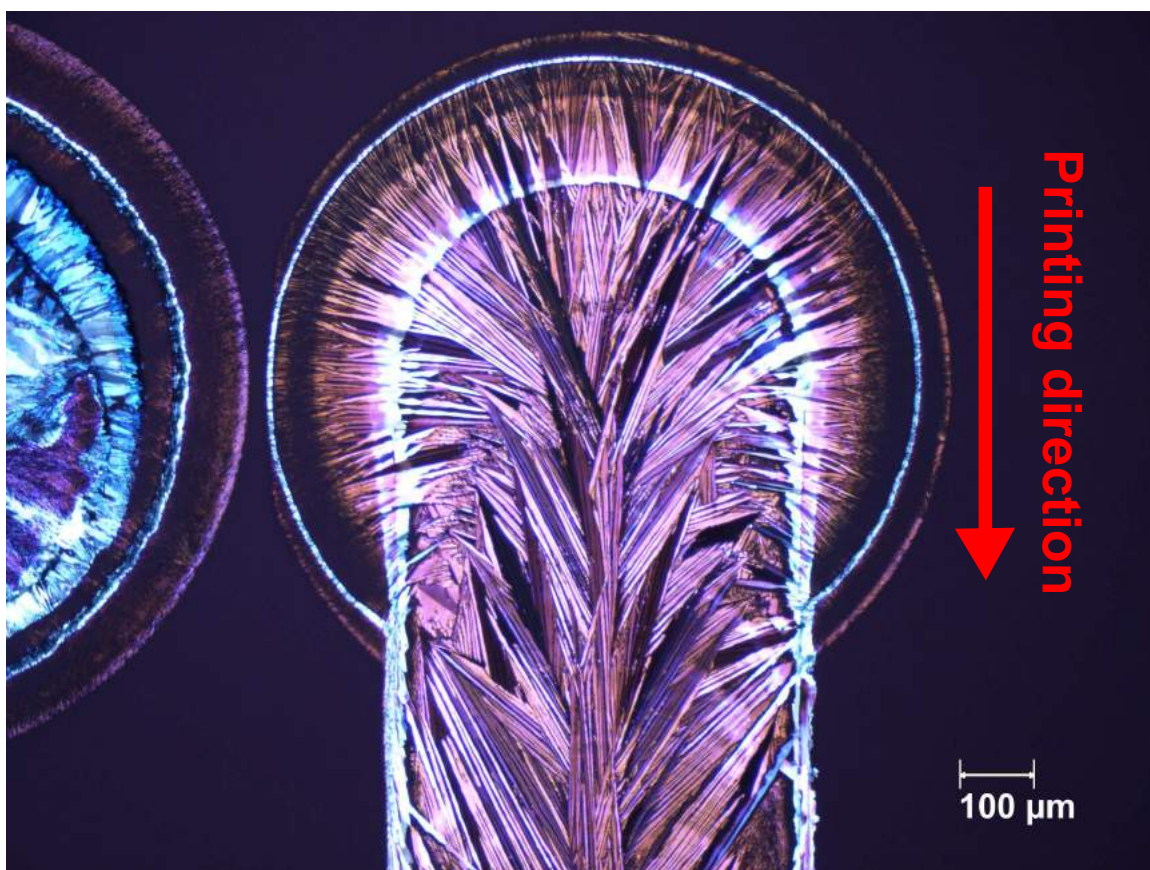
Figure 6.9: Exaggerated seeding picture. The nucleation of the seeds are formed due
to the differential volume of the contact meniscus.
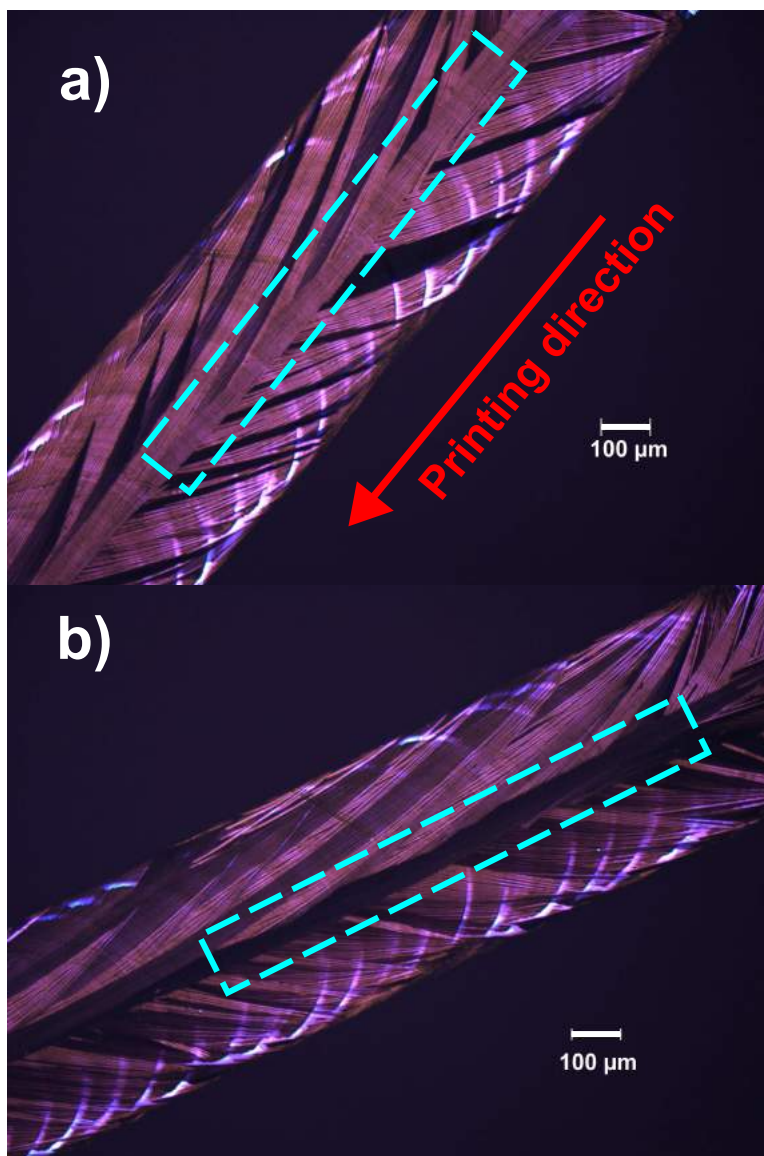
Figure 6.10: Cross polarized image of the printed TIPS-pentacene crystal. a) The crystal domain at maximum intensity b). The crystal domain extinguished polarized light almost completely when rotated about 45°. The intensity change indicates that the crystal domain formed is well aligned.
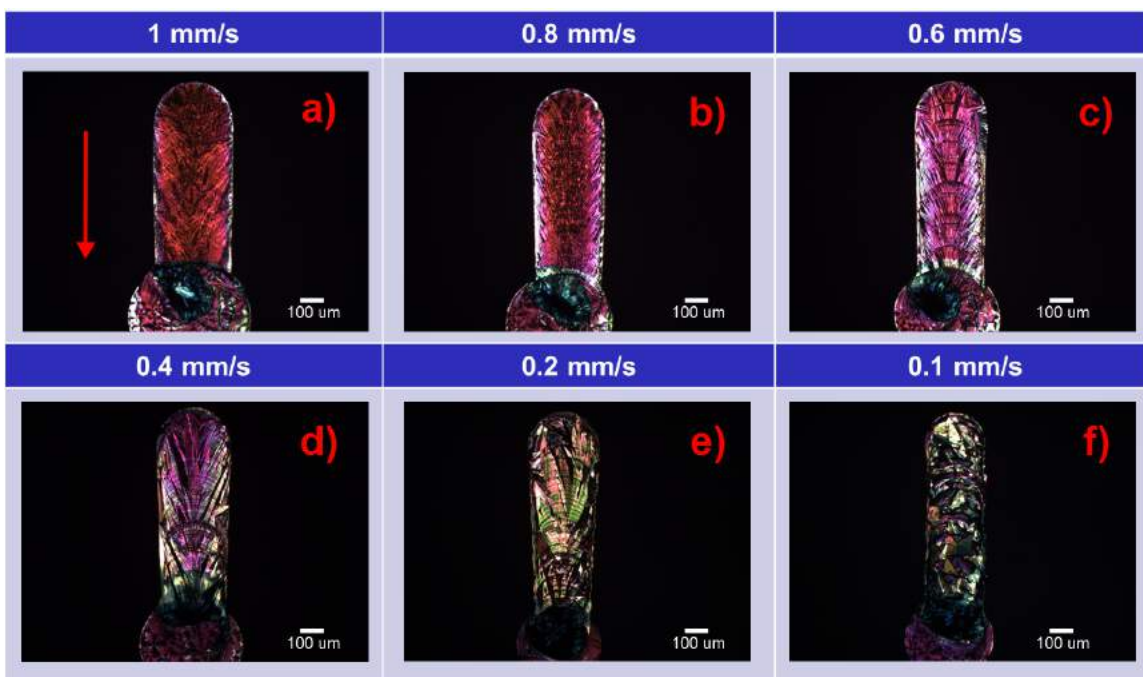
Figure 6.11: Cross polarized image of the printed TIPS-pentacene crystal with varying speed. a) - f) Cross-polarized images of pneumatically printed TIPS-pentacene thin films formed from printing speed of 1 mm/s, 0.8 mm/s, 0.6 mm/s, 0.4 mm/s, 0.2 mm/s, and 0.1 mm/s respectively. The red arrow indicates the printing direction.]
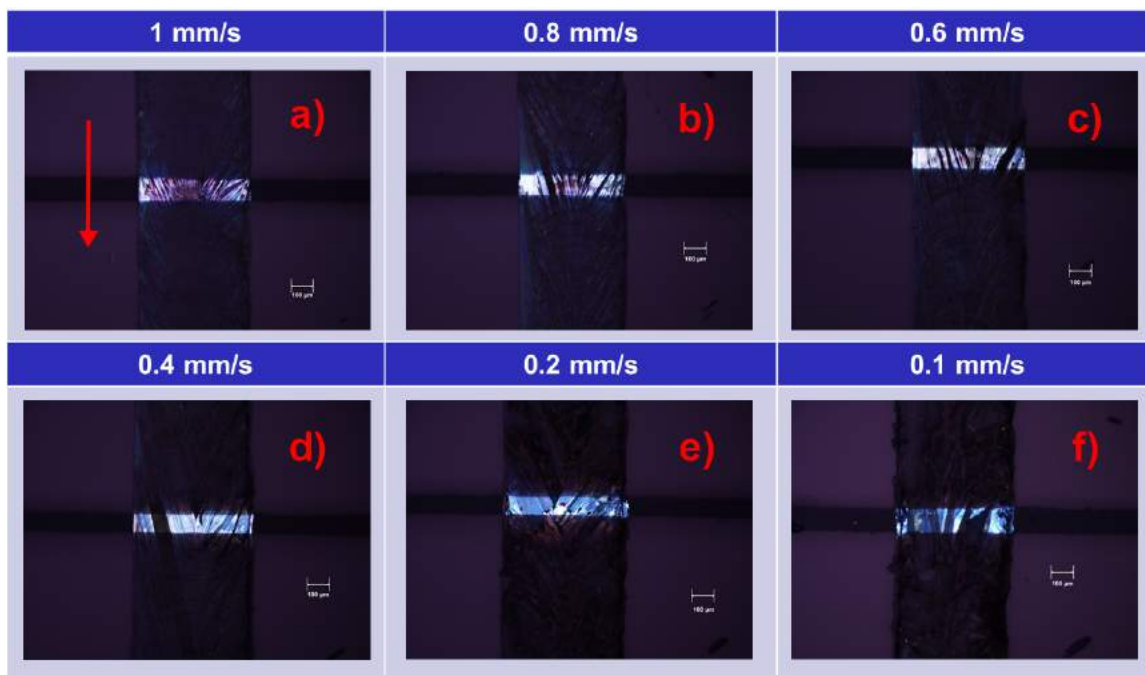
Figure 6.12: Cross polarized image of the top-view of the TFT devices with printed TIPS-pentacene film with varying speed. a) - f) Cross-polarized images of pneumatically printed TIPS-pentacene thin films formed from printing speed of 1 mm/s, 0.8 mm/s, 0.6 mm/s, 0.4 mm/s, 0.2 mm/s, and 0.1 mm/s respectively. The red arrow indicates the printing direction.
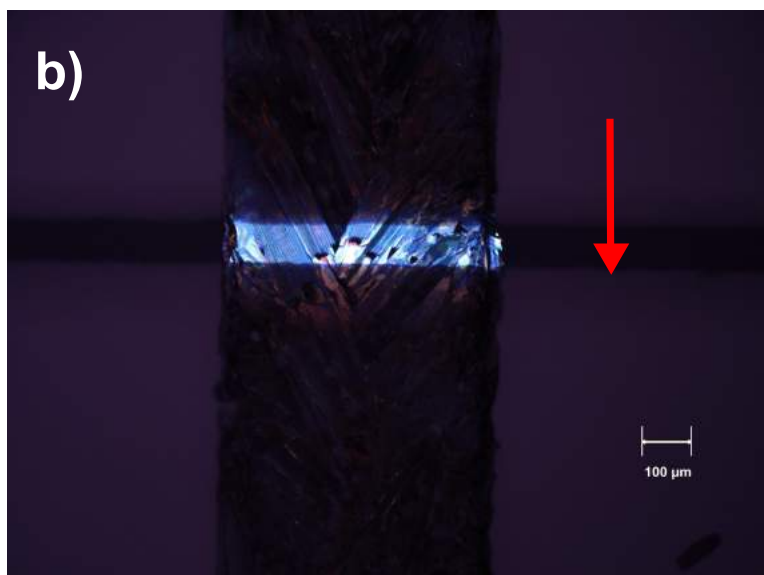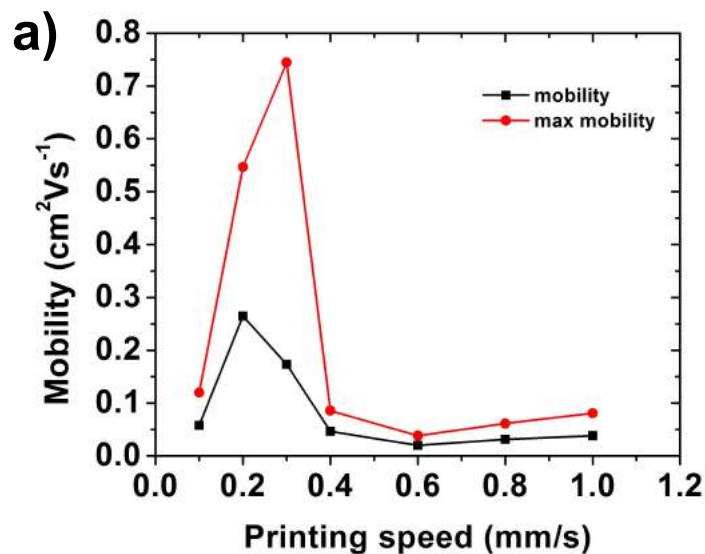
Figure 6.13: The TIPS-pentacene mobility vs printing speed plot. a) The mobility against printing speed. The optimal printing speed at 0.2 mm/s resulted in highest average mobility of above 0.25 cm^2/Vs. The maximum mobility of 0.75 cm^2/Vs is obtained at a printing speed of 0.3 mm/s. b) The top-view of the TFT devices with printed TIPS-pentacene film at printing speed of 0.3 mm/s.
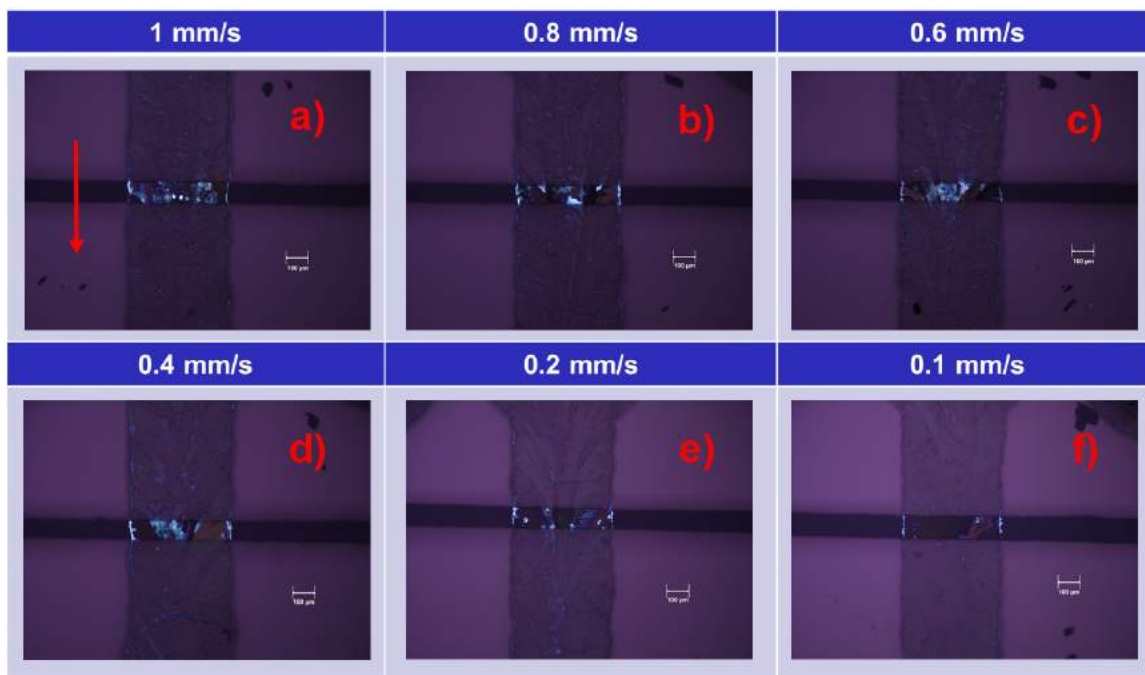
Figure 6.14: Cross polarized image of the top-view of the TFT devices with printed C8-BTBT film with varying speed. a) - f) Cross-polarized images of pneumatically printed C8-BTBT thin films formed from printing speed of 1 mm/s, 0.8 mm/s, 0.6 mm/s, 0.4 mm/s, 0.2 mm/s, and 0.1 mm/s respectively. The red arrow indicates the printing direction.
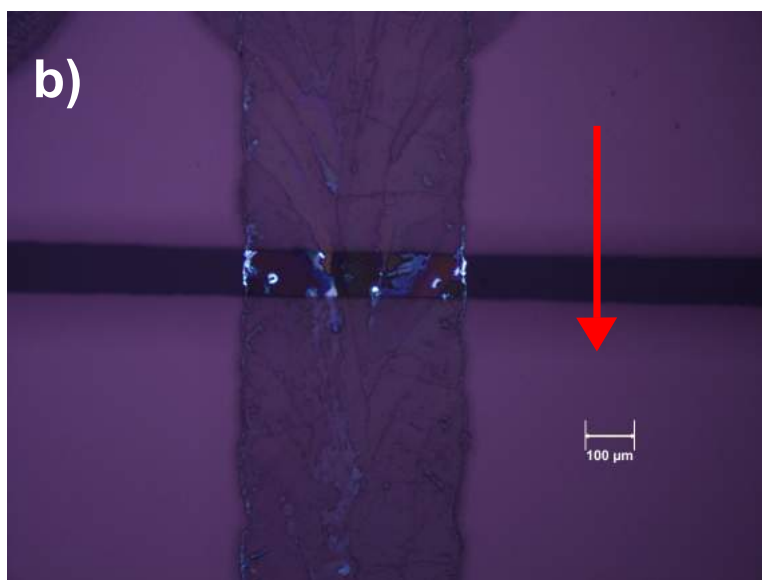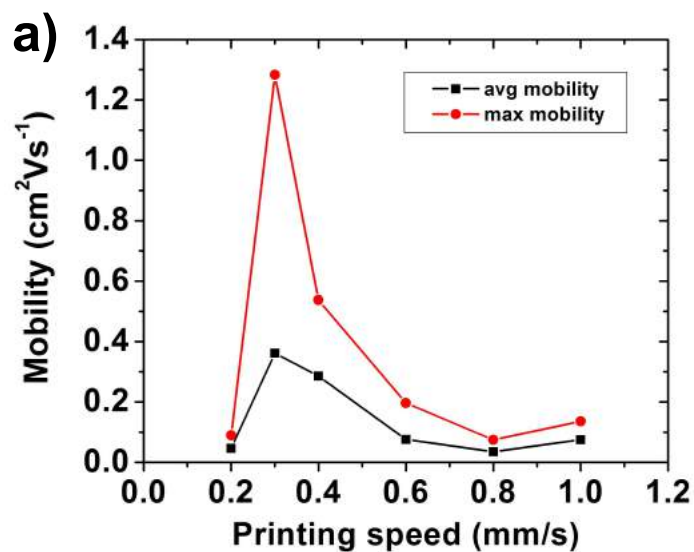
Figure 6.15: The C8-BTBT mobility vs printing speed plot. a) The mobility against printing speed. The optimal printing speed at 0.2 mm/s resulted in highest average mobility of above 0.25 cm^2/Vs. The maximum mobility of 0.75 cm^2/Vs is obtained at a printing speed of 0.3 mm/s. b) The top-view of the TFT devices with printed C8-BTBT film at printing speed of 0.3 mm/s

Chapter 7

Conclusion

Solution processed circuitries are expected to be the main driving force to achieve low cost, large area, flexible electronics. However, the commercialization of solution processed flexible electronics still face several challenges. The passive components such as capacitors are limited in frequency range and operating voltage. The active components such as transistors suffer from low mobility leading to limited current-carrying capacity. The fabrication process and material choices significantly impacts the electrical performance of the fabricated devices just as in traditional silicon technology. My thesis demonstrated the optimization of the performance of printed capacitors and transistors through investigation of several aspect of the device structure and fabrication process.

The optimization of the printed asymmetric nanoparticle/polymer composite capacitors is achieved through bias condition and electrode material consideration. Thin film metal oxide nanoparticle/polymer composites have enormous potential to achieve printable and solution-deposited high-k dielectrics. The combination of high-k ceramic nanoparticle enables room temperature deposition of high dielectric constant thin film without the need of high temperature co-firing process. The polymer matrix host fills the packing voids left behind by the nanoparticles resulting in higher effective dielectric permittivity as a system and suppresses surface states to reduced dielectric

loss. Such composite systems have been employed in a number of flexible electronic applications such as the dielectrics in both capacitors and thin film transistors. One of the most important properties of thin film capacitors is the breakdown field. In a typical capacitor system, the breakdown process leads to catastrophic failure that destroys the capacitor; however, in a nanoparticle/polymer composite system with self-healing property, the point of breakdown is not well-defined. The breakdown of the dielectric or electrodes in the system limits the leakage observed. It is possible, however, to define a voltage/field tolerance. Field tolerance is defined as the highest practical field at which the device stays operational with low failure rate by qualifying the devices with defined leakage current density. The optimization of the field tolerance of $(Ba,Sr)TiO_3(BST)$/parylene-C composite capacitors is achieved by studying the influence of the electromigration parameter on leakage and field strength through the inherit asymmetrical structure of the fabricated capacitors.

The composite device exhibits a five orders of magnitude improvement in the leakage current under positive bias of the bottom electrode relative to the pure-particle device, and four orders of magnitude improvement when the top electrode is positively biased. The voltage tolerance of the device is also improved and asymmetric (44 V vs. 28 V in bottom and top positive bias, respectively). This study demonstrates the advantage of this class of composite device construction, but also shows that proper application of the device bias in this type of asymmetrical system can yield an additional benefit.

The symmetrical dielectric system is used to investigate the dependence of the field tolerance of nanoparticle/polymer composite capacitors on the electromigration parameter of the electrodes. The field tolerance is suppressed by selecting the polarity used in nanoparticle $(Ba,Sr)TiO_3$/parylene-C composite film-based capacitors. Metals including gold, silver, copper, chromium, and aluminum with comparable surface conditions were examined as the electrodes. The asymmetric silver, aluminum, gold, copper, and chromium electrode devices show a 64 %, 29 %, 28 %, 17 %, 33 %,

improvement in the effective maximum field tolerance, respectively, when comparing bias polarity. The field at which filament formation is observed shows a clear dependence on the electromigration properties of the electrode material, and demonstrates that use of electromigration resistant metal electrodes offers an additional route to improving the performance of capacitors using this nanoparticle/polymer composite architecture.

In the second part of my thesis, the advantages of the pneumatic printing process are demonstrated. Multiple materials including conductive and semiconductor materials can be deposited using this printing method. Printed source, drain, and gate thin film transistor with drop-casted organic semiconductors are fabricated to employed in an inverter with uniform performance. The minimum spacing of 30 to 45 μm has been demonstrated.

Small molecule organic semiconductors are attracting immense attention as the active material for the large-area flexible electronics due to their solution processability, mechanical flexibility, and potential for high performance. However, the ability to rapidly pattern and deposit multiple materials and control the thin-film morphology are significant challenges facing industrial scale production. The manipulation of the crystal growth combined with induced seeding of the organic semiconductors have been demonstrated with pneumatic printing process to achieve oriented crystal domain with high mobility.

The dependence of the mobility of printed thin film 6,13-bis(triisopropylsilylethynyl) pentacene [TIPS-pentacene] and C8-BTBT on printing conditions is investigated, and the result indicates that the formation of well-ordered crystals occurs at an optimal head translation speed. A maximum mobility of 0.75 cm^2/(Vs) is achieved with 0.3 mm/s printing speed and 1.3 cm^2/(Vs) with 0.3 mm/s printing speed at 50 °C for TIPS-pentacene and C8-BTBT respectively.

In summary, the main advantages of employing pneumatic printing technique for printing organic semiconductors have been shown in this work. 1) simple setup and

process, 2) multi-material layered deposition applicable to wide range of solution viscosity, 3) control over crystal seeding and growth.

The fabrication process and material choices significantly impacts the electrical performance of the fabricated devices. My thesis demonstrated the optimization of the performance of printed capacitors through investigation of bias condition and failure mechanism of the device structure. The optimization of printed organic thin film transistors are achieved through employing pneumatic printing process to enable seeding and aligned crystal domain growth. The optimization techniques explored in this work have great potential for advancing printed electronics.

Chapter 8

List of Contributions

1. **Shyuan Yang***; Van Tassell*, B.; Le, C.*; Huang, L.; Liu, S.; Chando, P.; Byro, A.; Liu, X.; Gerber, D.L.; Leland, E.S.; Sanders, S.; Kinget, P.R.; Kymissis, I.; Steingart, D.; O'Brien, S., "Metacapacitors: Printed Thin Film, Flexible Capacitors for Power Conversion Applications," Power Electronics, IEEE Transactions on , Accepted (*Equal contribution)

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5. Kim, Chang-Hyun, Htay Hlaing, **Shyuan Yang**, Yvan Bonnassieux, Gilles Horowitz, and Ioannis Kymissis. "Impedance spectroscopy on copper phthalocyanine diodes with surface-induced molecular orientation." Organic Electronics 15, no. 8 (2014): 1724-1730.

6. **Shyuan Yang**, Ioannis Kymissis, Eli S. Leland, Shuangyi Liu, and Stephen O'Brien. "Influence of electromigration on the maximum operating field of (Ba, Sr) TiO3/parylene-C composite capacitors." Journal of Vacuum Science & Technology B 31, no. 6 (2013): 060603.

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8. **Shyuan Yang**, Brian R. Tull, Nadia K. Pervez, Limin Huang, Eli S. Leland, Daniel A. Steigart, Stephen O'Brien, and Ioannis Kymissis. "Asymmetric leakage in (Ba, Sr) TiO3 nanoparticle/paryleneC composite capacitors." Journal of Polymer Science Part B: Polymer Physics 51, no. 1 (2013): 35-38.

9. **Shyuan Yang**, Steve Park, Yvan Bonnassieux, and Ioannis Kymissis. "Organic Semiconductor Crystal Growth Manipulation via Pneumatic Printing Technique" Manuscript in preparation.

10. **Shyuan Yang**, Steve Park, Johannes Bintinger, Sejal Jain, and Ioannis Kymissis. "Ultra Low Cost Disposable Sensor platform" Manuscript in preparation.

Part III

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