Ionizing Radiation Effects on Graphene Based Field Effects Transistors

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ABSTRACT

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Graphene, first isolated in 2004 by Andre Geim and Konstantin Novoselov, is an atomically thin two-dimensional layer of hexagonal carbon that has been extensively studied due to its unique electronic, mechanical, thermal and optical properties. Its vast potential has led to the development of a wide variety of novel devices such as, transistors, solar cells, batteries and sensors that offer significant advantages over the conventional microelectronic ones.

Although graphene-based devices show very promising performance characteristics, limited has been done in order to evaluate how these devices operate in a radiation harsh environment. Undesirable phenomena such as total dose effects, single event upsets, displacement damage and soft errors that silicon-based devices are prone to, can have a detrimental impact on performance and reliability. Similarly, the significant effects of irradiation on carbon nanotubes indicate the potential for related radiation induced defects in carbon-based materials, such as graphene.

In this work, we fabricate graphene field effect transistors (GFETs) and systematically study the various effects of ionizing radiation on the material and device level. Graphene grown by chemical vapor deposition (CVD) along with standard lithographic and shadow masking techniques, was used for the transistor fabrication.

GFETs were subjected to different radiation sources, such as, beta particles (electron radiation), gamma (photons) and ions (alpha, protons and Fe particles) under various radiation doses and energies. The effects on graphene's crystal structure, transport properties and doping profile were examined by using a variety of characterization tools and techniques. We demonstrate not only the mechanisms of ionized charge build up in the substrate and displacement damage effects on GFET performance, but also that atmospheric adsorbents from the surrounding environment can have a significant impact on the radiation hardness of graphene. We developed different transistor structures that mitigate these effects and performed computer simulations to enhance even further our understanding of radiation damage.

Our results show that devices using a passivation layer and a shielded gate structure were less prone to irradiation effects when compared to the standard back-gate GFETs, offering less performance degradation and enhanced stability over prolonged irradiation periods. This is an important step towards the development of radiation hard graphene-based devices, enabling operation in space, military, or other radiation sensitive environments.

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Chapter 1

Introduction

1.1 Background and Motivation

Our lives today depend more than ever on the continuous advancements of electronics and semiconductor industry. It's been more than 50 years since the invention of the first transistor and few years later the integrated circuit, that scientists and engineers have managed to shrink the transistor gate length while increasing the transistor density and performance. The so-called "Moore's Law" has been driving the whole industry with great success, reducing the cost of electronics, while at the same time improving functionality and performance. The race of scaling hasn't been easy, as the semiconductor industry had to face multiple challenges when designing and fabricating transistors with gate lengths of 100 nanometers or less. Today, on the brink of sub-10 nm transistors and as we approach the physical limitation of silicon-based technology, the need of new novel materials and device structures is of crucial importance.

Many different materials besides silicon have been proposed, such as III-V materials like GaAs, InGaAs, InP or SiGe that can outperform traditional silicon devices on a variety of different applications. In conjunction with techniques like high-k dielectrics, strained silicon channels, FINFETs and recently 3D integration, the

semiconductor industry has been able to keep up with the growing need for faster and more efficient devices.

Carbon electronics have been suggested as a potential and very promising candidate for the next generation of electronics and nanodevices [1]. Since the first studies on carbon nanotubes (CNTs) and buckyballs (C^{60}), researchers have utilized these new nanomaterials by exploiting their unique properties for a variety of novel applications. Recently, graphene has been the prominent candidate, as it combines exceptional electrical, mechanical, thermal and optical properties [2-5], in a 2D crystal lattice. Very high carrier mobility, ambipolar behavior, record high thermal conductivity, very high mechanical strength and nearly perfect optical transparency are just some of the amazing properties of graphene. From high performance RF transistors [6], to energy storage applications [7], biosensors [8], flexible displays [9], and organic photovoltaics [10] graphene related research has boomed since its isolation in 2004 from Geim and Novoselov [11].

Limited has been done though, to examine, how graphene-based devices operate in a radiation harsh environment. Conventional electronics suffer from significant performance and reliability issues when exposed to high-energy ionizing radiation [12]. To this day, research has been mostly focused on the effects of process related irradiation (10-200 KeV energy range) during device fabrication [13-15]. The effects of higher energy radiation (MeV range) such as the one found in space environment or after the deployment of weapons of mass destruction (WMDs) remain mostly unknown. There are several challenges associated with radiation damage on graphene. The fact that graphene

has minimal cross-section to interact with radiation and that the carbon to carbon bonds have an entropic drive to destabilize and form 3D or amorphous assemblies may play an important role on its radiation hardness. In addition, its sensitivity to environmental doping and the role of the substrate/dielectric are two key factors that can significantly affect graphene's electronic performance and need further investigation.

This work aims to investigate the effects of high-energy radiation (alpha, beta, gamma and ion) on graphene-based field effect transistors (GFETs). We focus on the effects on the material and device level, and propose different device structures that can mitigate those effects. Finally, we integrate the fabricated GFETs on a small satellite (cubesat) for in-situ radiation measurements in low Earth orbit (LEO) environment.

1.2 Graphene Properties

1.2.1 Crystal and Band Structure

Graphene is a single layer of sp^2 hybridized carbon atoms arranged in a honeycomb lattice as shown in figure 1.1. This crystal structure gives rise to a unique band structure that is responsible for the exceptional electronic properties of graphene. Each carbon atom is spaced about 1.42 Å from its neighbor one, and linked through strong intra-layer covalent bonds that are responsible for the excellent mechanical properties and stability of graphene. In contrast, the forces between different graphene layers are van der Walls [16, 17] with a spacing in the order of 3.35 Å. As a consequence, the isolation of a single sheet of graphene is favorable and can be easily achieved through exfoliation.

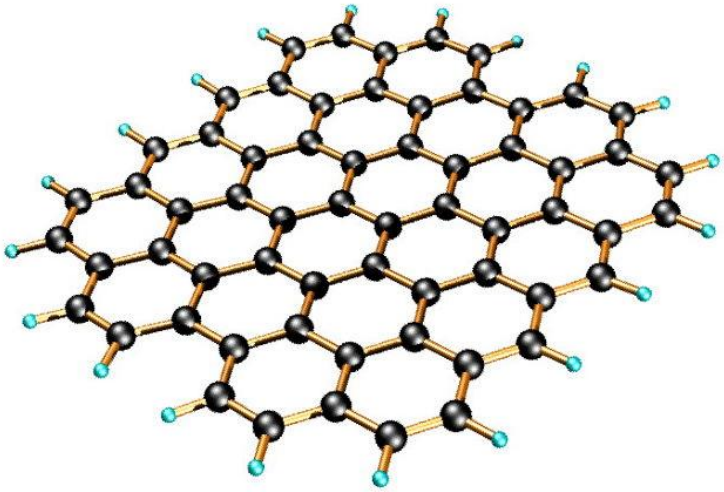

Figure 1.1. Schematic representation of graphene's honeycomb crystal structure.

Bulk graphite for example, which is the most common allotrope of carbon, consists of thousand interconnected layers of graphene that are loosely bound and can be separated by applying small forces (i.e. scotch tape method).

Graphene's band structure is the source of its peculiar electronic properties. Each carbon atoms shares three σ bonds with its neighbor atoms and one out of plane π bond (in z-direction). All the π-bands are hybridized together to create a π-band, which gives rise to an electronic structure where the valence band and the conduction band meet at the Dirac points. The Dirac points are location in K-space (momentum) on the edges of the Brillouin zone. Thus, graphene is considered a zero band-gap material (figure 1.2) with a linear dispersion relation that can be approximated by

$$E = \hbar v_F \sqrt{k_x^2 + k_y^2} \tag{1.1}$$

where the wavevector k is measured from the Dirac points. This linearity implies that effective mass of charge carriers is zero (massless Dirac fermions) which leads to unprecedented carrier mobility. With Fermi velocity (v_F ~10^6 m/s) that is independent from energy, charge carriers in graphene form a two-dimensional electron gas (2DEG) similar to materials like GaAs-AlGaAs heterojunctions [18] and topological insulators [19].

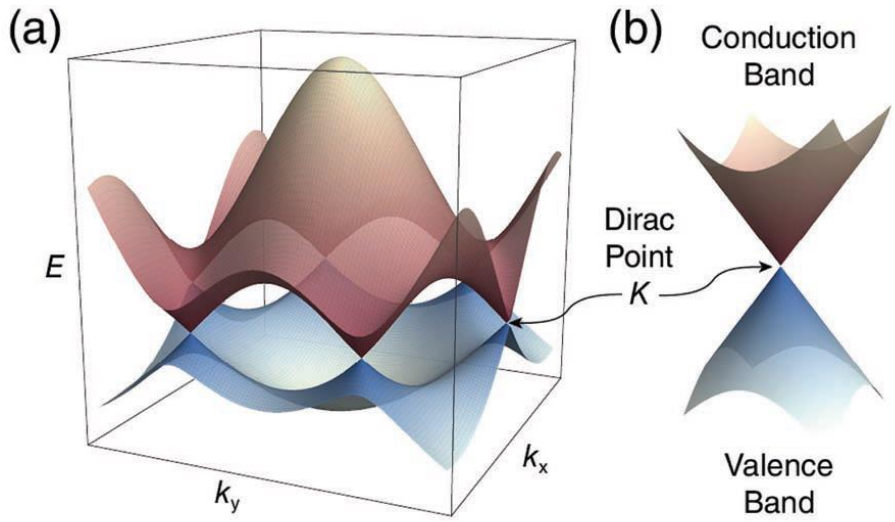

Figure 1.2. (a) Band structure of graphene (b) Linear dispersion relation of graphene showing the position of the charge neutrality point (Dirac point).

Electrostatic doping (such as the one applied by an external electric field) can change the carrier type (electron or hole) and the carrier density (from 10^{11} cm^{-2} to 10^{13} cm^{-2}) of graphene resulting in a Fermi level within the conduction or valence band. By connecting the carrier density n to the momentum k, we can write the relation Eq. 1.1 as

$$E = \hbar v_F \sqrt{\pi n} \tag{1.2}$$

This results to a clear ambipolar behavior of graphene that plays a key role in the operation and performance of GFETs.

1.2.2 Electronic and Transport Properties

Graphene's feature that has attracted the highest interest is its remarkably high carrier mobility, with reported values up to 200,000 cm^2/Vs for suspended samples at cryogenic temperatures [20]. Room temperature mobility can reach values up to 140,000 cm^2/Vs [21]. The main scattering mechanism is through acoustic phonons that are responsible for the intrinsic limit of mobility mentioned above. When graphene is supported by a substrate such as Si/SiO_2 the mobility is limited to values of ~ 40,000 cm^2/Vs as charged impurity scattering is the main cause of mobility degradation [22]. As a consequence, increased impurity and defect density due to the environment or the fabrication/transfer process can limit the real world performance and increase the hysteric behavior of such graphene-based devices.

There are two transport regimes in graphene. Charge carriers can have can be ballistic transport even at room temperature [23] where they can travel without scattering for several hundreds of microns. On the other hand, due to impurities, interaction with the substrate, defects and edges and ripples of graphene, transport is diffusive and temperature dependent. Saturation velocity is in the order of 7×10^5 m/s while resistivity of graphene sheets can be as low as 10^{-6} Ωcm [22]. The maximum current densities can be as high as 5×10^8 A/cm, which is orders of magnitude higher than copper.

As the lack of bandgap is limiting the use of graphene in applications that a low off-current is required (digital logic applications), researchers have been intensively studying the prospects of inducing a sizeable bandgap in intrinsic graphene. There are three main ways that a bandgap can be opened in graphene: cutting graphene in nanoribbons and confining carriers to one dimension, applying an electric field to bi-layer graphene and applying strain [24-26]. Bandgaps in excess of 200 meV have been experimentally showcased but mobility numbers decrease significantly when a bandgap is induced [43], as shown in figure 1.3. Digital logic applications need a bandgap comparable to the one of silicon (1.1 eV), which entails nanoribbons of few nanometers wide (as bandgap is inversely proportional to nanoribbon width). Furthermore, rough edges or any other disorder on the nanoribbon geometry will have a significant effect on the bandgap thus, making their fabrication extremely challenging.

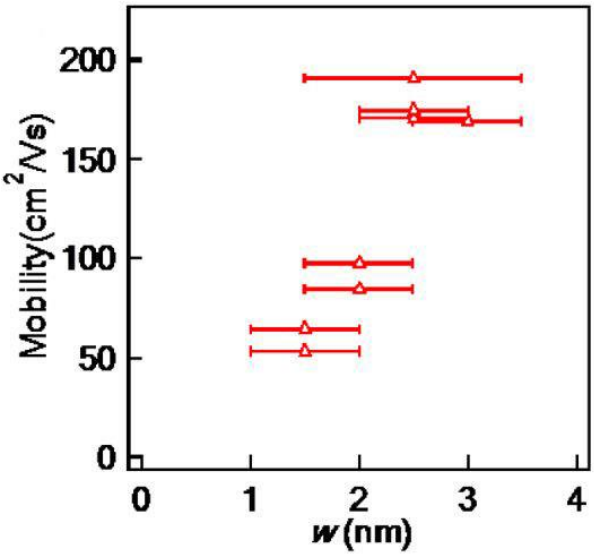

Figure 1.3. Graphene's mobility dependence on the nanoribbon size.

1.2.3 Other Properties

Graphene's mechanical properties are as impressive as its electrical ones. Due to the sp^2 bonds, graphene has an instrinsic tensile strength of 130 GPa and a Young modulus of 1 TPa [28], making it the strongest material in existence. In addition, graphene's fracture strain is in the order of 38%, making it suitable for use in flexible electronics.

Graphene exhibits record high thermal conductivity of approximately 5300 $W \cdot m^{-1} \cdot K^{-1}$ [29] and an optical transparency of 97.7% in the visible spectrum [30] with reflectance as low as 0.1%. With a sheet resistance of ~0.1-6kΩ/□ it is a very good candidate for use as a transparent conductor. Graphene is also chemically inert surface with exceptional stability up to 1000 °C.

1.3 Graphene Synthesis

To this day, there are various methods for the synthesis and production of graphene. Each method has its own advantages and challenges, with some focusing on higher quality graphene, where others are targeted for large-scale production and scalability. Techniques like Chemical Vapor Deposition (CVD), mechanical exfoliation, epitaxial growth on silicon carbide, unzipping carbon nanotubes and sonication/reduction of graphene oxide (GO) can be used for the production of single or multi-layer graphene. In the next section, we are focusing our analysis on the most widely used methods

1.3.1 Mechanical Exfoliation

This is the method that Geim and Novoselov used in order to isolate single graphene sheets from a piece of graphite [11]. The so-called “Scotch Tape Method” uses an adhesive tape to separate graphene layers from a highly oriented pyrolytic graphite and transfer them to a flat substrate (figure 1.4a). This method produces the best quality graphene flakes, but with very limited control on the size, thickness and location. Transferred flakes can be identified with the use of optical microscopy or Raman spectroscopy. This makes mechanical exfoliation the ideal method for high quality device fabrication as it gives the ability to access the intrinsic properties of graphene. However, lack of scalability limits the use from more practical applications.

1.3.2 Epitaxial Growth on Silicon Carbide

This method is based on the thermal decomposition of SiC when heated between 1000 °C to 1500 °C in ultra high vacuum (UHV) [31]. Silicon will sublimate from the substrate while carbon atoms reconstruct and form graphitic layers (figure 1.4b). The thickness of the layers depends strongly at the temperature, however precise control of the exact number of layers still remains a challenge. The main advantage of this method is that it is scalable and can be conducted using commercially available SiC wafers. Although large-scale synthesis is possible, graphene grown films have to be transferred to a target substrate for device processing. As a result, epitaxial growth produces lower

quality graphene compared to exfoliation and is primarily limited by the high cost of SiC wafers.

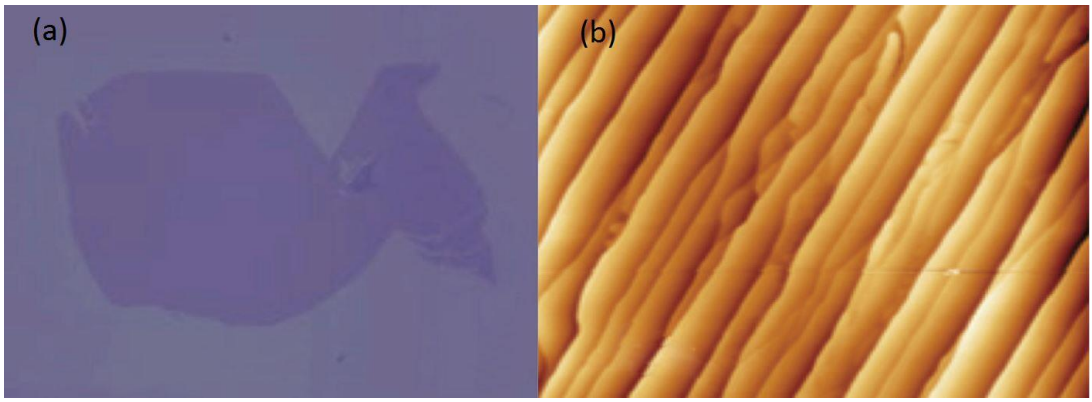

Figure 1.4. (a) Optical image of exfoliated graphene on top of SiO_2 (b) AFM image of graphene grown on SiC.

1.3.3 Chemical Vapor Deposition (CVD)

Graphene grown by CVD is one of the most promising methods available for producing high quality and scalable graphene films. By thermal decomposition of hydrocarbons (such as methane) on transition metals substrates (Ru, Co, Ni, Cu) [33-36] single or multilayer graphene films can be grown (figure 1.5a). Followed by a transfer process, CVD grown films can be transferred to arbitrary substrates for further device processing. The number of graphene layers is highly depended on the solubility of carbon on the target substrate. For example, when Ni (high solubility substrate) is used, carbon atoms dissolve into the substrate at high temperatures (1000 °C) and then segregate during cooling, to form 1-10 layers of graphene. However, poor thickness control makes impractical for use in electronic device fabrication.

In contrast, carbon has very low solubility in copper (Cu) and thus, Cu substrates are preferred for use in the CVD process. That enables complete monolayer coverage of

the substrate as a self-limiting growth mechanism prevents the formation of multilayer films [37] as shown in figure 1.5b.

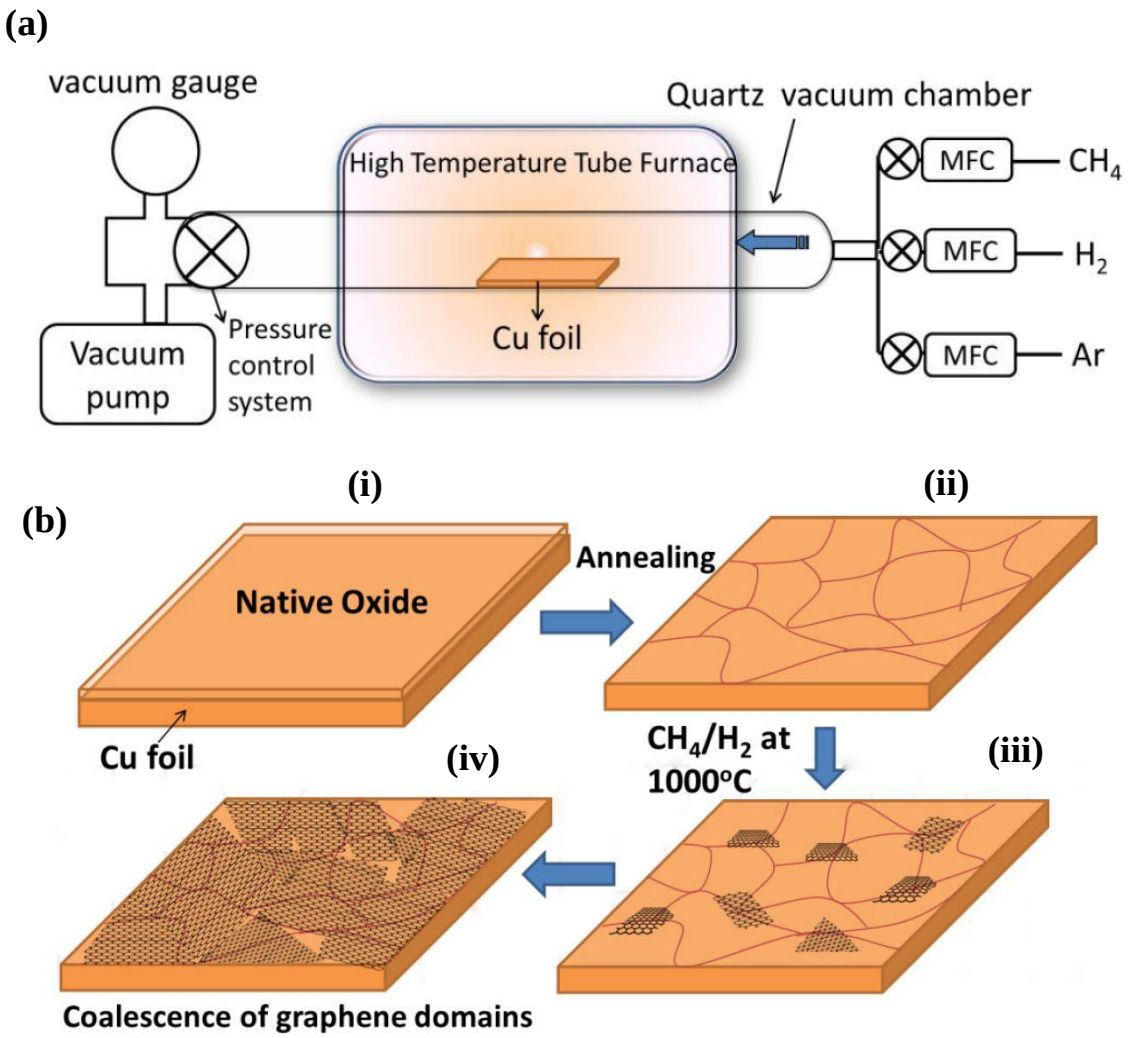

Figure 1.5. (a) Schematic illustration of a graphene CVD system (b) (i) Copper substrate with native oxide (ii) H_2 annealing removes the native oxide (iii) Nucleation of graphene islands after decomposition of carbon from methane at 1000 °C (iv) formation of graphene film with different lattice orientation.

It was first demonstrated by Rouff's group in 2009 [36] and recently a roll-to-roll process was demonstrated where they produced layers up to 30 inches wide [38]. CVD graphene is formed by multiple micron-sized domains, which are randomly aligned and

give rise to inter-domain defects [39]. Significant effort from multiple research groups has been carried out in order to reduce the number of grain boundaries and growth related defects, thus, matching the quality of exfoliated graphene. The scalability and cost effectiveness of this method makes it the prominent synthesis technique for large area graphene electronics.

1.4 Scope of Research

This work aims to investigate the effects of radiation damage mechanisms in graphene-based devices. Our fabricated graphene-based field effect transistors (GFETs) are tested under high-energy radiation (alpha, beta, gamma and ion) conditions. By using a set of characterization tools and probes we focus on the effects on the material and device level, emphasizing on the performance degradation metrics after irradiation. Specifically, the effects on the carbon-to-carbon bonds and crystal lattice, the degradation of graphene's transport properties, the role of the environmental doping, and finally, the substrate/ gate dielectric interaction, are thoroughly studied.

In addition, we propose and develop different device structures that can mitigate the irradiation effects. Our radiation-hardened devices make use of an encapsulation layer for protection from the ambient environment (reactive oxygen and water) and an insulated gate structure that isolates the device from the substrate effects. Finally, the fabricated GFETs are put on board a satellite (Λ-sat) for real time radiation measurements in low Earth orbit environment.

Chapter 2

Graphene Field Effect Transistors (GFETs)

2.1 Introduction

It's been more than four decades that the metal oxide field effect transistor (MOSFET) has been dominating the electronic device industry. Digital electronic circuits that are found nowadays on myriad applications are solely dependent on the evolution and performance of MOSFETs. Scaling transistor's gate length has been the driving force for the semiconductor industry, enabling the transistor density to double every 24 months (Moore's Law). While the cost per transistors keeps decreasing, scaled MOSFETs perform better and consume less power [41]. However, as we reach sub-100 nm gate lengths, a lot of challenges arise regarding the fabrication and operation of transistors. The so-called short channel effects (velocity saturation, drain induced bias lowering, threshold voltage roll-off etc.) are responsible for the degradation of performance and unpredictable behavior of scaled devices [42]. Consequently, there is growing need for new materials and device structures that are robust against those effects.

Graphene was introduced as a potential candidate to replace silicon for the fabrication of the next generation field effect transistors [27]. GFETs exploiting graphene's unique properties, such as very high carrier mobility, monoatomic thickness, and high saturation velocity, could enhance performance and reduce the short channel

effects for extremely scaled transistors. Unfortunately, due to lack of a sizeable bandgap, GFETs suffer from very poor on-off ratio (I_{on}/I_{off}) making them unsuitable for CMOS logic applications. However, the use of GFETs in radio frequency applications [6] is very promising, as RF transistor's performance is not dependent on their switch-off properties (they operate in on-state). The high carrier mobility of graphene leads to very high cutoff frequency (f_t) operation, which is the most important figure of merit for RF transistors.

The primary focus of this work is to study the effects of irradiation on graphene-based devices using GFETs as our testing platform. In the next section, we discuss the basic operation of GFETs focusing on performance metrics that are relevant to our radiation damage study.

2.2 Device Structure and Operation

As shown in figure 2.1 the standard GFET structure resembles a lot of similarities compared to a conventional MOSFET. In few words, field effect transistors consist of three electrodes (drain, gate and source) along with a dielectric layer separating the gate electrode from the channel. The key concept of a MOSFET is that channel conductivity can be controlled by applying a gate voltage (V_{gs}). The main structural difference between the MOSFET and GFET is that the conductive channel in MOSFETs (made of silicon), which is induced when a large enough Vgs (Vgs>Vt) is applied, is replaced by graphene. That results in a FET device structure (GFET) with significantly different performance and device characteristics than conventional MOSFETs.

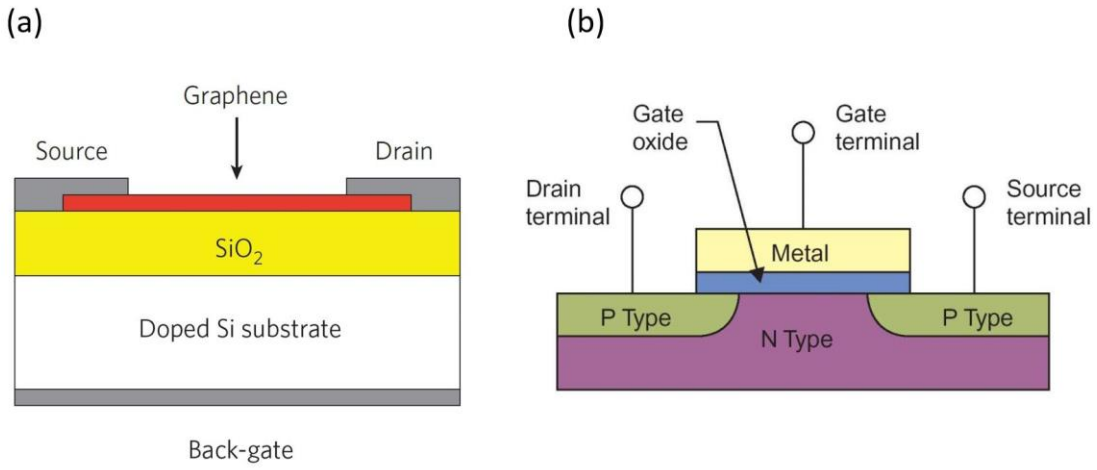

Figure 2.1. (a) Schematic illustration of a back-gate GFET (b) Schematic illustration of a conventional NMOS.

GFET's main principle of operation is based on the tuning of the charge carrier density (electrons or holes) when applying an electric field (gate voltage) between the substrate and the graphene channel. As a consequence, GFETs have ambipolar behavior, thus, don't need to be doped (as in the case of silicon-based MOSFETs) to operate as a p-type or n-type transistors. When a gate voltage is applied, a surface charge density of the form

$$n = \varepsilon_0 \varepsilon V_g / te \tag{2.1}$$

where $\varepsilon_0\varepsilon$ is the permittivity of dielectric, Vg is the applied back-gate voltage, t is the thickness of the oxide and e is the electron charge, is induced. As we can see from figure 2.2a, the applied gate voltage (positive or negative) can change the position of Fermi level (E_f), which can either move inside the valence or conduction band. Theoretically,

the charge density (n) should be zero at the Dirac point [3], but thermal excited carriers and electrostatic spatial inhomogeneities prevent that from happening (figure 2.2b) [118].

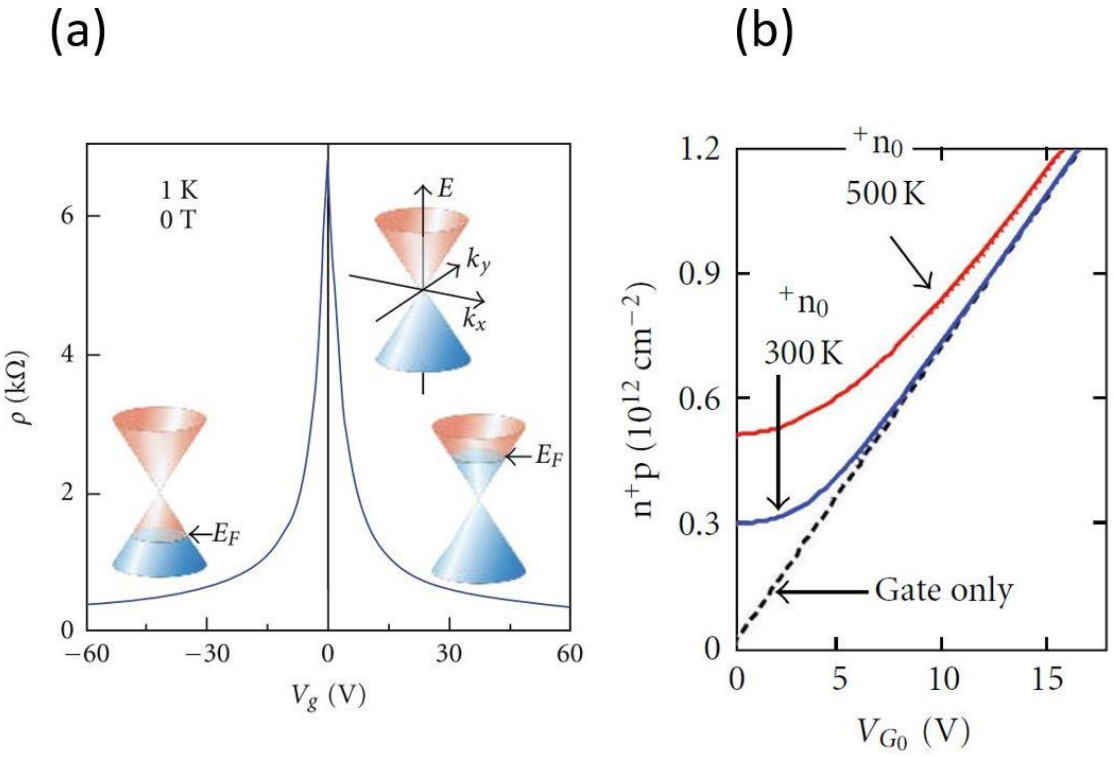

Figure 2.2. (a) Ambipolar behavior of GFETs, Fermi level position change as a function of Vgs (b) Temperature depended charge density of graphene.

Therefore, GFET exhibits unique transfer characteristic that embodies the ambipolar behavior discussed above. As seen in figure 2.3, when a large positive gate voltage is applied the channel accumulates electrons (n-type channel), whereas a negative gate voltage will lead to accumulation of holes (p-type channel). These two distinct branches meet at the Dirac point (minimum conductivity point). The position of the Dirac point is of crucial importance as it gives a good indication of the intrinsic doping levels [44] and it is directly related to the sheet carrier density, n as $n=C_g(V_g-V_{Dirac})/e$, where C_g is the gate capacitance and e is the elementary charge.

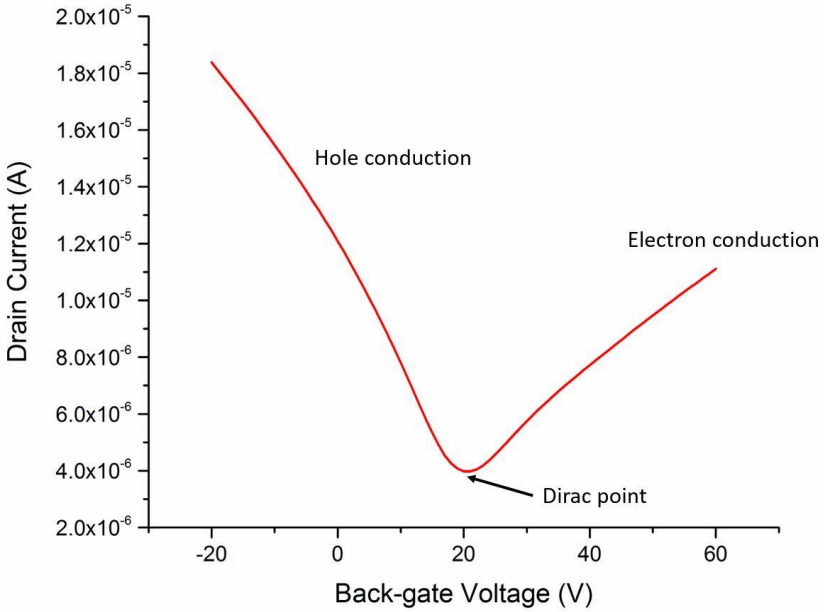

Figure 2.3. Transfer characteristic (Id-Vgs) of GFET showing the two distinct regions of conduction (hole-electrons) and the position of Dirac point.

Another important metric for the performance of GFET is field effect mobility (μ_{FE}). Although mobility is arguably the most frequently stated advantage of graphene, actual device μ_{FE} values vary significantly. Due to imperfections on graphene's crystal lattice [45], impurities [44], interaction with the substrate [22], cracks and ripples [46], μ_{FE} is severely affected as charge carriers withstand increased scattering. The extraction of μ_{FE} can be computed directly from the transfer curve of graphene using the following equation

$$\mu_{FE} = \frac{L_{ch} g_m}{W_{ch} C_g V_{DS}} \tag{2.2}$$

where L_{ch} and W_{ch} are the length and width of graphene channel, C_g is the gate capacitance per unit area and g_m the intrinsic transconductance expressed as:

$$g_m = \frac{d\, I_D}{d\, V_{gs}} \tag{2.3}$$

The μ_{FE} for the fabricated devices in our study range from the 300-1,500 cm^2/Vs, which is comparable to values reported using small grain CVD graphene and room temperature measurements [47].

2.3 Device Fabrication

GFET fabrication is a multi-step process that involves three main operations: Graphene CVD growth, transfer to the desirable substrate and finally device fabrication. Each step needs to be optimized as much as possible in order to minimize fabrication induced defects and unintentional doping that can limit GFET's performance. In the following sections we are going to discuss in details all the necessary steps and optimizations we performed to fabricate our GFETs.

2.3.1 CVD Growth

The CVD grown graphene we used this work was synthesized in Prof. Hone lab using a low-pressure CVD (LPCVD) system shown in figure 2.4a. Graphene was grown in a 1-inch tube furnace at 1000 °C on top of 25 μm copper foils. Before the actual growth, copper foils were annealed (800 °C) using hydrogen at a pressure of 50 mTorr in order to remove the native copper oxide. Subsequently, methane is introduced in the tube

and growth is conducted at 300 mTorr for 30 minutes. Figure 2.4b shows a copper foil with a single layer of graphene on top (SLG) right after growth.

Figure 2.4. (a) CVD system used for graphene growth (courtesy of Hone's group) (b) Copper foil right after CVD synthesis.

2.3.2 Graphene Transfer

Graphene transfer is an important step during GFET fabrication since it determines to a great extent, the overall quality and performance of the final device. Transfer induced defects such as, increased p-doping from impurities trapped between the interfaces, and structural defects (cracks and wrinkles) of graphene, need to be minimized during the transfer process [48,49].

Our transfer process (figure 2.5) starts with the spin coating of a thin layer of poly(methyl methacrylate) (PMMA) acting as a supporting layer on top of the Cu foil at 3000 rpm for 45 s, followed by an annealing step at 145 °C for 2 min. In order to etch unwanted graphene from the backside of the Cu foil, reactive ion etching (RIE) was used

for 20 s at 50 W. Polydimethylsiloxane (PDMS) stamps were prepared, cured at 80 °C for 90 min, and placed on top of the PMMA layer as an extra supporting layer. We developed a slightly modified transfer process compared to the standard PMMA method [50] where adding PDMS stamps on top of PMMA gives us the advantage of being able to transfer graphene with few defects and low impurity doping. The whole Cu foil/ graphene/PMMA/ PDMS stack was inserted in ammonium persulfate (APS) copper etchant solution for 5 h, followed by an overnight rinsing step in deionized (DI) water, and a final 24 h drying step before being transferred. Si/SiO2 substrates were previously cleaned by Piranha to eliminate possible organic contaminants on the surface. Substrates were heated at 180 °C as the PDMS/PMMA/graphene stack was placed carefully on top, promoting adhesion between graphene and the substrate. Substrates were then submerged in a chloroform bath for 2 h in order to dissolve PMMA and rinsed in isopropyl alcohol (IPA). Thermally evaporated Cr/Au (3 nm/50 nm) was deposited using a shadowmask for defining the drain/source contacts. Shadowmasking was used in our process in order to reduce the possible unwanted contamination/doping of graphene, as is the case when using a standard lithographic process [51].

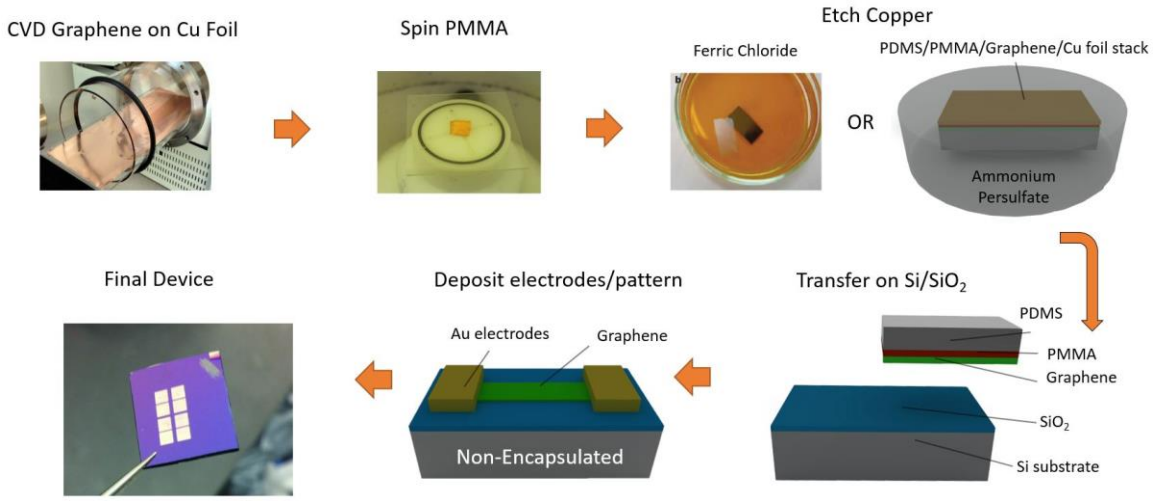

Figure 2.5. Graphene transfer steps from growth to final back-gate device fabrication.

2.3.3 Raman Spectroscopy

Raman spectroscopy is a very important characterization tool and a very convenient way to characterize the crystal quality, thickness (number of graphene layers), disorder and doping profile of graphene [52-54]. As it is a non-destructive measurement, it can be applied to evaluate the quality of as-grown or transferred graphene. The most prominent peaks in the Raman spectrum (figure 2.6) are the G band (~1580 cm^{-1}), the 2D band (~2680 cm^{-1}) and the D band (~1350 cm^{-1}).

The G band is due to in-plane vibrations of the sp^2 carbon atoms and consists the most prominent peak of graphitic materials. The 2D band comes as a result of the two-phonon resonance process and the D band (also called the “defects” peak) comes from the in-plane optical phonons (corresponding to the induced defects) of the crystal lattice. The absence of D peak is a result of a high quality (high crystallinity) graphene lattice. In addition, the shape of 2D peak and its intensity compared to G peak is used to characterize the number of graphene layers present. When this ratio (I_{2D}/I_G) is more than

two [53], graphene consists of one single layer of carbon. Furthermore, the position of G and 2D peaks (and more specifically the upshift) as well as the broadening of 2D peak (FWHM) is indicative of the doping profile of graphene.

As shown in figure 2.6, the quality of graphene used in our devices is very good, with no D peak present (high crystallinity) and I_{2D}/I_G ratios of more than 3. As it will be evident later in the thesis, Raman spectroscopy will be our primary characterization technique to evaluate the radiation-induced defects and the doping profile of irradiated graphene.

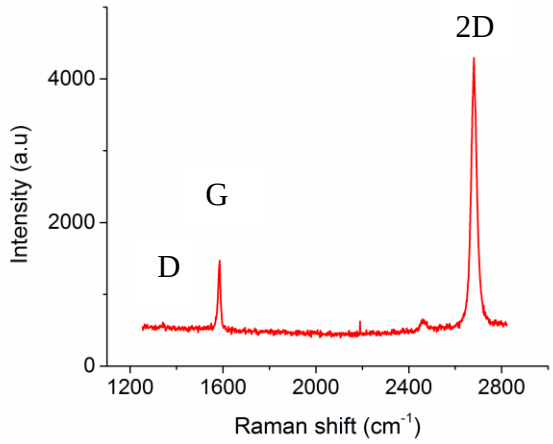

Figure 2.6. Raman spectrum of graphene on top of Si/SiO_2 substrate.

2.3.4 Non-encapsulated GFETs

The standard back-gate GFET structure is our reference device for studying the radiation effects on graphene. As shown in figure 2.7a,c, the graphene channel is exposed to both ambient environment and incoming radiation, giving us the advantage to perform surface characterization techniques (such as Raman and X-Ray photoelectron spectroscopies) on the device. All non-encapsulated device structures were fabricated on top of thermally grown 300 nm SiO_2 on a heavily p-doped Si substrate that we use as our

local back-gate. As described before, drain and source electrodes (Cr/Au) were patterned using shadowmasks with channel lengths of 100 μm and channel widths varying from 1-3 mm. Some of the first devices tested, as shown in figure 2.7b, were fabricated using standard lithographic processes, with channel lengths as low as 10 μm.

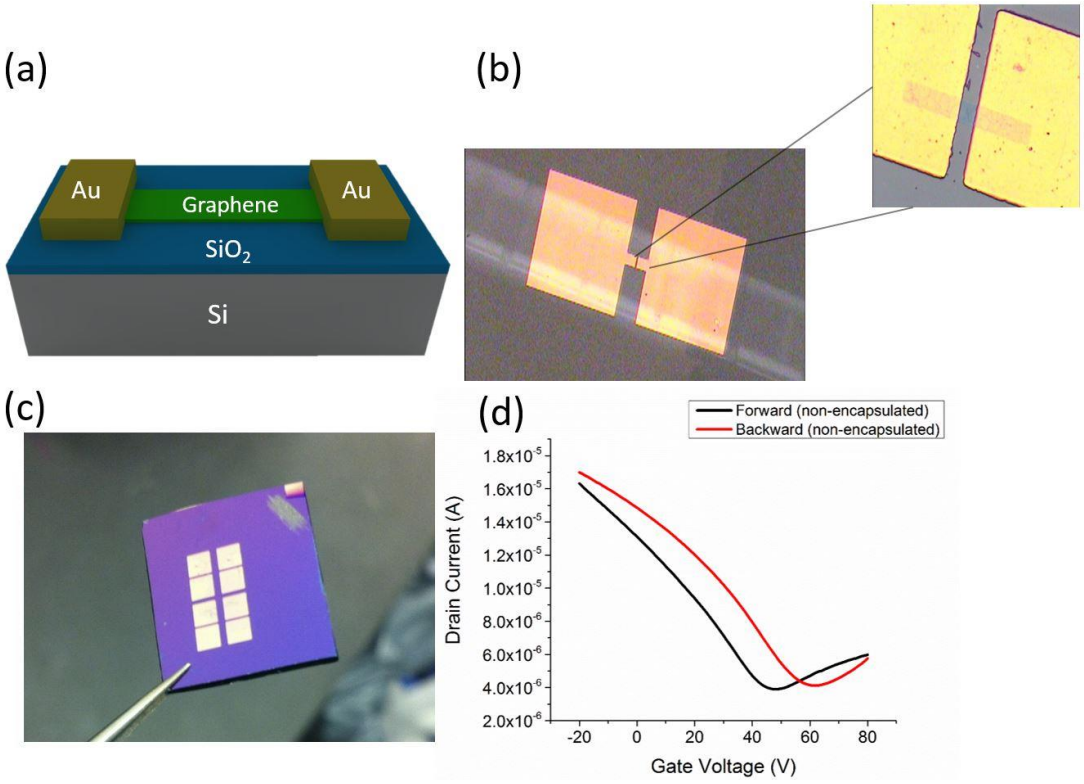

Figure 2.7. (a) 3D schematic of the fabricated back-gate GFET (b) Optical image of the lithographically processed device with a 10 μm x 10 μm channel (W x L) (c) Finished back-gate structure using shadowmasking (d) Typical I_d-V_{gs} curve of the non-encapsulated back gate devices (Hysteretic behavior).

The lithographic process was abandoned as the main fabrication technique, since those devices were suffering from severe p-doping. This is due to the increased number of fabrication steps (spin coating of the photoresist, development, lift-off) that resulted in increased impurity doping of graphene [51]. Figure 2.7d, shows a typical transfer curve of the non-encapsulated GFET. All devices structures throughout this work were

electrically characterized using the Keithley 4200 Parameter Analyzer and a 3-probe setup, at room temperature and ambient atmosphere. Field effect mobilities of non-encapsulated devices were between 300-800 cm^2/Vs (at carrier densities of 0.5-1.2 $x10^{12}$ cm^{-2}), limited from the increased scattering (small grain graphene), impurities [44], interaction with the SiO_2 [22], cracks and ripples and unintentional doping from the surrounding environment [55]. The position of the Dirac point, for the majority of devices, was between 20-60 V, indicating p-doped behavior. Unfortunately, these devices show hysteretic behavior (ΔV_{Dirac} ~10-20 V) due to the trapped charges in the gate oxide (SiO_2)/graphene-oxide interface, as well as the PMMA residue that remains on graphene after transfer.

It is evident form the electrical measurements of the non-encapsulated devices that a passivation layer is needed in order to operate in ambient environment. Moreover, as it will be later discussed, encapsulating graphene enhances the radiation shielding properties of GFETs.

2.3.5 Encapsulated GFETs

Graphene's large surface to volume ratio means that the surrounding environment can directly affect its electronic properties due to the chemical adsorbents that can cause unintentional doping [55]. In order to achieve very high electron mobility or cut off frequency, graphene devices must be isolated from the environment, often operating under ultra-high vacuum conditions and at temperatures as low as 5K. When a back-gated graphene transistor is exposed to the ambient environment, water molecules and oxygen will get adsorbed, leading to a p-doped graphene surface, where the Dirac point shifts to

higher gate values and the electron conduction gets suppressed even further [56]. Increased doping results in reduced performance and reliability of the fabricated graphene devices, limiting their use in practical applications where high vacuum and low temperatures conditions cannot be met. Consequently, characterizing and understanding the effect of the surrounding environment on graphene as well as developing an encapsulation method that will limit undesirable doping are of prominent importance.

Various methods, such as inserting a fluoropolymer between graphene and the gate dielectric [57], capping graphene with a thin oxide layer [58,59], or encapsulating the graphene channel with an organic semiconductor [60], have shown that the electrical characteristics and stability of graphene field effects transistors (GFETs) can be further improved when isolated from the environment. In addition, graphene encapsulated between hexagonal boron nitride (hBN) flakes has been demonstrated [61], exhibiting exceptional air stability while making it insusceptible to the surrounding environment. However, some of these methods are impractical for being integrated when using CVD grown graphene, as they are based on the use of mechanical exfoliation, while others do not achieve prolonged insulation from the environment for more than few weeks. We have developed an encapsulation method that is based on the deposition of a thin Parylene-C and aluminum layer on top of the exposed graphene that resolves the aforementioned problems. Parylene-C belongs to a family of polymers that has already been used as a water/moisture barrier for organic light emitting diode (OLED) passivation [62] and as coating for flexible electronics applications [63]. In addition, the

combination of Parylene-C and aluminum has been reported to provide excellent passivation and stability of air-sensitive organic semiconductor devices [64].

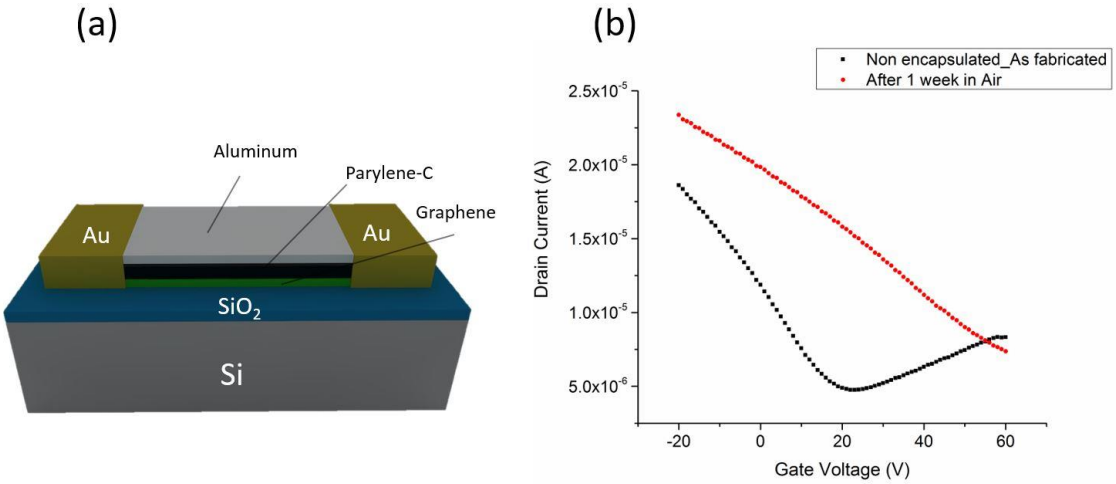

Figure 2.8. (a) 3D schematic of the encapsulated back-gate GFET (b) Transfer characteristics of the non-encapsulated GFET before and after 1 week of air exposure.

The fabrication process for the encapsulated device is identical with the one described before (non-encapsulated device), with an additional deposition of 1.25 μm of Parylene-C (CVD method) and 50 nm of thermally evaporated aluminum film (figure 2.8a). Transfer characteristics of the fabricated device without any encapsulation layer are shown on figure 2.8b. The Dirac point of the as-fabricated device is at 22.3V with a field effect mobility of 877 cm^2/Vs showing clear p-doped behavior in ambient environment. This p-doped behavior is in accordance with previous reports where functional groups [65], adsorbents [66], and trapped water molecules between graphene and substrate can cause this p-doping effect. Furthermore, measurements taken a week after the device was left in air clearly show the positive Dirac shift expected from additional p-doping of graphene due to adsorbed molecules. In the absence of any

passivation/encapsulation layer, the Dirac point shifts to gate voltage values higher than 60V and the field effect mobility degraded to 512 cm^2/Vs, a substantial difference from values attained immediately after fabrication. Many studies so far have indicated that an annealing step on a fabricated device [67,68] is crucial in order to recover the lost performance caused by the unintentional p-dopants. As we show in figure 2.9a, annealing the device at 180 °C for 1 min on a hotplate was enough to desorb the p-dopants on the surface and set the performance of the device to its as-fabricated levels. Although annealing is definitely one way to reset the device performance to the as-fabricated state, it has limited practical use in real-world device applications and does not offer a permanent solution since the device will again return to a p-doped state when left in air.

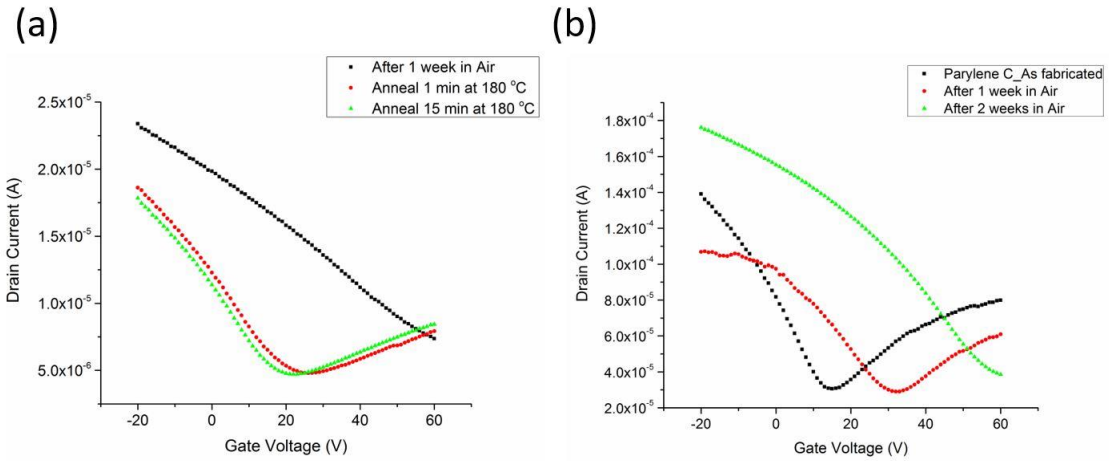

Figure 2.9. (a) Effect of hotplate annealing at 180 °C to the air exposed non-encapsulated device (b) I_d-V_{gs} transfer characteristic of devices encapsulated with Parylene-C layer of 1.25 μm after 1 and 2 weeks of air exposure.

Figure 2.9b shows the effect of encapsulation when 1.25 μm of Parylene-C was deposited on top of graphene. The as-fabricated device initially had a Dirac point at 14.1V with μ_{FE}=1860 cm^2/Vs. After being exposed to air for a week, the Dirac point shifted to 32V with a mobility of 1206 cm^2/Vs. Performance degradation of our device

continued, and after two full weeks of air exposure the Dirac point shifted to values higher than 60 V, and to μ_{FE} less than 965 cm^2/Vs. A ΔV_{Dirac} of 50V after 2 weeks of air exposure clearly suggests that an encapsulation layer consisting only from Parylene-C is not enough to fully passivate the device from the surrounding environment.

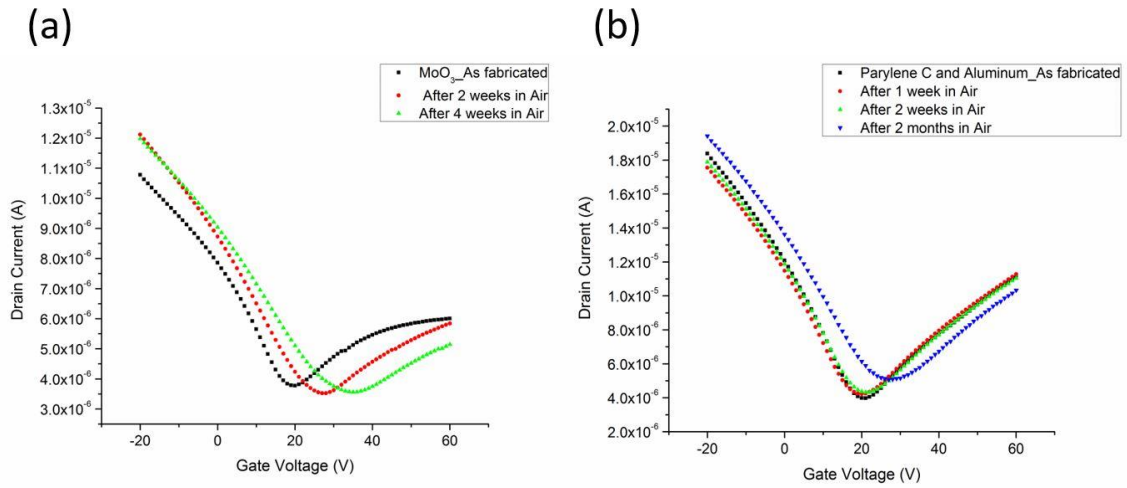

Figure 2.10. (a) Transfer characteristic of GFETs with an encapsulation layer consisting of 1.25 μm Parylene-C/50 nm MoO_3 after 2–4 weeks of ambient air exposure. (b) Id-Vgs of the device encapsulated with 1.25 μm Parylene-C/50 nm Al after being exposed to ambient air for as long as 2 months.

In order to enhance the passivation properties even further, we thermally evaporated a 50 nm MoO_3 layer on top of the Parylene-C. MoO_3 belongs to the metal oxide family of materials that exhibit great stability in air and have been used in OLED fabrication. Figure 2.10a shows the effect of the Parylene-C/MoO_3 encapsulation layer deposition on top of graphene channel area. An initial V_{Dirac} of 19.1V shifted to values of 26V and 35V after 2 and 4 weeks of air exposure, a substantial improvement over the Parylene-C encapsulation layer that was characterized before. The Parylene-C only encapsulated device exhibited a V_{Dirac} shift of 50V after 2 weeks of air exposure, whereas the combination of Parylene-C/MoO_3 encapsulated device exhibited a V_{Dirac} shift of 6.9

V. In addition, μ_{FE} of the as-fabricated device fell from 593 cm^2/Vs to 507 cm^2/Vs (14.5% decrease) and to 436 cm^2/Vs (26.48% decrease) after 2 and 4 weeks in air, , a much improved behavior when compared to the Parylene-only device that saw its mobility degrade for more than 48% (from 1860 cm^2/Vs to 965 cm^2/Vs). These results clearly indicate the importance of a second layer on top of Parylene-C to further improve the passivation of graphene from the surrounding environment.

Further optimization of the encapsulation layer resulted in replacing MoO_3 with an aluminum layer that we deposited on top of Parylene-C. In agreement with previous studies, aluminum reacts with atmospheric oxygen when exposed to air, forming a thin layer of Al_2O_3 [69] that further inhibits the penetration of oxygen into the material. The oxygen blocking property of aluminum is highly desirable in our devices, where in conjunction with the Parylene-C layer we expect improved air stability. Figure 2.10b shows the transfer characteristics of GFETs fabricated with an encapsulation layer consisting of 50 nm Al deposited on top of 1.25 μm of Parylene-C. The device exhibits a V_{Dirac} shift of 1V when exposed to air for two weeks, while μ_{FE} deviates little from the as-fabricated values. Measurements after two months of ambient air exposure reveal that the device is still performing very close to the initial performance metrics with a ΔV_{Dirac} of 8.2V and μ_{FE} of 964 cm^2/Vs (a 5.5% decrease from the as-fabricated value). GFETs with a Parylene-C/Al passivation layer performed significantly better than the other fabricated devices, with promising air stability operation under months of air exposure and without the need for an annealing step.

In summary, air stable operation of GFETs was achieved from the development of an encapsulated version of our standard transistor structure. Fabricated devices exhibited very little performance and mobility degradation over a long period of time, with reduced electron-hole conduction asymmetry and minimal Dirac voltage shift. Our results show that the combination of Parylene-C and aluminum thin films deposited on top of the exposed graphene area are an excellent water/oxygen barrier fully compatible with the transistor fabrication process.

2.3.6 Insulated Gate GFETs

Figure 2.11a shows the insulated gate GFET device structure. Until now, both non-encapsulated and encapsulated devices used the heavily p-doped silicon substrate as a local back-gate. However, this may pose significant problems when these devices will be irradiated since the charge collection volume (silicon) is orders of magnitude higher (500 μm Si thickness) compared to a thin metal gate. For that reason, a 50 nm aluminum gate was thermally evaporated on top of the Si/SiO_2 substrate, followed by a 100 nm SiO_2 gate oxide film using plasma enhanced chemical vapor deposition (PECVD). The previously used Parylene-C/aluminum encapsulation method was also used on the insulated gate structures.

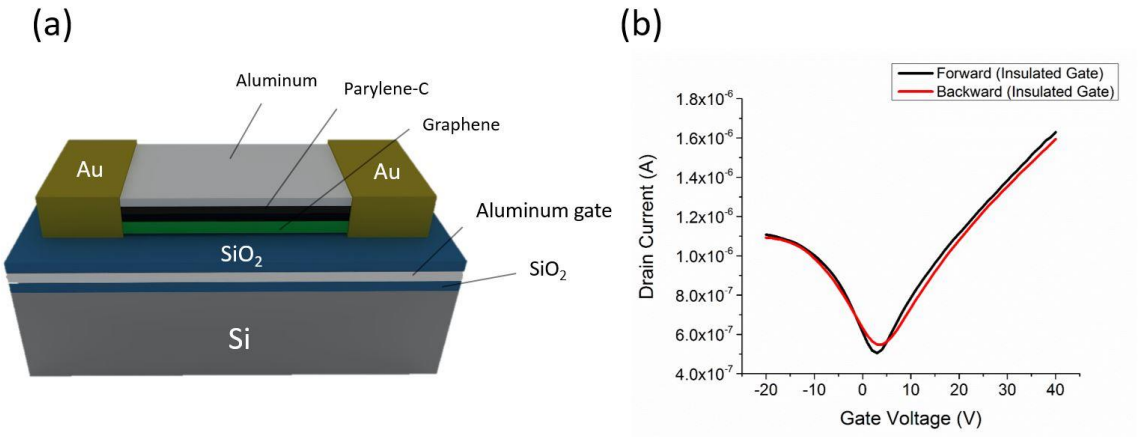

Figure 2.11. (a) 3D schematic of the insulated gate GFET (b) Transfer characteristics (I_d-V_{gs}) curve of insulated gate devices (no hysteresis).

On additional advantage of our insulated gate structure is that it suppresses the hysteresis effects on GFET operation. Hysteresis is mainly attributable to surface adsorbed water molecules in conjunction with hydroxylation of the SiO_2 surface, as well as charge traps between graphene and oxide interface. Figure 2.11b shows that almost no hysteresis is observed on non-irradiated insulated gate devices, in complete contrast to the hysteresis curve in figure 2.7d where non-encapsulated back-gated devices exhibited a 14 V positive shift of the Dirac point.

2.4 Chapter Summary and Conclusions

In this chapter, we described the operation and fabrication of our main structure, the GFET. Electrical and Raman characterization was conducted, focusing on device properties that are relevant to our GFET irradiation study. Electrical characterization results for the non-encapsulated structure showed hysteretic behavior, performance degradation, and increased instability when these devices had to operate in ambient

environment. This led to the development of a passivation layer, made of Parylene-C and aluminum, which offered substantially improved GFET performance. Finally, a third, insulated gate design structure was developed, with even better stability and performance characteristics. Up to this point, all device measurements conducted were in ambient environment, without any irradiation involved. In the next chapter, we describe the main types and sources of radiation that the aforementioned devices will be exposed to.

Chapter 3

Ionizing Radiation

3.1 Introduction

The term “ionizing radiation” refers to radiation that has enough energy to free electrons from atoms or molecules when interacting with them. Ionizing radiation consists of energetic particles (such as protons, alpha, ions) or electromagnetic waves (gamma, X-rays) travelling at high speeds with a variety of energies (from KeV to TeV). Exposure to ionizing radiation poses not only a significant risk for living beings (DNA structural damage), but to electronic devices as well. As it will be later discussed in this chapter, microelectronic devices are subject to radiation-induced degradation of their key performance metrics when exposed to a variety of radiation sources. We will examine the main types and sources of radiation, and focus in great detail on the various effects that electronic devices undergo when exposed.

3.2 Types of Ionizing Radiation

3.2.1 Alpha particles

Alpha particles consist of two protons and two neutrons (a helium nucleus) and are mostly produced by alpha decay (figure 3.1a). They have energies (kinetic energy) ranging from 1-7 MeV, and thus they are considered highly ionizing radiation. The carry

an electric charge of +2e, a net spin of zero, and travel with a velocity up to 5% the speed of light. Alpha particles can be found in space radiation environments (originating from galactic cosmic rays and solar radiation), nuclear explosions (weapons of mass destruction) and nuclear fission. Due to their charge and relative large mass, alpha particles can be stopped easily by human skin or a sheet of paper (figure 3.1b) and can travel only few centimeters in air.

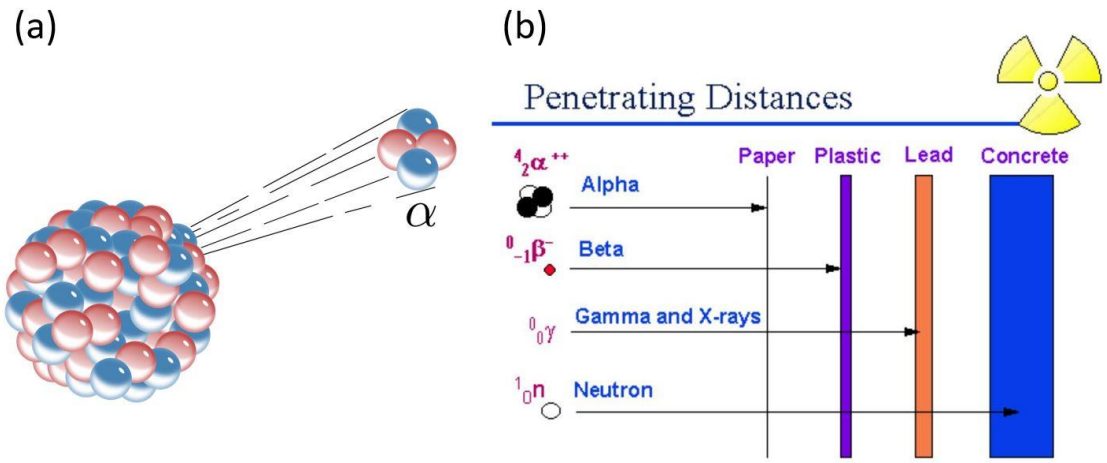

Figure 3.1. (a) Emission of alpha particles from alpha decay (b) Penetrating distance for various types of radiation.

3.2.2 Beta particles

Beta particles (or beta rays) are high-energy, high-speed electron radiation mostly produced from beta decay (figure 3.2a). Since it consists of electrons, it carries an electric charge (e) and its energy varies from few KeV to MeV. Beta radiation can be found in space, nuclear and solar radiation, but it can be also generated from equipment used for imaging (like scanning electron and transmission microscopies). It has medium

penetrating power, and as figure 3.1b shows, few millimeters of plastic or aluminum are enough to block the beta rays.

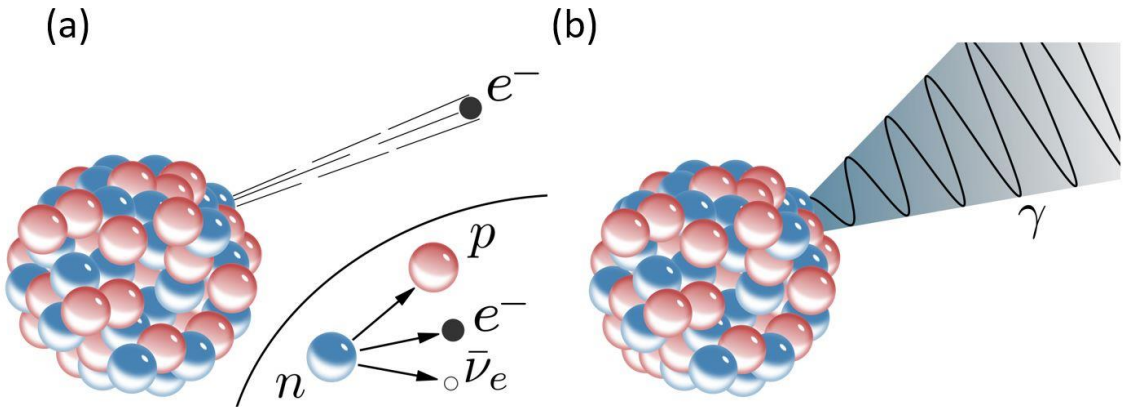

Figure 3.2. (a) Emission of beta particles from beta decay (b) Emission of gamma rays from a nucleus.

3.2.3 Gamma Rays

Gamma rays are high-energy photons (electromagnetic radiation) produced from radioactive decay of an atomic nucleus (figure 3.2b). As alpha and beta particles, they can be found in space (cosmic rays), radioactive decay and from terrestrial sources (lightning strikes). In addition, when charged particles like alpha, beta and ions interact with matter, they can produce significant amounts of gamma rays through bremsstrahlung radiation (deceleration radiation). They typically have frequencies higher than 10^{19} Hz (wavelengths lower than 10^{-11} meters), and energies ranging from 100 KeV to several MeV. In case of space radiation and more specifically high-energy gamma ray bursts, energies can be as high as TeV. Since photons are massless particles without any electric

charge, gamma rays can penetrate through large amounts of mass (figure 3.1b), making shielding extremely challenging.

3.2.4 Ion irradiation

Ion irradiation is more generic term used, since it involves irradiation from a wide variety of particles, including alpha, beta and gamma rays. Charged particles, such as HZE ions (high atomic number and energy), protons and neutrons, can interact with matter through a range of different mechanisms. In our study, we mostly focus on the ion radiation particles that are present in space radiation (protons and HZE ions) and the ones coming from tools used during semiconductor fabrication (ion implanters).

3.3 Sources of Ionizing Irradiation

3.3.1 Space Radiation

Space radiation involves a wide variety of particles and energies originating from multiple sources, as shown in figure 3.3 [72].

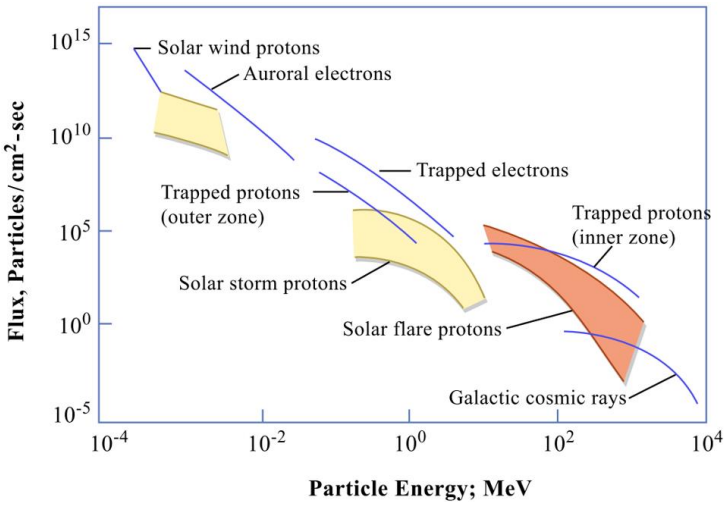

Figure 3.3. Flux and energy distribution of the various types of space radiation.

This causes electronic devices exposed to space irradiation undergo multiple effects and face multiple challenges at the same time. In this section, we are going to focus on the three principal sources of ionizing radiation (galactic cosmic rays, solar radiation and particles trapped in the geomagnetic field).

Galactic cosmic rays originate from sources outside our solar system (Milky way galaxy, supernova explosions) and involve particles with energies from MeV to TeV range. Cosmic rays are isotropic and mainly consist from protons (85%), alpha particles (14%) and HZE particles (1%) (figure 3.4a). Since cosmic radiation particles have very high kinetic energies (figure 3.4b), they can create to significant damage and reliability issues to electronic devices. More specifically, HZE atoms (such as magnesium, silicon and iron) are high penetrating ions with a charge higher than zero that travel with almost the speed of light.

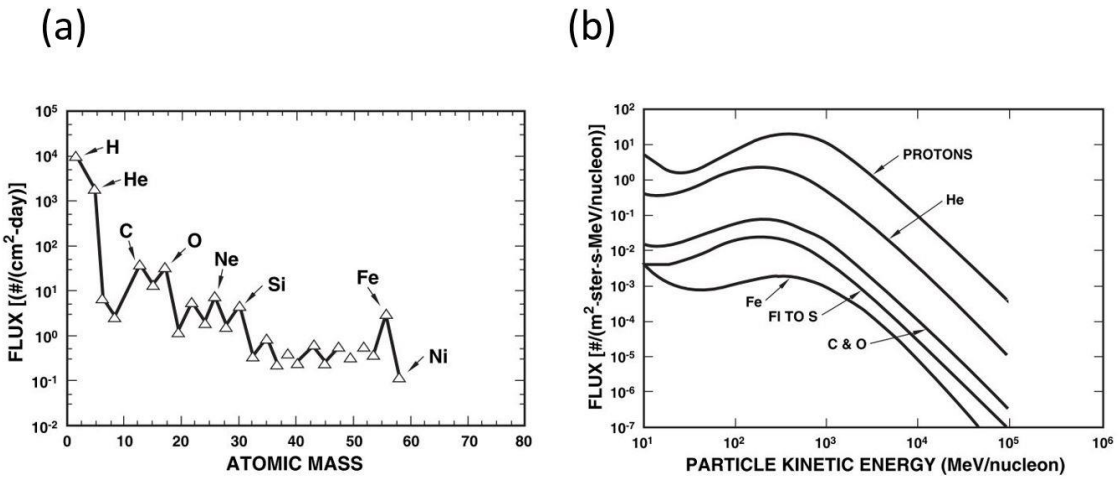

Figure 3.4. (a) Flux of GCR for various atomic masses (b) Energy spectrum of GCR.

Solar radiation is the second most important source of energetic particles in space. It mainly consists from protons and alpha particles (95%) and heavier atoms (5%) with

energies of several MeV. Our sun follows a 11-year cycle of activity with solar particle events and coronal mass ejections every few years (figure 3.5a). During that period, the total proton fluence can go as high as 10^{10} cm^{-2} with energies over 30 MeV. Solar radiation involves charged particles with relatively high mass, and along with GCRs, are responsible for most of the radiation damage in space. One important thing to note is that, when solar radiation is at its peak, cosmic ray flux is at its minimum (figure 3.5b).

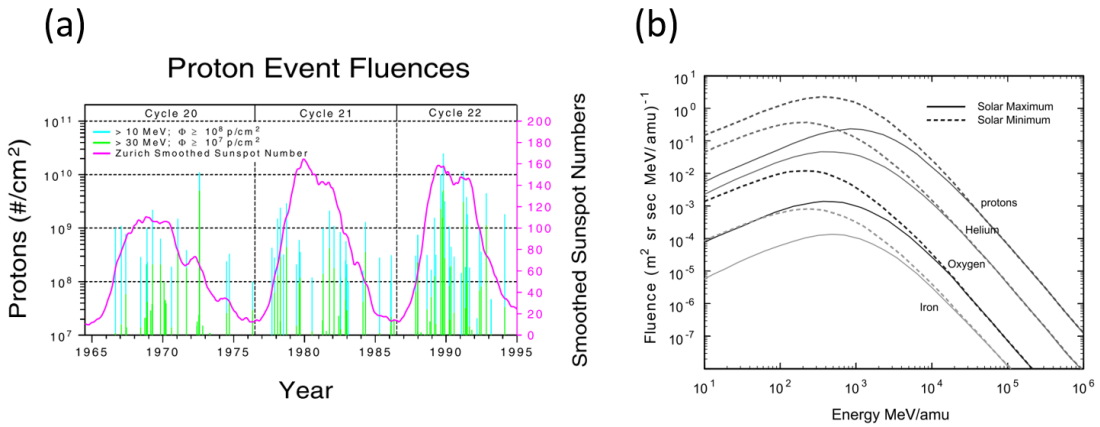

Figure 3.5. (a) Proton fluence based on different solar cycles (b) Solar cycle effect on GCR energy spectrum.

The third radiation source in space is the radiation coming from the trapped particles due to the magnetic field of the earth (figure 3.6a). The so-called Van Allen radiation belts, are zones near earth that charged particles, such as the ones from GCR and solar activity are trapped. The belts contain mostly protons and electrons, extending from an altitude of 1,000-60,000 km above the surface of the earth. The energies of the trapped particles vary with distance, as shown in figure 3.6b, and can pose a significant risk for the spacecraft or satellites when crossing through those regions.

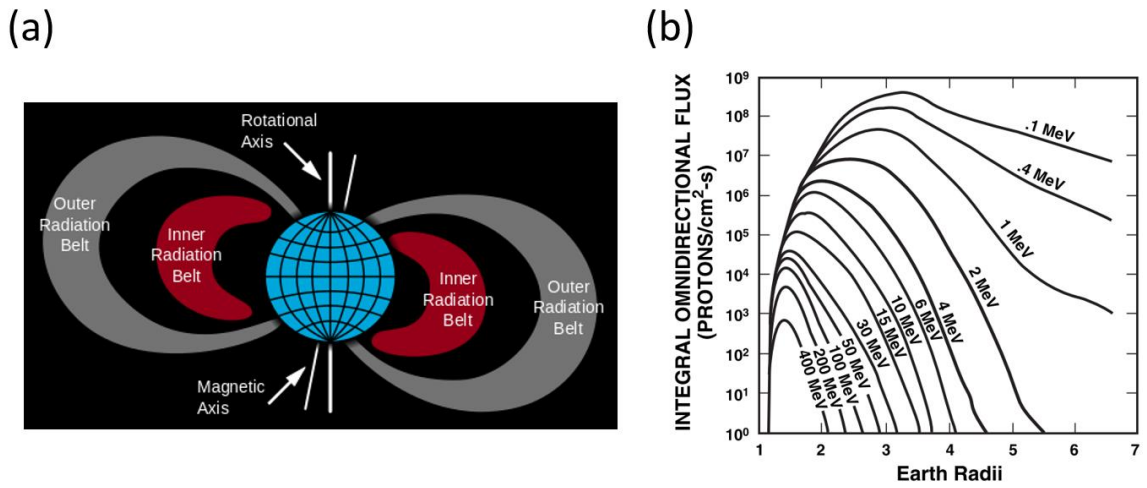

Figure 3.6. (a) Schematic illustration of the Van Allen radiation belts (b) Proton flux distribution as a function of distance and energy.

3.3.2 Secondary Radiation

When primary radiation particles with sufficient high energies interact with matter, they can create nuclear interactions with the atoms of the target material [72] (figure 3.7). As a consequence, secondary particles (in the form of X-rays, alpha particles, protons and neutrons, Bremsstrahlung radiation) are emitted and thus, increase the radiation damage of the devices. The two most important mechanisms are target and projectile fragmentation, where either GCR particles will collide with heavy nucleuses and create two or more secondary particles or HZE particles will collide with the atoms and create larger projectile fragments. The produced secondary particles can continue ionizing other atoms while decelerating, creating even more damage. Although it's hard to eliminate the effects of secondary radiation, recent studies [75] have found that using materials with high hydrogen content can decrease significantly its effects.

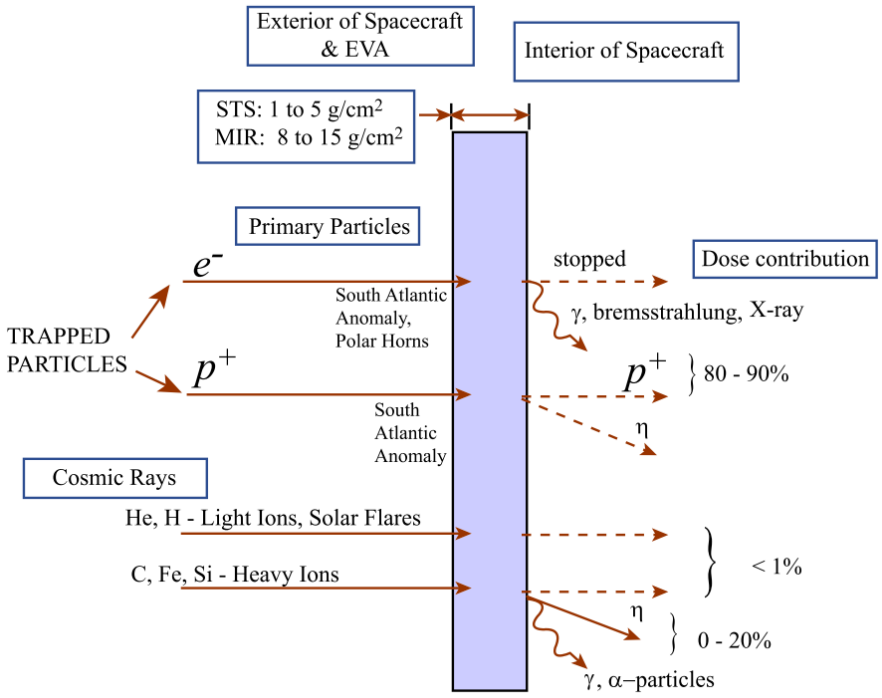

Figure 3.7. (a) Schematic illustration of the secondary radiation produced due to the interaction of primary radiation particles with matter.

3.3.3 Weapons of Mass Destruction (WMD)

WMD consists a broad category of weapons, including nuclear, radiological, chemical and biological ones, which cause significant harm to a large number of humans or human-made structures. For our study, we focus on the nuclear weapons since their use can cause significant damage due to radiation. More specifically, about 5% of energy released during a nuclear blast is in the form of radiation. Nuclear explosions involve the emission of high-energy neutrons and gamma radiation that originate from the energy producing fission and fusion reactions. The dose rates are delivered for very short time (10 ns to 10 μs) with fluences greater than 10^{10} n/cm^2 and energies up to 14 MeV.

3.3.4 Process Related Radiation

Process related radiation refers to the ionizing radiation that graphene based devices are exposed during the various fabrication steps. Processes such as, scanning electron microscopy (SEM), transmission electron microscopy (TEM) and e-beam lithography (EBL) can expose graphene to energetic electrons up to 200 KeV [13]. Furthermore, UV-ozone [76], reactive ion etching (RIE) [77] and deposition techniques such as plasma enhanced chemical vapor deposition (PECVD) or sputtering [78], can induced significant structural defects to graphene. This category of radiation involves energies significant lower than the aforementioned radiation sources (space, nuclear and secondary), nevertheless, it is the type that most research groups have been focusing when studying graphene.

3.4 Radiation Effects on Electronic Devices

3.4.1 Interaction with Matter

As we already discussed in the previous paragraphs, ionizing radiation interacts with matter and in the case of electronic devices, several unwanted effects take place [79,80]. To begin with, we have to define the units used in radiation dosimetry. The amount of energy loss per unit length of a particle passing through a material is called linear energy transfer (LET) and has units of MeV/cm (sometimes MeV per g/cm^2, energy per areal density). Furthermore, absorbed dose is measured in rad (absorbed energy of 100 ergs/g of material) or in gray (equivalent to 100 rad = 1 J/kg). The rate of energy loss, dE/dx for a particle passing through matter is expressed:

$$dE/dx = \frac{f(E)MZ^2}{E} \tag{3.1}$$

where x is the distance traveled in units of mass/area, f(E) is a function of particle energy E, M is the mass and Z is the charge of the ionizing particle. Thus, the greater the energy and mass of the ionizing particle, the greater the energy produced over a given length inside a material (more radiation damage).

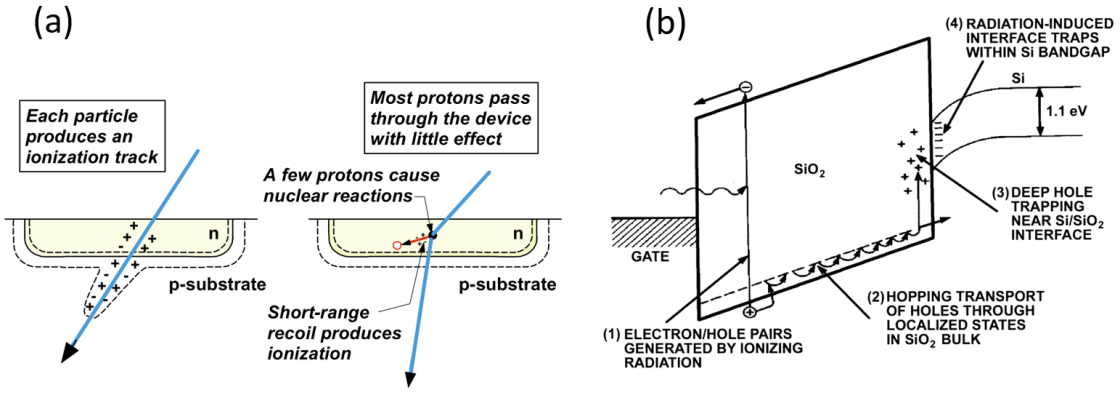

Figure 3.8. (a) Ionization path of radiation particles inside semiconducting materials (b) Effects of irradiation on the band diagram of a MOS transistor.

Ionization is the primary effect that semiconductor materials undergo when irradiated (figure 3.8a). Every particle will produce an ionization track, colliding with the atoms of the semiconductor and causing nuclear reactions. As shown in figure 3.8b, there are several effects that occur in the device. At first, electron from the valence band can get excited to the conduction band, as radiation can provide energy higher than the given bandgap. Free electrons and holes generated from radiation are free to move (diffuse and drift), until they recombine or get trapped. In addition, traps already existing in the oxide and at the Si/SiO_2 interface provide excellent sites for the low mobility holes generated

by irradiation. All this leads to charge buildup and significant threshold voltage shifts in MOS structures.

3.4.2 Single Event Effects (SEEs)

Single events are phenomena that occur from a single energetic particle. SEEs can be both destructive and nondestructive, depending on the particle energy, mass and interaction with the device. There are three main SEEs: single event upsets (soft errors), single event latchup (soft or hard error) and single event burnout (hard failure).

Single event upset (SEU) is a condition where a bi-stable element (memory) changes its value due to the impact of an energetic particle. A single particle can SEUs are transient soft errors and occur in both digital and analog electronic devices. SEUs are a result of the free charge created from the ionization and are nondestructive.

Single event latchups (SEL) on the other hand, are a type of short-circuit phenomena that occurs in irradiated integrated circuits. Due to the induced current state, devices can lose functionality making SELs potentially destructive. However, if power is quickly removed or current is limited, excessive damage may be avoided.

Finally, the most catastrophic events are single event burnouts (SEB). In this case, energetic particles can create high current states that to lead to permanent device failure. In case of formation of a conductive path through the gate oxide (dielectric breakdown), SEB is called single event gate rupture (SEGR).

3.4.3 Total Ionizing Dose (TID)

Total ionizing dose refers to the total absorbed dose (measured in rad or gray) over a period of time. TID mainly induces threshold voltage shifts (figure 3.9) on electronic devices, increases device leakage and power consumption, creates timing changes and limits device functionality. Different device structures (MOSFET, SOI, BJT) have different response on TID effects. Table 3.1 shows the radiation hardness characteristics of different transistor families.

Table 3.1: TID tolerance of various transistor families

TECHNOLOGY	TOTAL DOSE HARDNESS - Rads (Si)
BIPOLAR:	
TTL/STTL	1×10^6
ECL	1×10^7
IIL	1×10^6
Linear	1×10^4
MOS:	
NMOS	7×10^2
CMOS (Bulk)	3×10^3
CMOS/RH	1×10^7
CMOS-SOS	1×10^6

TID effects are usually dominated by protons and electrons, and devices that withstand higher TIDs are called radiation hardened. Shielding is necessary in order to protect microelectronic devices from the effects of TID.

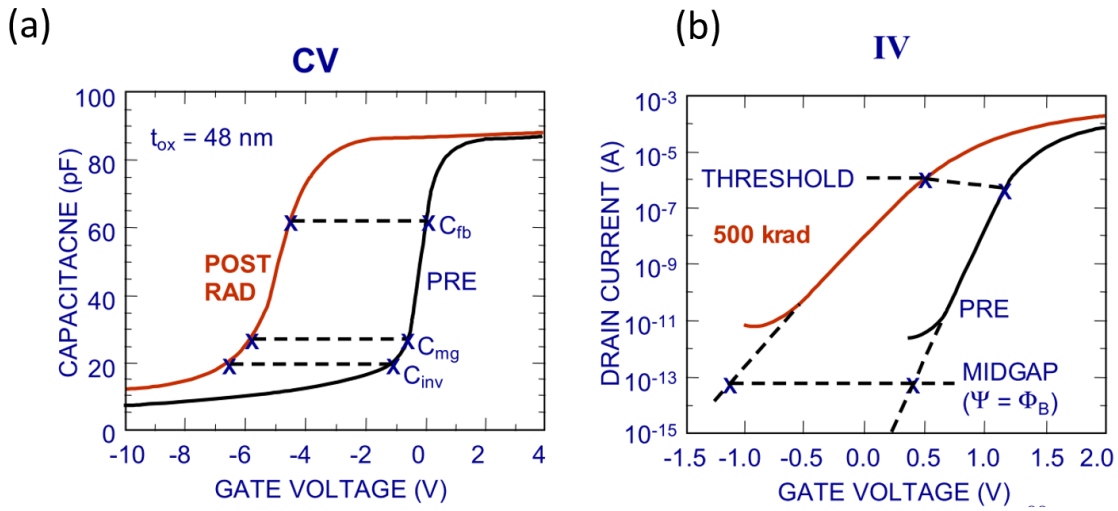

Figure 3.9. (a) CV change due to the TID effects (hole and interface traps) (b) Threshold voltage shift due to TID.

3.4.4 Displacement Damage

Displacement damage refers to the deformation of the crystal lattice due to impact from a high-energetic particle (Figure 3.10). Protons, neutrons and heavier atoms are mainly responsible for creating lattice defects on crystalline-based materials.

Devices that highly depend on the crystal structure of their materials (such as transistors, solar cells and optoelectronic devices) show displacement damage sensitivity. In some cases, the lattice damage can be severe enough to change the bandgap of the material. The amount of damage is dependent on the incident particle's energy, mass and type of target material and it has a cumulative effect (similar to TID).

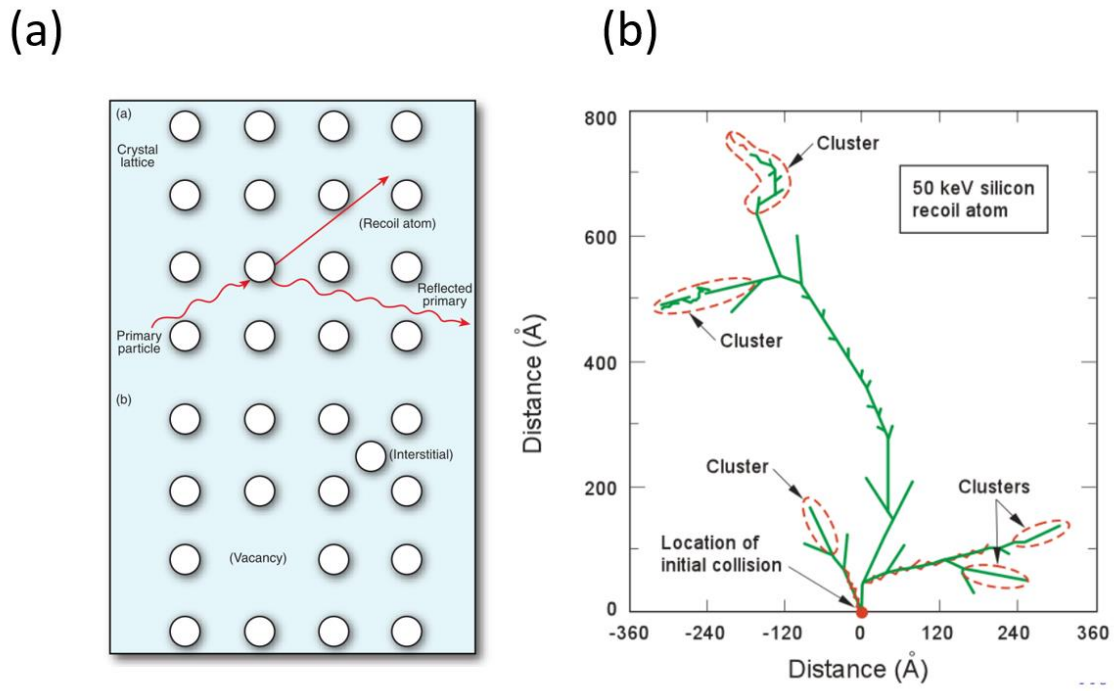

Figure 3.10. (a) Schematic illustration of the displacement damage in a crystal lattice (b) Damage clusters produced by the collision of particles.

3.5 Chapter Summary and Conclusions

Ionizing radiation in the form of energetic particles (protons, electrons, photons and ions) poses a significant challenge on the operation and reliability of modern electronics. The variety of radiation sources, including space radiation, nuclear, secondary and radiation during the fabrication process, makes the protection and shielding of the devices increasingly difficult. Our study focuses on effects such as displacement damage and total ionizing dose on GFETs. Graphene's atomic thickness gives it minimal interaction volume with radiation, but at the same time, its properties are directly related to its high crystalline quality (prone to displacement damage). Moreover, GFETs sensitivity to mobile/trapped charges makes it prone to TID effects. All these

phenomena are crucial for the non-encapsulated device structure, since there is no protection from radiation. Finally, our radiation-hardened structures (encapsulated and insulated gate) are evaluated and tested under the same exact conditions to highlight their advantages over the standard back-gate GFETs.

Chapter 4

Gamma Irradiation

4.1 Introduction

As discussed in the previous section, gamma rays (high-energy photons) interaction with matter has a detrimental impact on the performance and reliability of electronic devices. We expect gamma radiation to have a significant impact on GFET performance, as prior studies have shown that it can create electrically active defects in substrates and additionally increase the trap density between interfaces [76, 83, 15]. For instance, graphene can be used as a radiation sensor [84], in which the detection mechanism relies on the sensitivity of graphene's resistivity to local electric field changes caused by radiation induced ionized charges in the underlying substrate. Others have also identified gamma radiation effects and displacement damage mechanisms on graphene's lattice structure [85], while Raman spectroscopy studies have shown p-doped behavior of irradiated graphene [86]. In addition, encapsulated hBN graphene devices have been tested under X-Ray irradiation highlighting the effects of boron nitride as radiation shield [87]. This body of work demonstrates not only mechanisms of ionized charge build up in the substrate and displacement damage effects on GFET performance, but also that atmospheric adsorbents from the surrounding environment can have a significant impact on the radiation hardness of graphene.

For our gamma irradiation study we used a ^{60}Co source at the Chemistry Department of Brookhaven National Laboratory (figure 4.1). The dose rate was approximately 1 kGy/hr (due to the 5.26 year half-life of ^{60}Co, the dose rate decreased slightly over the course of these experiments). Field-effect mobilities (μ_{FE}) were extracted from measured I_d-V_{gs} characteristics and the Dirac point of each device was obtained in order to identify any possible effects of irradiation on overall performance and doping profile. All gamma exposures and electrical characterization was performed in ambient environment.

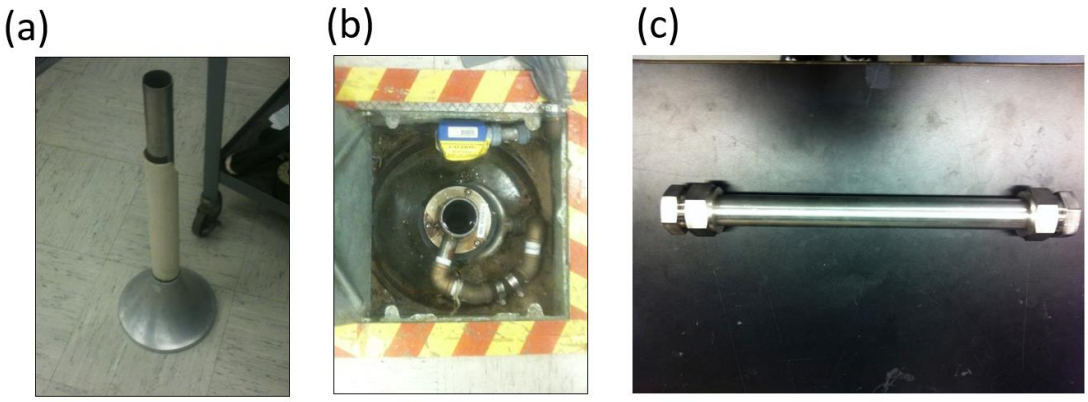

Figure 4.1. (a) Air filled tube sample holder (b) Actual ^{60}Co setup (c) Nitrogen filled tubes for isolating our samples from the effects of oxygen/water.

4.2 Electrical Characterization

Transfer curves of the non-encapsulated devices irradiated with various doses in an air-filled environment are shown in figure 4.2. After 2.2 kGy of gamma irradiation, the GFET exhibits a slight change in μ_{FE}, where the mobility of the as-fabricated device decreases by 13.7%. At the same time, the Dirac point shifts toward higher back-gate bias by 12 V, indicating increased p-doped behavior of the device. In addition, non-

encapsulated devices that were subjected to 26.4 kGy of irradiation as shown in the inset of figure 4.2, exhibit a larger decrease in μ_{FE} (30.53% decrease) and a higher ΔV_{Dirac} of 20 V compared to devices that were subjected to 2.2 kGy.

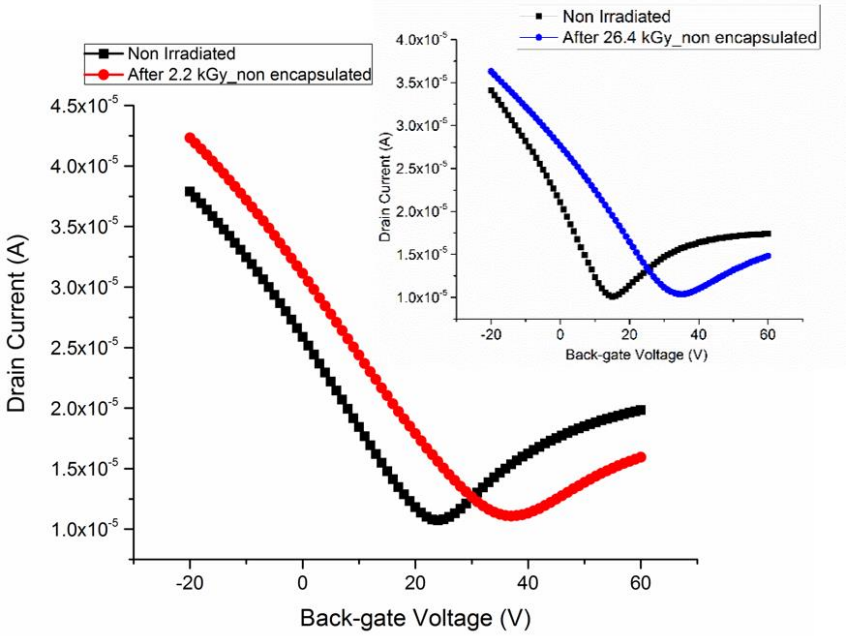

Figure 4.2. Transfer characteristics for non-encapsulated GFETs irradiated with 2.2 kGy (a) and 26.4 kGy (inset).

To further investigate the role of the ambient environment during irradiation, we performed exposures of non-encapsulated devices in a nitrogen environment to eliminate any oxygen/ozone contribution that we previously observed (figure 4.1c). Samples were sealed inside N_2-filled tubes and subsequently irradiated with 2.2 kGy and 26.4 kGy gamma rays under the same conditions as before. Results (figure 4.3) show a substantial improvement of the irradiated devices in a N_2 environment when compared to the air exposed devices. Specifically, GFETs shown in figure 4.3 exhibit a ΔV_{Dirac} of 2 V and a μ_{FE} decrease of 0.84% after 2.2 kGy of irradiation, whereas GFETs irradiated under the

same conditions in an air environment (figure 4.2) exhibit a ΔV_{Dirac} of 12 V and a μ_{FE} decrease of 13.7%. Similarly, devices exposed to 26.4 kGy of radiation had a ΔV_{Dirac} of 6 V and a μ_{FE} decrease of 5.61% in N_2 atmosphere (inset of figure 4.3) while a ΔV_{Dirac} of 20 V and a μ_{FE} decrease of 30.5% was observed in ambient air (inset of figure 4.2).

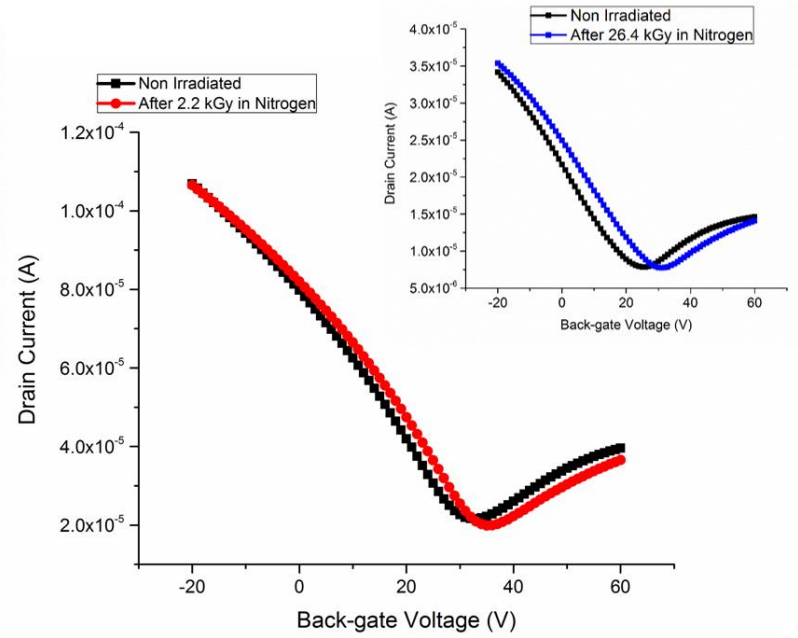

Figure 4.3. Transfer characteristics of GFETs irradiated with 2.2 kGy (b) and 26.4kGy (inset) in nitrogen filled environment.

4.2 Surface and Structural Analysis

4.2.1 Raman Spectroscopy

The Raman spectrum of the as-transferred CVD graphene on Si/SiO_2 is shown in figure 4.4a. The absence of a D-peak in the Raman spectrum shows the high crystalline quality of the CVD-graphene, and the I_{2D}/I_G intensity ratio of more than three clearly confirms the monolayer nature of the transferred layer. Figure 4.4b shows Raman spectra analysis of non-irradiated and irradiated devices subjected to 2.2 kGy and 26.4 kGy. Our

primary focus is the ratio of D band (~1350cm^{-1}) to G band (~1580-1600 cm^{-1}) (I_D/I_G), as it is a measure of the degree of disorder of single layer graphene (SLG) [88]. Non-irradiated graphene samples have I_D/I_G=0.03, whereas the samples irradiated with 2.2 kGy and 26.4 kGy of gamma rays have I_D/I_G=0.165 and I_D/I_G=0.182, respectively. This increase in I_D/I_G can be attributed to possible displacement damage on the graphene lattice that can lead to vacancies or local structural defects through the Compton effect as previous reports have found [89]. As the G band position is sensitive to chemical doping because of the strong electron – phonon interaction in graphene [90], any noticeable increase due to irradiation can provide valuable information concerning the doping profile of our samples. G-band exhibited a 4.93 cm^{-1} shift towards higher wave numbers after samples were exposed to 2.2 kGy of gamma radiation and a further 1.02 cm^{-1} shift when tested under 26.4 kGy, substantiating the increase in p-doping, in good agreement with the transport data.

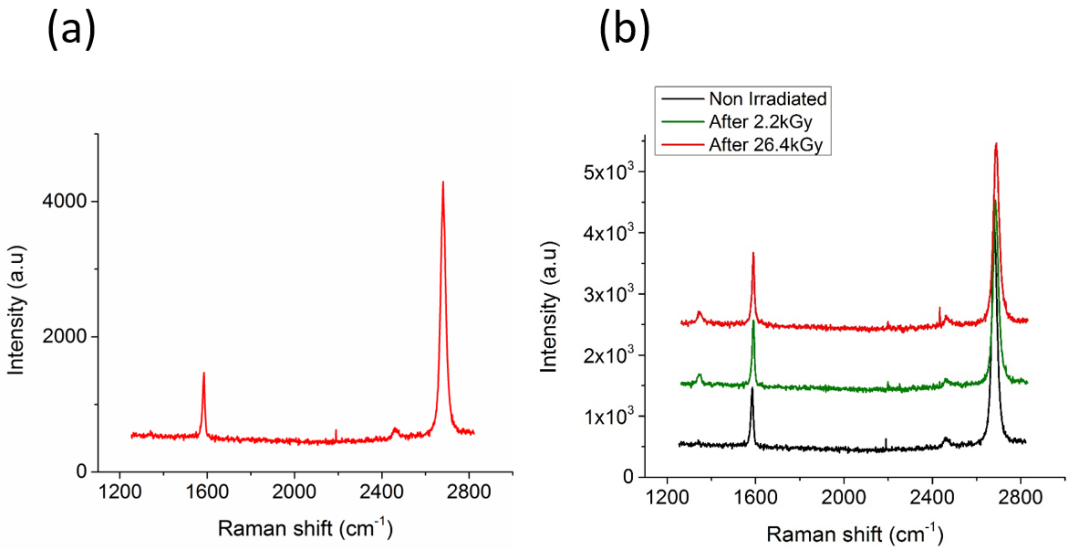

Figure 4.4. (a) Raman spectra of single-layer graphene (SLG) on a Si/SiO2 substrate (b) Raman spectrum of the irradiated devices.

4.2.2 X-ray Photoelectron Microscopy Analysis (XPS)

XPS is a surface analysis technique that illuminates the sample with X-rays in order to excite its electrons into vacuum. These electrons are then collected by a series of detectors, and based on their number and kinetic energies, valuable information for the compositional analysis of the sample is obtained. This is very useful in our study since we want to detect possible doping effects due to irradiation.

XPS spectra were collected using a Phi system with a standard Mg Kα source and spot size of ~100 microns. In figure 4.5, C1s XPS data from three different device configurations are presented and peaks were fit using a Gaussian-Lorentzian blend. The data are comprised of four peaks positioned at ~284.5 eV, ~285.2 eV, ~286.4 eV, and ~288.6 eV, corresponding to C-C, C-OH, C-O-C, and -COOH bonds, respectively. Table 4.1 shows the percent area that each peak makes up of the total C1s spectral area. UV-ozone exposed graphene suffers from high oxygen adsorption and doping [91], while others have shown that gamma radiation induces ozone formation in air [92]. For these reasons, a UV-ozone treated sample was included in our XPS measurements, to compare its oxygen content to that of the gamma irradiated sample. Both UV-ozone and 26.4 kGy gamma radiation treatment show similar trends. The main carbon peak decreases, while the C-OH, C-O-C and -COOH peaks increase in area. These results clearly indicate that gamma irradiation increases the adsorption of oxygen resulting in degraded electronic performance. A passivation layer is therefore crucial to isolate graphene from oxygen if these devices need to operate in a radiation sensitive environment.

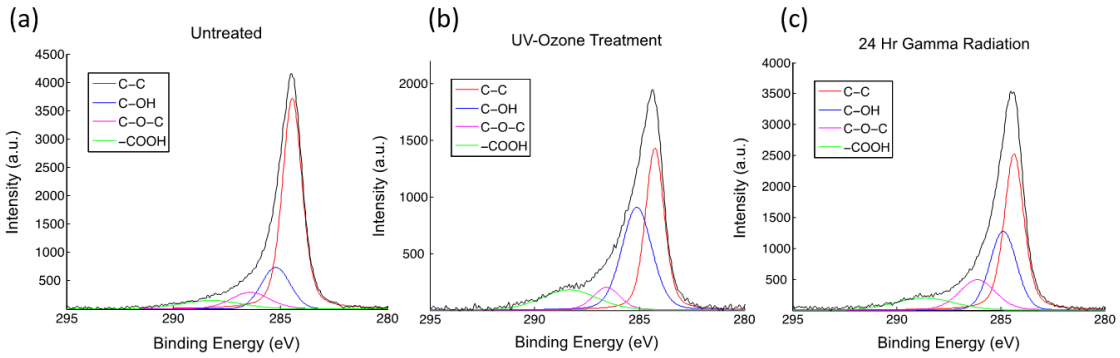

Figure 4.5. Carbon 1s XPS data from three different device configurations: non-irradiated (a), UV-ozone treated samples (b) and after 26.4 kGy gamma rays (c).

Table 4.1| XPS C1s bond area after gamma irradiation

	No Irradiation Bond Area %	**UV-Ozone Bond Area %**	**26.4 kGy Bond Area %**
C-C	66.4	40.0	46.8
C-OH	16.4	38.4	27.7
C-O-C	9.7	7.6	15.3
-COOH	7.5	14.0	10.2

4.3 Encapsulated/Insulated Gate Device Performance

Based on the results from our XPS and N_2 measurements, we employed our encapsulated GFETs in order to shield graphene from the surrounding environment while being irradiated. Encapsulated GFETs have already enabled our devices to operate for several weeks in ambient environment with minimal performance degradation [93]. Encapsulated GFETs were subjected to the same irradiation conditions as before, and as

figures 4.6a,b show, they perform significantly better when compared to the non-encapsulated devices. Specifically, non-encapsulated devices demonstrate a ΔV_{Dirac} up to 43 V when irradiated with 184.8 kGy, while the V_{Dirac} of encapsulated devices shifts only 14 V. In addition, μ_{FE} of the non-encapsulated GFETs was severely affected with a decrease up to 33.2% when the encapsulated devices only lost 5.7% compared to the as-fabricated μ_{FE} values. These results clearly highlight the effectiveness of the encapsulation layer as a barrier to reactive oxygen and ozone.

Besides displacement damage and ambient environment contributions, radiation-induced defects in the substrate and substrate/oxide interface can have a significant effect on device performance. Carrier lifetimes, mobilities and carrier densities can be negatively affected as energy deposited by radiation creates electrically active defects in the substrate [94]. These radiation mechanisms may further affect our non-encapsulated and encapsulated devices since they both use silicon as a back-gate electrode. For this reason, we developed and tested our insulated gate structure in which the buried Al layer was used as a back-gate electrode.

Figures 4.6a shows that irradiation can cause a ΔV_{Dirac} of up to 5 V to the insulated gate devices, a substantial improvement over the encapsulated devices tested before (which exhibited a ΔV_{Dirac} of up to 14 V under the same irradiation conditions). In addition, the μ_{FE} of the insulated gate devices as shown in Figure 4.6b, decreased by only 2% after irradiation, whereas encapsulated devices suffered from a 6% decrease in μ_{FE}.

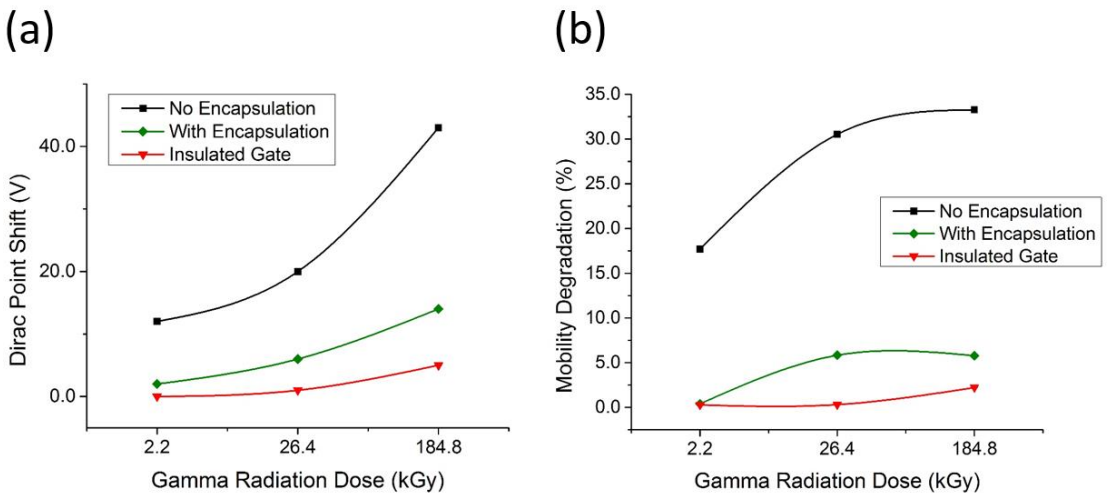

Figure 4.6. V_{Dirac} shift and (a) mobility degradation (b) data for the three different device structures.

Table 4.2 shows all the results of mobility degradation and Dirac point shift for all device configurations. It is clear that non-encapsulated devices suffer from severe performance hit, while encapsulated and insulated gate devices offer improved radiation hardness when exposed to the same radiation doses.

Table 4.2 | Effects of gamma irradiation on different device structures

	Non-Encapsulated		Encapsulated		Insulated gate	
	ΔV_{Dirac} (V)	**μ_{FE} decrease (%)**	**ΔV_{Dirac}**	**μ_{FE} decrease (%)**	**ΔV_{Dirac}**	**μ_{FE} decrease (%)**
2.2kGy	12	13.7	2	0.4	0	0.2
26.4kGy	20	30.5	6	5.8	1	0.3
184kGy	43	33.2	14	5.7	5	2.2

4.4 Chapter Summary and Conclusions

Gamma radiation poses a significant challenge to the performance and reliability of next generation graphene-based devices. In this chapter, we studied the effects of gamma radiation on GFETs and developed a novel method to shield them. The ambient environment, radiation induced defects to the substrate, and displacement damage are three main factors contributing to GFET performance degradation. We demonstrate that both encapsulation and an insulated gate are needed to effectively produce gamma radiation-hard GFETs. Our proposed encapsulation and gate insulation structures successfully mitigate detrimental radiation effects and it remains to be seen in the subsequent chapters, if those devices remain radiation hardened under electron beam and ion irradiation.

Chapter 5

Beta Irradiation

5.1 Introduction

Beta irradiation in the form of e-beam is the second category of radiation tests for our fabricated GFETs. Previous studies have been mostly exploring e-beam energies covering the 20-200 KeV range, which mainly comes from electron-based microscopy/lithography that graphene devices are exposed to during fabrication.

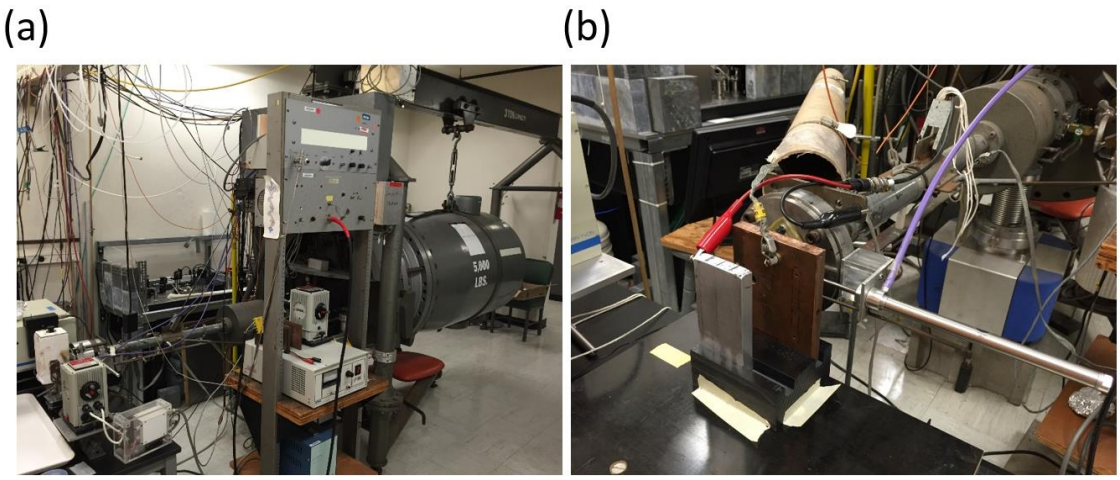

Figure 5.1. (a), (b) BNL's Van de Graaff used for the radiation of our devices. All e-beam tests conducted in ambient environment.

Specifically, electron-beam radiation has shown to induce a strong Raman D-peak (indicating potential displacement damage to graphene's crystal lattice), as well as, resistivity increase in CVD grown graphene [95]. Furthermore, similar studies have found that the Dirac point shifts to lower gate values as a consequence of the trapped

holes at the SiO_2/Si interface [13].In this chapter, we report the effects of high-energy electron-beam irradiation with doses ranging from 5.1*10^14 e/cm^2 to 4.72*10^15 e/cm^2. All e-beam irradiation took place at the Chemistry Department of Brookhaven National Laboratories (BNL) using a 1.5 MeV Van de Graaff in ambient atmosphere, as shown in figure 5.1.

5.2 Electron Beam Simulation

In the case of e-beam irradiation, we first start our analysis with Monte Carlo simulations of electron trajectory in our devices. That will give us a good estimation of the penetration depth and damage that high-energy electrons (1.5 MeV) will induce. The software package used is CASINO, a program developed from a team of researchers from University of Sherbrooke [96]. With the help of CASINO, we were able to create the exact device structures (non-encapsulated, encapsulated and insulated gate GFETs) that we tested later on at Brookhaven National Laboratories.

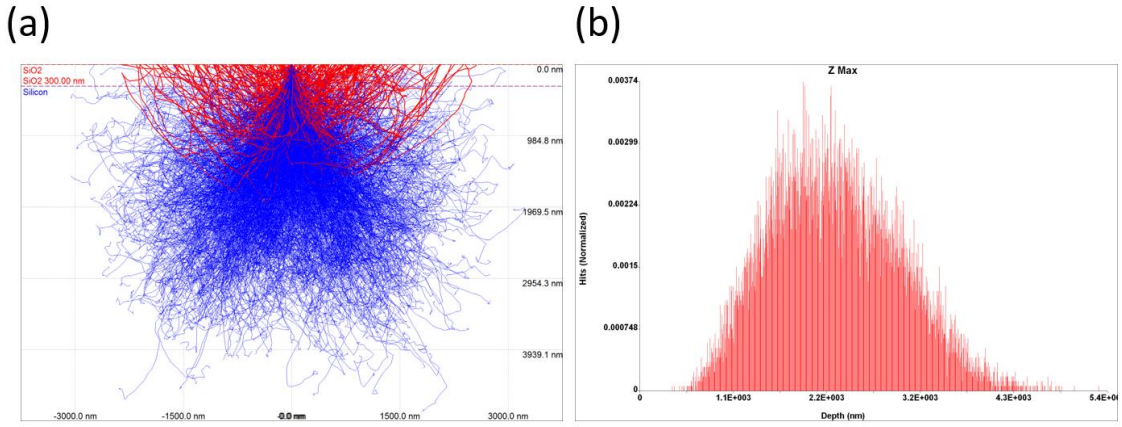

Figure 5.2. (a) Electron trajectory simulation for the non-encapsulated devices hit by a 20 KeV e-beam (b) Distribution of maximum depth of electrons.

Figure 5.2 shows the simulation of a 20 KeV e-beam hitting our non-encapsulated device structure. Interestingly, and although we used only 20 KeV e-beam (our BNL tests involve 1.5 MeV), electrons will penetrate the SiO_2 (300 nm) and proceed inside the silicon substrate for almost 4 μm. This means that radiation damage will take place in both the oxide and substrate (local back-gate) even at low energies. Running the same simulation (20 KeV) using the insulated gate GFET structure (figure 5.3a, b) resulted in similar behavior (regardless the extra layers of Parylene-C and Al on top).

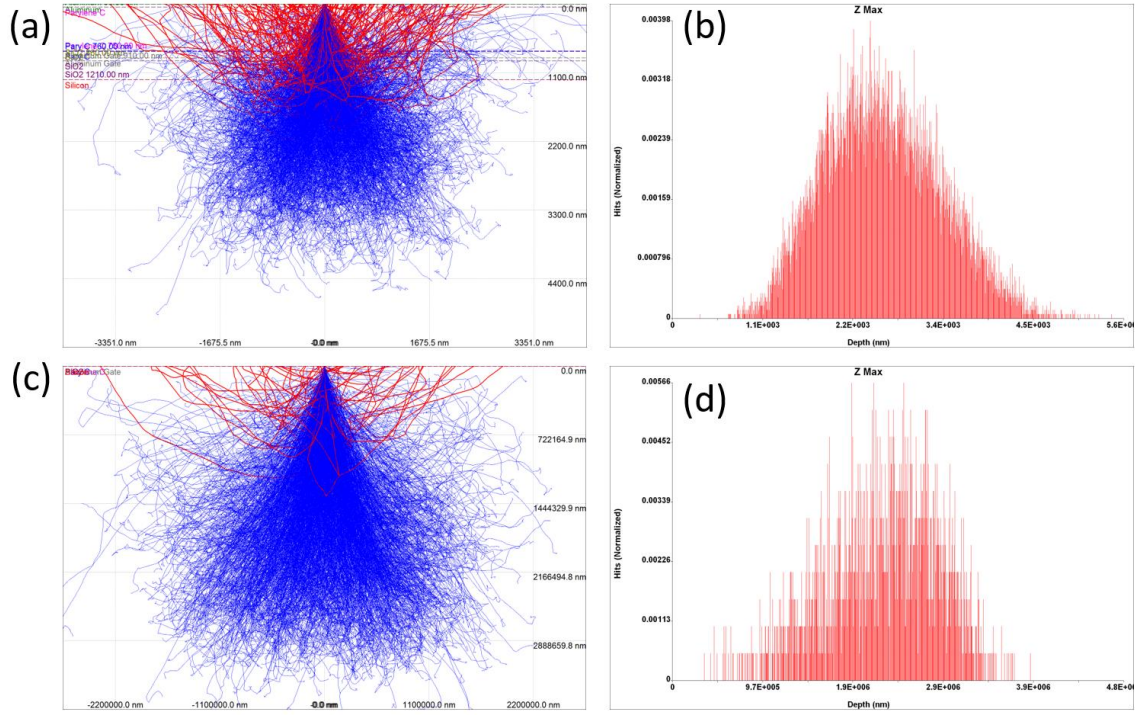

Figure 5.3. Electron trajectory simulation for the insulated gate devices hit by a 20 KeV (a) and 1.5 MeV (c). Distribution of maximum depth of electrons for 20 KeV (b) and 1.5 MeV (d).

Finally, 1.5 MeV e-beam simulations were conducted on the insulated gate GFET. As shown in figure 5.3c, the range of electrons extends to almost 3 mm. This means that

electrons will pass through our entire sample (total sample thickness ~ 500 μm) creating damage to all layers.

5.3 Electrical Characterization

For the electrical characterization of the irradiated GFETs, we used the same setup and process like the one for gamma radiation. All device structures were electrically characterized before and after beta irradiation using a Keithley 4200 Parameter Analyzer and a 3-probe setup.

Figure 5.4a shows the Dirac point shift of all the device structures after being irradiated with doses ranging from 5.1*10^14 e/cm^2 to 4.72*10^15 e/cm^2. As in the gamma radiation case, a positive Dirac point shift was observed for the non-encapsulated devices, in contrast to previous studies, where a negative shift was measured [13]. We believe this deference is due to the fact that our beta radiation exposure happened in ambient environment, and not under high vacuum, as is the case in other studies. The positive shift can be attributed to the increase adsorption of ozone produced from the e-beam [101], similar to our gamma radiation study, resulting in a heavily p-doped surface. Furthermore, our encapsulated and insulated gate device structures experience a negative shift of their Dirac point, since the effect of the ambient environment was eliminated this time, due to the protection from the passivation layer. The negative shift originates from the interaction of the electron beam with the substrate (Si/SiO_2). More specifically, e-beam will generate electron-hole pairs, where the less mobile holes are trapped between the interfaces, creating a positive bias that attracts electron in graphene (n-doped) [97].

Figure 5.4b shows the mobility degradation results for the irradiated devices. The non-encapsulated device structure suffers from a significant μ_{FE} decrease (up to 59% compared to the as-fabricated value). In contrast, both encapsulated and insulated gate devices exhibit a much smaller decrease (up to %16 and %7 respectively). In accordance to the gamma radiation results, the insulated gate device structure offers the best post irradiation behavior with significantly better performance characteristics than the other two structures.

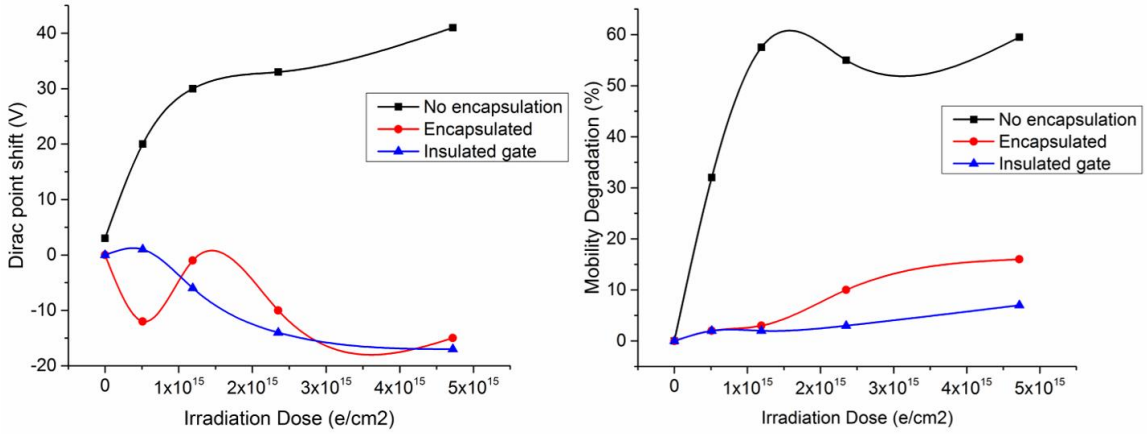

Figure 5.4. V_{Dirac} shift and (a) mobility degradation (b) data for the three different device structures after exposed to beta radiation.

Table 5.1 shows collectively all the results of mobility degradation and Dirac point shift for all device configurations.

Table 5.1 | Effects of beta irradiation on different device structures

	Non-Encapsulated		Encapsulated		Insulated gate	
(e/cm^2)	**ΔV_{Dirac} (V)**	**μ_{FE} decrease (%)**	**ΔV_{Dirac}**	**μ_{FE} decrease (%)**	**ΔV_{Dirac}**	**μ_{FE} decrease (%)**
No e-beam	3	0	0	0	0	0

5.1 x 10^{14}	20	32	-12	2	1	2
1.19 x 10^{15}	30	57.5	-1	3	-6	2
2.35 x 10^{15}	33	55	-10	10	-14	3
4.72 x 10^{15}	41	59.5	-15	16	-17	7

5.4 Surface and Structural Analysis

5.4.1 Raman Spectroscopy

Raman spectrum measurements were conducted on non-encapsulated GFETs in order to evaluate the crystal lattice damage after e-beam irradiation. We expect substantial displacement damage to our devices, in contrast to our gamma radiation study, where we saw a marginal increase in the I_D/I_G ratio. Our results show that there is significant damage to the crystal lattice of graphene, in accordance to what prior studies have found [13,89]. Figure 5.5a shows the effects of 4.72*10^15 e/cm^2 on the Raman spectrum of graphene. There is a big increase of the D peak (defects peak) intensity, the peak that is associated with the crystalline quality of graphene. The high I_D/I_G (~0.97) ratio, indicates that crystalline graphene transforms into nanocrystalline one, following the amorphization trajectory proposed by Ferrari and Robertson [98]. Figure 5.5b shows the collective results of the I_D/I_G ratio as a function of radiation dose. There is a rapid increase of the I_D/I_G (from 0.1 to 0.65) after graphene is exposed to a dose of 5.1*10^14 e/cm^2, saturating to a value of almost 1 for higher doses.

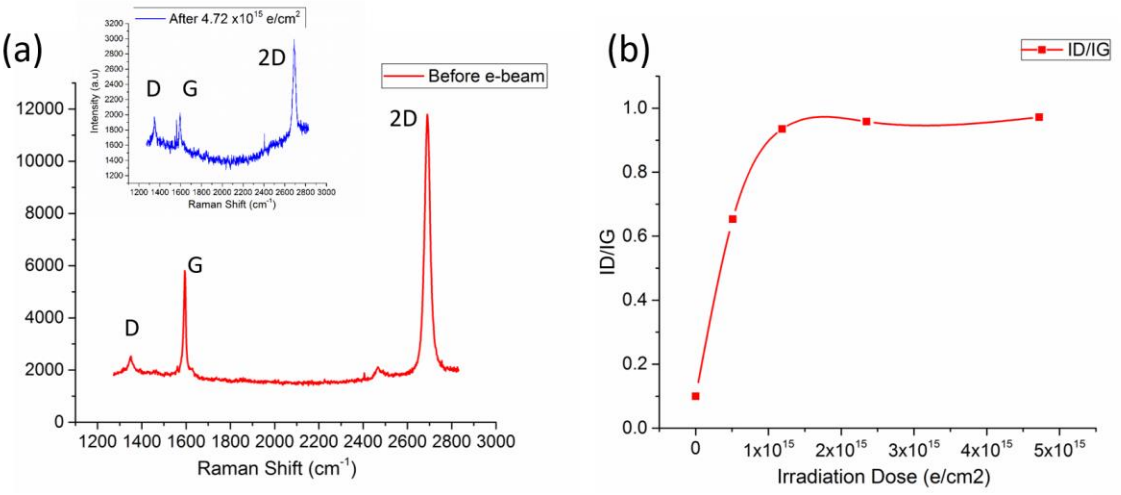

Figure 5.5. (a) Raman spectrum of non-encapsulated device before and after 4.72*10^15 e/cm^2 (inset) (b) I_D/I_G ratio as a function of beta radiation dose.

This is an important result, since it differentiates the e-beam irradiation effects from our previous gamma study. We saw that the primary degradation mechanisms when graphene is exposed to gamma rays are the contribution of environment (reactive oxygen and ozone) and the substrate damage. In addition to those two mechanisms, e-beam irradiated samples suffer from significant displacement damage, that needs to be accounted for, when developing radiation hard GFETs.

5.4.2 X-ray Photoelectron Microscopy Analysis (XPS)

In the same way to our gamma radiation study, we measured the XPS spectrum using a Phi system with a standard Mg Kα source and spot size of ~100 microns. In figure 5.6, C1s XPS data from two different device configurations are presented and peaks were fit using a Gaussian-Lorentzian blend. The data are comprised of four peaks positioned at ~284.5 eV, ~285.2 eV, ~286.4 eV, and ~288.6 eV, corresponding to C-C, C-OH, C-O-C, and -COOH bonds, respectively. Table 5.2 shows the percent area that each peak makes up of the total C1s spectral area. After irradiation the main carbon peak

decreases, while the C-OH, C-O-C and -COOH peaks increase in area, due to the interaction of e-beam with ambient atmosphere. This results to degraded electronic device performance, in the same way to what gamma radiation samples exhibited.

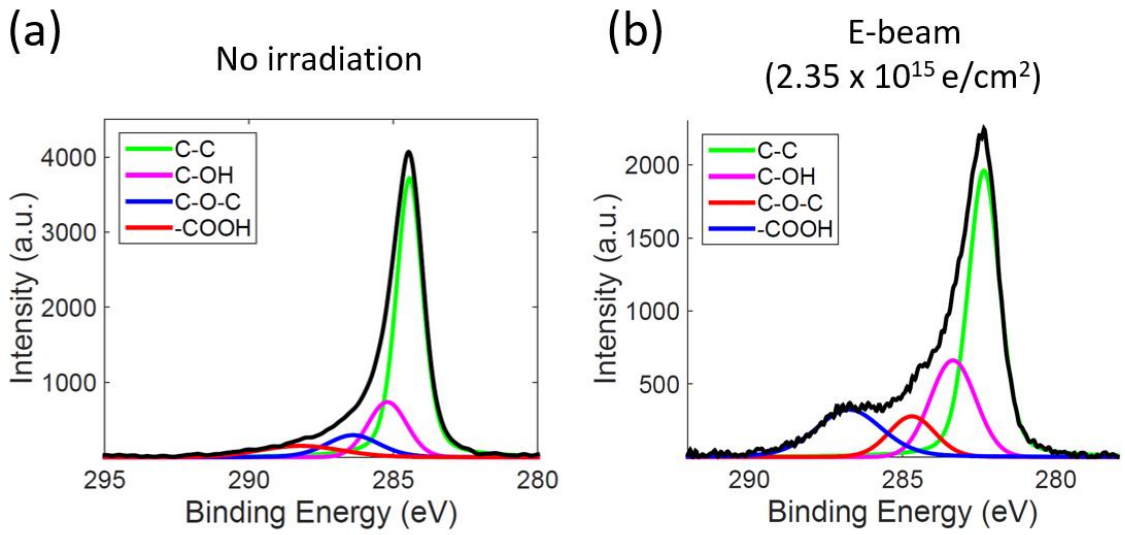

Figure 5.6. Carbon 1s XPS data from two different device configurations: non-irradiated (a), after 2.35 x 10^{15} e/cm^2 beta radiation (b).

Table 5.2 | XPS C1s bond area after beta irradiation

	No Irradiation **Bond Area %**	**E-beam** **(2.35 x 10^{15} e/cm^2)** **Bond Area %**
C-C	66.5	52.9
C-OH	16.4	20.8
C-O-C	9.7	9.4
-COOH	7.5	16.9

5.4.3 Transmission Electron Microscopy Analysis (TEM)

Based on our Raman spectroscopy study, we concluded that displacement damage (DD) is a key degradation mechanism on e-beam irradiated samples. Unfortunately, neither Raman nor XPS are techniques that would allow us to image the exact crystal lattice damage. Transmission electron microscopy on the other hand, has the ability to image samples with sub-nanometer resolution, making ideal for the displacement damage study. Our TEM measurements were conducted using the FEI Talos F200X (S/TEM) microscope, under both 80 KeV and 200 KeV.

Prior studies on carbon nanomaterials, such as carbon nanotubes and graphene, have found that the threshold acceleration voltage for knock-on damage is in the order of 80-90 KeV [99,100]. This means that, at energies of 1.5 MeV, we are above that threshold, fact that explains the increase in defects peak intensity from our Raman analysis. Unfortunately, irradiating at 1.5 MeV cannot happen inside the TEM microscope, since our samples were irradiated at BNL facilities. This limits our imaging capabilities and energies to the available modes of our TEM setup, which are 80 KeV and 200 KeV.

For our imaging we used single layer graphene transferred on ultra-fine 2000 mesh copper TEM grids. Graphene is suspended on 6.5 μm grid holes with a pitch of 12.5 μm (figure 5.7).

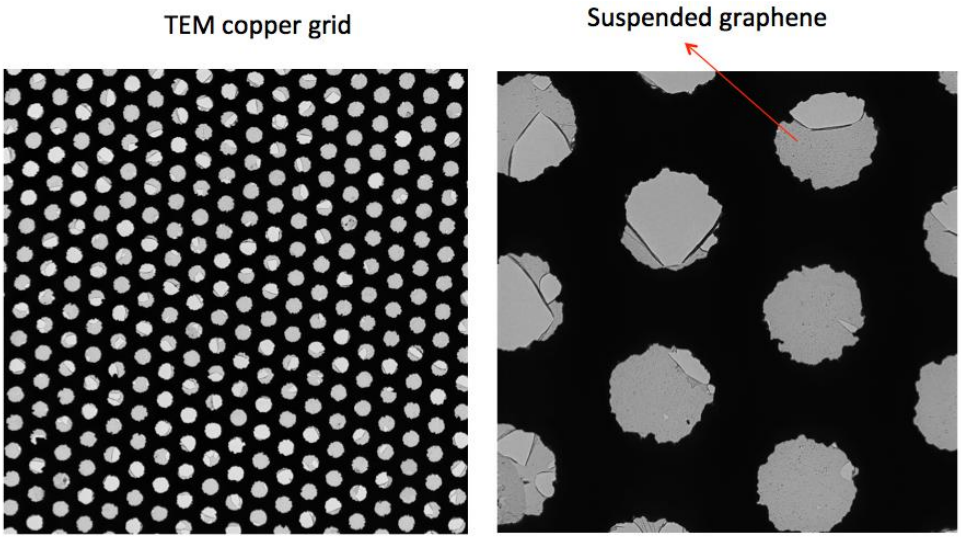

Figure 5.7. Suspended graphene on 2000 mesh TEM copper grid

We first tested our TEM grids under 80 KeV. Although this energy is close to the threshold knock-on damage, hole formation to the crystal lattice can be initiated at energies as low as 20 KeV [100] when graphene contains defects or adsorbents (water, oxygen). Figure 5.8 shows the effects on the crystal lattice after graphene was exposed to 80 KeV for 10-60 seconds. After 10 seconds, graphene is already subject to structural changes, as the edges of the film start to shrink and curl. Continuing the irradiation for more seconds increases the deformation of graphene as shown in figure 5.8d.

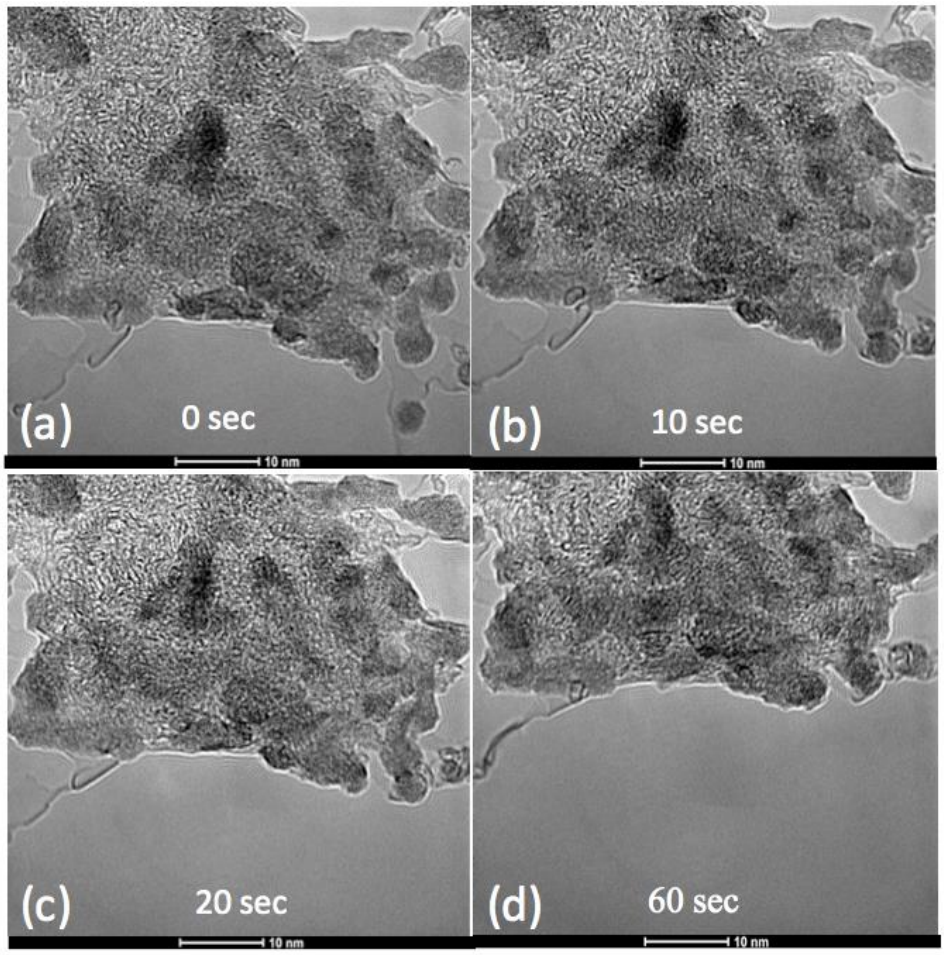

Figure 5.8. (a) TEM imaging before irradiation, at 80 KeV (b) after 10 seconds, (c) after 20 seconds and (d) after 1 minute of irradiation.

We continue our TEM analysis with the TEM set at 200 KeV. Since this is twice the threshold knock-on energy needed, we expect to have significantly more crystal lattice damage than 80 KeV. Our claim is verified from the results shown in figure 5.9. Ten seconds of irradiation are enough to create significant lattice damage, as seen in figure 5.9b, with graphene edges shrinking considerably. After 60 sec, the lattice deformation is much bigger than the one we observed with the 80 KeV sample.

In conclusion, the TEM gave us a unique opportunity to image the lattice damage that we first observed with Raman spectroscopy. The displacement damage in both energies (80 KeV and 200 KeV) is significant (scales with the incident e-beam energy), and must be taken into account, for devices operating under beta radiation.

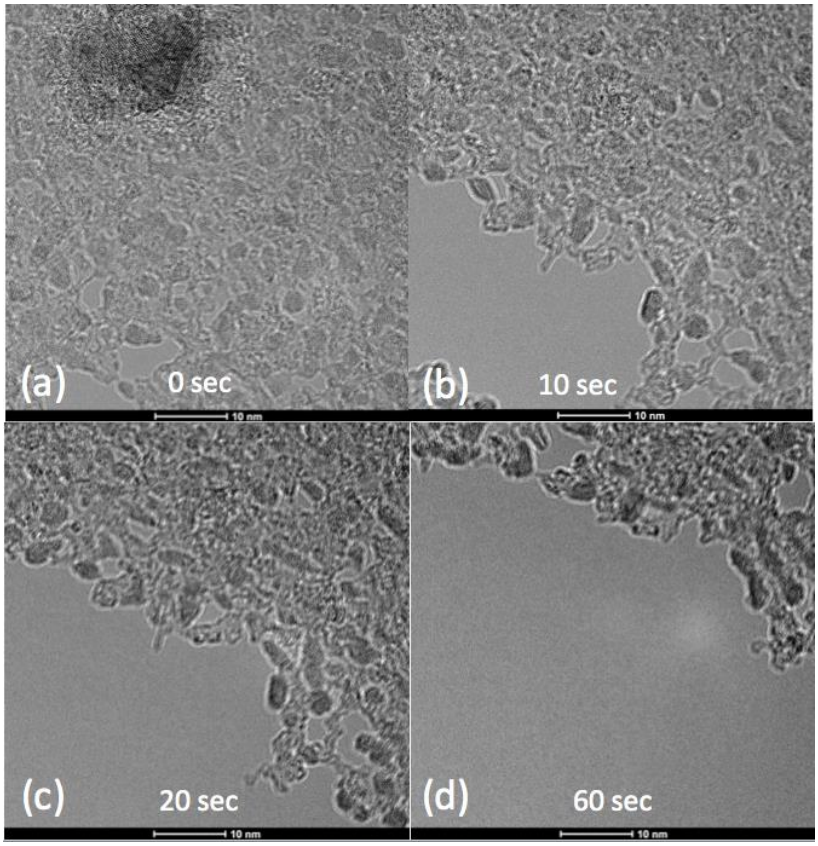

Figure 5.9. (a) TEM imaging before irradiation, at 200 KeV (b) after 10 seconds, (c) after 20 seconds and (d) after 1 minute of irradiation.

5.5 Chapter Summary and Conclusions

In this chapter, GFETs were subjected to various doses of beta irradiation in order to examine the effects on the device and material level. All three previous devices structures were tested (non-encapsulated, encapsulated and insulated gate), with the insulted gate GFETs showing drastically better radiation tolerance than the other two

structures. Raman spectroscopy conducted on the non-encapsulated devices showed severe lattice damage (increased D peak intensity), and XPS measurements resulted on a graphene surface with significantly higher oxygen content than the untreated sample. Finally, by employing TEM imaging, we were able to visualize the lattice deformation due to irradiation. Although the gamma radiation damage was primarily attributed to the environmental contribution and substrate effects, a third and equally important degradation mechanism (displacement damage) is present in the case of beta irradiation.

Chapter 6

Ion Irradiation

6.1 Introduction

Ion irradiation refers to a broad category of energetic particles with kinetic energies high enough to cause ionization. Previous studies have shown that, ions such as Ar^+, C+ and He can cause defects and increased impurity scattering on irradiated graphene samples [102-104]. Most of these studies though, have looked into the impact of ions with energies ranging from 30-500 KeV. Our work, as in the case of beta and gamma radiation, is focused on exploring the effects of ions with kinetic energies as high as 1.5 MeV.

For our study we used three different ion irradiation sources, hydrogen (H), helium (He) and iron (Fe). We specifically chose these particles categories since we wanted to test our devices in an environment that resembles the one found in space. As we discussed in the third chapter, galactic cosmic rays (GCR) and solar radiation mainly consist of protons (H), alpha particles (He) and HZE atoms (such as Fe) with energies in the MeV-GeV range.

All ion irradiation experiments were conducted at University of Albany (Ion Beam Laboratory) using their Dynamitron particle accelerator (1.5 MeV H, He ions) and Extrion ion implanter (300 KeV Fe ions) systems as shown in figure 6.1. This time though, only non-encapsulated devices structures were tested, since all ion exposures

tests were conducted under vacuum (10^{-4} Torr) (encapsulation effect is not relevant) and our primary focus was on the displacement damage mechanism caused by the energetic ions.

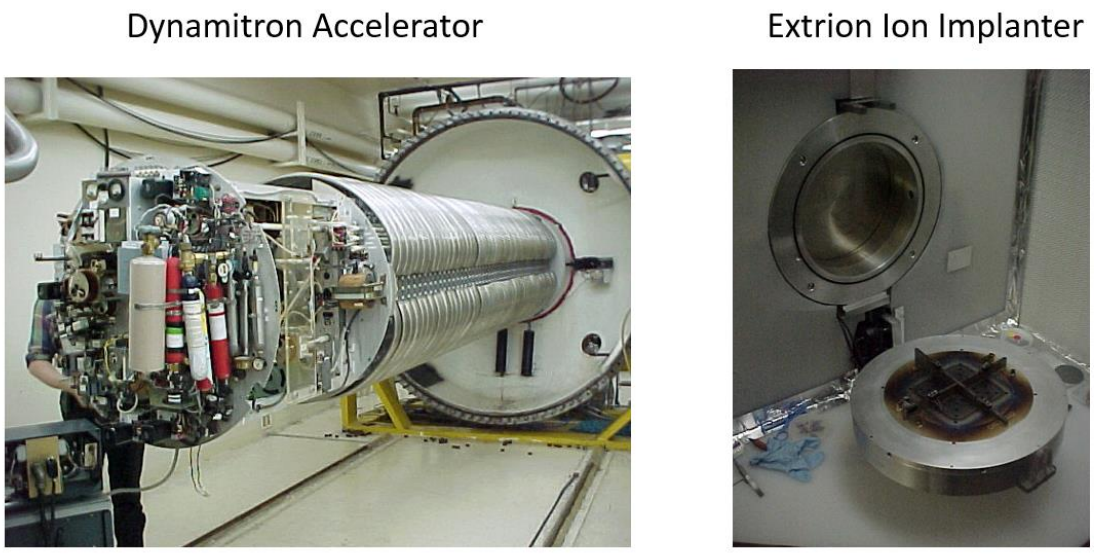

Figure 6.1. (a) The Dynamitron accelerator used for our 1.5 MeV H, He irradiation (b) The Extrion ion implanter used for the 300 KeV Fe ions.

6.2 Ion Radiation Simulation

In order to evaluate the range and damage of ions on our samples, we conducted simulations with SRIM (The Stopping and Range of Ions in Matter). SRIM is a software package that can calculate many features of the transport of ions in matter. Following the same procedure to our beta radiation simulations, we were able to construct the exact GFET structures (both non-encapsulated and insulated gate GFETs) simulating the effect of H, He and Fe radiation. Figure 6.2 shows the results of 1.5 MeV proton and alpha particle radiation to the non-encapsulated GFET device. We are mostly interested in the range of the particles, and the vacancies produced/ion/unit thickness (damage created).

The creation of target vacancies results from both ion/target atom collisions, and also from the collision cascades of recoiling target atoms.

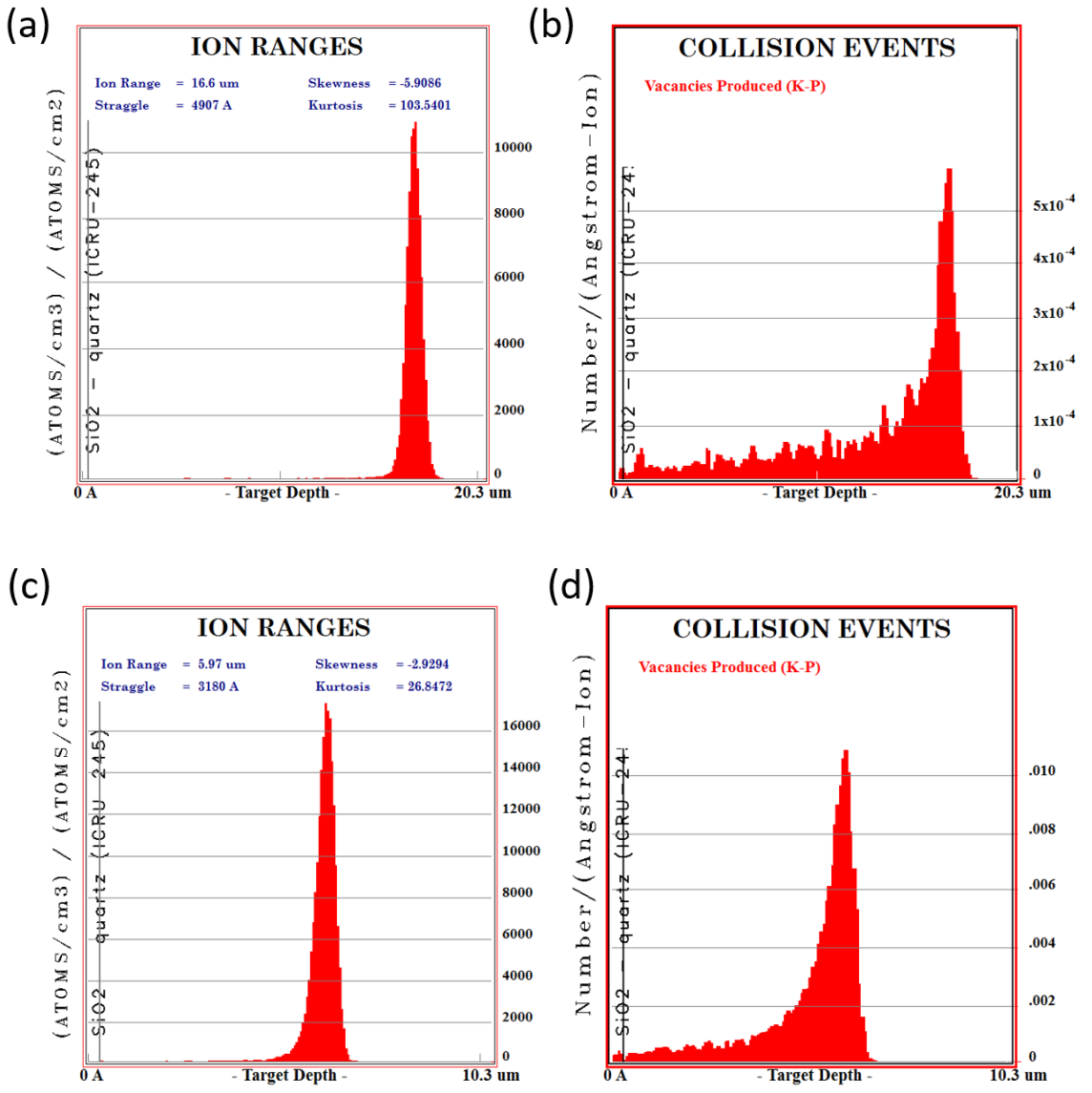

Figure 6.2. Non-encapsulated device: Ion range after 1.5 MeV proton (a) and alpha particle (c) irradiation. Vacancies produced after 1.5 MeV proton (b) and alpha particle (d) irradiation.

As seen from the results shown in figure 6.2a, the ion range is of the order of 16 μm for the case of proton irradiation and 6 μm for the alpha particles (figure 6.2c). It is

important to note that although heavier ions have smaller range they create more damage as seen in figure 6.2b, d.

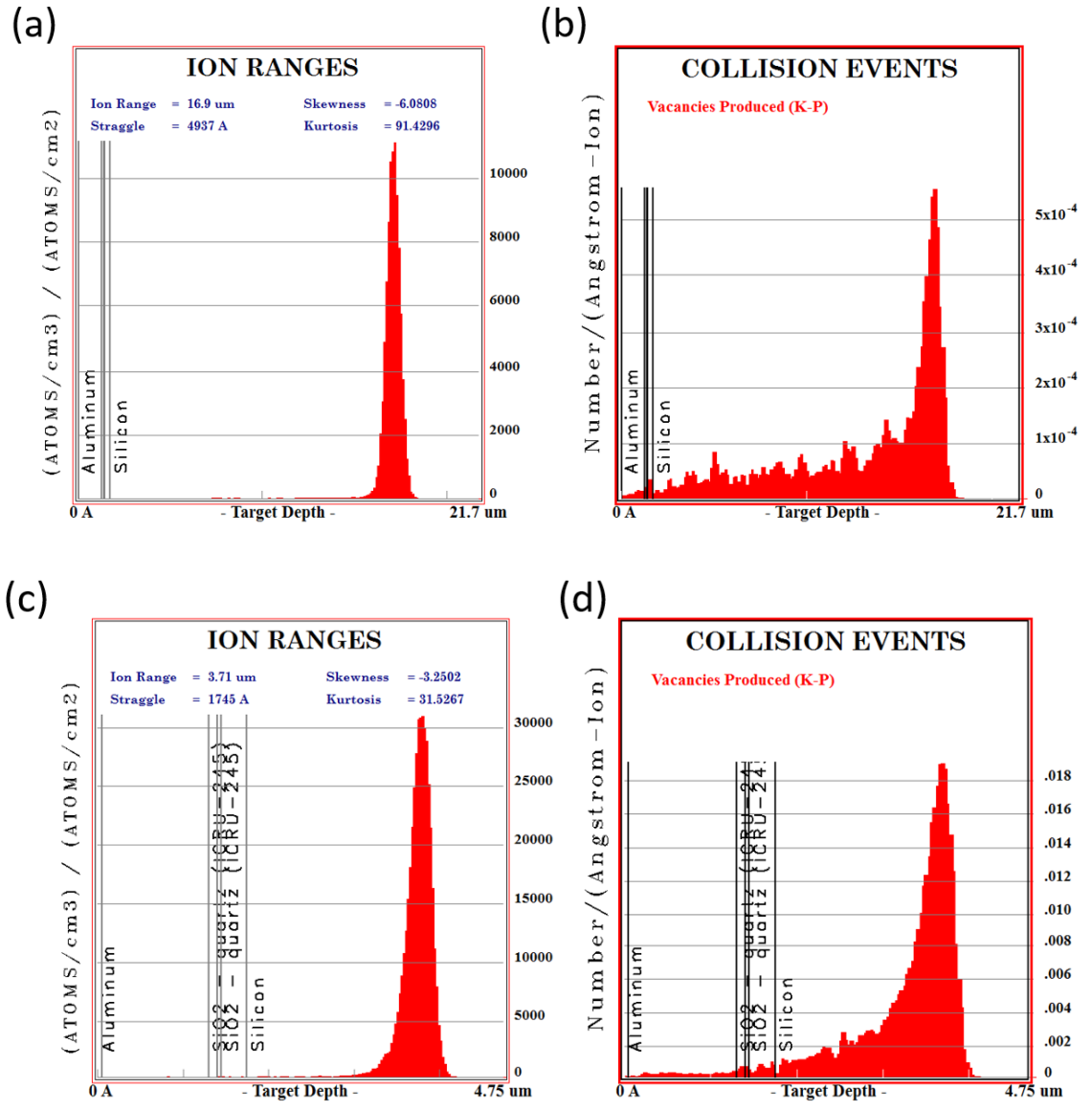

Figure 6.3. Insulated gate device: Ion range after 1.5 MeV proton (a) and alpha particle (c) irradiation. Vacancies produced after 1.5 MeV proton (b) and alpha particle (d) irradiation.

Ion range and damage simulations for insulated gate devices show very similar results to the non-encapsulated devices (figure 6.3). Again, the heavier alpha particles

will create more collision events compared to proton radiation. The ion range is slightly smaller than what it was before due to the encapsulation and dielectric layers that insulated gate GFETs have over the standard ones.

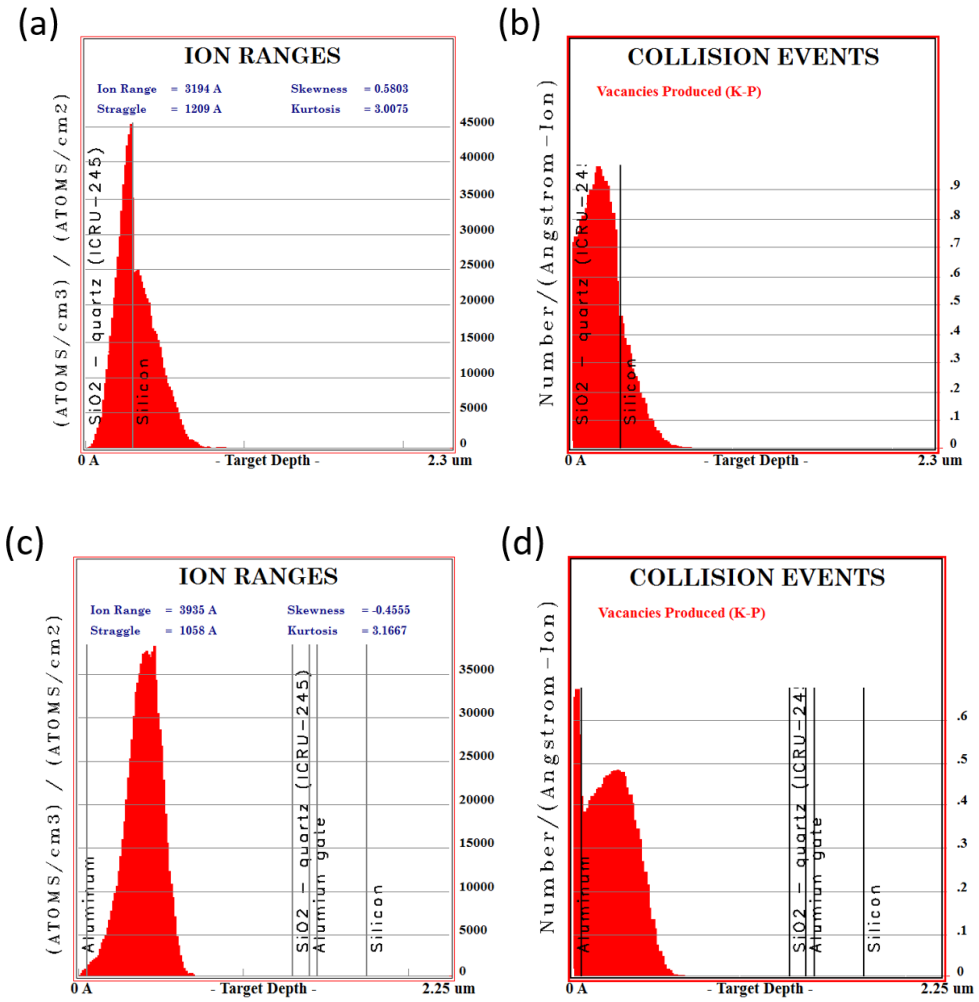

Figure 6.4. Range of 350 KeV Fe ions on non-encapsulated (a) and insulated gate (c) GFETs Vacancies produced after irradiation for non-encapsulated (b) and insulated gate (d) devices.

Finally, we run 350 KeV Fe simulations for both device structures. Figure 6.4 shows the ranges and damage caused by the iron ions. This time though, and due to the fact that Fe is a much heavier atom (compared to protons and alpha particles) the ion penetration depth is significantly smaller than what it was before. Specifically, Fe ions won't be able to penetrate more than few microns inside the device, and in the case of insulated gate the ions will stop before reaching graphene (figure 6.4c). This is a very important result, since the passivation layer will act as a radiation shield and prevent any displacement damage to the graphene layer.

6.3 Electrical Characterization

Our ion radiation analysis starts with electrical measurements of the non-encapsulated GFETs before and after ion exposure. Using the Keithley 4200 Parameter Analyzer and a 3-probe setup, we measured the Dirac point shift and mobility degradation of the devices after being exposed to various ion doses. Specifically, 3 different doses were examined (10^{14} -10^{15}-10^{16} ions/cm^2) of both proton and alpha particles. The energy of the ions was 1.5 MeV using the Dynamitron particle accelerator presented before. Unfortunately, iron (Fe) particle irradiation was not successful as we constantly run into problems using the 300 KeV Fe implanter, and experimental data (apart from simulation results) won't be presented in this thesis.

Figure 6.5 presents the collective results of the Dirac point shift for devices exposed to proton and alpha particles. As we can see from the results, both radiation sources affect the device behavior in a similar way with a positive Dirac point shift of up to 45 V.

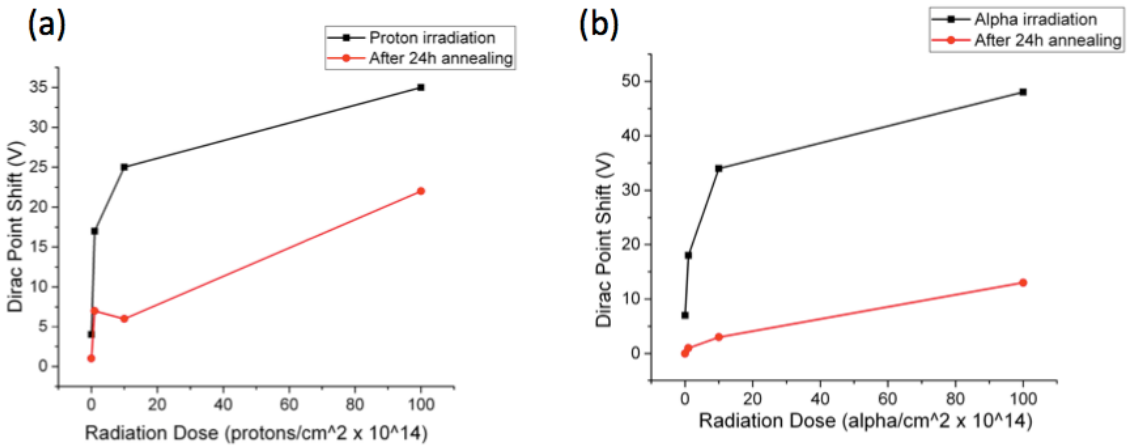

Figure 6.5. V_{Dirac} shift (before and after annealing) of non-encapsulated devices after exposure to proton (a) and alpha (b) radiation.

In order to further study the irradiation effects of ions we performed post-irradiation annealing at 180 °C for 24 h. Previous studies [91,103] have shown that an annealing step can be beneficial, as it can partially restore the order of the graphene lattice limiting the effects of displacement damage. As we observe in figure 6.5, there is a significant improvement of the Dirac point shift for annealed devices that indicates the presence of a healing mechanism. Of course, some improvement can be attributed to the desorption of the unwanted environmental dopants (such as water and oxygen), similarly to what we saw in our previous results [93], as the devices under test were non-encapsulated devices. In contrast to our desorption study though, the annealing wasn't enough to completely heal/restore the performance of the device to as-fabricated levels.

Figure 6.6 presents the mobility degradation results of GFETs under ion irradiation. In accordance to the $V_{Dirac\ shift}$ results presented above, exposed GFETs saw a dramatic decrease of their μ_{FE} (up to 80%) due to lattice damage caused by the ions.

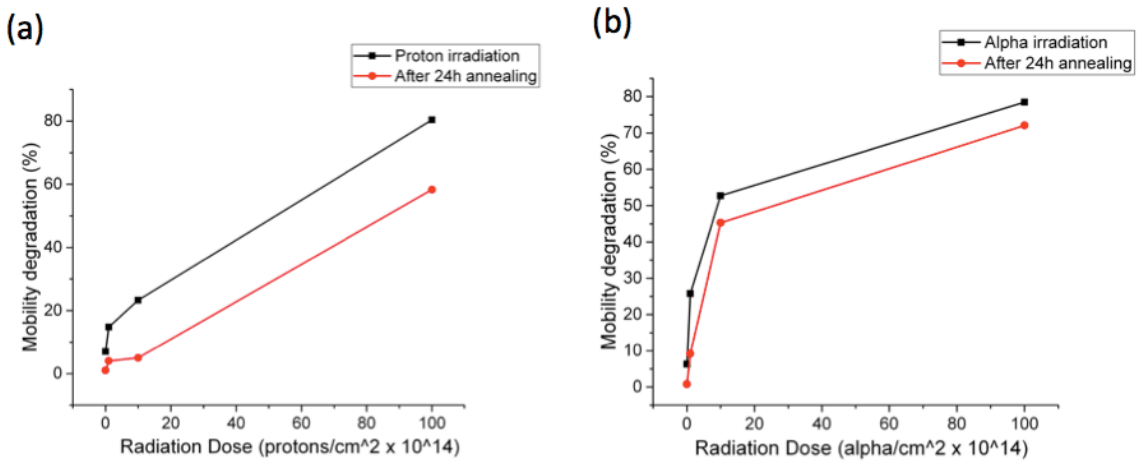

Figure 6.6. Mobility degradation (before and after annealing) of non-encapsulated devices after exposure to proton (a) and alpha (b) radiation.

It's also important to note that the effects of annealing on the μ_{FE} recovery are limited, with a moderate improvement after proton irradiation and a very small one in the case of alpha particles. Table 6.1 summarizes all the results from our ions radiation study.

Table 6.1 | Effects of ion irradiation on non-encapsulated GFETs

(ions/cm^2)	Non-Encapsulated Protons		Non-Encapsulated Alpha		Annealed Proton/Alpha			
	ΔV_{Dirac} (V)	**μ_{FE} decrease (%)**	**ΔV_{Dirac}**	**μ_{FE} decrease (%)**	**ΔV_{Dirac}**		**μ_{FE} decrease (%)**	
No ions	4	7	7	6.3	1	0	1	0.8
10^{14}	17	14.8	18	25.8	7	1	4	9.2
10^{15}	25	23.3	34	52.7	6	3	5	45.3
10^{16}	35	80.4	48	78.5	22	13	58.3	72.1

6.4 Raman Spectroscopy

Raman spectrum measurements were conducted on non-encapsulated GFETs, in order to evaluate the crystal lattice damage after ion irradiation. Our electrical

characterization results indicate substantial displacement damage, thus a high I_D/I_G ratio is expected. Figure 6.7a,b shows the results on graphene's Raman spectrum after exposure to 10^{16} ions/cm^2. We immediately notice the formation of an intense D peak (indicative of lattice damage) on both proton and alpha radiated samples. It is also evident that alpha particle irradiation causes considerably more lattice damage (by comparing the D peak and I_{2D}/I_G ratios) when compared to proton irradiation. This can be attributed to the increase mass of alpha particles compared to protons. In both cases, and similarly to our e-beam experiments, graphene is following the amorphization trajectory reported by previous studies [98].

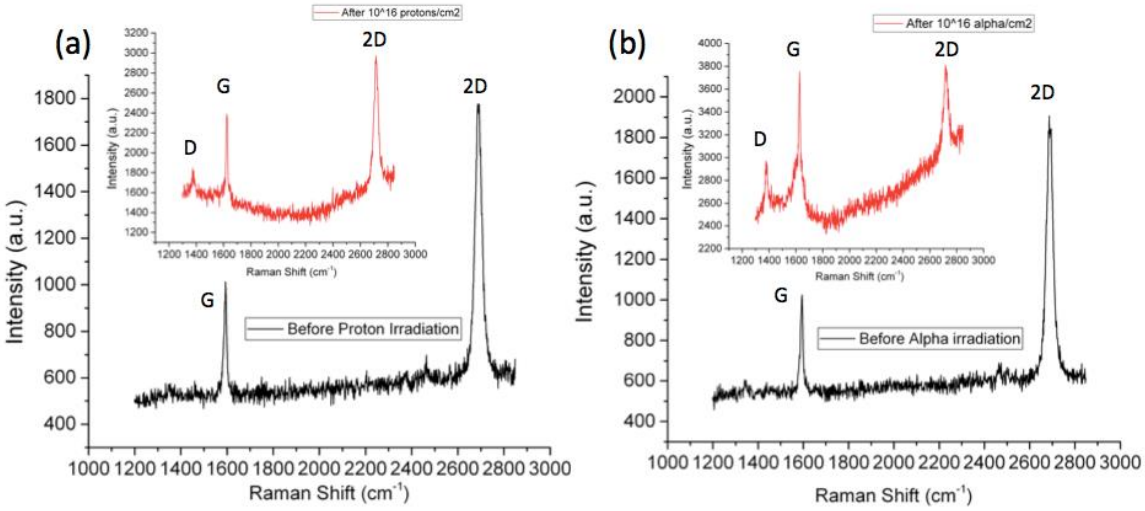

Figure 6.7. (a) Raman spectrum of non-encapsulated device before and after 10^{16} protons/cm^2 (inset) (b) Raman spectrum of non-encapsulated device before and after 10^{16} alpha/cm^2 (inset).

Figure 6.8 quantifies the I_D/I_G ratio of ion exposed GFETs. Irradiated devices show a significantly higher I_D/I_G ratio (up to 0.35) when compared to the as-fabricated GFETs. Ion induced lattice damage is moderate at doses up to 10^{15} ions/cm^2 and becomes substantial at a dose of 10^{16} ions/cm^2. Since the ion exposures were conducted under

vacuum environment, the lattice damage observed is entirely attributed to the energetic ions, as there is no contribution of reactive oxygen/ozone that we saw before. In addition, a significant upshift to in both G and 2D peak (from 20-35 cm^{-1} for protons and 25-45 cm^{-1} for alpha) along with the reduced I_{2D}/I_G ratios, confirm the radiation induced disorder for exposed devices.

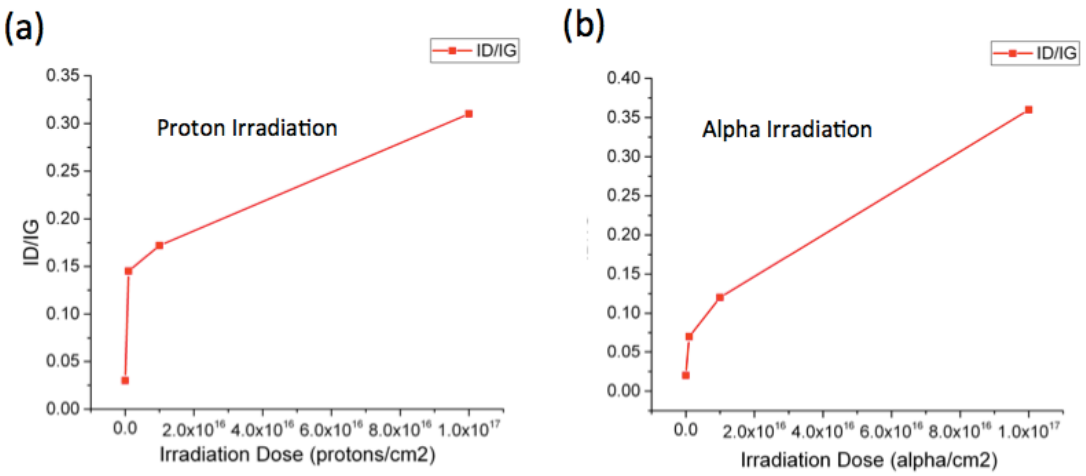

Figure 6.8. (a) I_D/I_G ratio as a function of proton radiation dose (b) I_D/I_G ratio as a function of alpha particle radiation dose.

6.5 Chapter Summary and Conclusions

In this chapter we performed ion irradiation testing (protons, alpha and iron atom simulations) in order to expand our understanding on the radiation hardness of our GFETs. We first performed simulations using the SRIM software package, focusing on the penetration depth (range) and displacement damage of the energetic ions on our samples. Simulation results indicated that GFETs suffer from significant lattice damage, which we verified with our electrical characterization and Raman analysis afterwards. Non-encapsulated devices exposed to different ion doses (10^{14}-10^{16} ions/cm^2) exhibited a

significant μ_{FE} degradation and V_{Dirac} shift. Furthermore, Raman spectroscopy results demonstrated that substantial lattice damage originates from the interaction of graphene's lattice with the ions. Increased lattice disorder is observed as a result of increased D peak intensity and reduced I_{2D}/I_G ratio to all irradiated devices.

Chapter 7

Lamdasat (Λ-sat) Cubesat Mission

7.1 Introduction

Λ-sat is a joint cubesat project across Columbia University, San Jose State University and NASA Ames research center. The project started in March 2013 towards a July 2014 launch with the Orbital Sciences Orb-2 resupply mission to the International Space Station (ISS). The main mission of Λ-sat is two-fold: First to demonstrate global communication capabilities with the maritime fleet for security specific applications and towards the problem of piracy using the AIS (Automatic Identification System) signal, and to pursue a fundamental understanding on the radiation hardness of graphene by doing in situ measurements in space. In situ measurements while our cubesat is orbiting earth will give us an insight on the exact processes and mechanisms that our graphene devices will undergo. Our circuit-board consisting from the actual graphene device plus the circuitry needed for the measurement, will measure and send us the transfer characteristic (I_d-V_{gs}) of the irradiated GFETs for as long as the cubesat will stay in orbit.

In addition, Λ-sat is custom designed with a 3-fault tolerant architecture using COTS (commercial-of-the-shelf) components in order to lower the overall cost and explore the cost effectiveness of such design. Λ-sat is planned to be launched from the ISS JAXA small satellite orbital deployer (SSOD) to low earth orbit and remain functional for a period of approximately 6 months. Throughout that 6-month period it

will constantly collect data from both AIS and graphene experiment and send it back to Earth for further analysis.

Finally, Λ-sat is the first Greek microsatellite in space, and as such, it will be used to address STEM (science, technology, engineering and math) educational objectives.

7.2 Satellite Mission

7.2.1 Communication Experiment

The Automatic Identification System (AIS) consists a key safety maritime traffic tracking system used by vessel traffic services (VTS), for the identification and location of vessels through the exchange of data between nearby ships, AIS base stations and communication satellites (Satellite-AIS). Is has a supplemental use to radars, which still consist the primary method of collision avoidance. The IMO (international maritime organization) requires all vessels with gross tonnage of 300 or more, as well as all passenger ships to install and use AIS.

Each AIS transponder consists of one VHF transmitter, two VHF TDMA receivers, one VHF Digital Service Calling (DSC) receiver and links to shipboard display and sensor systems via standard marine electronic communications (such as NMEA 0183, also known as IEC 61162). It automatically broadcasts vessel information using Time Division Multiple Access (TDMA) using the globally allocated marine band channels 87 and 88 (figure 7.1). There are two channels used, channel A at 161.975 MHz (87B) and Channel B at 162.025 MHZ (88B). In addition, AIS uses GMSK modulation, thus, ordinary VHF receivers have to disable filtering (it destroys GMSK data) in order to

receive and read the AIS signal. Figure 7.2 shows an example of the information included in a received AIS message from a Greek vessel.

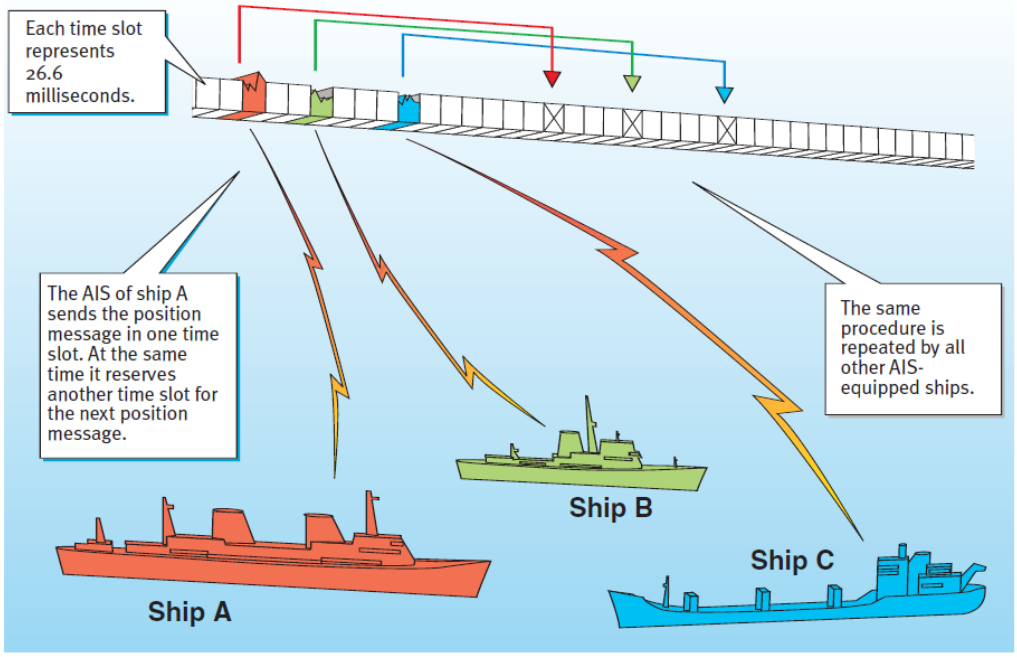

Figure 7.1. AIS message transmission between ships using TDMA.

The development of satellite-based AIS (S-AIS) started with few experimental missions in 2005, and since then, various companies and governments have tested the idea of having communication satellites with AIS capabilities [105-106]. The biggest advantage of S-AIS is that satellites can receive/transmit AIS signals from a much larger footprint than what terrestrial base stations and vessels can. By employing a constellation of small satellites in low earth orbit, a global AIS communication network can be established, offering unprecedented visibility into maritime traffic.

AIS sentece and data					
Sentence	MMSI	Message Type	Class	Vessel Name	Comments
!AIVDM	239692000	5	A	BLUE STAR ITHAKI	Base Position
!AIVDM	371793000	1	A	Harlequin	Position Report A
!AIVDM	237614000	4	A	Mytilene	Position Report A

Vessel data and dynamic information	
AIS Message Type	4
MMSI	237614000
IMO number	7332672
Call Sign	SYMK
Vessel Name	MYTILENE
Destination	Piraeus
ETA	2013-10-14 07:10 (UTC)
Speed	17.7kn
Course	257°
Longitude	37.46113
Latitude	25.05397

Figure 7.2. Example of a received AIS message.

The focus of our experiment is to utilize S-AIS for security reasons, and more specifically, for piracy monitoring in selected areas of the earth. Satellite AIS data enables us to detect changes in vessel's route/velocity, which can indicate that a ship is in danger. In addition, by analyzing the traffic patterns, we can identify and mark high-risk areas, helping authorities to determine safer shipping routes.

7.2.2 Science Experiment

The second part of the mission of Λ-sat is to test the radiation hardness of graphene in a real space environment. We should also note that, this mission is the first-ever graphene experiment in space. Graphene will be exposed to space radiation for the amount of time that the satellite will remain in orbit, which should be in the order of 6 months. As seen in figure 7.3a, there are three different GFETs on board, two non-

encapsulated and one insulated gate GFET. These are exactly the same device structures that we tested against alpha, beta, gamma and ion radiation, mounted at the bottom of the cubesat. As we already described in previous chapters, space radiation involves different particles (different charge, mass), with kinetic energies ranging from few MeV to GeV. Until now, the fabricated devices have been tested under one radiation source at a time, in contrast to what will happen in LEO. Furthermore, our satellite was launched in 2014, a year that the solar activity is at its peak (figure 7.3b), which means that our devices will be exposed to increased proton and alpha particle radiation.

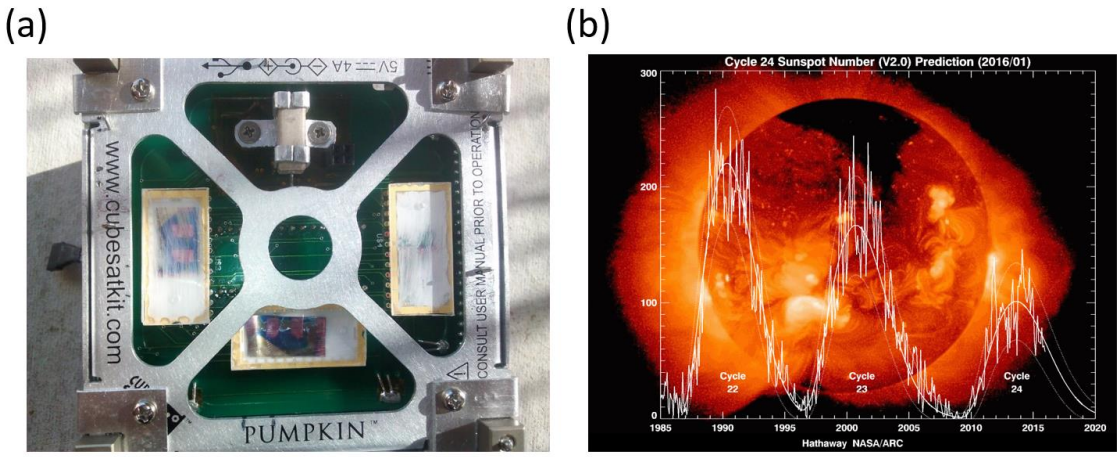

Figure 7.3. (a) Three GFETs mounted on Λ-sat (b) Solar cycle prediction.

Our terrestrial radiation tests indicated that three main mechanisms are responsible for the performance degradation of graphene, environmental contribution, substrate effects and displacement damage. In LEO, and despite the fact that the devices will operate in vacuum, the presence of reactive oxygen [107] can have similar effects to the ones we saw on earth.

7.3 Λ-sat Subsystems

7.3.1 System Overview

Λ-sat is a 1U cubesat (10x10x10 cm), designed to be deployed from the ISS in LEO (altitude of approximately 370-380 km). Its weight is 1.33 kg and the whole structure was built using the space qualified pumpkin aluminum frame. All the circuit boards on the satellite are custom made, using COTS components certified for -40 °C to 85 °C operation.

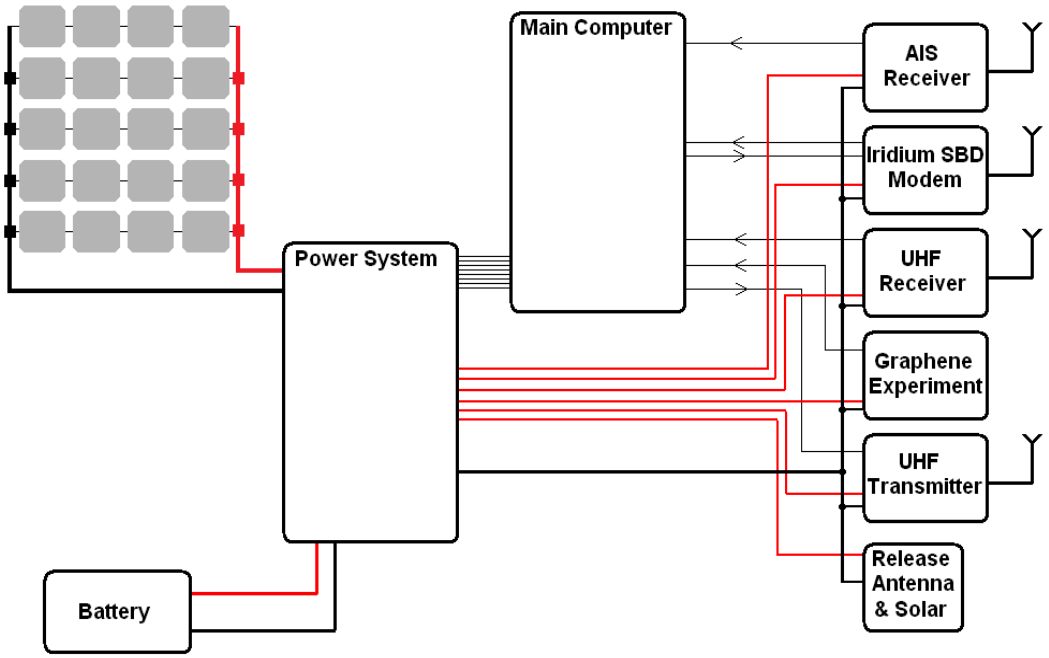

Figure 7.4. Λ-sat block diagram.

The Λ-sat block diagram is depicted in figure 7.4 with a high level overview of the main subsystems that need to work together in order for the satellite to operate. As shown in figure 7.4 the main subsystems of the satellite are: main computer board, power

system board, battery, solar panels, AIS receiver, iridium Modem, UHF receiver, graphene board, UHF transmitter and the needed antennas for the communication with Earth. Communication can be achieved with two different ways: Through HAM radio (stensat beacon) using the integrated antennas on the satellite or by utilizing the Iridium constellation for a faster and easier connection to the ground.

7.3.2 Main Computer

The main computer board, as shown in figure 7.5a, is the heart of the satellite. It is the board that coordinates all the functions and operations between the several subsystems. Three identical microcontrollers were used, implemented in a three-fault tolerance voting system for extra redundancy (figure 7.5b). Since we used COTS parts and not radiation hard electronics for our boards, we had to ensure that even if one of the microcontrollers fails, the main computer board would still function.

A watchdog timer checks for the normal operation of the three main microcontrollers and switches to the next one, in case of failure. It has five serial (Tx/Rx) communication ports (for all communication with the other components), two analog inputs and one internal oscillator at 4 MHz. Finally, a “remove before flight” pin connects battery to the main computer board, and a 40-minute timer starts counting down until the board powers on (safety mechanism required during the cubesat deployment from ISS).

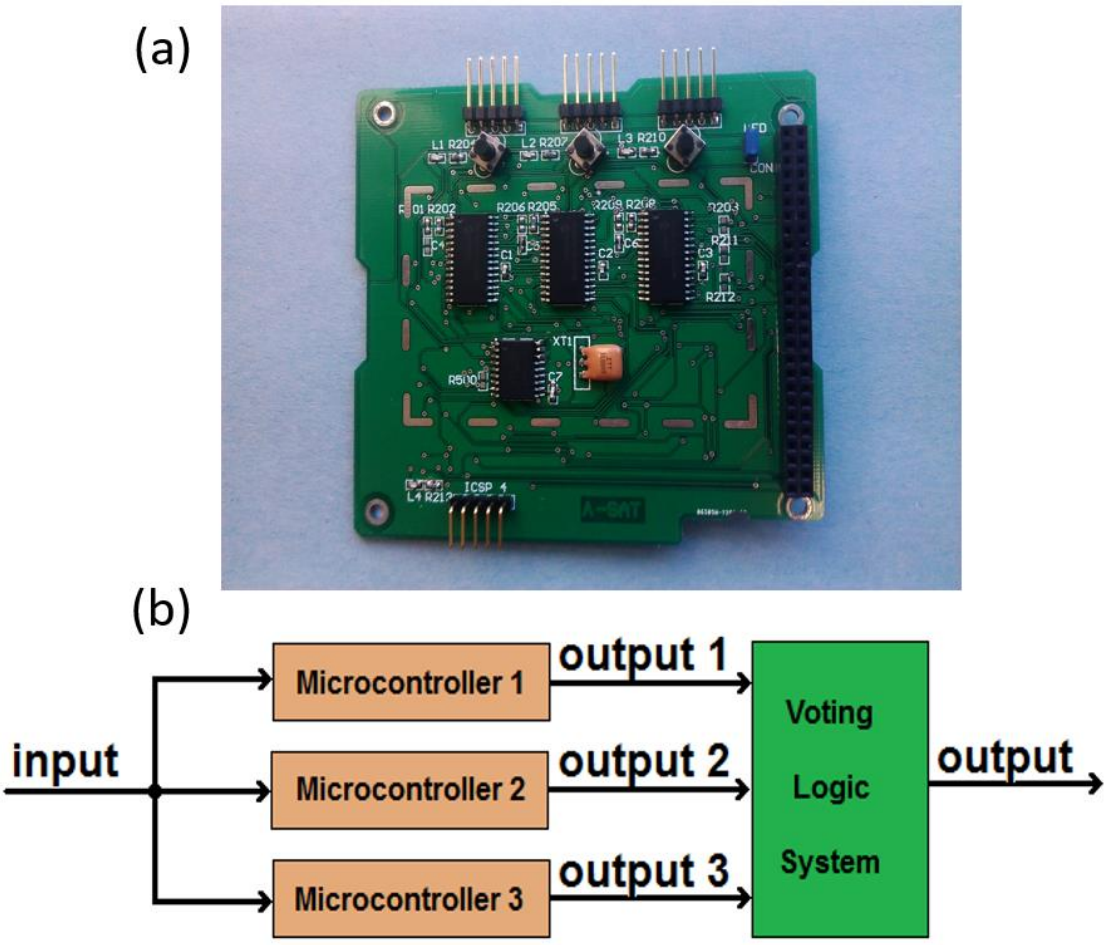

Figure 7.5. (a) Λ-sat main computer board (b) Schematic of the 3-fault tolerant voting system.

7.3.3 Power Board and Solar Panels

The power board, battery and solar panel arrays are the three key components for the generation, storage and distribution of available energy of the satellite. The main source of energy is the sun, and since the satellite will be orbiting earth every 90 minutes, half the orbit time will be behind earth. A very important factor for every satellite, and specifically for cubesats, is the total power budget. The fact that cubesats offer limited area to mount solar panels (in our case, only four sides can be utilized), makes power

consumption one of the prominent challenges when designing the satellite. The total power budget for Λ-sat is approximately 4 W, with the maximum power of solar panels at 3 W for a 1U design. This entails that the satellite will be most of time in a low power mode (sleep mode) in order to decrease power consumption and charge the batteries.

The solar panels used on the satellite are based on triple junction ($GaInP_2$/GaAs/Ge) cells with 29.5 % efficiency from spectrolab. Instead of using only the four sides of our satellite for mounting the panels, we developed a deployable mechanism (figure 7.6) that would give us 3 times the available area (similar to a 3U design). That enabled our satellite to operate in a high-power state (ON state) for more than 4 hours per day. The battery used is a Canon BP-930, a space qualified battery that NASA has already used in past missions. It is lithium ion based, with an output voltage of 7.4V, 4800 mAh capacity and weights 195 grams.

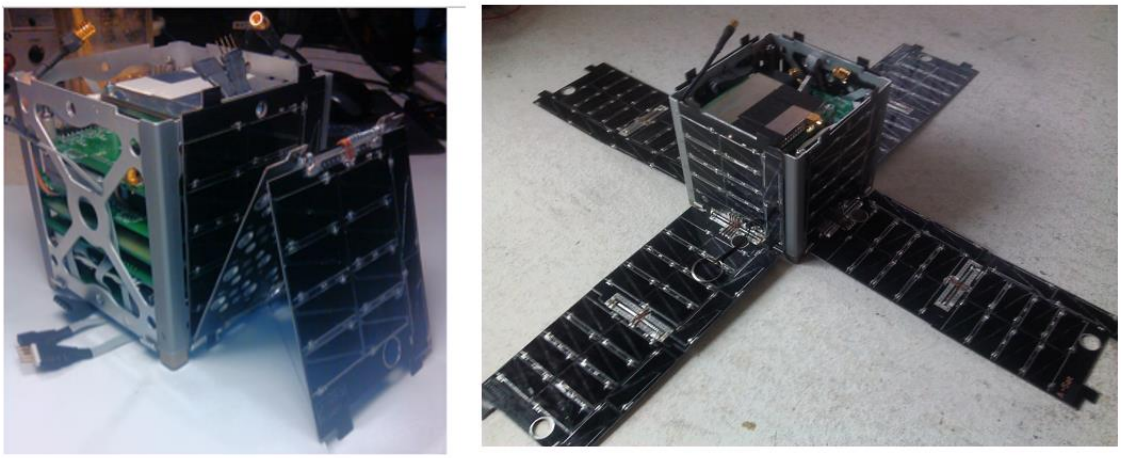

Figure 7.6. Λ-sat's deployable solar panel mechanism.

The power system board as shown in figure 7.7a,b has 8 independent inputs to accommodate the solar arrays mounted on the satellite. It manages the power generated

from the panels (total output of deployable panels ~ 16.5 W) and controls the battery charging.

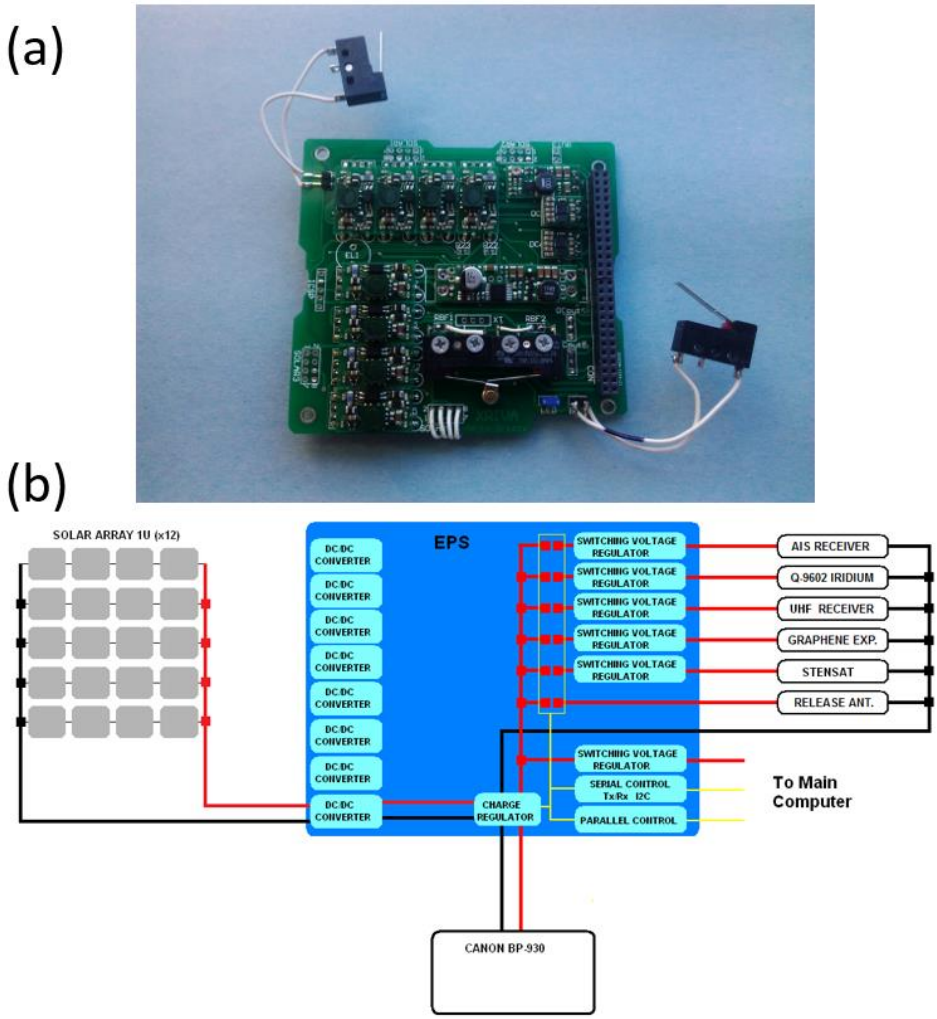

Figure 7.7. (a) The physical power board of Λ-sat (b) Block diagram of the power system board.

We have included an internal mechanism for powering the system directly from solar panels, in case of battery failure. There are 6 controlled power outputs for devices, fully protected against over-current, thermal and short circuit scenarios (4 outputs at 4.5-25 V up to 2 A, 2 outputs at 5 V up to 2A). In addition, there is an independent power output of 5 V/1 A for the main computer. It uses serial and parallel communication with the main

computer board, and has the ability to monitor the battery for overcharging/deep discharging.

7.3.4 Graphene Board

The board is based on an Arduino nano microcontroller, with a main task of measuring the transfer characteristic (I_d-V_{gs}) of the embedded GFETs. The measurements will be conducted 4 times per day, and the results will be stored to the main memory of the satellite until sent to earth. Three devices are on board (2 non-encapsulated and 1 insulated gate structure) with 2 working transistors each (for a total of 6 GFETs). The evolution of the Dirac point shift and mobility degradation through the I-V curve of GFETs will give us the necessary information to evaluate the radiation effects on the device from the space environment. The block diagram of the graphene board is depicted in figure 7.8. Through the use of Arduino's 5 V analog outputs and the selection of the appropriate operational amplifiers, we were able to generate the V_{gs} and V_{ds} voltages for our device operation. We have included a temperature sensor in order to store the temperature associated with each measurement.

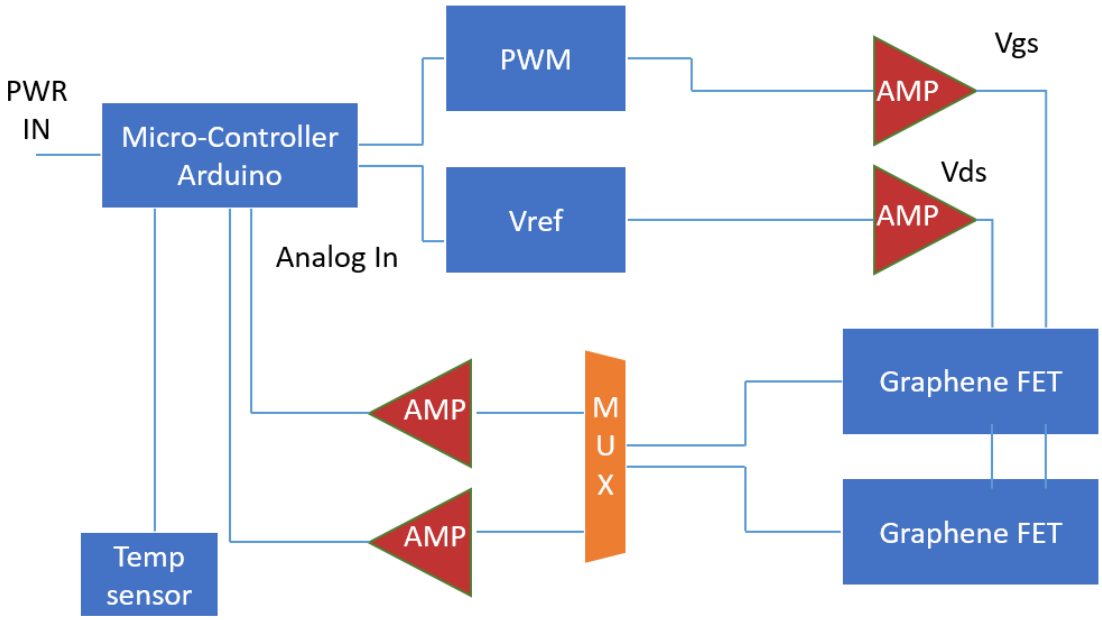

Figure 7.8. Graphene board block diagram.

Each measurement will take approximately ~ 5 sec, while the max power consumption of the board is 1 W. After the measurement is completed, the board sends the data to the main board (Baud rate 9600), which then sends the graphene results to earth, either by using HAM radio or through the Iridium communication network. Figure 7.9a shows the final graphene board along with the included hysteresis rods (magnetic). The role of the magnetic rods is to align the spin of satellite (which otherwise would be random) with the magnetic field of the earth. With the rods on the graphene board, Λ-sat will be completing two full rotations on every orbit (figure 7.9b).

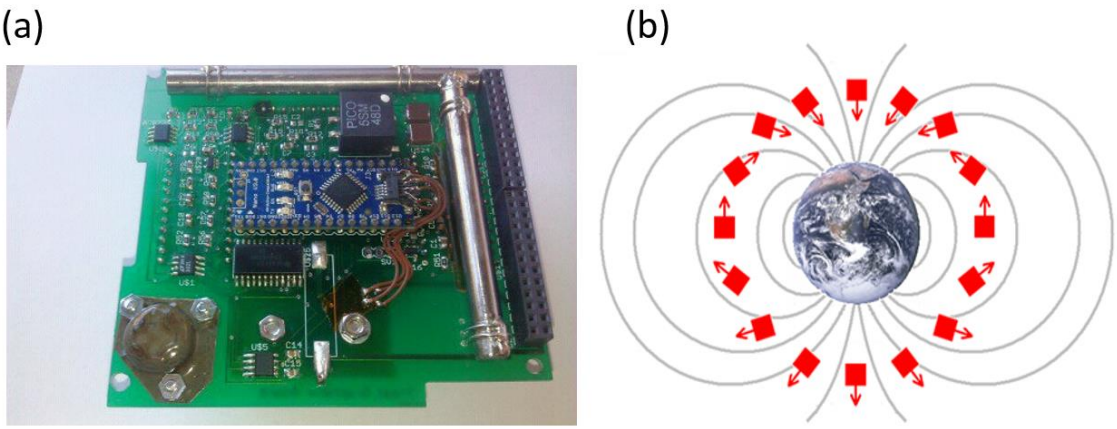

Figure 7.9. (a) The final graphene board with the hysteresis rods included (b) Schematic of the controlled rotation of the satellite when aligned with the magnetic field of earth.

7.3.5 Iridium and Radio Communications

Our satellite was designed to be able to send date back to earth utilizing two different communication channels. We are using the standard HAM radio (stensat beacon) at 437.462 MHz (UHF) as our back up communication method (figure 7.11b). This is due to the difficulties of tracking the satellite while in orbit and the need of a ground station to pick up and decode the transmitted signals. Our main communication method is based on using the Iridium constellation of satellites. Iridium network consists of 66 communication satellites with global coverage orbiting in LEO (781 km altitude). That methods gives us a significant advantage over the traditional radio communication since data can be retrieved and parsed via computer servers on PC based applications, making it far more reliable than HAM radio (figure 7.10a). The iridium modem used, is the model SBD 9602 (figure 7.10b) and is responsible to transmit the AIS, graphene and housekeeping data to the iridium network.

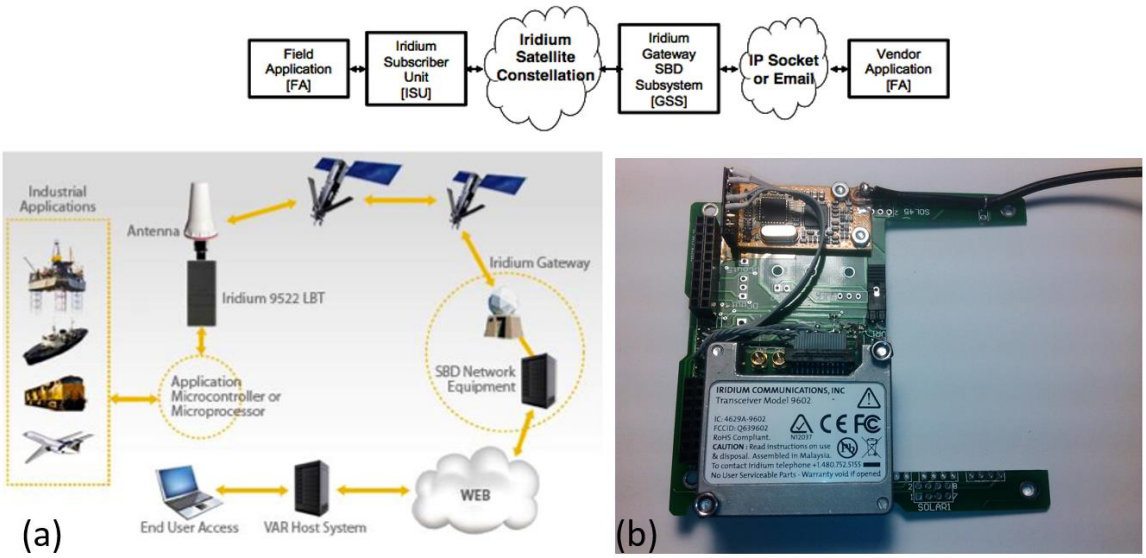

Figure 7.10. (a) Schematic description of the Iridium global network of satellites (b) The SBD 9602 Iridium modem used on Λ-sat.

Finally, figure 7.11a shows the AIS receiver used for the reception and decoding of the maritime VHF band (model ARS 100). It is capable of both on-board processing and digital sampling, with excellent sensitivity and low power consumption (< 1.5 W).

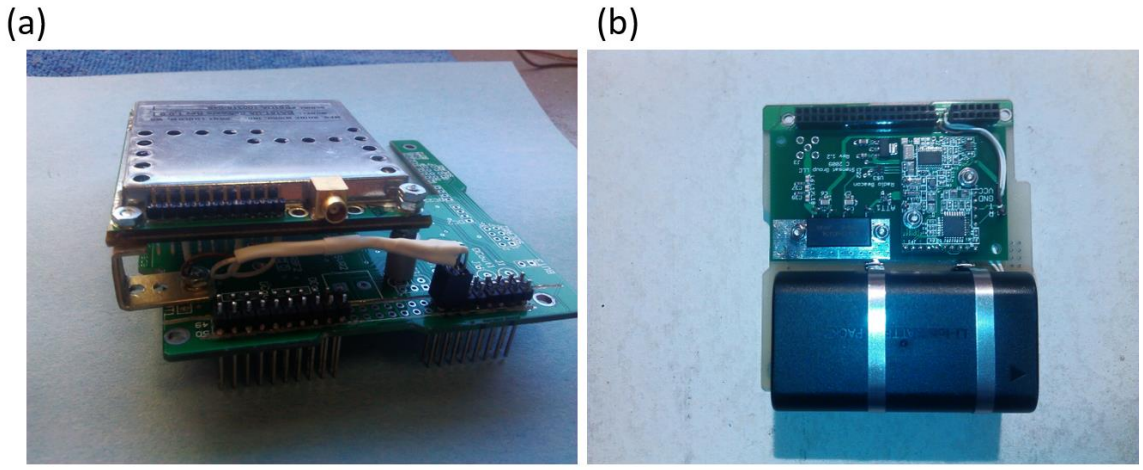

Figure 7.11. (a) AIS receiver used in Λ-sat (b) UHF transmitter used for HAM radio communication.

7.4 Launch Operations

Prior to the delivery of Λ-sat to NASA (March 2014), the satellite had to get ISS certification through a variety of tests. Through the completion of vibrational, thermal, electrical, and vacuum tests, the satellite was certified for safe ISS operation. After the delivery to NASA (figure 7.12) the satellite will be delivered to NanoRacks and will get placed into the NanoRacks CubeSat Deployer. The satellite is stowed in a Common Transfer Bag (CTB) for the launch.

Λ-sat launched from NASA Wallops island, on July 13th 2014. It was part of the ISS resupply mission, Orb-2, transferring the necessary cargo/experiments to the space station. The launch vehicle used was the Antares rocket from Orbital ATK, with the Cygnus spacecraft delivering the cargo to ISS (figure 7.13a,b). Finally, through some series of unexpected delays, Λ-sat was deployed from ISS on March 3rd 2015 and stayed in low earth orbit until the end of June 2015 (figure 7.13c).

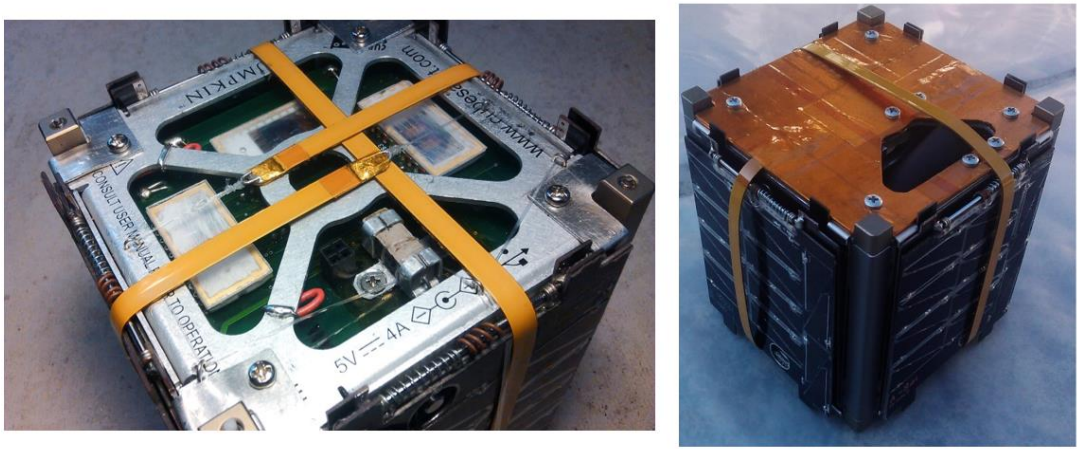

Figure 7.12. Λ-sat as-delivered to NASA for launch preparation.

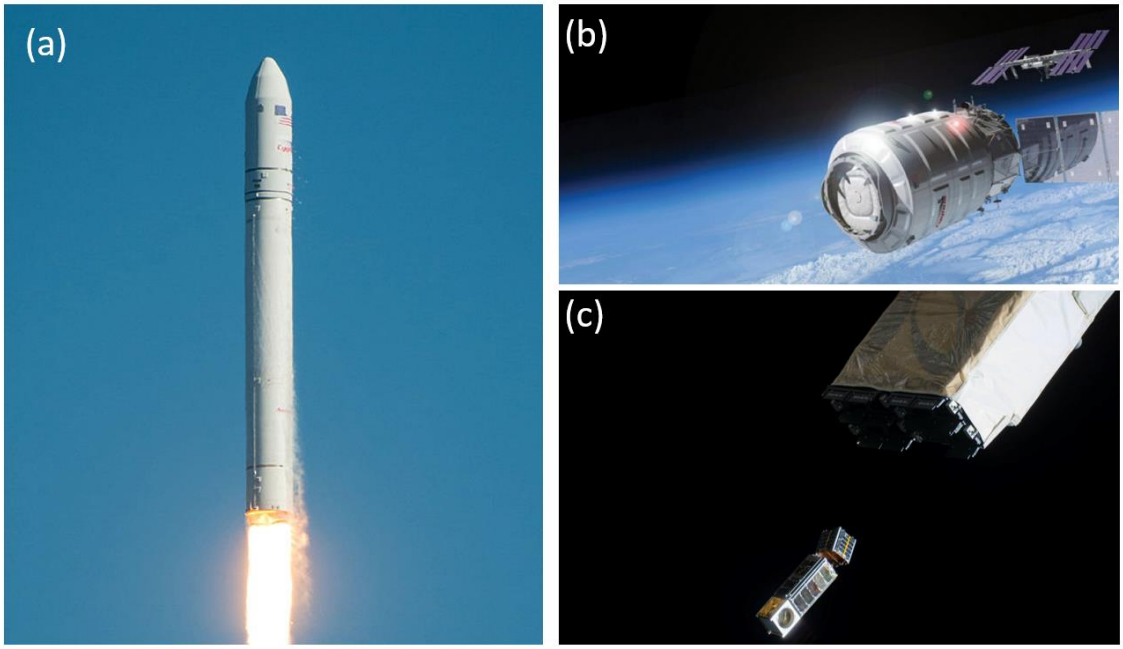

Figure 7.13. (a) Antares rocket during launch, Orb-2 resupply mission (b) Cygnus spacecraft 8 min post launch in LEO (c) Λ-sat deployment from ISS using the JAXA small satellite orbital deployer.

7.5 Chapter Summary and Conclusions

The Λ-sat project was successfully completed with the deployment of the satellite from ISS. From start to finish, it took almost 2 years to complete and deliver a flight certified satellite to NASA. Λ-sat is the first satellite to include graphene on board and test the radiation hardness in a real space environment. In addition, it is the first cubesat that employed the Iridium satellite constellation as a more efficient and reliable communication channel to earth. Unfortunately, due to several delays and accidents that happened during the satellite mission (JAXA deployer problem, Orb-3 mission accident) the satellite was deployed almost a year after the planned date. While Λ-sat was orbiting earth, we were able to establish some form of communication (inconsistent) receiving housekeeping data from the satellite back to earth. There were no experimental data

received, either from the graphene experiment or the AIS receiver. We believe that the main problem of the satellite was the inability to sustain enough battery charge, thus, operating for more than few minutes.

Chapter 8

Conclusions and Future Work

8.1 Contributions of this Work

This thesis demonstrates the effects of ionizing radiation on graphene-based field effect transistors. It mainly focuses on the degradation and damage mechanisms on the material and device level when exposed to high-energy particles. In addition, several methods to improve the radiation hardness of graphene are tested, and device structures with improved radiation tolerance are developed.

We first successfully fabricate GFETs, with low impurity doping and good performance characteristics. The basic back-gate transistor structure is then enhanced with devices employing a passivation layer and an insulated gate design. The encapsulation layer based on a thin film of Parylene-C and aluminum, gave our devices superior air stability and very low performance variability when exposed to ambient environment.

We start our irradiation testing by exposing our GFETs to gamma rays. Electrical characterization post-irradiation revealed a significant performance hit to the non-encapsulated device structure. Performing irradiations under nitrogen environment and using XPS measurements we proved that a very important mechanism of degradation is the generation of reactive oxygen/ozone due to gamma rays. Encapsulated devices

exhibited superior performance characteristics compared to devices with no passivation layer. Furthermore, Raman measurements were used to identify the possible displacement damage to the crystal lattice of graphene, which was minimal in the case of gamma rays. Finally, our insulated gate GFETs exhibit improved gamma radiation hardness by minimizing the influence of the radiation induced defects of the substrate.

Following the gamma irradiation, GFETs are tested against high-energy beta irradiation (MeV). We first perform Monte Carlo simulations for all device structures in order to get an estimation of the range and damage from the energetic electrons. Raman spectroscopy revealed that the crystal lattice is severely affected this time. High-energy electrons can cause significant displacement damage, which can be estimated from the increased intensity of graphene D peak (defects peak). TEM measurements revealed that lattice damage happens in energies as low as 80 KeV. Moreover, encapsulation is again essential, since beta rays induce the formation of reactive oxygen and ozone molecules from the interaction with the ambient environment. Lastly, the insulated gate GFETs exhibit the smallest performance degradation by combining a passivation layer with a thin aluminum gate.

Our final radiation experiments were conducted by testing our GFETs against ion irradiation, similar to the one found in space. More specifically, proton and alpha particles (cosmic rays/solar radiation) with kinetic energies of 1.5 MeV were used. Simulation performed prior to irradiation showed that we should expect increased lattice damage compared to the beta rays, due to the heavier atoms used. Our electrical and

Raman analysis showed that, as expected, performance degradation caused by the lattice damage is significant and comparable to the beta radiation case.

The last task of our radiation experiments was to study the performance of our devices in a real radiation environment. We successfully completed the Λ-sat program, in collaboration with SJSU and NASA Ames, in order to build a satellite for in-situ radiation measurements in low earth orbit. Our cubesat microsatellite had double mission: 1) Monitor the performance of the embedded GFETs while evaluating the degradation due to space radiation and 2) Establish communication through the use of AIS with maritime vessels in order to improve safety in high risk areas of the planet. Our satellite launched towards ISS with the Orb-2 resupply mission (July 2014), and was successfully deployed several months after that (March 2015).

8.1 Future Work

This thesis evaluated the radiation effects on graphene-based devices by testing several GFET structures against a variety of radiation sources. We mostly focused on identifying the effects on the material and device level, looking into the transport properties and lattice damage of graphene.

While our analysis revealed the main mechanisms of degradation using the GFET as our testing platform, there are several other graphene-based devices that exploit different properties of graphene. Specifically, the effect of irradiation on the mechanical, optical, and thermal properties of graphene needs to be evaluated, since these devices may show completely different behavior than our irradiated GFETs.

Our radiation tests were conducted with the devices under zero bias. It would be worthwhile to test the radiation hardness of GFETs when connected to a power source. The effect of soft errors (single events upsets, latchups and burnouts) can be detrimental, and cannot be evaluated unless the device is in the ON state.

Finally, different shielding methods have to be tested. The sensitivity of graphene to the underlying substrate and oxide layer is crucial for the retention of its intrinsic properties. As a result, different selection of materials has the potential to improve graphene's radiation hardness even further.

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Appendix A

Effect of Vacuum Thermal Annealing on GFETs

A.1 Introduction

A variety of encapsulation methods have been proposed to prevent unintentional doping [57-60], increasing the stability of GFTEs while operating in air. In addition, methods such as current annealing [55], solvent treatment [67], thermal annealing [108], and oxygen plasma cleaning [109] have been widely used to etch or desorb the unwanted dopants from graphene and regain device performance to as-fabricated levels. However, encapsulated GFETs are still prone to the effects of the environment after prolonged air exposure (weeks to months) as oxygen and water molecules can still slowly diffuse through the encapsulation layers. Furthermore, cleaning methods present only a temporary solution, since devices have to be kept under vacuum or at low temperatures, limiting their use in real world applications.

In this work, we combine both encapsulation and thermal annealing techniques to mitigate the effects of the environment, recover the electronic performance of GFETs to as-fabricated values, and examine the question of whether encapsulation layers also trap water inside the device system. Using a low thermal budget encapsulation method that we previously presented [93] we study the effects of varying vacuum annealing time on encapsulated devices and propose a mechanism of recovery. In addition, by testing non-encapsulated devices in oxygen only (dry air) and an ambient air (O2/H2O) environment

we were able to highlight the contribution of each dopant on the Dirac point shift and mobility degradation of GFETs. Our results clearly show that vacuum annealing can further enhance the air stability of encapsulated devices by reversing the effects of dopant diffusion after prolonged periods of air exposure.

A.2 Materials and Methods

Back-gated GFETs were fabricated using graphene grown by chemical vapor deposition (CVD) following the same process steps as described in chapter 2. Similarly, non-encapsulated (uncapped) devices were immediately inserted into a CVD system to deposit 1.25 μm of Parylene-C followed by a 50 nm thermally evaporated aluminum layer on top. Another set of devices was encapsulated with the same method after one week of air exposure.

For the electrical measurements, the devices were placed on a heating plate in a vacuum chamber (20 mTorr) and with the aid of a probe station and pA meter/DC voltage source HP 4140B, the transfer characteristics IDS-VGS at VDS=50 mV were obtained, either in vacuum environment or in ambient atmosphere for the long-term degradation study. Two or more devices were examined for each case, under the same conditions mentioned above. In order to investigate the long term electrical performance, devices were left in ambient environment (20 °C, 40-50% humidity).

A.3 Results and Discussion

Figure A.1 shows the Dirac point change for the uncapped SLG-FET as a function of annealing time for 390 and 450 K at vacuum. It has to be noted that the transfer

characteristics were measured in-situ during the annealing. In both annealing conditions the Dirac point is decreasing with increasing annealing time while the decrease rate along with ΔV_{Dirac} value depend on the annealing temperature. According to the literature [55-56], the decrease of Dirac point may be correlated with to the desorption of functional groups, adsorbents, and trapped water molecules between the graphene and the SiO_2

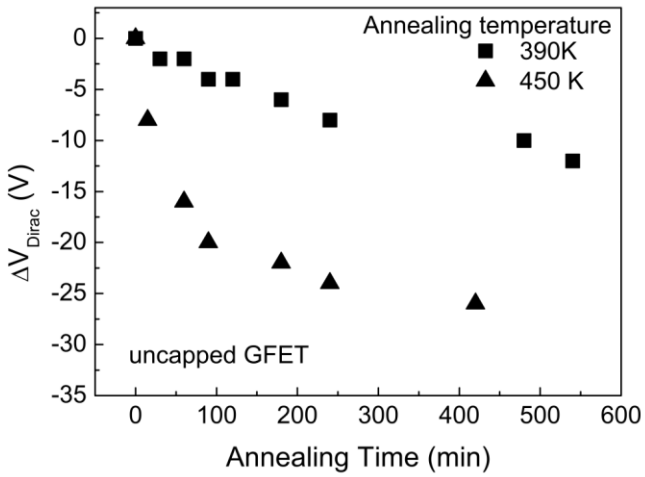

Figure A.1. Dirac point change of the uncapped SLG-FET as a function of annealing time for temperatures 390 K and 450 K.

In order to evaluate the influence of the humidity on the position of Dirac point, the uncapped transistor was subjected to several conditions and the transfer characteristics were monitored as shown in Figure A.2. Initially, the I_{DS}-V_{GS} curve demonstrates a clear p-type behavior with an estimated Dirac point around 50 V and a field effect mobility (μ_{FE}) of 100 cm^2/Vs. After 5 hours of vacuum annealing at 450 K, the Dirac point shifted towards lower gate voltage values while μ_{FE} increases by 59% (from 100 cm^2/Vs to 159 cm^2/Vs), as seen from the transfer characteristics slope in the left part of the curve. Within the vacuum chamber dry air was introduced and the transfer

characteristics were monitored after 15 minutes and 24 hours. It is seen that even after 24 hours of exposure to dry air, the curve is slightly shifted towards higher gate voltage values as μ_{FE} stays the same. Finally, the sample was exposed to ambient atmosphere, and after 10 minutes of exposure the I_{DS}-V_{GS} curve exhibited an abrupt shift towards higher gate voltages. Similarly, 4 hours of continuous air exposure of the uncapped device resulted in a positive V_{Dirac} shift to the direction of the initial (before vacuum thermal annealing) curve with a μ_{FE} of 113 cm^2/Vs (28.9% decrease).

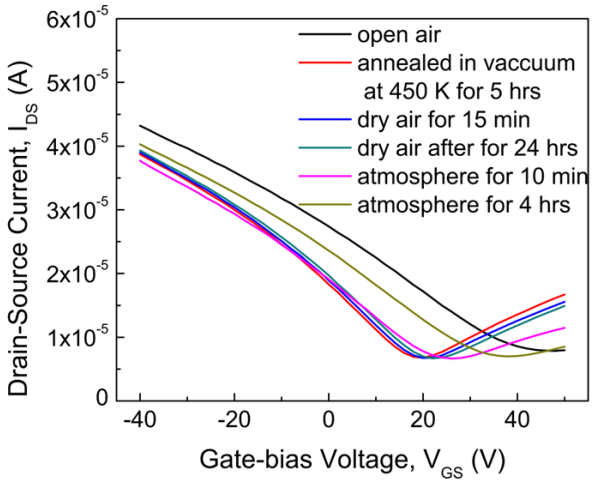

Figure A.2. Transfer characteristics (V_{DS}=50 mV) of uncapped graphene FET after various conditions.

Figure A.3 illustrates the extracted Dirac point voltage during the conditions mentioned above. Initially, the Dirac point voltage is found at 46 V, and after 5 hours of thermal annealing in vacuum, it drops down to less than 20 V. The exposure to dry air has minor effects on the device, as after 24 hours, the V_{Dirac} slightly increases at around 22 V. However, when the G-FET is exposed to ambient atmosphere for both 10 minutes and 4 hours, the V_{Dirac} increases to 26 V and 38 V respectively.

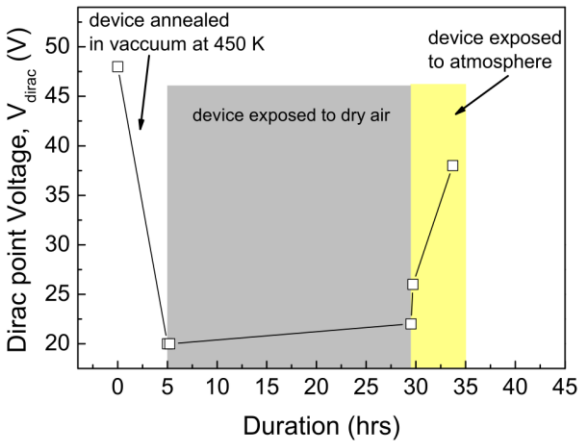

Figure A.3. Dirac point extracted from electrical measurements of uncapped graphene FET at various environmental conditions. The effect of the dry air and the exposure to air are shown.

The experiments in dry air and ambient atmosphere clearly show that the transfer characteristics of uncapped GFETs are highly dependent on the humidity that exists in air and a capping layer can be applied in order to provide adequate protection against moisture penetration. The proposed encapsulation method based on a Parylene-C and aluminum passivation layer, which offers excellent stability for a long period of time and significantly reduces moisture penetration. To this end, we prepared devices with Parylene/Al coating in two different ways: i) the coating layers were deposited immediately after the manufacturing of the GFET and ii) the coating layers were deposited after leaving the GFET in ambient atmosphere for one week. Our goal was to fabricate devices that have already adsorbed humidity prior to the application of the capping layers.

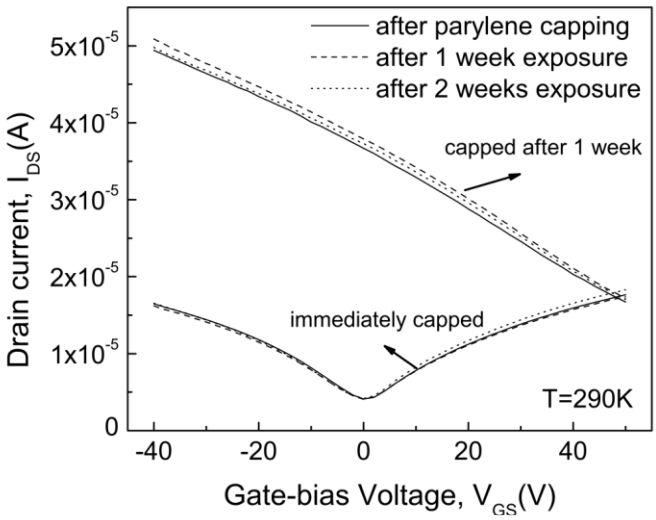

Figure A.4. Transfer characteristics of SLG-FETs encapsulated with Parylene/Al i) immediately after fabrication and ii) after 1-2 weeks of air exposure.

Figure A.4 shows the transfer characteristics of the two types of devices as a function of their exposure time. We observe that the immediately capped device exhibits a near-zero Dirac point voltage, with excellent stability over a period of 1-2 weeks. On the other hand, the devices that have been coated with Parylene/Al after the device have been deliberately exposed to air for one week, demonstrate a Dirac point voltage that exceeds 50 V, likely due to humidity adsorption before the capping layer application. However, even for this case, the transfer characteristics of the coated devices are slightly affected by the additional 2 weeks of exposure in air. It may therefore be deduced that the Parylene/Al coating presents an excellent protection to both the moisture penetration of the air's humidity and the humidity already adsorbed, if any, by the device. The latter can present some technological limitations on the conditions under which the encapsulation may take place. For instance, if the device has already been exposed to environmental conditions before the application of the capping layers, the system will trap water vapor

inside and degradation of the transfer characteristics will be permanent. Hence, it would be of great importance if such devices can be "repaired" after the deposition of the Parylene/Al encapsulation. To this end, vacuum annealing at 393 K for various durations was performed to encapsulated transistors.

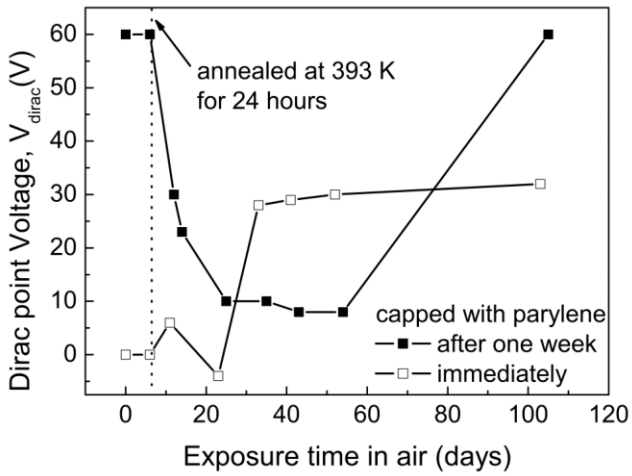

Figure A.5. Dirac point voltage variation of SLG-FETs capped with Parylene/Al i) immediately after fabrication and ii) after 1 week of exposure in air. The devices were annealed at 393 K in vacuum for 24 hours and the Dirac point voltage was monitored for 100 days of exposure to atmosphere.

Figure A.5 illustrates V_{Dirac} as a function of exposure time in air for both immediately capped transistors and those that have been capped after one week in air. Prior to the exposure the devices have been heated up to 393 K in vacuum for 24 hours. In the case of the immediately capped devices, the thermal annealing did not seem to have any particular effect on the Dirac point voltage, as slight modifications from 5 V to -5 V were observed after several days of ambient atmosphere exposure. However, when the device was measured after 30 days of air exposure, the transfer characteristics were degraded so that the V_{Dirac} was measured at around 30 V and this degradation remained for more than

100 days. An abrupt drop of V_{Dirac} down to 30 V was observed on devices that were originally degraded after thermal annealing for 24 hours at 393 K. In addition, when the device was left to air, the decrease of V_{Dirac} continued, and after 40-50 days, it achieved the lowest value of 9 V. When the device was measured again after 100 days of air exposure, it was found that V_{Dirac} increased up to 60 V, similar to its initial (before annealing) state. A similar experiment was conducted, where the devices were annealed at the same conditions as before, except that the annealing duration was limited to 3 hours. The results are shown in Figure A.6.

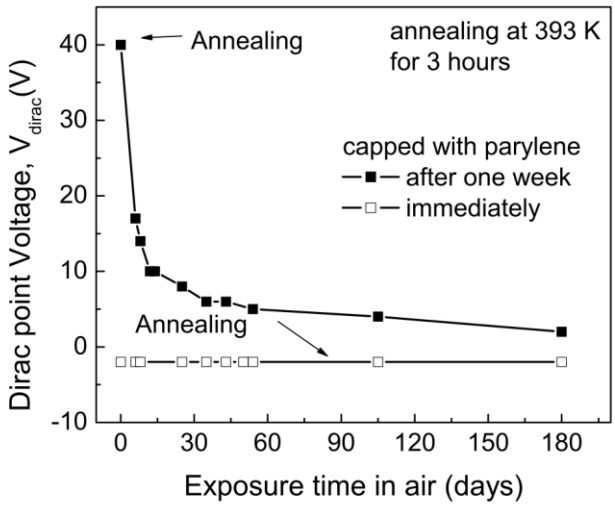

Figure A.6. Dirac point voltage variation of SLG-FETs capped with Parylene/Al i) immediately after fabrication and ii) after 1 week of exposure in air. The devices were annealed at 393 K in vacuum for 3 hours and the Dirac point voltage was monitored for 180 days of exposure to atmosphere.

We observe that for the immediately capped device, V_{Dirac} exhibits no modification after annealing, even if the device is exposed to air for more than 180 days. In the case of capped devices that were exposed for one week, the effect of thermal annealing remains significant, as V_{Dirac} is reduced from 40 V to 17 V, continuing to

rapidly decrease for the next 60 days of exposure. For the next 120 days the device exhibits rather stable behavior with a slight decrease of V_{Dirac}.

A.4 Conclusions

From the above experiments and observations, we conclude that vacuum annealing of encapsulated devices has an important and continuous impact on the electrical performance of GFETs. It is well documented that Parylene-C water diffusivity is relatively low, in the order of 10^{-9} cm^2/s, and increases almost exponentially with increasing temperature [110]. Our proposed mechanism is that the thermal annealing in vacuum triggers the desorption of water vapor molecules from the graphene surface to the Parylene-C film, shifting Dirac point to lower gate values (reduced p-doping). As figures A.5, A.6 show, the duration of the annealing plays a crucial role on the lifetime stability of the devices. While GFETs that were subjected to different annealing times show similar initial behavior with a significant reduction in p-doping (negative V_{Dirac} shift), their long term stability is drastically different. Devices annealed for 24 hours exhibit an increase in their Dirac point after 20-40 days of annealing, whereas, GFETs annealed for 3 hours show no performance degradation for more than 6 months. It is likely that an extended annealing time damages the encapsulation layer, allowing water vapor and oxygen to diffuse from the ambient environment to the graphene surface.

Appendix B

Amorphous Silicon – Graphene Anodes for Lithi12um Ion Batteries

B.1 Introduction

It is well known that for applications such as Electric Vehicles (EV), new batteries with high capacity and extended lifetime at elevated temperatures and high charging rates are needed [111, 112]. Towards this direction, silicon is probably the most promising material for the next generation of Li-ion batteries due to its low discharge potential and to its extremely high capacity in lithium [113-114]. However, the intercalation of the lithium atoms within the silicon material provokes a high increase of its volume (up to 300%), that progressively leads to the pulverization of the layer resulting in poor cycling and high irreversible capacity loss. To improve the number of cycles, several routes have been proposed that allow the silicon to be able to expand in all direction (nanostructures) and/or to enhance its mechanical properties with the substrate (usually copper foil) [115-116].

Out of the many possible applications of graphene, energy storage in the form of new advanced batteries incorporating graphene/Si anodes can be a promising advancement in the all growing need for higher capacity/faster charging time Li Ion

Batteries. With its superior electrical conductivity, high surface area and great mechanical strength, graphene can help release the strain and keep the structure integrity intact while the lithium intercalation takes place at the anode.

B.2 Materials and Methods

Copper has almost zero solubility of carbon at high temperatures which leads to a growth mechanism of carbon nucleation sites adsorbed to the Cu surface forming a continuous polycrystalline single layer graphene film. The larger grain size of copper foils compared to the evaporated or sputtered copper films on arbitrary substrates is able to give us a more crystalline single layer graphene (SLG) with better uniformity and surface flatness. By using the CVD method, single layer graphene is grown on both sides of the foil, and it is preferable to utilize the graphene that lays on the top side. Since the foil itself is placed on top of a carrier glass substrate, some of the foil's bottom surface area will not be exposed to the CVD gases resulting on defective SLG or no growth at all. Our next step is to remove any patches of defective SLG on the bottom side utilizing dry etching methods, namely RIE, where oxygen ions will impinge and remove all the organic substances from the foil, thus graphene.

Amorphous silicon was grown by DC magnetron sputtering. The deposition was performed at room temperature by sputtering a 4-inch c-Si target with argon flow rate at 20 sccm and at pressure of 7 mTorr. The substrates of SLG/Cu and Cu foils were introduced at the same chamber for every condition of silicon growth. The resulting silicon film thickness was estimated by both the methods of UV-Vis spectroscopy and

Dektak profilometry. Films with varied thickness from 40 nm to 400 nm were obtained. Raman spectroscopy was performed in order to reveal the amorphous nature of the film.

The electrochemical measurements were carried out using two-electrode Swagelok cells with pure lithium foil as counter electrode and Si-based materials as working electrodes, at room temperature. The electrolyte used was 1.0 M LiPF6 in a 50:50 (w/w) mixture of ethylene carbonate and dimethyl carbonate. Cell assembly was carried out in an Ar-filled glovebox with concentrations of moisture and oxygen below 1.0 ppm. The charge/discharge tests were performed using a BaSyTec multichannel battery tester in a voltage window of 1.5–0 V with a current of 0.02 mA. The mass of the electrode was calculated solely from the a-Si thickness and considering silicon density of 2.3 g/cm^3. It has to be noted that the single layer graphene mass was not taken into account as it is estimated negligible compared to the a-Si film.

B.3 Results and Discussion

Raman spectroscopy was also employed to show the amorphous nature of the deposited silicon as shown in figure B.1a. Indeed, the broad peak centered at 480 cm-1 along with the fact that no peak is present at 521 cm-1 demonstrates that the silicon is amorphous with no crystalline phase within the volume of the film. Concerning the half-cell performance of the silicon-based anodes, 40-nm-thick a-Si was deposited on top of Cu, SLG/Cu and non-uniform/SLG/Cu foils. Figure B.1b shows the discharging specific capacity of a-Si based anodes as a function of the number of cycles. We have to mention that for our cells, the discharging process denotes the Li deintercalation from the anode

material. It is observed that the initial specific capacity of the a-Si/Cu anodes is higher than the a-Si/SLG/Cu anodes.

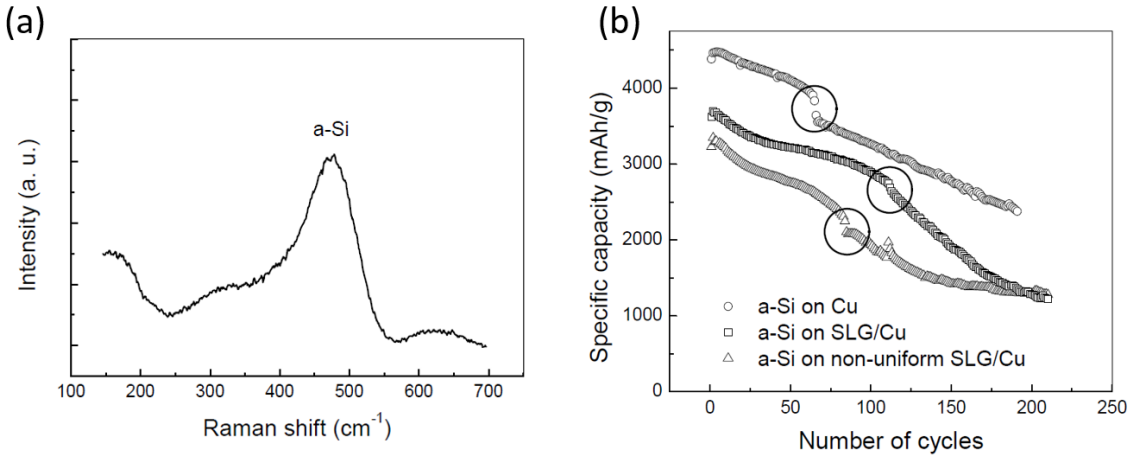

Figure B.1. (a) Raman spectra of DC-sputtered silicon on copper foil. The existence of a broad peak centered at 480 cm-1 Raman shift unveils the amorphous nature of the grown silicon (b) Discharging specific capacity of silicon based anodes on copper and SLG/copper foils as a function of number cycles. The charging/discharging procedure was performed at 0.02 mA current. The a-Si thickness was 40 nm.

More specifically, a-Si/Cu anode exhibits an initial capacity of more than 4000 mAh/g and drops at 2375 mAh/g at the end of 200 cycles almost linearly. In addition, an abrupt loss of capacity is noticed after 60 cycles. Regarding the a-Si/SLG/Cu electrodes, we present both the performance of the a-Si/non-uniform SLG/Cu (back side dry etched sample without top protection) and of the a-Si/SLG/Cu in terms of cycling behavior. In the case of a-Si/non-uniform SLG/Cu the specific capacity varies from 3220 mAh/g to 1330 mAh/g stabilized after 180 cycles. Once again, we witness a sudden loss of the capacity after 80 cycles. Finally, the a-Si/SLG/Cu electrode exhibits initial capacity of 3620 mAh/g lowering down to 1250 mAh/g at the end of 210 cycles, which seems to be close to its stabilized value. In this case, no abrupt capacity drop is observed during the

cycling procedure, providing an indication that the graphene could potentially lower the stress of the a-Si film and therefore withhold, up to a certain limit the volume expansion of the silicon. This is more supported by the observation that the non-uniform SLG anode exhibits almost the same behavior than the a-Si/Cu anode, since it contains also parts with a-Si directly deposited on copper foil. However, the performance of the lower capacity provided by the graphene silicon anode still needs to be clarified.

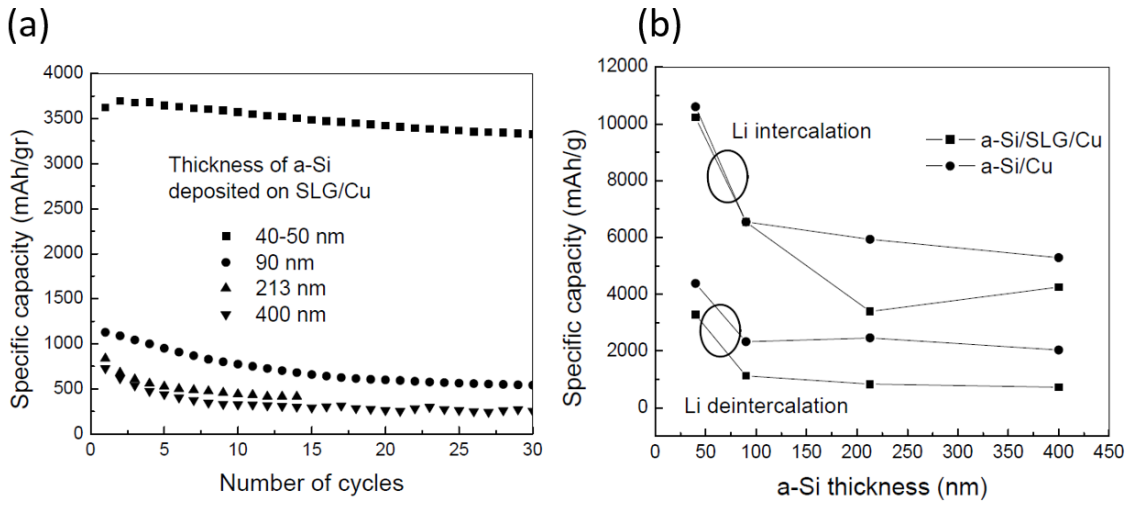

Figure B.2. (a) Specific capacity as a function of cycle number for a-Si/SLG/Cu anodes with various thicknesses of deposited a-Si. The charging/discharging procedure was performed at current of 0.02 mA. (b) Maximum specific capacity during the first Li intercalation and deintercalation into a-Si/SLG and –Si anodes with various a-Si thicknesses.

In order to investigate more closely the effect of the mechanical stress to the graphene based anodes, figure B.2a exhibits the performance of a-Si/SLG/Cu electrodes over cycling with a variety of a-Si thicknesses. It is observed that the initial as well as the final (after 10-20 cycles) specific capacity decreases with increasing a-Si thickness, with no abrupt change in the capacity, thus supporting the previous suggestion. More precisely, for the 40-nm-thick a-Si sample, the specific capacity is well above 3500

mAh/g whereas for 400-nm-thick a-Si it is less than 750 mAh/g. Moreover, for thicker samples the stabilized capacity is achieved in less cycles than the thinner ones. However, when the electrodes with various thicknesses are charged and discharged with the same current (thus different C-rate), the thicker electrodes should exhibit higher specific capacity. This contradiction could be attributed to the fact that during cycling the loss of anode material (due to the pulverization of a-Si) becomes more important for thicker silicon since the volume expansion is more pronounced. Since the specific capacity is calculated by taking into account only the initial a-Si, then it becomes obvious that any material change during cycling will lead to an underestimation of its value (i.e. if during the 20th cycle only half of the material is still on the anode, the extracted specific capacity should be multiplied by a factor of 2 to provide the "real" specific capacity).

In figure B.2b we compare the first charging (Li intercalation) and discharging (Li deintercalation) specific capacity for a-Si and a-Si/SLG/graphene anodes. We remark that the highest specific capacity appears for the 40-nm-thick sample. In addition, in all cases, the first Li intercalation specific capacity is much higher than the respective deintercalation. This is typically attributed to the formation of the Solid Electrolyte Interface (SEI), where Li ions are consumed at the electrolyte/anode interface in order to create a thin solid layer which passivates the anode. Finally, it is noticeable that a-Si/Cu exhibits larger Li deintercalation capacity than a-Si/SLG/Cu for all samples independently of the silicon thickness. To be able to clarify these findings it is essential to take into account the effect of the electrode resistance. Figure B.3a shows the typical simplified equivalent circuit of a cell battery. During charging and discharging a constant

current is applied and the voltage is measured at the two terminals. It is clear that if the resistance of the electrode is increased Rm is also increased and then the voltage of the cell will decrease for the same charging and discharging current.

Figure B.3b represents the first charging and discharging cycles for cells with a-Si/non-uniform SLG/Cu, a-Si/SLG/Cu and a-Si/Cu electrodes. During discharging the a-Si/Cu electrode voltage attains 1 V for a larger capacity compared to the other ones. We have to note that the maximum discharging specific capacitance is extracted at 1 V with a constant current of 0.02 mA; thus an electrode with an increased resistance will achieve 1 V prior to the maximum Li deintercalation and the specific capacity can be considered as an “effective” value. Consequently, we suggest that aSi/SLG/Cu electrodes exhibit higher resistance, which “mask” their actual specific capacity. In the literature [117], it has been shown that the graphene/silicon contact represents a rectifying diode behavior with a potential barrier of between 0.41-0.45 eV depending on the silicon doping. This further support that the graphene/silicon combination adds resistance to the cell deteriorating its performance. In the near future, more investigation will be held with the focus on changing this rectifying behavior to an ohmic contact and lowering the total resistance of the electrode.

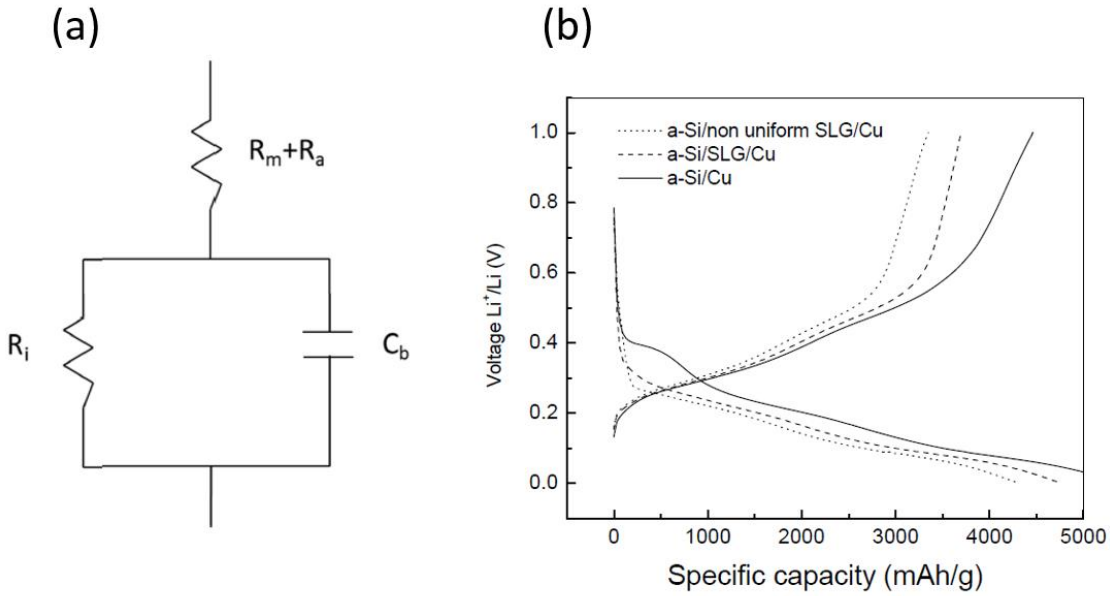

Figure B.3. (a) Typical equivalent circuit for a cell battery. R_m is the resistance accounting for the terminals, electrodes and interconnections, R_a for the electrolyte and the separator, R_i for the internal non-linear resistance between the electrolyte and the electrode and C_b the capacitance between the plates of the cell. (b) First charging and discharging cycles for half-cell with 40-nm-thick silicon-based anodes. The charging/discharging procedure was performed at 0.02 mA current.

B.4 Conclusions

This work presents a study on amorphous silicon – graphene anodes for the lithium ion battery technology. Low defect density single layer graphene was deposited by CVD on copper foil demonstrated by Raman. On top of the graphene, we grew amorphous silicon by DC sputtering with various thicknesses. With the above materials used as anodes Li-ion half cells were prepared and electrochemical measurements were carried out resulting in electrodes with specific capacity that exceed 2000 mAh/g. In comparison to electrodes without graphene it t was shown that the single layer graphene prevents the large pulverization phenomena that occur within the amorphous silicon during the electrochemical cycling. However, it was also shown that the addition of

graphene in silicon-based electrodes demonstrates lower specific discharging capacity, which was attributed to the rectifying contact between the a-Si and the graphene.