Excimer Laser Crystallization of Silicon Thin Films for Monolithic 3D Integration

Fabio Carta

Submitted in partial fulfillment of the
requirements for the degree
of Doctor of Philosophy
in the Graduate School of Arts and Sciences

COLUMBIA UNIVERSITY

2015

©2015
Fabio Carta
All Rights Reserved

ABSTRACT

Excimer Laser Crystallization of Silicon Thin Films for Monolithic 3D Integration

Fabio Carta

In 1964 the first metal oxide semiconductor (MOS) integrated circuit (IC) became available. Shortly after in 1965 Gordon Moore predicted the pace of the device density increase in ICs. His prediction became a self-fulfilling prophecy, which taking advantage of the formal device scaling rules introduced by Robert Dennard in 1974, drove the evolution of the integrated electronic industry.

In conventional two dimensional ICs, devices are integrated into a single layer of silicon in what is called the front end of line (FEOL) fabrication. Additional layers on top of the devices serve as inter-dielectric isolating layer and metal interconnects and are fabricated in the back end of line (BEOL) process. Scaling the dimension of devices allows for an increase in device density, improvement on device switching speed and reduction of the cost per device. The conjunction of these benefits drove the industry thus far. Over the past decade further scaling the devices while achieving also an increase in performance and cost benefits became extremely difficult. As the dimensional scaling of complementary MOS (CMOS) devices reaches its limits, three dimensional ICs (3DICs) are increasingly being considered as a path to achieve higher device densities. 3DICs offer a way to increase density by using multiple device layers on the same die, reducing the interconnect distance and allowing for a decrease in signal delay. Among different fabrication techniques, monolithic 3D integration is potentially more cost effective but requires high performance devices, a process compatible with transistor integration in the BEOL stack and needs to deliver a

high device density and uniformity in order to be adopted by the very large scale integration (VLSI) industry.

This work focuses on a particular laser crystallization technique to achieve monolithic device integration. The technique, called Excimer Laser Crystallization (ELC), makes use of an excimer laser to achieve a large grain polycrystalline thin-film starting from an amorphous layer, allowing integration of high quality thin-film transistors (TFTs). Thus far, the ELC technique has been studied on thin-films typically deposited on top of quartz substrate or Si/SiO_2 wafers. On the other hand state of the art VLSI integration uses more advance BEOL stacks with low-κ material as interlayer dielectrics (ILDs) to passivate the copper (Cu) interconnect lines. This thesis focuses on three different key aspect to enable laser crystallization in the BEOL for device integration: 1. Excimer laser crystallization of amorphous silicon on low-k dielectric; 2. Excimer laser crystallization of amorphous silicon on BEOL processed wafer; 3. VLSI of TFTs on excimer laser crystallized silicon.

The ELC of amorphous silicon on low-k dielectric is first explored through one dimension (1D) finite element method (FEM) simulation of the temperature evolution during the laser exposure in two different systems: 1. amorphous silicon deposited on top of SiO_2 dielectric; 2. amorphous silicon deposited on top of low-κ dielectric. Simulations predict that is necessary a lower laser energy for crystallizing the silicon on the low-κ material. Experimental observations confirm the predicted behavior yielding a 35% lower energy for crystallization of thin-film silicon on top of a low-κ dielectric. Material characterization through defect enhanced SEM micrograph, Raman spectroscopy and XRD analysis shows an equivalent material morphology for the two system with a preferential (111) crystal orientation for the SiO_2 system.

Silicon crystallization on BEOL processed wafer is studied through a combination of 1D FEM simulation and experimental observation on a silicon layer deposited on top of a SiO_2 dielectric protecting the underlying damascene Cu structure. 1D FEM show that during the silicon laser exposure, because of the short pulse width of the

laser (30 ns), the heat is retained in the amorphous silicon layer allowing its melting while keeping the temperature of the Cu lines below 320 °C which is a favorable condition for monolithic integration in the BEOL. Further experimental evidences show the ability of crystallizing a-Si on such structure while preserving the physical and electrical properties of the Cu lines.

The feasibility of monolithic VLSI 3D integration is demonstrated through integration of TFTs devices on 200 mm silicon wafers. The integration process and performance of the TFTs device are modeled through technology computer aided design (TCAD) simulations which are used to define the process flow and the fabrication parameters. Characterization of the TFTs over multiple die yield good device performance and uniformity. TFTs characterized with 1.5 V of supply voltage have a sub-threshold slope down to 79 mV/decade, current density up to 26.3 μA/μm, a threshold voltage of 0.23 V, current On/Off ratio above 10^5 and device field effect mobility up to 19.8 $cm^2/(V\times s)$ for LPCVD-sourced silicon. Furthermore, the Levinson method allows characterization of the trap density in the thin-film polysilicon devices yielding a mean value 8.13×10^{12} cm^{-2}.

This work present an integration scheme which proves to be compatible with VLSI in the BEOL of wafers. It paves the way to further development which could lead to an high performance, cost effective, monolithic 3D integration approach useful in application such as reconfigurable logic, display, heterogeneous integration and on chip optical communications.

Table of Contents

List of Figures

List of Tables

Acknowledgments

There are many persons I own my most sincere gratitude to. First, I would like to thank my advisor, Professor Ioannis Kymissis, for his valuable guidance over the years I spent at Columbia University. His scientific curiosity and intelligence inspired me since the day I joined his lab. I would like also to thank all the former and present members of the Columbia Laboratory for Unconventional Electronics. I own a particular thank to Shyuan Yang, Hassan Edrees, Dr. Htay Hlaing, Dr. Jon Beck, Dr. Yu-Jen Hsu, Dr. Vincent Lee, Dr. Marshall Cox, Dr. Brian Tull, and Dr. Nadia Pervez: from all of them I learned a lot and they helped me through various stage of my research.

I would like to deeply thank Dr. Stephen Gates for all the hours spent discussing over the phone and in person about the 3DIC project. His guidance and attention to details have been fundamental to the success of this project.

I would like to thank Dr. Daniel Edelstein for giving me the opportunity three years ago to start this project during the internship at the IBM T. J. Watson Research Center. It has been an amazing learning experience.

I would like to thank Professor James Im and many members of his research group, which shared with me their equipment and helped me in various phase of my work. In particular I would like to sincerely thank Dr. Alexander Limanov, for spending countless hour in the lab adjusting the laser parameter and crystallizing samples. Without his support my work would not be possible.

I would like to thank Dr. Simone Roux, mentor of my first internship at IBM during the writing of my Master thesis, from where all this adventure started. She is

a terrific scientist whom I deeply admire and who thought me a lot about how fun research is.

I would also like to thank my family for all their love: mom and dad, Anna and Matteo, Marina and Tonino, Giulia, Paolo and Mirjam and Sofie. I grew up all my life with you and you always represented my role model: your unwillingness to settle and your effort in continuously pushing further your knowledge and skills always inspired and shaped me.

Finally and most importantly I would like to thank my wife Michelle. She started this adventure by my side and stayed with me all the way through the other side, she really is an incredible woman whom I love very much. Without her I would have never survived the dark side of the PhD.

To Michelle, Anna, Matteo, Mom, Dad
for all their love and support.

Chapter 1

Introduction

1.1 Background and Motivations

Since the introduction of the first commercially available metal oxide semiconductor (MOS) based integrated circuits (IC) in 1964, the electronic industry based its success on the lateral scaling of transistors. Shrinking device dimensions yielded three different benefits: 1. Increase in the switching speed of the transistor, which used to correspond to an increase of the circuit performance; 2. Increase in the device density, which allows an increase in the functionality of each chip; 3. Decrease of the cost per transistor. In 1965 Gordon Moore was the first to observe a trend in the increase rate of the number of transistor in a circuit and predicted that the number of transistor in ICs will double ever year. In 1975 Moore revised his forecast doubling the time to two years, what today is called the Moore's law. Since then the industry put extreme effort in keeping the pace in scaling the transistor. The ability of fulfilling Moore's law is now being questioned not only due to technological difficulties, but also due to cost considerations and to physical limitations[1; 2; 3; 4]. Over the past decade, the technological difficulties in following Moore's law with classic scaling, forced engineers to increase the complexity of the integration process. The 90 nm node implemented strain in the silicon channel of devices to

improve the performances; The 45 nm added high-κ/metal-gate stack to reduce the leakage, and low-κ inter-layer dielectric plus copper (Cu) interconnect to decrease coupling capacitance, improve electromigration and decrease metal resistivity [5; 6]. Nevertheless, complementary MOS (CMOS) technology faces challenges. Since conventional field effect transistors (FETs) devices are not able to deliver the performance requested by the industry, innovative device geometry such as FinFETs are implemented but at the cost of increased difficulty in fabrication and incompatibility with other processes [7]. Moreover, the increasing complexity in the metal lines required to interconnect the devices (tens of kilometers in an area of square centimeters) cause an increase in the signal delay which affect the overall performance. As the lateral scaling becomes extremely difficult and expensive and the benefit unclear, three dimensional (3D) integration technology is being considered as a new approach that can deliver increase in device density, chip functionality and performance [2; 8; 9] at a lower cost.

1.2 Three Dimensional Integration

3D integration has recently generated great interest because of the benefit it delivers without requiring further device scaling. The most immediate advantage of 3D integration is the substantial reduction of the interconnect length between devices and between different circuit modules. This causes a decrease of the overall capacitance which allows a reduction of the energy-delay product up to 47% compared to planar integration due to simplified routing [2]. Also, the smaller overall wire capacitance allows a FETs to drive a greater number of logic gates without reaching the maximum capacitance that it can drive and as well allows a decrease of the coupling capacitance in between lines which reduce the noise. At chip level, stacking multiple device layer vertically enables partitioning the same circuit on multiple level which decreases the footprint of the chip. It also makes possible the integration on the same

chip of different channel material such as germanium or III-V materials [2]. At system level, 3D integration delivers very high interconnect densities which is required by high-performance processor (>10^5 pins/cm^2) [7].

3D integrated circuits (3DICs) are mainly studied through two approaches: 1. Three dimensional integration achieved through wafer stacking and through silicon VIA (TSV) interconnect; 2. Monolithic 3D integration.

1.2.1 Wafer Stacking Three Dimensional Integration

3D stacking is a top-down approach where multiple 2DICs are independently processed and then assembled to form a three dimensional circuits where metal lines run throughout the thickness of the structures to allow interconnection of multiple device layers: through silicon VIA (TSV). The chip stacking can be achieved through different schemes: package-to-package, die-to-die, die-to-wafer and wafer-to-wafer approaches. Package-to-package technology and die-to-die stacking allow selection of good die which increases the overall yield, but they suffer from a limited interconnect density which limit the increase in performance compared to classic 2D integration. Also, they require individual handling of the wafer which affect the cost [9]. Wafer scale integration approaches (i.e. wafer-to-wafer) allow TSV to be scaled by 20× which improves both bandwidth and overall performance of the system. On the other hand, it suffers from decrease in yield which can be limited by using circuits redundancy and fault tolerant techniques. Figure 1.1 illustrate the different integration methods which enable wafer-to-wafer integration. The face-to-back integration scheme requires bonding the top side of one wafer with the bottom side of the second wafer. Before bonding, the second wafer is thinned down to 20-50 μm by chemical mechanical polishing. In such scheme the number of interconnects running between the two wafers depends on the number of TSVs. Scaling the TSVs is necessary to achieve high bandwidth but depends on the aspect ration of the TSV diameter (D_{TSV}) to silicon thickness (T_{Si}). Therefore, by decreasing the silicon thickness it is possible

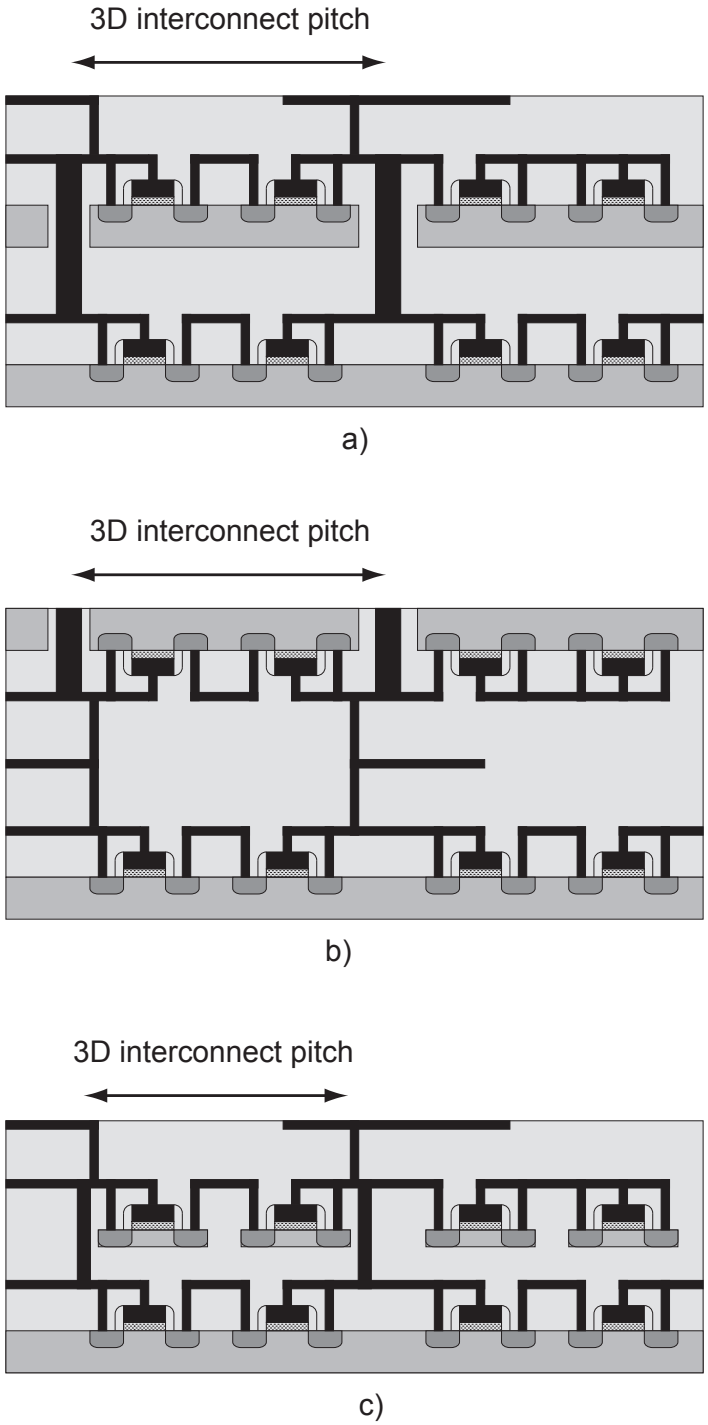


Figure 1.1: Cross-sections of the different wafer-to-wafer integration scheme: a) back-to-back integration approach; b) face-to-face; c) SOI based integration scheme. Adapted from [10] © [2004] IEEE.

to increase the interconnect density allowing much higher bandwidth. On the other hand, handling ultra thin wafers poses different mechanical challenges such as wafer warping which affects the strain in the devices and makes wafer alignment difficult. On the contrary, in face-to-face wafer bonding the number of interconnect between device layer is decoupled from the TSVs number, which allows achieving higher interconnect density. However, the improved number of interconnect is only achievable for two layers, while the interconnection of multiple layer is still limited by the TSVs number. A third approach is based on silicon on insulator (SOI) wafers, where the buried oxide (BOX) layer can be used as etching stop layer allowing complete removal of the silicon substrate after bonding the top surface to a glass substrate. Bonding to a glass wafer permits easier handling during the thinning process and achieves better alignment capability. The use of BOX layer as etching stop yield much thinner systems (overall thickness around 1-2 μm) which in turn increases the interconnect density and decreases their length improving the system bandwidth. However, there are some drawback associated with this technique, in particular the etching of the thick silicon substrate could lead to chemical contamination of the device layer which is now only protected by the BOX, and its removal could as well affect the strain in the devices [8]. Major challenges in the wafer stacking integration schemes include high-quality/low-temperature bonding (<400°C), good alignment, contact and process reliability and contact density. Above 400°C degradation of the back end of line (BEOL) stack, such as copper roughening, low-κ dielectric decomposition and drift of electrical performance, could compromise the integrity of the CMOS processed wafers.

1.2.2 Monolithic Three Dimensional Integration

Monolithic 3D integration is a bottom-up approach that does not require wafer stacking. This fabrication scheme is based on the sequential integration and interconnection of multiple device layers using standard CMOS technology. After integration of

the front end of line (FEOL) device (i.e. the first layer of devices which is integrated on the bulk silicon wafer or SOI wafer), additional layer of semiconductor material are deposited/bonded and devices integrated. This technique enables: 3D contact density close to the planar process one (VIA density up to 100 million/mm^2 projected using the 14nm node ground rules [2]); It allows excellent alignment precision since the alignment capability for such process is only tool-dependent; Reduction of total wires length (>10%) and reduction in the circuit footprint (∼30%) are also achieved for ASIC design [10]. One of the challenges of this approach is to deliver high performing circuitry on the additional semiconducting layers without requiring high temperature steps that would affect the FEOL circuitry.

There are different technique to fabricate the additional device layers: wafer bonding, solid phase crystallization, metal induced crystallization and excimer laser crystallization. Wafer bonding is a technique capable of delivering high performing circuitry thanks to the single crystal quality of the additional layer, but it drives up the cost of the integration process related to the bonding process. It differs from the wafer stacking process because of the lack of devices on the second wafer, which relax the constraint on the alignment. Solid phase crystallization and metal induced crystallization are two techniques which use high temperature step to improve the crystallinity of an amorphous semiconducting layer. The main advantage is the simplicity and low cost of this integration scheme. The amorphous layer can be deposited at room temperature, afterwards an annealing at elevated temperature improves the electrical conduction. On the other hand, this high temperature step affects both the FEOL devices and metal interconnect degrading their electrical and physical parameters. Excimer laser crystallization (ELC) is a technique which takes advantage of the short-duration/high-energy pulse of an excimer laser to quickly melt an amorphous layer deposited on top of a CMOS processed wafer. The laser is therefore able to quickly melt the top layer without letting enough time for the heat to reach the underlying circuit. ELC is a great technique which achieves good crystallinity while

meeting the thermal budget of BEOL stack. The detail of this technique will be discussed in Chapter 2.

1.3 Metal Oxide Semiconductor Field Effect Transistors

MOS Field Effect Transistors (MOSFETs) are among the most important device for Very Large Scale Integration (VLSI) of circuits. Figure 1.2 show a cross-section of a MOSFET. It is a four terminal device where the flow of the current between the source and drain terminals is modulated by the voltage applied to the gate and drain electrodes. The fourth terminal, body contact, can be used to modulate the threshold voltage of the device and is commonly referenced to the source terminal. In a traditional n-channel MOSFET the source and drain region are heavily n-doped to create a back-to-back p-n junctions with the p-body of the transistor. The p-n junctions block the current flow in either directions when the gate voltage is below a defined threshold. The gate electrode is capacitively coupled to the device channel through the gate dielectric, which does not allow current to flow from the channel to the gate. When the gate electrode is biased it attract either majority or minority carrier at the channel interface. In a n-channel MOSFET if V_{GS} is negative majority carrier (holes) are attracted at the opposite channel interface and the device enter its accumulation mode, where no current flow because of the back-to-back p-n junctions. When V_{GS} is positive minority carrier start accumulating on the channel and when the voltage is above the threshold voltage a continuous inversion layer between source and drain is formed and current can flow. Any further increase in gate voltage accumulates additional carrier in the channel at a rate determined by the capacitor relationship $Q_{CHANNEL} = C_{OX}(V_{GS}\text{-}V_T)$ where C_{OX} is the capacitance of the gate dielectric, V_t is the threshold voltage of the device and (V_{GS}-V_T) is the overdrive voltage. Assuming a fixed gate voltage, when a small drain voltage is applied to the device, electrons

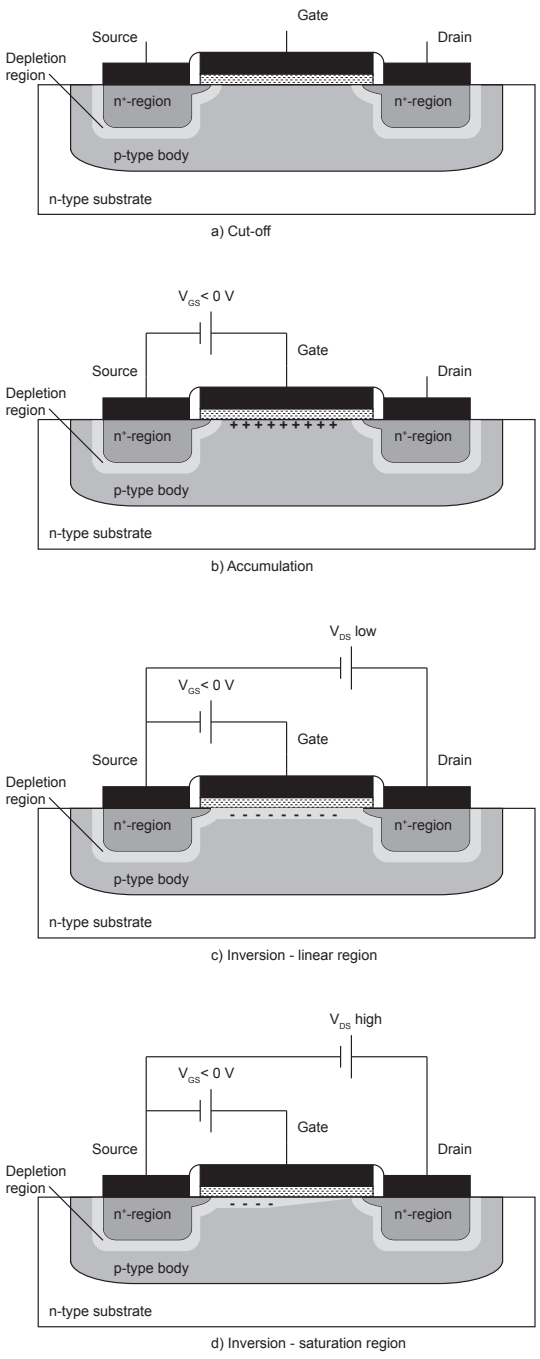


Figure 1.2: Conventional inversion mode n-channel MOSFET: a) Device in its equilibrium state; b) When V_{GS} is negative the device is in accumulation mode and does not conduct current; c) When V_{GS} is positive and above threshold value and V_{DS} is small the device is in inversion mode in linear region; d) When V_{GS} is positive and above threshold value and V_{DS} is above or equal to the overdrive voltage the device is in inversion mode in saturation region.

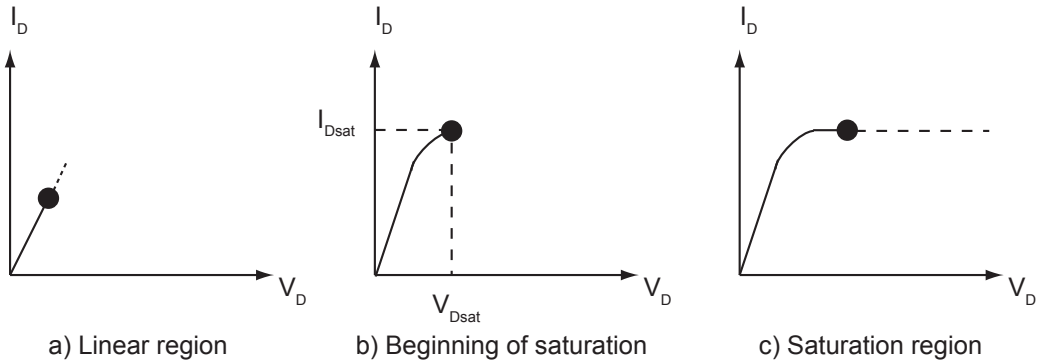


Figure 1.3: A schematic diagram of the operation mode of a MOSFET; a) I-V behavior in linear region when a small V_{DS} is applied; b) Onset of the saturation region; c) I-V behavior in saturation region. Adapted from reference [12].

flow from the source to the drain and the channel act as a linear resistor. This operation mode is called linear region and is schematically represented in figure 1.2c and its I-V characteristic in figure 1.3a. Upon increasing the V_{DS} voltage the field generated by the drain voltage begins to cancel the field applied by the gate and the inversion layer narrows. This reduces the rate at which the drain current increase, figure 1.3b. As V_{DS} keep increasing the inversion layer keep narrowing until it reaches the pinch-off point when its thickness became zero. After this point the current stop increasing with the voltage and the device enter its saturation region, figure 1.2d and figure 1.3c. Figure 1.4 summarize the device trans-characteristic, which is the current output at the variation of the gate bias for fixed drain biased and the device output characteristic, which is the current output at the variation of the drain bias for different applied gate bias.

Depending on the different region of operation the current in the transistor is usually described by a different set of equation:

- *Cut-off* region. When $V_{GS} < V_T$ no current flows in the transistor because of the back-to-back p-n diodes and the current can be simply written as:

$$I_D = 0[A] \tag{1.1}$$

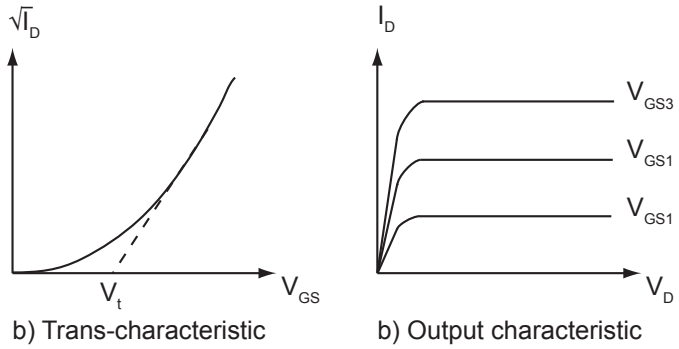


Figure 1.4: a)Trans-characteristic curve of a n-channel MOSFET. b) Output characteristic of a n-channel MOSFET. Adapted from reference [13].

- *Linear* region. When $V_{GS} > V_T$ and $V_{DS} < (V_{GS}\text{-}V_T)$ the current increase proportionally to the increase in V_{DS}:

$$I_D = \frac{W}{L}\mu C_{OX}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS} \tag{1.2}$$

- *Saturation* region. When $V_{GS} > V_T$ and $V_{DS} > (V_{GS}\text{-}V_T)$ pinch-off occurs and the current saturates at the value:

$$I_D = \frac{1}{2}\frac{W}{L}\mu C_{OX}(V_{GS} - V_T)^2 \tag{1.3}$$

Where W/L are the geometrical width (W) and length (L) of the MOSFET channel and μ is the field effect mobility of the carriers.

1.4 Junction Field Effect Transistor

Junction Field Effect Transistor (JFET) is a device which use the depletion region of two p^+-n junction reverse biased to control the current flowing between two terminals. Figure 1.5 shows the schematic cross-section of a JFET: it is a four terminal device where the current flow between the source and drain terminal is modulated by the variation of the depletion width controlled by the bias applied at the gate and drain electrodes.

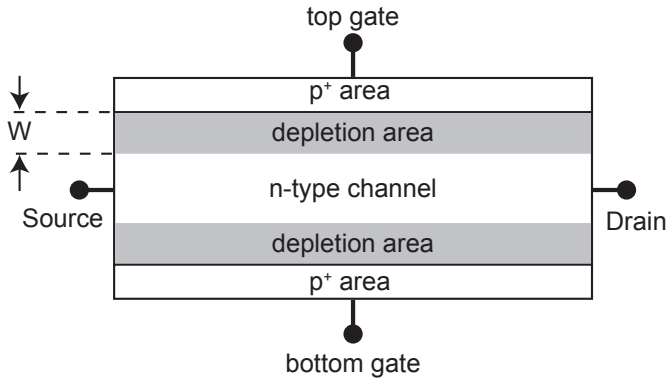


Figure 1.5: Cross-section of a JFET device.

Figure 1.6 illustrate how the voltages applied on the device modulates the dimension of the depletion width and the resulting electrical characteristic. The top and bottom p^+-n junction need to be reverse biased so that most of the current flows from the source terminal to the drain one. When the voltage applied on the drain terminal is low, a little current flows from the two terminal proportional to V_{DS}/R, where R is the channel resistance and V_{DS} is the voltage applied across the drain/source terminals, figure 1.6a. But, as the voltage on the drain increases, the depletion width of the two p-n junction increase and the channel available for conduction narrows, so that the rate of increase of the current actually decreases. If the drain voltage keep increasing, the two depletion regions will join each other at the pinch-off point, condition shown in figure 1.6b. As the drain voltage further increase, after the pinch-off point is formed, there is no increase in drain current and the device stays in the saturation region, figure 1.6c. As seen already in the case of the MOSFET, also for the JFET depending on the region of operation its behavior is described by a different set of equation:

- *Linear* region. For small V_{DS} the current increases proportionally with the increase in V_{DS}:

$$I_D = I_P[\frac{V_{DS}}{V_P} - \frac{2}{3}(\frac{V_{DS} + V_{GS} + V_{bi}}{V_P})^{3/2} + \frac{2}{3}(\frac{V_{GS} + V_{bi}}{V_P})^{3/2}] \qquad (1.4)$$

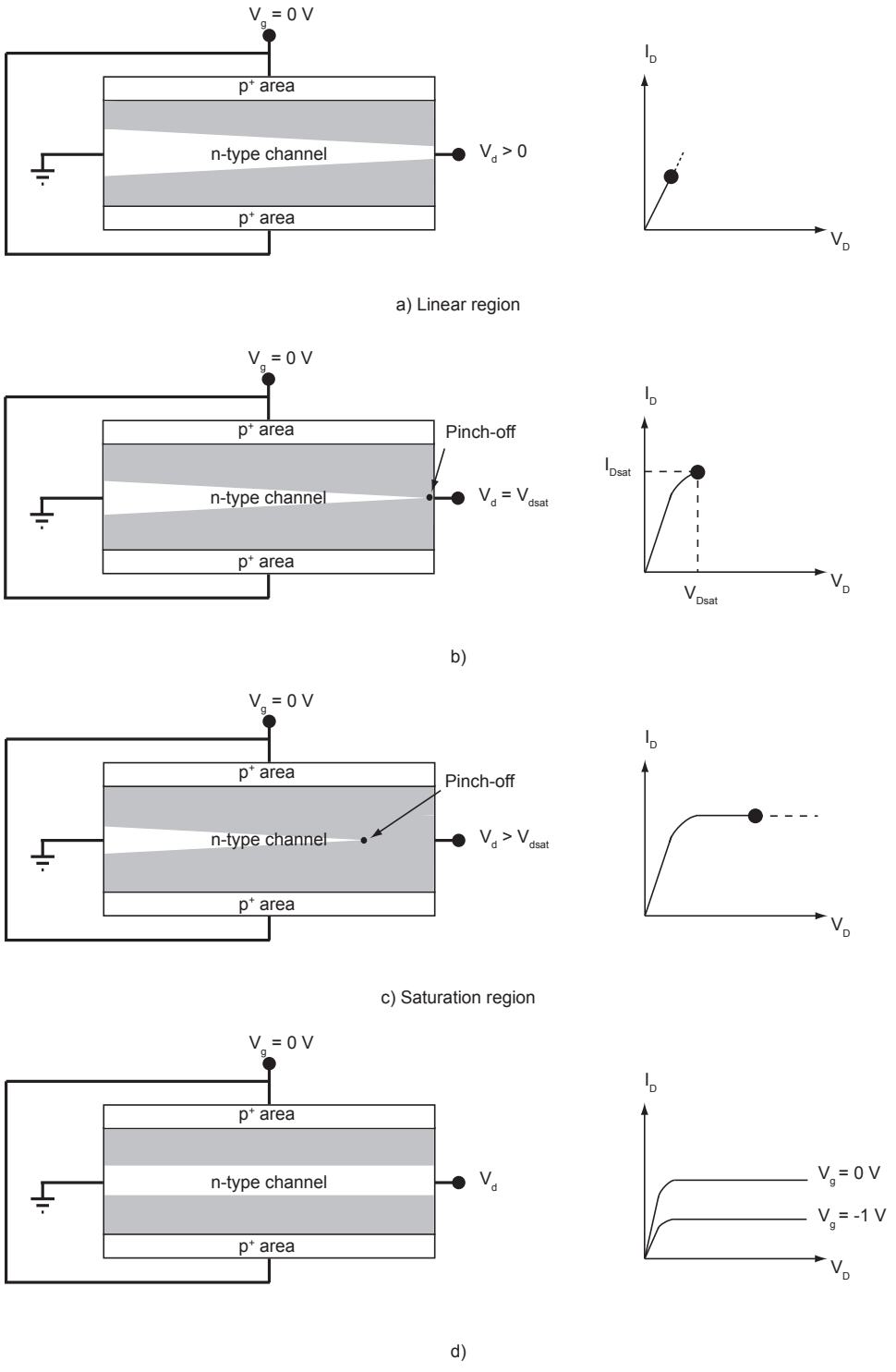


Figure 1.6: Modulation of the depletion width in the channel depending on the voltages applied and electrical characteristic. Adapted from reference [12].

$$I_P = \frac{W\mu q^2 {N_D}^2 a^3}{\epsilon_s L} \tag{1.5}$$

$$V_P = \frac{qN_D a^2}{2\epsilon_s} \tag{1.6}$$

where W is the channel width, L the length, 2a is the total thickness of the n-type region, ϵ_s is the relative dielectric constant of the channel material, N_D the channel doping, q the elementary charge and V_P is the voltage necessary to apply on the drain to achieve pinch-off.

- *Saturation* region. For V_{DS} above V_P pinch-off occurs and the current saturates at the value:

$$I_D = I_P[\frac{1}{3} - (\frac{V_{GS} + V_{bi}}{V_P}) + \frac{2}{3}(\frac{V_{GS} + V_{bi}}{V_P})^{3/2}] \tag{1.7}$$

1.5 Polycrystalline Silicon Thin-Film Transistors

The focus of this thesis is on enabling excimer laser crystallization of silicon (Si) deposited in its amorphous phase in the BEOL of wafers. The material resulting after excimer laser crystallization is a polycrystalline silicon material (polysilicon), which is characterized by the presence of grain boundaries separating different grains as opposed to mono crystalline silicon (c-Si) which is a continuous defect free single crystal layer of silicon. Grain boundaries are planar defects in the crystal structure which separate individual single crystal area. Grain boundaries have a high concentration of dangling bonds which presence, because of their highly reactive nature, lead to a reduction of the electrical properties of the devices integrated in such material. Dangling bonds usually cause deep state in the middle of the bandgap of the semiconductor which acting as trapping state increase the recombination rate of carriers in the material affecting the current behavior in the polysilicon thin-film transistors (TFTs). Figure 1.7 schematically represent the regions in a polycrystalline material, charge distribution and band diagram. A comprehensive model of the electrical conduction in a polycrystalline material was first described by Seto in [11] and further refined

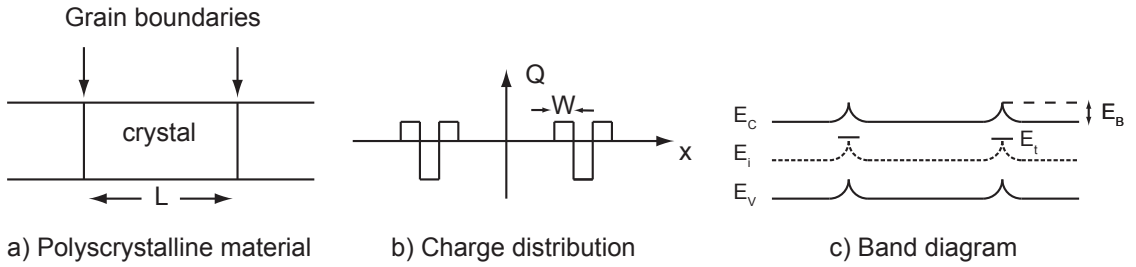


Figure 1.7: a) Schematic representation of the grain boundaries in polysilicon; b) Grain boundaries effect in the charge distribution; c) Grain boundaries effect in the band diagram.

by Baccarani in [12]. It assumes that: 1. the material is composed of an identical chain of grains separated by grain boundaries which thickness is negligible compared to the dimension of the crystal; 2. The grains boundary contain a concentration of traps N_t per unit area located at energy E_t with respect to the intrinsic Fermi level; 3. There is a concentration of shallow donor which are uniformly distributed and totally ionized. The current in a polycrystalline material can then be described through a grain boundary trapping model where the carriers need to overcome the potential barrier associated with the grain boundaries through thermionic emission [13; 14; 15; 16], figure 1.7c. The barrier at the grain boundaries is associated to a depletion region which form due to the trapping of carrier at the interface and can be written as:

$$E_B = \frac{q^2 W^2 N_g}{8\epsilon} \tag{1.8}$$

The barrier height depends on the carrier concentration: at low concentration, the number of trap states is higher than the one of carriers, therefore more carriers are trapped at increasing concentration and the barrier height increase; at high concentration, the grains are partially depleted, therefore both the width of the depletion region and the barrier height decrease with increasing doping concentration [17]. Based on the grain boundary trapping model the current in a polycrystalline semiconductor

can be written as:

$$I_D = \frac{W}{L}\mu C_{ox}(V_{GS} - V_T)V_{DS}\exp(\frac{-qV_B}{kT}) \tag{1.9}$$

Starting from this model, Levinson in [18] shows that the current of a TFTs in a polycrystalline material can be expressed directly as a function of the trap density in the material:

$$I_D = \frac{W}{L}\mu V_{DS}C_{ox}\exp(\frac{-q^3N_t^2t}{8\epsilon kTC_{ox}V_{gs}}) \tag{1.10}$$

Where q is the elementary charge (1.602×10^{-19} C), k is the Boltzmann's constant (1.381×10^{-23} J/K), T is the temperature and N_t is the trap concentration in the material in cm^{-2}.

1.6 Scope of this Research

The aim of this work is to validate laser crystallization as a way to achieve monolithic 3D integration of devices in the BEOL of wafers. Figure 1.8 illustrate a standard BEOL wafer. The copper interconnect are distributed over different layer. Because the resistance of the interconnect lines is a function of their dimension, small lines (higher resistance) are used to connect nearby devices, which ensure a small signal propagation delay (RC constant) because of the short distance. Larger copper lines (lower resistance) are used to connect distant device at reasonable time constant. When two copper lines on different layer intersect they form a parasitic capacitance which affect again the signal delay. To reduce this capacitance low-κ dielectric are used as inter-layer passivation. However, the copper/low-κ stack can only withstand temperature below 400 °C.

To demonstrate that ELC is a reliable and uniform process for VLSI monolithic 3D integration, this thesis focuses on three key aspects of the fabrication process:

1. Excimer laser crystallization of silicon deposited on low-κ dielectric, and comparison of the material morphology and texture with the one achieved on SiO_2 thermal buffers.

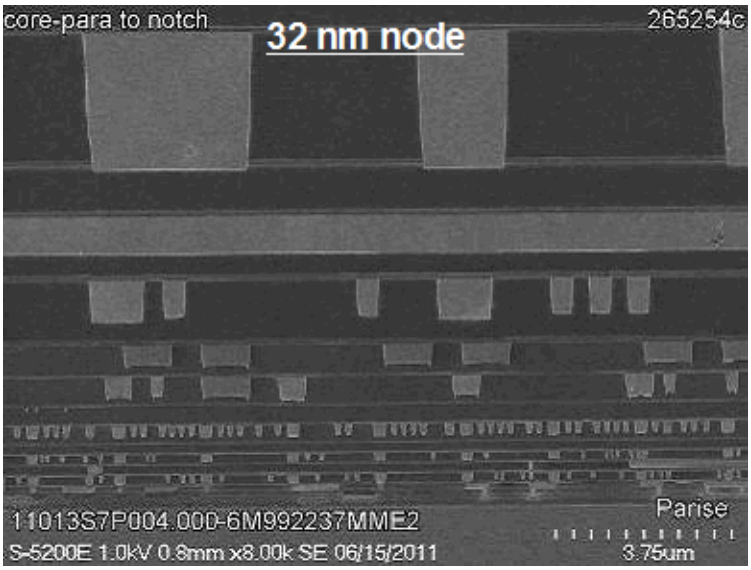


Figure 1.8: Cross-section of an back end of line processed wafer. Copper lines are distributed over different layer to connect the different devices process in the front end of line. Low-κ dielectric is used in between copper lines as passivation layer.

2. Excimer laser crystallization of silicon deposited on BEOL processed wafer, and investigation of the effect of the laser process on the copper lines.

3. VLSI of TFTs on excimer laser crystallized silicon, and investigation of the device performance and uniformity.

1.7 Organization of this Thesis

Chapter 2 presents the specific techniques used to crystallize the amorphous silicon, briefly discusses the available techniques for the amorphous silicon deposition, and presents a base model for the finite element simulation which will be expanded in the following chapters for particular cases. Chapter 3 discusses the laser crystallization of silicon when deposited on low-κ dielectrics and compare it when crystallizing on SiO_2 dielectrics. Finite element method simulations are used to study the temperature

evolution in the wafer stack during laser exposure. SEM, AFM, Raman and XRD demonstrate that the microcrystalline structure in the two systems are equivalent. The same chapter presents the crystallization on Cu integrated wafer. It adapts the thermal model developed in chapter 2 to the wafer stack under study and presents experimental result of the laser exposure and electrical characterization of the buried copper lines. Chapter 4 discusses the TCAD simulation that are used to define the fabrication process of devices required to meet given target parameters. Finally, chapter 5 covers the monolithic VLSI TFTs study. Starting from technology computer aided design it develops a fabrication process which is carried out in 200 mm wafers and discusses the characterization of the integrated device.

Chapter 2

Excimer Laser Crystallization of Silicon Thin Films

2.1 Introduction

As discussed in Chapter 1, the performance of polycrystalline devices are directly affected by the microcrystalline structure of the material in which they are integrated. Different ways of achieving a polycrystalline material on top of a general substrate exist. Approaches such as solid phase crystallization or metal induced crystallization usually require a combination of relatively high-temperature/short-time or long-times/low-temperature to achieve sufficiently large grain polysilicon. At a glass-substrate compatible temperature of 600 °C the crystallization could take tens of hours to be completed [19]. Moreover, films crystallized through solid phase crystallization technique are characterized by high intra-grain density, which limit the performance of devices [19]. On the contrary, laser crystallization of amorphous silicon is a pulsed laser technique which achieves large grain polycrystalline material through a low temperature process [20; 21; 22; 23] at fast timescale.

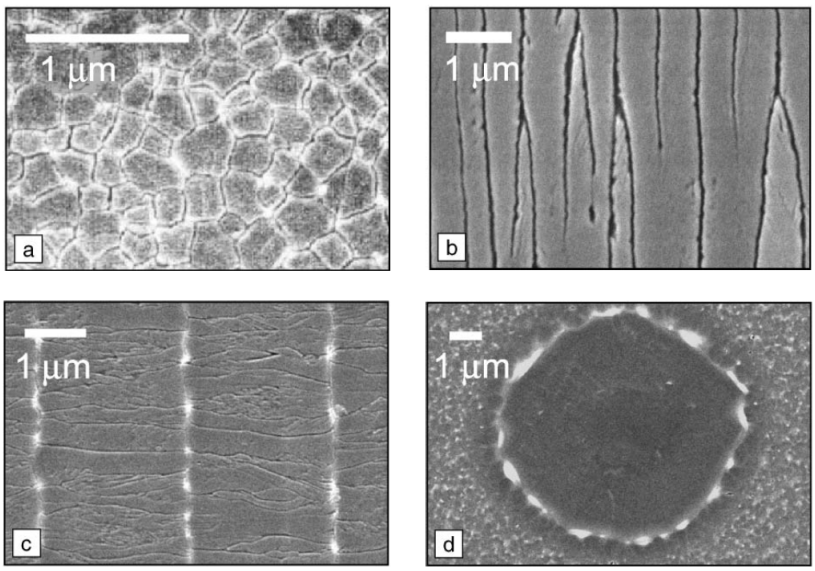


Figure 2.1: Scanning electron microscopy of defect-etched Si films showing different polysilicon microstructure achieved with different pulsed-laser techniques: a) excimer-laser annealing; b) line-scan SLS; c) two-shot SLS; d) dot-SLS [22].

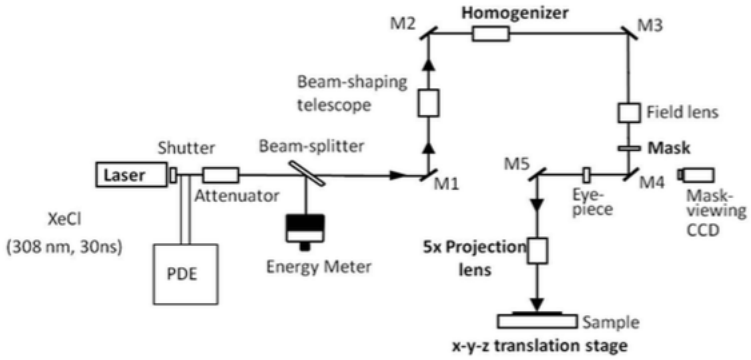
2.2 Sequential Lateral Solidification

Figure 2.1 report the comparison between different pulsed laser crystallization techniques. Excimer laser annealing (ELA) technique, Figure 2.1a, relies on a narrow laser energy window where the super lateral growth (SLG) phenomenon can be triggered [24; 25]. SLG yield a large grain polysilicon material as result of a nearly-complete thin-film melting, which leaves few isolated solid clusters located at the bottom of the liquid material from which grain growth is triggered. Unfortunately, the processing window for this technique is very narrow resulting unpractical for manufacturing purposes: a small variation of the laser energy above the thin-film full melt threshold could completely melt the solid clusters resulting in random nucleation yielding a small grain polysilicon. Sequential lateral solidification (SLS) is a particular crystallization technique, based on pulsed-laser. It was developed in the 1990s to overcome the limited performance of amorphous silicon TFTs used in the dis-

play industry as driving devices [26], providing a manufacturing robust process. SLS achieves super lateral growth by controlling the shape and area of the film completely melted by the laser [24; 25]. This way it achieves a directionally solidified microstructure which grains are non-equiaxed and have an overall low defect density [26; 27; 28]. Figure 2.1 presents three different kind of SLS: line-scan SLS; two-shot SLS and dot-SLS. This work relies mainly in the line-scan and two-shot methods to achieve crystallization of thin a-Si layer.

Figure 2.2 illustrates the Microlas laser setup in the Material Science Department at Columbia University, where the crystallization part of this work is carried out. The general working scheme of the line-scan and two-shot SLS processes is an iteration of two steps: 1) irradiation of a defined area of the film to achieve complete melting; 2) translation of the substrate. Figure 2.3 illustrate the crystallization process in more details. It start with patterning the laser beam in a rectangular aperture using a photolitographic mask with dimension that depends on the desired technique. The laser in the Microlas setup is a XeCl with a wavelength 308 nm and a pulse full width half maximum (FWHM) of 30 ns extendable to 220 ns through the use of a pulse extender. The first pulse completely melt the irradiated area which is usually around 4 to 7 microns wide and can have a length up to 5 cm depending on the technique, step 1 in figure 2.3. Upon cooling, lateral growth proceed from the lateral unmelted region toward the middle of the molten area, step 2 in figure 2.3. The lateral growth process stops when either the two opposite growth fronts meet at the center of the irradiated area or when the molten silicon become sufficiently supercooled that random nucleation occurs at the center of the area. The width of the irradiated area has a direct effect on which of this two scenario happens. While in the line-scan SLS it is possible to erase the random nucleation in the material with the following shot, in two-shot SLS is important that the two front meet in the middle to obtain a good quality material. The next step (step 4 in figure 2.3) involves a micro-translation of the stage before the second shot melts a new area. Depending on the translation

(a)



(b)

Figure 2.2: Microlas laser setup. a) Photograph of the SLS system used. b) Diagram of the laser system [32].

step size either line-scan SLS or two-shot SLS can be achieved. In line-scan SLS the translation step is smaller than half of the beam width, this allows the lateral growth during the second shot to template from the structure obtained during the first shot, elongating the grains. This technique results in a river like structure with indefinitely long grains, but it is affected by a low throughput and localized grain texture which can affect the device uniformity [29]. In two-shot SLS the stage is translated by little less than a full beam-width, this way the second shot achieves a polycrystalline morphology similar to the one achieved during the first shot, separated by grain boundaries. Even though the two-shot material can offer better device uniformity [29; 30] and higher throughput, it yields a material with lower mobility due to the higher number of grain boundaries. Figure 2.4 shows the SEM micrographs of the defect Secco etched polysilicon obtained with the two different SLS techniques in the Microlas setup.

2.3 SLS on Physical Vapor Deposited Silicon

Enabling SLS technique to achieve 3D monolithic integration in the BEOL of wafers requires meeting a tight thermal budget on the processes necessary for TFTs integration. SLS techniques are common in the display industry where the temperature limit is set at 600 °C due to the glass substrate; but, as described in chapter 1, the BEOL stack is composed of subsequent layers of Cu interconnect and inter-layer dielectrics, which cannot withstand temperature above 400 °C.

The typical wafer stack for SLS crystallization is an active layer of Silicon, on top of a thermal buffer, which is most commonly SiO_2. The silicon layer when processing on top of quartz or glass substrate can be deposited through a number of techniques. Low pressure chemical vapor deposition (LPCVD) allow deposition of silicon from a silane (SiH_4) or disilane (Si_2H_6) precursor at temperature of 550 °C or 470 °C respectively. Plasma enhanced chemical vapor deposition (PECVD) allows deposition of

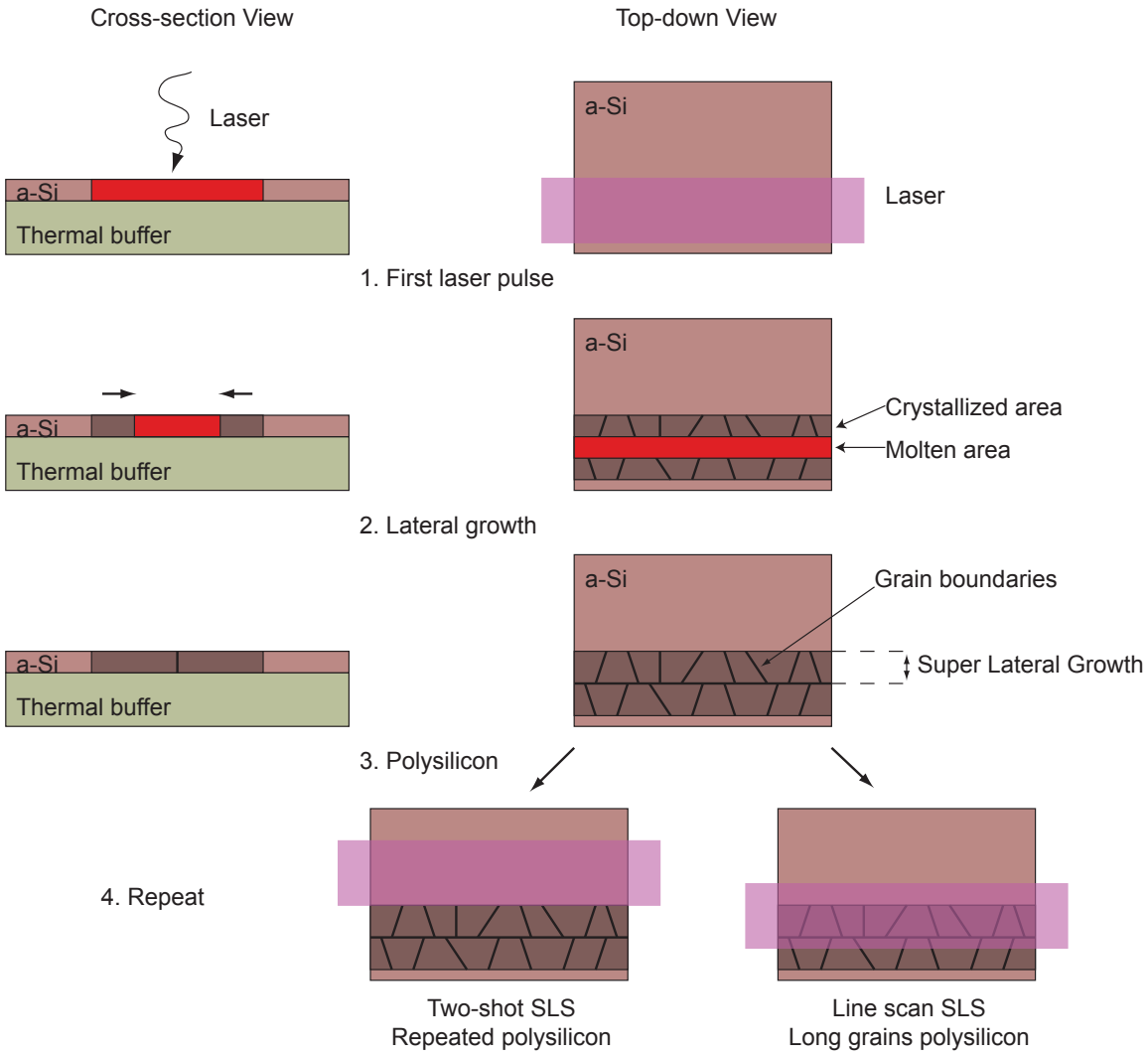
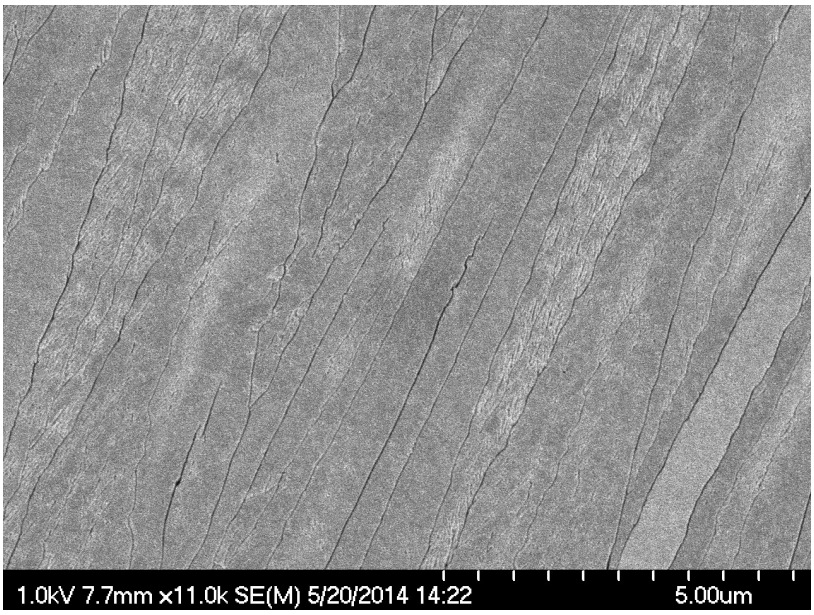
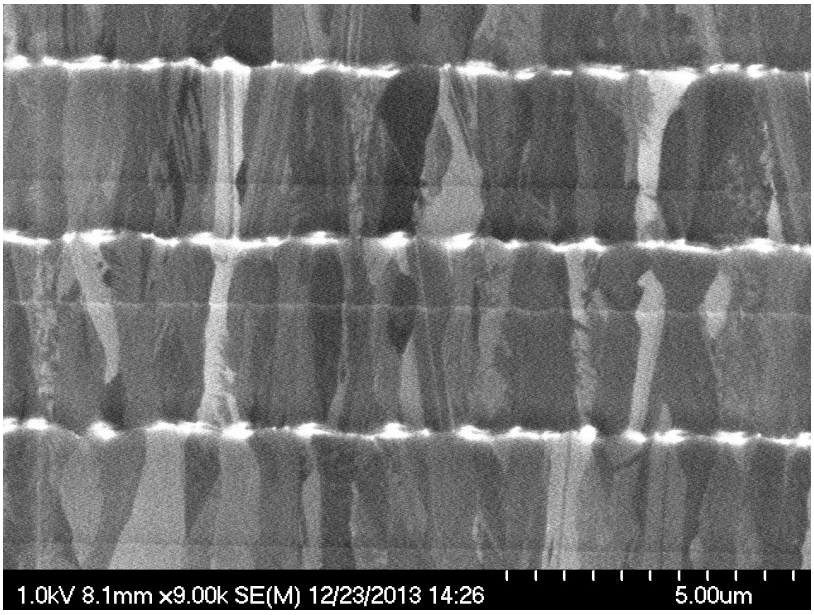


Figure 2.3: A schematic representation of the sequential lateral solidification (SLS) process. Left column is the cross-section of the process while the right column represents the top-down view.



(a)



(b)

Figure 2.4: SEM micrograph of the defect Secco etched polysilicon obtained through SLS process with the Microlas setup: a) line-scan SLS; b) two-shot SLS.

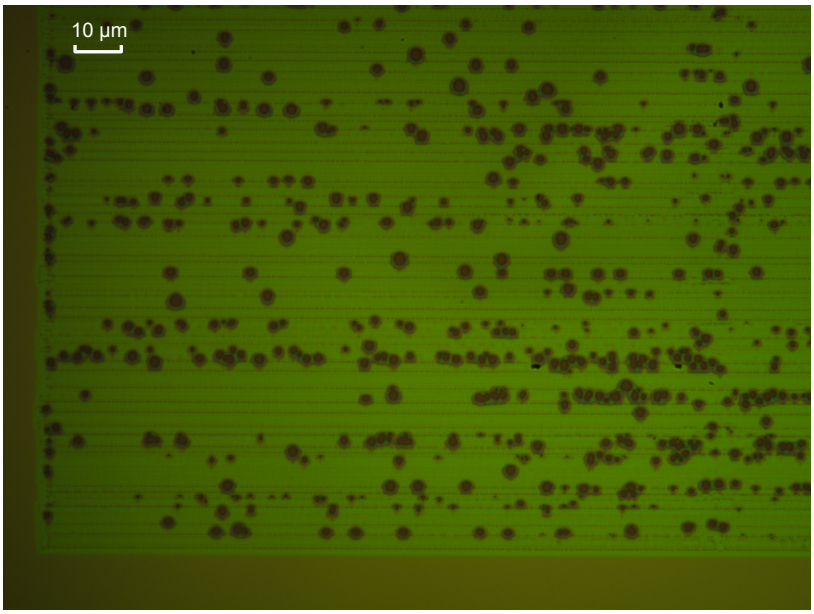
an amorphous silicon layer at temperature around 300 °C. However films deposited by PECVD have an high hydrogen content (above 10 atom % [31]) which can lead to film ablation upon laser exposure due to the explosive release of hydrogen. An established way of dehydrogenating the silicon film prior to laser exposure is by furnace annealing at 500 °C, resulting incompatible with BEOL wafers, or by lower laser energy exposure [32].

Physical vapor deposition (PVD) methods can be used to achieve deposition of silicon thin-film at substantially lower temperatures. In particular we used PVD sputtering to deposit 100 nm of a-Si on top of 1 μm of SiO_2 thermal buffer on a 200 mm wafer. Crystallization of such material only required annealing of 350 °C to ensure material crystallization without damage, providing a process compatible with the BEOL stack. Figure 2.5 shows the silicon layer exposed to the SLS process as deposited and after annealing at 350 °C.

2.4 One-dimensional Finite Element Method Simulation

Crystallization of silicon on BEOL integrated wafers is a major challenge due to the low thermal variation that the Cu-interconnect and low-κ dielectrics can withstand. Pulsed lasers with short wavelength and short pulse duration achieves the full melt of the silicon layer without compromising the stability of the buried layers. Finite element method (FEM) simulation is a great tool to study the effect of different thermal buffers and stack composition on the temperature evolution during the irradiation process. Based on the approach by Förster and Vogt [33] we developed a model that will be extensively used throughout this work and adapted to the different cases under study.

During the irradiation process, the laser beam irradiating the samples is relatively homogeneous and the lateral dimension of the irradiated area can be bigger than the



(a)

(b)

Figure 2.5: Micrograph of the Si thin-film after excimer laser exposure on: a) as deposited thin-film; b) thin-film annealed at 350 °C for 30 minutes after deposition.

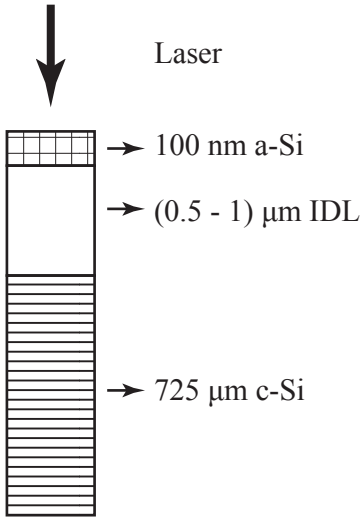


Figure 2.6: Wafer structure used in the FEM laser simulation. The top layer is 100 nm of a-Si on 1μm of SiO_2 on 725 μm of Si substrate. The laser beam irradiates the top surface perpendicularly for 30 ns, and the temperature evolution is measured for 5 μs.

vertical dimension of the structure (up to 1.5 mm by 1.5 mm) which allow to reduce the problem to a one dimensional model. The simplest structure under study is a three layer structure: 100 nm of amorphous silicon, 1 μm of SiO_2; and 725 μm of Si substrate. Upon irradiation heat accumulates on the top silicon layer following the law:

$$\frac{\partial T}{\partial t} = \frac{\alpha}{\rho \cdot C_p} I(x,t) + \frac{1}{\rho \cdot C_p} \frac{\partial}{\partial t}(\kappa \frac{\partial T}{\partial t}) \tag{2.1}$$

where I(x,t) is the power density of the laser at a depth x from the surface and time t, T is the temperature, and ρ, C_p, κ and α are respectively the density, specific heat, thermal conductivity and absorption coefficient of the material. The power density of the laser at a certain depth is expressed by:

$$I(x,t) = I_0(t) exp(-\alpha \cdot x)(1 - R) \tag{2.2}$$

Table 2.1: Material parameters of the a-Si thin film when in the solid and liquid phase [36].

Parameters	**Expression**	**Description**
κ_{a-Si} [W cm^{-1} K^{-1}]	$(1.3\times10^{-11}$(T-900)^3 $+1.3\times10^{-9}$(T-900)^2 $+1.0\times10^{-6}$(T-900) $+1.0\times10^{-2})$	Thermal conductivity of a-Si
$C_{p,a-Si}$ [J g^{-1} K^{-1}]	(0.1711·T/1865 +0.952)	Heat capacity of a-Si
$T_{m,a-Si}$ [K]	1440	Melting point of a-Si
ρ_{a-Si} [Kg m^{-3}]	2260	Density of a-Si
$R_{a-Si,s}$	0.58	Reflectivity of solid a-Si
$R_{Si,l}$	0.72	Reflectivity of liquid Si
α_{a-Si} [cm^{-1}]	$1.75{\cdot}10^{+6}$	Absorption coefficient of a-Si

where I_0 is the impinging power density and R is the reflectivity of the material. As the top silicon layer heats up, it transitions from a solid state to a liquid one. To accurately model the heat accumulation and transfer in the simulated stack, it is necessary to consider the variation of the amorphous silicon properties when transitioning from the solid to the liquid state. This can be done by expressing all the variable affected by phase transition through a sum of therm following the form:

$$A \cdot (1 - H(t)) + B \cdot H(t) \tag{2.3}$$

A and B represent the variable value when the material is in its solid state or liquid state and H(t) is a smoothed step function centered at the melting point of amorphous Si. Table 5.1 list the value of the material parameters used in the simulation.

Figure 2.7 shows the simulated temperature of the top silicon surface layer after

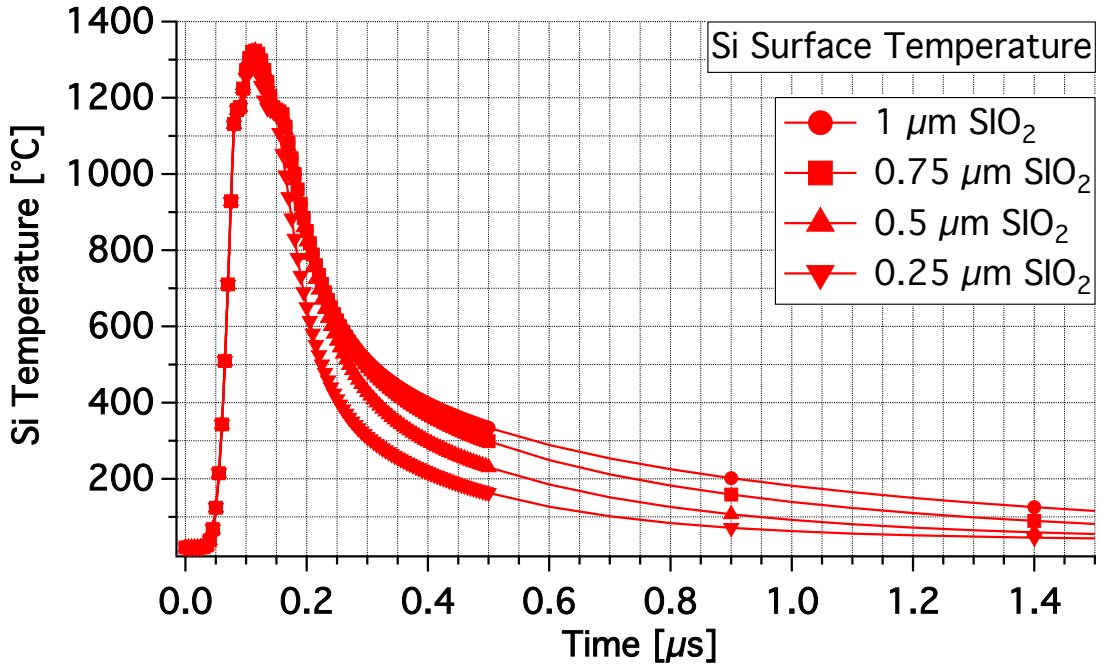


Figure 2.7: Simulated temperature of the silicon film surface during laser process. The temperature quickly reaches the melting temperature of the amorphous silicon and cool down below 200°C after 0.9 μs.

a laser pulse centered at 100 ns and with a 30 ns width irradiates the wafer. Upon irradiation the top layer quickly reaches the amorphous silicon melting temperature ($\sim$ 1167) where a plateau can be observed. This is related to the transition of the material properties from the solid to liquid phase. The cooling ramp is affected by the thickness of the thermal buffer underneath the Si thin film and for the thicker dielectric, the material reaches a temperature below 200°C after 0.9 μs. The repetition rate used in the experiments reached a maximum of 30 Hz which is a shot every 33 ms, plenty of time for the material to go back to room temperature before the next shot, avoiding accumulation of heat at each shot.

2.5 Conclusion

Sequential lateral solidification is a technique capable of crystallizing thin film on temperature sensitive substrates. Monolithic integration in the BEOL of wafers requires tuning of the integration process to meet the thermal constrain. Usual deposition technique such as LPCVD and PECVD are either above the thermal limit or require annealing step above it. PVD deposition through argon sputtering proved to be a suitable technique which require processing temperature below 350 °C, resulting compatible with Cu and low-κ integrated wafers. Finite element method simulation can be used to explore the temperature variation within the crystallized stack. We defined a base model which takes into account the variation of the properties depending on the phase of the silicon layer. This model will be further explored to study the temperature variation on different interfaces depending on the thermal buffer material and thickness.

Chapter 3

Excimer Laser Crystallization on Back End of Line low-κ/Cu Integrated Wafers

3.1 Introduction

Back end of line is the second portion of the fabrication of integrated circuits, through which the individual component integrated in the front end of the line, are interconnected. Figure 3.1 illustrates a wafer where the FEOL devices are interconnected through BEOL stack: a sequence of multilayer structure where patterned metal lines are buried in inter-layer dielectrics (ILD) and run throughout the wafer. It is a hierarchical structure where the bottom lines (the one closer to the device layer) have the smaller dimension and connect nearby devices, while the upper lines have the larger dimension and interconnect the far edges of the die. The speed of an electrical signal in a complete IC circuit is given by the contribution of two components: the transistor gate delay and the RC delay. The RC delay is the signal propagation time across a metal line connecting different devices. To estimate this delay, to each of the line running throughout the die area is associated a resistance, and to each of

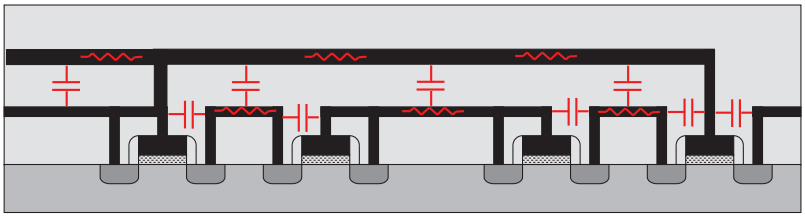


Figure 3.1: Interconnect lines in a BEOL integrated wafer. In red are represented the lump parasitic component which characterize multilayer metal structure: resistance of the line (R) and parasitic capacitance (C_{par}) used in equation 3.1 to estimate the signal delay.

the metal line crossing another line at different metallization layer is associated a parasitic capacitance. The combination of the resistance and the capacitance affects the signal delay:

$$\tau = R \cdot C_{par} = 2\rho\kappa\epsilon_0(\frac{4L^2}{P^2} + \frac{L}{T^2}) \tag{3.1}$$

where ρ is the metal resistivity, κ the relative dielectric constant of the ILD, ϵ_0 is vacuum permittivity, L is the line length, P is the metal pitch and T is the metal thickness. Figure 3.2 shows the comparison of the different delays and their sum in an IC circuit. As the dimension of the metal lines and devices in a circuit shrink, the RC delay becomes the dominant factor and limits the operating frequency of the circuit [34]: this is mainly due to the increase of line resistivity. Originally the BEOL of circuits was composed of aluminum (Al) lines buried in SiO_2 dielectrics, but to further decrease the signal delay, industry moved to a stack made of copper lines and low-κ passivation layer to take advantage of the reduced resistivity and parasitic capacitance. Therefore, to enable ELC for advanced monolithic 3D integration it is necessary to explore such crystallization technique on BEOL Cu/low-κ integrated structures.

One limitation to 3D integration in the BEOL is the thermal budget of the metal

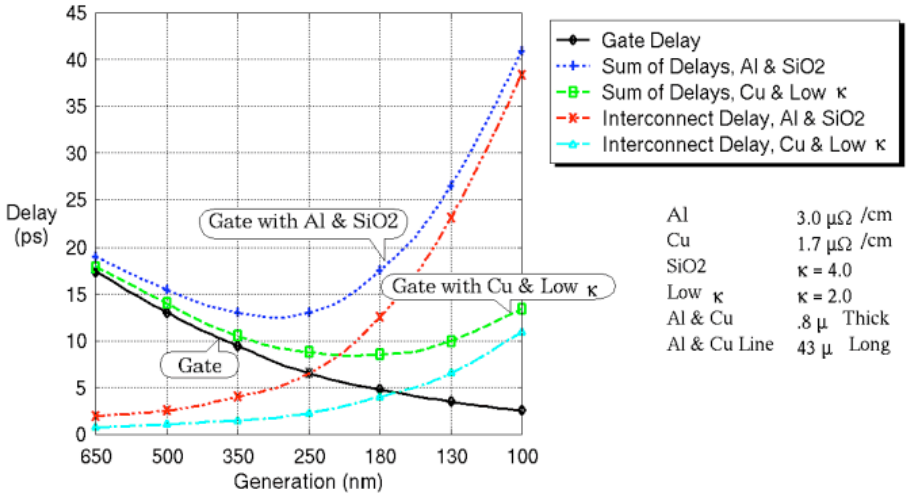


Figure 3.2: Interconnect delays versus gate delay and their sum for different BEOL materials [38].

interconnect and low-κ dielectrics. Integration in the BEOL process has a stringent thermal budget requirement, which limits the substrate temperature below 400°C. Above 400°C, Cu interconnect roughening, SiCOH dielectric decomposition, silicide contact changes and other degradation mechanisms are all accelerated. While other techniques to deposit polysilicon layers exist, such as solid phase crystallization and metal induced crystallization, they require applying the same high temperatures to the whole wafer stack, which is impractical for monolithic 3D integration. ELC of amorphous silicon is an efficient way to achieve good quality polysilicon while meeting the BEOL thermal budget requirements.

This chapter explores the use of excimer laser process on amorphous silicon deposited on low-κ dielectric and the effect of the laser exposure on the electrical properties of the buried copper lines.

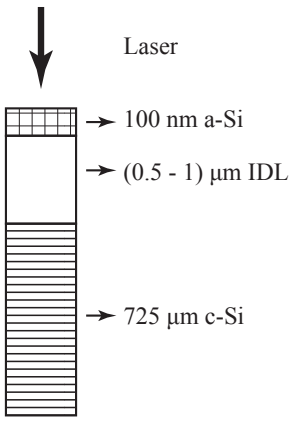


Figure 3.3: Wafer structure fabricated for studying the compatibility of low-κ substrates with the excimer laser crystallization process. Three wafers include a SiO_2 thermal buffer at three different thicknesses, while other three present a low-κ thermal buffer (i.e. SiCOH with $\kappa = 3.0$). This same structures are used in the FEM simulations.

3.2 Excimer Laser Crystallization of a-Si on low-κ Dielectrics.

To explore the possibility of crystallizing the a-Si thin film on low-κ dielectrics we start from studying six different silicon wafers; figure 3.3 shows the fabricated structure which is also used in the simulation. On three wafers SiO_2 dielectric are deposited at different thicknesses (1 μm, 0.75 μm and 0.5 μm), and the other three have a low-κ dielectric of the same three thicknesses. The low-κ dielectric material has a dielectric constant of 3.0 and is deposited by plasma enhanced chemical vapor deposition in a 200 mm chamber. The material is an organosilicate glass with a network structure of Si-O bonds and pendant Si-CH_3 groups, also referred to as a SiCOH dielectric: a standard material in the BEOL integration. As mentioned in Chapter 2, different deposition technique for a-Si exists, among these the PVD sputtering can be used to deposit a-Si thin film while keeping the process temperature below the thermal

Table 3.1: Material parameters of the SiCOH and SiO_2 based dielectric.

Parameters	**SiCOH**	**SiO_2**
Dielectric constant [ ]	3.0	3.9
Thermal conductivity [W m^{-1} K^{-1}]	0.4	1.4
Density [g cm^{-3}]	1.4	2.2
Heat capacity [J K^{-1} g^{-1}]	0.636	0.730

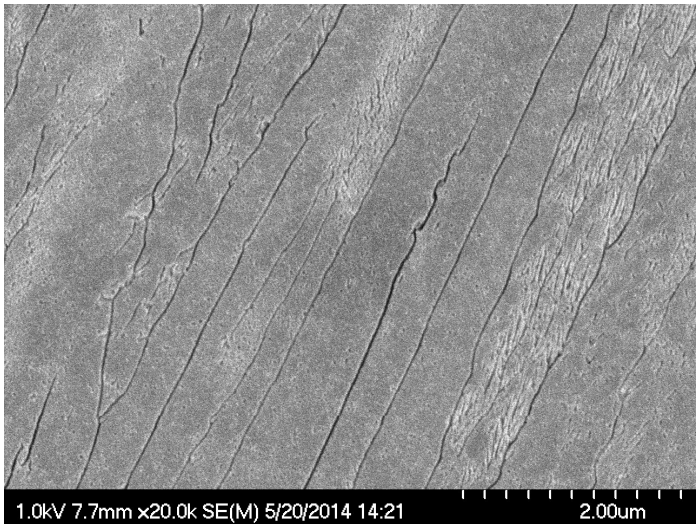
budget. After depositing 100 nm of a-Si, in order to drive out any trapped gas, all of the wafers are annealed at 350°C for 30 minutes, before further processing. This set of experiments use the line-scan SLS to crystallize the amorphous film, which as shown earlier, results in longer grains with a river like structure.

The described structure is implemented in FEM simulation which expanding from model introduced in Chapter 2 take into account the different thermal buffer materials and thickness. Table 3.1 lists the physical parameters of the dielectrics used in the simulation. While the density, thermal conductivity, and dielectric constant of the SiCOH correspond to measured values [35; 36], the heat capacity is calculated starting from the SiO_2 sample using the ratio between the material density of the low-κ and the SiO_2 as a scaling factor. In the SiO_2 case, the standard properties in the COMSOL Multiphysics library are used and listed in table 3.1 for comparison. The simulated temperatures are measured at the a-Si layer surface. The energy of the laser used in the FEM simulation is constant for all dielectric materials and thicknesses, this way the influence of the dielectric on the maximum temperature reached by the a-Si thin film can be studied. The heat profiles for different thickness of the same dielectric show little difference in the maximum temperature reached, in agreement with experimental observation where the laser fluence did not required any adjustment. At the same time it has a great effect on the cooling rate of the a-Si layer, as shown in figure 3.10. The different thermal buffers material have a tremendous impacts on the maximum

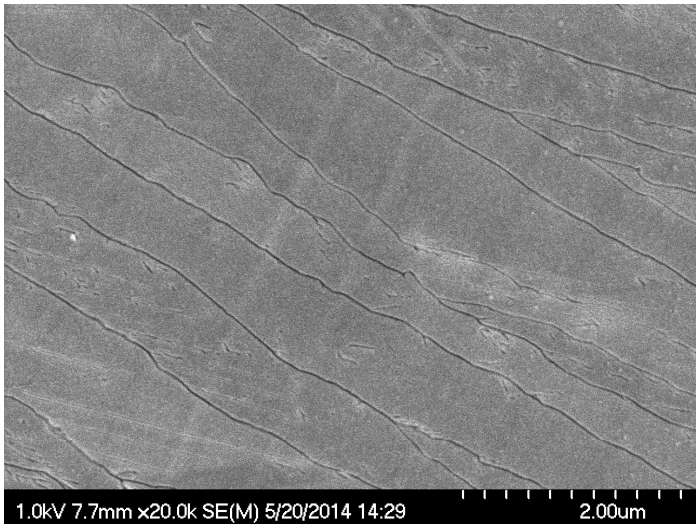
temperature reached during the process: the lower thermal conductivity of the SiCOH allows achieving the a-Si melting temperature ($\sim 1167°C$) at a lower laser fluence than the SiO_2 thermal buffer. The thermal profiles in fig. 3.10 show plateaus around the melting temperature of the a-Si layer for all the simulated cases; these are related to the variation of the material properties in accordance with the transition from the solid state to the liquid one. This transition is simulated with a smoothed step function as discussed in Chapter 2.

The crystallization of the wafers is carried out in an ambient environment at room temperature using the same laser setup and experimental condition. The only parameter adjusted between crystallization is the average laser fluence which is optimized for the two different dielectric materials, in accordance with what observed from simulations. The laser intensity is directly measured, after successful crystallization, through an energy monitor that replaces the sample. Each measurement is the average intensity of 40 laser pulses. An average taken over 10 different measurements yields the estimated laser fluence, which is 974 mJ/cm^2 in the case of SiO_2 dielectric and 630 mJ/cm^2 for the SiCOH dielectric, a 35% reduction. While the different thermal buffer has a big impact on the energy requirement for fully melting the thin-film, the different thicknesses of the same dielectric material has little effect and the laser fluence does not need to be adjusted. Figure 3.4 shows two SEM pictures of the ELC material with a SiO_2 and low-κ dielectric for the thinnest layer: 0.5 μm. Secco etch is used to remove the grain defect providing contrast for the SEM picture. The crystallized material shows very long grains with grain boundaries parallel to the laser scan direction and an average width of 540 nm for the SiO_2 sample and 570 nm for the low-κ sample.

Figure 3.6 reports the Raman spectra of the thin-film Si before and after undergoing the crystallization process for the thinnest low-κ dielectric (0.5 μ). The Raman spectrum of a-Si shows a broad peak around 480 cm^{-1}, which is characteristic of the material phase, and a second peak centered at 520 cm^{-1}, related to crystalline



(a)



(b)

Figure 3.4: SEM images of two Secco etched samples crystallized with Line-Scan SLS. a) is the Si surface on top of 0.5 μm of SiO_2 thermal buffer; b) is the Si surface on top of 0.5 μm of SiCOH thermal buffer. The ELC material has very long grain along the laser scan direction, with an average width of 540 nm for the SiO_2 sample and 570 nm for the low-κ sample.

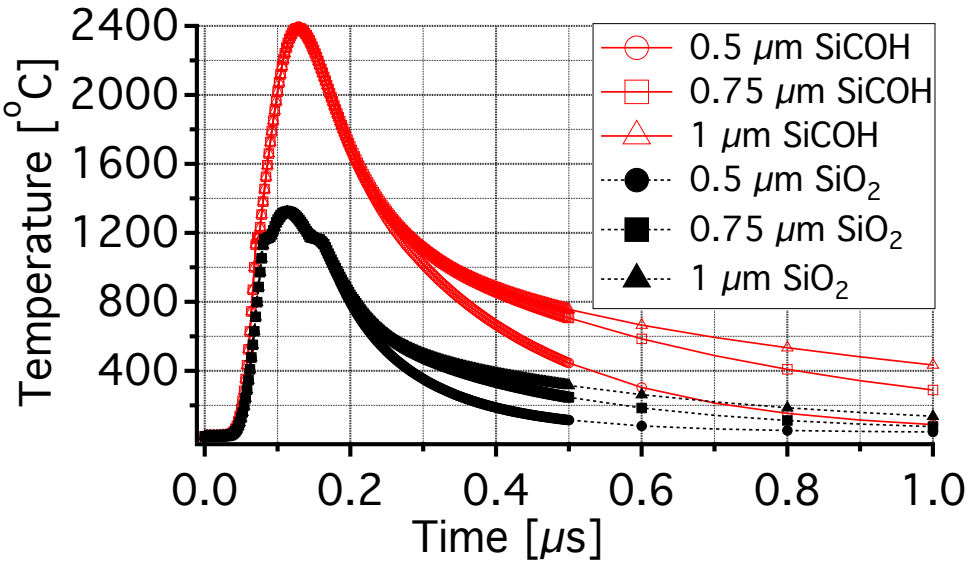


Figure 3.5: 1D FEM simulation of the temperature evolution of the a-Si layer during the crystallization process on SiCOH and SiO_2 dielectrics at different thicknesses. The laser energy is constant in all the simulations to show the effect of the thermal buffer on the maximum temperature reached.

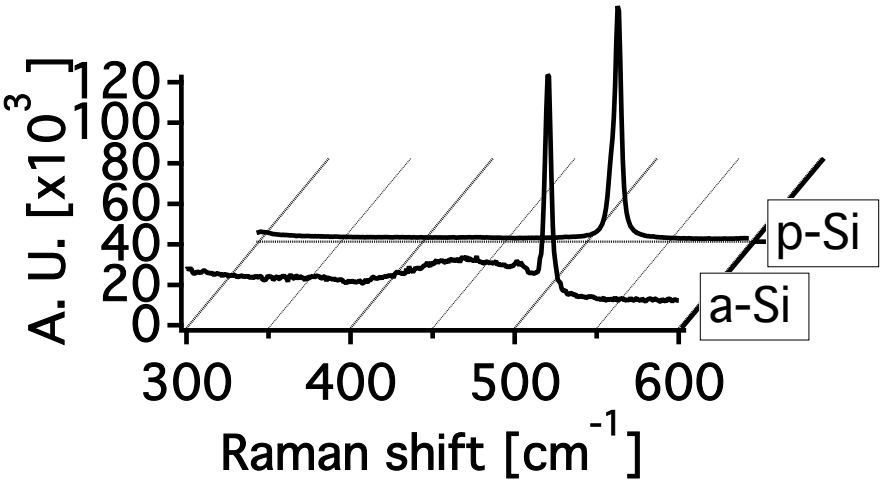


Figure 3.6: Raman spectra of the Si surface before (labeled as a-Si) and after laser processing (labeled as p-Si).

silicon [37; 38], which is attributed to the substrate. In microcrystalline silicon the position of the Raman shift falls in the 500 cm^{-1} - 520 cm^{-1} range, depending on the dimension of the grains [39]. After the ELC process the Raman spectra of both the SiO_2 and low-κ samples have a single peak which is the convolution of the substrate contribution and the laser crystallized polycrystalline material contribution (peak around 517 cm^{-1}) [39; 40]. The ratio between the contribution of the c-Si substrate and the polysilicon surface is used as indication of the crystalline ratio of the top layer. Figure 3.7 reports the relative peak area plotted against the Raman shift for all the crystallized films. All the wafers show very close values in the peak position and their intensity independently of the material and thickness, which demonstrates a consistent crystalline ratio in all the samples.

Figure 3.8 shows XRD spectra which reveal the crystallographic orientation of the grains from both SiO_2 and low-κ samples. The material obtained through line-

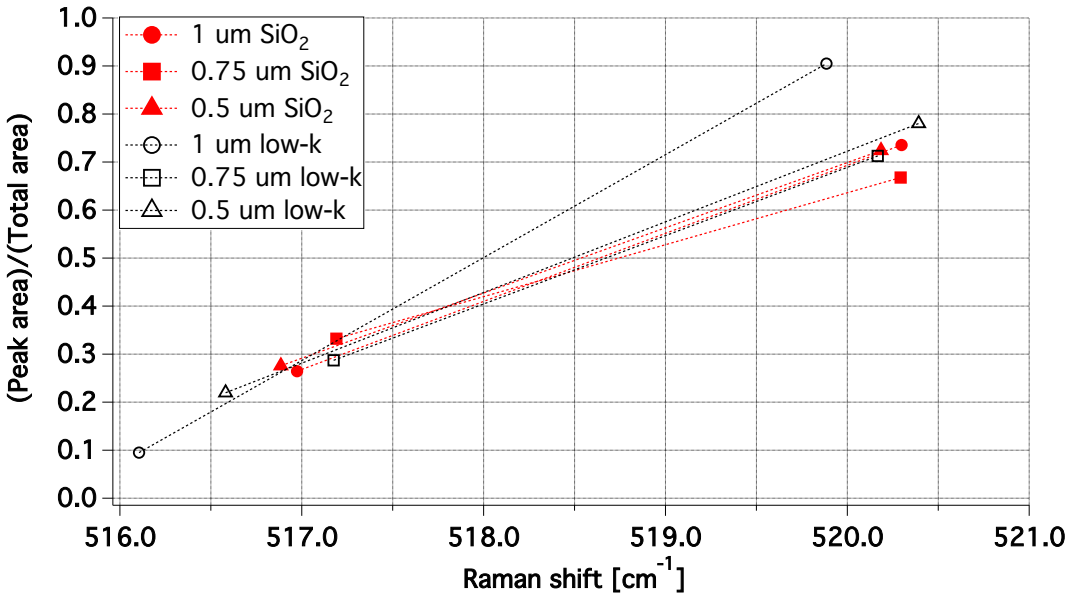


Figure 3.7: Peak area ratio of the Raman spectra for the different dielectric and relative thicknesses.

scan SLS is characterized by non equiaxial grains which are much longer along the laser scanning direction. Due to the anisotropy of the grains the XRD spectra are collected with the X-ray beam impinging on the sample both on a direction parallel and perpendicular to the grain length, to check for possible preferential crystallization directions. The inset shows the diffraction scan from the as-deposited sample before ELC which has no obvious diffraction peaks consistent with the amorphous nature of the film. In contrast, XRD spectra from the ELC samples with SiO_2 dielectric show three main peaks corresponding to the (111), (220) and (311) crystal orientations. However, integrated intensity of the 111 peak is 9.83× higher than the 220 peak in the parallel scan (3.64× for perpendicular scan) and 18.60× higher than the 311 peak (7.13× for perpendicular scan) indicating preferred (111) texture normal to the sample surface. This observation is consistent with the results from previous studies [41; 42]. Although 0.5 μm thick SiO_2 sample exhibits slightly weaker 111 peak, no significant changes in the crystallinity of the grains is observed for different dielectric

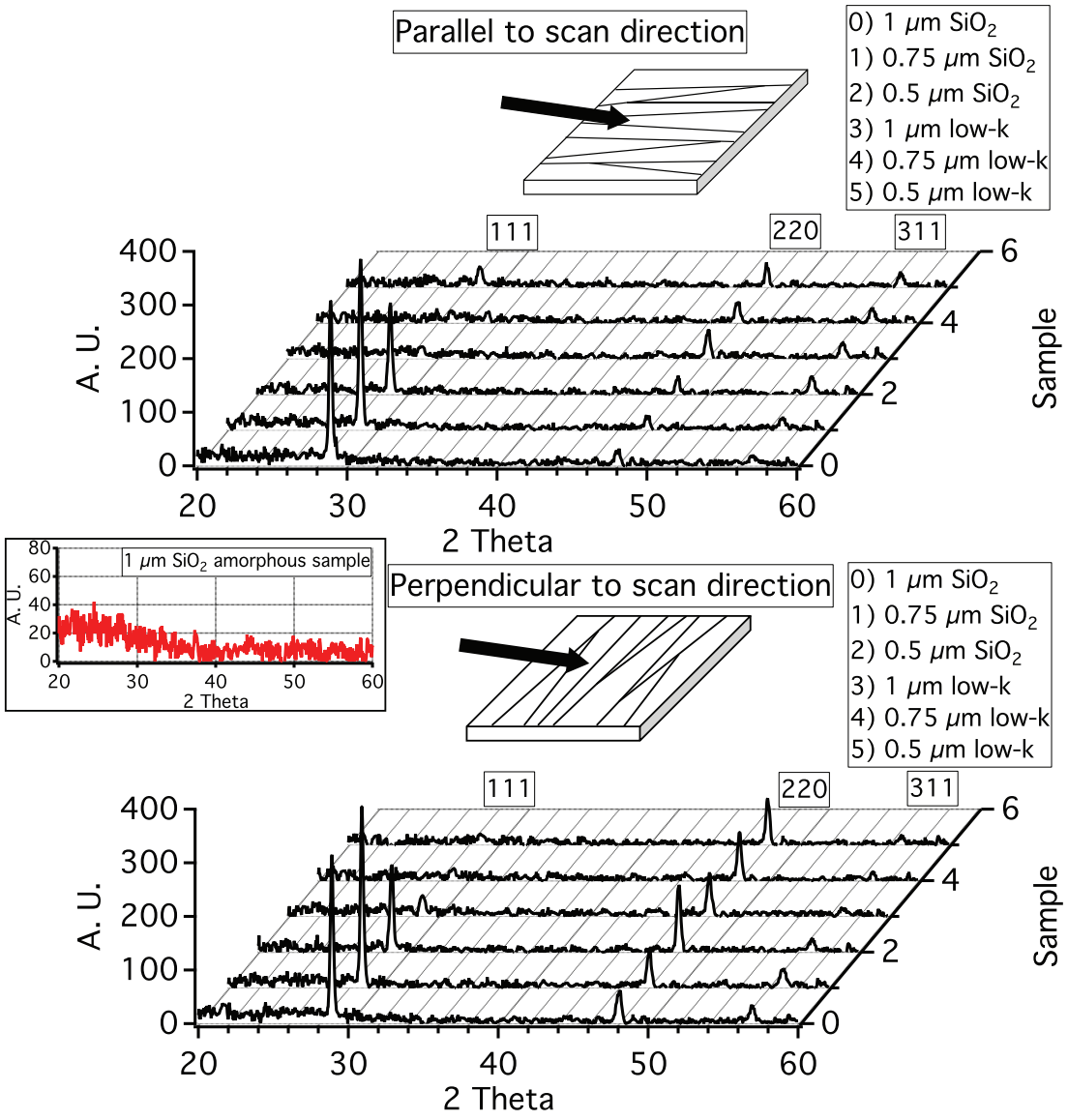


Figure 3.8: XRD spectra of the different samples taken both parallel and perpendicular to the grain growth direction. The inset shows the XRD of an amorphous sample for comparison.

thickness. In case of the ELC samples with low-κ dielectric, the intensity of the 111 peak is greatly reduced indicating that there is no (111) preferential orientation in the surface normal direction. We note however that in-plane preferential orientation might exist for these grains and are not investigated in this studies. Nevertheless, this set of experiments demonstrate the capability of crystallizing the a-Si thin-film on top of low-κ thermal buffers.

3.3 Effect of Excimer Laser Crystallization on the Cu Lines of a BEOL Integrated Wafer

After demonstrating crystallization on low-κ material, the focus of the experiment shift toward exploring the effect of the crystallization process on the buried Cu lines. In this case the structure under study is fairly more complicated than the one used in the low-κ experiments, and it is showed in figure 3.9. In the wafer under test, single-Damascene Cu lines are buried among dielectric layers with a standard process. The SiN layers acts as a diffusion barriers and RIE-stop layers for subsequent line/via patterning. Crystallization on Cu integrated wafers is carried out on a 200 mm wafer and to obtain a fair throughput uses the two-shot SLS technique to crystallize the wafer.

FEM simulations are refined to take into account the structure under study showed in figure 3.9. Figure 3.10 shows a 1D thermal evolution in the BEOL structure during excimer laser irradiation and Table 3.2 reports the material properties used in the simulations.

The simulations study the temperature at the Si surface (figure 3.10a) and at the Cu surface (figure 3.10b) during one laser shot at different SiO_2 thermal buffer thicknesses. The simulation starts with a pulse width (FWHM) of 30 ns, centered at 100 ns, irradiating the surface of the silicon. The energy of the laser is constant to highlight the influence of the dielectric thickness on the maximum temperature reached by the

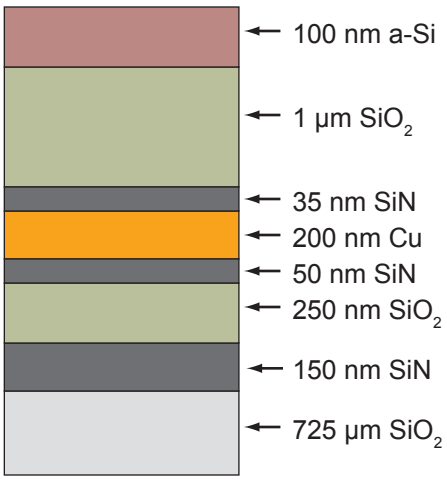
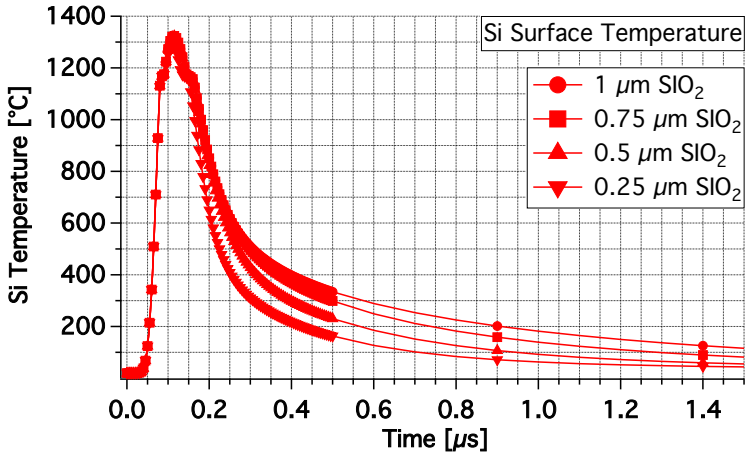


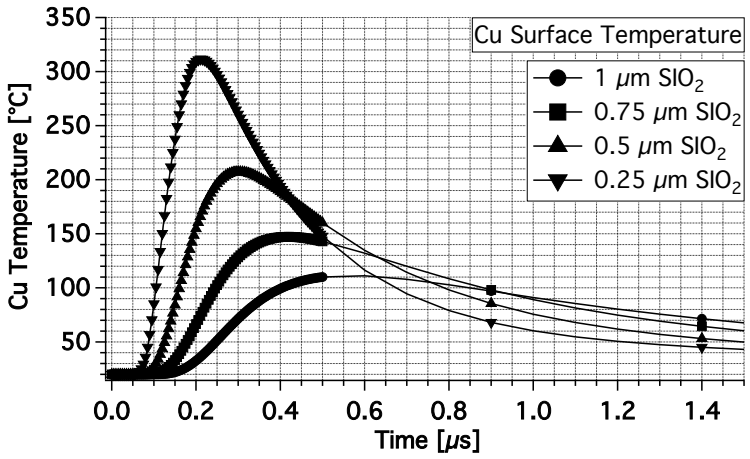
Figure 3.9: Cross-section schematics of the Cu structure integrated on 200 mm wafer. The same structure is used in the experimental part and 1D simulations.

Table 3.2: Material parameters of the SiN, Cu and SiO_2 used in the 1D simulations.

Parameters	**SiN**	**SiO_2**	**Cu**
Thermal conductivity [W m^{-1} K^{-1}]	24.5	1.4	400
Density [g cm^{-3}]	2.5	2.2	8.7
Heat capacity [J K^{-1} g^{-1}]	0.17	0.73	0.39



(a)



(b)

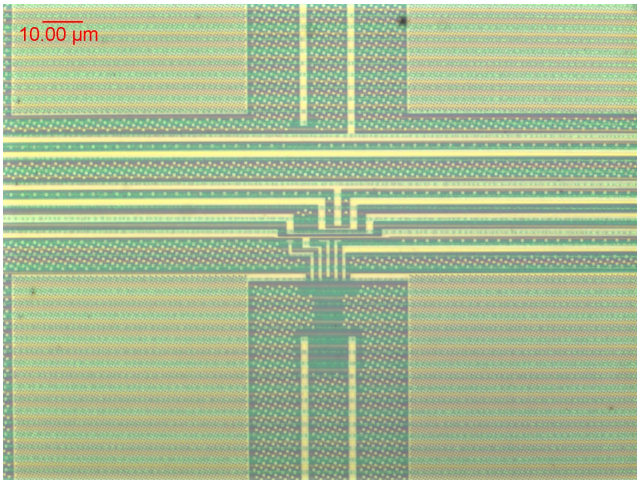
Figure 3.10: 1D FEM simulations of the temperature evolution during the SLS crystallization on BEOL integrated wafers. (a) Surface temperature of the silicon layer during laser irradiation for different thermal buffer thicknesses. (b) Surface temperature of the copper layer during laser irradiation for different thermal buffer thicknesses. The simulation shows that the Cu layer temperature stays below 320 °C even for the thinnest thermal buffer.

silicon and copper surfaces. Upon irradiation the silicon surface quickly reaches the a-Si melting temperature (∼1167 °C) while the heat is spread throughout the structure. While the silicon maximum temperature does not show a strong dependance on the dielectric thickness, the Cu temperature is greatly impacted. Nonetheless, even for the thinner simulated SiO_2 thermal buffer simulated (0.25 μm) the buried metal line does not reach a temperature above 320 °C, which is favorable condition for monolithic integration on BEOL structures.

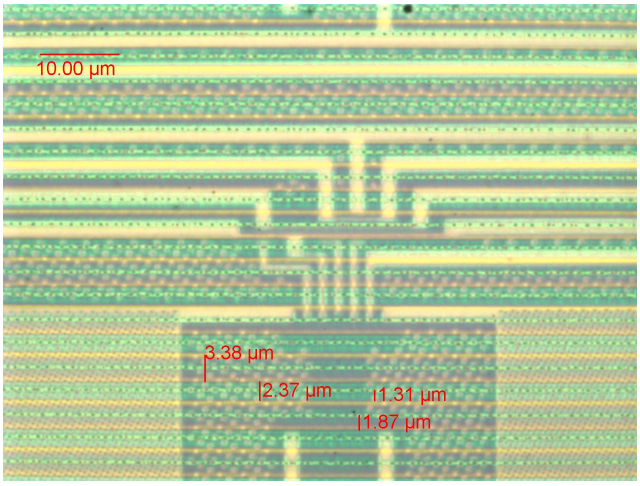
Figure 5.3 presents the top view optical micrographs of the recrystallized structure. The optical micrographs show the characteristic morphology of an SLS crystallized Si film where, when the micrograph focuses on the polysilicon surface (figure 5.3a), is possible to observe the beam-width of the different shots (3.38 μm and 2.37 μm) and the extension of the SLG grains (∼1.6 μm). The micrograph focus on the interconnect layer (figure 5.3b) shows the physical integrity of the copper lines after laser processing.

Figure 5.2 shows the Raman spectra of the material before and after crystallization. In accordance with what observed during the SiO_2/low-κ study, the spectrum of the sample not exposed to laser irradiation is characterized by a broad peak centered at 463 cm^{-1}, which relates to the Si amorphous phase of the top layer, and a second peak centered at 520 cm^{-1}, which is characteristic of single-crystal Si and corresponds to the contribution coming from the Si substrate. Upon laser crystallization, the Raman peak narrows and shifts toward 513 cm^{-1}, consistent with microcrystalline Si, with peaks in the 500 cm^{-1} - 520 cm^{-1} range, depending on the dimension of the grains [39]. In this case the polysilicon peak appears as a left shoulder on the peak related to the single crystal substrate, consistent with what previously observed.

Figure 3.13 examines the electrical characteristic of the Cu layer. The metal resistance is measured at 10 different wafer locations which were not exposed to the excimer laser, and 10 different locations which were exposed to the SLS process. The plot represents the mean resistance value, and its standard error. The data spread



(a)



(b)

Figure 3.11: Optical micrographs of the SLS crystallized silicon on a Cu damascene structure. (a) Focus on the copper layer allows inspection of the Cu lines, which do not show physical degradation related to the thermal process. (b) Focus on the surface of the silicon layer show a crystallized structure with grain length between 1.31 μm and 1.87 μm separated by the protrusion at the center of the irradiated area.

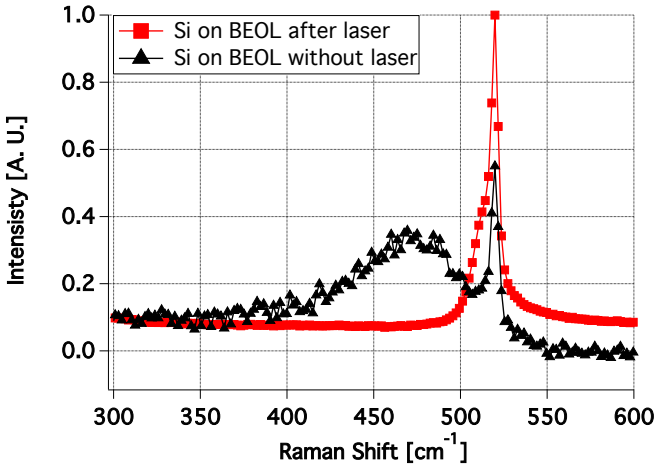


Figure 3.12: Raman spectra of the silicon material with and without crystallization. The amorphous silicon is characterized by a broad peak centered around 463 cm^{-1}. The polycrystalline silicon has a Raman peak centered around 513 cm^{-1}. The peak centered at 520 cm^{-1} is related to the single crystal nature of the substrate.

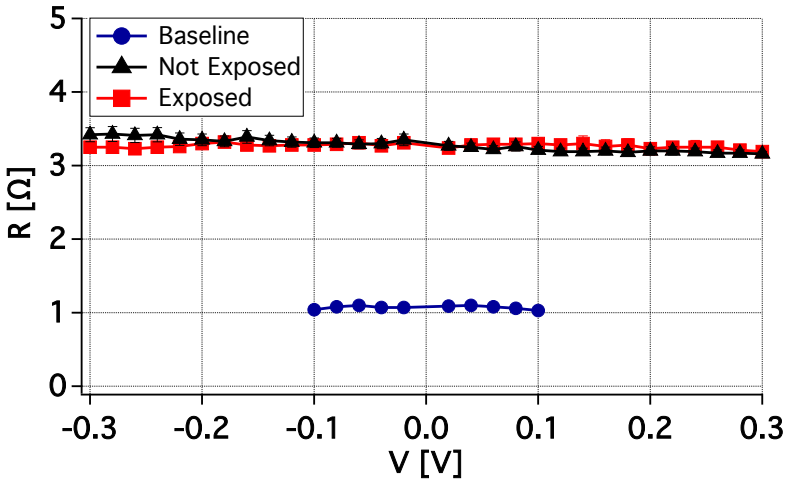


Figure 3.13: Resistance of the Cu layer with and without being exposed to the laser process. The resistance of the Cu layer does not show variation upon exposure. The plot represent the mean value and standard error from 10 different wafer locations.

is relatively small with a standard deviation below 0.33 Ω. Comparison between exposed vs. protected Cu lines during the laser process shows no difference: the electrical properties of the buried copper layer are not affected by the laser process.

3.4 Conclusions

In this chapter, we demonstrate the excimer laser crystallization of amorphous silicon on low-κ dielectrics for monolithic 3D integration in the BEOL of processed silicon wafers and the compatibility of this process with Damascene-Cu structure protected by a thermal buffer.

The crystallization on low-κ dielectrics requires about 35% less energy than required for otherwise equivalent SiO_2 dielectrics, because of the difference in thermal conductivity between the two materials. The long grains characteristic of the process reach a width of 500 nm. Raman analysis of the crystallized wafers does not show any major difference in the quality of the polysilicon. The XRD spectra show a preferential (1,1,1) orientation for the silicon on top of SiO_2 dielectrics independent of the scan direction, while it does not show a preferential direction for the polysilicon on low-κ materials. We conclude that low-κ materials are preferred over SiO_2 interlevel dielectrics for BEOL 3D integration of active silicon devices, and that the low thermal conductivity of low-κ materials yields superior processing characteristics and protection of underlying metal interconnects.

Concerning laser crystallization of an amorphous Si thin film on Cu BEOL-integrated wafers for monolithic 3D integration. A 1D FEM simulation shows how the temperature of the Cu Damascene structure during Si excimer laser irradiation stays below 320°C, even for a 0.25 μm thick SiO_2 thermal buffer. This is well below the maximum temperature limit allowed by monolithic integration on BEOL wafers. Optical micrographs of the irradiated wafer do not show any physical degradation of the copper lines. Raman analysis of the wafer stack confirms achievement of a polysil-

icon structure upon excimer laser exposure, with a Raman peak centered around 513 cm^{-1}, characteristic of microcrystalline Si. Electrical characterization of the Cu lines does not show any resistance variation or degradation upon exposure. We conclude that Cu/low-κ wafers are a suitable substrate for monolithic 3D integration of active Si devices in the BEOL through SLS techniques.

Chapter 4

TCAD Simulation for Device Integration in the BEOL

4.1 Introduction

Technology computer aided design (TCAD) is a useful tool that models the semiconductor fabrication and semiconductor device electrical characteristic depending on technological variables. It allows changing fabrication parameter such as implantation doping, annealing time, annealing gas, etching times, device geometry and many others, and simulates the electrical characteristics of the resulting device. In particular, we used the tool Sentaurus Workbench of the Synopsis TCAD suite, to developed a fabrication process for different class of devices to meet the target parameter that were given in the designing phase. The devices characterized in chapter 4 are the results of the simulation work that is presented in the following sections.

Sentaurus Workbench integrates a series of different tools to accurately simulate different part of the integration and characterization process. In particular the tool used in the following simulations are: Sentaurus Process, Sentaurus Structure Editor, Sentaurus Device, and Sentaurus Inspect. Sentaurus Process and Structure Editor tool can define, in substantially different ways, the structure of the device under

Property	Target Value
R_{ON} [Ω]	1×10^{3}
On/Off ratio	$> 10^{4}$
Voltage to switch [V]	0.5 to 1
Time to switch [s]	$< 1\times10^{-6}$

Table 4.1: Target parameter for a polysilicon device.

study. Sentaurus Device, solves the appropriate physical and electrical equation on the structure passed by the process or structure tool, simulating the electrical characteristic of the device. Sentaurus Inspect allows the parameter extraction from the current-voltage characteristic generated in the previous step.

The main goal of these simulations is to reduce the number of fabrication iteration necessary to achieve a device that satisfies the requirements which are listed in table 4.1. The possible applications for the device designed in these chapters include switching applications in which low power, and good On/Off ratio are among the most important factor. Because of this the focus of the following simulations is mainly on the JFETs and TFTs device family.

4.2 Simulation Methods

Two different tool are used to design and mesh the devices under study: Sentaurus Process and Sentaurus Structure Editor. The process tool start from a block of single crystal silicon and simulates all the step required by the fabrication process of a device (e.g. lithography, deposition, diffusion, etching) and output the final structure; the structure editor tool directly allows the designing of the structure without simulating all the fabrication steps. While the process tool is a more accurate way of simulating the device structure taking into account dopant diffusion and other

effect of the fabrication process, the Structure editor quickly allows to obtain a device structure to use for evaluating the electrical performance. In either cases the starting active channel material is a single crystal structure, which has substantially different morphology compared to our SLS-crystallized material. As previously discussed in Chapter 1 to model the electrical conduction in a polycrystalline material it is possible to represent the grain boundaries as single-energy level trap centered at the middle of the band gap. In Sentaurus Device the source-code can be modified in the electrical simulation to introduce a precise trap density N_t centered at energy E_t to mimic electrical behavior in a polycrystalline thin-film.

4.2.1 JFETs TCAD Simulations

Figure 4.1 show the JFET designed with the structure editor tool in Sentaurus. As opposed to the classic JFET structure presented in chapter 1, the simulated one contains a single p^+-n junction to control the modulation of the channel. The doping unbalance allows for the depletion region to be mainly modulated in the channel part. The device is designed with a channel length of 300 nm and W/L of 10. The metal contact are modeled with a resistance of 100 Ω and the source and drain region are doped with 5×10^{14} cm^{-2} of phosphorus. The channel is characterized with a trap density N_t of 5.77×10^{11} cm^{-2}.

In a JFET by controlling the voltage applied on the gate is possible to modulate the depletion width of the p^+-n junction which in turn allows or inhibit current flow between source and drain. Figure 4.2 show the trans-characteristic of a simulated JFET. The depletion region width W of a p^+-n junction, using the abrupt junction approximation, can be expressed as:

$$W = \sqrt{\frac{2\epsilon_s(V_{bi} - V_A)}{qN_d}} \tag{4.1}$$

where ϵ_s is the relative dielectric constant of the channel material, q the elementary charge, N_d the channel doping, V_A is the external voltage applied across the junction

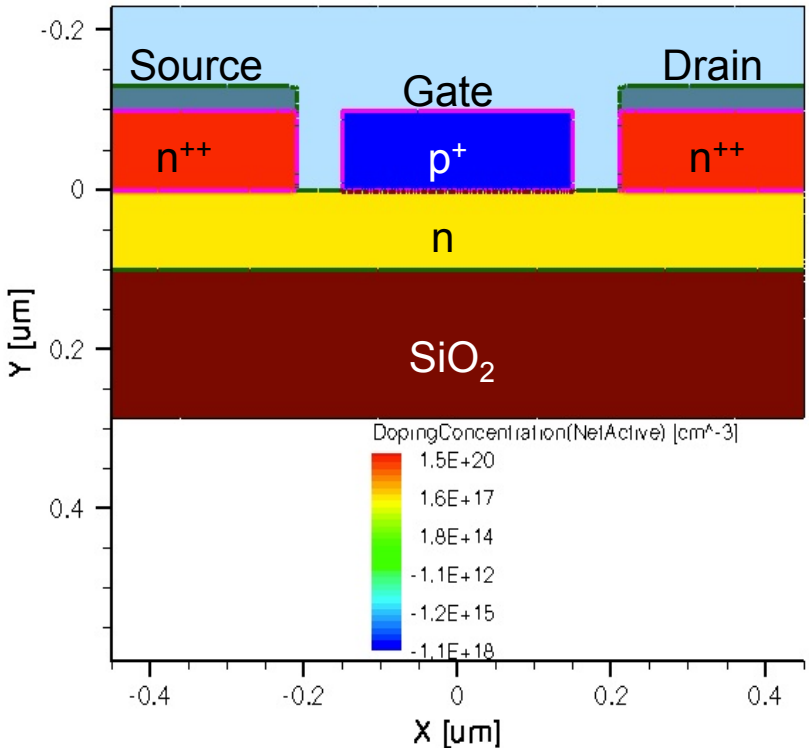


Figure 4.1: Cross-section of a JFET designed with the structure editor tool of Sentaurus. The source and drain are highly phosphorus doped silicon region on top of which aluminum contact are deposited. The gate is highly boron doped silicon on top of 100 nm of lightly doped phosphorus material deposited on a SiO_2 thermal buffer.

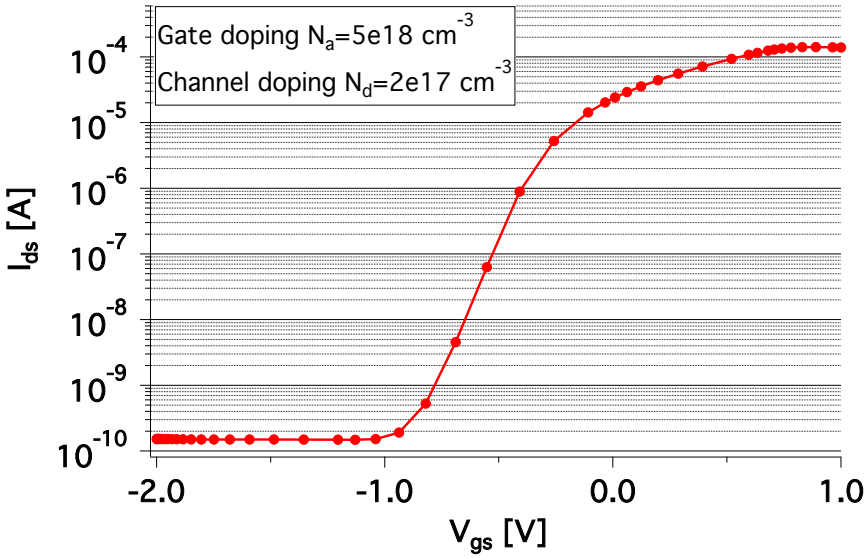


Figure 4.2: Trans-characteristic of a simulated JFET device with boron gate doping of 5×10^{18} cm^{-3} and phosphorus channel doping of 2×10^{17} cm^{-3}.

and V_{bi} is the built in potential of the p$^+$-n junction:

$$V_{bi} = \frac{\kappa_B T}{q} \cdot ln(\frac{N_a N_d}{{n_i}^2}) \tag{4.2}$$

Equation 4.1 shows the effect of the channel doping on the width of the depletion region which must be properly choosen to allow switching On and Off the device. Figure 4.3 shows the Matlab simulation of the modulation of the depletion width of the JFET p$^+$-n junction as function of the channel doping and gate voltage, without taking into account the drain voltage effect. Figure 4.4 shows the Sentaurus electrical simulation of the JFET device across the same channel doping and gate voltage variation taking also into account an applied drain voltage of 1 V. This simulation show how a small variation in the active channel doping level can have a dramatic effect on the performance of the devices. As figure 4.4 shows, it appears difficult to obtain a good performing device with a relatively simple fabrication process. In particular the voltage swing necessary for turning the device from the Off state to the On one is larger than the one targeted in the designing phase. These simulations

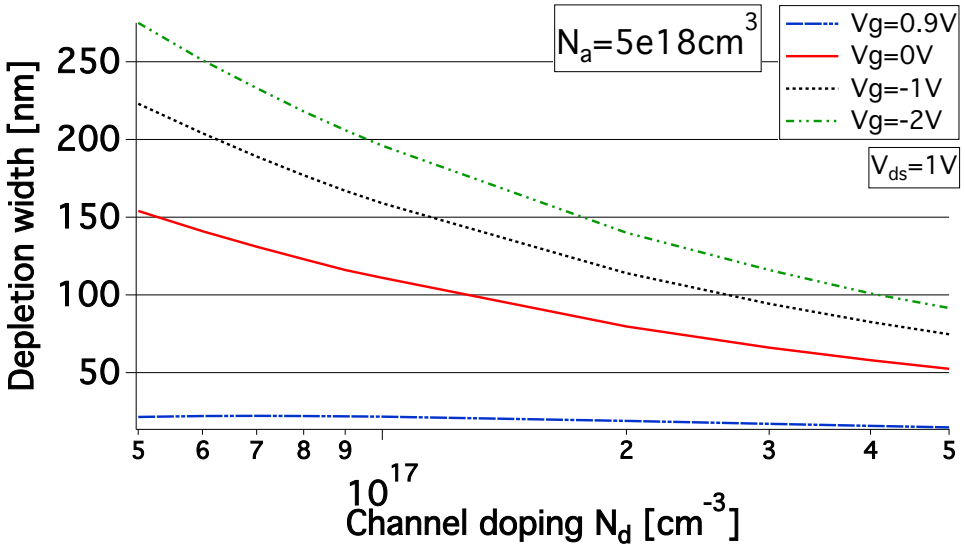


Figure 4.3: Matlab simulated variation of the p^+-n junction depletion width of a JFET with a fixed gate doping and variating channel doping level at different gate voltages.

show the necessity to have at least a 2 V swing for optimal operation. Even with such larger swing the On resistance of the device will be around tens of kΩ which is distant from the target value.

4.2.2 TFTs TCAD Simulations

A different class of devices simulated are thin-film transistors. Figure 4.5 shows the cross-section of one of the simulated TFTs. The geometrical dimension of the TFTs are fixed by the photolithographic mask used and therefore did not change. The device simulated is a n-type device with a channel length of 300 nm, a high-κ HfO_2 dielectric at different thicknesses and polysilicon gate. The trap density is consistent with the one used in the JFET simulation: 5.77×10^{11} cm^{-2}. The source and drain contact are in aluminum and have a resistance of 100 Ω; the source and drain pocket are doped with 5×10^{14} cm^{-2} of phosphorus. Other parameter are changed during the

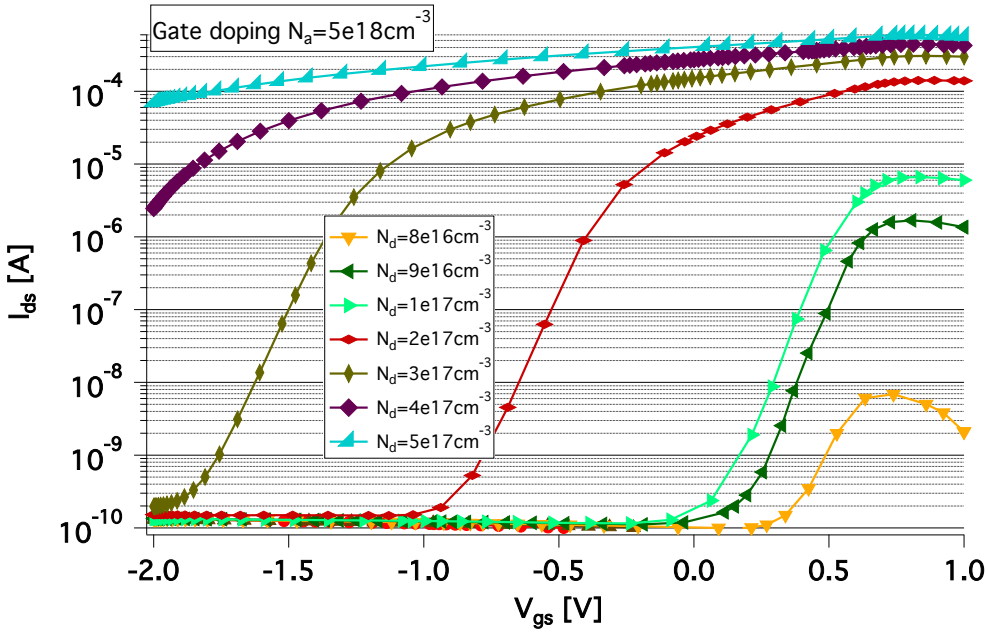


Figure 4.4: Sentaurus electrical simulation on a JFET device with different channel doping level.

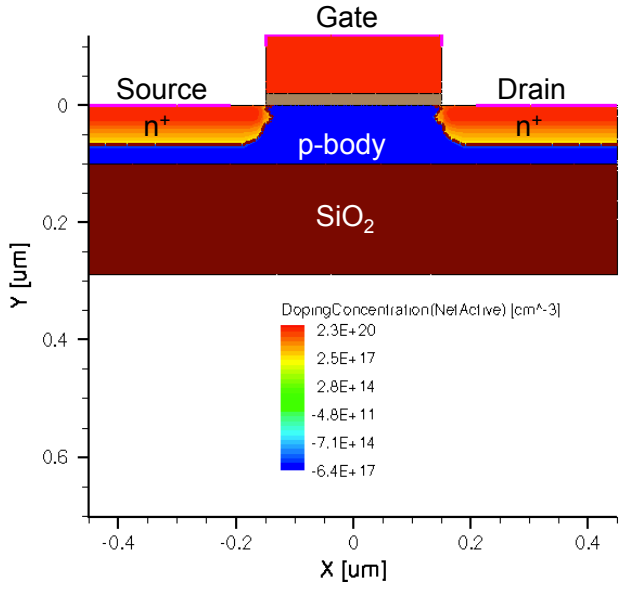


Figure 4.5: Cross-section of a TFTs implemented through the process simulator tool of Sentaurus.

simulation to find the best performing device, such as: the level of the boron channel doping N_a and the thickness of the gate dielectric T_{ox}. Rapid thermal annealing time for the dopant activation, dopant implantation energy and dose are also later simulated to achieve an optimal source and drain doping profile.

Figure 4.6, 4.7 and 4.8 report the simulated TFTs trans-characteristic with variation of channel doping at different gate dielectric thicknesses. For all the different characteristic, as the concentration of the dopants in the channel is increased, the threshold voltage shifts toward more positive values, because higher gate voltage is needed to deplete and finally invert the population in the channel. The trans-characteristic shift affects both the maximum On current achievable at 1 V, which decreases, and the minimum Off current measured at 0 V which also decreased. Figure 4.9 , 4.10 and 4.11 summarize the effect of the gate dielectric thickness variation and channel doping on the threshold voltage, On/Off current ratio and On resistance. As Figure 4.9 shows it is possible in case of TFT device to get closer to the given target parameter than with a JFET device. In particular the voltage swing can be kept at 1 V, obtaining as well a good On resistance and On/Off ratio and overall device performance more robust to process parameters variation.

An important aspect of a TFT fabrication is the pocket doping. In particular the implantation energy, implantation dose, annealing temperature and annealing time greatly affect the profile of the pocket and in turn, the device performance. To properly choose this parameter we complement Sentaurus with the software SRIM (Stopping and Range of Ions in Matter) to select a combination of implantation energy/dose and annealing temperature/time condition. Figure 4.12 shows the SRIM simulation result on the dopant implantation. From the peak concentration in the simulation is possible to back up the dose necessary to implant to achieve a precise doping level in the pocket. In our case in order to have a pocket doping of 5×10^{19} cm^{-3} we found that the best combination of parameter is an implantation energy of 10 keV and a tilt angle of 7 degrees, and a dose of 1×10^{14} cm^{-2}.

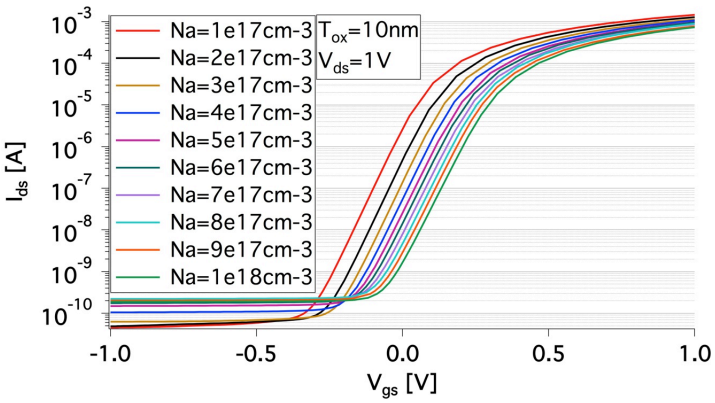


Figure 4.6: Effect of the variation in doping level of the TFT body on the trans-characteristic of the device with a HfO_2 gate oxide of 10 nm thick.

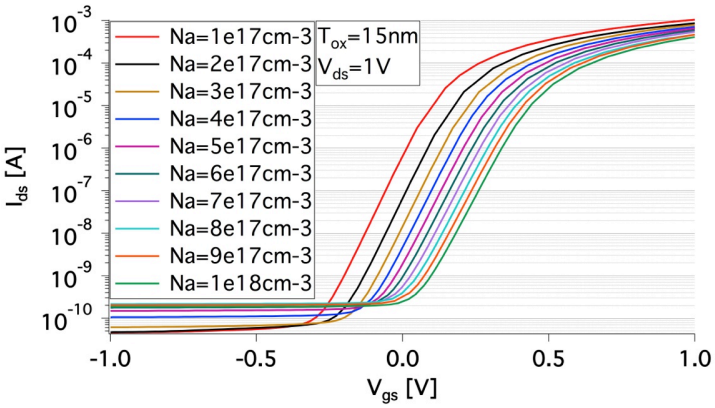


Figure 4.7: Effect of the variation in doping level of the TFT body on the trans-characteristic of the device with a HfO_2 gate oxide of 15 nm thick.

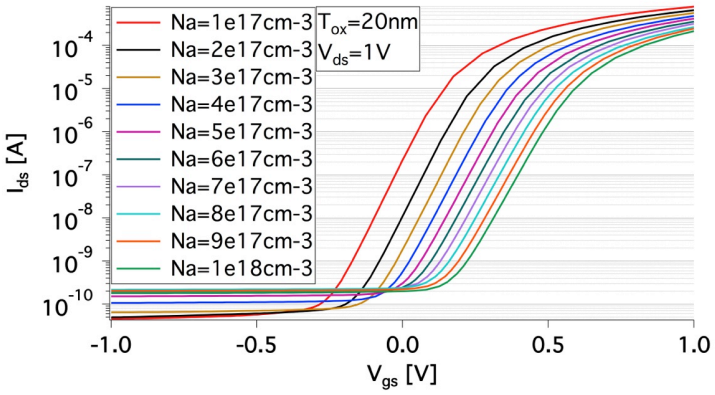


Figure 4.8: Effect of the variation in doping level of the TFT body on the trans-characteristic of the device with a HfO_2 gate oxide of 20 nm thick.

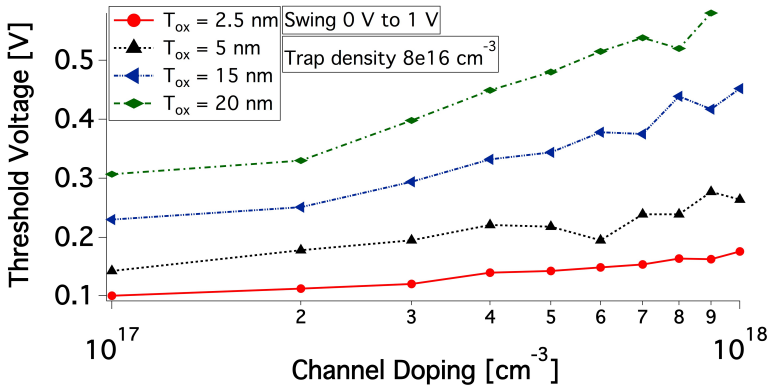


Figure 4.9: Effect of the variation in doping level of the TFT channel on threshold voltage.

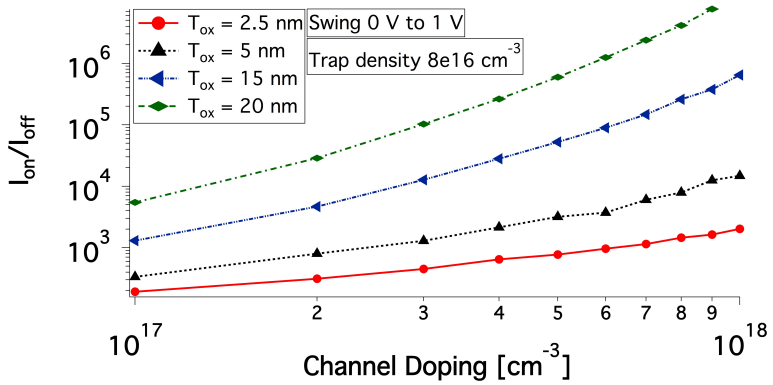


Figure 4.10: Effect of the variation in doping level of the TFT channel on I_{on}/I_{off} ratio.

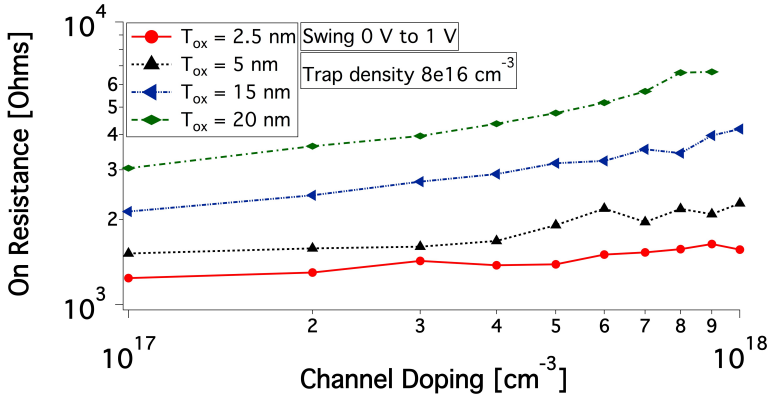
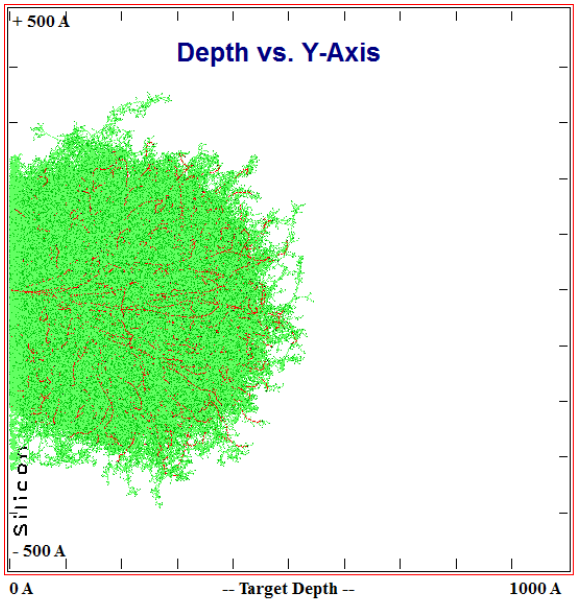
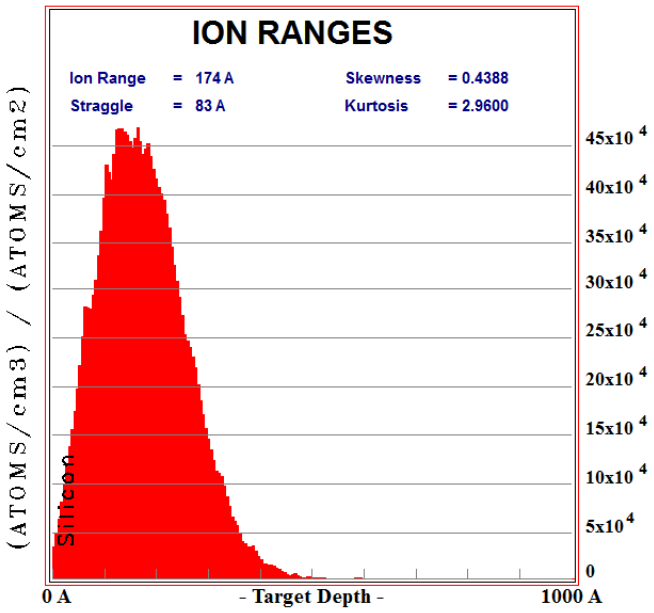


Figure 4.11: Effect of the variation in doping level of the TFT channel on On resistance.



(a)



(b)

Figure 4.12: SRIM simulation of the phosphorus implantation at 10 keV with a wafer tilt of 7 degrees. 2×10^4 Ions simulated. a) Shows the ions range when implanted in a silicon material. b) Shows the dopant profile and their peak concentration.

To become electrically active the dopants need to be annealed so that the doping atoms (either donor or acceptor) can substitute part of the silicon atoms in the lattice. This require an annealing step to provide the energy necessary to the system. By changing the temperature and time of the annealing step it is possible to modify the profile of the dopant achieved during implantation, and therefore this parameter must be selected carefully. To assess the best temperature/time combination we used once again the Sentaurus Process tool. Figures 4.13 and 4.14 show the effect of the temperature on the dopant profile for two different annealing time, 10 and 20 seconds respectively. The condition selected for the integration step are an annealing temperature of 800° for 20 seconds.

4.3 Conclusions

This chapter summarize the work that is necessary before the device can be physically integrated. From the definition of the parameter that the device must meet, extensive simulations helped in defining all the technological parameter that need to be optimized to meet the target performance. We simulated both JFETs and TFTs performance on polysilicon material. Table 4.2 summarize the result of the simulation, which indicates that TFTs on the polysilicon material can obtain a better matching with the target parameter given at the beginning of the designing phase. This simulation served to define a fabrication process and integrate the devices which are discussed in the following chapter.

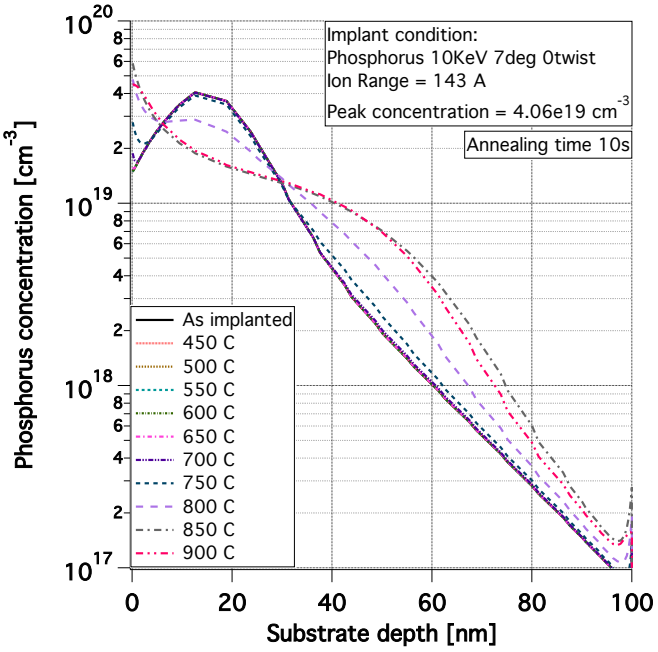


Figure 4.13: Temperature effect on the dopant profile for a 10 seconds annealing step.

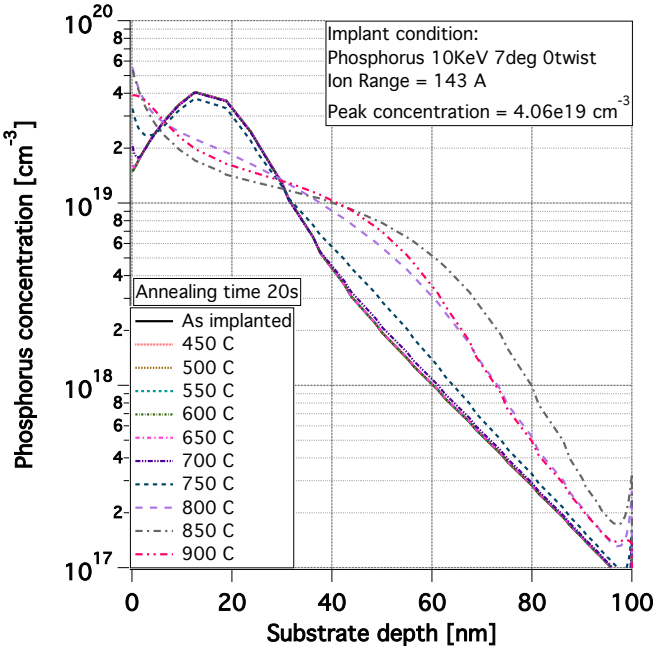


Figure 4.14: Temperature effect on the dopant profile for a 20 seconds annealing step.

Property	Target Value	TFT	JFET
R_{ON} [kΩ]	1	1 - 4	5 - 100
On/Off ratio	$> 10^4$	10^4 - 10^6	10^4 - 10^6
Voltage to switch [V]	0.5 to 1	1	2.5
Time to switch [s]	$< 1{\times}10^{-6}$	-	-

Table 4.2: Target parameter for a polysilicon device.

Chapter 5

Excimer Laser Crystallization of Silicon Thin Films for Monolithic 3D Integration for VLSI

5.1 Introduction

After demonstrating excimer laser crystallization of thin film in the BEOL of integrated wafers, this chapter focuses on the performance that devices integrated in the resulting material can achieve. Starting from Technology Computer Aided Design (TCAD) simulation based on the software Sentaurus and discussed in chapter 4, we developed a fabrication process which allowed us to meet the target performance. This chapter discusses the fabrication process of the devices and their characterization.

5.2 VLSI of Polycrystalline Silicon TFTs

The devices designed in chapter 4 are integrated on 200 mm wafers; when crystallization happens over this relatively big area, throughput is an important parameter to consider. Because of this, two-shot SLS is selected as crystallization technique

for this set of experiment. As discussed in chapter 2, two-shot SLS differs from line scan SLS in the translation distance in between shots. This yields a material with varying grain morphology: whereas in line scan SLS the silicon is characterized by long and narrow grains, in two-shot SLS the material is characterized by a repeated crystalline structure with shorter grains. Although the achievement of longer grain in the line-scan SLS can have a positive effect on the mobility of the devices, it can have detrimental effect on their uniformity. Because this techniques template from an initial structure, it can keep localized grains with completely different textures throughout the area of the wafer, affecting the device uniformity. On the contrary, in two-shot SLS, even though the smaller grain structure suffer from a reduction in the maximum electrical performance of the device, the technique offers some advantages. Because of the repeated crystalline structure, silicon grains with different texture are randomly distributed across the wafer and is therefore able to achieve better device uniformity [43]. Moreover, because of the increased stage translation distance, the two-shot approach offers an increased throughput [44] which is beneficial in VLSI production.

Figure 5.1 shows the integration steps for the fabrication of inversion mode TFTs. Integration starts with a standard 200 mm Si wafer on top of which we deposit 1 μm SiO_2 through PECVD and 100 nm of a-Si through LPCVD. Even though LPCVD is not completely compatible with a fabrication process for integration in the BEOL, it has the advantage of providing a very pure silicon layer that is stable during the ELC process because it lacks the hydrogen present in PECVD which evolves during laser crystallization of the silicon film. The lack of hydrogen in the film means that the grain boundaries are not natively passivated, which affects the overall electrical performance of the devices. Post integration hydrogenation is a step that could be added to improve the device performance [45; 46; 47; 48]. The silicon layer is then implanted with boron to provide the background doping for the TFTs with a concentration of 4×10^{17} cm^{-3}. Wafer irradiation with the excimer laser simultaneously crystallizes the

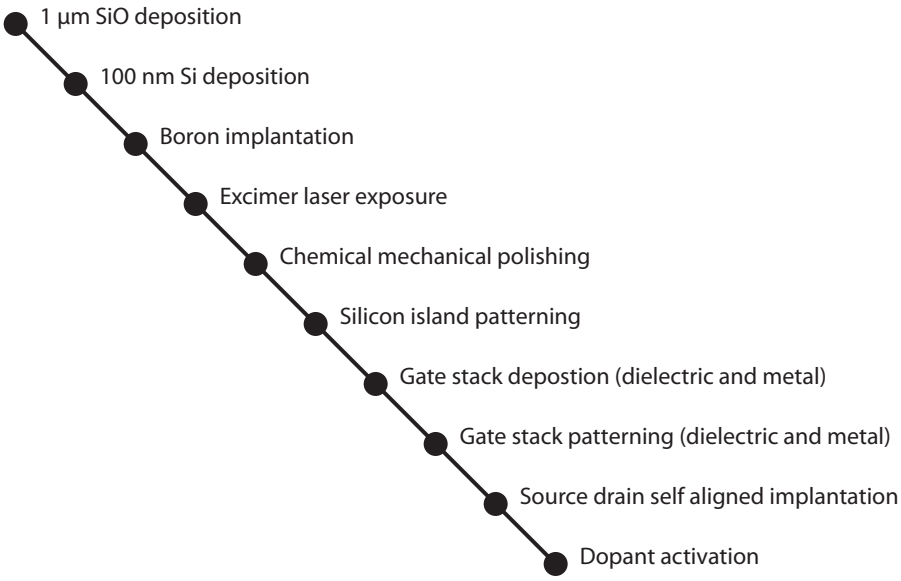


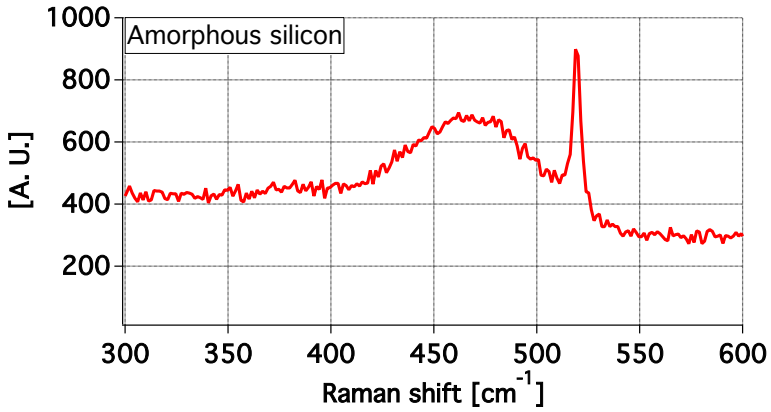
Figure 5.1: Fabrication flow for the integration of lateral TFTs on 200 mm wafer using two photolithographic steps.

material and activates the dopants. The silicon layer is then patterned into islands, which helps isolate devices and decrease the cross-talk. The gate dielectric is a layer of HfO_2 with an equivalent oxide thickness of 2.0 nm, on top of which metal layers are deposited and patterned as a gate contact. Subsequently, the device are implanted with a self aligned process to achieve a peak phosphorous doping of 5×10^{19} cm^{-3}. The dopants are activated with rapid thermal annealing at 800 °C for 20 s in a nitrogen environment.

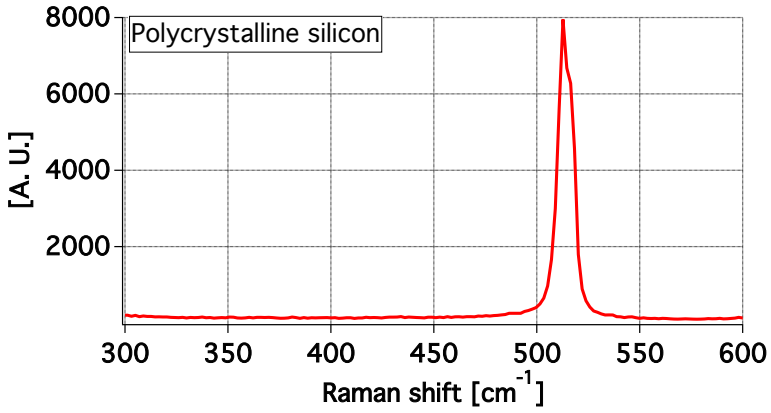
5.3 Material and Device Characterization

Figure 5.2 reports the Raman spectra of the material before and after crystallization. In accordance with the data presented in chapter 3 it is possible to confirm the correct transition of the material from its amorphous phase to a polycrystalline phase.

Figure 5.3 shows the characteristic morphology of a 2 shot ELC material measured

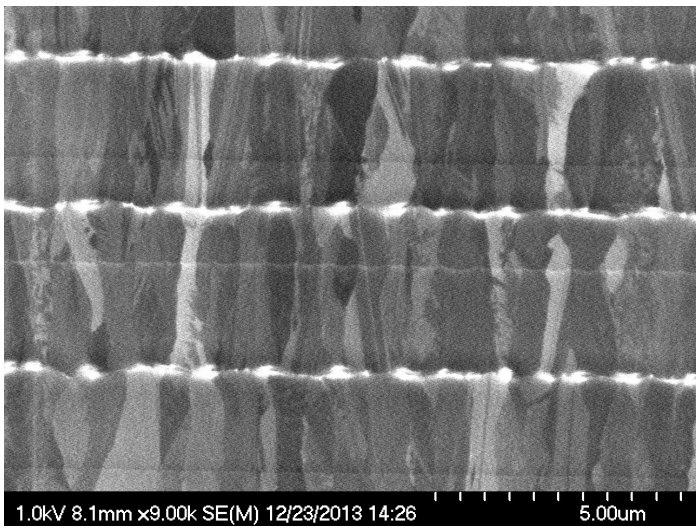


(a)

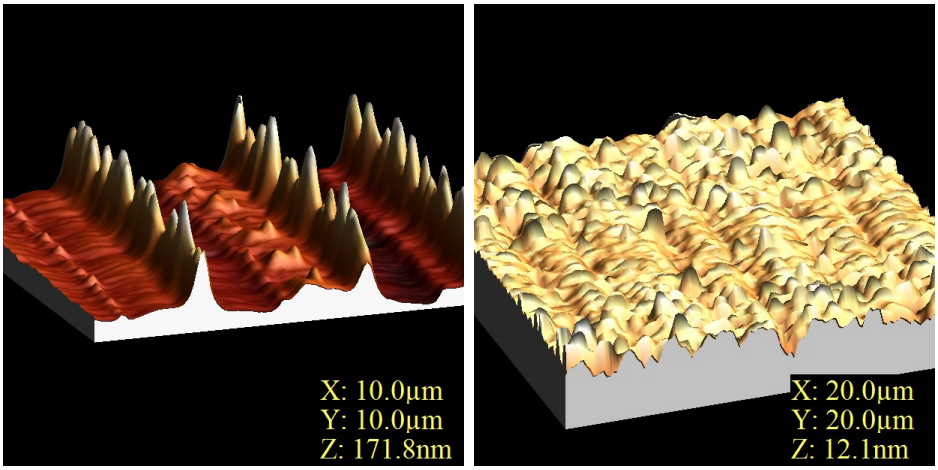


(b)

Figure 5.2: Raman spectra of the silicon material (a) before and (b) after crystallization. The amorphous silicon is characterized by a broad peak centered around 480 cm^{-1}. The polycrystalline silicon has a Raman peak centered around 513 cm^{-1}.



(a)

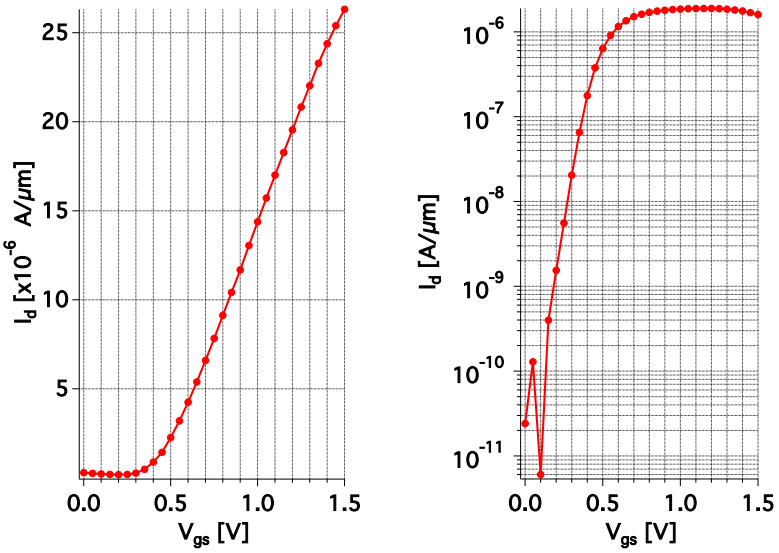


(b) (c)

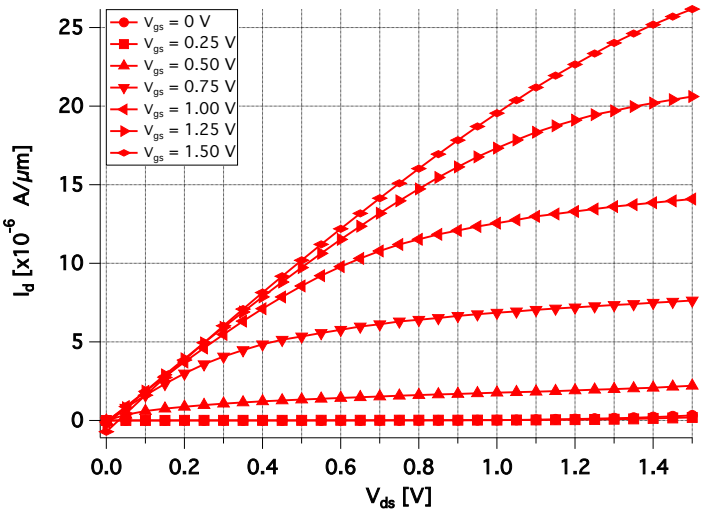
Figure 5.3: a) Secco defect enhanced SEM micrograph of the two-shot SLS silicon showing the polycrystalline morphology. b) AFM 3D micrographs of the polycrystalline material, which shows tall protrusions where the grains join each other. The measured RMS roughness is 26.6 nm. c) AFM 3D micrograph of the polycrystalline material after CMP with a measured RMS roughness of 0.87 nm.

by AFM. The 2 shot SLS crystallized material is characterized by narrow and tall protrusions arising at the center of the re-solidified area where the grains join each other (figure 5.3b). This is caused by the difference in material density of the silicon when in its solid vs. liquid phase. The density of solid Si is 2.33 g$\times$cm^{-3}, while it is 2.57 g$\times$cm^{-3} at its melting point. During the crystallization process (figure 2.3) the silicon starts cooling from the edges of the molten area at the liquid/solid interface and proceeds towards the center of the irradiated area. This causes an accumulation of material at the center of the re-solidified area which causes the protrusion. The Root Mean Square (RMS) roughness of the as crystallized polysilicon is 26.6 nm with maximum peak height of 160 nm. Before further fabrication the wafers are chemically-mechanically polished (CMP) to obtain a smooth surface with a RMS roughness of 0.87 nm, Fig. 5.3c, which helps decrease the trap density at the Si/SiO_2 interface of the TFTs gate stack and improves the 2σ uniformity.

We characterized multiple TFTs devices on different dies across the 200mm substrate. Fig. 5.4 shows the output characteristic and trans-characteristic in both the saturation and linear region for the smaller device with a W/L of 1/0.3 μm/μm. All of the tested devices show proper switching behavior with a supply voltage of 1.5 V. The change in slope of the current for high V_{gs} in Fig. 5.4a is related to a relatively high contact resistance. The high contact resistance is due to the simplified integration process, which does not include metal deposition and silicide formation for the source and drain contact. Nevertheless, the integrated device shows good performance with a threshold voltage of 0.23 V extracted in the saturation region and a maximum driving current of 26.31 μA/μm. Fig. 5.4b shows the trans-characteristic in the linear region when 100 mV is applied at the drain to source terminals. The devices show a low sub-threshold slope of 87.7 mV/decade and an On/Off current ratio of 3.08×10^5. Fig 5.5 report the capacitance vs voltage extraction for the larger TFTs with a W/L of 95/10 μm/μm, which matches the one expected for a SOI device. From the capacitance curve we extracted a C_{ox} of 1.79×10^{-6} F/cm^2 with an



(a) (b)



(c)

Figure 5.4: Characteristic behavior of a monolithically integrated TFT with W/L of 1/0.3 μm/μm (a) TFT trans-characteristic in the saturation region with V_{ds} = 1.5 V. The extracted threshold voltage is 0.23 V. (b) TFT trans-characteristic in the linear region with V_{ds} = 100 mV. The extracted sub-threshold slope is 87.7 mV/decade and I_{On}/I_{Off} is 3.08×10^5 (c) TFTs output curves at different V_{gs}.

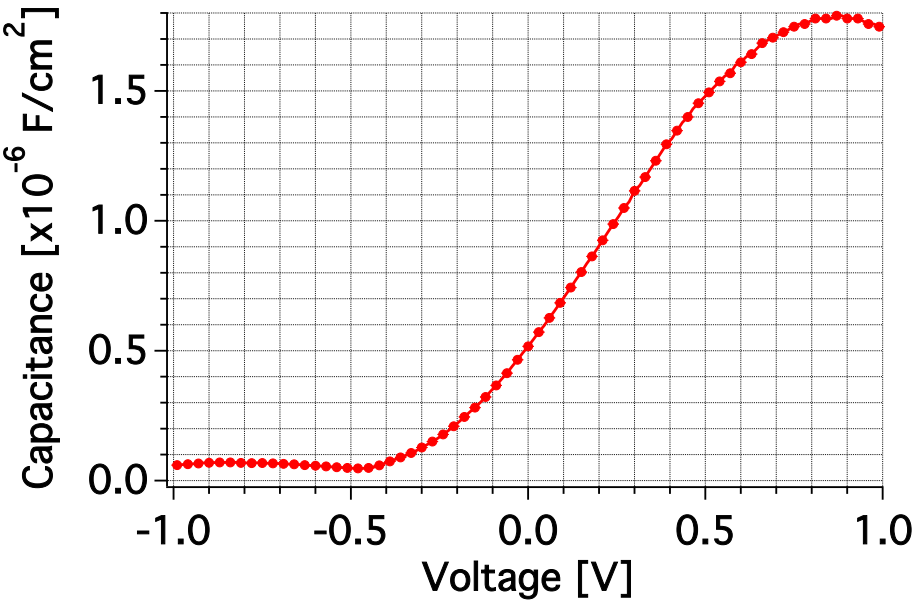


Figure 5.5: Normalized mean capacitance vs voltage characteristic for the bigger devices with W/L of 95/10 μm/μm. The capacitance shows the trend characteristic of a silicon on insulator device.

equivalent oxide thickness of 2.0 nm.

Table 5.1 reports the statistical distribution of the parameter extracted for all of the devices together with the standard deviation for all the different geometries. Overall the devices show good uniformity over multiple dies.

The electrical performance of the polysilicon devices are affected by the grain size and related number of grain boundaries in the material. Electrical conduction in a polycrystalline material is usually described using the grain boundary trapping model, where carriers need to overcome the potential barrier associated with the grain boundaries [16; 15; 14; 13]. Under the assumptions presented in chapter 1, Levinson in [18] shows that the TFT current in a polycrystalline material can be expressed as a function of the trap density in the material:

Table 5.1: Device geometry and extracted parameters of the fabricated TFTs. The values reported are the mean values and standard deviation. Within 2σ will fall the 95.4% of the data.

W/L [μ**m**/μ**m**]	$\mathbf{V}_{T-SAT}$ [**V**]	**SS** [**mV/decade**]	$\mathbf{I}_{ON}$ [μ**A**/μ**m**]
95/10	0.38 ($2\sigma = 1.48\times10^{-2}$)	80.51 ($2\sigma = 8.44$)	1.60 ($2\sigma = 0.30$)
9.5/0.6	0.25 ($2\sigma = 3.56\times10^{-2}$)	84.76 ($2\sigma = 5.76$)	4.03 ($2\sigma = 0.54$)
1/0.8	0.42 ($2\sigma = 3.66\times10^{-2}$)	86.63 ($2\sigma = 10.44$)	17.43 ($2\sigma = 3.7$)
1/0.6	0.36 ($2\sigma = 1.18\times10^{-1}$)	79.64 ($2\sigma = 16.46$)	21.79 ($2\sigma = 6.20$)
1/0.5	0.36 ($2\sigma = 1.84\times10^{-1}$)	80.84 ($2\sigma = 5.98$)	21.92 ($2\sigma = 0.78$)
1/0.3	0.32 ($2\sigma = 8.642\times10^{-2}$)	81.98 ($2\sigma = 11.1$)	21.53 ($2\sigma = 8.62$)

$$I_d = \frac{W}{L}\mu V_{ds} C_{ox} \exp\left(\frac{-q^3 N_t^2 t}{8\epsilon k T C_{ox} V_{gs}}\right) \tag{5.1}$$

Dividing by V_{gs} and taking the natural logarithm of (5.1) is possible to write:

$$ln(I_d/V_{gs}) = ln\left(\frac{W}{L}\mu V_{ds} C_{ox}\right) + \left(\frac{-q^3 N_t^2 t}{8\epsilon k T C_{ox}}\right) * \frac{1}{V_{gs}} \tag{5.2}$$

Therefore, by plotting $\ln(I_{ds}/V_{gs})$ vs $1/V_{gs}$ it is possible to extract the trap density in the material from the slope of the curve for each TFT. Fig. 5.6 shows a representative plot. Extraction of the trap density over 21 TFTs yields a value of 7.63×10^{12} cm^{-2} with a standard deviation of 6.89×10^{11} cm^{-2}.

5.4 Conclusion

With this work we demonstrate a method for fabricating fully monolithically integrated 3DICs through ELC on 200 mm wafers for VLSI applications. Lateral transistors fabricated with two-shot SLS show good performance with a threshold voltage

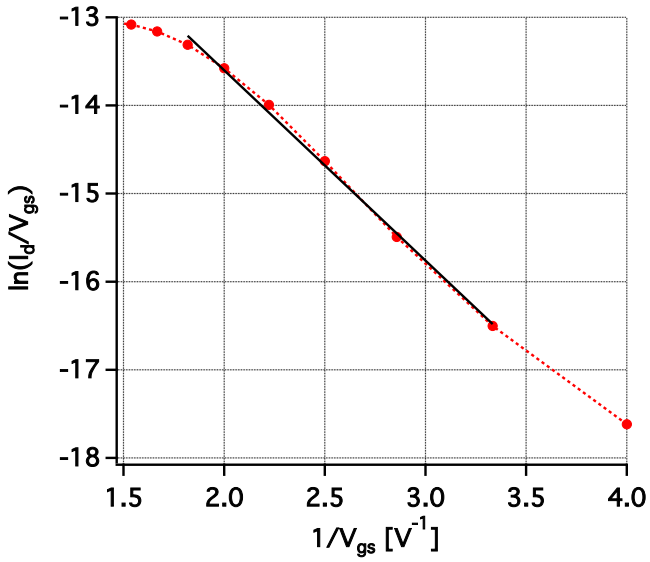


Figure 5.6: Plot of $\ln(I_{ds}/V_{gs})$ vs $(1/V_{gs})$ for a single TFT with a W/L of 1/0.3 μm/μm. From the slope of the curve it is possible to extract the trap density in the TFT channel. For this particular device, the trap density is 8.13×10^{12} cm^{-2}.

of 0.23 V, a maximum current I_d of 26.31 μA/μm, on/off current ratio above 10^5, and a sub-threshold slope of 79.6 mV/decade. From capacitance measurements we extract a C_{ox} of 1.79×10^{-6} F/cm^2 with an equivalent oxide thickness of 2.0 nm. From device characterization over multiple dies we measured the 2σ uniformity, and further characterized the trap density in the material through the Levinson method reporting a mean value of 7.63×10^{12} cm^{-2}. These results demonstrate that two-shot SLS provides performance adequate for a number of applications, while offering several advantages over line scan approaches for device integration including high fabrication throughput and device uniformity.

Chapter 6

Conclusions

6.1 Summary

This thesis demonstrates the use of excimer laser crystallization to achieve the monolithic three dimensional integration of devices in the back end of line process. This work mainly focuses on three key aspects of the fabrication process: 1) Excimer laser crystallization of amorphous silicon thin film on low-κ (i.e. SiCOH) integrated wafers; 2) Excimer laser crystallization of amorphous silicon thin film on back end of line integrated wafers; 3) Integration of thin film transistor on excimer laser crystallized silicon. The laser crystallization part of this work was carried out with two particular techniques: line-scan sequential lateral solidification and two-shot sequential lateral solidification.

The excimer laser crystallization of amorphous silicon thin-film on top of low-κ thermal buffers is experimentally investigated and compared with the crystallization of the similar film on top of more well understood SiO_2 dielectric. Simulations of the different structures under study allow understanding the variation of the laser energy necessary to crystallize the film, which simulation show to be lower when crystallizing film on low-κ dielectrics. Experiments confirmed this energy to be 35% lower for crystallizing silicon thin film deposited low-κ thermal buffer. This difference is mainly

related to the lower thermal conductivity and material density of the SiCOH dielectric. Scanning electron microscopy of the material after Secco defect etch to enhance the grain boundaries contrast, shows a very similar morphology of the polysilicon film on the two thermal buffer at different dielectric thicknesses. This similarity is confirmed through Raman spectroscopy that shows a very similar crystalline ratio in all the structure under study. X-Ray diffraction analysis is used to study the texture of the polysilicon film and show that the silicon grains have a preferential (111) growing direction when crystallized on the SiO_2 film, while the one on SiCOH do not show preferential alignment.

The excimer laser crystallization of a-Si in the BEOL of wafer is problematic mainly because of the presence of buried copper lines. Any process done on a BEOL integrated wafer has to ensure a temperature in the wafer stack below 400°C. This poses a big challenge on both the technique used to deposit the silicon thin-film and the crystallization technique that can be use to crystallize the deposited material. Excimer laser crystallization, due to the short pulse width and the 308 nm wavelength which is mostly absorbed by the top silicon layer, allows crystallization of the film while keeping to a minimum the amount of heat that reaches the Cu interconnect. Simulations of the laser irradiation on a BEOL integrated wafer show that the maximum temperature reached by the Cu lines has a maximum of 320°C when the thermal buffer separating the top silicon layer from the buried copper line is merely 0.25 μm. Experiments demonstrate through Raman spectroscopy the ability to crystallize an a-Si film on top of a BEOL integrated wafer, while electrical characterization of the buried Cu lines show no resistance degradation and optical microscopy confirms no physical degradation either.

Extensive simulation are used to design a fabrication process for thin film devices to meet given spec. TCAD simulations allow to properly choose many of the technological parameter requested during the integration process. Finally, the integration of thin film transistors on top of laser crystallized material shows good performance,

meeting the targeted parameter, and confirm the suitability of this crystallization technique to achieve monolithic 3D integration.

6.2 Future Work

This thesis demonstrate the possibility of integrating devices in the BEOL Cu/lowκ integrated wafers. However, some question still remains open and some details need further study.

While we demonstrate the laser activation of the channel dopant on blanket films, the activation of pocket dopant after self aligned process (therefore with a transistor gate structure in place) still need fine tuning to achieve high percentage activation without damaging the metal gate stack.

A different direction for future work would be a detailed study of the crystallization on low-κ dielectric and why the texture of the material differs from the one achieved in the SiO_2 case. There is also the need to investigate SiCOH decomposition or degradation effect due to the temperature.

Finally, while the device integrated in this work are on recrystallized silicon on bare SiO_2/Si wafers, there is still work that can be done toward integration at wafer scale of devices in both the front end of line device and back end of line their interconnection and performance assessment.

Bibliography

[1] D. Mamaluy, X. Gao, and B. Tierney, "How much time does fet scaling have left?," in *Computational Electronics (IWCE), 2014 International Workshop on*, pp. 1–2, June 2014.

[2] M. Vinet, P. Batude, C. Fenouillet-Beranger, F. Clermidy, L. Brunet, O. Rozeau, J. Hartmannn, O. Billoint, G. Cibrario, B. Previtali, C. Tabone, B. Sklenard, O. Turkyilmaz, F. Ponthenier, N. Rambal, M. Samson, F. Deprat, V. Lu, L. Pasini, S. Thuries, H. Sarhan, J.-E. Michallet, and O. Faynot, "Monolithic 3d integration: A powerful alternative to classical 2d scaling," in *SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2014 IEEE*, pp. 1–3, Oct 2014.

[3] K. J. Kuhn, "Considerations for ultimate cmos scaling," *IEEE Trans. Electron Devices*, vol. 59, no. 7, pp. 1813–1828, 2012.

[4] K. Kuhn, "Cmos scaling for the 22nm node and beyond: Device physics and technology," in *VLSI Technology, Systems and Applications (VLSI-TSA), 2011 International Symposium on*, pp. 1–2, April 2011.

[5] M. Bohr, "The new era of scaling in an soc world," in *Solid-State Circuits Conference-Digest of Technical Papers, 2009. ISSCC 2009. IEEE International*, pp. 23–28, IEEE, 2009.

[6] C.-H. Jan, "10 years of transistor innovations in system-on-chip (soc) era," in *Solid-State and Integrated Circuit Technology (ICSICT), 2014 12th IEEE International Conference on*, pp. 1–4, IEEE, 2014.

[7] A. W. Topol, D. La Tulipe, L. Shi, D. J. Frank, K. Bernstein, S. E. Steen, A. Kumar, G. U. Singco, A. M. Young, K. W. Guarini, *et al.*, "Three-dimensional integrated circuits," *IBM Journal of Research and Development*, vol. 50, no. 4.5, pp. 491–506, 2006.

[8] S. Koester, A. Young, R. Yu, S. Purushothaman, K. Chen, D. La Tulipe, N. Rana, L. Shi, M. Wordeman, and E. Sprogis, "Wafer-level 3d integration technology," *IBM Journal of Research and Development*, vol. 52, pp. 583–597, Nov 2008.

[9] P. Batra, D. LaTulipe, S. Skordas, K. Winstel, C. Kothandaraman, B. Himmel, G. Maier, B. He, D. Gamage, J. Golz, W. Lin, T. Vo, D. Priyadarshini, A. Hubbard, K. Cauffman, B. Peethala, J. Barth, T. Kirihata, T. Graves-Abe, N. Robson, and S. Iyer, "Three-dimensional wafer stacking using cu tsv integrated with 45nm high performance soi-cmos embedded dram technology," in *SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), 2013 IEEE*, pp. 1–2, Oct 2013.

[10] S. Bobba, A. Chakraborty, O. Thomas, P. Batude, V. F. Pavlidis, and G. De Micheli, "Performance analysis of 3-d monolithic integrated circuits," in *3D Systems Integration Conference (3DIC), 2010 IEEE International*, pp. 1–4, IEEE, 2010.

[11] J. Y. Seto, "The electrical properties of polycrystalline silicon films," *Journal of Applied Physics*, vol. 46, no. 12, pp. 5247–5254, 1975.

[12] G. Baccarani, B. Ricco, and G. Spadini, "Transport properties of polycrystalline silicon films," *Journal of applied physics*, vol. 49, no. 11, pp. 5565–5570, 1978.

[13] A. Waxman, V. Henrich, F. Shallcross, H. Borkan, and P. Weimer, "Electron mobility studies in surface space-charge layers in vapor-deposited cds films," *Journal of Applied Physics*, vol. 36, no. 1, pp. 168–175, 1965.

[14] H. Van Heek, "Hall mobility of electrons in the space-charge layer of thin film cdse transistors," *Solid-State Electronics*, vol. 11, no. 4, pp. 459–462, 1968.

[15] R. Graeffe, *Ph.D. Thesis*. Helsinki Technical University, 1969.

[16] T. J. Coutts, *Active and passive thin film devices*. Academic Pr, 1978.

[17] P. Antognetti, *Process and device simulation for MOS-VLSI circuits*. No. 62, Springer Science & Business Media, 1983.

[18] J. Levinson, F. Shepherd, P. Scanlon, W. Westwood, G. Este, and M. Rider, "Conductivity behavior in polycrystalline semiconductor thin film transistors," *Journal of Applied Physics*, vol. 53, no. 2, pp. 1193–1202, 1982.

[19] C. V. D. Wilt, M. G. Kane, a. B. Limanov, a. H. Firester, L. Goodman, J. Lee, J. R. Abelson, a. M. Chitu, and J. S. Im, "Low-temperature poly-si silicon thin-film transistors and circuits on flexible substrates," *MRS Bulletin*, vol. 31, no. June, pp. 461–465, 2006.

[20] T. Sameshima, S. Usui, and M. Sekiya, "Xecl excimer laser annealing used in the fabrication of poly-si tft's," *Electron Device Letters, IEEE*, vol. 7, no. 5, pp. 276–278, 1986.

[21] L. Mariucci, A. Pecora, R. Carluccio, and G. Fortunato, "Advanced excimer laser crystallization techniques," *Thin Solid Films*, vol. 383, no. 1, pp. 39–44, 2001.

[22] A. Voutsas, "Advances in laser annealing technology for poly-si material engineering and ultra-high-performance device fabrication," in *Advanced Thermal Processing of Semiconductors, 2002. RTP 2002. 10th IEEE International Conference of*, pp. 183–191, IEEE, 2002.

[23] R. Bergmann and J. Werner, "The future of crystalline silicon films on foreign substrates," *Thin Solid Films*, vol. 403, pp. 162–169, 2002.

[24] J. S. Im, H. Kim, and M. O. Thompson, "Phase transformation mechanisms involved in excimer laser crystallization of amorphous silicon films," *Applied Physics Letters*, vol. 63, no. 14, pp. 1969–1971, 1993.

[25] J. S. Im and H. Kim, "On the super lateral growth phenomenon observed in excimer laser-induced crystallization of thin si films," *Applied Physics Letters*, vol. 64, no. 17, pp. 2303–2305, 1994.

[26] R. S. Sposili and J. S. Im, "Sequential lateral solidification of thin silicon films on sio2," *Applied Physics Letters*, vol. 69, no. 19, pp. 2864–2866, 1996.

[27] J. S. Im, R. S. Sposili, and M. Crowder, "Single-crystal si films for thin-film transistor devices," *Applied physics letters*, vol. 70, no. 25, pp. 3434–3436, 1997.

[28] A. Limanov, V. Borisov, A. Y. Vinokhodov, A. Demin, A. Eltsov, Y. B. Kirukhin, and O. Khristoforov, "Development of linear sequential lateral solidification technique to fabricate quasi-single-crystal super-thin si films for high-performance thin film transistor devices," in *Perspectives, Science and Technologies for Novel Silicon on Insulator Devices*, pp. 55–61, Springer, 2000.

[29] G. S. Ganot, *Laser Crystallization of Silicon Thin Films for Three-Dimensional Integrated Circuits*. PhD thesis, COLUMBIA UNIVERSITY, 2012.

[30] S. D. Brotherton, M. A. Crowder, A. B. Limanov, B. Turk, and J. S. Im, "Characterization of poly-si tfts in directionally solidified sls si," in *Proc. Asia Display/IDW ',01*, pp. 387–390, 2001.

[31] P. C. Van der Wilt, *Formation of crystalline-silicon islands for thin-film transistors by excimer-laser-induced lateral growth*. TU Delft, Delft University of Technology, 2003.

[32] P. Mei, J. Boyce, M. Hack, R. Lujan, R. Johnson, G. Anderson, D. Fork, and S. Ready, "Laser dehydrogenation/crystallization of plasma-enhanced chemical vapor deposited amorphous silicon for hybrid thin film transistors," *Applied physics letters*, vol. 64, no. 9, pp. 1132–1134, 1994.

[33] J. Förster and H. Vogt, "Excimer laser-annealing of amorphous silicon layers," *Simulation*, vol. 88, p. 90, 2011.

[34] P. Garrou, C. Bower, and P. Ramm, *Handbook of 3d integration: volume 1-technology and applications of 3D integrated circuits*. John Wiley & Sons, 2011.

[35] F. Chen, J. Gill, D. Harmon, T. Sullivan, B. Li, A. Strong, H. Rathore, D. Edelstein, C.-C. Yang, A. Cowley, and L. Clevenger, "Measurements of effective thermal conductivity for advanced interconnect structures with various composite low-k dielectrics," in *Reliability Physics Symposium Proceedings, 2004. 42nd Annual. 2004 IEEE International*, pp. 68–73, April 2004.

[36] A. Grill, V. Patel, K. Rodbell, E. Huang, S. Christiansen, and M. Baklanov, "Characteristics of low-k and ultralow-k pecvd deposited sicoh films.," in *MRS Proceedings*, vol. 716, pp. B12–3, Cambridge Univ Press, 2002.

[37] K. Kitahara, R. Yamazaki, T. Kurosawa, K. Nakajima, and A. Moritani, "Analysis of stress in laser-crystallized polysilicon thin films by raman scattering spectroscopy," *Japanese journal of applied physics*, vol. 41, no. 8R, p. 5055, 2002.

[38] K. Kitahara, T. Ishii, J. Suzuki, T. Bessyo, and N. Watanabe, "Characterization of defects and stress in polycrystalline silicon thin films on glass substrates by raman microscopy," *International Journal of Spectroscopy*, vol. 2011, 2011.

[39] M. Efremov, V. Bolotov, V. Volodin, L. Fedina, and E. Lipatnikov, "Excimer laser and rapid thermal annealing stimulation of solid-phase nucleation and crystallization in amorphous silicon films on glass substrates," *Journal of Physics: Condensed Matter*, vol. 8, no. 3, p. 273, 1996.

[40] P. Lengsfeld, N. Nickel, C. Genzel, and W. Fuhs, "Stress in undoped and doped laser crystallized poly-si," *Journal of applied physics*, vol. 91, no. 11, pp. 9128–9135, 2002.

[41] S.-I. Kuroki, Y. Kawasaki, S. Fujii, K. Kotani, and T. Ito, "Seed-free fabrication of highly bi-axially oriented poly-si thin films by continuous-wave laser crystallization with double-line beams," *Journal of The Electrochemical Society*, vol. 158, no. 9, pp. H924–H930, 2011.

[42] M. Miyasaka and J. Stoemenos, "Excimer laser annealing of amorphous and solid-phase-crystallized silicon films," *Journal of applied physics*, vol. 86, no. 10, pp. 5556–5565, 1999.

[43] J. B. Choi, Y.-J. Chang, C.-H. Park, Y.-i. Kim, J. Eom, H. D. Na, I.-D. Chung, S. H. Jin, Y.-R. Song, B. Choi, *et al.*, "9.2: Sequential lateral solidification (sls) process for large area amoled," in *SID Symposium Digest of Technical Papers*, vol. 39, pp. 97–100, Wiley Online Library, 2008.

[44] C.-W. Kim, K.-C. Moon, H.-J. Kim, K.-C. Park, C.-H. Kim, I.-G. Kim, C.-M. Kim, S.-Y. Joo, J.-K. Kang, and U.-J. Chung, "21.4: Development of sls-based system on glass display," in *SID Symposium Digest of Technical Papers*, vol. 35, pp. 868–871, Wiley Online Library, 2004.

[45] D. Kaplan, N. Sol, G. Velasco, and P. Thomas, "Hydrogenation of evaporated amorphous silicon films by plasma treatment," *Applied Physics Letters*, vol. 33, no. 5, pp. 440–442, 1978.

[46] J. Pankove, M. Lampert, and M. Tarng, "Hydrogenation and dehydrogenation of amorphous and crystalline silicon," *Applied Physics Letters*, vol. 32, no. 7, pp. 439–441, 1978.

[47] Y. Uchida, H. Kanoh, O. Sugiura, and M. Matsumura, "Hydrogen-radical annealing of chemical vapor-deposited amorphous silicon films," *Japanese journal of applied physics*, vol. 29, no. 12A, p. L2171, 1990.

[48] B.-C. Ahn, K.-I. Usami, H. Kanoh, O. Sugiura, and M. Matsumura, "The effects of post-hydrogenation on amorphous-silicon thin-film transistors," *Electronics and Communications in Japan (Part II: Electronics)*, vol. 76, no. 10, pp. 66–73, 1993.

[49] R. S. Dahiya, G. Metta, M. Valle, A. Adami, and L. Lorenzelli, "Piezoelectric oxide semiconductor field effect transistor touch sensing devices," *Applied Physics Letters*, vol. 95, no. 3, p. 034105, 2009.

[50] K. Ren, S. Liu, M. Lin, Y. Wang, and Q. Zhang, "A compact electroactive polymer actuator suitable for refreshable braille display," *Sensors and Actuators A: Physical*, vol. 143, no. 2, pp. 335–342, 2008.

[51] F. Xia, R. Klein, F. Bauer, and Q. Zhang, "High performance p (vdf-trfe-cfe) terpolymer for biomems and microfluidic devices," in *MRS Proceedings*, vol. 785, pp. D5–8, Cambridge Univ Press, 2003.

[52] K. H. Lee, G. Lee, K. Lee, M. S. Oh, S. Im, and S.-M. Yoon, "High-mobility nonvolatile memory thin-film transistors with a ferroelectric polymer interfacing zno and pentacene channels," *Advanced Materials*, vol. 21, no. 42, pp. 4287–4291, 2009.

[53] I. Graz, M. Kaltenbrunner, C. Keplinger, R. Schwödiauer, S. Bauer, S. P. Lacour, and S. Wagner, "Flexible ferroelectret field-effect transistor for large-area sensor skins and microphones," *Applied physics letters*, vol. 89, no. 7, p. 073501, 2006.

[54] T. Levard, P. J. Diglio, S.-G. Lu, C. D. Rahn, and Q. Zhang, "Core-free rolled actuators for braille displays using p (vdf–trfe–cfe)," *Smart Materials and Structures*, vol. 21, no. 1, p. 012001, 2012.

[55] Z.-Y. Cheng, V. Bharti, T.-B. Xu, H. Xu, T. Mai, and Q. Zhang, "Electrostrictive poly (vinylidene fluoride-trifluoroethylene) copolymers," *Sensors and Actuators A: Physical*, vol. 90, no. 1, pp. 138–147, 2001.

[56] Y.-J. Hsu, Z. Jia, and I. Kymissis, "A locally amplified strain sensor based on a piezoelectric polymer and organic field-effect transistors," *Electron Devices, IEEE Transactions on*, vol. 58, no. 3, pp. 910–917, 2011.

[57] Q. Zhang, V. Bharti, and X. Zhao, "Giant electrostriction and relaxor ferroelectric behavior in electron-irradiated poly (vinylidene fluoride-trifluoroethylene) copolymer," *Science*, vol. 280, no. 5372, pp. 2101–2104, 1998.

[58] C. Huang, R. Klein, F. Xia, H. Li, Q. Zhang, F. Bauer, and Z. Cheng, "Poly (vinylidene fluoride-trifluoroethylene) based high performance electroactive polymers," *Dielectrics and Electrical Insulation, IEEE Transactions on*, vol. 11, no. 2, pp. 299–311, 2004.

[59] F. Bauer, E. Fousson, and Q. Zhang, "Recent advances in highly electrostrictive p (vdf-trfe-cfe) terpolymers," *Dielectrics and Electrical Insulation, IEEE Transactions on*, vol. 13, no. 5, pp. 1149–1154, 2006.

[60] S.-J. Kim and I. Kymissis, "An electrostrictive high dielectric constant fluorinated terpolymer sheet fabricated by a melt and stretch extrusion process," *Journal of materials science*, vol. 45, no. 24, pp. 6834–6836, 2010.

[61] S. P. Lacour, H. Prahlad, R. Pelrine, and S. Wagner, "Mechatronic system of dielectric elastomer actuators addressed by thin film photoconductors on plastic," *Sensors and Actuators A: Physical*, vol. 111, no. 2, pp. 288–292, 2004.

[62] Z. Jia, V. W. Lee, Y.-J. Hsu, and I. Kymissis, "Laboratory pentacene and parylene evaporation systems for fabricating organic thin film devices," *Journal of Vacuum Science & Technology B*, vol. 29, no. 2, p. 022401, 2011.

[63] E. Fortunato, N. Correia, P. Barquinha, L. Pereira, G. Gonçalves, and R. Martins, "High-performance flexible hybrid field-effect transistors based on cellulose fiber paper," *Electron Device Letters, IEEE*, vol. 29, no. 9, pp. 988–990, 2008.

[64] T.-B. Xu, Z.-Y. Cheng, and Q. Zhang, "High-performance micromachined unimorph actuators based on electrostrictive poly (vinylidene fluoride–trifluoroethylene) copolymer," *Applied physics letters*, vol. 80, no. 6, pp. 1082–1084, 2002.

[65] L. Dobrescu, M. Petrov, and C. Ravariu, "Threshold voltage extraction methods for mos transistors," in *Semiconductor Conference, 2000. CAS 2000 Proceedings. International*, vol. 1, pp. 371–374, IEEE, 2000.

[66] I. Kymissis and A. I. Akinwande, "Organic field emission device integrated with organic transistor," *Electron Devices, IEEE Transactions on*, vol. 52, no. 8, pp. 1907–1914, 2005.

[67] P. Heremans, J. Genoe, S. Steudel, K. Myny, S. Smout, P. Vicca, C. Grillberger, O. R. Hild, F. Furthner, B. van der Putten, *et al.*, "Thin-film transistors and circuits on plastic foil," in *Proceedings of the International Electron Devices Meeting-IEDM*, pp. 371–374, 2009.

[68] K. Myny, M. J. Beenhakkers, N. A. van Aerle, G. H. Gelinck, J. Genoe, W. Dehaene, and P. Heremans, "A 128b organic rfid transponder chip, including manchester encoding and aloha anti-collision protocol, operating with a data rate of 1529b/s," in *IEEE International, Solid-State Circuits Conference, 2009*, pp. 206–207, IEEE, 2009.

[69] K. Myny, E. van Veenendaal, G. H. Gelinck, J. Genoe, W. Dehaene, and P. Heremans, "An 8b organic microprocessor on plastic foil.," in *IEEE International, Solid-State Circuits Conference, 2011*, pp. 322–324, 2011.

[70] M. Jung, J. Kim, J. Noh, N. Lim, C. Lim, G. Lee, J. Kim, H. Kang, K. Jung, A. D. Leonard, *et al.*, "All-printed and roll-to-roll-printable 13.56-mhz-operated 1-bit rf tag on plastic foils," *Electron Devices, IEEE Transactions on*, vol. 57, no. 3, pp. 571–580, 2010.

[71] J. Noh, D. Yeom, C. Lim, H. Cha, J. Han, J. Kim, Y. Park, V. Subramanian, and G. Cho, "Scalability of roll-to-roll gravure-printed electrodes on plastic foils," *Electronics Packaging Manufacturing, IEEE Transactions on*, vol. 33, no. 4, pp. 275–283, 2010.

[72] W. Zhang, M. Ha, D. Braga, M. J. Renn, C. D. Frisbie, and C. H. Kim, "A 1v printed organic dram cell based on ion-gel gated transistors with a sub-10nw-per-cell refresh power," in *IEEE International, Solid-State Circuits Conference, 2011*, pp. 326–328, IEEE, 2011.

[73] E. Cantatore, T. C. Geuns, G. H. Gelinck, E. van Veenendaal, A. F. Gruijthuijsen, L. Schrijnemakers, S. Drews, and D. M. de Leeuw, "A 13.56-mhz rfid system based on organic transponders," *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 1, pp. 84–92, 2007.

[74] M. Seok, "Performance and energy-efficiency improvement through modified cpl in organic transistor integrated circuits," in *ACM/IEEE International, Symposium on Low power electronics and design, 2012*, pp. 215–220, ACM, 2012.

[75] I. Kymissis, C. Dimitrakopoulos, and S. Purushothaman, "High-performance bottom electrode organic thin-film transistors," *Electron Devices, IEEE Transactions on*, vol. 48, no. 6, pp. 1060–1064, 2001.

[76] D. J. Gundlach, L. L. Jia, and T. N. Jackson, "Pentacene tft with improved linear region characteristics using chemically modified source and drain electrodes," *Electron Device Letters, IEEE*, vol. 22, no. 12, pp. 571–573, 2001.

[77] H. Klauk, U. Zschieschang, J. Pflaum, and M. Halik, "Ultralow-power organic complementary circuits," *Nature*, vol. 445, no. 7129, pp. 745–748, 2007.

[78] I. Kymissis, C. D. Dimitrakopoulos, and S. Purushothaman, "Patterning pentacene organic thin film transistors," *Journal of Vacuum Science & Technology B*, vol. 20, no. 3, pp. 956–959, 2002.

Appendix A

Electroactive polymer actuator with monolithically integrated OFETs control

A.1 Introduction

Electroactive polymers (EAP) that respond to electric fields and mechanical stimulation through piezoelectric and/or electrostrictive effects have found application in a range of devices [49; 50; 51; 52; 53; 54; 55; 56]. Poly-(vinylidene fluoride) (PVDF) and its copolymer with trifluoroethylene (PVDF-TrFE) are among the most explored polymer ferroelectric materials in this class. PVDF-TrFE copolymers show a ferroelectric-paraelectric transition associated with a large strain (10%) and a large ferroelectric hysteresis cycle [57; 58]. It has been shown that modifying the PVDF-TrFE copolymer by addition of a third monomer, chlorofluoroethylene (CFE), can convert the material to a relaxor ferroelectric eliminating the hysteresis cycle but retaining the polarizability associated with this class of materials [58; 59]. This allows the formation of a low modulus high-dielectric constant polymer sheet with outstanding electrostrictive properties. Large sheets of the material can be formed from suspensions of the

polymer or through melt-stretch extrusion of the terpolymer resin [60].

There has been some work exploring the use of this electrostrictive PTC terpolymer material to effect macroscopically significant mechanical actuations under external electrical control. Cheng [55], for example, shows a macroscopic displacement of a unimorph structure under 65 V/μm actuation across a 22 μm thick PVDF-TrFE layer; for a total bias voltage around 1.4 kV. While this level of voltage is suitable for a range of applications, creating an active matrix and providing digital control of such systems requires signaling at significantly smaller voltages than applied to the electrostrictor material. A possible solution is the use of photoconductor switches [61], but their monolithically integration on the EAP requires the deposition of additional layers that can reduce the achievable strain. We have demonstrated a PTC bimorph actuator that monolithically integrates two CMOS organic field effect transistor (OFET)-based level shifters to apply a high electric field to each layer of the structure under a reduced control voltage in the system. This permits bending control of the bimorph to be managed by low-voltage electronics while achieving macroscopic displacement in the electrostrictor bimorph system.

A.2 Material and methods

Stretched PTC sheets were provided by Strategic Polymer Sciences of State College PA; their properties are reported in table A.1. The minimum thickness of the film is 3μm.

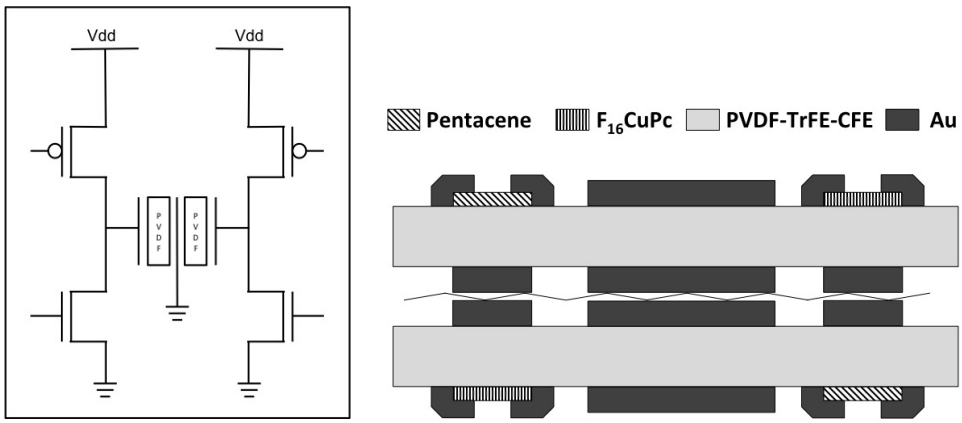
While the PTC is a highly stable material, all of the fabrication steps have been performed inside a glovebox cluster that is continuously scrubbed for water vapor, oxygen, and particles. This protects the organic semiconductors and reduces the risk of particle incorporation at interfaces causing catastrophic defects under high voltage bias. The PTC sheet is mounted in a custom tensioned frame structure. 40nm gold electrodes are deposited on the PTC, which serve as electrodes for the terpolymer

Property	Value
Strain [100V/μm]	2.5%
Young's Modulus [MPa]	700
Dielectric Constant	45
Dielectric Loss	5%
Minimum Film Thickness [μm]	3

Table A.1: Properties of the PVDF-TrFE-CFE layer.

actuators and gate electrodes for the transistors. On the opposite surface of the PTC layer the control transistors are deposited with a top electrode configuration (figure A.1). The n-type transistors are fabricated using F16CuPc (Lumtec) and the p-type devices are fabricated using pentacene (Lumtec). Both of the semiconductor layers are 30nm thick and the transistors have been designed with W/L=2000 μm / 100μm. The pentacene is evaporated in a custom made evaporator that is integrated with the golvebox and allows us to reach high-vacuum ($<10^{-7}$ torr) and deposit with a low deposition rate ($\approx$1 angstrom/sec) to optimize the process [62]. After the deposition of the top source/drain electrodes, two identical unimorph structures are thermally bonded together to form a bimorph in a thermal press at 100°C for 40 minutes under a 1000 pound load. The exposed polymer regions fuse under these conditions, and the gold electrodes appear to weld during this lamination process, forming a single central electrode.

Another PTC sample is fabricated without controlling OFET and used to characterize the properties of the electrostrictive material.



(a) (b)

Figure A.1: a) Schematic of the controlling circuit. Two organic CMOS circuit control the output voltage applied across the PTC layer. b) Crossection of the bimorph. The PTC sheets are laminated together through thermal bonding.

A.3 Results and discussion

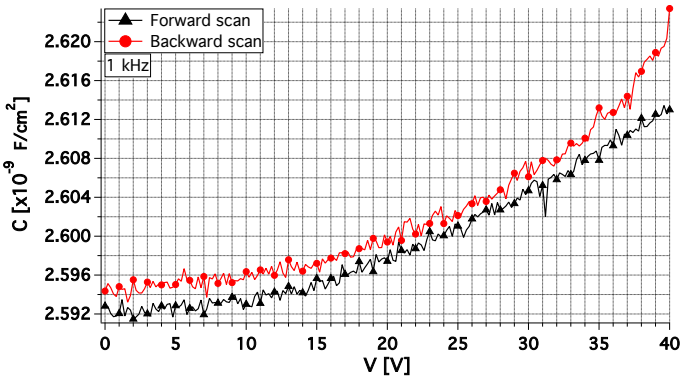
Figure A.2 reports the results from the characterization of the electroded PTC without an OFET. These sample dimensions correspond to the dimensions of the electrodes used to actuate the material in the bimorph structure. In Figure A.2a, the C-V measurement of the PVDF layer is reported with the measurement taken at 1KHz. This measurement shows the level of strain achieved in the film. When an electric field is applied across the material, a thickness decrease (and a corresponding extension along the oriented stretched direction) is observed, which can also be measured through capacitance. Figure A.2a shows the measurement taken as both a forward and backward voltage scan ranging from 0 V to 40 V. Both the variation of capacitance related to the electrostrictive modulation of the thickness and the lack of ferroelectric hysteresis through incorporation of the CFE in the terpolymer system can be observed. In Figure A.2b the capacitance characteristic of the dielectric layer in the 100Hz - 100 MHz range is shown. A capacitance of 6.4 nF can be observed at low frequencies. The 3 dB bandwidth of the electrostrictive material is around 90

KHz. Figure A.2c presents a 40 V I-V sweep across the electrostrictive layer. At 40 V the leakage current has its maximum value around 5×10^{-10} A, demonstrating a suitable characteristic for use as a dielectric layer in the TFTs employed in the level shifting circuit.

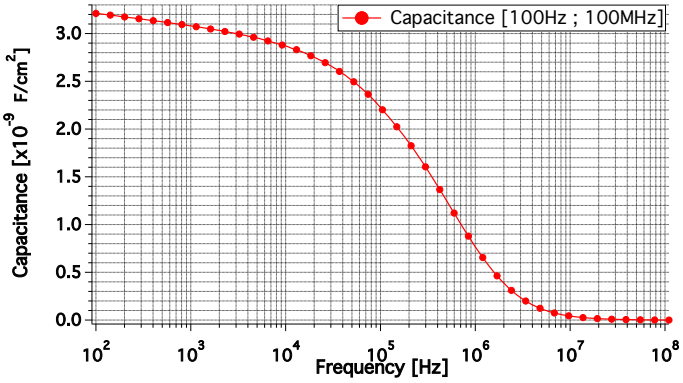
The need for high electric field across the PTC during its mechanical actuation requires the use of an OFET capable of handling high voltages across the gate, source, and drain electrodes. This implies the use of a dielectric layer that has a high-κ and sufficient thickness and voltage breakdown resistance to permit actuation. The use of an additional gate dielectric layer however, would clamp the film and limit the displacement achievable by the terpolymer sheet. A solution is to use the terpolymer material itself as the gate dielectric of the control transistors. The idea of using the substrate as the gate dielectric of an FETs has been previously explored; this layer is also called an interstrate by some groups [63].

The intrinsic strain capability of the PTC copolymer layer is 2.5% at 100 V/μm. Because of the clamping effect of the electrode layers and bonding with the mating polymer, the effective strain in the final device is reduced. This reduction can be computed following [50; 64] and taking into account the ratio of the Young's modulus of the various materials and their thicknesses. Minimizing the number of layers is important to get the maximum deflection from the structure. Our devices minimize the number of layer necessary using the same material as substrate, dielectric layer, and actuating material.

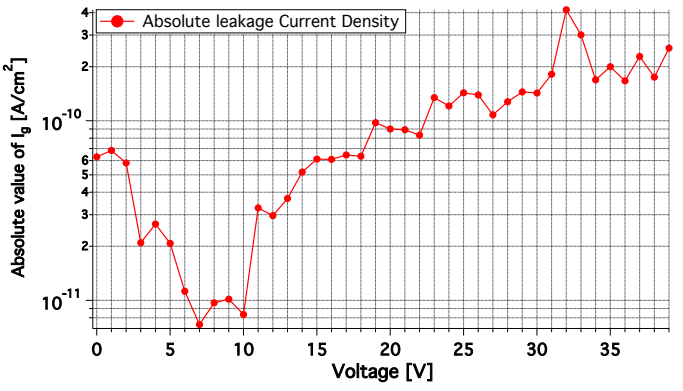
The OFETs used have been characterized and the curves are reported in figure A.3. The OFETs show reasonable performance for devices with a low-capacitance gate dielectric. The field effect mobility of the transistors is computed from the output curve and is found to be 0.012 $cm^2/(V\times s)$ for the pentacene transistor and 0.0015 $cm^2/(V\times s)$ for the F_{16}CuPc transistor. The one order of magnitude difference between the p-type and n-type semiconductor mobilities observed is consistent with other values reported in literature. The threshold voltages are extracted from



(a)



(b)



(c)

Figure A.2: PVDF-TrFE-CFE characterization: a) Capacitance Vs Voltage, measured at 1 KHz. b) Capacitance Vs Frequency. c) Leakage current Vs Voltage.

the transfer characteristic following the linear extrapolation method in the saturation region [65] and are found to be -5 V for the p-type semiconductor and 10 V for the n-type device. Forward and backward I_D vs V_{DS} measurement did not show any difference, confirming that the incorporation of the third monomer CFE in the polymeric structure switch the behavior of the material from ferroelectric to electrostrictive.

The bias levels for the system were selected to allow complementary switching of the devices and charge/discharge of the capacitor formed by the electrostrictor element. Figure A.4 shows the input-output characteristic of the level shifter; a V_{GS} of 60 V supports a V_{OUT} of 199 V. This structure can be scaled to higher V_{DD} voltages (see, for example [66]). The transconductance difference between the n-OFET and p-OFET leads to an asymmetry in the charge/discharge time.

The setup for the characterization of the bimorph structure includes a side camera from which pictures are taken to measure the radius of curvature of the electrostrictor. Table A.2 reports the extracted parameter together with the controlling values. It can be observed that the radius of curvature decreases as the V_{DD} increases, indicating a strain increase in the active layer. The measured strain is smaller than the strain nominally expected from the PTC and measured in a unimorph. This is due to the clamping effect of the electrodes deposited on each side of the film, together with the clamping effect of the second inactive actuator layer with its electrodes. A macroscopic displacement of the bimorph structure occurs when a high electric field is applied across the active layer, curling the structure entirely with a radius of curvature of 7.5 mm along a length of 2 cm.

A.4 Conclusions

We have investigated a P(VDF-TrFE-CFE) polymer bimorph structure controllable with low voltage through an integrated CMOS OFET control system. The electrostrictor material is used as substrate, dielectric layer for the control circuitry, and

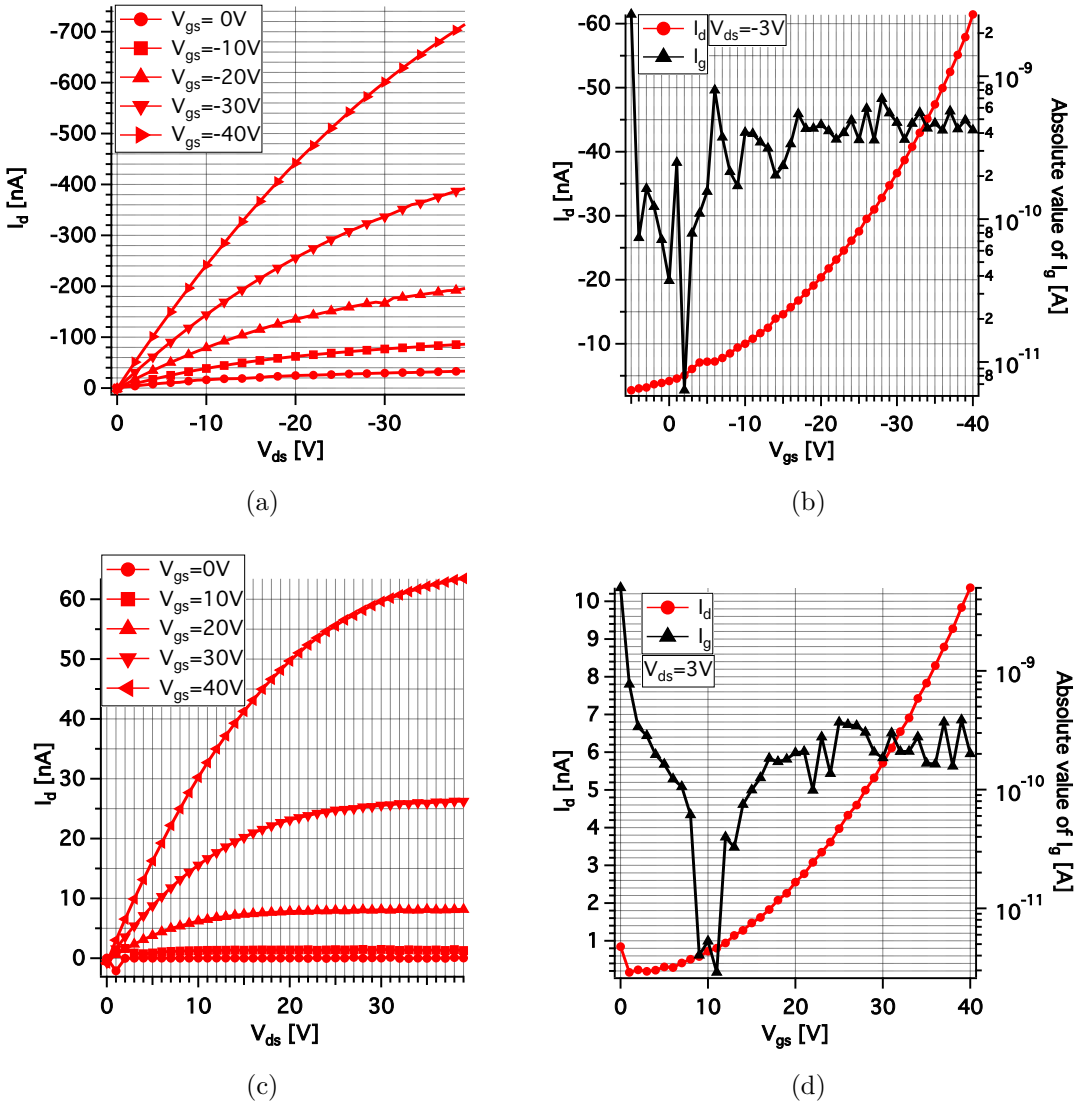


Figure A.3: Characterization curves of the monolithically integrated OFETs with electrostrictive dielectric. a) and c) are the output curves of the Pentacene and F_{16}CuPc TFTs respectively. b) and d) are the trans-characteristic of the Pentacene and F_{16}CuPc TFTs respectively.

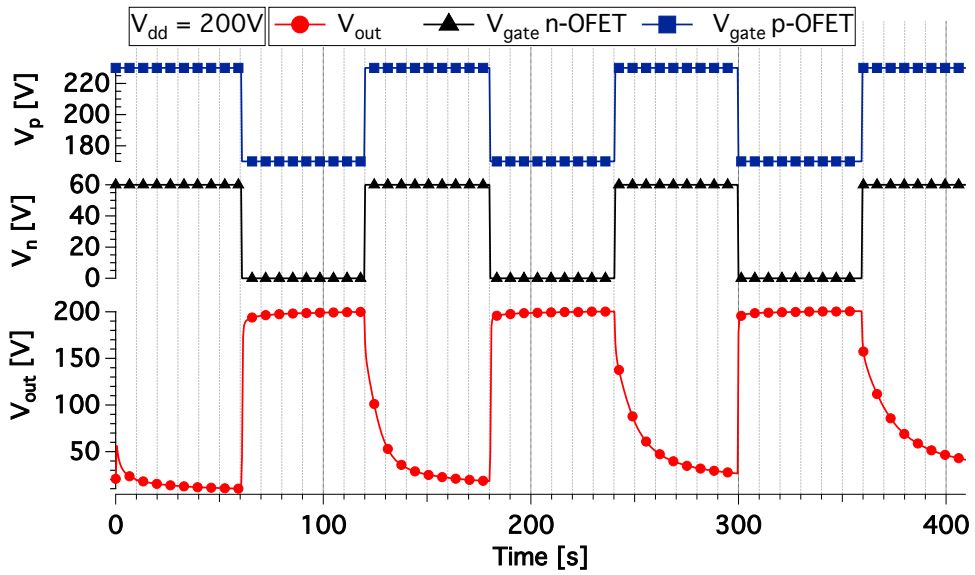


Figure A.4: Level shifter output characteristic. The controlling circuit outputs 199 V when the p-OFET is in ON condition and the n-OFET is OFF, while it outsources 18 V when the n-OFET is ON and the p-OFET is OFF.

$\mathbf{V}_{DD}$ [V]	$\mathbf{V}_{GS-p}$ [V]	$\mathbf{V}_{GS-n}$ [V]	ρ [mm]	ϵ [%]
200	220-160	0-60	11.4	0.043
250	270-210	0-60	10.5	0.047
300	330-260	0-70	9	0.055
400	430-360	0-70	7.5	0.078

Table A.2: Bimorph characterization table. V_{GS-p} refer to the gate-source voltage applied on the pTFT, V_{GS-n} on the nTFT, ρ is the radius of curvature and ϵ is the strain measured in percentage on the top film surface.

as an active mechanical layer for the bimorph structure. The design allows the OFET to sustain the high voltage required for actuation and minimizes the number of layers in the structure maximizing the observed displacement. The device is actuated by applying a V_{DD} voltage up to 400 V, and a 60 - 70 V signal is used for switching the electric field applied across the terpolymer. The radius of curvature of the actuated structure ranges from 11.4 mm under $V_{DD} = 200$ V to 7.5 mm under a bias of 400 V. The strain level reduction from that observed in the PTC polymer film is caused by the clamping effect of the electrode layers and of the mating inactive unimorph. This architecture can be scaled to larger systems with more sites controlled using commercial silicon electronics-compatible controlling voltages and higher V_{DD} voltages to further increase the observed strain.

Appendix B

Organic electronic circuits for digital applications

B.1 Introduction

Organic field effect transistors (OFETs) have gained significant interest due to their proprieties, many of which are not available in silicon technologies, including mechanical flexibility [67; 68; 69; 70; 71], low-temperature processing, roll-to-roll processability [70; 71], large area coverage, biocompatibility, light weight, and low cost. In spite of the significant progress in organic electronics, OFETs still face challenges. N-type semiconductors have inferior performance when compared with their p- counterparts, both in terms of mobility ($> 10\times$ lower in n-devices) and threshold voltages. The lack of a good n-type semiconductor among organic materials, complicates the integration of complementary metal-oxide semiconductor (CMOS) for logic applications. While in silicon technology p-type devices are moderately weaker ($\sim 2\times$) and upsized to balance the rise and fall delay, in organic electronics the strong strength imbalance forces designers to upsize the n-type by $10\times$ (or more) to keep the resistivity comparable in the pull-down and pull-up networks, increasing self-loading and area overhead.

Different ways to approach this problem exist. One solution involves the use of resistor-load gates [72] or a zero-V_{gs} saturated load [68; 73]. These techniques use only p-type OFETs to implement digital gates, eliminating the problems related to the use of n-type semiconductors. Although they solve the area and self-loading problem, they suffer from other limitations such as large static current, high power consumption and limited output swing [74].

In order to mitigate this challenges, we propose a modified complementary pass-transistor logic (mCPL) family (figure B.1) extending from our prior simulation-based work [74]. We introduce mCPL inverters which use both n- and p-type OFETs in the pull-down network. The p-OFET in the pull-down branch helps the n-type OFET in switching the output node, reducing the fall delay. The mCPL design also allows for an equal sizing of the p- and n- OFETs in the inverter design reducing the area overhead, and making the design more robust toward process variations. This also allows for the use of smaller devices while significantly improving delay and efficiency. mCPL NAND and NOR gates are designed such that their critical paths are dominated mostly by p-OFETs, improving switching times. mCPL is also characterized by dual inputs and outputs. This dual rail causes more wiring overhead but provides a free logic inversion. Although basic NOR and NAND designs do not include an inverter as their final stage, buffering between inputs and outputs is important for large-scale cascaded gate integration. To improve this buffering we included an mCPL inverter in the single logic gate design.

All the fabricated and tested mCPL gates have demonstrated significantly better performance than the CMOS counterparts.

B.2 Materials and methods

Figure B.2 shows the cross-section of the fabricated device. OFETs are fabricated using a bottom gate/bottom contact configuration. This configuration usually offers

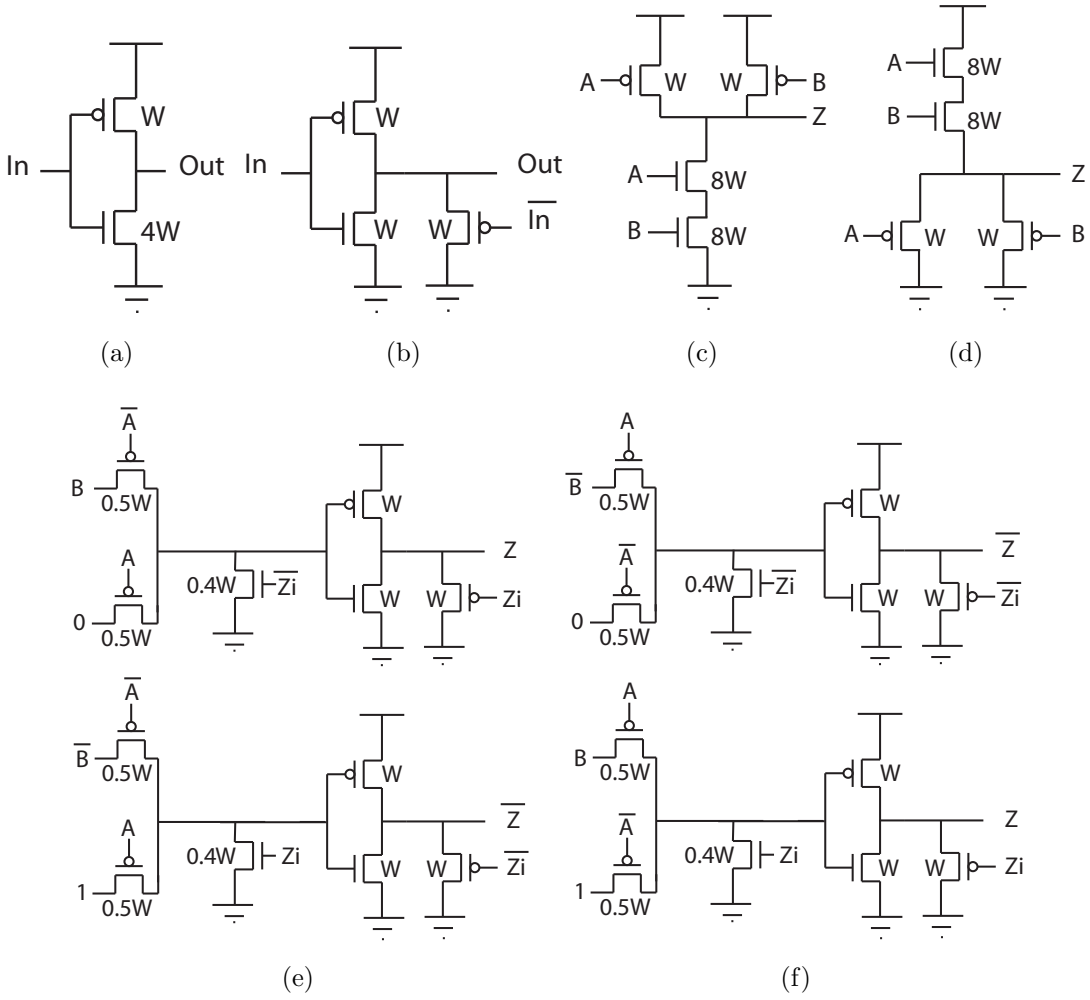


Figure B.1: Design schematic of a) CMOS inverter; b) mCPL inverter; c) CMOS NAND gate; d) CMOS NOR gate; e) mCPL NAND gate; f) mCPL NOR gate.

worse performance when compared with bottom gate/top contact approaches [75; 76]. On the other hand, the difficulties inherent in patterning organic semiconductors with conventional photolithographic processes generally limit the configuration choice to the bottom gate/bottom contact arrangement. All the device compared in this work are fabricated with the same FETs configuration and are integrated on the same substrate.

5 nm Cr and 50 nm Au metallization is deposited on top of a glass substrate through thermal evaporation. The Cr layer acts as adhesion layer for the subsequent Au deposition. The Au has a reasonably matching work function for charge injection into organic FETs, which makes it the most common choice for electrodes. The first metal layer is then patterned through photolithography and a wet etching process providing electrodes for the OFETs and wiring interconnection. 20 nm of Al_2O_3 is deposited through atomic layer deposition (ALD) at 150°C to provide a high quality layer as a gate oxide. Via openings are etched through the oxide using a CHF_3-based dry etch in an inductively coupled plasma (ICP) etcher. 5 nm of Cr and 50 nm Au are deposited and patterned on top of the oxide layer.

A self-assembled monolayer (SAM) (n-octadecylphosphonic acid, Strem chemicals) is then selectively deposited on the gate oxide by soaking the substrate in a 5 mM solution of phosphonic acid in isopropyl alcohol for 3 hours [77]. The SAM layer promotes a good molecular stacking for the p-semiconductor deposition, improving the effective mobility, subthreshold characteristics, and energy efficiency. 40 nm of pentacene (Lumtec) is evaporated in a custom made evaporator integrated in a glove-box which allows evaporation under high-vacuum ($< 10^{-7}$ torr) and low deposition rates (≈ 0.1 angstrom/sec) [62] to optimize the semiconductor deposition. 250 nm of parylene-C (pary-C, Specialty Coating Systems) is deposited through chemical vapor deposition (CVD) on top of the pentacene layer to allow its patterning [78] and to retard degradation of the device. The pary-C layer act as a barrier layer, protecting the pentacene from photoresist and solvent exposure during its patterning. The pary-

Parameters	**Value**
W_p [μm]	250
W_n / W_p (CMOS design)	4
W_n / W_p (mCPL design)	1
L_n , L_p [μm]	15
t_{ox} [nm]	20

Table B.1: Design parameter for the CMOS and mCPL circuits.

C and pentacene layer is selectively etched with an O_2 plasma in a ICP etcher. The photoresist is left on top of the parylene to avoid exposure to photoresist stripping, which can damage the semiconducting layer. As last step 40 nm of F_{16}CuPc (Lumtec) are thermally deposited on the structure at $\approx$ 0.1 angstrom/sec. Table B.1 reports the parameters used in the designing of the circuitry.

B.3 Results

Ellipsometry on the the Al_2O_3 dielectric layer measures a thickness of 20 nm. The oxide capacitance for the two different OFETs present different values. In the case of p-OFET the gate capacitance is a combination of the SAM layer and ALD oxide with a measured total capacitance of (349$\pm$0.988) nF/cm^2, while for the n-OFET the total capacitance is (416$\pm$0.472) nF/cm^2 and is only related to the Al_2O_3 layer.

Figure B.3 shows the typical transfer and output curves of the fabricated p-OFET and n-OFET. Table B.2 shows the measured and extracted parameters for 10 p-OFETs and 10 n-OFETs. The leakage current shows values in the 10^{-10} A range at maximum driving voltages $|V_{GS}| = |V_{DS}| = 6$ V. The field effect mobility in the saturation region of the p-type transistors is up to 40$\times$ higher than the n-type devices. Threshold voltages are extracted in the saturation region following the linear

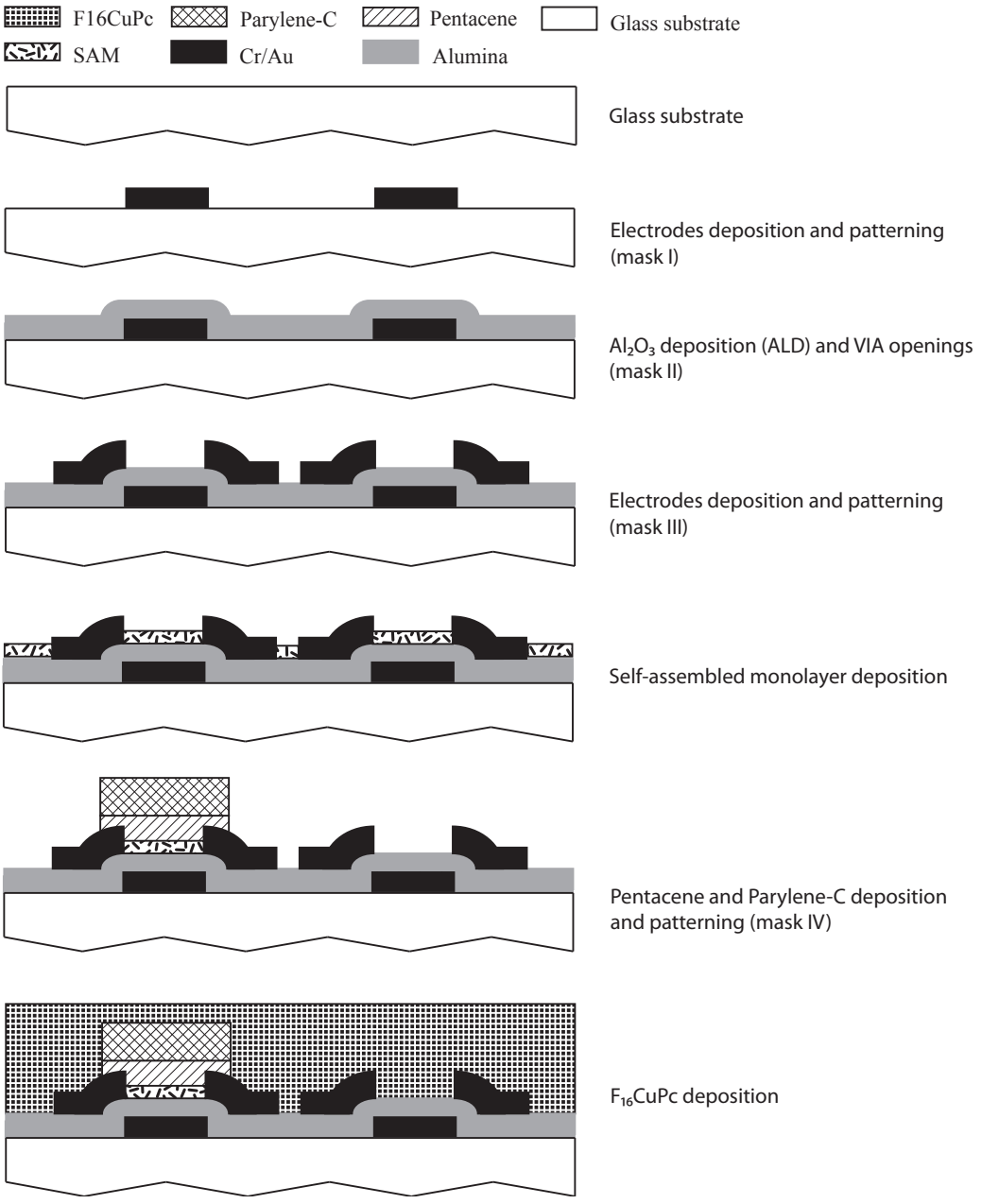


Figure B.2: Cross-section of the fabricated device

Parameters	**pFET mean values**	**nFET mean values**
Drain current [A]	$(2.44\pm0.11)\times10^{-06}$	$(2.39\pm0.42)\times10^{-08}$
Leakage current [A]	$(2.04\pm0.26)\times10^{-10}$	$(5.68\pm1.84)\times10^{-10}$
Threshold voltage [V]	0.69 ± 0.06	2.13 ± 0.12
Mobility [$cm^2/(V \times s)$]	$(1.89\pm0.08)\times10^{-02}$	$(4.84\pm1.03)\times10^{-04}$

Table B.2: Measured and extracted OFET parameter. Each value represent the average and standard error of a population of 10 OFETs.

extrapolation method [65]. The maximum drain current at $|V_{GS}| = |V_{DS}| = 6$ V, shows two orders of magnitude difference between the two devices. The different ratio between field effect mobility and driving current is related to the different threshold voltage in the two types OFETs as well as a the presence of the SAM in the p-OFET case which improves the molecular stacking and therefore field effect mobility of the pentacene.

In classic CMOS inverter designs, the ratio of driving current would force the designer to make the width of the n-type FET 100× the width of the p-FET to keep the resistance in the two network branches comparable. In the mCPL inverter design, however, the p-FET in the pull-down network allows us to keep a 1:1 ratio between the p- and n- FETs, reducing the device footprint. Figure B.1 and table B.1 illustrate the schematic and the sizes of the devices for the different logic gates.

Figure B.4 reports the voltage transfer curve (VTC) of the inverter in CMOS and mCPL. The two curves plot the mean value and standard error of 10 different devices in each logic. The standard deviation for the two logic gates has a maximum value of 1.14 in the CMOS case and 0.32 in the mCPL, which shows the improved robustness against process variation of the newly proposed logic architecture. Figure B.4 also shows how the mCPL allows for a better swing for the output curve, however this can be related to both differences in the threshold voltage in the two types OFETs as well

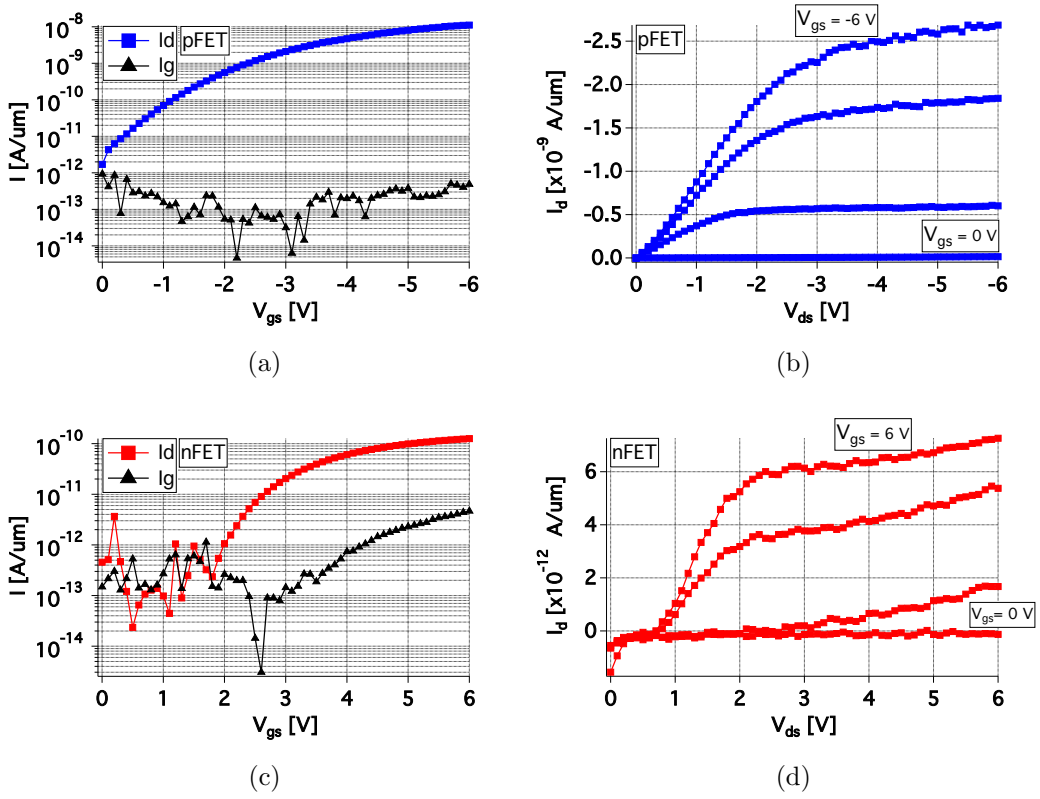


Figure B.3: a) pOFET transfer curve; b) pOFET output curve; c) nOFET transfer curve; d) nOFET output curve.

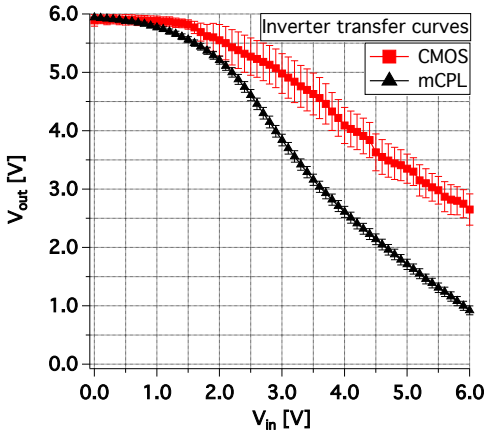
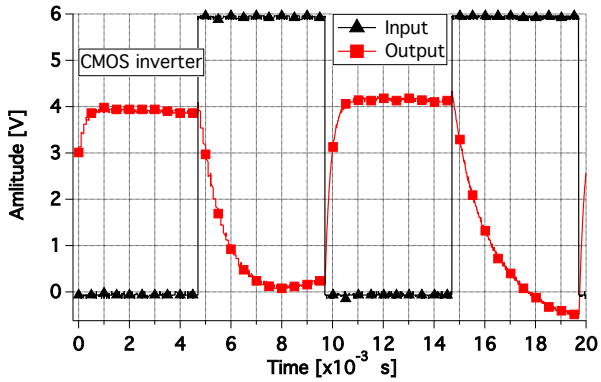


Figure B.4: Transfer curve of a single stage inverter for both CMOS and mCPL logics. The mCPL exhibits an output swing closer to a rail-to-rail voltage.

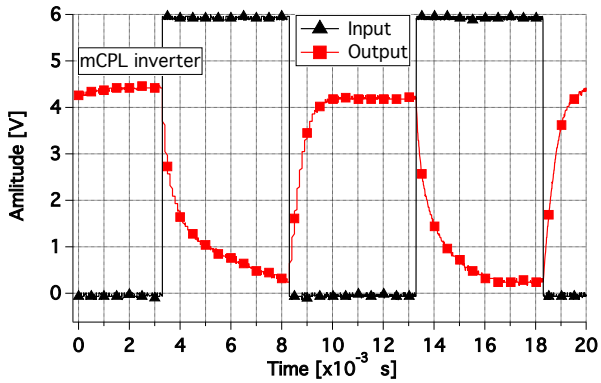
as the CMOS inverter OFETs sizing which is not robust toward process variations.

Figure B.5 illustrates the frequency output characteristic of the two logic styles, which confirms the enhanced swing in the mCPL case. The frequency characteristic of the inverters are measured at the output of an inverter stage which is loaded with other four inverters of the same architecture (using a fan out of 4) to provide a realistic load to the circuit. Figure B.6 shows the slew rates and delay both for the falling and rising cases in the two architectures. The mCPL circuit outperforms the CMOS in all metrics with a 1.5× better rise and fall slew rates, 1.2× better rise delay and 2.5× better fall delay.

In the characterization of the NAND and NOR gate for the two logic styles, each gate is loaded with a capacitance representing the input capacitance of another stage. The input capacitance value in the case of the CMOS gates is 45 pF while in the mCPL design it is 15 pF. Figure B.7 shows the comparison of the slew rates and delay for the NOR and NAND gate implemented in both logic families. An accurate measurement for the delay and slew rates in logic gates uses the least number of branches in the logical path to switch the output node. At the same time, one should switch the device involving the highest number of capacitors to evaluate the worst



(a)



(b)

Figure B.5: a) 100 Hz output characteristic of a CMOS single stage inverter loaded with Fan Out of 4. b) 100 Hz output characteristic of a mCPL single stage inverter loaded with Fan Out of 4.

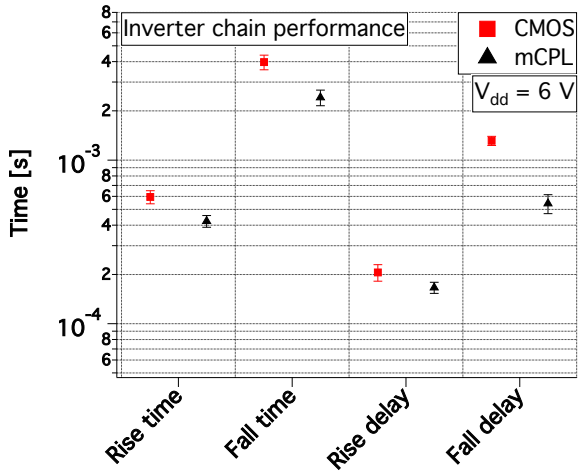
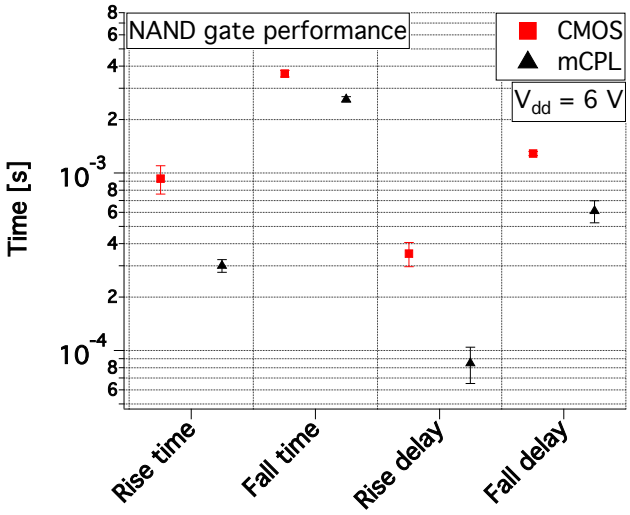


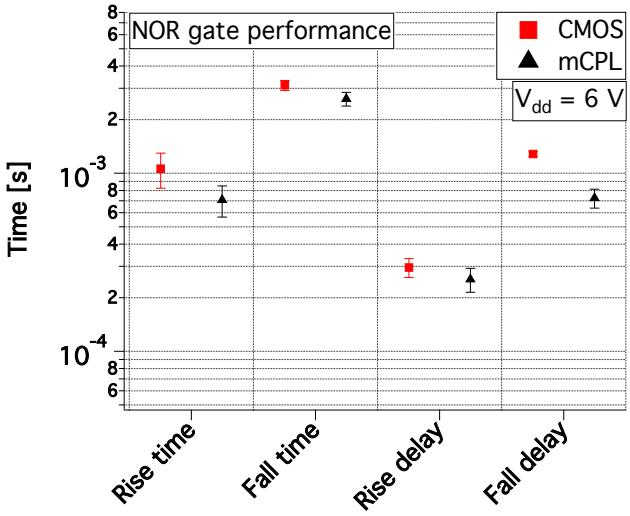
Figure B.6: Switching times and delay comparison of the mCPL and CMOS logic for inverter stage loaded with a fan out of 4.

case scenario. For instance, in the NOR CMOS gate (figure B.1d), two cases are considered; the pull up and pull down of the output node (Z). In the former, the worst case scenario occurs when the input B = 0 V and the input A is switched from V_{DD} to 0 V. In pull down, the worst case is when only one of the transistors is on. This is determined for each gate individually.

The performance of the mCPL NOR gate show a 1.5× better rise time and almost comparable fall time (1.2×), a slightly better rising delay (1.2×), and a 1.8× better fall delay. The NAND gate shows an improved speed for the mCPL logic with a 3× and 1.4× faster slew rate in the rising and falling case respectively as well as 2.1× better falling delay and 4.1× better rising delay. Due to the difference in input capacitance of the two logic design, the estimation on the power consumption per operation indicates a 3× more efficient gate in the mCPL.



(a)



(b)

Figure B.7: Switching times and delay comparison of the NAND (a) and NOR (b) logic gates both for the mCPL and CMOS design.