Challenges and Solutions for High Performance Analog Circuits with Robust Operation in Low Power Digital CMOS

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Abstract

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In modern System-on-Chip products, analog circuits need to co-exist with digital circuits integrated on the same chip. This brings on a lot of challenges since analog circuits need to maintain their performance while being subjected to disturbances from the digital circuits. Device size scaling is driven by digital applications to reduce size and improve performance but also results in the need to reduce the supply voltage. Moreover, in some applications, digital circuits require a changing supply voltage to adapt performance to workloads. So it is further desirable to develop design solutions for analog circuits that can operate with a flexible supply voltage, which can be reduced well below 1V. In this thesis challenges and solutions for key high performance analog circuit functions are explored and demonstrated that operate robustly in a digital environment, function with flexible supply voltages or have a digital-like operation.

A combined phase detector consisting of a phase-frequency detector and sub-sampling phase detector is proposed for phase-locked loops (PLLs). The phase-frequency function offers robust operation and the sub-sampling detector leads to low in-band phase noise. A 2.2GHz PLL with

a combined phase detector was prototyped in a 65nm CMOS process, with an on-chip loop filter area of only 0.04mm^2. The experimental results show that the PLL with the combined phase detector is more robust to disturbances than a sub-sampling PLL, while still achieving a measured in-band phase noise of -122dBc/Hz which is comparable to the excellent noise performance of a sub-sampling PLL.

A pulse-controlled common-mode feedback (CMFB) circuit is proposed for a 0.6V-1.2V supply-scalable fully-differential amplifier that was implemented in a low power/leakage 65nm CMOS technology. An integrator built with the amplifier occupies an active area of 0.01mm^2. When the supply is changed from 0.6V to 1.2V, the measured frequency response changes are small, demonstrating the flexible supply operation of the differential amplifier with the pulse-controlled CMFB.

Next, models are developed to study the performance scaling of a continuous-time sigma-delta modulator (SDM) with a varying supply voltage. It is demonstrated that the loop filter and the quantizer exhibit different supply dependence. The loop noise performance becomes better at a higher supply thanks to larger signal swings and better signal-to-noise ratio, while the figure of merit determined by the quantization noise gets better at a lower supply voltage, thanks to the quantizer power dissipation reduction. The theoretical models were verified with simulations of a 0.6V-1.2V 2MHz continuous-time SDM design in a 65nm CMOS low power/leakage process.

Finally, two design techniques are introduced that leverage the continued improvement of digital circuit blocks for the realization of analog functions. A voltage-controlled-ring-oscillator-based amplifier with zero compensation is proposed that internally uses a phase-domain representation

of the analog signal. This provides a huge DC gain without significant penalties on the unity-gain bandwidth or area. With this amplifier a 4th-order 40-MHz active-UGB-RC filter was implemented that offers a wide bandwidth, superior linearity and small area. The filter prototype in a 55nm CMOS process has an active area of 0.07mm^2 and a power consumption of 7.8mW at 1.2V. The in-band IIP3 and out-of-band IIP3 are measured as 27.3dBm and 22.5dBm, respectively. A digital in-situ biasing technique is proposed to overcome the design challenges of conventional analog biasing circuits in an advanced CMOS process.

A digital CMFB was simulated in a 65nm CMOS technology to demonstrate the advantages of this digital biasing scheme. Using time-based successive approximation conversion, the digital CMFB provides the desired analog output with a more robust operation and a smaller area, but without needing any stability compensation schemes like in conventional analog CMFBs.

In summary, analog design techniques are continuously evolving to adapt to the integration with digital circuits on the same chip and are increasingly using digital-like blocks to realize analog functions in highly-integrated SOC chips. The signal representation in analog circuits is moving from traditional electrical signals such as voltage or current, to time and phase-domain representations. These changes make analog circuits more robust to voltage disturbances and supply variations. In addition to improved robustness, analog circuits based on timing signals benefit from the faster and smaller transistors offered by the continued feature scaling in CMOS technologies.

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Chapter 1

Introduction

1.1 Motivation

The continued advancement of CMOS technologies has fueled tremendous progress in low-cost and highly-integrated System-on-Chip products over the past decades. However, the integration of analog and digital circuits on a single chip leads to a lot of design challenges for the analog circuits which are shown in Fig. 1.1. Robust operation in the presence of disturbances or supply noise that couple through the substrate or supply from digital functions has become an essential requirement for analog circuits. Nevertheless, it is difficult for high performance analog circuits to maintain robustness because they have more sensitivity to signal quality, and less immunity to disturbances or interference. In addition, the analog circuits are required with flexible supply operation because digital core circuits need a higher supply to increase the operating frequency and process more applications, but a lower voltage at sleep mode to save idle power. The supply-scalable analog

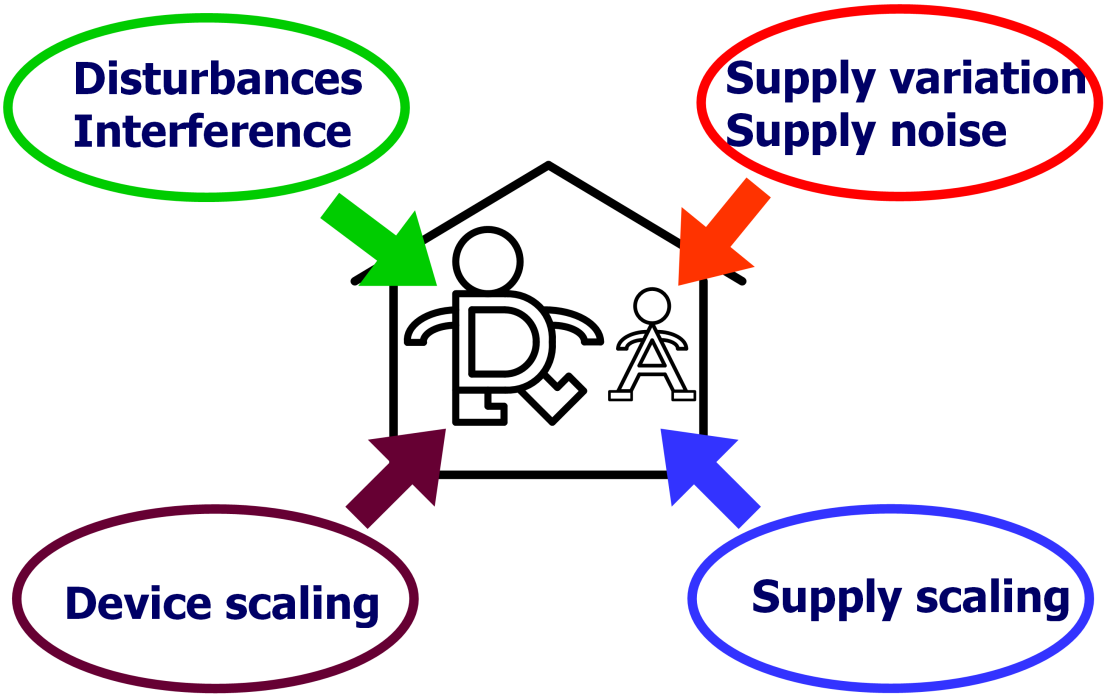


Figure 1.1: Design challenges to analog circuits integrated with digital circuits

circuits also help extend battery life because they are able to fully use the power of batteries. However, these analog circuits with large supply tolerances meet the problems of limiting signal headroom, especially in low power/leakage CMOS technologies.

Additionally, digital circuits benefit from smaller and faster devices through the advancement of the CMOS technology, but the device scaling brings with it design difficulties to analog parts such as a low analog power gain by small output impedance and short-channel effects including drain-induced barrier lowering (DIBL), punch-through, and velocity saturation. Fig. 1.2 summarizes the transistor performance of the projected technology nodes from 2013 to 2026 by the International Technology Roadmap for Semiconductors, 2013 [Online]. With a steady reduction of the feature size and effective gate oxide thickness, the cut-off frequency of the CMOS transistors is increasing, while their available supply voltage is scaled down accordingly for power density.

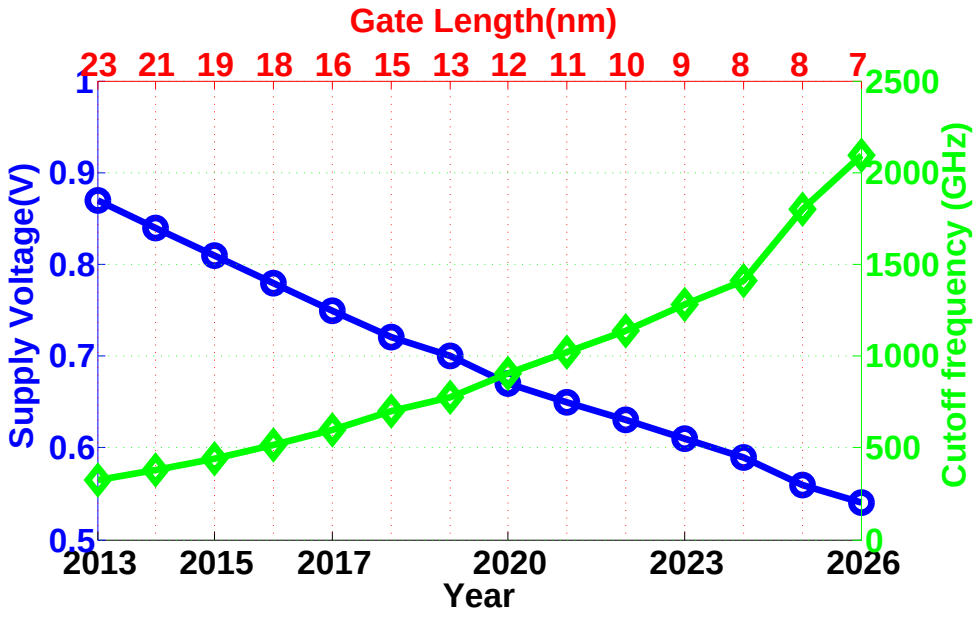


Figure 1.2: The supply voltage, cut-off frequency and minimum gate length of transistors from 2013 to 2026 by ITRS

This scaling trend is pushing the analog interface to adopt digital approaches by replacing traditional voltage or current operation to time/frequency/phase operation and taking advantage of supply or device scaling, but keep the voltage or current inputs and outputs. The time or phase operation only has two discrete levels of voltage or current so that it is not sensitive to disturbances or supply changes and has more scaling benefits. Fig. 1.3 shows the two examples of the time operation: frequency modulation and pulse-width modulation.

In this dissertation, several analog examples are demonstrated to explore challenges and solutions for high performance analog circuits with robust operation, flexible supply operation, or digital-like operation. The research vehicles include a 2.2GHz phase-locked loop, an integrator with a zero of 10MHz, a 2MHz continuous-time sigma-delta modulator, a 4th-order 40MHz continuous-time filter, and a differential amplifier.

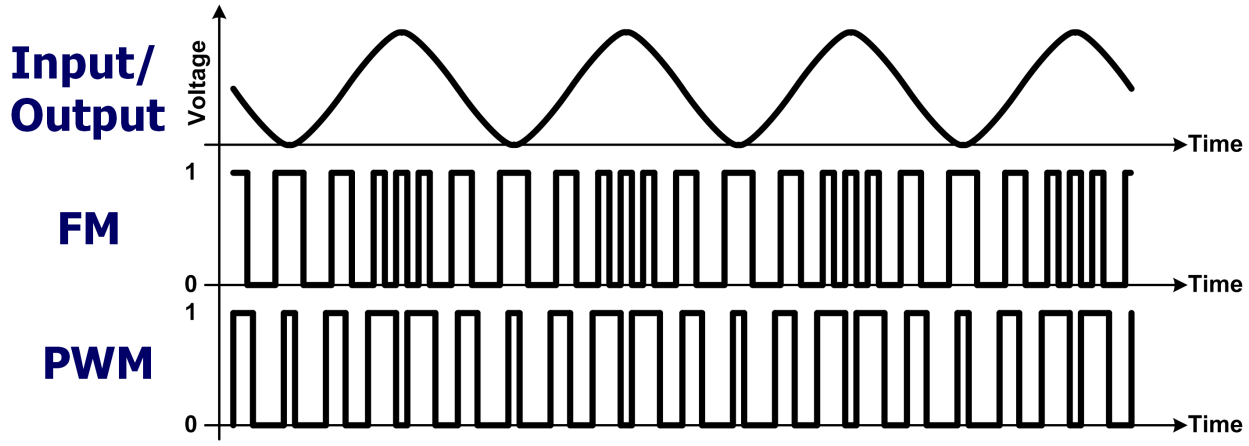


Figure 1.3: Examples of the time operation: frequency modulation and pulse-width modulation

1.2 Outline

Most of the research contributions to this dissertation show the challenges and solutions of high performance analog circuits integrated with digital circuits and are included in the publications [3] [7] [33] [49]. The dissertation is organized as follows. Chapter 1 presents a motivation for the dissertation. In chapter 2, a combined phase detector was provided for PLLs with robust operation under disturbances while offering low in-band phase noise and low jitter. Chapter 3 describes a pulse-controlled CMFB for a fully-differential amplifier from 0.6V to 1.2V in a low power/leakage CMOS technology. In chapter 4, the supply-scaling models of a continuous-time sigma-delta modulator were verified by circuit simulations with the supplies between 0.6V and 1.2V. Chapter 5 shows a VCO-based amplifier with zero compensation for getting a large DC gain without any penalties associated with the large DC gain. Chapter 6 introduces a digital biasing solution using ultra-compact digital circuits for analog interfaces. In chapter 7, a summary of these works is given with one possible direction for extending the topics of study included in this dissertation.

Chapter 2

A Sub-Sampling-Assisted Phase-Frequency Detector for Low-Noise PLLs with Robust Operation under Supply Interference

It has recently been demonstrated that sub-sampling phase detectors (SSPDs) enable phase-locked loop (PLL) realizations with very low in-band noise [1] [2] [3]. However, the PLL can become susceptible to disturbances or interference via substrate or power supply coupling as experienced in SOC, which could put the PLL out of lock. A tri-state phase-frequency detector with a dead-zone is traditionally added to act as an auxiliary frequency-locked loop (FLL) to enable the PLL to regain lock, albeit after a long delay. A different solution is proposed to combine a tri-state PFD with an SSPD wherein the PLL is prevented from losing its lock while simultaneously achieving the superior in-band phase noise performance. A 2.2GHz integer-N PLL has been prototyped in

a 65nm CMOS process to demonstrate the advantages of the proposed combined phase detector. It has been experimentally verified that the PLL is more robust to disturbances than a PLL with a sub-sampling phase detector; it further achieves a measured in-band phase noise of -122dBc/Hz when operating with the proposed combined PD from a 1.1V supply.

2.1 Introduction

Phase-locked loops (PLLs) are crucial building blocks for clock synthesis or carrier frequency generation in practically all system-on-chip (SOC) integrated circuits. Key performance metrics are low jitter or phase noise, and low power dissipation. However, in the context of SOC applications, robust operation in the presence of disturbances or interference that couple through the substrate or supply from large digital functions into the (embedded) PLL has become an essential requirement.

Jitter of a PLL is an important concern in clock synthesis applications. For a given power budget, [4] has shown that the minimum jitter for a PLL is achievable when the contribution from the out-of-band portion of the PLL's phase noise spectrum equals the contribution from the in-band portion. Further, an equal distribution of power between the VCO and the PLL blocks has been proven to be the optimum strategy. The power budget for the VCO is thus fixed to half of the available power budget, and after optimizing the VCO design for the best phase noise performance, the PLL's jitter can be improved only by lowering the in-band noise (and accordingly increasing the PLL's loop bandwidth).

The choice of the phase detector (PD) design is critical as the noise of the PD is a significant contribution to the in-band phase noise of a PLL. Tri-state phase/frequency detectors (PFDs) are

popular for their inherent ability to discriminate both phase and frequency, thus widening the acquisition range of the PLL [5]. Recently, a PLL using sub-sampling phase detectors (SSPDs) has been demonstrated with ultra-low in-band phase noise [6]. However, PLLs using SSPDs have very small capture ranges, can false lock and are sensitive to disturbances (often on the VCO's supply or coupling through the substrate) which can push the PLL out of its locked state. An auxiliary FLL in the form of a tri-state PFD with dead-zone fixes the capture range and false lock problems. It also helps regain the lock after the PLL loses lock due to a disturbance or interference, but as shown below it requires a long acquisition time which may not be acceptable in many clock synthesis applications.

In this chapter, I would like to present a sub-sampling-assisted phase-frequency detector named by a combined phase detector which maintains the low in-band phase noise feature of [6], but makes it as robust to disturbances as PFD-based PLLs. This prevents the PLL from losing lock and thus eliminates the time wasted in lock re-acquisition when the PLL's output is unreliable. Further, the robustness is achieved without compromising the in-band phase noise performance of the PLL.

The rest of the chapter is organized as follows: section 2.2 discusses the operation of the proposed combined PD [7] and describes the measures to ensure robustness. Section 2.3 presents simulations demonstrating the lack of interference robustness in PLLs with sub-sampling-based phase detectors while PLLs with the proposed combined PD offers a similar robustness as PLLs with a PFD. Section 2.4 presents a detailed noise analysis of the combined PD, showing its superior noise performance over PFDs. Section 2.5 describes the circuit implementation of the blocks of a

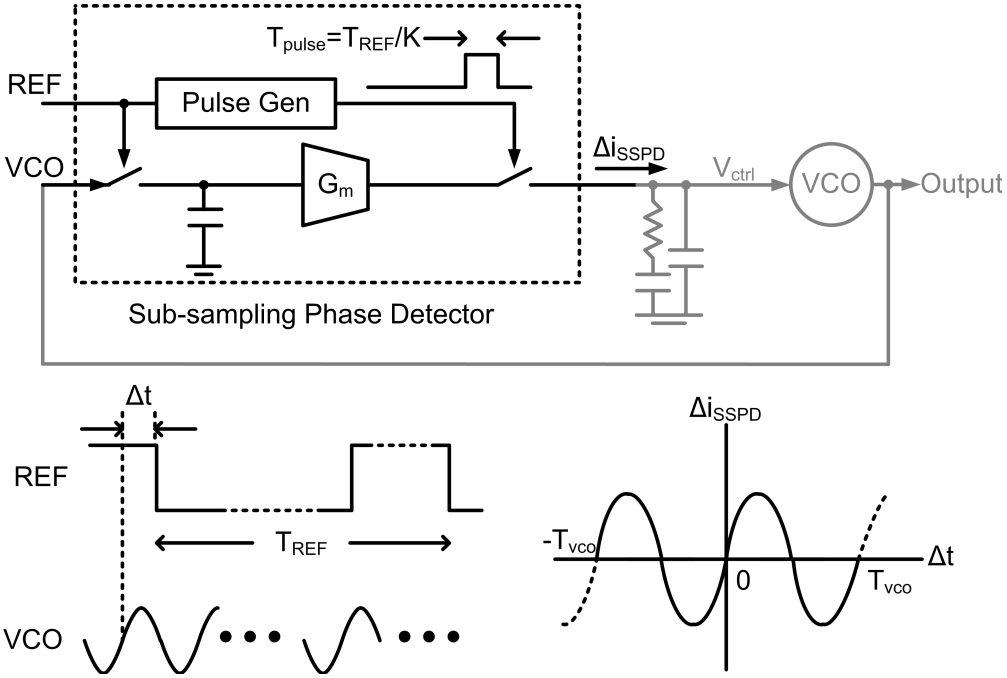


Figure 2.1: Block diagram of a sub-sampling phase detector and associated waveforms and characteristics

2.2GHz PLL prototype with the combined PD. Section 2.6 presents the experimental results with a focus on the robustness of PLL operation to disturbances on power supply while achieving a low in-band phase noise.

2.2 Developing a Combined Phase Detector Designed for Robustness

The block diagram of a standard SSPD [6] is shown in Fig. 2.1 and its basic operation can be summarized as follows. The VCO output voltage, $v_{\mathrm{VCO}}(t) = A_{\mathrm{VCO}} \sin(\omega_{\mathrm{VCO}} t + \Delta\phi_{\mathrm{VCO}})$, with an amplitude A_{VCO} and an angular frequency $\omega_{\mathrm{VCO}} = 2\pi/T_{\mathrm{VCO}}$. The phase $\Delta\phi_{\mathrm{VCO}}$ is sampled

at falling edges of the input reference signal REF. The reference is assumed to be frequency-locked to the VCO, so that its angular frequency $\omega_{\mathrm{REF}} = 2\pi/T_{\mathrm{REF}} = \omega_{\mathrm{VCO}}/N$, but with a time shift $\Delta t = \Delta\phi_{\mathrm{REF}}/\omega_{\mathrm{REF}}$ between falling edges of REF and corresponding VCO zero crossings. The voltage sample, $\hat{v} = A_{\mathrm{VCO}}\sin(\Delta\phi_{\mathrm{VCO}}) = A_{\mathrm{VCO}}\sin(\omega_{\mathrm{VCO}}\Delta t) = A_{\mathrm{VCO}}\sin(N\Delta\phi_{\mathrm{REF}})$ is converted into a current with a transconductor with transconductance G_{m}. That current is gated and only steered to the loop filter for a duration $T_{\mathrm{pulse}} = T_{\mathrm{REF}}/K$ and then integrated by the loop filter. K is the ratio of the reference period to pulse width and is the gain reduction factor of the SSPD. The loop filter has a time constant much larger than $1/\omega_{\mathrm{REF}}$ so that only the average of the current matters for modeling the phase detector operation in a steady state.

Because of the equality of $\Delta\phi_{\mathrm{VCO}}$ and $N\Delta\phi_{\mathrm{REF}}$, there is an additional gain factor N at REF input of the SSPD compared to its VCO input. Thus, the equivalent phase domain model of the SSPD can be shown as Fig. 2.2.

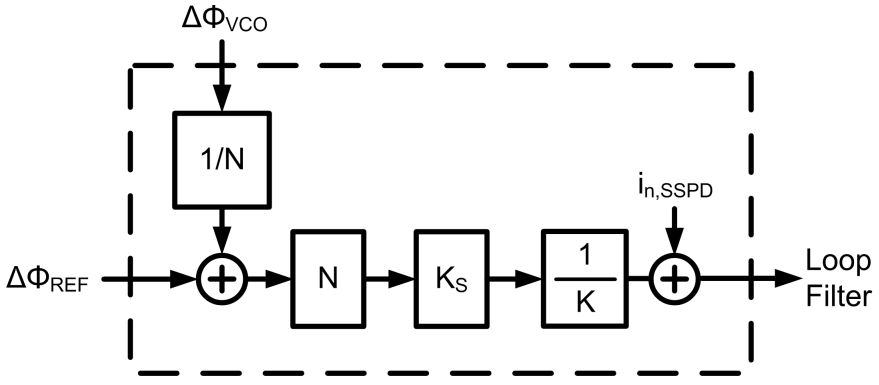


Figure 2.2: Phase domain model of the sub-sampling phase detector

A PLL with the SSPD can achieve very low in-band phase noise [6]. However, the SSPD only performs phase detection with small locking range and no frequency detection. As a result, the PLL operating only with the SSPD may be locked to any harmonic of f_{REF}. To overcome the

frequency locking problem of the SSPD, [6] uses a tri-state PFD with a dead zone (DZ) of ($-\pi$, π) as an auxiliary FLL (referred to as FLL-assisted SSPD for simplicity). The auxiliary FLL is activated only when the magnitude of the timing error exceeds $T_{\mathrm{REF}}/2$. The PLL subjected to disturbances requires a long lock re-acquisition time, as will be discussed in section 2.3.

The core idea of the proposed phase detector is to combine the SSPD and the tri-state PFD in such way that the frequency-locked loop feature is always active. The comparison between an FLL-assisted SSPD and the proposed combined phase detector comprised of a tri-state PFD with a charge pump (CP) and an SSPD is shown in Fig. 2.3. The transfer characteristic of the combined phase detector is shown in Fig. 2.4. It is formed by summing the characteristics of the tri-state PFD/CP and the SSPD. The y-axis shows the averaged output current of the combined phase detector $\overline{I_{\mathrm{out}}}$ for a given time difference Δt between the falling edges of the REF signal and the corresponding zero-crossings of the VCO.

To retain the same frequency locking ability of a tri-state PFD, the zero output of the combined phase detector may only occur at $\Delta t = 0$ and the combined phase detector needs to produce positive currents for all positive Δt and negative currents for all negative Δt. To achieve this, the maximum output current of the SSPD must be smaller than the output current of the PFD/CP for $\Delta t = (\pm 3/4)T_{\mathrm{VCO}}$, which is $\pm 3I_{\mathrm{CP}}/(4N)$ where I_{CP} is the charge pump current of the tri-state PFD/CP. When keeping the sub-sampling phase detector's output current smaller than $3I_{\mathrm{CP}}/(4N)$, the combined phase detector will continue to operate as a frequency detector in the presence of frequency errors and, as a result, the PLL will have a single stable locking point. It is noted that the

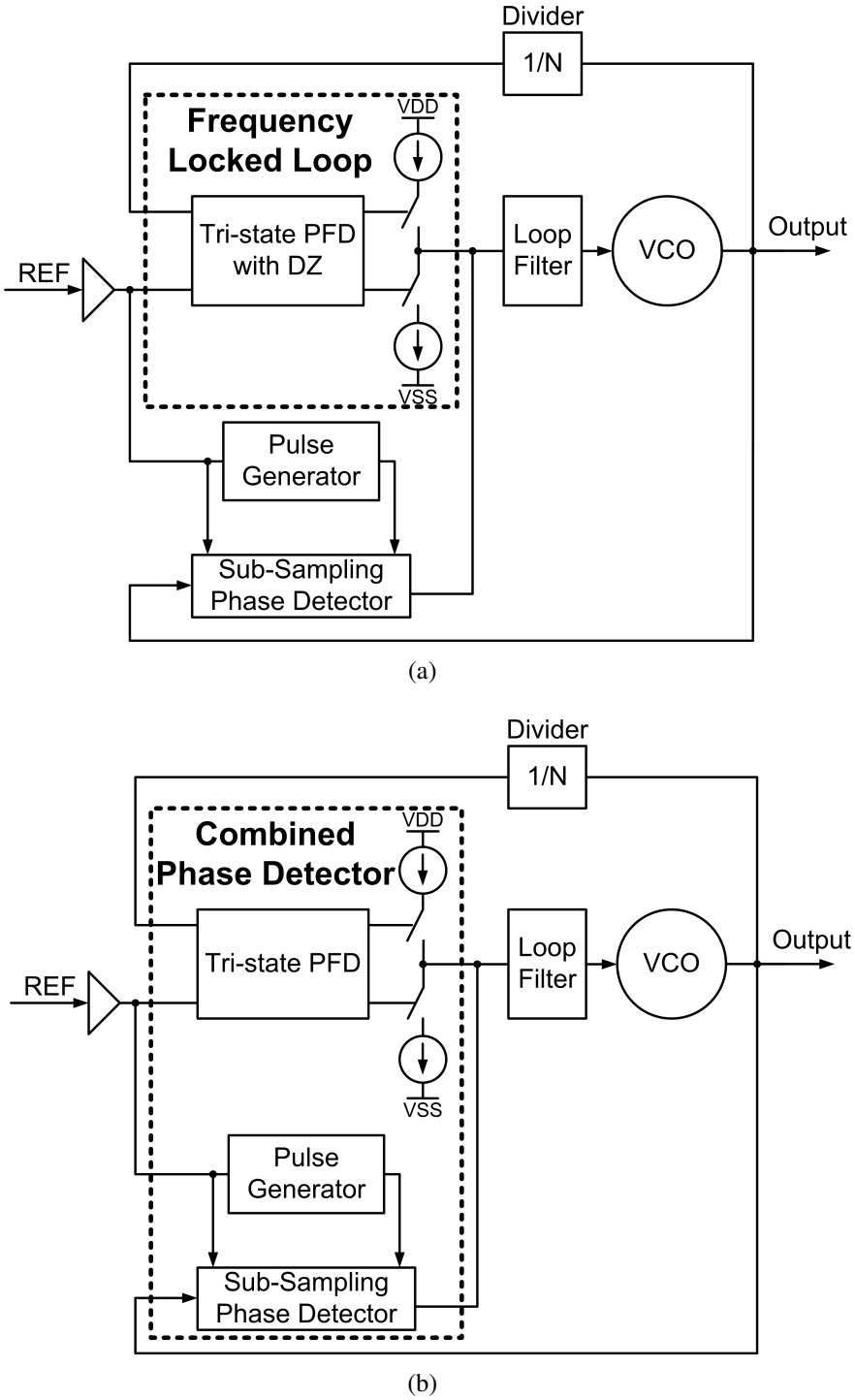


Figure 2.3: PLL block diagram comparing the combined PD (b) with an FLL-assisted SSPD (a). The tri-state PFD in the combined PD does not have a dead zone (DZ).

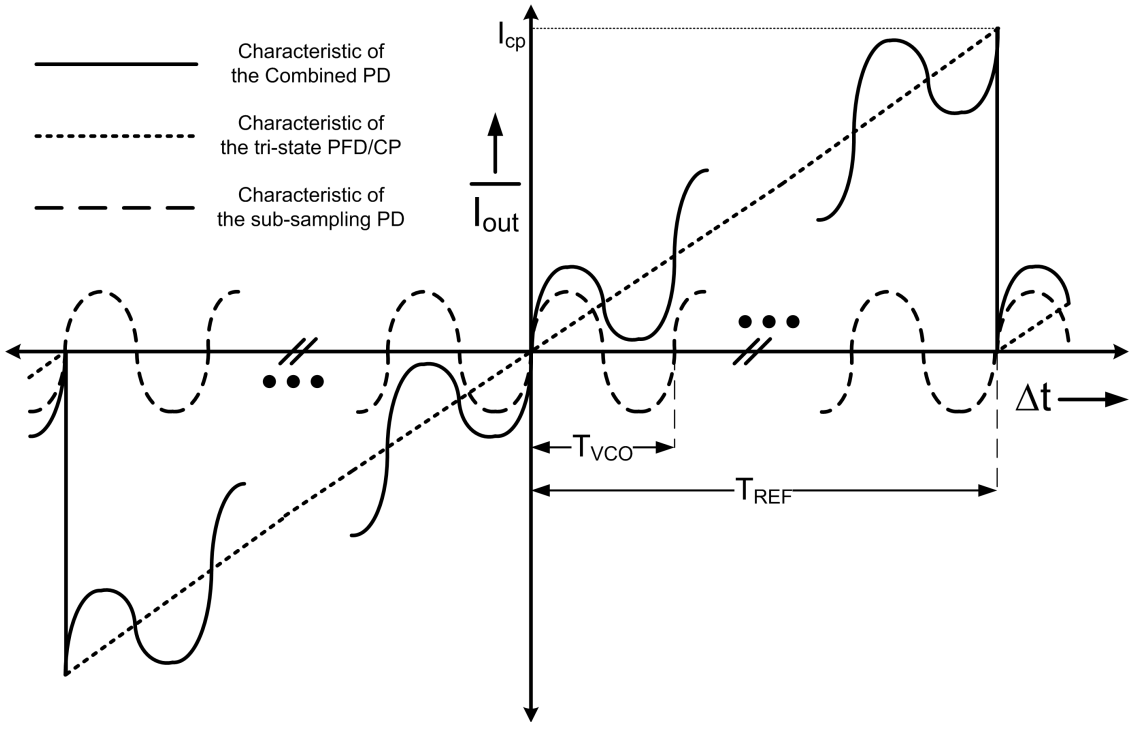


Figure 2.4: Characteristics of the combined phase detector, the PFD, and the sub-sampling PD

gain of the combined PD in the transfer characteristic is dominated by the gain of the sub-sampling PD.

Except for frequency locking at the divisor of an integer, the PLL with the combined phase detector is also able to work with a fractional division ratio which is not allowed for a sub-sampling PLL. While operating in the fractional-N mode, the PLL with the combined PD is similar to a charge-pump PLL rather than a sub-sampling PLL because the maximum current of the sub-sampling PD is much smaller than I_{CP} and the sub-sampling PD can be viewed as a small non-zero current source at the output of the combined PD. Thus, as the PLL with a fractional divisor is locking, there is a non-zero steady-state phase difference input to the combined PD because of the output current offset caused by the sub-sampling PD.

Even though the combined PD can be used for a fractional-N PLL, there are some challenges brought by this PD. The combined PD essentially is a non-linear PD, so the modulated quantization error of the PLL will be folding back to lower frequencies and then degrades phase noise. In addition, the non-zero balanced phase difference of the PLL is inappropriate for some applications requiring small static phase errors.

2.3 Simulation-based verification of the Locking Issues in Sub-Sampling-based Phase Detectors and Robustness of the Combined Phase Detector

This section presents simulation-based evidence to demonstrate the locking issues in PLLs with sub-sampling-based phase detectors in contrast to the robustness of PLLs with tri-state PFDs. It will be shown that a PLL with the combined PD, which retains the frequency detecting capabilities of the tri-state PFD, is as robust as a PFD-based PLL.

Transient simulations were conducted on type II third-order PLLs using (a) an SSPD, (b) an FLL-assisted SSPD, (c) a conventional tri-state PFD, and (d) the combined PD. Verilog-A based behavioral models were used to describe the circuit blocks. The PLLs were driven by a reference frequency of 50MHz with the parameters set as follows: N=44; K_{VCO}=150MHz/V; a loop filter consisting of a parallel capacitor 1.3pF and a resistor 12.6kΩ in series with a capacitor 31.7pF. A disturbance in the form of a current pulse is injected into the loop filter to measure the dynamics of the loop in various cases.

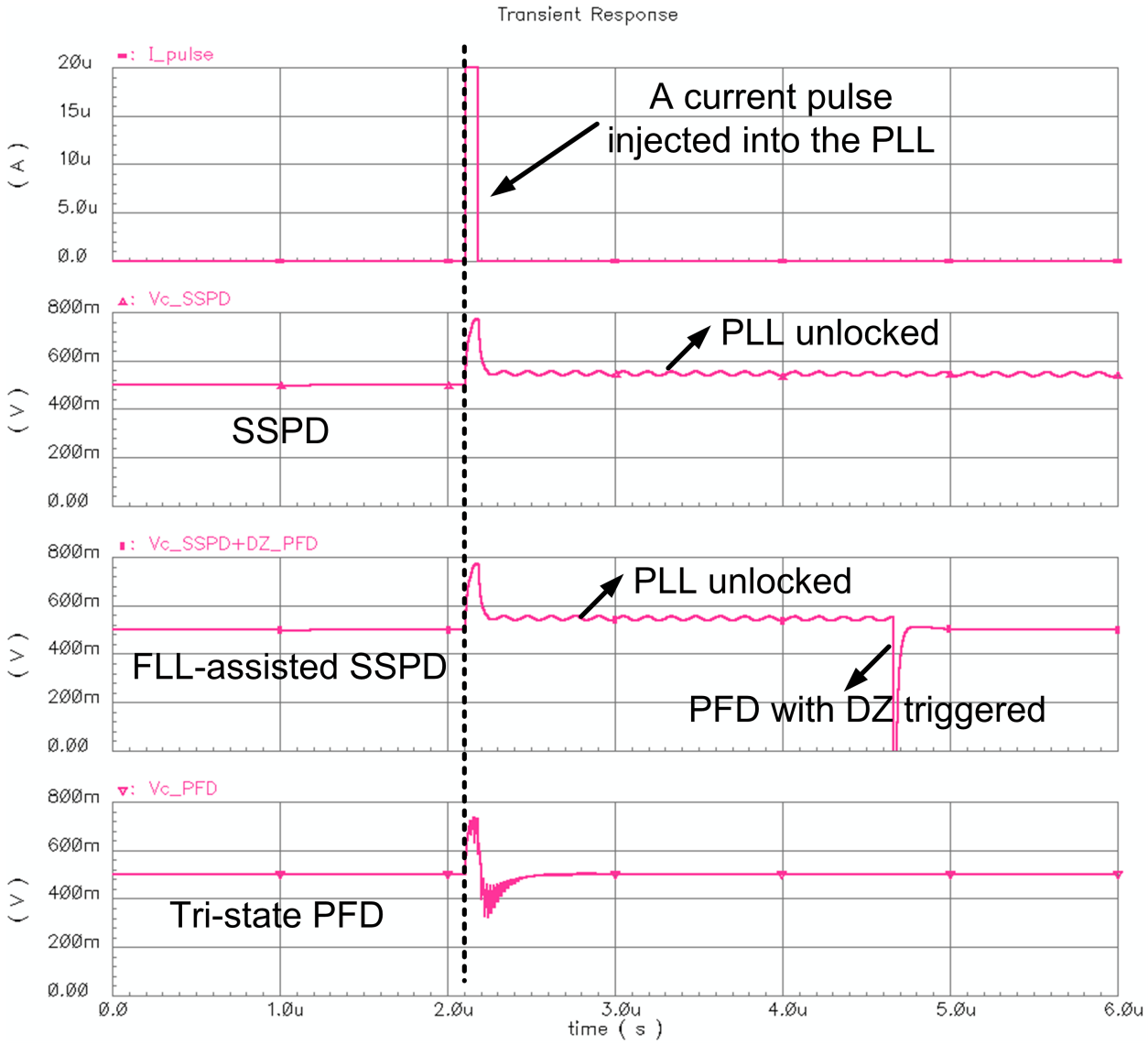


Figure 2.5: Interference robustness simulation results for PLLs with different types of phase detectors; an SSPD-only PLL loses lock; a PLL with an FLL-assisted SSPD reacquires lock, albeit after a long time (2.5μs in this example) during which the PLL is unlocked; a PLL with a PFD operates robustly for the same disturbance.

Fig. 2.5 shows the simulated transient of VCO control voltage in PLLs using (a) an SSPD, (b) an FLL-assisted SSPD, and (c) a tri-state PFD. The PD gains of the PLLs with the above PDs are set to the same value of $K_{\mathrm{PD}} = 0.25/(2\pi)$(mA/radian) so that they have the same loop response. After the disturbance occurs, the PLL using just the SSPD goes out of lock due to its narrow locking range given the lack of frequency detection capabilities. The PLL using the conventional tri-state PFD, however, is very robust to disturbances and remains locked, as shown by the simulation. In the PLL using an FLL-assisted SSPD, the FLL (dead-zone PFD) [6] is enabled only when the magnitude of the phase error is greater than π and is quiet while the phase error falls within the DZ. The lock-re-acquisition time of the PLL with the FLL-assisted SSPD is simulated to be $2.5\mu s$. For the same magnitude of the disturbance, a PLL with the conventional PFD is observed to recover to steady state as quickly as within $0.4\mu s$.

When the PLL with an FLL-assisted SSPD is pushed out of lock by a disturbance, the phase error needs to exceed π for the FLL to engage the relocking process. The associated lock-re-acquisition time ΔT can be estimated as follows. Due to the disturbance, there is an error voltage $\Delta V(t)$ on the VCO control voltage; this voltage change leads to a phase change $\Delta\phi_{\mathrm{VCO}}$ equal to the integral of $2\pi K_{\mathrm{VCO}}\Delta V(t)$. The phase error at the phase detector, $\Delta\phi_{\mathrm{REF}}$, is $\Delta\phi_{\mathrm{VCO}}/N$ and reaches a magnitude of π after a time ΔT calculated from:

$$\left| \int_0^{\Delta T} \frac{K_{\mathrm{VCO}}\Delta V(t)}{N} dt \right| > 0.5, \tag{2.1}$$

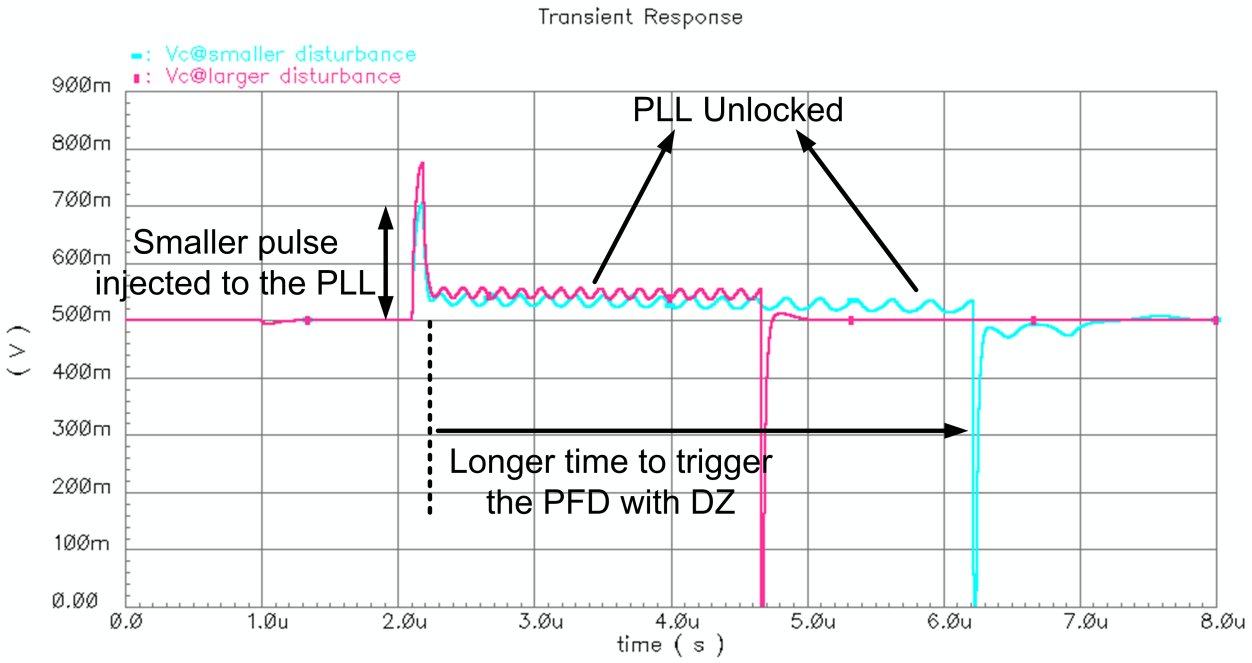


Figure 2.6: Simulated results of a PLL using an FLL-assisted PFD subjected to disturbances of different strengths

If $\Delta V(t)$ is approximated to be constant, the lock-re-acquisition time can be computed as

$$\Delta T = 0.5\frac{N}{K_{\text{VCO}}\Delta V}. \tag{2.2}$$

Eq. (2.2) shows that the lock re-acquisition time depends on the strength of the disturbance; the PLL will have a longer lock re-acquisition time for a weaker disturbance[1], because it takes more time for the magnitude of the phase error to accumulate to π. This phenomenon was verified using simulations. The PLL with the FLL-assisted SSPD was observed to have a simulated lock-re-acquisition time of $2.5\mu s$ for a stronger disturbance while it is $4\mu s$ for a weaker disturbance as shown in Fig. 2.6.

[1]Note that the disturbance has to remain sufficiently large to unlock the PLL.

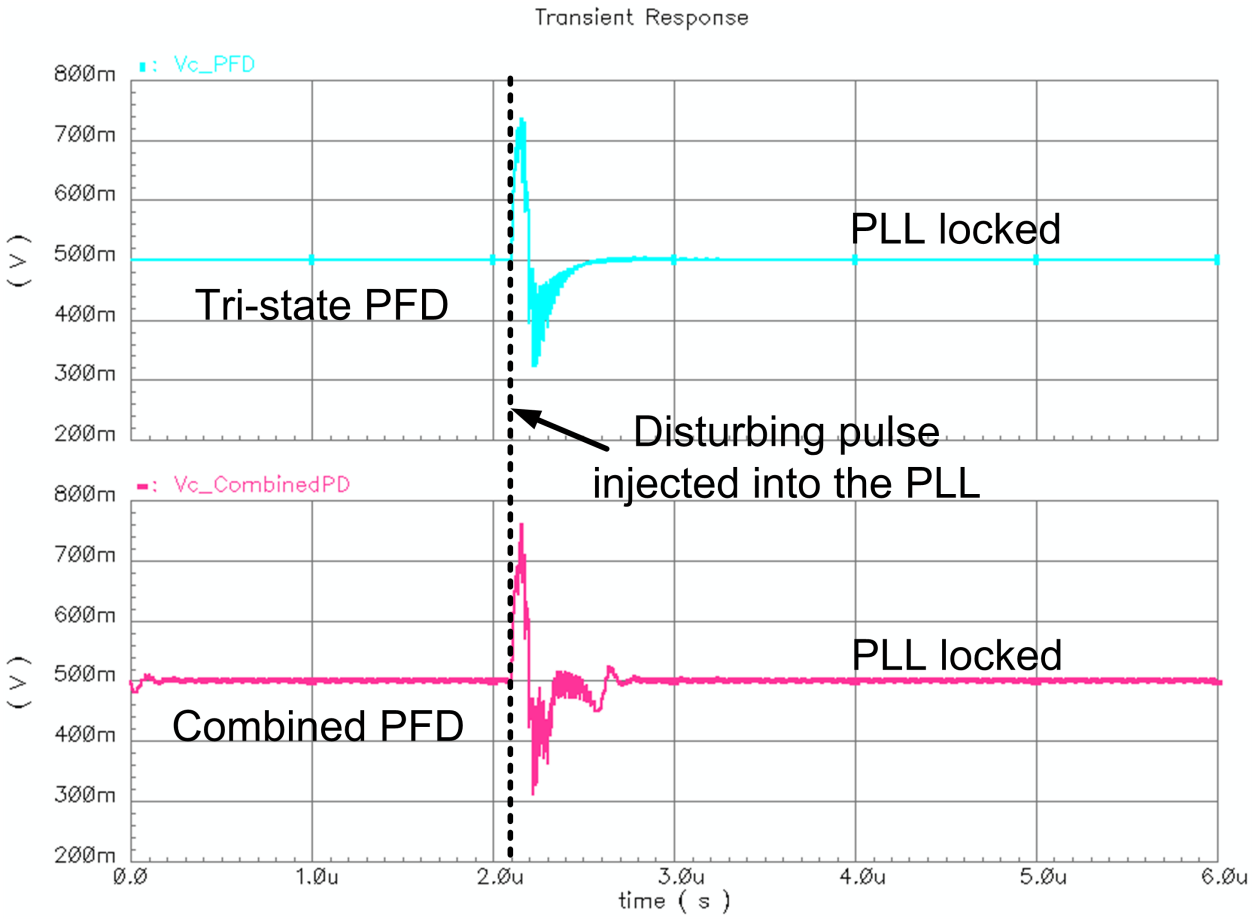


Figure 2.7: Simulation results of the PLL with a conventional PFD and the proposed combined PD under the disturbance

A comparison is made for PLLs with a tri-state PFD and the proposed combined PD by adding an SSPD to the PFD. Transient response of their control voltages to a disturbance is shown in Fig. 2.7. The simulation results show that the PLLs with the PFD and the combined PD have a similar robustness when subjected to disturbances. Due to the retention of the frequency detecting feature of a conventional tri-state PFD, a PLL using the combined PD is prevented from losing lock and thus the long lock-re-acquisition time (as in the case of an FLL-assisted SSPD) can be avoided.

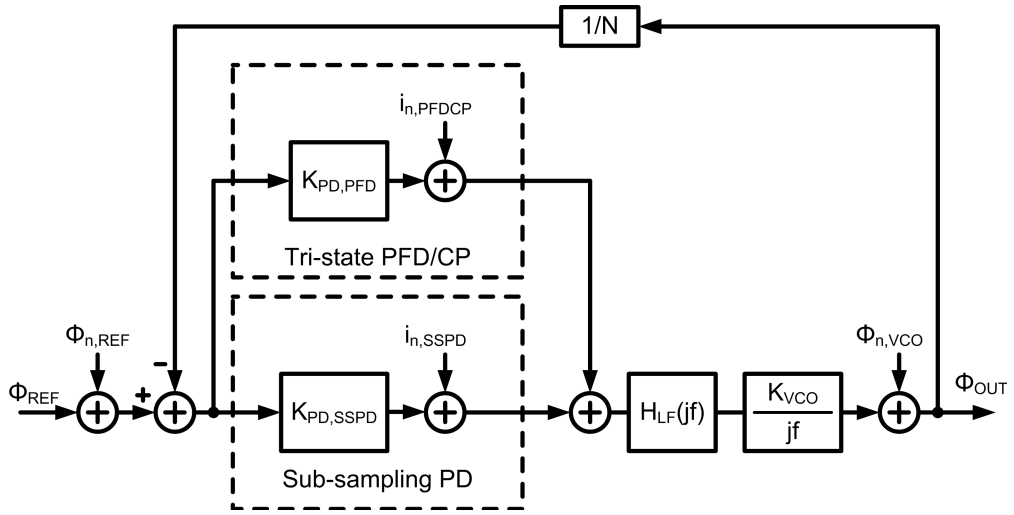


Figure 2.8: Phase domain model for the PLL with the combined phase detector

2.4 Noise Analysis for the Combined Phase Detector

Now it is demonstrated that a combined phase detector has a superior noise performance than a tri-state PFD. The phase domain model of the PLL with a combined PD in locked condition is shown in Fig. 2.8. $H_{\mathrm{LF}}(jf)$ is the transfer function of the loop filter, K_{VCO} is the frequency tuning gain of the VCO, and $K_{\mathrm{PD,PFD}}$ is the gain of the tri-state PFD/CP. The gain of the sub-sampling PD, $K_{\mathrm{PD,SSPD}}$, is given by:

$$\begin{aligned} K_{\mathrm{PD,SSPD}} &= \frac{\overline{\Delta i_{SSPD}}}{\Delta\phi_{\mathrm{REF}}} = N \cdot \frac{\overline{\Delta i_{SSPD}}}{\Delta\phi_{\mathrm{VCO}}} \\ &= N\left(\frac{S}{\omega_{\mathrm{VCO}}} G_{\mathrm{m}}\right)\frac{T_{\mathrm{pulse}}}{T_{\mathrm{REF}}} = N \cdot K_S \cdot \frac{1}{K} \end{aligned} \tag{2.3}$$

where $\overline{\Delta i_{SSPD}}$ is the averaged output current of the sub-sampling phase detector and S is the slope of the VCO signal around the SSPD's operating point. $S = A_{\mathrm{VCO}}\omega_{\mathrm{VCO}}$ and $K_S = A_{\mathrm{VCO}}G_{\mathrm{m}}$ when locked around the zero-crossing of the VCO.

The gain of the combined phase detector is now $K_{\mathrm{PD,comb}} = K_{\mathrm{PD,PFD}} + K_{\mathrm{PD,SSPD}}$. Under the condition to maintain the frequency detecting ability derived in section 2.2, the maximum gain of the combined phase detector around the zero-timing-error point can be expressed by:

$$\begin{aligned} K_{\mathrm{PD,comb,MAX}} &= \frac{\overline{I_{\mathrm{out}}}}{\Delta\phi_{\mathrm{REF}}} = \frac{I_{\mathrm{CP}}}{2\pi} + \left(\frac{3I_{\mathrm{CP}}}{4N}\right)\frac{T_{\mathrm{REF}}}{T_{\mathrm{VCO}}} \\ &\approx 5.7 \cdot \frac{I_{\mathrm{CP}}}{2\pi} = 5.7 \cdot K_{\mathrm{PD,PFD}}. \end{aligned} \tag{2.4}$$

Using the phase-domain model, the power spectral density of the output phase noise of the PLL, $S_{\phi,\mathrm{n,out}}$, can be derived as:

$$\begin{aligned} S_{\phi,n,out} = &\left|\frac{1}{1+L(jf)}\right|^2 S_{\phi,n,\mathrm{VCO}} + \left|\frac{L(jf)\cdot N}{1+L(jf)}\right|^2 S_{\phi,n,REF} \\ &+ \left|\frac{L(jf)\cdot N}{1+L(jf)}\right|^2 \frac{1}{K^2_{\mathrm{PD,comb}}} \left(S_{i,n,\mathrm{PFDCP}} + S_{i,n,\mathrm{SSPD}}\right) \end{aligned} \tag{2.5}$$

where $S_{\phi,n,\mathrm{block}}$ is the noise power spectral density from a specific 'block' and $L(jf)$ is the loop transfer function of the PLL, equal to $K_{\mathrm{PD,comb}} \cdot H_{\mathrm{LF}}(jf) \cdot (K_{\mathrm{VCO}}/(jf))/N$.

If the PFD/CP noise is decided by the thermal noise current of the CP, the output power spectral density of the PFD/CP can be expressed by:

$$S_{i,n,\mathrm{PFDCP}} = 4kT\gamma\left(\frac{gm_{\mathrm{CP}}}{I_{\mathrm{CP}}}\right) I_{\mathrm{CP}} \left(\frac{T_{\mathrm{idle}}}{T_{\mathrm{REF}}}\right)$$

where gm_{CP} is the transconductance of the CP current sources and $(T_{\mathrm{idle}}/T_{\mathrm{REF}})$ is the duty cycle of switching the CP on in a steady state to avoid the dead zone.

The main contributors to the noise of the SSPD are the sampling switch and the transconductor. Timing errors due to the noise in the pulse generator changes pulse width which marginally changes the gain of the SSPD which is inconsequential. The power spectral density of the total output current noise of the SSPD can be derived to be:

$$S_{i,n,\mathrm{SSPD}} = \frac{\overline{v_{\mathrm{n,samp}}^2}}{f_{\mathrm{REF}}/2} \cdot \frac{G_{\mathrm{m}}^2}{K^2} + \frac{S_{i,n,\mathrm{Gm}}}{K} \tag{2.6}$$

where $\overline{v_{\mathrm{n,samp}}^2}$ is the variance of the noise voltage at the output of the sampler consisting of the sampling switch and the capacitor C_{samp}; $S_{i,n,\mathrm{Gm}}$ is the power spectral density of the current noise of the transconductor. Noted that $S_{i,n,\mathrm{Gm}}$ is divided by K rather than K^2 because the current noise of the transconductor is sampled by a pulse signal with a duty cycle $(1/K)$ so that the noise has an extra aliasing factor of K to the output. Assuming white noise, $\overline{v_{\mathrm{n,samp}}^2}$ is (kT/C_{samp}) and $S_{i,n,\mathrm{Gm}} = 8kT\gamma G_{\mathrm{m}}$.

In the combined PD, the circuit noise sources from the SSPD undergo an additional attenuation by K in (2.6) due to the gating with a narrow pulse width when compared to the tri-state PFD/CP's noise sources. Due to this attenuation, the contribution from the SSPD to the noise at the output of the combined PD is negligible and thus the total output noise is close to $S_{i,n,\mathrm{PFDCP}}$. For example, with f_{REF}=50MHz, C_{samp} =20fF, G_{m}=0.5mA/V and K=44π, $S_{i,n,\mathrm{SSPD}}$ is -247.3 dBc/Hz while $S_{i,n,\mathrm{PFDCP}}$=-238.6 dBc/Hz given I_{CP}=0.25mA, $(gm_{\mathrm{CP}}/I_{\mathrm{CP}})$=10 and $(T_{\mathrm{idle}}/T_{\mathrm{REF}}) = 5\%$.

Because of the addition of the SSPD, the total gain of the combined PD, $K_{\mathrm{PD,comb}}$, is larger than the gain of the PFD/CP, $K_{\mathrm{PD,PFD}}$. Therefore, compared with the PFD/CP, the combined PD has smaller input-referred noise because of the larger gain, but similar output noise. From (2.4),

it can be derived that the combined PD's gain can be up to 5.7 times (15dB) higher than the gain of the tri-state PFD/CP. This increased gain of the combined PD without any additional significant noise increase results in up to 15dB smaller noise contributions from the phase detector to the PLL's noise (referred to its input).

For a PLL design with a given loop transfer function $L(jf)$, the noise contributions in (2.5) from the VCO and the reference remain unaltered with the choice of a phase detector. Assuming the same VCO and reference frequency and loop filter design, the total phase detector's gain is also largely unaltered. Comparing a combined PD with a conventional PFD/CP given the same total phase detector's gain, the output noise of the combined PD dominated by its PFD/CP's noise is smaller than the noise of the conventional PFD/CP because the combined PD has smaller PFD/CP's gain and CP current while most gain of the combined PD is provided by the SSPD. As a result, the use of the combined PD gives smaller noise contribution to the PLL than the conventional tri-state PFD/CP used alone.

2.5 Circuit Design of a Low In-band Phase Noise PLL with Robust Operation

Based on the analysis presented above, a PLL using the proposed combined phase detector can maintain the disturbance robust operation of a PFD-based PLL while offering superior jitter performance similar to SSPD-based PLLs. These unique advantages of the proposed combined phase detector have been demonstrated with an integer-N PLL prototype targeted at clock synthesis or

two-step PLL (cascaded PLL) applications [8,9]. It operates with a reference frequency of 50MHz and provides an output at 2.2GHz with a loop bandwidth of 5MHz.

The phase domain model for the PLL with combined phase detector (see Fig. 2.8) is the same as for a classical integer-N PLL but with a lower noise phase detector. The PLL parameters such as $K_{\mathrm{PD,comb}}$, K_{VCO}, as well as the loop filter parameters can be determined for a given reference frequency, output frequency and settling behavior using a classical design procedure as outlined e.g. in [4]. Once these parameters are determined, the phase detector circuit level design proceeds as explained below.

2.5.1 Combined Phase Detector

To retain the frequency detecting ability of a tri-state PFD, the maximum output current of the SSPD in the combined PD needs to be smaller than $3I_{\mathrm{CP}}/(4N)$ as discussed in section 2.2. Leaving some margins for error in the gain of the SSPD, the maximum output current of the SSPD is chosen to be:

$$\overline{\Delta i_{\mathrm{SSPD,max}}} = \frac{K_S}{K} = \frac{2I_{\mathrm{CP}}}{\pi N} < \frac{3I_{\mathrm{CP}}}{4N} \tag{2.7}$$

Now, the total gain of the combined PD can be expressed as:

$$K_{\mathrm{PD,comb}} = \frac{I_{\mathrm{CP}}}{2\pi} + \frac{NK_S}{K} = \frac{5I_{\mathrm{CP}}}{2\pi} \tag{2.8}$$

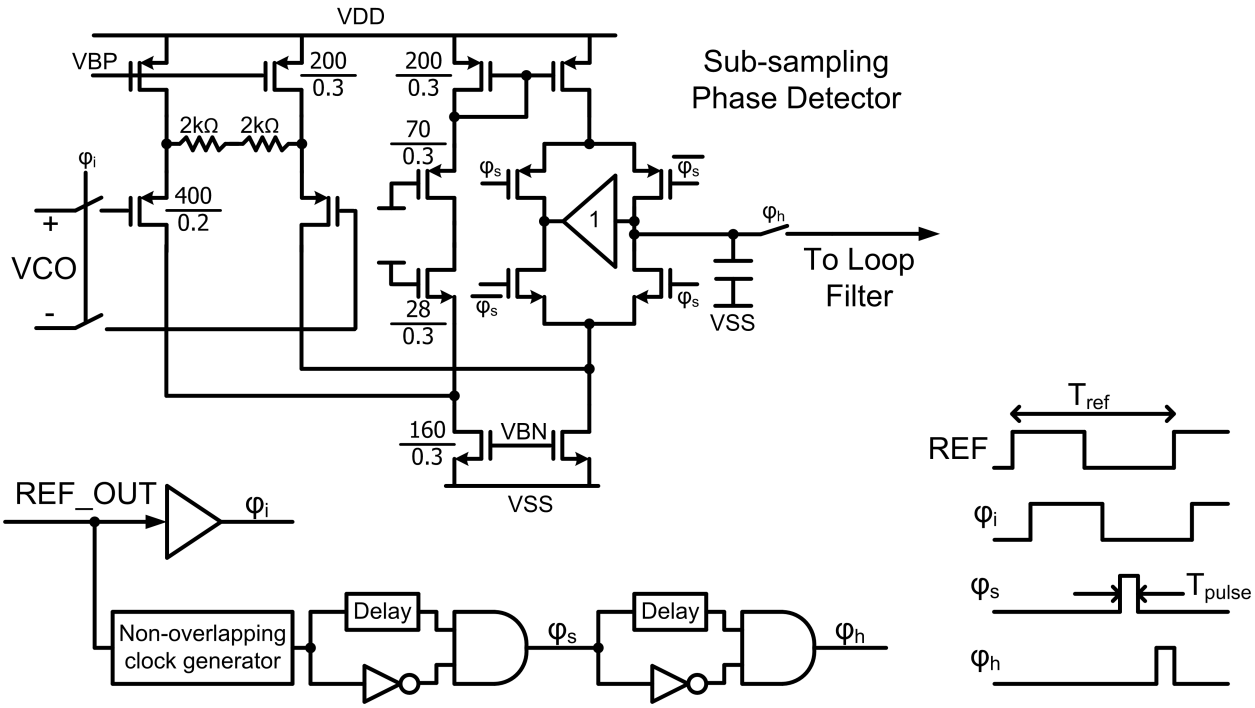


Figure 2.9: Circuit implementation of the sub-sampling phase detector. The units for W and L are μm.

Given $K_S = A_{\mathrm{VCO}} G_{\mathrm{m}}$, the value of the transconductor can be calculated as:

$$G_{\mathrm{m}} = \frac{4}{5} \times \frac{K_{\mathrm{PD,comb}}}{A_{\mathrm{VCO}}} \times \frac{K}{N} \tag{2.9}$$

Assuming $K_{\mathrm{PD,comb}} = \frac{1.25}{2\pi}$(mA), $A_{\mathrm{VCO}} = 1$V differential and the gain reduction factor of K is chosen to be πN, the value of the transconductor, G_{m}, is equal to 0.5(mA/V) and I_{CP}=0.25(mA). Given the chosen parameters, the overall in-band phase noise contributed by the band-limited

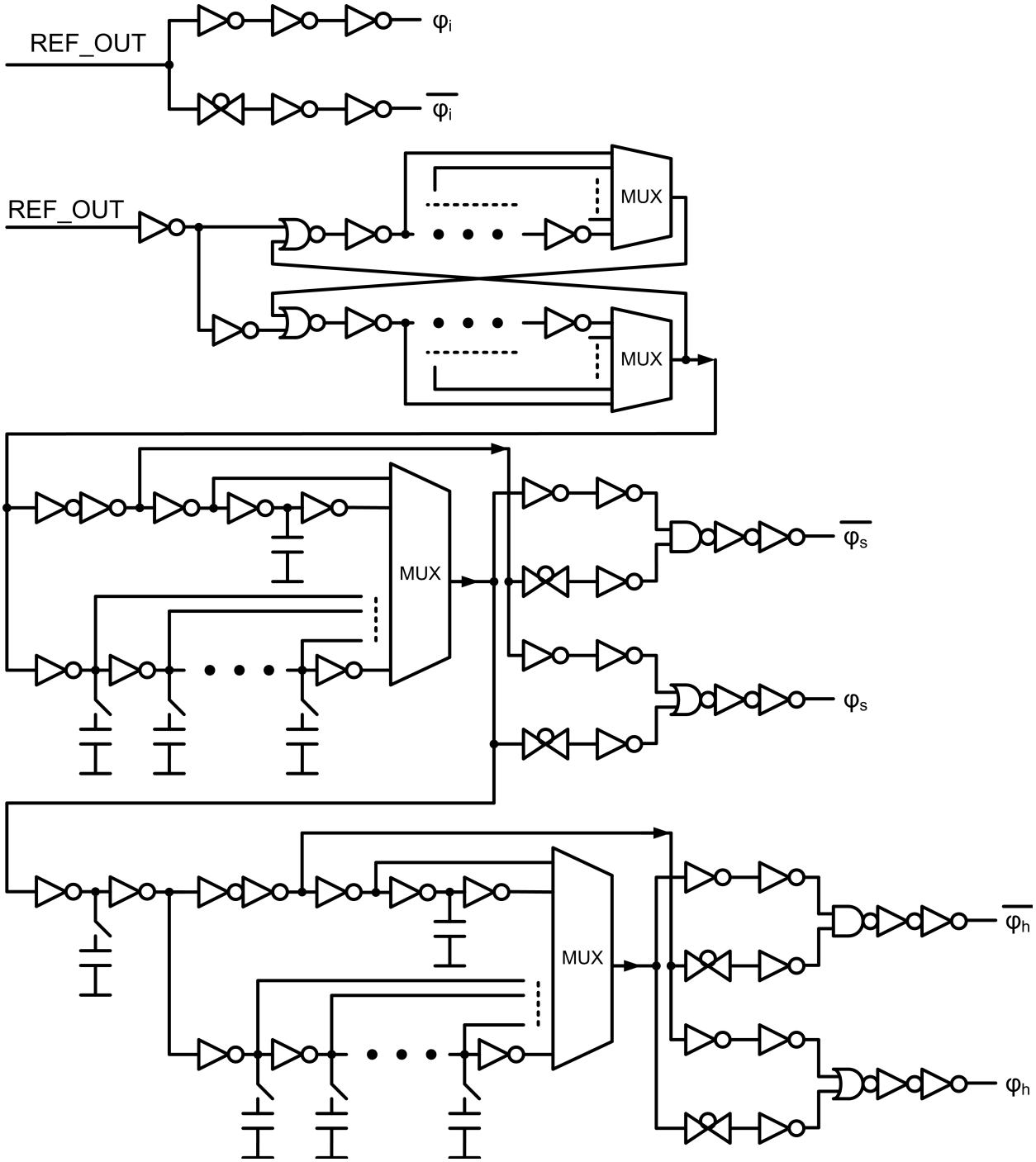


Figure 2.10: Detailed implementation of the pulse generator used in the sub-sampling PD

SSPD noise and PFD/CP noise is given by:

$$\begin{aligned}\mathcal{L}_{\text{inband}} &= \frac{N^2}{2}\left(\frac{S_{i,n,\text{SSPD}}+S_{i,n,\text{PFDCP}}}{K^2_{\text{PD,comb}}}\right)=\frac{N^2}{2}\left(\frac{16S_{i,n,\text{SSPD}}}{25K^2_{\text{PD,SSPD}}}+\frac{S_{i,n,\text{PFDCP}}}{25K^2_{\text{PD,PFD}}}\right)\\ &=\frac{16}{25}\left(\frac{kT}{C_{\text{samp}}}\cdot\frac{1}{A^2_{\text{VCO}}}\cdot\frac{1}{f_{\text{REF}}}+\frac{4kT\gamma}{G_{\text{m}}}\cdot\frac{K}{A^2_{\text{VCO}}}\right)+\frac{8\pi^2kT\gamma N^2}{25I_{\text{CP}}}\left(\frac{gm_{\text{CP}}}{I_{\text{CP}}}\right)\left(\frac{T_{\text{idle}}}{T_{\text{REF}}}\right)\end{aligned} \quad (2.10)$$

With f_{REF}=50MHz, N=44, C_{samp} =20fF, $(gm_{\text{CP}}/I_{\text{CP}})$=10 and $(T_{\text{idle}}/T_{\text{REF}}) = 5\%$, the overall inband noise floor is as low as -134.2 dBc/Hz.

The detailed transistor implementation of the sub-sampling phase detector is shown in Fig. 2.9. A sample-and-hold filter is used to reduce the reference ripple caused by the sub-sampling phase detector because it generates a SINC function with a notch at reference frequency [10]. Fig. 2.10 shows the detailed circuits of the pulse generator programming the pulse width and delay by changing the delay cells between two inputs of the AND gates. In addition, a unity-gain buffer is inserted in the transconductor to maintain the same voltages at the current sources' drain nodes and at the capacitor of loop filter. The buffer reduces the output current ripple due to charge sharing between these nodes during switching.

2.5.2 Voltage Controlled Oscillator, Programmable Divider and Loop Filter

The circuit implementation of the VCO is shown in Fig. 2.11. An inverter-based LC-VCO is chosen to avoid the flicker noise contribution from the bias current source [11]. The VCO uses a 6-bit control for setting the capacitance of the capacitor bank to tune the frequency coarsely and standard MOS varactors for fine-tuning the frequency. The VCO was designed to have a

frequency tuning gain (K_{VCO}) of 150MHz/V (fine-tuning) and a tuning range from 1.9GHz to 2.3GHz (including coarse tuning). The simulated phase noise is -112dBc/Hz at 1MHz offset and the used Q of the inductor is 6.6 at 2.2GHz.

The block diagram of the programmable divider is shown in Fig. 2.12. The divider has a ripple structure similar to a truly modular divider which is composed of a chain of divide-by-2 or 3 modules [12] [13]. Unlike [12], the cell in this implementation provides an additional modulus of 4 in addition to 2 and 3 to extend the programmable range. This block was fully synthesized with standard logic cells.

As shown in Fig. 2.13, the on-chip loop filter consists of a series resistor with the value of

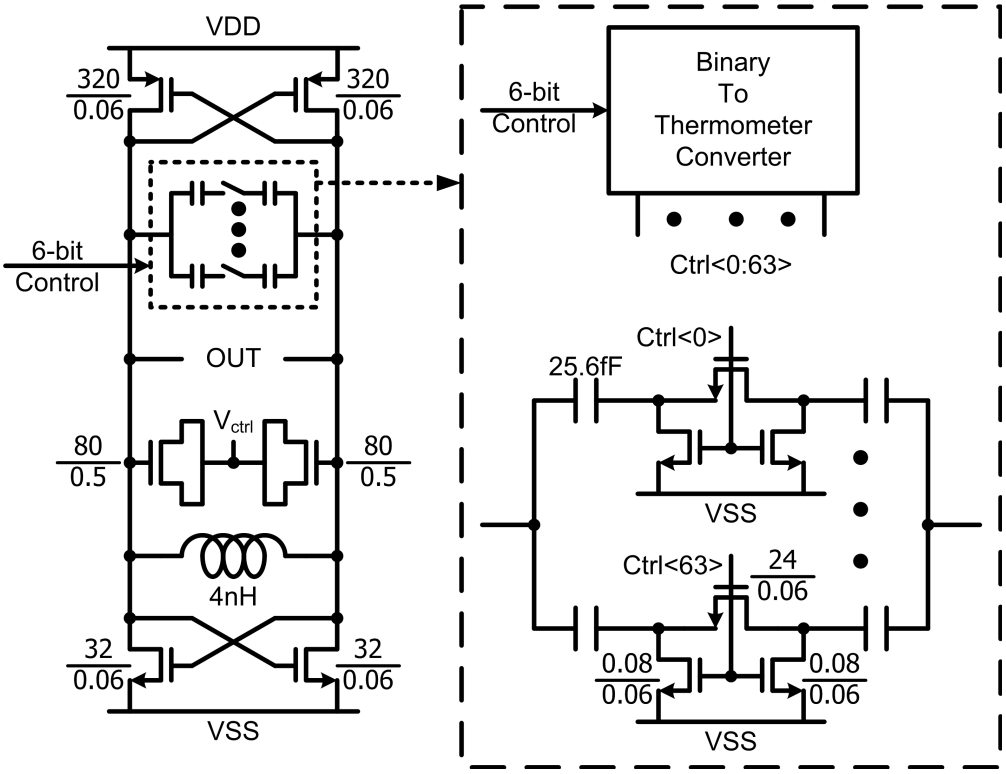


Figure 2.11: Circuit implementation of the LC-VCO used in the PLL. The units for W and L are μm.

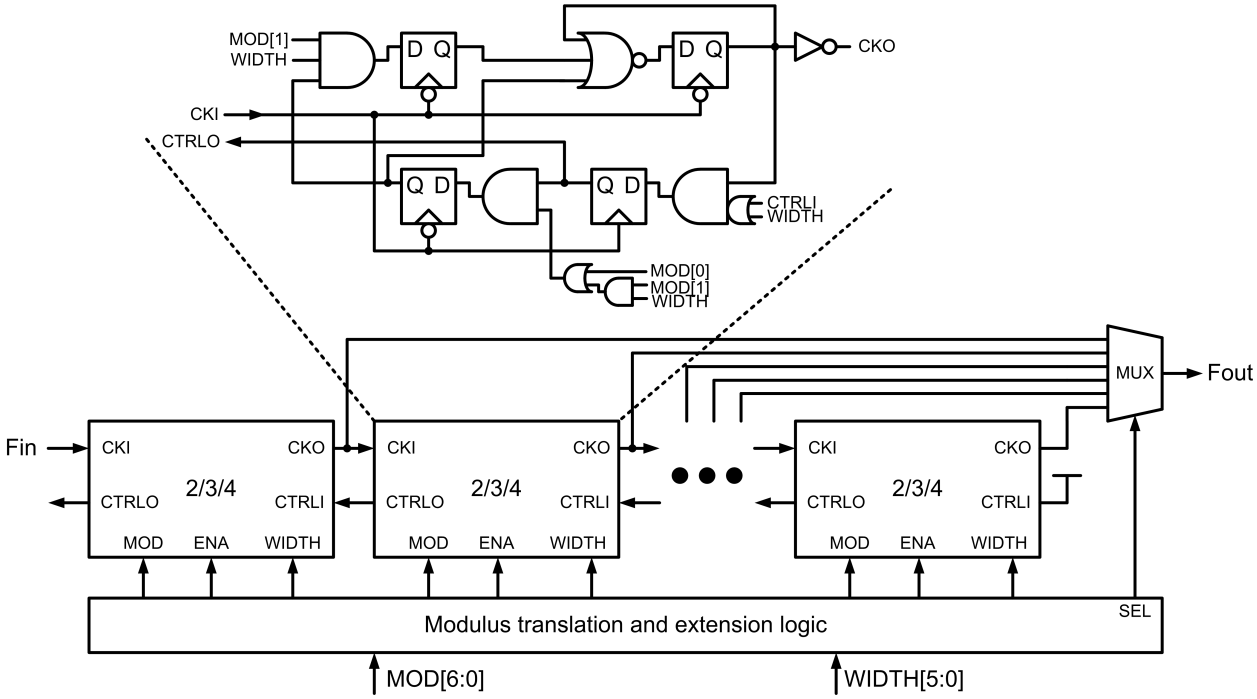


Figure 2.12: Block diagram of the frequency divider

12.6kΩ, a series capacitor of 31.7pF and a parallel capacitor of 1.3pF. These small capacitor sizes in the loop filter can be implemented on-chip with MOM capacitors to avoid leakage. A unity-gain buffer is placed between the loop filter and the VCO to isolate the loop filter from pulling by the large VCO swing since only a small capacitance is used in loop filter for wide loop bandwidth. This buffer acts as a first-order filter that increases the order of the loop filter; its noise only impacts the loop filter noise contribution which is not a significant noise contribution in the PLL.

2.6 Experimental Results

The proposed PLL was implemented in a 65nm digital low leakage CMOS process. Fig. 2.14 shows the die photo of the chip. It occupies an area of 0.24mm^2 (without bond-pads) while its

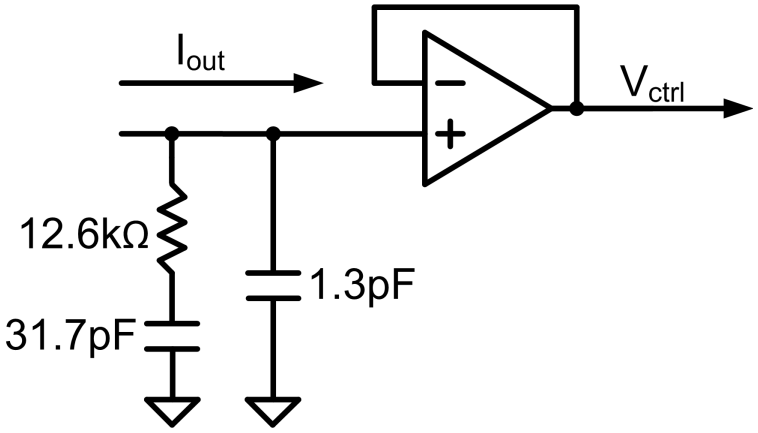


Figure 2.13: Loop filter implementation

loop filter area is 0.04mm^2. The circuits draw 8mA (excluding the 50Ω output buffers) of which 3mA is drawn by the LC-VCO. The prototyped PLL can operate with three different modes for the phase detector: tri-state PFD only, sub-sampling PD only, and combined PD.

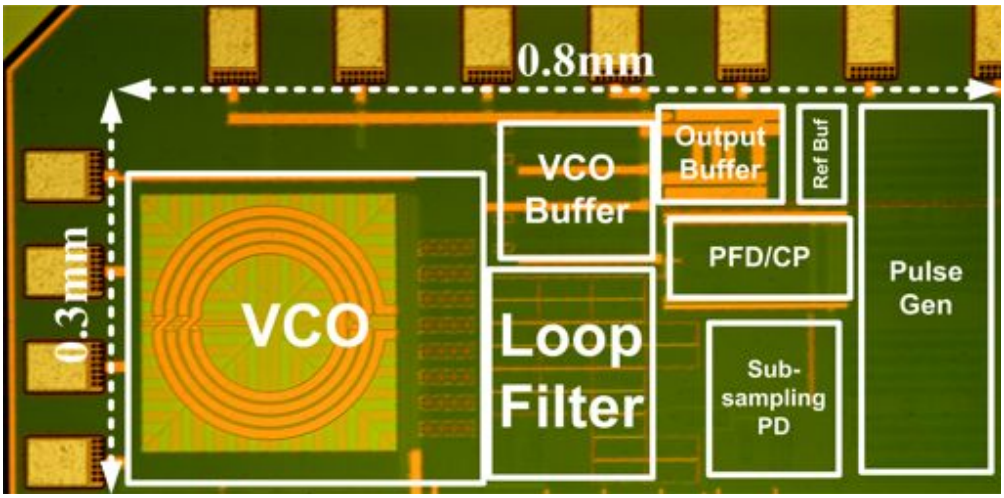
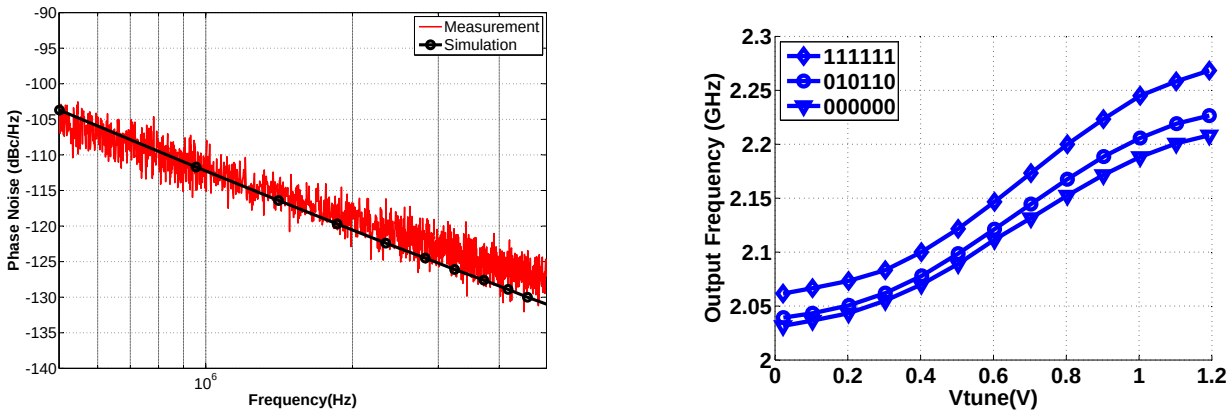


Figure 2.14: Die photo of the PLL

The measured phase noise and tuning curves of the VCO are shown in Fig. 2.15. The measured phase noise is -112dBc/Hz at 1MHz offset which matches the simulation. The measured frequency tuning range of the VCO is from 2.04GHz to 2.22GHz for the cap-bank setting of 6'b010110 and



(a) (b)

Figure 2.15: (a) Measured and simulated phase noise spectrum of the VCO (b) Measured tuning curve of the LC-VCO for three cap-bank settings

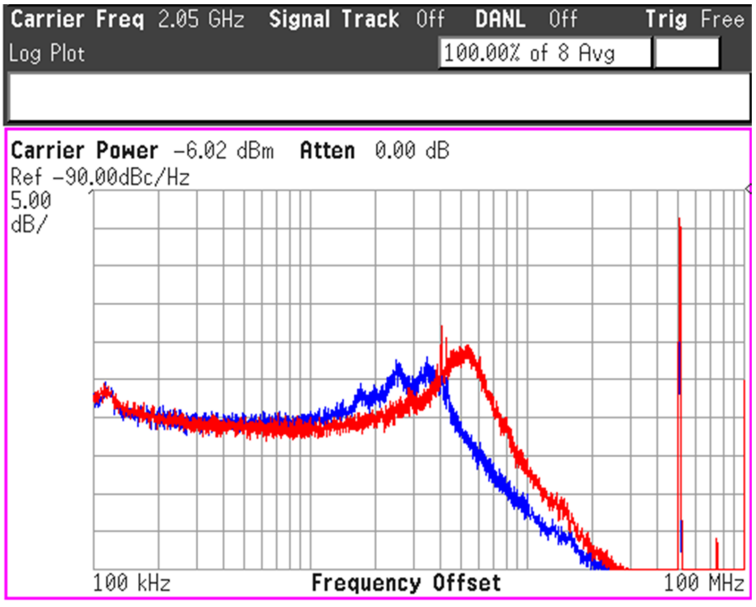


Figure 2.16: Measured phase noise spectrum of the PLL when operating with a reference frequency of 50MHz and a divisor of 41 and output frequency of 2.05GHz (blue trace lower bandwidth and lower peaking) and divisor of 44 and output frequency of 2.2GHz (red trace higher bandwidth and with higher peaking)

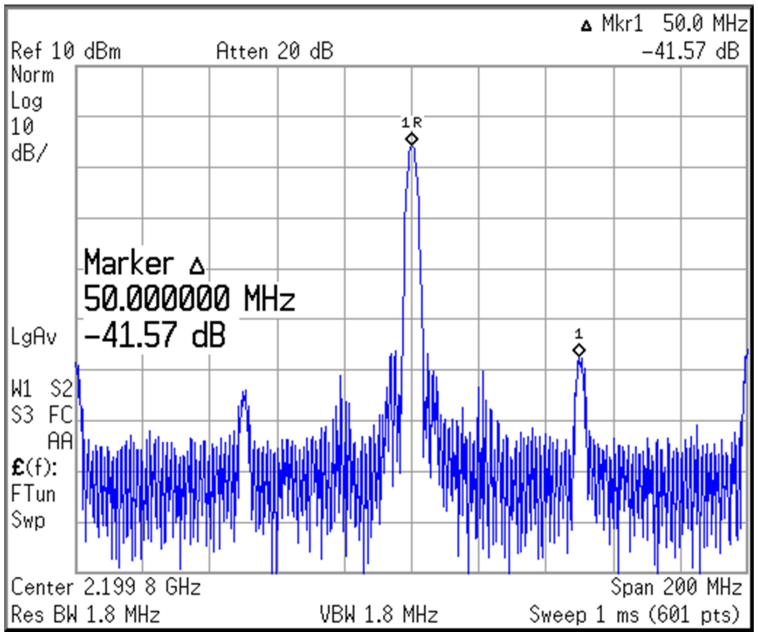


Figure 2.17: Measured reference spurs of the PLL when operating at 2.2GHz

using coarse tuning the VCO output frequency range is from 2.03GHz to 2.27GHz. The PLL was driven with a 50MHz crystal reference source [14]. The output frequency can be set from 2.05GHz to 2.2GHz in steps of 50MHz by changing the frequency division ratio with the above cap-bank setting. The in-band phase noise level is very consistent across the output frequency range. Fig. 2.16 shows the output phase noise spectrum of the PLL, measured with an Agilent E4446 Spectrum Analyzer, at two different output frequencies, 2.05GHz and 2.20GHz respectively.

The reference spurs in the PLL output have been measured in Fig. 2.17. The relatively large reference spur comes from the kickback in a sub-sampling PD [15] and coupling from reference signal to VCO supply through the ESD circuitry. [2]

Larger reference spurs were observed in the sub-sampling PLL because the spurs are not sup-

[2]The dependence of the reference spur on the interaction between the VCO and SSPD discussed in [15] was also observed in the measurement by changing the size of the inverter-based buffer between the VCO and SSPD. The spur reduction technique adopted for an SSPD can be applied into the combined PD.

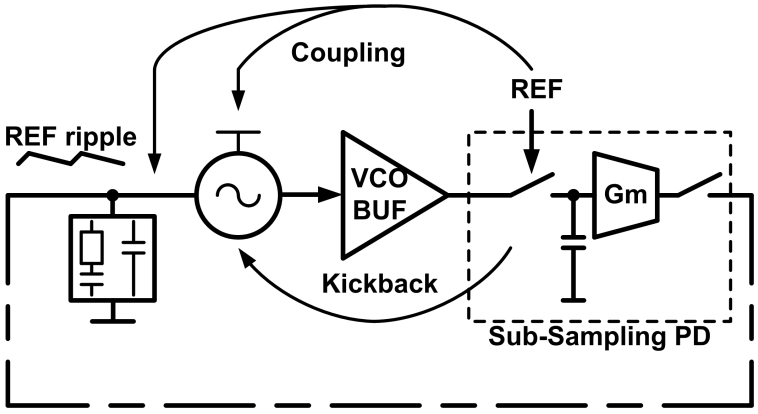


Figure 2.18: Root causes to reference spurs in a sub-sampling PLL

pressed by its wide loop bandwidth. The reference spurs of a sub-sampling PLL are usually generated by the ways shown in Fig. 2.18. The first one is the coupling from input reference to the supply or the control voltage of the VCO. But, it can be decreased by careful layout and good isolation between critical blocks. Secondly, the reference spurs are due to the leakage of loop filter which requires the sub-sampling PD to provide compensating current for its pulse-controlled duration and then leads with a large ripple on the control voltage of the VCO. The reference ripple can be reduced by implementing the loop filter with a sample-and-hold filter or MOM capacitors for few reference disturbances from the sub-sampling PD to loop filter.

The reference spurs are also caused by the kickback from the sub-sampling PD through a VCO buffer and then to the VCO. It is a serious problem to a sub-sampling PLL because the VCO output is constantly sampled by the reference signal in the SSPD. Thus, the reference spurs would be generated by directly modulating the VCO output with the reference disturbance. In addition, non-ideal effects of the sampling switch such as charge injection or clock feed-through and the VCO load change caused by the sampling operation can also influence the VCO output and make

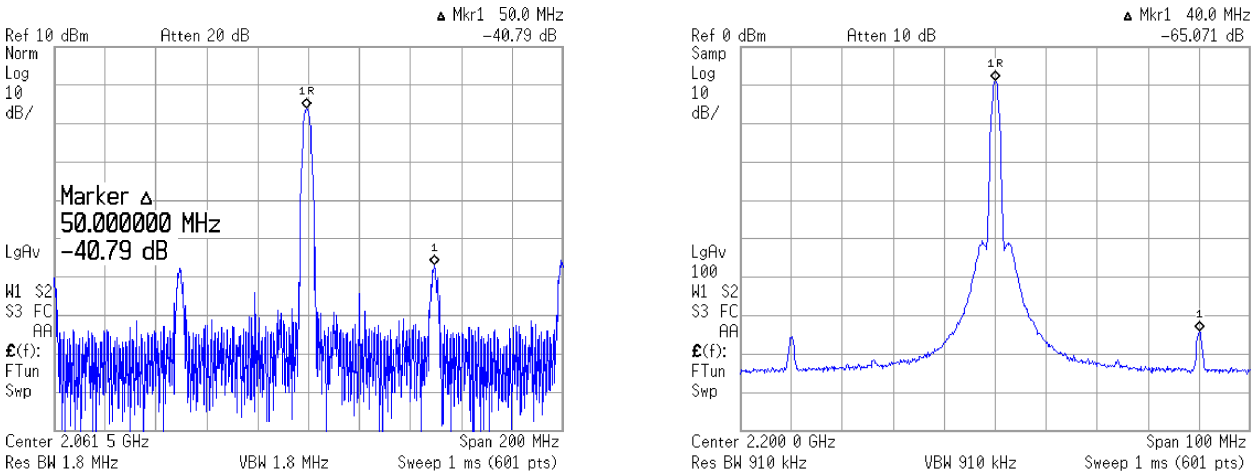
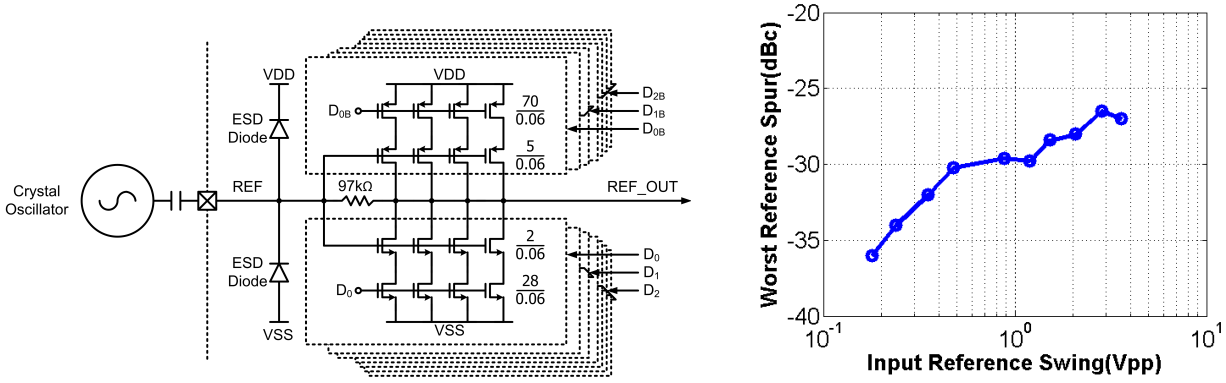


Figure 2.19: (a) Measured VCO output spectrum while the SSPD's output is disabled (b) Measured reference spurs by decreasing the driving setting of the buffer between the VCO and SSPD as f_{REF}=40MHz

reference spurs become large. The reference spurs is reduced by increasing the isolation between the SSPD and VCO. The impact of the kickback was observed by disabling the SSPD output, but keeping the VCO output being disturbed by the SSPD. In this case, the measured spurs at the VCO output were shown in Fig. 2.19(a). Besides, while the PLL is locking, smaller reference spurs were measured in Fig. 2.19(b) by changing the size of the inverter-based VCO buffer to increase isolation as well as lowering input reference frequency to reduce kickback.

The reference spurs were also observed for different reference swings. The reference swing is adjusted by the digitally controlled strength of the reference buffer as Fig 2.20(a). While changing the reference swing, the worst reference spurs were measured in Fig. 2.20(b) showing that larger reference swing leads to poorer reference spurs because it makes the kickback become more serious. It is noted that there may be large variations on the measured reference spurs given the certain reference swing because the spurs are more related with the edges of reference and VCO



(a) (b)

Figure 2.20: (a) Circuit diagram of the reference buffer with the digitally controlled strength (b) Measured reference spurs for different reference swings

signals as discussed in [15]. In fact, to alleviate the problem of high reference spurs caused by the sub-sampling PD, the techniques proposed in [15] can also be applied into future versions of the combined PD.

2.6.1 Robustness of the Phase Detector to Supply Voltage Disturbances

It has been experimentally verified that a PLL with the proposed combined PD has a better rejection to disturbances on the power supply compared to a PLL with a sub-sampling PD alone.

A PLL integrated with digital circuits may experience periodic disturbances through the substrate, the power supply or other means. In the experimental set-up, these disturbances were collectively modeled as periodic impulses to the supply voltage of the VCO. Periodic impulses were chosen to mimic the effect of digital circuits and the supply voltage of the VCO was chosen because the sub-sampling PD is most sensitive to phase change of VCO's output.

The disturbances are generated by applying a pulse signal to VCO supply through a large ac-

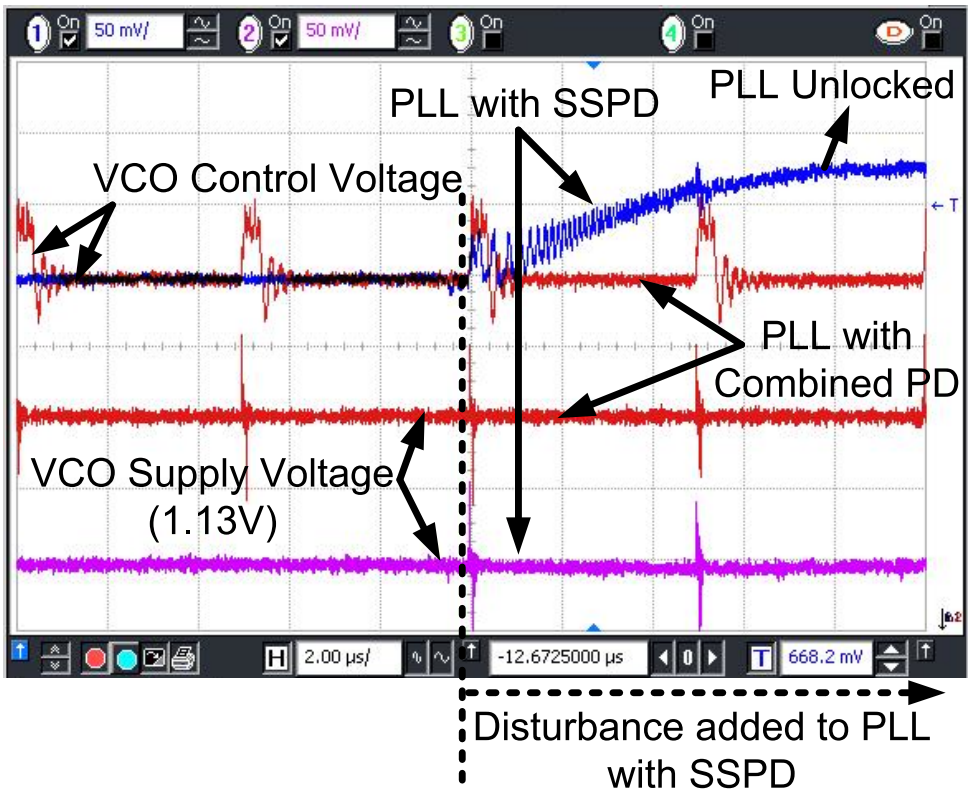


Figure 2.21: Effect of VCO supply voltage disturbances on the PLL's operation; using the combined PD the PLL can sustain substantial disturbances; using the sub-sampling PD only, the PLL loses lock as soon as the disturbances are applied.

coupling capacitor. Fig. 2.21 shows the effect of these supply voltage disturbances on a PLL using the combined PD versus the sub-sampling PD alone. For supply disturbances with the peak-to-peak swing of around 100mV, the control voltage of the VCO in a PLL with the combined PD shows periodical ripples, but returns to the original value. However, the control voltage of VCO in a PLL with the sub-sampling PD alone jumps to another value which makes the PLL lose lock after turning on the disturbances.

Fig. 2.22 shows another result confirming the superior immunity of the PLL with a combined PD to disturbances. While supply disturbances are present, the PLL is switched between two

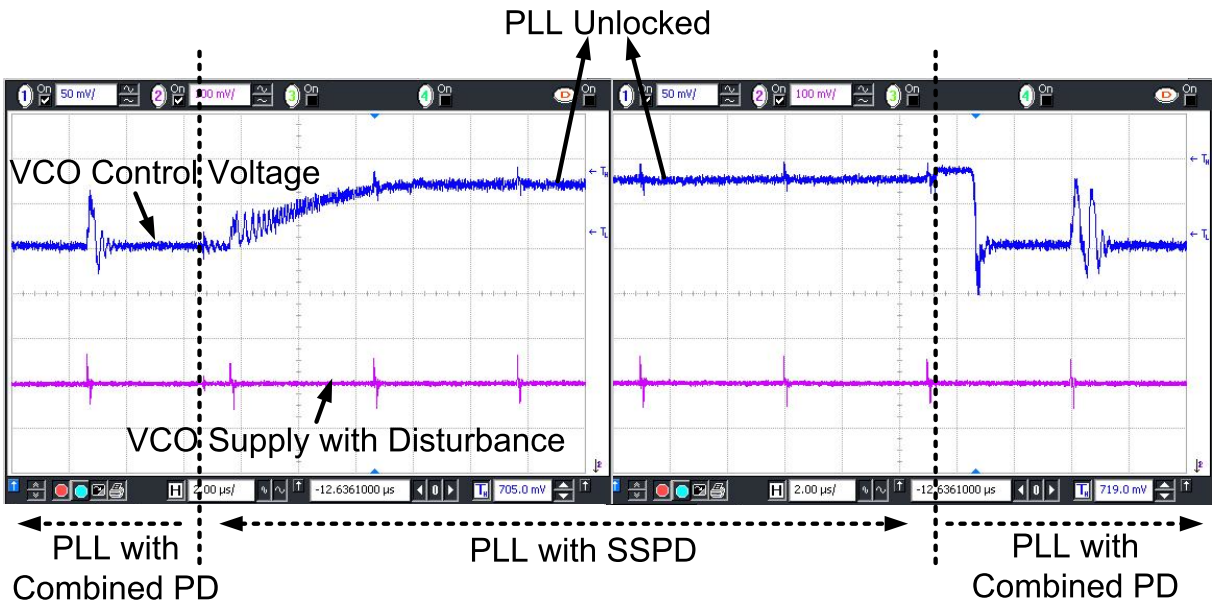


Figure 2.22: While operating with disturbances on the VCO supply, the PD of the PLL is switched between the combined and sub-sampling-only operation mode; in sub-sampling-only mode, the PLL loses lock, but it recovers as soon as switching back to combined operation mode.

modes of phase detection: one with the combined PD and the other with sub-sampling PD only. When the phase detection mechanism is changed from the combined PD to the sub-sampling PD, the control voltage of VCO jumps to another value and the PLL looses lock due to the disturbances on the VCO's supply. As soon as the PFD is reactivated and the PLL operates with the combined PD again, the control voltage of the VCO goes back to the original value and the PLL locks correctly.

2.6.2 Low In-band Phase Noise

The output phase noise spectra of the PLL with the combined phase detector and with the tri-state PFD alone (i.e. the sub-sampling phase detector is turned off) are measured with an Agilent

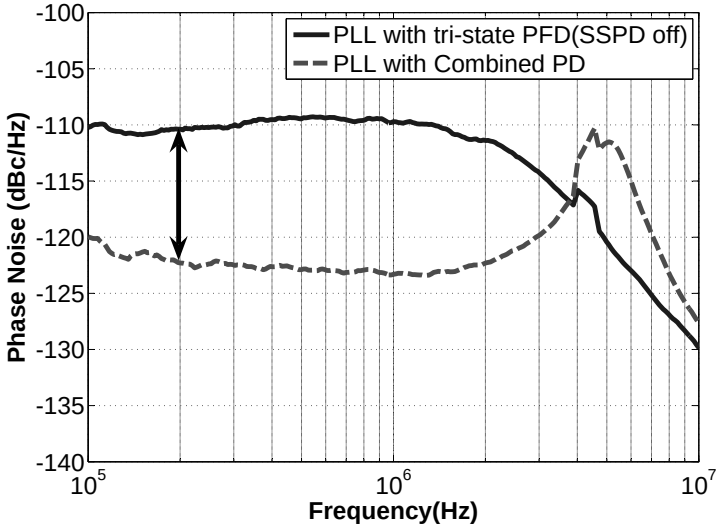


Figure 2.23: Measured phase noise spectrum of the PLL when operating at 2.2GHz with the combined phase detector and the tri-state phase detector only

E5052A Signal Analyzer and compared in Fig. 2.23. By turning on the sub-sampling phase detector, the in-band phase noise is reduced from -110dBc/Hz to -122dBc/Hz at a 200-kHz frequency offset. The measured RMS jitter shows an improvement from 564fs to 448fs (integrated from 100kHz to 10MHz) and from 649fs to 484fs (integrated from 10kHz to 40MHz). The in-band phase noise reduction is 12dB, even though the phase detector's gain increase suggests a possible improvement up to 14dB[see (2.4) and (2.8)]. However, in this measurement when operating with the combined phase detector, the in-band noise becomes dominated by the reference phase noise, and at that point the increased phase detector gain has no more effect [see (2.5)].

The reference noise from the used 50MHz CPRO XTAL was measured by -157dBc/Hz at 200 kHz in Fig. 2.24; this results in an in-band phase noise of -124dBc/Hz at 200 kHz with a divisor of 44. The measured noise level is -122dBc/Hz; the 2dB increase can be attributed to the noise contributed by the on-chip reference buffer. In addition, a set of measurements was done by using

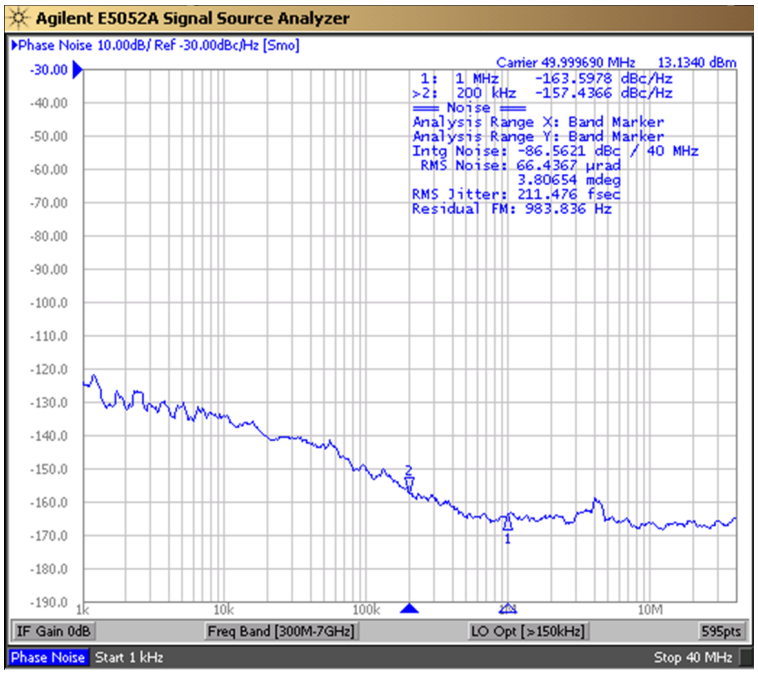


Figure 2.24: Measured phase noise spectrum of the used crystal reference source showing -157.4dBc/Hz at 200kHz and -163.6dBc/Hz at 1MHz.

increasing pulse widths (i.e. reducing K) and thus increased the combined phase detector's gain; the in-band phase noise initially reduced as expected; but it stopped reducing at a -122dBc/Hz level most likely due to the contribution of the reference noise given its measured level as calculated above since the PD's noise contribution for large pulse widths is not dominated to the in-band phase noise.

The noise peaking observed in Fig. 2.23 at the edge of the loop bandwidth when operating with the combined phase detector is caused by the reduced phase margin due to an increased loop bandwidth while the sub-sampling phase detector is active[3]. The peaking observed in measurement is seen in simulation also. Fig. 2.25 shows a comparison of the measured phase noise spectrum

[3]The PLL was required to operate both with a combined PD and tri-state PFD in order to demonstrate the phase noise improvement. When the PLL is switched to using the combined PD, its phase margin degrades, resulting in noise peaking. However, in a real design, the PLL will only be operating with a combined PD. The loop bandwidth and phase margin requirements will be known a-priori and the issue of noise peaking can be avoided.

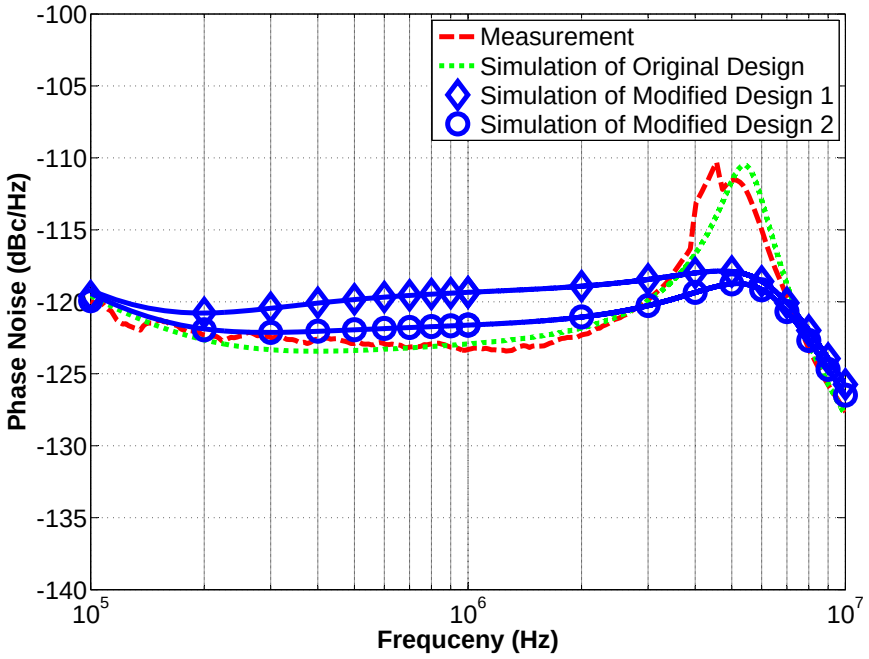


Figure 2.25: A comparison between the measured and simulated phase noise spectrum of the PLL using the combined phase detector, and the simulated phase noise spectrum of the PLL with a modified loop filter to improve the loop's phase margin.

with simulated phase noise spectrum of the PLL. The peaking can be removed in a redesign by changing the loop filter so that there is a better phase margin for the PLL. A simulation was done with a first modified loop filter changing the loop's pole and zero so that the PLL with the combined PD has a 46-degree phase margin and no peaking. The modified loop filter has a series RC branch with a series resistor of 9.2kΩ and a series capacitor of 69.1pF, and a parallel capacitor of 0.17pF. A second design example uses a modified loop filter with a series resistor of 9.2kΩ and a series capacitor of 69.1pF and a parallel capacitor of 0.5pF for a 42-degree phase margin but lower in-band noise. Fig. 2.25 shows the simulated phase-noise spectrum of the PLLs with the modified loop filters which maintain excellent in-band phase noise performance. The RMS jitter integrated

from 10kHz to 10MHz is 448fs in the measurement, 447fs in the simulation of the original design, 339fs for the modified design 1 and 294fs for the modified design 2.

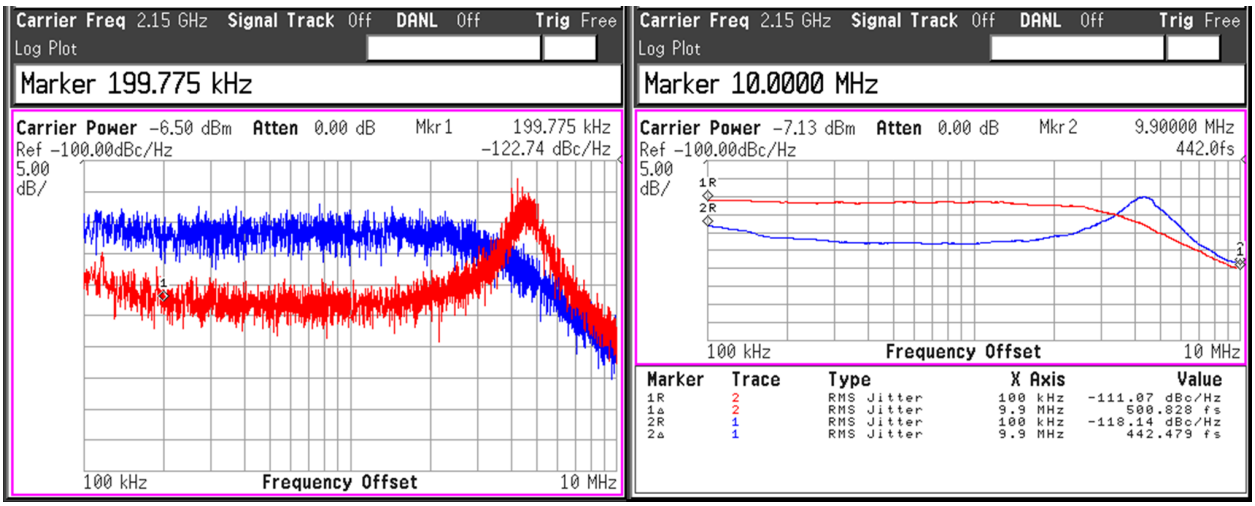


Figure 2.26: Measured phase noise spectrum of the PLL with the combined PD and the tri-state PFD only as the output frequency of 2.15GHz

With the divisor of 43, the output spectrum of the PLL with the combined PD and the tri-sate PFD was measured in Fig. 2.26. By changing from the tri-state PFD to the combined PD, the measured in-band phase noise is reduced from -112dBc/Hz to -123dBc/Hz at a 200-kHz frequency offset and the measured RMS jitter shows an improvement from 501fs to 442fs (integrated from 100kHz to 10MHz). Compared with operating at 2.2GHz, the in-band phase noise of the PLL at 2.15GHz is a little better because the lower division ratio reduces the noise contribution from the phase detector and reference.

The in-band phase noise level is a function of the amplitude of the applied reference signal [6, 7]. The measured in-band phase noise is plotted as a function of the peak-to-peak reference amplitude in Fig. 2.27 while keeping the supply voltage of the chip constant at 1.1V; the reference buffer in the design has a simulated small signal gain of 8.6x when operating from 1.1V; a 20dB/dec

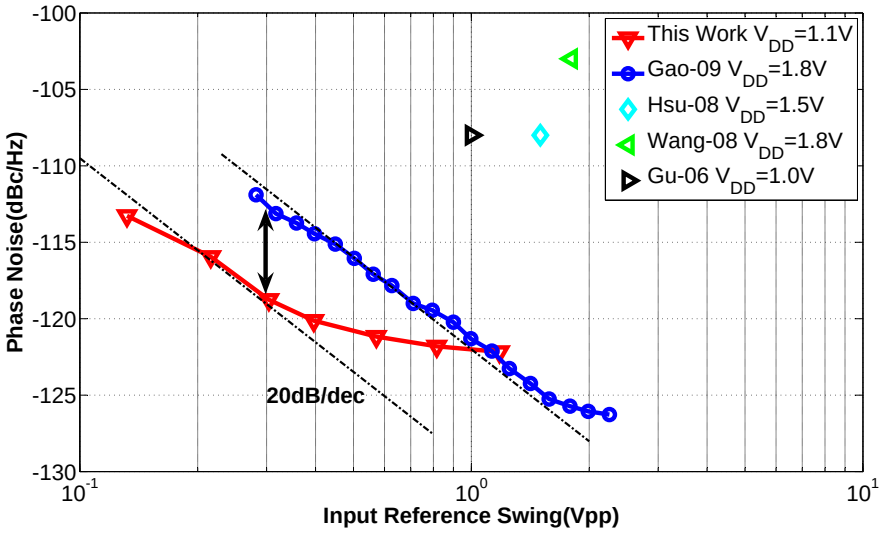


Figure 2.27: Measured in-band phase noise vs reference swing; the presented PLL operates at 1.1 V, whereas Gao-09 [6] operates at 1.8V; for Hsu-08 [16], Wang-08 [17] and Gu-06 [18] the peak-to-peak reference swing has been assumed to be equal to the respective chip supply voltage.

improvement is observed until the phase-noise stops improving for large reference swings which result in slewing of the output reference buffer.

In comparison with the PLL in [6], operating with a 1.8V supply, the PLL has a 6dB better in-band phase noise at the reference amplitudes lower than 300mV. Due to a smaller available supply voltage in 65nm, the PLL cannot use the same large reference signal as in the 180nm technology. Even with a larger available reference signal, the PLL achieves an inband phase noise comparable to [6, 15]. A detailed comparison of this work with other implementations is summarized in Table 2.1.

2.7 Conclusions

This chapter proposes a combined PD for PLLs with robust operation under disturbances while offering low in-band phase noise and low jitter. The combined PD uses a low noise sub-sampling PD in parallel with a conventional tri-state PFD in such way that it retains the frequency locking feature of a tri-state PFD while obtaining the superior in-band phase noise performance of a sub-sampling PD.

Simulation-based comparison of an SSPD, an FLL-assisted SSPD, a conventional tri-state PFD and the combined PD shows that a PLL using an SSPD is sensitive to any disturbance, a PLL using an FLL-assisted SSPD will regain lock but after a long delay of being unlocked, while a PLL using the combined PD is immune to disturbances and quickly reaches steady state after disturbances, similarly to PLLs with traditional PFDs.

Measurement-based comparison of the robustness of the combined PD and the SSPD has been made and the combined PD was experimentally shown to be more robust. The measured in-band phase noise of the PLL is improved from -110dBc/Hz to -122dBc/Hz at 200kHz between the conventional PFD and the combined PD.

Table 2.1: Performance comparison table

	This work	[6]	[15]	[16]	[18]	[19]	[20]	[21]	[22]
Output Frequency	2.2GHz	2.21GHz	2.21GHz	3.67GHz	3.125GHz	2.08GHz	3.1GHz	4GHz	2.3GHz
Reference Frequency	50MHz	55.25MHz	55.25MHz	50MHz	62.5MHz	130MHz	108MHz	40MHz	48MHz
Supply Voltage	1.1V	1.8V	1.8V	1.5V	1V	1.2V	1.2V	1.2V	1.8V
Inband Phase Noise @Maximum A_{REF}	-122dBc/Hz @ 200kHz	-126dBc/Hz @ 200kHz	-121dBc/Hz @ 200kHz	-108dBc/Hz @ 400kHz	-108dBc/Hz @ 100kHz	-119dBc/Hz @ 1.4MHz	-110dBc/Hz @100kHz	-105dBc/Hz @ 200kHz	-112dBc/Hz @ 50kHz
Reference Spur	-41.6dBc	-46dBc	-80dBc	-65dBc	-	-47.8dBc	-	-71dBc	-55dBc
Power	8.8mW	7.6mW	3.8mW	46.7mW	25mW	20.4mW	27.5mW	5mW	17.3mW
Active Area	$0.24mm^2$	$0.18mm^2$	$0.20mm^2$	$0.95mm^2$	$0.43mm^2$	$0.42mm^2$	$0.32mm^2$	$0.22mm^2$	$0.75mm^2$
CMOS Technology	65nm	0.18μm	0.18μm	0.13μm	0.13μm	65nm	65nm	65nm	0.18μm

Chapter 3

A Supply-Scalable Differential Amplifier With Pulse-Controlled Common-Mode Feedback

This work proposes a pulse-controlled common-mode feedback circuit for a supply-scalable fully-differential amplifier. The pulse-controlled common-mode feedback circuit overcomes the large area cost associated with a conventional R-C common-mode feedback circuit while maintaining a high gain and large output signal range for the amplifier. The amplifier is implemented in a low power/leakage 65nm CMOS technology with NMOS and PMOS threshold voltages of 0.36V and -0.44V and operates at a supply voltage of 0.6V to 1.2V. The prototype has an active area of $0.01mm^2$ and it consumes 1.21mW at 0.6V, 1.94mW at 0.9V, and 3.07mW at 1.2V. The measured output noise spectrum density is $21.5nV/\sqrt{Hz}$ at 0.6V, $26.1nV/\sqrt{Hz}$ at 0.9V, and $30.3nV/\sqrt{Hz}$ at

1.2V. For a total harmonic distortion of 1%, the maximum signal of the amplifier with frequency 10MHz is measured as -2.3dBm at 0.6V, 3.8dBm at 0.9V, and 6.1dBm at 1.2V; as expected, the linearity of the amplifier depends on its signal headroom which is in scale with the supply voltage.

3.1 Introduction

In the self-power or battery-free energy harvesting systems such as vibration-driven generators, the generated voltage strongly depends on external excitation and has much large variation. A power management with such voltage input is usually required to provide a stable supply to analog circuits, but it increases the cost and complexity of the systems [23]. Therefore, it is a desirable objective to have analog interfaces with flexible supplies. In addition, the analog interface circuits in modern mobile systems tend to operate at different supply voltage because the systems usually need higher supply voltage to process more applications, but lower voltage at sleep mode to save idle power. The supply-scalable analog interfaces also help extend the battery life because the systems supplied by batteries are able to tolerate larger voltage drop and then fully use the power of batteries shown in Fig. 3.1.

Supply-scalable circuits are receiving more attention in recent years [24] [25] because they are suitable for energy-harvesting systems with unstable supplies, but without extra power management. However, they meet more design challenges than low voltage circuits in a low power/leakage CMOS technology with transistors with large threshold voltage, especially for fully-differential amplifiers. The large threshold voltage leads to small margins on operating points of the amplifier making its bandwidth and gain easily become insufficient under a supply change. Body-input or

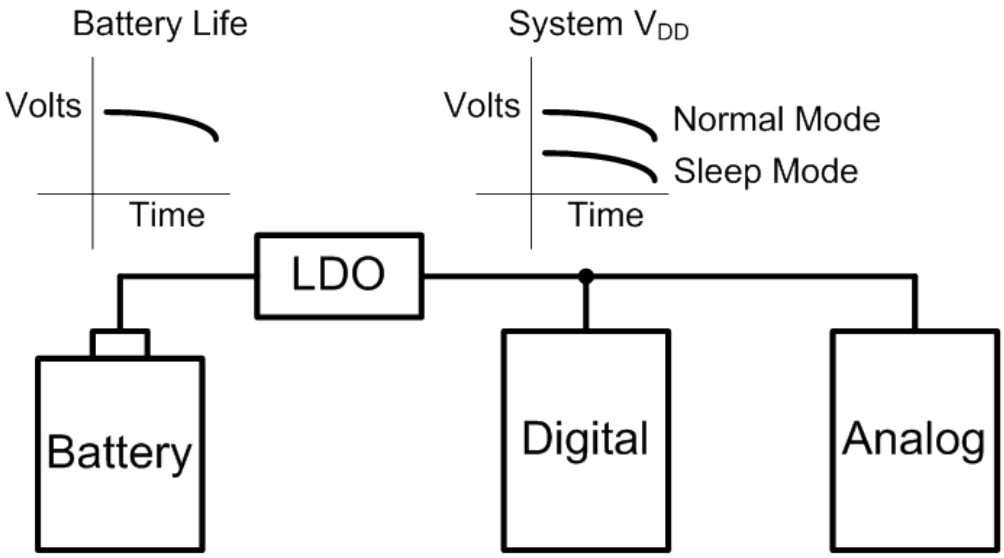


Figure 3.1: Analog circuits with flexible supply operation in mobile systems

body-bias circuits [26] can be applied to lower the threshold voltage by biasing the body-source junction for low voltage operation, but they have limited uses at a high supply. The on-resistance of analog switches associated with the threshold voltage has much variation to supplies which limits signal swing and bandwidth [27]. Switch bootstrapping circuits [28] are widely used for reducing the on-resistance of switches in low voltage circuits, but they may suffer from reliability problems for flexible supply operation. At a low supply, the gate-to-source voltage of the transistors for switches is fixed by the supply voltage to minimize switch non-idealities, but it may make the gate voltage exceed the breakdown voltage of the transistors while the supply voltage becomes high.

In addition to the challenges associated with differential signal path, the common-mode feedback circuit is another bottleneck for flexible supply operation. Three commonly used common-mode feedback circuits are: a passive R-C common-mode feedback circuit [29], an active differential-pair common-mode feedback circuit [30] and a switched-capacitor common-mode feedback cir-

cuit [31]. The R-C common-mode feedback circuit can operate at different supplies, but requires large resistance to maintain the high DC gain and large output swing. Differential-pair common-mode feedback circuit does not need large area passive components, but it has limited linear signal range for the main amplifier and is not suitable at a low supply. The switched-capacitor common-mode feedback circuit also has a smaller passive area, but its loop bandwidth and stability is very sensitive to the supply voltage because of the supply-dependent on-resistance of the switches. In addition, a big unsettled summing error leading to a wrong common-mode voltage for large differential signals can be caused by the large and nonlinear on-resistance switch resistance; at a low supply, these switches can not fully turn due to the large threshold voltage in low power/leakage processes. A novel pulse-controlled common-mode feedback circuit (PC CMFB) is proposed to significantly reduce the area of passive components and overcome the limitations of switch on-resistance for supply scaling.

A supply-scalable fully-differential amplifier with the PC CMFB was implemented in a low power/leakage CMOS process. Compared with conventional common-mode feedback circuits, the proposed PC CMFB has a smaller passive area without a gain reduction of the main amplifier. The chapter is organized as follows. Section 3.2 discusses the operation of the pulse-controlled common-mode feedback circuit. Section 3.3 describes the circuits of the supply-scalable fully-differential amplifier with the PC CMFB and section 3.4 presents the measurement results.

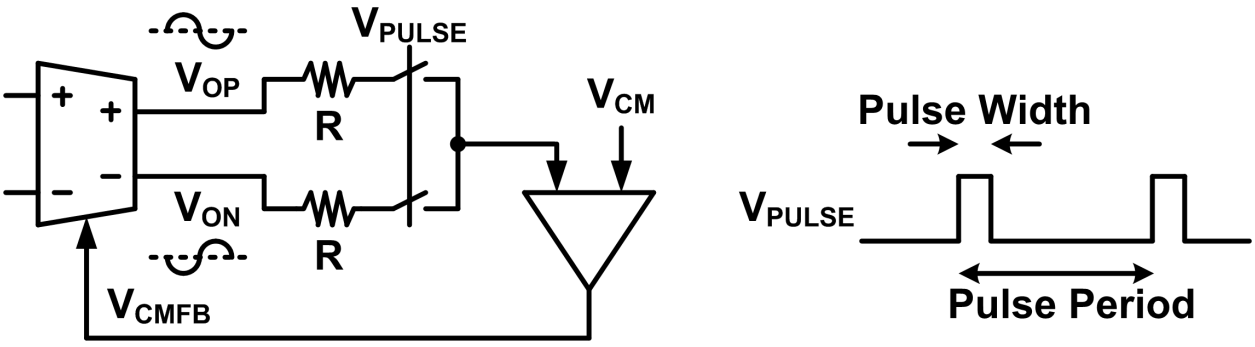
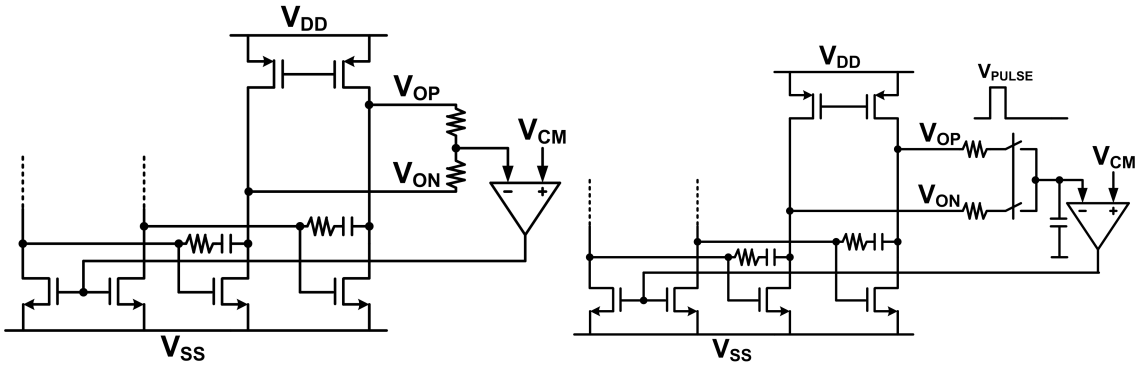


Figure 3.2: Proposed pulse-controlled common-mode feedback circuit

3.2 Pulse-controlled Common-mode Feedback

The block diagram of the proposed pulse-controlled common-mode feedback circuit is shown in Fig. 3.2. The pulse-controlled common-mode feedback circuit uses a similar structure to a R-C common-mode feedback circuit, but it replaces large resistors with smaller area pulse-controlled resistors to reduce the total area and cost of the common-mode feedback circuit. Fig. 3.3 shows the comparison between a conventional RC common-mode feedback circuit and the proposed pulse-controlled common-mode feedback circuit applied to the output stage of a fully differential two-stage amplifier. The pulse-controlled resistance can be implemented with small passive resistors followed by switches which turn on with a small duty cycle to have an equivalent large resistance [32]. By time-gating the resistors, their value gets multiplied by the inverse of the gating duty cycle and their area gets reduced by the duty cycle. While the area is smaller, the PC CMFB maintains the large output swing for the amplifier and does not reduce its gain. The impact of a large on-resistance of the switches is negligible since it is in series with a relatively large resistor. The resistors further isolate the amplifier output signal from the switching artifacts. As a result, the



(a) (b)

Figure 3.3: (a) Conventional passive R-C common-mode feedback circuit (b) Proposed pulse-controlled common-mode feedback circuit

PC CMFB enables a small-area fully-differential amplifier implemented in a low power/leakage CMOS technology.

3.3 Implementation of a Supply-scalable Amplifier with the PC CMFB

To demonstrate the concept of the pulse-controlled common-mode feedback circuit, a fully-differential supply-scalable amplifier with the CMFB in feedback was implemented as shown in Fig. 3.4. In the chosen configuration, the input and output common mode can be set independently to verity the CMFB circuit. The operation of the feedback amplifier is an integrator with a zero and has a 0dB gain at around 10MHz. The low-frequency gain of the integrator is limited by the DC gain of the amplifier which is around 40dB. The ideal transfer function is given by $-(1+s/\omega_z)/(s/\omega_p)$, where ω_z is 10.61MHz and ω_p is 7.96MHz.

To have the same frequency response of the integrator for supply voltages from 0.6V to 1.2V,

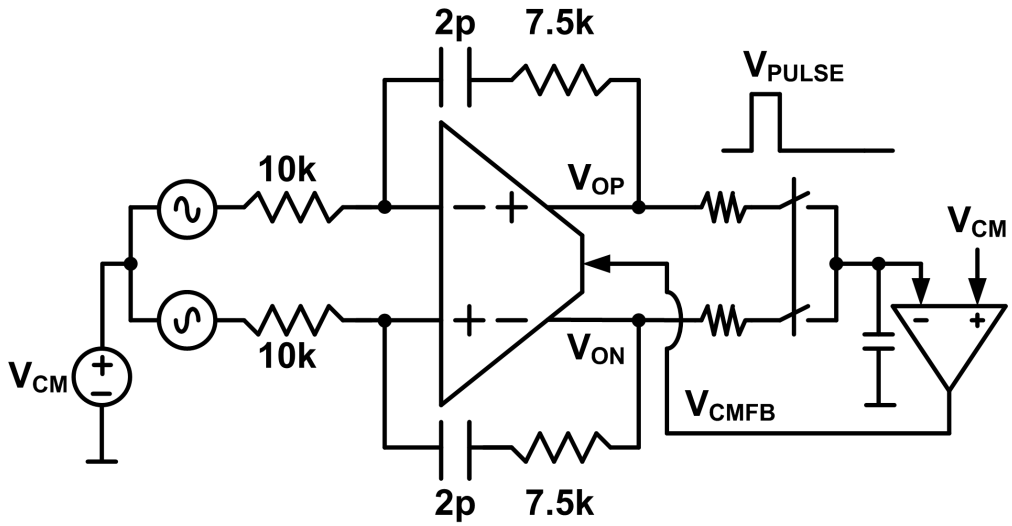


Figure 3.4: Fully differential amplifier with the proposed pulse-controlled common-mode feedback circuit in a feedback application

the gain and bandwidth of the amplifier and thus the transconductance are designed for small supply dependence. To achieve this, the changes in the gate-source voltage and bias current of transistors need to be kept small while scaling the supply voltage and common-mode voltage of the amplifier. Because the voltage at a high impedance node may not completely follow the supply change, the operating point of this node needs to be referred to a ground voltage independent of the supply voltage. For this reason, a two-stage OTA topology with an N-type second stage is selected (Fig. 3.5) since the NMOS gate voltage undergoes only minor changes when the supply voltage is changed. For the N-type output stage, a P-type input stage is used. Cascode transistors are avoided to facilitate operation down to a supply of 0.6V.

The detailed circuit of the differential amplifier with the pulse-controlled common-mode feedback circuit is shown in Fig. 3.5 and designed in a 65nm low power/leakage CMOS technology. While only changing the supply voltage and associated common-mode voltage, simulations show

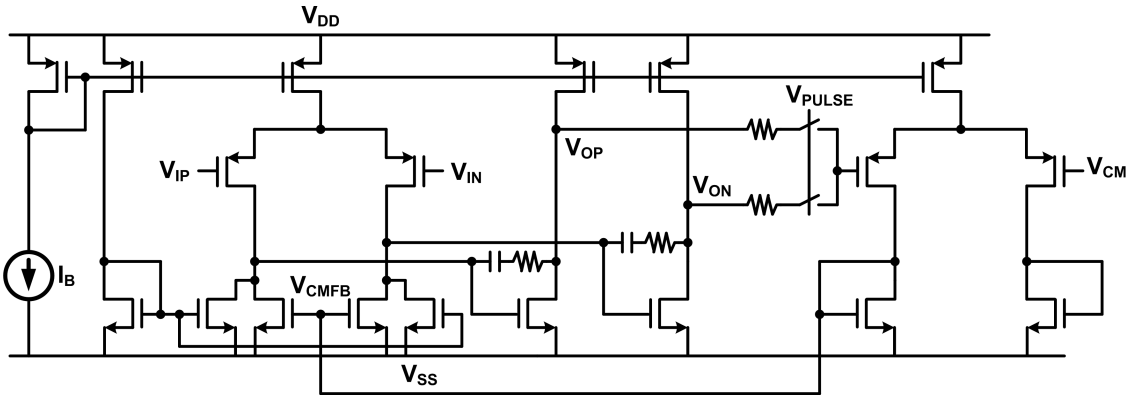


Figure 3.5: Circuit implementation of the supply scalable differential amplifier with the PC CMFB

that the unity-gain bandwidth of the amplifier is 674MHz at V_{DD}=0.6V, 906MHz at V_{DD}=0.9V and 1061MHz at V_{DD}=1.2V. The bandwidth variation is mainly caused by the variation of bias current for the supply voltage. After adjusting the bias current I_B of the amplifier, the unity-gain bandwidth is 1060MHz at V_{DD}=0.6V, 1059MHz at V_{DD}=0.9V and 1061MHz at V_{DD}=1.2V, which shows 0.2% variation for the supply change.

The pulse-controlled common-mode feedback circuit (Fig. 3.5) consists of the pulse-controlled resistance controlled by a pulse signal V_{PULSE} and a differential one-stage amplifier with an output signal V_{CMFB} to control the output common-mode voltage of the main amplifier. To track the common-mode voltage quickly, the period of the pulse signal is chosen as small as possible at the expense of more switching power. In addition, a too large pulse period results in a long off time for switches which may make the amplifier lose the common-mode feedback function. The width of the pulse signal relative to the period decides the value of pulse-controlled resistance, but it is limited by finite delay and rise/fall time of switches. In the presented implementation, the pulse period was chosen as 1ns and pulse width as 0.2ns; an equivalent resistance of 50kΩ is achieved by using a resistor of only 10kΩ. As a result, by using the PC CMFB, the area of the used resistors

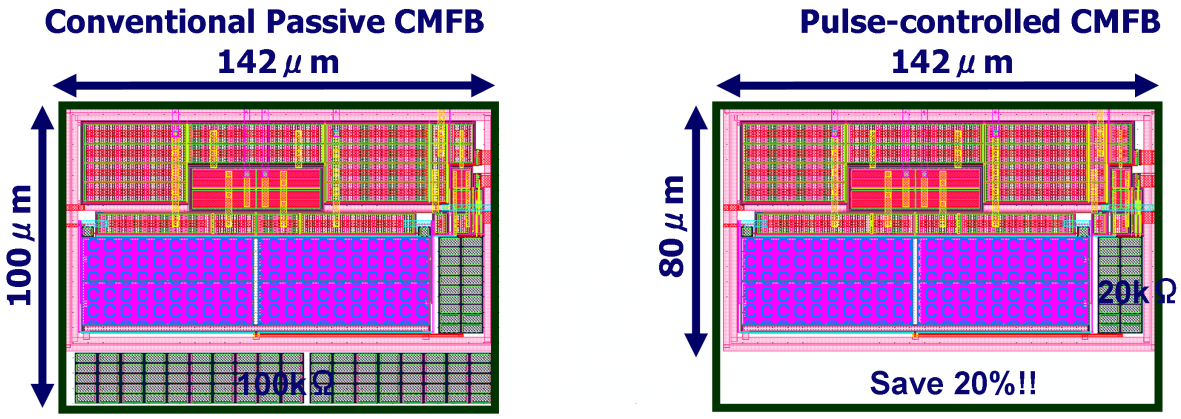


Figure 3.6: Layout comparison of the amplifier with RC CMFB and PC CMFB

Table 3.1: Simulation results

Supply Voltage		0.6V	0.9V	1.2V
Power	Total	1.21mW	1.94mW	3.07mW
	CMFB	0.04mW	0.09mW	0.16mW
UGB		674MHz	906MHz	1061MHz
Adjusted UGB		1060MHz	1059MHz	1061MHz

is reduced by 400% and the total area of the overall amplifier is reduced by 20% compared with using an RC CMFB. The layout of the amplifier with different CMFB is compared in Fig. 3.6 showing that the total area has been dominated by the core amplifier while using the PC CMFB. The simulated power consumption of the amplifier and its PC CMFB is 1.21mW and 0.04mW at V_{DD}=0.6V, 2.04mW and 0.09mW at V_{DD}=0.9V, and 2.99mW and 0.16mW at V_{DD}=1.2V. The simulation results are summarized in Table 3.1.

The stability of the PC CMFB is checked by giving a disturbance to the CMFB loop in the amplifier as Fig. 3.7. The disturbance in the form of a current pulse is injected into a high impedance node of the CMFB loop. The transient simulation measures the dynamics of the loop and shows that the CMFB loop can be recovered to the original state smoothly after injecting the impulse.

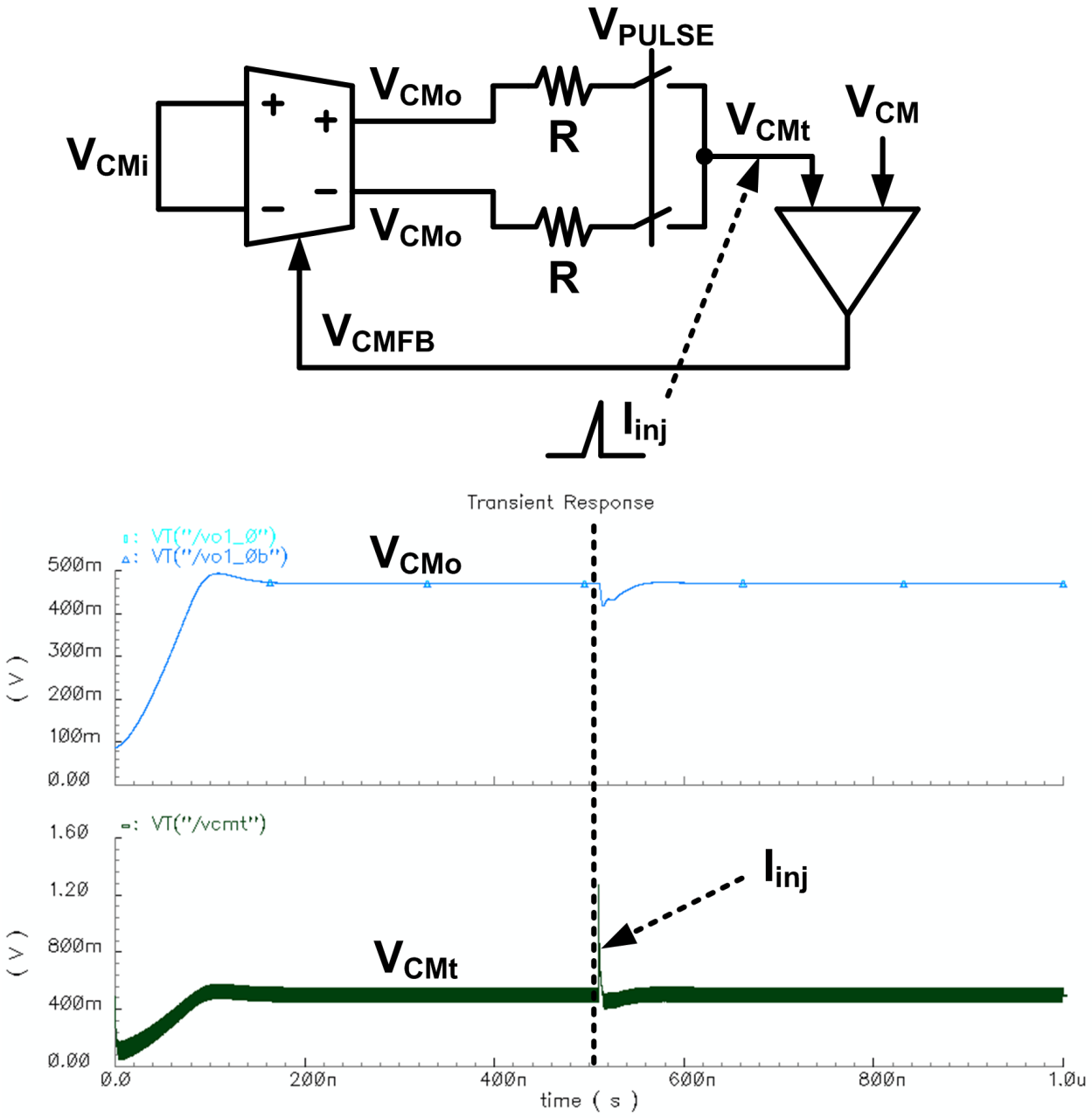


Figure 3.7: Simulation with injecting a large current impulse

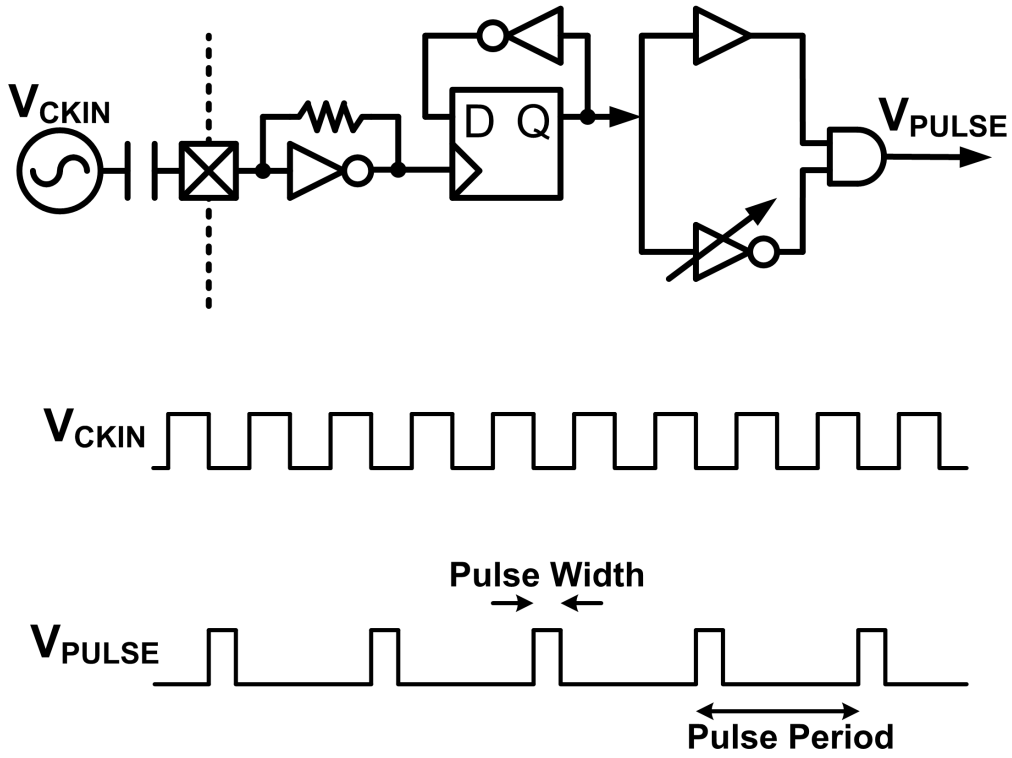
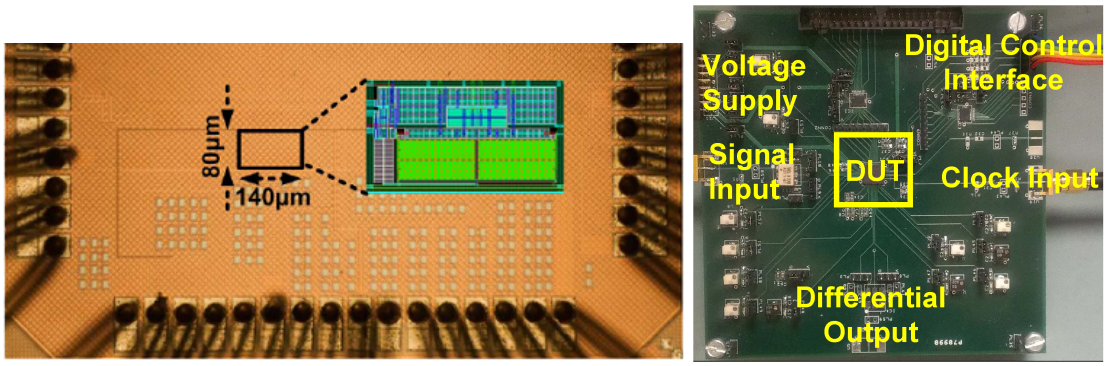


Figure 3.8: Schematic of the pulse timing generator for the PC CMFB

The pulse signal V_{PULSE} is generated by the pulse timing generator shown in Fig. 3.8. It consists of a clock buffer, a divide-by-2 divider and a programmable pulse-width circuit adjusting the pulse width by changing the delay between two inputs of an AND gate.

3.4 Experimental Results

The differential amplifier with PC CMFB was prototyped in a low power/leakage 65nm CMOS process with relatively large threshold voltages of 0.36V (NMOS) and -0.44V (PMOS). Fig. 3.9(a) shows the die photo of the differential amplifier with the PC CMFB with an active area of 0.01mm^2. The test bench of the differential amplifier is shown in Fig. 3.9(b) including a balun for the dif-



(a) (b)

Figure 3.9: (a) Die photo and layout inset of the differential amplifier with the PC CMFB (b) Measurement setup of the amplifier with the PC CMFB

ferential signal input and a 2GHz clock input for the PC CMFB. The power consumption of the amplifier with the PC CMFB is measured by 1.21mW at V_{DD}=0.6V, 1.94mW at V_{DD}=0.9V and 3.07mW at V_{DD}=1.2V matching the simulations.

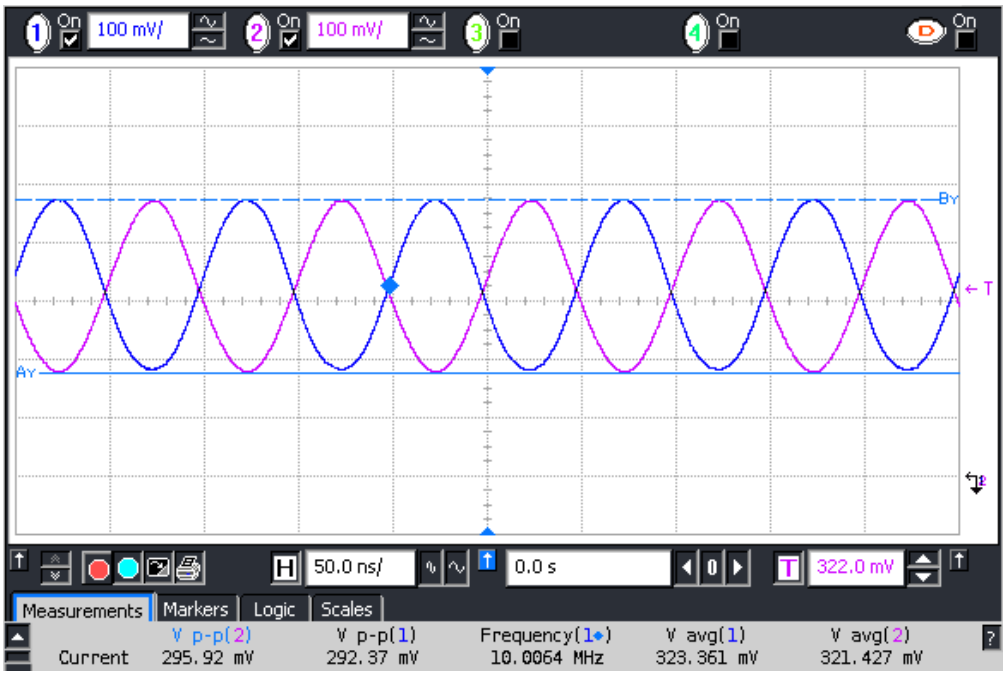


Figure 3.10: Measured time-domain waveform of the differential output of the amplifier with the PC CMFB at V_{DD}=0.6V

While applying a differential input signal with a frequency of 10MHz and swing of 600mVpp, the measured output waveform of the amplifier with the PC CMFB at V_{DD}=0.6V is shown in Fig. 3.10. The measured common-mode voltage of the differential outputs is close to a half of the supply voltage. By applying an external differential-to-single-ended buffer, the measured wide-band and inband output spectrum of the amplifier with the PC CMFB is shown in Fig. 3.11. The output spectrum of the amplifier shows no significant tones caused by the PC CMFB. Given the input with the frequency of 10MHz and power of 0dBm, the amplifier at V_{DD}=0.6V has a SFDR of -45.46dBc.

By varying the reference common-mode voltage with the above differential input to the amplifier, the measured output common-mode voltage with respect to the input common-mode voltage for the supplies of 0.6V, 0.9V and 1.2V is shown in Fig. 3.12. The measurement shows the linear common-mode signal range of 0.3V, 0.6V and 1.0V for the supply voltage of 0.6V, 0.9V and 1.2V respectively. The ideal and measured frequency response of the feedback implemented by the amplifier is shown in Fig. 3.13. The measured frequency response at different supplies is close to the ideal one showing that the amplifier with the PC CMFB is able to operate from 0.6V to 1.2V. The measured output noise power spectrum density of the amplifier with the PC CMFB between 10MHz and 100MHz is 21.5nV/$\sqrt{\text{Hz}}$ at V_{DD}=0.6V, 26.1nV/$\sqrt{\text{Hz}}$ at V_{DD}=0.9V and 30.3nV/$\sqrt{\text{Hz}}$ at V_{DD}=1.2V showing the similar noise performance over supplies. According to the change of the noise performance, the input transconductance of the amplifier increases by about 3dB by doubling the supply voltage matching the change of the unity-gain bandwidth in the simulations. The

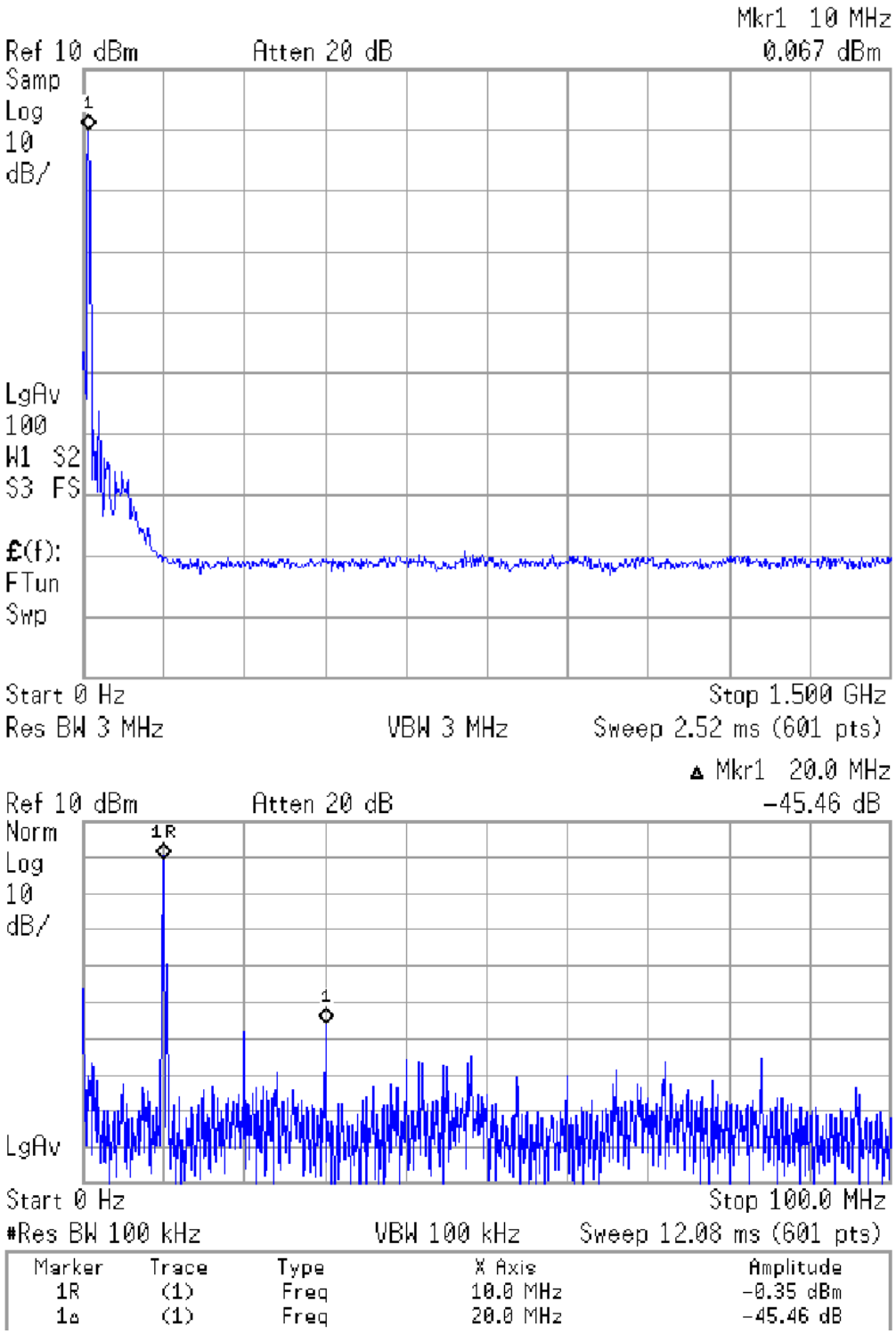


Figure 3.11: Measured wideband output spectrum (top) of the amplifier with a 10MHz, 0dBm input and its inband output spectrum from 0 to 100MHz (bottom)

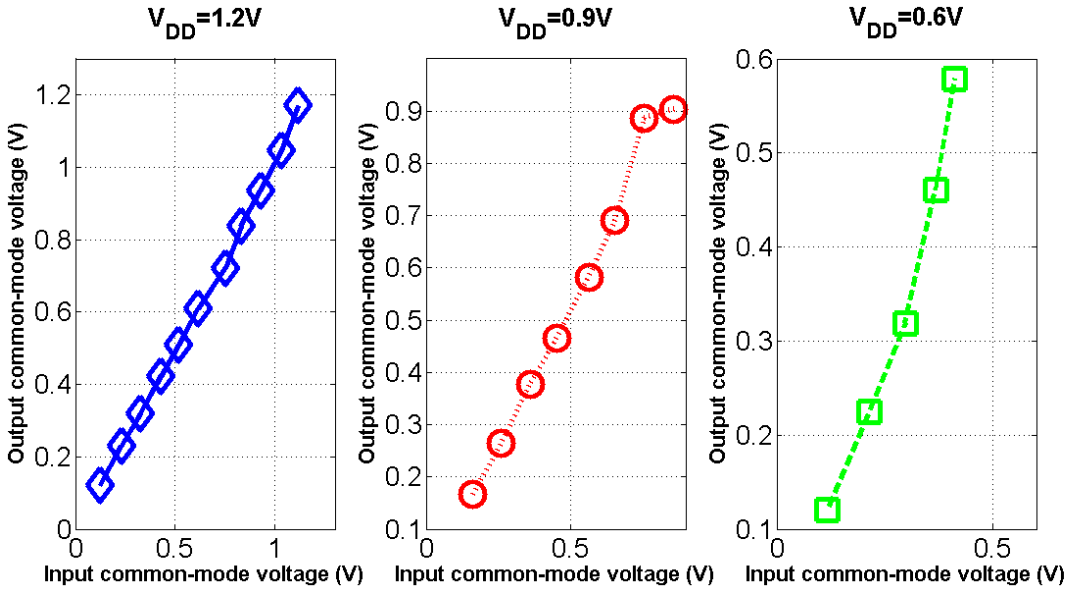


Figure 3.12: Measured output common-mode voltage of the amplifier with the PC CMFB while varying the common-mode reference and operating at different supplies from 0.6V to 1.2V

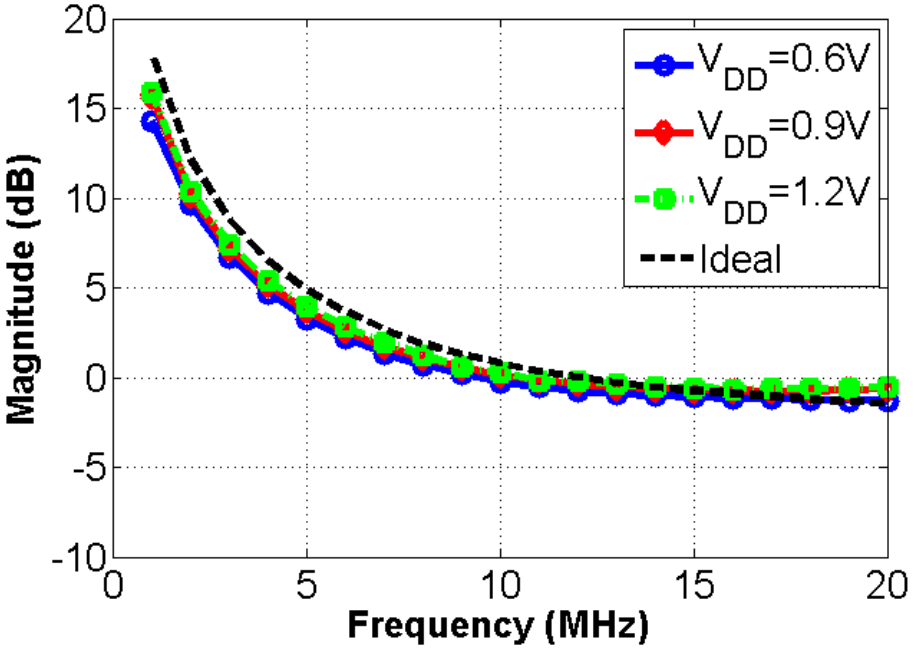


Figure 3.13: Comparison between the ideal transfer function and the measured frequency response of the feedback amplifier for different supplies

Table 3.2: Performance summary

Technology	65nm CMOS		
V_{THN}/V_{THP}	0.36V/-0.44V		
Active Area	0.01mm^2		
Supply Voltage	0.6V	0.9V	1.2V
Common-mode Voltage	0.3V	0.45V	0.6V
Power Consumption	1.21mW	1.94mW	3.07mW
Output Noise PSD	21.5nV/$\sqrt{\text{Hz}}$	26.1nV/$\sqrt{\text{Hz}}$	30.3nV/$\sqrt{\text{Hz}}$
Maximum Input Signal for 1% THD	-2.3dBm	3.8dBm	6.1dBm

transconductance is larger at a higher supply voltage because the bias current is increased by the larger drain to source voltage.

The linearity of the amplifier with the PC CMFB is measured by sweeping its input signal power for the total harmonic distortion (THD) of 1%. With the input frequency of 10MHz, the maximum input power of the amplifier for 1% THD is given by -2.3dBm at V_{DD}=0.6V, 3.8dBm at V_{DD}=0.9V and 6.1dBm at V_{DD}=1.2V. The linearity of the amplifier is poorer at a low supply because of its smaller signal headroom associated with the supply voltage. Given the fixed V_{dsat} $\approx$120mV, the linearity of the amplifier depends on the signal headroom with the supply scaling of (V_{DD}-2V_{dsat}). The performance of the amplifier with the PC CMFB is summarized in Table 3.2 demonstrating that the amplifier with the PC CMFB in a low power/leakage CMOS technology has a small area and suitable for flexible supply operation.

3.5 Conclusions

This work proposes a 0.6V-1.2V fully-differential amplifier with pulse-controlled common-mode feedback circuit realized in a low power/leakage 65nm CMOS technology. The pulse-controlled common-mode feedback circuit results in a fully-differential amplifier with large output swing but less area cost than conventional common-mode feedback circuits. When the supply is changed from 0.6V to 1.2V, the measured frequency response changes are small and the measured output noise spectrum density only changes from 21.5nV/$\sqrt{\text{Hz}}$ to 30.3nV/$\sqrt{\text{Hz}}$ demonstrating the flexible supply operation of the differential amplifier with the PC CMFB.

Chapter 4

Effects of Supply Scaling on the Performance of Continuous-Time Delta-Sigma Modulators

The dependence of the performance of a continuous-time delta-sigma modulator (DSM) on its supply voltage is analyzed. The performance and the benchmark figure of merit (FoM) mainly depend on the power dissipation, and the thermal noise contributions from the analog loop filter, and the quantization noise from the quantizers. Theoretical estimates for the supply dependence of loop noise and quantization noise and their respective FoM are derived and verified with simulations for a 2MHz third-order continuous-time DSM, while operating from a supply between 0.6V to 1.2V in a low power/leakage CMOS process. At a larger supply voltage, the FoM related to the loop filter noise improves; whereas at lower supplies, the FoM related to the quantization noise improves.

As a result, the overall FoM of the DSM reaches an optimum at a particular supply. The supply voltage with the best FoM of the DSM is derived with the supply-scaling FoM of the loop filter and quantizers. For the equal FoM of the loop filter and quantizers at a supply $V_{DD,0}$, the optimal supply voltage is $0.66V_{DD,0}$.

4.1 Introduction

Supply-scalable circuits are now becoming popular, since they are suitable for unstable supplies and help extend the usage time of self-powered wearable devices such as pressure sensors, temperature sensors and motion sensors, in which the generated power strongly depends on external excitation and has large variation [23] [33]. The supply dependence of Nyquist-rate ADCs or quantizers was studied by voltage-scalable SAR ADCs [25] and zero-crossing-based pipelined ADCs [24]. However, the supply-scaling performance of a continuous-time delta-sigma modulator (CT DSM) widely used in communication systems is still under discussion because the DSM consists of a loop filter and quantizers which have different supply dependence. The loop filter is formed by analog amplifiers which suffer from smaller signal swing and headroom, while its supply voltage is lower; the quantizer is a digital-like circuit which has the benefit of reducing operating (dynamic) power and current leakage at a lower supply. It is thus important to understand the effects of power supply scaling on the performance of the CT DSM.

In this work, theoretical models have been derived to predict the scaling of the loop filter and quantizers of a CT DSM with the supply voltage. Using these models, a projection is made for the supply scaling of the performance and its figure of merit (FoM) of the CT DSM. The supply

voltage for the best FoM of the overall modulator is derived with the supply dependence of the loop filter and quantizers. The theoretical models are verified by circuit simulations of a third-order CT DSM with scalable supplies from 0.6V to 1.2V for WCDMA baseband applications. The CT DSM is implemented in a low power/leakage CMOS technology with transistors having large threshold voltages. Amplifiers of the modulator are designed for the same bandwidth and gain at different supplies because poor supply-dependent amplifiers may easily make the DSM unstable or directly downgrade the dynamic range by changing the noise transfer function of the modulator. In addition, during supply scaling, the on-resistance of analog switches has large variation which limits the signal swing and bandwidth [24] of the modulator.

This chapter is organized as follows: section 4.2 briefly reviews the performance contributors of a CT DSM; section 4.3 discusses the supply scaling of the performance of the DSM; section 4.4 describes the implementation of the CT DSM with the flexible supply operation; and finally, section 4.5 presents the simulated results of the supply-scalable DSM.

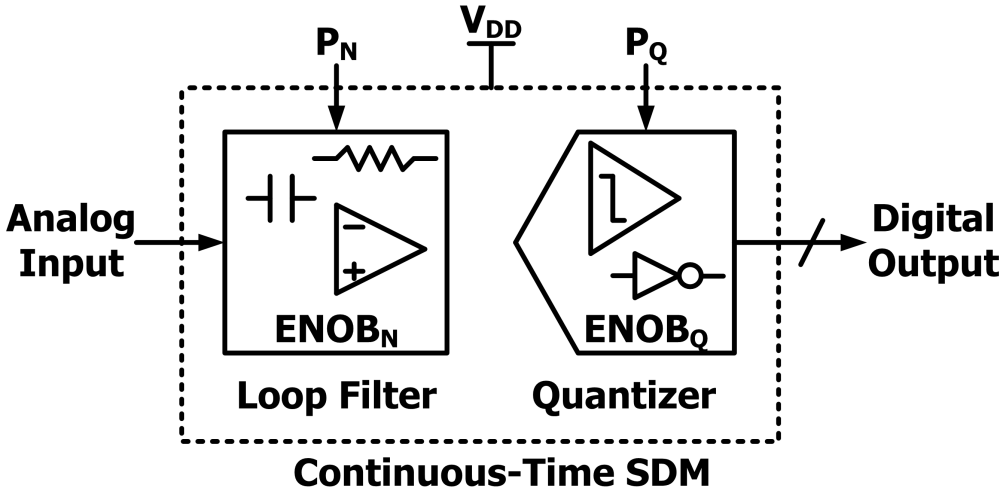


Figure 4.1: Noise contributions to a continuous-time delta-sigma modulator

4.2 Performance-Setting Elements in a Continuous-time Delta-sigma Modulator

A CT DSM consists of an analog loop filter and quantizers as shown in Fig. 4.1. The loop filter has the power consumption of P_{N} and noise performance in terms of the effective number of bits of $ENOB_{\mathrm{N}}$ or $SNR = S^2/N^2 \approx 2^{2ENOB_{\mathrm{N}}}$; the flash-type quantizers have P_{Q} and signal-to-quantization ratio to the overall DSM represented by $ENOB_{\mathrm{Q}}$ or $SQR = S^2/Q^2 \approx 2^{2ENOB_{\mathrm{Q}}}$ which depends on its bit number, modulator's order and oversampling ratio. The noise performance of the overall DSM contributed by loop noise and quantization noise can be expressed by: $SQNR = S^2/(N^2 + Q^2) \approx 1/(2^{-2ENOB_{\mathrm{N}}} + 2^{-2ENOB_{\mathrm{Q}}})$. Because of different relationship between noise performance and power, the figure of merit (FoM) of the loop filter and quantizers can be respectively defined as [34]:

$$\mathrm{FoM_N} = \frac{P_{\mathrm{N}}}{2 \cdot BW \cdot 2^{2ENOB_{\mathrm{N}}}}; \mathrm{FoM_Q} = \frac{P_{\mathrm{Q}}}{2 \cdot BW \cdot 2^{ENOB_{\mathrm{Q}}}}$$

where BW is desired signal bandwidth.

The dynamic range of a CT DSM is usually limited by circuit noise, so the figure of merit $\mathrm{FoM_{SDM}}$ of the overall DSM can be defined by:

$$\begin{aligned} \mathrm{FoM_{SDM}} &= \frac{(P_{\mathrm{Q}} + P_{\mathrm{N}})}{2 \cdot BW \cdot SQNR} = \frac{(P_{\mathrm{Q}} + P_{\mathrm{N}})}{2 \cdot BW} \cdot \left(\frac{1}{2^{2ENOB_{\mathrm{Q}}}} + \frac{1}{2^{2ENOB_{\mathrm{N}}}} \right) \\ &= (1+k)\,\mathrm{FoM_Q}* + \left(1 + \frac{1}{k}\right) \mathrm{FoM_N} \end{aligned}$$

where $k = P_{\mathrm{N}}/P_{\mathrm{Q}}$ is the power ratio of the loop filter and quantizers and $\mathrm{FoM_{Q}}* = \mathrm{FoM_{Q}}/2^{\mathrm{ENOB_{Q}}}$.

Assume $\mathrm{FoM_{N}}$ and $\mathrm{FoM_{Q}}$ are kept the same while considering the trade-off between power consumption and noise performance of the loop filter and quantizers. Given signal bandwidth BW, $\mathrm{FoM_{N}}$ and $\mathrm{FoM_{Q}}*$, the power ratio k_{opt} for the minimum $\mathrm{FoM_{SDM}}$ depends on the FoM of the loop filter and quantizers and can be derived as:

$$k_{opt} = \sqrt{\frac{\mathrm{FoM_{N}}}{\mathrm{FoM_{Q}}*}} = \sqrt{\frac{P_{\mathrm{N}}2^{2ENOB_{\mathrm{Q}}}}{P_{\mathrm{Q}}2^{2ENOB_{\mathrm{N}}}}} \tag{4.1}$$

Moreover, to get the optimal $\mathrm{FoM_{SDM}}$ of a CT DSM, the noise performance ratio of the loop filter and quantizers needs to be equal to the inverse of their power ratio i.e.

$$SQR/SNR = 2^{2ENOB_{\mathrm{Q}}}/2^{2ENOB_{\mathrm{N}}} = P_{\mathrm{N}}/P_{\mathrm{Q}}$$

where SNR is decided by the required overall noise performance of the CT DSM and then P_{N} is contributed by corresponding loop amplifiers. Therefore, for optimizing the figure of merit of a CT DSM, SQR according to the quantization noise needs to be set 10dB higher than SNR if P_{N} is ten times larger than P_{Q}.

A multi-bit topology becomes popular to relax the design requirements of the loop filter in a CT DSM because it can achieve the same dynamic range by using a low-order loop filter and a low oversampling ratio. The low oversampling ratio reduces the clock rate and then the required unity-gain bandwidth of the loop amplifiers [35]. While increasing the bits of the quantizers of the DSM, P_{Q} increases and then P_{N} decreases for a required overall power budget. Therefore, the

SQR needs to be chosen close to *SNR* for the multi-bit CT DSM with the optimal $\mathrm{FoM_{SDM}}$. If the loop filter and quantizers have the same power, the optimal multi-bit CT DSM with has equal noise contribution from the loop filter and quantizers.

4.3 Models for the Supply Scaling of CT DSM Performance

The supply-scaling effects on the quantization noise, loop noise and the overall performance of the DSM respectively are discussed by using a scaling factor of α representing that the supply voltage is changed from $V_{\mathrm{DD,0}}$ to $\alpha V_{\mathrm{DD,0}}$. At $V_{\mathrm{DD,0}}$, the quantizers have $P_{\mathrm{Q,0}}$, $ENOB_{\mathrm{Q,0}}$ and $\mathrm{FoM_{Q,0}}$; the loop filter has $P_{\mathrm{N,0}}$, $ENOB_{\mathrm{N,0}}$ and $\mathrm{FoM_{N,0}}$.

It is worth mentioning that the signal transfer function and the noise transfer function of the DSM are assumed to be independent of the supply voltage during the supply-scaling operation. While scaling the supply voltage, the maximum input signal swing is also scaled to optimize the dynamic range of the DSM. Given BW, the dependence of the overall energy-per-conversion of the DSM on the supply voltage can be discussed by its different supply-dependent error sources. One is quantization noise from quantizers with $P_{\mathrm{Q},\alpha}$, $ENOB_{\mathrm{Q},\alpha}$ and $\mathrm{FoM_{Q,\alpha}}$; the other is circuit noise of the loop filter with $P_{\mathrm{N},\alpha}$, $ENOB_{\mathrm{N},\alpha}$ and $\mathrm{FoM_{N,\alpha}}$.

4.3.1 Dependence of the Quantization Noise on the Supply Voltage

Assume that the noise performance of the quantizer is only dominated by quantization noise rather than other error sources such as device noise or comparator offset. The performance of the quantizers evaluated by $2^{ENOB_{\mathrm{Q},\alpha}}$ is constant over supply scaling since quantization noise scales with

the supply voltage. The power consumption of the quantizers $P_{\mathrm{Q},\alpha}$ is proportional to α^2 because the current consumption of the quantizers depends on the supply voltage. The impact of the supply voltage on the figure of merit to evaluate the energy per conversion of the quantizers can be expressed by:

$$\mathrm{FoM}_{\mathrm{Q},\alpha} = \frac{(\alpha^2 P_{\mathrm{Q},0})}{2 \cdot BW \cdot 2^{ENOB_{\mathrm{Q},0}}} = \alpha^2 \mathrm{FoM}_{\mathrm{Q},0} \tag{4.2}$$

Thus, the figure of merit of the quantizers is better for a lower supply voltage, but poor for a higher supply voltage.

4.3.2 Dependence of the Loop Filter Noise on the Supply Voltage

The noise performance of the loop filter at $\alpha V_{\mathrm{DD},0}$ is defined by $2^{2ENOB_{\mathrm{N},\alpha}}$ and proportional to α^2 because circuit noise is constant, but the signal swing is scaled by the supply. It is assumed that the loop filter is a current-limited circuit i.e. its bias current is constant over supply changing. The power consumption of the loop filter, $P_{\mathrm{N},\alpha}$, is proportional to α. Due to the supply-dependent noise performance and power consumption, the supply scaling of FoM of the loop filter can be shown as:

$$\mathrm{FoM}_{\mathrm{N},\alpha} = \frac{(\alpha P_{\mathrm{N},0})}{2 \cdot BW \cdot (\alpha^2 2^{2ENOB_{\mathrm{N},0}})} = \frac{1}{\alpha} \mathrm{FoM}_{\mathrm{N},0} \tag{4.3}$$

In summary, the loop filter has better FoM at a higher supply, but is poorer at a lower supply.

From the supply scaling of $\mathrm{FoM}_{\mathrm{Q},\alpha}$ and $\mathrm{FoM}_{\mathrm{N},\alpha}$, the supply-scaling FoM of the overall DSM

in terms of α which is a trade-off between FoM of the loop filter and quantizers can be expressed by:

$$\mathrm{FoM}_{\mathrm{SDM},\alpha} = \frac{\mathrm{FoM}_{\mathrm{Q},\alpha}}{2^{ENOB_{\mathrm{Q},0}}}\left(1+\frac{k_0}{\alpha}\right)+\mathrm{FoM}_{\mathrm{N},\alpha}\left(1+\frac{\alpha}{k_0}\right) \tag{4.4}$$

where $k_0 = P_{\mathrm{N},0}/P_{\mathrm{Q},0}$ is the power ratio of the loop filter to quantizers at the supply voltage $V_{\mathrm{DD},0}$. From Eq. (4.1), $k_0 = \sqrt{\mathrm{FoM}_{\mathrm{N},0}/\mathrm{FoM}_{\mathrm{Q}*,0}}$ and is constant to the supply voltage.

Because $\mathrm{FoM}_{\mathrm{N}},\alpha$ is better at a higher supply, but $\mathrm{FoM}_{\mathrm{Q}},\alpha$ is better at a lower supply, there is an optimal supply to minimize the overall energy per conversion of the DSM. The optimal supply-scaling factor for the best $\mathrm{FoM}_{\mathrm{SDM},\alpha}$ is derived as:

$$\begin{aligned}\alpha_{opt} &= \frac{-k_0}{6}+\sqrt[3]{\frac{k_0^2}{4}-\frac{k_0^3}{216}+\frac{k_0^2}{4}\sqrt{1-\frac{k_0}{27}}} \\ &+ \sqrt[3]{\frac{k_0^2}{4}-\frac{k_0^3}{216}-\frac{k_0^2}{4}\sqrt{1-\frac{k_0}{27}}}\end{aligned} \tag{4.5}$$

The optimal supply-scaling factor depends on the power ratio of the loop filter to quantizers at $V_{\mathrm{DD},0}$. For the same power of the loop filter and quantizers at $V_{\mathrm{DD},0}$ i.e. $k_0 = 1$, the supply voltage giving the best FoM of the delta-sigma modulator is $0.66V_{\mathrm{DD},0}$.

Based on the different supply dependence of the loop filter, quantizers and the overall DSM, their supply-scaling models are summarized in Fig. 4.2. While increasing the supply voltage, $ENOB_{\mathrm{Q}}$ is not changed, but $ENOB_{\mathrm{N}}$ increases. P_{Q} and P_{N} both are increased by the increased supply voltage. While the supply voltage goes down, $\mathrm{FoM}_{\mathrm{N}}$ to the loop noise becomes worse, but $\mathrm{FoM}_{\mathrm{Q}}$ to the quantization noise is better. The supply voltage that gives the best FoM of the overall

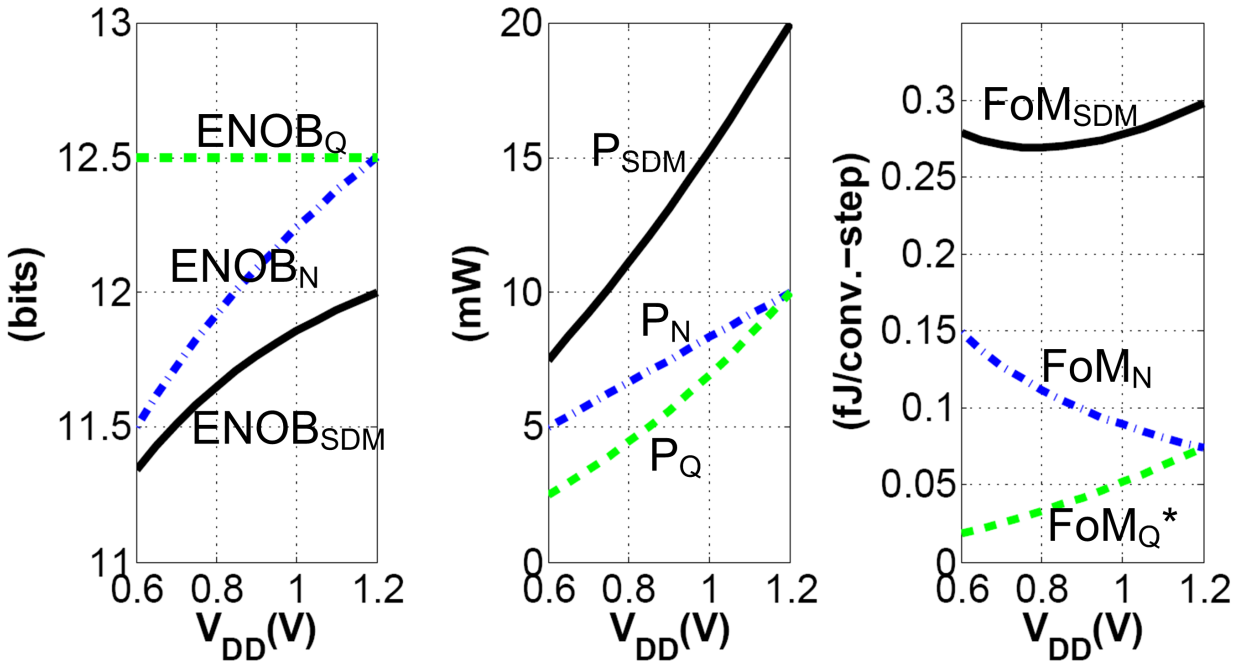


Figure 4.2: Supply-scaling performance models of the loop filter, quantizers and overall DSM ($\text{FoM}_{\text{Q}}* = \text{FoM}_{\text{Q}}/2^{\text{ENOB}_{\text{Q}}}$)

DSM is decided by the supply-scaling FoM of the loop filter and quantizers. Given the same FoM of the loop filter and quantizers at 1.2V, the best FoM of the overall DSM is at 0.8V.

4.4 Design Example of a Supply-Scalable Continuous-time Delta-sigma Modulator

To demonstrate the supply-scaling concepts, a continuous-time delta-sigma modulator with the signal bandwidth of 2MHz is simulated in a low power/leakage CMOS 65nm process. In the simulations, the signal level and common-mode voltage of the loop filter, the reference voltage of quantizers are set proportional to the supply voltage. For the target dynamic range of around 70dB,

a third-order four-bit DSM with an oversampling ratio of 25 is chosen to make quantization noise below circuit noise over the supply change. A cascaded 2-1 topology is chosen for the third-order DSM because it allows more aggressive loop coefficients and fewer stability issues while changing the supply voltage.

Fig. 4.3 shows the architecture of the CT DSM with flexible supply operation. The input-feedforward structure using a multi-input quantizer [36] for a CT DSM is used to reduce the internal signal swing without the need for a critical summing amplifier. The linearity of the CT DSM is improved by the absence of the summing amplifier and the small internal signal swing since the input of the loop filter only contains quantization noise, but not a large signal input. However, the

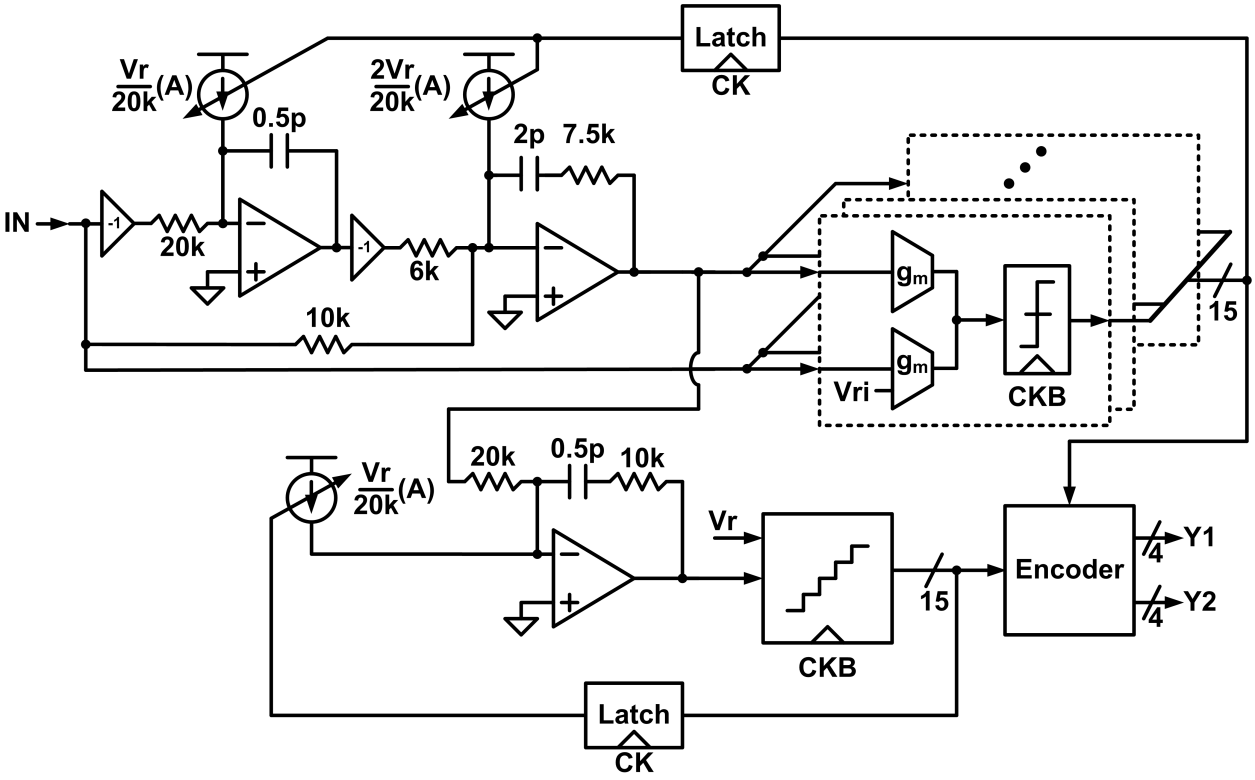


Figure 4.3: Architecture of the supply-scalable continuous-time delta-sigma modulator

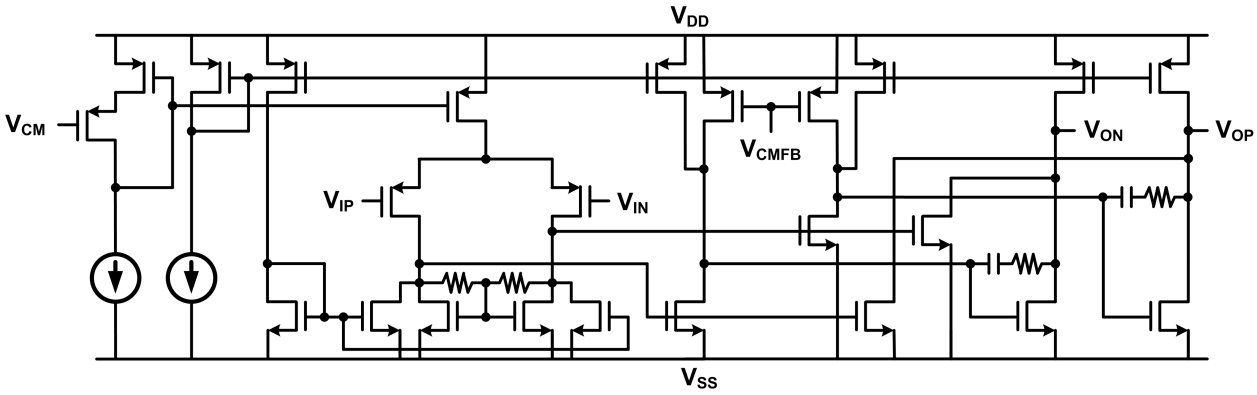


Figure 4.4: Schematic of the first amplifier of the loop filter

small internal signal may not be kept while an extra feedback path is added to fix the problem of excess loop delay in wide-band CT DSMs. Thus, this work uses the distributed feedforward and feedback structure with a multi-input quantizer to solve excess delay problem and keep small internal swing at the same time. The transfer function of the CT DSM is derived by applying bilinear z-transform to the transfer function of a standard discrete-time modulator with a fixed sampling delay of $z^{-1/2}$ for excess loop delay and the zero-order-hold delay by the quantizers.

The amplifiers of the supply-scalable DSM are designed for the same gain and bandwidth over the supply change to maintain the similar noise transfer function of the modulator. Three-stage architecture with feed-forward compensation shown in Fig. 4.4 is designed as the first amplifier to meet the tight requirement of a large DC gain at low voltage operation. The feed-forward compensation is chosen to cancel one of the poles of the three stages while the doublet and slow settling is not a big concern in this work. While only changing the supply voltage, simulations show that the unity-gain bandwidth of the amplifier is 364MHz at V_{DD}=0.6V, 289MHz at V_{DD}=0.9V and 286MHz at V_{DD}=1.2V. The simulated Bode plot of the amplifier is shown in Fig. 4.5 for the supply from 0.6V to 1.2V with the step of 0.15V. After adjusting the bias current of the amplifier, the unity-

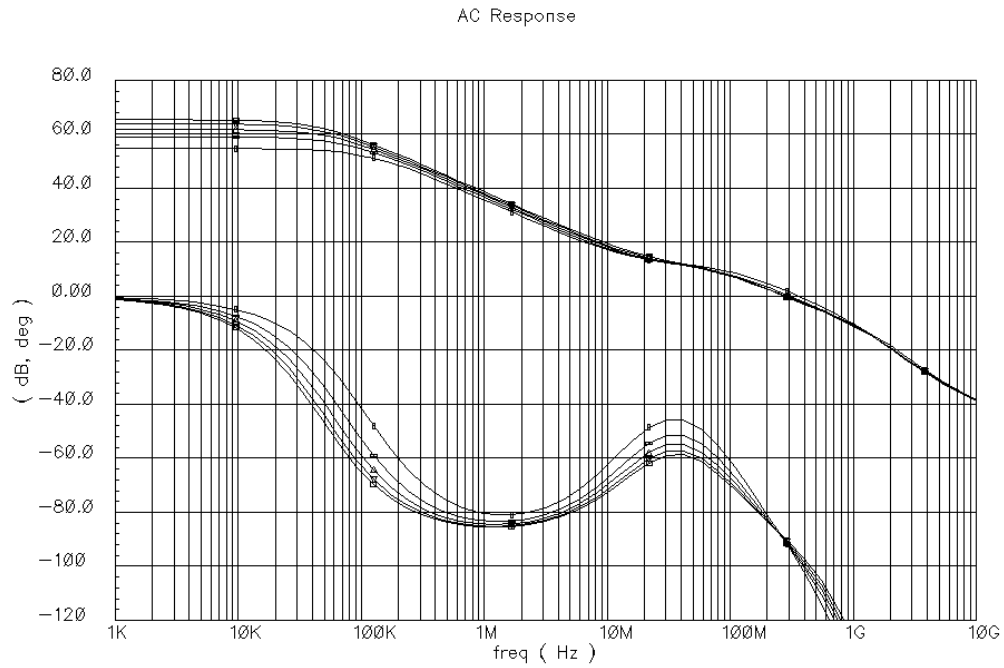


Figure 4.5: Simulated Bode plot of the first amplifier for supplies of 0.6V, 0.75V, 0.9V, 1.05V and 1.2V

gain bandwidth is 364MHz at V_{DD}=0.6V, 364.9MHz at V_{DD}=0.9V and 365.3MHz at V_{DD}=1.2V, which shows 0.4% variation for the supply change. Because the dc gain requirement is relaxed for other loop amplifiers, two-stage amplifiers are used to save the area and power consumption. While only changing the supply voltage, simulations show that the unity-gain bandwidth of the amplifier is 674MHz at V_{DD}=0.6V, 906MHz at V_{DD}=0.9V and 1061MHz at V_{DD}=1.2V. After adjusting the bias current of the amplifier, the unity-gain bandwidth is 1060MHz at V_{DD}=0.6V, 1059MHz at V_{DD}=0.9V and 1061MHz at V_{DD}=1.2V, which shows 0.2% variation.

The first multi-input quantizer of the DSM is implemented by a 4-bit flash type with two-input comparators as Fig. 4.6. The two inputs of the comparator are the difference between $Vi1$ and reference voltage $Vref$, and $Vi2$ where $Vi1$ is the loop filter's input with larger signal swing and $Vi2$ is the loop filter's output with small quantization noise. The differential output of the

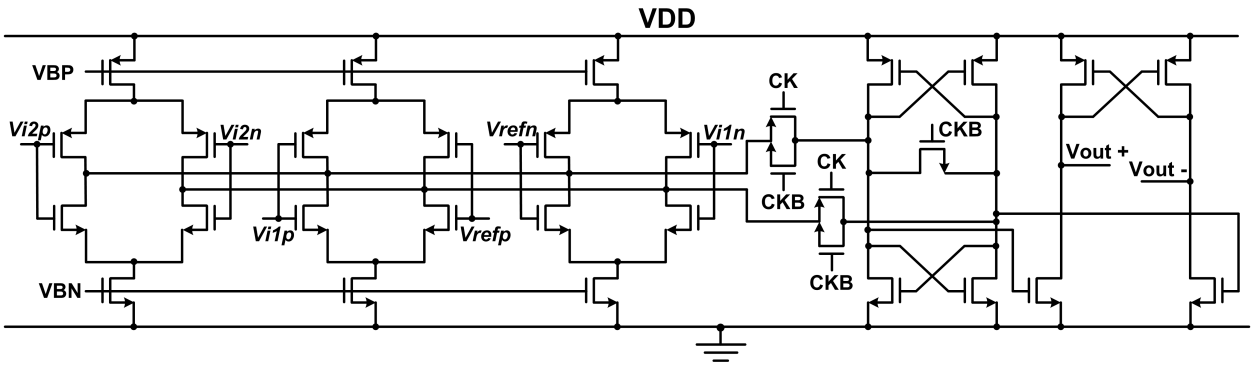


Figure 4.6: Circuit of the two-input comparator used for the first quantizer

comparator is the sum of the inputs and can be expressed by:

$$G[(V\mathrm{i2p}-V\mathrm{i2n})+(V\mathrm{i1p}-V\mathrm{refp})+(V\mathrm{refn}-V\mathrm{i1n})]$$

$$=G[(V\mathrm{i1p}-V\mathrm{i1n})-(V\mathrm{refp}-V\mathrm{refn})+(V\mathrm{i2p}-V\mathrm{i2n})]$$

where G is the gain of the comparator. The comparator consists of three differential transconductors, a regenerative latch and a SR latch. The transistors of the transconductors are properly sized to reduce comparator offset due to mismatch. For the clock rate of 100MHz and the input frequency of 1.95MHz, the simulation of the quantizer shows that the signal-to-quantization ratio is 25.8dB at V_{DD}=0.6V and 25.7dB at V_{DD}=1.2V. The FoM of the quantizer is 0.96pJ/conv.-step at V_{DD}=0.6V and 3.84pJ/conv.-step at V_{DD}=1.2V which matches the supply-scaling model of a quantizer. The quantizer used in the second stage has the same structure as the first one, but is formed by one-input comparators.

The fifteen comparators' outputs of the quantizer are fed to an encoder for 4-bit binary output. The comparator's output is also connected to the latch of a sub-DAC [37] shown as Fig. 4.7. The

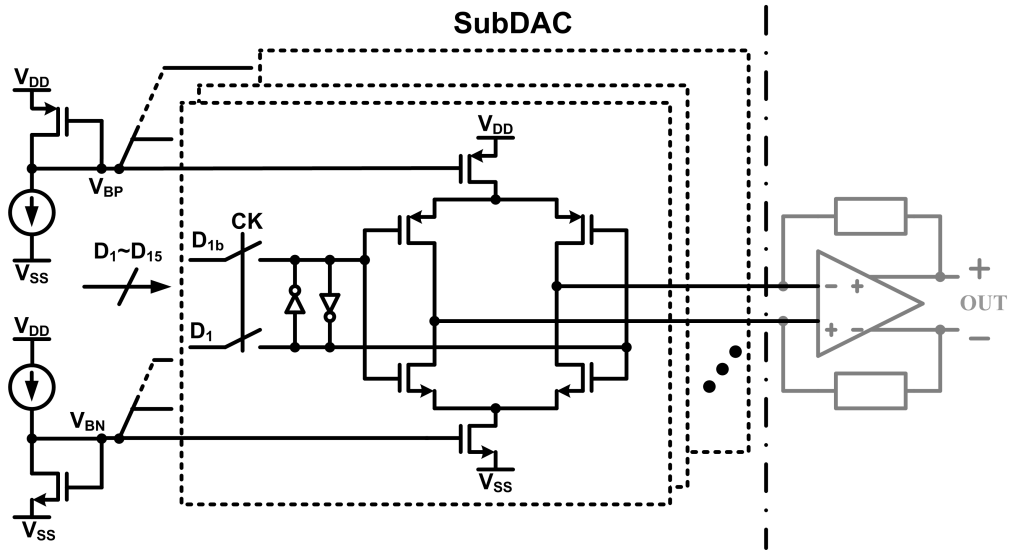


Figure 4.7: Sub-DAC realization using fifteen current-steering cells

sub-DAC operates in a current mode rather than a voltage mode to avoid the need for low switches' on-resistance. Otherwise, it may need extra bootstrap circuits or low-V_T devices for getting the low on-resistance of switches [25].

4.5 Simulation Results of the Supply-Scalable Continuous-time Delta-sigma Modulator

Fig. 4.8 shows the layout of the DSM implemented in a 65nm digital low power/leakage CMOS technology with an active area of 0.2mm^2. To clarify the different contributions from the loop filter and quantizers to the cascaded 2-1 CT DSM, a simulation at different supplies was done with a DSM implemented by a transistor-level loop filter and behavioral sample-and-hold circuits used to replace quantizers. Moreover, the DSM simulation with transient noise only calculated

Figure 4.8: Layout of the cascaded 2-1 CT DSM

loop noise, but no quantization noise. With the input frequency of 1MHz and signal bandwidth of 2MHz, the noise performance of the DSM with flexible supply operation was simulated by the signal-to-noise ratio equal to 73.7dB at V_{DD}=0.6V, 77.6dB at V_{DD}=0.9V and 80.6dB at V_{DD}=1.2V. It is noted that the modulator only including the transistor-level loop filter was expected to have better noise performance than the DSM with complete transistor-level circuits because sub-DACs' noise also contributed to the overall noise performance. The power consumption of the DSM only considering loop filter was simulated by 4.40mW at V_{DD}=0.6V, 7.37mW at V_{DD}=0.9V and 10.69mW at V_{DD}=1.2V. For changing the supply voltage, there was good correspondence between the analytical models and the transistor-level simulation of the prototype shown in Fig. 4.9. A higher supply voltage gave better FoM contributed by loop noise, but a lower supply voltage made the FoM poorer.

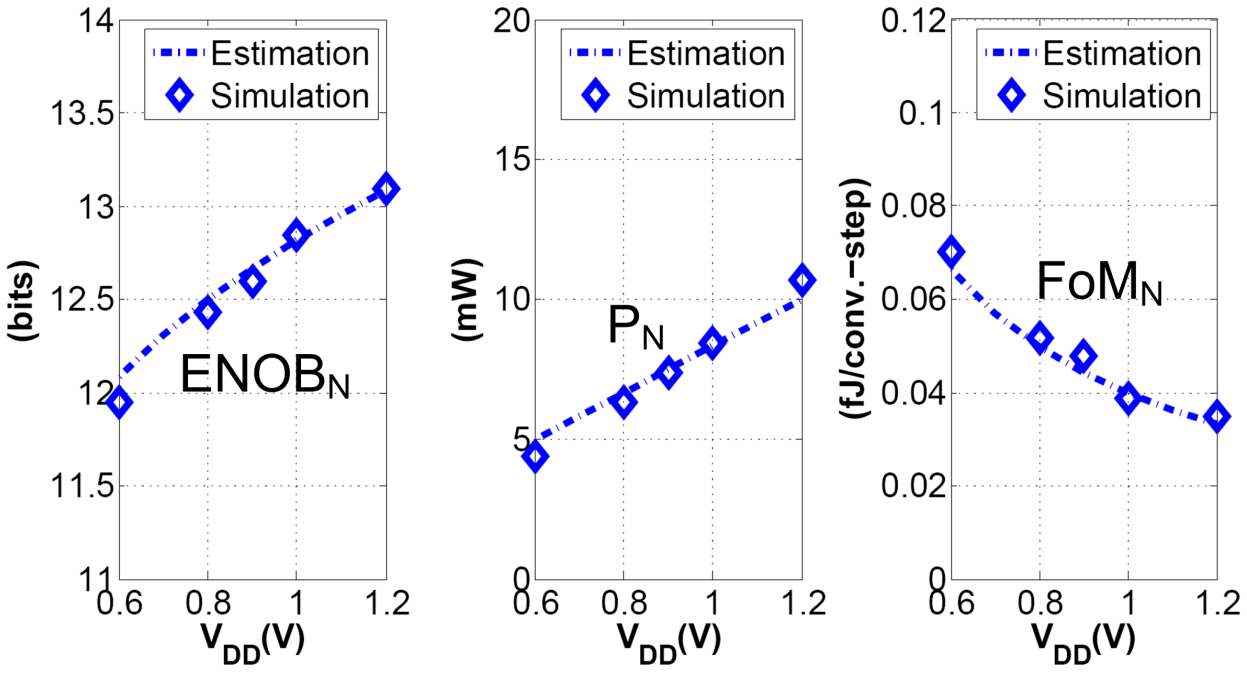


Figure 4.9: Comparison between the simulation and analytical models of the DSM with a transistor-level loop filter and behavioral sample-and-hold circuits while sweeping the supply voltage

The overall performance of the CT DSM was simulated by the complete transistor-level circuits with transient noise. This simulation used the input frequency of 1MHz, the signal bandwidth of 2MHz and the sampling frequency of 100MHz. The performance of the DSM, which was expressed by SQNR (signal to quantization noise and noise ratio), was 69.7dB at V_{DD}=0.6V, 71.8dB at V_{DD}=0.8V, 72.4dB at V_{DD}=0.9V, 73.0dB at V_{DD}=1.0V and 73.9dB at V_{DD}=1.2V. The power consumption of the overall DSM consisting of the loop filter and quantizers was 6.96mW at V_{DD}=0.6V, 11mW at V_{DD}=0.8V, 13.22mW at V_{DD}=0.9V, 15.64mW at V_{DD}=1.0V and 21.3mW at V_{DD}=1.2V. By sweeping the supply voltage, Fig. 4.10 shows the simulated results matching the estimation of the supply-scaling models and the optimal supply voltage giving the best FoM of 0.272 fJ/conv.-step between 0.7V and 0.8V.

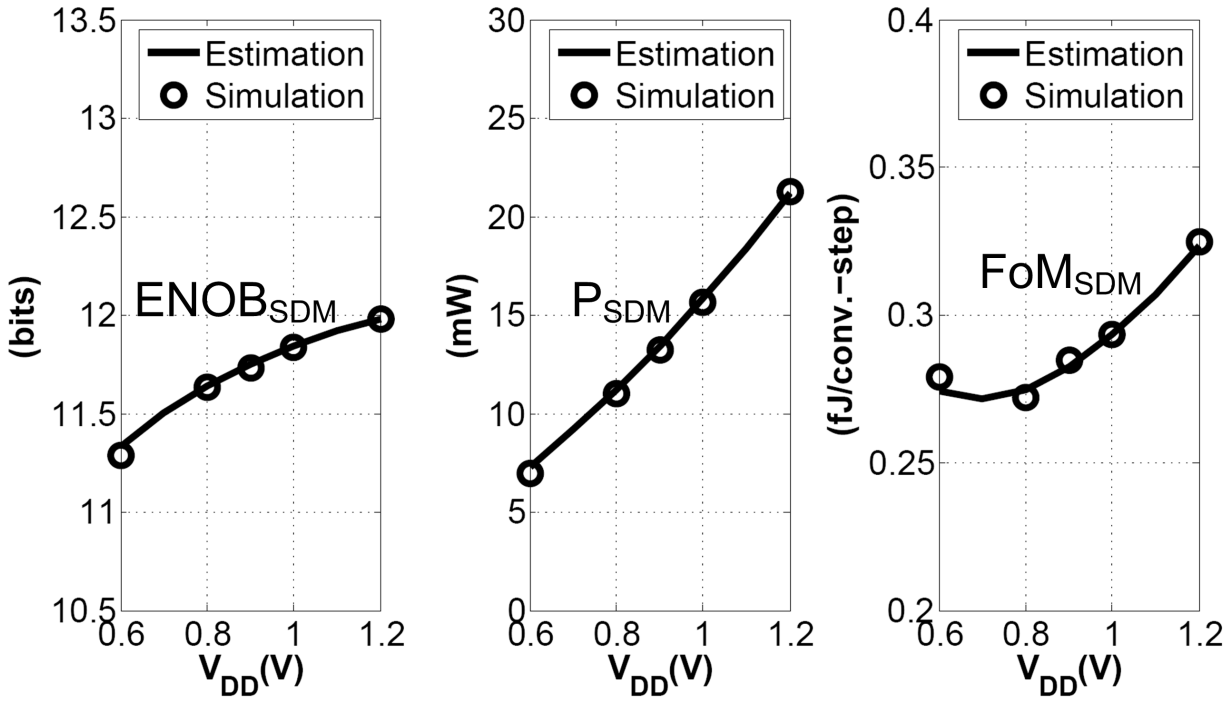


Figure 4.10: Simulated and estimated performance of complete transistor-level CT DSM as a function of the supply voltage

The summary and comparison of the ADC performance is listed in Table 4.1. Compared to other sub-1V sigma-delta ADCs and supply-scalable ADCs, this work shows better performance in terms of the area and FoM.

4.6 Conclusions

In this work, theoretical models of the supply-scaling loop noise and quantization noise of a CT DSM were analyzed and verified by circuit simulations. While the supply voltage went down, the FoM of the loop filter became worse, but the FoM of the quantizers was better. In contrast, by increasing the supply voltage, the FoM by the loop noise became better, but the FoM by the

Table 4.1: Performance comparison table

	[38]	[39]	[27]		This Work		
ADC Type	CT DSM	CT DSM	Pipelined		CT DSM		
CMOS Technology	0.18μm	0.13μm	0.13μm		65nm		
V_{THN}/V_{THP}	0.5V/-0.5V	0.22V/-0.25V	-/-		0.36V/-0.44V		
Active Area	0.6mm^2	0.9mm^2	0.98mm^2		0.2mm^2		
Supply Voltage	0.5V	0.5V	0.5V	1.2V	0.6V	0.8V	1.2V
Signal Bandwidth	25kHz	1MHz	5MHz	30MHz	2MHz		
Input Range (Vppdiff)	1.0	1.0	0.8		0.68	0.91	1.36
Power (mW)	0.3	3.4	3.0	45.6	6.96	11.0	21.3
Dynamic Range (dB)	74	61.9	52.9	53.3	69.7	71.8	73.9
FoM (fJ/conv.-step)	0.358	1.644	2.305	3.195	0.279	0.272	0.325

$$\text{FoM} = \frac{\text{Power}}{2 \cdot \text{BW} \cdot 2^{2(\text{DR}-1.76)/6.02}}$$

quantization noise was worse. The supply voltage that gave the best FoM of the DSM was decided by the supply-scaling FoM of the loop filter and quantizers. A CT DSM with its supply from 0.6V to 1.2V for WCDMA applications was simulated in a 65nm CMOS low power/leakage process to demonstrate the concepts of the supply-scaling models. The simulations showed a good match to the derived models for a supply change and the best FoM in sub-1V sigma-delta ADCs and supply-scalable ADCs.

Chapter 5

A 40MHz 4th-order Active-UGB-RC Filter using VCO-Based Amplifiers with Zero Compensation

This work describes a 4th-order active-UGB-RC filter using VCO-based amplifiers with zero compensation. The VCO-based amplifier intrinsically has a huge DC gain without the associated stability penalties of conventional multi-stage amplifiers such as reducing unity-gain bandwidth or requiring a large area by compensation schemes. By using the large gain of the amplifier, the filter achieves a small area and good linearity performance for a signal bandwidth of 40MHz. The filter prototype in a 55nm CMOS process has an active area of 0.07mm^2, and a power consumption of 7.8mW at 1.2V. The measured in-band IIP3 and out-of-band IIP3 are 27.3dBm and 22.5dBm, respectively.

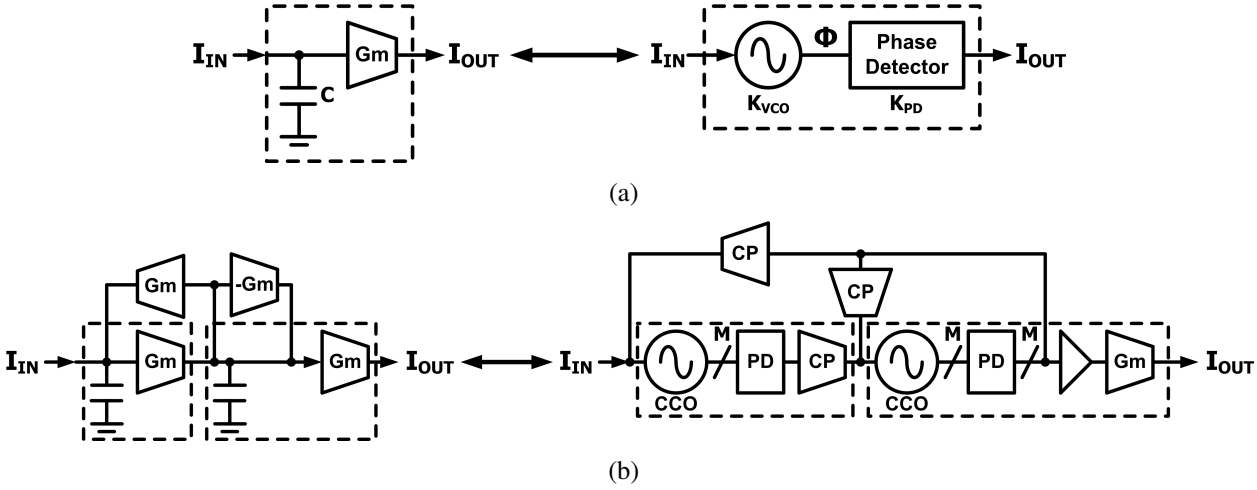


Figure 5.1: Comparisons of a continuous-time filter using the Gm-C type and ring-oscillator-based structure by taking the examples of (a) an integrator and (b) a biquad

5.1 Introduction

With the advancement of CMOS technologies, designers have been facing more and more challenges to design a wide-band and high-gain operational amplifier. Nano-scale short-channel devices have smaller output impedance and operate with lower supply voltages, forcing the use of a multi-stage topology (e.g. three or more) for a high-gain amplifier. However, more stages entail more poles which lead to stability difficulties and require a reduction in unity-gain bandwidth (UGB) or more power dissipation or areas. For the realization of continuous-time filters, a ring-oscillator-phase-detector combination has been used to realize a phase-domain integrator [40], eliminating the need for amplifiers or transconductors and capacitors. Fig. 5.1 shows the comparison between Gm-C filters and the ring-oscillator-based filters by using the examples of an integrator and a biquad. By keeping voltage/current input and output, the signal operation of the ring-oscillator-based circuits is changed from voltage/current domain to phase domain by using a VCO/CCO and a phase detector. The VCO has its output phase proportional to the time integral of

the applied input voltage/current signal which can then be viewed as an ideal CT integrator. However, there are some limitations for ring-oscillator-based integrators. First, the ring-oscillator-based integrators remove the need for capacitors, which is good for continuous-time signal operation; but it cannot be used for discrete-time signal operation because this needs a capacitor to store static signal power. In addition, the linearity of the ring-oscillator-based integrator is limited by the non-linear voltage-to-frequency conversion, which operates in an open loop. Filters with ring-oscillator-based integrators are also more power-hungry than active-UGB-RC filters [41], where the required number of amplifiers is cut in half for a given filter order by choosing the unity-gain bandwidth of amplifiers comparable to filter cut-off frequency.

Generally, ring-oscillators have not yet been used to substitute for amplifiers in analog circuits like switched-capacitor circuits, or continuous-time analog front-end circuits. A VCO-based amplifier with zero compensation is proposed to replace conventional operational amplifiers. The VCO-based amplifier intrinsically has a very large DC gain without any of the stability penalties associated with the large DC gain in conventional multi-stage amplifiers. Section 5.2 discusses the concept of the VCO-based amplifier. Section 5.3 describes the implementation of a continuous-time active-UGB-RC filter using VCO-based amplifiers and Section 5.4 presents the measurement results.

5.2 A VCO-based Amplifier with Zero Compensation

Fig. 5.2 shows the concept of a previous VCO-based amplifier proposed in [42]. Different from the ring-oscillator-based integrator, the VCO-based amplifier operates in a closed loop and be-

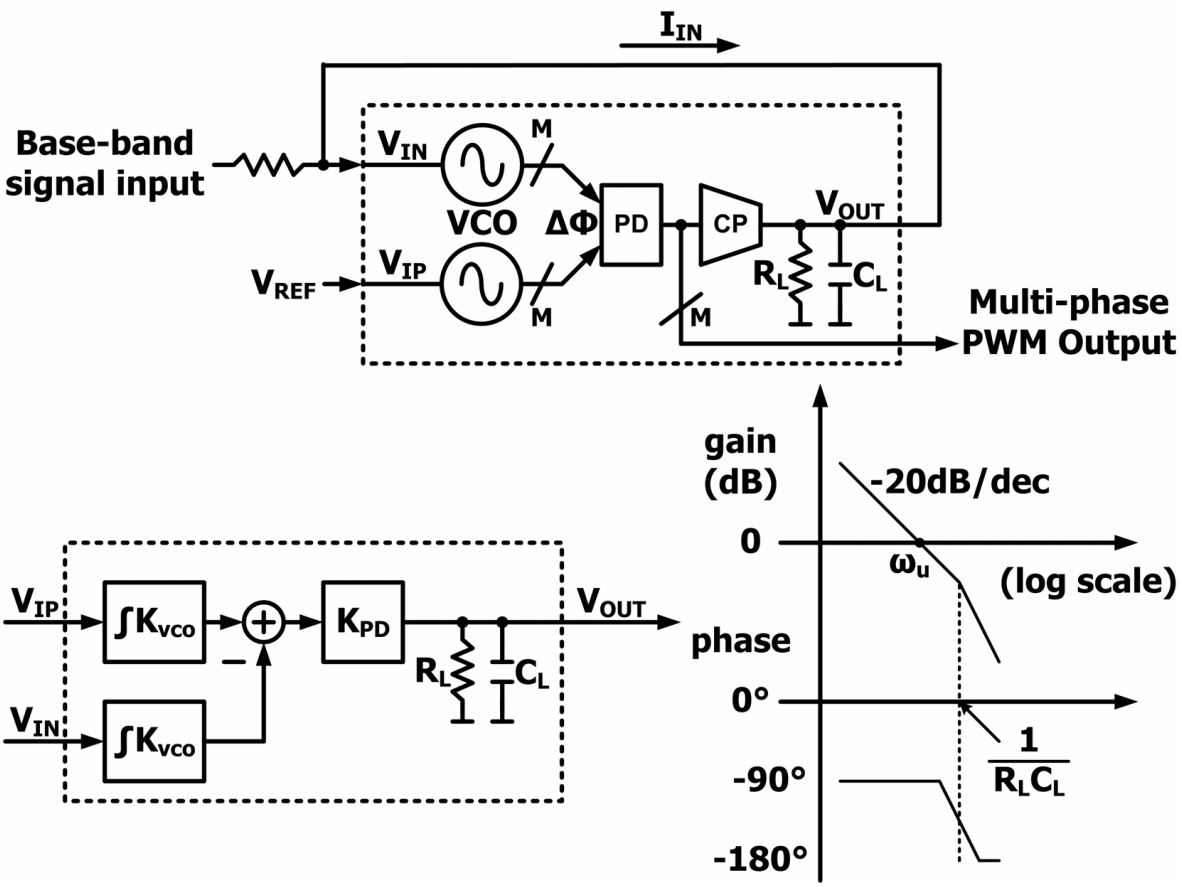


Figure 5.2: Earlier proposed VCO-based amplifier [42] whose use is limited to RF modulator applications

haves as an ideal amplifier with infinite gain and bandwidth so that its input can be virtual-ground. In addition, sub-blocks' gains of the ring-oscillator-based integrator are part of a desired overall transfer function, but this is not the case for the VCO-based amplifier. However, the use of the VCO-based amplifier has been limited to provide a PWM output for an RF modulator, since this amplifier cannot drive any large output load, given that the resulting output pole is below the unity-gain bandwidth and causes stability problems. In fact, if only driving a small load such as 100Ω in parallel with 50fF, the VCO-based amplifier can easily achieve the low-frequency gain of 200dB at

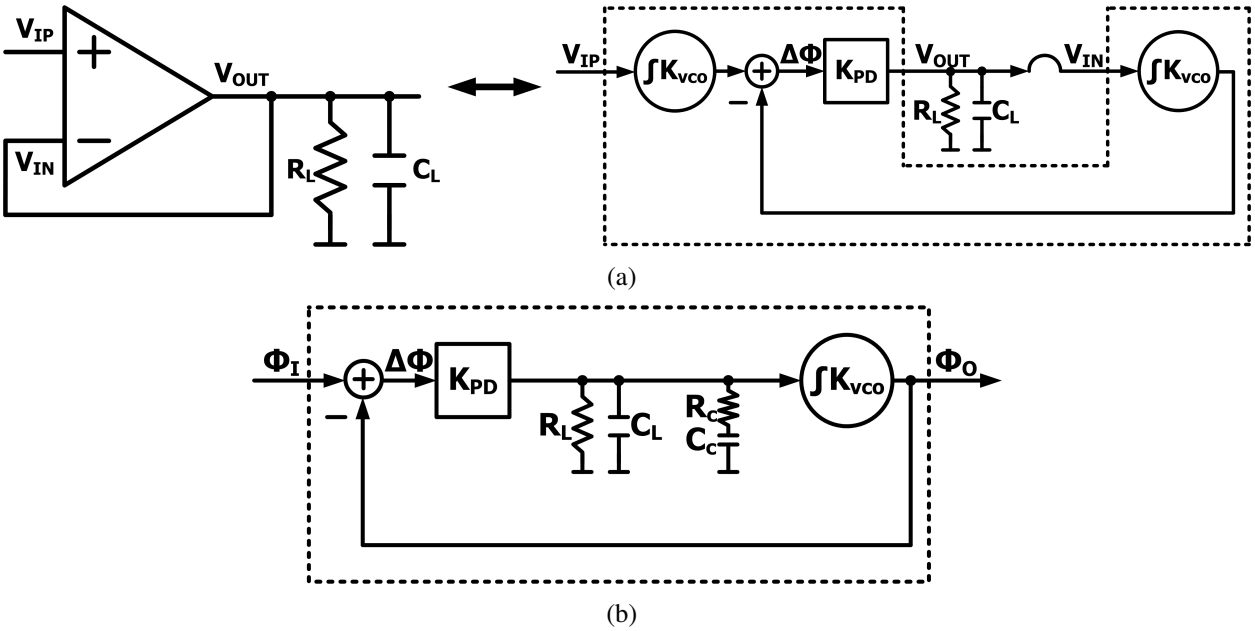


Figure 5.3: (a) A unity-gain buffer using the prior VCO-based amplifier (b) The phase domain model of a type-II 3rd order PLL with the divisor equal to one

1Hz, and the unity-gain bandwidth of 10GHz with the phase margin being larger than 70 degrees in its Bode plot simulation.

Taking an example of a unity-gain buffer implemented by the VCO-based amplifier, Fig. 5.3(a) shows an unstable loop because there are two poles below the UGB of the amplifier. To overcome this limitation, a VCO-based differential amplifier with zero compensation is proposed for general-purpose applications and can be used as a replacement for conventional operational amplifiers. The VCO-based amplifier with zero compensation has an infinite DC gain in open loop, due to the voltage-to-phase integration operation in the VCO. When applied in a unity feedback configuration, the amplifier operates similarly to a type-II 3rd-order phase-locked loop with a feedback divisor equal to the one which is shown in Fig. 5.3(b).

The comparison of the phase domain model and Bode plot for the prior VCO-based amplifier

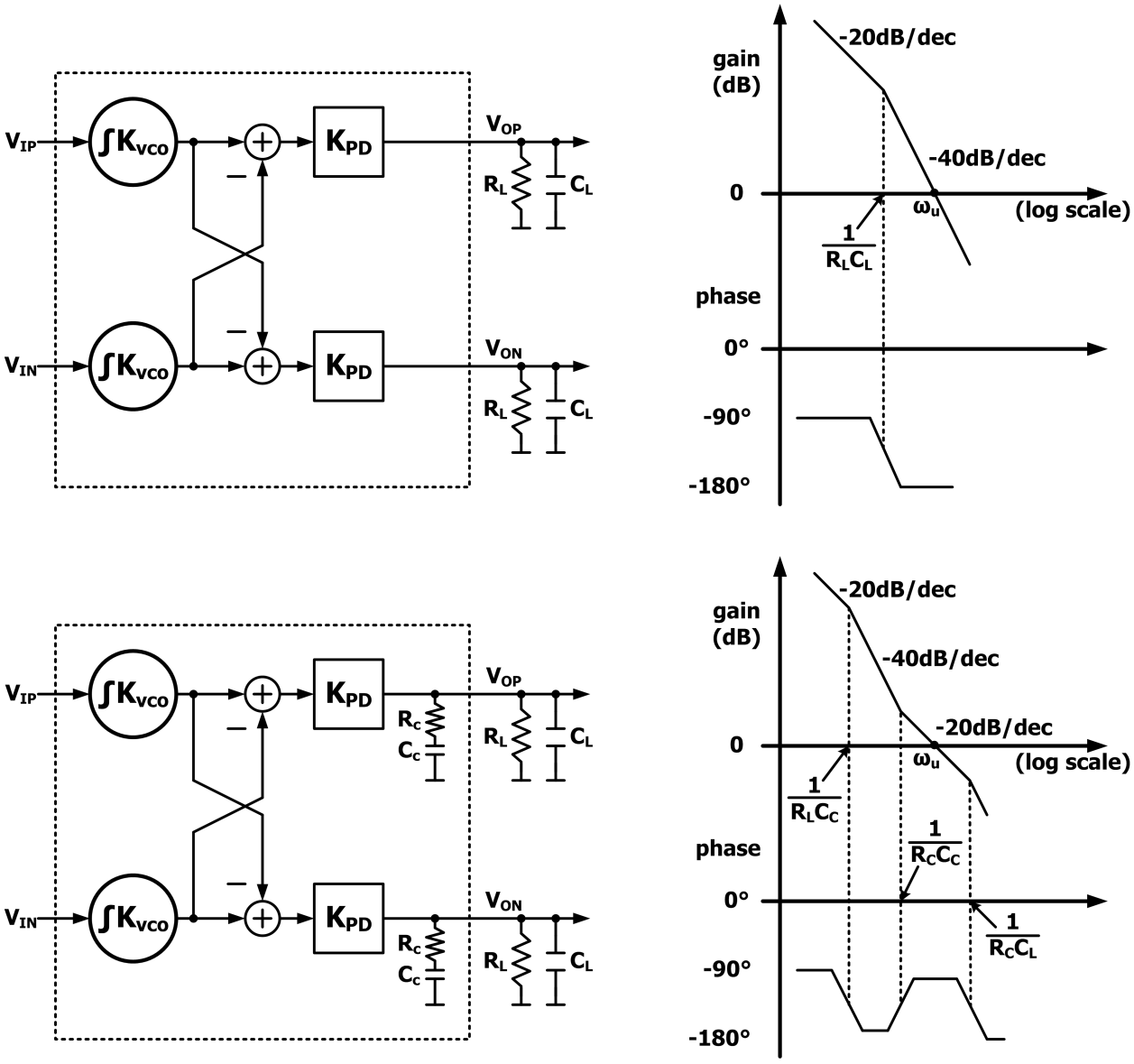


Figure 5.4: The comparison of prior VCO-based amplifier and the proposed VCO-based amplifier with zero compensation

and the proposed VCO-based differential amplifier with zero compensation is shown in Fig. 5.4. Without the compensation, the Bode plot of the VCO-based amplifier has a zero phase margin, while its output pole is much smaller than its UGB. But, after applying the zero compensation, which is inspired by the PLL design, a zero is inserted below the UGB so that the phase margin is improved and the loop using the VCO-based amplifier becomes stable. The zero is created by a series R_C-C_C at the output to compensate the output pole due to R_L and C_L. The value of R_C is chosen smaller than R_L and C_C is chosen larger than C_L. With the chosen R_C and C_C, the open-loop transfer function H(s) is:

$$H(s) = \frac{4\pi K_{VCO} K_{PD}(1+s/\omega_z)R_L}{s(1+s/\omega_{p2})(1+s/\omega_{p3})} \sim \frac{4\pi K_{VCO} K_{PD}(1+s/\omega_z)}{s^2 C_C(1+s/\omega_{p3})}$$

where $\omega_{p2} = 1/(R_L C_C)$, $\omega_{p3} = 1/(R_C C_L)$, and $\omega_z = 1/(R_C C_C)$. There are two low-frequency poles, one at DC, and one at $1/(R_L C_C)$; a zero at $1/(R_C C_C)$ and a third pole at $1/(R_C C_L)$ in the frequency response. The amplifier has a sufficient phase margin if its unity-gain frequency ω_u falls between the zero and the third pole. ω_u is approximately $4\pi K_{VCO} K_{PD} R_C$ if it is indeed sufficiently smaller than the third pole and sufficiently larger than the zero. With the zero compensation, the VCO-based amplifier is capable to drive a desired output load with the infinite DC gain, but without the stability problems related with its unity-gain bandwidth.

As a design example of the VCO-based amplifier with zero compensation, the gain K_{VCO} of the VCO is chosen by 4GHz/V; K_{PD} of the phase detector is set by 0.18mA/radin. The compensated zero consists of the resistor $R_C = 150\Omega$ and the capacitor $C_C = 7$pF. When driving an output load of 1pF//5kΩ, the simulated results of the VCO-based amplifier in Fig. 5.5 shows its DC gain of

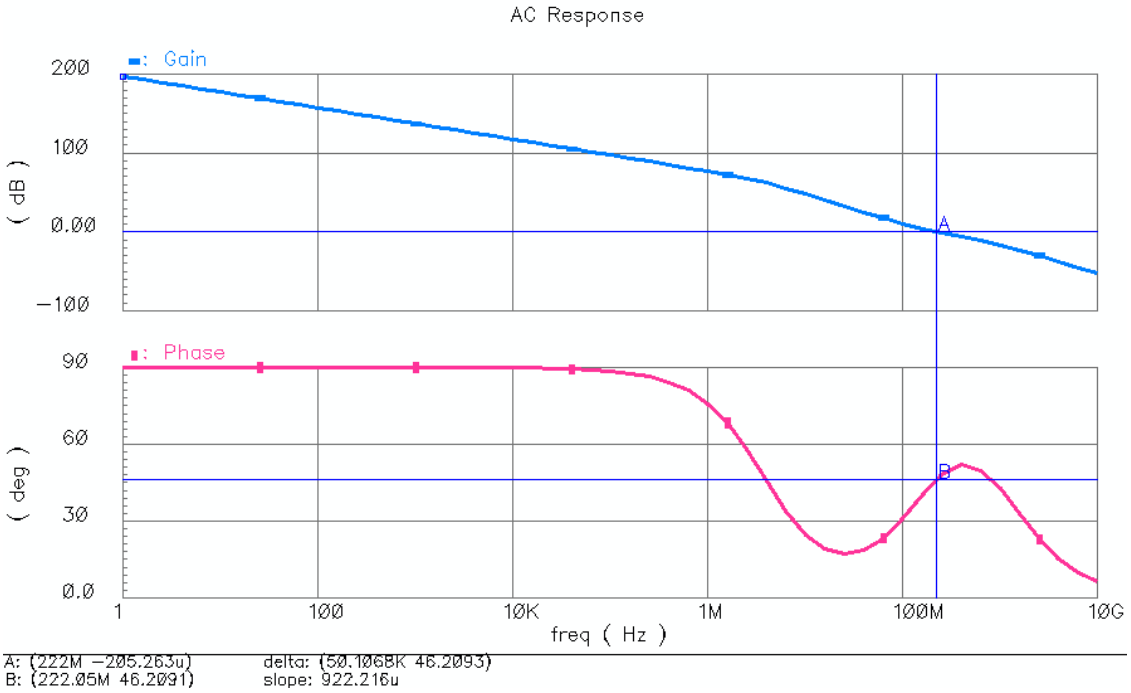


Figure 5.5: Simulated Bode plot of the VCO-based amplifier with zero compensation

197dB, unity-gain bandwidth of 222MHz and a 46-degree phase margin. The simulated UGB is close to $2K_{VCO}K_{PD}R_C$ as expected.

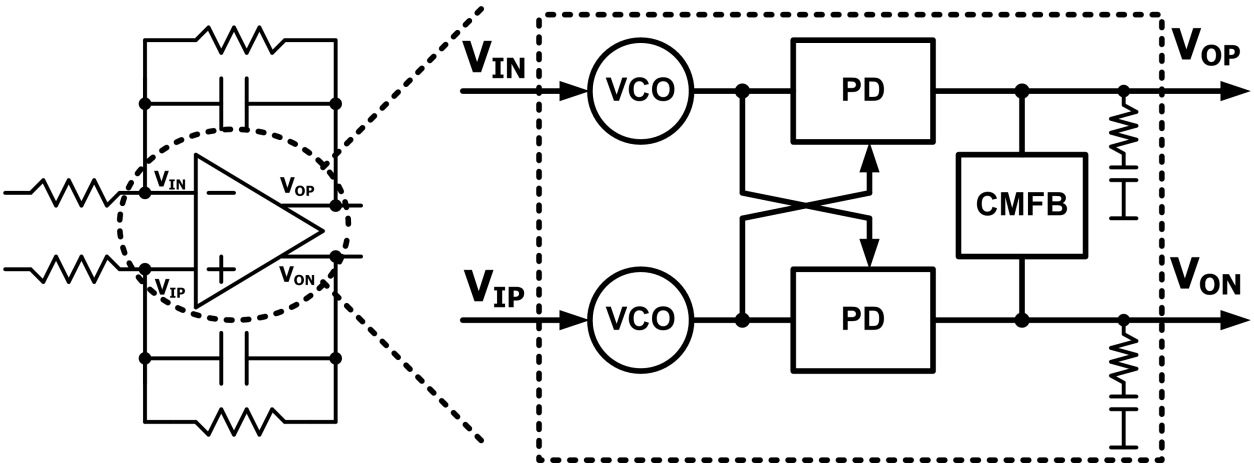


Figure 5.6: Block diagram of a first-order filter using the proposed VCO-based amplifier with zero compensation

Fig. 5.6 shows an example of an active-RC first-order filter implemented by replacing a conventional differential amplifier with the proposed differential VCO-based amplifier with zero compensation. Except for a high DC gain, the differential VCO-based amplifier has a very large common-mode rejection ratio (only limited by mismatches, similar to a traditional differential pair) because any change at the common-mode voltage does not result in a phase difference and thus no change in the amplifier's output resulting in a zero common-mode voltage gain.

The VCO-based structure does have the following possible non-idealities. The output spectrum of the VCO-based amplifier may have the spurs around the VCO oscillation frequency and its harmonics. The spurs will be small due to the bandwidth limitations in the output stages if the VCO oscillation frequency is chosen high enough from the desired signal bandwidth. Mismatches between the two ring oscillators lead to differential DC offset at the amplifier's input. This DC offset is small and can be reduced by the compact layout of the two oscillators. The non-linear V-to-F conversion in the VCO leads to a voltage dependent K_{VCO} and limits the input linearity of the VCO-based amplifier. The effect of this nonlinearity is strongly reduced when used in a feedback configuration. The input-referred noise of the VCO-based amplifier is dominated by the phase noise of the VCO; the contributions of the phase detector and the common-mode feedback circuit are small thanks to the large gain K_{VCO} of the ring-oscillator VCOs. In simulations, the VCO-based amplifier with ring oscillators shows a similar noise performance as conventional amplifiers for a given linearity and power performance.

The circuit implementation of the differential VCO-based amplifier is shown in Fig. 5.7. The differential voltage input controls two ring oscillators to obtain a voltage-to-phase conversion. Ring

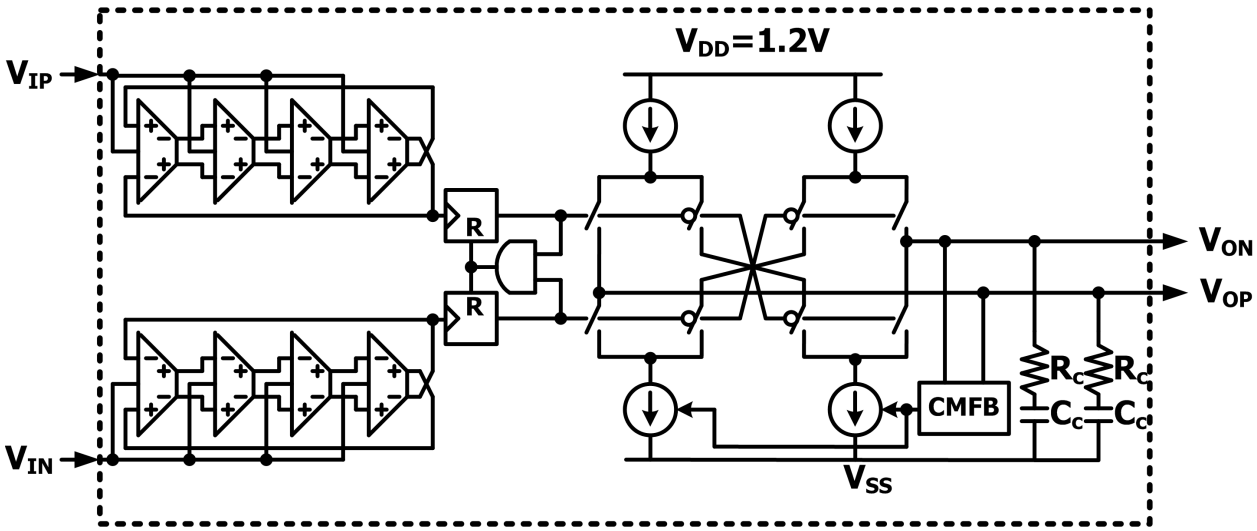
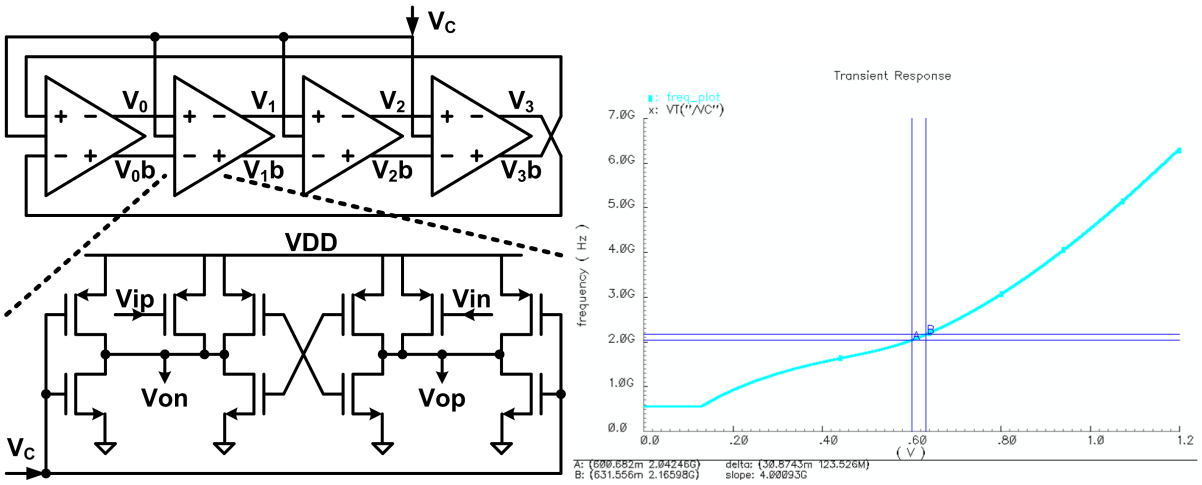


Figure 5.7: Schematic of the proposed VCO-based amplifier with zero compensation

oscillators are chosen for their larger tuning gain K_{VCO} and much smaller area than LC oscillators. A tri-state phase-frequency detector (PFD) consisting of high speed D-flip-flops determines the phase difference between the two oscillators' output. A charge pump (CP) is used to convert this phase difference from the tri-state PFD to the output current with a gain K_{PD}. A passive-RC common-mode feedback circuit maintains the output common-mode voltage of the amplifier.

The VCO-based amplifier with zero compensation was designed and simulated in a 55nm CMOS technology. A differential four-stage ring oscillator was designed with the gain K_{VCO} of 4GHz/V and oscillation frequency of 2GHz so that its input available voltage range can be close to a supply voltage while keeping the oscillation frequency sufficiently high. The detailed circuits of the oscillator and the simulated output frequency with respect to its input voltage V_C are shown in Fig. 5.8. The simulated phase noise of this ring oscillator is -81dBc/Hz at 1MHz offset and its figure of merit is around -151dBc/Hz. The input-referred noise of the oscillator is 31.5nV/$\sqrt{\text{Hz}}$ which is the dominant noise source of the VCO-based amplifier.



(a) (b)

Figure 5.8: (a) Circuits of the ring oscillator (b) The simulated characteristic of the ring oscillator showing K_{VCO}=4GHz at the output frequency 2GHz

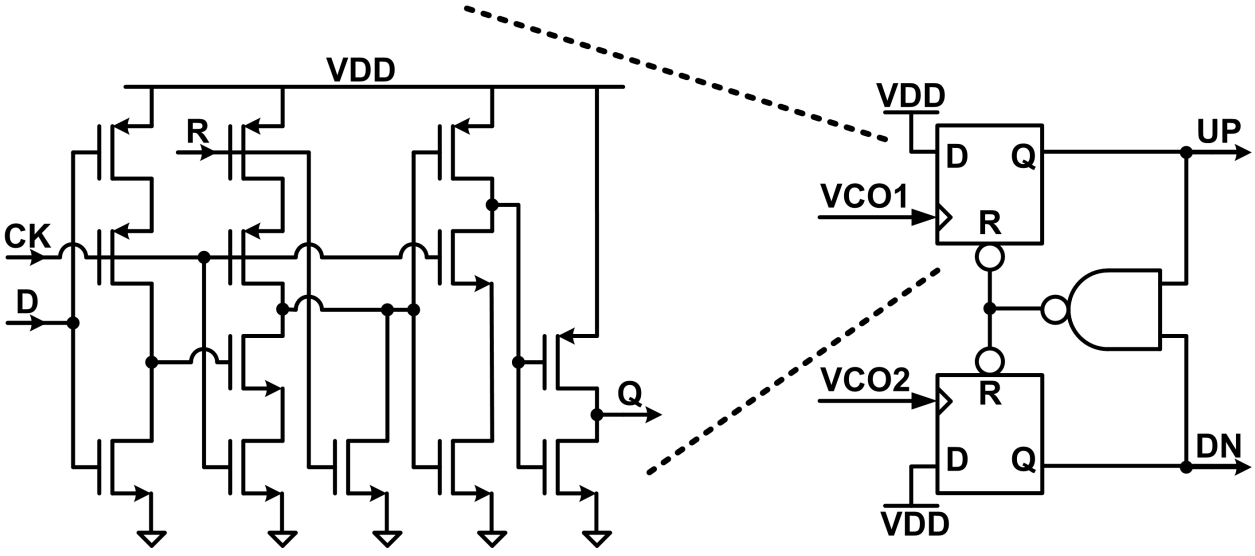


Figure 5.9: Schematics of the phase-frequency detector with high speed D-flip-flops

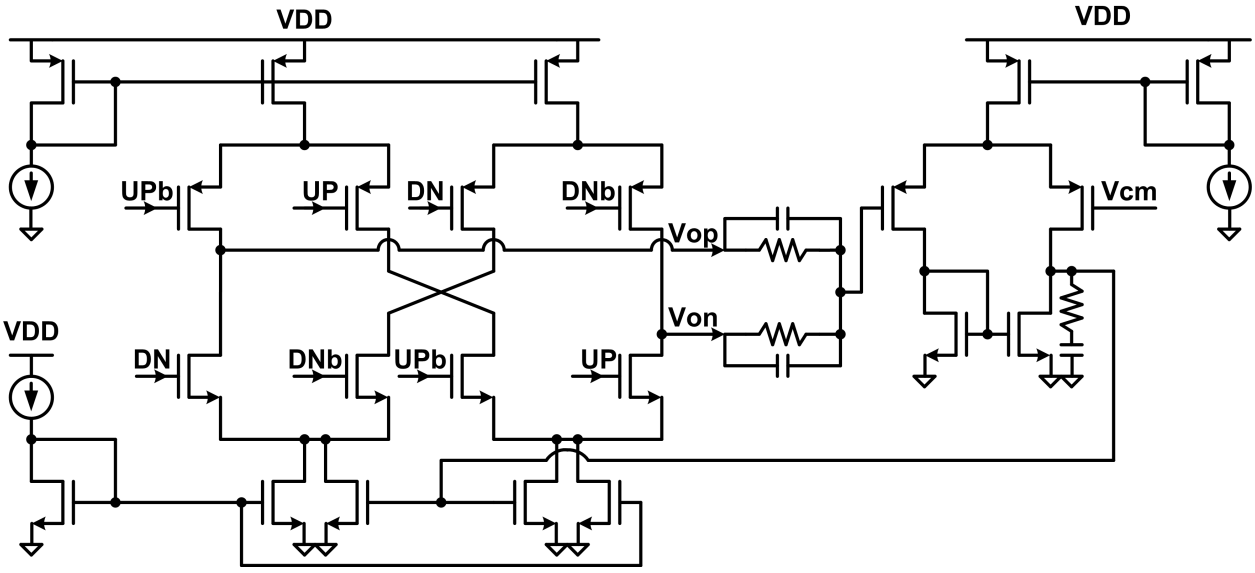


Figure 5.10: Implementations of the charge pump and common-mode feedback circuit

Fig. 5.9 shows the circuits of the tri-state PFD and its D-flip-flops. The true single-phase-clock D-flip-flops are used because their input frequency is up to 2GHz and the PFD needs the idle time of 100ps. The charge pump is formed by a pair of UP and DN current sources for differential outputs. The UP and DN current are designed by 1.13mA for the gain K_{PD} of 0.18mA/radin. In addition, the UP and DN current sources have 3-bit programmable current control and can also be adjusted externally. The schematics of the charge pump with differential outputs and the passive common-mode feedback circuit are shown in Fig. 5.10. A series of resistance and capacitance is added to improve the stability of the common-mode feedback circuit.

The overall VCO-based amplifier consumes 4.4mW from a 1.2V supply including the power consumption of 0.7mW from two ring oscillators, 0.6mW from the PFD and 3.1mW from the CP. It is worth mentioning that a multi-phase VCO structure requiring more PFD and CP may not be

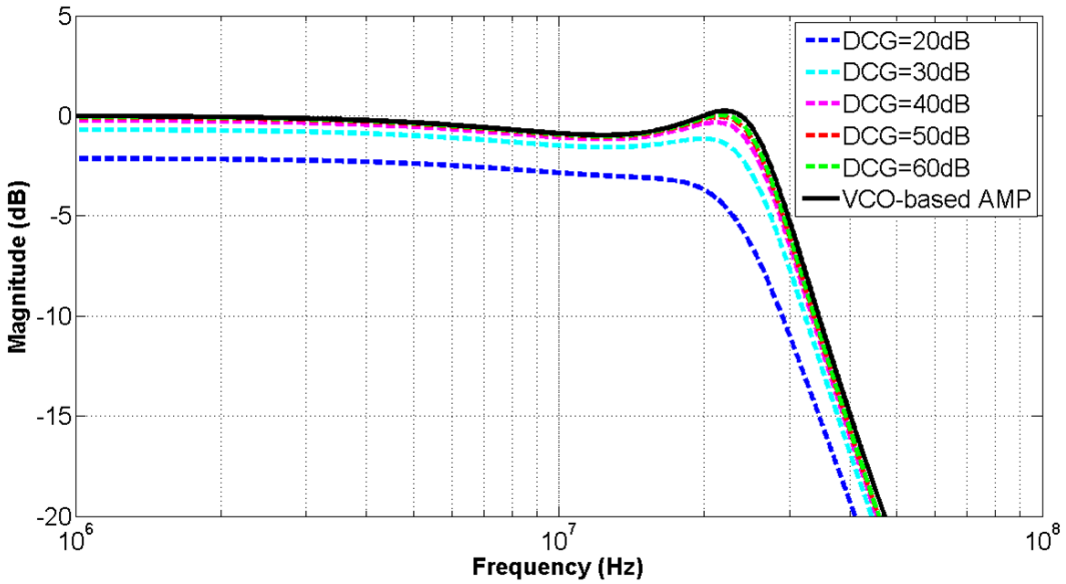


Figure 5.11: Comparisons of a 3rd-order Chebyshev active-RC filter using the amplifiers with different DC gains and the VCO-based amplifiers

suitable for the designed VCO-based amplifier because the CP's power is dominated in the total power of the amplifier in this design.

The proposed VCO-based amplifier breaks the trade-off between a DC gain and UGB of an amplifier for a given power budget. In other words, the VCO-based amplifier does not have the drawback of a finite DC gain no matter what its UGB is. By using the VCO-based amplifier, an active-RC filter does not suffer from integrator loss and a switched-capacitor circuit is not limited by settling static error due to a finite DC gain. As an example, the transfer function of an active-RC Chebyshev Filter using the amplifiers with different DC gains and the VCO-based amplifier is compared in Fig. 5.11.

5.3 Active-UGB-RC Filter Implementation

To demonstrate the use of proposed VCO-based amplifiers, a 4th-order active-UGB-RC low-pass filter has been designed by replacing the conventional OTAs with the VCO-based amplifiers. Fig. 5.12 shows the block diagram of a 4th-order active-UGB-RC low-pass filter consisting of two amplifiers with the unity-gain bandwidth ω'_u and ω_u which are comparable to the filter cut-off bandwidth [41]. It is noted that in traditional active-RC filters, the amplifiers' UGB is made much larger than the filter bandwidth so that the filter bandwidth is only decided by passive components such as resistance and capacitance. The advantage of this active-UGB-RC filter is saving the power and area while only using half numbers of amplifiers. However, it requires RC and UGB tuning for changing the cut-off frequency of the filter. The transfer function of the amplifiers can be approximated as $A = \omega'_u/s$ and $A = \omega_u/s$, and then the transfer function of the filter in Fig. 5.12 is derived as:

$$\begin{aligned}
\mathrm{H(s)} &= \frac{1}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + 1} \\
a_4 &= \frac{R^2(C+C_p)^2}{\omega_u \omega'_u} \\
a_3 &= \left(\frac{RC}{\omega_u} + \frac{RC}{\omega'_u} + \frac{3+R/R_F}{\omega_u \omega'_u}\right) R(C+C_p) \\
a_2 &= \frac{R^2(C+C_p)}{R_F \omega'_u} + (RC + \frac{1}{\omega'_u})\left(\frac{R}{R_F \omega_u} + RC + \frac{2}{\omega_u}\right) \\
a_1 &= \frac{R}{R_F}(RC + \frac{1}{\omega'_u})
\end{aligned} \tag{5.1}$$

The four poles of the filter are decided by passive components and the UGB of the ampli-

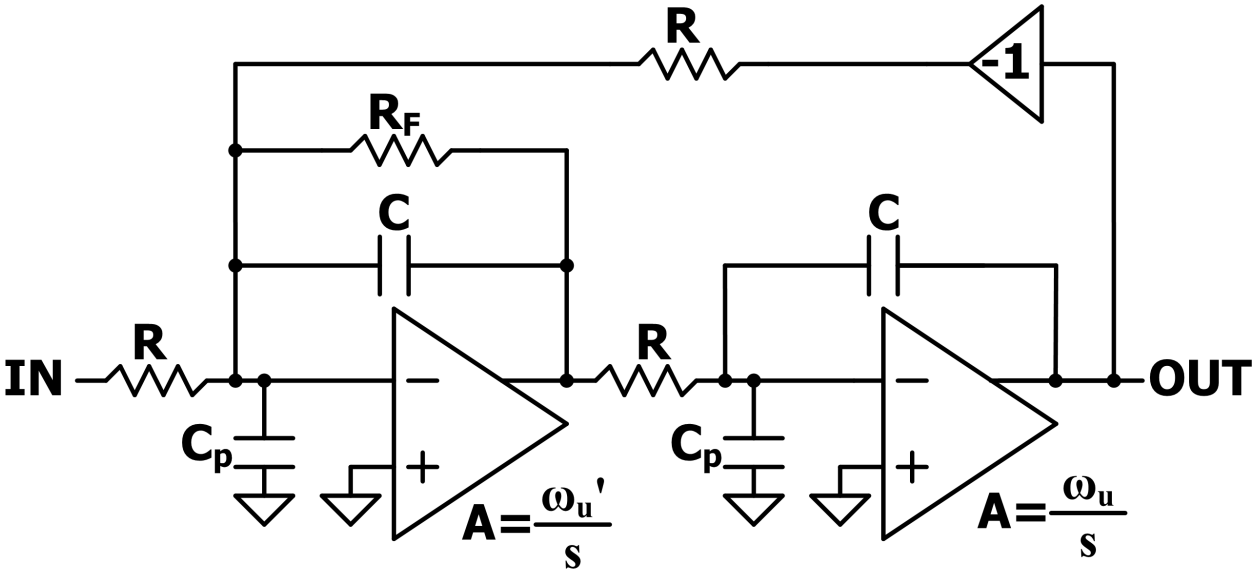


Figure 5.12: Block diagram of a 4th-order active-UGB-RC filter realized with one biquad while limiting the UGB of the amplifiers to obtain additional integrators [41]

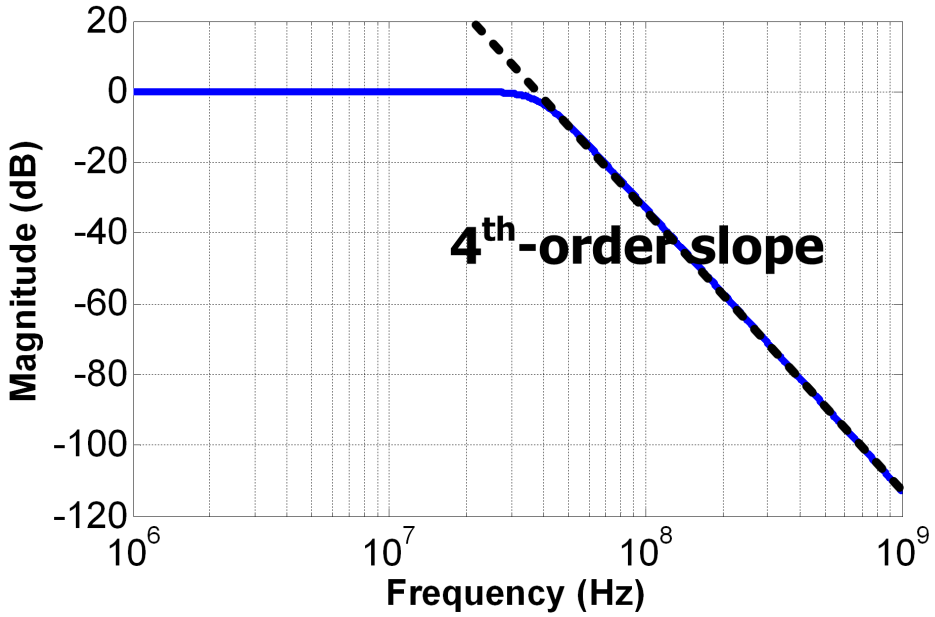


Figure 5.13: The frequency response of a 4th-order Butterworth low-pass filter implemented by a 4th-order active-UGB-RC filter using a biquad

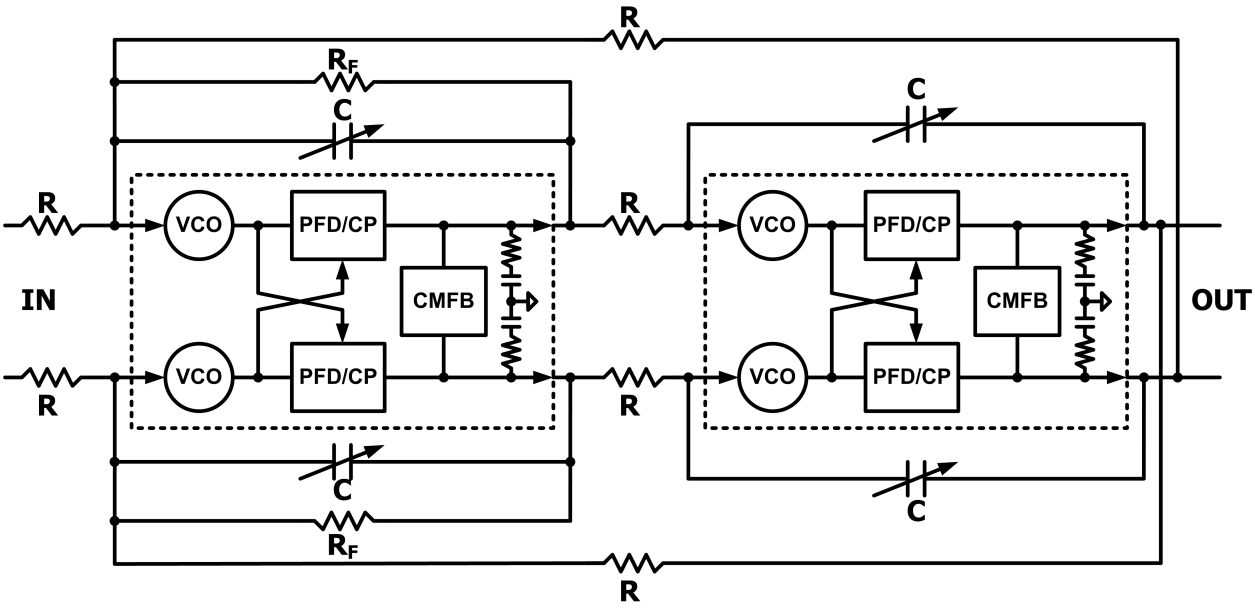


Figure 5.14: Architecture of the 4th-order active-UGB-RC filter using the VCO-based amplifiers with zero compensation

fiers. Fig. 5.13 shows the frequency response of a 4th-order Butterworth low-pass filter implemented by the 4th-order transfer function with ω_u=220MHz, ω'_u=528MHz, C=0.73pF, R=5kΩ and R_F=1.85kΩ.

The 4th-order active-UGB-RC low-pass filter using VCO-based amplifiers presented in this chapter is shown in Fig. 5.14. The VCO-based amplifier with zero compensation behaves like an integrator when the desired unity-gain bandwidth is much below the third pole of the VCO-based amplifier. Compared to [40] where integration is done exclusively in the phase domain, the active-UGB-RC implementation proposed here has improved linearity thanks to the use of linear passive components and feedback linearization. The cut-off frequency of the filter can be adjusted by changing the capacitor values or the unity-gain bandwidth of the VCO-based amplifiers, which can be easily adjusted by changing charge-pump current.

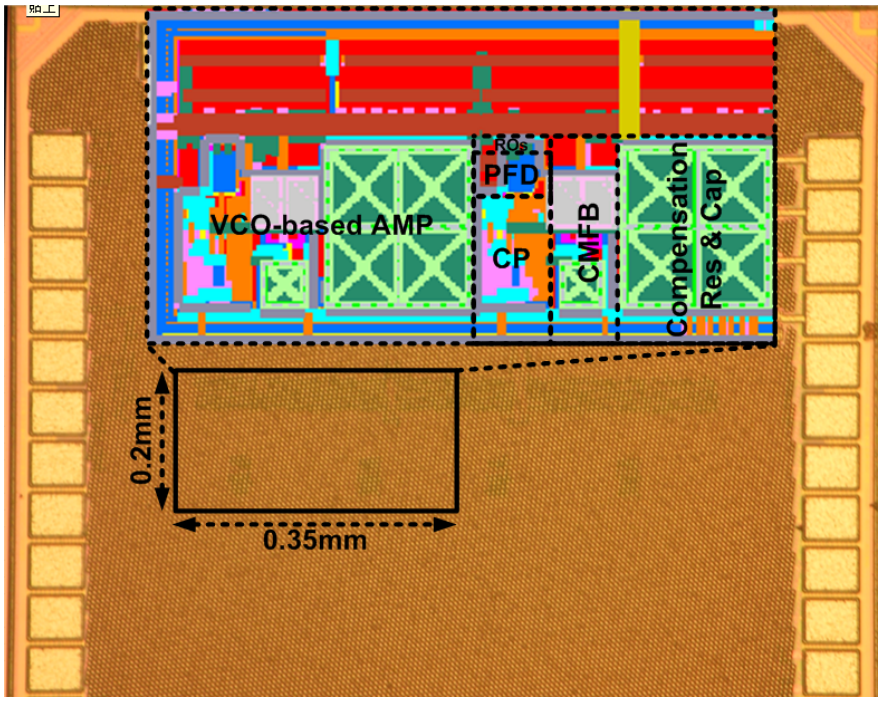


Figure 5.15: Die photo of the 4th-order filter with an insert of the layout

In summary, the proposed filter leverages linear passive components and feedback while implementing the active blocks using highly digital-like circuits compatible with technology scaling.

5.4 Experimental Results

The active-UGB-RC filter using the proposed VCO-based amplifiers with zero compensation was prototyped in a 55nm CMOS process. Fig. 5.15 shows the die photo of the 4th-order filter with the active area of 0.07mm^2 and the different area contributions from the ROs, PFD and CP. The total area is small because it does not need large area of gm as conventional amplifiers. The test bench of the filter is shown in Fig. 5.16 which includes a wide-band differential buffer to drive 50Ω load. The differential buffer has the 3dB bandwidth of 1GHz.

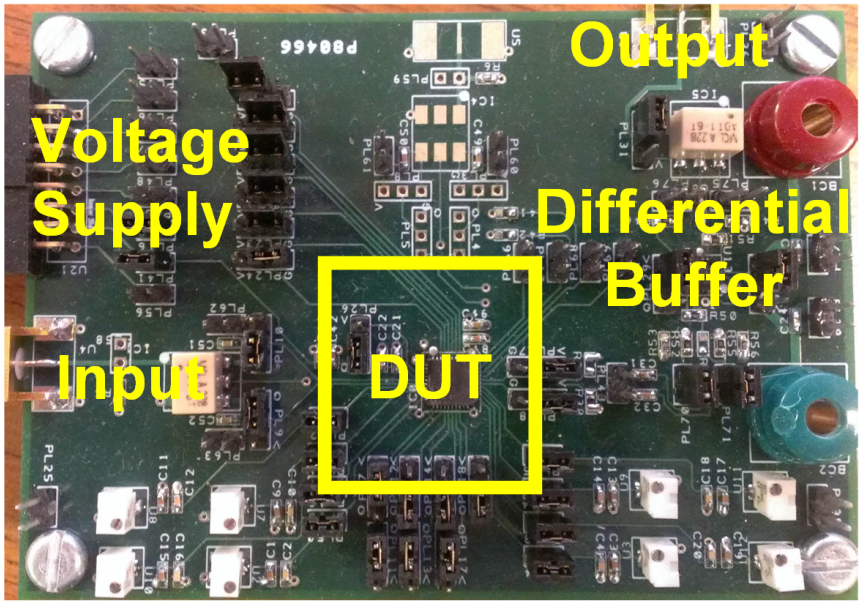


Figure 5.16: Measurement setup of the 4th-order active-UGB-RC filter

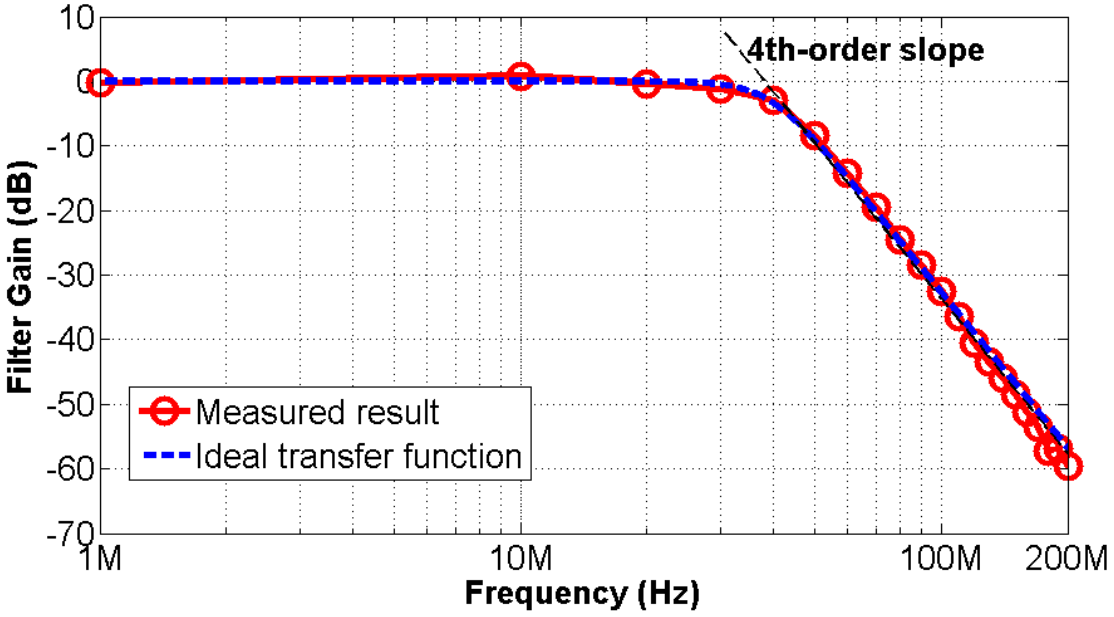


Figure 5.17: Measured frequency response of the 4th-order 40MHz filter compared with the ideal transfer function of a 4th-order Butterworth filter

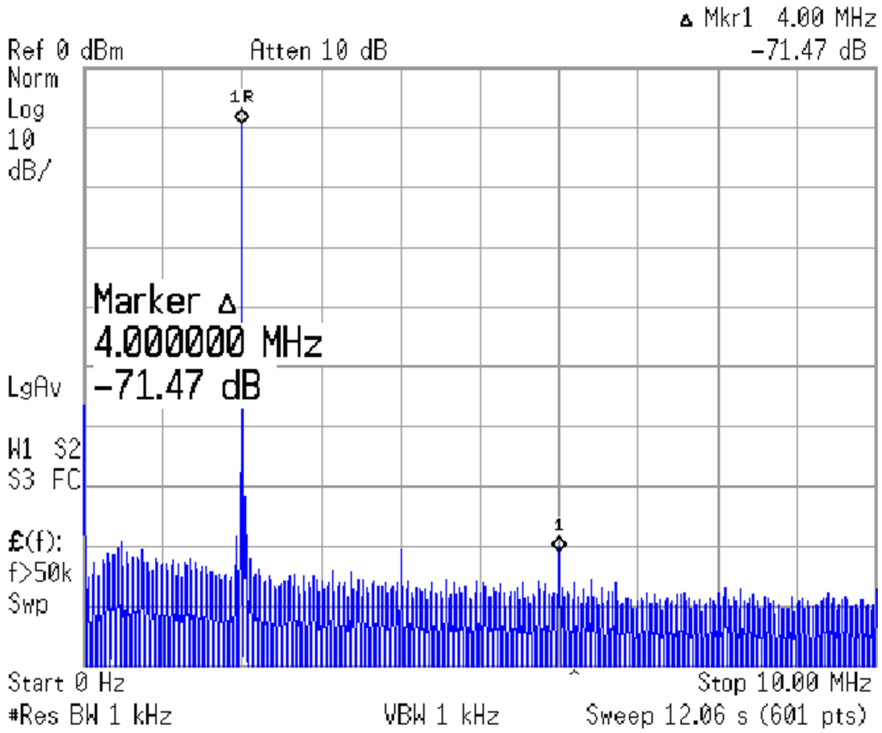


Figure 5.18: Measured narrow-band output spectrum the filter with a 2MHz and -3dBm input

The filter draws 7.8mW from a supply voltage of 1.2V. Fig. 5.17 shows the measured filter frequency response of the filter with a 3dB bandwidth of 40MHz and a slope of 80dB per decade, which is closely matching to the ideal transfer function of a 4th-order 40MHz Butterworth filter. While applying a 2MHz -3dBm differential input, the output spectrum of the filter shown in Fig. 5.18 is measured with an SFDR of 71.47dB for the bandwidth of 40MHz. The measured wide-band output spectrum in Fig. 5.19 shows that the largest spur caused by the VCO-based amplifier is at 1.573GHz and 46.6dB below the input for the VCO oscillation frequency 1.571GHz and a single-tone input at 2MHz.

The measured IM3 is shown in Fig. 5.20 to be -74.6dBc at 2.4MHz with the two-tone input at 2MHz and 2.2MHz. The in-band IIP3 is measured with the same tones while the out-of-band IIP3

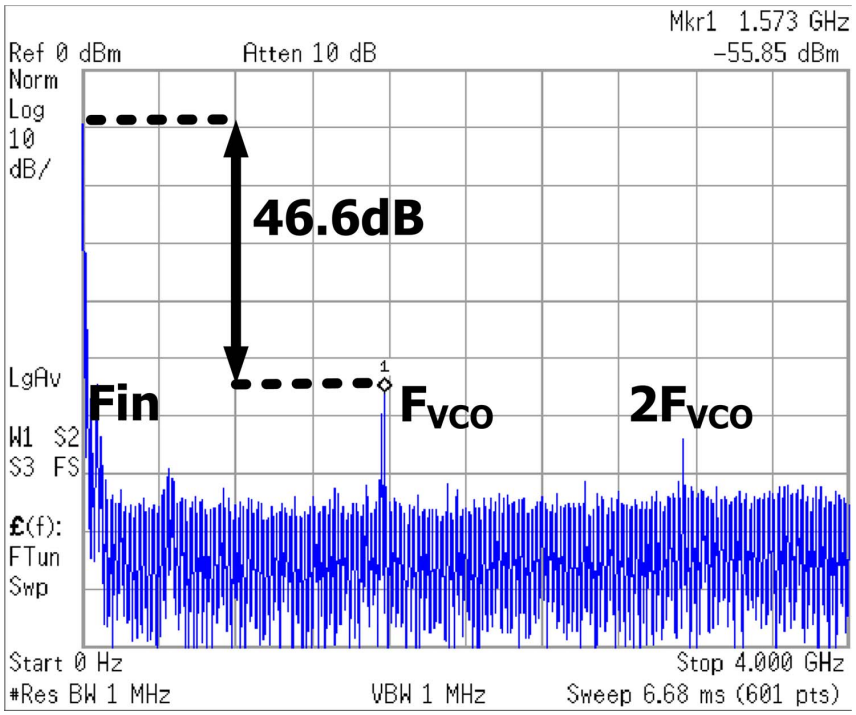


Figure 5.19: Measured wide-band output spectrum of the filter showing the high-frequency spurs caused by the VCO-based amplifier

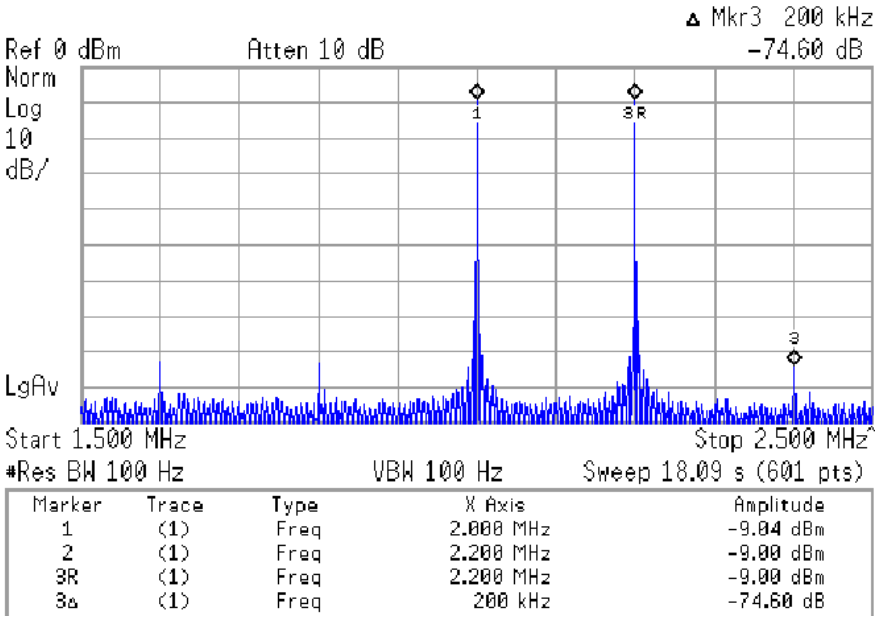
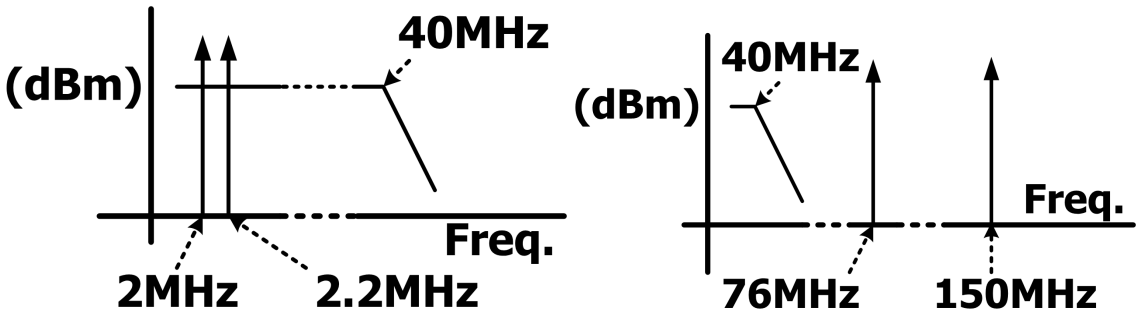


Figure 5.20: Measured output spectrum of the filter for a two-tone input with the power level -9dBm at the frequency of 2MHz and 2.2MHz



(a) (b)

Figure 5.21: (a) Two-tone input for the measurement of in-band IIP3 (b) Two-tone input for the measurement of out-of-band IIP3

is measured with two tones at 76MHz and 150MHz (Fig. 5.21). Fig. 5.22 shows that the measured in-band IIP3 is 27.3dBm and the out-of-band IIP3 is 22.5dBm.

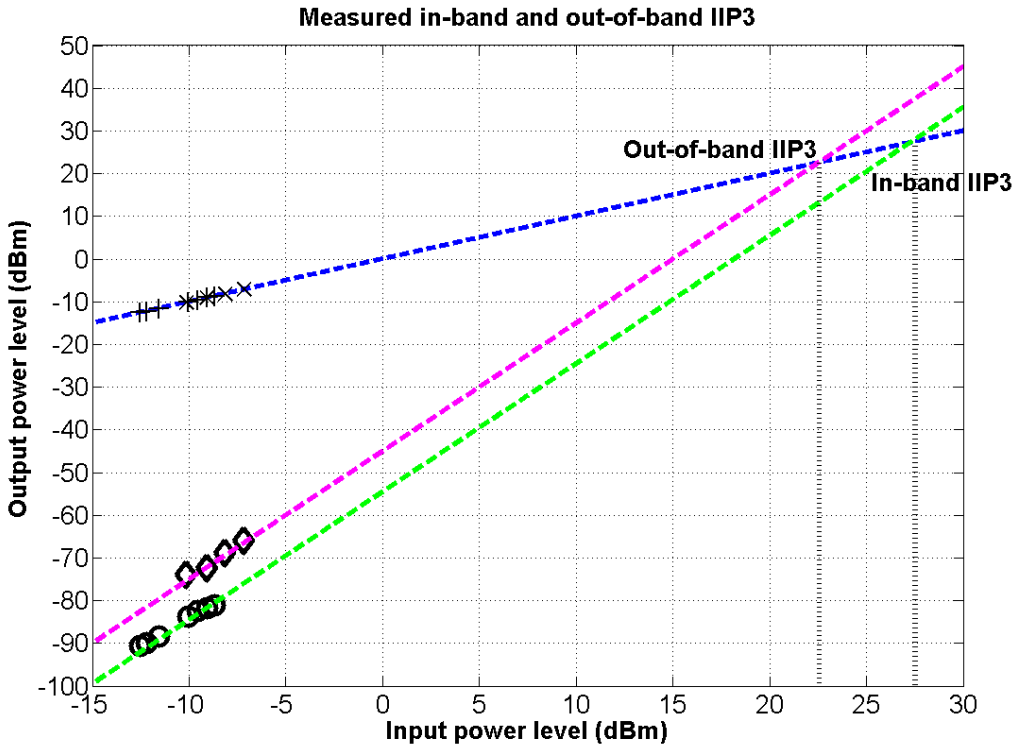


Figure 5.22: Measured in-band IIP3 with two tones at 2MHz and 2.2MHz and out-of-band IIP3 with two tones at 76MHz and 150MHz

Table 5.1: Filter Performance Comparison

	[40]	[41]	[43]	[44]	[45]	This Work
Supply Voltage	0.55V	1.2V	1.0V	1.0V	1.5V	1.2V
Topology	Type-A	Type-C	Type-B	Type-B	Type-B	Type-C
BW	7MHz	11MHz	10MHz	20MHz	19.7MHz	40MHz
Order	4	4	5	5	5	4
Noise ($nV/Hz^{1/2}$)	23.6	11	143	52	30	96
Out-of-band IIP3	-	-	-	8dBm	-	22.5dBm
In-band IIP3	8.7dBm	21dBm	21.3dBm	26dBm	18.3dBm	27.3dBm
Power	2.9mW	14.2mW	4.6mW	7.5mW	11.25mW	7.8mW
Area	$0.29mm^2$	$0.9mm^2$	$0.25mm^2$	$1.53mm^2$	$0.2mm^2$	$0.07mm^2$
CMOS Technology	90nm	$0.13\mu m$	$0.12\mu m$	$0.13\mu m$	$0.13\mu m$	55nm
FoM_1(fJ)	0.5	0.11	0.89	0.15	0.34	0.28
FoM_2(fJ$\times mm^2$)	0.15	0.099	0.22	0.23	0.068	0.02

Type-A: Gm-C, Type-B: Active-RC, Type-C: Active-UGB-RC

$FoM_1 = \frac{Power}{BW \times Order \times SFDR}$; $SFDR_{dB} = \frac{2}{3}(IIP3_{dBm} - P_{noise,dBm})$ and $FoM_2 = \frac{Power \times Area}{BW \times Order \times SFDR}$ [43]

The performance comparison of the filter is summarized in Table 5.1 demonstrating that the active-UGB-RC filter using the proposed VCO-based amplifier offers a wide bandwidth and has superior linearity than filters using conventional amplifiers or ring-oscillator integrators. In addition, the filter has a small area and a competitive figure of merit particularly when considering the contribution of area [43].

5.5 Conclusions

This work proposed a VCO-based amplifier with zero compensation to replace conventional operational amplifiers in analog circuits. The VCO-based amplifier has a huge DC gain without any significant associated penalties on its unity-gain bandwidth and area. A 4th-order 40-MHz

active-UGB-RC filter implemented with the VCO-based amplifier offers a wide bandwidth, superior linearity, and a small area.

Chapter 6

Digital In-situ Biasing Technique

This work presents a highly digital in-situ biasing solution for analog interfaces in nanoscale CMOS technologies. The digital biasing scheme uses a time-based successive approximation conversion to provide the desired analog functions with the voltage/current input and output. The digital biasing circuit gets benefits from scaled devices with a small dimension and a high Ft, but with no design difficulties by the advanced CMOS process. By taking advantage of ultra-compact digital logic for control and adaptation, the digital biasing circuit does not suffer from the impact of intra-die variations because it eliminates the need for shared biasing approaches. A digital common-mode feedback circuit (CMFB) for a fully-differential amplifier was simulated to demonstrate the advantages of the digital insitu biasing scheme. The digital CMFB designed in a 65nm CMOS process provides a desired output common-mode voltage as a conventional analog CMFB, but does not need any stability compensation schemes. Compared with the analog CMFB, the

digital CMFB with the digital-like structure is more robust and also has a much smaller area and no need for large passive components.

6.1 Introduction

Today, highly-integrated systems are implemented in a nanometer CMOS technology because digital core circuits take advantage of smaller and faster scaled devices. However, the trend has brought scaling challenges to analog domains like small signal headroom, low power gain by small output impedance, and short-channel effects that include drain-induced barrier lowering, punch-through, and velocity saturation. Therefore, the fact that digital intensive solutions are replacing analog circuits, but providing the same analog functions is attracting a lot of attention.

Fig. 6.1 shows different time-based, frequency-based or phase-based circuits with a truly dig-

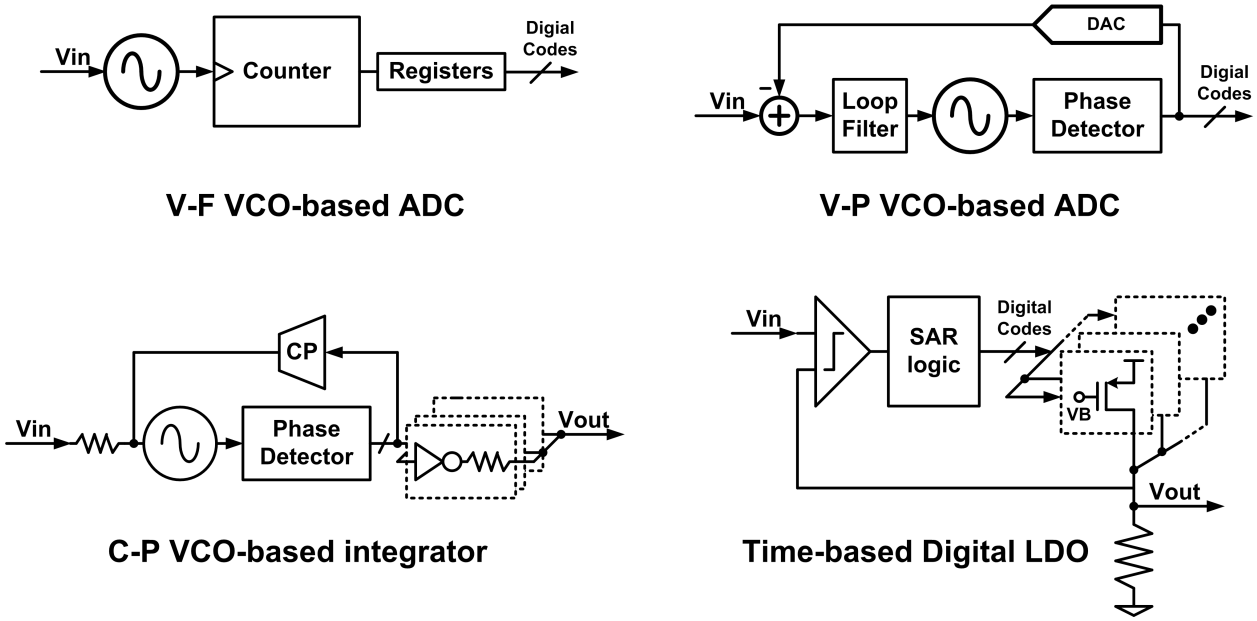


Figure 6.1: Block diagrams of different time-based, frequency-based or phase-based circuits

ital nature were developed to solve scaling problems by converting the signal processing from voltage/current domains to time, frequency or phase domains. A voltage-to-frequency VCO-based or time-based ADC [47] uses VCOs to transfer input voltage to a frequency and then gets a corresponding count in sampling registers as its digital output. However, this suffered from poor linearity because the entire non-linear transfer characteristic of the VCO was used in an open loop configuration. To improve the linearity, a voltage-to-phase VCO-based ADC [46] processes its signal in phase domain with a XOR phase detector and puts the VCO in a feedback loop. The output phase of the VCO is the time integral of its input voltage, so the VCO behaves as an ideal integrator, forcing small input swing to the VCO in the feedback loop. However, its inner loop filter still needs to face scaling challenges. In addition, the VCO-based ADCs are limited for applications of requiring an analog output. A current-to-phase VCO-based integrator [48] was provided with current-to-phase operation for the functions of analog filters. But, its VCO may have a large current input and there is a DC pole created by the integrator which may limit its uses. A time-based digital low-drop regulator [50] was proposed to decrease scaling difficulties by replacing its inner error amplifier with a comparator and shift register, but this was limited by comparator hysteresis or metastability.

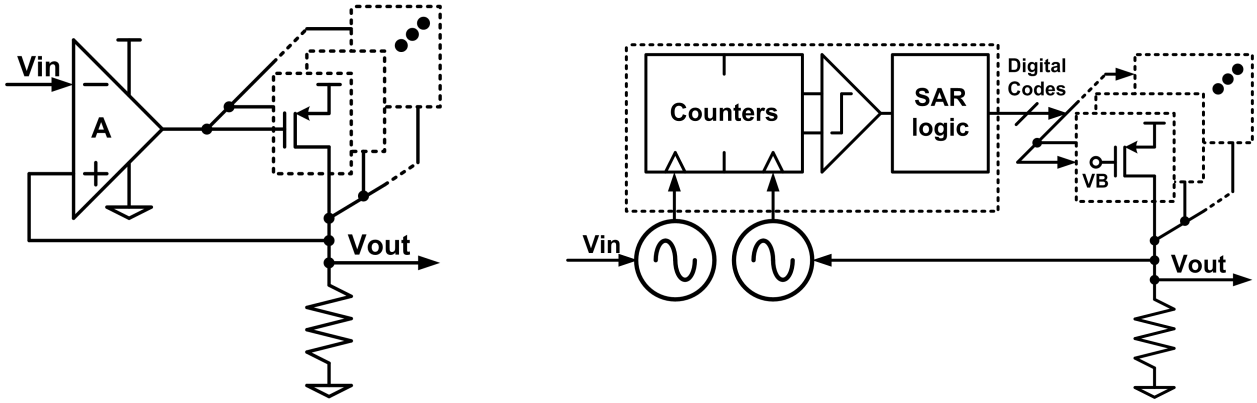
A voltage-to-phase VCO-based amplifier [49] was proposed to replace conventional analog amplifiers for general-purpose applications. The VCO-based amplifier uses zero compensation to solve the stability problem caused by the DC pole and output pole while still getting the benefits of an infinite DC gain. However, the compensation may require a large area of passive components according to the output load. A digital insitu biasing solution using a voltage-to-frequency VCO-

based circuit in a successive-approximation (SAR) loop is proposed for general-purpose analog interfaces. To explore the advantages of the digital biasing concept, a digital common-mode feedback circuit was simulated as a demonstration. The chapter is organized as follows. Section 6.2 introduces the digital biasing concept as a low-cost and robust solution compared to the analog biasing schemes; in section 6.3, a digital CMFB using the digital biasing technique is proposed for a fully-differential amplifier. Section 6.4 describes the detailed implementation and simulated results of the digital CMFB.

6.2 The Digital Biasing Technique

The digital biasing technique is proposed to overcome the challenges of conventional analog biasing circuits in advanced digital CMOS processes. A time-based successive-approximation structure is introduced using a voltage-to-frequency VCO-based circuit that puts VCOs in a successive-approximation loop to minimize their input swing for good linearity. Fig. 6.2 shows the examples of a voltage regulator using an analog biasing technique and a digital biasing technique.

The voltage regular using the proposed digital biasing scheme consists of two ring-based VCOs, counters, SAR logic, and digital-controlled current sources. The ring-based VCOs are chosen over LC-type oscillators for their larger tuning range and much smaller area. The output frequency difference of the VCOs is proportional to their applied input voltage difference with a voltage-to-frequency gain and converted to a counting number by the counters. Based on the counting number, the SAR logic gives the corresponding output codes to control the numbers of



(a) (b)

Figure 6.2: A voltage regulator uses (a) an analog biasing technique and (b) a digital biasing technique

the current sources. By adjusting current sources, the voltage difference decreases to zero and the output voltage of the regular follows the input reference voltage as expected.

Compared to the analog biasing technique using voltage or current operation, the proposed digital biasing circuit works with time/frequency operation while keeping voltage/current input and output. Since only the sampling time edge is a concern to the digital biasing, the circuit is not limited by the signal headroom and not sensitive to any supply change or variation because its voltage operation only has two discrete levels of supply and ground voltage. In addition, because the digital biasing circuit implemented with compact digital gates has a very small area, it also avoids the need for shared biasing and allows in-situ biasing for each circuit to improve circuit robustness against intra-die process variability.

6.3 A Digital Common-mode Feedback Circuit Adopting the Digital Biasing Technique

A common-mode feedback circuit is an important and essential analog block, but analog common-mode feedback circuits suffer from further challenges for technology scaling. A digital common-mode feedback circuit is illustrated in a 65nm CMOS process to demonstrate the advantages of the digital biasing technique. A differential amplifier with the digital common-mode feedback circuit is shown in Fig. 6.3. The digital CMFB senses the output common-mode voltage of the differential amplifier and then adjusts the digitally-controlled bias current to make the output common-mode voltage track a desired reference voltage.

The output common-mode voltage is decided by the different numbers of bias current cells with

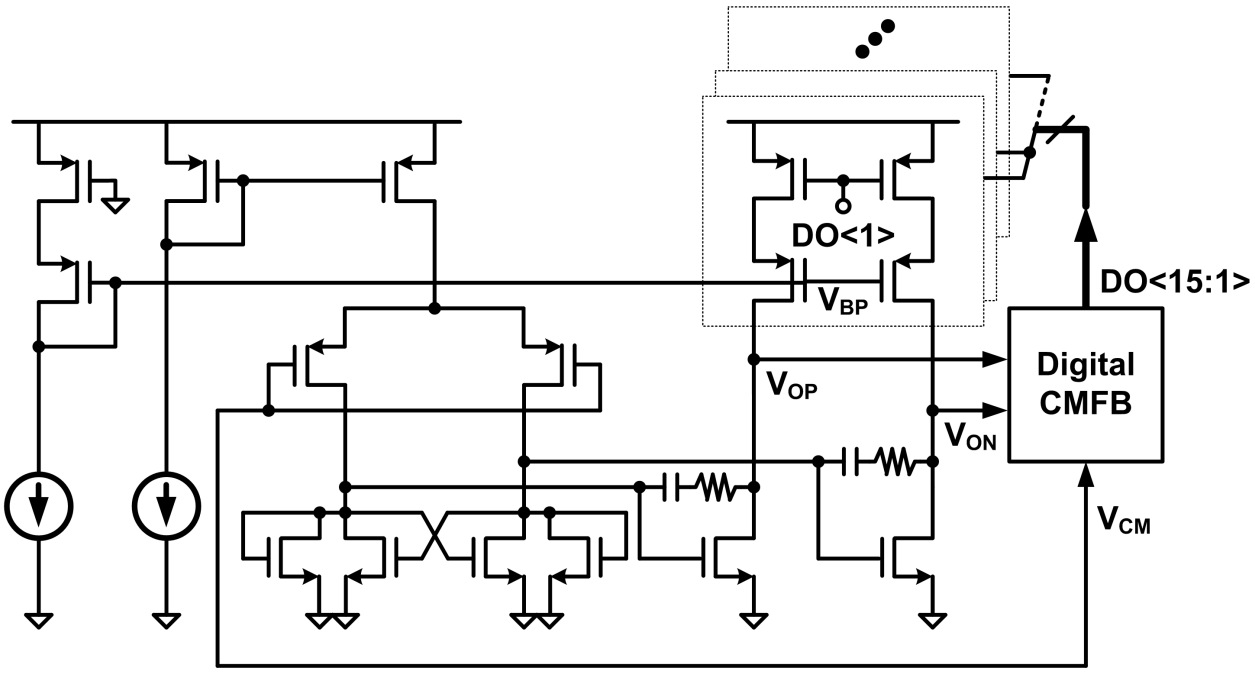


Figure 6.3: A fully-differential amplifier with a digital common-mode feedback circuit

finite output impedance due to channel-length modulation. The unit current of the cell is chosen appropriately for the required resolution of the output common-mode voltage. For example, for the maximum error of 40mV between the output common-mode voltage and the desired voltage, the unit current needs to be smaller than 16μA, while the output impedance of the main amplifier is 2.5kΩ.

The numbers of the bias current cells will not be changed if the difference between the output common-mode voltage and the desired voltage is smaller than the required maximum error. Certain control codes of the bias current cells need to be guaranteed for making the output common-mode voltage within the desired voltage and the required resolution. Otherwise, the digital CMFB loop may never reach a steady state and the output common-mode voltage will keep changing because there are no codes acceptable to the digitally-controlled current. The criterion to stop changing the control codes of current cells depends on the required resolution, the frequency gain of oscillators and a counting window which will be shown in SAR operation. The total number of current cells is decided by covering the maximum PVT variation of the output common-mode voltage. Fifteen cells are chosen in the design example from the circuit simulations.

6.4 Implementation of the Digital CMFB

The block diagram of the digital CMFB is shown in Fig. 6.4. The voltage-frequency conversion circuit converts the voltage difference between the output common-mode voltage of the main amplifier and the desired common-mode voltage to a frequency difference. Based on the frequency

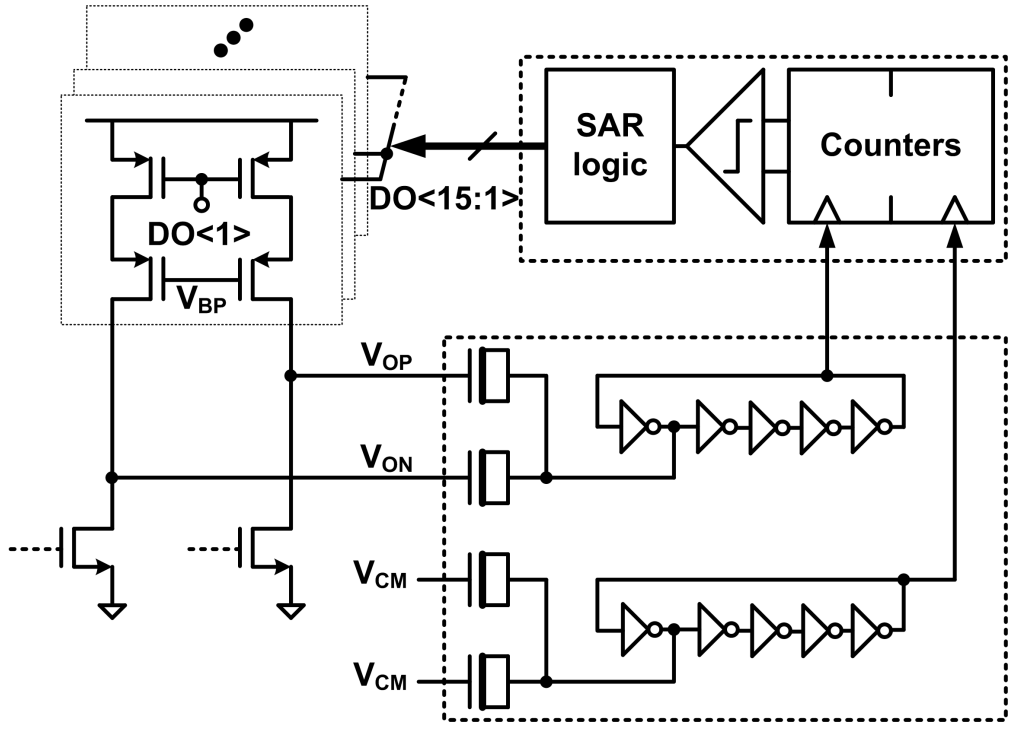


Figure 6.4: Digital common-mode feedback circuit

difference, the SAR logic gives corresponding codes to the digitally-controlled bias current and changes the output common-mode voltage to the desired voltage.

6.4.1 Voltage-frequency Conversion

Fig. 6.5 shows the circuit of the voltage-frequency conversion which consists of two pairs of varactors and two ring oscillators. The output common-mode voltage and the desired common-mode voltage are converted to two oscillators' output frequencies by using the C-V behavior of the varactors and can be explained as follows.

Because the capacitor value of a varactor strongly depends on its cross voltage ΔV_{cap}, the capacitance of the varactor with a voltage coefficient of k_0 can be expressed by: $C = C_0 + k_0 \Delta V_{\text{cap}}$.

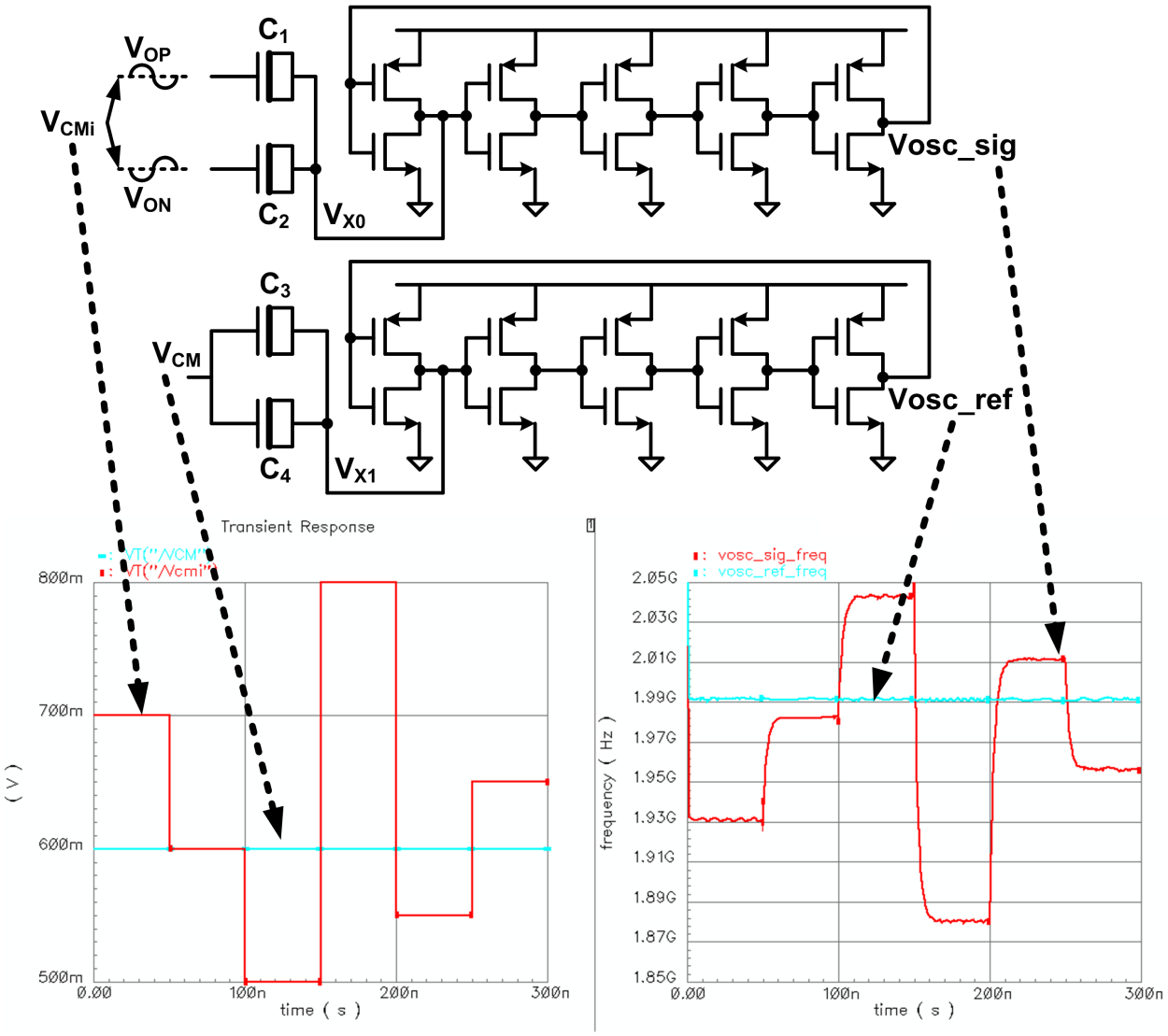


Figure 6.5: Circuits and simulations of the voltage-frequency conversion

It is noted that the high-order terms of the varactor are small and neglected. Assume that the output differential voltage signals of the main amplifier are: $V_{OP} = V_{CMi} + \Delta V$ and $V_{ON} = V_{CMi} - \Delta V$ where V_{CMi} is the output common-mode voltage and ΔV is the output signal voltage swing. Given the differential signals and the desired voltage V_{CM}, the output frequencies of the two oscillators, f_{Vosc_sig} and f_{Vosc_ref}, proportional to $(C_1 + C_2)$ and $(C_3 + C_4)$ respectively are derived by:

$$f_{Vosc\_sig} \propto 2\left(C_0 + k_0\left(V_{CMi} - V_{X0}\right)\right)$$

$$f_{Vosc\_ref} \propto 2\left(C_0 + k_0\left(V_{CM} - V_{X1}\right)\right)$$

V_{X0} and V_{X1} will be equal while the two oscillators are matched to each other. Therefore, the frequency difference of the two oscillators is proportional to $(V_{CMi} - V_{CM})$ with a voltage-to-frequency gain. If the voltage-to-frequency gain is larger, the CMFB loop has shorter reaction time and more voltage accuracy, but it also brings with higher oscillation frequency, more power and more coupling from the oscillators to the main amplifier.

Giving a design example of the voltage-frequency conversion with ΔV=0.3V and V_{CM}=0.6V, the gain is chosen by 500MHz/V and the oscillation frequency is 1.99GHz. So, the frequency resolution is 20MHz for the maximum voltage error of 40mV. The corresponding simulation result in Fig. 6.5 shows that the output frequency of the oscillator becomes smaller while its input voltage is larger; the output frequency is larger for a smaller input voltage.

6.4.2 Successive-approximation Operation

Fig. 6.6 shows the operation of the successive-approximation conversion. The frequency difference of two signals, Vosc_sig and Vosc_ref, is converted to a count number by using two counters with a counting window. The counting window is chosen by frequency resolution. For example, the window is 500ns for properly detecting the frequency difference of 20MHz.

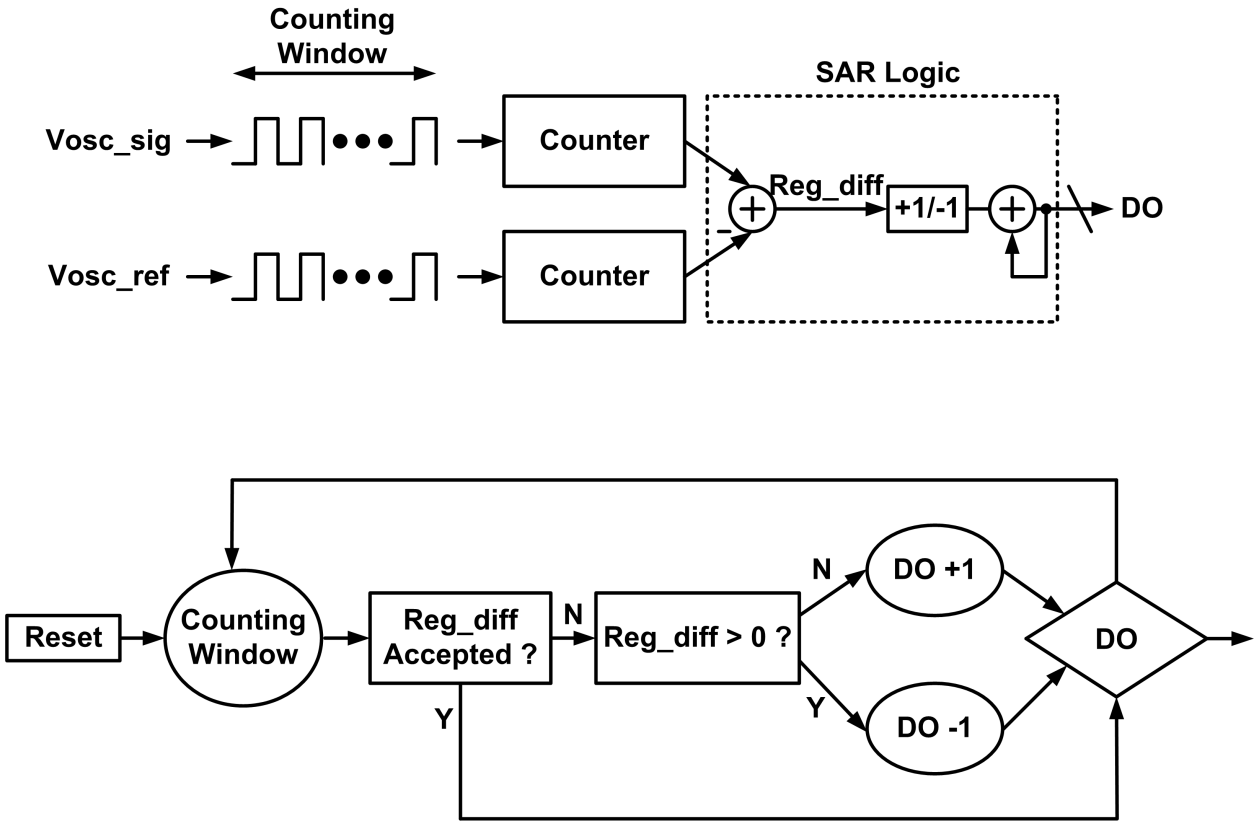


Figure 6.6: The successive-approximation operation and the state diagram of the SAR logic

Based on the count difference of Reg_diff, the SAR logic generates the digital code *DO* to change the output common-mode voltage of the main amplifier. The state diagram of the SAR logic is shown in Fig. 6.6. The output code *DO* of the SAR logic is chosen by one step change every cycle to avoid a large jump at the output common-mode voltage. This may just make the

reaction time a little longer because there are a few codes required for one voltage change. For example, even if one cycle takes 600ns, the longest reaction time to adjust the code from 0 to 15 only takes 9μs.

The simulation results of the overall differential amplifier with the digital CMFB is shown as Fig 6.7. The output differential signals of the main amplifier suddenly jump to a level close to the supply or ground voltage once when there is a change at the desired common-mode voltage V_{CM}). The output common-mode voltage of the amplifier has this jump because of the change of its input common-mode voltage. However, the output common-mode voltage is monotonicity recovered back to the desired common-mode voltage after the operation of the digital CMFB.

By using the voltage-frequency conversion, the digital CMFB does not need any extra stability compensation schemes as analog CMFB because there is only one low-frequency pole created by the output load in the CMFB loop. In addition, the digital CMFB has a discrete-time behavior and is robust to any supply variation while operating with full-swing logic signals.

6.5 Conclusions

This work introduced a digital insitu biasing technique to overcome the design challenges of conventional analog biasing circuits in the advance CMOS process. The digital biasing technique used a voltage-to-frequency successive-approximation loop to provide desired analog functions. A digital CMFB using the digital biasing scheme was simulated with a fully-differential amplifier in a 65nm CMOS technology. The digital CMFB used a voltage-frequency VCO-based circuit followed by SAR logic to adjust the digitally-controlled bias current for the desired output common-mode

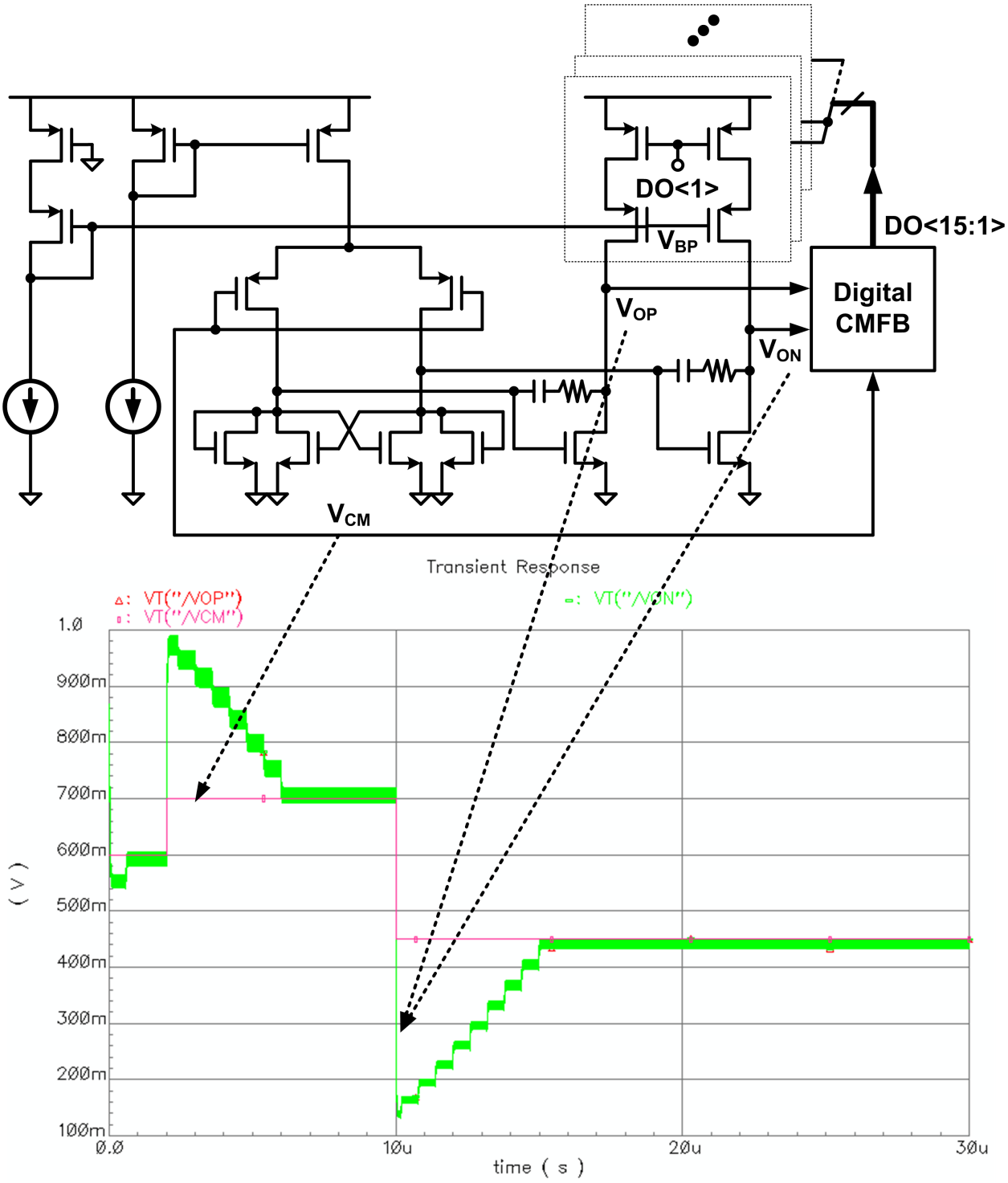


Figure 6.7: The simulated result of the digital CMFB

voltage. By using the time-based operation, the digital CMFB was robust to any change of signal headroom or supplies. Compared with analog CMFB, the digital CMFB implemented by the ultra-compact digital logic had a small area and did not need any stability compensation schemes because there was only one low-frequency pole in the loop.

Chapter 7

Summary

In this dissertation, challenges and solutions for high performance analog circuits integrated with digital circuits in low-power CMOS have been discussed with several analog examples. The research vehicles of the analog design examples cover different critical aspects of design challenges for analog circuits in SOC products. The disturbances or interference from digital circuits may make analog functions fail. The supply variation or noise due to digital operation may degrade analog performance. The device scaling brings short channel effects while the supply scaling reduces signal headroom and margin of analog circuits. The research efforts push high performance analog circuits that operate with robustness and flexible supplies, to become digitalized. The summary of each aspect is made as below and the possible direction for extended study will be discussed later.

A novel combined phase detector was proposed to offer a phase detector solution which allows for the realization of low in-band phase noise PLLs with a vastly superior robustness to supply

interference and disturbances. Compared to conventional PLLs with tri-state PFDs, the PLL with the combined phase detector achieved much lower in-band phase noise. In addition, the proposed PLL had the similar in-band phase noise performance to sub-sampling PLLs, but it was more robust to disturbances than sub-sampling PLLs.

A new pulse-controlled common-mode feedback circuit was introduced for supply-scalable differential amplifiers while implementing with large V_T devices in low power/leakage CMOS technologies. The pulse-controlled CMFB is formed by small resistance followed by switches which turn on with a small duty cycle to have equivalent large resistance. The proposed CMFB overcomes the large area cost associated with a conventional RC CMFB, and the limitations of the supply-dependent on-resistance of the switches by a switched-capacitor CMFB.

The supply-scaling performance of a continuous-time sigma-delta modulator was analyzed and verified with the transistor-level simulation of a 2MHz third-order CT SDM in a low power/leakage CMOS process. Given different supply-scaling loop noise and quantization noise, the overall figure of merit of the SDM reaches an optimum at a particular supply. The supply voltage giving the best FoM of the SDM is decided by the supply-scaling performance of the loop filter and quantizers.

A general-purpose VCO-based amplifier with zero compensation was proposed to replace conventional amplifiers in analog circuits while behaving as a digital-like circuit benefiting from advanced CMOS technologies. The VCO-based amplifier intrinsically has a huge DC gain without reducing unity-gain bandwidth or requiring large areas through compensation schemes. A filter using the large gain of the amplifier achieves a small area and good linearity performance.

A digital insitu biasing scheme was proposed as a low-cost and robust solution to analog inter-

faces in a nanoscale CMOS process. The digital biasing circuit gets benefits from scaled devices, but does not suffer from the design difficulties of using the scaled devices. A digital CMFB using the digital biasing scheme was simulated with a fully-differential amplifier. Compared with analog CMFB, the digital CMFB has a much smaller area and more robustness.

The future work to extend these studies for high performance analog circuits in a digital CMOS is discussed as below. The VCO-based amplifier with zero compensation was proposed as a general-purpose amplifier, but it suffers from large passive components required for the compensation according to the output load. To overcome the challenges by the output load, the output stage consisting of inverters and resistors [48] was proposed for low open-loop output impedance, and thus a high-frequency output pole. However, the delay of the output stage may degrade the signal phase and cause a stability problem. The work in [51] introduces a switched-mode output stage with the continuous-time FIR filtering techniques to solve this problem. By using the switched-mode output stage, a voltage-to-phase VCO-based amplifier can be implemented without any large components. This provides an alternative solution as a load-agnostic general-purpose amplifier, which may need further studies.

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