Defect Mediated Sub-Bandgap Optical Absorption in Ion-Implanted Silicon Nano-Wire Waveguide Photodetectors

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ABSTRACT

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Silicon has numerous benefits as a photonic integrated circuit platform, including optical transparency from 1.1 μm to greater than 5 μm, tight optical confinement due to its high index of refraction, high third order non-linearity, and lack of two photon absorption at wavelengths above 2.2 μm. Additionally, silicon photonics has the added benefit of decades of fabrication knowledge from the CMOS industry. Despite these advantages, an enormous challenge exists in two areas, optical sources for silicon photonic integrated circuits, and on the other end, optical detectors for silicon photonic integrated circuits. The same bandgap energy that leads to the optical transparency at telecom and mid-infrared wavelengths, limits both generation and detection in this same regime. This dissertation focuses on the detection problem, exploring the use of defect-mediated sub-bandgap optical absorption in ion-implanted silicon nano-wire waveguides.

Section I of this dissertation focuses on fabrication and the ion-implantation process, including a primer on Shockley-Read-Hall theory and its application to defect-mediated sub-bandgap optical absorption.

Section II examines the devices for use at telecom wavelengths. In Chapter 4, the fabrication and characterization of metal-semiconductor-metal ion-implanted silicon nano-wire waveguide photodiodes is examined. These devices require minimal fabrication, are compatible with standard CMOS fabrication processes, and exhibited responsivities as high as 0.51 A/W and frequency responses greater than 2.6 GHz. With improved fabrication tolerances, frequency responses of greater than 10 GHz are expected. Chapter 5 examined these ion-implanted photodiodes in a *p-i-n* configuration as a high speed data interconnect, demonstrating error free operation at 10 Gbs with expected sensitivities approaching that of Ge detectors.

Section III extends the above research to longer wavelengths, starting with data reception at 1.9 μm in Chapter 6, exhibiting an approximate 5 dB penalty in sensitivity compared to the same diodes at 1.55 μm, at a data rate of 1 Gbs, limited by RC due to the 2 mm length of the device. Chapter 7 goes even further, characterizing Si^+ implanted silicon nano-wire waveguides for operation between 2.2 μm and 2.35 μm. These devices showed responsivities as high as 9.9 mA/W, with internal quantum efficiencies approaching 5%. Chapter 8 concludes with the characterization of Zn^+ implanted silicon nano-wire waveguides operating in the same wavelength regime, exhibiting higher overall responsivity, albeit at a much higher reverse bias. These long wavelength devices open up new areas of research for silicon photonics, allowing for CMOS compatible detectors operating into the mid-infrared region, useful for chemical sensing, free-space communications, and medical imaging.

Table of Contents

LIST OF FIGURES vi

LIST OF TABLES xvi

ACKNOWLEDGEMENTS xvii

DEDICATION xxi

CHAPTER ONE: Introduction 1

1.1 History of Lightwave Communications 1

1.2 Silicon Photonics 7

1.3 Silicon Detectors 9

1.3.1 Heterogeneous PDs 10

1.3.2 Si/Ge PDs 11

1.3.3 Graphene Detectors 12

1.3.4 Schottky MSM 12

1.4 Scope of Work 13

SECTION I: FABRICATION AND ION IMPLANTATION 15

CHAPTER TWO: Fabrication 16

2.1 Device Structure 16

2.2 Fabrication 17

2.2.1 Metal-Semiconductor-Metal PDs 17

2.2.2 p-i-n Device Fabrication 25

CHAPTER THREE: Ion Implantation 27

3.1 Ion Implanter Operation 27

3.2 Types of defects 32

3.3 Photodetection via Trap Assisted Optical Absorption 34

3.4 Stopping Range of Ions in Matter Simulations 39

SECTION II: TELECOM WAVELENGTH DETECTORS 44

CHAPTER FOUR: Metal-semiconductor-metal ion-implanted Si waveguide photodetectors for C-band operation 45

4.1 Background 45

4.2 Device Operation, Design, and Fabrication 47

4.2.1 Device Operation 47

4.2.2 Device Design 48

4.2.3 Device Fabrication 50

4.3. Results and Discussion 52

4.3.1 Responsivity and Internal Quantum Efficiency 52

4.3.2 Frequency Response 57

4.4 Conclusion 59

CHAPTER FIVE: 10 Gb/s Error-Free Operation of CMOS-Compatible All-Silicon Ion Implanted Waveguide Photodiodes at 1.55μm 60

5.1 Background 60

5.2 Measurements and Results 63

5.2.1 Experimental setup 63
5.2.2 Detector sensitivity 63
5.2.3 L1, L2, and initial state photocurrent 65
5.3 DISCUSSION 67
5.3.1 Receiver Sensitivity 67
5.3.2 Frequency Response 68
5.4 CONCLUSION 69
SECTION III: LONG WAVELENGTH OPERATION 71
CHAPTER SIX: Error-Free Operation of an All-Silicon Waveguide Photodiode at 1.9 µm 72
6.1 BACKGROUND 72
6.2 MEASUREMENTS AND RESULTS 74
6.2.1 Experimental Setup 74
6.2.2 Results 75
6.3 DISCUSSION 77
6.3.1 Responsivity 77
6.3.2 Frequency Response 80
6.4 CONCLUSION 82
CHAPTER SEVEN: Si^{+}-implanted Si-wire waveguide photodetectors for the mid-infrared 83
7.1 BACKGROUND 83
7.2 DEVICE DESIGN AND FABRICATION 85
7.3 RESULTS AND DISCUSSION 87

7.3.1 Photocurrent and Linearity 87
7.3.2 Responsivity 89
7.3.3 Absorption and Internal Quantum Efficiency 91
7.3.4 Frequency Response 94
7.4 LOSS CALCULATIONS 95
7.5 CONCLUSION 96
CHAPTER EIGHT: Extrinsic photodiodes for integrated mid-infrared silicon photonics 97
8.1 BACKGROUND 97
8.2 THEORY, FABRICATION AND EXPERIMENTAL SETUP 100
8.2.1 Theory of Zn Substitutional Defects for Sub-Bandgap Absorption 100
8.2.2 Fabrication 102
8.2.3 Experimental Setup 104
8.3 RESULTS 105
8.3.1 Responsivity 105
8.3.2 Absorption Coefficient 106
8.5 LOSS CALCULATIONS 109
8.6 CONCLUSION 111
CHAPTER NINE: Conclusion and Future Work 113
9.1 Conclusion 113
9.2 Future Work 116
REFERENCES 118

LIST OF FIGURES

1.1. (a). Image of the photophone transmitter and (b) receiver invented by Alexander Graham Bell in 1880. Compared with the telephone, the device was large and was dependent upon appropriate weather conditions 2

1.2. Coaxial versus Optical Fiber Attenuation versus frequency for multiple types of coaxial cable and both single and multimode fibers operating at varying wavelengths. Graph from [14] 4

1.3. (a). IBM concept image of a multicore processor with optical data routing between cores [27,28]. (b). IBM concept of a switching PIC capable of routing optical data between cores as shown in concept sketch [28] 7

1.4. (a). Device render featuring a photodetector (red feature on left side of the cube) and modulator (blue feature on right side of the cube) along with silicon transistors (red sparks on the far right of cube) integrated on a single silicon chip. [38] (b). Angled view of chip with the optical waveguides highlighted in blue and high speed copper electrical interconnects highlighted in yellow [38].....8

1.5. Absorption coefficient versus wavelength for several common semiconductor materials. The relatively high and indirect bandgap of 1.1 eV in silicon limits detection to wavelengths less than 1.1 μm, while smaller bandgap materials such as Ge and InGaAs have photodetection beyond 1.6 μm, making them suitable for telecom wavelengths. Graph from [57] 10

2.1. (a) Device cartoon for the MSM devices fabricated from 220 nm Soitec SOI wafers [90]. The coupler region is shown at the edge of the chip, followed by an

adiabatic taper into the waveguide. The waveguide is ion-implanted in the region with the 'wings' to create the photodiode. Waveguide dimensions for both the MSM and *p-i-n* devices are given in the insets, whereas wing height varied and is discussed in the individual chapters. (b). Scanning Electron Microscope (SEM) image of completed MSM devices 17

2.2. (a). Initial layers with the Si substrate followed by a 3 μm SiO_2 layer and then a 220 nm Si layer, topped with a ~90 nm layer of HSQ (not to scale). (inset) Labeled layers of the substrate after application of HSQ. (b). Pattern defined in HSQ after electron-beam lithography. (c). Development of HSQ leaves HSQ waveguide pattern over Si layer. (d). Initial etch of Si leaving a ridge of between 40 – 70 nm to be patterned to define the 'wings'. (e). After definition and etching, the waveguide is complete. (f). Final step in the process is the deposition of the metal contacts, resulting in the completed waveguide structure 18

2.3. SEM image of Silicon NWWG along with pillars resulting from incomplete removal of particles during the development process. Image from [19] 21

2.4. (a). SEM top view image of waveguide and contacts. A significant number of nano-scale particles can be seen on top of the contacts, believed to be left over from the lift-off and caused by sonication. (b). After performing tests on the devices, the nano-scale particles would collect on the sidewalls of the waveguide, leading to device failure at higher voltages 23

2.5. SEM image of cleaved facet showing the fan out coupler.....25

3.1. Illustration of the ion implanter used at the IBL facility in Albany. Illustration provided by [100].....28

3.2. (a). Mass spectrum analyzer output for the Si implantation, with the Si and F peaks clearly visible along with a residual Ar peak. (b). Mass spectrum analyzer output for the Ar implantation, with the Ar peak clearly visible, along with a residual N_2 peak 31

3.3. (a). Initial crystal lattice structure prior to implantation. (b). Ion implantation results in vacancies where the an atom is knocked out of its lattice site, interstitials, where an atoms end up in between lattice sits, and substitutional defects, where the ion implanted replaces an atom in its lattice site. (c). The divacancy defect common in implanted silicon is the result of the mobile vacancies meeting up and forming a stable defect consisting of two vacancies. (d). In the case of self-implantation and sufficient annealing, a large number of interstitials are found in the within the Si lattice. (e-f). With sufficient annealing, these interstitials are mobile and tend to from small clusters, from 3 – 10 atoms [107].....33

3.4. (a). During ion implantation where the substrate face is perpendicular to the direction of the ions, a phenomenon called ‘tunneling’ can occur, where the ion travels deep into the target material without encountering any collisions. (b). To reduce the chance of tunneling, the target material was set a 7˚ angle off the perpendicular.....34

3.5. (a). For photodetection without trap state assistance, the photon energy must be greater than the band gap of the semiconductor. In addition, in the case of silicon, which has an indirect band gap, a phonon is also required to account for the momentum change. (b). Using trap state assistance, a photon with an energy less

than that of the bandgap but near the level of the trap state can excite an electron to the trap state. If the trap state is sufficiently close to the conduction band, the electron is then thermally excited to the conduction band.....36

3.6. Illustration of the four processes involved in SRH theory, each defined in the text above.....37

3.7. (a). Cross-section of *p-i-n* waveguide with modal intensity super-imposed. (b). One dimensional cut of the waveguide cross-section down the center showing both the normalized mode intensity as a function of depth in the waveguide and the normalized defect concentration, for a Si^+ implantation energy of 190 keV, as a function of depth in the waveguide.....41

3.8. Results of TRIM calculations on the 'wing' area of the Si NWWG PDs. The collision events is a measure of the vacancies produced, however the results do not account for self-annealing due to the elevated temperature of the NWWGs 43

4.1. (a). Device cartoon with lower inset showing the cross-section of a *p-i-n* device from [4] and upper inset giving the cross-section of our MSM structure. (b). SEM image of 250 μm device.....47

4.2. (a). Band diagram of MSM device without application of a bias. (b). Band diagram of MSM device with the application of the flat band bias demonstrating photodetection.....48

4.3. Simulated parasitic loss verses waveguide-contact gap for 750 × 220 nm waveguide with wing heights of 50 nm and 150 nm at λ = 1550 nm. (insets) Mode intensity for the quasi-TE guided mode for both 50 nm (lower) and 150 nm (upper) wing heights. The lower modal confinement of the 150 nm-wing height

increases the required contact gap for a given amount of parasitic loss. For devices reported here, the waveguide-contact gap is 2.3μm 49

4.4. SEM images of fabricated devices. (a). View of the waveguide sidewalls showing no measurable roughness over the length of 1 μm. (b). Top view of waveguide with wings and contacts; the contact separation is 5.4 μm. (inset) High-magnification view of the waveguide showing waveguide width of 763 nm.....51

4.5. (a). Responsivity *versus* bias voltage with error bars for 1mm long PDs. (inset) Photocurrent for ≈1 mW optical power and dark current for typical 1mm long PD. (b). Responsivity verses wavelength from 1550 nm to 1610 nm for a 30 V bias, the dashed line is a second-order polynomial fit to illustrate the trend 54

4.6. (a). Measured modal absorption coefficient verses wavelength from 1530 nm to 1610 nm. The data was smoothed to reduce noise in our measurement setup and thus obtain a general trend. (b). Linearity of device with input optical power at λ = 1550 nm from .015 mW to 13 mW, corresponding to power incident on detector 2.2 μW to 2 mW 56

4.7. Frequency response for a 1mm device at 40-50V along with simulation results for a carrier mobility of 50 V/cm^{2}s.....58

5.1. (a). Cross-section of a 520 nm × 220 nm Si NWWG with 50 nm wings. The channel waveguide section is Si^+ ion implanted with 10^{13} cm^{-2}, while the wings are doped p and n to form a *p-i-n* photodiode. The device is clad in SiO_2, and contacts are formed with a TiN/W Damascene process, and capped with Al. The finite-element method calculated quasi-TE mode is overlaid. (b). Top view of the device, showing the PD region as well as the cleaved facet fan-out tapers used for

input coupling from the LTF, and (c). Experimental setup for measuring detector sensitivity 62

5.2. Receiver sensitivity curves for (a). the L = 250 μm device at 2.5 Gb/s, (b). The L = 250 μm device at 10 Gb/s, and (c). the L = 3 mm device at 2.5 Gb/s. The launch power shown in dBm is the power launched on-chip from the LTF, not including facet loss 64

5.3. Eye Diagrams for the L = 250 μm and L = 3 mm devices for 5 V, 10 V, and 15 V reverse bias voltages, taken after the TIA-LA. Red outlines signify error-free operation 65

5.4. (a). Measured dark current and photocurrent for the L = 250 μm device in the initial, L1, and L2 states plotted on a log scale as a function of reverse bias voltage V_{bias} with 17 dBm CW input power at λ = 1.55 μm, and (b). Calculated 3dB frequency of the PD as a function of device length L, decomposed into it's constituent components. The eye diagram of the L = 3 mm device (inset), shows that the PD is RC-time constant limited 67

6.1. (a). Device cartoon indicating waveguide, contacts, wings, implant region, and adiabatically tapered coupler, with inset giving cross-sectional dimensions. The waveguide implant region is doped with a dose of 1013 cm^{-2} Si^{+} ions. The "wings" are 50 nm high with the heavily doped regions concentration of 10^{19} cm^{-3} and lower doped regions concentration of 10^{18} cm^{-3}. The contacts are formed with deposited Al and a 10 nm Ti adhesion layer. (b). Experimental setup for measuring BER, with solid lines representing electrical connections, and dashed lines representing fiber 74

6.2. (a). Sensitivity curve for a 2 mm-long PD operating with a 25 V reverse bias at 1Gb/s. Input power shown is the input power prior to coupling into chip. The received power is 16.5 dB down due to coupling and on-chip power splitter losses. (inset) Eye diagram for a 13.5 dBm input power. Eye is clearly open both horizontally and vertically corresponding to error-free operation. (b). Calculated responsivity versus voltage based on measured coupling loss, splitter loss, and 100% absorption. A ≈5 dB penalty was seen between 1.9 μm and 1.55 μm operation. (inset) Dark current vs reverse bias for device 76

6.3. Confinement factor (red - dashed) and parasitic loss (blue) as a function of wavelength. Insets show guided mode at 1.55μm and 1.9μm 78

6.4. Responsivity at 1.9 μm as a function of both height and width. A peak is reached for a height of 0.24 μm and a width of 0.66 μm. Expected responsivity for this device at 1.55 μm is 72 mA/W and for an interstitial device is between 54 to 86 mA/W.....80

7.1. Sketch of the device with inset showing a false color SEM cross-section of a *p-i-n* device with the calculated mode at 2.2 μm incident on the waveguide.....85

7.2. (a). Photocurrent and dark current plot for PD 1 annealed at 200˚C with 3.0 ± 1.2 mW launch power and PD 3 annealed at 350˚C with 2.7 ± 0.6 mW launch power. (b). Photocurrent versus launch power showing linearity for PD 1 and PD 3 under the same conditions. All measurements were taken at λ = 2.2 μm 88

7.3. (a). Responsivity versus annealing temperature for the three devices taken at λ = 2.2 μm. The peak at 200°C is consistent with the formation and subsequent

annealing of the divacancy defect. Error bars are based on the measured deviation in measured loss prior to the detector. (b). Responsivity versus bias voltage for PD 1 and PD 3 taken at λ = 2.2 μm under different annealing conditions 90

7.4. (a). Measured absorption coefficients for implanted channel and rib waveguides. Error bars for the channel waveguides ranged from a minimum error of ≈ 11 dB/cm occurring at 2.35 μm to ≈ 14 dB/cm occurring at 2.2 μm, while varied significantly for the rib guides, ranging from 6 to 27 dB/cm. Due to lower losses of the channel guides, the laser amplified spontaneous emission was used for measurements resulting in a continuous spectral function. (b). Calculated IQE for PD 1 after annealing at 200˚C anneal and PD 2 after annealing at 350˚C.....93

7.5. Frequency response for PD 2 (250 μm) and PD 3 (3 mm) at λ of 2.2 μm after the 200˚C anneal. The frequency response indicates the devices are limited by capacitance. The slight oscillatory modulation on the response curves was a result of reflections in measurement apparatus and was seen in other detector measurements.....94

8.1. (a). Normalized response of bulk silicon photoconductors for different dopants, re-plotted from [3]. Dopants are designated as either p-type or n-type depending upon whether the resultant trap state is closer to the valence band or conduction band, respectively. (b). False color SEM cross-section of the p-Si:Zn-n PD with finite-element-method calculated quasi-TE mode intensity at a wavelength of 2.3 μm superimposed. The waveguide has a 90 nm-thick SiO2 hardmask and 3 μm-thick buried-oxide-layer substrate. (c). Top-view optical microscope image of the

PD. The red dashed line indicates the position of the SEM cross-section shown in (b) 99

8.2. (a). Band diagram of the p-Si:Zn-n, photodiode with defect levels $E_{d1} \approx E_v + 0.3$ eV and $E_{d2} \approx E_v + 0.58$ eV in the Si:Zn region [4, 5]. The doping profile is illustrated by the false-color SEM shown below. (b). Photocurrent I_{ph} versus input optical power P_{in} along with linear fits. The linear correspondence indicates a single-photon excitation process. The higher implantation dose is shown for a 3 mm length PD 101

8.3. SRIM calculated Zn^+ implantation profile for an acceleration voltage of 260 keV 103

8.4. Experimental setup. ISO = isolator, FC = fiber collimator, PR = polarization rotator, LTF = lensed tapered fiber 105

8.5. Responsivity as a function of reverse bias voltage for (a). 250 μm device and (b). for 3 mm device. Insets: dark current as a function of reverse bias voltage for un-implanted diode (black dashed line) and PDs with Zn^+ doses of 10^{12} cm^{-2} (red solid line) and 10^{13} cm^{-2} (blue solid line). Responsivity as a function of wavelength for (c). 250 μm device and (d). 3 mm device. The decrease in responsivity with increasing wavelength is due to parasitic absorption 106

8.6. (a). Modal absorption coefficients due to Zn^+ implantation after 350˚C anneal. (b). Modal absorption coefficient vs annealing temperature for Zn^+ dosage = 10^{12} cm^{-2}. Each subsequent annealing step was performed for 10 minutes 107

8.7. Fraction of total power absorption due Zn+ implantation, $\alpha_{eff,Zn}/\alpha_{eff,tot}$, for a Zn^+ dose = 10^{12} cm^{-2} and (b) Zn^+ dose = 10^{13} cm^{-2} 108

8.8. Measured system losses with error bars.....111

LIST OF TABLES

3.1. List of materials used in TRIM calculations.....60

3.2. Implantation simulation conditions and results 61

7.1. Implantation parameters of the three tested PDs 106

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"True wisdom comes to each of us when we realize how little we understand about life, ourselves, and the world around us."

- Socrates

DEDICATION

To Ruby and our unborn child.

“In the end there doesn’t have to be anyone who understands you, there just has to be someone who wants to.”

- Robert Breault

CHAPTER ONE:
Introduction

1.1 History of Lightwave Communications

Many think of lightwave communications as a relatively recent technology, but light was used as early as the 8th century BC by the ancient Greeks to transmit simple messages [1]. With fire signals being limited to essentially single bit messages, the Greeks developed more complex systems, including a telegraph-like system, involving torches and water basins. In such a system, both the receiver and sender possessed identical water basins with spigots [2]. The sender would use a torch to signal the receiver to release of water from an identical pre-filled basin, and when the level of the water in the sender's basin reached the desired coded message, a torch was again used to signal the receiver to stop the release of water [2]. The message was encoded in the water left in the basin, allowing more complex messages to be sent [2]. However, there were still several problems with this system, including data rate (still only a limited number of messages could be sent), errors, and most notably that it still relied on transmission through an unreliable medium (air). As such, the ancient Greeks began to rely on couriers as a far more reliable method [1]. Couriers remained the favored way to transmit data over long distances for many centuries. During that time both reliability and data rates were improved with the invention of the printing press and better papers, however, transmission of information still relied on a courier system.

Although couriers were the preferred method for long distance and long messages, lightwave communications still found its uses in history from Paul Reverie (one if by land, two if by sea) to modern day traffic control where traffic controllers can use light guns to direct aircraft

in the event of a loss of communications [3,4]. As early as the 19th century Aldis lamps were used to transmit messages between ships [5]. These lamps were also used in WWII aircraft in periods of darkness and reduced visibility to allow pilots to keep track of the aircraft around them and distinguish between allied and axis aircraft [6]. Such signals still continue in use in navies today, especially useful in periods of radio silence or in an electronic warfare environment. Still these lightwave communications systems have the same reliability issues as the fire signals of the ancient Greeks, where weather, human error, and low data rates limit the usefulness.

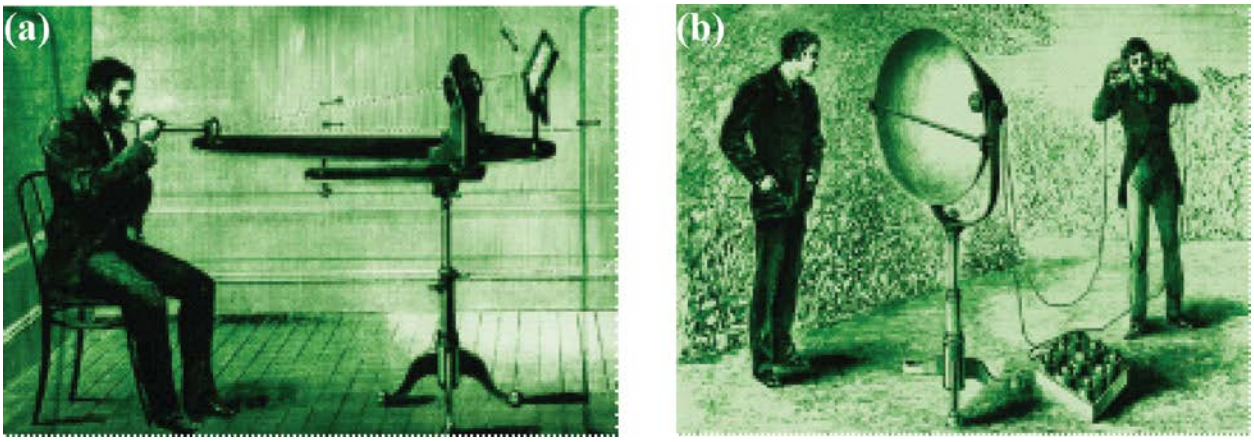

Figure 1.1 (a). Image of the photophone transmitter and (b) receiver invented by Alexander Graham Bell in 1880. Compared with the telephone, the device was large and was dependent upon appropriate weather conditions.

The invention of the telegraph in 1836 was a major step in information technology, opening up the ability to transmit complex messages in real time over vast distances, and allowing people across the country communicate directly [7]. A skilled operator could transmit data at rates up to 15 – 20 words per minute [8]. The invention of the telephone in 1875 [1] took this a step further, allowing voice to be transmitted over wire for the first time, again a major leap in data transmission. During this same time period, light again was studied as a method to transmit data, when Alexander Graham Bell invented the photophone in 1880 [1], only five years after his first

demonstration of the telephone. Like the telephone before it, the photophone was capable of transmitting voice data but by using light instead of wire. The photophone was demonstrated by transmitting voice from the roof of the Franklin school to the window of his laboratory over 250m away [9]. Despite Bell's success, his invention was met with a particularly scathing editorial in the New York Times on 30 August 1880 [10]:

> "The ordinary man…will find a little difficulty in comprehending how sunbeams are to be used. Does Prof. Bell intend to connect Boston and Cambridge…with a line of sunbeams hung on telegraph posts, and, if so, what diameter are the sunbeams to be…?...will it be necessary to insulate them against the weather…?...until (the public) sees a man going through the streets with a coil of No. 12 sunbeams on his shoulder, and suspending them from pole to pole, there will be a general feeling that there is something about Prof. Bell's photophone which places tremendous strain on human credulity."

With the technology still not there for reliable transmission using light, the photophone was forgotten over the far more reliable and successful telephone. However, now, over one hundred years later, we can answer many of the derisive questions posed in the editorial. Although our line of sunbeams will not be hung on telegraph posts, they will be strung underground, and yes they will be insulated against weather. The vast majority of the sunbeams will have a diameter ~9 μm, the diameter of standard single mode fiber [11], and although we don't see a man going through the streets with a coil of No. 12 sunbeams on his shoulder and suspending them from pole to pole, we do see men with fiber reels installing them under our city streets, inside our buildings, and even in between our servers.

So how did we make this jump from what the editorial calls placing a strain on human credulity to now being so common we think nothing about it, and what drove us to use

'sunbeams' instead of electricity, and finally where are we going? The second question is easy to answer, it is all about bandwidth and long distance transmission. The ever increasing demand for information has required greater and greater bandwidth to get there. These beams of light, are now capable of transmitting terabits of data over hundreds of kilometers [12,13]. Figure 1.2 illustrates the benefits of fiber optic communications, showing associated loss in dB/km *versus* frequency for telephone through fiber cables. The benefits of fiber are exceedingly clear, but the 'jump' to get there was not easy.

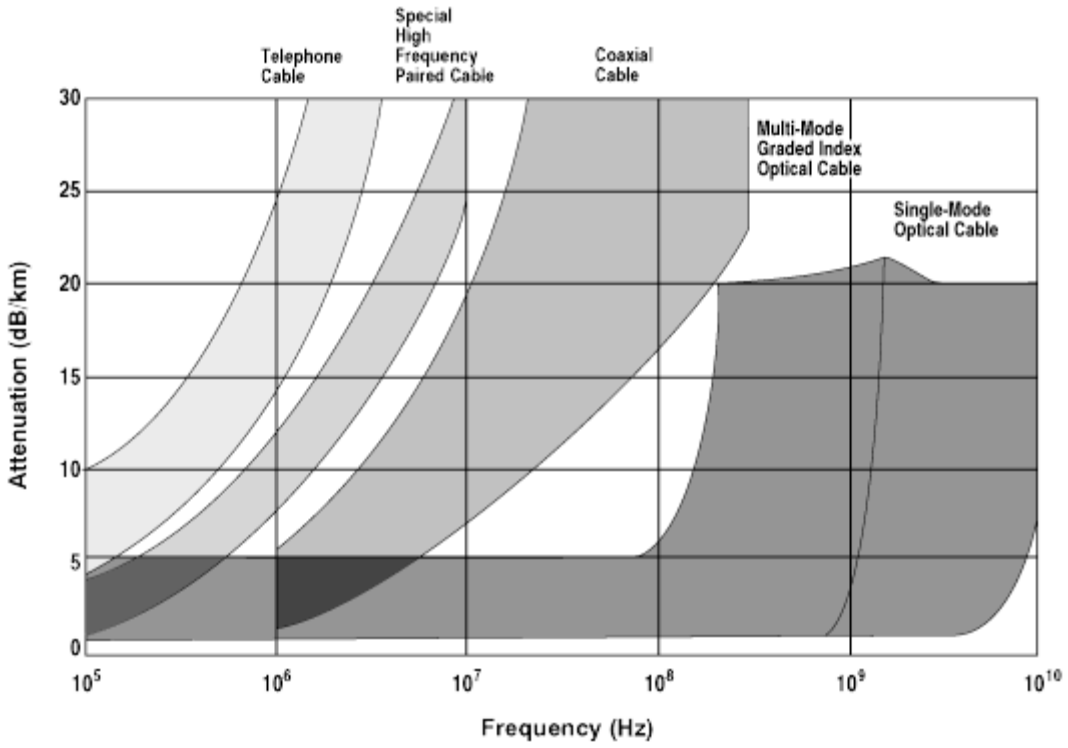

Figure 1.2. Coaxial *versus* Optical Fiber Attenuation *versus* frequency for multiple types of coaxial cable and both single and multimode fibers operating at varying wavelengths. Graph from [14].

Two technological hurdles needed to be reached prior to lightwave communications reaching maturity. First, we needed to be able to reliably create 'sunbeams,' in a manner such that we can modulate them, direct them, and contain them, and then we needed to be able to transmit those 'sunbeams' in a suitable medium. As the ancient Greeks (and perhaps Alexander Graham Bell

as well) had discovered, transmitting through air was not the most reliable medium, so an alternate method was needed.

The problem with the 'sunbeams' was solved with the initial demonstration of the laser in 1960 [15], a coherent source of light with a narrow bandwidth was capable of being modulated, directed, and contained (based on the process of total internal reflection which was documented in 1870). With a reliable light source and a way to guide it, there was a renewed interest in lightwave communications. Again, another hurdle was discovered, as existing glasses suitable for guiding had losses ~1000dB/km [1], making it impossible to transmit light data over any appreciable distance. Then, in 1966, Charles K. Kao and George Hockham of STC Laboratories in Harlow England proposed that low loss fibers could be fabricated by removing the contaminates in glass [16], spurring research towards that ends. Soon after, Corning Glass Works was developing fibers with losses ≈ 20 dB/km [17]. Finally, in 1977, General Telephone and Electronics transmitted live telephone traffic through fiber optic cables in Long Beach, CA [18].

Decades later, fiber optics dominate long haul communications and has been the backbone of the information age, allowing information to be transferred around the world at unheard of speeds from any time period in human history. With the conquest of worldwide communications, engineers started find applications at ever smaller scales, including local area networks (LANs) and metropolitan-area-networks (MANs), and even making its way to fiber to home applications [19-22].

This trend towards increasingly smaller scales ultimately leads to chip scale photonics where light is envisioned transferring data between CPUs, with optical waveguides replacing the venerable copper interconnects, providing greater bandwidth at lower energies [23-26]. This

increase in aggregate bandwidth between CPU cores is essential for continued increase in computation power [23-26]. In the past, processing power increases were accomplished with clock-frequency-scaling, but as clock-frequency-scaling has reached its limits, chip makers are turning to multiple core systems to increase computational power [23-26]. However, full realization of the potential of multiple core systems rely on the ability to transfer data from one core to another, and the wire interconnects currently used drastically increase signal attenuation and power dissipation with the increased data rates necessary [23-26]. With the parasitic losses in metallic interconnects limiting the speed of data transfer, optical links provide a path forward for high-capacity on-chip communication networks [23-26], allowing for the continued increase in computational power.

To make this move from global to chip scale, designers had many challenges to overcome including finding a suitable platform capable of such chip-scale integration. With fiber optic technology (essentially SiO_2 waveguides) unsuitable for large chip-scale integration, researchers turned to other materials with desirable optical qualities and the concept of the photonic integrated circuit (PIC).

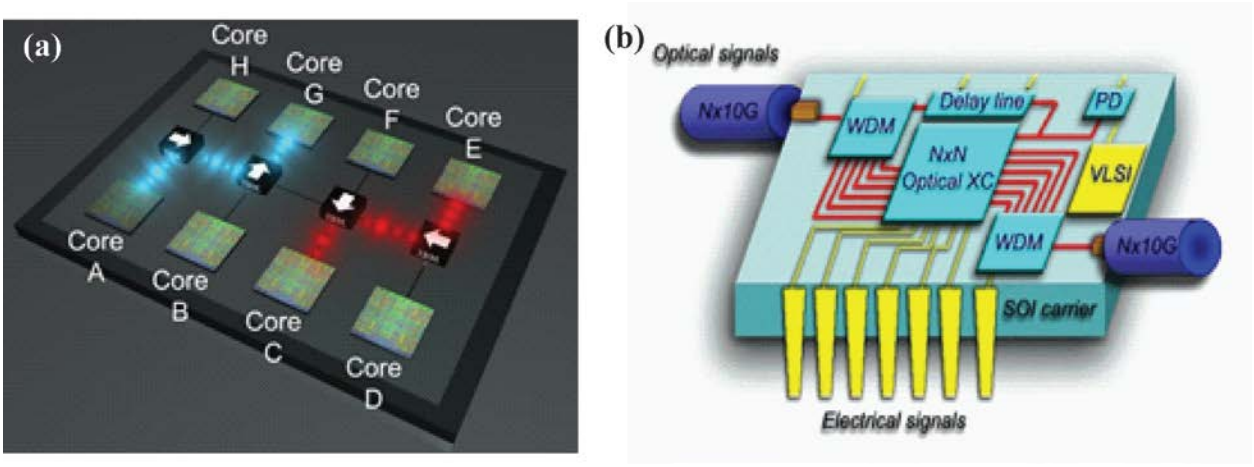

Figure 1.3 (a). IBM concept image of a multicore processor with optical data routing between cores [27,28]. (b). IBM concept of a switching PIC capable of routing optical data between cores as shown in concept sketch [28].

The PIC is essentially the analog to the integrated circuit, where discrete optical devices are fabricated on a single chip to create an integrated system. Figure 1.3(b) shows a concept of a silicon photonic integrated circuit by IBM which performs all optical routing of multiple channels, each supporting 10 Gbps [28]. It is envisioned that such a chip could be used to transmit data between CPU cores as shown in Fig. 1.3(a). With a wide open selection of materials to choose from, multiple platforms for photonic integrated circuits have been explored including InP [19,29-31], $LiNBO_3$ [19,32], and GaAs [19,33-37], with many leading to important devices used in optical communication systems today as modulators, transmitters, and receivers [29-32,34,36]. Despite many different promising aspects of these materials, they all face fabrication challenges and integration issues with today's silicon based integrated circuit infrastructure [19]. An ideal platform would not only have excellent optical properties, but would also be low-cost, easy to fabricate, and could fit in with existing integrated electronics.

1.2 Silicon Photonics

In 2012, IBM announced a technology breakthrough in which they integrated optical components side-by-side with silicon transistors on a single silicon chip using standard 90 nm semiconductor fabrication [38] as shown in Fig. 1.4. With this technology, wavelength division multiplexers (WDM), modulators, and detectors can all be integrated on a single silicon chip along with CMOS electrical circuits [38], allowing for a single-chip optical communication transceiver to be fabricated in a CMOS foundry rather than from an assembly of multiple parts made with other semiconductor technologies [38]. With data rates as high as 25 Gbps [38] and WDM capability [38], this technology brings IBM one step closer to achieving the concept of optical routing of data between CPU cores highlighted in Fig. 1.3. This is just one example of

where silicon photonics is headed, but numerous additional companies are working in this area including Intel, Luxtera, and CISCO [39-41] to name a few.

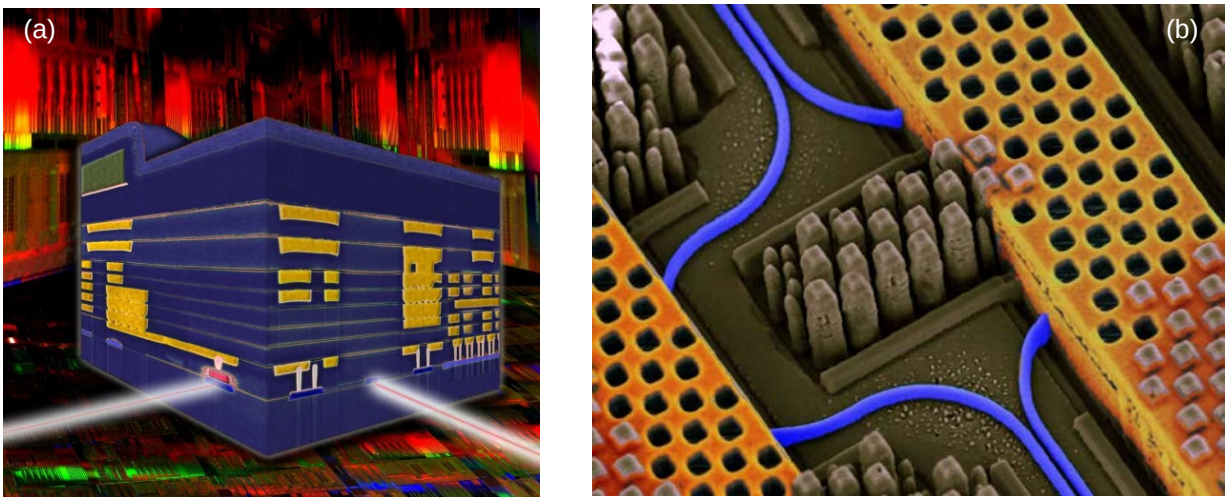

Figure 1.4 (a). Device render featuring a photodetector (red feature on left side of the cube) and modulator (blue feature on right side of the cube) along with silicon transistors (red sparks on the far right of cube) integrated on a single silicon chip. [38] (b). Angled view of chip with the optical waveguides highlighted in blue and high speed copper electrical interconnects highlighted in yellow [38].

Although silicon photonics can be traced as far back as the 1980's with the research done by Soref and Bennet [42], it wasn't until recently that silicon photonics truly emerged as a leading technology. In the last decade, silicon photonics has grown from mainly waveguides, switches, and modulators in the 1980s to everything from arrayed-waveguide-gratings to Y-junctions, capable of performing a wide range of functions, and new devices being demonstrated every day.

There are numerous benefits to using silicon as a platform for photonic integrated circuits, with perhaps the most compelling being the already intact infrastructure for growing, processing, and manufacturing silicon devices and the most important being its optical transparency at telecom wavelengths and beyond (1.1 μm – 10 μm [43]). Silicon as a high index of refraction of material also has the added benefit of extremely tight confinement of light, allowing for sub-wavelength waveguides on the scale of λ/n. This tight confinement results in smaller cross-sectional areas for waveguides, with common waveguide dimensions of ≈ 400 nm high by 200

nm wide [44], and tighter bends, with radii < 5 μm [44]. These sub-micron scale waveguides and tight bends are essential for minimizing overall footprint of silicon photonic devices, and produce other benefits due to their high field densities within the guides, particularly for non-linear applications as in [19, 45-56].

Despite these advantages and the significant number of both active and passive devices, there are still some inherent challenges, including the indirect bandgap nature of silicon, and its optical transparency at telecom wavelengths (both an advantage and disadvantage). While the transparency allows for the guiding of light, it presents challenges when trying to incorporate photodetectors.

1.3 Silicon Detectors

With a vast library of passive and active components, silicon photonic integrated photodetectors still present some challenges in terms of fabrication complexity and cost. Perhaps the greatest benefit of using silicon photonics is the CMOS compatibility, making a CMOS compatible detector, with no additional processing, either front or rear end, highly desirable. However, as seen in Fig. 1.5 [57], the bandgap of silicon limits photodetection to $\lambda < 1.1$ μm. To overcome this intrinsic limit, there are several competing technologies that can be integrated into silicon photonic integrated circuits, including Heterogeneous III-V material PDs, Ge on Si PDs, Graphene PDs, and Si Schottky barrier internal photoemission PDs.

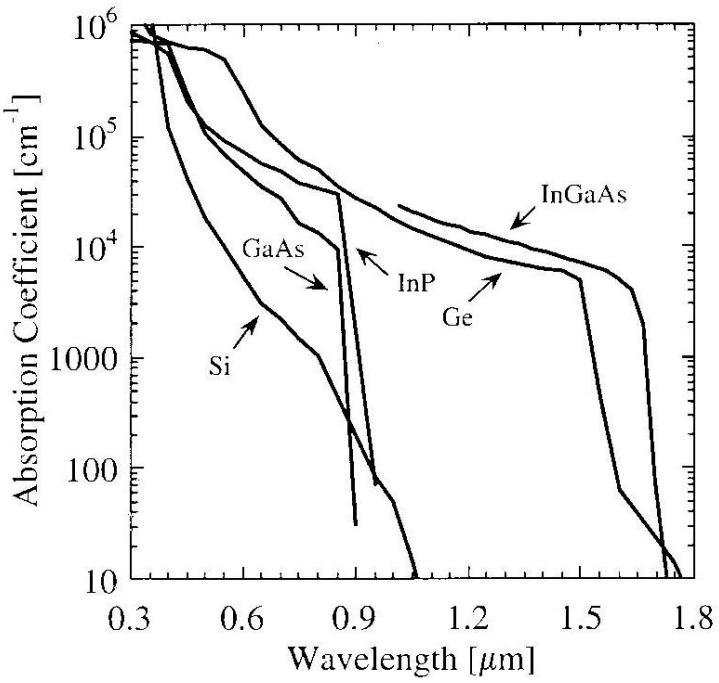

Figure 1.5. Absorption coefficient versus wavelength for several common semiconductor materials. The relatively high bandgap of 1.1 eV in silicon limits detection to wavelengths less than 1.1 µm, while smaller bandgap materials such as Ge and InGaAs have photodetection beyond 1.6 µm, making them suitable for telecom wavelengths. Image from [57].

1.3.1 Heterogeneous PDs

Heterogeneous PDs are usually comprised of a III-V semiconductor PD integrated onto a silicon platform, where the direct bandgap and the low bandgap energy of the III-V material allow for detection beyond 1.55 µm [58]. The wavelength range of these detectors can even be stretched beyond standard telecom wavelengths, into the long mid-infrared regime utilizing quantum-dot and quantum-well structures [58], making them suitable to areas such as chemical sensing, medical imaging, and surveillance [58].

These detectors are capable of extremely low dark currents on the order of pAs, and responsivities as high as 1 A/W at 1.55 µm [59]. However, due to the large lattice mismatch between the substrate material (usually GaAs) and silicon, integrating these into a CMOS fabrication process has been challenging [58,59]. It's only been recent that multiple groups have

demonstrated the ability to integrate these detectors in a CMOS fabrication process by using an InGaAs detector along with a divinylsiloxane-bisbenzocyclobutene (DVS-BCB) adhesive die-to-wafer bonding process [59]. The DVS-BCB layer is placed over a silicon waveguide etched onto an SOI platform and a grating coupling in the waveguide directs the light vertically into the bonded detector, completing the connection between the silicon waveguide and the InGaAs PD [59].

1.3.2 Si/Ge PDs

An alternate to the heterogeneous approach is by growing Ge or Si/Ge on Si. Although Ge also has an indirect bandgap similar structure to Si, its lower bandgap energy of 0.7 eV allows it to detect efficiently beyond 1.6 μm, making it attractive as a telecom wavelength PD. These detectors have been demonstrated with bandwidths greater than 40 GHz and responsivities as high as 1.1 A/W [59]. To form the detectors, Ge can be deposited on Si using chemical vapor deposition (CVD). However, a primary challenge with this approach has been the lattice mismatch between Si and Ge of 4.2% [60]. This lattice mismatch induces strain when growing a heteroexpitaxial layer of Ge or Si/Ge on Si [60], creating a significant number of dislocations for growth beyond a certain "critical thickness" [60]. These dislocations degrade performance through increased dark current and decreased responsivity [60].

To incorporate these detectors into a CMOS fabrication process, a "front end of the line" process is utilized where Ge epitaxy is inserted between steps of polygate formation and contact metallization [58]. Recently Luxtera and MIT, using 130 nm and 150 nm technologies, respectively, have demonstrated this technique to integrate Ge PDs in a CMOS compatible manor [58].

1.3.3 Graphene Detectors

Multiple graphene devices have been demonstrated, including PDs, modulators, polarizers, and saturable absorbers [61,62]. Its two dimensional structure, extremely high electron mobility, and its extremely large absorption of light over a vast bandwidth, where a single monolayer absorbs 2.3% of incident light [61], make it ideal for PDs. Graphene photodetectors have already been demonstrated with responsivities ranging between 3.6 mA/W [61] to 57 mA/W [62] and frequency responses as high 10 GHz [61], with predicted capability beyond 100 GHz [62].

1.3.4 Schottky MSM

A final technique that requires no additional processing to be compatible with CMOS integration is the use of a Schottky barrier to allow sub-bandgap detection. These devices rely on the excitation of carrier across a metal-semiconductor junction Schottky barrier, which for a p-type Si, can be tailored from 0.2 – 0.6 eV depending on metal type and doping [58]. These detectors have been incorporated into silicon waveguide PDs and have been studied extensively [58,59,63]. They are able to achieve low dark currents (~ nAs), high speed (~ 150 GHz) [59], and are comparatively easy to fabricate, in a process that is CMOS compatible and requiring no additional processing steps. Additionally, these detectors can be also be utilized for mid-infrared detection like the III-V PDs as due to the ability to tailor the Schottky barrier to ~ 0.2 eV.

Their main drawback is that they suffer from very low quantum efficiency [59]. Researchers have been able to improve this utilizing surface Plasmon polaritons (SPP), as was done in [63], where a symmetric SPP Schottky contact PD was demonstrated with a responsivity of 0.1 A/W and dark current of 21 nA [58, 59, 63], but at the cost of increased fabrication complexity [59].

1.4 Scope of Work

All of the active PDs presented above have many advantages, but share (excluding the Schottky MSM PDs) the need for additional processing beyond standard CMOS fabrication steps [19]. An alternative detector type is based on defect-enhanced Si nano-wire-waveguides (NWWG) [64-82]. These detectors work based on Shockley-Read-Hall recombination theory, where sub-bandgap trap states associated with lattice defects or substitutional atoms in the lattice are optically active, allowing for photodetection beyond the bandgap of Si. These devices have been shown to have responsivities greater than 1 A/W [64], frequency responses ~ 35GHz [64], and dark currents of just a few nanoamps [64-66]. They have been shown to work in numerous applications including power monitoring [67], wavelength monitoring [68], thermal tuning [69], and variable optical attenuation [70]. They have the potential to be used as optical interconnects with data rates of 10Gb/s demonstrated at 1.55μm [71], and 1 Gb/s at 1.9 μm [72]. Additionally, with the exception of the graphene and Schottky barrier devices, the PDs listed above are limited to operation around 1.6 – 1.8 μm without utilizing exotic techniques such as bandgap engineering using super-lattices [83], whereas the defect enhanced detectors have demonstrated photodetection beyond $\lambda = 2.4$ μm [84-86] with the potential to go to 3.3μm and higher [87].

The scope of this thesis will describe our research done on defect-enhanced photodetectors, starting with Section I which discusses fabrication and implantation of the Si NWWGs used and includes a primer on SRH theory and its application to defect enhanced photodetection as in [88]. Section II will focus on PDs operating in the telecom regime, with Chapter 4 focusing on the design, simulations, and results of a Si-waveguide ion implanted Metal-Semiconductor-Metal (MSM) detector and Chapter 5 focusing on data rate experiments for *p-i-n* detectors implanted and annealed under different conditions at wavelengths of 1.55 μm. Finally, Section III will

cover longer wavelength operation of the implanted Si NWWGs, with Chapter 6 demonstrating error free operation of a Si^+ implanted Si NWWG PD at a wavelength of 1.9 μm and Chapters 7 and 8 characterizing devices for operation in the mid-infrared, with wavelengths from 2.2 to 2.4 μm.

SECTION I: FABRICATION AND ION IMPLANTATION

CHAPTER TWO:
Fabrication

2.1 Device Structure

Two types of diodes are used in this thesis, *p-i-n* diodes fabricated at MIT Lincoln Laboratories [64-66] and MSM diodes in fabricated at Brookhaven National Laboratories. Each set of diodes underwent similar implantation procedures as will be discussed in Chapter 3, and were tested using the same equipment under similar conditions, detailed in subsequent chapters. The general structure of the devices (both MSM and *p-i-n*) is shown in Fig. 2.1. The waveguides consist of two fan out tapers on each end utilized for coupling light onto and off of the chip. The couplers were then adiabatically tapered to a sub-micron channel waveguide clad with SiO_2 underneath and air all around, except for the waveguide mask which was SiO_2 for the *p-i-n* diodes and Hydrogen silsesquioxane (HSQ) for the MSM diodes. For the PD section of the device, the channel waveguide was adiabatically tapered into a rib waveguide with the 'wings' as shown in Fig. 2.1. The 'wings' allowed for carrier transport between the contacts, creating the electrical connection between the contacts and the PD. Following the device, the rib waveguide was adiabatically coupled back into a channel waveguide which was then adiabatically tapered into the wide coupler region.

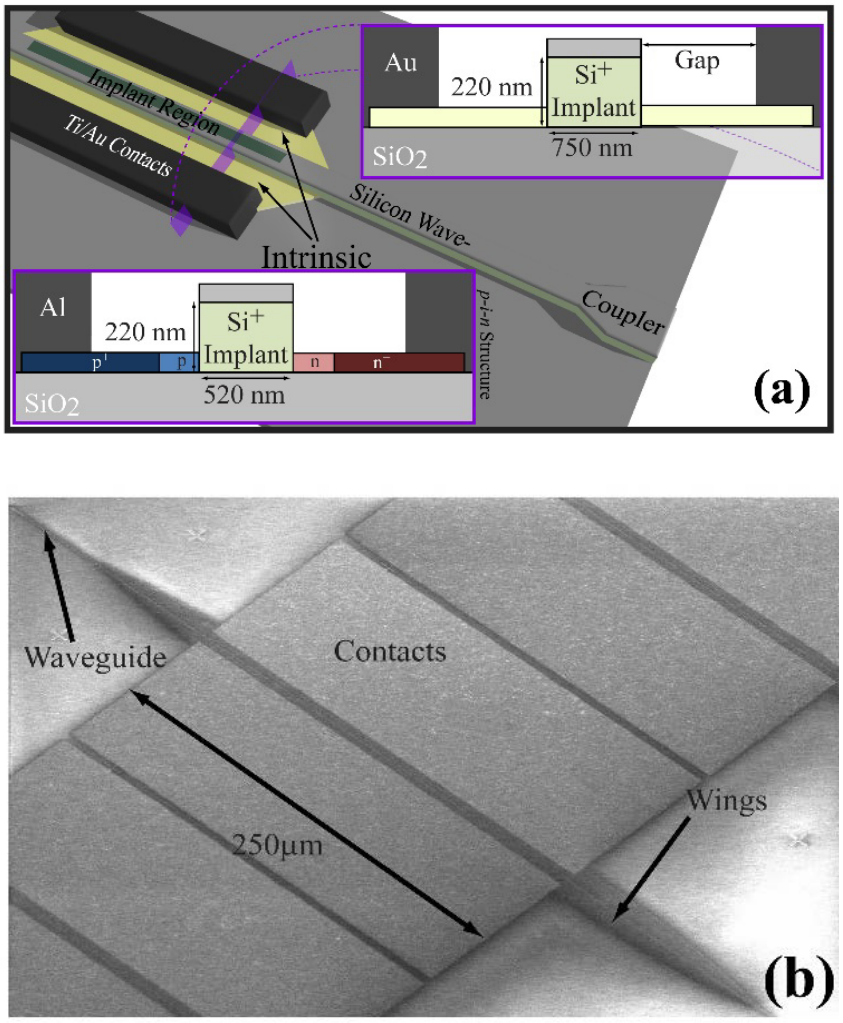

Figure 2.1. (a) Device cartoon for the MSM devices fabricated from 220nm Soitec SOI wafers [90]. The coupler region is shown at the edge of the chip, followed by an adiabatic taper into the waveguide. The waveguide is ion-implanted in the region with the 'wings' to create the photodiode. Waveguide dimensions for both the MSM and *p-i-n* devices are given in the insets, whereas wing height varied and is discussed in the individual chapters. (b). Scanning Electron Microscope (SEM) image of completed MSM devices.

2.2 Fabrication

2.2.1 Metal-Semiconductor-Metal PDs

Fabrication began with Soitec SOI [89] wafers which consisted of a 220 nm Si top layer followed by a 3 µm SiO_2 insulating layer and a 625 µm Si carry wafer. The 3 µm SiO_2 layer was key in ensuring no coupling of mode power to the substrate, especially at the longer wavelengths considered in this thesis. The top layer of Si had a resistivity of 10-20 Ω-cm with a slight *p*

doping of ~ 1×10^{15} cm^{-3}. Figure 2.2 (a) inset shows the layers of the initial Si wafer along with a top layer of HSQ used as a negative electron beam resist for defining the waveguides.

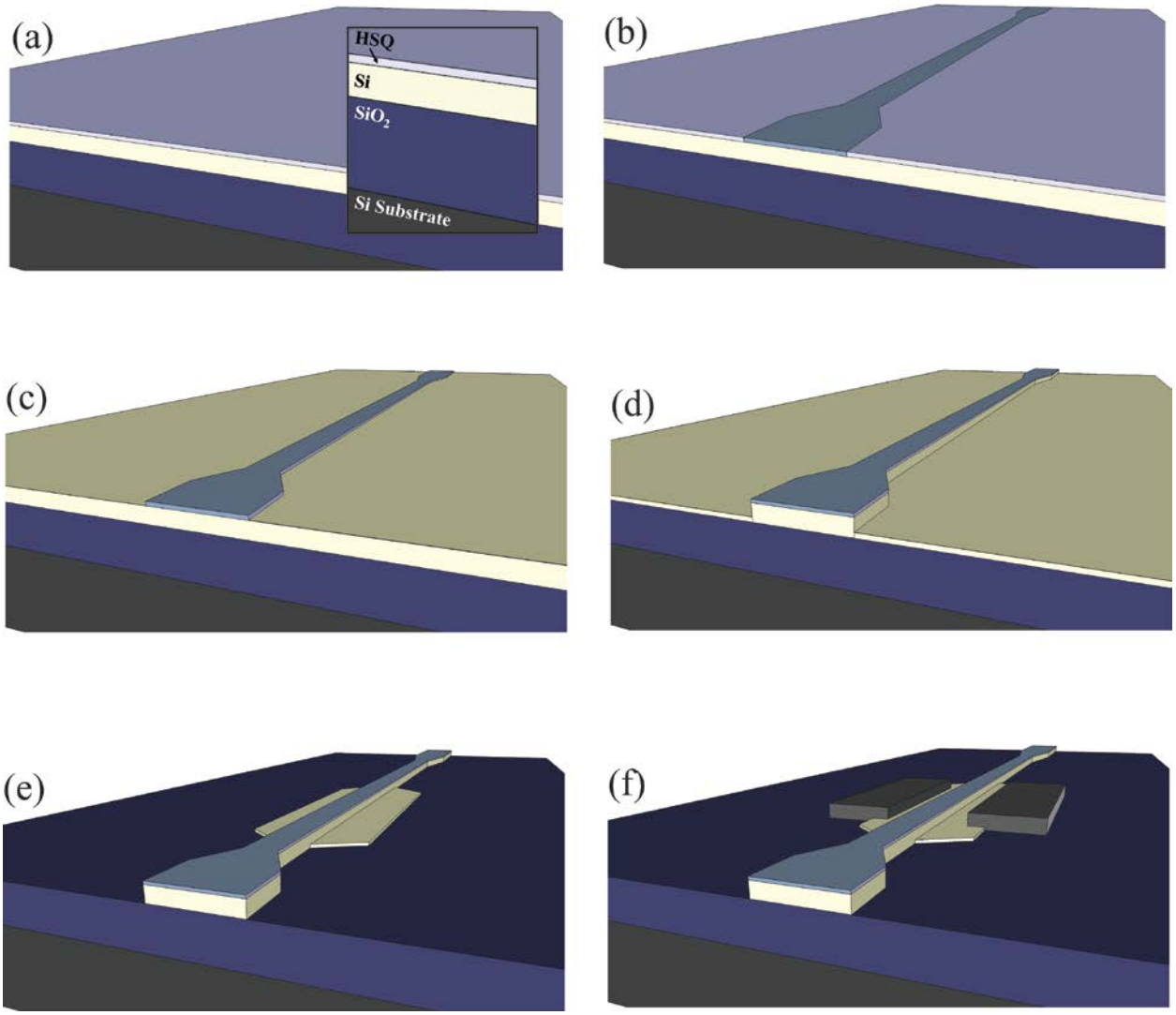

Figure 2.2 (a). Initial layers with the Si substrate followed by a 3 μm SiO_2 layer and then a 220 nm Si layer, topped with a ~90 nm layer of HSQ (not to scale). (inset) Labeled layers of the substrate after application of HSQ. (b). Pattern defined in HSQ after electron-beam lithography. (c). Development of HSQ leaves HSQ waveguide pattern over Si layer. (d). Initial etch of Si leaving a ridge of between 40 – 70 nm to be patterned to define the 'wings'. (e). After definition using S1811 (not illustrated) and etching, the waveguide is complete. (f). Final step in the process is the deposition of the metal contacts using S1811 as liftoff (not illustrated), resulting in the completed waveguide structure.

Prior to applying the HSQ resist, the wafers underwent a thorough cleaning process to ensure any particulates were removed and baked at high temperature to remove any moisture and prevent poor resist adhesion. The wafers were initially diced into ~ 1 cm x 1 cm pieces. The

pieces were then subject to three immersive baths with sonication for 5 minutes each. The initial bath was in acetone, followed by methanol, and then isopropanol alcohol. The sonication ensured the surface was free of fine particulates which could distort and add roughness to the nano-scale waveguides. Following the baths, the chips were dried using compressed N_2 and then subjected to a bake. The bake process was at 350˚C for 40 minutes to ensure removal of any surface moisture which would prevent good adhesion of the resist. Additionally, the chips then were subjected to an O_2 plasma clean at 100 W for 2 minutes and the application of a hexamethyldisilizane (HMDS) monolayer utilizing a Yield Engineering Systems HMDS oven [90].

After cleaning and the application of an HMDS layer, the chips were then spin coated with Dow Corning XR1541-006 at 4500 RPM for 45 seconds, resulting in a layer between 90-120 nm of HSQ [91]. XR1541-006 is a type of flowable oxide composed of a 6% concentration of HSQ [91], which provides excellent etch resistance and is ideally suited for use as a hard mask. Although HSQ requires an extremely high dose when compared to other electron beam resists such as ZEP [19], the fact that it is a negative resist, and thus only required exposure along the waveguide themselves, more than offset the exposure time increase due to the larger dose requirement. An additional benefit of the HSQ was its ability to make high contrast ratio structures resulting in nearly vertical waveguide sidewalls [19] and being able to produce repeatable and reliable pattern definitions [19]. Given the high index nature of Si, and the nano-scale size waveguides in which there exists a significant overlap between the field and the sidewalls, the Si NWWG properties are extremely sensitive to geometry, in particular to scattering losses induced from sidewall roughness. The HSQ process developed in [19] and followed and refined here allowed for sidewall roughness on the order of ~ 5nm or less [19].

After applying the resist, the chips were then baked at 80˚C for 4 minutes, ensuring all solvent was removed from the resist. Another N_2 blow dry was used to remove any stray particles prior to writing.

The pattern transfer was done utilizing a JEOL 6300FS electron beam lithography tool [92] with a 100 kV acceleration voltage, a 2 nm spot size and between 4 – 10 nA beam current. A laser interferometer state allowed for very accurate stitching (< 9nm) between write fields [92], again crucial given the sensitivity of the mode to waveguide roughness and the NWWG lengths of ~ 0.75 cm. The Layout BEAMER software [93] used to transfer the Graphic Data System (.gds) file containing the write pattern to the e-beam writer also featured Proximity Effect Correction, crucial for these waveguide structures, as the layer of HSQ acts as a charging layer causing distortion and/or deflections of the electron beam profile [93]. Figure 2.1(b) illustrates the pattern transfer into the HSQ after e-beam exposure.

The chips were then developed utilizing a "salty" developer. The salty developer consisted of a mix of 1% NaOH to 4% NaCl in de-ionized (DI) water. The salty developer was critical in creating a high contrast mask [19,94]; key to making the near vertical and low roughness sidewalls necessary for low loss propagation in Si NWWGs. Previous research showed an unintended effect of the development process where particulates would remain on the chip after the rinse and give way to Si pillars after etching as shown in Fig. 2.3 [19]. To alleviate this, the chips were subjugated to a series of sonication steps during development. Initially the chips were placed in a bath of salty developer and sonicated for 5 s. They were then immediately removed from the bath and then placed in a second bath of salty developer. They again were sonicated for 5 s and then remained in the second bath for 10 minutes to ensure full development. After the second bath of salty developer, they were then placed in a stop bath of DI water,

sonicated for 2 s, and remained in the stop bath for another 10 minutes. The addition of the sonication virtually eliminated the stray particles landing on the chip seen in Fig. 2.3 [19].

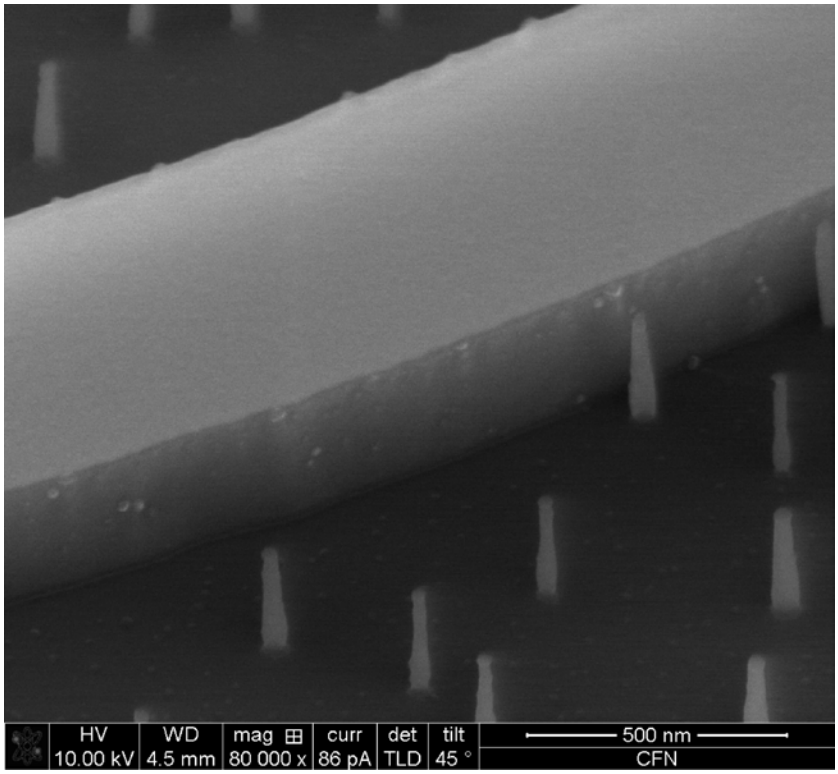

Figure 2.3 SEM image of Silicon NWWG along with pillars resulting from incomplete removal of particles during the development process. Image from [19].

Previously two separate etching processes were developed for the SOI wafers, one consisting of a cryogenically cooled process at -100˚C of SF_6/O_2 [19] and the other of HBr/Cl at 20˚C [19]. For this work, the HBr/Cl etch was used exclusively due to its near room temperature operation, reducing overall processing time, and more importantly due to its slower and more controllable etch rate, allowing for the creation of the 'wings' as shown in Fig. 2.1 and 2.2. Although the etch rate was consistent during sessions, there were some inconsistencies noted between sessions, requiring recalibration prior to each initial etching of the waveguides. These inconsistencies are likely related to small amounts of contaminants left over from other processes, but this has not been exhaustively tested yet. To achieve the desired wing thickness of

~ 50 nm, an etch time of ~ 75 – 90 s was needed, resulting in 'wing' heights of 40 – 70 nm for the fabricated waveguides, with devices tested having 'wing' heights ~ 60 nm.

After initial etching, leaving a rib waveguide structure over the entire chip as shown in Fig. 2.2(d), the wings were defined utilizing a second pattern and etch. The second pattern consisted of an 16 μm wide x 250 μm – 3mm long rectangular section centered on the Si NWWG with the addition of an linear adiabatic taper of 100 μm at each end as shown in the Fig. 2.2(e). Photolithography was used for this portion due to lower required tolerances and the relative ease of photolithographic process after initial mask creation. Although an adiabatic taper was used, simulations showed the scattering loss between an adiabatic taper and no taper for the wings of 50 nm height was negligible. To enhance adhesion of the photoresist, the chip was treated again in the YES HMDS oven, creating a HMDS monolayer prior to spin coating. Following the adhesion layer, ma-N 1410 resist was spin coated on at 3000 RPM for 30 seconds to create a roughly 1 μm thick layer of resist. After spinning, the resist was baked on a hot plate for a period 90 s at 100˚C. The resist was then exposed utilizing a MA-6 mask aligner to a dose of 300 mJ/cm^2, and developed in ma-D 533 for 40 s followed by a stop bath in DI water for 30 s.

Following development of the mask, the chips were again etched utilizing the HBr/Cl etch as above for a period of 1 minute to ensure the final layer of Si was completely removed, and leaving the desired waveguide structure with the wings in the soon to be PD portion of the devices as shown in Fig. 2.2 (e).

With the waveguide, 'wings,' and coupler structures defined, the final step prior to implantation was contact deposition. The contact mask was also defined using photolithography and the MA-6 mask aligner. For the devices presented in Chapter 4, a positive mask utilizing Shipley 1811 photoresist was used to define the contact regions with two different contact

separations were utilized (2 μm and 4 μm) to test both the alignment process and lift-off process. The resist was spin coated at 4000 RPM onto the chip, following an O_2 plasma clean for 2 minutes after the final silicon etch and an application of HMDS as above. The S1811 was exposed to a dose of approximately 60 mJ/cm^2 and developed in MF319 for a period of 20 s, followed by a stop bath of DI water for 15 s.

After development of the mask, the contact metal was deposited using a Lesker 75 PVD system utilizing electron beam evaporation [95] and a deposition rate of 0.5 – 1 Angstrom/s. After metal deposition, lift-off was performed using a warm bath of Microposit® 1165 remover at a temperature of 80˚C resulting in the final device structure as seen in Fig. 2.2(f). Of the two different contact separations, the results from the 2 μm separation were unsuitable, as the lift-off failed between the contacts, leaving shorts across the waveguide. The 4 μm contact separation mask provided cleaner results, but during liftoff sonication was used to assist in the removal of some of the unwanted metal resulting in fine particles as seen in Fig. 2.4(a). At lower voltages, these particles did not impact performance, however at the higher voltages, the particles would collect on the sides of the waveguide as seen in Fig. 2.4(b), causing shorts, and limiting experimental results to a reverse bias of voltage 50 V.

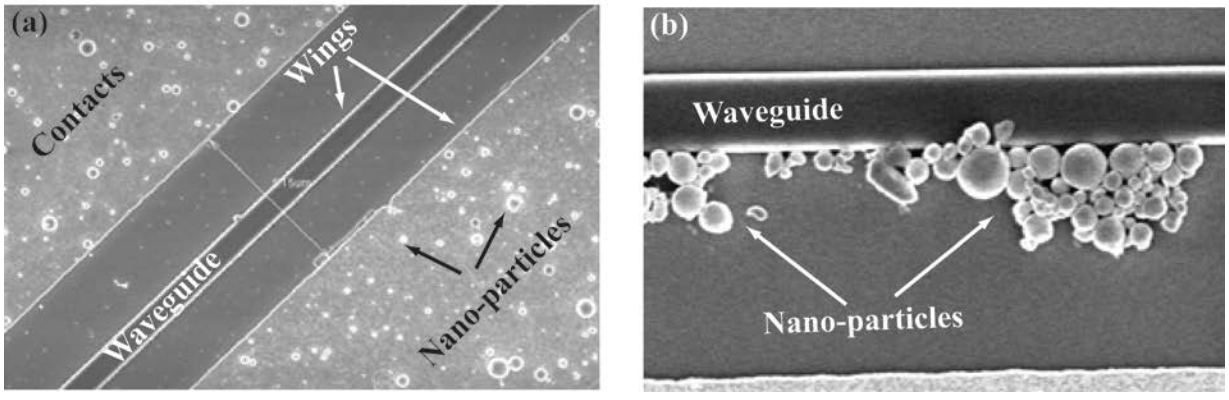

Figure 2.4 (a) SEM top view image of waveguide and contacts. A significant number of nano-scale particles can be seen on top of the contacts, believed to be left over from the lift-off and caused by sonication. (b). After performing

tests on the devices, the nano-scale particles would collect on the sidewalls of the waveguide, leading to device failure at higher voltages.

Although S1811 is often used in liftoff, it's non-vertical sidewalls allows for the creation of a near conformal layer of the metal, degrading lift-off, especially at the scales tested. Alternative methods include using dual layer techniques [96-98] or by using ma-N 1410 [99]. When over-exposed, ma-N 1410 creates an under-etch, preventing this non-conformal layer [99], and allowing for clean lift off at smaller scales. Initial tests show that the limit of alignment using the ma-N 1410 resist with the MA-6 mask aligner allows for contact separation ~ 2-3 μm, enough to reduce bias voltage by approximately one-half and increase frequency response. To further reduce bias and increase frequency response, the contacts need to be brought to within 1.5 μm of each other, or approximately 0.425 μm from the edge of the waveguide, which is discussed further in Chapter 4. To reach this level of precision, a dual layer PMMA resist can be used in conjunction with the JEOL 6300 EBL machine [97].

The final step in the fabrication of the MSM PDs was ion implantation. Ion implantation was completed at the Ion Beam Laboratory at the State University of Albany under the conditions discussed in the Chapter 3. Prior to implantation, an ion implantation mask was made again using photolithography and the MA-6 mask aligner at BNL. Shipley 1811 photoresist was used for its thick coating, to ensure the implantation only implanted desired areas. The windows for the implantation varied in length from 250 μm to 3mm, and were 8 μm wide to allow for easy manual alignment. However, this wide window resulted in implantation of the wings as well, likely altering electrical properties, reducing mobility and increasing resistance based on evidence presented in later chapters. After implantation, the chips were then cleaved to expose the coupling region as shown in Figure 2.5 below. Coupler design is discussed further in Chapter 4.

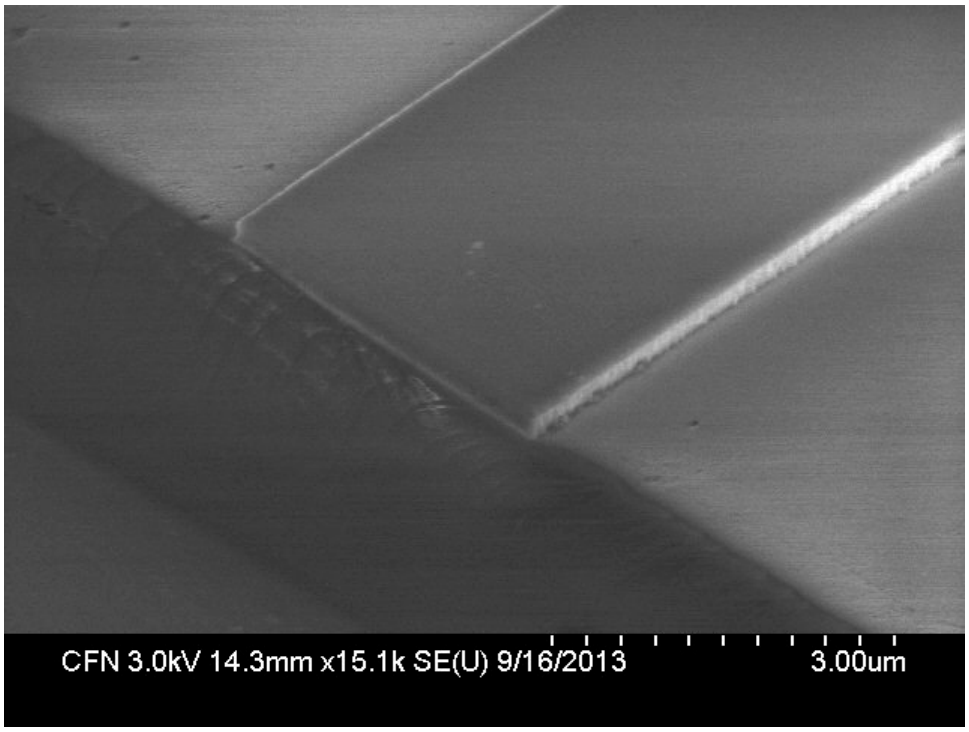

Figure 2.5 SEM image of cleaved facet showing the fan out coupler.

2.2.2 p-i-n Device Fabrication

The *p-i-n* devices in Chapter 5 were fabricated at MIT Lincoln Labs as described in [64,65]. The Si waveguide channel was 520 × 220 nm with 50 nm high 'wings' for the electrical connection to the contacts [64,65]. The 'wings' were doped with concentrations of 10^{19} cm^{-3} and 10^{18} cm^{-3} for the p^+, n^+ and *p*, *n* regions respectively [64,65], with the p^+, n^+ regions used for good electrical contact with the contact pads. The devices were then masked and subsequently ion-implanted with Si^+ at an ion energy of 190 keV [64,65] with the implantation window limited to within 10's of nms of the waveguide [64,65]. Following implantation the devices were subjected to a maximum temperature of 475˚C for two minutes, annealing the ion implanted devices [64,65], creating interstitial cluster defects as discussed in Chapter 5. Coupling onto and off of these devices was accomplished through 5 μm wide fan-out tapers at the device edges [64,65]. These devices were tested for frequency response and data rate in Chapter 5.

Alternatively, the *p-i-n* devices used in Chapter 6 were fabricated as described in [66]. Again, the Si waveguide channel was 520 × 220 nm with 50 nm high 'wings' for the electrical connection to the contacts and doped as above [66]. The devices were then masked and subsequently ion implanted with Si^+ at an ion energy of 190 keV [66] with the implantation limited to within 10's of nanometers of the waveguide [66]. However, a thermal oxide layer was not grown, and the devices were exposed to a maximum temperature of only 300˚C for a period of 60 s [66]. The lower temperature limited annealing of the divacancy defect as discussed in Chapter 3. Following implantation contacts were placed consisting of a 300 nm layer of Al on top of a 10 nm W adhesion layer [66]. Coupling onto and off of the chip was accomplished through 5 μm fan out tapers at the edges [66].

A final set of *p-i-n* devices were fabricated as in the paragraph above and [66], however, ion-implantation was not done. These devices were ion-implanted at the IBL with Si^+, Ar^+, and Zn^+, creating different defects and trap states as discussed in the next chapter, and were used in chapters 7-8. The ion implantation process for these devices followed the procedures outlined above for the MSM devices and presented in Chapter 3. As with the MSM PDs, the implantation region was no longer limited to the waveguides, possibly altering key diode characteristics as discussed in Chapter 3 and later chapters.

CHAPTER THREE:
Ion Implantation

A major experimental component in this thesis – in fact an "experimental enabler" – is that of ion implantation. This technique enables insertion of the desired impurity ion via acceleration using a high voltage source. This chapter summarizes the method, the instrumentation, and the materials physics of this process.

Our ion implantation step was completed at the Ion Beam Laboratory at the State University of Albany utilizing their 400 keV Varian (Extrion) 400-10A Implanter. Multiple ion species were used for implantation, including Si^+, Ar^+, and Zn^+, and were implanted at energies ranging from 180 – 280 keV, allowing for tailoring of the ion implantation depth and damage profiles in the waveguides.

3.1 Ion Implanter Operation

An illustration of the workings of the ion beam implanter is shown in Fig. 3.1 [100]. An ion implantation setup generally consists of an ion source, an extractor, an analyzer, and an accelerator followed by the target.

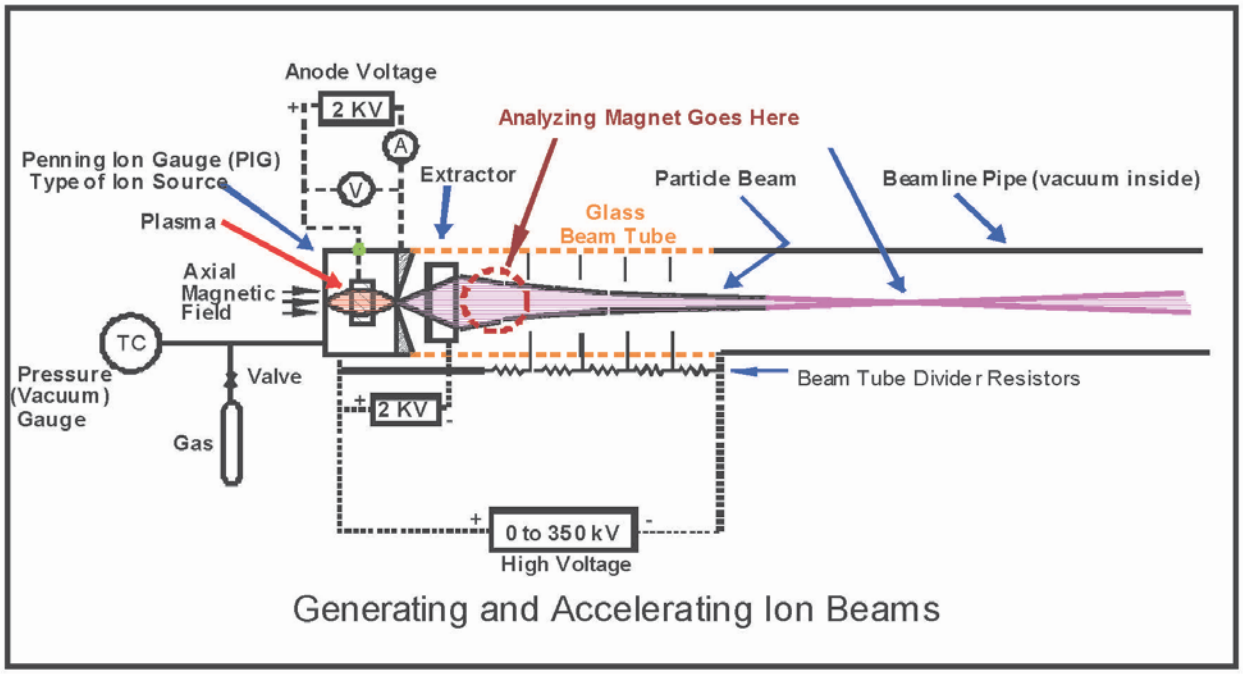

Figure 3.1 Illustration of the ion implanter used at the IBL facility in Albany. Illustration provided by [100].

A Penning Ion Guage (PIG) ion source, named after the inventor of a vacuum gauge similar to the ion source, was used to provide the ions [100]. To achieve ionization of the neutral atoms, a small chamber in the source is filled with the desired neutral atoms either in the form of an atomic or molecular vapor. In the center of this chamber is a small charged cylinder (anode), biased to ~2000 V as referenced to the end walls of the chamber (cathodes) [100]. Electrons accelerated towards the anode from the cathodes collide with the neutral gas, stripping away an outer shell electron on the atomic species of choice [100]. Subsequently the original and ionized electrons continue towards the anode with the possibility of additional collisions to create more ions and creating a cascading effect [100]. The ionized atoms are concomitantly accelerated towards the chamber walls in the opposite direction of the electrons due to their positive charge [100]. A small aperture at one end of the chamber provides an escape path for the ions, as shown in Fig. 3.1. After exiting the ion source, an extractor then accelerates the ions away from the exit and towards the analyzer magnets (as shown in red in Fig. 3.1).

Gas density plays a critical role in the operation of the ion source, as ionization events are reduced if the density is either too low or too high [100]. If the density is too low the collision probability is reduced due to fewer atoms in the chamber. On the other end, if the density of the gas is too high, the mean time between collisions of an ion with an atom decreases, decreasing the energy of the electron to a point where it is insufficient to ionize the atom [100]. Note that even with the gas density optimized, this is a very inefficient ion source [100]. To enhance performance, a magnetic coil is wrapped around the source creating an axial magnetic field [100]. This magnetic field directs the electrons and ions to spiral around the field lines, increasing path length and thus the probability of collision with neutral atoms [100]. To prevent a runaway of the electric current, the anode power supply is connected in series with a resistor. As the plasma current increases due to increased ionization, the anode voltage drops, stabilizing the system [100].

In order to create ions from solids, such as the Zn^+ used to implant some of the devices in this work, the (typically) metal is placed around the exit aperture in the chamber (possible due to the vertical mounting of the ion source in this setup). The chamber is then operated as above, with the ionized gas particles accelerated towards the exit aperture. The ions that are not aligned with the aperture collide with the metal target material around the aperture, thus sputtering the metal into the chamber. These sputtered metal atoms are then ionized as well, and then accelerated towards the exit aperture. In the present work, Ar was ionized and used to sputter the Zn to create the Zn^+ ions. Another class of ions is created from molecular gases. For example, instead of using bulk Si for implantation, a gaseous molecular compound such as of SiF_4 is used for Si^+ ions. The gaseous molecules are dissociated in the plasma and ionized, eliminating the need to

sputter off of a solid target. Note that the ionization reactions used in this work are provided below:

(3.1)

$$Si + e^- = Si^+ + 2e^- \quad (3.1)$$

$$Ar + e^- = Ar^+ + 2e^- \quad (3.2)$$

$$Zn + e^- = Zn^+ + 2e^-. \quad (3.3)$$

An extractor and the analyzer follow the ion source. Whereas the extractor ensures the ions clear the ion source, the analyzer uses a magnetic steering field to separate ions of different energy and different atomic weights, steering the undesired ions out of the primary ion stream. The ions of different energies are created through different degrees of ionization, as a single ion can become doubly or higher charged (up to charge 5 or higher for heavy atoms) through multiple collisions between the ions and electrons in the plasma. The different charged ions then exit the chamber with different energies for each charge. Different atomic weight ions are seen when sputtering a solid source or when using a molecular gas, such as is the case for Si^+ and Zn^+ implantation. Again, these different atomic weighted ions exit the chamber and are sorted by the analyzer.

As an example, Fig. 3.2 shows the mass spectrum output of the Extrion ion beam for both Si^+ ion and Ar^+ ion implantation. In the case of the Si^+ implantation, the Si peak is well defined, along with a peak for F, a component of the SiF_4 gas used for the Si^+ source. An additional peak is seen for Ar, likely due to some residual gasses in the chambers. For the Ar^+ source, again the peak is clear, with only one other peak for N_2, likely remnants of purging the system. These undesired ions are steered away from the main beam line by the analyzer ensuring only the desired Si^+ and Ar^+ impact the target wafer during implantation.

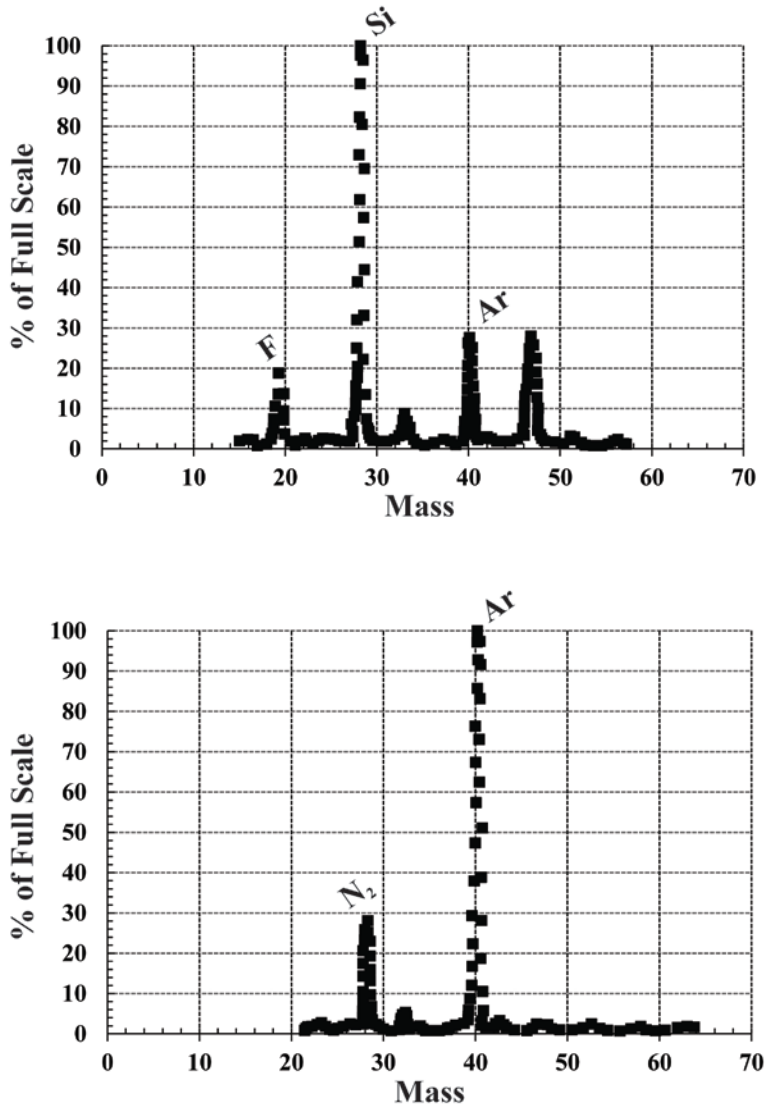

Figure 3.2 (a) Mass spectrum analyzer output for the Si implantation, with the Si and F peaks clearly visible along with a residual Ar peak. (b) Mass spectrum analyzer output for the Ar implantation, with the Ar peak clearly visible, along with a residual N_2 peak.

An additional acceleration stage is placed before the ions impact the target. The voltage of this acceleration stage can be set from 0 to 350 kV, creating ions of energy of 50 – 400 keV (based on an extractor voltage of 50 kV). The final accelerated ions are passed through an aperture and scanned across a 2 in x 2 in area containing the target material.

The ion beam current and diameter were used to measure dose based on the following equation:

$$\Phi = I \cdot t \Big/ e \cdot A \tag{3.4}$$

where Φ is the dose measured in cm^{-2}, I is the beam current, e is the electron charge, and A is the beam area. The current density (I/A) for implantation ranged from ~ 2 – 15 nA/cm^2, resulting in implantation times ~ 5 – 20 minutes for the majority of the devices presented in this work.

3.2 Types of defects

The process of ion implantation has long been known to create a variety of defects in a silicon crystal lattice, depending on ion energy, ion species, annealing temperature, and dose. These defects are created via nuclear interactions and are due to the fact that the ion energy exceeds the atomic binding energy in the solid. Several different defect classes are highlighted in Fig. 3.3. For this research, the target material consisted of a Si NWWG, and the implantation consisted of Si^+, Ar^+, and Zn^+ ions. During implantation, the ions enter the crystal lattice and collide with Si atoms in the lattice. With sufficient energy, the ions can displace a Si atom from its lattice site, creating a vacancy defect and a Si interstitial defect as shown in Fig. 3.3(b). Depending on the target ion species and energy, the target ion then can then become an interstitial impurity, or in the case of both Si^+ and Zn^+, could insert itself into the lattice as a substitutional impurity, also shown in Fig. 3.3(b).

During implantation beam energy is deposited in the crystal target, thus increasing the temperature inside the Si; this temperature rise can be sufficient for the defects to anneal out [101,102]. In particular, the single vacancies are known to be mobile at temperatures as low as 150K [103] in *p*-type Si, and even lower in *n*-type Si [103]. These mobile vacancies along with any lattice Si interstitials may recombine, restoring the lattice site and leaving interstitials (of either or both Si ions and the implanted ions) as in Fig. 3.3(d), or encounter another vacancy and

combine to form a divacancy, which is stable to much higher temperatures than the single vacancy in Si, as in Fig. 3.3(c). In addition to the vacancies being mobile, silicon interstitials are also extremely mobile even at low temperatures allowing for recombination with vacancies, trapping by impurities [104], or formation of interstitial clusters as shown in Fig. 3.3(e-f) [105-107]. Another defect found in these ion-implanted devices is the vacancy-oxygen (VO) complex where a vacancy defect and an oxygen impurity form a stable energy state [66]. The VO defect is also a potential source of absorption in the telecom wavelength regime [66]. Other defects form as well, but those listed above are the ones primarily discussed in this work. Note that the level of implantation dose discussed here is far below that needed to serious damage the Si waveguide, although effects such as reduced mobility or increased optical scattering can result.

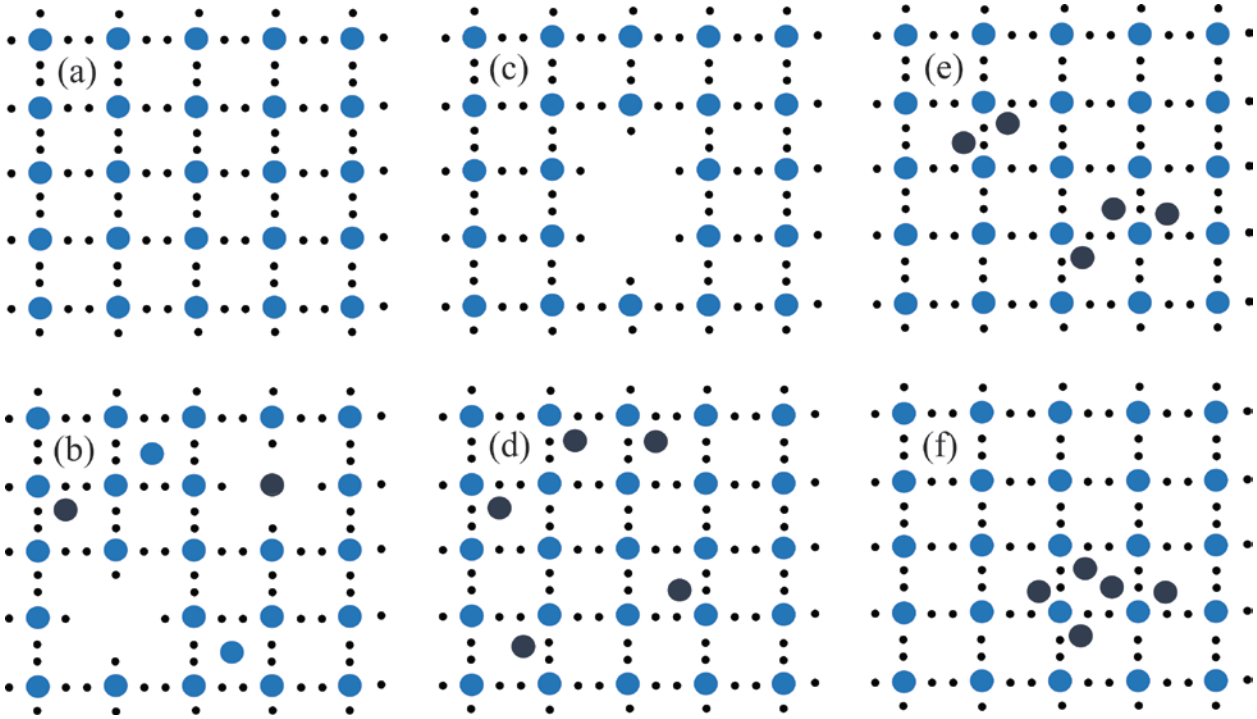

Figure 3.3 (a). Initial crystal lattice structure prior to implantation. (b). Ion implantation results in vacancies where the an atom is knocked out of its lattice site, interstitials, where an atoms end up in between lattice sits, and substitutional defects, where the ion implanted replaces an atom in its lattice site. (c). The divacancy defect common in implanted silicon is the result of the mobile vacancies meeting up and forming a stable defect consisting of two vacancies. (d). In the case of self-implantation and sufficient annealing, a large number of interstitials are found in the within the Si lattice (with the Si interstitials represented with dark blue dots). (e-f). With sufficient annealing, these interstitials are mobile and tend to from small clusters, from 3 – 10 atoms [107].

An additional consideration in ion implantation is the angle of implantation. Due to the crystalline structure of the Si, it is possible for an ion to travel a great distance into the structure without causing a collision in a process called channeling, [108] illustrated in Fig. 3.4. To minimize channeling, the implantation done in this work had the substrate placed at a 7˚ angle [108] as shown in Fig. 3.4.

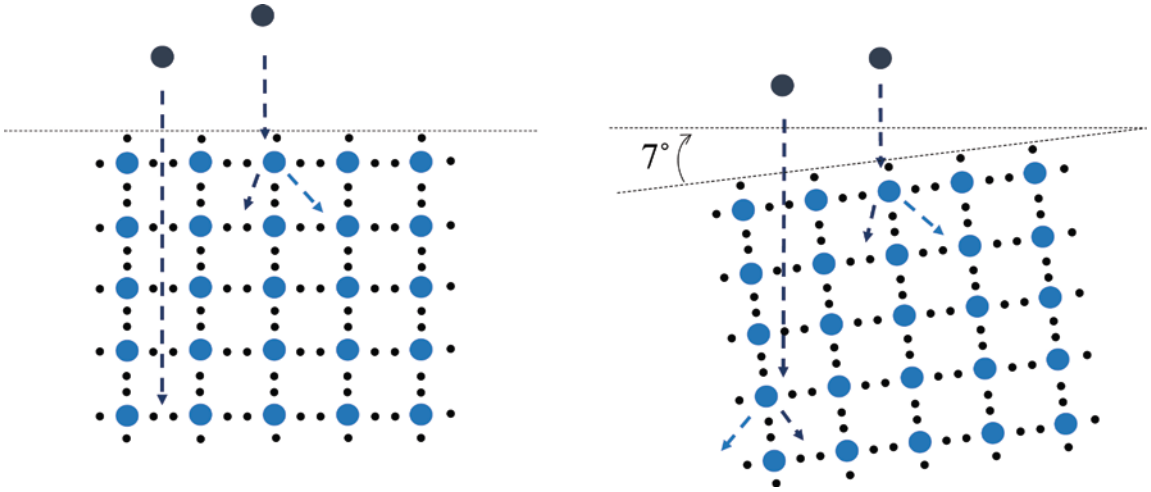

Figure 3.4 (a) During ion implantation where the substrate face is perpendicular to the direction of the ions, a phenomenon called 'tunneling' can occur, where the ion travels deep into the target material without encountering any collisions. (b) To reduce the chance of tunneling, the target material was set a 7˚ angle off the perpendicular.

3.3 Photodetection via Trap Assisted Optical Absorption

Each of the defects discussed previously are known to create trap states in the energy bandgap of Si. These trap states have been studied extensively within the last decade to create Si NWWG PDs [64-82,84-86]. Perhaps the most studied of these trap states is the divacancy defect and this defect is the focus of much of this work. With its optical detection being strong at 1.55 μm as shown in later chapters and [66,87] and with it being the apparent source of detection at 2.5 μm presented in this work, the divacancy defect in a Si NWWG appears to be an excellent absorption detector state for use with in telecom into the mid-IR wavelength range.

The divacancy defect is known to be associated with three different energy levels (trap states) within the Si bandgap depending on its charge state [109]:

$$V_2^{2-} \approx E_c - 0.23\text{eV} \tag{3.5}$$

$$V_2^{2-} \approx E_c - 0.42\text{eV} \tag{3.6}$$

$$V_2^{2-} \approx Ev + 0.20\text{eV} \tag{3.7}$$

where the superscript of V_2 is the charge state of the divacancy defect, E_c is the conduction band energy level, and E_v is the valance band energy level. In addition to the divacancy several other defects are introduced with ion implantation, including interstitials clusters [110], vacancy-oxygen pairs [111] and others states related to doping and contaminants [111]. Despite these other defects and multiple trap levels, detectors dependent upon the divacancy defect can be accurately modeled using Shockley-Read-Hall (SRH) theory and a single dominant defect level at E_c – 0.4 eV [88]. Figure 3.5 illustrates photodetection without and with a single recombination center, as was modeled in [88]. Although previously modeled in literature [88], a summary of SRH theory as it pertains to optical generation by sub-bandgap photons is provided below as a primer.

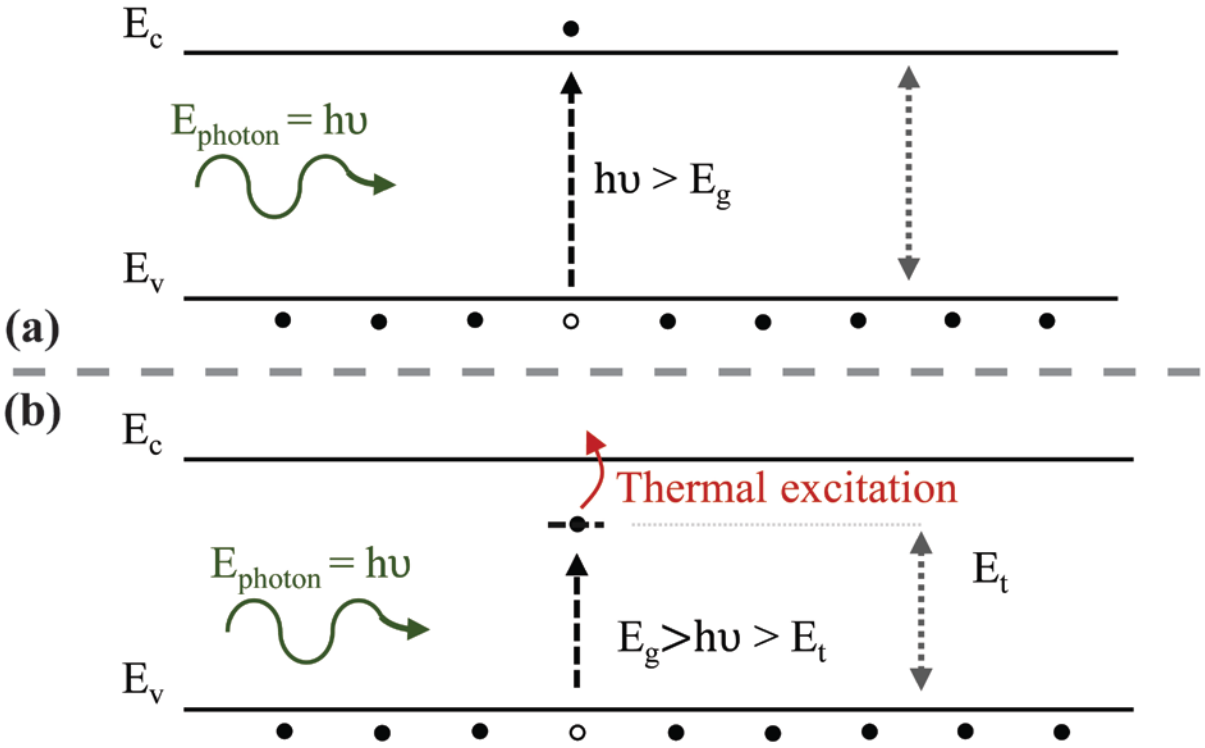

Figure 3.5 (a). For photodetection without trap state assistance, the photon energy must be greater than the band gap of the semiconductor. In addition, in the case of silicon, which has an indirect band gap, a phonon is also required to account for the momentum change. (b). Using trap state assistance, a photon with an energy less than that of the bandgap but near the level of the trap state can excite an electron to the trap state. If the trap state is sufficiently close to the conduction band, the electron is then thermally excited to the conduction band.

The introduction of a trap state within the band gap allows for four different processes to occur: generation of a hole in the valence band by excitation of an electron to the trap state (G_p); generation of an electron in the conduction band by excitation from an occupied trap state to the conduction band (G_n); capture of an electron from the conduction band to the trap state (U_n); and finally capture of an electron from the trap state to the valence band (U_p). These processes are illustrated in Fig. 3.6 below.

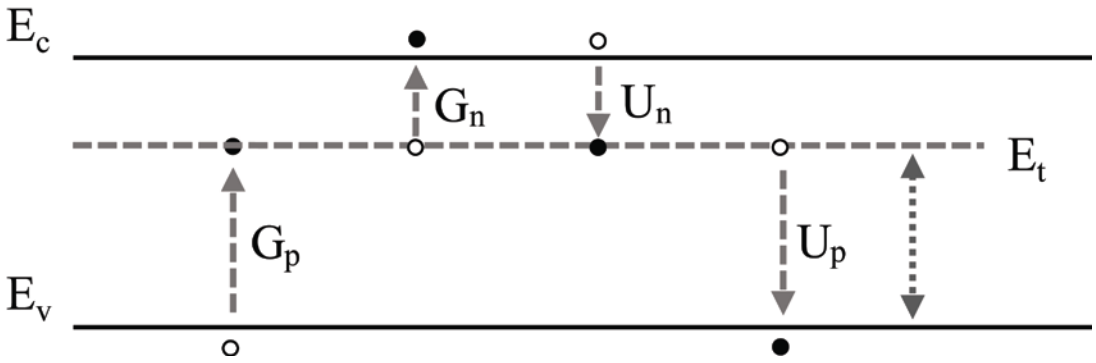

Figure 3.6. Illustration of the four processes involved in SRH theory, each defined in the text above.

In steady state, these processes balance out such that:

$$U_n - G_n = U_p - G_p. \tag{3.8}$$

In the presence of light and using the fact that G_n is dominated by thermal excitation and is much greater than U_p [88] for the divacancy, a single additional term, G_p^{opt}, is added to the model, accounting for the excitation of an electron to the trap state [88]. Thus, the total hole generation rate becomes [88]:

$$G_p' = G_p + G_p^{opt}. \tag{3.9}$$

Since G_n is much greater the U_p, the electron elevated to the trap is then thermally excited into the conduction band.

In order for there to be a net generation of carriers, the trap level must act as a generation center and have a hole generation rate G_p' (recall $G_n >> U_p$), therefore each hole results in an electron in the conduction band) greater than the electron recombination rate, U_n [88]. Relating generation and recombination rates to the physical parameters of the material and trap states, such as: $c_{n,p}$, the coefficients of electron and hole thermal recombination, N_t, the trap state density, n_t, the trap state density occupied by an electron, and *n'* and *p'* the physical parameters related to the energy level of the trap state [88], gives:

$$U_n = C_n(N_t - n_t)n \tag{3.10}$$

$$G_n = C_n n_t n' \tag{3.11}$$

$$U_p = C_p n_t p \tag{3.12}$$

$$G_p = C_p(N_t - n_t)p'. \tag{3.13}$$

Finally, using these equations in conjunction with the condition that G_p' must be greater than U_n gives [88]:

$$G_p^{opt} > (N_t - n_t)(C_n n - C_p p'). \tag{3.14}$$

Depending on the relation of n to p' (as C_n and C_p are similar in magnitude), the required optical generation rate can be either positive or negative [88]. From [88], the optical generation rate can be calculated as:

$$G_p^{opt} = I(x,y)\frac{\lambda}{hc}\alpha e^{-\alpha z} \tag{3.15}$$

where $I(x,y)$ is the optical mode intensity, λ is the wavelength, h is Planck's constant, c is the speed of light, z is the distance along the material, and α is the material absorption coefficient. For the devices studied in this work, α was found to be between 15 – 60 cm^{-1}. In [88] α was related to the divacancy defect concentration by:

$$\alpha = \frac{N_t}{7.7\cdot 10^{16}\mathrm{cm}^{-2}}. \tag{3.16}$$

Simulations using the model discussed above, i.e. that derived from [88], along with measured parameters for the divacancy trap states, matched well with experimental results, thus providing a solid theoretical foundation for the operation of these photodetectors. However, in many cases a single dominant trap model is insufficient, opening the door for additional research in this area.

3.4 Stopping Range of Ions in Matter Simulations

In order to determine proper ion implantation conditions, Stopping Range of Ions in Matter (SRIM) and Transport of Ions in Matter (TRIM) [112] simulations were used. SRIM (a well developed open source code) utilizes a group of programs to calculate the stopping and range of ions in matter. The software uses a quantum mechanical treatment of ion-atom collisions, where the ion and atom have a screened Coulomb collision, including exchange and correlation interactions between the overlapping electron shells [112]. The software also uses statistical algorithms to improve the speed of the simulations by allowing the ion to make jumps between calculated collisions and then averaging the collision results over the intervening gap [112]. The main outputs used in this work from the SRIM calculations were the ion depth profile and the collision events profile. It is important to note that the SRIM software performs the above calculations at 0 K [101], thus ignoring annealing that may occur due to the temperature of the implantation chamber or to the increase of temperature inside the lattice due to the implantation [102]. For the work presented here, the damage profile was more important than the actual damage density, as the desire was to match the damage profile with the optical mode intensity to ensure maximum overlap between the absorption region and the optical mode.

The TRIM program (a second open source code) expands the capability of the SRIM program by calculating the ion ranges and damage profiles in multiple layered structures [112] such as the waveguide structures present in Chapter 2. The individual layers are defined by the user, including compound layers such as SiO_2 and HSQ. For the compound materials, TRIM can calculate the material density based on the stoichiometric formula, however the calculations are likely inaccurate [112]. For greater accuracy, the user has the option of either choosing from the extensive list of compound materials provided with the TRIM program along with their known

densities [112] or of overriding the calculated density with the actual density of the compound if known [112]. Table 3.1 below lists the materials used in this work, along with their stoichiometric formula, calculated density from the SRIM program, and the actual density used (if different from calculated. For the buried-oxide layer, the density of amorphous SiO_2 listed in the SRIM list of materials [112] was used as the SOITEC wafers uses a thermal oxide growth and implantation to form the buried oxide layer [113].

Table 3.1 List of materials used in TRIM calculations.

Material	Stoichiometric Formula	Calculated Density (g/cm3)	Used Density (g/cm3)
HSQ	$H_8Si_8O_{12}$	1.3	1.4 [114]
Silicon	Si	2.32	2.32
Buried Oxide	SiO_2	1.72	2.32 [112]
Silicon Substrate	Si	2.32	2.32

The TRIM calculations were done based on the layers of the Si NWWGs from Chapter 2. For the MSM devices, an HSQ mask was used for the top layer, whereas a SiO_2 mask was used for the *p-i-n* devices from MIT Lincoln Labs. Table 3.2 below gives data for both masking methods utilizing the density of HSQ from [114] and that of thermal oxide from the software [112]. The profiles were found based on simulations of at least 10,000 ions, to ensure a high fidelity distribution.

Initial starting values for ion implantation energies were based on literature of previously implanted devices [64-66]. The implantation energy for Si^+ and Ar^+ implantations was set to maximize the overlap of the mode ($\lambda = 1.55$ μm) with the lattice damage as the defect believed responsible for absorption at lower annealing temperatures is the divacancy as discussed above.

Figure 3.7 below shows the calculated mode intensity for a *p-i-n* device along with the overlap of the damage distribution due to ion implantation with the modal intensity down the center of the waveguide. Matching the peak of the defect density distribution with that of the mode intensity ensures a maximum overlap between the defects responsible for photodetection and the optical mode.

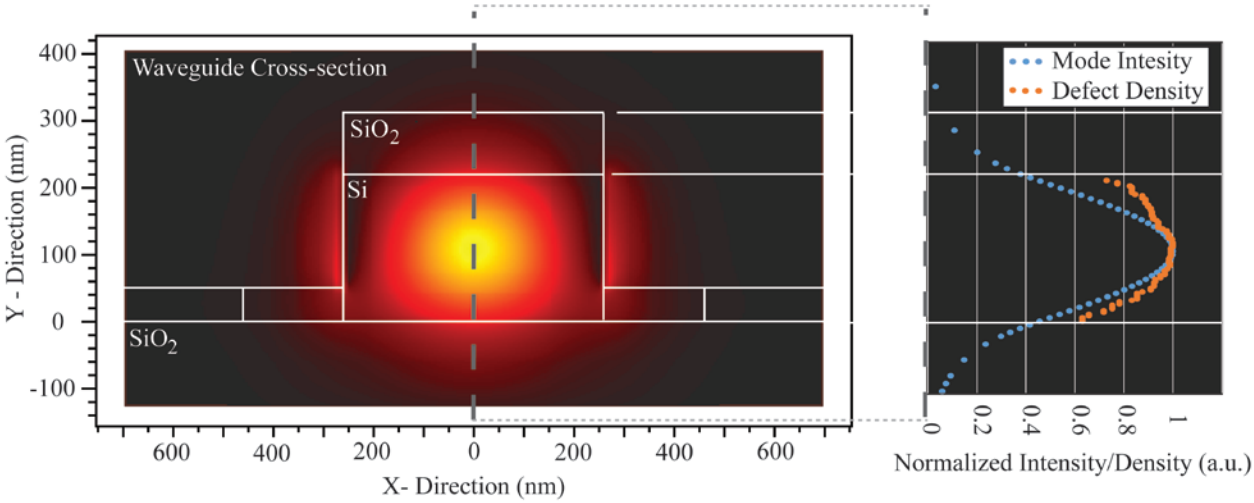

Figure 3.7 (a). Cross-section of *p-i-n* waveguide with modal intensity super-imposed. (b). One dimensional cut of the waveguide cross-section down the center showing both the normalized mode intensity as a function of depth in the waveguide and the normalized defect concentration, for a Si^+ implantation energy of 190 keV, as a function of depth in the waveguide.

Table 3.2 below gives the damage and ion peak depth peaks and the damage straggle for different ions implanted at different energies and into different masking layers (as discussed in Chapter 2). In the case of the Zn^+ implantation, the desired defect is the substitutional defect, in which a Zn atom replaces a Si atom in the crystal lattice, therefore the ion peak is the relevant parameter and matched with the mode intensity peak.

Table 3.2 Implantation simulation conditions and results.

Implantation Ion	Mask Layer (Chapter 1)	Ion Energy (keV)	Damage Peak Depth (nm)	Damage Peak Straggle (nm)	Ion Peak Depth (nm)
Si^+	SiO_2	180	190	121	248
	HSQ	180	209	118	279
Si^+	SiO_2	190	201	146	262
	HSQ	190	220	130	292
Si^+	SiO_2	200	206	148	305
	HSQ	200	240	152	274
Ar^+	SiO_2	260	204	164	270
	HSQ	260	188	121	270
Zn^+	SiO_2	260	116	77	184

Additional simulations were run for the wing region of the Si NWWG diodes to determine if the damage done during implantation is significant enough to alter the diode properties as is discussed in the later chapters. Figure 3.8 shows the damage profile for a 50 nm Si layer over the buried oxide layer, where the damage profile represents collision events. The initial damage is significant, on the order of 4×10^{20}, however this does not take into account self-annealing, which reduces the numbers of vacancies produced significantly [101]. The number of collision events in the wings is comparable to that found in the waveguides ($\sim 6\times10^{20}$), suggesting that the

total number of vacancies (and hence divacancies) in the wings is on the same order of that found in the waveguides. From [88], the divacancy concentration is on the order of $10^{17} – 10^{18}$ cm^{-3} for the Si implantation doses used, which is comparable to the doping levels in the *p-i-n* devices. As the divacancy is known to act as compensation doping [115], the ion implantation likely altered the diode characteristics in the devices implanted as discussed in later chapters.

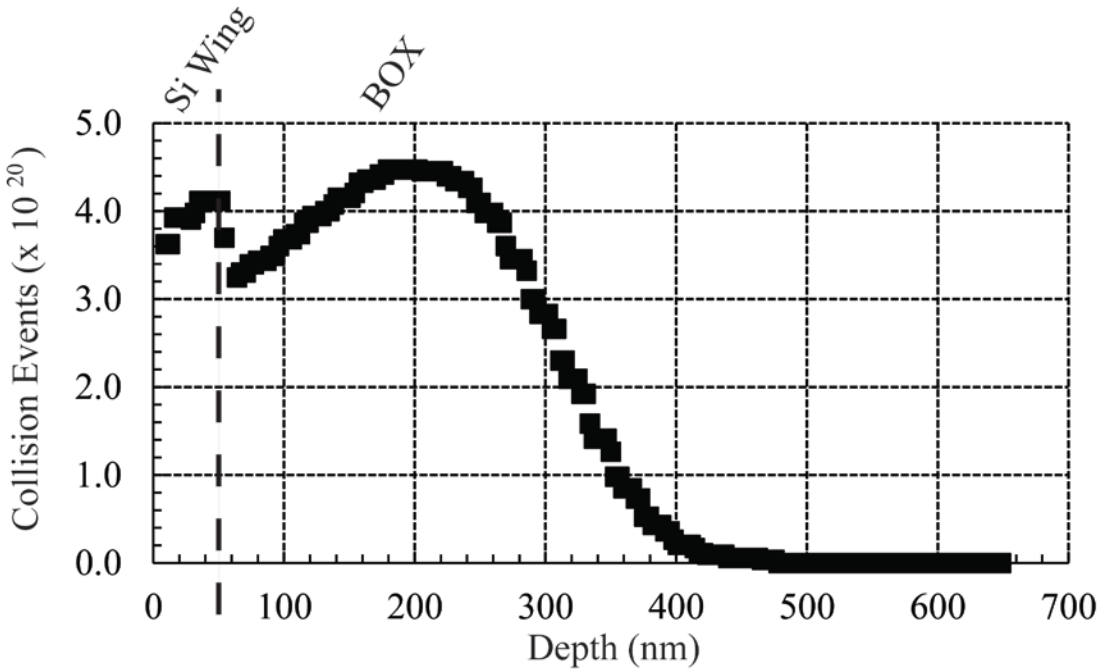

Figure 3.8. Results of TRIM calculations on the 'wing' area of the Si NWWG PDs. The collision events is a measure of the vacancies produced, however the results do not account for self-annealing due to the elevated temperature of the NWWGs.

SECTION II: TELECOM WAVELENGTH DETECTORS

CHAPTER FOUR:
Metal-semiconductor-metal ion-implanted Si waveguide photodetectors for C-band operation[1]

4.1 Background

Ion-implanted Si waveguide photodetectors (PDs) have recently been incorporated into numerous photonic integrated circuits and systems [64-82,116-118]. By implanting Si with a selected atomic species, photodetection from 1550 nm to beyond 1900 nm has been achieved [64-82,116,117], opening up the ability to incorporate detectors for the telecom band and beyond in integrated Si systems. These devices have been demonstrated with bandwidths greater than 35 GHz and responsivities up to 10 A/W [64] along with error-free data transmission at wavelengths of 1550 nm [71] and 1900 nm [72]. Multiple configurations have been used to enhance detector responsivity, including resonant-cavity-enhanced detectors [73] and avalanche-multiplication detectors [74,119]. These ion-implanted waveguide PDs have been incorporated in Si photonic devices for power monitoring [67], wavelength monitoring [68], thermal tuning [69], and variable optical attenuation [70].

The majority of these devices are based on reverse biased *p-i-n* rib waveguide diodes, similar to the structure shown in the bottom inset of Fig. 4.1(a). These *p-i-n* diodes require multiple masking and alignment steps, and have significant junction capacitance [64,120]. An alternative metal-semiconductor-metal (MSM) structure, commonly used in planar geometries [121], has been proposed and demonstrated for carrier removal in 2D Photonic Crystal (PC) cavities [120]

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[1] This chapter adapted from:

1. B. Souhan, R. R. Grote, J. B. Driscoll, M. Lu, A. Stein, H. Bakhru, and R. M. Osgood, "Metal-semiconductor-metal ion-implanted Si waveguide photodetectors for C-band operation," Opt. Express **22**, 9150-9158 (2014)

as well as for Ge [122] and InGaAs [123] photodetectors integrated on Si. Where a *p-i-n* PD relies on a reversed bias *p-i-n* junction, the MSM structure relies on back-to-back Schottky barriers. By applying a bias across the Schottky contacts, carriers generated in the semiconductor region are swept out to the contacts while the barrier height prevents dark current across the device, unlike internal photoemission devices where carriers are excited over the barrier to generate photocurrent [124]. The MSM PD has a simplified fabrication procedure as well as having a lower capacitance when compared with *p-i-n* diodes of similar dimensions [120]. The lower capacitance/length makes the MSM ideally suited for the longer low-absorption-coefficient ion-implanted Si waveguide PDs. Additionally, the lack of contact doping makes the MSM useful for carrier removal [120] in nonlinear four-wave mixing devices [52]. However, the top contact MSM design used in [122,123] creates significant parasitic optical loss resulting in substantially reduced responsivity. To decrease parasitic loss, the metal-semiconductor Schottky contacts are moved to the "wings" of the PD structure, as shown in Fig. 4.1(a).

In this chapter, we demonstrate MSM PDs based on a Si rib-waveguide geometry as shown in Fig. 4.1(a). The absorbing region of the PD is formed by implanting Si^+ ions to introduce divacancy defects that absorb at 1550 nm. Device responsivity of > 0.5 A/W is achieved along with a frequency response of 2.6 GHz for a 50 V bias. Bias voltage is a strong function of contact separation and can be reduced to ≈ 15 V with reduced contact spacing. Analysis shows that the frequency response is not limited by the MSM-contact configuration, but is likely due to reduced low-field mobility as compared to intrinsic Si. Simulation of an optimized device shows an increased frequency response of ≈ 9.8 GHz at 15 V, making it suitable for a broad array of Si photonic integrated circuit applications.

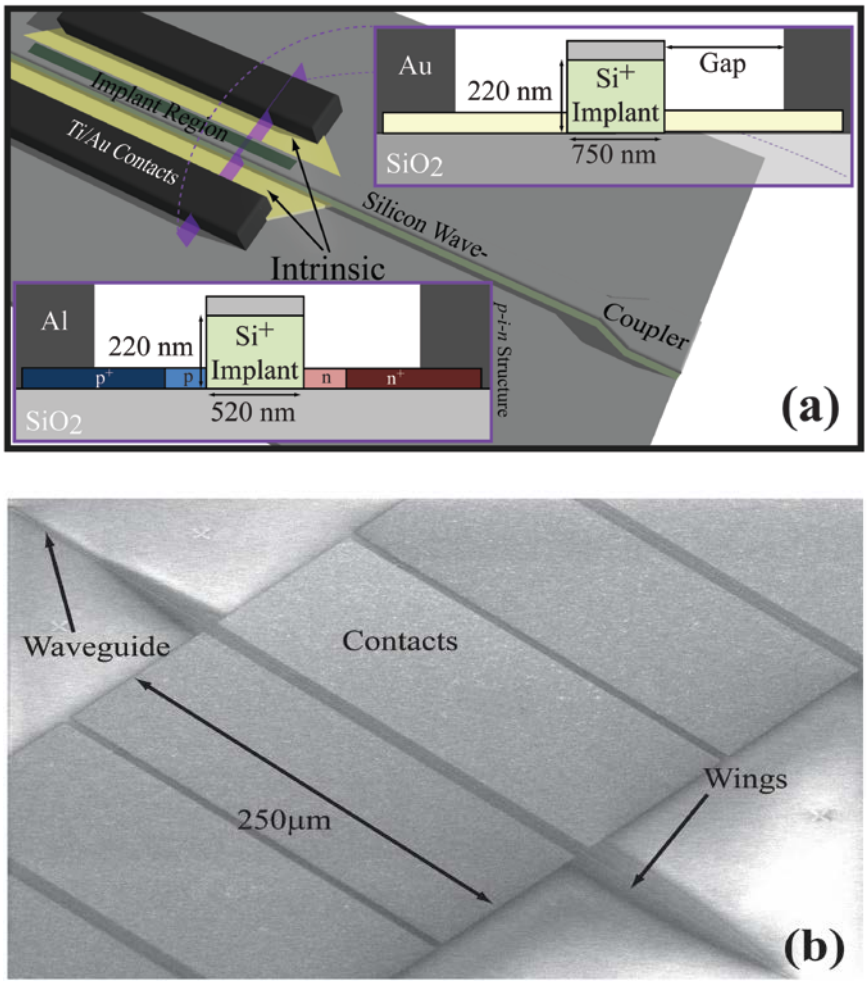


Figure 4.1. (a) Device cartoon with lower inset showing the cross-section of a *p-i-n* device from [66] and upper inset giving the cross-section of our MSM structure. (b) SEM image of 250 µm device.

4.2 Device Operation, Design, and Fabrication

4.2.1 Device Operation

A *p-i-n* PD relies on a single *p-i-n* junction creating a potential barrier, which with the application of a reverse bias blocks carrier flow across the device while simultaneously creates a strong electric field in the intrinsic region where generated carriers are quickly swept towards the contacts, creating photocurrent. The MSM on the other hand consists of two back to back Schottky barrier diodes with an energy band diagram as shown in Fig. 4.2. The Schottky barrier present at each contact prevents carrier flow through the device, while the built in potential

creates a barrier to carriers generated in the semiconductor region. With the application of a bias (device is symmetrical), the Schottky barrier remains in place, but the built in potential is reduced until it virtually disappears creating the flat band condition as shown in Fig. 4.2(b). At this point, the Schottky barriers still prevent carriers from transporting across the contacts, however carriers generated in the semiconductor region are swept apart and towards the contacts creating photocurrent as in the case of the *p-i-n* diodes.

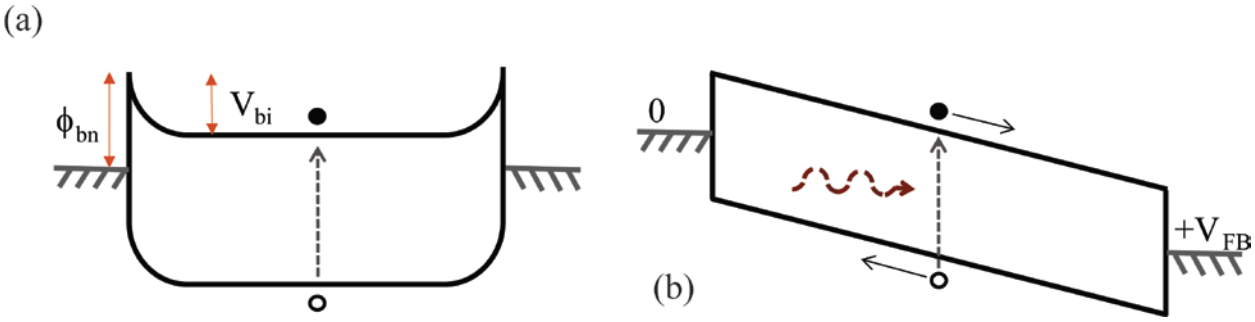


Figure 4.2 (a) Band diagram of MSM device without application of a bias. (b). Band diagram of MSM device with the application of the flat band bias demonstrating photodetection.

4.2.2 Device Design

Previous MSM waveguide PDs based on Ge [122] or InGaAs [123] utilized Schottky contacts directly on top of the waveguide allowing for low operating voltage and high frequency response. Due to the lower absorption coefficients of 8 – 200 dB/cm associated with Si ion-implanted waveguides [64-66], the parasitic loss from such a design is significantly greater than the defect-mediated absorption coefficient, resulting in poor responsivity. The alternate design presented here utilizes a rib-waveguide structure similar to *p-i-n* devices in [64-66] with the contacts on either side of the waveguide, creating Schottky barrier contacts with the wings, as shown in Fig. 4.1(a). The wings provide the necessary electrical connection between the waveguide and contacts as well as alter the distribution of the electric field so as to facilitate carrier transport. The tight confinement of the rib-waveguide mode allows for the contacts to be

placed close to the channel section, thus reducing the operating voltage and increasing the frequency response.

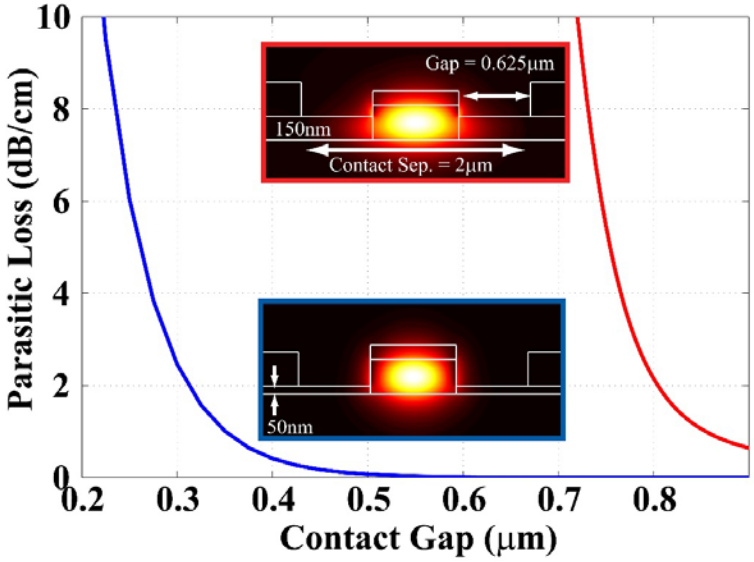


Figure 4.3. Simulated parasitic loss verses waveguide-contact gap for 750×220 nm waveguide with wing heights of 50 nm (blue) and 150 nm (red) at λ = 1550 nm. (insets) Mode intensity for the quasi-TE guided mode for both 50 nm (lower) and 150 nm (upper) wing heights. The lower modal confinement of the 150nm-wing height increases the required contact gap for a given amount of parasitic loss. For devices reported here, the waveguide-contact gap is 2.3μm.

Using finite element method (FEM) analysis, the amount of parasitic loss in the device is found to be strongly dependent on wing height and contact spacing. Contact structure can also impact parasitic loss, but is not examined here. Sellmeier equations were used for the Si and SiO_2 indices of refraction, while free-carrier effects in Si were modeled based on the data from [42] and Ti/Au contacts were modeled using data from [125]. The FEM results for quasi-TE modes are shown in Fig. 4.3 for wing heights of 50 nm and 150 nm with 15 nm/150 nm Ti/Au Schottky contacts. Increasing the wing height decreases the modal confinement, resulting in a reduced modal overlap with the implanted region and an increased parasitic loss from the contacts. Moving the contacts further apart can reduce this parasitic loss, but will also increase the required bias voltage, along with the carrier transit time. Ideally, for minimal parasitic loss,

a wing height of ~50 nm is desired. We note that other metals such as Cu and Al [124] may be used in place of the Ti/Au combination for CMOS compatibility.

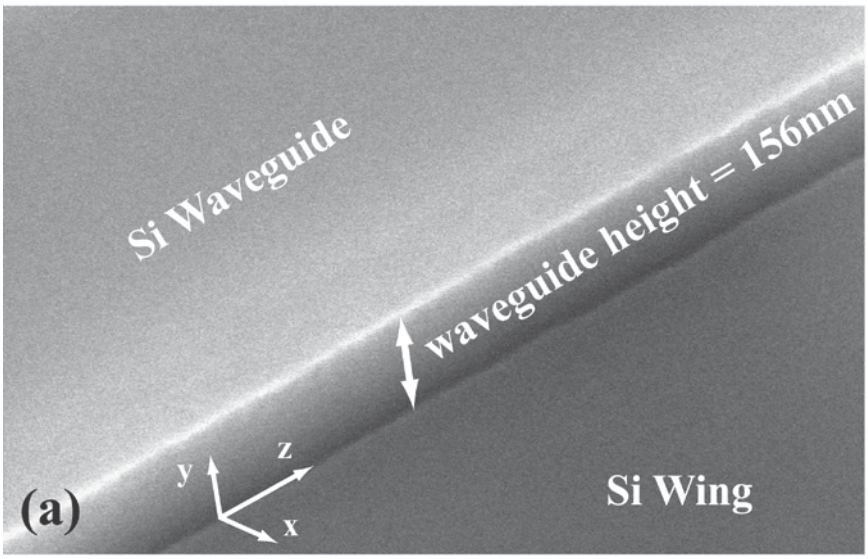
Fan-out tapers are utilized to couple between a lensed-tapered fiber (LTF), and the Si waveguide detector. These fan-out tapers are designed for a ~6 dB coupling loss per facet by mode-matching between Gaussian profile of the LTF with a spot size of 2.5 μm [126] and a coupler width of 3.85 μm. The coupler adiabatically tapers down to the 750 nm wide channel waveguide input to the PD over a length of 100 μm.

The electrical characteristics of the PD are modeled using the RSoft LaserMod package from Synopsis [127]. The static electric field produced by applying a bias voltage across the contacts was modeled using a Poisson solver, while the Boltzmann transport equations are solved numerically to determine the carrier-transit-time. Frequency response was determined by simulating an optical impulse function incident on the device and performing a Fast-Fourier Transform on the resultant current transient response.

4.2.3 Device Fabrication

A thorough description of the fabrication process is presented in Chapter 2, however a brief description is present here. The devices shown in Fig. 4.4 were fabricated at Brookhaven National Laboratory on SOITEC [113] silicon-on-insulator (SOI) wafers with a 220 nm 14-22 Ωcm resistivity *p*-type Si layer and a 3 μm buried oxide layer (BOX) layer. The waveguides were defined using electron beam lithography with a 90 nm hydrogen silsesquioxane (HSQ) hard-mask. The mask was developed with a 1% wt NaOH/4% wt NaCl aqueous mixture, followed by a inductively coupled plasma etch utilizing HBr and Cl chemistry to define the waveguide, while leaving ≈ 60-64 nm of the top Si layer. A second mask utilizing MaN-1410 negative photoresist defined the wing sections of the PD and the remaining Si layer was etched

away, leaving a Si-nanowire waveguide adiabatically coupled to a Si rib waveguide, as shown in Fig. 4.1(a). The NaOH/NaCl development process is known to provide very high contrast [26] while the inductively coupled plasma etch provides clean side walls with roughness on the order of 3 nm [19,52]. Contact windows were patterned using a single layer of Shipley S1811 resist for liftoff, followed by a 1 min O_2 plasma clean. The contacts were deposited via electron-beam deposition of a 15nm layer of Ti for adhesion followed by a 150nm layer of Au for the contact pads. Devices were subsequently masked to open a 1mm window and implanted at the Ion Beam Laboratory, at the State University at Albany with 1×10^{13} cm^{-2} Si^{+} ions at an implant energy of 195 keV, beam current density of $7nA/cm^2$ beam current density, and beam diameter of $\approx$ 4 mm. The implantation energy and dose were based on prior reports of ion-induced defects [64-66] and Stopping Range of Ions in Matter (SRIM) calculations [112] from Chapter 3. After implantation the devices were annealed in steps of 50°C starting at 150°C, for 10 minutes at each step. Results reported here were after the 250°C anneal, which corresponded to the maximum responsivity. The final device dimensions are shown in Fig. 4.4. Waveguide width and contact spacing are 763 nm and 5.4 μm, respectively.



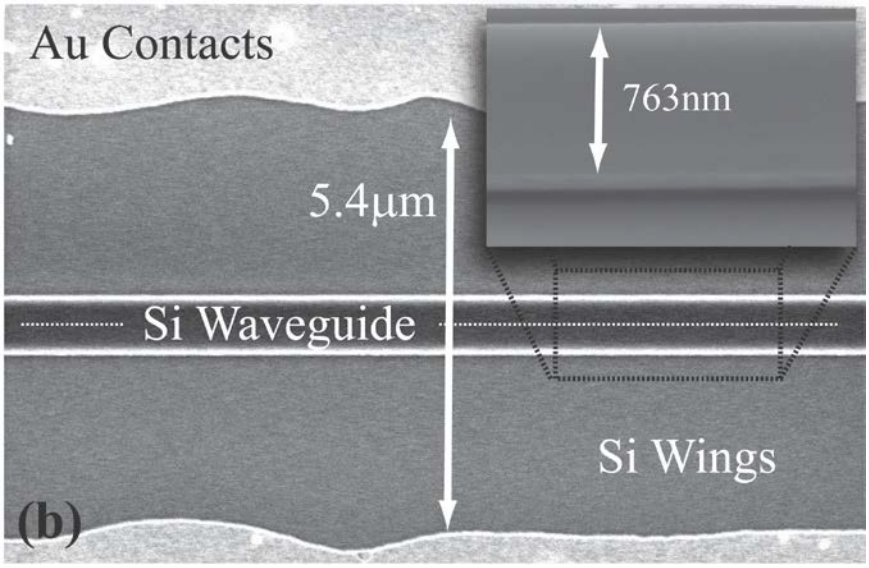


Figure 4.4. SEM images of fabricated devices. (a) View of the waveguide sidewalls showing no measurable roughness over the length of 1 μm. (b) Top view of waveguide with wings and contacts; the contact separation is 5.4 μm. (inset) High-magnification view of the waveguide showing waveguide width of 763 nm.

4.3. Results and Discussion

4.3.1 Responsivity and Internal Quantum Efficiency

To determine the detector responsivity and internal quantum efficiency, coupling loss is first determined at 1550 nm by measuring insertion loss through the devices prior to implantation and utilizing the cutback method on various PD lengths. Loss is measured for PD lengths of 0 μm, 250 μm, 500 μm, and 1mm as part of a total device length of 3 mm. The insertion loss is measured to be 16.6 dB with a standard deviation of 1 dB. Analysis of variance showed no significant difference in insertion loss versus device length. This is expected due to the low wing height and adiabatic taper, which minimizes scattering and parasitic losses between the waveguide and PD. Scattering loss between the coupler and device is lumped into the insertion loss, and scattering loss along the device was negligible based on the cutback measurements. For responsivity and internal quantum efficiency measurements, coupling loss (including

scattering loss before and after the device) is assumed to be half the measured insertion loss, equating to 8.3 dB, matching well with a simulated loss of 6 dB.

Responsivity is found by subtracting the dark current I_{dark} from the photocurrent under illumination I_{ph} and dividing by the incident power on chip, $\Re = \left(I_{ph} - I_{dark} \right) / P_{inc}$. Figure 4.5(a) shows the measured responsivity and standard deviation over a bias range from 0 to 50 V for the ten 1 mm length devices. The high bias voltage is not intrinsic to the MSM contact configuration; rather, it is required for the large contact spacing of our devices. Based on Poisson solver calculations, a reduction in contact separation from 5.4 μm down to 1.5 μm reduces the bias voltage required for 0.51 ± 0.13 A/W from 50 V to less than 15 V. Increasing bias voltage increases responsivity with no photocurrent plateau, similar to the results of [75]. The smooth increase in responsivity above 30V is unlikely due to avalanche multiplication, as the simulated DC fields in the device were significantly less than required for avalanche breakdown. The increase is believed due to improved carrier collection arising from an increase in carrier velocity. The frequency response measurements in the following section indicate the carriers are far from saturation velocity, resulting in significant increase in carrier velocity with increased bias. Alternatively the increase may be from other forms of carrier multiplication seen MSM PDs [121,128]. Figure 4.5(b) shows the responsivity decreasing with wavelength by 50% from 1550 nm to 1610 nm.

The initial dark current prior to annealing is 10's of nanoamps. However, the dark current increases with successive annealing steps and levels off in the 10's of microamps after 200°C, which is higher than those reported for *p*-*i*-*n*-based ion-implanted devices [64-66]. We attribute this behavior to contact degradation during annealing since Ti is known to diffuse into Au between 200°C-400°C [129]. Contact degradation has also been shown to be a source of

unusually high dark current in *p-i-n* devices [118]. We expect that this dark current can be reduced by using a diffusion barrier such as Pt. The defect states in the wings may also contribute to the higher than expected dark current, therefore we expect limiting implantation to the channel region of the waveguide, should reduce dark current as well.

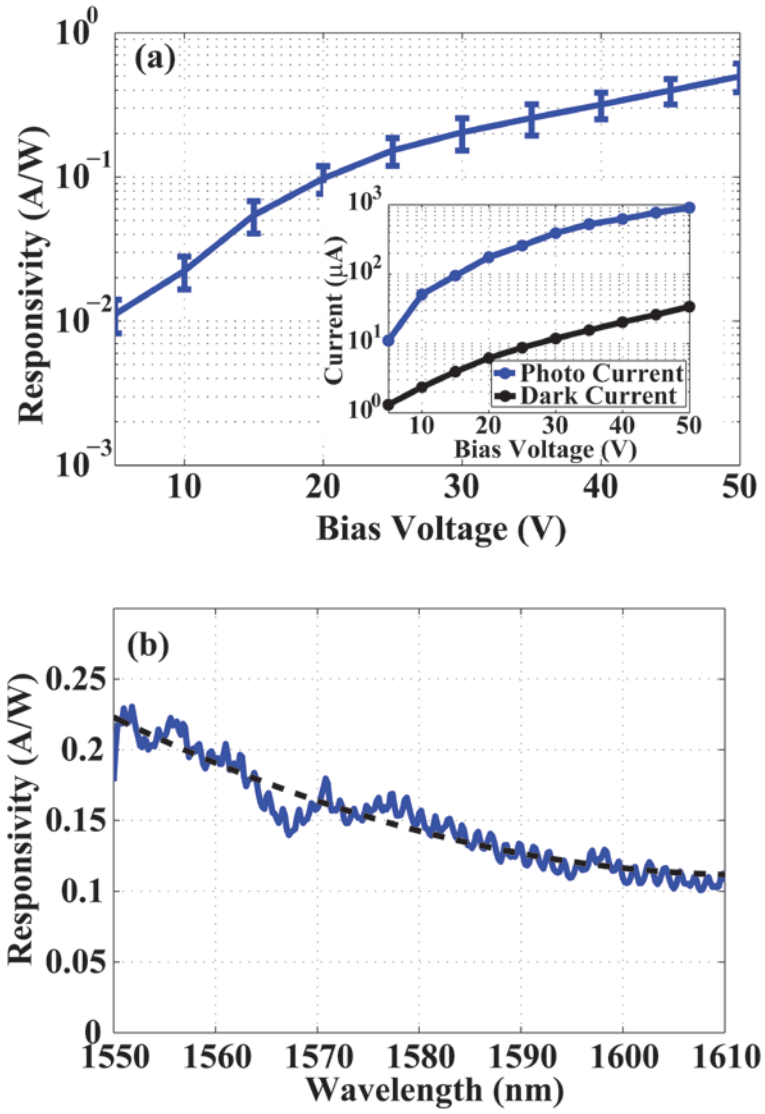


Figure 4.5 (a) Responsivity *vs* bias voltage with error bars for 1mm long PDs. Error bars were calculated from measurements across multiple devices and include uncertainties in coupling loss and coupling alignment. (inset) Photocurrent for ≈1mW optical power and dark current for typical 1mm long PD. (b) Responsivity verses wavelength from 1550nm to 1610nm for a 30V bias, the dashed line is a second-order polynomial fit to illustrate the trend.

In order to determine the detector internal quantum efficiency, $\eta = 1.24\left(I_{ph} - I_{dark}\right)/\left(\lambda P_{abs}\right)$, where P_{abs} is the absorbed power in detector and λ is the free space wavelength in micrometers, the absorption losses for the devices are first calculated by subtracting out the insertion loss measured prior to implantation from the measured insertion loss after ion implantation. Using this technique a modal absorption coefficient of 185 ± 70 dB/cm at 1550 nm is measured, matching well with other ion-implanted detectors in the literature [65,66]. Utilizing the average absorption coefficient of 185 dB/cm for the 1mm devices, η is found to be between 42 ± 8% at a 50 V reverse bias. This result is significantly higher than previous reports of 16% [64-66] for devices annealed at 300°C. We hypothesize that the different annealing and implantation conditions impact the quantum efficiency by changing defect distribution and concentration, as the quantum efficiency matches closely with previous results seen under similar annealing conditions in *p-i-n* Ar^+ ion-implanted devices [130]. Additionally, MSM PDs have been known to exhibit gain [121,128], attributed to either induced tunneling currents caused from built up charges at the cathode and anode of the device or to photoconductive gain from long life-time traps [121].

The modal absorption coefficient *versus* wavelength for a typical device is shown in Fig. 4.6(a). An increase in absorption with wavelength is expected for divacancy absorption centers in ion-implanted bulk Si [87], which is consistent with our measurements. Since the calculated changes in parasitic loss and confinement factor are negligible in this wavelength range, the decrease in responsivity with wavelength shown in Fig. 4.5(b) is due to a reduced internal quantum efficiency at longer wavelengths, which is consistent with observations of [72].

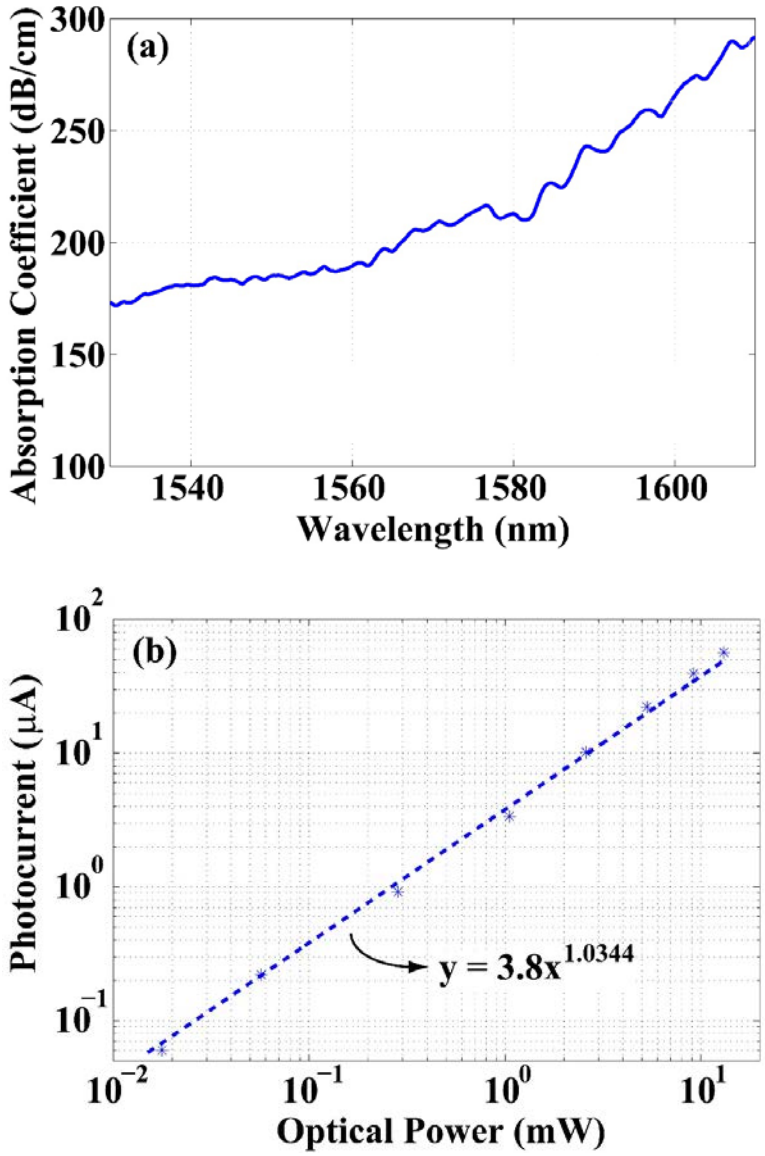


Figure 4.6. (a) Measured modal absorption coefficient *versus* wavelength from 1530 nm to 1610 nm. The data was smoothed to reduce noise in our measurement setup and thus obtain a general trend. (b) Linearity of device with input optical power at λ = _1550 nm from .015 mW to 13 mW, corresponding to power incident on detector 2.2 μW to 2 mW.

To measure device linearity with signal power, an erbium doped fiber amplifier is used to provide a variable signal source of up to 13 mW, corresponding to a maximum PD input power of $\approx$ 2 mW. With this variable source, linearity is measured over approximately three decades with a slope of 1.03 in Fig. 4.6(b), matching well with previous results [66,118] and demonstrating that these ion-implanted devices operate via a single-photon absorption process.

4.3.2 Frequency Response

A lightwave component analyzer (LCA) is used to determine the frequency response of the PD for bias voltages of 40 V and 50 V; the results are shown in Fig. 4.7 along with simulation results for a reduced carrier mobility as discussed below. Although the results are somewhat noisy, as the photocurrent was measured near the noise floor of the LCA, the 3dB point was well defined over several measurements. The resonance around 200-300 MHz was linked to the overall test setup, and the dip around 1.5GHz in the 50V measurement was attributed to the connection between the bias tee and the probes. The simulated curves are for a device with reduced carrier mobility, which is discussed below. The frequency response of 2.6 GHz at 50 V is significantly lower than that expected from simulation models based on intrinsic Si. For the given bias, the carriers are expected to be close to saturation velocity with a frequency response of ≈ 20 GHz. Capacitance and carrier gain can impact frequency response, but based on measured PD characteristics and device simulations, we attribute the reduced response to decreased low-field mobility.

A Keithley 590 CV Analyzer was used to measure the total-device and contact-pad capacitance operating at 100 kHz. The measured capacitance of ~70 fF/mm results in calculated RC-limited frequency response of 45 GHz for the 1 mm device (assuming a 50 Ω load). The measured device frequency responses of 2-3 GHz suggest that the response is not limited by capacitance, but by other factors.

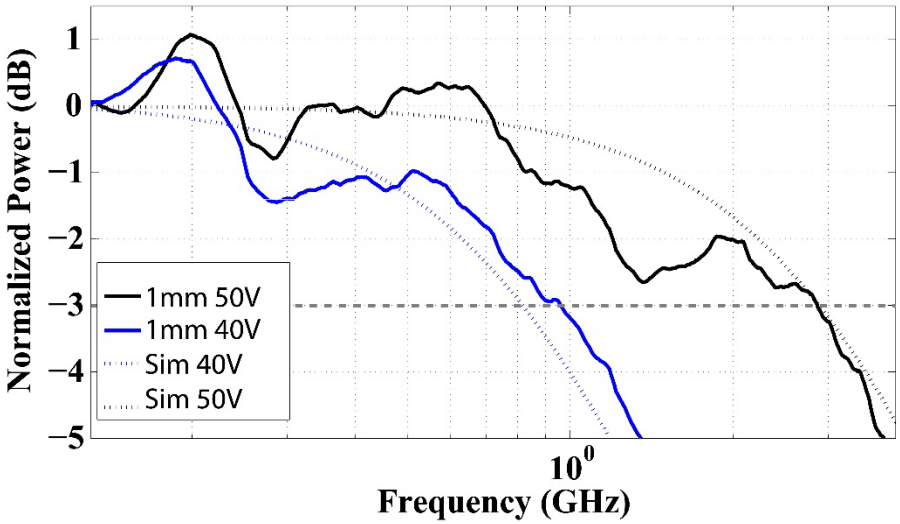


Figure 4.7. Frequency response for a 1mm device at 40-50V along with simulation results for a carrier mobility of 50 V/cm^{2}s.

Furthermore, the nearly three-fold increase in frequency response going from a 40 V to 50 V bias does not match simulations where carriers are near saturation velocity. The increase in response with bias voltage suggests the carriers are far from saturation velocity, indicating a decrease in carrier mobility compared to that in intrinsic Si. Mobility is known to decrease with the incorporation of trap states, in particular those created by divacancy defects [131,132]. For example, in reference [64], the surface-carrier mobility for implanted devices is shown to be several orders of magnitude lower for both electrons and holes after implantation. Assuming the bulk mobility follows the same trend as the surface mobility [64] a reduced frequency response is expected. Further reduction in low-field mobility is also expected from the degradation of the contacts with annealing, as Au is known to act as a carrier scattering center in Si [133].

In order to study the impact of decreased mobility, simulations at bias voltages of 40 V and 50 V were performed for different electron and hole mobilities and compared with experimental results. A mobility of ≈ 50 V/cm^{2}s matches the measured device frequency response well. Our simulations clearly show that a reduction in carrier mobility can account for the observed

frequency responses. Utilizing this reduced mobility a device with a contact spacing of 1.5 μm (gap equivalent to 0.375 μm) was simulated at bias voltages of 10 V, 15 V, and 20 V, resulting in frequency response of 4.7 GHz, 9.8 GHz, and 13.8 GHz, respectively. Further increase in frequency response is expected with an increase in bias voltage as the carriers are not at saturation velocity and with further decrease in contact spacing.

4.4 Conclusion

A monolithic ion-implanted Si MSM PD based on a rib waveguide has been demonstrated for the first time to the best of our knowledge. Responsivity is measured to be ≈ 0.51 A/W at 50 V bias with a frequency response of 2.6 GHz. The calculated quantum efficiency of 42% was found to be significantly higher than previously reported values of 16% for Si implanted waveguides, likely due to different annealing conditions. Results from previous ion-implanted detectors coupled with simulation results show an optimized device is capable of frequency responses greater than 9.8 GHz at bias voltages ≈ 15 V. These devices have the potential to be incorporated into many Si-based photonic integrated circuits due to their high performance and ease of fabrication. The devices can also be made CMOS compatible by replacing the Ti/Au Schottky contacts with Cu.

CHAPTER FIVE:
10 Gb/s Error-Free Operation of CMOS-Compatible All-Silicon Ion Implanted Waveguide Photodiodes at 1.55μm[2]

5.1 Background

Integrated photodetectors (PDs) operating in the C band are of paramount importance for the realization of on chip optical links, as they enable the end optical-to-electronic (OE) data conversion required for Si photonics. These detectors, as realized on the silicon-on-insulator (SOI) platform, must be high-speed and CMOS-compatible to support the high data rate conversion of optical signals in highly confined Si nanowire waveguides (Si NWWG) to the electrical data signals that can be processed by monolithically integrated electronics. However, there exists an inherent difficulty in integrating a material that absorbs in the C-band into a CMOS-compatible SOI based process due to material constraints. Recently, there has been significant progress towards this goal with the hybrid integration of III-V materials [134], and with the integration of Ge [135-137]. Although these solutions have produced high performance devices, Ge integration requires a large number of fabrication steps, a high thermal budget, and the need for a Ge back-end process to produce low dislocation density devices [135], while hybrid III-V integration requires modifications to the standard CMOS process.

Devices that use methods other than intrinsic material absorption for photodetection, referred to as extrinsic PDs, have been demonstrated, including: internal photoemission PDs utilizing a Si

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[2] This chapter adapted from:

R. R. Grote, K. Padmaraju, B. Souhan, J. B. Driscoll, K. Bergman, and R. M. Osgood, "10 Gb/s Error-Free Operation of All-Silicon Ion-Implanted-Waveguide Photodiodes at 1.55μm," IEEE Photon. Technol. Lett. **25**, 67-70 (2013).

NWWG-Schottky contact [138,139], deposited poly-Si PDs utilizing surface state absorption [140], and PDs that utilize sub-bandgap defect state absorption *via* ion implantation of the Si NWWG [64-77]. Although these extrinsic Si NWWG PDs are simpler to fabricate, they typically have much lower responsivities (on the order of mAs/W) as compared to intrinsic PDs (0.8 to 1 A/W for Ge [135]) as well as lower absorption coefficients which requires a substantially longer device length. Ion implanted detectors have shown the best overall performance of these extrinsic Si NWWG PDs, while only requiring one extra implantation step and no high temperature processing. Various implantation species have been used to induce absorption, including H^+ [75], He^+ [79], Ar^+ [80], Se^+ [81], and B^+ [76]; however, Si^+ implanted Si NWWG PDs [64-66,75,76,80,81] have the largest reported responsivities of these ion implanted detectors. Recently, Si^+ ion implanted Si NWWG *p-i-n* photodiodes have been demonstrated with a bandwidth of > 35 GHz and responsivities of 0.5 to 10 A/W [64]. These devices are fully CMOS compatible and have responsivities which are comparable to intrinsic PDs. Due to their weak absorption coefficient of 8-23 dB/cm, these Si^+ implanted Si NWWG PDs have recently found use as in-line power monitors because of their ability to generate photocurrent without attenuating a large fraction of the optical power in the waveguide [141]; resonant cavity enhancement (RCE) has also been employed to decrease the device footprint while maintaining a large external quantum efficiency [73,77,142,143].

Here, we demonstrate error-free operation [bit-error-rate (BER) $\leq 10^{-12}$] of a 250 μm long Si^+ ion-implanted Si NWWG *p-i-n* PD as shown in Fig. 5.1(a-b) at 2.5 Gb/s and 10 Gb/s as well as error free operation of a 3 mm long PD at 2.5 Gb/s [71]. The sensitivity as a function of bias voltage is measured, and the frequency response limitations of the device are explored. Additionally, we explore the effects of bringing the diode into a highly absorbing state *via*

forward biasing, as reported in [64-66], and show that a 15 dB improvement in receiver sensitivity can be expected. We find that the frequency response of the device is primarily RC-time-constant limited, and thus, the L = 3 mm PD has a larger sensitivity than the L = 250 μm device due to its larger device capacitance, despite having a longer absorption length and a larger responsivity. We show that, by decreasing the device capacitance, 40 Gb/s operation is possible in these Si^+ implanted Si NWWG PDs. To the best of our knowledge, this is the first systems level exploration of an extrinsic Si NWWG PD on the SOI platform as well as the first demonstration of error free operation of such a device.

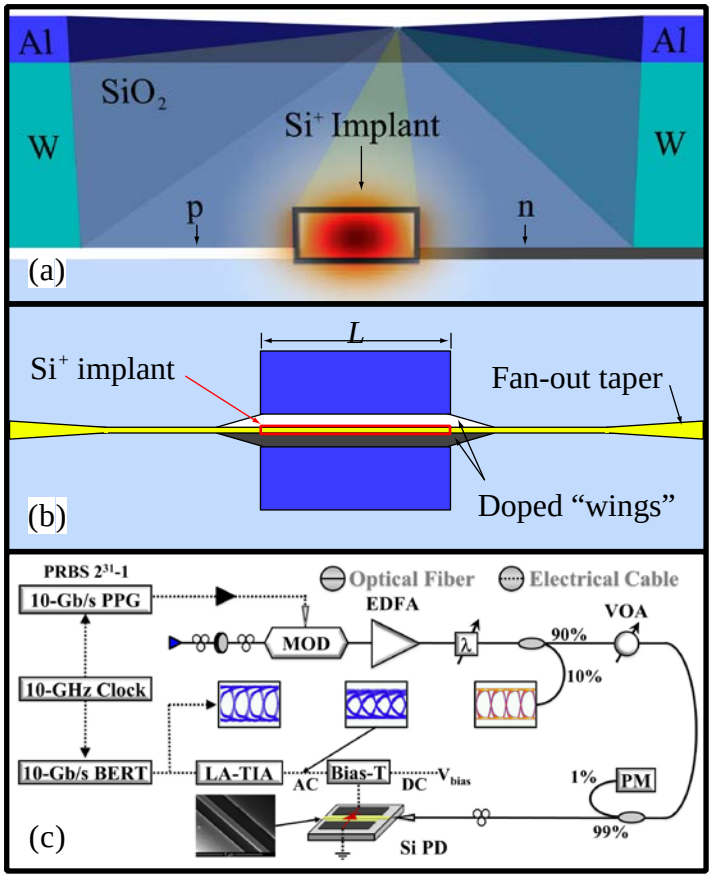

Figure 5.1. (a) Cross-section of a 520 nm × 220 nm Si NWWG with 50 nm wings. The channel waveguide section is Si^+ ion implanted with 10^{13} cm^{-2}, while the wings are doped *p* and *n* to form a *p*-*i*-*n* photodiode. The device is clad in SiO_2, and contacts are formed with a TiN/W Damascene process, and capped with Al. The finite-element method calculated quasi-TE mode is overlaid. (b) Top view of the device, showing the PD region as well as the cleaved facet fan-out tapers used for input coupling from the LTF, and (c) experimental setup for measuring detector sensitivity.

5.2 Measurements and Results

5.2.1 Experimental setup

The measured Si^+ ion-implanted Si NWWG *p-i-n* PDs were fabricated on the CMOS line at MIT Lincoln Laboratory, as described in Chapter 2, with dimensions given in the caption of Fig. 5.1. The experimental setup for measuring the sensitivity of these PDs is shown in Fig. 5.1(c), with a 10 Gb/s or 2.5 Gb/s 2^{31}-1 pseudorandom bit sequence (PRBS) of non-return-to-zero (NRZ) data being generated by a pulse-pattern generator (PPG). The PPG is then used to drive a $LiNbO_3$ modulator, which imprints the electrical signal onto a 1.55 μm optical carrier. The modulated light signal is sent to an erbium-doped fiber amplifier (EDFA) followed by a square pass-band filter, to reduce the amplified spontaneous emission noise. The optical eye is monitored through a 10/90 tap on a digital communications analyzer (DCA), and a variable optical attenuator (VOA) is used to attenuate the power being launched on-chip for BER measurements. Another tap, with a 1/99 split, sends the signal to an optical power meter (PM) to accurately monitor the power being launched on chip from the lensed-tapered fiber (LTF). The PD is electrically contacted with 40-GHz rated probes, and a bias tee is utilized to apply a DC bias. The demodulated electrical data signal is sent to a transimpedance amplifier (TIA), followed by a limiting amplifier (LA), and the signal from the LA is sent to either a bit-error-rate tester (BERT) (for BER measurements, shown in Fig. 5.2) or a DCA (for eye diagram measurements, shown in Fig. 5.3).

5.2.2 Detector sensitivity

The receiver sensitivity curves for the L = 250 μm device at 5 V, 10 V, and 15 V biases are shown in Fig. 5.2(a,b) for 2.5 Gb/s and 10 Gb/s data reception, respectively. Receiver sensitivity curves for the L = 3 mm device at 2.5 Gb/s are shown in Fig. 5.2(c). The power shown in Fig.

5.2 is the power being launched on-chip from the LTF (measured on the 1/99 tap), and does not take into account facet loss from the fan-out tapers [Fig. 5.1(b)]. The facet loss is estimated to be 15 dB/facet for our devices based on measurements of the total fiber-to fiber insertion loss. However, the facet loss has previously been reported to be as low as 7 dB ± 2 dB/facet [66], and thus the sensitivity of the device is expected to be decreased by 7 to 15 dB from the on-chip launch power. We believe that the discrepancy between our measured facet loss and the previously reported value is due to imperfections in the facet caused by polishing.

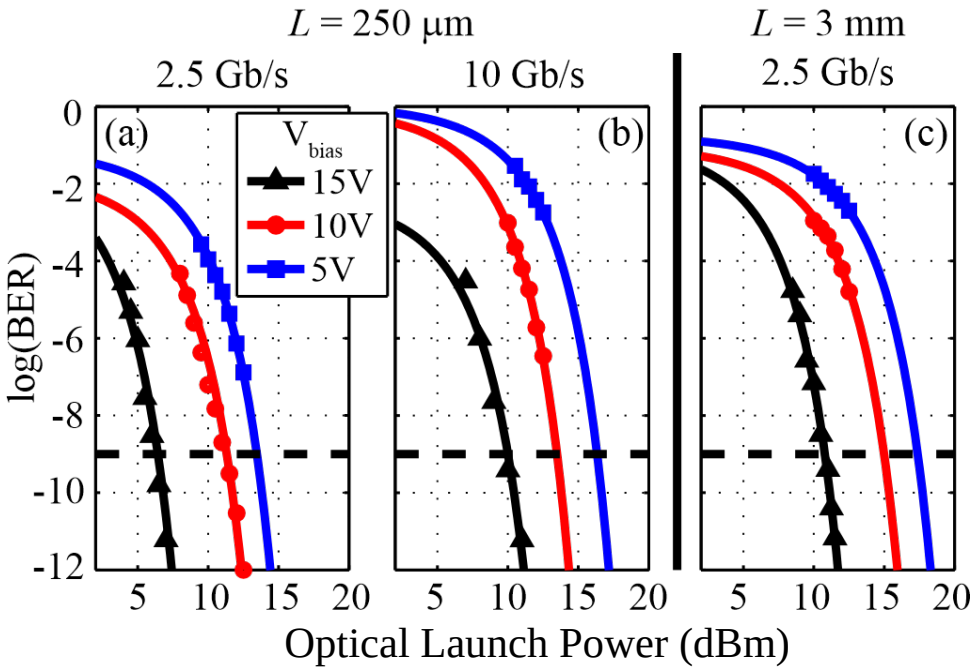

Figure 5.2. Receiver sensitivity curves for (a) the L = 250 μm device at 2.5 Gb/s, (b) the L = 250 μm device at 10 Gb/s, and (c) the L = 3 mm device at 2.5 Gb/s. The launch power shown in dBm is the power launched on-chip from the LTF, not including facet loss.

We demonstrate error-free operation at 10 Gb/s for a 15V bias, and at 2.5 Gb/s at 15V and 10V biases. For the L = 250 μm device the sensitivity at 2.5 Gb/s is measured to be 7.4 dBm and 12.3 dBm for the 15V and 10V biases, respectively. At 10 Gb/s, the sensitivity is 11.1 dBm when biased at 15V. For the L = 3 mm device the sensitivity at 2.5 Gb/s is measured to be 11.7 dBm at 15V bias. The data points in Fig. 5.2 have been fit with the complimentary error function [144]

using nonlinear least squares curve fitting. The eye diagrams for the detected signal after the TIA-LA are shown in Fig. 5.3, with the error-free cases shown in a red outline. Error-free operation is achievable at lower bias voltages; however a redesigned coupler is required to decrease the necessary launch power. Additionally, the contacts can be redesigned to increase the internal field in the device, and the L2 absorbing state can be used to improve sensitivity, as discussed in the following sections.

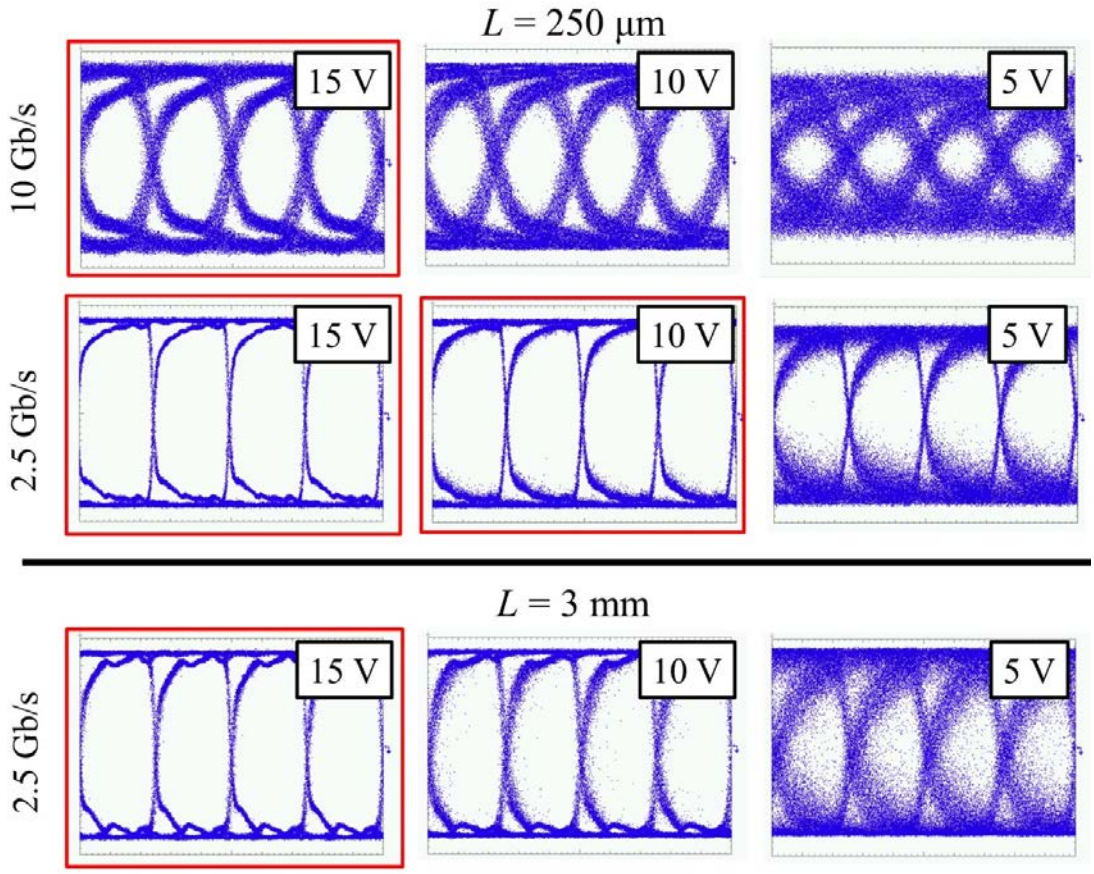

Figure 5.3. Eye Diagrams for the L = 250 μm and L = 3 mm devices for 5V, 10V, and 15V reverse bias voltages, taken after the TIA-LA. Red outlines signify error-free operation.

5.2.3 L1, L2, and initial state photocurrent

The photocurrent generated in the Si^+ ion implanted Si NWWG PDs is believed to be due to interstitial clusters that form after processing the devices at 475°C [64], which allow for mid-bandgap transitions of photo-excited carriers. It has previously been shown that these absorbing

defects have two stable states, which are labeled L1 and L2 [64]. The PD can be brought into the L1 state, which has a relatively weak absorption coefficient of α = 8 dB/cm, by heating at 250°C for 10s. Subsequently, the detector can be brought into the L2 state, which has a larger absorption coefficient of α = 18-23 dB/cm, by forward biasing the device at a current of 200 mA per cm of device length [65]. In the "initial" state, which is simply the device as fabricated, the generated photocurrent lies between the L1 and L2 state, as shown in Fig. 5.4 for the L = 250 μm device. The DC photocurrent shown in Fig. 5.4(a) is found by launching a 17 dBm CW signal on-chip from a LTF and measuring the generated photocurrent on a picoammeter as a function of reverse bias voltage applied by a DC power supply. The receiver sensitivity measurements presented in the previous section were performed using the device in the initial state; however, our photocurrent measurements show that a > 15 dB receiver sensitivity improvement at all measured bias voltages can be expected by operating the photodiodes in the L2 state as compared to the initial state.

The dark current shown in Fig. 5.4(a) ranges from 6.7 nA at 5 V reverse bias to 136.2 nA at 15 V reverse bias, which is substantially less than the 10's of μAs [135,136] reported for typical Ge detectors. The dark current in Ge detectors results from dislocation defects in the Ge layer however, CMOS compatible Ge detectors fabricated by selective area deposition have recently been demonstrated with 3 nAs of dark current at 1 V bias [137]. These devices require a large number of fabrication steps, back-end Ge integration, and a thermal budget of 630°C, while achieving comparable dark current and responsivity to the simpler to fabricate Si^+ ion implanted Si NWWG PDs.

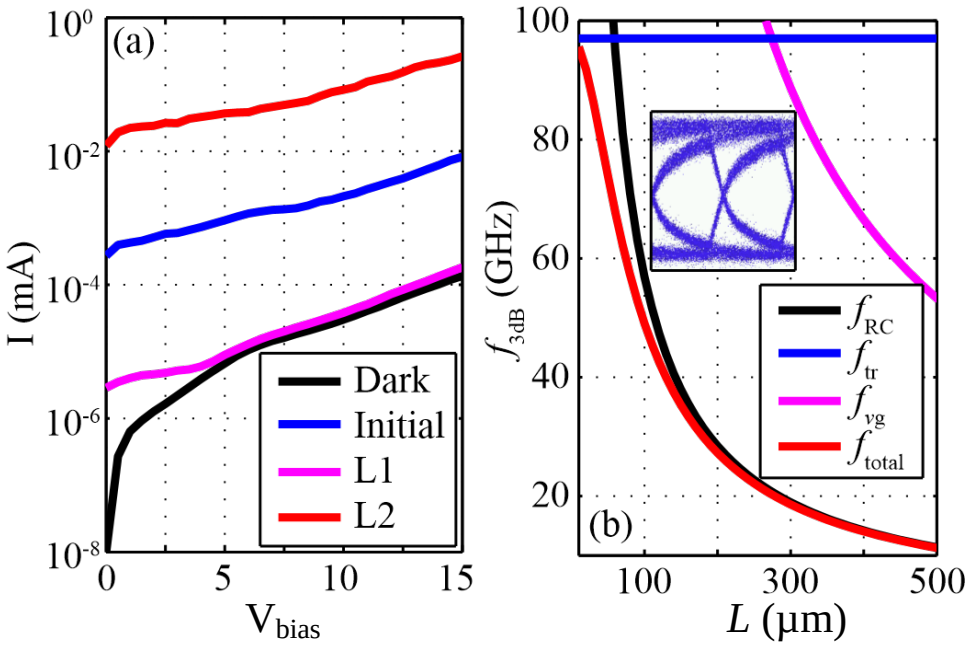

Figure 5.4. (a) Measured dark current and photocurrent for the L = 250 μm device in the initial, L1, and L2 states plotted on a log scale as a function of reverse bias voltage V_{bias} with 17 dBm CW input power at λ = 1.55 μm, and (b) calculated 3dB frequency of the PD as a function of device length L, decomposed into it's constituent components. The eye diagram of the L = 3 mm device (*inset*), shows that the PD is RC-time constant limited.

5.3 DISCUSSION

5.3.1 Receiver Sensitivity

The receiver sensitivity of the L = 250 μm PD at 10 Gb/s [shown in Fig. 5.2(b)] can be improved by > 15 dB when utilizing the PD in the L2 state, as shown in the previous section. Assuming that the PD is being operated in the L2 state, and taking in to account the 7 to 15 dB facet loss, the on-chip sensitivity for the Si NWWG PD is predicted to be between -20 and -12 dBm for BER = 10^{-9} at 10 Gb/s with 15V bias. Thus, our on-chip sensitivity is comparable to the -14 dBm sensitivity of the Ge PD measured in [136] for BER = 10^{-9} at 10 Gb/s with 3.2V bias. While the device footprint and bias voltage required for the Si^{+} implanted Si NWWG PD are large compared to the Ge PD for a comparable sensitivity, the footprint can be decreased by utilizing RCE [73,77,142,143] and the required bias voltage can be lowered by redesigning *p-n*

doped wings, or by using a metal-semiconductor-metal (MSM) configuration to achieve a larger internal field for the same applied bias.

5.3.2 Frequency Response

The calculated 3dB frequency of the diode as a function of device length is shown in Fig. 5.4(b), where the 3dB frequency has been decomposed into its constituent components: the transit-time limited bandwidth f_{tr}, the group velocity limited bandwidth f_{vg}, and the RC time constant limited bandwidth f_{RC}. The carrier transit-time is calculated to be ≈ 97 GHz with an assumed carrier saturation velocity of intrinsic Si (v_{sat} = 1×10^7 cm/s) by using the commercially available LaserMOD software package from RSoft Design Group, Inc. [127], which numerically solves the Boltzmann transport and Poisson equations for a 2D cross-section of the PD [Fig. 5.1(b)]. Note that the carrier transit time depends only on the spacing of the *p*-*n* junction, and not on *L*. The group velocity limited bandwidth is calculated using v_g = 7×10^9 cm/s and the method of [65,142] with an assumed absorption coefficient of α = 28 dB/cm (20 dB/cm for ion implanted absorption and 8 dB/cm for free carrier absorption in the *p* and *n* doped wings [65]), while the RC time constant limited bandwidth is found by linearly fitting the measured device capacitance values for the L = 250 μm and L = 3 mm devices [64] to find a capacitance per unit length of .53 fF/μm, and assuming a 50Ω load.

It can be seen from Fig 5.4(b) that the total electrical bandwidth of this device geometry follows closely with the RC time constant limit, deviating only at short devices lengths of L < 200 μm. For the measured device capacitances, the RC time constant limits the PD electrical response to ≈ 21 GHz for the L = 250 μm device, and ≈ 2.1 GHz for the L = 3 mm device. The eye diagram of the L = 3 mm device before the TIA-LA is shown in Fig. 5.4(*inset*), where it can be seen that the decay time of the signal is longer than the bit slot. For a 2.5 Gb/s signal, the bit

slot is 400 ps, while the decay time for a 2.1 GHz RC-limited device corresponds to ≈ 470 ps. Thus, the device geometry tested is RC time constant limited, with the capacitance increasing linearly with device length. At L = 3 mm the frequency response limitation of 2.1 GHz causes a sensitivity penalty as compared to the L = 250 μm device which out-weighs the increase in responsivity gained by increasing L. Device capacitance must be minimized to over-come this sensitivity penalty for the L = 3 mm device, and for the L = 250 μm device to operate at higher data rates.

The frequency response of the devices can be substantially increased by optimizing device geometry to decrease the total device capacitance [144,145]. If the capacitance of the L = 3 mm device is decreased to $C \leq 0.362$pF, the frequency response is limited to f_{3dB} = 8.8 GHz by the optical group velocity, resulting in a reduction in receiver sensitivity for 2.5 Gb/s operation. Similarly, the L = 250 μm capacitance must be decreased to C =70.7 fF for a 50 GHz frequency response, which is sufficient for 40 Gb/s operation. The ultimate limit for the frequency response of the L = 250 μm device is the transit time limit of ≈ 97 GHz, which requires $C \leq 35.4$ fF.

5.4 CONCLUSION

Error-free operation of an all-Si ion implanted PD operating at 1.55 μm has been demonstrated for 2.5 Gb/s and 10 Gb/s data reception. For the L = 250 μm device error-free operation was achieved for 15V bias at 10 Gb/s and for 15V and 10V bias at 2.5 Gb/s, while error free operation for the L = 3 mm device was shown for 15V bias at 2.5 Gb/s.

Present GE PDs generally offer better performance; however, they impose the significant burden of a challenging materials system. It has been shown that Si^+ implanted Si NWWG PDs have dark currents, responsivities, and sensitivities comparable to reported Ge devices. A

significant improvement in frequency response can be achieved by reducing device capacitance and a >15 dB improvement in receiver sensitivity can be expected by operating the PDs in the L2 state, which will make Si^+ implanted NWWG PDs comparable with Ge PDs. The performance of Si^+ implanted NWWG PDs, and the ease with which they can be integrated into a standard CMOS process flow, makes them an excellent candidate for usage as receivers and in-line power monitors in the Si photonics platform.

SECTION III: LONG WAVELENGTH OPERATION

CHAPTER SIX:
Error-Free Operation of an All-Silicon Waveguide Photodiode at 1.9 μm[3]

6.1 BACKGROUND

High-traffic networks and telecommunication systems requiring increased optical-link capacity have propelled the search for ways to increase link aggregate bandwidth. Techniques utilizing advanced modulation formats, massive wavelength parallelism, and spatial parallelism have led to demonstrations exceeding 100 Tb/s [146-149]. A complementary approach for increasing bandwidth is to utilize wavelengths beyond the standard communications band [150]. Recently, a 10 Gb/s data transmission rate at 1884 nm was demonstrated with Si photonics, opening up the possibility of telecom channels out to 2 μm [150]. However, these long-wavelength (> 1.7 μm) signals pose an inherent challenge for on-chip detection due to the fact that they are beyond the band edge of Ge, the material most often used for integrated Si photonic receivers [136]. Bandgap engineering using super-lattices [83] and bonding of III-V materials [151] can achieve detection at these longer wavelengths, but require processing beyond standard Complementary Metal-Oxide-Semiconductor (CMOS) practices. An alternate approach for long-wavelength data reception beyond the U-band (1625 nm – 1675 nm) is to utilize extrinsic photodetectors (PDs), where sub-bandgap absorption in Si waveguides is induced *via* ion implantation. This additional fabrication step is fully compatible with standard CMOS technology [66].

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[3] This chapter adapted from:

B. Souhan, C. P. Chen, R. R. Grote, J. B. Driscoll, N. Ophir, K. Bergman, and R. M. Osgood, "Error-Free Operation of an All-Silicon Waveguide Photodiode at 1.9μm," IEEE Photon. Technol. Lett. **25**, 2031-2034 (2013).

One structure that has shown promise is based on Si^+ ion implanted waveguide PDs with the primary defect responsible for absorption believed to be the Si interstitial cluster [64]. These devices have been shown to have absorption coefficients up to 20 dB/cm, bandwidths of > 35 GHz, and internal quantum efficiencies (IQE) up to 0.8 A/W at 5 V for an operating wavelength at 1.55 μm [64]. Error-free data transmission of 10 Gb/s operating at 1.55 μm wavelength was recently demonstrated with performance comparable to that of Ge detectors [71,116]. Alternatively, these same devices can be operated utilizing absorption from the Si-divacancy defect, caused by the dislocation of lattice atoms during ion implantation [65,66,88]. Each of these two devices (interstitial and divacancy) have different post-implantation maximum processing temperatures. The interstitial devices are processed at 475°C or higher, whereas the divacancy devices are processed at below 300°C [65]. Although the IQE of the divacancy defect is lower (0.2 A/W at 5 V [66] compared to 0.5-0.8 A/W for interstitial clusters [64,66]), it has a waveguide absorption coefficient ranging from 100 to 200 dB/cm [65,66,88]. The increase in absorption offsets the lower quantum efficiency and affords for shorter devices, resulting in higher responsivities for devices of < 250 μm in length. In the original research from Fan and Ramdas on deuteron-irradiated Si, a peak in absorption around 1.8μm was observed for Si divacancy defects [87]. Thus by utilizing devices implanted with Si ions and processed at temperatures below 300°C, detection and data transmission can be achieved at wavelengths up to 1.9μm [72,117] or longer [152].

In this chapter, we demonstrate error-free operation (Bit Error Rate (BER) < 10^{-9}) of a 2 mm-long Si^+ ion implanted waveguide PD with 1 Gb/s data rates at 1.9 μm. The sensitivity of this divacancy device is calculated from the measured data; the responsivity is measured and compared to operation at 1.55 μm. Theoretical analysis suggests operation at 10 Gb/s is possible

with only a 3 dB loss in sensitivity compared to operation at 1.55 μm. To the best of our knowledge, this is the first systems-level demonstration of a monolithic Si waveguide PD operating at wavelengths beyond 1.8 μm.

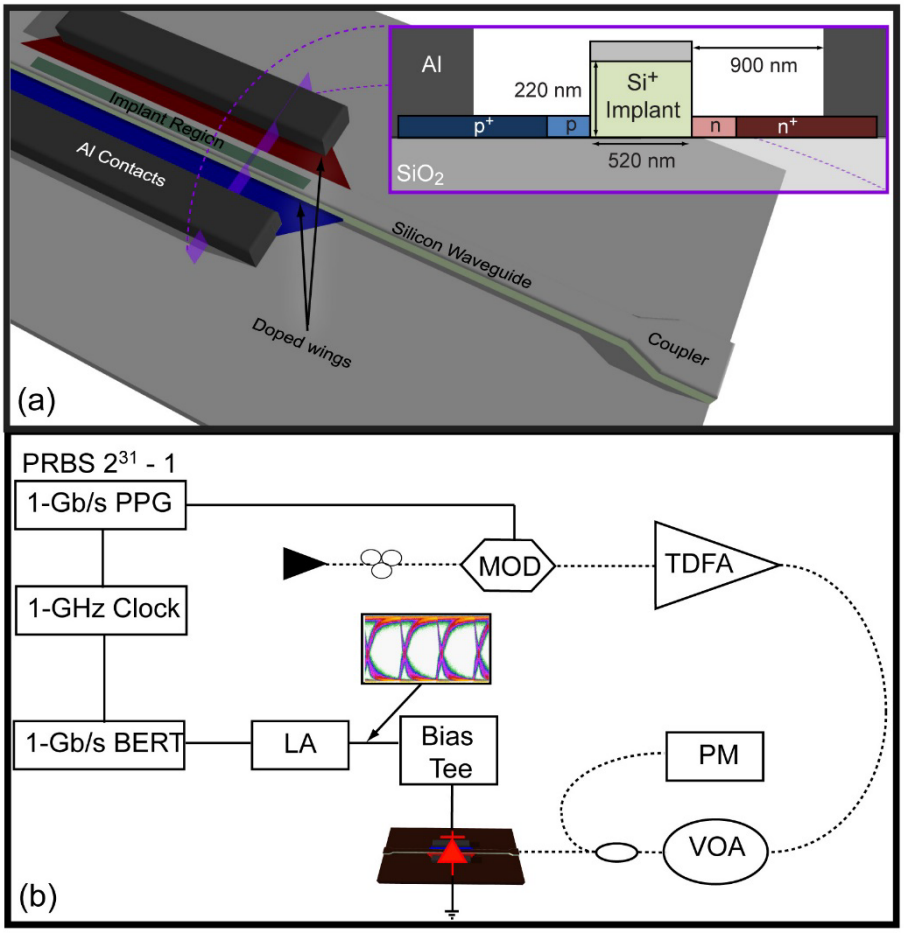

Figure 6.1. (a) Device cartoon indicating waveguide, contacts, wings, implant region, and adiabatically tapered coupler, with inset giving cross-sectional dimensions. The waveguide implant region is doped with a dose of 10^{13} cm^{-2} Si^{+} ions. The "wings" are 50 nm high with the heavily doped regions concentration of 10^{19} cm^{-3} and lower doped regions concentration of 10^{18} cm^{-3}. The contacts are formed with deposited Al and a 10 nm Ti adhesion layer. (b) Experimental setup for measuring BER, with solid lines representing electrical connections, and dashed lines representing fiber.

6.2 MEASUREMENTS AND RESULTS

6.2.1 Experimental Setup

The Si^{+} implanted Si waveguide *p-i-n* PDs were fabricated on the CMOS line at MIT Lincoln Laboratory, as described in [65], with dimensions given in Fig. 6.1(a) and a Si^{+} implantation

energy of 190 keV. As shown in Fig. 6.1(b), 1 Gb/s non-return-to-zero (NRZ) data is generated by a pulse pattern generator (PPG), and used to drive a $LiNbO_3$ modulator, which imparts the signal onto a 1.9μm carrier. The modulated optical signal is then sent to a thulium-doped fiber amplifier (TDFA), and a variable optical attenuator (VOA) is used to control the power being launched on-chip for BER measurements. A 1% power tap after the VOA diverts a portion of the signal to an optical power meter (PM) for input-power monitoring. The optical signal from the VOA is coupled to the waveguide fan-out taper shown in Fig. 6.1(a). The PD is contacted with electrical probes rated for 40 GHz operation, and a 12 GHz rated bias tee is used to apply a DC bias. The electrical data signal is connected to a Limiting Amplifier (LA) and sent to either a bit-error-rate tester (BERT) or digital communications analyzer (DCA) for eye diagram measurements [Fig. 6.2(a) inset]. A C-V analyzer (not shown) is used to measure PD capacitances.

6.2.2 Results

The Si^+ implanted Si waveguide receiver sensitivity curve for a 2 mm PD is shown in Fig. 6.2(a) at a 25 V reverse bias, with the power shown giving the off-chip launched power measured using a 1/99 tap. Total input and output facet loss is measured to be 27 dB utilizing transmission tests through straight waveguides at 1.55 μm. Photocurrent is then measured after alternating the side of the input. Since the measured difference in photocurrent is less than 1dB, the loss from each facet is taken to be equivalent, resulting in a ≈ 13.5 dB facet loss. An additional 3 dB of loss is assumed due to an on-chip power splitter prior to the PD.

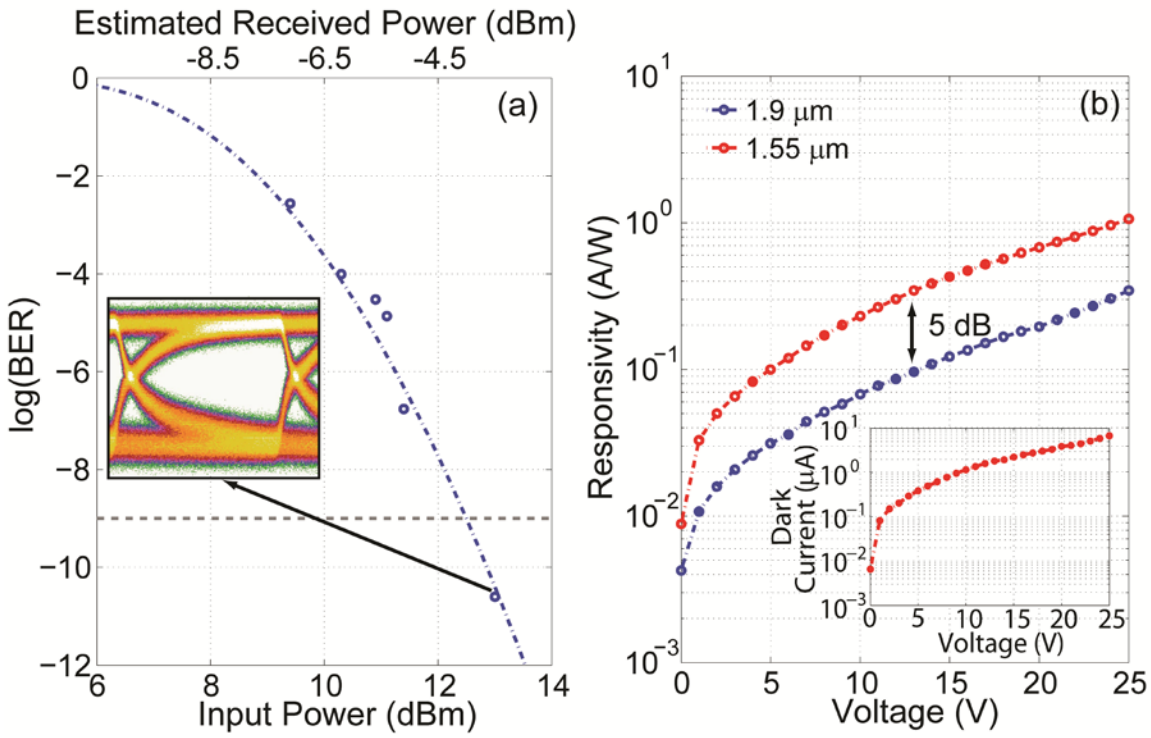

Figure 6.2. (a) Sensitivity curve for a 2 mm-long PD operating with a 25V reverse bias at 1Gb/s. Input power shown is the input power prior to coupling into chip. The received power is 16.5 dB down due to coupling and on-chip power splitter losses. (inset) Eye diagram for a 13.5 dBm input power. Eye is clearly open both horizontally and vertically corresponding to error-free operation. (b) Calculated responsivity versus voltage based on measured coupling loss, splitter loss, and 100% absorption. A ≈5 dB penalty was seen between 1.9 μm and 1.55 μm operation. (inset) Dark current vs reverse bias for device.

Error-free operation is demonstrated at 1 Gb/s for the 2mm device at a 25 V bias. The 25 V reverse bias provides enough current gain to drive the LA, overcoming significant optical losses of the non-optimized device. It is believed the device is operating in avalanche mode at this high bias similar to devices in [65]. The measured data is fit with a complimentary error function using nonlinear least-squares curve fitting, in order to attain a sensitivity estimate for the device [144]. Sensitivity is measured to be 12.4 dBm (-4.1 dBm after accounting for average coupling loss) for the 2 mm PD. The eye diagram measured prior to the LA for an error-free case is inset in Fig. 6.2(a), and shows data rate is limited by frequency response. Measured dark current (inset of Fig. 6.2(b)) is nearly two orders of magnitude less than the photocurrent, having negligible impact on device sensitivity.

Responsivity at both 1.9 μm and 1.55 μm is measured and shown in Fig. 6.2(b). The photodetector operation at 1.9 μm shows a ≈ 5 dB loss in responsivity throughout the reverse bias range measured. Improved on-chip performance can be achieved by redesigning the waveguide and photodiode for operation at 1.9 μm instead of 1.55 μm.

6.3 DISCUSSION

6.3.1 Responsivity

In [14] the divacancy defect showed peak absorption strength at 1.8μm with a measured absorption coefficient at 1.9 μm averaging 1.45 times higher compared to that at 1.55 μm for both implanted doses of deuterium. Based on previous measurements of the absorption coefficient at 1.55 μm being ≈ 100 dB/cm [66], the absorption coefficient at 1.9 μm is assumed to be ≈ 145 dB/cm. With >99% of the power absorbed in the 2 mm device at 1.55 μm and 1.9 μm, the measured responsivity at 1.9 μm is expected to be equivalent to the responsivity at 1.55 μm, assuming that all other parameters are equal. To account for the difference between measured and expected responsivity values, Finite Element Method (FEM) analysis is utilized to determine the confinement factor, Γ, and the parasitic loss per unit length, α_{pl}, as a function of wavelength for the PD with dimensions as given in inset of Fig. 5.1(a). Free-carrier effects in the wings of the device are modeled using data from [42]. The Sellmeier coefficients [153] are used for the intrinsic-Si regions and for the buried oxide and SiO_2 cover layers; the coefficients for the Al contacts are from [154]. The calculated Γ and α_{pl} are plotted as a function of wavelength in Fig. 6.3.

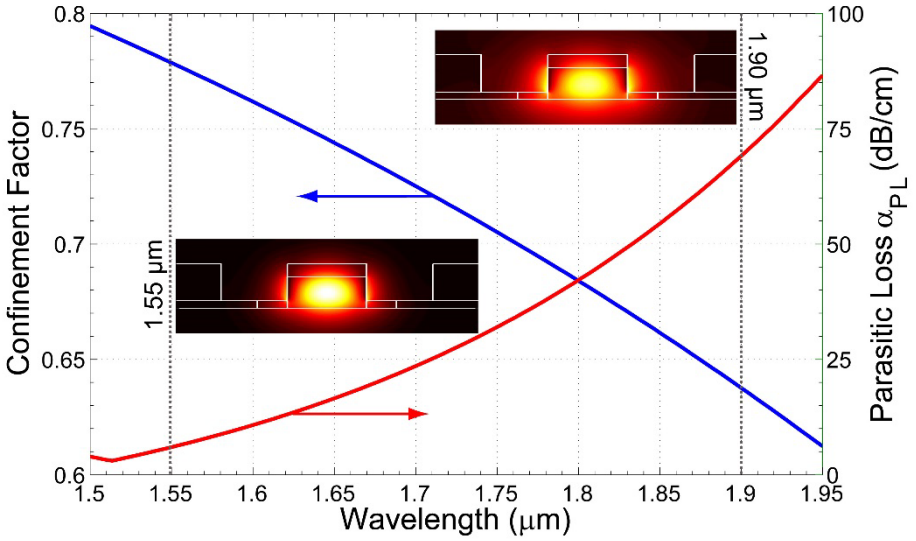

Figure 6.3 Confinement factor (red - dashed) and parasitic loss (blue) as a function of wavelength. Insets show guided mode at 1.55 μm and 1.9 μm.

The calculated α_{pl} at 1.55 μm is found to be 5.5 dB/cm, matching well with previous measurements of 8 dB/cm [64] for the same PD structure. The parasitic loss is increased significantly as Γ is decreased due to the increased overlap of the field with the doped wings. This increase in overlap results in an α_{pl} at 1.9 μm of 16 dB/cm as Γ decreased to 0.637.

The responsivity, $\Re$, is calculated assuming > 99% absorption and using the expression

$$\Re = \Gamma \cdot \zeta \cdot \alpha_{abs}/(\alpha_{abs} + \alpha_{pl}) \tag{6.1}$$

where ζ is the IQE, and α_{abs} is the absorption coefficient. The ratio between α_{abs} and α_{pl} is considered separate from IQE to account for the percentage of power absorbed versus loss due to varying α_{pl}. The increase in α_{pl} and decrease in Γ accounts for nearly 25% of the measured difference.

The change in facet loss between the Lensed Tapered Fiber (LTF) and the waveguide fan-out taper is estimated by computing the overlap integral of the LTF with the coupler modes. The mode from the LTF is estimated utilizing a Gaussian profile with the manufacturer specified spot

size at 1.55 μm of 2.5 μm [20]. The mode profile at 1.9 μm is estimated to be approximately 20% larger, matching closely with the change in mode profile in the coupler and resulting in an estimated change in coupled power of less than 0.5 dB.

The remaining difference between the theoretical and measured responsivity at 1.9 μm is either from a change in IQE at 1.9 μm compared to 1.55 μm, or due to a wavelength dependent change in the absorption coefficient under thermal annealing.

To optimize the design of the PD for operation at 1.9 μm, FEM analysis is used to examine both the confinement factor and parasitic loss as a function of waveguide height and width. Utilizing the calculated terms, the responsivity,

$$\Re = \Gamma \cdot \zeta \cdot \alpha_{abs} / \left(\alpha_{abs} + \alpha_{pl}\right) \cdot e^{-\left(\alpha_{abs}+\alpha_{pl}\right)\cdot L}, \tag{6.2}$$

is maximized. A PD length of 250μm is assumed, allowing direct comparison to the interstitial-based PD previously demonstrated for a 10 Gb/s data rate in [71,116]. Fig. 6.4 shows the surface plot of the calculated responsivity at 5 V as a function of waveguide width and height for an assumed device length of 250 μm. The maximum responsivity of 38 mA/W is generated by a device that is 0.66 μm wide by 0.24 μm high and is within 3 dB of the calculated responsivity of 72 mA/W for the tested device at 1.55 μm. Further, this 1.9 μm divacancy device compares well with calculated responsivity of between 54 to 86 mA/W at 1.55 μm of the 250 μm interstitial device in [71,116], based on the measured absorption coefficient and IQE [64].

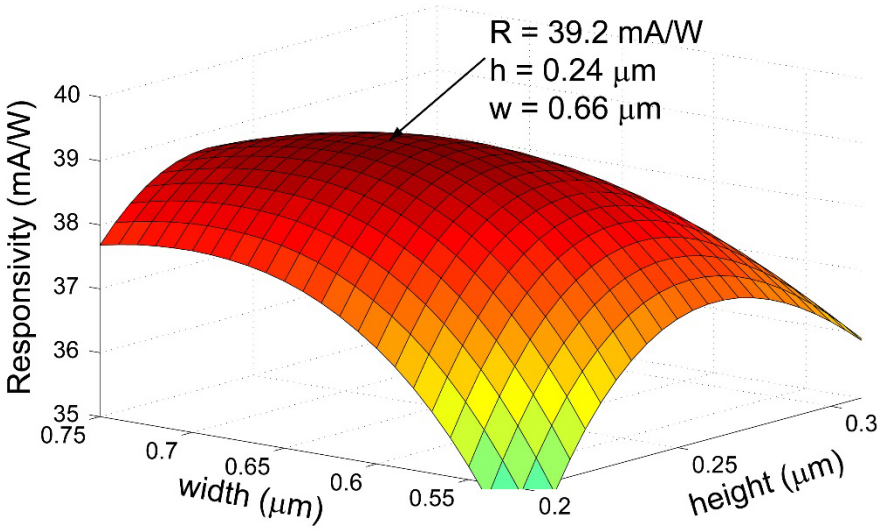

Figure 6.4. Responsivity at 1.9 μm as a function of both height and width. A peak is reached for a height of 0.24 μm and a width of 0.66 μm. Expected responsivity for this device at 1.55 μm is 72 mA/W and for an interstitial device is between 54 to 86 mA/W.

6.3.2 Frequency Response

To determine the impact of optimizing the waveguide structure for operation at 1.9 μm, the individual frequency response components of the device are analyzed, focusing on carrier-transit time, optical-transit time, and device capacitance. The total frequency response of the PD is then calculated from $f_{tot}^{-2} = (f_{transit}^{-2} + f_{optical}^{-2} + f_{RC}^{-2})$.

A commercial simulation package (LaserMod [127]) is used to solve Poisson's equation and the Boltzmann transport equations for the given and optimized device structures to estimate carrier-transit time. A 0.2 ps Gaussian pulse is used to simulate the PD impulse response. The resultant current pulse is then Fourier transformed to get the estimated carrier-transit frequency response. The carrier-transit frequency response, assuming velocity saturation, for the PD with dimensions in Fig. 6.1(b) is calculated to be ≈100 GHz, matching well with previously calculated values of 95 GHz [64]. The response dropped to ≈ 78 GHz for the optimized device due to the

increased aggregate transit length. Although this value is not insignificant, its impact on overall PD frequency response is shown to be minimal.

The frequency response for optical-transit time is based on device length, group velocity, and absorption coefficient, and can be found utilizing the transfer function from [64]:

$$\frac{P(\omega)}{P(0)} = \frac{{v_g}^2\alpha^2}{F^2(\omega^2 + {v_g}^2\alpha^2)}\left[1 - 2(1-F)cos\left[\frac{\omega \ln(1-F)}{v_g\alpha}\right] + (1-F)^2\right] \qquad (6.3)$$

where $\omega = 2\pi f$, α = attenuation coefficient in cm^{-1} (including absorption and parasitic loss), v_g is the group velocity in cm/s, and F is the percentage of light absorbed by the guide. Group velocities are found through FEM analysis, with the optimized PD having a $v_g = 7.5 \cdot 10^9$cm/s at 1.9μm, and the tested PD having $v_g = 7.3 \cdot 10^9$ cm/s at 1.55 μm. The calculated optical-transit frequency response is 137 GHz for a 250 μm optimized PD operating at 1.9 μm and 131 GHz for a 250 μm PD with the dimensions given in Fig. 6.1(b) at 1.55 μm. For the interstitial device demonstrated in [71,116], the calculated optical-transit time is 129 GHz, with a slight decrease in frequency response due to the lower absorption coefficient. The slight differences across the devices have little impact on the final calculated frequency response below.

Frequency response due to capacitance is found based on a 50-Ω load, with the wing resistance assumed to be negligible. Capacitance is measured for several device lengths resulting in a capacitance versus length relation of ≈ 0.34 pF/mm utilizing a Keithley 590 CV analyzer at 100 kHz. For the PD with width and height as tested and a length of 250 μm, the calculated frequency response is 37 GHz. To determine the impact of the optimized PD's width and height, capacitance is calculated for the diode by using LaserMod simulation software and for the contact structure and wings by using conformal mapping technique [155]. The calculated capacitance for the PD with dimensions as tested is found to be 0.27 pF/mm, matching within

20% of the measured values. Utilizing the same technique on the modified structure resulted in an approximate 4.5% decrease in capacitance. Decreasing the measured capacitance values by 4.5% results in an estimated frequency response of 39GHz for the optimized PD dimensions.

The total frequency response for the optimized PD and the tested PD of 250 μm length is calculated to be 33.8 GHz and 33.5 GHz, respectively. The decrease in response due to an increase in transit time is offset by a slightly lower capacitance and slightly higher v_g.

6.4 CONCLUSION

An all-Si ion-implanted waveguide PD has been demonstrated with 1 Gb/s error-free data reception at 1.9μm. To the best of our knowledge, this is the first demonstration of a monolithic Si waveguide PD operating at wavelengths beyond 1.8 μm. Responsivity at 1.9 μm was found to be 5 dB less than at 1.55 μm, with nearly 25% of the penalty coming from an increase in parasitic loss and a decrease in modal confinement.

A theoretical analysis optimized the waveguide for operation at the longer wavelength. The modified PD was compared to a previously demonstrated interstitial-based PD, with the new structure showing near identical frequency response and a 3 dB penalty in responsivity. Based on this analysis, 10 Gb/s error-free data reception is theoretically achievable for this modified device operating with wavelengths from 1.55μm to 1.9μm and with an estimated loss in sensitivity at 1.9 μm of only 3 dB, enabling high-data-rate long-wavelength communications on-chip.

CHAPTER SEVEN:
Si^+-implanted Si-wire waveguide photodetectors for the mid-infrared[4]

7.1 BACKGROUND

Recently, the inherent transparency of integrated Si photonic structures to both single- and two-photon absorption experiments and applications in the mid-infrared (IR) range ($\lambda = 2 - 5$ μm) has begun to be utilized, giving rise to new applications in chemical and biological sensing, free-space communications, and spectroscopy [156]. Additionally, this wavelength region holds promise for yielding new spectral bands for optical communication systems [156]. The introduction of thulium-doped fiber amplifiers designed to operate in the 2 μm range has been shown to facilitate the use of additional communication bands beyond 1.3 μm and 1.55 μm [72,150], while the investigation of several materials and components is also underway for use in the 2 μm – 3 μm range [84-86,157-159], including hollow-core fiber technology that has recently been shown to be applicable for transmission systems at even longer wavelengths [160].

Currently, the majority of mid-IR photonic systems have been composed of discrete components rather than a truly integrated system [156]. One vital component for a complete integrated system is an integrated photodetector (PD). Several researchers have demonstrated heterogeneously integrated detectors for the mid-IR made from GeSn [158], GaSb [158], PbTe colloidal quantum dots [158] and PbTe photoconductors using chalcogenide glass waveguides [84]. While many of these devices exhibit high responsivities, the heterogeneous integration of

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[4] This chapter adapted from:

B. Souhan, R. R. Grote, C. P. Chen, Hsu-Cheng Huang, J. B. Driscoll, M. Lu, A. Stein, H. Bakhru, K. Bergman, W. MJ Green, and R. M. Osgood, "Si^+-implanted Si-wire waveguide photodetectors for the mid-infrared," Optics Express **22**, 27415-27424 (2014)

binary materials incorporated into a Si photonic system requires additional processing beyond traditional Complimentary-Metal-Oxide-Semiconductor (CMOS) processes.

Alternatively, ion implantation is well known to create optically active sub-bandgap trap-states in Si due to a variety of lattice defects, including divacancies, vacancy-oxygen complexes, and Si interstitial clusters; note that this process is distinct from substitional doping used pervasively in doping for Si electronics which can also be used for mid-infrared detection [161]. The formation of these different defects depends on the annealing temperature and implant species, and this approach has been utilized extensively to make on-chip Si nano-wire waveguide (Si NWWG) PDs for 1.55μm [64-71,116,162]. These ion-implanted Si NWWG PDs have been used in numerous systems including data interconnects [7,116], power monitors [67], wavelength monitors [68], thermal device stabilization controllers [69], and variable optical attenuators [70]. These devices are known to exhibit high frequency response, low dark current, and responsivities greater than 1 A/W [64], making them ideal for numerous applications.

Only recently have ion-implanted PDs been explored for the mid-IR band with the demonstration of both boron and zinc implanted Si NWWG *p-i-n* PDs [85,86,157]. Responsivities of 1.7 mA/W was seen for the boron implanted PDs (reverse bias unknown) [157], and as high as 87 mA/W (20V reverse bias) [85,86] was seen for the zinc implanted PDs at a wavelength of 2.2 μm. Furthermore, PD operation is expected out to 3.3 μm based on experimental data from deuterium implanted Si for PDs [87].

In this chapter, *p-i-n* PDs based on a Si rib-waveguide geometry with a 520 nm × 220 nm channel section and 50 nm 'wings' as shown in Fig. 7.1 are used to characterize CMOS compatible Si^+ ion-implanted Si NWWGs at $\lambda = 2.2 - 2.3$ μm for different annealing temperatures and implantation conditions. The Si^+-implanted devices measured in this paper

varied in responsivity (λ = 2.2 μm) from 5 – 10 mA/W after annealing at 200˚C and 2.5 – 7 mA/W after annealing at 350˚C; both at a 5 V reverse bias. Further, internal quantum efficiencies (IQE) ranging from 2.7% − 4.5% for a 5 V reverse bias are calculated. The detector's frequency response is measured to be 1.7 GHz, limited by an un-optimized RC time constant. The dark current is found to be as low as 8.5 pA at 0 V to 3.55 nA at 10V for a 250 μm length device annealed at 350˚C. The demonstrated device characteristics, combined with the relatively simple additional processing requirements, illustrate the potential benefits of using Si^+ implanted detectors in various long-wavelength integrated-Si-photonic applications.

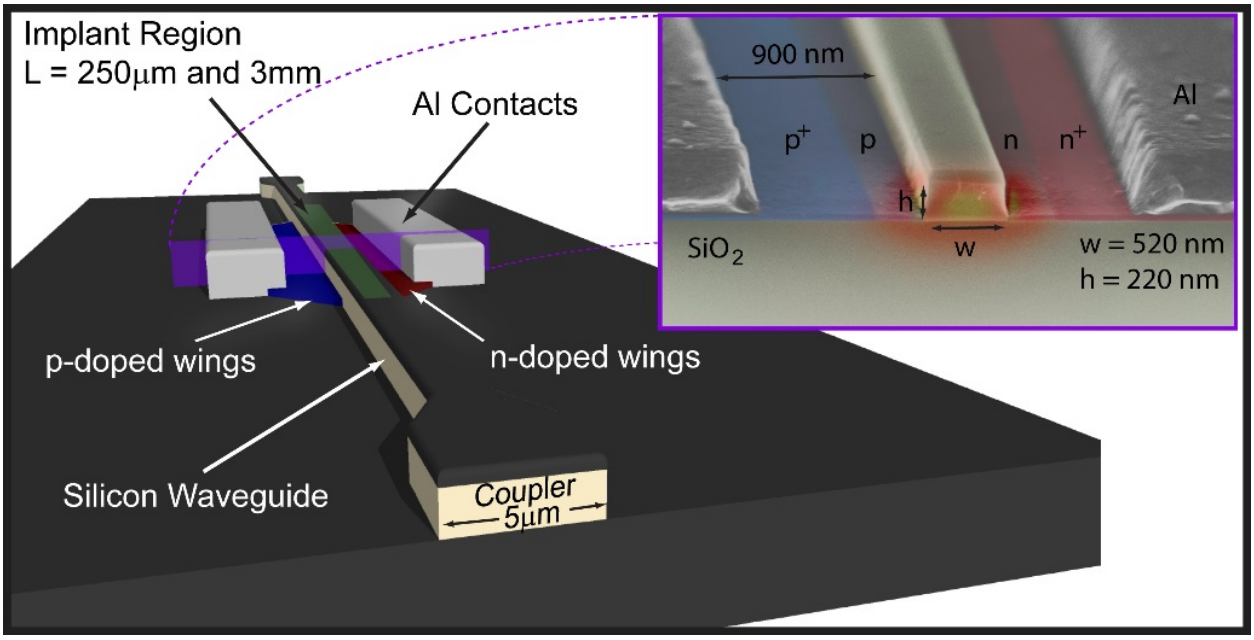


Figure 7.1. Sketch of the device with inset showing a false color SEM cross-section of a *p-i-n* device with the calculated mode at 2.2 μm incident on the waveguide.

7.2 DEVICE DESIGN AND FABRICATION

The *p-i-n* devices were fabricated at MIT Lincoln Labs as described in [66] and Chapter 3. The Si waveguide channel was 520 × 220 nm with 50 nm high 'wings' for the electrical connection to the contacts. The contacts consisted of 300 nm Al on top of a 10 nm W adhesion layer. Coupling onto and off of the chip was accomplished through 5 μm wide fan out tapers. Due to

the low absorption coefficient of the devices, not all of the optical power was absorbed, allowing for transmission measurements through the devices. The 'wings' were doped with concentrations of 10^{19} cm^{-3} and 10^{18} cm^{-3} for the p^+, n^+ and p, n regions respectively. Additional rib and channel waveguides for basic absorption-coefficient measurements were fabricated as described in [162] with channel dimensions for both of 650 × 220 nm and 73 nm 'wings' for the rib waveguides. These waveguides were not made into PDs, only undergoing the ion-implantation process, with no doping or contacts to minimize parasitic losses. Both sets of devices were subsequently masked to open windows ranging from 250 μm to 3 mm in length and implanted at the Ion Beam Laboratory, at the State University at Albany. The implantation dose was 1×10^{13} cm^{-2} Si^+ with an implantation energy of 190 keV and beam-current densities of ≈ 10 nA/cm^2 and ≈ 15 nA/cm^2. The beam diameter was between 3-4 mm and scanned over a 2 in radius circle, in which the chips were placed. Contact photolithography was used to create an ion implantation mask using Shipley 1811, with a 250 μm – 3 mm by 8 μm window centered over the channel section of the Si NWWG. The implantation energy and dose were based on prior reports of ion-induced defects [64-66] and Stopping Range of Ions in Matter (SRIM) calculations [112] and were chosen such that the defect concentration overlapped maximally with the fundamental quasi-TE waveguide mode. After implantation the devices were annealed in atmosphere at 150°C for 10 minutes and the PD response was characterized. Subsequently, the same PD devices were annealed at an elevated temperature of 200°C for 10 minutes, and characterized again. This process was repeated with annealing temperatures increasing in increments of 50°C up to a final temperature of 350°C. This final annealing temperature was constrained by reflow of the contacts. For photocurrent measurements, three *p-i-n* devices were used with the parameters given in Table 7.1 below.

Table 7.1. Implantation parameters of the three tested PDs.

	Implant Window Length	Implant Energy	Dose	Beam Current Density
PD 1	3 mm	190 keV	10^{13} cm^{-2}	15 nA/cm^2
PD 2	250 μm	190 keV	10^{13} cm^{-2}	10 nA/cm^2
PD 3	3 mm	190 keV	10^{13} cm^{-2}	10 nA/cm^2

7.3 RESULTS AND DISCUSSION

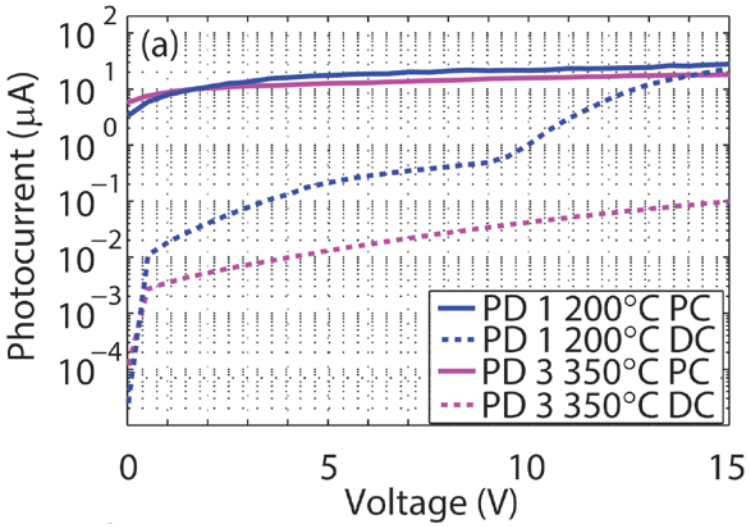
7.3.1 Photocurrent and Linearity

Device measurements were taken utilizing a tunable external-cavity Cr^{2+}:ZnSe laser, operating across a wavelength range from λ = 2.2 to 2.4 μm. A fiber collimator was used to couple light into a standard single-mode fiber, which in turn was connected to a lens tapered fiber (LTF) for coupling light onto the chip. Optical input power was measured at the connection of the SMF and LTF with an infrared optical spectrum analyzer (OSA). An additional LTF was used to couple the output optical power from the chip. Optical output power was measured utilizing an OSA at the end of a 1 m section of SMF. System losses were characterized utilizing several un-implanted straight waveguides on each chip following the procedures described in section 7.4 and section 8.5. Total input optical power losses prior (including LTF loss, coupling loss, and waveguide loss) to the PD were 9.2 – 11.8 dB for PD 1 and 7.9 – 9.7 dB for PDs 2 and 3.

Figure 7.2(a) shows the measured photocurrent for PD 1 (annealed to 200˚C) at λ = 2.2 μm for an incident power of 3.0 ± 1.2 mW, and the photocurrent for PD 3 (annealed to 350˚C) at λ = 2.2 μm with an incident power of 2.7 ± 0.6 mW. The photocurrent measurements exhibited diode-like characteristics, verifying the results were not from photoconduction. Although the photocurrent flattens and is slightly lower for PD 3 after the higher annealing temperature, the corresponding dark current decreased by over an order of magnitude, thus reducing noise

equivalent power improving detector performance and decreasing overall power consumption [124]. The significant increase in dark current seen in PD 1 at 10 V is believed due to the onset of avalanche multiplication, however there is little increase in overall photocurrent, suggesting it is a poor avalanche detector under these implant and anneal conditions.

To measure device linearity, the laser output power was varied via the adjustment of focusing of the free-space-to-SMF connection. The results for PD 1 (200˚C annealing) and PD 3 (350˚C) are shown in Fig. 7.2(b) for $\lambda = 2.2$ μm. It is clear from the unity slope of the graph that the detectors are linear over ≈ 4 decades, from an incident power of ≈ 0.5 μW to ≈ 3.7 mW. Linearity of photocurrent generation with input power was observed for all PDs, annealed at temperatures >150˚C, verifying the defect-mediate absorption is a single-photon process.



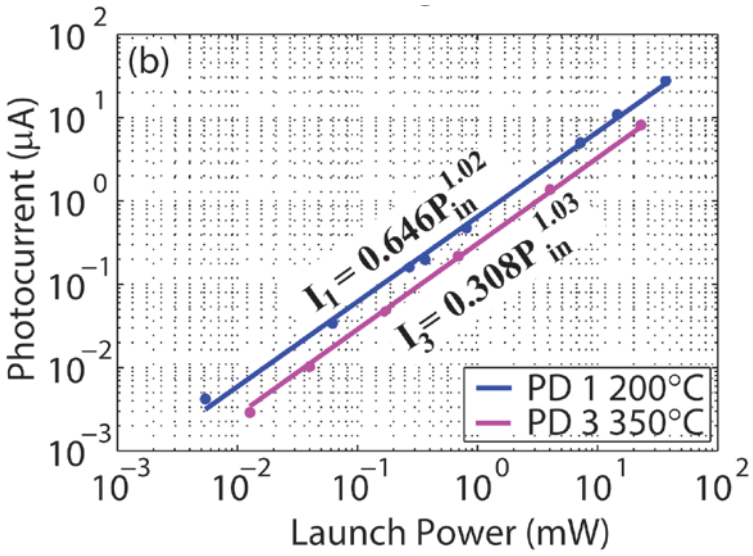


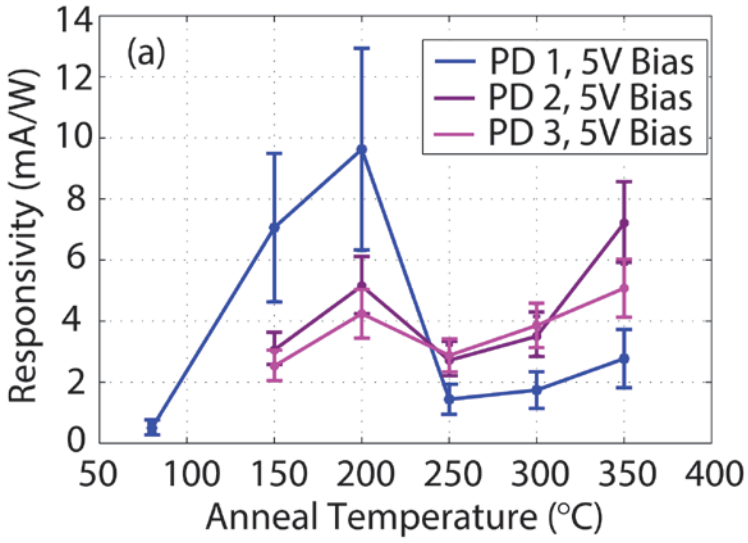
Figure 7.2. (a) Photocurrent and dark current plot for PD 1 annealed at 200˚C with 3.0 ± 1.2 mW launch power and PD 3 annealed at 350˚C with 2.7 ± 0.6 mW launch power. (b) Photocurrent *versus* launch power showing linearity for PD 1 and PD 3 under the same conditions. All measurements were taken at λ = 2.2 μm.

7.3.2 Responsivity

Responsivity was found by subtracting the photodiode dark current from the light current with illumination and dividing by the incident power in the detector, $\Re = \left(I_{light} - I_{dark}\right) / P_{inc}$. Figure 7.3(a) shows the measured responsivity at 5 V *versus* annealing temperature for the three devices. The responsivity curves for all devices show local maxim for 200˚C annealing. As the annealing temperature increased beyond 250˚C, again for all devices, responsivity resumed increasing until the maximum anneal temperature of 350˚C was reached. The peak at 200˚C is believed due to the formation and subsequent annealing of the divacancy defect, as it has previously been observed in ion-implanted PDs in this temperature range [64-66,87] and is also known to anneal out around this temperature [64-66,87]. The cause of the increase in responsivity due to additional annealing above 250˚C is not fully established, however this increase is tentatively attributed, in part, to non-optically active carrier recombination centers annealing out, increasing carrier lifetime and flattening out of the photocurrent seen in Fig.

7.2(a). However, as the divacancy defect is known to anneal out in this temperature range, it is unclear whether the divacancy is still the primary absorption state or if other defect states are contributing, such as surface states or Si interstitials. Further work needs to be done in identifying and characterizing the defects at throughout the different annealing temperatures for Si^+ implanted devices. Additionally, a significant difference was seen between the two different implantation currents, suggesting that implantation current is a critical parameter in determining device characteristics [163], but further study on implantation conditions is required as significant variations have been seen in these devices.

Figure 7.3(b) shows the responsivity as a function of bias voltage for PD 1 after annealing at 200˚C and PD 3 after annealing at 350˚C, along with the responsivity for an un-implanted device. As seen in our photocurrent measurements in Fig. 7.3(a), the additional annealing flattens the response, resulting in only a ≈ 50% loss in responsivity in reducing the bias from 5 to 0 V.



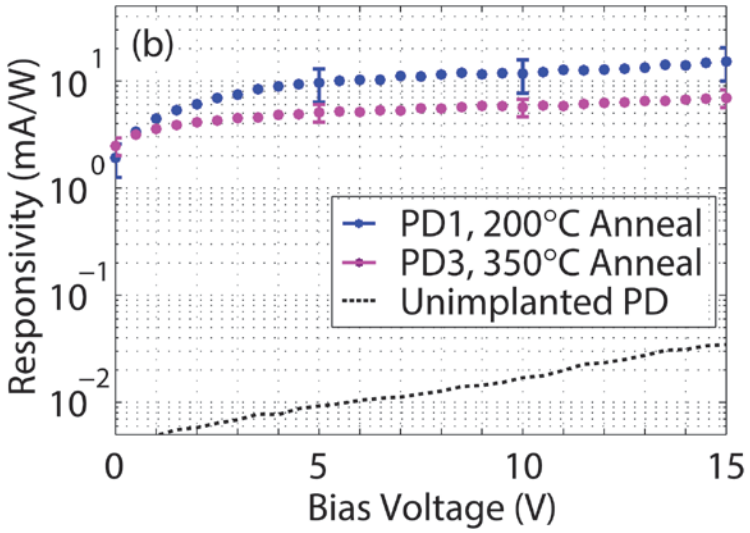


Figure 7.3 (a) Responsivity *versus* annealing temperature for the three devices taken at λ = 2.2 μm. The peak at 200°C is consistent with the formation and subsequent annealing of the divacancy defect. Error bars are based on the measured deviation in measured loss prior to the detector. (b) Responsivity *versus* bias voltage for PD 1 and PD 3 taken at λ = 2.2 μm under different annealing conditions.

7.3.3 Absorption and Internal Quantum Efficiency

Implantation-induced modal absorption coefficients for the waveguides were found using the cutback method on sets of three of different-length ion-implanted rib and channel waveguides. The channel waveguides were implanted under the same conditions as PD 2 and PD 3 (beam current density ≈ 10 nA/cm^2), while the rib waveguides were implanted under the same conditions as PD 1 (beam current density ≈ 15 nA/cm^2). The material absorption coefficients as shown in Fig. 7.4(a) were determined from the measured modal absorption coefficients by doing a parameter scan with a finite-element-method solver. We calculated and plotted the material absorption coefficients, $\alpha_{material}$, in order to compare measurements from different waveguide geometries and bulk data from the literature.

Despite the difference seen in the measured responsivities for waveguides annealed at 200˚C for different implantation conditions, our measured material absorption coefficients were found to be in good agreement. Further, the bulk absorption coefficients at 200˚C of 58 - 73 dB/cm at λ

= 2.2 μm were well matched to ~ 60 dB/cm value reported for bulk Si with deuterium implantation at λ = 2.214 μm [87]. A significant decrease was seen in absorption coefficient with annealing to 350 ˚C, suggesting annealing out of defects.

Device IQE was estimated based on the measured modal absorption coefficients, the measured responsivities, and the PD parasitic loss found by measuring transmission through un-implanted *p-i-n* PDs. Since the *p-i-n* PDs were designed for operation at 1.55 μm, the parasitic losses were significant, ranging from 249 dB/cm to 826 dB/cm for λ = 2.2 to 2.3 μm [85,86].

Responsivity in A/W can be expressed in terms of an external quantum efficiency η_e as: $\Re = \eta_e \cdot \lambda / 1.24$, with λ in micrometers. In the absence of reflection, the external quantum efficiency for a waveguide PD, η_e, is:

$$\eta_i \cdot \alpha_{modal} / (\alpha_{modal} + \alpha_{par}) \cdot (1 - e^{-(\alpha_{modal} + \alpha_{par}) \cdot L}), \tag{7.1}$$

where η_i is defined as the percentage of electron-hole pairs absorbed by photoactive defects that contribute to current (IQE). The ratio $\alpha_{modal} / (\alpha_{modal} + \alpha_{par})$ determines the ratio of photons absorbed *versus* loss to parasitic losses and *L* is the length of the device. Using these equations, η_i was calculated to be between 2.7 ± 0.9% to 4.5 ± 1.1% for a bias voltage of 5 V at λ = 2.2 μm. The large error for the PD 1 at λ = 2.225 μm was a result of the large difference in the measured absorption coefficient at that wavelength and due to limited data. Figure 7.4(b) shows the IQE versus wavelength, with the general trend of decreasing IQE with increasing wavelength. The IQE of PD 2 after annealing at 350˚C appears higher than that of PD 1 despite the lower responsivity at λ = 2.2 μm; note however, that the difference was within the measurement error.

As mentioned earlier, the *p-i-n* devices used for measurements were initially designed for operation at λ = 1.55 μm. With the doping of the wings in close proximity to the waveguide, and

the small contact separation, the parasitic losses of the devices were extremely high. Redesigning the device such that the contacts and doped wing regions are spaced further from the waveguide, such as carried out in [74], will enable the parasitic losses to be significantly reduced. If parasitic losses are reduced to ~ 7 dB/cm, responsivities ≈ 60 – 70 mA/W are possible based on the measured absorption coefficients and calculated IQEs. Avalanche multiplication, as demonstrated in [74] for λ = 1.55 μm operation, may lead to even greater responsivities.

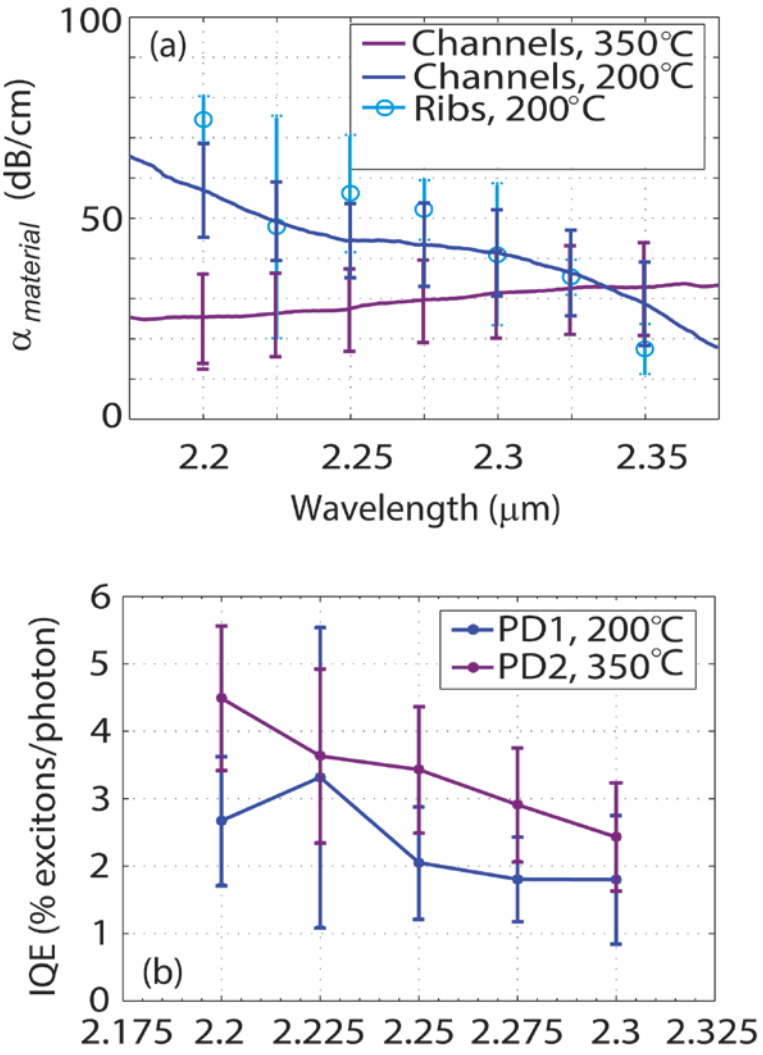


Figure 7.4. (a) Measured absorption coefficients for implanted channel and rib waveguides. Error bars for the channel waveguides ranged from a minimum error of ≈ 11 dB/cm occurring at 2.35 μm to ≈ 14 dB/cm occurring at

2.2 μm, while varied significantly for the rib guides, ranging from 6 to 27 dB/cm. Due to lower losses of the channel guides, the laser amplified spontaneous emission was used for measurements resulting in a continuous spectral function. (b) Calculated IQE for PD 1 after annealing at 200˚C anneal and PD 2 after annealing at 350˚C.

7.3.4 Frequency Response

A lightwave component analyzer (LCA) in conjunction with an EOSpace long-λ (2-μm) $LiNbO_3$ modulator [164] was used to determine the frequency response of PD 2 and PD 3 after annealing each to 200˚C. The normalized responsivities using 50 Ω loads were measured versus frequency. A bias voltage of 20 V was used along with λ = 2.2 μm for PD 2, while a bias voltage of 25V was used for PD 3 due to its lower responsivity. The increase in frequency response seen for a decrease in length suggested the devices are resistance-capacitance limited, which was also seen for similar devices at shorter wavelengths [65,66]. Simple calculations show that given the waveguide dimensions, the electric field from a 20 V bias would be sufficiently high for the carriers to reach saturation velocity, despite the reduction in carrier mobility in ion implanted regions [162]. With device optimization, including limiting implantation to the waveguide region, so as to mitigate implantation-induced RC degradation, frequency responses of greater than 10 GHz are expected. Such an improvement was demonstrated in [65,66] for similar but shorter-wavelength SiWG photodiodes.

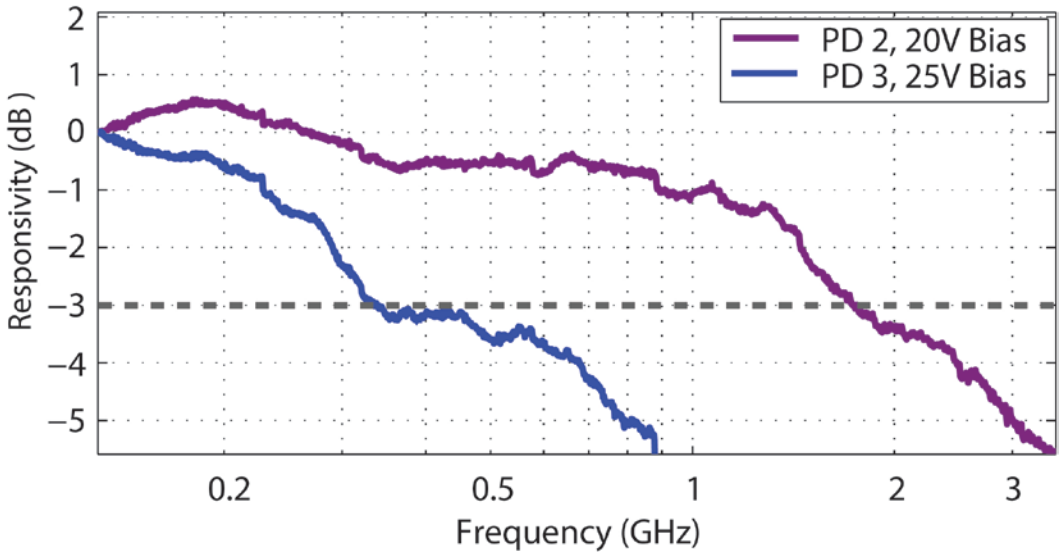


Figure 7.5. Frequency response for PD 2 (250 μm) and PD 3 (3 mm) at λ of 2.2 μm after the 200˚C anneal. The frequency response indicates the devices are limited by capacitance. The slight oscillatory modulation on the response curves was a result of reflections in measurement apparatus and was seen in other detector measurements.

7.4 LOSS CALCULATIONS

To determine total loss prior to the detector, the cutback method was used on waveguides consisting of the same 5 μm x 220 nm coupling fan-out taper sections and un-implanted straight waveguide sections. Multiple measurements were done on multiple devices for each chip, resulting in an average total loss and standard deviation. Loss measurements were initially done in dB and the converted to the appropriate ratio of P_{out}/P_{in} prior to averaging and finding the standard deviation. The conversion to the ratio was done based on the assumption of normally distributed error *versus* a log-normal distribution. The results gave a total loss prior to the PD, including LTF loss, coupling loss, and waveguide loss.

Responsivity was determined by utilizing the average loss to calculate incident power with the error bars calculated based on the standard deviation of the input power as determined from the above measurements.

$$\Re = I_{photo} / (P_{inc} \pm \Delta P_{inc}) \tag{7.2}$$

For the IQE measurements, the propagation of error formulas for both multiplication of two standard variables (f = A·B) and division of two standard variables (f = A/B) assuming negligible covariance were used:

$$\sigma_f \approx |f| \sqrt{\left(\frac{\sigma_A}{A}\right)^2 + \left(\frac{\sigma_B}{B}\right)^2} \tag{7.3}$$

$$\sigma_f \approx |f| \sqrt{\left(\frac{\sigma_A}{A}\right)^2 + \left(\frac{\sigma_B}{B}\right)^2}, \tag{7.4}$$

respectively. Using the above propagation of error equations and the IQE equation,

$$\eta_i = \frac{1.24}{\lambda} \cdot (\Re \pm \Delta\Re) \cdot \left(1 + \frac{\alpha_{par} \pm \Delta\alpha_{par}}{\alpha_{modal} \pm \Delta\alpha_{modal}} \right) / (1 - e^{-(\alpha_{modal} + \alpha_{par}) \cdot L}), \quad (7.5)$$

Both average IQE and standard deviation of IQE were found. A final assumption was made that the standard deviations in the responsivity and absorption coefficients were significantly greater than the standard deviation of the fractional absorbed power. Although this was done to simplify the problem, it is also valid due to the large absorption coefficients, resulting in little change in fractional absorption with the change in absorption coefficients.

7.5 CONCLUSION

CMOS compatible integrated Si^+-implanted Si NWWG photodetectors have been demonstrated and characterized for use in the mid-IR. These devices have measured maximum responsivities of ~ 10 mA/W for a 5 V reverse bias, higher than previously reported for other ion-implanted waveguide detectors at this wavelength [85,86,157], and responsivities as high as 3 mA/W with dark currents in the 10's of picoamps for a zero voltage bias. The detector frequency response was measured to beat 1.7 GHz, with elimination of implantation in the device wings expected to lead to a factor of 5-10 increase in frequency responses. Significant increases in responsivity ≈ 60 - 70 mA/W are expected based on the calculated IQE of 2.7 – 4.5%. Although this responsivity is significantly lower than that reported for heterogeneously integrated detectors based on binary materials, the low dark current, CMOS compatibility, and high speed operation makes these devices desirable for a variety of applications in integrated Si photonic systems.

CHAPTER EIGHT:
Extrinsic photodiodes for integrated mid-infrared silicon photonics[5]

8.1 BACKGROUND

Silicon photonics has recently been proposed for a diverse set of applications at mid-infrared wavelengths [157,165], the implementation of which require on-chip photodetectors. In planar geometries, dopant-based extrinsic photoconductors have long been used for mid-infrared detection with Si and Ge acting as host materials [166]. Leveraging the dopant-induced sub-bandgap trap-states used in bulk photoconductors for waveguide integrated mid-infrared detectors offers simple processing, integration, and operation throughout the mid-infrared by appropriate choice of dopant. In particular, Si doped with Zn forms two trap levels ≈ 0.3 eV and ≈ 0.58 eV above the valence band [167,168], and has been utilized extensively for cryogenically cooled bulk extrinsic photoconductors [166,169]. Here, we demonstrate room temperature operation of Zn^+ implanted Si nano-wire waveguide (Si NWWG) photodiodes (PDs) in the 2.2 μm to 2.4 μm wavelength range.

While a number of Si NWWG-integrated optoelectronic devices have been explored in this wavelength range, efficient photodetection remains an important and challenging task. Thus, spectral translation of mid-infrared signals to the telecom regime via four-wave mixing in Si NWWGs has been proposed for on-chip detection [55], which makes use of integrated PDs in the telecommunications wavelength range. However, this method requires a high-powered pump

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[5] This chapter adapted from:

R. R. Grote, B. Souhan, N. Ophir, J. B. Driscoll, K. Bergman, H. Bahru, W. M. J. Green, and R. M. Osgood, "Extrinsic Photodiodes for Integrated Mid-Infrared Silicon Photonics," arXiv:1406.6420, Optica **1**, 264-267(Aug 14)

laser and long, on-chip-waveguide lengths to achieve efficient wavelength conversion. Alternative solutions for on-chip mid-infrared detection have utilized heterogeneous integration of both narrow-bandgap semiconductors [84,158,170] and graphene [171] with Si NWWGs. Though viable PDs have been demonstrated, heterogeneous integration schemes present an inherent difficulty by imposing constraints on material quality and fabrication process compatibility.

Extrinsic detectors, which utilize absorption transitions from dopant-induced trap-states within the bandgap of a host material, present a simple solution for high-performance on-chip mid-infrared PDs and alleviate the need for heterogeneous integration. These PDs can potentially be integrated into a standard CMOS process flow by adding an ion implantation and annealing step after activation of the source and drain implants, and prior to the deposition of back-end dielectrics and interconnect metalization. Alternatively, this additional fabrication step can be performed as a post-process, as is done here. Indeed, CMOS-compatible Si NWWG PDs that utilize Si lattice defects have been demonstrated [64-66,71], though these detectors are limited in their processing thermal budget and spectral range of detection. However, the Si dopants used in bulk photoconductors cover a range of wavelengths from 1.5 μm to greater than 25 μm [Fig. 8.1 (a)] while doped Ge bulk photoconductors operate out to wavelengths greater than 100 μm [166]. By leveraging the materials commonly found in Si photonics processes, dopant-induced transitions can be exploited for integrated PDs operating throughout the mid-infrared.

For the 2.2 μm to 2.4 μm wavelength range Zn and Au dopants have been shown to produce a suitable trap-state level in Si [167], and planar photoconductive detectors based upon these dopants have been demonstrated [166,169,170]. While photoconductive detectors require liquid nitrogen cooling, it has very recently been shown that Si hyperdoped with Au can generate

photocurrent up to a wavelength of 2.2 µm at room temperature with a Schottky contact configuration [161]. Since cooling is not required to eliminate dark current in diode-based detectors, room temperature operation is achieved with the PDs explored here as well. Although Au and Zn are generally not CMOS compatible, as they can diffuse into Si and adversely affect carrier mobility, the other dopants in Fig. 8.1 (a) do not pose such a restriction. For the wavelength range explored here, Si:Se could be substituted for CMOS compatibility, and has been demonstrated for a Si NWWG PD operating at 1.55 µm [81].

In this chapter, we present room temperature operation of Zn^{+}-implanted Si waveguide photodiodes from 2.2 µm to 2.4 µm, with measured responsivities of up to 87 ± 29 mA/W and low dark currents of < 10 µA. Photocurrent generation is achieved by transitions from dopant-induced sub-bandgap trap-states located ≈ 0.58 eV above the valence band to the conduction band, resulting in a peak detection wavelength of ≈ 2.3 µm. The wavelength of operation can be extended across the mid-infrared by choosing a dopant with an appropriate trap level, opening the possibility for on-chip detection throughout the mid-infrared.

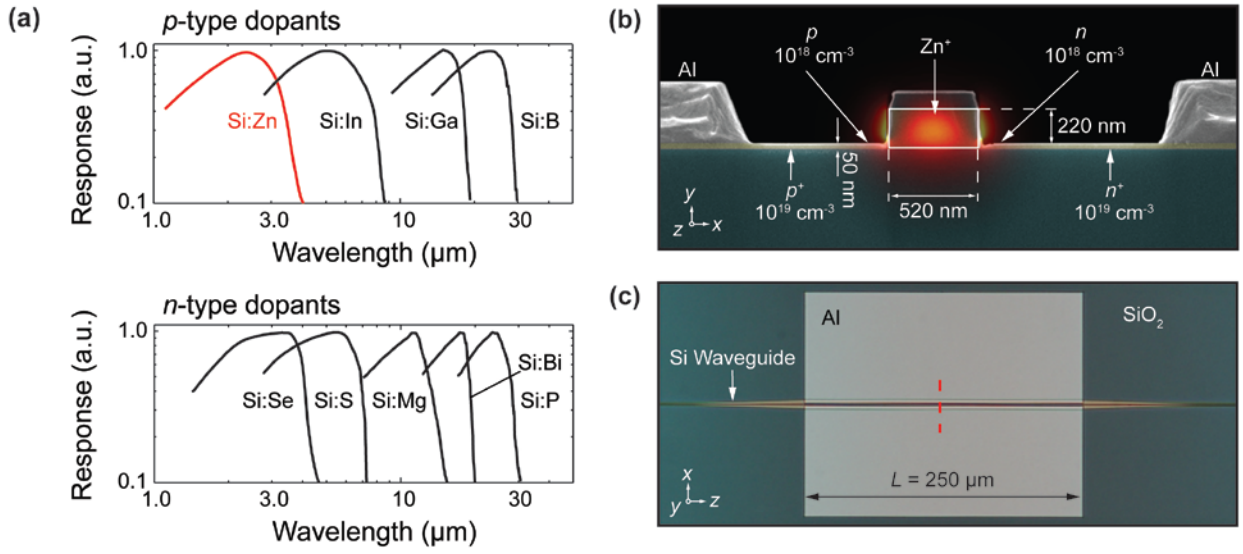

Figure 8.1. (a) Normalized response of bulk silicon photoconductors for different dopants, re-plotted from [3]. Dopants are designated as either *p*-type or *n*-type depending upon whether the resultant trap state is closer to the

valence band or conduction band, respectively. (b) False color SEM cross-section of the *p*-Si:Zn-*n* PD with finite-element-method calculated quasi-TE mode intensity at a wavelength of 2.3 μm superimposed. The waveguide has a 90 nm-thick SiO2 hardmask and 3 μm-thick buried-oxide-layer substrate. (c) Top-view optical microscope image of the PD. The red dashed line indicates the position of the SEM cross-section shown in (b).

8.2 THEORY, FABRICATION AND EXPERIMENTAL SETUP

8.2.1 Theory of Zn Substitutional Defects for Sub-Bandgap Absorption

For the 2.2 μm to 2.4 μm wavelength range Zn and Au dopants have been shown to produce a suitable trap-state level in Si [167], and planar photoconductive detectors based upon these dopants have been demonstrated [166,169]. While photoconductive detectors require liquid nitrogen cooling, it has very recently been shown that Si hyperdoped with Au can generate photocurrent up to a wavelength of 2.2 μm at room temperature with a Schottky contact configuration [162]. Since cooling is not required to eliminate dark current in diode-based detectors, room temperature operation is achieved with the PDs explored here as well. Although Au and Zn are generally not CMOS compatible, as they can diffuse into Si and adversely affect carrier mobility, the other dopants in Fig. 8.1 (a) do not pose such a restriction. For the wavelength range explored here, Si:Se could be substituted for CMOS compatibility, and has been demonstrated for a Si NWWG PD operating at 1.55 μm [81].

Our Si:Zn PDs are based on a *p*-*i*-*n* diode fabricated in a 250 μm-long Si rib/ridge waveguide with 520 nm × 250 nm channel section and a 50 nm doped Si ridge used to form ohmic contacts to Al, as shown in Fig. 8.1(b,c). The intrinsic region of the *p*-*i*-*n* diode corresponds to the channel section of the Si NWWG, and is implanted with Zn^+ to form the *p*-Si:Zn-*n* PD. Two Zn^+ implantation doses are investigated, 10^{12} cm^{-2} and 10^{13} cm^{-2}, corresponding to estimated average Zn concentrations inside the channel section of the waveguide of $N_{Zn} = 4.5 \times 10^{16}$ cm^{-3} and $N_{Zn} = 4.5 \times 10^{17}$ cm^{-3}, respectively. The Zn concentrations are estimated by averaging the stopping range of Zn^+ inside of the Si device layer, which is calculated by SRIM software [112]. Based on

these calculations, an acceleration voltage of 260 keV is chosen for maximum overlap between the generated trap states and the quasi-TE waveguide mode. Subsequent to implantation, the PDs are annealed in atmosphere for a series of increasing temperatures, reaching a maximum of 350˚C, and the responsivity was found to increase with each anneal.

The detection mechanism of our p-Si:Zn-n PDs is believed to be due to substitutional Zn atoms in the Si lattice, which act as a double-acceptors and result in the two defect levels [Fig. 8.2(a)] with energy levels of $E_{d1} \approx E_v + 0.3$ eV and $E_{d2} \approx E_v + 0.58$ eV [167,168]. While the position of the Fermi level in the Si:Zn region is not known, the excess carrier concentration is below that of the *p* and *n* regions, ensuring that the Si:Zn region will be fully depleted with the application of a reverse bias voltage. Photon-induced transitions occurs between E_{d2} and the conduction band, which corresponds to a transition energy of $E_g - E_{d2} = 1.12$ eV – 0.58 eV = 0.54 eV with a peak absorption wavelength of ≈ 2.3 μm. Photocurrent generation due to this transition is shown to be a single-photon process by the linearity measurements in Fig. 8.2(b). The presence of E_{d1} does not contribute to photocurrent generation in the wavelength range of interest; however, its presence should impact the thermally assisted re-population rate of E_{d2} and thus the internal quantum efficiency, η_i, of the PD.

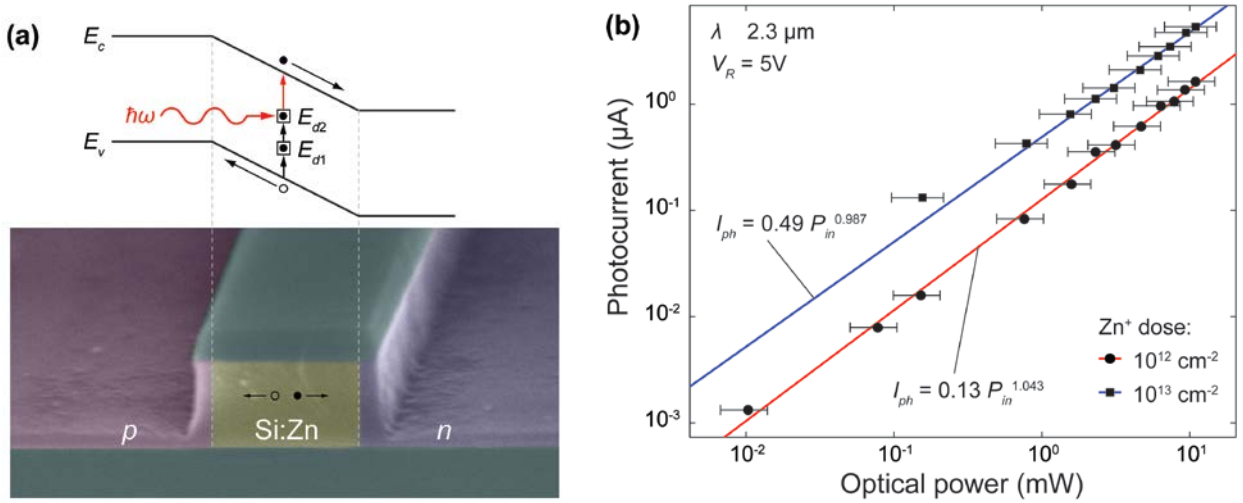

Figure 8.2. (a) Band diagram of the p-Si:Zn-n, photodiode with de-ect levels $E_{d1} \approx E_v + 0.3$ eV and $E_{d2} \approx E_v + 0.58$ eV in the Si:Zn region [4, 5]. The doping profile is illustrated by the false-color SEM shown below. (b) Photocurrent I_{ph} versus input optical power P_{in} along with linear fits. The linear correspondence indicates a single-photon excitation process. The higher implantation dose is shown for a 3 mm length PD.

8.2.2 Fabrication

Our Si:Zn PDs are based on a *p*-*i*-*n* diodes fabricated on the CMOS line at MIT Lincoln Laboratory as described in [66] and Chapter 2, using SOI with a 3 μm BOX in a 250 μm-long Si rib/ridge waveguide with 520 nm × 250 nm channel section and a 50 nm doped Si ridge used to form ohmic contacts to Al, as shown in Fig. 8.1(b,c). Subsequently, contact photolithography was used to define a Shipley S1811 implantation mask at Brookhaven National Laboratory, and Zn^+ ion implantation was performed in the Ion Beam Laboratory, State University of New York at Albany. The intrinsic region of the *p*-*i*-*n* diode corresponds to the channel section of the Si NWWG, and is implanted with Zn^+ to form the *p*-Si:Zn-*n* PD.

Two Zn^+ implantation doses are investigated, 10^{12} cm^{-2} and 10^{13} cm^{-2}, corresponding to estimated average Zn concentrations inside the channel section of the waveguide of $N_{Zn} = 4.5 \times 10^{16}$ cm^{-3} and $N_{Zn} = 4.5 \times 10^{17}$ cm^{-3}, respectively. The Zn concentrations are estimated by averaging the stopping range of Zn^+ inside of the Si device layer, which is calculated by SRIM software [112]. An acceleration voltage of 260 keV was used, corresponding to a stopping range of 118 nm into the waveguide as calculated by SRIM software [112], resulting in the maximum overlap between the induced defect concentration and the fundamental quasi-TE mode of the waveguide. The ion beam was launched 7˚ from normal incidence to the sample surface, and implantation current densities of 1 nA/cm^2 and 3-7 nA/cm^2 were used for the 10^{12} cm^{-2} and 10^{13} cm^{-2} implantation doses, respectively.

The SRIM calculated dose profile is shown in Fig. 8.3. The averaged Zn concentration in the waveguide is estimated by integrating the Gaussian fit over the 220 nm length of the silicon device layer, and multiplying by the dose. The ion stopping range is adjusted by changing the acceleration voltage. For the PDs explored here, an acceleration voltage of 260 keV was used to place the stopping range in the center of the Si device layer such that the fundamental quasi-TE mode of the Si NWWG (Fig. 8.1 (b)) had maximum overlap with the resultant trap-states.

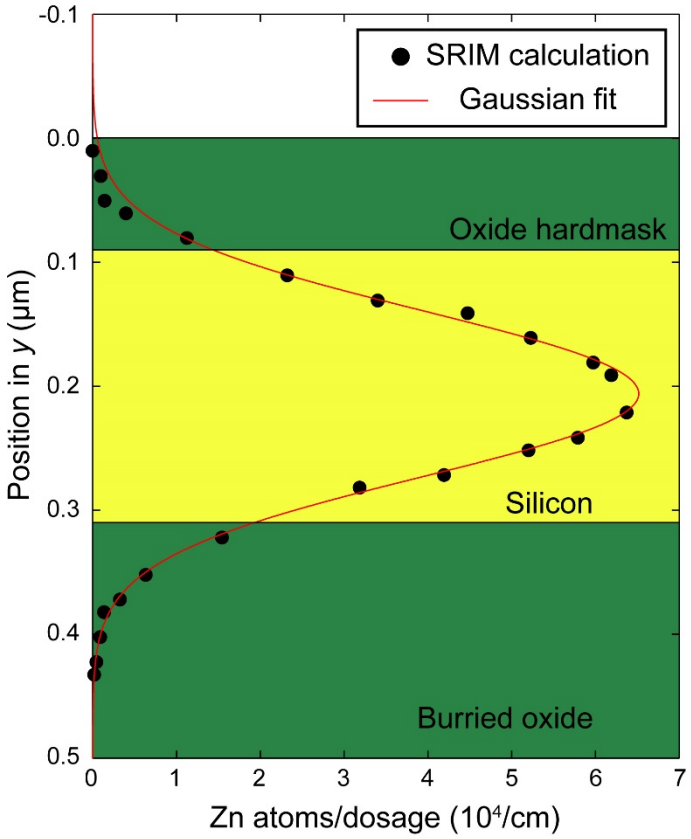

Figure 8.3. SRIM calculated Zn^+ implantation profile for an acceleration voltage of 260 keV.

Post implantation, the devices were annealed in atmosphere at 250˚C for 10 minutes. Subsequently, a series of anneals were performed with increasing temperatures in 50˚C steps for 10 minutes per step. Photocurrent and transmission measurements were taken between each step, and the device performance was found to improve with each annealing cycle.

The amorphization threshold is taken to be the dose for which the concentration of implantation-induced lattice defects accounts for 10% of the total available Si lattice sites. This corresponds to a defect concentration of 5×10^{21} cm^{-3} for Si. Based on the SRIM calculations the threshold dose for amorphization is 2×10^{13} cm^{-2}; however, these calculations do not take thermal effects into account. Thus, the SRIM estimation is an underestimate of the amorphization threshold dose. Even so, this conservative estimate shows that the doses explored here are below the amorphization threshold.

8.2.3 Experimental Setup

Our measurement setup is shown in Fig. 8.4. An external cavity Cr^{2+}:ZnSe tunable laser (IPG Photonics) passes through an isolator (ISO) and is free-space coupled to a single-mode fiber (SMF) using a fiber collimator (FC). The SMF is also connected to a polarization rotator (PR) followed by a single-mode lensed tapered fiber (LTF) designed for a 2.5 μm spot-size and working distance of 14μm at l = 1.55μm (Oz optics). The LTF couples into a 5 μm × 220 nm nm fan-out tapered silicon waveguide, which adiabatically decreases in width over a length of 450 μm to a 520 nm 220 nm channel waveguide. The PR is used to ensure that only the quasi-TE (QTE) mode of the waveguide is being excited, which produces maximum photocurrent as the overlap with the Zn^{+} implanted region is larger than that of the quasi-TM mode. The channel waveguide adiabatically tapers into a rib/ridge waveguide with a 50 nm ridge and the same channel dimensions over a length of 100 μm, which then enters the Zn+ implanted-silicon-waveguide photodiode. Reverse-bias voltage is applied and current is measured using a Keithley 2400 Source/Meter through electrical probes, which are landed on Al contact pads. Power transmitted through the photodiode is out-coupled in an identical manner to the input coupling, and passes through an SMF patch cable to a Yokogawa AQ6375 optical spectrum analyzer.

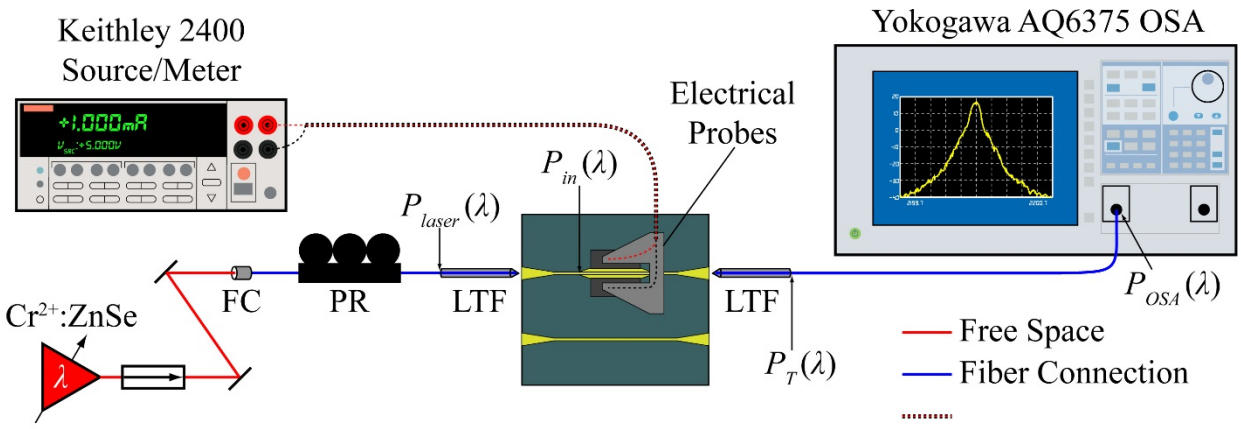

Figure 8.4. Experimental setup. ISO = isolator, FC = fiber collimator, PR = polarization rotator, LTF = lensed tapered fiber.

8.3 RESULTS

8.3.1 Responsivity

The responsivity, defined as $R = I_{ph}/P_{in}$, where I_{ph} is the photocurrent and P_{in} is the on-chip optical power entering the PD, is measured as a function of reverse bias voltage with 2.2 μm wavelength excitation [Fig. 8.5 (a,b)]. While the dark current (Fig. 8.5(a,b), inset) increases with dopant concentration, it remains below 10 μA for all devices even at the maximum reverse bias voltage of 20 V under which measurements were taken. The responsivity is largest at shorter wavelengths [Fig. 8.5(c,d)], reaching a maximum of 8.3 ± 2.6 mA/W and 34.1 ± 10.6 mA/W for doses of 10^{12} cm^{-2} and 10^{13} cm^{-2}, respectively, at a wavelength of 2.2 μm and a reverse bias of 20 V. For 3 mm length PDs, maximum responsivities of 87 ± 29 mA/W are measured under similar conditions, and the dark current remained below 10 μA at 20 V reverse bias (see Fig. 8.5(a,b). The decrease in responsivity with increasing wavelength is due to parasitic absorption from the contacts (free-carrier absorption in *p*, *n* doped regions as well as the Al regions), which increases from > 30% at 2.2 μm to > 89% at 2.4 μm for a dose of 10^{12} cm^{-2}, and from > 10% at 2.2 μm to > 85% at 2.4 μm for a dose of 10^{13} cm^{-2}. The parasitic absorption has been

determined by transmission measurements through an un-implanted diode with the same geometry, *p*, *n* doping, and contact metalization.

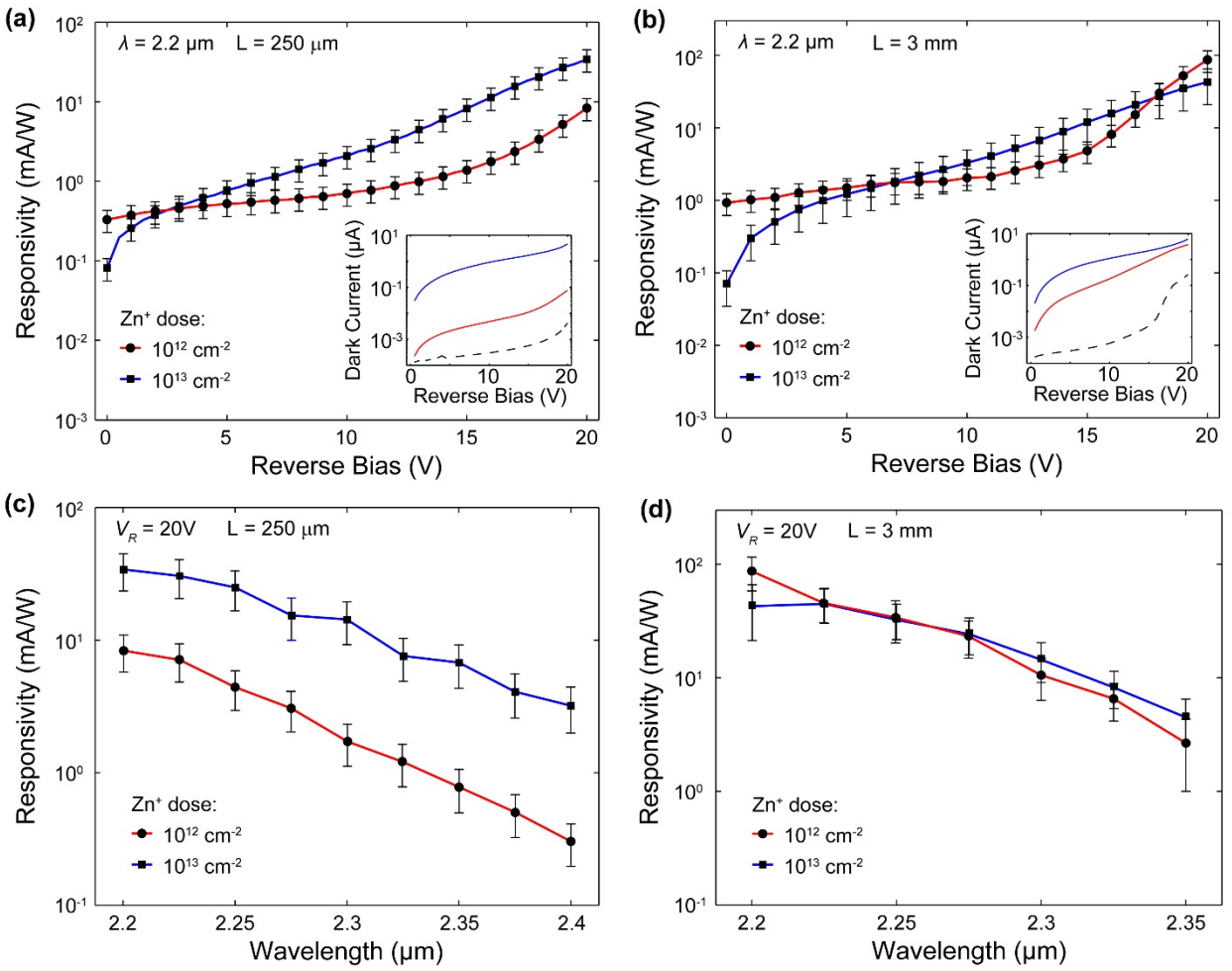

Figure 8.5. Responsivity as a function of reverse bias voltage for (a) 250 μm device and (b) for 3 mm device. Insets: dark current as a function of reverse bias voltage for un-implanted diode (black dashed line) and PDs with Zn^+ doses of 10^{12} cm^{-2} (red solid line) and 10^{13} cm^{-2} (blue solid line). Responsivity as a function of wavelength for (c) 250 μm device and (d) 3 mm device. The decrease in responsivity with increasing wavelength is due to parasitic absorption.

8.3.2 Absorption Coefficient

Transmission measurements were performed for Zn^+ implanted PDs, and were repeated for an un-implanted diode (having identical *p* and *n* implants and contact metallization as the Zn^+ implanted PD) of the same length. Using these measurements, the effects of parasitic absorption

in the Al contacts is taken into account by calculating the modal absorption coefficient, $\bar{\alpha}_{eff} = -\bar{T}/L$ [dB/cm], where T is the power transmission in dB and L = 250 μm. By subtracting the parasitic absorption $\alpha_{eff,par}$, measured from an un-implanted diode, from the absorption coefficient due to defects shown in Fig. 8.6 is determined: $\bar{\alpha}_{eff,Zn} = \bar{\alpha}_{eff,tot} - \bar{\alpha}_{eff,par}$. The contact absorption becomes dominant for λ > 2.325 μm, resulting in the loss of responsivity with increasing wavelength seen in Fig. 8.5(c,d).

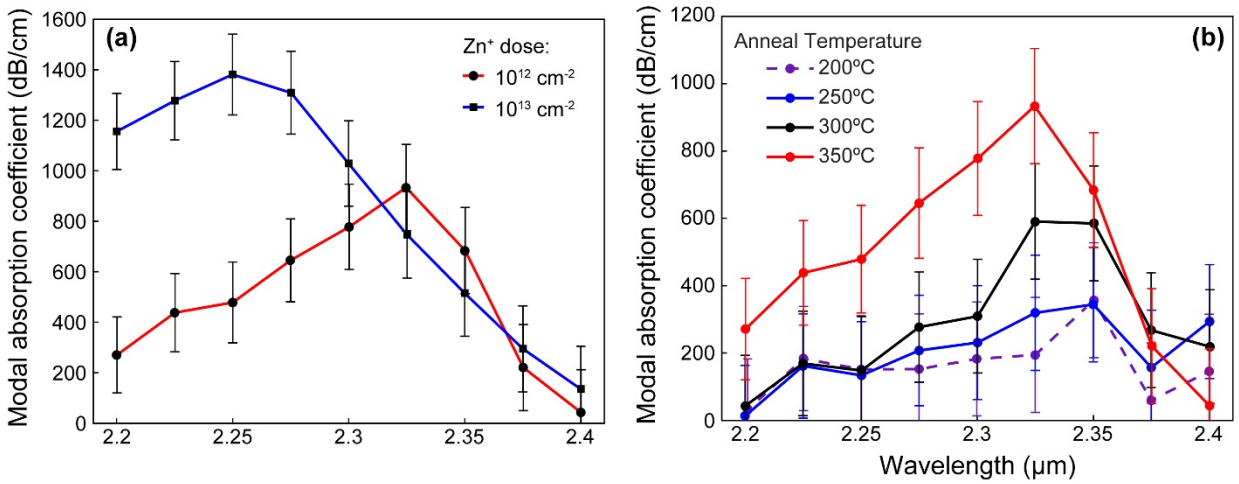

Figure 8.6. (a) Modal absorption coefficients due to Zn^+ implantation after 350˚C anneal. (b) Modal absorption coefficient vs annealing temperature for Zn^+ dosage = 10^{12} cm^{-2}. Each subsequent annealing step was performed for 10 minutes.

The modal absorption coefficient for the 10^{12} cm^{-2} Zn^+ dose PD at each annealing step is shown in Fig. 8.6(b). The absorption peak associated with the E_{d2} to conduction band transition located between 2.325 μm and 2.350 μm can be seen to emerge with increasing anneal temperature. The annealing temperature was limited to 350˚C, since the 100 nm thick Al contacts were found to reflow above this temperature.

The transmission measurements used to find the modal absorption coefficients can also be used to determine the fraction of power absorbed in the PD that is due to Zn^+ implantation.

Using the parasitic absorption coefficient, $\alpha_{eff,par}$, and the absorption coefficient of a *p*-Si:Zn-*n* PD, $\alpha_{eff,tot}$, the fraction of power absorbed by Zn^+ implantation can be found by noting that:

$$P_{abs,Zn} = \alpha_{eff,Zn} P_{in} \int_0^L \exp\left(\alpha_{eff,tot} z\right) \mathrm{dz} = \frac{\alpha_{eff,Zn}}{\alpha_{eff,tot}} P_{abs,tot}. \tag{8.1}$$

The fraction of absorption due to Zn^+ implantation is shown in Fig. 8.7 (with error bars determined as described in 8.5), and is calculated as:

$$\frac{P_{abs,Zn}}{P_{abs,tot}} = \frac{\alpha_{eff,Zn}}{\alpha_{eff,tot}} = 1 - \frac{\alpha_{eff,par}}{\alpha_{eff,tot}}. \tag{8.2}$$

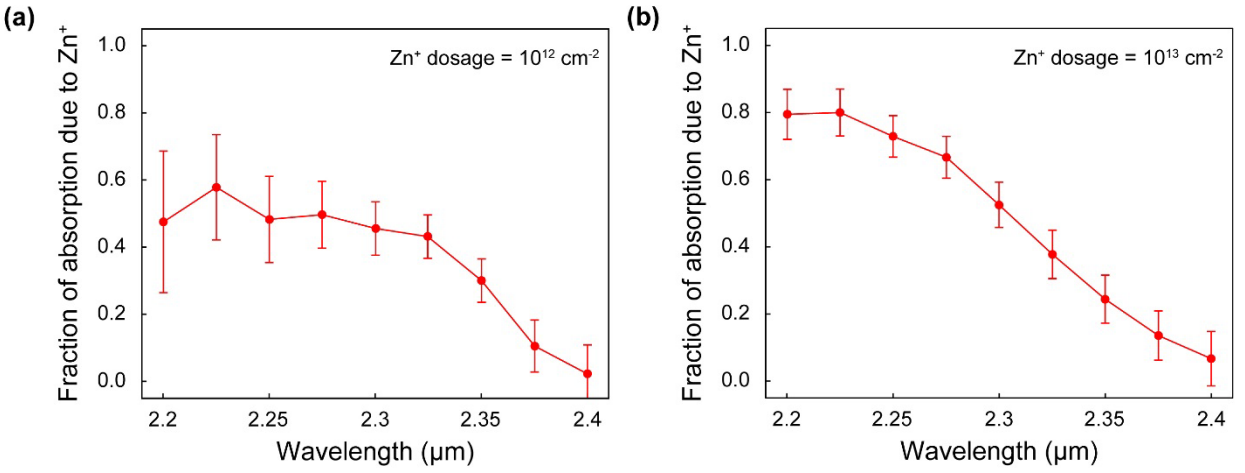

Figure 8.7. Fraction of total power absorption due Zn^+ implantation, $\alpha_{eff,Zn}/\alpha_{eff,tot}$, for a Zn^+ dose = 10^{12} cm^{-2} and (b) Zn^+ dose = 10^{13} cm^{-2}.

Even with parasitic absorption taken into account, these measurements indicate that η_i is below 5%, which is significantly lower than the reported values of η_i = 20% at a wavelength of 2.4 μm for Si:Zn bulk photoconductive detectors fabricated by diffusion doping [169]. Though diffusion doping of Zn in Si results in electrical activation by forming substitutional defects on Si lattice sites [169], activation of the Zn^+-implanted Si used here is not well characterized. For Zn^+ implantation doses above the amorphization threshold, Zn out-diffusion and Si recrystallization occur concurrently between 300˚C and 500˚C annealing [172,173], and a significant fraction of

Zn atoms remain on interstitial lattice sites throughout the process [173]. Although the Zn^+ doses used are below the amorphization threshold dose of 3×10^{14} cm^{-2} [174], Si lattice defects caused by implantation are expected to remain for annealing temperatures below 550˚C [173]. The post-implantation annealing temperature used here was limited to 350˚C to avoid reflow of the Al contacts, suggesting that there are two factors limiting η_i of the *p*-Si:Zn-*n* PDs: (1) lattice defects that remain in the Si lattice after annealing, and (2) the fraction of implanted Zn atoms that have not been activated. The responsivity was found to increase with increasing annealing temperatures, suggesting that activation can be improved further with higher-temperature annealing.

8.5 LOSS CALCULATIONS

Error bars are determined by uncertainties in losses from the measurement setup, which include lensed-tapered fiber (LTF) losses and single-mode fiber transmission/bending losses. Additionally, uncertainty in the waveguide facet loss from fan-out tapers couplers have also been taken into account and as well as temporal fluctuations in the laser output as tracked by the transmitted power.

The total fiber-to-fiber transmission loss is measured by aligning two lensed-tapered fibers at their focal distance with the sample removed, and is defined in dB as $P_{F2F} = P_{laser} - P_{OSA}$, where P_{laser} and P_{OSA} are shown in Fig. 8.8. This loss is averaged over four measurements to determine the mean and standard deviation, $\overline{P_{F2F}}$ and σ_{F2F}, respectively. The transmission loss through the connecting fiber in dB is found as $P_{CF} = P_T - P_{OSA}$, and is also averaged over four measurements to find the mean and standard deviation $\overline{P_{CF}}$, σ_{CF}. The loss due to

transmission through a single LTF is calculated as $\bar{P}_{LTF} = \frac{1}{2}(\bar{P}_{F2F} - \bar{P}_{CF})$ and the standard deviation is found by propagation of error $\sigma_{LTF} = \frac{1}{2}\sqrt{\sigma_{F2F}^2 + \sigma_{CF}^2}$.

Facet loss was determined by coupling both LTFs to the on-chip 5μm × 220nm fan-out tapers, and averaging over 14 transmission measurements through straight waveguides to find $\bar{P}_{FL} = \frac{1}{2}(\mathbb{E}\{P_{laser} - P_{OSA}\} - \bar{P}_{F2F})$, resulting in the mean, $\overline{\bar{P}_{FL}}$, and standard deviation $\sigma_{LTF} = \frac{1}{2}\sqrt{\text{var}\{P_{laser} - P_{OSA}\} + \sigma_{F2F}^2}$ shown in Fig. 8.8.

To determine error bars for the responsivity, the on chip power entering the PD is determined in milliwatts $\bar{P}_{in}[\text{mW}] = 10^{(\bar{P}_{laser} - \bar{P}_{FL} - \bar{P}_{LTF})/10}$, and the propagation of error is approximated by a Taylor series expansion $\sigma_{in}[\text{mW}] = \bar{P}_{in}\frac{\ln 10}{10}\sqrt{\sigma_{laser}^2 + \sigma_{FL}^2 + \sigma_{LTF}^2}$. The mean responsivity is calculated as $\bar{R} = \frac{I_{ph}}{\bar{P}_{in}}$ resulting in a standard deviation of $\sigma_R \approx \bar{R}\frac{\sigma_{in}}{\bar{P}_{in}}$.

The error bars for the modal absorption coefficient in Fig. 8.6 of the are determined by measuring the optical power transmission through the PD $\bar{T} = \mathbb{E}\{P_{in} - P_{OSA}\} - 2\bar{P}_{FL} - \bar{P}_{F2F}$ through a PD of length L = 250 μm, with the modal absorption coefficient being defined as $\bar{\alpha} = -\bar{T}/L$. The standard deviation is determined by propagation of uncertainty to be $\sigma_\alpha = \frac{1}{L}\sqrt{\text{var}\{P_{laser} - P_{OSA}\} + 4\sigma_{FL}^2 + \sigma_{F2F}^2}$. This calculation is repeated with measurements from an un-implanted diode, and the modal absorption coefficient due to Zn^+ implantation is defined as $\bar{\alpha}_{eff,Zn} = \bar{\alpha}_{eff,tot} - \bar{\alpha}_{eff,par}$ with standard deviation $\sigma_{\alpha,Zn} = \sqrt{\sigma_{\alpha,tot}^2 + \sigma_{\alpha,par}^2}$.

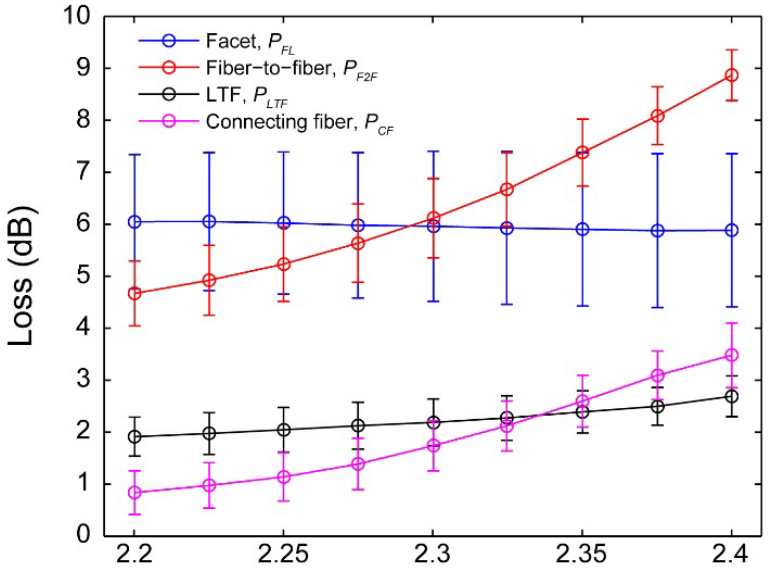

Figure 8.8. Measured system losses with error bars.

8.6 CONCLUSION

Though certain Si lattice defects and surface states can generate photocurrent from sub-bandgap photons, this is not believed to be the dominant mechanism in our devices. The Si divacancy defect has been shown to be optically active in the wavelength range explored here [66]; however, these particular lattice defects anneal out at temperatures above 300˚C [65]. While optically active Si interstitial clusters have been shown to form at higher annealing temperatures in Si^{+}-implanted Si [64], cluster formation is aided by the presence of excess implanted Si atoms [175]. The concentration of Si interstitials is expected to be significantly lower in Si:Zn. Additionally, measurements of Si+-implanted Si NWWG PDs in Chapter 7 with identical geometry and similar dosages to the PDs explored here exhibit significantly different characteristics in the 2.2 μm to 2.4 μm wavelength range, and do not display a peak in their absorption coefficient at the transition energy associated with Si:Zn. Indeed, no optically active Si lattice defects have been identified with the ≈ 0.54 eV absorption transition observed in Fig. 8.2 [176]. Thus, the absorption coefficients measured and the post-implantation annealing

temperature used indicate that contributions to photocurrent generation by Si lattice defects are not substantial. Interstitial Zn and Si atoms are believed to remain in the waveguide, though they are most likely contributing to optical scattering and increased carrier recombination rather than photocurrent generation.

Our results illustrate the potential for silicon photonic extrinsic photodiodes operating at mid-infrared wavelengths. The use of dopants for trap-state engineering in diode configurations allows for design of on chip PDs with the device parameters such as dark current, internal quantum efficiency, and peak detection wavelength being controlled through adjustments to the trap-state levels and populations. Beyond photodetection, trap-state transitions can emit photons under the proper conditions [177], creating the prospect for on-chip waveguide-integrated sources and detectors operating throughout the mid-infrared wavelength band.

CHAPTER NINE:
Conclusion and Future Work

9.1 Conclusion

Over forty years ago, lightwave communications went from solely being transmitted through air, an unreliable medium, and generally interpreted with human eyes (the photophone withstanding), an unreliable instrument, to being the backbone of high-speed long-distance world-wide data communications. With fiber cables reaching losses of ≈ 0.2 dB/km and bit rates reaching 40 Gb/s, accurate and reliable information is being transmitted and received at rates unimaginable even one hundred years ago.

We are now at the cusp of a new revolution in lightwave communications, going from worldwide data connectivity, to connectivity at the chip level, where individual computing cores no longer use copper wire interconnects to transmit data but rely on high speed optical links consisting of silicon waveguides. Although the waveguides themselves have matured significantly, with losses less than 3 dB/cm in silicon, the actual optical to electrical interconnects are still in question. Many competing technologies exist, each with its own advantages and disadvantages. Heterogeneous and Ge based detectors both offer excellent performance, but fail to fit perfectly in with the current CMOS fabrication process that has been the standard for electronics devices for years.

In this this work, ion implanted Si NWWG PDs were fabricated, characterized, and tested at telecom wavelengths through mid-infrared wavelengths. Section I of this dissertation has discussed in detaip the fabrication of the devices used, along with detailing the ion-implantation process and theory of trap-assisted sub-bandgap photodetection.

Section II of this dissertation has focused on devices designed for telecom frequencies. In Chapter 4, metal-semiconductor-metal Si NWWG were fabricated and characterized. With responsivity as high as 0.51 A/W and a calculated internal quantum efficiency of 42%, these devices compared well with both heterogeneous and Ge detectors (with responsivities typically around 1 A/W). The frequency response of the device was measured at 2.6 GHz and found to be limited primarily by fabrication. Both the 5 μm spacing of the contacts and implantation of the wings contributed to the comparatively the low frequency value of the response. Simulations showed an expected frequency response of ≈ 10 GHz with closer contact spacing. Further, better control on the implantation region, containing it to within the waveguide, and not reducing the mobility of the wings, will increase frequency response significantly more.

In Chapter 5, Si^+ implanted NWWG photodetectors were studied for use as high speed optical interconnects. Error-free data reception was demonstrated at data rates of 2.5 Gb/s and 10 Gb/s at a bias voltage of 15V for a 3 mm long PD and a 250 μm long PD, respectively. The data rate was found to be primarily RC limited, however characterization of similar devices showed frequency responses as high as 35 GHz, suggesting data rates approaching 40 Gb/s should be achievable. The sensitivity of the 250 μm device was found to be approximately 5.3 dBm after accounting for coupling loss. By properly conditioning the PDs, a 15 dB improvement in sensitivity is expected. With error free data rates of 10 Gb/s, low dark current, and sensitivities predicted to reach ≈ -9 to -10 dBm, these devices are comparable in performance with Ge detectors.

In section III of this dissertation, several devices were characterized for longer wavelength operation, including error-free data transmission at 1.9 μm, corresponding well to the

amplification range of thulium doped fiber amplifiers, and characterization of PDs operating in the mid-infrared range of 2.2 – 2.4 μm.

In Chapter 6, Si^+ ion-implanted NWWG PDs were characterized for operation at 1.9 μm and demonstrated with error-free data reception at 1 Gb/s. With photodetection out to 1.9 μm, these devices open up the possibility of new communication channels for on-chip data routing, which extend further into the IR region, beyond that of typical Ge and GaAs PDs. The detectors showed a reduction in responsivity of approximately 70% with respect to operation at 1.55 μm, with 25% of this reduction due to an increase in parasitic loss from a decrease in modal confinement. Optimizing the waveguide and wing region for operation at λ = 1.9 μm and using shorter devices is expected to result in data transmission rates beyond 10 Gb/s with an approximate 3 dB penalty in sensitivity when compared to operation at 1.55 μm.

Chapters 7 and 8 demonstrated detection for ion-implanted waveguides out to 2.4 μm, well into the mid-infrared region, with uses ranging from chemical sensing to free-space communications. Chapter 7 explored Si^+ implanted waveguides for detection in the mid-IR ranging from 2.2 μm to 2.35 μm. With a 5 V reverse bias, these devices had responsivities as high at $\approx$ 10 mA/W, higher than that for previously reported devices, including the Zn^+-implanted devices discussed in Chapter 8, and only nanoamps of dark current. Reducing the reverse bias to 0 V resulted in only a 3 dB loss in photocurrent and a dark current in the 10's of picoamps. With a measured absorption coefficient ranging from approximately 30 – 60 dB/cm, the IQEs of the PDs were calculated to be around 2.7 – 4.5%. With IQEs in this range, responsivities of greater than 60 - 70 mA/W are expected. Frequency response was also measured, and found to be RC limited at 1.7 GHz,, suggesting high speed error-free data reception of upwards 2.5 Gb/s is achievable.

Chapter 8 further explored mid-infrared photodetection in Si NWWG by examining Zn^+ as an alternate implant species. Although the Si^+ implanted devices measured in Chapter 7 continued to show significant detection in the mid-infrared after annealing at 350˚C, the divacancy is known to anneal out at these temperatures, limiting the thermal budget. The optically active state for Zn implantation is based on a substitutional impurity instead of a defect, making it thermally stable to temperatures greater than 600˚C. These devices exhibited responsivities as high as 87 ± 29 mA/W and currents of < 10 μA.

9.2 Future Work

The PDs tested at the longer wavelengths used structures that were optimized for telecom wavelengths, resulting in significant parasitic loss as high as over several hundred dB/cm for λ in the 2.2 to 2.4 μm range. The MSM devices fabricated in Chapter 4 can easily be tailored for operation at these longer wavelengths, requiring no doping in the wings for operation, reducing parasitic loss. In addition, due to the fabrication tolerances, implantation in the 'wing' region of the PDs likely reduced frequency response as the divacancy defect is known to both reduce mobility and to act as compensation doping. Devices fabricated specifically for the mid-infrared region and with better implantation controls will increase both responsivity and frequency response.

In addition to improving fabrication procedures, additional study is needed to find alternate implant species. As Zn is generally avoided in CMOS fabrication due to its ability to diffuse in Si, effecting carrier mobility and impacting doping, Se is a possible alternate, creating sub bandgap states at levels similar to Zn without the worry of diffusion through the Si. Another implant that requires additional study is Ar. The Si^+ implanted devices studied here are based on the divacancy defect which is known to anneal out around 300˚C. Alternatively, Ar^+

implantation has been shown to create sub-bandgap trap states stable to temperatures beyond up to at least 400˚C. With the sub-bandgap trap states at levels similar to those associated with the divacancy, and thermal stability up to 400˚C, these devices can improve the thermal budget for the ion-implanted PDs operating in the telecom to mid-infrared range. Finally, as stated in Chapter 8, a host of other implant species can be used to tailor the PD for the desired wavelength range, opening up several other research areas.

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