RF Frontend for Spectrum Analysis in Cognitive Radio

Karthik Tripurari Jayaraman

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ABSTRACT

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Advances in wireless technology have sparked a plethora of mobile communication standards to support a variety of applications. FCC predicts a looming crisis due to the exponentially growing demand for spectrum and it recommends to increase the efficiency of spectrum utilization. Cognitive Radio (CR) is envisioned as a radio technology which detects and exploits empty spectrum to improve the quality of communication.

Spectrum analyzer for detecting spectrum holes is a key component required for implementing cognitive radio. Mitola's vision of using an RF Analog-to-Digital (ADC) to digitize the entire spectrum is not yet a reality. The traditional spectrum analysis technique based on a RF Front end using an LO Sweep is too slow, making it unsuitable to track fast hopping signals.

In this work, we demonstrate an RF Frontend that can simplify the ADC's requirement by splitting the input spectrum into multiple channels. It avoids the problem of PLL settling by incorporating LO synthesis within the signal path using a concept called Iterative Down Converter.

An example 0.75GHz-11.25GHz RF Channelizer is designed in 65nm Standard CMOS Process. The channelizer splits the input spectrum (10.5GHz bandwidth) into seven channels (each of bandwidth 1.5GHz). The channelizer shows the ability to rapidly switch from one channel to another (within a few ns) as well as down-converting multiple channels simultaneously (concurrency). The channelizer achieves a dynamic range of 54dB for a bandwidth of 10.5GHz, while consuming 540mW of power.

Harmonic rejection mixer plays a key role in a broadband receiver. A novel order-scalable harmonic rejection mixer architecture is described in this research. A proof-of-principle prototype has been designed and fabricated in a 45nm SOI technology. Experimental results demonstrate an operation range of 0.5GHz to 1.5GHz for the LO frequency while offering harmonic rejection better than 55dB for the 3rd harmonic and 58dB for the 5th harmonic across LO frequencies.

While cognitive radio solves the spectrum efficiency problem in frequency domain, the electronic beam steering provides a spatial domain solution. Electronic beam forming using phased arrays have been claimed to improve spectrum efficiency by serving more number of users for a given bandwidth. A LO path phase-shifter with frequency-doubling is demonstrated for WiMAX applications.

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To my family,

Chapter 1

Introduction

Demand for wireless communications services is exploding, placing tremendous strain on the capacity of wireless communications networks. Fig. 1.1 shows the allocation of the frequency spectrum in the United States of America (USA). With a plethora of new wireless standards coming up, there is a scarcity of available spectrum. Communication industry stake-holders are aggressively searching for sustainable solutions to this ever-worsening problem.

While almost all RF spectrum is allocated, most of it is either unused or underutilized. [1] has documented the usage of frequency spectrum from 30MHz to 3GHz. Some of the conclusions of their research are:

- There are a number of bands that have low measured spectrum occupancy. 420-450 MHz (Amateur/Radio-location), 745-810 MHz (Public Safety), 960-1020 MHz (Aviation) 1240-1300 MHz (Amateur) 1400-1430 MHz (Space/Satellite), 1430-1520

Figure 1.1: Allocation of the Frequency Spectrum in United States of America.

MHz (Telemetry), 1525-1710 MHz (Mobile Satellite/Meteorological), etc are a few of them.

- The TV bands exhibit far more activity than those listed above.
- The 900 MHz (Cellular) and 1900 MHz (PCS) bands show a great deal of down-link activity. Up-link activity, though, is very low.

FCC acknowledges the "looming crisis" over the capacity of broadband networks. At CES 2010, the Chairman of FCC, Julius Genachowski, emphasized on the necessity for quick and effective solutions.

Electronic beam steering is envisioned to improve spectrum efficiency by exploiting space dimension [2]. The spatial filtering at the transceiver can substantially improve the

signal-to-noise-plus-interference ratio (SNIR). With the use of electronic beam-steering, the same frequency band can be re-used in a different spatial sector without causing any interference or decline in the quality of communication service. Substantial research has been conducted in phased-array based multiple antenna transceivers to realize beam steering. [3; 4; 5].

While beam steering enables us to solve the spectrum efficiency problem in spatial domain, Cognitive Radio (CR) can solve the problem using frequency domain. CR is envisioned as a radio technology which autonomously detects and exploits empty spectrum to improve the quality of communication. These technologies include, the ability of devices to determine their location, sense spectrum use by neighboring devices, change frequency, adjust output power, and even alter transmission parameters and characteristics. The potential of CR technology has given rise to developments with the promise of inexpensive adaptable radio architectures [6].

Active research is being conducted on software defined radio (SDR) [7; 8; 9]. These transceivers are capable of changing their operating characteristics (frequency band, bandwidth, modulation scheme, etc) dynamically. A key missing block at this point is a spectrum analyzer that records the spectrum usage in the neighborhood, thereby enabling the SDR to adapt to the environment. This work focusses on RF front-end architecture and circuits for spectrum analysis with a focus towards quick scanning of broad bandwidth.

1.1 A Brief description of possible approaches in spectrum analysis

This section presents the challenges in circuit implementation of a spectrum analyzer. In order to emphasize the challenge, the following heuristic assumptions are made: let the signal (to be analyzed) bandwidth be 10GHz, resolution bandwidth 10MHz, Noise Figure (NF) of the RF spectrum scanner be 9dB, and the peak interferer power be -35dBm.

$$\text{Total analysis bandwidth} = 10GHz \tag{1.1}$$

$$\begin{aligned} \text{kT in 1Hz} &= -174dBm \\ \text{1MHz RBW} &= +60dB \\ \text{Noise Figure} &= +19dB \\ \text{Noise floor} &= -95dBm \\ \text{Peak interferer power} &= -35dBm \end{aligned}$$

$$\text{Dynamic range} = 60dB \tag{1.2}$$

1.1.1 Mitola's vision for cognitive radio

Mitola [10] envisioned the use of a RF analog-to-digital converter (ADC) as the RF front-end. All radio functions are realized in a programmable digital signal processor (DSP). While this is possibly the most flexible RF front-end that one can come up with, an ADC

to meet the requirements presented in (1.2) is still far from achievable. Fig. 1.2 shows the

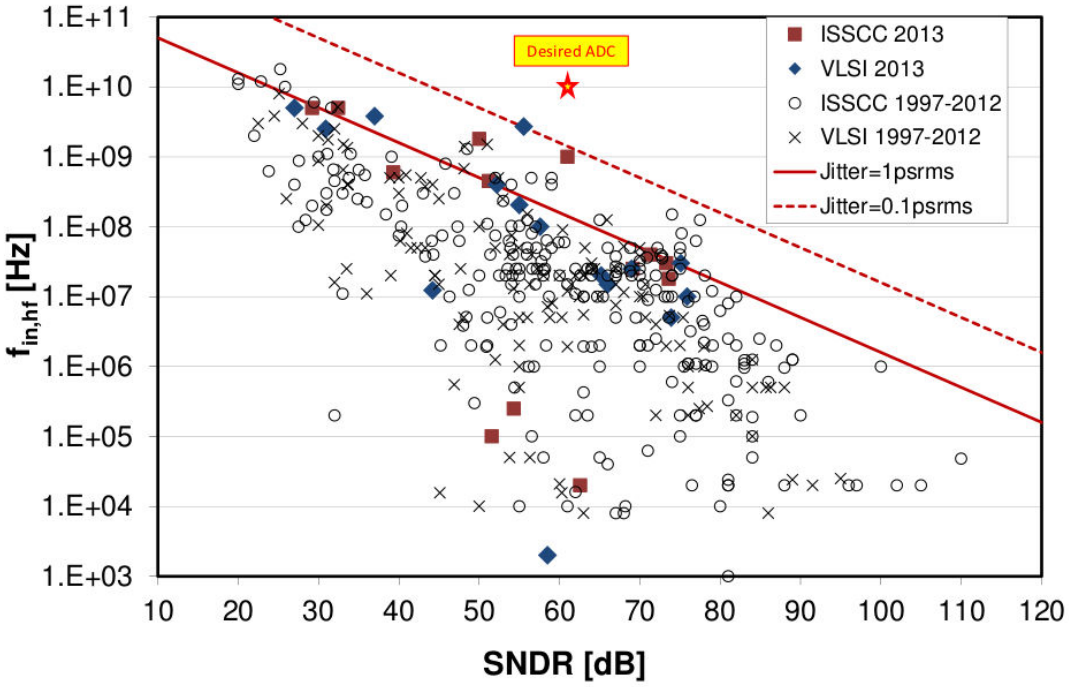


Figure 1.2: Available state-of-art ADCs and the specification of a typical ADC used for spectrum analysis.

state-of-art ADCs published in ISSCC and VLSI since 1997. It can be seen that the desired ADC's specification is still beyond the reported state-of-art ADCs. Further, a very stringent requirement on the jitter of the clock source ($<<$100fs) is necessary.

Despite the above stated disadvantages, direct digitization of the input signal is advantageous for its quick spectrum analysis ability. A FFT of the output of the ADC gives us the information about the spectrum. The time taken to analyze the spectrum is inversely proportion to its resolution bandwidth. For a resolution bandwidth of 10MHz, it is possible to analyze the spectrum in 100ns.

1.1.2 Spectrum analysis using traditional RF receivers and sweeping LO

Fig. 1.3 shows the block diagram of a RF receiver that can be used for spectrum analysis. The input signal is down-converted with an LO (of frequency f_{LO}) and filtered using a low-pass filter. The low-pass filter attenuates all the out-of-band blockers, thus simplifying the requirements of the ADC (both in speed and dynamic range). The dynamic range of

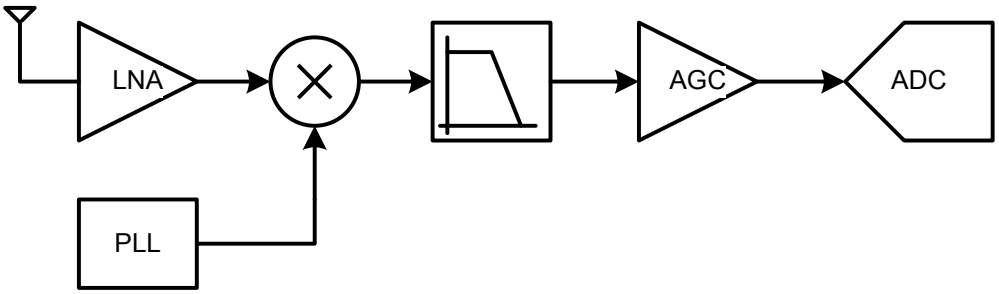


Figure 1.3: Block diagram of a RF receiver with a narrow output bandwidth used for spectrum analysis.

such system is then limited by that of the LNA-Mixer. Recent advances in software defined radio have demonstrated ways to increase the dynamic range by using techniques like [11; 9; 7; 8; 12].

The spectrum analyzer scans the spectrum sequentially, down-converting one channel at a time, by sweeping the frequency of LO. Every change in f_{LO} is associated with a PLL settling time. The total analysis time is given by

$$T_{\mathrm{total}} = N \cdot T_{\mathrm{analysis}} + (N-1) \cdot \left(T_{\mathrm{PLL,settling}} + T_{\mathrm{LPF,settling}}\right) \tag{1.3}$$

For a total analysis bandwidth of 10GHz, analyzed one 10MHz channel at a time, the

number of channels to be analyzed are $N = 1000$. If the PLL bandwidth is 1MHz, the settling time is of the order of $1\mu s$. For accurate frequency output, PLL will take a longer duration to settle. For this calculation, a PLL settling time $T_{\text{PLL,settling}} = 1\mu s$ is assumed. Similarly, the low-pass filter settling time is $T_{\text{LPF,settling}} = 100n$. For a resolution bandwidth of 10MHz, the T_{analysis} is 100ns. The total analysis time is then $\approx 1.2ms$.

Such a spectrum analyzer would not be able to track frequency hopping signals whose rate of hopping exceeds 835Hz.

1.2 A RF channelizer approach in spectrum analysis

Two fundamental approaches of spectrum scanning were described in section 1.1. While direct digitization has an advantage of enabling rapid spectrum analysis, the ADC requirements are beyond today's state-of-art ADC's specifications. The RF receiver base down-conversion requires a simplified ADC at the cost of total spectrum measurement time. In this work, a RF channelizer approach in spectrum scanning is proposed.

Fig. 1.4 shows the block diagram of a spectrum scanner using a RF channelizer. The RF channelizer divides the input signal, of bandwidth "B", into N channels, each of bandwidth "$\frac{1}{N} \cdot B$". The output of the RF channelizer is digitized by the ADC.

When the input spectrum is split into N parallel channels (in frequency domain), the ADC will have to accommodate a smaller number of interferers. For further analysis, an uniform distribution of interferers across the spectrum and equal power of the interferers are assumed. For a N times narrower bandwidth, there would be N times smaller number

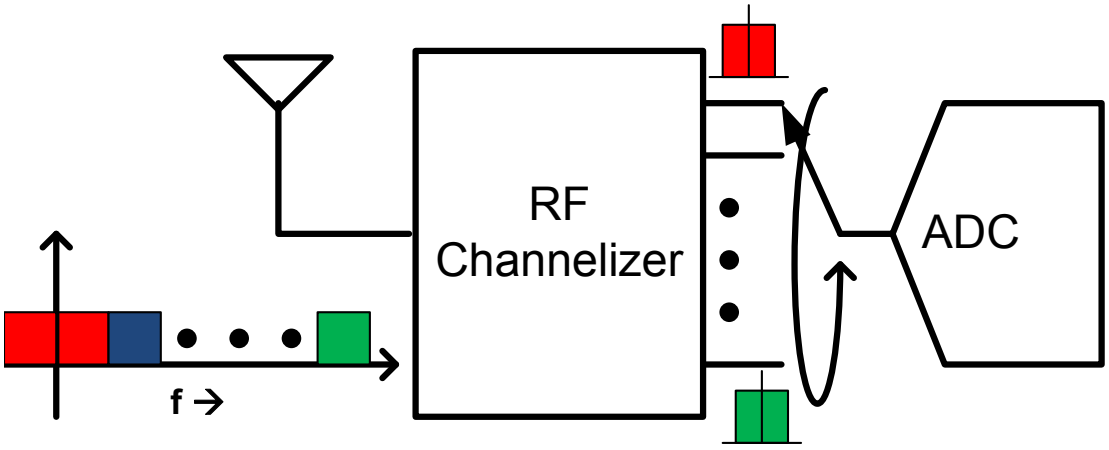


Figure 1.4: Block diagram of a spectrum analyzer using RF channelizer approach to frequency channelize the input to simplify the ADC requirements.

of interferers. In other words, if there are $k \cdot N$ interferers in bandwidth B at the input, the number of interferers would be k in each channel at the output of the RF channelizer. Let the interferer signal at the input be

$$x_{\text{int}}(t) = Acos(\omega_1 t) + ... + Acos(\omega_{kN} t). \tag{1.4}$$

After RF channelization, the interferer signal in channel "M" is

$$\hat{x}_{\text{int}} = Acos\left(\omega_{(M-1)\cdot N+1} t\right) + ... + Acos\left(\omega_{(M-1)\cdot N+k} t\right). \tag{1.5}$$

The amplitude of the interferer decreases from kN to k. Thus the dynamic range requirement of the ADC decreases by 20log(N).

Further, the sampling speed of the ADC is reduced by a factor of N. For the spectrum scanner requirements presented in section 1.1, the RF channelizer approach simplifies the ADC requirements to achievable levels. Fig. 1.5 plots the dynamic range (DR) and sampling speed requirements of the ADC vs. the number of channels (N).

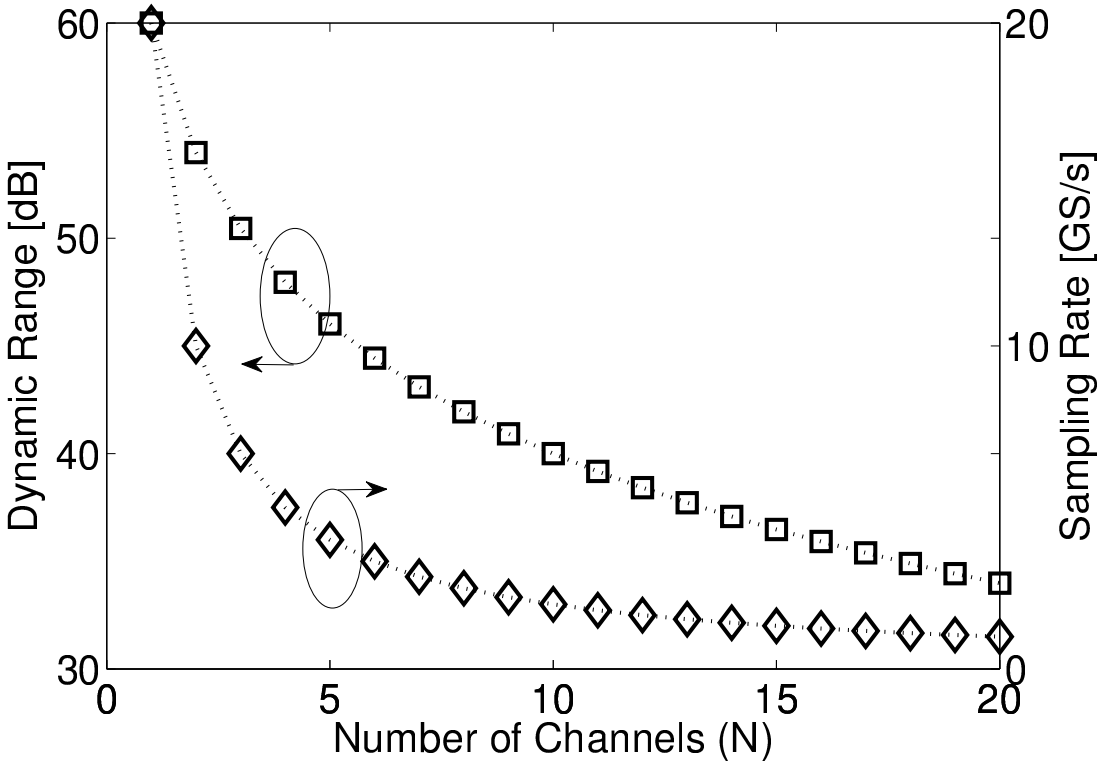


Figure 1.5: Requirements of the ADC vs. number of channels generated by the RF channelizer.

Fig. 1.6 plots the spectrum scanning duration vs the number of channels of the RF channelizer. It can be noted that the spectrum scanning duration increases with an increase in number of channels.

1.3 Summary of the contributions of this research

- Fig. 1.6 shows that the PLL settling time is an important bottleneck to reducing the spectrum scanning duration. [13] introduced an idea known as Iterative Down-Conversion (IDC). The IDC, operating with a fixed frequency PLL, incorporates the role of frequency synthesis within the signal path using a cascade of image-reject

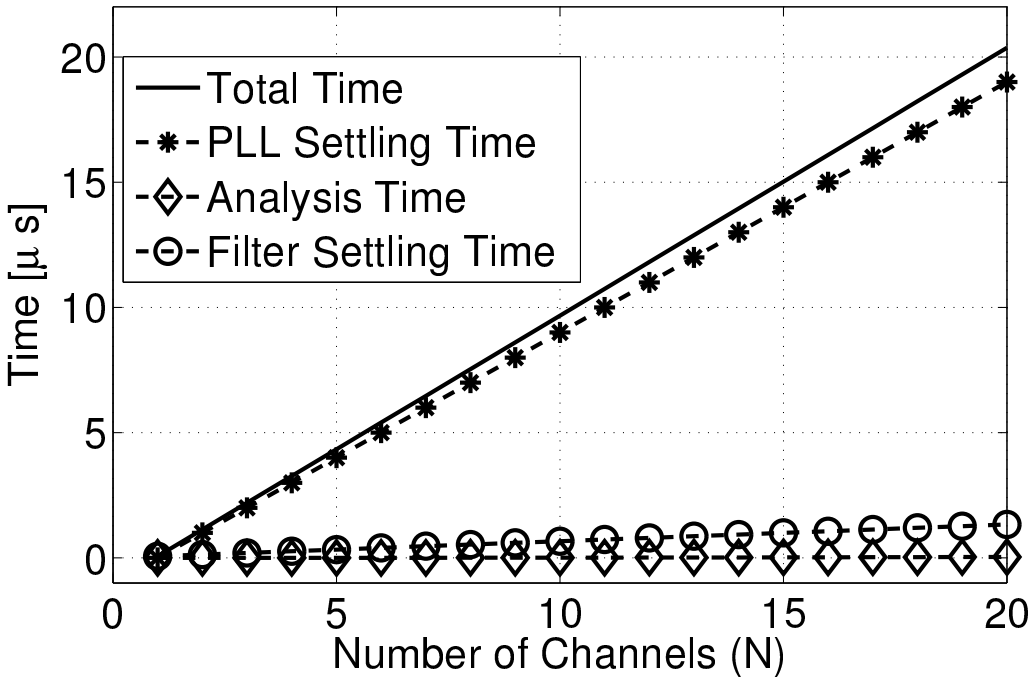


Figure 1.6: Spectrum analysis duration of an RF-channelizer based spectrum analyzer.

mixers. We present a study of adaptation of an IDC to implement the RF channelizer. The fundamental limitation to the dynamic range, signal leakage to adjacent channels, is analyzed.

- In order to overcome the limitations of an IDC, a novel 3-way-splitting IDC is developed. The 3-way-splitting IDC architecture enables the use of filtering to compliment harmonic rejection of the mixer in order to improve the signal leakage.

- A 0.75GHz-11.25GHz RF channelizer implementation in 65nm CMOS technology. The RF channelizer splits the input signal into seven channels each of bandwidth 1.5GHz. In order to demonstrate both concurrency (multiple outputs being available simultaneously) and fast-switching between channels, a partially concurrent 3-output

fast-switching RF channelizer is demonstrated.

- A circuit block called multi-mode mixer is developed. The multi-mode mixer can operate either as a mixer or a transparent block, passing the input directly to the output. As will be shown later, the multi-mode mixer enables the reduction of hardware and thus in considerable reduction in the area of the chip. Further, the mixer enables the reduction of load for the driving circuitry of the preceding stage. This is capable of considerable power savings, particularly when used in high bandwidth situations.

- The rejection of higher harmonics of a mixer is crucial in many applications. For instance, it limits the signal leakage performance in an IDC, relaxes the filter requirements in the 0.75GHz-11.25GHz RF channelizer, etc. As the bandwidth of the cognitive radio increases, there is a need for harmonic rejection mixers which can operate at LOs of multiple GHz and reject higher harmonics of LO. A novel order-scalable, high-LO-frequency harmonic rejection mixer architecture is developed.

- Feature size of a transistor is scaled in successive technologies to improve the speed of the transistors. Power supply scaling is necessary along with feature size scaling in order to maintain reliable operation of a CMOS transistor. Technology scaling has benefited digital circuits in terms of speed as well as power consumption. The increase in fT has also helped analog circuits in terms of bandwidth and noise figure. To exploit these advantages of technology scaling, SoCs are implemented in modern technologies.

At high speeds or high dynamic range operation of an ADC, the jitter of its clock source becomes a performance limiting factor. We present a study on the effect of power supply scaling on a PLL's jitter.

- Electronic beam steering has been shown to be an effective way to solve the problem of spectrum scarcity. Phased array is an important component of this technology and phase shifter is an essential circuit block. An analysis of various techniques of phase shifting is presented and a frequency-doubling phase shifter architecture for multi-antenna transceiver systems is demonstrated.

1.4 Organization of the Thesis

This thesis is further organized as follows.

Chapter 2 introduces the principle of Iterative down-conversion. The technique of incorporating frequency synthesis within the signal path is described. Fundamental dynamic-range limiting phenomena of the IDC architecture in terms of signal leakage are explained.

Chapter 3 elaborates on the evolution of the novel 3-way IDC architecture to overcome the limitations of an IDC. The 3-way-splitting IDC architecture is used to implement a 0.75GHz-11.25GHz RF Channelizer. A detailed design methodology for the 0.75GHz-11.25GHz RF channelizer is then presented. A comparison of this architecture with other RF Channelizers is presented based on the simulation results.

Chapter 4 presents a harmonic rejection mixer architecture capable of operating for a

wide range of LO frequencies. The mixer can be configured to suppress any particular harmonic of the LO or multiple harmonics simultaneously. The level of suppression of each harmonic is controlled by a set of independent gain and phase tuning parameters. Feasibility of extension of this concept to higher order harmonics is also demonstrated. A proof-of-principle prototype has been designed and fabricated in a 45nm SOI technology.

Chapter 5 presents an analysis of the effect of power supply scaling on a PLL's jitter. Feature size of the transistors in CMOS technology is scaled down to enhance the f_T of the transistors. The supply voltage is also scaled down simultaneously to ensure reliable operation of the transistors. Digital circuits benefit from this scaling. The scaling of dynamic range-power trade-off of mixed signal circuits is limited by parameters such as Jitter of the clock source. We propose a theory to describe the scaling of a PLLs Jitter as a function of the power supply. This chapter presents theory for scaling of various sources of noise in a PLL. Based on the scaling of noise of individual blocks, a theory is proposed for the jitter of the PLL.

Chapter 6 presents a digitally controlled frequency-doubling phase-shifter architecture for the implementation of multiple-antenna GHz transceiver systems. It takes a 1.75GHz input and produces two phase-shifted outputs at 3.5GHz. It consists of a Delay Locked Loop (DLL) followed by symmetric XOR frequency doublers and phase interpolators. The phase shifter prototype in 90nm standard CMOS has a phase shift range of 360 with a resolution of 22.5.

Chapter 2

Iterative Down-Conversion for Broadband Signal Frequency Channelization

2.1 Abstract

In this chapter, the concept of Iterative down-conversion (IDC) using a cascade of image-reject mixers is discussed. The ability of IDC to simultaneously down-convert multiple channels at the same time (concurrency), while using a fixed frequency phase-locked loop are presented.

The effect of mixer non-idealities such as finite image rejection and harmonic rejection on signal leakage from one channel to another is discussed. Further, an estimate of

harmonic and image rejection levels for various gain and phase mismatches is presented.

2.2 Introduction

Simultaneous reception of multiple channels from a wide spectrum is of interest in applications such as cognitive radio, UWB radio, etc. Recently, frequency interleaved ADC is envisioned as an alternative to time-interleaved ADC. This requires an RF front-end circuit that can concurrently down-convert multiple channels. An Iterative Down-Converter (IDC) was proposed in [13] to achieve this purpose.

An initial version of IDC was reported for a UWB interference detector [14]. The IDC channelizes and scans the input signal in a time-sequential manner. An unfolded version of this architecture that introduces concurrency is proposed in [13]. This architecture merges LO synthesis within the signal path through the use of cascaded image-reject mixers, and divides the incident spectrum into contiguous channels without spectral gaps.

In this chapter, we focus on the fundamental dynamic range limiting factors of the IDC architecture. Every stage of down-conversion in the IDC employs mixers with non-idealities such as finite image rejection and harmonic rejection. The effect of the non-idealities on the leakage from one channel to another is discussed.

The rest of the chapter is organized as follows: section 2.3 describes the principle of operation of cascaded image-reject mixers. Section 2.4 analyzes the effects of finite harmonic rejection on the performance of an IDC. Harmonic rejection for various gain and phase mismatches are presented. Section 2.5 analyzes the effect of finite image rejection

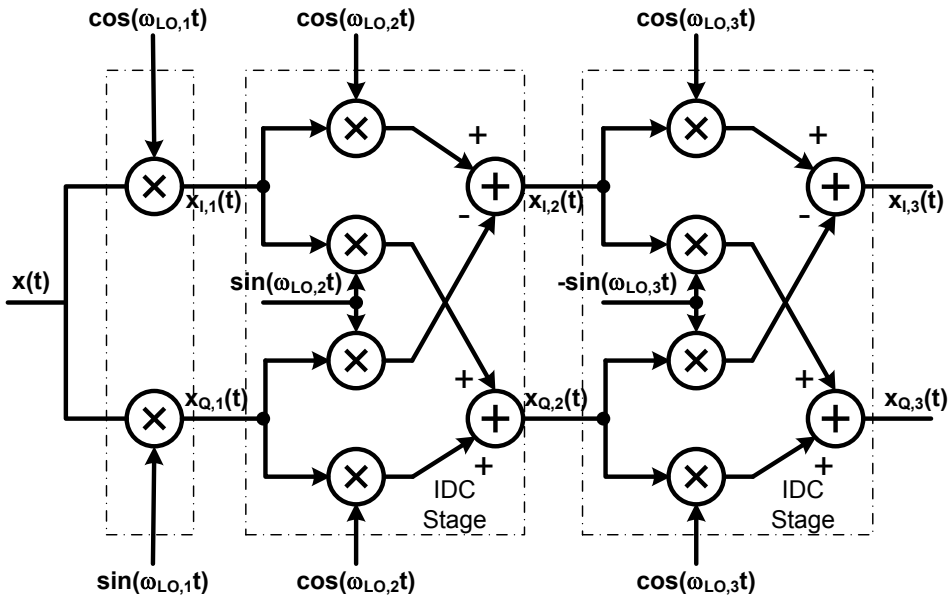


Figure 2.1: An example implementation of an Iterative Down-Conversion using cascaded image-reject mixers.

on the performance of an IDC. Section 2.6 presents the simulation results of a typically achievable RF timing offset in 45nm SOI technology and 65nm CMOS technology. Finally, the conclusions are presented in section 2.7.

2.3 Operation of cascaded image-reject mixers

Fig. 2.1 shows an example implementation of an IDC using cascaded image reject mixers. In the first stage of frequency translation, the input $x(t)$ is multiplied by quadrature LOs of angular frequency $\omega_{\mathrm{LO},1}$. The outputs of the first stage are

$$\begin{aligned} x_{\mathrm{I},1}(t) &= x(t)\cdot\cos\left(\omega_{\mathrm{LO},1}t\right) \\ x_{\mathrm{Q},1}(t) &= x(t)\cdot\sin\left(\omega_{\mathrm{LO},1}t\right) \end{aligned} \tag{2.1}$$

Frequency translation of signal in stage-II can be described using (2.2).

$$\begin{aligned} x_{\mathrm{I},2}(t) &= x_{\mathrm{I},1}(t)\cdot\cos(\omega_{\mathrm{LO},2}t) - x_{\mathrm{Q},1}(t)\cdot\sin(\omega_{\mathrm{LO},2}t) \\ &= x(t)\cdot\cos[(\omega_{\mathrm{LO},1}+\omega_{\mathrm{LO},2})t] \\ x_{\mathrm{Q},2}(t) &= x_{\mathrm{Q},1}(t)\cdot\cos(\omega_{\mathrm{LO},2}t) + x_{\mathrm{Q},1}(t)\cdot\sin(\omega_{\mathrm{LO},2}t) \\ &= x(t)\cdot\sin[(\omega_{\mathrm{LO},1}+\omega_{\mathrm{LO},2})t] \end{aligned} \tag{2.2}$$

An LO of $\omega_{\mathrm{LO},1}+\omega_{\mathrm{LO},2}$ is artificially synthesized within the signal path using cascade of image-reject mixers operating with LOs of $\omega_{\mathrm{LO},1}$ and $\omega_{\mathrm{LO},2}$. Similarly, an LO of $\omega_{\mathrm{LO},1}-\omega_{\mathrm{LO},2}$ can be synthesized by flipping the polarities of one of the LOs. This is demonstrated in the third frequency translation stage of the IDC in Fig. 2.1. The outputs of the IDC can be calculated as

$$\begin{aligned} x_{\mathrm{I},3}(t) &= x(t)\cdot\cos[(\omega_{\mathrm{LO},1}+\omega_{\mathrm{LO},2}-\omega_{\mathrm{LO},3})t] \\ x_{\mathrm{Q},3}(t) &= x(t)\cdot\sin[(\omega_{\mathrm{LO},1}+\omega_{\mathrm{LO},2}-\omega_{\mathrm{LO},3})t] \end{aligned} \tag{2.3}$$

An output of N^{th} IDC stage, $x_{N+1}(t)$ (=$x_{I,N+1}(t)+j\cdot x_{Q,N+1}(t)$), can be conveniently represented using complex exponentials as

$$\begin{aligned} x_N(t) &= x_{N-1}(t)\times \mathrm{e}^{\left(j\cdot d_N\omega_{\mathrm{LO,N}}t\right)} \\ x_N(t) &= x(t)\times \mathrm{e}^{\left(\sum_{k=1}^{N} j\cdot d_k\omega_{\mathrm{LO,k}}t\right)} \end{aligned} \tag{2.4}$$

where d_N is $+1$ if the mixing operation is an up-conversion and -1 if it is a down-conversion.

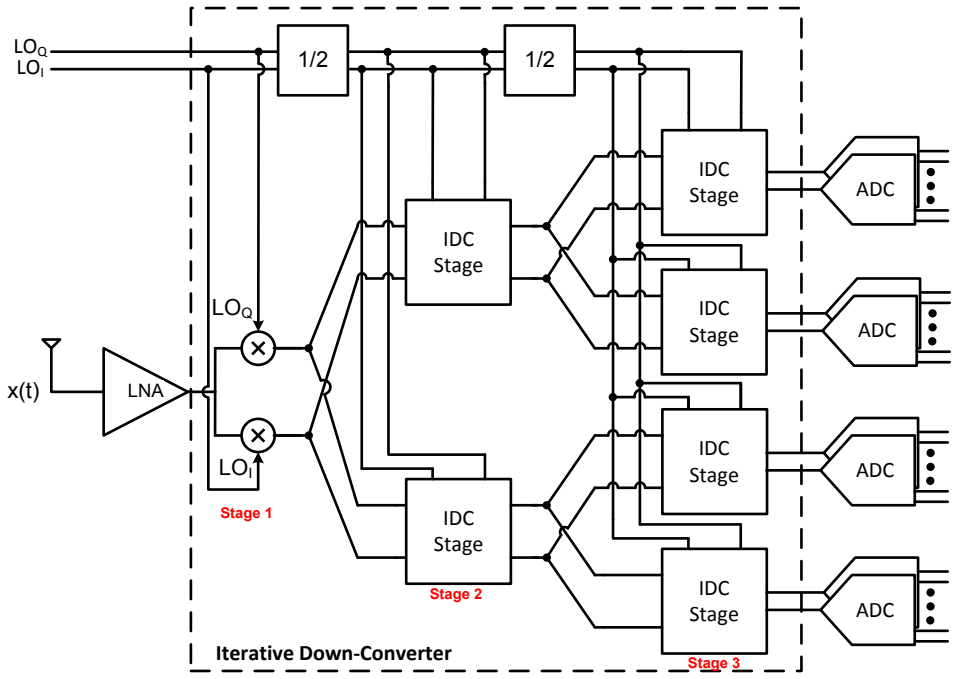


Figure 2.2: Block diagram of an implementation of a 3-stage IDC with 4 output channels.

A fully concurrent version of iterative down-converter using cascade of image reject mixers is shown in Fig. 2.2. LO frequency in any stage of frequency translation is chosen to be half of the frequency used in the previous stage. Thus the IDC requires only one fixed frequency PLL, with the rest of the LOs derived using divide-by-2 circuits. The frequency translation in an IDC can be represented as

$$y(t) = x(t)\mathrm{e}^{j\cdot\omega_{\mathrm{LO}}t\cdot\left(1\pm\frac{1}{2}\pm\ldots\pm\frac{1}{2^{N-1}}\right)} \tag{2.5}$$

For an input signal with a bandwidth B, the frequency of the LO for the fist mixer, ω_{LO}, is $2\pi\left(\frac{B}{2}\right)$. After undergoing N stages of frequency translation, the signal is divided into 2^{N-1} parallel complex channels each with a bandwidth of $\frac{B}{2^{N-1}}$.

2.4 Effect of finite harmonic rejection of a mixer

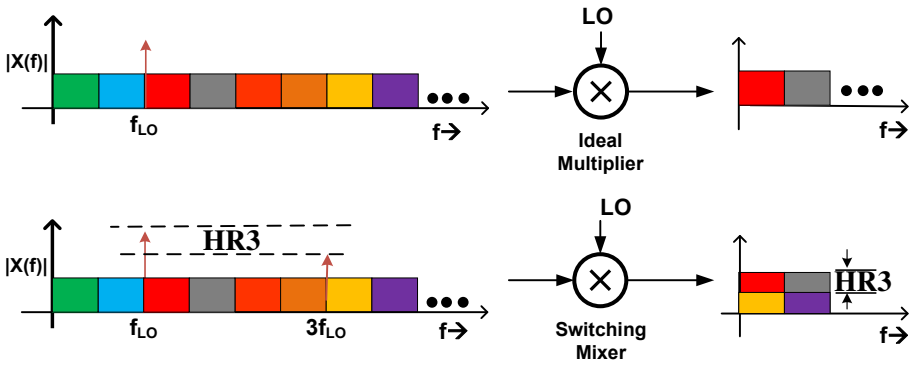


Figure 2.3: Frequency translation in a stage of an IDC using ideal multipliers. and real mixers.

The analysis of an IDC presented in section 2.3 assumes ideal multipliers to explain the principle of operation. In a practical implementation of an IDC, the multipliers would be replaced with switching mixers [15; 16]. The switching mixers multiplies the RF signal with a square-wave whose frequency corresponds to that of the LO. The spectrum of a 50% duty-cycle square-wave contains tones not only at its fundamental frequency (ω_{LO}), but also at the odd harmonics of the LO ($3\omega_{LO}$, $5\omega_{LO}$, $7\omega_{LO}$ ...).

The effect of finite third harmonic rejection is illustrated in Fig. 2.3[1]. Signals around the harmonics of the LO are spuriously down-converted into the desired channel. An undesired blocker can potentially be down-converted into the channel of interest due to a finite harmonic rejection and degrade the SNR of the desired channel. The dynamic range of an IDC is then limited by the harmonic rejection in the mixers.

[1]The effect of higher harmonics is similar. Signals around the corresponding harmonics of the LO get spuriously down-converted into the desired channel.

2.4.1 Pre-filtering to relax harmonic rejection requirements

One way to overcome the limitation is to attenuate the blockers around the harmonics of LO. This can be done by using a low-pass filter before the mixer. Fig. 2.4 shows the typical filter roll-off and suppression of signals around the third and the fifth harmonics of the LO for a Chebyshev filter with an in-band ripple of 3dB. The effect of low-pass filter on the signal leakage due to finite harmonic rejection is shown in Fig. 2.5. For the example shown, considering a finite roll-off offered by a low-pass filter, it does not alleviate the third harmonic rejection limitations. However, for higher harmonics, the attenuation provided by the filter compliments the harmonic rejection of the mixer. Thus the harmonic rejection ratios requirements for the mixers are relaxed.

2.4.2 Achievable harmonic rejection in mixers

A block diagram of a harmonic rejection mixer (HRM) proposed in [17] is shown in Fig. 2.6(a). The HRM comprises of three unit mixers whose conversion gains are in the ratio $1 : \sqrt{2} : 1$ and LO phases are offset by 45°. Upon addition of the three outputs, the signals around the third and fifth harmonic of LO add destructively while signals around the fundamental of the LO add constructively.

However, in the presence of gain and phase mismatches, the cancellation is not perfect. A block diagram of a HRM with mismatches is shown in Fig. 2.6(b). The third harmonic rejection (HR_3) is defined as the ratio of conversion gains of signal around the fundamental of the LO and the conversion gain of the signals around the third harmonic of the LO. For

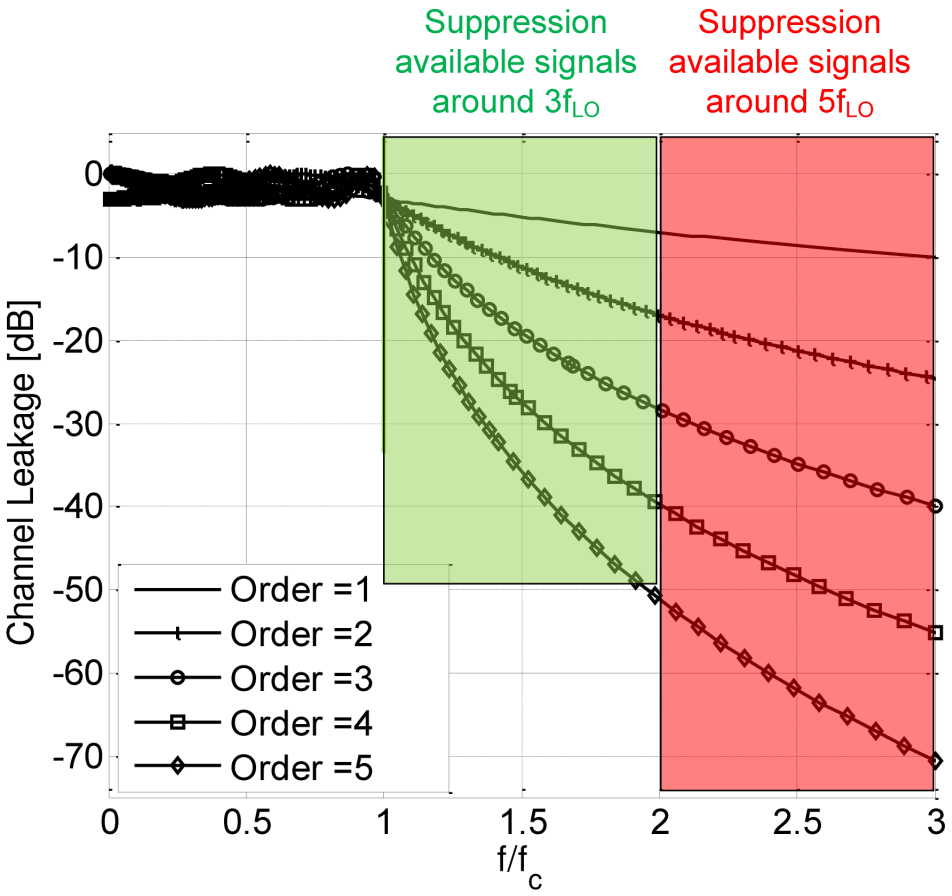


Figure 2.4: Typical roll-off of Chebyshev low-pass filter for various orders.

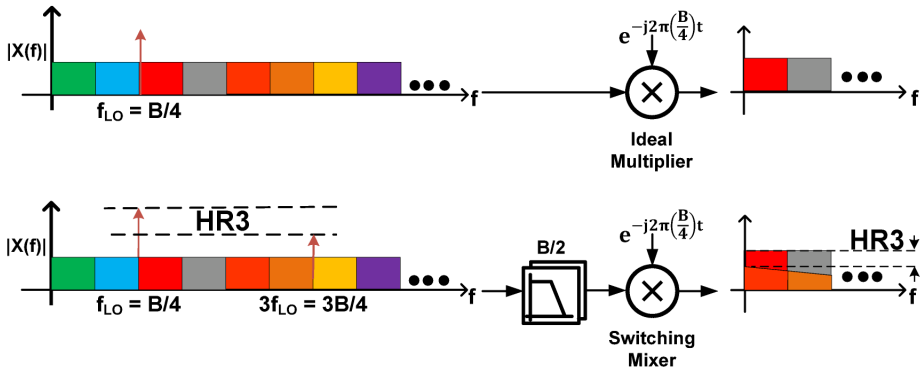


Figure 2.5: A low pass filter to relax the harmonic rejection requirements of the IDC unit cell.

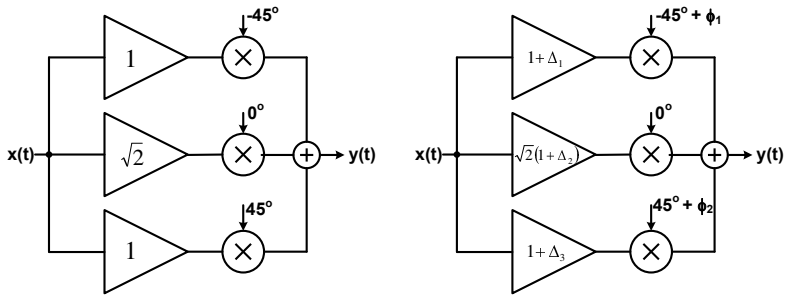


Figure 2.6: (a) A block diagram of a classical harmonic rejection mixer. (b) A block diagram of a classical harmonic rejection mixer including mismatches.

gains of $1+\Delta_1$, $\sqrt{2}(1+\Delta_2)$, $1+\Delta_3$ and phases of $-45^\circ+\phi_1$,0 and $45^\circ+\phi_2$, HR_3 can be calculated as

$$HR_3 = \frac{\sqrt{2}\cdot\lambda_2 + \lambda_1\cdot e^{j(-\pi/4+\phi_1)} + \lambda_3\cdot e^{j(+\pi/4+\phi_2)}}{\sqrt{2}\cdot\lambda_2 + \lambda_1\cdot e^{3j(-\pi/4+\phi_1)} + \lambda_3\cdot e^{3j(+\pi/4+\phi_2)}}. \tag{2.6}$$

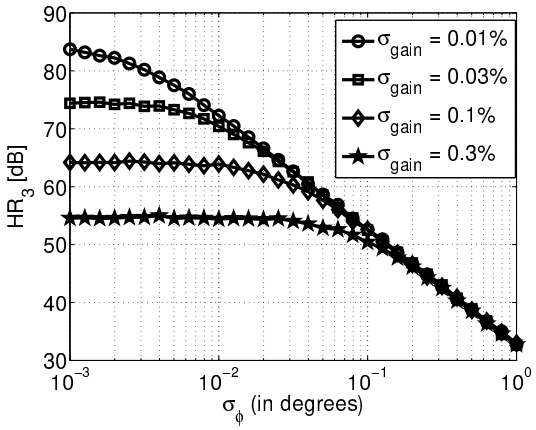
Similarly, the fifth harmonic rejection (HR_5) is defined as the ratio of conversion gain of the signals around the fundamental of the LO and the conversion gain of the signals around the fifth harmonic of the LO. HR_5 can be calculated as

$$HR_5 = \frac{\sqrt{2}\cdot\lambda_2 + \lambda_1\cdot e^{j(-\pi/4+\phi_1)} + \lambda_3\cdot e^{j(+\pi/4+\phi_2)}}{\sqrt{2}\cdot\lambda_2 + \lambda_1\cdot e^{5j(-\pi/4+\phi_1)} + \lambda_3\cdot e^{5j(+\pi/4+\phi_2)}} \tag{2.7}$$

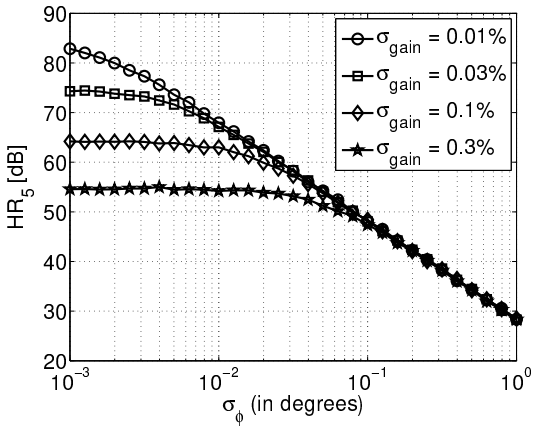
where $\lambda_i = 1+\Delta_i$. The achievable third harmonic rejection is plotted in Fig. 2.7(a)[2].

In order to achieve -60dB or less channel to channel signal leakage, the third-harmonic rejection of the mixers have to be greater than 60dB. This translates to a gain match re-

[2]The figure plots harmonic rejection vs the standard deviation of gain and phase errors. For every standard deviation, Δ and ϕ were generated 1000 times using Gaussian random number generator and the harmonic rejection was computed. The harmonic rejection was computed, averaged in linear scale and then converted converted to dB scale.



(a)



(b)

Figure 2.7: Achievable harmonic rejection ratios for the classical harmonic-reject mixer as a function of gain and phase mismatches.

quirement of better than 0.1% and a phase matching requirement of better than 0.03°. For an LO of 5GHz, the timing match is required to be better than 16.5fs for the harmonic reject mixer.

2.5 Effect of finite image rejection of the quadrature mixers

The effect of finite image rejection of the quadrature mixers is illustrated in Fig. 2.8. Finite image rejection in a mixer results in signal leakage from undesired channels; thereby in a degradation of SNR. The signal leakage is directly proportional to the image rejection of the mixer.

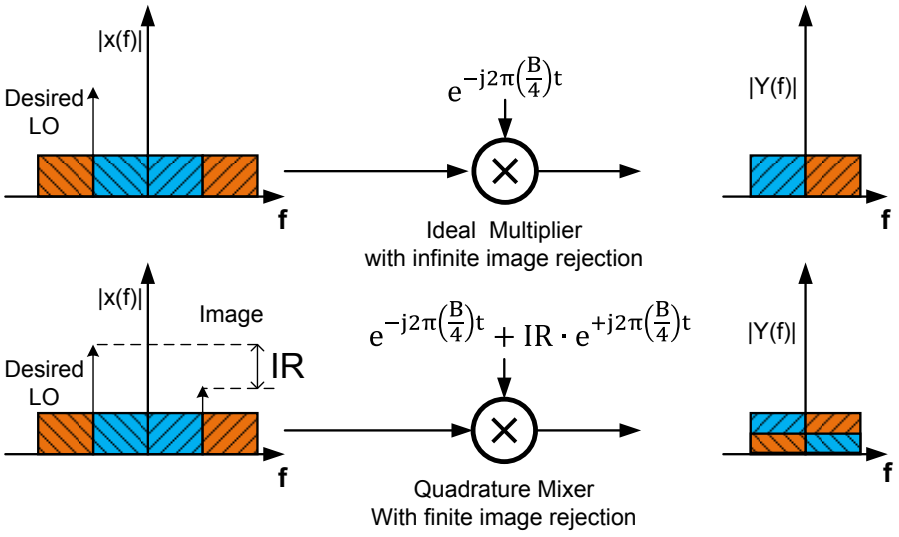


Figure 2.8: Effect of finite image rejection on signal leakage.

2.5.1 Achievable image rejection ratios

The effect of gain and phase mismatches on image rejection is in [18]. For a gain mismatch, Δ, and a phase mismatch, ϕ, the achievable image rejection can be calculated as

$$IR \approx \frac{\Delta^2 + \phi^2}{4} \tag{2.8}$$

Fig. 2.9 shows typical image rejection values for various phase and gain mismatches between the I and Q phases. Polyphase filters are proposed in [19] to filter the image and

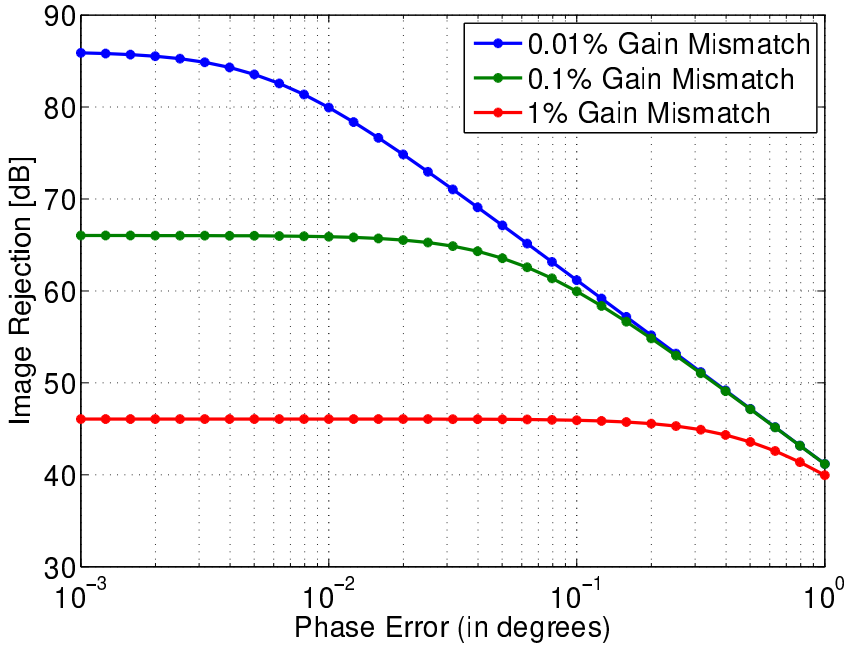


Figure 2.9: Image rejection as function of gain and phase mismatches between the I and Q signal paths.

improve the image rejection in narrow band systems. However, considering the broadband nature of the image signal (spanning from DC to signal bandwidth, B) Pre-filtering techniques used for relaxing the harmonic rejection requirements do not work in the case of image rejection mixer. The IQ calibration described in [20] can help improve the image

rejection of the last stage but does not help the leakage in previous stages. The SNR is then limited to the raw image rejection in a quadrature mixer.

2.6 Typical mismatches in gain and timing due to statistical variations in MOS transistors

From section 2.4 and section 2.5, it is clear that gain and phase error are crucial limiting factors to SNR in an iterative down-converter. In this section, an estimate of typical gain errors and phase errors are presented.

2.6.1 Gain errors

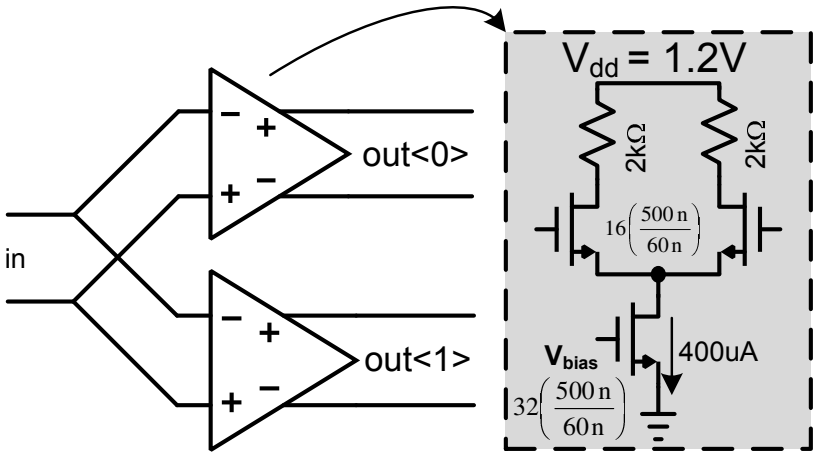


Figure 2.10: Monte-Carlo simulation results for the ratio of gains of two identical amplifiers. Distribution based on data from thousand runs.

The simulation setup used for the experiment is shown in Fig. 2.10. In order to get an estimate of typical Gain errors, the small-signal gain ratios of the two amplifiers are

measured. A 1000-run Monte-Carlo simulation was conducted to measure the gain ratio of the two amplifiers. It shows that the statistical variation in MOS transistor parameters can cause the rising edges to be offset with a $\sigma_{\text{gain,ratio}} = 1.2\%$. The amplifier consumes $420\mu A$ from a 1.2V supply.

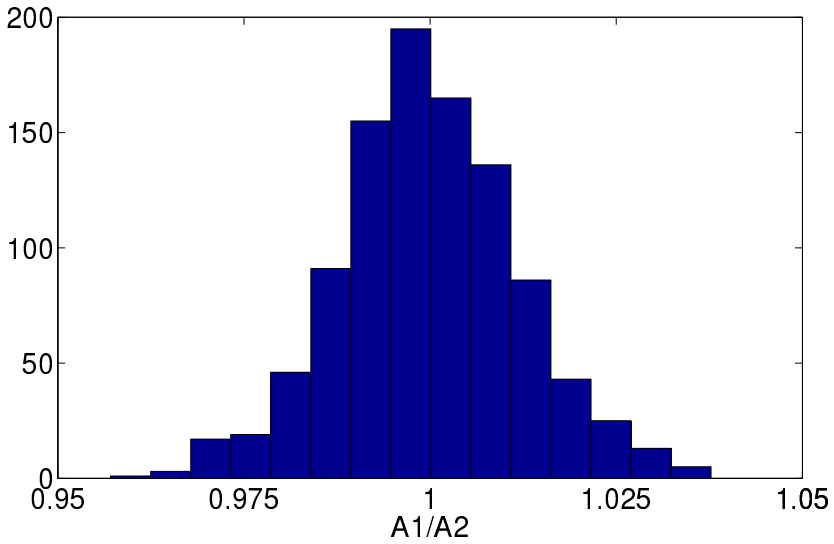


Figure 2.11: Monte-Carlo simulation results for the ratio of gains of two identical amplifiers. Distribution based on data from thousand runs.

2.6.2 Timing errors

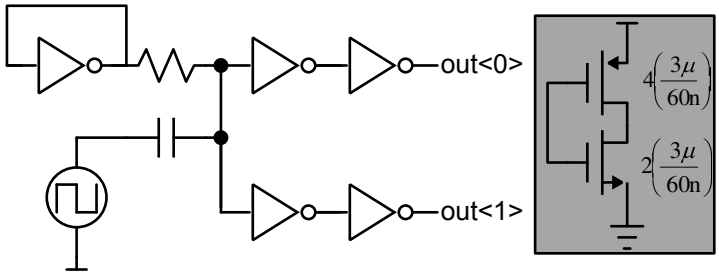


Figure 2.12: A simulation setup to estimate the timing difference between two clock buffers.

The simulation setup used for the experiment is shown in Fig. 2.12. In order to get an estimate of typical RF timing offsets, the time differences between the rising edges of two inverters are measured. A 1000-run Monte-Carlo simulation was conducted to measure the timing mismatch between two inverters. It shows that the statistical variation in MOS transistor parameters can cause the rising edges to be offset with a $\sigma_{\Delta t} = 132$fs. The image

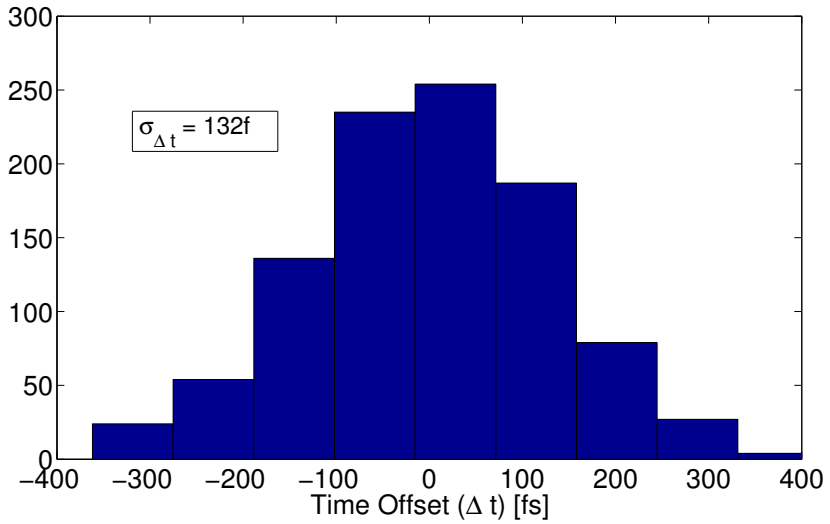


Figure 2.13: Monte-Carlo simulation results of timing offsets between the rising edges of two inverter outputs. Distribution based on data from thousand runs.

rejection needs to be better than 60dB which translates to a gain matching of better than 0.1% and phase matching of better than 0.1°. For an LO of 5GHz, the timing match is required to be better than 55fs. The power consumption in each inverter is $200\mu W$. The variability can be reduced by increasing the device size and the power consumption.

2.7 Conclusions

The IDC based RF channelizer is capable of channelizing the input spectrum (with a bandwidth B) into 2^{N-1} parallel outputs (each with a bandwidth of $\frac{B}{2^{N-1}}$) after N stages of frequency translation. The IDC operates with a fixed frequency PLL, thus simplifying the LO generation greatly.

Signal leakage is unavoidable with every stage of mixing. Further, it is directly proportional to image rejection or harmonic rejection. So, important limiting factors of the dynamic range of the RF channelizer are the finite harmonic rejection and image rejection.

In order to achieve -60dB or less channel to channel signal leakage, the third-harmonic rejection of the mixers have to be greater than 60dB. This translates to a gain match requirement of better than 0.1% and a phase matching requirement of better than 0.03°. For an LO of 5GHz, the timing match is required to be better than 16.5fs for the harmonic reject mixer.

The image rejection needs to be better than 60dB which translates to a gain matching of better than 0.1% and phase matching of better than 0.1°. For an LO of 5GHz, the timing match is required to be better than 55fs.

2.8 Future work

A concurrent iterative down-converter described in this chapter down-converts all the channels simultaneously. The dynamic range is limited by the signal leakage due to finite image

and harmonic rejection of the mixers. Baseband digital signal processing techniques could be used to cancel the signal leakage and recover the SNR in digital domain. This will enable power-efficient implementations of the IDC, thanks to the relaxed requirements on signal leakages.

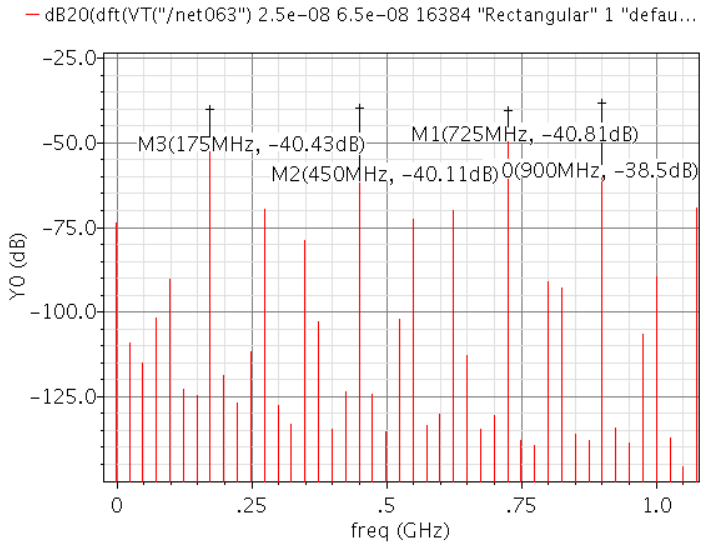


Figure 2.14: Simulated spectrum of the input signal to a 4-channel IDC built in 45nm SOI Technology.

An example 4-channel IDC, shown in Fig. 2.2, was implemented in 45nm SOI technology. The IDC channelizes the input spectrum between DC and 1GHz into 4 signals each of 250MHz bandwidth. The spectrum of the input and output of the IDC are shown in Fig. 2.14 and Fig. 2.15 respectively.

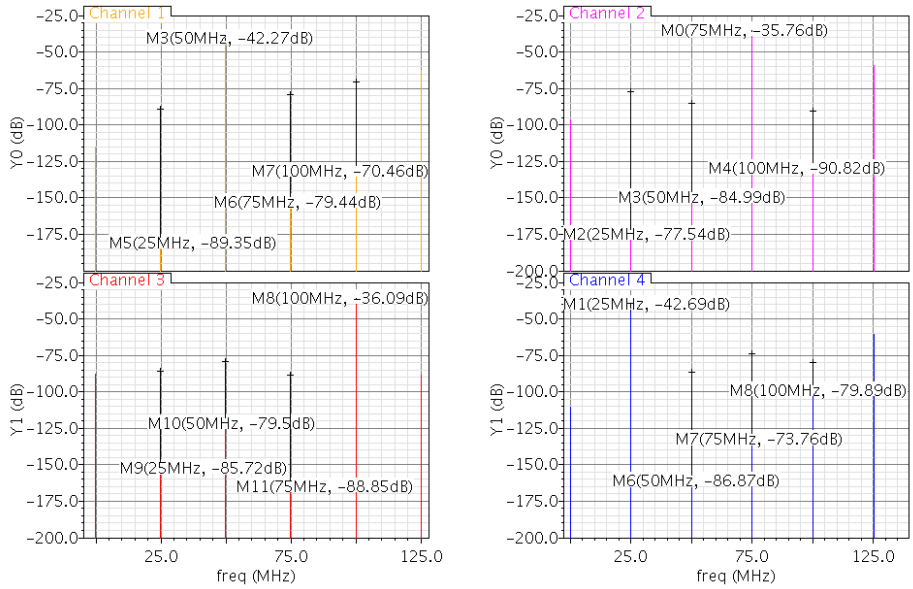


Figure 2.15: Simulated spectrum of the outputs of the 4-channel IDC built in 45nm SOI Technology.

Table 2.1: Summary of signal leakage in the 4-channel IDC built in 45nm SOI technology.

Source Destination	Channel 1	Channel 2	Channel 3	Channel 4
Channel 1	–	-43dB	-35dB	-45dB
Channel 2	-34dB	–	-54dB	-38dB
Channel 3	-44dB	-53dB	–	-43dB
Channel 4	-47dB	-37dB	-44dB	–

2.8.1 Post processing

Since all the outputs of the IDC are available, any leakage can be potentially cancelled. In order to demonstrate the feasibility, the simulation output shown in the previous section is used. The leakage transfer function was measured and the outputs are weighed and summed accordingly to remove the spurious leakages. If y1, y2, y3 and y4 are the ideal outputs of

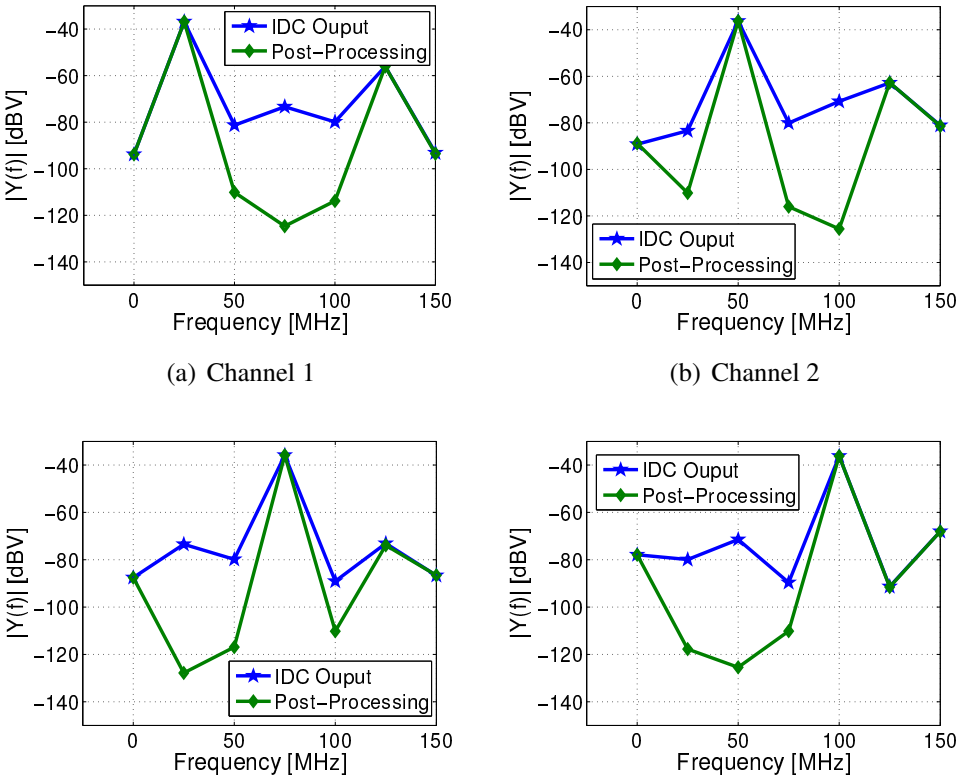
the IDC, the real outputs (with signal leakage) is given by

$$\begin{bmatrix} y1' \\ y2' \\ y3' \\ y4' \end{bmatrix} = \begin{bmatrix} \alpha_{11} & \alpha_{12} & \alpha_{13} & \alpha_{14} \\ \alpha_{21} & \alpha_{22} & \alpha_{23} & \alpha_{24} \\ \alpha_{31} & \alpha_{32} & \alpha_{33} & \alpha_{34} \\ \alpha_{41} & \alpha_{42} & \alpha_{43} & \alpha_{44} \end{bmatrix} \times \begin{bmatrix} y1 \\ y2 \\ y3 \\ y4 \end{bmatrix} \tag{2.9}$$

where α_{ij} is a complex number to represent the amplitude scaling and phase shift of the leaked signal.

Based on the leakage transfer function, an estimate of y1, y2, y3 and y4 could be calculated as

$$\begin{bmatrix} \hat{y1} \\ \hat{y2} \\ \hat{y3} \\ \hat{y4} \end{bmatrix} = \begin{bmatrix} 1 & -\alpha_{12} & -\alpha_{13} & -\alpha_{14} \\ -\alpha_{21} & 1 & -\alpha_{23} & -\alpha_{24} \\ -\alpha_{31} & -\alpha_{32} & 1 & -\alpha_{34} \\ -\alpha_{41} & -\alpha_{42} & -\alpha_{43} & 1 \end{bmatrix} \times \begin{bmatrix} y1' \\ y2' \\ y3' \\ y4' \end{bmatrix} \tag{2.10}$$



(a) Channel 1 (b) Channel 2

(c) Channel 3 (d) Channel 4

Figure 2.16: Improvement in signal leakage after post-processing.

The algorithm described in (2.10) was implemented in matlab and the improvement in the signal leakage is shown in Fig. 2.16

Chapter 3

A 750MHz-11.25GHz Fast Channel Switching RF Channelizer with Three Concurrent Ouputs

3.1 Abstract

In this chapter, we propose an RF front-end architecture based on iterative down-conversion. The use of iterative down-conversion enables the incorporation of LO synthesis inside the signal path which enables rapid channel hopping. An example 0.75GHz-11.25GHz RF front-end is implemented in TSMC 65nm CMOS process. The RF front-end channelizes the input spectrum into seven outputs each of 1.5GHz bandwidth. The RF channelizer exhibits ability of rapid channel switching, as well as concurrency. The 0.75GHz-11.25GHz

RF front-end channelizes the input with an average dynamic range of 54dB, consuming an average power of 540mW, offering a spectrum-analysis-energy efficiency of 1.73GHz/uJ.

3.2 Introduction

Futuristic radio standards like cognitive radio (CR) are envisioned to communicate over any available spectrum in a broad spectrum bandwidth making broadband signal analysis a necessity. Direct time-domain sampling and digitization of a multi-GHz signal with multiple incident blockers is a challenging task. Alternatively, frequency channelization can be used wherein the input spectrum is decomposed into multiple channels of narrower bandwidth. The task of digitizing its output is simplified thanks to the (1) reduced sampling rate requirements and (2) reduced dynamic range requirements due to the filtering of out-of-band blockers.

Active research is being conducted on broadband signal analysis and frequency channelization [21; 22; 13].

Wang presents an architecture with multiple parallel receivers to down-convert multiple bands simultaneously [22]. The main drawback of this architecture is the signal leakage from one channel to another. An active splitter can be used to provide isolation between multiple receive paths. However, the circuit driving multiple receivers (typically the LNA) is loaded with a large capacitance which restricts the bandwidth.

Goel demonstrates a two stage frequency translation architecture in [21] where the input signal is first up-converted to an IF of 12GHz and then down-converted using a fixed 12GHz

frequency. This architecture is shown to be robust to signal leakages. However, it still suffers from the long scanning duration due to the PLL settling time.

[13] presents the idea of iterative down-converter (IDC) to solve the problem of LO synthesis in broadband frequency channelizers. It uses a cascade of image rejection mixers to incorporate LO synthesis into signal path. However, stringent interstage filtering is required in the architecture to mitigate degradation from signal leakage caused by non-ideal image rejection or harmonic rejection of individual mixers.

The focus of this research is to develop a RF front-end device called RF channelizer which splits the input signal into multiple channels. This relaxes the requirements for the ADC sampling the output of the channelizer. Additionally, the RF channelizer ensures agile channel hopping which enables rapid spectrum analysis.

In this chapter, a novel 3-way splitting IDC architecture is introduced for an improved signal leakage performance. A prototype RF channelizer is designed using the 3-way splitting IDC to demonstrate features of concurrency and rapid channel switching.

3.2.1 Summary of the contributions of this research

In this chapter, novel architectural ideas to realize RF channelizers are presented. These have been implemented in a partially concurrent RF channelizer with an input bandwidth of 0.75 to 11.25GHz and an output bandwidth of 1.5GHz.

Here we summarize the key research contributions at the system level.

- A new 3-way iterative down-converter approach has been developed that overcomes

the shortcomings of the original 2-way bifurcating iterative down-converter for RF applications.

- An additional path is added to accommodate the use of realistic filtering (i.e. sufficiently low order) functions that can be realized on chip at RF frequencies.

- By introducing appropriate interstage RF filtering, the harmonic reject mixing requirements are alleviated to levels that are feasible for on-chip implementation.

- The architecture is amenable for a concurrent implementation as well as a fast-switching single output implementation. A partially concurrent RF channelizer is implemented to demonstrate feasibility of both.

A prototype of the channelizer has been realized in a 65nm CMOS technology. At the circuit level, a multi-mode mixer has been invented. The multi-mode mixer re-uses the mixer hardware to implement (a) signal mixing and (b) signal transmission with polarity control. The idea of multi-mode mixer has enables the re-use of 5.25GHz filter, thereby saving area.

3.2.2 Organization of the sections in this chapter

Rest of this chapter is organized as follows: section 3.3 describes the evolution of the novel 3-way IDC architecture, section 3.4 discusses the development of the RF channelizer using the IDC, section 3.5 describes the requirements (linearity, noise figure, harmonic rejection and so on) of the channelizer, section 3.6 presents the transistor level design of the circuit

blocks, section 3.7 presents simulation results, section 3.8 discusses the simulation results and compares it the existing state-of-art. Conclusion are presented in section 3.9.

3.3 Three-way splitting IDC architecture

A detailed description of signal leakage mechanisms in cascaded image-rejection mixer based IDC has been presented in chapter 2. Signal leakage is unavoidable with every stage of mixing. Further, it is directly proportional to image rejection or harmonic rejection. So, important limiting factors of the dynamic range of the RF channelizer are the finite harmonic rejection and image rejection. In order to achieve -60dB or less channel to channel signal leakage, the third-harmonic rejection of the mixers has to be greater than 60dB. This translates to a gain match requirement of better than 0.1% and a phase matching requirement of better than 0.03°. For an LO of 5GHz, the timing match is required to be better than 16.5fs for the harmonic reject mixer. The image rejection needs to be better than 60dB which translates to a gain matching of better than 0.1% and phase matching of better than 0.1°. For an LO of 5GHz, the timing match is required to be better than 55fs.

In order to overcome the above limitations, a three-way splitting iterative down-converting (3-way-IDC) is developed in this chapter. This architecture enables a low-pass filter to compliment harmonic rejection mixer to improve the spurious leakage.

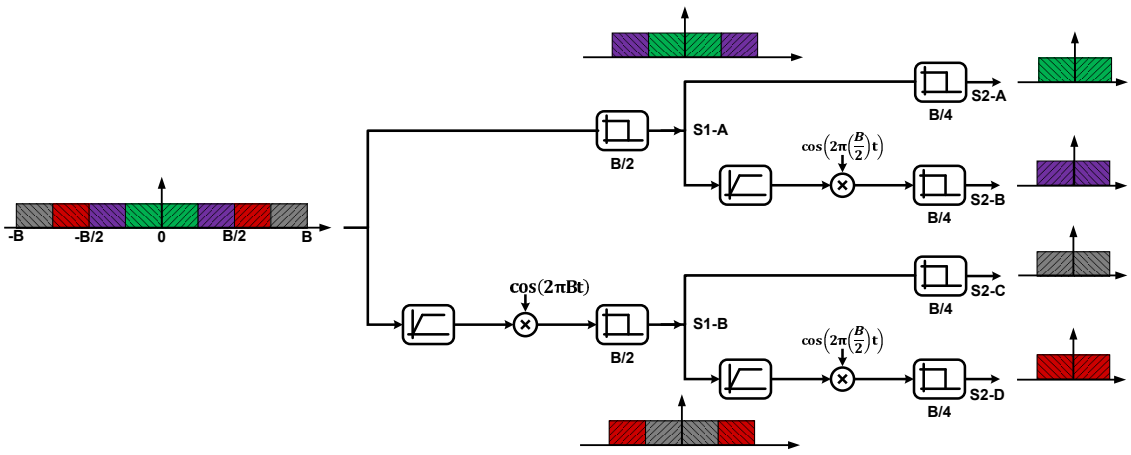


Figure 3.1: A channelizer to split the input spectrum of bandwidth B into two channels of bandwidth B/2 using brick wall filters.

3.3.1 Development of the 3-way-IDC

The unit cell of a 3-way-IDC is shown in Fig. 3.1. A signal bandwidth of bandwidth B is input to the 3-way-IDC. Output "S1-A" is a low-pass filtered version of the input. The bandwidth of the low-pass filter is $\frac{\mathrm{B}}{2}$. In other words, "S1-A" contains lower half of the input spectrum. In the other path, the signal is mixed with $f_{\mathrm{LO}} = \mathrm{B}$ and then low-pass filtered (with a bandwidth $\frac{\mathrm{B}}{2}$). Output "S1-B" contains the upper half of the spectrum. The 3-way-IDC bifurcates the input spectrum and passes the signals to the next stage. The next stage is a similar unit cell, operating at half the LO frequency and signal bandwidth.

In the discussions so far, the low-pass filters have been assumed to be brick-wall filters. A high frequency signal (above $\frac{\mathrm{B}}{2}$) is an image of the desired signal for the next stage's mixer. In the absence of a brick wall filter, the high frequency signal would undergo only a finite attenuation. This results in spurious leakage of undesired channels. The effect of using a real filter is shown in Fig. 3.2.

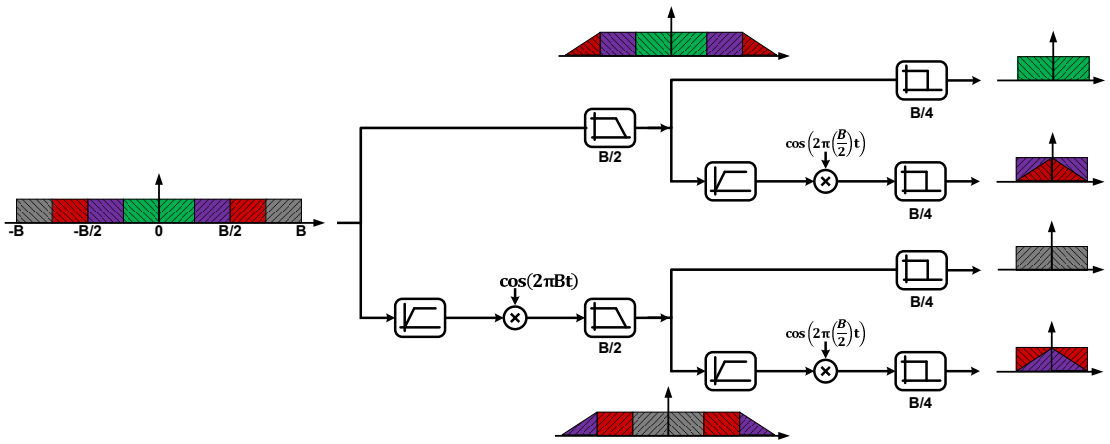


Figure 3.2: The behavior of the channelizer using real filters: signal leakage.

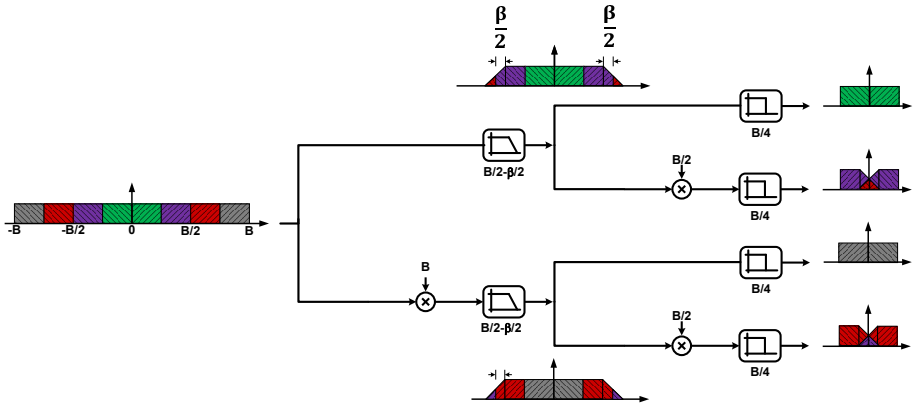


Figure 3.3: Signal leakage reduced by decreasing the bandwidth of the filter. The leakage is attenuated to negligible levels at the cost of loss of signals around midband.

The drawback of a finite filter roll-off and its associated signal leakage can be overcome by using a filter of a lower bandwidth, $\frac{B-\beta}{2}$, as shown in Fig. 3.3. By using a smaller bandwidth, the signal leakage is reduced, possibly to negligible levels. Further reduction of signal leakage is possible by increasing the value of β.

By using a filter of smaller bandwidth, $\frac{B-\beta}{2}$, a signal of bandwidth β around midband is available in neither of the two outputs. A third path is introduced in the unit cell in order

to recover the signals around the midband as shown in Fig. 3.4.

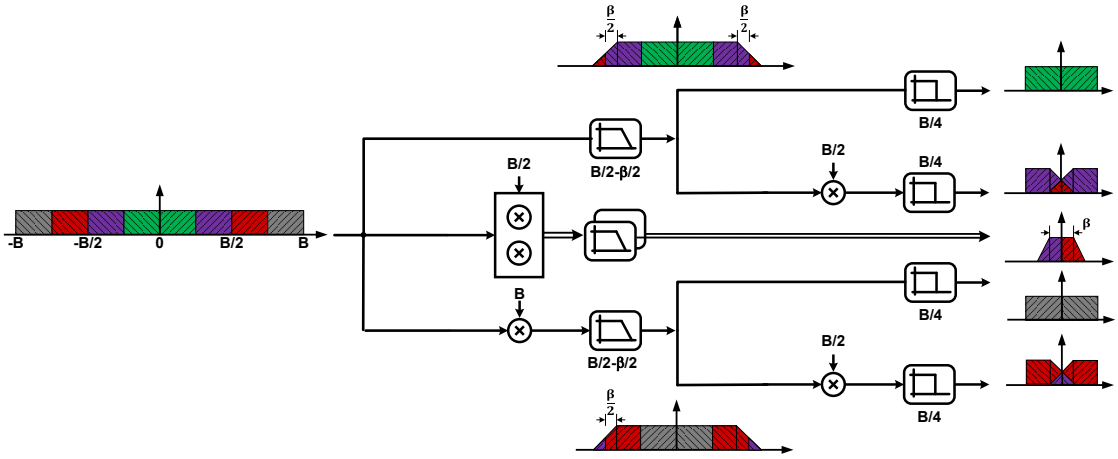


Figure 3.4: Recovery of signals around midband by using the midband recovery path.

The modified IDC unit cell implementation and its operation is shown in Fig. 3.5. The

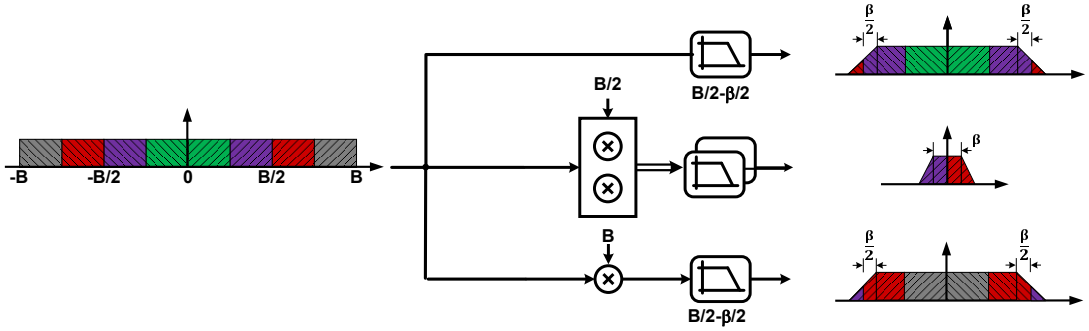


Figure 3.5: Conceptual understanding of the 3-Way splitting IDC.

mid-band recovery path is created to relax the roll-off requirements of the low-pass filter in the top and bottom path. A bandwidth β is down converted directly to baseband. The signal leakage for various values of β and filter order is shown in Fig. 3.6[1].

It can be seen that increasing β relaxes the filter roll-off requirements for a certain

[1] A Chebyshev filter with an in-band ripple of 3dB is assumed for the simulations.

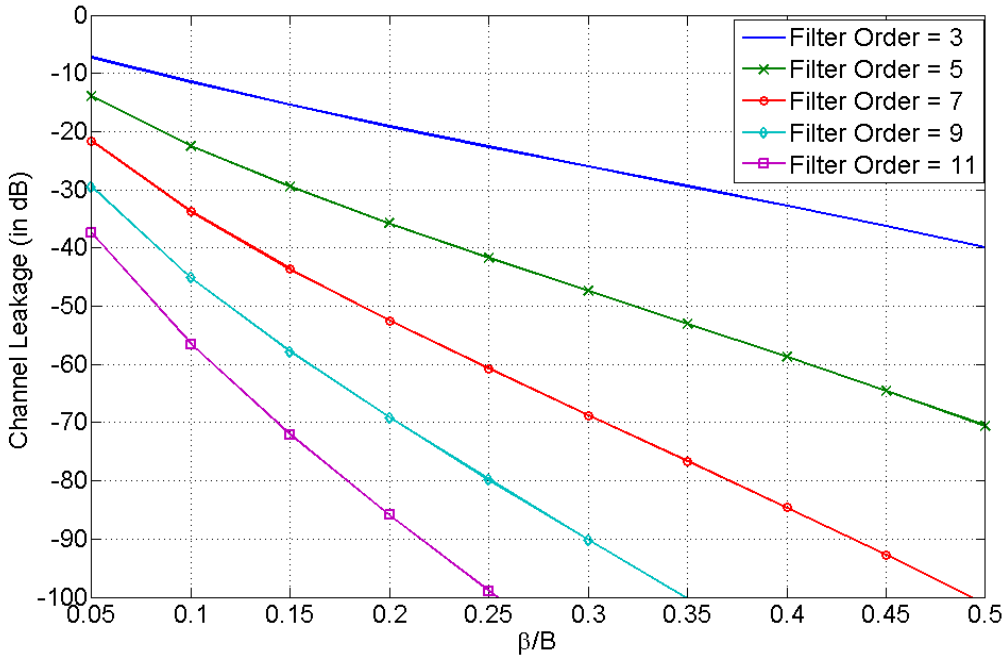


Figure 3.6: Channel leakage due to subsequent mixing as a function of filter order and β

signal leakage requirement or decreases the signal leakage for a given filter order. The cost of increasing β is increased bandwidth of the midband ($\left(\frac{B-\beta}{2} - \frac{B+\beta}{2}\right)$).

3.3.2 Advantages of a 3-Way iterative down-converting RF channelizer

- Simplification of mixer requirements.
  - No mixer is required in low band; the signal passes through the filter directly through to the output.
  - Mixing in the high band requires relaxed image rejection or harmonic rejection based on the filter in the previous stage.

  - I/Q mixer in midband recovery path requires relaxed harmonic rejection based on the filtering in the previous stage.

- Filter order can be traded-off with mid-band bandwidth. Further, introduction of harmonic rejection mixers or image rejection mixers can reduce the filter requirement greatly.

- Fixed frequency PLLs are required.

3.4 An implementation of RF channelizer based on the proposed three-way iterative down-converting architecture

A fully concurrent RF channelizer is shown in Fig. 3.7. It channelizes a bandwidth of 10.5GHz (750MHz-11.25GHz) into seven parallel bands. All the output channels are available simultaneously at the same time.

The operation of the RF channelizer is described in Fig. 3.8 and Fig. 3.9. The input to the channelizer consists of signals from 750MHz to 11.25GHz. After amplification in LNA, the signal is frequency channelized into three ways as shown in Fig. 3.8. Signals around the midband, 5.25GHz to 6.75GHz, is directly down-converted using a 6GHz I/Q Mixer. For this stage, β is chosen to be 1.5GHz. Thus the output of the IQ mixer is a signal with a bandwidth of 1.5GHz (complex signal: -750MHz to 750MHz). The remaining spectrum is

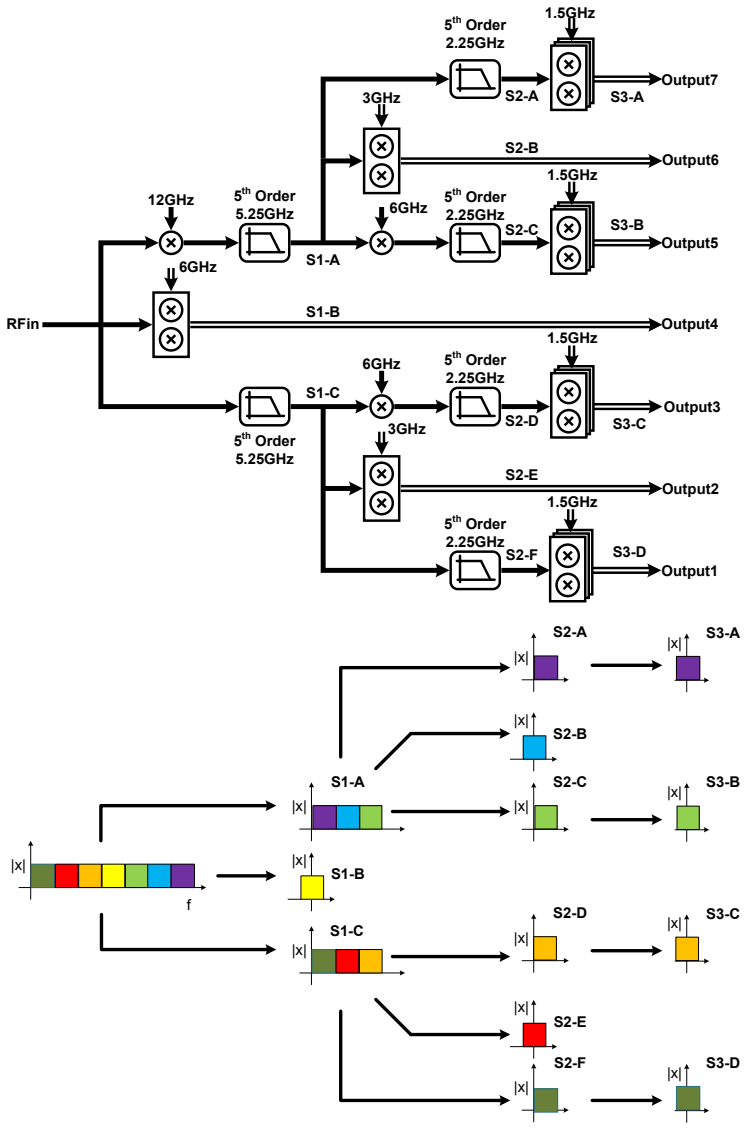


Figure 3.7: Block diagram of a fully concurrent 0.75GHz-11.25GHz RF channelizer.

bifurcated into two signals each of bandwidth 4.5GHz. The output of Stage 1 is passed to the second stage.

The operation of the second stage is similar to the first. Signals around the midband, 3GHz (or 9GHz), is directly down-converted using a 3GHz (or 9GHz) I/Q mixer. The signal leakage in this path is limited by a combination of filter roll-off in the first stage and

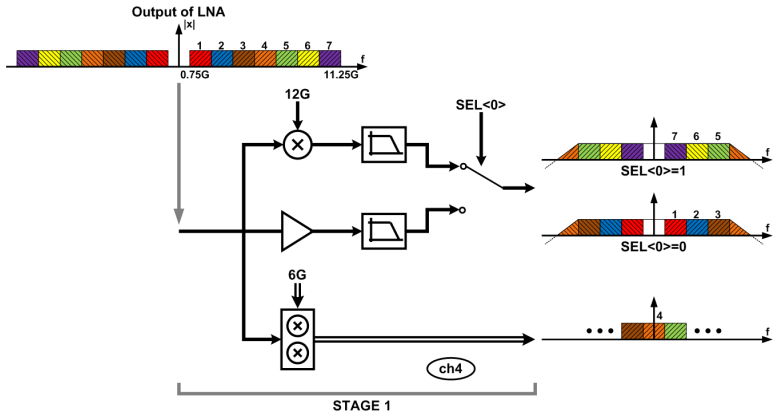


Figure 3.8: Operation of first iterative down-converting stage of the RF channelizer.

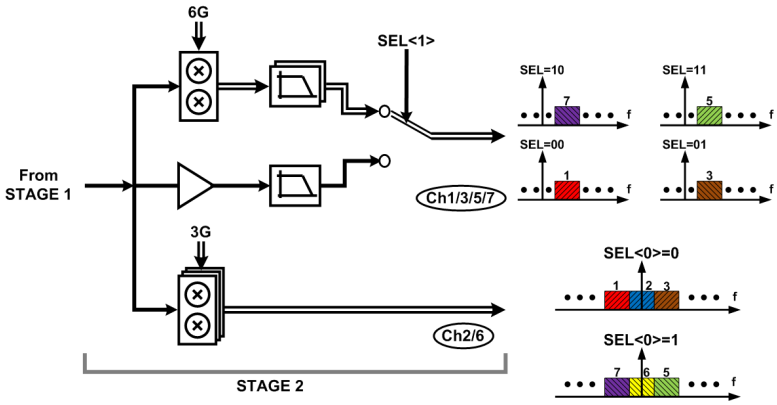


Figure 3.9: Operation of the second down-converting stage of the RF channelizer.

harmonic rejection of the I/Q mixer. In order to improve the signal leakage, a I/Q harmonic rejection mixer is used. The remaining spectrum is bifurcated. In this stage, the complexity of mixers is higher. A simple mixer in the first stage becomes an IQ mixer. An IQ mixer of first stage becomes a I/Q harmonic rejection mixer. However, these mixers are operating at lower frequencies than the ones in the first stage.

The RF channelizer presented in Fig. 3.7 describes a concurrent version, wherein all the outputs of the channelizer are available simultaneously. In order to demonstrate the fast switching in addition to the concurrency feature, the architecture is modified to a partially

concurrent version as shown in Fig. 3.10.

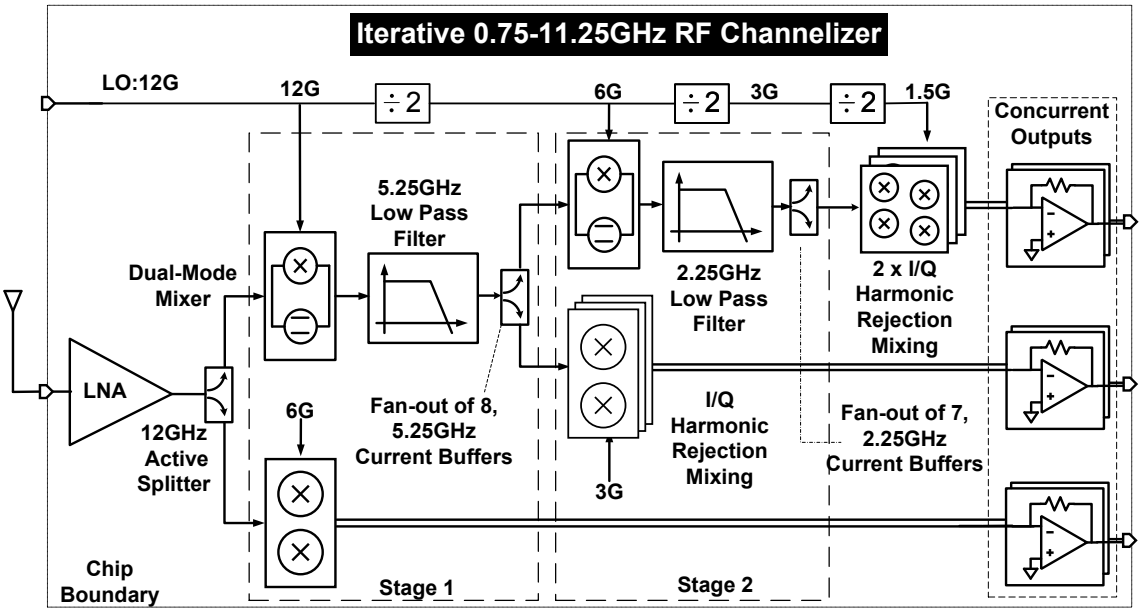


Figure 3.10: Block diagram of a partially concurrent-output RF channelizer.

The top and bottom path of the first down-conversion stage (in Fig. 3.7) have been merged into one path. The merger requires a special block which can operate in two modes: (a) mixing mode (b) transparent mode. In our implementation, the special block is called the multi-mode mixer. Further discussion of the multi-mode mixer is presented in section 3.6.1.

The input to the first down-conversion stage is assumed to have a bandwidth of 11.25GHz and higher frequencies are assumed to be absent or sufficiently attenuated[2]. However, the same assumption does not hold for the second down-conversion stage. The 5.25GHz filter has a finite filter roll-off. Since the attenuation of the image signal (6.75GHz and higher) may not be sufficient, an I/Q mixer is used (in place of a simple mixer of stage 1).

[2]In reality, this can be done by using a high quality off-chip filter if filter is necessary.

Similarly, signals around the third harmonic of the 3GHz mixer may not be sufficiently attenuated by the filter. In order to overcome the finite suppression, a harmonic rejection mixer is used (in place of an I/Q mixer of stage 1).

A simplification similar to a merger in stage 1 (as discussed above) is applied to the second down-conversion stage also. The top and bottom paths (in Fig. 3.7) are merged into one path.

The proposed RF channelizer has three concurrent outputs.

- Output 1: Channel 4 (6GHz $\pm$ 0.75GHz)
- Output 2: Channel 2 or 6 (3GHz or 9GHz $\pm$ 0.75GHz)
- Output 3: Channel 1 or 3 or 5 or 7 (1.5GHz or 4.5GHz or 7.5GHz or 10.5GHz $\pm$ 0.75GHz)

3.5 System requirements

The channelizer is being designed to have a noise floor at -95dBm and accommodate a blocker power of up to -35dBm. In the following subsections, the noise figure, linearity and other specifications for the channelizer and its blocks are derived.

3.5.1 Noise figure

In one of the target applications of the RF channelizer, the final bandwidth of the output channel is 1MHz. The noise power in this channel, at the input of the RF channelizer is

$$\begin{aligned} \text{Noise power} = -174 + 10\log(1e6) &= -114\text{dBm} \\ \text{Noise floor level} &= -95\text{dBm} \\ \text{Noise figure} &= 19\text{dB} \end{aligned} \tag{3.1}$$

3.5.2 Linearity

3.5.2.1 IIP3 requirement

The interferers are assumed to be located at frequencies such that the third order inter-modulation products fall on top of the desired signal. In order to calculate the IIP3 requirement for the channelizer, the third order inter-modulation terms are assumed to be equal to the noise floor.

$$\text{Power of the unwanted third order inter-modulation terms} = -95\text{dBm} \tag{3.2}$$

$$\text{Power of the inter-modulating interferers} = -35\text{dBm} \tag{3.3}$$

$$\text{IIP}_3 = -35\text{dBm} + 1/2 \times (94 - 35) = -5\text{dBm} \tag{3.4}$$

In the presence of N pairs of interferers, the inter-modulation products are assumed to add up in power. In that case, the power of each inter-modulation product should be at most $-94\text{dBm} - 10\log(\text{N})$. The IIP_3 requirement is then given by

$$\text{IIP}_3 = -5\text{dBm} + 5\log(\text{N}) \tag{3.5}$$

3.5.2.2 IIP2 requirement

The interferers are assumed to be located at frequencies such that the second order inter-modulation products fall in the same channel as the desired signal. In order to calculate the IIP2 requirement for the channelizer, the power of the second order inter-modulation terms are assumed to be equal to the noise floor.

$$\text{Power of the unwanted second order inter-modulation terms} = -95\text{dBm} \quad (3.6)$$

$$\text{Power of the inter-modulating interferers} = -35\text{dBm} \quad (3.7)$$

$$\text{IIP}_2 = -35\text{dBm} + (95 - 35) = 25\text{dBm} \quad (3.8)$$

In the presence of multiple pairs of interferers, the inter-modulation products are assumed to add up in power. In that case, the power of each inter-modulation product should be at most $-95\text{dBm} - 10\log(\text{N})$. The new IIP_2 is then given by

$$\text{IIP}_2 = 25\text{dBm} + 10\log(\text{N}) \quad (3.9)$$

The IIP2 requirement is achievable with careful layout, without calibration [23].

3.5.3 Motivation for the 12GHz/ 13GHz PLL

The RF channelizer employs multiple stages of down-conversion (section 3.4). In all the modes of operation of the channelizer, the last stage of down-conversion is a zero-IF down-conversion. The channelizer is then blind to signals close to the LO of the last down-conversion stage due to (a) LO-to-RF coupling and (b) 1/f noise. In 12GHz operation of

the PLL, the RF channelizer is blind to input signals at 1.5GHz, 3GHz, 4.5GHz, 6GHz, 7.5GHz, 9GHz and 10.5GHz. 13GHz operation of the PLL moves the blind spots away from these frequencies, thus enabling the recovery of the signals.

The dual frequency (12GHz/ 13GHz) operation of the PLL is then needed to ensure that the RF channelizer is able to scan the entire spectrum without blind spots.

3.5.4 Filtering and harmonic/image rejection requirements

In addition to the noise and linearity, the channelizer also suffers from SNR degradation due to signal leakages arising from impairments like image rejection and harmonic rejection. Fig. 3.11-3.17 show the dominant signal leakage mechanisms.

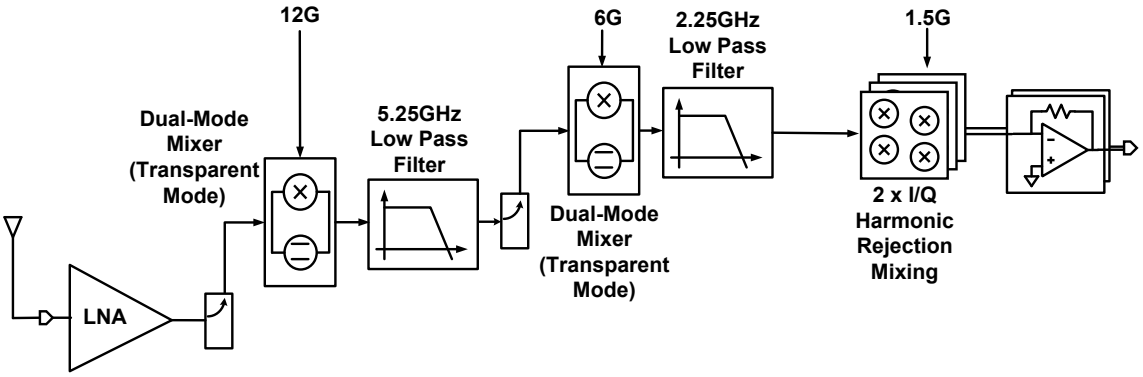
Based on the above signal leakage mechanisms, requirements for each block for better than 60dB (or 70dB) signal leakage levels are recorded in the Table 3.1.

Table 3.1: Image rejection and harmonic rejection requirements.

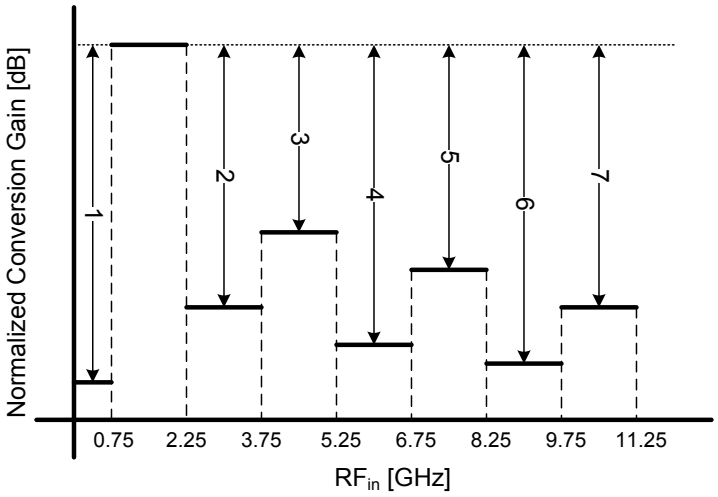
		Signal Leakage <-60dB	Signal Leakage <-70dB
1st stage 12G Mixer		No HR,IR requirements	No HR,IR requirements
1st stage 6G Mixer: IR		60dB*	70dB*
1st stage LPF		5.25G, 5th order	5.25G, 5th order
2nd stage 6G mixer: IR		38dB	48dB
3G mixer	IR	60dB*	70dB*
	HR3	14dB	24dB
2nd stage LPF		5th order	5th order
1.5G mixer	IR	60dB*	70dB*
	HR3	18dB	28dB

*Off-chip I/Q calibration can improve the image rejection.

In order to meet the requirements shown in Fig. 3.18, a fifth order elliptic filter is cho-



(a)

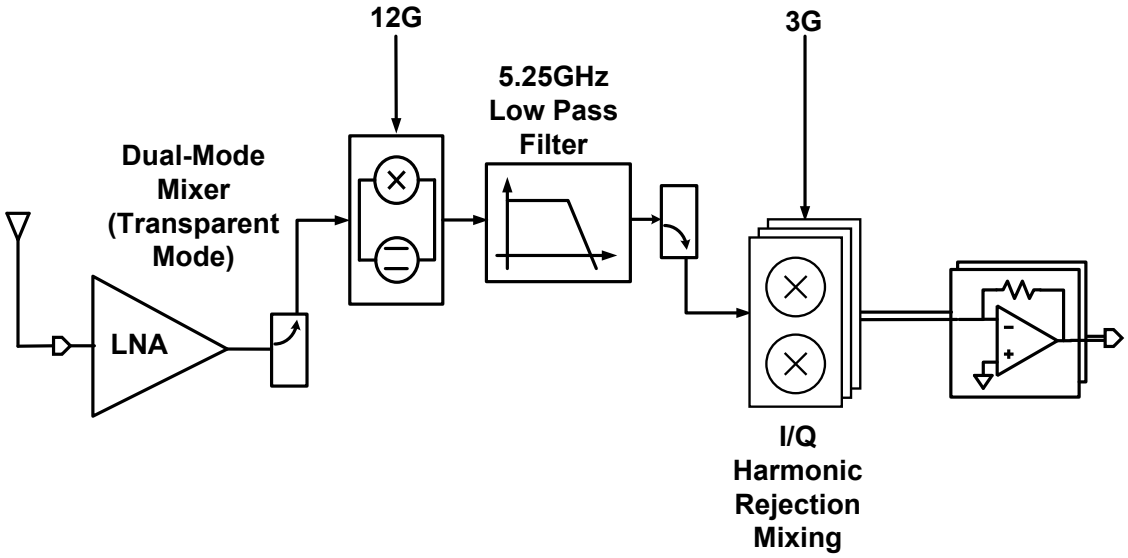


1: RF Feed-through in 1.5GHz mixer
2: Filtering in 2.25GHz + 2nd harmonic rejection of 1.5GHz mixer
3: Filtering in 2.25GHz + 3rd harmonic rejection of 1.5GHz mixer
4: Filtering in 2.25GHz, 5.25GHz + 4th harmonic rejection of 1.5GHz mixer
5: Filtering in 2.25GHz, 5.25GHz + 5th harmonic rejection of 1.5GHz mixer
6: Filtering in 2.25GHz, 5.25GHz + 6th harmonic rejection of 1.5GHz mixer
7: Filtering in 2.25GHz, 5.25GHz + 7th harmonic rejection of 1.5GHz mixer

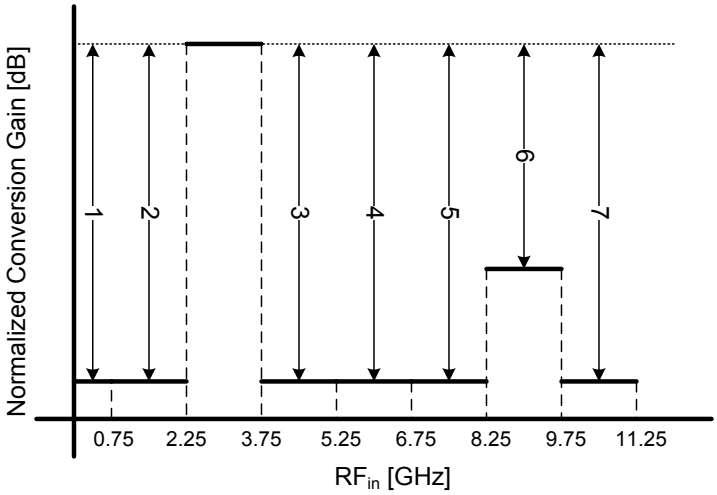
(b)

Figure 3.11: Signal leakage in channel 1.

sen.



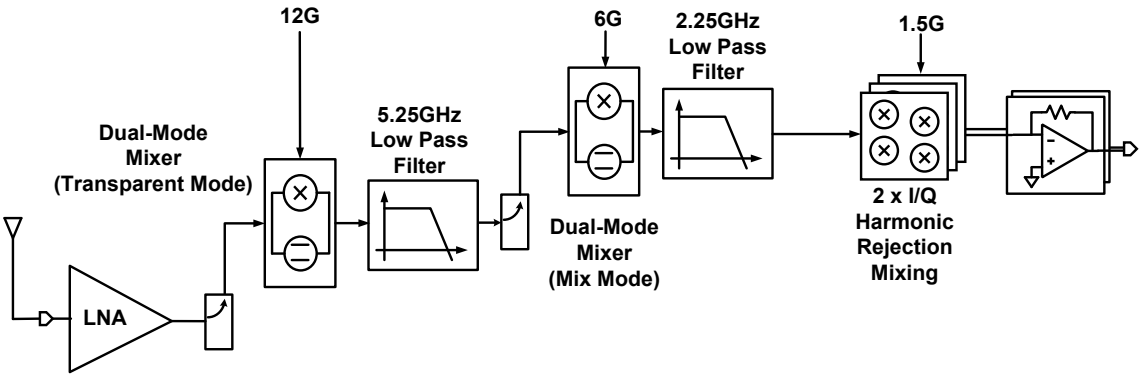
(a)



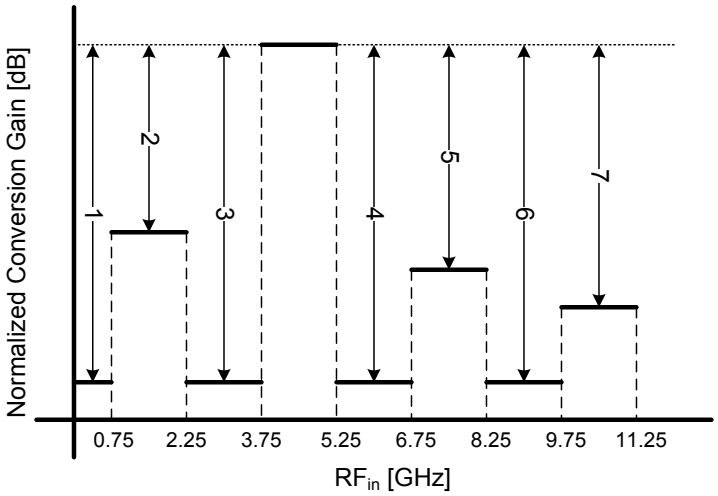
1: RF Feed-through in 3GHz mixer
2, 3, 4, 5, 7: Spurious mixer down-conversion ($M.f_{RF} - N.f_{LO}$)
6: Filtering in 5.25GHz + third harmonic rejection of 3GHz mixer

(b)

Figure 3.12: Signal leakage in channel 2.



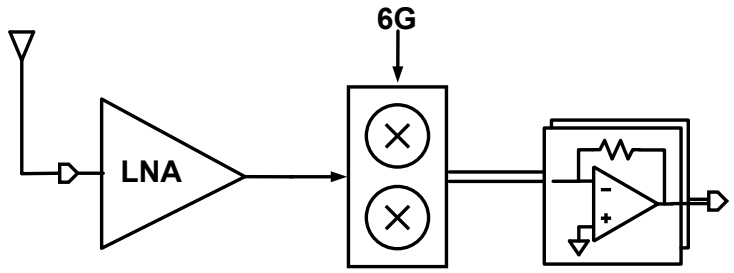
(a)



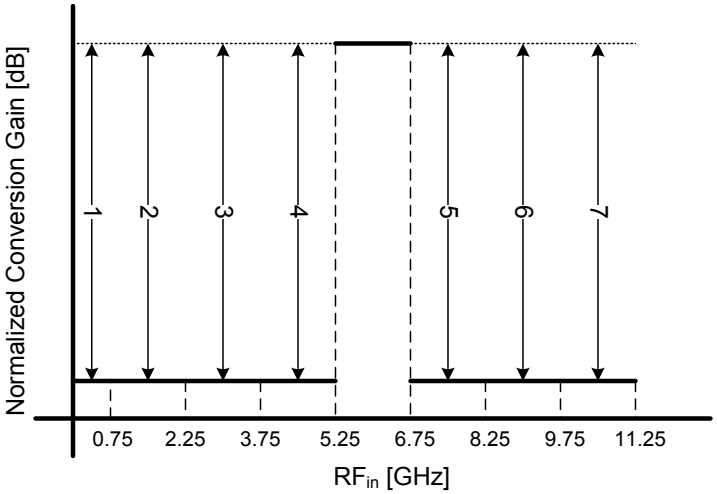
1, 3, 4, 6 : Spurious mixer down-conversion: $M.f_{RF} - N.f_{LO}$
2: RF feedthrough in 6GHz mixer
5: 5.25GHz Filtering + Image rejection in 6GHz mixer
7: 5.25GHz Filtering + 3rd harmonic rejection in 1.5GHz mixer

(b)

Figure 3.13: Signal leakage in channel 3.



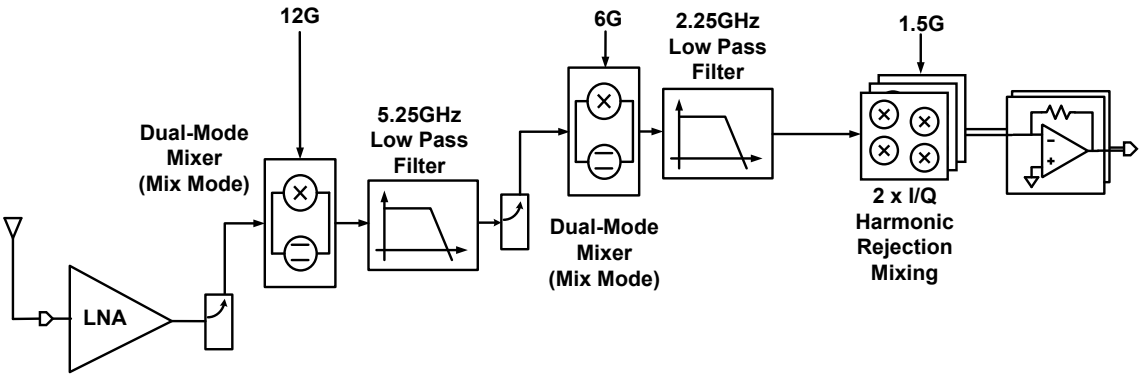
(a)



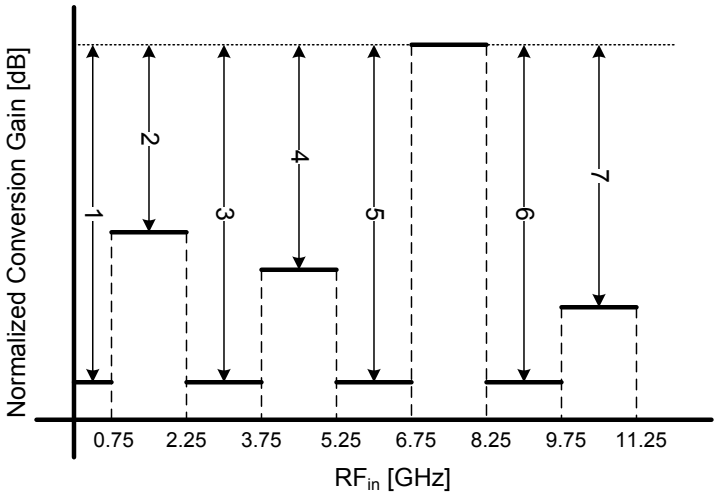
1: RF feed through in 6GHz mixer
2-7: Spurious mixer down-conversion: $M.f_{RF} - N.f_{LO}$

(b)

Figure 3.14: Signal leakage in channel 4.



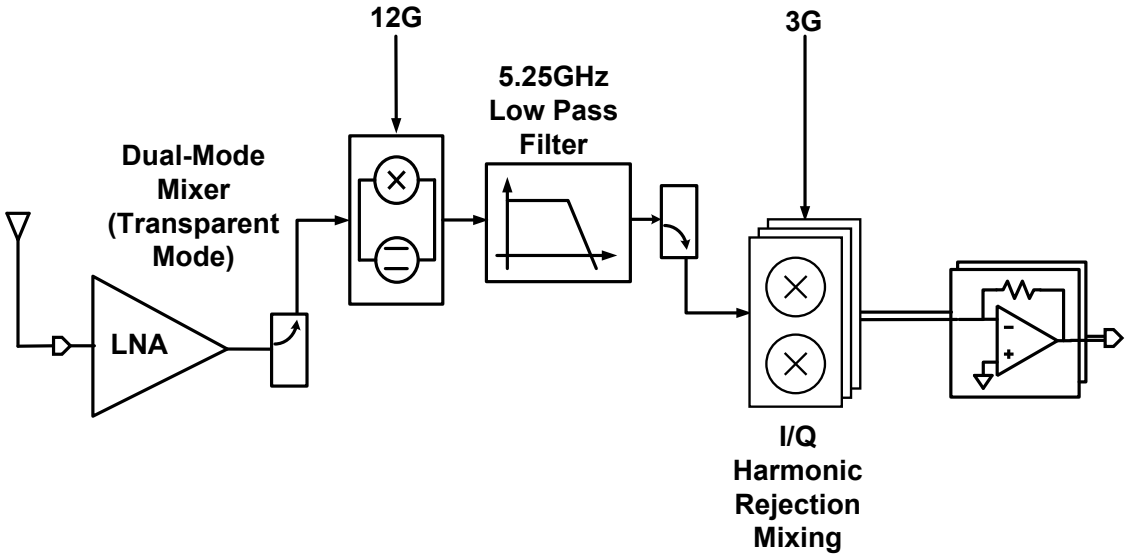
(a)



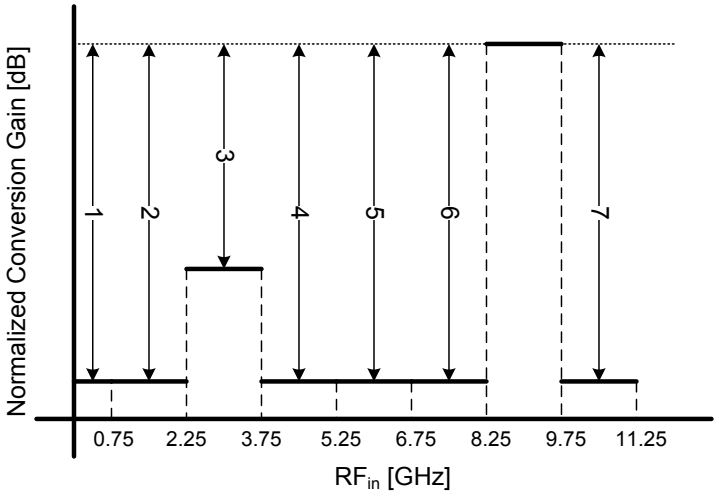
1, 3, 5, 6 : Spurious mixer down-conversion: $M.f_{RF} - N.f_{LO}$
2: 5.25GHz filtering + 3rd harmonic rejection of 1.5GHz mixer
4: 5.25GHz Filtering + Image rejection in 6GHz mixer, RF Feed-through in 12GHz mixer
7: 2.25GHz filtering + 3rd harmonic rejection in 1.5GHz mixer,
RF feed through in 6GHz mixer

(b)

Figure 3.15: Signal leakage in channel 5.



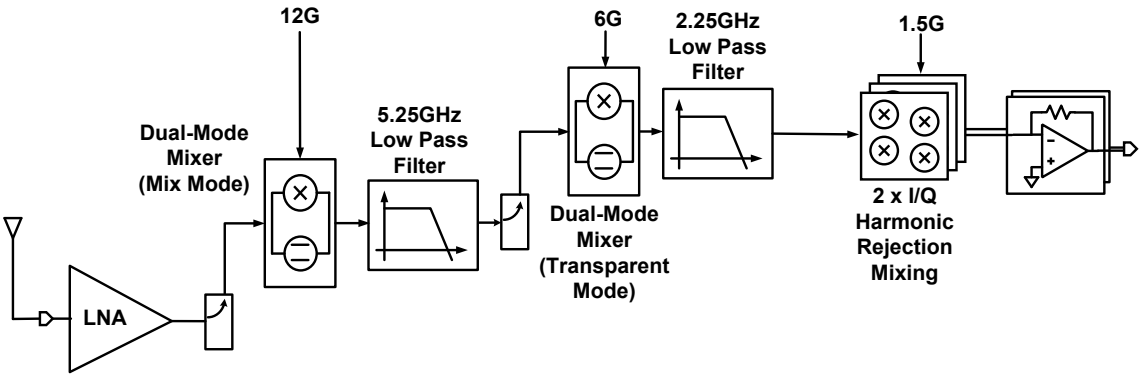
(a)



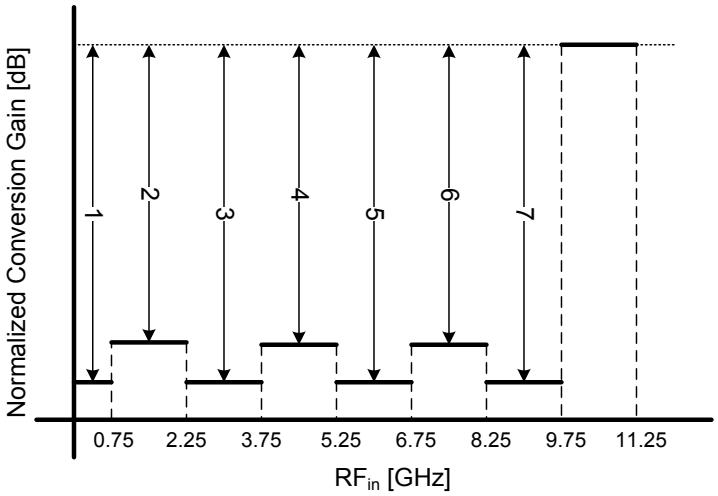
3: Filtering in 5.25GHz + third harmonic rejection of 3GHz mixer
1,2,4,5,6,7: Spurious mixer down-conversion ($M.f_{RF} - N.f_{LO}$)

(b)

Figure 3.16: Signal leakage in channel 6.



(a)



2: RF feed through in 12GHz mixer
4: 2.25GHz filtering + 5.25GHz filtering + 5^{th} harmonic rejection in 1.5GHz mixer
6: 2.25GHz filtering + 3^{rd} harmonic rejection in 1.5GHz mixer
1, 3, 5, 7 : Spurious mixer down-conversion: $M.f_{RF} - N.f_{LO}$

(b)

Figure 3.17: Signal leakage in channel 7.

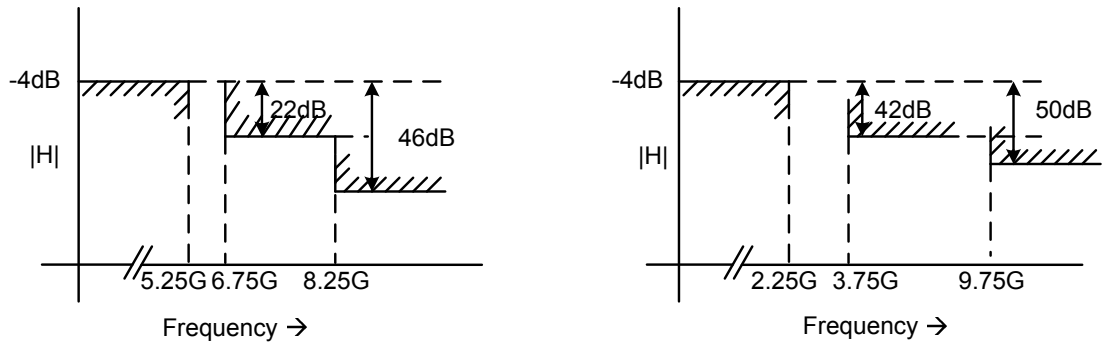


Figure 3.18: Filter requirements

3.6 Circuit Design

The critical blocks of the RF channelizer are low-noise transconductance amplifier (LNTA), multi-mode mixer, current buffer, harmonic rejection mixers (HRMs), filters, trans-Impedance amplifiers (TIA), and frequency dividers. In this thesis, description of multi-mode mixer [3], HRMs and filters [4] will be presented.

3.6.1 Multi-mode mixers

A circuit with an ability to switch between being transparent and a mixer, multi-mode mixer, can reduce the hardware in the channelizer. This enables the re-use of the filter and thus a large area savings. In the RF channelizer, multi-mode mixers are used in

1. The 12GHz mixer/ transparent block driving the 5.25GHz filter.

2. The 6GHz IQ mixer/ transparent block driving the 2.25GHz filter.

Fig. 3.19 shows the schematic of 12GHz multi-mode mixer. Based on the desired channel, the block can be operated either in the mixer mode or in transparent mode. In order to accomplish this, the LO signals are ac coupled to the gate of switches, and the dc-gate bias voltages are set by an on-chip bias generator (described in section 3.6.2). When the mixing

[3]Circuit design developed in collaboration with Yang Xu. Yang Xu made the 12GHz multi-mode mixer and Karthik Tripurari made the 6GHz I/Q multi-mode mixer.

[4]Filter design was done in collaboration with Branislav Jovanovic. The filter requirements and order were developed by Karthik Tripurari. Layout of the filter and electro-magnetic simulations were performed by Branislav Jovanovic.

mode is desired the LO input is enabled and when the transparent mode is desired, the LO input is disabled. The DC gate bias voltages of the switches are set such that the pair of switches connecting one terminal of the output is turned on while others are turned off.

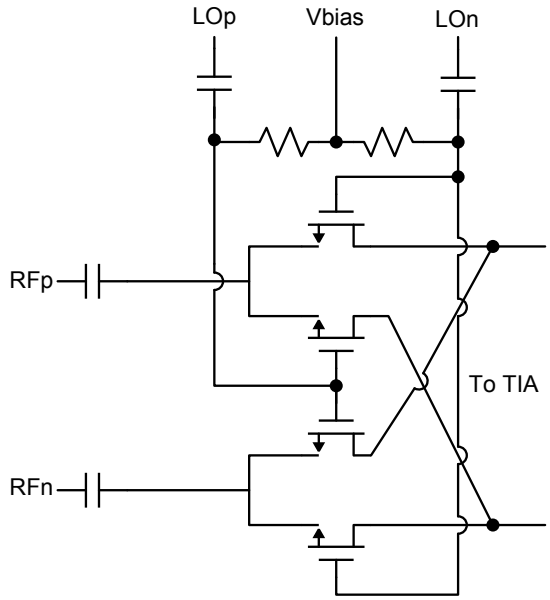


Figure 3.19: Schematic of multi-mode 12GHz mixer

The operating point of the source and drain nodes of these switches are designed to be approximately $0.5 \cdot V_{\mathrm{DD}}$. In order to maintain high on-conductance of the switches, the V_{GS} is preferable to be closer to V_{DD}. Having a low ON-resistance of the switch is important to maintain good linearity of the mixer. For this purpose, in the transparent mode of operation, the gate of ON-switches are set to 1.8V in transparent mode of operation.

In the mixing mode operation, the gate bias determines the level of overlap between different phases of LO. The value of the gate bias is made programmable in order to control the LO overlapping levels of the passive mixer across PVT variations. Nominally, it is set to 0.9V. The effective LO waveforms or the signals at the gate are shown in Fig. 3.20.

The body of the switches is connected to drain to make sure the Vgb will be not higher than VDD to avoid break down. All the switches are put into different deep-N-wells to separate the body from the substrate.

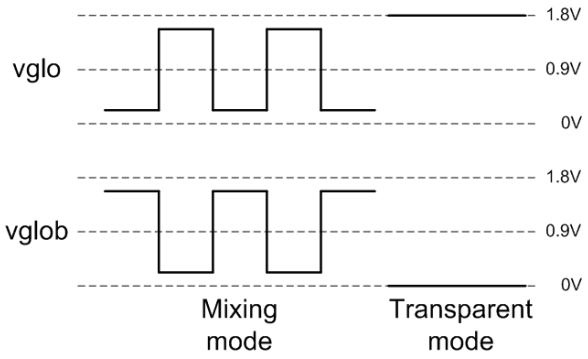


Figure 3.20: LO waveforms for the multi-mode mixer

Multi-Mode 6GHz IQ mixer The operation of the multi-mode-IQ-Mixer is similar to the operation of the multi-mode-12G-mixer in the first stage; the 6G IQ multi-mode mixer can operate either in the transparent mode or the mixer mode. The circuit diagram of the multi-mode-IQ-Mixer is shown in Fig. 3.21. In the transparent mode, the switches of the Q-path are turned off (connected to ground) and the switches in I-path are driven by a DC input (1.8V for the ON-switch and 0V for the OFF-switch). So the output of the mixer is equal to the input. When IQ mixing is required, the mixer is driven by a 6GHz 25% duty cycled IQ LO. The dc-bias voltage of the gate is set to 0.9V. In order to overcome PVT variations and the associated LO overlap variations, the gate operating point is made programmable.

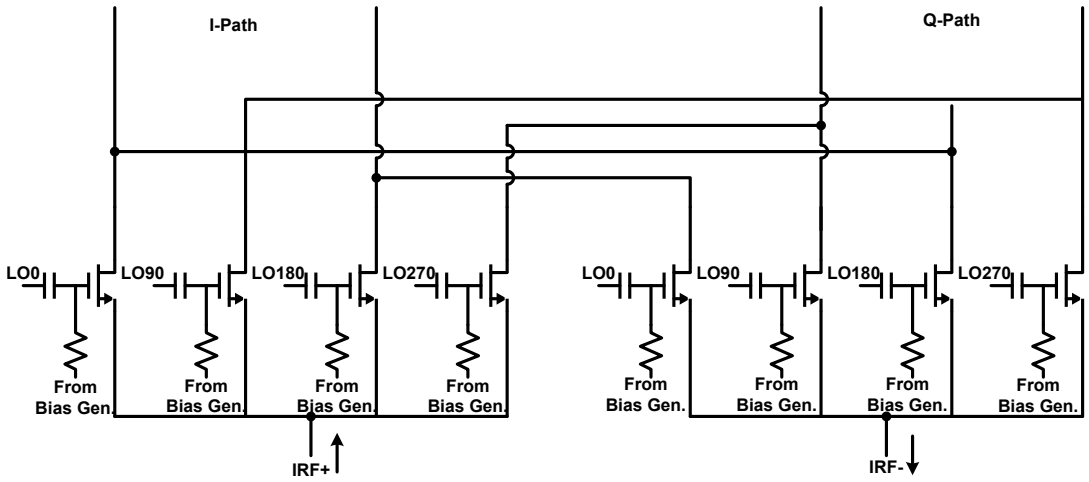


Figure 3.21: Schematic of the IQ mixer.

3.6.2 Gate-Biasing for multi-mode mixer

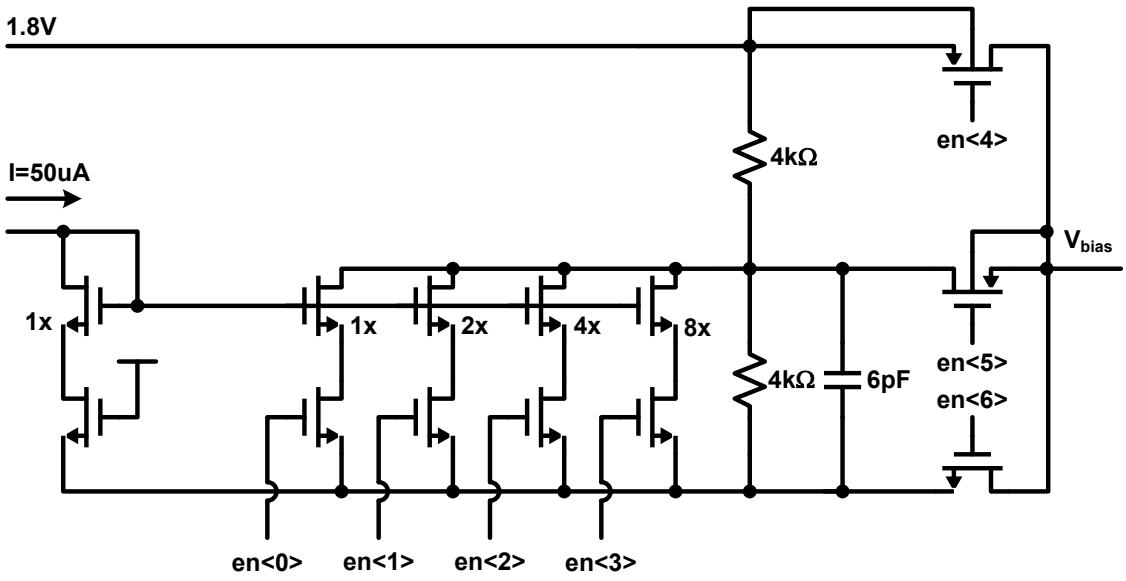


Figure 3.22: Schematic of the voltage bias generator. Vbias is used to bias the dc voltage of the mixer gate

The multi-mode mixer requires gate-biasing voltages of 0V (for turning off a switch), 1.8V (for fully turning on a switch in transparent mode) and some programmable values

between 0.6V to 0.9V (for operation in mixing mode). The voltage bias generator shown in Fig. 3.22.

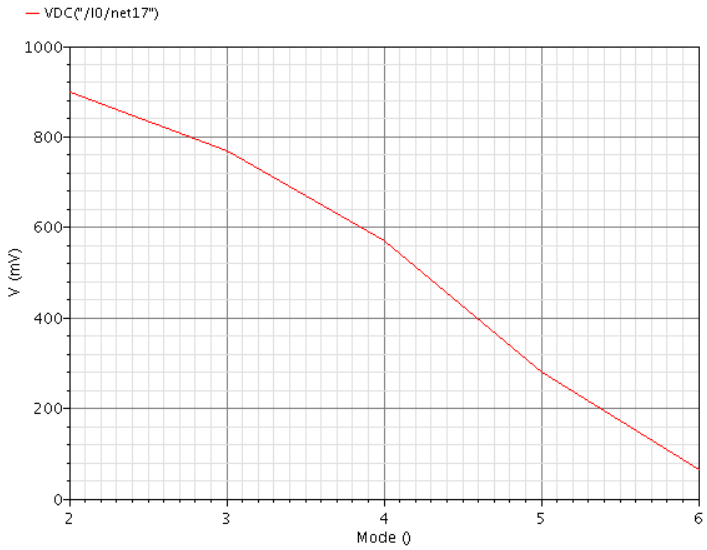


Figure 3.23: Gate bias voltage as a function of digital control

The value of Vbias can be controlled depending the setting of en<7:0>. For reliable operation of the circuit, 2.5V devices were used in this circuit block. All the logic levels were translated to 1.8V. Fig. 3.23 shows the variation of the output DC bias voltage when the controls for the bleeding current is varied.

The RF channelizer's ability to switch rapidly from one mode of operation to another is limited by the time taken by the voltage bias generator to settle. The worst case settling time scenario is when the bias generator switches from 1.8V to 0.9V. The settling time is a function of the values of resistors used in the resistor divider, the load cap and the storage cap. Fig. 3.24 shows the bias settling for an estimated load cap of 500fF. Faster settling is achievable by reducing the resistance value used for voltage division at the cost

of increasing power consumption.

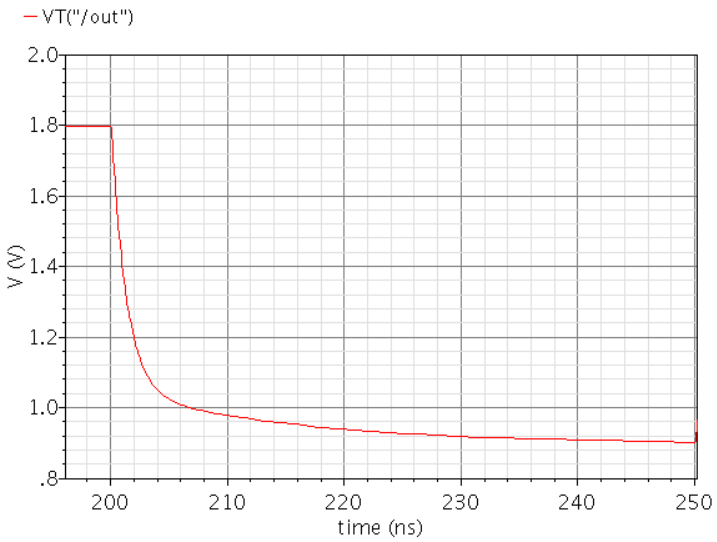


Figure 3.24: Gate bias starting from 1.8V and settling to 0.9V when mode is switched from transparent to mixing mode.

3.6.3 Filter design

The low-pass filters in the RF channelizer enable

- Splitting of the frequency channels.
- Attenuation of out-of-band blockers and relax the harmonic rejection requirements of the following mixers.
- Attenuation of the out-of-band blockers and relax the image rejection requirements of the following mixers.

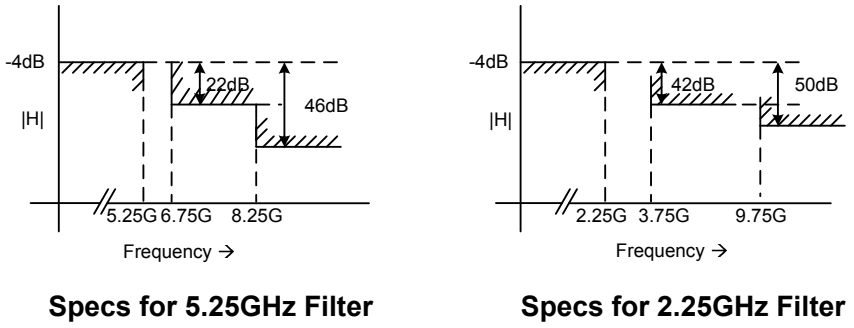


Figure 3.25: Filter specifications.

Fig. 3.25 shows the requirement of the filters. A fifth order elliptical filter was chosen in order to achieve the sharp roll-off requirements. Considering the frequencies of operation of the filter, a passive LC-ladder filter architecture was selected.

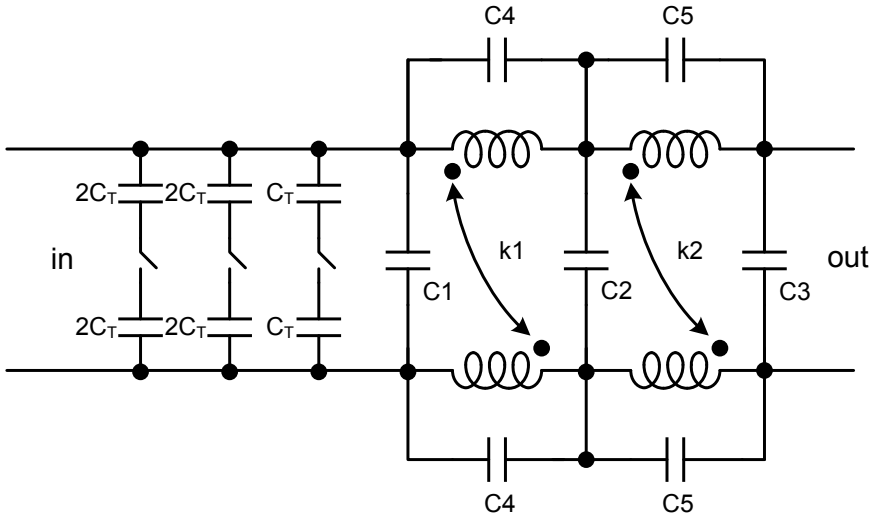


Figure 3.26: Filter schematic

The low pass filter is made programmable using switched capacitors in parallel with C1. There are 3-bits of control for tuning the filter bandwidth.

Table 3.2: Components values used in the 5.25GHz and 2.25GHz LC-filters.

	5.25GHz Filter	2.25GHz Filter
C1	480fF	2.1pF
C2	1.8pF	5.2pF
C3	320fF	1.7pF
C4	1.7pF	2.3pF
C5	1pF	1pF
CT	260fF	340fF
L1	260pH	640pH
L2	290pH	650pH
k	0.5	0.6

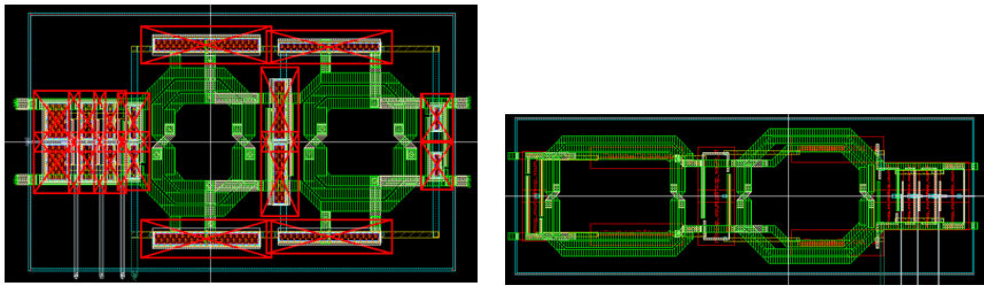
The schematic of the fifth order LC filter is shown in Fig. 3.26. The component values used of the 2.25GHz filter and the 5.25GHz filter is shown in Table 3.2.

The transformers have quality factor of 21 at 5GHz for 2.25GHz filter and 15 for 5.25GHz filter. Coupling coefficients are between -0.5 and -0.6.

3.6.3.1 Filter simulation results

The layouts of the passive 5.25GHz filter and 2.25GHz filter are shown in Fig. 3.27(a) and Fig. 3.27(b) respectively. They occupy an area of 372um x 225um and 615um x 210um, respectively. Fig. 3.28 shows the simulated transfer function of the filter and their specifications. The blue curve is the transfer function from the electro-magnetic simulation of the case where only the filter was simulated isolated from any other circuits. The red curve is the transfer function of the filter surrounded by components, clock lines, digital busses etc, as in the final version of the gds file that was submitted for tape-out.

The 2.25GHz filter meets all the specs out-of-band attenuation of more than 50dB. Both



(a) (b)

Figure 3.27: (a) Layout of 5.25GHz low-pass filter. (b) Layout of 2.25GHz low-pass filter

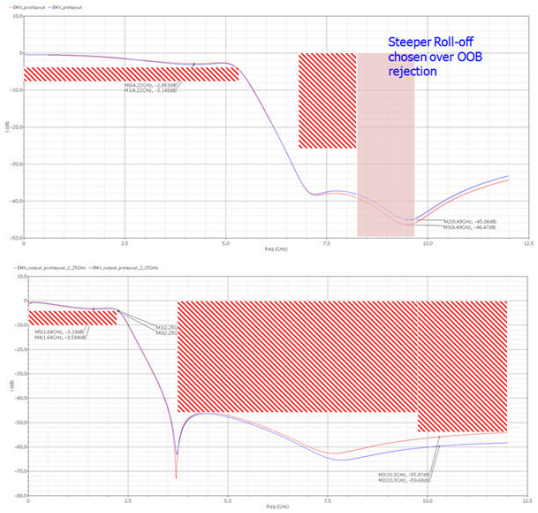


Figure 3.28: AC response 5.25GHz and 2.25GHz low-pass filters vs. specs

curves, pre-layout and post-layout one have very similar response in band, and out-of-band discrepancy is larger due to the longer routing.

The 5.25GHz filter meets the specs except around 8.25GHz-9.75GHz. This results in a reduced suppression of out-of-band blockers. However, this can be compensated by having a better third harmonic rejection of the 3GHz harmonic rejection mixer.

3.6.4 Harmonic rejection mixer

The block diagram of a harmonic rejection mixer (HRM) used in the RF channelizer is shown in Fig. 3.29. A classical HRM architecture demonstrated in [17] is chosen for its ability to extend to high frequencies of operation.

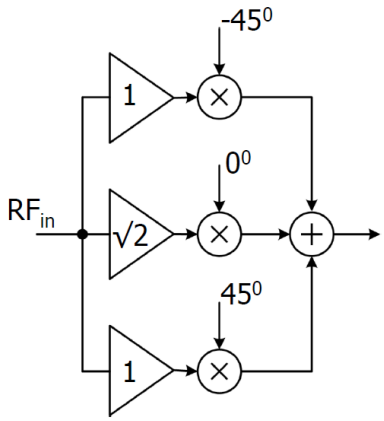


Figure 3.29: Block diagram of the harmonic rejection mixer used in the RF channelizer.

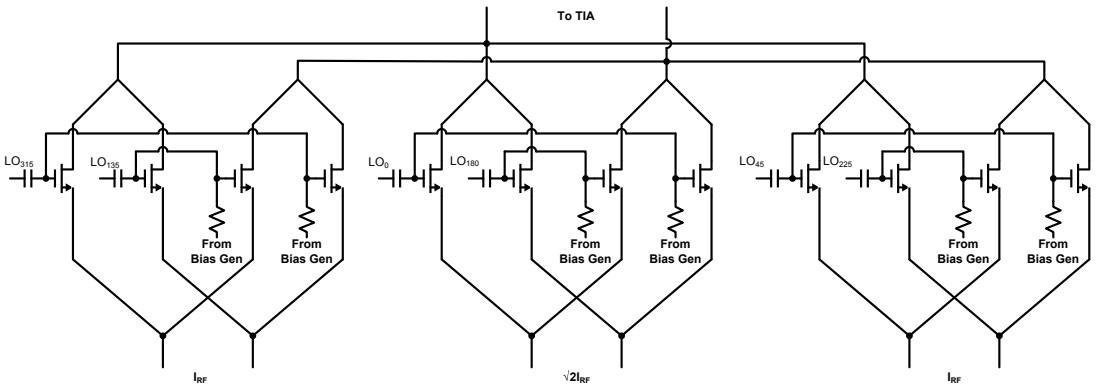
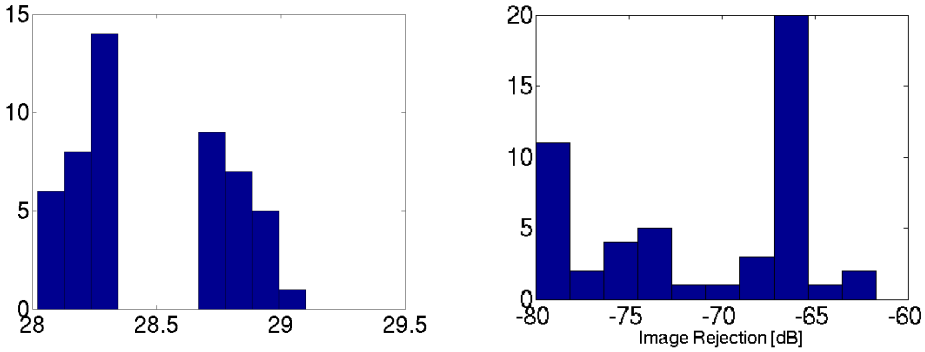


Figure 3.30: Schematic capture of the harmonic rejection mixer.

3.6.4.1 3-GHz I/Q harmonic rejection mixer

Fig. 3.30 shows the circuit implementation of the HRM. The multiple LO phase required by the mixer is derived using frequency divide-by-4 circuit. The ratio-ed currents are produced by the preceding current buffer.

Monte-Carlo simulation was conducted to estimate the harmonic rejection and the image rejection of the mixer. The desired harmonic rejection is 15dB. Simulation results, shown in Fig. 3.31(a), demonstrate 13dB better harmonic rejection.



(a) Third harmonic rejection. (b) Image rejection.

Figure 3.31: Monte-Carlo simulation results (50 runs) for the 3-GHz harmonic rejection mixer.

The simulated image rejection is shown in Fig. 3.31(b). Simulations demonstrate image rejection of better than 60dB. Further improvement in image rejection can be achieved by using off-chip calibration described in [20].

Table 3.3: Monte-Carlo simulation results for the 3-GHz harmonic rejection mixer.

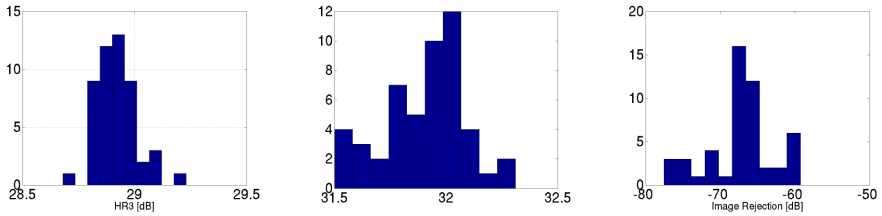
	TT, 27C, 1.2V	SS, 100C, 1.1V	FF, 0C, 1.2V
HR3 [dB]	28	28	28
IR [dB]	71±6	61±5	64±3

Table 3.4: Monte-Carlo simulation results summary for the 1.5GHz harmonic rejection mixer.

	TT, 1.2V, 27C	SS, 1.1V, 70C	FF, 1.2V, 0C
HR3 [dB]	28	32	29
HR5 [dB]	32	37	32
IR [dB]	67 ± 5	53 ± 5	67 ± 5

3.6.4.2 1.5GHz I/Q harmonic rejection mixer

Based on the system design, a third and fifth harmonic rejection of greater than 15dB is required. Simulation results (shown in Fig. 3.32(a),3.32(b)) confirm that the required performance is achieved. Simulations demonstrate image rejection (Fig. 3.32(c)) of better than 60dB. Further improvement in image rejection can be achieved by using off-chip calibration described in [20].



(a) Third harmonic rejection. (b) Fifth harmonic rejection. (c) Image rejection.

Figure 3.32: Monte-Carlo simulation results (based on 50 runs) for the 1.5GHz harmonic rejection mixer.

3.7 RF channelizer system simulation results

Fig. 3.33 shows the layout of the integrated chip. The chip was designed in a standard 65nm TSMC CMOS process. The chip occupies an area of 2mmx1mm including the bondpads

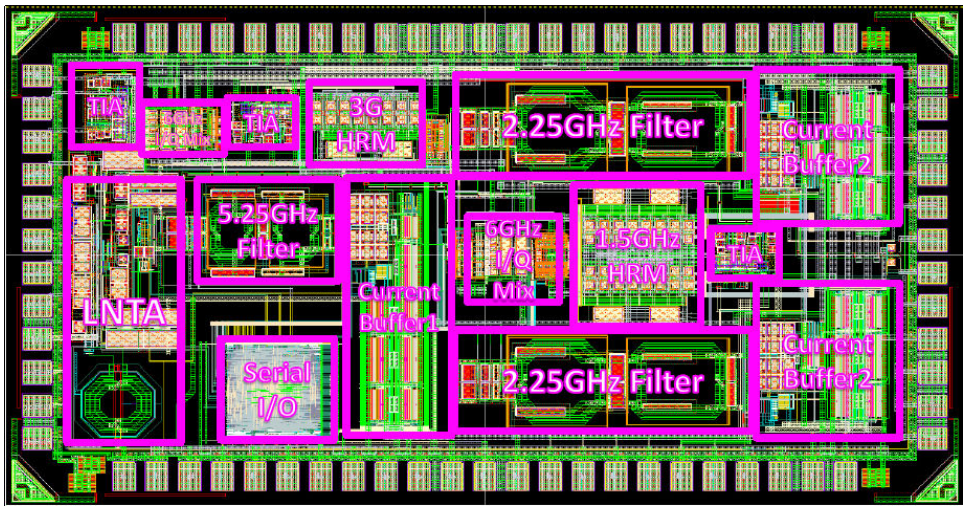


Figure 3.33: Layout of the integrated chip.

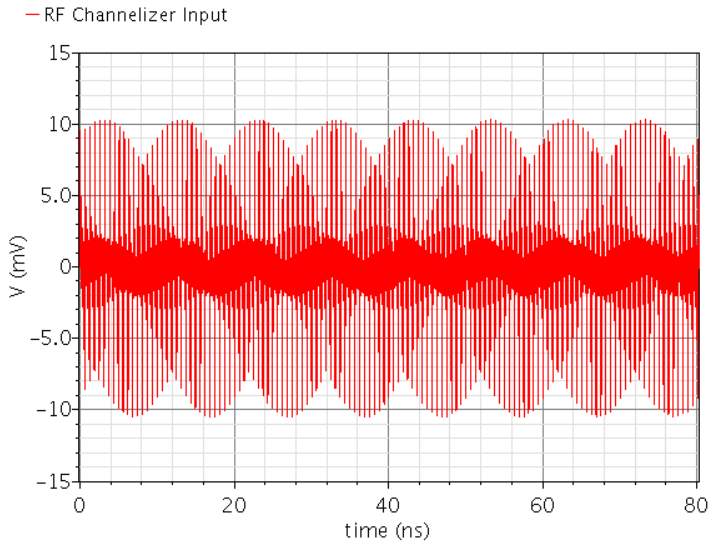
and ESD circuits.

This section presents some of the key simulation results to demonstrate the features of the RF channelizer. The RF channelizer was designed in 65nm TSMC technology. After layout, the chip occupies an area of 2mmx1mm.

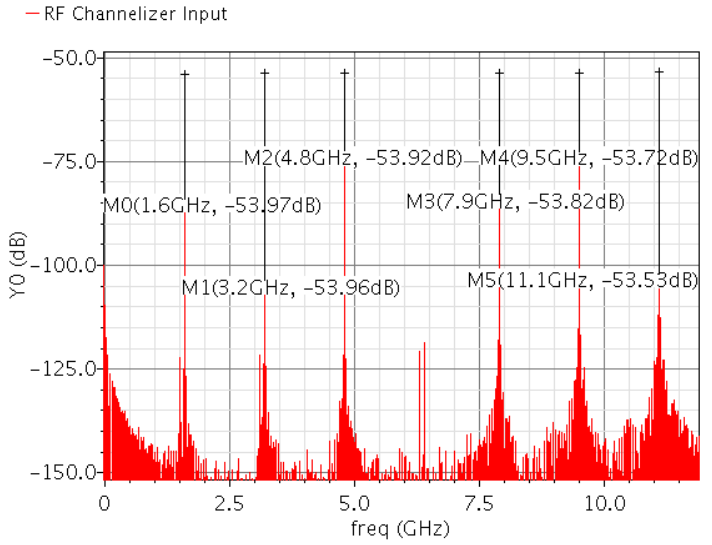
3.7.1 Fast switching

One of the important features of the RF channelizer is its ability to switch rapidly between receiving one channel to another. In order to demonstrate this, a signal shown in Fig. 3.34 is input to the RF channelizer. The input signal contains sinusoids of frequency 1.6GHz (Channel 1), 3.2GHz (Channel 2), 4.8GHz (Channel 3), 7.9GHz (Channel 5), 9.5GHz (Channel 6), and 11.1GHz (Channel 7).

As described earlier, the RF channelizer is capable of producing three concurrent outputs. For the fast switching feature simulation, the focus is on the concurrent output 1



(a)



(b)

Figure 3.34: Input signal to the RF channelizer used for testing its fast switching abilities.

which down-converts channel 1, 3, 5, and 7.

Fig. 3.35 shows the output of the concurrent channel 1. The output is observed to switch

between 100MHz, 300MHz, 400MHz, and 600MHz, corresponding to signals in channel 1, 3, 5, and 7 respectively. The channel switching time can be seen to be less than 10ns.

The simulation was conducted using schematic netlist under nominal operating conditions (27C, typical corner, 1.2V supply).

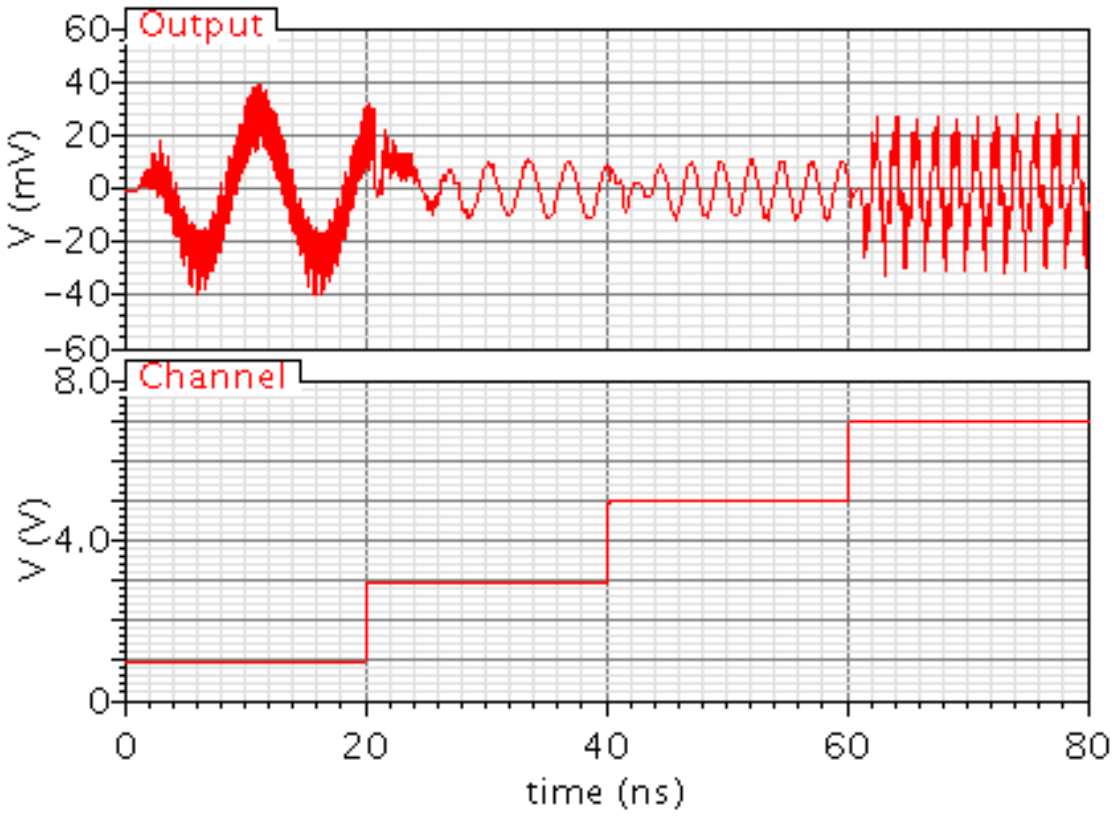
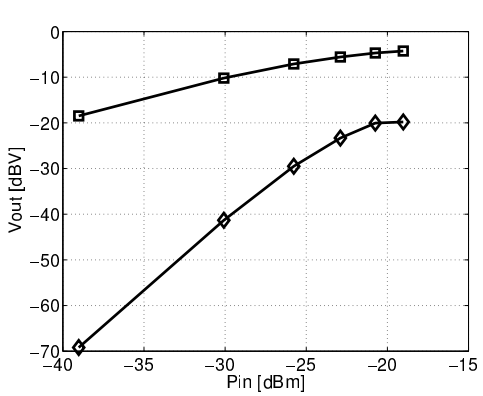


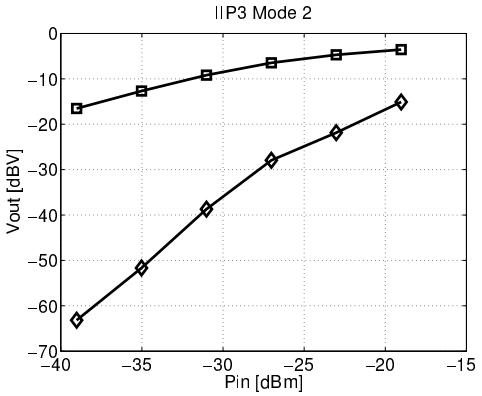
Figure 3.35: Simulation demonstrating fast switching feature of the CLASIC RF channelizer. The output switches between channels 1, 3, 5, and 7.

3.7.2 Linearity, Noise Figure and Spurious Free Dynamic Range

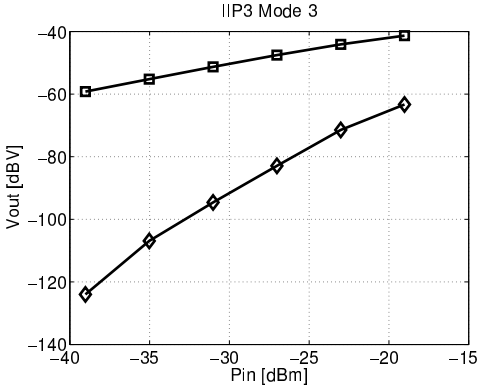
The simulation was conducted with all the circuits (Signal path, LO path, biasing circuits) realized using transistors. Model bond-wire inductance and bond-pad capacitance were also included along with ESD protection diodes.



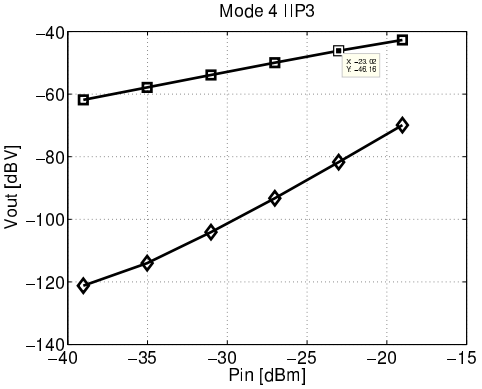
(a) IIP3 = -16dBm



(b) IIP3 = -13dBm

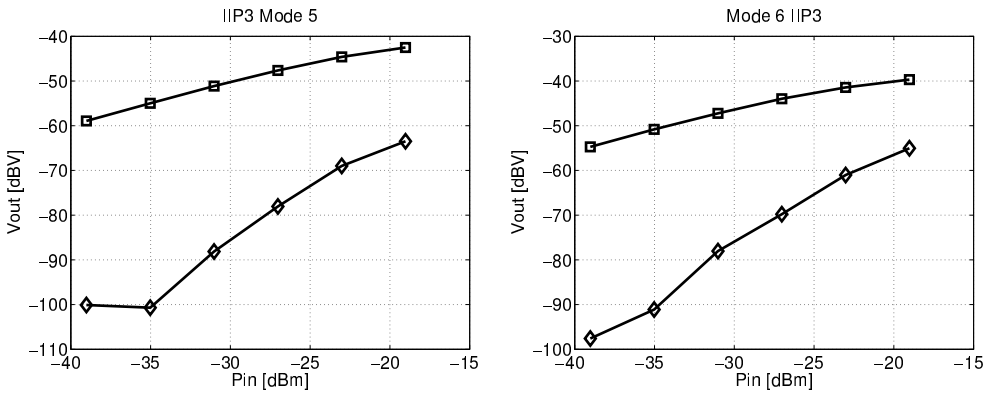


(c) IIP3 = -9dBm



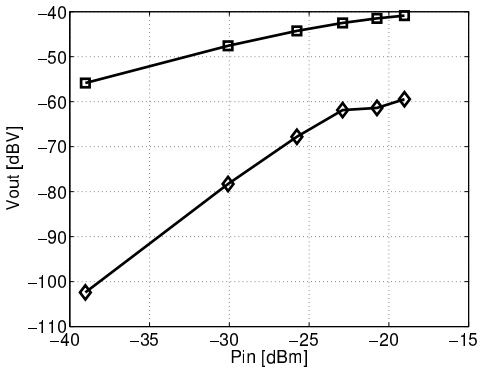
(d) IIP3 = -6dBm

The gain was set to be the maximum. The same gain settings were used for both Linearity and Noise Figure simulations in order to compute the dynamic range fairly. The control bits were setup using veriloga modules. Nominal operating conditions (typical corner, 27C



(e) IIP3 = -13dBm

(f) IIP3 = -15dBm



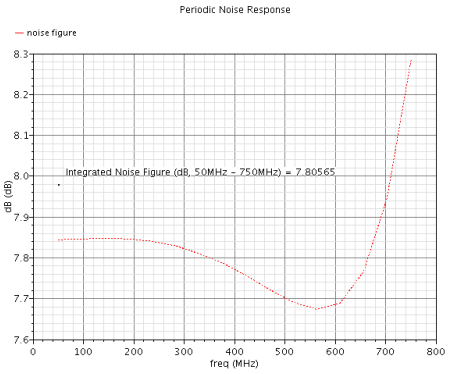
(g) IIP3 = -14dBm

Figure 3.36: A summary of the RF channelizer's IIP3 simulation results.

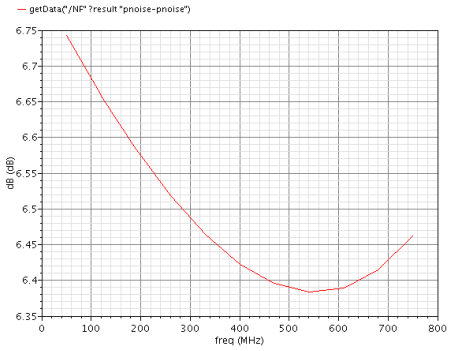
and 1.2V) were used for the simulations.

PSS + Pnoise analysis was used to simulate the Noise Figure. The Noise Figure simulations were conducted with the circuits (Signal path, LO path, biasing circuits) realized using transistors. The control bits were setup externally using veriloga modules. Blocks which were inactive (turned-off), ESD circuits and bond-wires were removed in order to enable the convergence of the PSS simulator. Nominal operating conditions were used for the simulations.

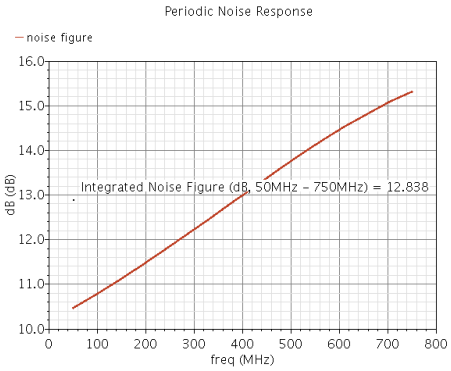
A summary of the IIP3 and Noise Figure simulation results are presented in Table. 3.5.



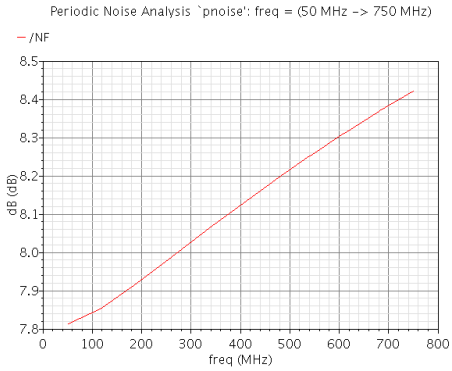
(a)



(b)



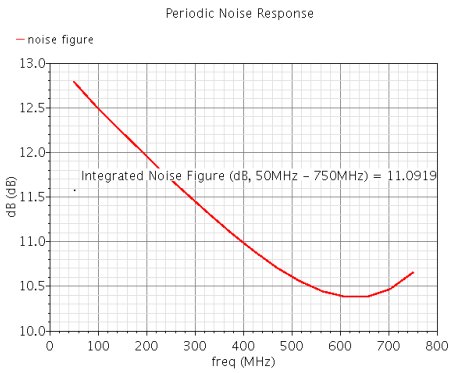
(c)



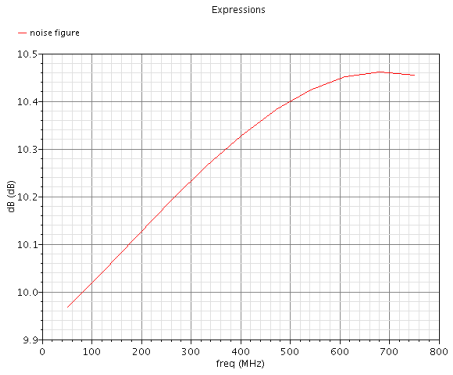
(d)

SFDR is calculated using the formula

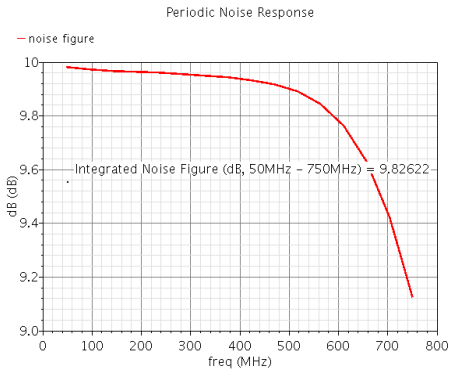
$$SFDR = \frac{2}{3} \times (IIP3 - P_{\text{Noise}}) \tag{3.10}$$



(e)



(f)



(g)

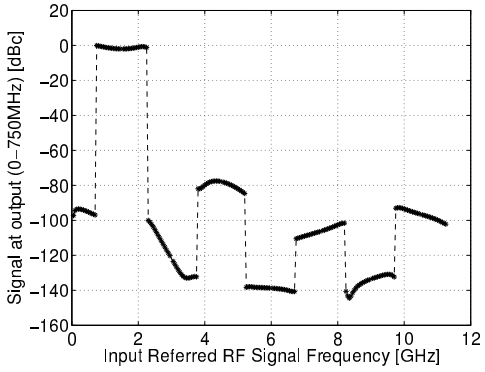
Figure 3.37: A summary of the RF channelizer's Noise Figure simulation results.

Table 3.5: Simulated IIP3, Noise Figure and SFDR of the RF channelizer in various configurations.

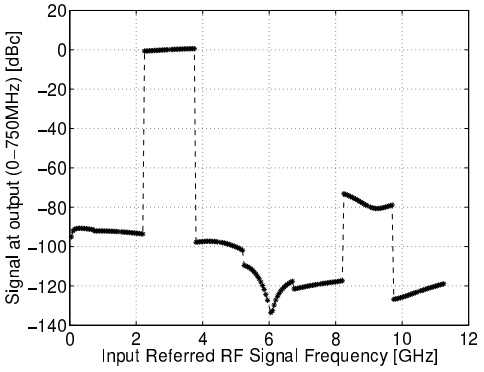
Channel	IIP3 [dBm]	Noise Figure [dB]	Noise Floor [dBm] [5]	Dynamic Range [dB]
1	-13	7.8	-106	62
2	-16	6.7	-107	61
3	-9	13	-101	61
4	-6	8.1	-106	67
5	-13	11	-103	60
6	-15	10.2	-104	60
7	-14	9.8	-104	60

3.7.3 Signal leakage

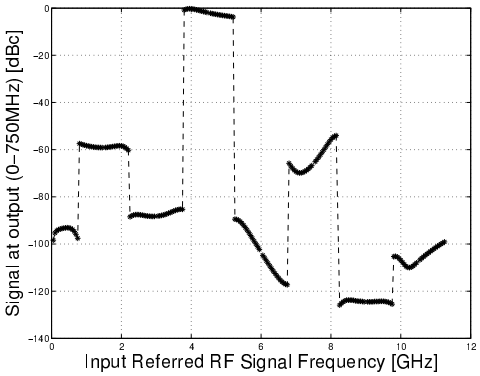
Fig. 3.38 plots the results of signal leakage simulations. The plots show the output power as a function of input frequency. Every plot is expected to have one band with a strong output which is the desired channel. Outputs of signals at other input frequencies are normalized with respect to the desired channel.



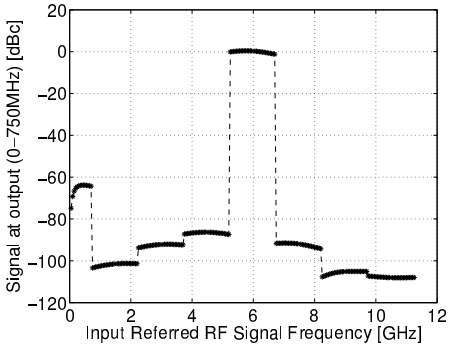
(a) Channel 1



(b) Channel 2

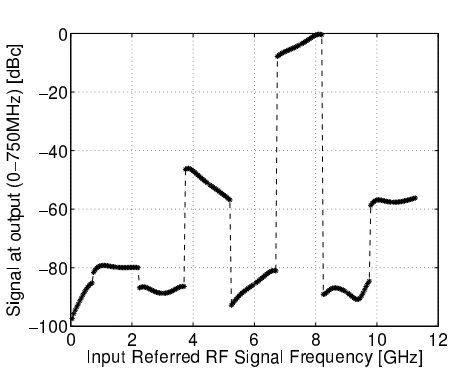


(c) Channel 3

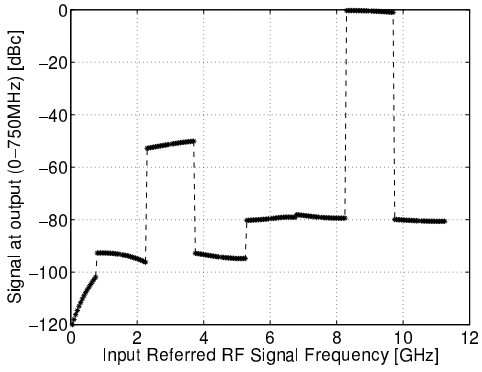


(d) Channel 4

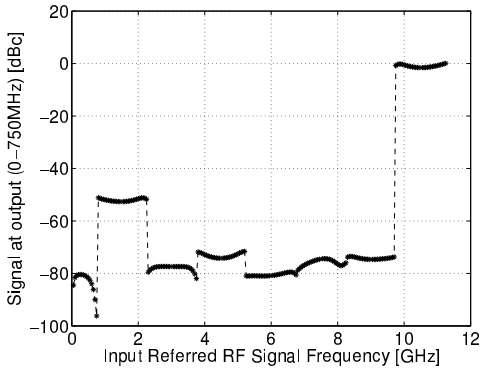
PSS + PXF analysis was performed in order to simulate the signal leakage. The simulations were conducted with all the circuits (Signal path, LO path, biasing circuits) realized using transistors. Blocks which were inactive (turned-off) were removed in order to en-



(e) Channel 5



(f) Channel 6



(g) Channel 7

Figure 3.38: A summary of signal leakage in various modes of operation of the CLASIC RF channelizer.

able the convergence of the PSS simulator. The control bits were setup externally using veriloga-a modules. Nominal operating conditions (27C, typical corner, 1.2V supply) were used for the simulations.

3.7.4 Dynamic Range of the RF channelizer

The dynamic range of the RF channelizer is limited by the in-band IIP3 and the Noise Floor of the RF channelizer. However, when the leaked signal is greater than the noise

floor, the SNR is then limited by the signal leakage. Hence, the dynamic range is defined as the lower value of the SFDR and channel leakage. Fig. 3.39 plots the dynamic range in every channel. The dynamic range varies between 45dB and 62dB depending on the mode

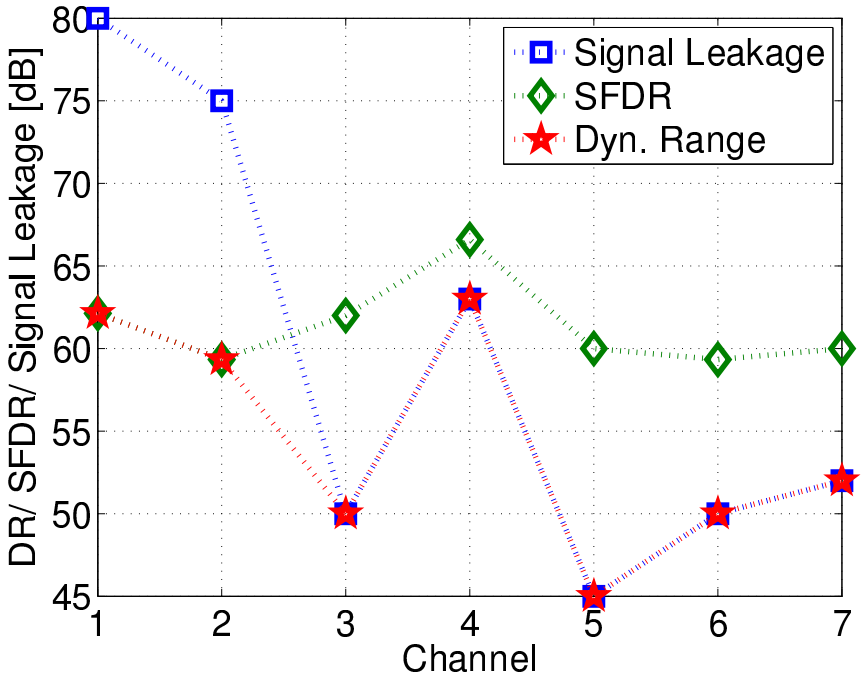


Figure 3.39: The dynamic range of the RF channelizer

of operation of the RF channelizer. In order to compare with other channelizers, ADCs, an average dynamic range was used. The average dynamic range across various modes of operation is 54.5dB.

The lowest dynamic range in channel 5 is limited by the signal leakage from channel 3. The RF feed-through in the 12GHz mixer limits the dynamic range to 45dB. In order to improve the dynamic range, the RF feed-through in the 12GHz mixer needs to be lowered. RF feed-through in mixers puts a fundamental limitation on the achievable dynamic range

with this architecture.

3.7.5 Power consumption

Table. 3.6 shows the breakdown of power consumed in various blocks in various modes of operation. The peak power consumption occurs in mode 5 when all the blocks of the chip are turned on. The average current consumption across all the modes of operation is 450mA from 1.2V supply.

Table 3.6: Power breakdown for the RF channelizer when configured for different channels

Channel	Low-Noise Amplifier [mA]	Current Buffers [mA]	12G LO Buffers [mA]	TIA [mA]	Bias Circuits [mA]	LO Path [mA]	Total [mA]
1	62	290	48	45	2	38	485
2	62	165	48	45	2	38	360
3	62	415	48	45	2	60	632
4	62	0	48	45	2	38	195
5	62	415	48	45	2	64	636
6	62	165	48	45	2	42	364
7	62	290	48	45	2	42	489

3.8 Comparison of our RF channelizer to the state of the art

In this section we review the simulated performance of the RF channelizer developed in this project with other channelizer approaches available in the literature. A comparison between different techniques is made based on various assumptions which are also presented in this section.

3.8.1 Definitions

Key terms used in this comparison are defined as follows:

- T_{hop}: Time taken by the receiver to hop from down-converting one channel to another.
- T_{analysis}: Time taken by the base-band signal processor to analyze a given signal with 1MHz RBW. For the purpose of calculations, it is chosen as $1\mu s$.
- T_{total}: Total time taken by the spectrum analyzer (including T_{hop} and T_{analysis}) to analyze the complete spectrum with a 1MHz RBW.
- E: Total energy consumed in analyzing the spectrum (including the baseband signal processing) with a resolution bandwidth of 1MHz.
- BW/E: Total bandwidth analyzed for every unit total energy consumed.
- Spurious signal leakage: ratio of conversion gains of an undesired channel to a desired channel.

- SFDR is equal to $\frac{2}{3} \times (IIP3 - P_{\text{noise}})$.
- Dynamic range is equal to the lower quantity among spurious channel leakage and SFDR.

3.8.2 Calculations

Mitola envisioned a cognitive radio receiver to be an RF ADC [10]. The direct digitization of the input signal allows to analyze the signal in real-time. An example implementation of such an ADC with 10GHz bandwidth is demonstrated in [24]. At an operating speed of 20GSPS, the ADC is reported to have a dynamic range of 29dB, while consuming 10W. The lower bound on the energy required to analyze the input bandwidth with a 1MHz resolution bandwidth—and thus an analysis time $T_{\text{analysis}} \geq 1\mu s$—can now be computed as follows.

$$\begin{aligned} T_{\text{total}} &= T_{\text{analysis}} = 1\mu s \\ E &= T_{\text{total}} \cdot P_{\text{ADC}} = 10\mu J \end{aligned} \tag{3.11}$$

A more recent example of an ADC with a higher dynamic range is demonstrated in [25]. The ADC digitizes a signal bandwidth of 2.7GHz with a dynamic range of 55dB consuming 500mW of power [6].

$$\begin{aligned} T_{\text{total}} &= T_{\text{analysis}} = 1\mu s \\ E &= T_{\text{total}} \cdot P_{\text{ADC}} = 550nJ \end{aligned} \tag{3.12}$$

[6] An additional 50mW of power is assumed for PLL to generate 5.4GHz clock with 100fs jitter [26].

Wang demonstrates an RF Receiver capable of analyzing input signal with a bandwidth 3.1GHz to 10.6GHz in [22]. They employ 7 parallel channels each catering to a bandwidth of 1100MHz. However, since the output bandwidth of each of these receivers is 800MHz, two sessions of analysis is required; the PLL is required to switch once. Considering the PLL has a bandwidth of 5MHz, T_{hop} is at least 200ns. The output of the receiver is assumed to be digitized using an ADC and rest of the processing to be done digitally. The power consumption for the ADC was estimated based on [25] to be $P_{ADC} = 150mW$.

$$\begin{aligned} T_{\text{total}} &= 2 \cdot T_{\text{analysis}} + 1 \cdot T_{\text{hop}} = 2.2\mu s \\ E &= 2 \cdot T_{\text{analysis}} \cdot P_{\text{ADC}} + T_{\text{total}} \cdot P_{\text{Channelizer}} = 1.07\mu J \end{aligned} \tag{3.13}$$

Goel et. al, demonstrates a scanning spectrum analyzer, based on a two-step mixing approach in [21]. The output bandwidth of the receiver is 22MHz, which is limited by the bandpass filter used to suppress the blockers at image frequencies. The spectrum analyzer scans a spectrum from DC-6GHz. The receiver hops 272 times before scanning the entire spectrum. With a designed PLL BW of 100kHz, T_{hop} is $10\mu s$ and T_{total} is 2,993 μs.

$$\begin{aligned} T_{\text{total}} &= 273 \cdot T_{\text{analysis}} + 272 \cdot T_{\text{hop}} = 2993\mu s \\ E &= T_{\text{total}} \cdot P_{\text{Channelizer}} = 2031\mu J \end{aligned} \tag{3.14}$$

This work demonstrates a fast-switching partially concurrent RF channelizer. The RF channelizer splits the input bandwidth of 10.5GHz into 7 channels. The channelizer provides three concurrent channels: channel 4, channel 2 or 6, channel 1 or 3 or 5 or 7. The channelizer can hop from one channel to another in 10ns. P_{ADC} is assumed to be 280mW

based on [25]. Further, a PLL power of 50mW is assumed to be on all the time while calculating the energy of the spectrum analysis.

$$\begin{aligned} T_{\text{total}} &= 4 \cdot T_{\text{analysis}} + 3 \cdot T_{\text{hop}} = 4.03\mu s \\ E &= 7 \cdot T_{\text{analysis}} + \frac{T_{\text{total}}}{7} \sum_{k=1}^{7} \left(P_{\text{channel,k}} + P_{\text{PLL}} \right) = 6.27\mu J \end{aligned} \tag{3.15}$$

$P_{\text{channel,k}}$ is the power consumed by the RF channelizer in receiving channel k.

3.8.3 Figure of Merit

A Figure of Merit (FoM) is proposed in this section in order to be able to compare the various approaches described above. The parameters of interest for a spectrum analyzer are its dynamic range and the bandwidth analyzed per unit of Energy consumed.

The bandwidth analyzed is directly proportional to the energy consumed by the spectrum analyzer. More bandwidth can be analyzed by operating multiple analyzers in parallel (at the cost of power consumption) or by operating the a single analyzer for a longer time. In both cases the energy consumed is the same ($E = P \cdot T$). Thus we can conclude that the energy consumption and bandwidth analyzed have a direct trade-off described by the following equation:

$$E \propto BW. \tag{3.16}$$

FoM for active filters used in [27] indicates that the dynamic range is directly proportional to the power consumption of the active filters. By extending this idea to a RF frontend, dynamic range of a spectrum analyzer is directly proportional to its power con-

sumption, and thus the energy consumption of the spectrum analyzer. Thus we can conclude that energy consumption and dynamic range of the spectrum analyzer have a trade-off described by the following equation:

$$E \propto DR. \tag{3.17}$$

Based on (3.16) and (3.17), the FoM can be derived as

$$FoM_{\text{Spectrum,Analysis}} = \frac{BW \cdot DR}{E} \tag{3.18}$$

3.8.4 Comparison

Table 3.7 summarizes the key performance metrics of channelizers published in the literature and Fig. 3.40 gives a graphical representation. The comparison methodology is presented in section 3.8

Fig. 3.40 plots the RF channelizer in comparison with various ADCs published in the last 15 years. The RF channelizer achieves an average dynamic range of 54dB while analyzing a signal bandwidth of 10.5GHz.

Fig. 3.41 plots the analysis bandwidth per unit energy against dynamic range for various RF channelizers. This work is second only to Wu's ADC [25] in terms of energy efficiency. However, we offer four times the bandwidth of [25] and it has to be considered that the power consumption increases quicker than a linear scaling with bandwidth for circuits with multi-GHz bandwidths that operate closer to the fT limit of the technology. Wang's concurrent receiver is presented in [22], Goel's spectrum analyzer is presented in [21] and Poulton's ADC is presented in [24].

Table 3.7: A comparison of our 0.75-11.25GHz RF channelizer based spectrum analyzer with the existing state-of-the-art channelizers based spectrum analyzer.

	[Wang]	[Goel]	[Poulton]	[Wu]	This work
Feature	Concurrent	Scanning	Direct digitization	Direct digitization	Concurrent Fast-switching
Input BW [GHz]	3.1 -10.6	0-6	0-10	0-2.7	0.75-11.25
Power [mW]	342	678	10,050	550	590[7]
T_{hop} [μs]	0.2	10	-	-	0.01
T_{Total} [μs]	2.2	2,993	1	1	4.03
E [μJ]	1.07[8]	2,031	10.05	0.55	6.27[9]
BW/E [GHz/μJ]	6.99	0.003	1	4.9	1.73
IIP3 [dBm] (50)	-5/-9	10	N.A	N.A	-5/-10
NF [dB] (50)	2.5/14	N.A	N.A	N.A	7/12
Sensitivity [dBm] (1MHz BW, 9dB SNR)	-101/-91	-82 [10]	N.A	N.A	-98/-93
Signal leakage [dB]	-36	N.A	N.A	N.A	80/45
Dynamic range [dB]	36	61	29	55	62/45

N.A: Not Available

3.9 Conclusion

In this chapter, we propose an RF front-end architecture based on IDC. The RF front-end splits the input spectrum into channels of narrower bandwidth. The use of iterative down-conversion enables the incorporation of LO synthesis inside the signal path which enables rapid channel hopping.

An example 0.75GHz-11.25GHz RF channelizer implementation is used to demonstrate the features of rapid channel switching and concurrency. The 0.75GHz-11.25GHz RF channelizer splits the input 10.5GHz bandwidth into seven channels, each of 1.5GHz bandwidth with an average dynamic range of 54dB consuming an average power of 540mW.

Our channelizer analyzes 10.5GHz bandwidth with a dynamic range of 54dB, a spec

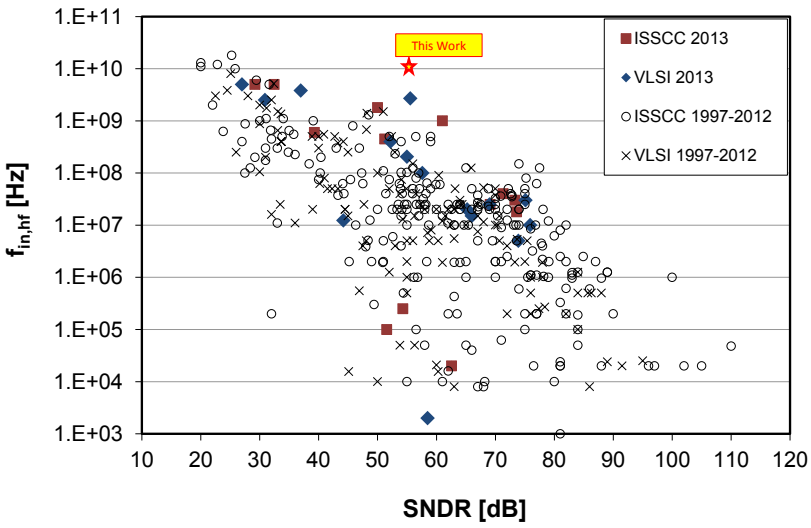


Figure 3.40: A chart plotting our work against the state-of-art ADCs.

that is unheard of in ADC literature. In comparison with state-of-art channelizers, our channelizer can analyze the highest bandwidth (10.5GHz) with an energy efficiency of 1.73GHz/uJ and 54dB of dynamic range.

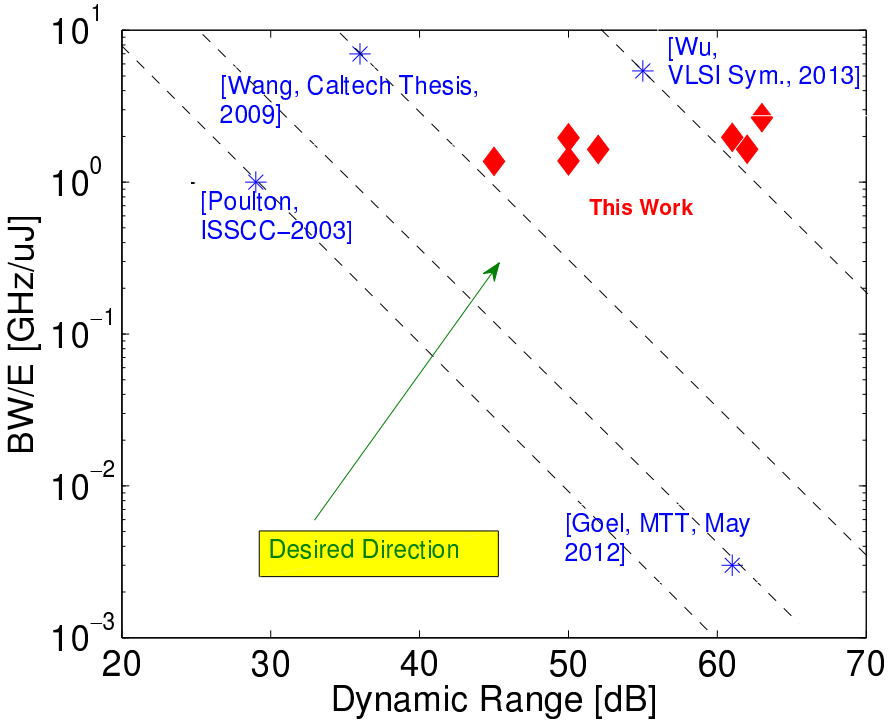


Figure 3.41: A chart plotting the analysis bandwidth per energy against the dynamic range for various RF channelizers.

Chapter 4

A 0.5GHz-1.5GHz Order Scalable Harmonic Rejection Mixer

4.1 Abstract

In this chapter, a harmonic rejection mixer architecture capable of operating for a wide range of LO frequencies is demonstrated. The mixer can be configured to suppress any particular harmonic of the LO or multiple harmonics simultaneously. The level of suppression of each harmonic is controlled by a set of independent gain and phase tuning parameters. Feasibility of extension of this concept to higher order harmonics is also demonstrated. [1]

A proof-of-principle prototype has been designed and fabricated in a 45nm SOI tech-

[1]This research was conducted in collaboration with Teng Yang. The idea and the architecture was developed by Karthik Tripurari, circuit design was done by Teng Yang, chip testing was conducted by both.

nology. Experimental results demonstrate an operation range of 0.5GHz to 1.5GHz for the LO frequency while offering harmonic rejection better than 55dB for the 3^{rd} harmonic and 58dB for the 5^{th} harmonic across LO frequencies. The mixer consumes 17mW of power from a 1V power supply while occupying an area of $0.352mm^2$.

4.2 Introduction

Harmonic rejection mixers (HRMs) have become a necessity in wide-band communication systems. Significant progress has been achieved in understanding the challenges since the classical HRM was demonstrated in [17; 28; 29].

A limitation of the classical HRM architecture is that the harmonic rejection performance is typically limited to about 30-40dB due to gain and phase mismatches [28; 30]. Two-stage mixing based HRMs have been demonstrated [31] to have superior harmonic rejection. However, there is not much published work using this technique for suppressing higher order harmonics.

The classical HRM architecture described in [17] rejects the 3^{rd} and 5^{th} harmonics leaving the higher order harmonics un-rejected. In order to suppress the higher harmonics, more LO phases and parallel paths are added. An adaptation of this idea has been demonstrated in [32] for TV-Tuner applications. However, this technique has not been demonstrated for LO's above 300MHz.

Superior harmonic rejection using calibration has been demonstrated in [30]. However, with an increase in the number of parallel paths, the number of elements to be tuned scales

up. The task of calibrating is harder as the exact source of mismatch becomes more unclear with the increasing number of LO phases and parallel paths.

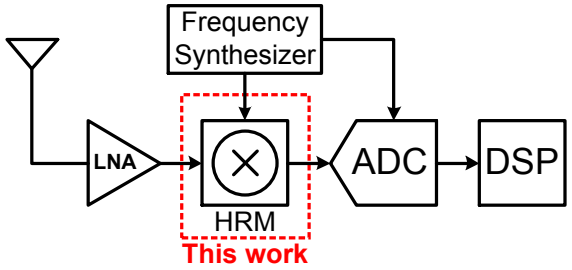


Figure 4.1: A cognitive radio receiver consisting of a broadband LNA, a harmonic rejection mixer, ADC-DSP for signal processing and a frequency synthesizer to produce various LOs and clocks.

Fig. 4.1 shows the block diagram of a cognitive radio receiver. The receiver consists of a broadband LNA, a HRM, a frequency synthesizer to generate wide range of frequencies, an ADC and a DSP. In order to enable simultaneous reception of multiple wireless signals (for instance Wifi, 3G, GPS, etc), the frequency synthesizer would be required to produce multiple LOs simultaneously. Unlike in TV-Tuner applications where the entire band is usually occupied, the spectrum in Cognitive Radios might not be full of strong blockers. For instance, there could be a blocker present around the n^{th} harmonic of LO while the signals around 3^{rd} harmonic are harmless.

In this chapter we demonstrate a HRM architecture that exploits the availability of multiple LOs and enables suppressing of any particular harmonic. Calibration for rejection of each harmonic of LO can be done independent of other. The rest of the paper is organized as follows: Section 4.3 describes the operation of the proposed harmonic rejection mixer architecture and makes some theoretical comparisons with the classical HRM in terms of achievable harmonic rejection. Section 4.4 provides details of the circuit implementation

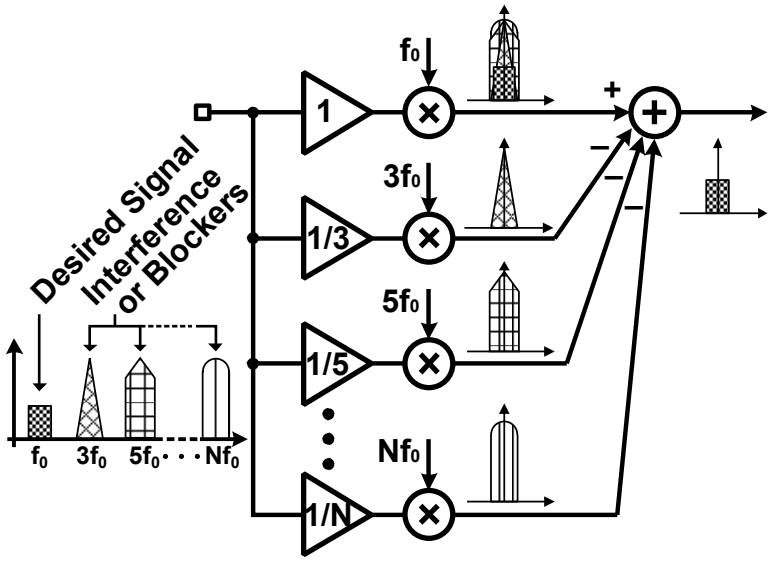


Figure 4.2: Block diagram of the reconfigurable HRM architecture

is provided. Section 4.5 gives the measurement results and the conclusions are presented in section 6.6.

4.3 The proposed harmonic rejection mixer

A model of the proposed harmonic rejection mixer with qualitative illustration of interference cancelling mechanism is shown in Fig. 4.2. The system consists of one main signal path which operates as a conventional mixer and multiple auxiliary paths for interference cancellation. Due to hard switching caused by the LO, interference around harmonic frequencies of LO are also down-converted to IF band and fall in same band as the desired signal. To cancel a particular down-converted interference, an associated auxiliary path is enabled to generate the opposite of the interference. The outputs of the two paths are added to cancel the interferer at the IF output.

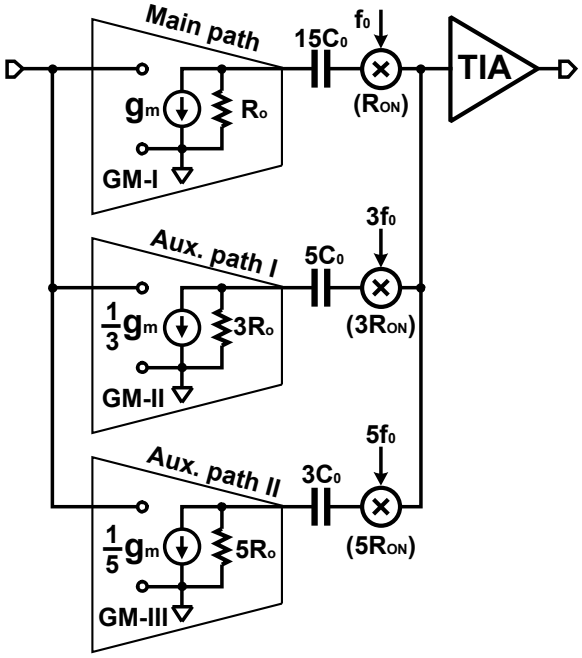


Figure 4.3: Design considerations enabling good gain matching for a perfect harmonic rejection.

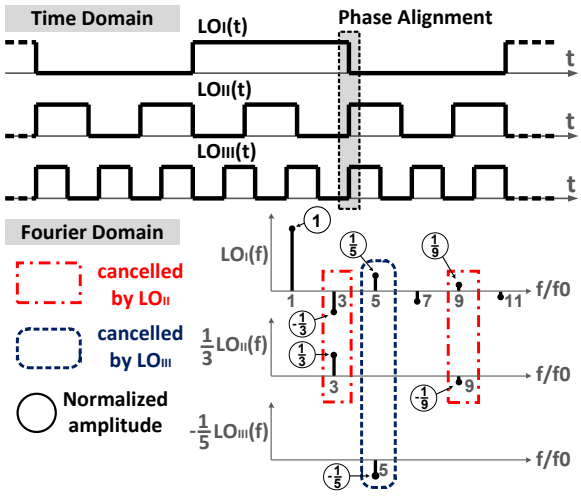


Figure 4.4: Appropriate LO phase alignment for a perfect harmonic rejection.

Depending on the blocker profile, the relevant auxiliary paths can be enabled to enhance the system's resilience to out-of-band interference. The other auxiliary paths can be disabled to reduce power consumption.

We have designed a prototype HRM with one main path and two auxiliary paths for 3^{rd} and 5^{th} harmonic rejection. The suppression of the 3^{rd} harmonic's products depends only on first auxiliary path, while the suppression of the 5^{th} harmonic's products depends on the second auxiliary path. Tuning of HR3 and HR5 can be done independently of each other.

In classical HRMs, the approximation of $\sqrt{2}$ leads to intrinsic gain errors, degrading the harmonic rejection ratio. Our proposed HRM requires a ratio of $1 : \frac{1}{3} : \frac{1}{5}$ which avoids approximation of irrational numbers.

4.3.1 Gain matching and LO Phase Alignment

Effective transconductance (G_{mX}) of a transconductor is given by

$$G_{mX} = \frac{R_{oX}}{R_{oX} + R_{ONX} - j\frac{1}{\omega C_X} + R_{TIA}} \cdot g_{mX} \tag{4.1}$$

where g_{mX} is the transconductance and R_{oX} is the output resistance of GM-X, C_X and R_{ONX} are AC-coupling capacitance and ON-resistance of the switches in signal path X and R_{TIA} is the input impedance of TIA. The appropriate transconductances, impedances and admittances for a perfect cancellation are shown in Fig. 4.3.

In addition to the requirements on the accuracy of signal amplitudes in various paths, there is also a requirement on the phases of LOs. The LO phase alignment for ideal rejec-

tion of the harmonics is shown in Fig. 4.4.

For a certain phase misalignment (θ) and gain mismatch (Δ) the theoretically achievable harmonic rejection is given by (4.2), where HR_n is the harmonic rejection (in dB) obtainable for n^{th} harmonic.

$$HR_n = 20\log\left(\frac{n}{\sqrt{\Delta^2 + n^2\theta^2}}\right) \tag{4.2}$$

Theoretically achievable harmonic rejection for various gain and phase mismatches are plotted in Fig. 4.5. It can be seen that our HRM has a higher achievable harmonic rejection when compared to classical HRM.

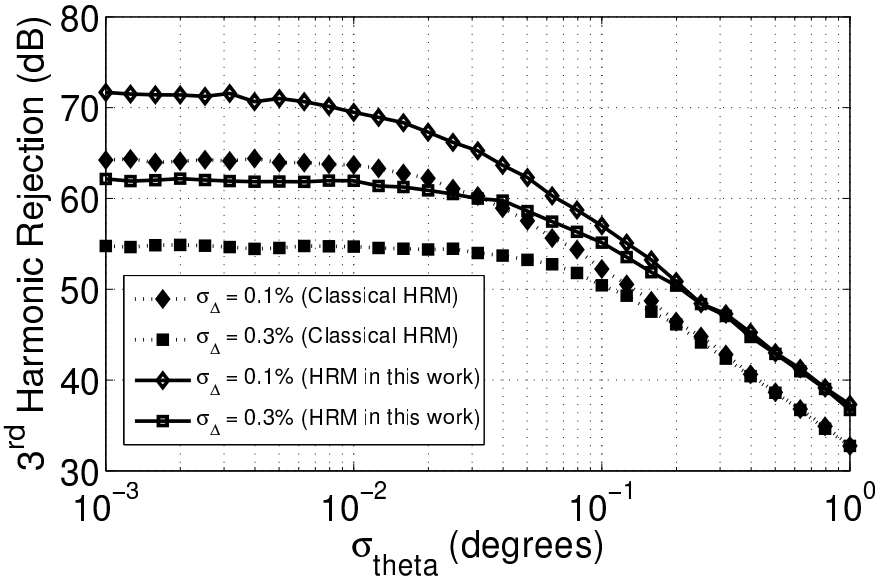


Figure 4.5: Theoretically achievable 3rd harmonic rejection in the presence of gain and phase mismatches for the proposed HRM architecture and the classical HRM.

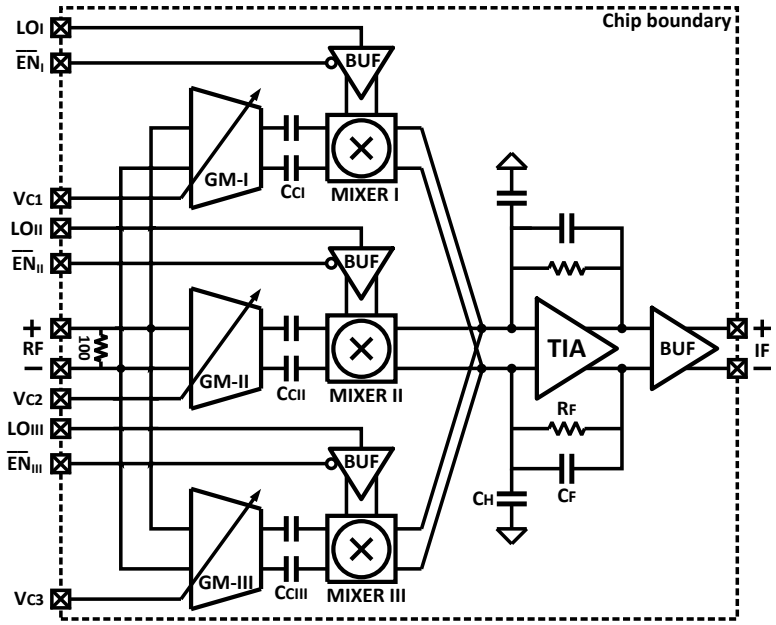


Figure 4.6: Block diagram of the harmonic rejection mixer.

4.4 Circuit implementation

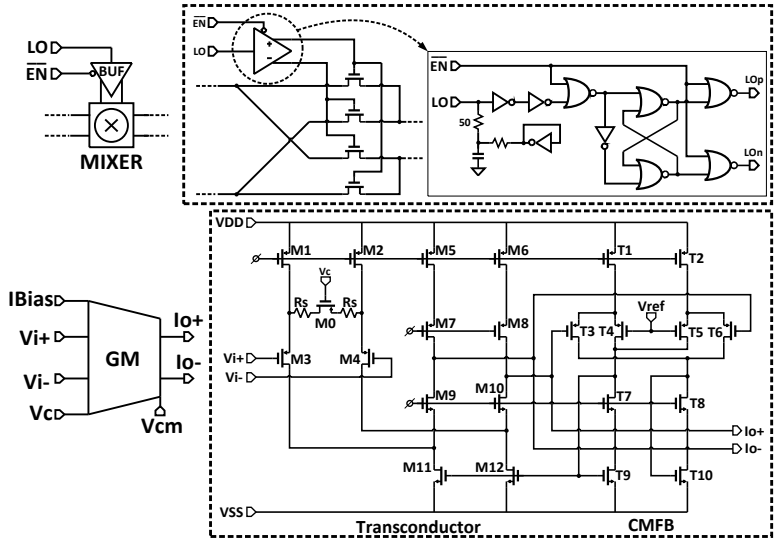


Figure 4.7: Circuit implementation of the tunable transconductor and passive mixer.

The block diagram of the implemented HRM is shown in Fig. 4.6. Input voltage signal drives three transconductors (GM-I, GM-II and GM-III). The currents are coupled to passive mixers through scaled AC-coupling capacitors. The harmonic components from main path are cancelled upon the addition of the down-converted signals. The TIA provides low input impedance for the passive mixers and converts signal current back to voltage.

In order to overcome any mismatch in transconductances, tuning is implemented in the transconductors. For enabling appropriate alignment of the LO phases (as shown in Fig. 4.4) a voltage controlled delay cell is needed. However, in this proof-of-concept prototype the voltage controlled delay has been realized off-chip.

4.4.1 Tunable Transconductors

The implementations of the transconductors are shown in Fig. 4.7. In order to achieve a perfect harmonic cancellation, $g_{mI} : g_{mII} : g_{mIII}$ needs to be designed with ratio of $1 : \frac{1}{3} : \frac{1}{5}$.

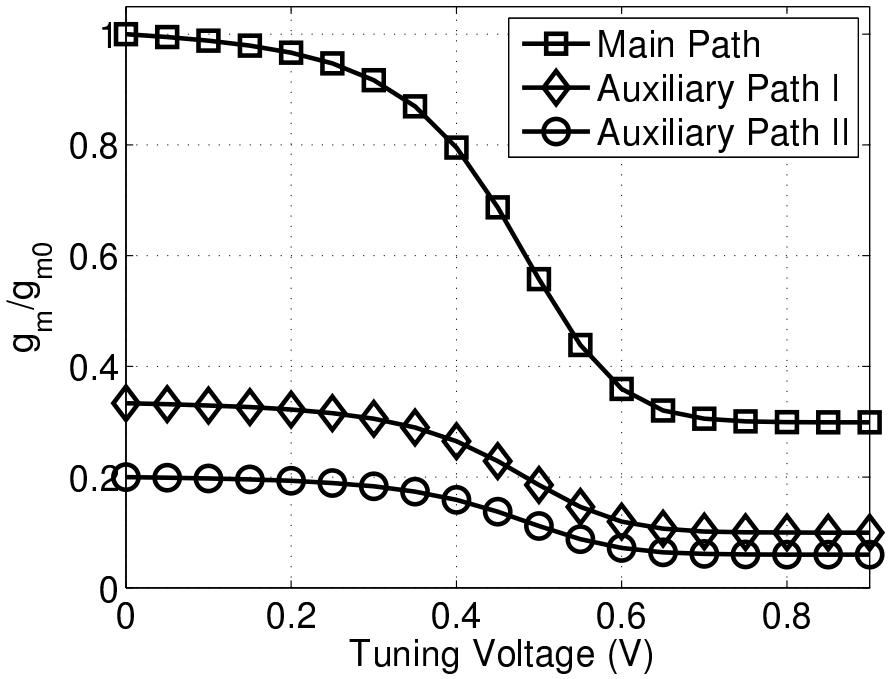


Figure 4.8: Simulated transconductance vs tuning voltage for the transconductors. The transconductances are normalized to 3mS (g_{m0}).

High output impedance is also required for transconductors so folded-cascode structure is implemented. The output impedances of three transconductors are scaled with ratio of $1:3:5$ and the values were designed as $7.2\text{k}\Omega, 21.6\text{k}\Omega, 36\text{k}\Omega$. In circuit implementation, scaling of g_m and R_{out} can be achieved by scaling the number of transistor fingers in the ratio ($F_I : F_{II} : F_{III} = 15 : 5 : 3$).

The tuning is realized by using voltage controlled degeneration resistors. The transconductance vs control voltage (V_c) is shown in Fig. 4.8.

4.4.2 Passive mixers

The three transconductors connect to three passive current-commutating mixers which are driven by LO buffers, as shown in Fig. 4.7. The mixers are AC-coupled to the transconductors with scaled capacitors and the lower cut-off frequency is 200MHz.

NMOS switches are used for passive mixers. $R_{ON,switch}$ are designed relatively smaller compared to $R_{out,GM}$ to avoid current loss. Also $R_{ON,switch}$ of three mixers are scaled with ratio of 1 : 3 : 5 to avoid mismatches.

In the LO buffer, non-overlapping clocks are generated by using cross-coupled NOR gates to avoid the case of partial turn-on of both the switches. NOR gate at outputs of clock buffer is used to disable the LO, thereby turning-off the particular signal paths when necessary.

4.4.3 Trans-impedance amplifier and output buffer

The topology of TIA is based on OTA with shunt-shunt feedback which reduce the input and output impedance. Parallel capacitors are added at input of TIA for decreasing high frequency signal swing. The output buffer is designed for 50Ω matching by using source follower structure.

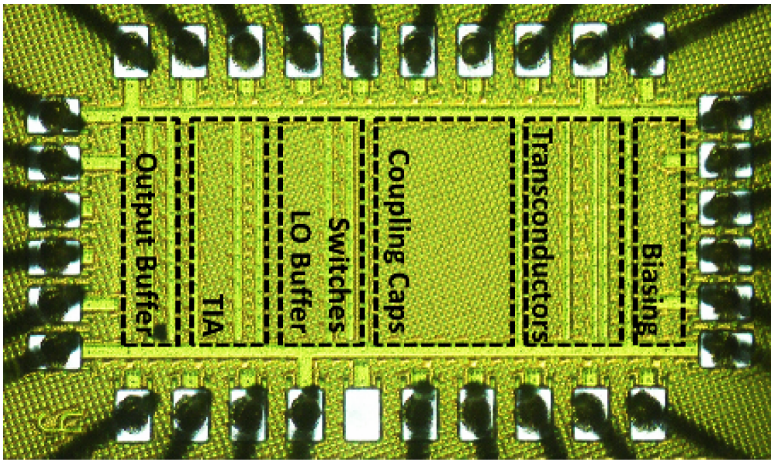


Figure 4.9: Die photo of the proof-of-concept harmonic rejection mixer chip.

4.5 Measurement results

The die-photo of the chip prototype is shown in Fig. 4.9. The chip was fabricated in 45nm SOI Technology. The active area of the HRM is $0.352mm^2$ ($800\mu m \times 440\mu m$).

At the time of paper submission, the transconductance and LO phase calibrations were done manually. The transconductance was controlled using an external voltage. Agilent E8257D signal generators were used to drive the LO ports of the mixer. The phase of the LO was controlled using the phase shifter inside the signal generators. The measurements results presented here are intended for proof of concept. Also, the harmonic rejection measurements were conducted for one harmonic at a time in order to demonstrate the ability to suppress a particular blocker without having to turn-on all the harmonic rejection paths.

Fig. 4.10 shows the measured harmonic rejection and the corresponding conversion gain at various LO frequencies. The harmonic rejection ratios (HRRs) were measured to be better than 55dB for 3^{rd} harmonic and above 58dB for 5^{th} harmonic for LO frequencies

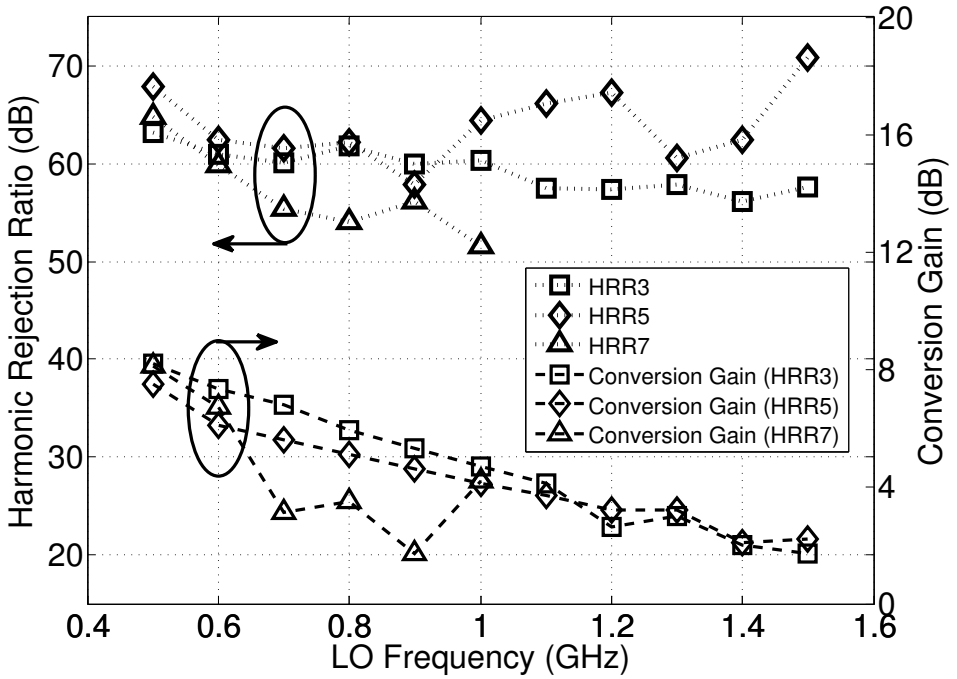


Figure 4.10: Measured 3rd, 5th and 7th harmonic rejection and the corresponding conversion gain of the mixer for various LO frequencies.

up to 1.5GHz.

In order to demonstrate the ease of extension to higher order harmonics, seventh harmonic rejection was also measured. Gm designed for cancelling the 5th harmonic was tuned to produce lesser transconductance. The measured seventh harmonic is also shown in Fig. 4.10.

A comparison of 3rd harmonic rejection with other existing HRMs is presented in Fig. 4.11. It can be seen that the proposed harmonic rejection mixer provides good rejection for a wide range of LO frequencies starting from 0.5GHz to 1.5GHz.

The mixer was measured to have a Noise Figure of 35dB, IIP3 of -3dBm and IIP2 of -2dBm while operating with a conversion gain of 8dB for an LO frequency of 800MHz.

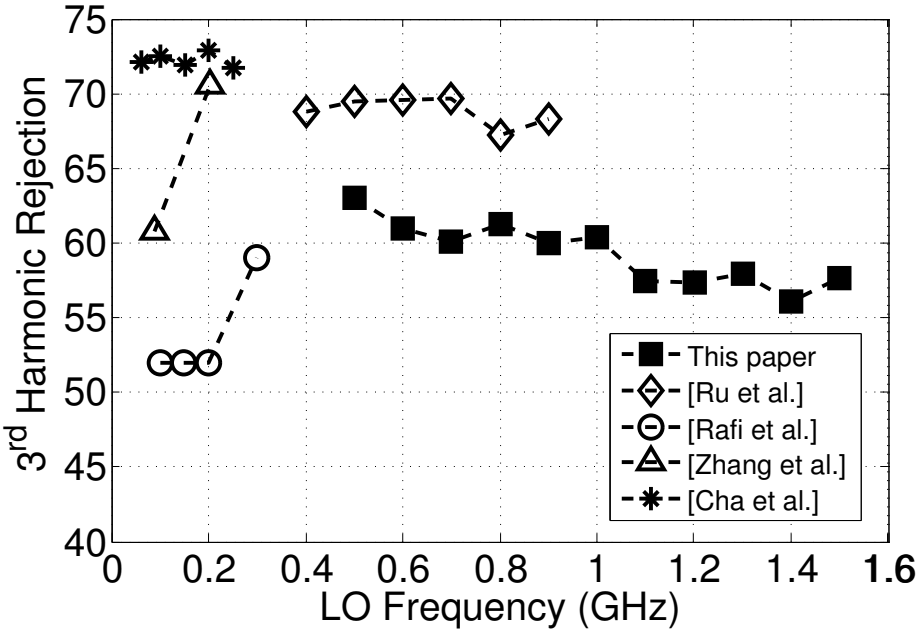


Figure 4.11: A comparison for the 3rd harmonic rejection at various LO frequencies with the state-of-the-art HRMs.

4.6 Conclusions

A 1.5GHz harmonic rejection mixer using auxiliary path cancellation technique for cognitive radio application has been demonstrated in this paper. This work exploits the availability of multiple LOs in a cognitive radio transceivers. It can be configured to suppress any particular harmonic of LO in addition to the ability of simultaneously suppressing multiple LO harmonics. The architecture could be easily extended to suppressing higher harmonics by adding additional parallel paths.

The proposed architecture has been prototyped in 45nm SOI technology to demonstrate 3rd and 5th harmonic suppression. The HRM is demonstrated to operate up to an LO of 1.5GHz providing >55dB of 3rd harmonic rejection and >58dB 5th harmonic rejection. In

comparison with existing state of art, we have demonstrated a harmonic rejection mixer that operates at a higher frequency. Further, the feasibility of extending the concept to a higher harmonic rejection has also been demonstrated using 7^{th} harmonic rejection measurements.

Chapter 5

Effect of Power Supply Scaling of CMOS Technology on PLL's Jitter

5.1 Abstract

Feature size of the transistors in CMOS technology is scaled down to enhance the f_T of the transistors. The supply voltage is also scaled down simultaneously to ensure reliable operation of the transistors. Digital circuits benifit from this scaling. The scaling of dynamic range-power trade-off of mixed signal circuits is limited by parameters such as jitter of the clock source. We propose a theory to describe the scaling of a PLL's jitter as a function of the power supply.

This chapter presents a theory for scaling of various sources of noise in a PLL. Based on the scaling of noise of individual blocks, a theory is proposed for the jitter of the PLL.

5.2 Introduction

The success of CMOS has been achieved by feature size scaling based on the rules proposed by [33]. As the gate oxide thickness is scaled down to keep the progress of transistor performance, the supply voltage, V_{DD}, needs to be scaled accordingly to prevent gate oxide breakdown. Lower supply voltages also reduce operating (dynamic) power in digital circuits. The integration of analog and digital circuits on a single chip is a key requirement to reduce the cost of a SoC, particularly in high-volume, low-profit-margin applications. Keeping a single power supply can reduce the number of flavors of transistors and the associated set of masks. It is thus believed that using the same power supply voltage for analog and mixed signal will reduce the cost of integration.

The performance of a mixed signal circuit is often a function of the jitter of a clock source. For instance, the ENOB of high resolution or high speed ADCs is limited by the jitter of the clock [34]. It is thus important to understand the effects of power supply scaling on the jitter of a PLL.

In this chapter, we derive a theoretical model to predict the scaling of noise of each critical block of the PLL. The theoretical model is verified using simulations. Based on these models, a projection is made on the scaling of jitter in PLLs with power supply.

Rest of the chapter is organized as follows: section 5.3 briefly reviews the noise sources in a PLL. Section 5.4 discusses the scaling of in-band phase noise of the PLL. Section 5.5 describes the phase noise of an oscillator and its scaling with power supply. Section 5.6 presents a mathematical derivation for the scaling of jitter with the power supply.

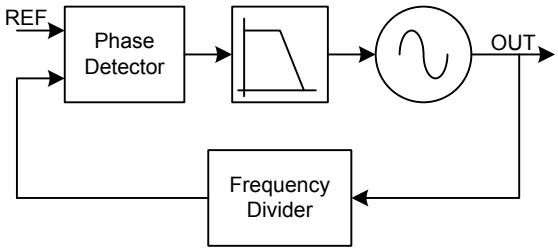


Figure 5.1: Block diagram of a PLL.

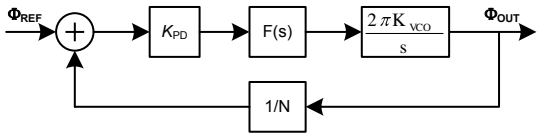


Figure 5.2: Linearized phase domain model of a PLL.

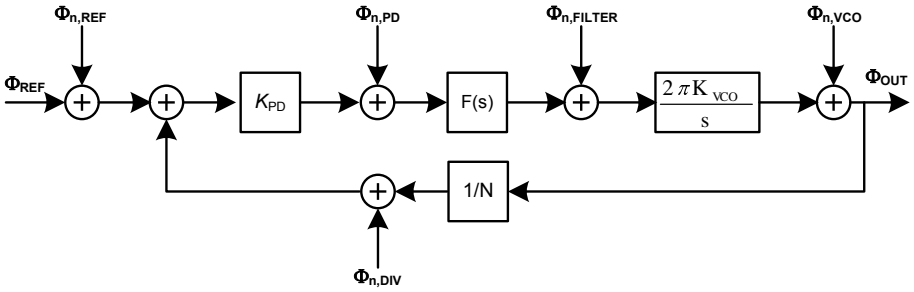
5.3 Overview of the significant noise sources

A generalized block diagram of a PLL is shown in Fig. 5.10 and its linearized phase domain model is shown in shown in Fig. 5.2. The loop gain $G_0(s)$ of the PLL is given by

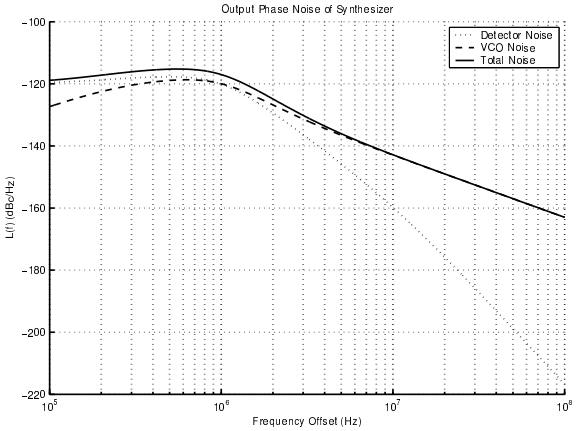
$$G_0(s) = \frac{K_{PD} \cdot F(s) \cdot 2\pi K_{\mathrm{VCO}}}{s \cdot \mathrm{N}} \tag{5.1}$$

where K_{PD} is the gain of the phase detector, $F(s)$ is the transfer function of the loop filter and K_{VCO} is the linearized tuning gain of the VCO.

Fig. 5.3(a) shows the various contributors to the phase noise of a PLL. The contribution from the loop filter can be made negligible by without adding power by either properly sizing the filter components or lowering K_{VCO} by design [35]. The noise contribution from the VCO undergoes a transfer function, $\frac{1}{1+G_0(s)}$, resulting in suppression within the loop-bandwidth. The noise contribution from the remaining blocks (referred to as loop components for simplicity) undergoes a transfer function, $N \cdot \frac{G_0(s)}{1+G_0(s)}$, resulting in suppres-



(a)



(b)

Figure 5.3: (a) Various contributors of noise in a PLL. (b) Phase noise spectrum at the output of the PLL with contributions from VCO, in-band components and overall.

sion beyond the bandwidth of the PLL. Fig. 5.3(b) shows a spectrum of phase noise of a PLL with the noise contributions from VCO dominating the out-of-band spectrum and the noise contributions form the loop components dominating the in-band spectrum.

5.4 Dependence of in-band phase noise performance on the supply voltage

The in-band phase noise of a PLL ($\mathcal{L}_{\text{in-band}}$) comprises of noise contributions from the phase detector ($\mathcal{L}_{\text{PLL,PD}}$), reference buffers ($\mathcal{L}_{\text{PLL,REF}}$) and the frequency divider ($\mathcal{L}_{\text{PLL,DIV}}$). In this section, we analyze the effect of power supply scaling on each of the noise source

5.4.1 Contribution from reference buffers

With the use of a sub-sampling PD [36] or a combined PD [37], the noise contribution from the phase detector to the PLL's in-band phase noise is shown to be significantly reduced. The in-band phase noise level in [36; 37] is limited by the noise from reference buffers [1]. In a practical implementation, the buffer is implemented as an inverter.

The rms phase noise of the reference signal at the output of the reference buffer is given by,

$$\overline{\phi^2_{\text{n,REF}}} = \left(\frac{2\pi f_{\text{REF}}}{SL}\right)^2 \times \overline{v^2_{\text{n,out,BUF}}} \tag{5.2}$$

where SL is the slope of the signal at the output of the buffer, f_{REF} is the reference frequency and $\overline{v^2_{\text{n,out,BUF}}}$ is the voltage noise at the output of the reference buffer.

For small reference swings,

$$SL = 2\pi f_{\text{REF}} G \frac{A_{\text{REF}}}{2} \tag{5.3}$$

[1] Assuming the availability of high phase purity crystal oscillators, the reference noise is dominated by the buffer.

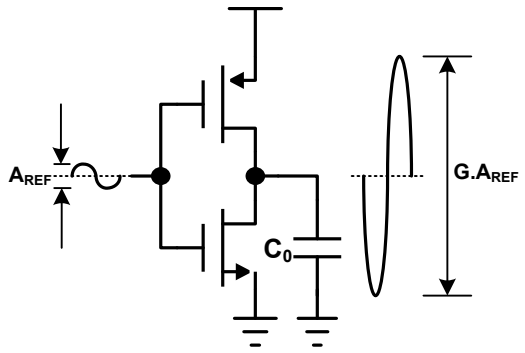


Figure 5.4: Operation of the reference buffer for small input signals.

and the phase noise at the output of the buffer circuit ($\mathcal{L}_{\rm BUF}(\Delta\omega)$) is given by

$$\begin{aligned}\mathcal{L}_{\rm BUF}(\Delta\omega) &= \frac{S_{\phi,n,\rm REF}}{2} = \frac{1}{2}\cdot\frac{\overline{\phi^2_{\rm n,REF}}}{f_{\rm REF}/2} \\ &= \frac{\overline{v^2_{\rm n,out,BUF}}}{f_{REF}G^2A^2_{REF}} \end{aligned} \tag{5.4}$$

where G is the voltage gain of the buffer, $f_{\rm REF}$ is the frequency of the reference signal and $A_{\rm REF}$ is the peak-to-peak amplitude of the reference signal at the input of the buffer [36; 38].

As the reference swing is increased, the buffer becomes slew-rate limited. Under this condition, the slope of the signal at its output is given by $\frac{I}{C_o}$, where C_o is the capacitance at the output of the reference buffer and I is its bias current source. One of the transistors of the buffer operate in cut-off region while the other is still in saturation region as shown in Fig. 5.6. I is then proportional to $V^2_{\rm DD}$. The phase noise power spectral density of the PLL

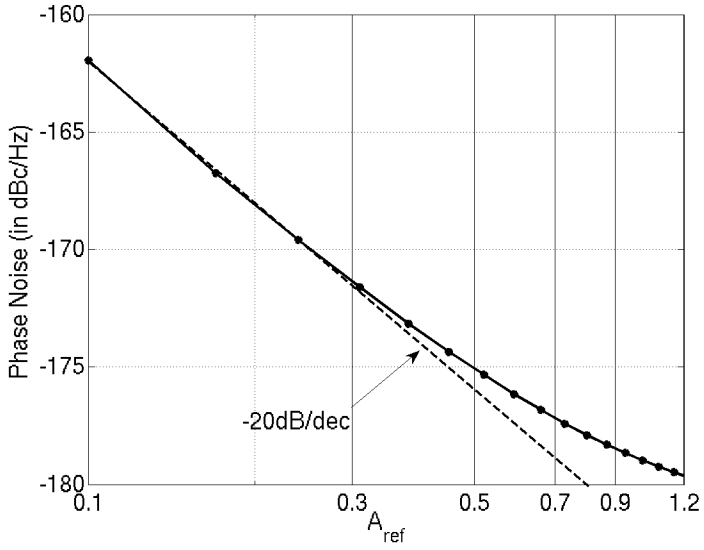


Figure 5.5: Simulated phase noise of reference signal at the output of the reference buffer as a function of amplitude of the reference.

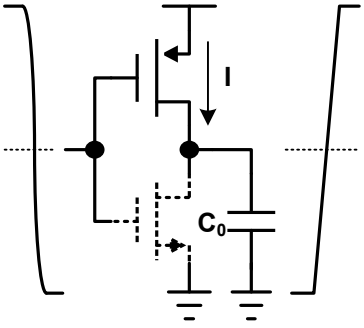


Figure 5.6: Operation of the reference buffer in the slew limited case.

due to the reference buffer is then given by

$$\begin{aligned} \mathcal{L}_{\text{PLL,ref}} &\approx \frac{N^2}{f_{\text{REF}}}\left(\frac{2\pi f_{\text{REF}} C_o}{I}\right)^2 \overline{v_{\text{n,out,BUF}}^2} \\ &= \frac{N^2}{f_{\text{REF}}}\left(\frac{2\pi f_{\text{REF}} C_o}{I}\right)^2 \frac{kT\gamma g_{\text{m,BUF}} r_o}{C_o} \\ &\propto \left(\frac{1}{V_{\text{DD}}}\right)^5 \end{aligned} \tag{5.5}$$

where $g_{\text{m,BUF}}$ is the transconductance of the transistors of the buffer and r_o is the resistance

at the output of the reference buffer.

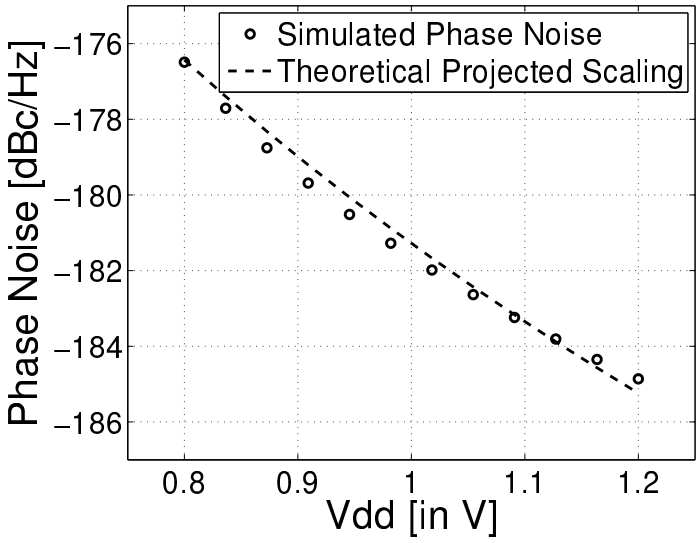


Figure 5.7: Simulated phase noise of the reference signal at the output of the reference buffer as a function of the power supply voltage.

5.4.2 Phase detector and the divider chain

A conventional tri-state PFD-CP has noise contributions from PFD and a charge pump. Under locked conditions, the charge pump's noise is attenuated by a factor of $T_{\mathrm{ON}}/T_{\mathrm{REF}}$ and tri-state PFD-CP's noise is arguably dominated by PFD which is a digital circuit. In order to reduce the noise contribution from the divider chain, a synchronizing d-flip flop (dff) is used at the output of the divider chain. The only noise from the divider is then that of the re-timing dff which is a digital circuit. The noise contributions from phase detector and divider chain would scale like a digital circuit which is approximated to as an inverter.

Table 5.1: Scaling of in-band phase noise with the power supply.

Power supply	V_{DD}	$\alpha \cdot V_{DD}$
Phase noise	$\mathcal{L}_{in-band}$	$\frac{1}{\alpha^5} \cdot \mathcal{L}_{in-band}$
Power $\left(= C_L V_{DD}^2 f\right)$	P_{loop}	$\alpha^2 \cdot P_{loop}$
FoM	$FoM_{in-band}$	$FoM_{in-band} - 30\log(\alpha)$

5.4.3 Scaling of FoM

The scaling of $\mathcal{L}_{in-band}$ is given by

$$\mathcal{L}_{in-band} \propto \left(\frac{1}{V_{DD}}\right)^5 \tag{5.6}$$

The FoM of the blocks of the loop contributing to the in-band phase noise is given by

$$FoM_{in-band} = 10 \cdot \log\left(\mathcal{L}_{in-band} \cdot \left(\frac{1\text{Hz}}{f_{out}}\right)^2 \cdot \frac{P_{loop}}{1\text{mW}}\right) \tag{5.7}$$

where P_{loop} is the power consumed by the loop components (reference buffer, PD and frequency dividers) [35]. Lower FoM is an indication of a better designed circuit. A summary of the scaling trends is tabulated in Table 5.1.

5.5 Scaling of oscillator's noise

Fig. 5.8 shows a current-biased NMOS cross-coupled pair LC oscillator with a biasing current I_{BIAS}. The oscillation frequency, f_0, is set by the parallel inductance L and capacitance C of the tank

$$f_0 = \sqrt{\frac{1}{2\pi LC}} \tag{5.8}$$

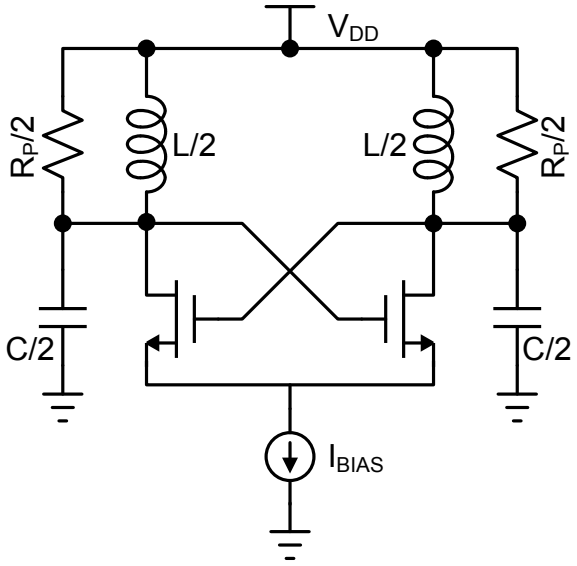


Figure 5.8: Schematic diagram of a current-biased NMOS cross-coupled pair LC oscillator.

5.5.1 Oscillation amplitude-Vdd trade-off

For sufficiently large amplitudes, the transistors in the cross-coupled pair switch between ON and OFF and steer the dc bias current (I_{BIAS}) to alternate sides of the tank. The resulting square-wave currents flow through the tank, which converts their fundamental frequency components into a sinusoidal output voltage while filtering out all other frequency components; the amplitude of the fundamental of the resulting differential output amplitude

$$A = \frac{2}{\pi} I_{\mathrm{BIAS}} R_P \tag{5.9}$$

where R_P is the parallel resistance of the tank.

As I_{BIAS} is increased, the amplitude of oscillation increases until it becomes limited by the power supply voltage. For optimal FoM, the I_{BIAS} is chosen such that the oscillator is just at the brink of voltage limited regime [39]. In order to study the effect of supply voltage scaling on the VCO, the I_{BIAS} is assumed to scale along with the power supply. In

other words, when the power supply is scaled by α (from $V_{DD,0}$ to V_{DD}), the amplitude of oscillation is also scaled by α.

$$\begin{aligned} V_{DD} &= \alpha V_{DD,0} \\ A &= \alpha A_0 \end{aligned} \tag{5.10}$$

5.5.2 VCO's phase noise

The phase noise of the LC oscillator at an offset frequency $\Delta\omega$ from the carrier frequency ω_0 can be expressed as

$$\mathcal{L}(\Delta\omega) = F \cdot \frac{4kT}{A^2} \cdot \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 \tag{5.11}$$

where F is the excess noise factor modeling the noise contribution from the active devices [40]. Extensive research has been conducted to determine an analytical expression for F. Based on the phasor analysis theory, an expression for the phase noise of the VCO is derived as

$$\mathcal{L}(\Delta\omega) = \frac{4kTR_P}{A^2} \cdot \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 \cdot \left(1+\gamma+\frac{\gamma g_{m,bias} R_P}{4}\right) \tag{5.12}$$

[41]

5.5.3 Scaling of an oscillator's FoM with its power supply

A phase noise-power consumption trade off exist for an oscillator. The quality of the oscillator is then measured by a FoM which is defined as [42]

$$\text{FoM}_{VCO} = 10 \cdot \log\left(\frac{\mathcal{L}(\Delta\omega) \cdot \left(\frac{\Delta\omega}{\omega_0}\right)^2 \cdot \frac{V_{DD} I_{BIAS}}{1\text{mW}}}{115}\right) \tag{5.13}$$

Table 5.2: Scaling trends of a current source biased oscillator biased as a function of its power supply.

	Cross-coupled pair and tank resistance noise dominant oscillator		Current source noise dominant oscillator	
Power supply	V_{DD}	$\alpha \cdot V_{\mathrm{DD}}$	V_{DD}	$\alpha \cdot V_{\mathrm{DD}}$
Bias current	I_{BIAS}	$\alpha \cdot I_{BIAS}$	I_{BIAS}	$\alpha \cdot I_{BIAS}$
Amplitude	A	$\alpha \cdot A$	A	$\alpha \cdot A$
Power	P	$\alpha^2 \cdot P$	P	$\alpha^2 \cdot P$
Phase noise	$\mathcal{L}$	$\frac{1}{\alpha^2} \cdot \mathcal{L}$	$\mathcal{L}$	$\frac{1}{\alpha} \cdot \mathcal{L}$
$\mathrm{FoM}_{\mathrm{VCO}}$	FoM	FoM	FoM	FoM $+10\log(\alpha)$

Using the expressions for $\mathcal{L}(\Delta\omega)$ in (5.12), the FoM can be computed as

$$\begin{aligned} \mathrm{FoM}_{\mathrm{VCO}} &= 10 \cdot \log\left[\frac{\mathrm{k}TR_{\mathrm{P}}}{Q^2A^2} \cdot \left(2 + 2\gamma + \frac{8\gamma g_{\mathrm{m,bias}} R_{\mathrm{P}}}{9}\right)\right] \\ &\quad + 10 \cdot \log\left[\frac{V_{\mathrm{DD}} I_{\mathrm{BIAS}}}{1\mathrm{mW}}\right]. \end{aligned} \tag{5.14}$$

When the power supply is scaled by α (from $V_{\mathrm{DD},0}$ to V_{DD}), the amplitude of oscillation is also scaled by α. Table 5.2 describes the scaling trends of a current source biased oscillator with the power supply.

FoM of an oscillator, where the noise is dominated by a cross-coupled pair's noise, remains constant, while the FoM of an oscillator, where the noise is dominated by its tail current source, increases by $10 \cdot \log(\alpha)$. In a real oscillator, both the sources contribute, and the FoM is expected to increase by a factor between 0 and $10 \cdot \log(\alpha)$.

Simulation is conducted to verify the scaling theory for a current biased oscillator shown in Fig. 5.8. The oscillator is designed to operate at a center frequency of 10GHz. Fig. 5.9 plots the phase noise of the oscillator at 1MHz offset and its FoM as a function of

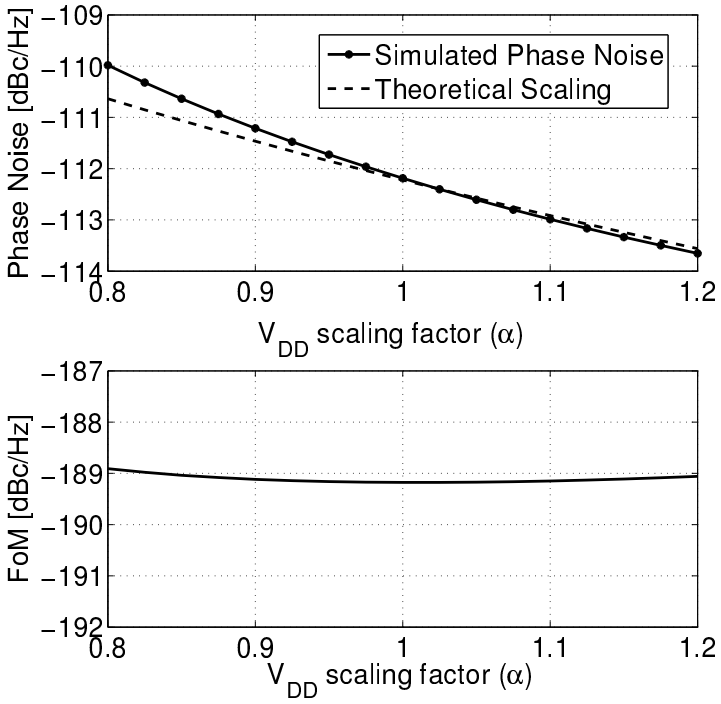


Figure 5.9: 10GHz oscillator's phase noise at 1MHz offset and FoM vs. V_{DD}. The oscillator's noise is dominated by its cross-coupled pair and its tank impedance.

the power supply. The oscillator's noise is dominated by its cross-coupled pair and its tank impedance [2]. The phase noise follows the scaling law, and the FoM of the oscillator is seen to be relatively constant.

5.6 Scaling of PLL's jitter with V_{DD}

Theories for the scaling of $FoM_{\mathrm{in-band}}$ and FoM_{VCO} were developed in section 5.4 and section 5.5, respectively. In this section we show the derivation of the theoretical estimate for the scaling of PLL's jitter with its power supply voltage. The oscillator is assumed to be

[2] An ideal current source is used as the tail current source. This enables the tail current to be noiseless.

cross coupled pair's noise dominated in this derivation. Results are presented for the case of tail current source's noise dominated oscillator.

5.6.1 Jitter of a PLL

The jitter of the PLL has two main contributors: loop components (in-band) and the VCO (out-of-band). The contribution from the loop-filter is assumed to be negligible. The contribution to jitter from the loop (in-band sources) is given by

$$\begin{aligned} \sigma^2_{\mathrm{t,in-band}} &= \frac{G_{\mathrm{in-band}} f_c}{\alpha^3 P_{\mathrm{in-band}}} \\ G_{\mathrm{in-band}} &= \frac{1}{2\pi^2 f_{c,0}} \cdot \int_0^\infty \left| \frac{G_0(s)}{1+G_0(s)} \right|^2 df \end{aligned} \tag{5.15}$$

where f_c is the bandwidth of the PLL, $P_{\mathrm{in-band}}$ is the power consumed in the phase detector and $G_0(s)$ is the loop gain of the PLL as a function of frequency [35] for a PLL bandwidth of $f_{c,0}$.

The contribution to jitter from the VCO is given by

$$\begin{aligned} \sigma^2_{\mathrm{t,VCO}} &= \frac{G_{\mathrm{VCO}}}{P_{\mathrm{VCO}} f_c} \\ G_{\mathrm{VCO}} &= 2 f_{c,0} \cdot \int_0^\infty \left| \frac{1}{s\,(1+G_0(s))} \right|^2 df \end{aligned} \tag{5.16}$$

The overall jitter of the PLL is then given by

$$\begin{aligned} \sigma^2_{\mathrm{t,PLL}} &= \sigma^2_{\mathrm{t,in-band}} + \sigma^2_{\mathrm{t,VCO}} \\ &= \frac{G_{\mathrm{in-band}} f_c}{\alpha^3 P_{\mathrm{in-band}}} + \frac{G_{\mathrm{VCO}}}{P_{\mathrm{VCO}} f_c} \\ P_{\mathrm{PLL}} &= P_{\mathrm{VCO}} + P_{\mathrm{in-band}} \end{aligned} \tag{5.17}$$

The jitter is now a function of (a) bandwidth f_c of the PLL, (b) power consumption of the PLL and (c) the power supply scaling factor (α).

5.6.2 Jitter as a function of power supply

We are interested in the scaling of the minimum jitter as a function of power supply. In order to understand this scaling, the minimum jitter is computed as function of α, by optimizing the bandwidth and power. For lowest jitter the power should be equally distributed between VCO and the loop components. The result is in agreement with the conclusions of [35]. The optimal bandwidth is given by

$$f_{\mathrm{c,opt}} = \alpha^{1.5} \cdot \sqrt{\frac{G_{\mathrm{VCO}}}{G_{\mathrm{in-band}}}}. \tag{5.18}$$

The lowest achievable jitter is given by

$$\sigma^2_{\mathrm{t,min}} = \frac{\sqrt{G_{\mathrm{VCO}} G_{\mathrm{in-band}}}}{P\alpha^{1.5}}. \tag{5.19}$$

where $\sigma^2_{\mathrm{t,min}}$ is the minimum jitter of the PLL and P is the power consumed in the PLL.

If an oscillator, whose noise is dominated by its tail current source, is used in the PLL, the lowest achievable jitter is then given by

$$\sigma^2_{\mathrm{t,min}} = \frac{\sqrt{G_{\mathrm{VCO}} G_{\mathrm{in-band}}}}{P\alpha}. \tag{5.20}$$

5.6.3 Simulation results

A third order, type II PLL (shown in Fig. 5.10) is used as a test vehicle to verify the theory developed in this section. The loop parameters of the PLL are described in the Table 5.3.

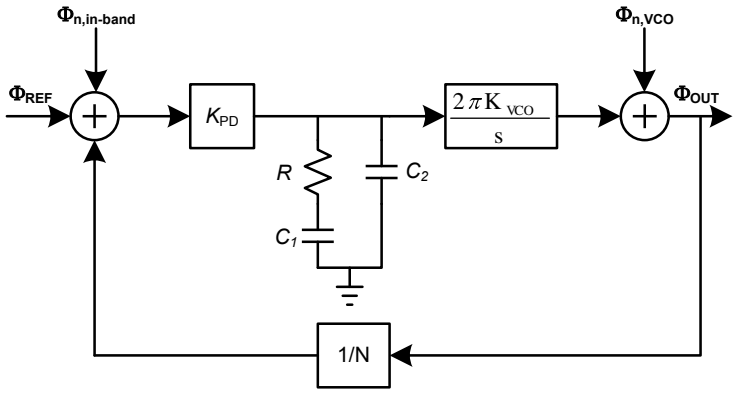


Figure 5.10: Simulation setup used for PLL jitter simulation. Linearized phase domain models are used for Phase detector and VCO.

Table 5.3: List of PLL parameter values used for minimum jitter for vdd=1V.

Parameter	Value
f_{out}	10GHz
f_{ref}	1GHz
C1	37pF
C2	370fF
Kvco	100MHz/V
Kpd	60uA/rad
R	1.6kΩ

Linearized phase domain models (verilоga) are built for the VCO and phase detector. The simulated jitter as a function of PLL's bandwidth for various power supply voltages is shown in Fig. 5.11. The simulation assumes the PLL to use an oscillator whose tail current sources contributes insignificant amount of noise (referred as oscillator 1 for simplicity).

Bandwidth is scaled by scaling C1, C2 and Kpd without altering the relative positions of the poles and zeros. This is done to ensure the phase margin does not alter. The effect of power supply variation is incorporated directly into the strength of the phase noise; $\mathcal{L}_{\text{in-band}}$ is made inversely proportional to V_{DD}^3 and $\mathcal{L}_{\text{VCO}}$ is made constant. A matlab based PLL

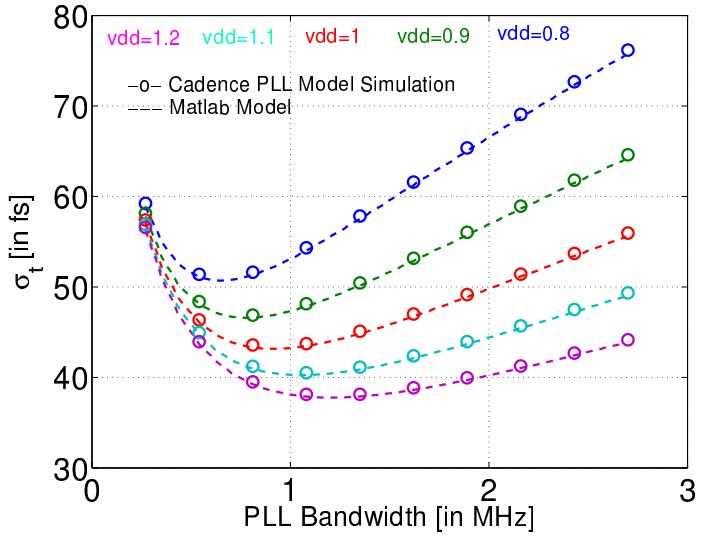


Figure 5.11: Jitter at the output of a 10GHz integer-N PLL as a function of PLL bandwidth for various V_{DD}s.

model was also built to verify the simulation results from cadence. Fig. 5.11 shows a close match between the two simulations.

Matlab simulations were conducted for PLLs using two kinds of oscillators: oscillator 1 (described previously) and oscillator 2 (noise contribution from the tail current source being dominant). Based on matlab simulations, minimum jitter at the output of a 10GHz integer-N PLL as a function of V_{DD} is plotted in Fig. 5.12. The simulation results and the theoretical jitter scaling model are found to have a close match.

5.7 Conclusions

In this chapter, theoretical estimates for the scaling of in-band phase noise and VCO phase noise on the supply voltage are derived. Based on these estimates, the scaling of a PLL's

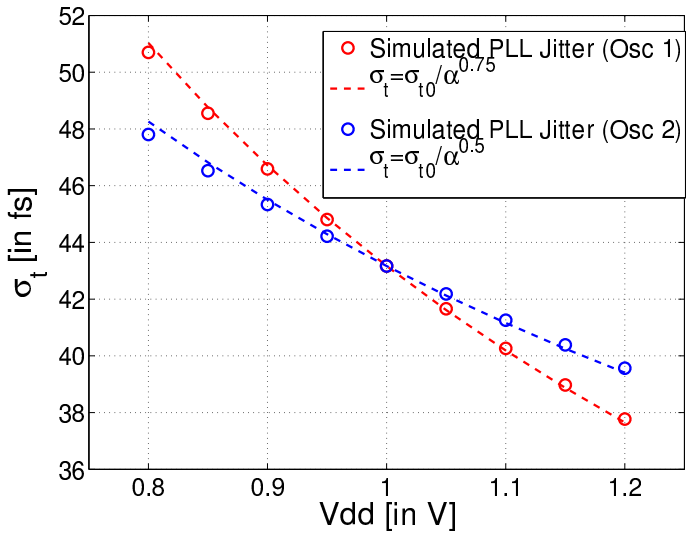


Figure 5.12: Minimum jitter at the output of a 10GHz integer-N PLL as a function of V_{DD}. The minimum jitter scales as $1/V_{DD}^{0.75}$ for a PLL using oscillator 1 (insignificant noise contribution from the tail current source), while it scales as $1/\sqrt{V_{DD}}$ for a PLL using oscillator 2 (noise contribution from the tail current source being dominant).

phase noise and jitter with the supply voltage is derived.

For a given power budget, the minimum jitter at the output of a PLL is found to scale as $\left(\frac{1}{V_{DD}}\right)^{0.75}$ when the oscillators tail current source's noise is insignificant. When the oscillators tail current source's noise is dominant, the jitter is expected to scale as $\left(\frac{1}{V_{DD}}\right)^{0.5}$.

Chapter 6

A Digitally Controlled CMOS Phase Shifter with Frequency Doubling for Multiple-Antenna, Direct-Conversion Transceiver Systems

6.1 Abstract

A digitally controlled frequency-doubling phase-shifter architecture is presented for the implementation of multiple-antenna GHz transceiver systems. It takes a 1.75GHz input and produces two phase-shifted outputs at 3.5GHz. It consists of a Delay Locked Loop (DLL) followed by symmetric XOR frequency doublers and phase interpolators. The phase

shifter prototype in 90nm standard CMOS has a phase shift range of 360° with a resolution of 22.5° and an INL $< 12°$ ($< 4°$ with external adjust), and consumes 55mW from a 1V supply.

6.2 Introduction

Beam steering using multiple-antenna transceivers is an emerging area of research for commercial wireless communication applications. Realizing narrow beams offers spatial filtering and can relax the receiver's linearity requirements, however, it requires accurate gain and phase matching in the various antenna transceivers. For RF systems operating from 800MHz to 5GHz, wavelengths in free space vary from 37.5 to 6cms and the transceivers thus reside on different chips on a PCB. The task of phase matching the different antenna signal paths is then more challenging than at mm-wave frequencies [43] and is divided into phase synchronization and accurate phase shifting. In this work, we address the problem of phase shifting in standard CMOS.

Trade-offs in implementing the phase shift in the RF signal path, or LO path, or digital baseband and IF stage have been extensively studied and summarized e.g. in [43]. For our application we prefer to implement LO path phase shift which is less challenging in terms of linearity or noise requirements compared to RF signal path solutions, while still offering relaxed linearity requirements for the blocks following IF signal combining. Passive phase shifters [44; 45] have very low power consumption, but occupy large area and have substantial signal loss. Moreover, achieving 360° of phase shift is very difficult and the

phase-shift voltage-control characteristics are strongly non-linear and subject to process, voltage and temperature variations.

The most common architecture for active phase shifters is to generate multiple phases with a delay-locked loop (DLL) or (ring oscillator) phase-locked loop (PLL) followed by phase interpolation circuits to increase resolution. E.g., in [46], a delta sigma is used to dither the phases and generate arbitrarily fine phase resolution for clocking but at the expense of spectral purity. For wireless applications we require more stringent spectral purity to mitigate reciprocal mixing in the receiver. Cartesian combining of quadrature LO signals is a possible solution, see e.g. [47], but in our multi-chip system realization distributing quadrature signals on the PCB would be a significant overhead.

This paper is organized as follows. Section 6.3 describes the constraints imposed by the system, section 6.4 discusses the implementation of the phase shifter with frequency doubling and finally section 6.5 presents the experimental results.

6.3 System constraints

The multiple-antenna receiver block diagram is shown in Fig. 6.1. To save power, a single high purity LO source is distributed on the PCB to the different transceiver chips where a phase shifter provides the correct phase to the receiver and transmitter (not shown) under the control of a digital code. To avoid LO-to-RF coupling in the direct conversion receiver or LO pulling in the direct conversion transmitter, the off-chip LO has to be necessarily at twice or half the RF frequency. For our target 3.5GHz WiMAX application, LO distribu-

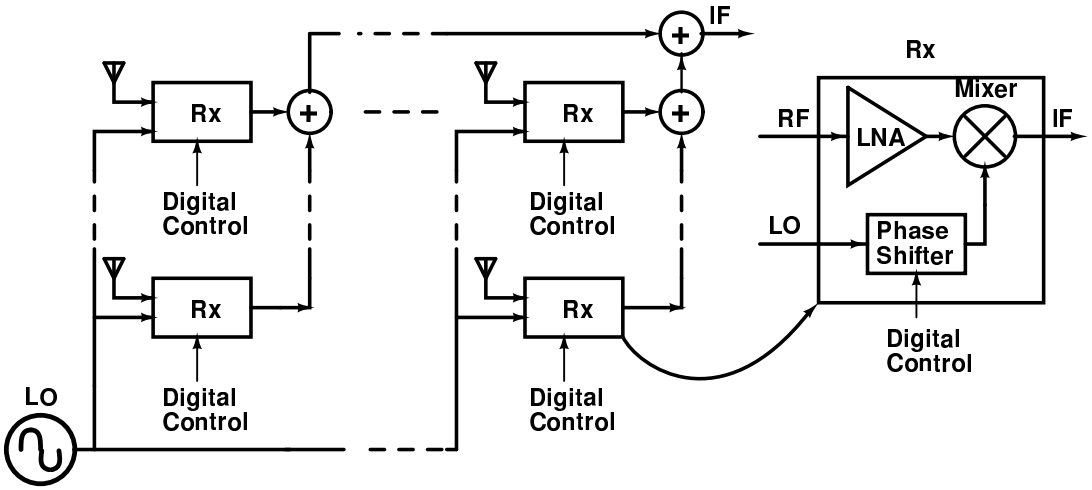


Figure 6.1: Block diagram of a multiple-antenna receiver

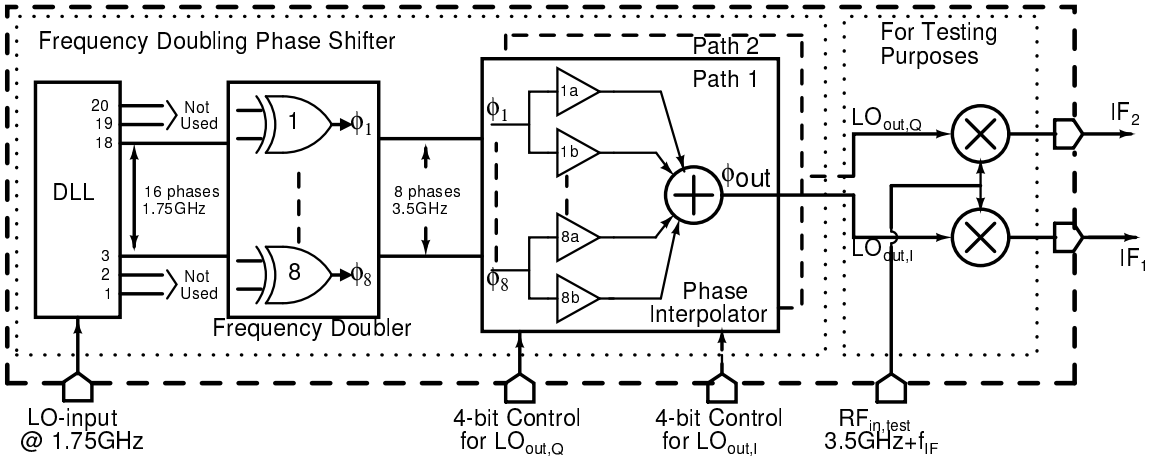


Figure 6.2: Block diagram of the frequency doubling phase shifter

tion at 1.75GHz is strongly preferred over 7GHz signal distribution across the PCB, thus necessitating the phase shifter to incorporate a frequency doubler.

6.4 Phase shifter with frequency doubling architecture and implementation

The block diagram of the frequency doubling phase shifter is shown in Fig. 6.2. A 20-cell DLL is the first stage of the phase shifter. Sixteen output phases spaced at 22.5° from a 1.75GHz DLL are appropriately combined in the frequency doubler to generate 8 phases spaced at 45° at 3.5GHz and then followed by phase interpolation to restore the resolution to 22.5° at 3.5GHz. Two phase interpolators are implemented and controlled by two separate 4-bit digital codes to generate two independent phase shifted output signals. In the final architecture, this will allow to generate quadrature signals but in the current prototype more phase shift combinations have been evaluated.

To facilitate testing, the chip prototype further contains two mixers driven by a common RF input signal and the phase shifted LOs so that the phase shift can be accurately determined at a low IF frequency.

6.4.1 Delay locked loop

The detailed block diagram of the DLL implementation is shown in Fig. 6.3. To operate at high frequencies, an XOR gate is preferred as phase detector given that frequency locking is not an issue. However, when the loop locks the inputs of the XOR phase detector will be in quadrature. The number of elements in the delay line has been increased to accommodate an additional phase shift of 90°. To generate phases which are multiples of $\frac{360^o}{16}$, a 20-stage

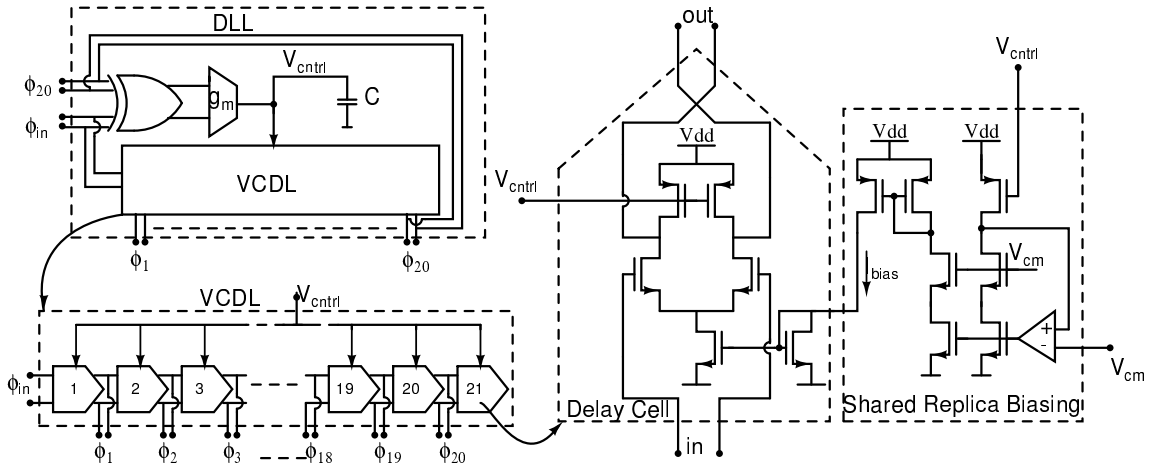


Figure 6.3: DLL and CMOS delay cell implementation and biasing

delay line was used. The first 2 and the last 2 phases are discarded and the middle 16 phases are used to drive the frequency doubler. To ensure identical loading, the discarded phases are also loaded with dummy frequency doubler stages. Any deterministic phase errors due to edge effects in the beginning or final stages of the loop are also avoided in this way.

A NMOS differential pair loaded with tunable resistive loads is used as the voltage controlled delay cell. The tunable resistance is implemented using pMOS transistors biased in triode region whose resistance is controlled by the gate voltage. As the delay, and thus the load resistance is changed, a replica bias circuit varies the cell's bias current to maintain a constant output common mode and amplitude.

The loop filter is integrated on chip with a g_m-C based integrator with an on-chip 200pF loop filter.

6.4.2 Frequency doubling

Frequency doubling is performed using an XOR gate driven by quadrature signals which are readily available from the DLL. Symmetrical loading of each DLL stage is crucial to avoid deterministic phase errors. The XOR gate presented in Fig. 6.4 is symmetric with respect to its differential inputs and its loading. It operates as follows: when both the differential inputs are of the same polarity, one of the paths on the left is turned ON, making the tail current to flow through PM1 and $V_{outp} - V_{outn}$ is negative; when the inputs are of opposite polarity, the current flows through $PM2$ and $V_{outp} - V_{outn}$ is positive. pMOS transistors biased in triode region are used to implement the load resistors and the XOR's bias current is generated by a replica biasing scheme to set the common mode at the output.

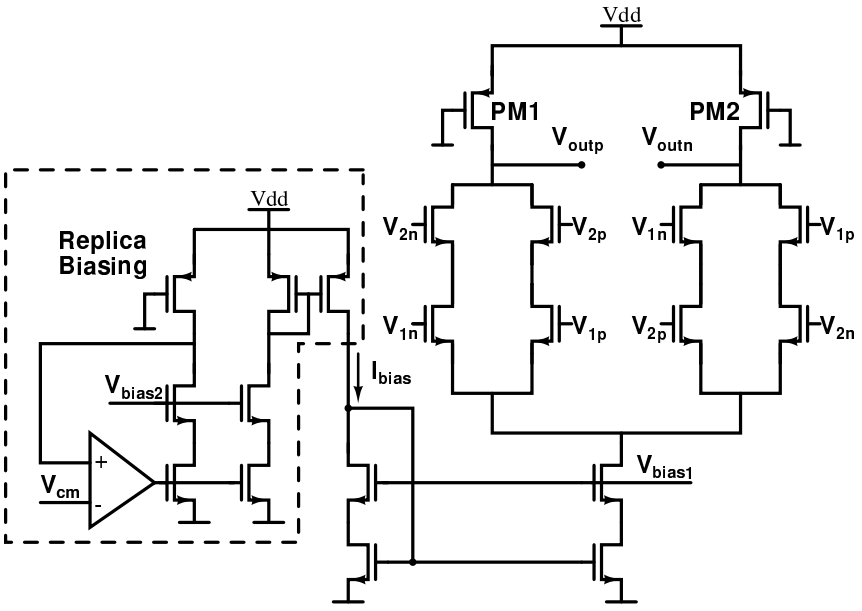


Figure 6.4: High speed symmetric XOR gate for frequency doubling

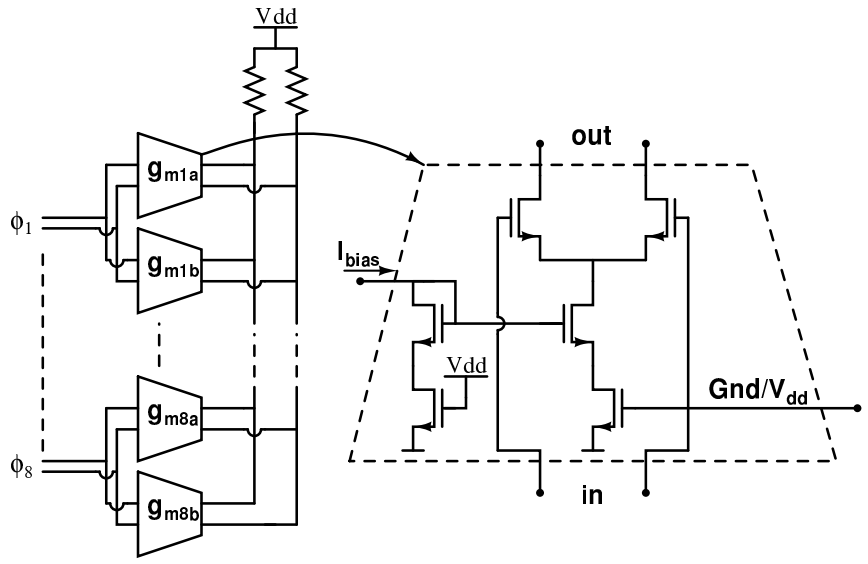


Figure 6.5: Phase interpolator implementation

6.4.3 Phase interpolation

The phase interpolator implemented in this chip is shown in Fig. 6.5. The outputs of differential transconductors are combined to perform interpolation. Depending on the desired output phase, the differential pairs in the transconductor are switched ON/OFF using an NMOS switch in series with the tail current source. When phase ϕ_i is desired at the output, transconductors g_{mia} and g_{mib} are turned ON; when the interpolation between phase ϕ_i and ϕ_{i+1} is desired, transconductors g_{mib} and $g_{m(i+1)a}$ are turned ON. By using two transconductors for every phase, the loading (and thus delay) of the summing node is made independent of the digital code. The resistive load of the interpolators is implemented with pMOS resistors, with a similar biasing arrangement as in the XOR circuit.

Table 6.1: A comparison of phase shifter implementations

	[44]	[46]	[48]	**THIS WORK**
Architecture	Passive	DSM Phase Interp.		DLL, Freq. Doubler, Phase Interp.
	Signal Path	CLK Path	CLK Path	LO Path
Operating Frequency	2GHz	0.5GHz- 1.5GHz	50MHz - 150MHz	3GHz-3.5GHz
Measurement Frequency	2GHz	1GHz	125 MHz	3.4GHz
Phase Resolution	N/A	$< 0.360°$	$1.40°$	$22.50°$
Phase Span	$< 360°$	$< 360°$	$360°$	$360°$
INL (time in ps)	N/A	-12 to 12	-62.5 to 62.5	-9.15 to 8.5 [-3.27 to 3.27 (w/ ext. adjust)]
INL (degrees)	N/A	-4.30 to 4.30	-0.780 to 0.780	-11.2 to 10.5 [-4 to 4 (w/ ext. adjust)]
Power	6.8mW	15mW	110mW	55mW (includes 2mW of test mixers)
Active Area	$0.75mm^2$	$0.48mm^2$	$1.156mm^2$	$0.49mm^2$
Technology	180nm	130nm	350nm	90nm
Power Supply	1.8V	1.2V	3.3V	1V

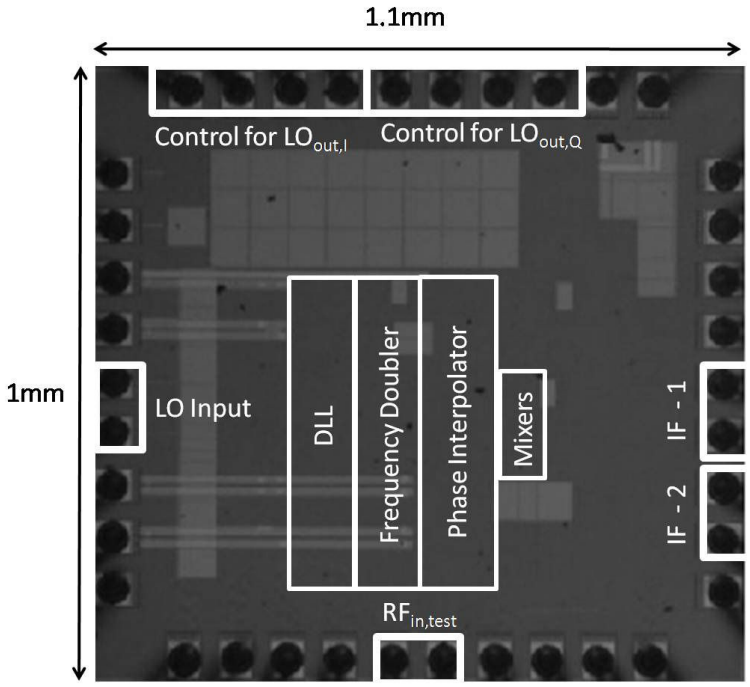


Figure 6.6: Die photograph

6.5 Measurement Results

A micro-photograph of the 90nm prototype die measuring $1.1mm^2$ and an active area of $0.49mm^2$ is shown Fig. 6.6; the die is packaged in a standard plastic 32-pin QFN package and mounted on a 4-layer FR-4 PCB.

Measuring phase shifts accurately at 3.5GHz is difficult given the high sensitivity to matching-network phase shifts, bond-wire lengths and trace/cable lengths – a length variation of only 0.6mm in trace/cable corresponds to a phase variation of 5°. Therefore the output phase difference is measured at a low 100kHz IF frequency by down-converting ($LO_{out,I}$, $LO_{out,Q}$) with on-chip double-balanced Gilbert-cell mixers driven by a common RF signal, $RF_{in,test}$.

In the intended application the phase shifter is required to produce double-frequency quadrature LO outputs ($LO_{out,I}$, $LO_{out,Q}$) with a controllable phase shift compared to the LO input, LO_{in}. We cannot directly measure the phase shift between the LO input and outputs, but measure the phase shift, $\Delta\phi(i)$ between the two independently controllable output signals; the control for the 'reference' signal, $LO_{out,Q}$, is kept constant and the control, i, for the 'test' signal, $LO_{out,I}$, is varied [1]. Now, the phase shift, θ_0, between the input LO_{in} and the reference, $LO_{out,Q}$, is constant. Then the actual phase shift between the LO_{in} and $LO_{out,I}$ is $\theta_0 + \theta(i)$[2]. In the intended application, a (factory) calibration will be used

[1] We confirmed experimentally that the measured incremental phase shift in the test path was independent of the choice of 'reference' control setting.

[2] The incremental phase shift was measured for every code i and the phase shift, $\theta(i)$, was computed as

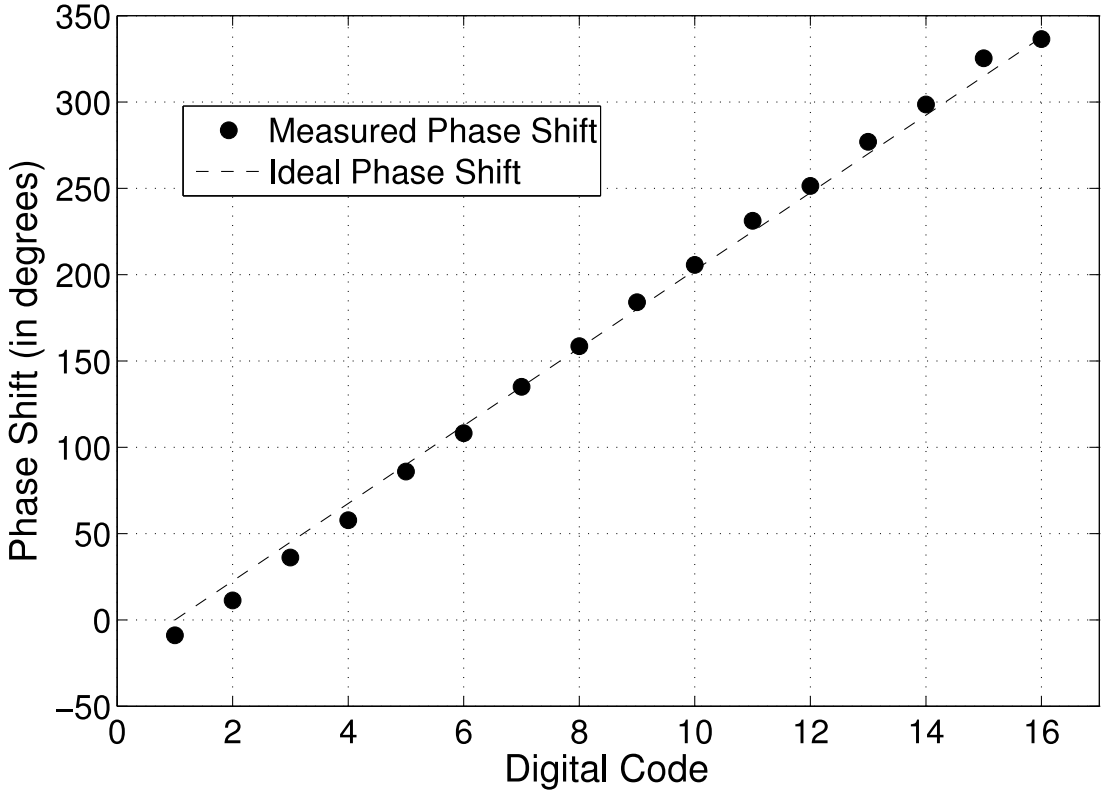


Figure 6.7: Measured phase shift vs digital code (Chip 1)

to eliminate θ_0, and here we focus on the linearity of $\theta(i)$ vs code compared to an ideal 22.5°/code characteristic.

Fig. 6.7 shows $\theta(i)$ vs digital code and Fig. 6.8 shows the INL vs digital code of the phase shifter. The systematic linear increase in INL is due to a systematic phase error in the DLL stages. The odd digital codes $i = 1,3,\ldots 15$ correspond to the eight frequency doubler outputs. From the measurement, it was estimated that they are separated by 47.9° instead of 45°. After DLL locking, the delay line control voltage, V_{cntrl} was measured to be much lower than designed; this significantly reduces the loop filter gain, explaining the

the cumulative sum of incremental phase shifts.

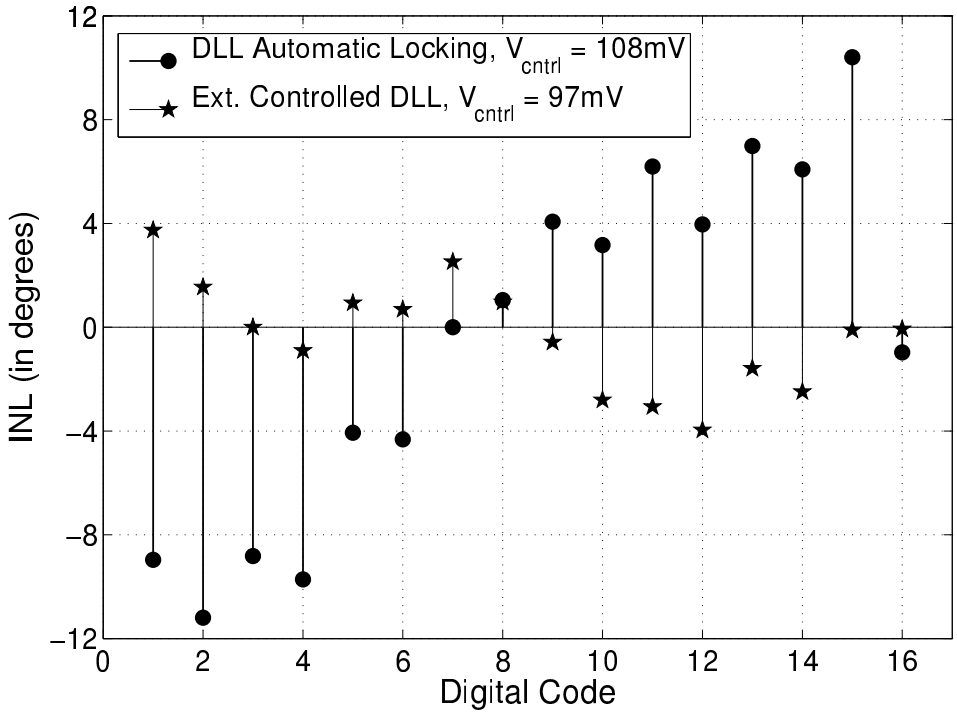


Figure 6.8: Measured INL vs digital code (Chip 1) for automatic DLL lock and external control voltage adjust

static phase error. V_{cntrl} was adjusted externally to decrease the systematic phase offset and the resulting INL is plotted in Fig. 6.9 for two prototype chips.

A summary of the measured chip performance is shown in Table 6.1 in comparison with other architectures; we note the high frequency of operation with high time accuracy and small area while offering a complete 360° phase shift range.

6.6 Conclusions

In this work, we present a compact, digitally controlled, frequency-doubling LO phase-shifter architecture for multiple-antenna transceiver systems operating in the GHz range.

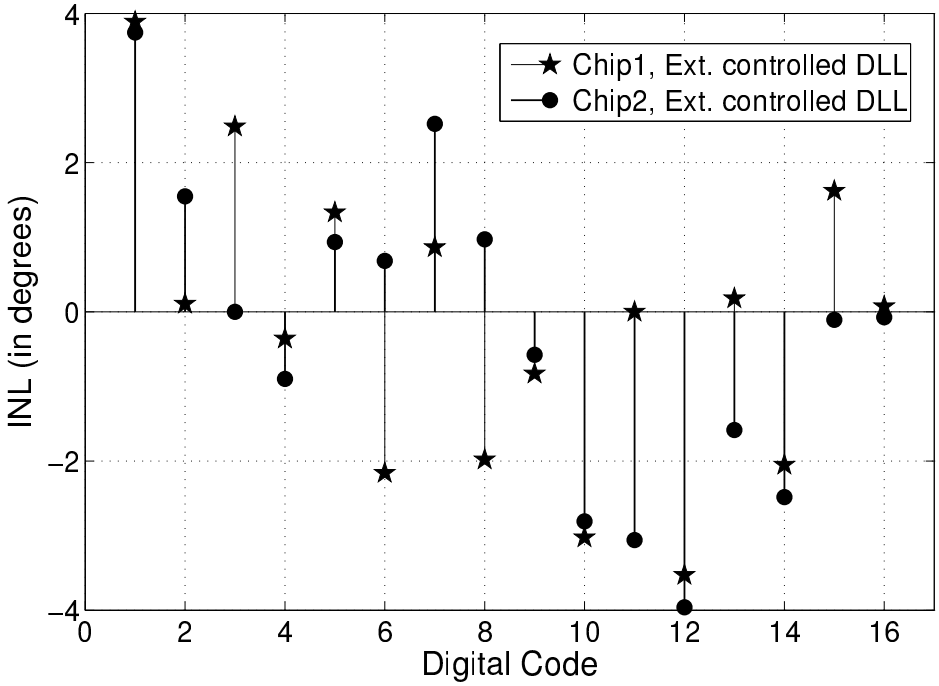


Figure 6.9: Measured INL vs digital code for Chips 1 and 2 with external control voltage adjust

In comparison to passive architectures, it does not suffer any signal loss and provides a complete 360° phase shift range. Our DLL based architecture operates with single input phase and doesn't need quadrature inputs as in Cartesian combiner [47], which reduces the complexity of a multiple-antenna system design significantly. Additionally, by not using a delta-sigma modulator for phase interpolation as in [46], we avoid the degradation of spectral purity of the LO.

The 90nm CMOS phase shifter prototype has a phase shift range of 360°, a resolution of 22.5° with an INL $< 12°$. The dominant source of non-idealities in the phase shift has been identified as the static phase offset at the DLL phase detector input due to insufficient loop gain. With external adjust of the DLL control voltage to reduce the phase detector

error, the INL reduces to $< 4^{\circ}$.

Chapter 7

Conclusion and Future Work

The PLL settling time is an important bottleneck to reducing the spectrum scanning duration. Gharpurey introduced an idea known as iterative down-conversion in [13]. The IDC, operating with a fixed frequency PLL, incorporates the role of frequency synthesis within the signal path using a cascade of image-reject mixers. We present a study of adaptation of an IDC to implement the RF channelizer. The fundamental limitation to the dynamic range, signal leakage to adjacent channels, is analyzed.

In order to overcome the limitations of an IDC, a novel 3-way IDC is developed. The 3-way IDC architecture enables the use of filtering to compliment harmonic rejection of the mixer in order to improve the signal leakage. A 0.75GHz-11.25GHz RF channelizer is implemented in 65nm CMOS technology using the 3-way IDC. The RF channelizer splits the input signal into seven channels each of bandwidth 1.5GHz. In order to demonstrate both concurrency (multiple outputs being available simultaneously) and fast-switching between

channels, a partially concurrent 3-output fast-switching RF channelizer is demonstrated.

A circuit block called multi-mode mixer is developed. The multi-mode mixer can operate either as a mixer or a transparent block, passing the input directly to the output. The multi-mode mixer enables the reduction of hardware and thus in considerable reduction in the area of the RF channelizer. Further, the mixer enables the reduction of load for the driving circuitry of the preceding stage. This is capable of considerable power savings, particularly when used in high bandwidth situations.

The rejection of higher harmonics of a mixer is crucial in many applications. For instance, it limits the signal leakage performance in an IDC, relaxes the filter requirements in the 0.75GHz-11.25GHz RF channelizer, etc. As the bandwidth of the cognitive radio increases, there is a need for harmonic rejection mixers which can operate at LOs of multiple GHz and reject higher harmonics of LO. A novel order-scalable, high-LO-frequency harmonic rejection mixer architecture is developed.

Feature size of a transistor is scaled in successive technologies to improve the speed of the transistors. Power supply scaling is necessary along with feature size scaling in order to maintain reliable operation of a CMOS transistor. Technology scaling has benefited digital circuits in terms of speed as well as power consumption. The increase in f_T has also helped analog circuits in terms of bandwidth and noise figure. To exploit these advantages of technology scaling, SoCs are implemented in modern technologies. At high speeds or high dynamic range operation of an ADC, the jitter of its clock source becomes a performance limiting factor. We present a study on the effect of power supply scaling on a PLL's jitter.

Phased array based electronic beam steering can be a effective way to solve the problem of spectrum scarcity. Phase shifter is an essential circuit block. An analysis of various techniques of phase shifting is presented and a frequency-doubling phase shifter architecture for multi-antenna transceiver system is demonstrated.

7.1 Topics for future research

The investigations that have formed this thesis have opened up several topics for future research. These topics are listed here briefly.

- A concurrent IDC described in chapter 2 down-converts all the channels simultaneously. However, the dynamic range is limited by the signal leakage due to finite image and harmonic rejection of the mixers. The IDC with becomes power in-efficient if each of its mixers requires superior harmonic and image rejection. In this context, baseband digital signal processing techniques could be used to cancel the signal leakage and recover the SNR in digital domain. These techniques would potentially relax the harmonic rejection and image rejection requirements of the mixers in the IDC which could result in large power savings in the mixers.

- In the context of broadband receivers, the linearity of LNA is an important consideration. Since there would be no filtering prior to the LNA, the LNA will be required to handle a large number of blockers without saturating. [49] has used N-path filtering techniques to suppress the blockers before amplification. However, LO re-radiation

is considered a serious problem with such designs. Further, there is a need for suppressing multiple blockers at LNA's input. This provides research opportunities in the field of high linearity broadband LNAs.

- The dynamic range of the RF channelizer discussed in Chapter 3 is shown in Fig. 7.1. The channels involving multiple stages of mixing tend to have lesser dynamic range. Alternate frequency planning can potentially minimimize the signal leakage. One

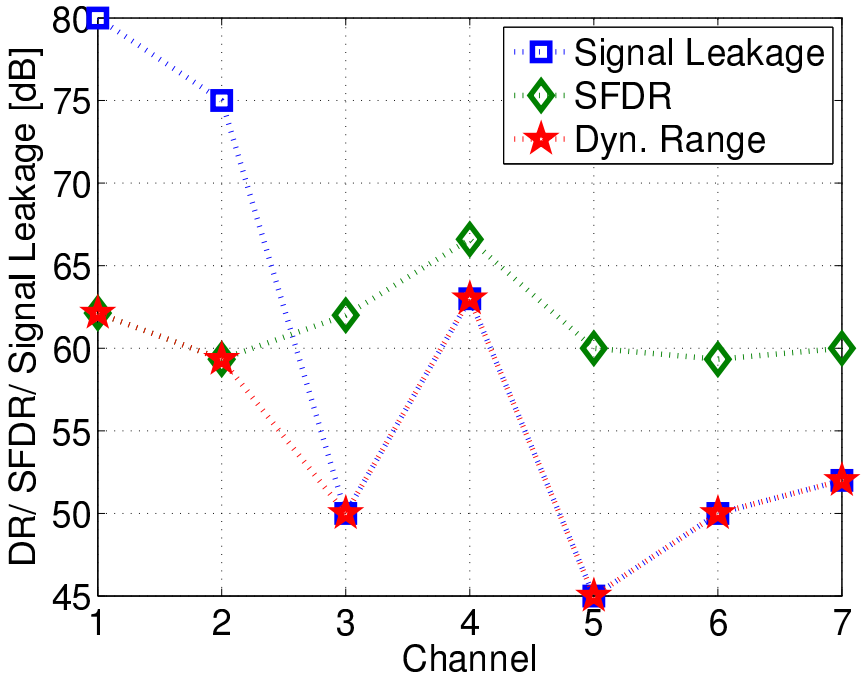


Figure 7.1: Dynamic range of the RF channelizer.

possible architecture is shown in Fig. 7.2. It has to be noted that the LOs are harmonically related. This presents opportunity for innovative PLL architectures that can switch from one LO to another rapidly, if not, generate them simultaneously.

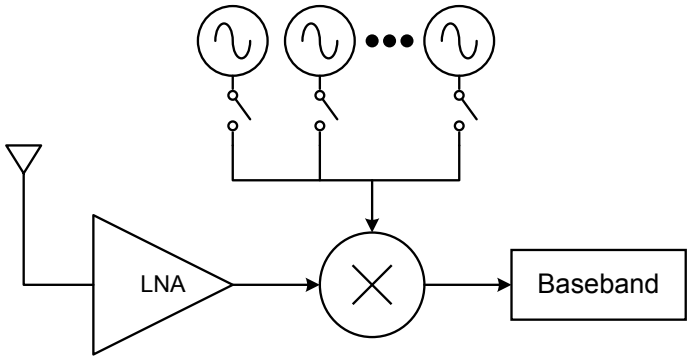


Figure 7.2: Alternate channelizer architecture with only one mixer in the signal path.

- Fig. 7.3 shows the operating principle of the harmonic rejection mixer demonstrated in chapter 4. For proof-of-concept measurements, tuning of the gains and LO phases was performed manually. There is a need for an automatic tuning mechanism is required for operation in a real application.

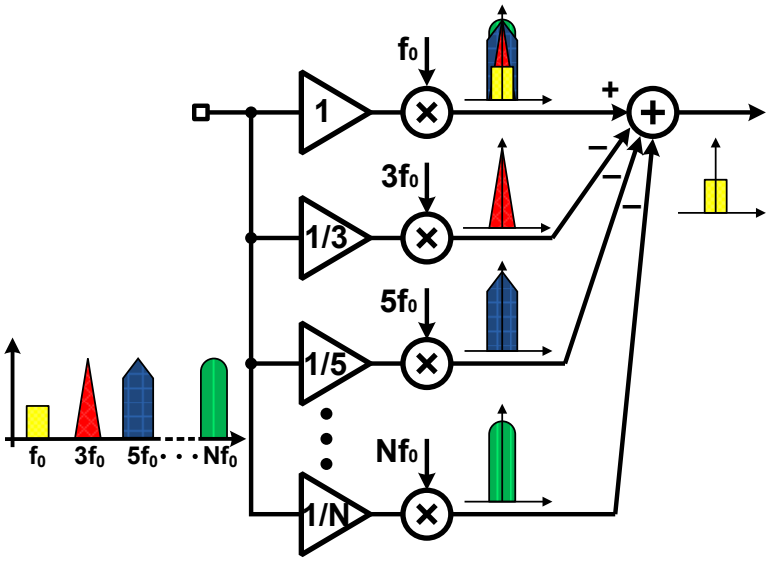


Figure 7.3: Operating principle of the proposed HRM.

The mixer requires harmonically related LO frequencies. $3 \times f_{LO}$, $5 \times f_{LO}$, ..., etc,

to be generated. This provides opportunity for innovation in low-power frequency synthesis circuits.

Investigation in these research topics would enable rapid spectrum analysis of a wide bandwidth with a higher dynamic range.

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