Design Techniques for Analog-to-Digital Converters in Scaled CMOS Technologies

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Abstract

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Analog-to-digital converters (ADCs) are analog pre-processing systems that convert the real life analog signals, the input of sensors or antenna, to digital bits that are processed by the system digital back-end. Due to the various issues associated with CMOS technology scaling such as reduced signal swings and lower transistor gains, the design of ADCs has seen a number of challenges in medium to high resolution and wideband digitization applications. The various chapters of this thesis focus on efficient design techniques for ADCs that aim to address the challenges associated with design in scaled CMOS technologies.

This thesis discusses the design of three analog and mixed-signal prototypes: the first prototype introduces current pre-charging (CRP) techniques to generate the reference in Multiplying Digital-to-Analog Converters (MDACs) of pipeline ADCs. CRP techniques are specifically applied to Zero-Crossing Based (ZCB) Pipeline-SAR ADCs in this work. The proposed reference pre-charge technique relaxes power and area requirements for reference voltage generation and distribution in ZCB Pipeline ADCs, by eliminating power hungry low impedance reference voltage buffers. The next prototype describes the design of a radiation-hard dual-channel 12-bit 40MS/s pipeline ADC

with extended dynamic range, for use in the readout electronics upgrade for the ATLAS Liquid Argon Calorimeters at the CERN Large Hadron Collider. The design consists of two pipeline A/D channels with four MDACs with nominal 12-bit resolution each, that are verified to be radiation-hard beyond the required specifications.

The final prototype proposes Switched-Mode Signal Processing, a new design paradigm that achieves rail-to-rail signal swings with high linearity at ultra-low supply voltages. Switched-Mode Signal Processing represents analog information in terms of pulse widths and replaces the output stage of OTAs with power-efficient rail-to-rail Class-D stages, thus producing Switched-Mode Operational Amplifiers (SMOAs). The SMOAs are used to implement a Programmable Gain Amplifier (PGA) that has a programmable gain from 0-12dB.

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Chapter 1

Introduction

This chapter provides a brief overview of CMOS technology scaling and the associated issues for analog and mixed-signal design. The need for analog-to-digital converters (ADCs) is briefly discussed followed by a general discussion on the design of Pipeline ADCs. Recent advances in Pipeline ADC design are discussed to provide a suitable context for the rest of the thesis.

1.1 CMOS Technology Scaling

Constant CMOS technology scaling in recent years towards finer device geometries has led to the development of very complex integrated systems. The International Technology Roadmap for Semiconductors (ITRS) forecasts that by the year 2021, CMOS gate lengths would have scaled down to 10nm. Fig. 1.1 and Fig. 1.2 show the ITRS projection for the scaling of the transistor gate length L_g and the intrinsic switching frequency with time [1] for two flavors of transistors for analog and mixed-signal applications . Technology scaling scaling in general leads to faster and

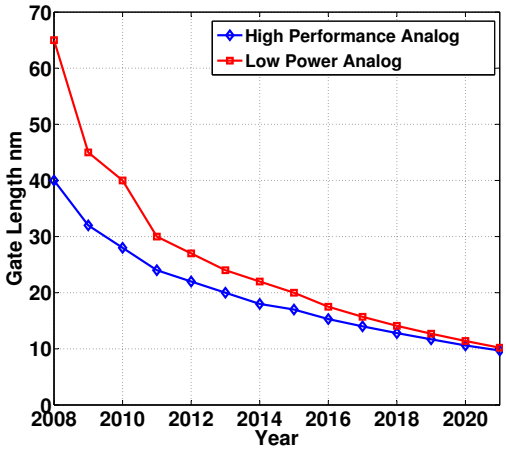

Figure 1.1: ITRS scaling roadmap for transistor gate length L_g.

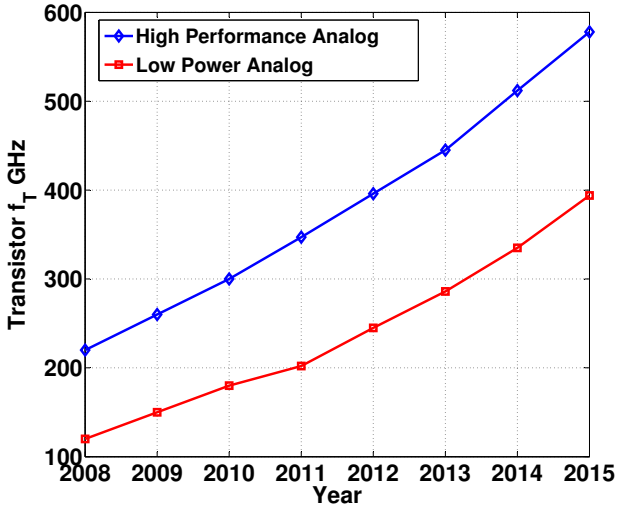

Figure 1.2: ITRS scaling roadmap for transistor f_T.

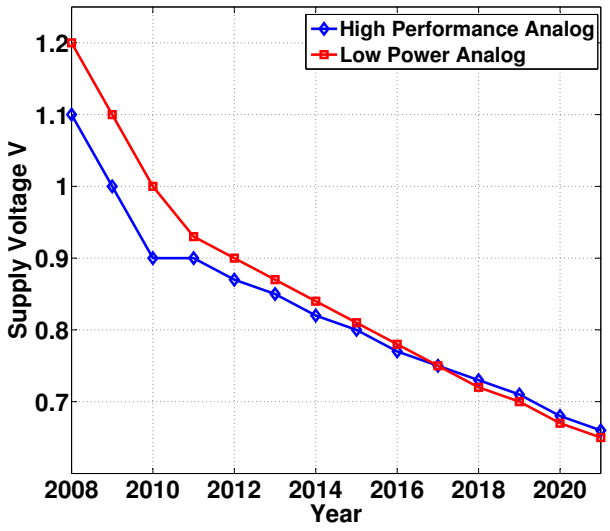

Figure 1.3: ITRS scaling roadmap for device supply voltage V_{DD}

smaller transistors but also increases device leakage due to gate-oxide tunneling, drain leakage etc. Hence, different flavors of devices are available for different applications. High Performance (HP) devices are typically used in applications where speed and performance are critical. For mobile devices, where power consumption is of prime importance, Low Power (LP) transistors are used.

Device scaling with technology greatly benefits digital circuits. As the devices becomes smaller, due to the higher switching frequency, the devices can operate faster. Smaller devices results in smaller device parasitic capacitances and hence a lower power consumption and also result in smaller die area, thus bringing the cost down. As device dimensions scale, in order for the gate terminal to retain control over the MOS channel, the gate oxide thickness also needs to scale. Thus, in order to guarantee reliability of the gate oxide against breakdown, there is also a steady scaling of the power supply. Analog and mixed-signal (AMS) circuits, on the other hand, face a number of challenges as a result of technology scaling. The shrinking power supply reduces the maximum available signal swing in AMS circuits, thus reducing the maximum achievable signal-to-noise ra-

tio [2]. Currently, noise margins are not yet an issue in digital circuits but play a critical role in the performance of AMS circuits. Fig. 1.3 shows the scaling of the device power supply in analog circuits.

AMS design relies on the use of negative feedback around amplifiers with large non-linear gains. The constant gate length scaling reduces the transistor intrinsic gain in scaled CMOS technologies, due to drain induced barrier lowering (DIBL). This in turn makes it very hard to achieve large gains with amplifiers designed in scaled CMOS technologies. The shrinking voltage supply also reduces the available device headroom, thus making it infeasible to achieve large gains by device stacking. As a result of various challenges faced by AMS designs in scaled CMOS technologies, such designs are typically done in older CMOS technologies with higher supply voltages.

In System-on-Package (SOP) designs, it is sometimes impractical, from a cost point of view, to have analog and digital dies fabricated in different technology nodes. Since the digital portions overwhelm the analog portions in terms of area, the analog circuits must be designed in the same technology node as their digital counterparts. Thus, the design of AMS circuits in scaled technologies requires a number of innovative techniques to overcome scaling challenges.

1.2 Analog-to-Digital Converters (ADCs)

Most real world signals of interest are analog in nature. The outputs of many sensors, like sound, light, pressure etc. are all analog in nature. Analog-to-digital converters (ADCs) are analog preprocessing systems that convert the real life analog signals, the input of sensors or antenna, to

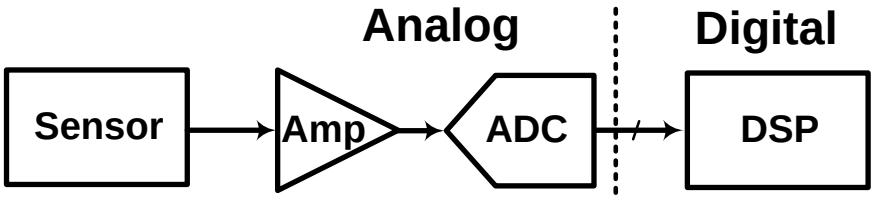

Figure 1.4: Block diagram of a signal processing chain.

digital bits that can processed by the powerful digital back-ends that are made possible by technology scaling.

Fig. 1.4 shows the setup of a general signal processing chain. The signal output from the sensor, which is analog in nature, is first conditioned by an analog pre-processor (Amp) which performs amplification and filtering of the input signal. The analog pre-processor then drives an ADC that performs analog-to-digital conversion. The digital bits output by the ADC are then fed to the digital signal processor (DSP) for further processing. It should be noted that a majority of the blocks in Fig. 1.4 are analog in nature. The rest of this section will describe a type of ADC called Pipeline ADCs which is the focus of interest of the next two chapters of this thesis.

1.3 Pipeline ADCs

Pipeline ADCs are popular choices for medium to high resolution applications for sampling rates from 100MHz to a few GHz. Pipeline ADCs, as the name suggests, consists of a number of pipelined stages in series. Each pipeline stage is called a multiplying digital-to-analog converter (MDACs). Fig. 1.5 shows the block diagram of a typical 1.5-bit/stage Pipeline ADC [3], along with the timing diagram and the residue characteristic. The 1.5-bit/stage architecture provides digital redundancy that relaxes the requirement of the subADC. Each ADC stage, known as an

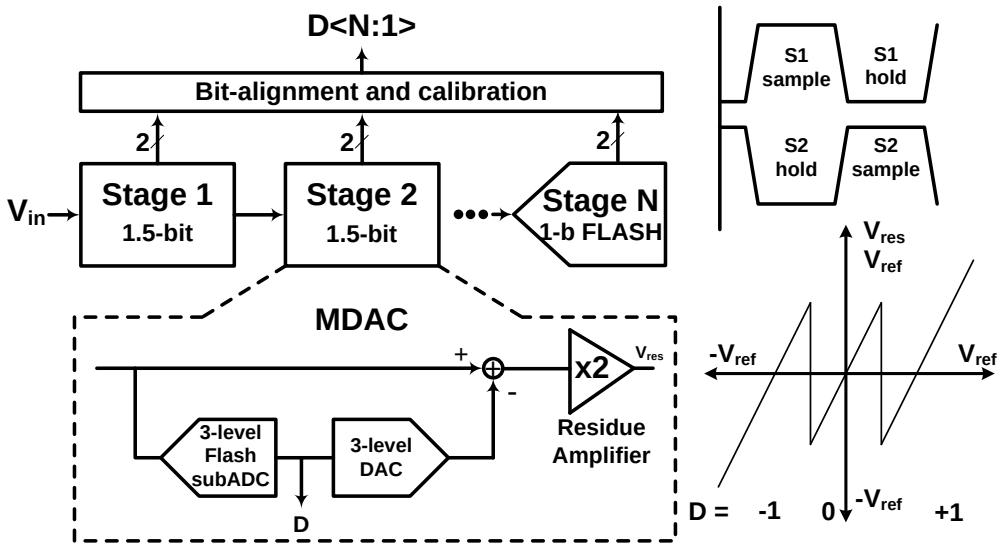

Figure 1.5: Block diagram of a 1.5-bit/stage Pipeline ADC.

MDAC, consists of an input sampling network, a 3-level flash subADC, a 3-level DAC (digital-to-analog converter) and a residue amplifier. The input signal is coarsely quantized by the subADC, subtracted with the DAC output, amplified by the residue amplifier and sent to the next stage for further quantization. Each MDAC outputs a certain number of bits which are then aligned to give the final digital word.

In any pipeline ADC, the signal ripples through the MDAC stages, and hence there is inherent latency in the digital word. The accuracy requirements of the pipeline MDACs relax as the signal propagates down the chain, with the 1^{st} MDAC stage being the most critical for the ADC noise and distortion performance. Typically, the residue amplifier consumes the majority of the power in the MDAC.

Fig. 1.6 shows a typical implementation of a 1.5-bit MDAC stage. The residue amplifier is typically implemented by a high-gain operational trans-conductance amplifier (OTA). The input differential signal V_{inp}, V_{inn} is sampled across the sampling capacitors C_1, C_2 during the sampling

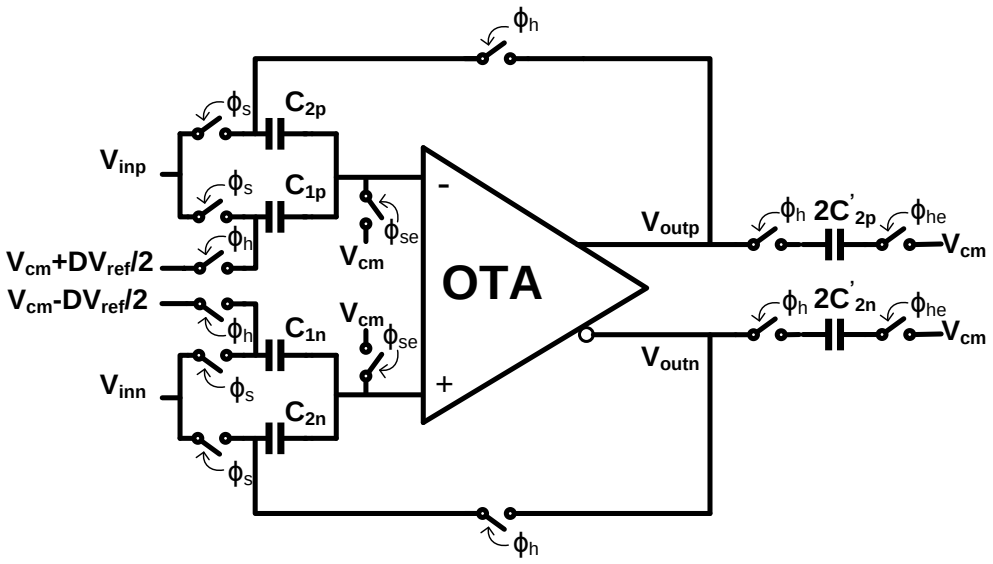

Figure 1.6: Typical implementation of a 1.5-bit MDAC stage.

phase ϕ_s. During the hold phase ϕ_h, based on the subADC decision D, the capacitors C_{1p}, C_{1n} are pulled to either $\pm V_{ref}, 0$ to implement the stage transfer characteristic $V_{res} = G(V_{in} + DV_{ref}/2), D = 0, \pm 1$, and G is the MDAC gain which is ideally 2. The 1^{st} MDAC stage has the most stringent noise and linearity requirements in a Pipeline ADC, as the noise and distortion added by the latter stages are attenuated by the 1^{st} stage gain when input-referred.

To determine the requirements on the OTA in Fig. 1.6, consider the design of a $N = 14 - bit$ MADC stage, with the sampling frequency $F_s = 50MHz$. The kT/C sampling noise requirements dictate that $C_1 = C_2 = 2.5pF$. In order for the MDAC gain G to be 14-bit accurate, the open-loop DC gain of the OTA should be $>$ 84dB. In scaled CMOS technologies, it is very challenging to obtain a DC gain of 84dB from a single-stage OTA design. In practice, achieving such a high DC gain would require the use of 3-stage OTA designs, which in turn brings in other factors like OTA stability, compensation etc.

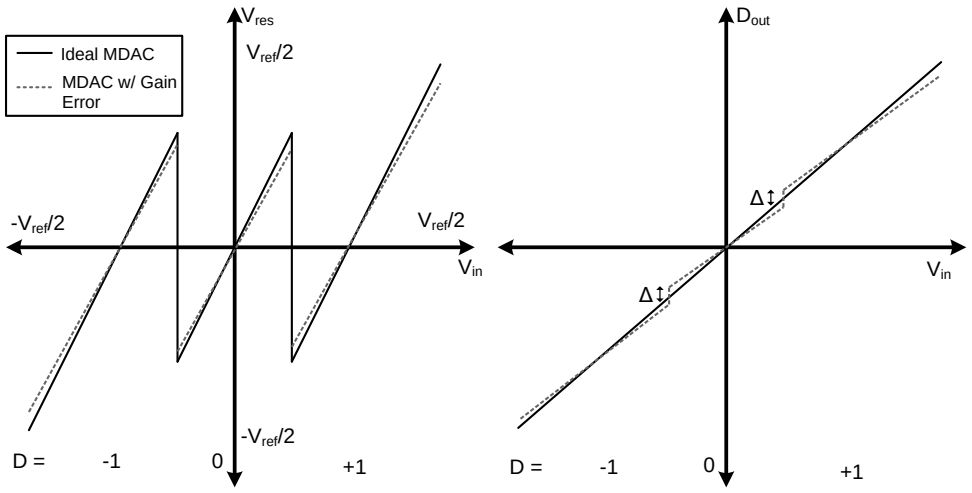

Figure 1.7: MDAC residue characteristic (left). Reconstructed output (right); V_{ref} - reference voltage; V_{res} - residue voltage; D - subADC decision; D_{out} - reconstructed output.

1.3.1 Digital Calibration

The gain G of the MDAC is determined to a large extent by the ratio of the sampling capacitors. For high-resolution ADCs, the matching requirements on the capacitors can become very stringent. Any mismatch between the capacitors causes the MDAC gain G to be different from its ideal value, leading to code jumps in the ADC transfer curve. But since capacitor mismatch is static in nature, it can be corrected by foreground digital calibration techniques by exploiting the redundancy inherent in MDAC architectures [3].

Fig. 1.7 shows the residue output V_{res} of the Stage 1 MDAC and the reconstructed output D_{out}, as a function of the input V_{in}, for an ideal MDAC and for an MDAC with gain error. Gain errors due to capacitor mismatch give rise to code jumps in the reconstructed output, as shown in Figure 1.7. The calibration algorithm consists of measuring the MDAC code jumps Δ by subsequent ADC

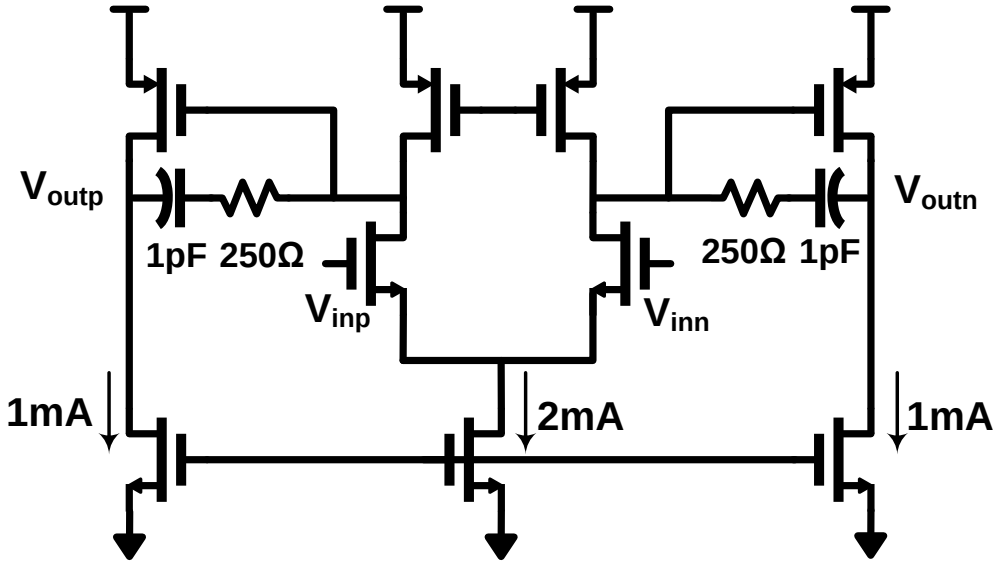

Figure 1.8: 2-stage Miller OTA.

stages and removing them digitally from the reconstructed digital output D_{out}. The calibration procedure starts with the last MDAC stage and moves backward to calibrate the Stage 1 MDAC.

Although it is true that digital calibration can also correct for finite OTA DC gain, it should be noted that capacitor mismatch is static in nature and does not vary with PVT (process, temperature and voltage). OTA DC gain on the other hand has a PVT dependence, thus the MDAC requires recalibration for every PVT change. In reality, depending on the application, it may be possible to perform periodic foreground digital calibration on the MDAC to correct for PVT induced drifts.

1.3.2 Challenges in OTA Implementation in Scaled-CMOS Technologies

As CMOS technology scales, it was seen in section 1.1 that the device operating supply voltage and intrinsic gain also reduce, thus making it much harder to design amplifiers with high signal swings and high DC gains. Consider the design of a 2-stage Miller-OTA to implement the residue

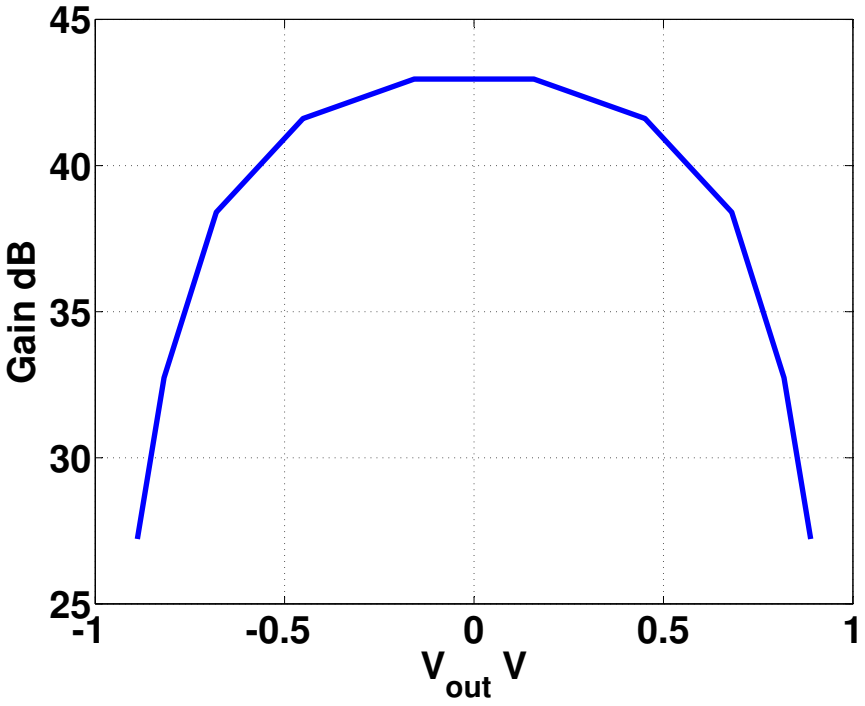

Figure 1.9: OTA gain vs. output voltage illustrating gain compression.

amplifier for the MDAC shown in Fig. 1.6. Assume that the MDAC is to be designed for 13-bit resolution, which sets the stage 1 sampling capacitors $C_1 = C_2 = 0.75pF$, and the 2^{nd} MDAC stage capacitance is 0.75pF. For the Miller-OTA shown in Fig. 1.8, the total load capacitance seen during the hold phase is close to 1pF. For simplicity, the compensating capacitor is also chosen to be 1pF. In a 65nm CMOS technology, the Miller-OTA of Fig. 1.8 can be designed to achieve a DC gain of only 43dB, with a unity gain bandwidth of 2.5GHz while burning 4mW from a 1.2V supply.

In scaled CMOS technologies, the lack of device voltage headroom limits the maximum achievable signal swing. To illustrate this point, Fig. 1.9 shows the open-loop DC gain of the Miller OTA as a function of its output swing V_{out}. Due to the lack of voltage headroom, it can be seen that the

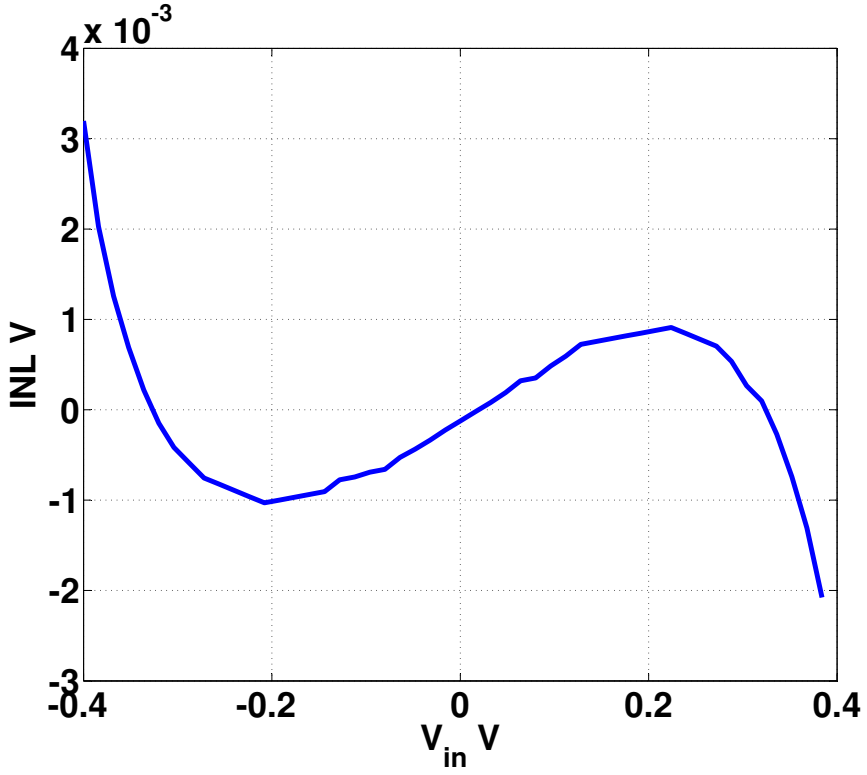

Figure 1.10: INL of the MDAC in Fig. 1.6 with the Miller OTA of Fig. 1.8.

OTA gain compresses with large V_{out}, dropping as low as 28dB. This in turn leads to a poor INL performance when the Miller OTA is used in the MDAC of Fig. 1.6.

Fig. 1.10 shows the INL (integral non-linearity) as a function of the input voltage V_{in} for the MDAC of Fig. 1.6. It can be seen that for an ADC full-scale range of 2.4V, the MDAC is only 9-bit accurate, as seen in Fig. 1.10.

1.4 Recent Advances in MDAC Residue Amplification

As shown in Fig. 1.9 and Fig. 1.10, the performance of classical OTA-based MDACs is severely limited by the limited available voltage headroom in scaled CMOS technologies. A number of

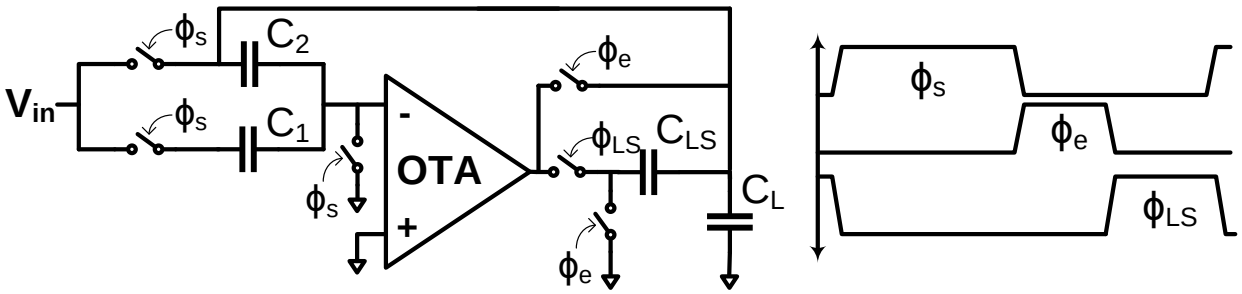

Figure 1.11: Correlated level shifting applied to a typical 1-bit/stage MDAC.

advances have been made in recent times to improve the efficient and performance of the residue amplifier in Pipeline ADCs. This section briefly reviews two such recent techniques that improve the MDACresidue amplifier performance in scaled CMOS technologies.

1.4.1 Correlated Level Shifting

Correlated level shifting [4] is a general switched-capacitor technique that greatly relaxes the output swing requirements of OTAs in scaled CMOS technologies, allowing the amplifier to achieve high gain and close to rail signal-swings. Techniques combining CLS OTAs with other residue amplification techniques have also been reported in literature [5].

Fig. 1.11 shows correlated level shifting applied to a typical 1-bit/stage MDAC. A single-ended version is shown for simplicity. During the sample phase ϕ_s, the input V_{in} is sampled across the capacitors C_1 and C_2. The residue amplification phase is split in two: a coarse estimation phase ϕ_e and a level shift phase ϕ_{LS}.

Fig. 1.12 shows the MDAC redrawn during the estimation phase and the level shift phase. During the estimation phase ϕ_e, a coarse value of the final output voltage of the MDAC V_{out} is stored on the level shifting capacitor C_{LS}. During the level shift phase ϕ_{LS}, the level shifting

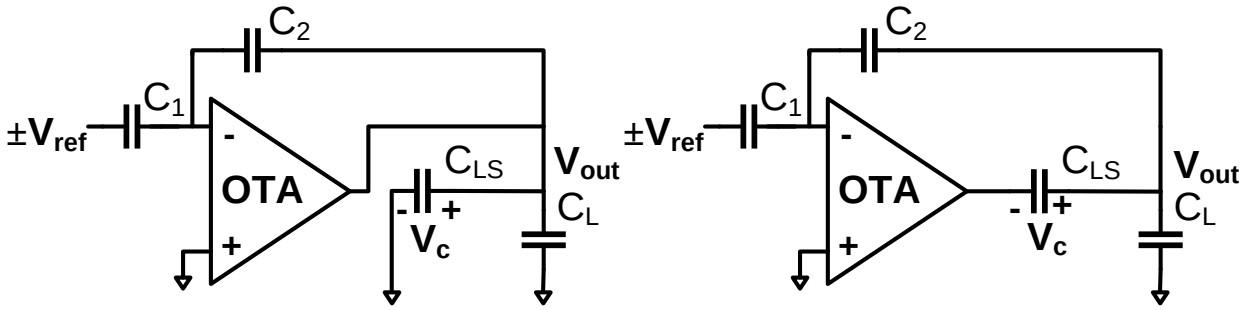

Figure 1.12: CLS-MDAC redrawn during: (left) Estimation phase ϕ_e; (right) Level shift phase ϕ_{LS}.

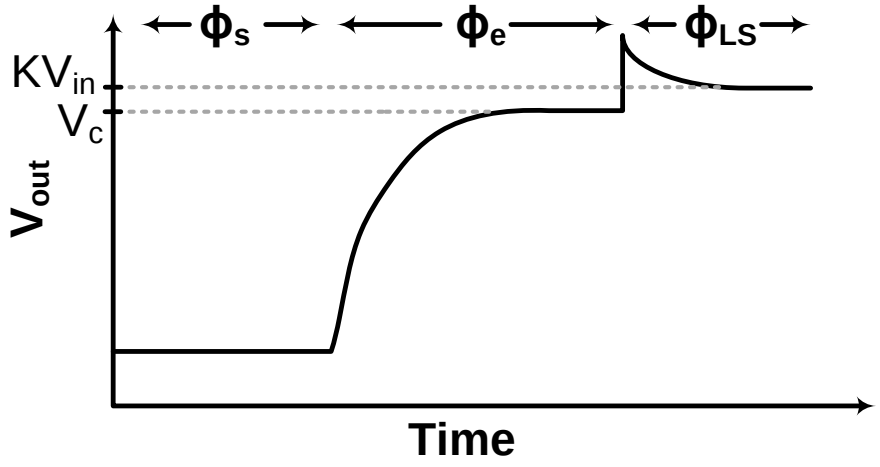

Figure 1.13: Waveform at the MDAC output V_{out}.

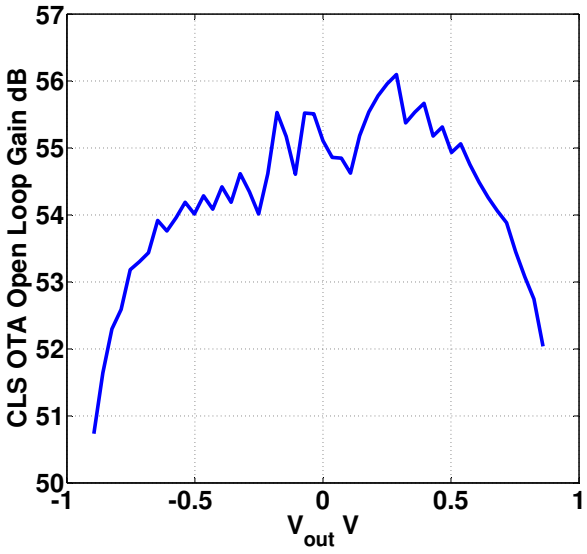

Figure 1.14: CLS OTA loop gain.

capacitor is connected in series between the OTA output and the load capacitor, as shown. The level-shift capacitor acts as a voltage source in series with the output of the OTA. As a result, the OTA output jumps to V_{cm}, thus eliminating the need for any signal swing. Fig. 1.13 shows the voltage waveform at the output of the MDAC. The MDAC output finally settles to KV_{in}, where K is the gain of the MDAC $K = (C_1 + C_2)/C_2$.

To illustrate the benefits of CLS, the MDAC of Fig.1.6 was implemented with the Miller OTA (Fig. 1.8) with CLS applied to it. Fig. 1.14 shows the loop gain of the CLS OTA as a function of the MADC output swing. It can be seen that the CLS OTA maintains a high loop gain for a close-to-rail output swing. Fig. 1.15 shows the INL of the MDAC as a function of the input voltage. It can be seen that the MDAC with the CLS OTA has a 4x improvement in the INL, besides having a larger output swing.

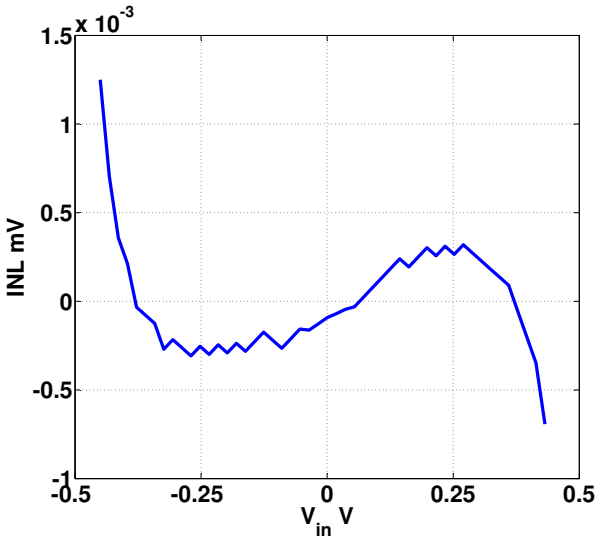

Figure 1.15: CLS OTA INL.

1.4.2 Zero-Crossing Based (ZCB) Circuits

ZCB circuits [6–9] are based on the fact that in any MDAC, charge transfer is complete when the input of the residue amplifier, at the end of the charge transfer phase, is at the common-mode voltage. ZCB circuits force this condition by replacing the residue amplifier by a continuous-time comparator and power-efficient current sources.

Fig. 1.16 shows the simplified implementation of a 1-bit/stage ZCB MDAC, along with the timing diagram. The residue amplifier in the ZCB MDAC is replaced by a continuous-time comparator and a current source. During the sample phase ϕ_s, the input V_{in} is sampled across the capacitors C_1 and C_2. At the start of the hold phase ϕ_h, a short pre-charge phase ϕ_p pulls the MDAC output to GND, since the ZCB MDAC outputs are uni-directional. The current source I_p charges the output V_{out} from GND, while the zero-crossing detector (ZCD), a continuous-time comparator, monitors

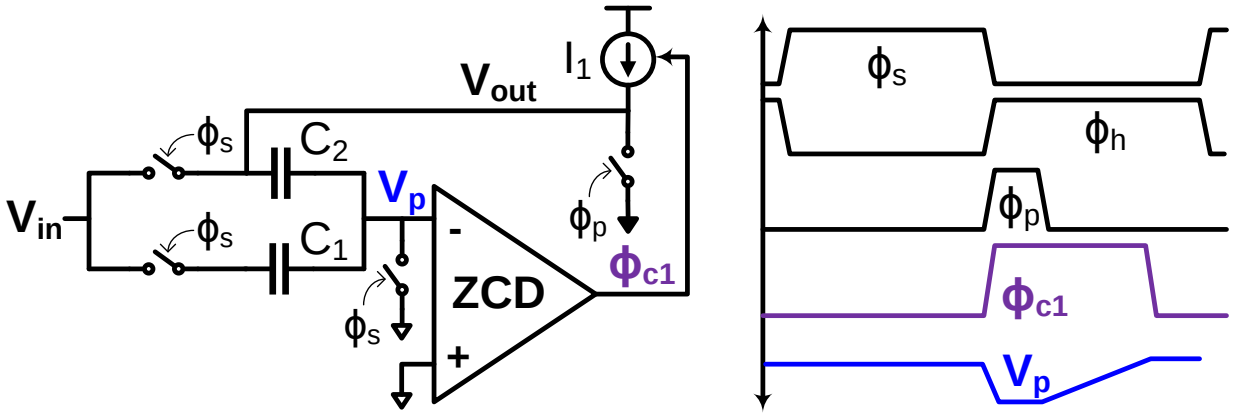

Figure 1.16: 1-bit/stage ZCB MDAC.

the node V_p. As soon as V_p crosses the common-mode voltage, the ZCD shuts off the output current source, after a certain delay T_{ZCD}, and thus charge transfer is completed.

ZCB circuits have a number of advantages. ZCB circuits have no stability issues unlike OTA-based MDACs. Also, the charge transfer mechanism is very efficient since all the power drawn by the output current sources is used for signal-path charging. The linearity of the ZCB MDACs depends on the output current being constant during the ZCD delay period T_{ZCD}. A number of techniques like dual-ramps technique [6], regulated cascode current sources [10] etc. can be implemented to improve MDAC linearity performance and will not be discussed further in this thesis.

1.5 Thesis Organization

The rest of the thesis is organized as follows: Chapter 2 introduces current pre-charging (CRP) techniques to generate the reference in MDACs of pipeline ADCs. CRP techniques are specifically applied to Zero-Crossing Based (ZCB) Pipeline-SAR ADCs in this work. The proposed reference

pre-charge technique relaxes power and area requirements for reference voltage generation and distribution in ZCB Pipeline ADCs, by eliminating power hungry low impedance reference voltage buffers. Dynamic Reference Loading (DRL), a variant of current reference pre-charging, is further proposed to reduce the loading due to the reference capacitors leading to improvements in the ADC noise performance. Two proof of principle reference pre-charged CRL/DRL ZCB Pipelined-SAR ADCs, implemented in 65nm CMOS, show an SFDR/SNR/SNDR 70dB/60.5dB/59.5dB at 18MHz and SFDR/SNR/SNDR of 77dB/70dB/66dB at 25MHz respectively, while consuming 4.5mW at 40MS/s and 4.8mW at 50MS/s for an FOM of 141fJ/step and 57fJ/step respectively. The ADCs do not require any additional power and/or area for reference voltage generation and distribution.

Chapter 3 describes the design of a radiation-hard dual-channel 12-bit 40MS/s pipeline ADC with extended dynamic range, for use in the readout electronics upgrade for the ATLAS Liquid Argon Calorimeters at the CERN Large Hadron Collider. The design consists of two pipeline A/D channels with four Multiplying Digital-to-Analog Converters with nominal 12-bit resolution each. The design, fabricated in the IBM 130 nm CMOS process, shows a performance of 68 dB SNDR at 18 MHz for a single channel at 40 MS/s while consuming 55 mW/channel from a 2.5 V supply, and exhibits no performance degradation after irradiation. Various gain selection algorithms to achieve the extended dynamic range are implemented and tested.

Chapter 4 introduces Switched-Mode Signal Processing, a new design paradigm that achieves rail-to-rail signal swings with high linearity at ultra-low supply voltages. Switched-Mode Signal Processing represents analog information in terms of pulse widths and replaces the output stage of OTAs with power-efficient rail-to-rail Class-D stages, thus producing Switched-Mode Operational

Amplifiers (SMOAs). The SMOAs are used to implement a Programmable Gain Amplifier (PGA) that has a programmable gain from 0-12dB, a peak SNR, SNDR and dynamic range of 55dB, 50dB and 69dB at an input full-scale of +4dBm (80% of the supply at 0.6V), while dissipating 6.6mW from a 0.6V supply.

Chapter 5 summarizes the thesis contributions and provides avenues for future work and improvement.

Chapter 2

Current Reference Pre-charging for Zero-Crossing based Pipelined ADCs

This chapter describes current pre-charging techniques to generate the reference in MDACs of pipeline ADCs. They are specifically applied to Zero-Crossing Based (ZCB) Pipeline-SAR ADCs in this work. The proposed reference pre-charge technique relaxes power and area requirements for reference voltage generation and distribution in ZCB Pipeline ADCs, by eliminating power hungry low impedance reference voltage buffers. Dynamic Reference Loading (DRL), a variant of current reference pre-charging, is further proposed to reduce the loading due to the reference capacitors leading to improvements in the ADC noise performance. A proof of principle reference pre-charged DRL ZCB Pipelined-SAR ADC, implemented in 65nm CMOS, shows an SFDR/SNR/SNDR of 77dB/70dB/66dB at 25MHz, while consuming 4.8mW at 50MS/s for an

FOM of 57fJ/step. The ADC does not require any additional power and/or area for reference voltage generation and distribution.

2.1 Background

Recent research focus in Pipeline ADCs has led to a number of power-efficient techniques for performing residue amplification [6–9, 11]. This has led to a constant improvement in the Nyquist Figure of Merit (FOM) [12] to well below 100fJ/step [13]. Although much emphasis has been on making the residue amplification lower power, there has been little or no attention on improving the power efficiency of blocks providing the inputs to the pipeline ADC i.e. the input signal and the reference voltage. The reference voltage is one of the three inputs to the ADC (along with the clock and the input signal) and its accuracy directly affects the ADC accuracy. Power hungry reference voltage buffers [14–16] have long been the traditional solution to providing accurate reference voltages to the ADC. However, the power-efficient implementation of the reference buffer is critical to realizing truly low power ADCs.

Zero-crossing based (ZCB) circuits [7–9] have recently emerged as low-power alternatives to traditional OTA-based (Operational Transconductor Amplifier) MDACs, replacing the power-hungry OTA with power-efficient current sources and a continuous-time comparator. Due to the absence of loop stability issues and gain-bandwidth trade-offs, ZCB circuits offer a lot of potential to achieve very low power ADC implementations with technology scaling. However, the reference buffer design in ZCB MDACs is even more complicated than in OTA-based MDACs, as the buffer

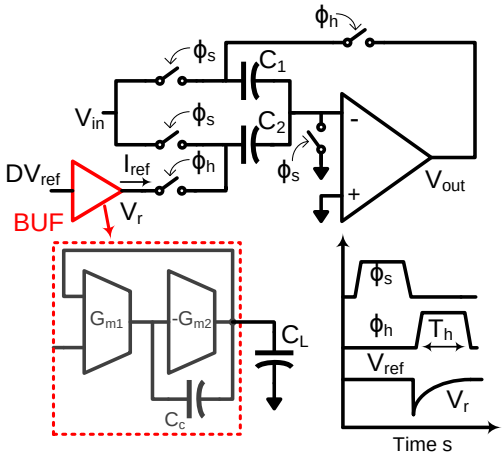

Figure 2.1: Circuit implementation of a typical 1-bit MDAC stage [3] with the timing diagram.

has only a fraction of the hold phase to settle to the desired accuracy. In addition, inter-stage reference noise coupling makes the reference voltage buffer requirements more stringent [10].

Reference buffers can consume a significant amount of power in typical ADC realizations: e.g. 6.2mW in [14], 4mW in [15] and 4.8mW in [16], and hence reducing the power consumption of the reference path can significantly improve the overall ADC efficiency.

The rest of the paper is organized as follows: Section 2.2 looks at the implementation challenges for voltage reference buffers in conventional OTA-based MDACs and additional reference path issues in ZCB MDACs. Section 2.3 introduces the proposed Current Reference Pre-charge (CRP) and the Dynamic Reference Loading (DRL) techniques [17]. Sections 2.4 and 2.5 discuss the ADC implementation details and the measurement results respectively.

2.2 Implementation Challenges for Voltage Reference Buffers

2.2.1 Voltage Reference Buffers for OTA-based MDACs

In order to derive the requirements on the reference buffer for OTA-based MDACs, consider the simplified single-ended version of a conventional 1-bit/stage Multiplying Digital-to-Analog Converter (MDAC) (see e.g., [3]), shown in Fig. 2.1, along with a possible implementation of the reference buffer BUF and the timing diagram. The input V_{in} is sampled onto the capacitors C_1 and C_2 during the sample phase ϕ_s. During the hold phase ϕ_h, which lasts for a duration T_h, depending on the subADC decision $D = \pm 1$, one of the plates of C_2 is pulled to $\pm V_{ref}$, thus performing the MDAC operation given by $V_{out} = KV_{in} + DV_{ref}$, where $K = (C_1 + C_2)/C_1$. The charge drawn from the reference buffer BUF at the end of ϕ_h is signal dependent and is given by $C_2|V_{in} - V_{ref}|$. The time-averaged (low frequency) current $\bar{I}_{ref}$ drawn from the reference buffer BUF is also signal dependent and its maximum value[1] is given by

$$\bar{I}_{ref,max} = \frac{V_{ref}C_2}{T_h}. \tag{2.1}$$

The signal-dependent DC voltage drop across the reference buffer must satisfy $|V_{ref} - \bar{V}_r| < V_{LSB}/4$, where $\bar{V}_r$ is the time-averaged reference buffer output voltage, $V_{LSB} = 2V_{ref}/2^N$ and N is the ADC resolution. Thus, the reference buffer (low frequency) output impedance has an upper bound given by

$$\bar{R}_{ref,op} < \frac{V_{LSB}}{4I_{ref,max}}. \tag{2.2}$$

[1]The minimum value of the current is 0.

For N = 12-bits, T_h = 10ns (F_s = 50MHz) and $V_{ref} = \pm 0.45$V (150mV headroom on a ± 0.6V supply, single-ended), kT/C requirements set $C_1 = C_2$ = 1pF and we obtain

$$\bar{R}_{ref,op} < 1.2\Omega. \tag{2.3}$$

The impedance given by (2.2) represents the upper bound on the low frequency output impedance of the reference buffer. In addition, the reference path should also provide dynamic (high frequency) currents to charge the capacitors within the hold period. There are two solutions that can be used to satisfy these requirements:

1. **Active Solution**: Using a strong reference voltage buffer. The need for a very small low frequency output impedance necessitates the use of a two-stage amplifier. One possible implementation of the reference buffer, using a 2-stage Miller-OTA in unity feedback, is shown in Fig. 2.1. C_L is the capacitor load to be driven by the reference buffer, which in this case is C_2 = 1pF, and C_c is the Miller compensating capacitor, chosen to also be 1pF (for simplicity). For the reference voltage V_{ref} to settle to within $V_{LSB}/4$ within the hold period (10ns), the reference buffer needs a closed-loop bandwidth of 300MHz. For a phase-margin of 60°, this requires G_{m1} = 2mS and G_{m2} = 4.2mS. Assuming a G_m/I ratio of 10, this requires a bias current of 400μA in G_{m1} (G_{m1} is differential) and 420μA in G_{m2}. Thus, the reference buffer, in this simple example, can consume close to 1mW. In practice, other MDAC stages of the pipeline also load the reference buffer (i.e. C_L is larger than 1pF) and with design margin, the reference buffer can consume a significant portion of the ADC core power , e.g., reference buffers consume 6.2mW in [14], 4mW in [15] and 4.8mW in [16].

2. **Passive Solution**: Using large reference decoupling capacitors. A weak, low bandwidth reference buffer is used in this case to provide the small low frequency output impedance required by (2.2) and the dynamic current drawn by C_2 during the hold period is provided by on-chip or off-chip decoupling capacitors or a combination of the two. On-chip decoupling capacitors can consume a large chip area. Off-chip decoupling capacitors are feasible at low sampling rates, but their performance is limited at high sampling rates due to the bondwire inductance. In ZCB Pipeline ADCs, inter-stage reference coupling ([10] and explained in Section 2.2.2) limits the performance of off-chip decoupling capacitors (due to the bondwire inductance) even at low sampling rates, and hence requires the use of large *on-chip* decoupling capacitors, which consume large on-chip area, e.g., the design in [9] requires 1nF of on-chip decoupling capacitance.

2.2.2 Additional Reference Path Issues in ZCB designs

ZCB designs suffer from more stringent settling requirements on the reference buffer than OTA-based designs. The first issue is that the amount of time available for reference settling in ZCB designs is only a fraction of the hold phase ϕ_h (known as the pre-charge phase which is typically 20% of the hold phase). This makes the required reference buffer output impedance, given by (2.2), five times more stringent.

The second, more serious, issue in ZCB MDAC designs is inter-stage reference noise coupling. In OTA-based designs, the current injected into the reference voltage gradually goes to zero at the end of the hold phase, when the charge transfer is completed. But in ZCB circuits, the current

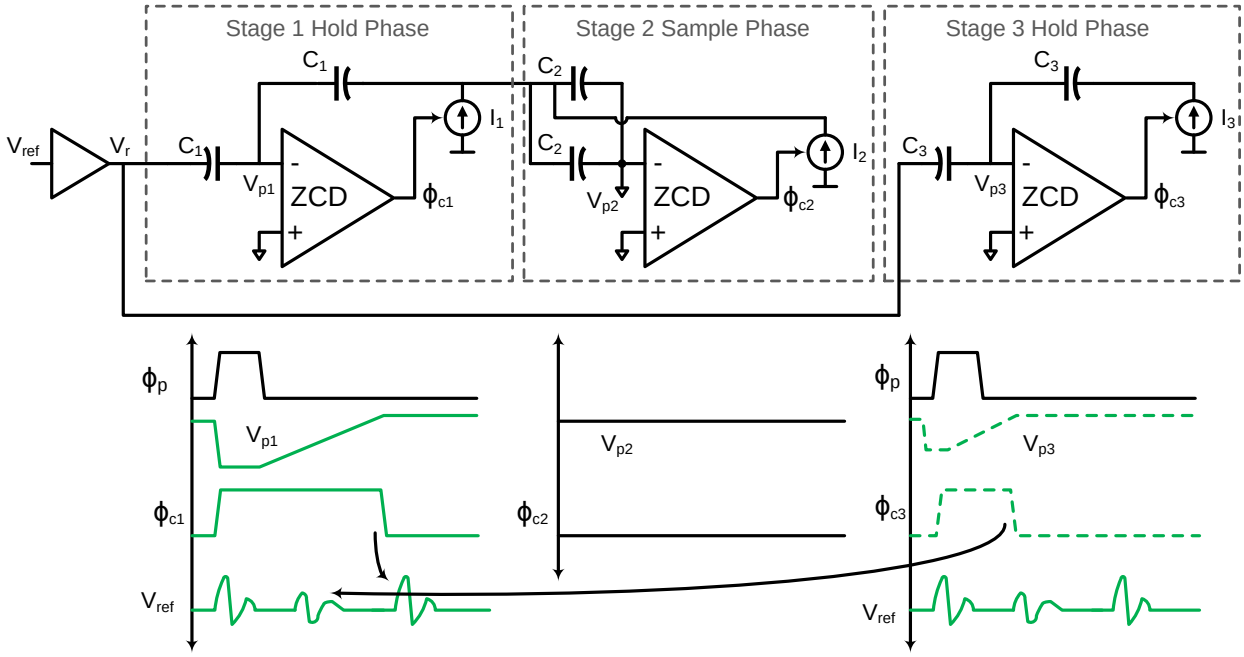

Figure 2.2: Inter-stage reference noise coupling in ZCB MDAC designs, here illustrated between Stage I and Stage III, further increases the reference buffer requirements.

instantaneously drops from a constant value, when the stage output current sources are on, to zero when the zero-crossing event T_{ZCD} is detected. Since T_{ZCD} is signal-dependent, this sudden current injection leads to a signal-dependent disturbance on the reference voltage due to the lower order stages, since the reference voltage is shared among all MDAC stages. This is shown graphically in Fig. 2.2, where three ZCB MDAC stages are shown for simplicity. The signal dependent zero-crossing event of the Stage III MDAC injects noise into the reference voltage and this affects the accuracy of charge transfer of the first MDAC Stage, in particular when the Stage III zero-crossing event occurs just before that of Stage I. The short time scales over which this noise injection happens (few 100s of ps) complicates the reference buffer design further in both ZCB Pipeline and ZCB Pipeline-SAR ADCs.

It is clear from these discussions that a low power reference path is critical to realize the true low power potential offered by ZCB circuits.

2.3 Low Power Current Reference Pre-charging Techniques

In order to address the issues associated with the reference path, we introduce Current Reference Pre-charging (CRP) [18]. It makes the reference path independent of the signal path and replaces power-hungry reference voltage buffers with power-efficient current sources. The following sections describe two versions of the proposed technique in detail.

2.3.1 Current Reference Pre-charging (CRP) with Constant Reference Loading (CRL)

Fig. 2.3 shows Current Reference Pre-Charging applied to a 7-level ZCB MDAC stage with a stage gain of 4; the timing diagram and the stage residue characteristic are shown in Fig. 2.4. During the sampling phase ϕ_s, the input is sampled across the signal capacitors $8C_{sigp}$, $8C_{sign}$. Concurrently, gated reference current sources I_{refp}<5:0>, I_{refn}<5:0> pre-charge the six reference capacitors C_{refp}<5:0>, C_{refn}<5:0> for a duration T_{ref}, to the nominal reference voltage given by

$$V_{ref} = \left(\frac{I_{refp}}{C_{refp}} - \frac{I_{refn}}{C_{refn}} \right) T_{ref}. \tag{2.4}$$

To ensure reference pre-charging is signal independent, pre-charge switches short the reference capacitors to V_{cm} during ϕ_{pr}. Fig. 2.5 shows the MDAC redrawn during the hold phase ϕ_h.

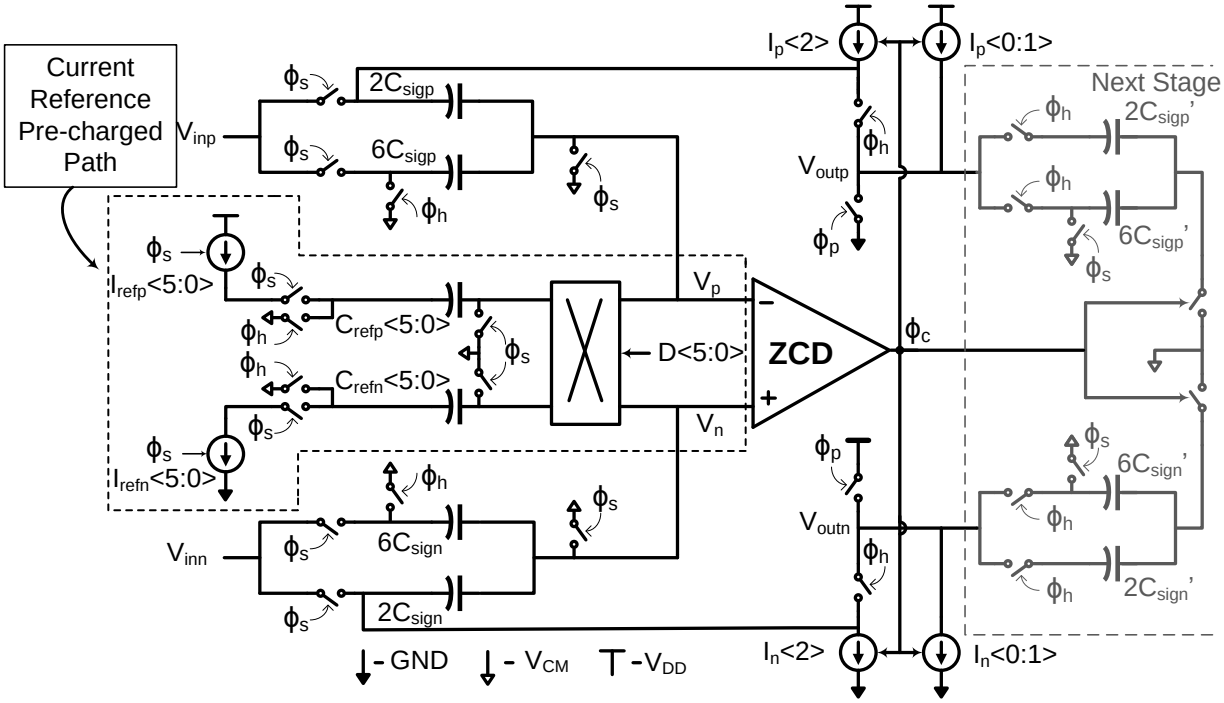

Figure 2.3: Schematic of the current reference pre-charged 7-level ZCB MDAC architecture (sub-ADC path and pre-charge switches not shown).

At the end of the pre-charge phase ϕ_p, depending on the thermometric-coded subADC decisions D <5:0>, the reference capacitors are connected appropriately to V_p and V_n, as shown in Fig. 2.5. At the end of ϕ_h, the charge from the signal and reference capacitors is transferred to the feedback capacitors, thus performing the MDAC operation given by

$$V_{out} = 4V_{in} + DV_{ref} \tag{2.5}$$

where D = 0, $\pm$1, $\pm$2, $\pm$3 is the subADC decision.

Note that with the chosen arrangement the feedback factor around the ZCD remains (subADC) *code-independent*. This version of CRP is termed Constant Reference Loading (CRL). It results

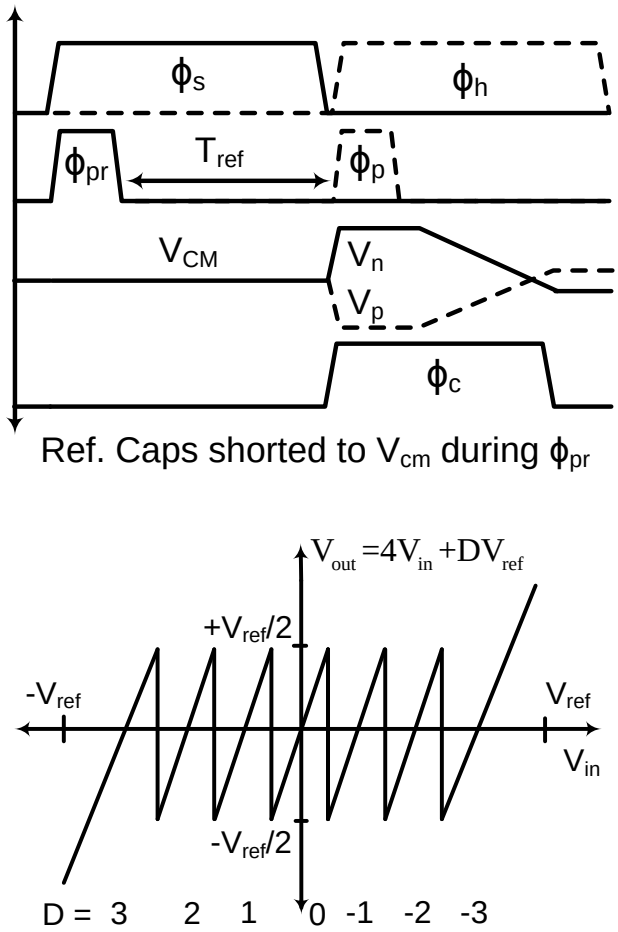

Figure 2.4: (top) Timing diagram; (bottom) Residue characteristic for the MDAC shown in Fig. 2.3.

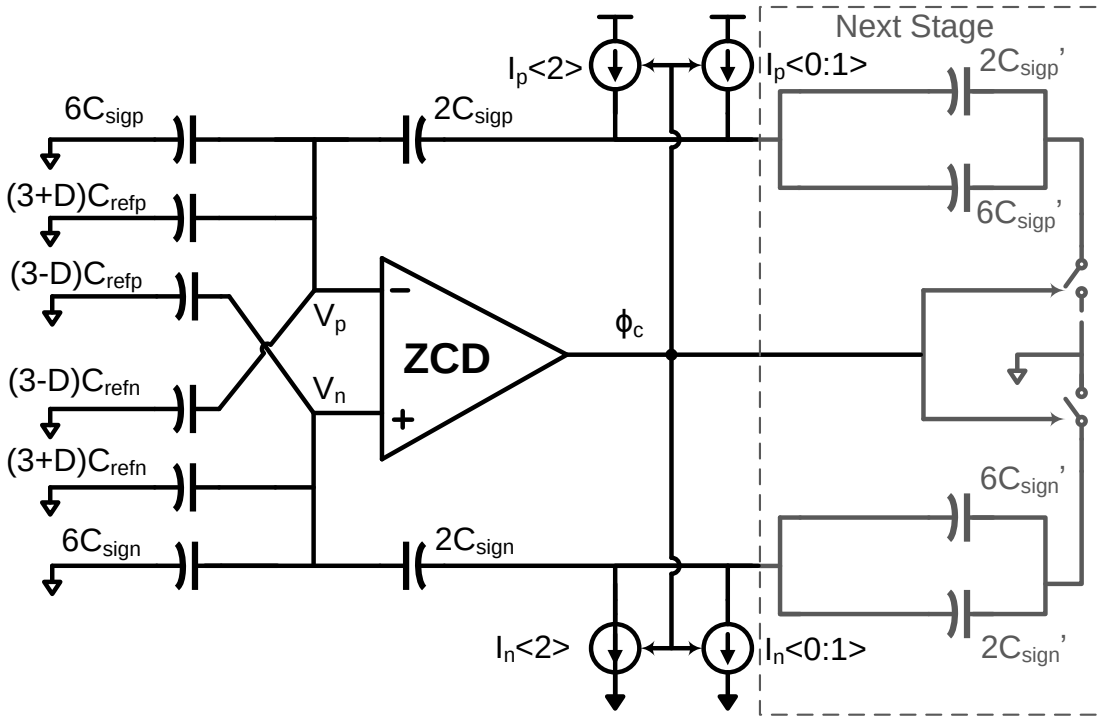

Figure 2.5: ZCB MDAC using current reference pre-charging with constant reference loading redrawn during the hold phase ϕ_h.

in a (subADC) code-independent overshoot at the output of the MDAC, due to the finite delay of the zero-crossing detector (ZCD). These overshoots can be compensated for in the foreground or background [8, 9].

By separating the signal and reference capacitors, the current drawn from the reference voltage is made signal independent and as a result, power hungry reference voltage buffers can be replaced with power-efficient current sources. Any errors associated with the locally generated reference can easily be calibrated with standard calibration techniques, as will be discussed in Section 2.3.4.

Earlier works on reference voltage pre-charging [19, 20] have been voltage based, requiring large off-chip decoupling capacitors (for a low-noise reference) and external reference voltage buffers. The reference double-sampling technique in [19] is not a viable solution in ZCB designs due to the inter-stage reference noise coupling issue described in Section 2.2.2. Current reference pre-charging technique replaces the reference voltage buffer with power-efficient gated current sources, which can also be looked at as the weakest reference voltage buffer, leading to a completely integrated (on-chip) solution. The reference network is localized to each stage, thus avoiding off-chip and on-chip noise coupling issues and simplifying the reference distribution. Stage-wise reference localization is especially beneficial in zero-crossing based implementations. It prevents the reference voltage of the first (most critical) stage of the pipeline from being disturbed by currents, injected into the reference voltage, from the later stages.

The separate reference capacitors, connected to V_p and V_n during the hold phase, however, lead to a reduction in the slope of the input waveform to the zero-crossing detector (ZCD), which in turn leads to more stringent noise requirements on the ZCD. For instance, if C_{ref} and C_{sig} are

typically chosen to be equal size as discussed in section 2.4.2, the feedback factor $\beta = 1/7$ for the MDAC in Fig. 2.3, when compared to $\beta = 1/4$ for a conventional 7-level MDAC. This requires a 2 times more stringent noise requirement on the ZCD for the MDAC in Fig. 2.3. But since the ZCD is only one among the major power consuming blocks in a ZCB MDAC (the others being the output current sources and the subADC), the power savings obtained by eliminating reference voltage buffers more than compensates for the required power increase in the ZCD due to the reduction in feedback factor. Dynamic Reference Loading (DRL) will be proposed below as a technique to reduce the effective reference capacitor loading.

Although CRP is described here in the context of a ZCB MDAC pipeline ADC stage, it can also be applied to Successive Approximation Register (SAR) ADCs, as shown in the implemented ADC prototype. Making the charge drawn from the reference path signal-independent is very beneficial in a SAR as the reference voltage needs to settle within each short SAR comparison cycle.

2.3.2 Input Range Extension (IRE)

One drawback of the residue characteristic of Fig. 2.4 is that the MDAC output goes close to the rails when the input is near $\pm V_{ref}$. Since the output current sources experience a larger voltage swing (and hence have lesser headroom), this affects the stage linearity. By adding two additional subADC levels at $\pm 7V_{ref}/8$ [9,21], as shown in Fig. 2.6, along with additional reference capacitors to limit the MDAC residue characteristic, the output of the MDAC can be limited to half the full scale. This in turn improves the linearity of the ZCB output current sources as they now have

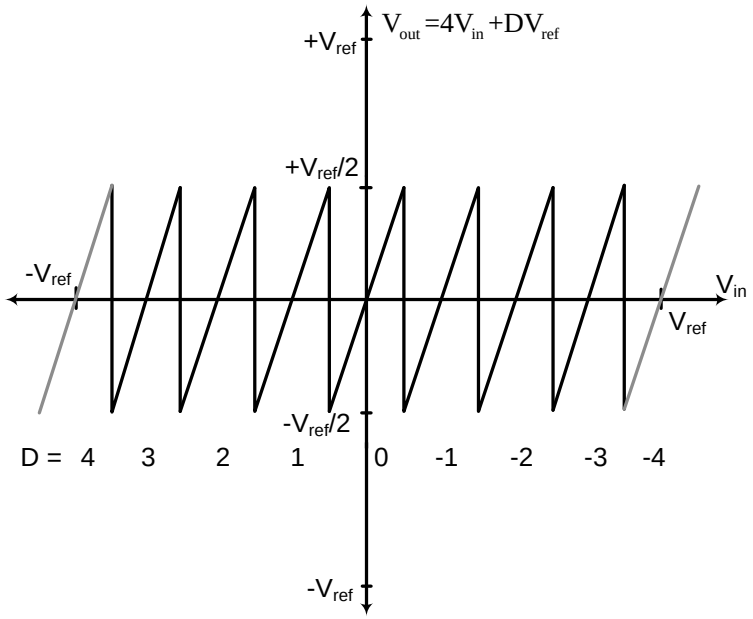

Figure 2.6: Residue characteristic for MDAC with Input Range Extension (IRE).

more headroom. Alternatively, the ADC can now accept input signal beyond its full-scale, without degrading the distortion performance, thus providing an Input Range Extension (IRE).

Although discussed here in the context of Current Reference Pre-charging in ZCB MDACs, it should be noted that IRE is a general technique that can also be applied to OTA-based MDACs or conventional ZCB MDACs to overcome voltage headroom issues. IRE comes at the expense of a small reduction in the MDAC feedback factor (due to the additional required reference capacitors), and two additional subADC comparators, which have a negligible impact on the total power consumption.

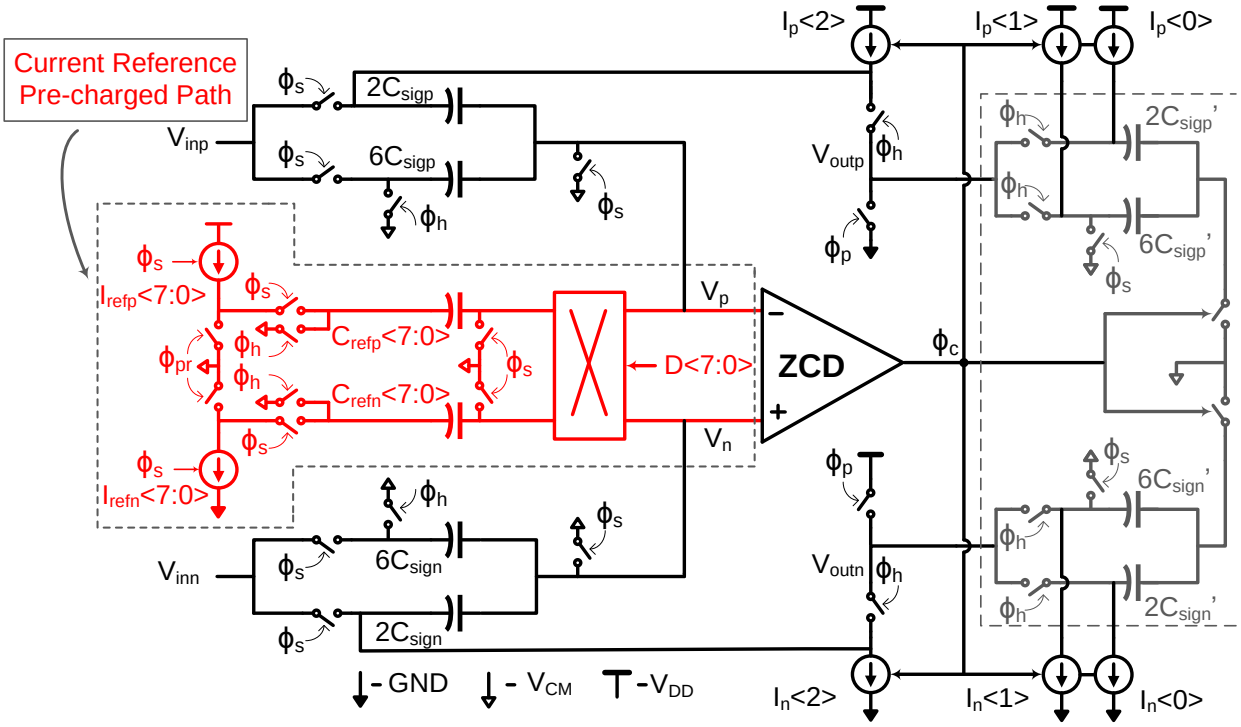

Figure 2.7: Schematic of the pre-charged 9-level ZCB MDAC architecture with dynamic reference loading and input range extension (subADC path not shown).

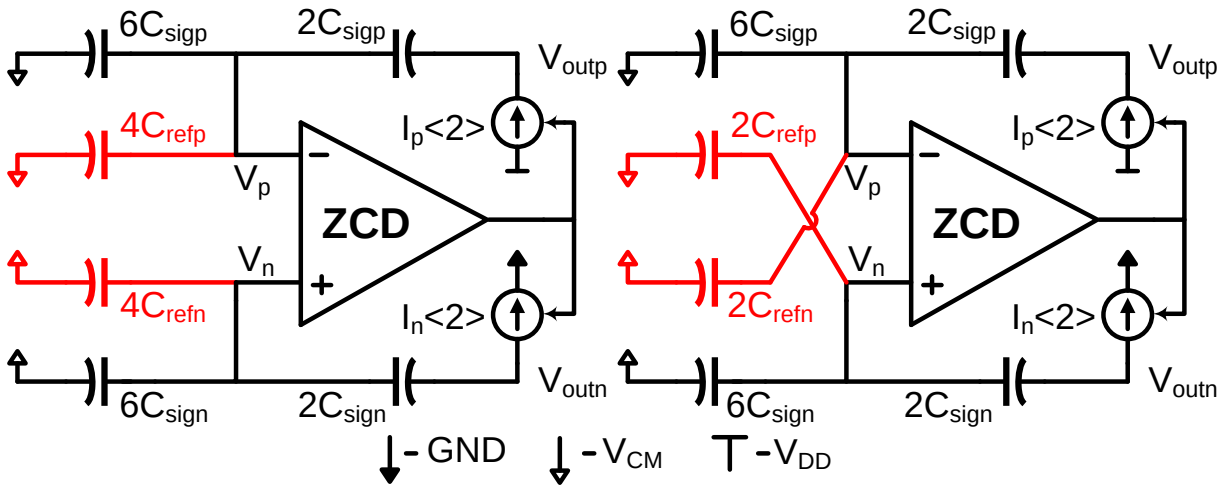

Figure 2.8: Dynamic reference loading MDAC during hold phase for two sub-ADC decisions: (left) D=2 and $V_{out}=4V_{in}+2V_{ref}$; (right) D=-1 and $V_{out}=4V_{in}-V_{ref}$

2.3.3 Current Reference Pre-charging with Dynamic Reference Loading (DRL)

We now introduce the Dynamic Reference Loading (DRL) technique [22] that reduces the effective reference capacitor loading, and thus relaxing the noise requirements on the ZCD, while still maintaining signal independent reference charging.

Fig. 2.7 shows the dynamic reference loaded ZCB MDAC stage with Input Range Extension (IRE) applied; its residue characteristic is given in Fig. 2.6 and its timing diagram in Fig. 2.4. During the sampling phase ϕ_s, the input is sampled across the signal capacitors $8C_{sigp}$, $8C_{sign}$. Concurrently, gated reference current sources I_{refp}<7:0>, I_{refn}<7:0> pre-charge the eight reference capacitors C_{refp}<7:0>, C_{refn}<7:0> for a duration T_{ref}, to the nominal reference voltage V_{ref} given by (2.4). During the hold/residue phase ϕ_h, the reference capacitors are connected appropriately to V_p, V_n *only as and when required* based on the subADC decisions D <7:0>, which are made during the pre-charge phase ϕ_p.

Fig. 2.8 shows the MDAC redrawn during the hold phase for two cases: when the MDAC performs $4V_{in}$+$2V_{ref}$, $4C_{refp}$ and $4C_{refn}$ capacitors are connected to V_p and V_n respectively; when the MDAC performs $4V_{in}$-V_{ref}, $2C_{refp}$ and $2C_{refn}$ capacitors are connected to V_n and V_p respectively; when the MDAC performs $4V_{in}$, none of the reference capacitors are connected to V_p and V_n. The remaining C_{refp} and C_{refn} capacitors are discharged during the hold phase ϕ_h to ensure reference pre-charging is signal independent.

Dynamic Reference Loading (DRL) reduces the average reference capacitor loading on nodes V_p and V_n and hence improves the average feedback factor β by 1.4 times (for a uniform input) when compared to the constant reference loading in [10] (with IRE included). This in turn relaxes the ZCD noise requirements and also reduces the noise contribution of the reference path. Since the effective feedback factor is now code-dependent, the ramp rate at the nodes V_p and V_n, and hence the overshoot of the zero-crossing based MDAC, is code-dependent. This code-dependent overshoot error can be effectively combined with reference capacitor mismatch errors and corrected with simple foreground digital correction as discussed below.

2.3.4 Digital Calibration Techniques for CRP

The value of the reference voltage, given by (2.4), cannot be known accurately beforehand. Large mismatches between the reference currents of successive MDAC stages can cause stage residue over-ranging (the residue output of one stage goes above the valid input range of the next stage). To avoid such large reference current mismatches, foreground reference current calibration routines,

described in Section 2.4.2, are implemented for coarse reference voltage alignment across the MDAC stages.

The residual reference voltage mismatch between MDAC stages, after foreground reference current calibration, will still give rise to code jumps in the ADC output characteristic. Since the value of the reference voltage is input-signal independent, this residual reference voltage mismatch can be combined with stage gain error (due to signal capacitor mismatch) and corrected with standard Digital Gain Error Correction [3], which also corrects for reference capacitor mismatches. The code-dependent MDAC overshoot, due to the code-dependent feedback factor in Dynamic Reference Loading (DRL), is identical to errors due to reference capacitor mismatches, and hence can be corrected with the same Digital Gain Error Correction [3].

Fig. 2.9 shows the residue characteristic for the Stage I CRP MDAC (of Fig. 2.3), for an ideal MDAC and for an MDAC with residual reference gain error and reference capacitor mismatches, along with the reconstructed digital output codes for the two cases. The calibration algorithm consists of measuring the code jumps Δ_1 etc. from the reconstructed ADC characteristic with the help of the back-end ADC and removing these errors digitally, which involves only digital addition and subtraction.

It should be noted that Digital Gain Error Correction, like in [3], only corrects for code jumps in the overall ADC transfer characteristic thus making the overall transfer characteristic linear, but still has global gain and offset errors (i.e. the ”gain” of the ADC is not exactly 1). For a lot of applications, such as in communication receivers, these global gain and offset errors are not of a concern as they do not give rise to any non-linearity. But in applications such as instrumentation

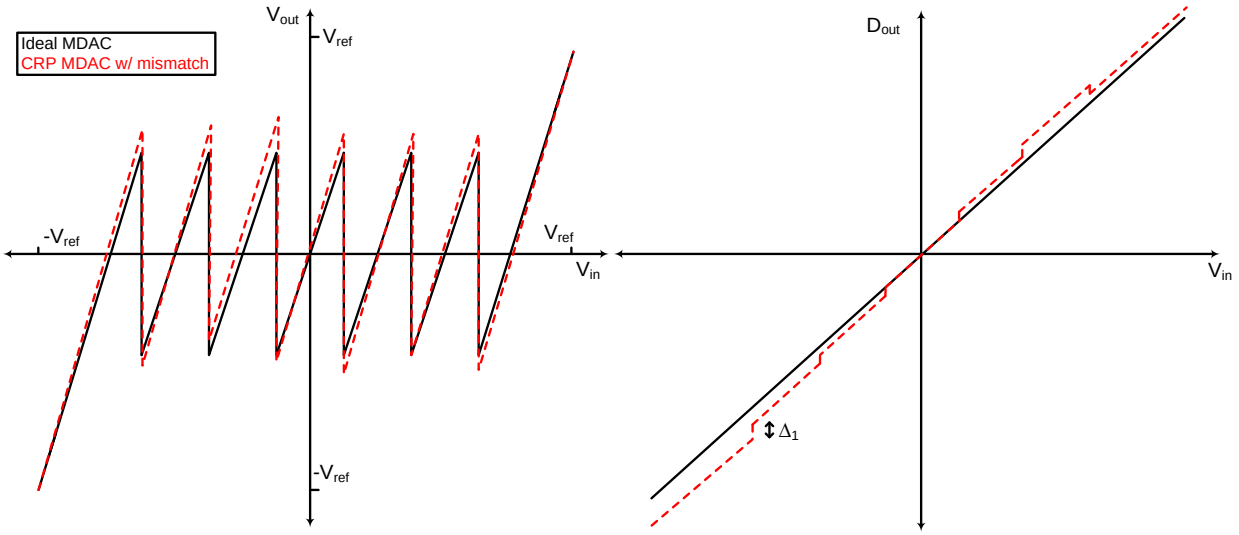

Figure 2.9: Digital foreground calibration of reference gain error and reference capacitor mismatches in CRP: (left) Residue characteristic; (right) Reconstructed digital output.

systems, the global gain and offset errors are of a concern and would need to be calibrated with respect to an absolutely known reference.

2.3.5 Non-Ideal Effects in CRP

The reference pulse duration T_{ref} is obtained from the sampling clock and hence jitter on the sampling clock will lead to noise charge sampled onto the reference capacitors, which in turn could limit the maximum SNR (Signal-to-Noise Ratio) that can be achieved by the CRP MDAC. In a 7-level MDAC stage [10] with a gain of 4, the maximum achievable SNR due to jitter on the reference pulse duration T_{ref} alone can be shown to be given by

$$SNR = 20log\left(\frac{2T_{ref}}{3t_j}\right), \tag{2.6}$$

where t_j is the absolute random ADC sampling clock jitter i.e. the jitter in the position of the ADC sampling clock edge when compared to an ideal jitter-free reference. From (2.6), T_{ref} needs to be maximized for a given clock rate to achieve the best SNR. By choosing the reference pulse duration to be half the clock period, the jitter requirement is seen to be close to that required on the ADC sampling clock for input signal sampling ($\approx$ 1.4ps for 12-bit SNR at 50MS/s). Dynamic Reference Loading (DRL), by reducing the effective reference capacitor loading, reduces the net noise contribution of the reference path further. The noise requirements on the reference path are discussed in more detail in Section 2.4.2.

Non-linear junction capacitors on the nodes V_p and V_n in Fig. 2.3 due to switch parasitics do not affect MDAC linearity as these nodes are close to V_{cm} at both the start and end of ϕ_h. Any drift on the reference voltage due to temperature can be corrected by periodic foreground or background calibration [23], in addition to relying on temperature independent generation of I_{ref} [24]. In general, DRL would require recalibration to combat the effects of temperature and supply drifts (changes in I_{ref}, ZCD delay, parasitic capacitors etc. with temperature).

2.4 ADC Circuit Implementation

2.4.1 System Architecture

The ADC prototype is targeted to achieve 12-bit performance at a sampling rate of 50MS/s in 65nm CMOS. The performance of SAR ADCs has been constantly improving with technology scaling, but low complexity single channel SARs in 65nm are still limited to ENOBs (Effective Number

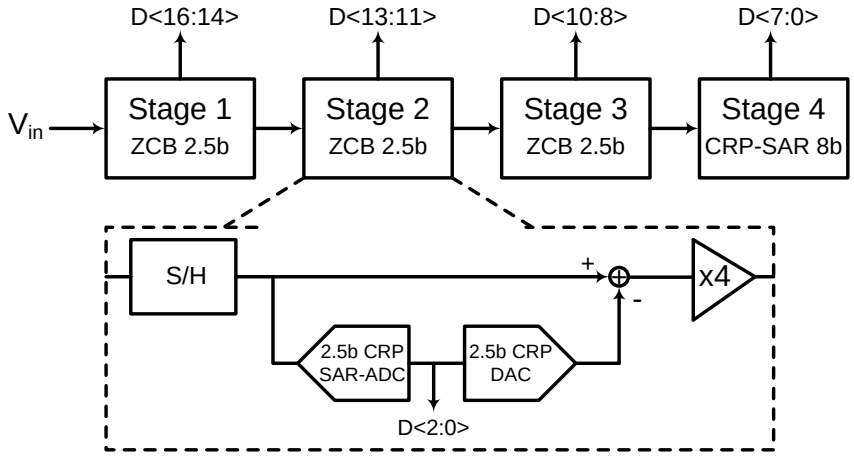

Figure 2.10: Architecture of the hybrid pipelined-SAR ADC (ADC_1) prototype with current reference pre-charging; D$< 16:0 >$ are the raw ADC bits before digital calibration.

of Bits) $<$ 10-bits at sampling rates of the order of 50MS/s [25, 26]. Hybrid Pipeline-SAR ADCs, with one or more Pipeline MDACs followed by a SAR, have been shown recently to offer very good performance [27, 28].

In the available 65nm process, it was found that a 8 or 9-bit 50MS/s SAR could be designed with very minimal complexity, so a hybrid Pipeline-SAR ADC architecture was chosen for the ADC prototypes. ZCB circuits potentially offer lower power operation than OTA-based designs in scaled technologies, with power-efficient current sources replacing OTAs [6, 8, 9]. Also, ZCB circuits do not suffer from stability issues and gain-bandwidth trade-offs like OTA-based designs. Increasing the number of bits resolved per stage reduces the required number of pipeline stages and leads to more aggressive power scaling [29], but also increases the subADC complexity and requires calibration for DAC non-linearities. Since calibration [3] is implicitly required for the proposed DRL CRP technique, a design with multiple bits per stage was selected.

Two ADC prototype were designed to demonstrate the proposed current reference pre-charging

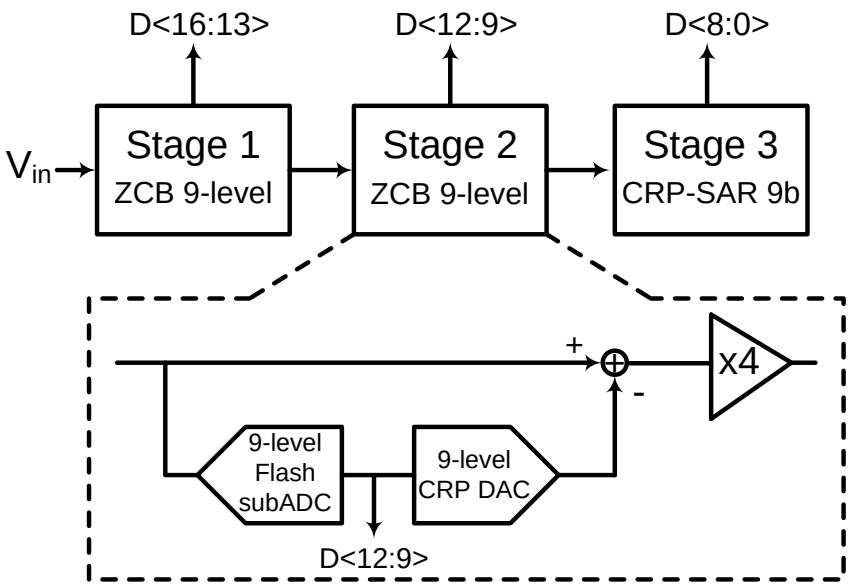

Figure 2.11: Architecture of the hybrid pipelined-SAR ADC (ADC_2) prototype with current reference pre-charging; D$< 16:0 >$ are the raw ADC bits before digital calibration.

techniques. The 1^{st} prototype ADC_1, shown in Fig. 2.10, consists of three 7-level ZCB MDAC stages, each with a gain of 4, providing 2 effective bits each, followed by an 8-bit CRP SAR stage. The ZCB MDAC for ADC_1 are based on the constant reference loading CRP MDAC architecture of Fig. 2.3.

The 2^{nd} prototype ADC_2, shown in Fig. 2.11, consists of two 9-level ZCB MDAC stages with IRE, each with a gain of 4, providing 2 effective bits each, followed by a 9-bit CRP SAR stage. The additional SAR bit is used to provide a higher resolution for start-up calibration.

For both ADC prototypes, CRP is implemented in *both* the ZCB MDAC stages and the SAR, completely avoiding the need for low impedance reference buffers and/or large on-chip reference decoupling capacitors.

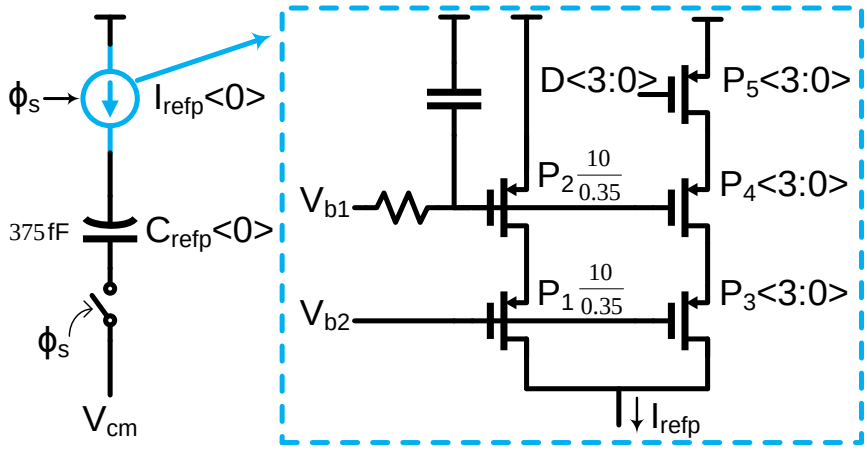

Figure 2.12: Single unit of the positive reference path (pre-charge switches not shown): All transistor dimensions are in $\mu m/\mu m$.

2.4.2 ZCB MDAC Implementation

Current Reference Pre-charged Path

The reference current sources I_{refp}<7:0> and I_{refn}<7:0> are implemented as digitally programmable cascoded current sources. Switches short the reference capacitors to V_{cm} during ϕ_{pr}. Hence, the reference current sources have no linearity requirements since they charge the reference capacitors from the same voltage every cycle. A smaller reference capacitor C_{ref} leads to smaller reference loading on nodes V_p and V_n. But since the amount of reference charge that needs to be transferred to the output is constant, the reference current sources would need to charge C_{ref} to a higher voltage, thus degrading their power supply noise rejection (PSRR). As a compromise between the reference capacitor loading and the PSRR, each C_{ref} is chosen to be equal to C_{sig}. The nominal reference voltage V_{ref} (2.4) is chosen to be 0.9V, which gives the reference current source a 200mV headroom with a 1.3V supply. Fig. 2.12 shows the implementation of a single unit of the posi-

tive reference path. The complete reference path consists of eight such units in parallel and eight complementary units for the negative reference path.

The noise variance on the reference capacitor C_{refp}, due to noise from the charging current I_{refp}, at the end of the reference pre-charge period T_{ref} in Fig. 2.12 is given by [30].

$$\overline{V_n^2} = \frac{2kT\gamma g_m}{C_{refp}^2} T_{ref} \qquad \text{or} \qquad \overline{V_n^2} = \frac{2kT\gamma}{C_{refp}^2} (I_{refp} T_{ref}) \left(\frac{g_m}{I_{refp}} \right) \tag{2.7}$$

where k is the Boltzmann constant, T is the temperature, g_m is the transconductance of transistor P_2, γ is the excess noise factor and I_{refp} is the positive reference current.

The value of the reference capacitor C_{refp} in (2.7) is set by the reference current source PSRR and the size of the input sampling capacitors (which are in turn determined by kT/C noise requirements). The reference pre-charge period T_{ref}, as required by (2.6), is maximized ($\approx$ 10ns for 50MS/s) to minimize SNR degradation due to reference clock jitter. C_{refp} and T_{ref}, along with (2.4), set the value of the reference current I_{refp}. Therefore according to (2.7), to minimize the noise contribution of the reference path, the reference current source is biased at a low g_m/I_{refp} ratio (7 in this design). The total noise contribution of the reference path (from simulation) is $80\mu V_{rms}$, leading to a 1.5dB degradation in the 12-bit SNR.

The bias for the current source is filtered to reduce the noise mirrored from the bias circuits. The current sources are made digitally programmable to enable reference current source calibration. Fig. 2.13 shows the simulated PSRR of a single unit of the positive reference path, showing a high-frequency PSRR of 27dB. All timing signals required by the reference path are generated by on-chip programmable delay cells.

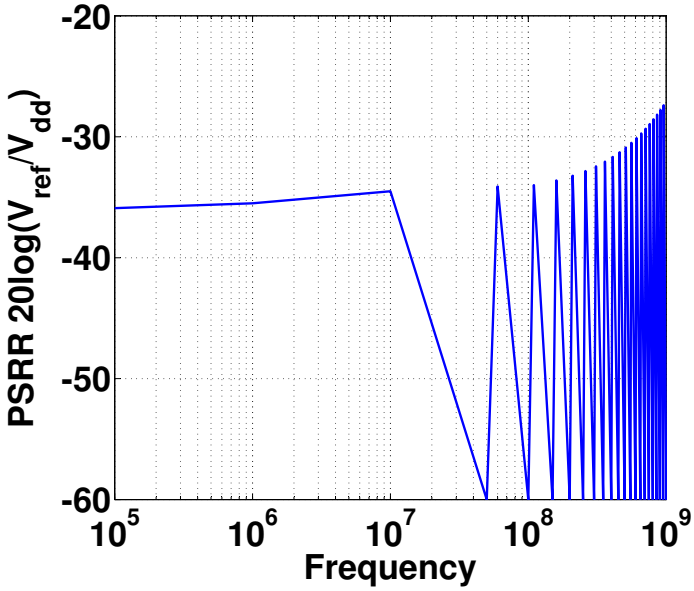

Figure 2.13: Simulated positive reference current source PSRR (single unit).

Mismatch between the reference current sources of successive stages of the pipeline can cause the residue output of one stage to go out of range of the next, thus causing an error that cannot be corrected with digital redundancy. In order to prevent reference over-ranging and maintain the residue within the valid input range, the foreground reference current calibration routine shown in Fig. 2.14 has been implemented for coarse reference voltage alignment across the MDAC stages. Using a dedicated pre-amplifier and latch, the calibration routine adjusts the strength of I_{refp} to set the positive reference voltage V_{refp} close to an external reference V_{extp}. It should be noted that the accuracy requirements on the reference V_{extp} are very much relaxed and it can be obtained by a simple resistive divider from V_{dd}. As described above, foreground digital calibration [3] is then performed to accurately determine the stage gains. Reference calibration circuitry is also implemented for the negative reference path, for both the ZCB pipeline stages and the final CRP SAR. The pre-amplifier in Fig. 2.14 is switched off after reference calibration to save power.

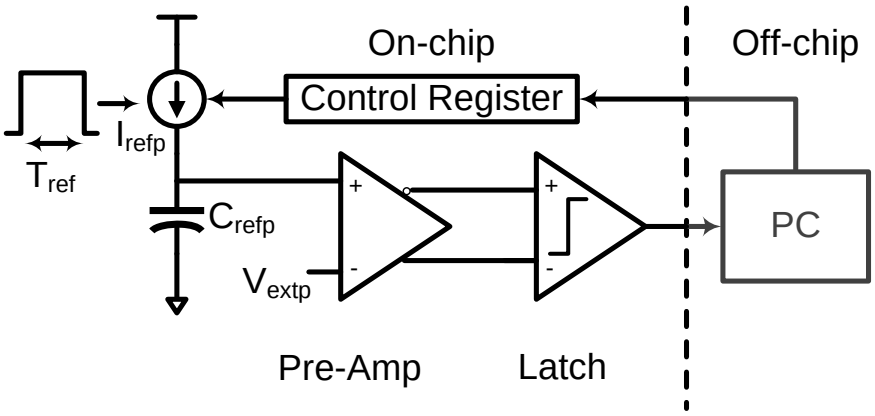

Figure 2.14: Reference current source calibration.

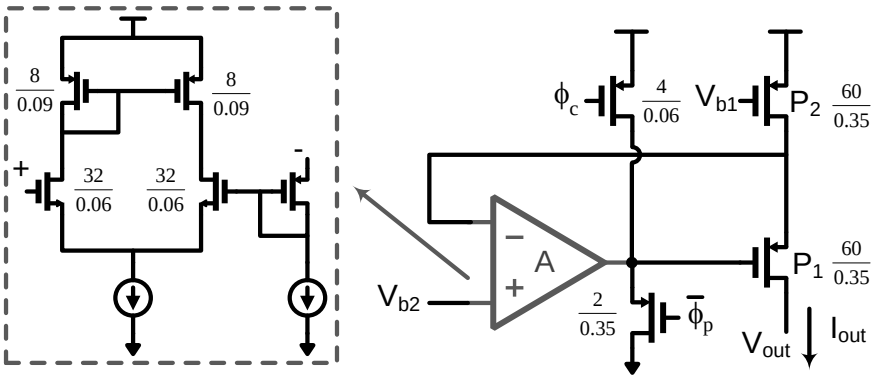

Figure 2.15: Output current source I_p implementation: All transistor dimensions are in $\mu m/\mu m$.

Output Current Source Implementation

The current sources I_p<0:2> and I_n<0:2> perform the actual charge transfer in the MDAC. Hence, their linearity directly affects the linearity of the MDAC [9]. This is because of the finite delay in the Zero-crossing detector (ZCD) during which any non-linearity in the output current is transferred onto to the next stage sampling capacitors. In order to improve the linearity performance of the the MDAC output current sources, they are implemented as regulated cascodes. Fig. 2.15 shows the implementation of I_p. As V_{out} rises during the charging of the output capacitors, the amplifier A regulates the gate voltage of P_1 to keep the drain of P_2, and hence I_{out}, constant.

The amplifier A dissipates 40% of I_{out} and is power gated when inactive to save power. This results only in a slight increase in the MDAC power consumption and hence the regulated cascode current source was selected for this design. To speed up settling during turn-on, the gate of P_1 is pulled down from V_{dd} to V_{dd} - $V_{th,p}$ ($V_{th,p} \approx V_{th,n} \approx 0.6$V in the current technology) with a PMOS during ϕ_p (in Fig. 2.4).

Any mismatch between the strengths of I_p and I_n leads to a common-mode error at the input of the ZCD. This common-mode error, to the first order, is rejected by the differential nature of the ZCD. In order to reduce the magnitude of the common-mode error presented to the ZCD, output current source calibration routines similar to Fig. 2.14 are implemented to set the strengths of I_p and I_n close to each other.

subADC Path for ADC_1

The subADC path consists of a sequential search SAR, with its own set of signal and reference capacitors. The thresholds of the SAR are obtained by capacitive division between the input signal and the reference and hence no reference buffer is required for the subADC. The subADC comparator is implemented as a CML style latch that makes its decision during the pre-charge phase ϕ_p. The subADC timing is controlled by an on-chip delay locked loop. The use of a sequential search SAR rules out any mismatch between the reference voltage of the flash and the MDAC which in turn would reduce the available redundancy.

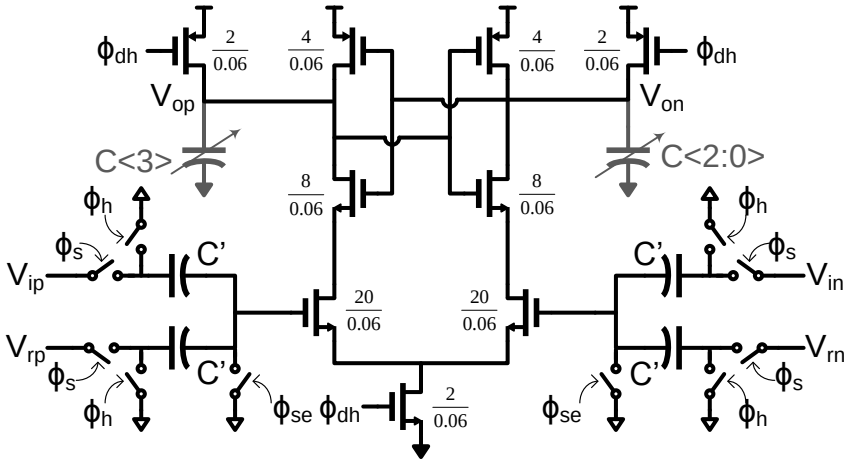

Figure 2.16: Flash comparator: ϕ_{se}/ϕ_{hd} - advanced/delayed versions of ϕ_s/ϕ_h: All transistor dimensions are in $\mu m/\mu m$.

subADC Path for ADC_2

The subADC decisions, D <7:0> in Fig. 2.3, are obtained from an eight comparator flash array. The flash thresholds (at $\{\pm 7/8, \pm 5/8, \pm 3/8, \pm 1/8\}V_{ref}$) are obtained by resistive division from a flash reference voltage of nominally V_{dd}. Fig. 2.16 shows the schematic of the comparator used in the subADC. Using separate signal and reference capacitors enables the use of a low power reference ladder, as the entire sampling phase is available to charge the reference capacitors. The total power drawn by the flash reference ladder is 32μW and is included in the total chip power consumption. All timing signals required by the subADC are generated by on-chip digitally tunable delay cells.

Using separate signal and reference capacitors has the disadvantage of increasing the input-referred subADC comparator offset. Comparator offsets can cause the stage output to go beyond the nominally designed level of $\pm V_{ref}/2$ in Fig. 2.4, which can potentially compromise output current source linearity. The 1σ input-referred comparator offset, obtained from Monte-Carlo sim-

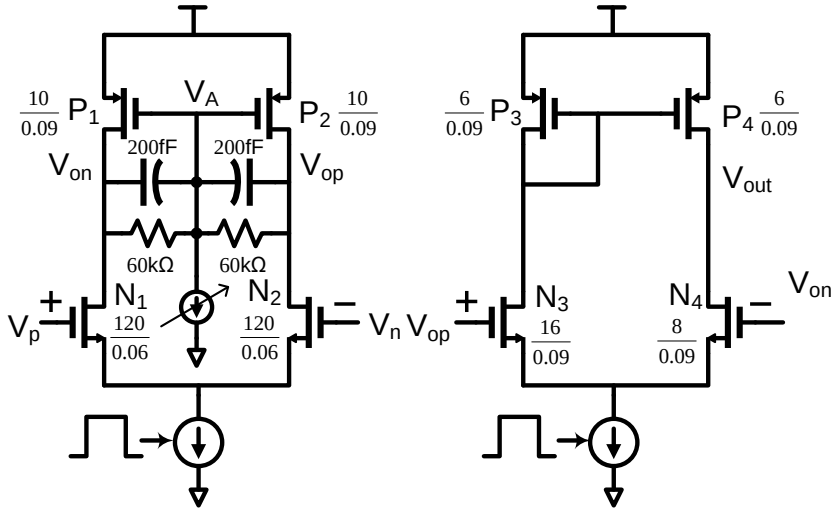

Figure 2.17: Schematic of the two-stage zero-crossing detector; all transistor dimensions are in $\mu m/\mu m$.

ulations, is 14mV. Although the offset is within the tolerable limit of the MDAC architecture, it was also made digitally tunable by a programmable MOS capacitor array C <3:0> at its output. The offset is tunable from -80mV to +80mV, in nominal steps of 10mV. Any mismatch between the references of the subADC and main reference paths reduces the available redundancy for the MDAC and affects stage linearity, as the MDAC output current sources experience a larger voltage swing. Foreground subADC calibration routines, by feeding a slow input ramp and aligning the heights of the different line segments of the MDAC residue characteristic, are implemented to reduce any such systematic mismatch. It should be noted that the input ramp used for this calibration has relaxed accuracy requirements as misalignment of the residue segments will only cause the MDAC output to be slightly beyond $\pm V_{ref}/2$, which only has a very slight effect on the output current source linearity.

Zero-crossing Detector (ZCD)

The ZCD performance is one of the factors that determine the noise and linearity performance of the MDAC. Fig. 2.17 shows the simplified schematic of the of the ZCD, which consists of a differential pre-amplifier followed by a differential-to-single-ended converter to provide improved common-mode rejection. In order to improve the ZCD noise performance, its bandwidth is limited by adding capacitors to the output of the first stage pre-amplifier, leading to smaller integrated noise power. The finite delay of the ZCD results in an overshoot at the MDAC output. The MDAC linearity depends on the overshoot being signal independent, which is satisfied if the output charging and discharging currents are constant during this delay period. It should be noted that the output current source linearity does not matter if they are turned off instantaneously after the zero-crossing event [9]. In order to relax the linearity requirements on the output current sources, this delay needs to minimized, which leads to a trade-off with the MDAC noise performance for a given ZCD bandwidth (higher ZCD bandwidth, lower delay, higher integrated noise and vice versa).

Transistors N_3 and N_4 are skewed to minimize the MDAC overshoot, while the stage linearity is still dependent on the linearity of the output current sources during the ZCD delay . The residual overshoot at the output of the MDAC is further compensated by a small capacitor array connected to V_p and V_n [8]. In order to save power, the ZCD is power gated when inactive. To enable fast settling, the node V_A in Fig. 2.17 is pulled to V_{dd} - $V_{th,p}$ with a PMOS during ϕ_p (in Fig. 2.4).

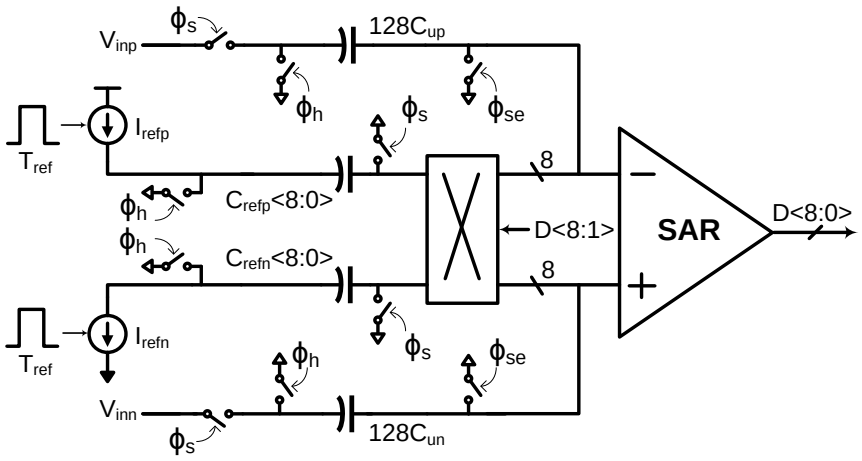

Figure 2.18: 9-bit SAR with current reference pre-charging (logic not shown).

2.4.3 9-bit Current-Reference Pre-charged SAR ADC for ADC_2

The 9-bit CRP SAR provides a power-efficient way to replace the latter stages of the pipeline. Fig. 2.18 shows the implementation of the SAR in ADC_2. The CRP SAR for ADC_1 is identical but with one less bit decision. Current reference pre-charging eliminates the need for a reference voltage in the SAR. Using separate signal and reference capacitors [20] is especially beneficial in a SAR, as the reference needs to settle within each short SAR comparison cycle. Depending on the SAR comparator decisions, the reference capacitors are connected appropriately to implement the binary search, as in [20]. The total the offset of the complete SAR path (e.g. due to switch charge injection) is compensated by a small capacitor array connected to its input, while the SAR comparator is sized to meet matching requirements.

The SAR timing can be implemented in either a synchronous or asynchronous fashion. Asynchronous SARs [31] require added complexity to detect comparator meta-stability issues and to set the time required for SAR capacitor array settling in a robust PVT-independent fashion. For the

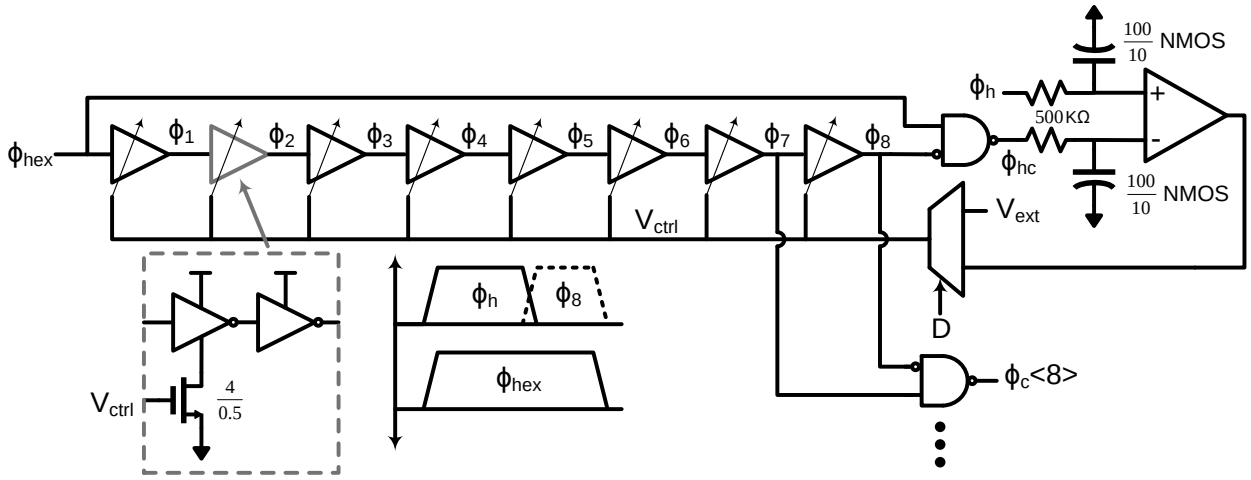

Figure 2.19: Delay-locked loop controlling SAR timing: All transistor dimensions are in $\mu m/\mu m$.

required SAR performance (9-bit at 50MS/s), the simplicity of a synchronous design was found to be more suitable. Fig. 2.19 shows the schematic of the delay-locked loop (DLL) that generates the SAR timing signals. An extended version of the hold phase clock ϕ_{hex} is passed through the delay chain, and the duty cycle of the signal ϕ_{hc} is compared with the duty cycle of the hold phase clock ϕ_h. Using an extended version of the clock has the benefit of the pulse not completely disappearing as it passes through the delay chain. When the loop is locked, the signals ϕ_1, ϕ_2 .. etc. will have the required phase relationship. One advantage of equalizing the duty cycles, and not the clock edges, of the delayed and reference clocks is that the loop will not false lock to the sub-harmonics of the clock. The DLL of Fig. 2.19 has the issue of not starting up if the loop finds itself in an all zero state (i.e. when $V_{ctrl} = 0$). To avoid this, the control voltage V_{ctrl} is forced to an external voltage through a MUX during startup, and then control is passed onto the loop.

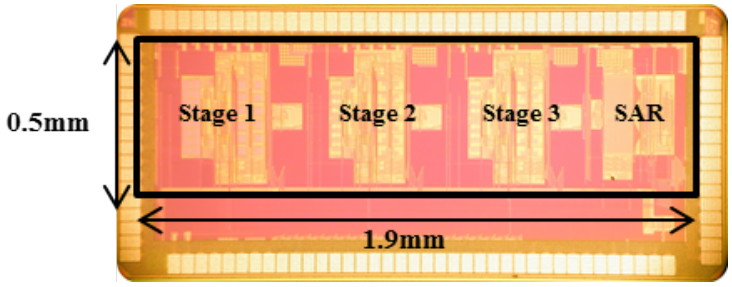

Figure 2.20: Die photo of the 65nm CMOS ADC prototype: ADC_1

2.4.4 Input Sampling and Clock Networks

The total input capacitance of the ADC (ADC_2) is 3pF single-ended, which gives a sufficient kT/C noise margin for the targeted 12-bit performance. The Stage II MDAC has a capacitance of 0.75pF (Stage III for ADC_1 in Fig. 2.10 is identical to Stage II). The input capacitance of the SAR is chosen to be close to Stage II to enable reusing the output currents sources from Stage I. The binary scaled SAR has a total capacitance of 0.69pF, with a 5.4fF unit capacitance. The input sampling switches are gate boosted to meet the linearity requirements at 50Msps [32].

In order to relax the jitter requirements on the clock distribution network, a 200MHz sinusoidal signal is fed to the chip and divided to generate the required 50MHz clock phases [33]. All required clock phases for the reference pre-charged path and the subADC path (signals ϕ_{pr} and ϕ_p in Fig. 2.4) are generated from the 50MHz clock using digitally programmable delay cells.

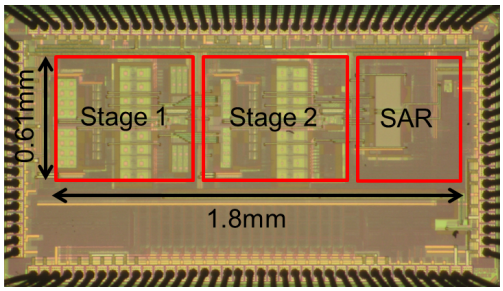

Figure 2.21: Die photo of the 65nm CMOS ADC prototype: ADC_2

2.5 Experimental Results

2.5.1 Measurement Setup

The two ADC prototypes were fabricated in a 65nm CMOS process. ADC_1, shown in Fig. 2.20, measures 0.95mm^2 while ADC_2[2], shown in Fig. 2.21, measures 1.1mm^2, which includes bias, programmability and supply decoupling[3] The dies were packaged in an 88-pin QFN package and soldered on a PCB and tested. The input sinusoidal signal was filtered and fed to the ADC through the Mini-Circuits ADT1-6T transformer that performs single-ended to differential conversion. All signals used for calibration were generated using an off-chip high resolution DAC (DAC7654) and fed to the chip by the ADC driver AD8138. The digital bits from the ADC are captured using a logic analyzer and all data processing is done offline in MATLAB.

The ADC_2 prototype requires only three external voltages: the nominal supply voltage V_{dd} of 1.3V, the common-mode voltage V_{cm} (nominally $V_{dd}/2$), and the flash reference (nominally V_{dd}), while ADC_1 requires only the nominal supply voltage V_{dd} of 1.35V and the common-mode voltage V_{cm} (nominally $V_{dd}/2$). The flash reference consumes only 32μW and in a differential

[2]The layout was not optimized for minimal area

[3]110pF of decoupling on V_{dd} and 40pF on V_{cm} was used to fill empty layout spaces.

implementation, the accuracy requirements on V_{cm} are very much relaxed and hence it can be obtained by a resistive divider from V_{dd}. It should be noted that the ADC does not require any accurate external reference voltage. A single global reference current is supplied externally and is required to be low noise, which in future fully-integrated implementations can be obtained as in [24].

2.5.2 Calibration Procedure

Additional input paths are included to calibrate the various stages; by tri-stating the output current sources of Stage I an external input can be provided to Stage II; similarly the output current sources of Stage II are tri-stated when providing a test input to the SAR. After chip power-up, reference current source calibration routines (see Section 2.4.2) set the references of the stages close to each other to avoid residue over-ranging. The strengths of the output current sources of the MDACs are then set close to each other by output current source calibration (see Section 2.4.2). The SAR is then put into its calibration mode and its offset is nulled. A slow ramp, generated by the off-chip DAC, is used to calibrate the SAR capacitor weights. Stage II is then put into its calibration mode and the external inputs are used to perform subADC calibration (see Section 2.4.2) and foreground Digital Gain Calibration (see Section 2.3.4). A similar procedure is then followed for the Stage-I MDAC.

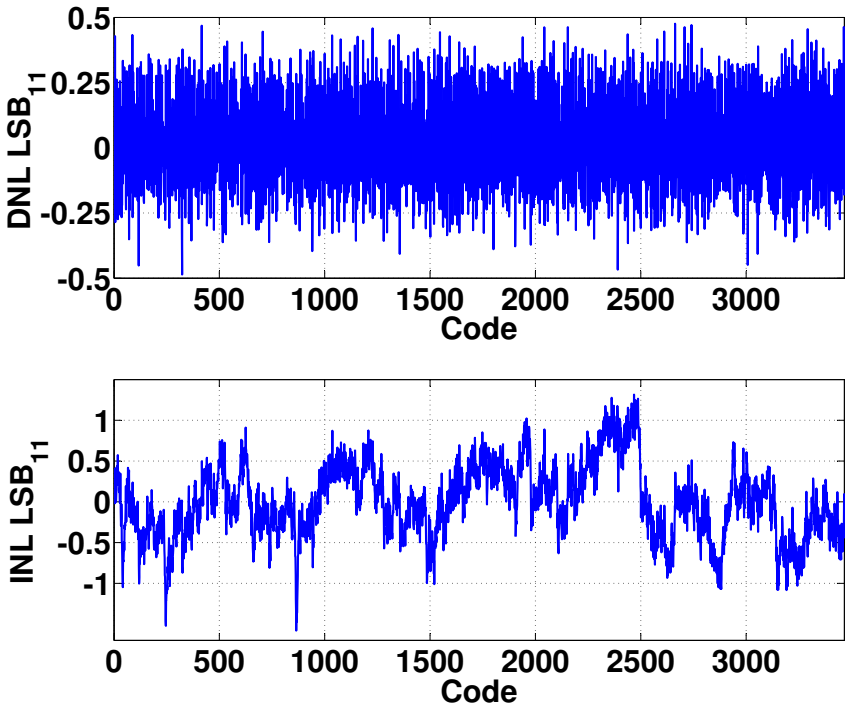

Figure 2.22: ADC static performance at 40Msps: INL/DNL after calibration.

2.5.3 ADC_1 Measurement Results

Static Performance

After calibration, the ADC has 3466 valid output levels, corresponding to a 11.7-bit resolution. Fig. 2.5.3 shows the measured INL/DNL at 40MS/s after foreground digital calibration. The INL is +1.31/-1.58 LSB_{11} and the DNL +0.47/-0.48 LSB_{11}, where LSB_{11} refers to a 11-bit LSB.

Dynamic Performance

Fig. 2.5.3 shows the dynamic performance of the combinations of Stage III and the SAR, after calibration, measured through the debug path. It can be seen that the Stage III and SAR combination has an SNDR, SFDR and SNR of 68dB, 53dB and 52dB respectively at 200KHz. The droop in

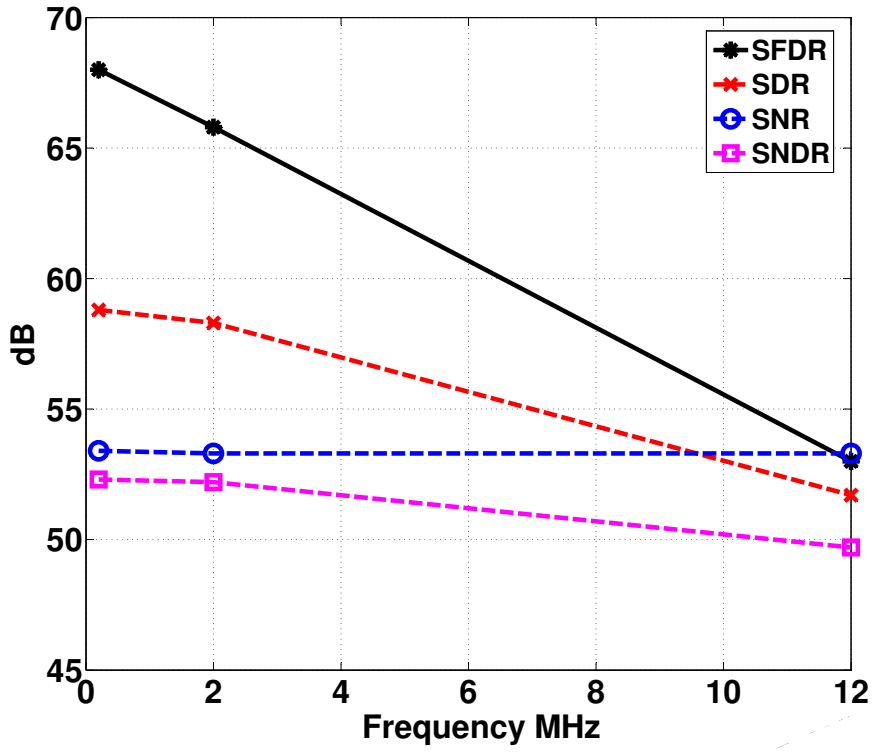

Figure 2.23: Dynamic performance of Stage III + SAR measured through the debug path.

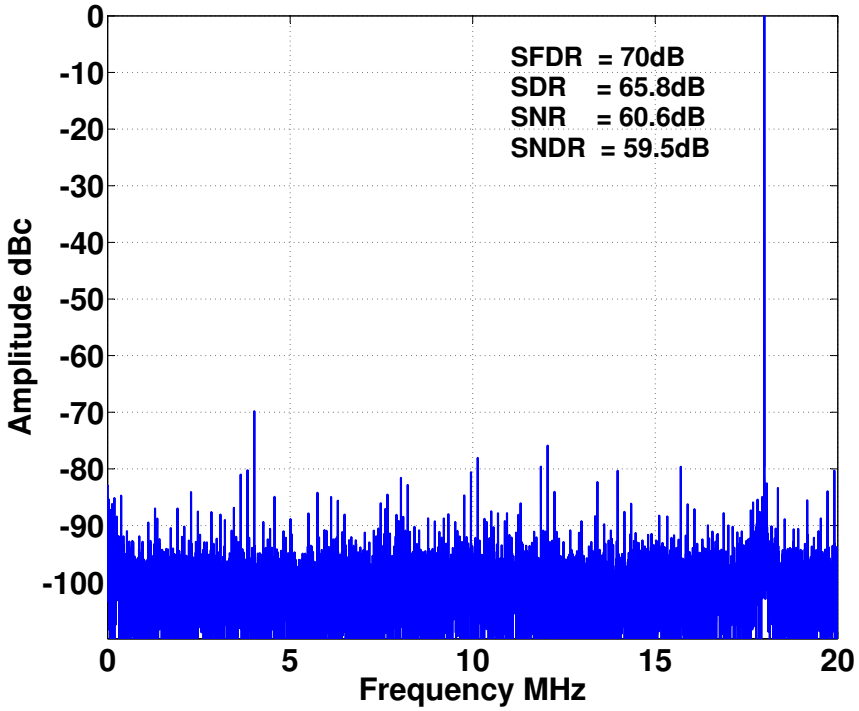

Figure 2.24: 16384-point FFT at 18MHz (Nyquist).

the SNDR as the input frequency is swept is due to distortion in the input sampling network of the debug path.

Fig. 2.5.3 shows the output FFT of the complete ADC for an 18MHz input signal. The SNDR at 18MHz is 59.5dB, yielding an ENOB of 9.7 bits.

Fig. 2.5.3 shows the complete ADC dynamic performance as a function of the input signal frequency. The SNDR varies by only 0.5dB up to 25MHz. The effective resolution bandwidth (ERBQ) is greater than 25MHz.

Fig. 2.5.3 shows the ADC dynamic performance as a function of the input amplitude at 2MHz. In ADC_1, unexpected offsets in the subADC path limit the input signal to 4dB below full-scale

Table 2.5.3 summarizes ADC_1 performance. The total power consumed by the ADC core is

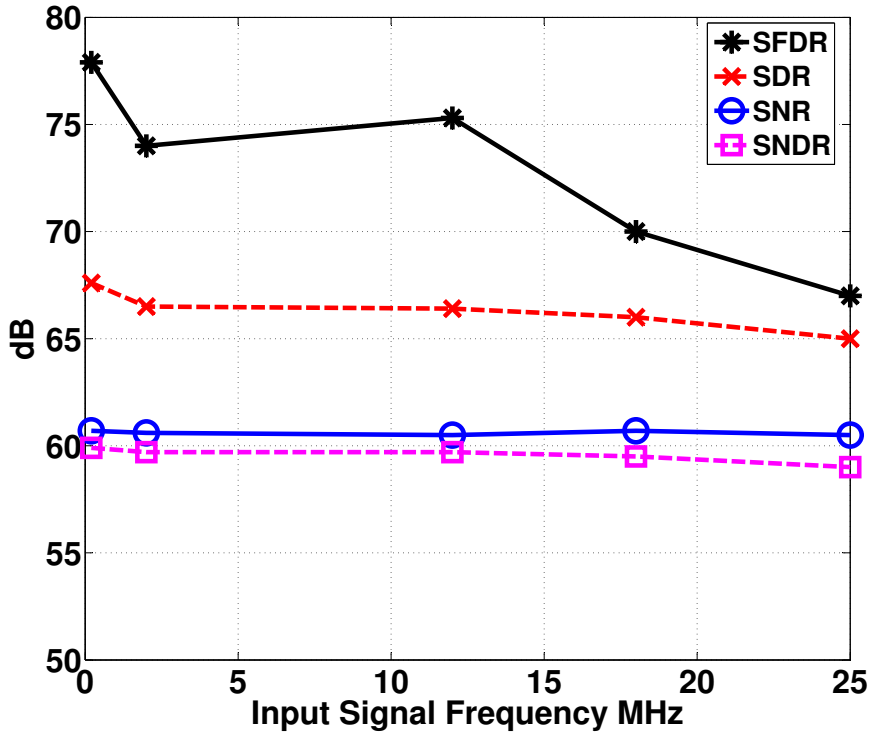

Figure 2.25: ADC_1 dynamic performance as a function of input frequency.

Table 2.1: ADC_1 Performance Summary

Die Area/Technology		0.95mm^2 in 65nm Low Leakage	
Resolution		11.7-bit (3466 levels)	
Sampling Rate		40 MS/s	
Supply Voltage		1.35V	
DNL (LSB_{11})	INL (LSB_{11})	+0.47/-0.48	+1.31/-1.58
SFDR/SDR/SNDR @ 18MHz		70dB/66dB/59.5dB	
Power		4.5mW	

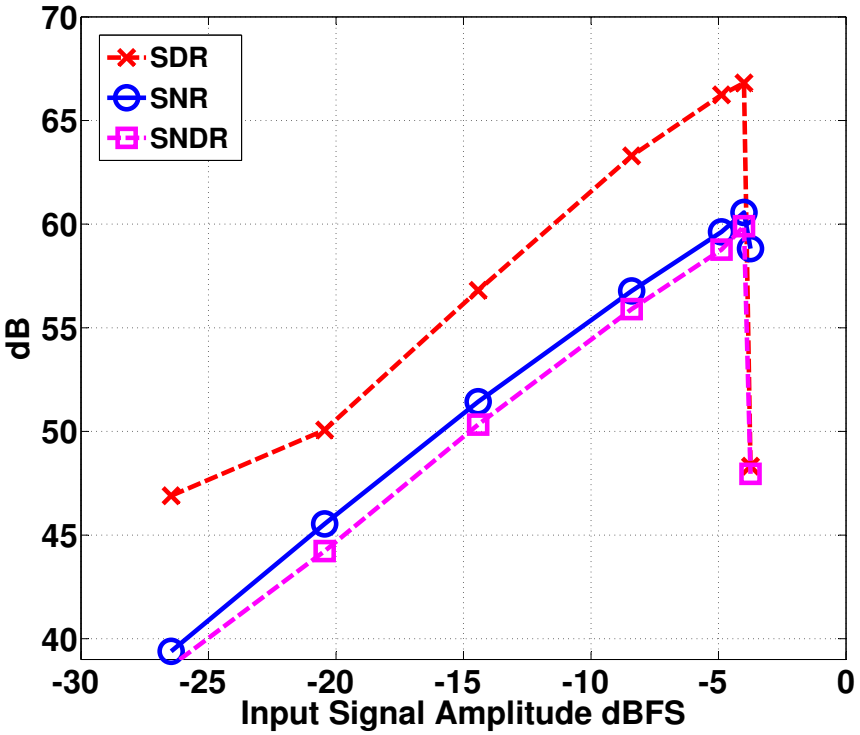

Figure 2.26: ADC_1 dynamic performance as a function of input amplitude at 2MHz.

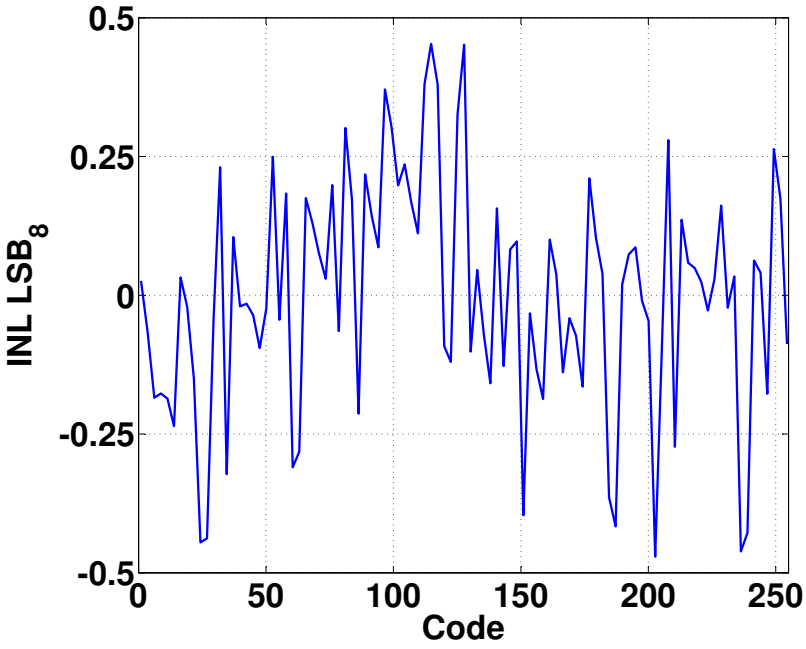

Figure 2.27: Measured SAR INL after calibration.

4.5mW from a 1.35V supply, requiring no additional power for the reference buffers which is typically required for other ADC implementations. The figure-of-merit at Nyquist is 142fJ/step, which includes the power consumed by the ADC references. The SDR of the ADC is close to 11-bit, and the SNDR performance is thermal noise limited since the input signal is limited to -4dBFS.

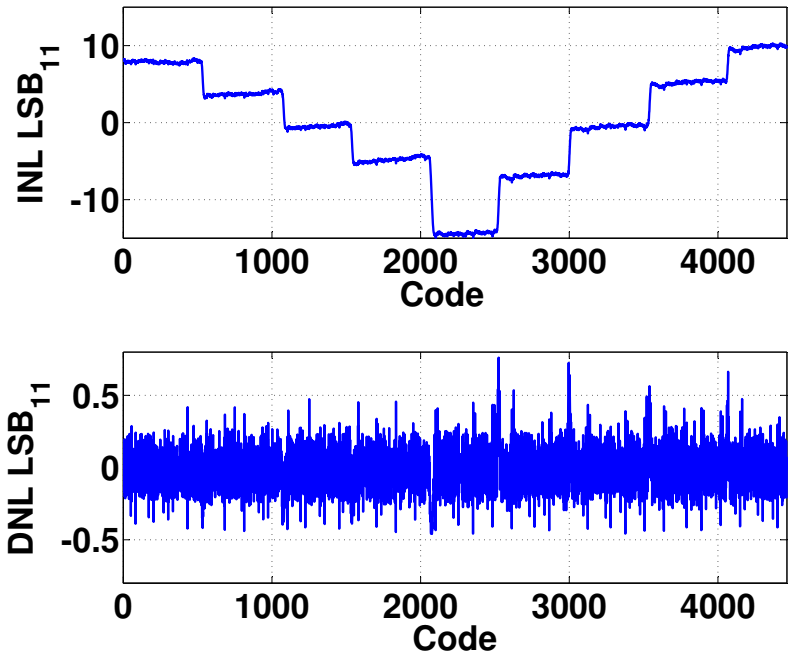

Figure 2.28: ADC_2 static performance at 50Msps: INL/DNL before calibration.

2.5.4 ADC_2 Measurement Results

Static Performance

Fig. 2.27 shows the measured INL of the SAR, after calibration, which is +0.48/-0.47 LSB_8, where LSB_8 refers to an 8-bit LSB (least significant bit). The measured noise performance of the SAR (for a grounded input) is 0.28 $LSB_{8,rms}$.

The static INL/DNL performance of the complete ADC was measured using a sine wave histogram test [34] at 200KHz. After calibration, the ADC has 4464 valid output levels, corresponding to a 12.1-bit resolution. Fig. 2.5.4 shows the measured INL/DNL before and after foreground digital calibration. Calibration improves the INL from +10/-15 LSB_{11} to +0.7/-0.86 LSB_{11}, the DNL from +0.76/-0.5 LSB_{11} to +0.5/-0.45 LSB_{11}, where LSB_{11} refers to a 11-bit LSB.

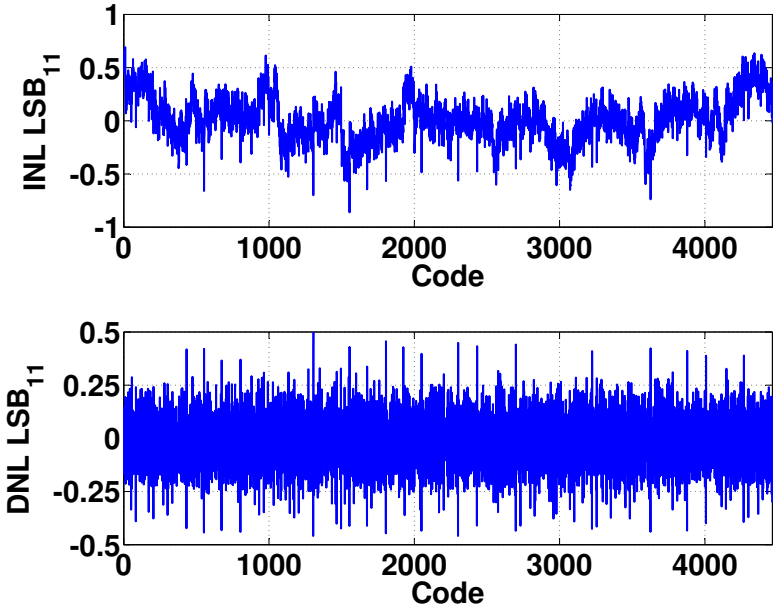

Figure 2.29: ADC_2 static performance at 50Msps: INL/DNL after calibration.

Dynamic Performance

Fig. 2.30 shows the FFT for a 200KHz sine wave input to Stage II after digital foreground calibration. The SFDR, SNDR and ENOB for the combination of Stage II plus the SAR are 75dB, 60.2dB and 9.75-bits respectively, for a full scale sine-wave input at 200KHz.

Fig. 2.5.4 and Fig. 2.5.4 show the 65536-point FFT of the complete ADC's reconstructed output at 200KHz, before and after digital foreground calibration respectively. The SFDR, SNDR and ENOB improve from 40dB, 39dB and 6.2-bits before calibration to 81dB, 67.1dB and 10.9-bits respectively after calibration. Fig. 2.33 shows the dynamic performance of the ADC as a function of the input frequency. It can be seen that the SNDR varies by only 1dB as the input frequency is swept from 200KHz to 25MHz. The SFDR, SNDR and ENOB at 25MHz (Nyquist) are 77dB, 66dB and 10.7-bits respectively.

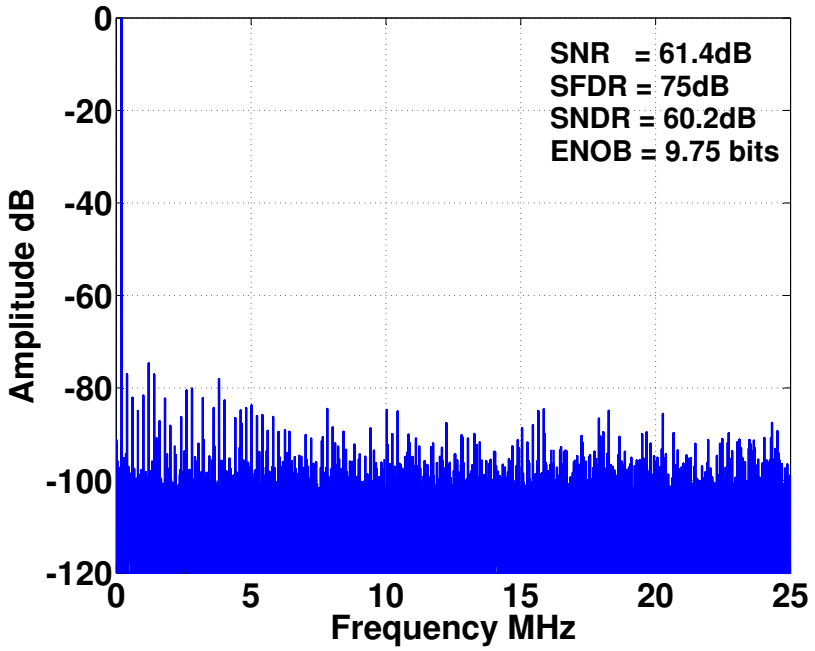

Figure 2.30: 65536-point FFT at 200KHz for Stage II + SAR.

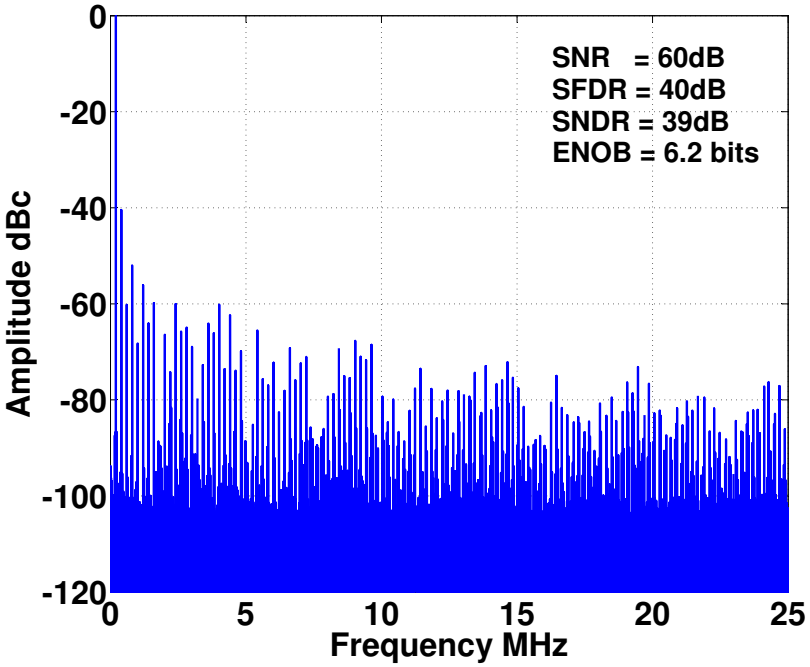

Figure 2.31: 65536-point FFT at 200KHz for the complete ADC: Before digital calibration.

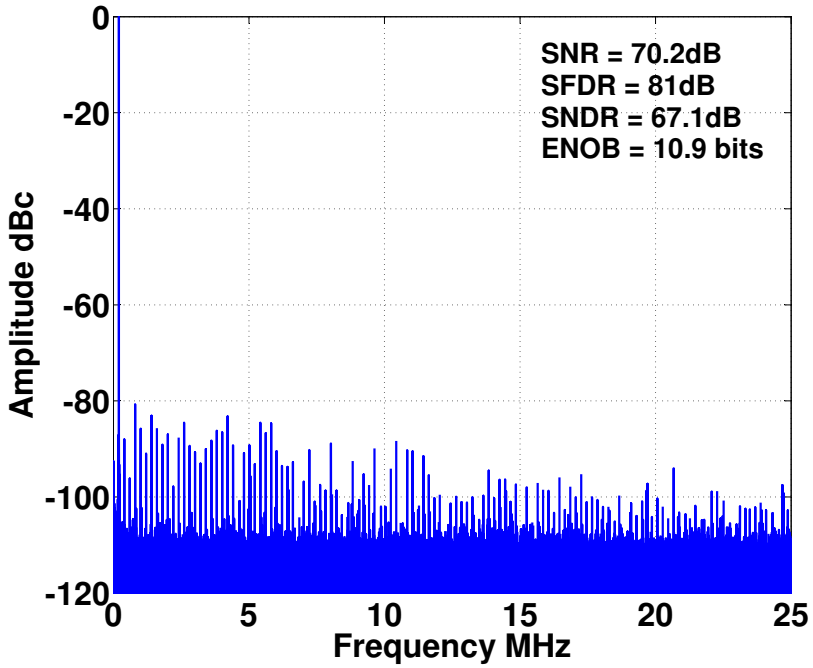

Figure 2.32: 65536-point FFT at 200KHz for the complete ADC: After digital calibration.

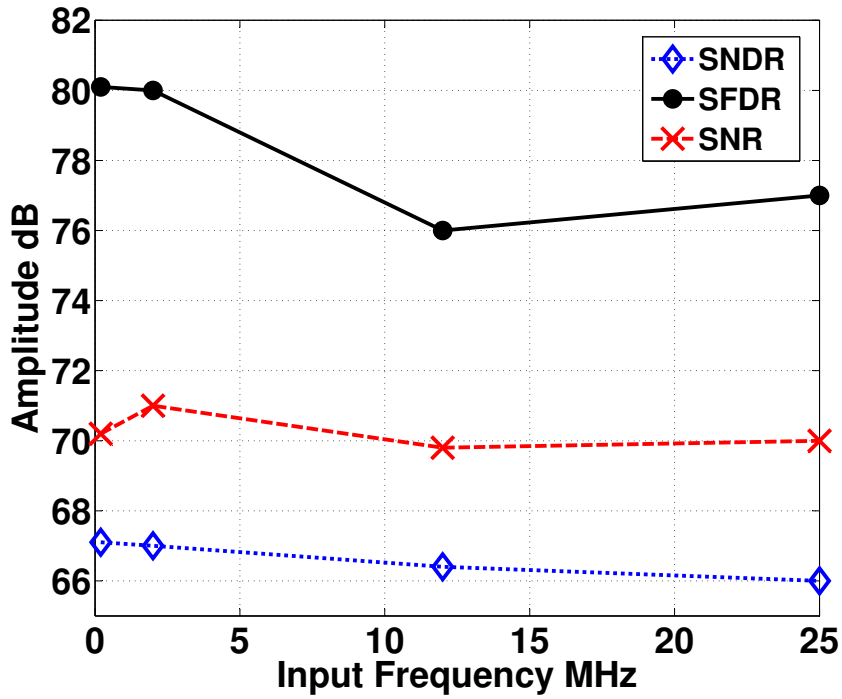

Figure 2.33: ADC_2 dynamic performance vs input signal frequency

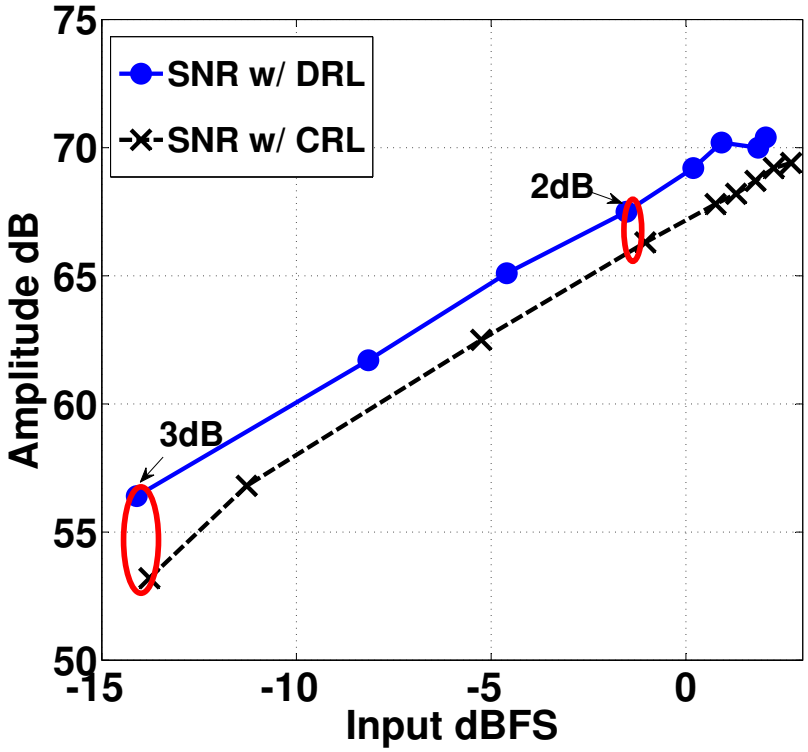

Figure 2.34: SNR vs input signal amplitude (at 200KHz) for DRL and CRL modes

Effect of Dynamic Reference Loading (DRL) on ADC Performance

The prototype can be configured to work in both Dynamic Reference Loading (DRL) and in Constant Reference Loading (CRL) modes. Fig. 2.34 shows the output SNR of the ADC as a function of the input amplitude at 200KHz. As expected, Dynamic Reference Loading improves the ADC noise performance by reducing the average reference capacitor loading (see Section 2.3.3). DRL provides 3dB better SNR at low input signal amplitudes and 2dB better SNR at higher input amplitudes.

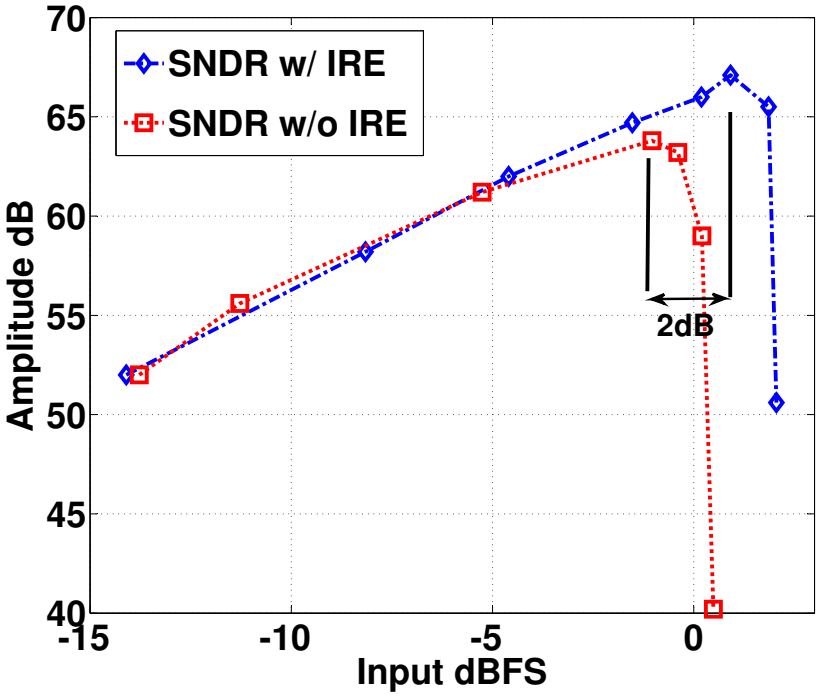

Figure 2.35: SNDR vs input amplitude (at 200KHz) with and without IRE; note that with IRE, the converter can operate with input signals up to 1dBFS

Table 2.2: ADC_2 Performance Summary

Technology	65nm CMOS
Supply Voltage	1.3V
Active Die Area	$1.1mm^2$
Resolution	12.1-bit (4464 levels)
Sampling Rate f_s	50Msps
DNL (LSB_{11})	+0.5/-0.45
INL(LSB_{11})	+0.7/-0.86
SFDR at 25MHz	77dB
SNDR at 25MHz	66dB
Power	4.8mW

Effect of Input Range Extension (IRE) on ADC Performance

Input Range Extension (IRE) [9, 21] implements two additional subADC levels at the extremes of the residue characteristic, i.e. at $\pm 7V_{ref}/8$ (Fig. 2.4), which enable the ADC to accept signals beyond its full-scale and still maintain its distortion performance. The prototype can be configured to disable the two additional subADC levels. Fig. 2.35 shows the SNDR of the ADC as a function of the input amplitude at 200KHz, with and without IRE. As expected, it can be seen that IRE provides a 2dB improvement in SNDR when compared to disabling the additional levels.

Table 2.2 summarizes the ADC performance. The ADC consumes 4.8mW from a 1.3V supply at 50Msps, requiring no additional area or power for the ADC references. Fig. 2.36 shows the power breakdown for the ADC prototype. It can be seen that the reference path consumes only 15% (310μW) of the Stage I power. A significant portion of the power consumed by the reference path goes into generating the reference timing signals, whose power will scale with technology.

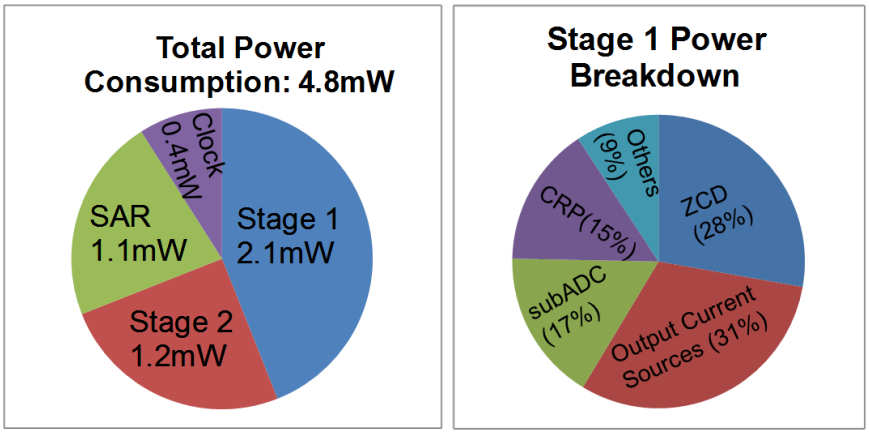

Figure 2.36: Power Breakdown

Figure of Merit Comparison

Table 2.3 compares the performance of this prototype with state-of-the-art ZCB designs. However, most published ZCB do not include the (external) reference buffer power in their FOM calculation. Reference buffers can consume a significant amount of power in typical ADC realizations: e.g., 6.2mW in [14], 4mW in [15], and 4.8mW in [16]. The presented work has a good FOM, and when the power consumed by the references is taken into account, its FOM_{TOT} stands out among other ZCB designs.

Fig. 2.37 compares the FOM of recently published ADCs [13] with $f_s > 40$Msps and SNDR > 60dB. The ADCs [8, 9, 35, 36] are zero-crossing based pipelines. [9] uses 1nF of on-chip reference decoupling capacitance to achieve the required reference path performance, while [8, 35] do not include the power consumed by the reference buffer. [36] has an on-chip reference buffer. [28] is a two-stage Pipeline-SAR ADC, which also does not include the reference buffer power. [37] is an oversampled converter which includes the reference path power in its FOM calculation. [38] makes use of background digital calibration to achieve its performance and to the best of our

Table 2.3: Comparison to State-of-the-Art ZCB Designs

		[9]	[8]	[35]	[36]	[10]	**This work**
Fs (Msps)		50	100	50	100-200	40	**50**
SNDR (dB)		62	63	68.1	63.7^{+}	59.7	**66**
Power (mW)	ADC Core	4.5	6.2	4.93	-	-	-
FOM_{SIG} (fJ/step)		88	53	47.5	-	-	-
Power (mW)	Ref. Buffer	-*	*4***	*4***	-	-	-
	Total	4.5	*10.2*	*8.93*	8.8^{+}	4.5	**4.8**
FOM_{TOT} (fJ/step)		88	*88*	*84*	137	142	**57**

$^{+}$Estimated at 50Msps from Fig. 9 in [36] and SNDR at 35MHz
*ADC has 1nF of on-chip reference decoupling capacitance
**Based on [15]

knowledge does not seem to include the reference buffer power. It can be seen from Fig. 2.37 that the presented work has an excellent FOM, even though all of the competitive designs do not include the reference path power in their FOM calculation.

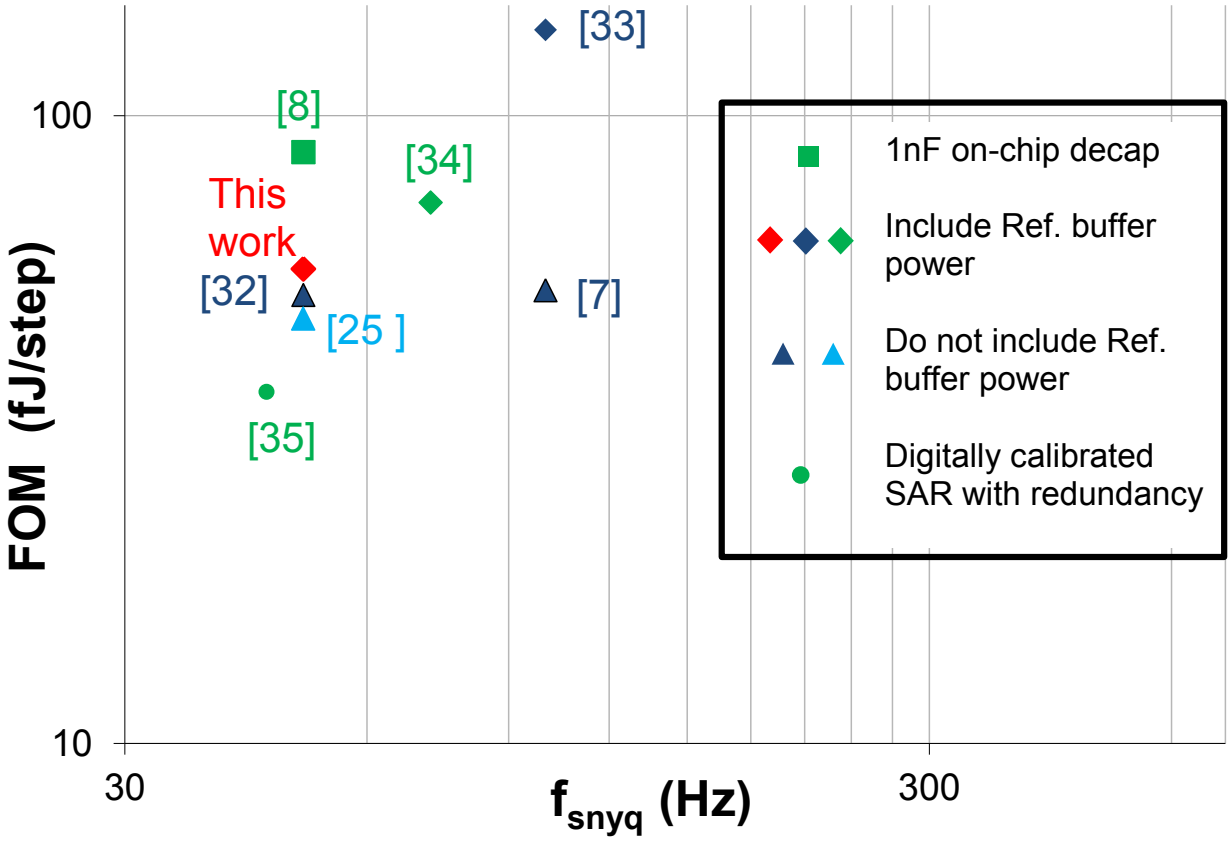

Figure 2.37: FOM comparison to $f_s > 40$Msps and SNDR > 60dB ADCs in [13]

Chapter 3

Radiation-hard Dual Channel Pipeline ADC for CERN Calorimetric Readout

This chapter describes the design and performance of a radiation-hard dual channel 40 MS/s pipeline ADC prototype with extended dynamic range. The future evolution of this ADC is intended for the upgraded electronics in the ATLAS Liquid Argon Calorimeter readout. The current prototype is used to establish the analog performance of the pipeline, to study the radiation tolerance of the ADC design and to determine the optimal gain selection procedure to be implemented in the future version of the chip.

3.1 Background

The Large Hadron Collider (LHC) at CERN in Geneva has been operational for physics research since 2010 [39]. In this proton-proton collider, designed to operate at center of mass energies of

7–14 TeV, the high luminosities ($> 10^{34}$ cm^{-2}s^{-1}) produce an intense radiation environment that the detectors and their electronics must withstand.

The ATLAS detector [40] is a multi-purpose apparatus constructed to explore the new particle physics regime opened by the LHC. The energy of the created electrons and photons is measured by a sampling calorimeter technique that uses liquid argon as its active medium. The front-end electronic readout of the ATLAS liquid argon (LAr) calorimeter consists of a combined analog and digital processing system [41]. To record the large dynamic range signals from the liquid argon calorimeter with high precision and to limit noise, a substantial portion of the electronic system is located on the ATLAS detector itself.

The LAr calorimeters of the ATLAS experiment have functioned with excellent reliability since installation in 2006 [42]. In 2012, they played a pivotal role in the observation of the Higgs boson, particularly in the diphoton and four electron channels [43]. Looking toward the future operation of the LAr calorimeters, there are several constraints: the existing front-end electronics limit the granularity, bandwidth and latency in the on-line event selection (level-1 trigger). Without modifications, the peak instantaneous luminosity of 3×10^{34} cm^{-2}s^{-1}, expected in the next few years, would force substantial increases in trigger thresholds. Additionally, the on-detector electronics, which are exposed to substantial radiation, are complex and contain many technologies, resulting in many potential opportunities for failure. The front-end electronics were qualified for radiation levels corresponding to 10 years of LHC operations [44]. The high luminosity running of the LHC (HL-LHC) [45], with instantaneous luminosities of 5×10^{34} cm^{-2}s^{-1} and an integrated luminosity of 3000 fb^{-1}, will exceed these design qualifications.

For the HL-LHC, planned for 2022, it will be necessary to upgrade all of the 1524 front end boards (FEBs), preparing the detector for the expected 3000 fb^{-1}. This replacement allows the design of a more flexible system that utilizes the full precision and granularity of the LAr calorimeters at trigger level and removes bandwidth and latency constraints. The simpler, "free running" architecture chosen results in an effectively infinite pipeline and bandwidth with little or no latency. This can be seen schematically in Figure 3.1, which shows the path of the signal from the detector to the data acquisition (DAQ) system. The new FEBs (upper left) will digitize the analog signals for all LHC bunch crossings. The data will be sent to an off-detector digital system, the Read Out Driver (ROD, upper right), that will provide input for a fully digital level-1 trigger system. The Liquid Argon Trigger Digitizer Boards (LTDB, lower left) and off-detector Digital Processing System (DPS, lower right) may then be used for a new level-0 trigger. Technically, the new FEBs require 40 MS/s digitization for all channels over a 16-bit dynamic range within the existing power, cooling and space constraints, and in a radiation environment. Thus, an important component of this upgrade is the creation of a suitable analog-to-digital converter (ADC). The ADC is shown in Figure 3.1 on the FEB, receiving the signal from the preamplifier-shaper, and also on the LTDB.

3.2 System Architecture

3.2.1 System Specifications

The ADC is designed to digitize the analog signal from a single calorimeter cell. The signal, a triangular pulse about 500 ns long, is first sent to a preamplifier and then split and again amplified

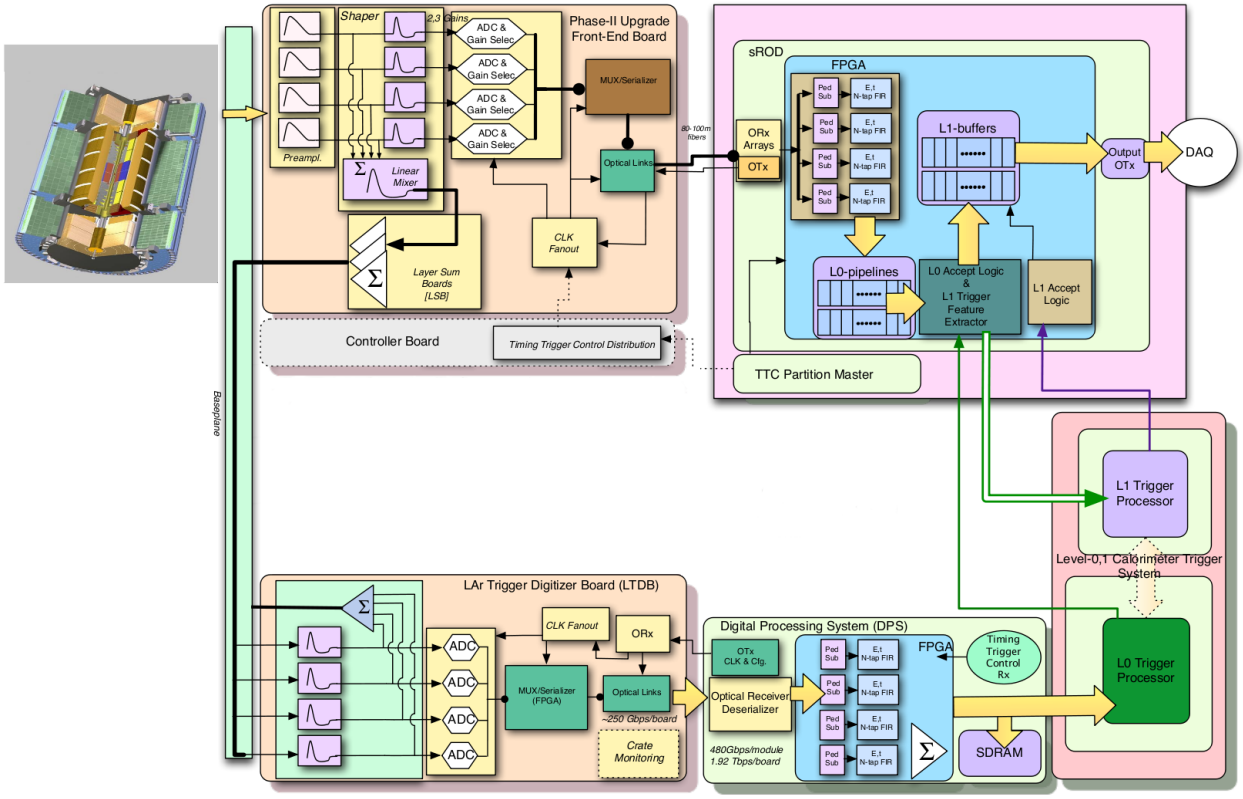

Figure 3.1: Block diagram for the proposed ATLAS Phase-II electronics upgrade. The ADC appears in the upper left box (FEB) and the lower left box (LTDB).

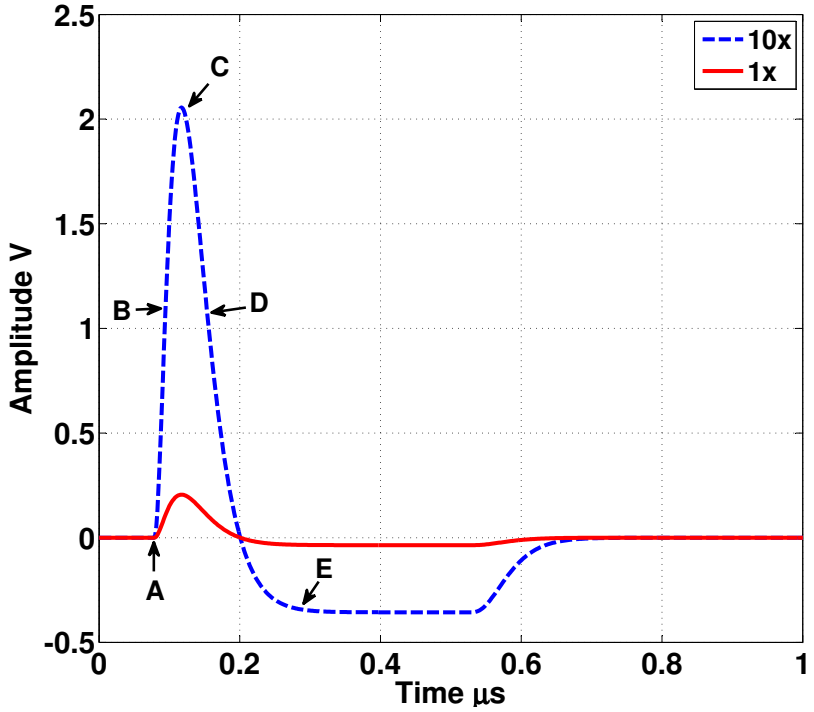

Figure 3.2: Pulse Shape with 1x (solid line) and 10x gain (dashed line).

by shaper chips to produce three pulses at overlapping linear gain scales, with gain ratios of approximately ten. Each signal is subject to a fast bipolar $CR-(RC)^2$ shaping function with τ = RC = 20 ns, resulting in a pulse shape similar to that shown in Figure 3.2 for the 1x and 10x gain channels. This pulse is sampled five times for digitization: typically one sample before the signal starts (point *A* in Figure 3.2), one during the rising edge (*B*), one at the peak (*C*), one during the falling edge (*D*) and one during the undershoot phase (*E*). With additional processing and calibration, the energy deposited in a particular calorimeter cell is determined based on these five samples.

The LAr calorimeter electronics upgrade must meet the following specifications:

- The calorimeter signals must be sampled and digitized at (minimally) a frequency of 40 MHz.

- The energy deposited in each calorimeter cell must be measured with a precision of better than 0.25% at high energy.
- A dynamic range of approximately 16 bits is needed to cover the energy range of interest, from a lower limit of approximately 50 MeV set by pile-up noise [41] up to a maximum of 3 TeV.
- 128 ADC channels must fit on a board 490 mm $\times$ 409.5 mm.
- The ADC must use less than 100 mW per channel.
- The ADC must be radiation tolerant to $\sim$ 1 MRad and have low single effect sensitivity.

This combination of requirements is not currently available commercially. The chip discussed in this paper is a proof-of-principle demonstration of a design meeting these specifications.

3.2.2 Radiation Tolerance

The radiation in the ATLAS detector is dominated by secondary particles produced by interactions of the primary particles with the detector elements. As a result, at the electronics location, the energies are rather low (less than a few GeV), the fluxes are high, and the direction of the radiation fields is homogeneous. The dominant radiation flux consists of photons and neutrons. Also contributing to the radiation are charged hadrons (mainly protons and pions). A high level of reliability of the electronics must be maintained during the estimated ten years of operation of the experiment. As mentioned in Section 3.2.1, the ADC needs to be radiation tolerant to $\sim$1 MRad.

The decrease in Total Ionizing Dose (TID) effects in thin oxide gates of MOS devices has been shown in [46, 47]. Although technology scaling has resulted in the gate oxide getting thinner, and hence less susceptible to TID damage, the Shallow Trench Isolation (STI) oxide of modern CMOS technologies ultimately limits the radiation tolerance of conventional CMOS circuits. It is possible with Hardness-By-Design layout techniques to eliminate this limitation and eventually push the radiation tolerance of circuits to the high level allowed by the thin gate oxide. The radiation hardness of IBM's 130 nm CMOS process for digital design has been shown [48] for both thin oxide and thick oxide MOS devices to a few tens of MRads. A key decision while implementing the ADC prototype is the choice of the power supply. The thin-oxide 130 nm devices have a rated supply of 1.2 V. The ADC chip is required to interface with the shaper chip, which will probably be implemented in a SiGe process with a supply of 3.3 V, and hence interfacing this signal to a 1.2 V domain will require attenuation and/or complicated level shifting. Signal attenuation from a 3.3 V regime to a 1.2 V regime will increase the noise requirements of the ADC. Also, implementing analog circuits in a 1.2 V supply is more challenging due to the reduced voltage headroom, which makes it infeasible to cascade MOS devices on top of each other. To address these issues, the prototype ADC is implemented on a supply of 2.5 V using thick-oxide devices. Although it was seen [48] that thin oxide devices are more radiation tolerant, thick oxide devices are still comfortably tolerant at the radiation levels required for this application ($\sim$ 1 MRad). The allowable input signal swing of the ADC is 2.4 V_{p-p} differential, which relaxes the noise requirements of the ADC. Measurement results in a radiation environment, on a previous design of a sample and hold amplifier in the same technology, showed that standard good analog layout practices were

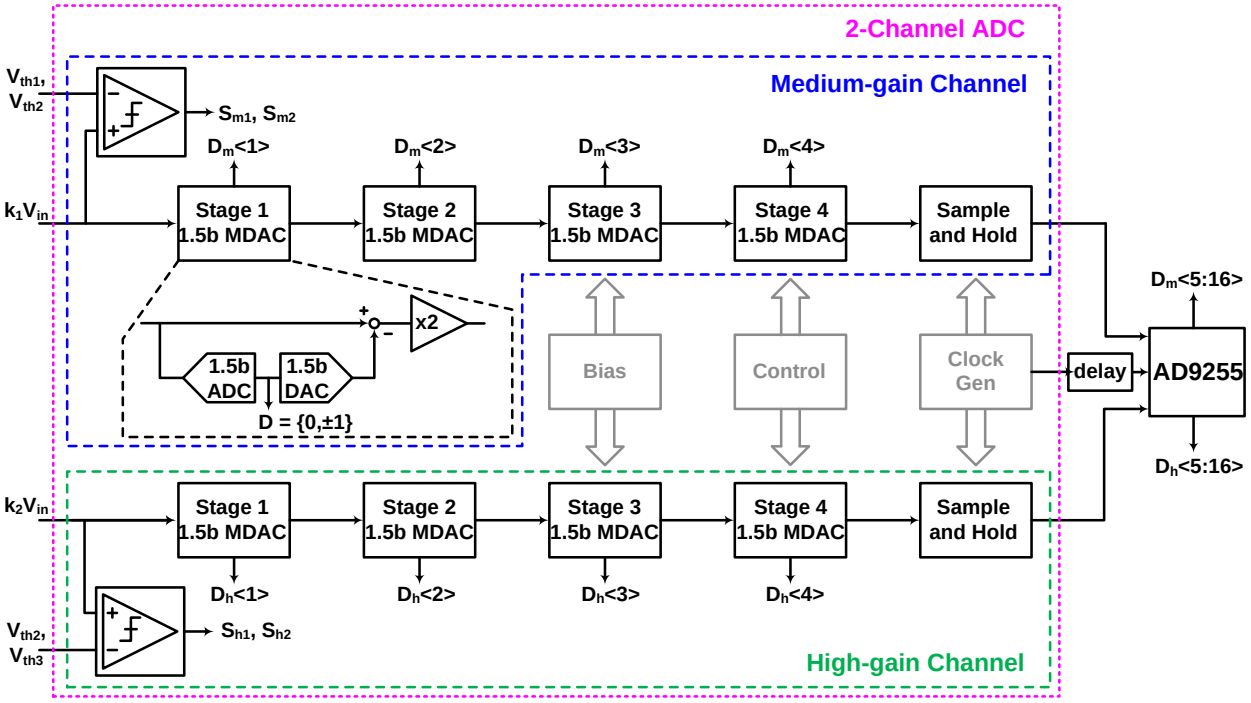

Figure 3.3: Prototype architecture.

sufficient to achieve the necessary radiation tolerance [49]. The measured radiation tolerance of this chip is discussed in Section 3.3.

3.2.3 Prototype Implementation

The goals of the current prototype are to establish the analog performance of the pipeline stages, to study the radiation tolerance of the ADC design and to determine the optimal gain selection procedure to be implemented in the future version of the chip. The system prototype architecture, shown in Figure 3.3, consists of two identical 12-bit 40 MS/s Pipeline ADC channels. The two channels, namely Medium Gain and High Gain, are fed with $k_1 V_{in}$ and $k_2 V_{in}$ respectively, where the gain factors k_1 and k_2 are provided by off-chip drivers and are nominally one and ten respectively.

This two-channel system prototype, with four MDAC (Multiplying Digital-to-Analog Converters) stages each, provides enough flexibility to test various gain selection algorithms to increase the effective system dynamic range (explained in Section 3.4). Each ADC channel in the current prototype consists of four MDAC stages with a gain of two each. Each MDAC stage resolves one bit, followed by a times two residue amplification. The three possible output codes ("1.5 bits") allow for the digital error correction. The analog residue of the fourth and final MDAC stage needs to be further resolved to 8-bit accuracy to determine the final 12-bit ADC word. This analog residue is fed to an on-chip Sample and Hold amplifier, which drives an external commercial 12-bit ADC (AD9255 [50]) for further digitization, i.e. to determine the eight least significant bits. In the current prototype, for simplicity, all MDACs are identical. Power scaling will be done in the final design to reduce the total chip power consumption. The implementation details of the ADC are further explained in the following sections.

MDAC Implementation[1]

Figure 3.4 shows the architecture of the 1.5-bit MDAC stage used in the pipeline ADC [51]. Further details on the implemented digital correction are explained in Section 3.2.3. The MDAC consists of a flip-around architecture with the input V_{in} sampled onto the sampling capacitors C_s and the flip-around capacitors C_f, during the sampling phase ϕ_s. Nominally, C_s and C_f are equal. In order to improve the linearity of the input sampling network, bottom-plate sampling, which uses an advanced version ϕ_{se} of the sampling phase, is implemented. At the beginning of the hold

[1]The MDAC design was done in collaboration with Jaroslav Ban of Nevis Laboratories, Columbia University.

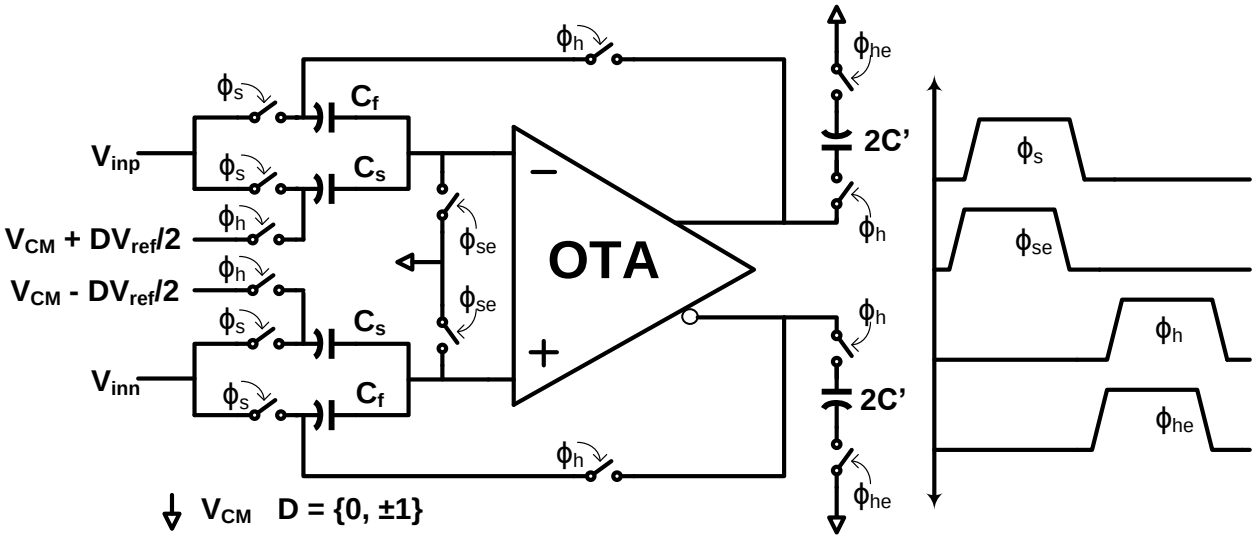

Figure 3.4: 1.5b MDAC stage (subADC not shown); ϕ_s/ϕ_h - sample/hold phase; ϕ_{se}/ϕ_{he} - advanced version of ϕ_s/ϕ_h; V_{CM} - common-mode voltage; V_{ref} - reference voltage; D - subADC decision.

phase ϕ_h, depending on the subADC decision D, the reference V_{ref} is appropriately connected to the capacitors, thus performing the required MDAC operation given by

$$V_{out} = 2V_{in} - DV_{ref} \tag{3.1}$$

where $D = 0, \pm 1$ is the subADC decision.

Fig. 3.5 shows a single unit of the subADC consisting of a flash comparator and an input sampling network. The separate sampling network of the subADC obviates the need for an Sample-and-Hold amplifier at the ADC input. The flash comparator is sized to comfortably meet the subADC offset requirements. Additional logic to perform gain calibration is included on-chip. MiM (Metal-insulator-Metal) capacitors are used because of their better matching and higher density in the given process. In order to avoid device reliability issues in a radiation environment,

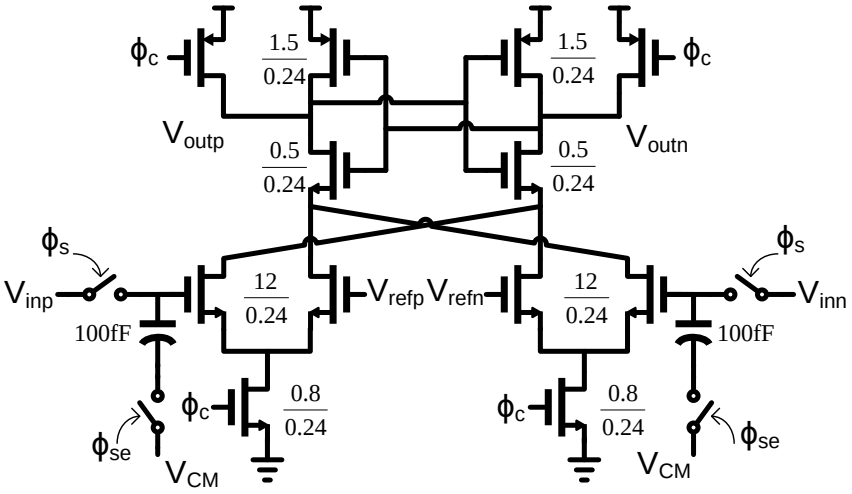

Figure 3.5: Single subADC unit; ϕ_s - sample phase; ϕ_{se} - advanced version of ϕ_s; ϕ_c - subADC comparison phase; V_{CM} - common-mode voltage; V_{refp}/V_{refn} - reference voltage.

clock gate boosting is not employed for the input sampling switches, which also avoids the need for triple well devices. Instead, bottom-plate sampling, along with appropriately sized thick-oxide transmission-gate switches, was found to satisfy the 12-bit linearity requirements at 40 MS/s.

OTA

Figure 4.1 shows the fully differential OTA (Operational Transconductance Amplifier) used in the MDAC (bias circuits not shown), along with the transistor sizes. The OTA consists of a single stage gain-boosted folded cascode amplifier with an NMOS input pair. The load capacitance of the OTA forms the dominant pole. Care is taken to make sure the pole-zero doublet formed by the gain-boosting amplifiers falls beyond the unit-gain frequency (UGB) of the OTA [52]. The boost amplifiers are also implemented as single-stage folded cascode amplifiers. The common-mode feedback amplifier A_1 is implemented as a PMOS differential pair with diode-connected NMOS

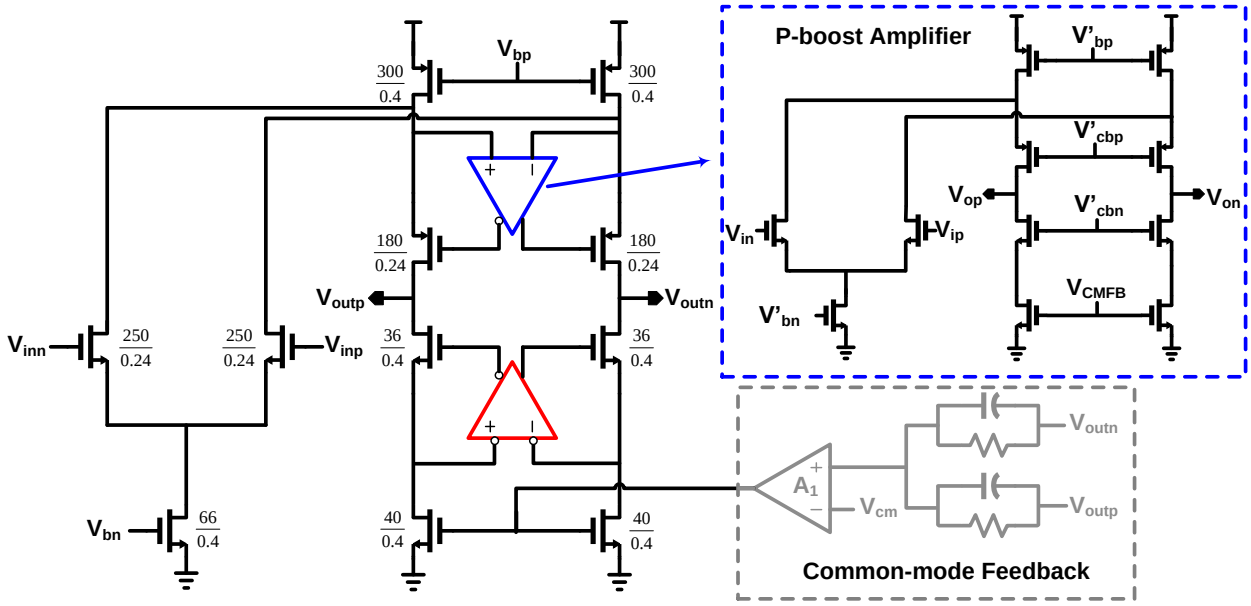

Figure 3.6: Folded-cascode OTA; V_{cm} - common-mode voltage; V_{CMFB} - common-mode feedback voltage; $V_{bn}, V'_{bn}/V_{bp}, V'_{bp}$ - NMOS/PMOS bias voltage; V'_{cbn}/V'_{cbp} - NMOS/PMOS cascode bias voltage; All dimensions in μm.

loads. The OTA is designed for a DC gain of 80 dB and a UGB of 450 MHz, thus providing enough margin for the targeted 12-bit performance at 40 MS/s.

Digital Gain Calibration

Foreground digital calibration is performed to correct for gain errors due to capacitor mismatch [3], exploiting the redundancy offered by the three possible codes produced to resolve one bit. Figure 3.7 shows the residue output V_{res} of the Stage 1 MDAC and the reconstructed output D_{out}, as a function of the input V_{in}, for an ideal MDAC and for an MDAC with gain error. Gain errors due to capacitor mismatch give rise to code jumps in the reconstructed output, as shown in Figure 3.7. The calibration algorithm consists of measuring the MDAC code jumps Δ by subsequent ADC stages and removing them digitally from the reconstructed digital output D_{out}. The calibration

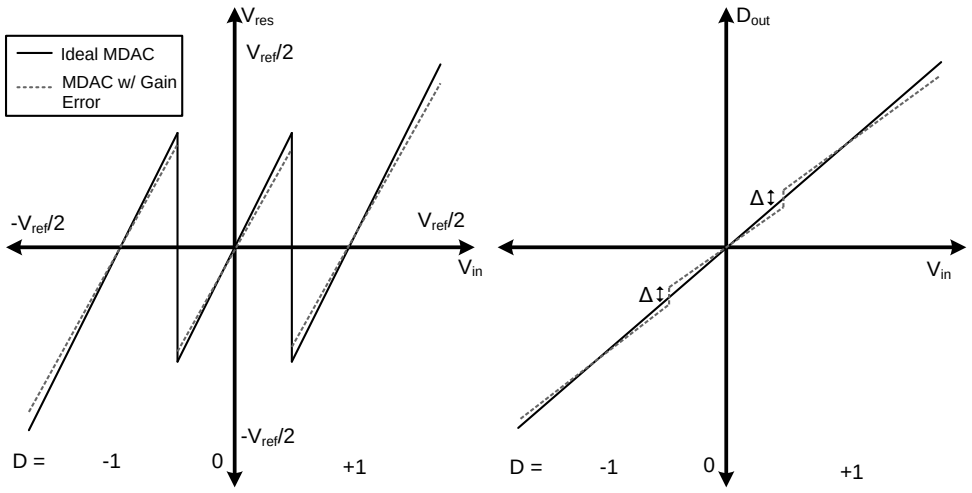

Figure 3.7: MDAC residue characteristic (left). Reconstructed output (right); V_{ref} - reference voltage; V_{res} - residue voltage; D - subADC decision; D_{out} - reconstructed output.

procedure starts with the last MDAC stage (Stage 4 MDAC in this prototype) and moves backward to calibrate the Stage 1 MDAC. An on-chip control register is used to put the ADC in calibration mode.

3.3 Measurement Results[2]

Figure 3.8 shows the die photograph of the 2-channel ADC prototype [53]. The chip occupies 6 mm^2. A 160 MHz sinusoidal clock is fed into the chip and divided down to generate the required 40 MHz clock phases. Going on-chip with a higher frequency clock reduces the jitter contribution due to the clock distribution path. To characterize the dynamic performance of the ADC, an input sinusoidal signal is filtered and fed to the commercial ADC input driver AD8138 which performs

[2]The measurement results were obtained in collaboration with Tim Andeen, Leu Zhou and Jaroslav Ban from Nevis Laboratories, Columbia University

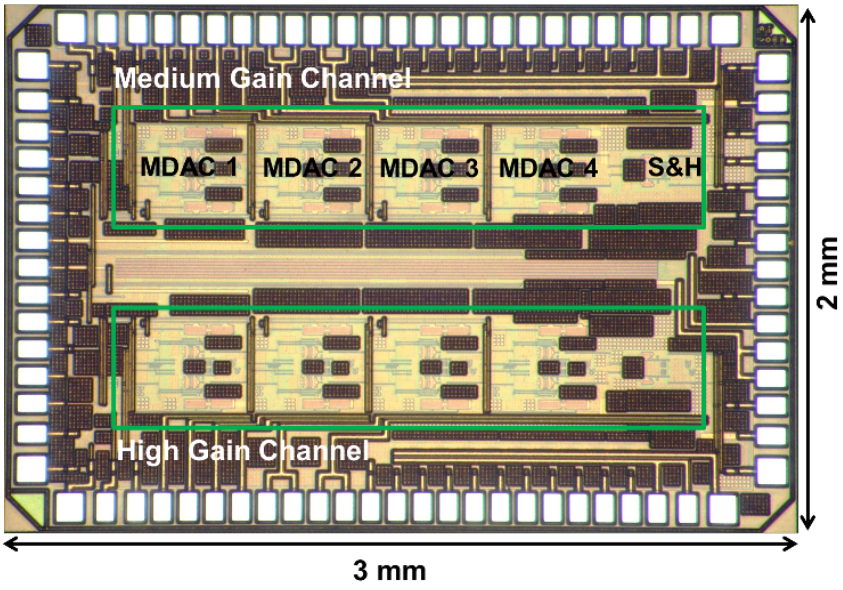

Figure 3.8: ADC die photograph

single-ended to differential conversion. The signal is split and sent to both the ADC prototype and the commercial ADC (AD9255). The analog residue from the prototype ADC is fed to a different channel of the commercial ADC for further digitization. The digital outputs from the prototype chip and the external ADC are collected by an on-board FPGA and all data processing is done offline.

3.3.1 ADC Performance

Both ADC channels were characterized extensively before and after irradiation.

Figure 3.10 shows the output Fast Fourier transform (FFT) of a 10 MHz input sine-wave before and after digital calibration. Calibration improves the spurious-free dynamic range (SFDR) from 52.7 dB to 77.8 dB while the signal-to-noise and distortion ratio (SNDR) improves from 49.8 dB

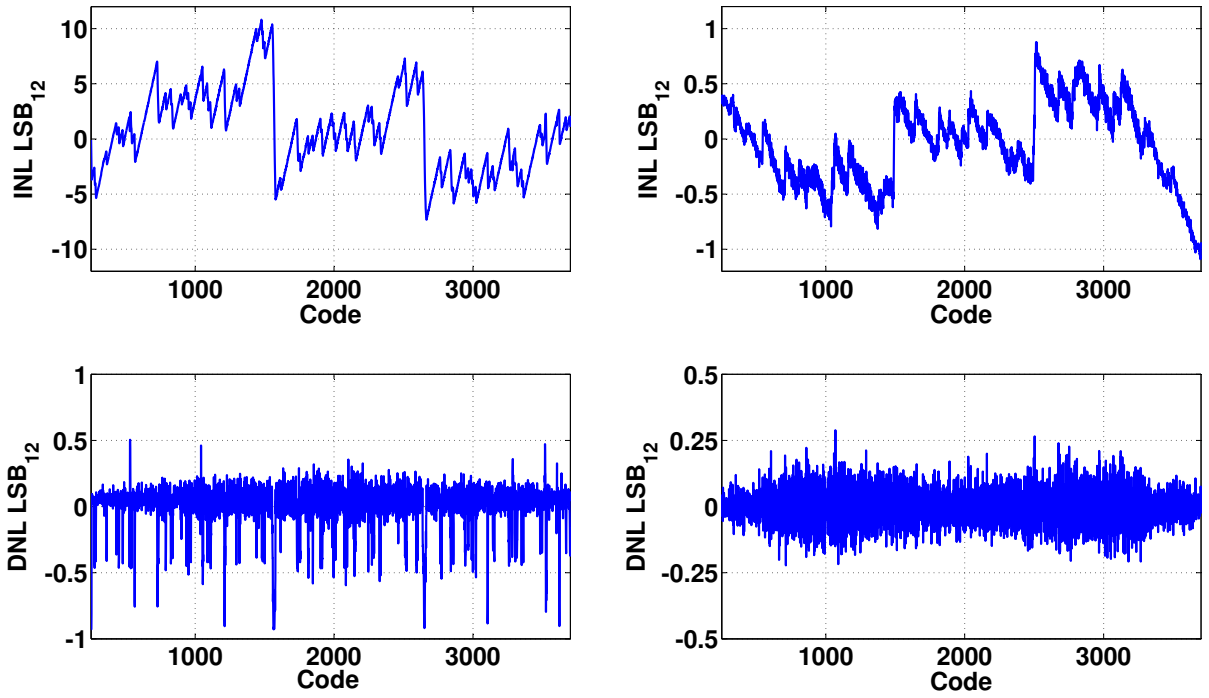

Figure 3.9: INL/DNL at 40 MS/s (*Chip 1*): (left) before calibration, (right) after calibration.

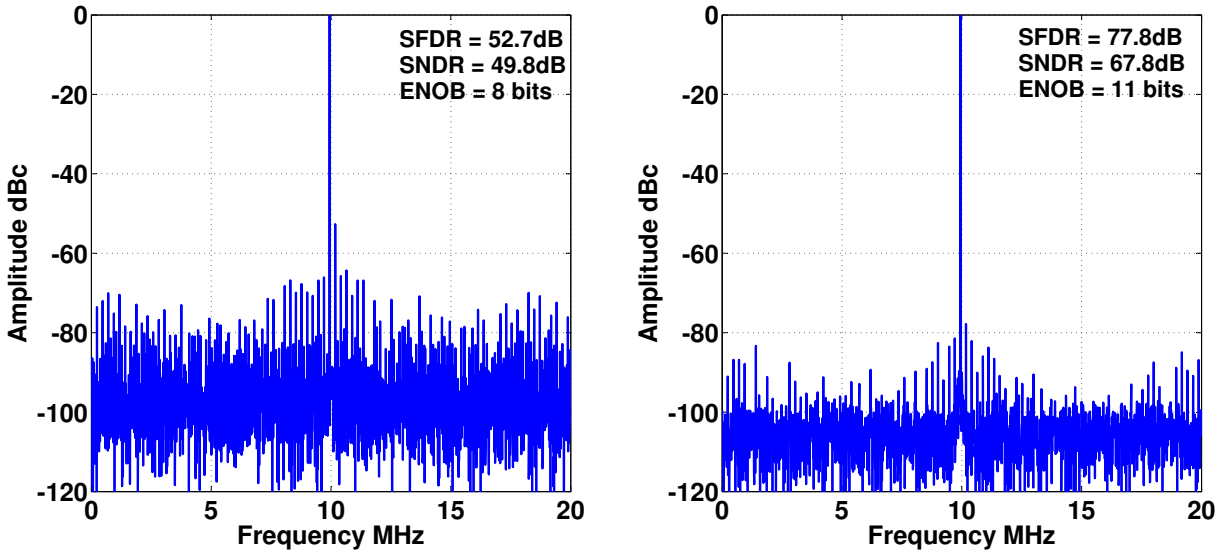

Figure 3.10: FFT for f_{in} = 10MHz (*Chip 1*): (left) before calibration, (right) after calibration.

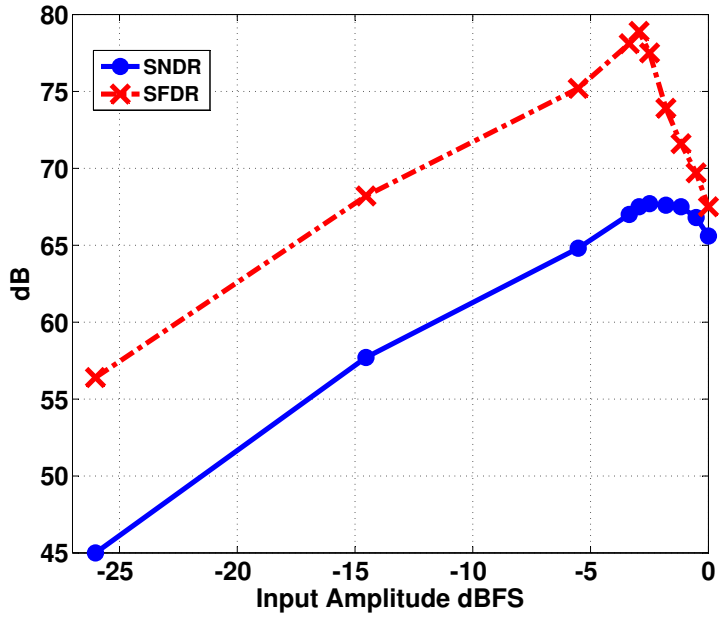

Figure 3.11: Dynamic performance vs. input amplitude (10MHz) (*Chip 1*).

to 67.8 dB. The effective number of bits (ENOB) at 10 MHz for the calibrated channel is 11-bits. The number of valid codes was limited to 3452 as the commercial ADC that further digitizes the analog residue limits the maximum input signal to 85% of the ADC prototype's full-scale, giving an effective resolution of 11.7-bits. Each MDAC stage consumes 11 mW from a 2.5 V supply. Since all stages are sized identically, the total analog power consumption of the chip is 55 mW per channel (4 identical MDAC stages followed by a Sample and Hold).

Figure 3.11 shows the SNDR and SFDR as a function of the input amplitude. As mentioned earlier, the valid input range of the on-board commercial ADC limits the maximum allowable input swing to the chip and hence the SNDR peaks at -2 dBFS.

To determine the crosstalk between the two ADC channels, the input to one of the channels was grounded while a full-scale sine-wave was applied to the other channel. Figure 3.12 shows

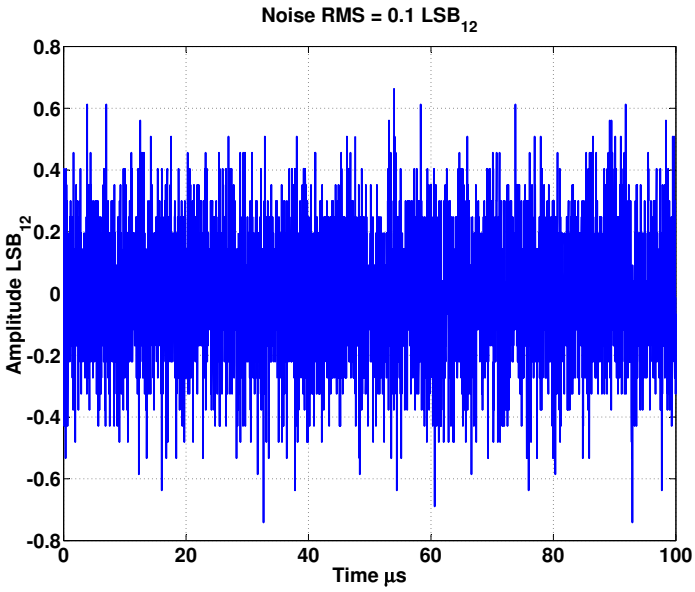

Figure 3.12: Crosstalk on Medium gain channel.

the output of the grounded channel. The RMS noise is 0.1 LSB RMS, showing no indication of crosstalk between the two channels.

3.3.2 Irradiation

To test the radiation tolerance of this ADC design, five chips were taken to the Massachusetts General Hospital Francis H. Burr Proton Therapy Center. Two of these (chips 1 and 2) had been fully characterized and showed excellent performance. The other three were selected using a socketed board (figure 3.13). This board provided power and a clock signal to the ADC. To confirm that the chips operated as expected, a pure sine wave signal was given as input (2 V_{p-p}) and the analog residue was observed on an oscilloscope.

To replicate the high radiation flux in the ATLAS detector, four of the chips were irradiated

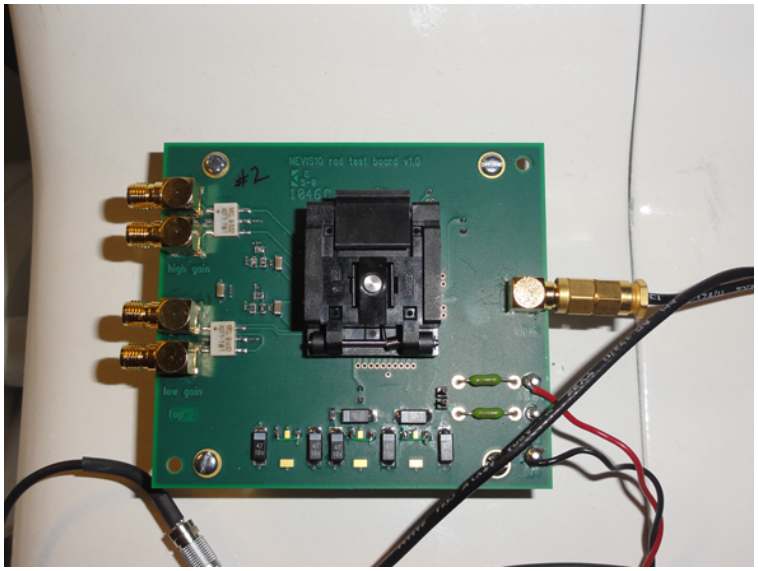

Figure 3.13: Test Board for Irradiation

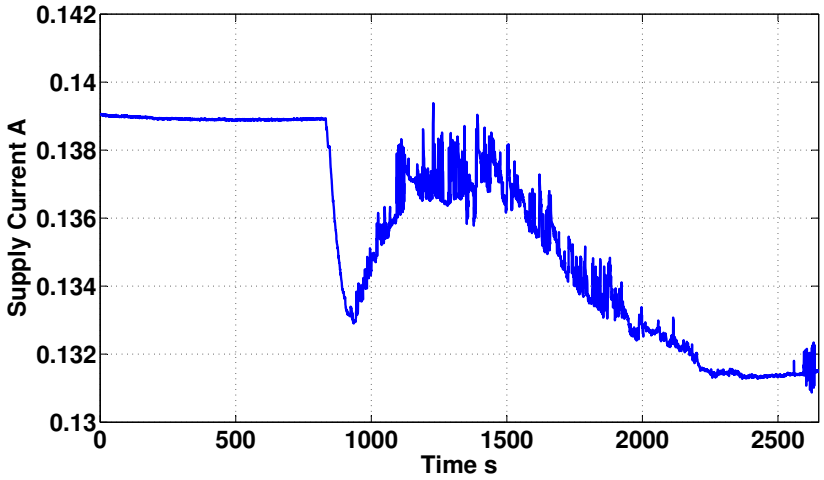

Figure 3.14: Current consumption variation during irradiation. Note the vertical scale. 2500 s corresponds to a dose of 5 MRad.

Table 3.1: Measurements of ADC performance before and after irradiation in a 227 MeV proton beam at f_{in} = 10 MHz.

Chip No.	Proton/cm^2	MRad	SNDR dB Pre/Post Irrad.	SFDR dB Pre/Post Irrad.	ENOB Pre/Post Irrad.
1	1.01 x 10^{14}	5.33	67.8/67.7	73.6/77.8	11/10.9
2	2.01 x 10^{14}	10.70	67.5/67.6	73.3/73	10.9/10.9

using the 227 MeV proton beam. During the irradiation, the chips were powered and a clock signal was applied, while the current drawn by the chip was monitored. Table 3.1 lists the dose for the two chips which received the largest dose. No further measurements were done using the three other chips which received smaller doses, given the performance of the high dose chips. In Figure 3.14, the current over the course of one test is seen to be relatively constant, between 0.13 and 0.14 A. The drop observed at about 900 seconds shows the beam turn on. The slight rise and fall of the current which follows is due to the heating of the chip as it is irradiated.

In order to confirm the operation of the ADC immediately after irradiation, a pure sine wave signal was again applied to the ADC input and the analog residue was observed on an oscilloscope. None of the chips ceased operation during the tests. After two months to ensure the chips became safe to handle, the two chips (chips 1 and 2) were re-mounted on the test boards and fully retested.

3.3.3 ADC Performance Post-irradiation

After irradiation the performance measurements were repeated and the results are shown in Table 3.1. The calibration constants, computed through the digital calibration routine, did not change after irradiation. Figure 3.15 compares the dynamic ADC performance before and after irradiation as a function of the input signal frequency, showing the radiation-hard nature of the design.

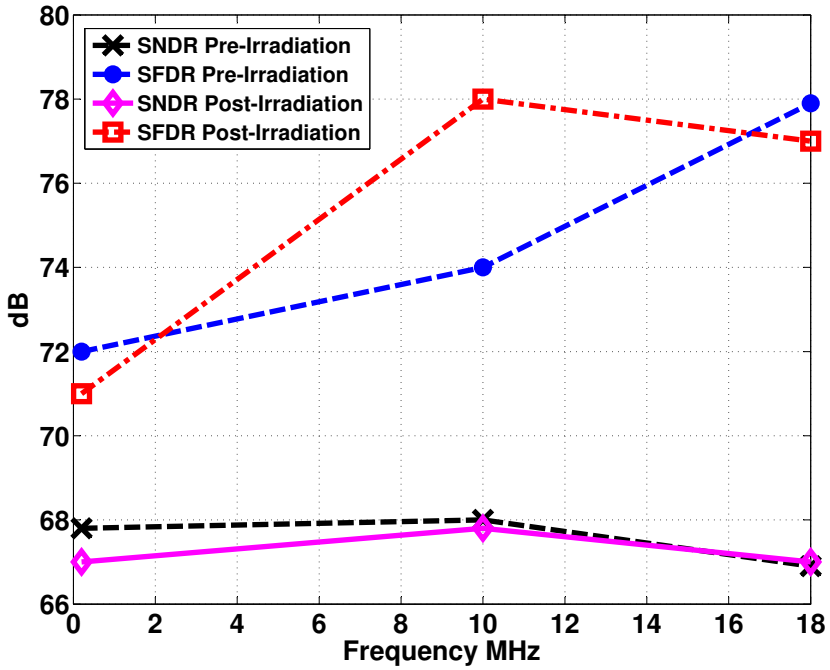

Figure 3.15: Dynamic performance before and after irradiation (5 MRad) (*Chip 1*).

3.4 Gain Selection

In the current detector, the 16-bit dynamic range with 12-bit precision requirement is met by using three analog gain channels. The three gain channels (each separated by a factor of approximately ten) are sampled by a 144-sample deep analog pipeline at 40 MHz [54]. An external trigger system identifies the bunch crossing of interest. When such a bunch crossing is identified, five samples for each gain are digitized with 12-bit precision, followed by digital gain selection. A particular channel is said to be saturated if its signal exceeds a certain threshold. Once saturation is detected, any signal from that particular channel is ignored for $\sim$ 500 ns (due to the recovery time required for the conditioning circuits in the signal path) and the data from the next lower unsaturated gain channel is used.

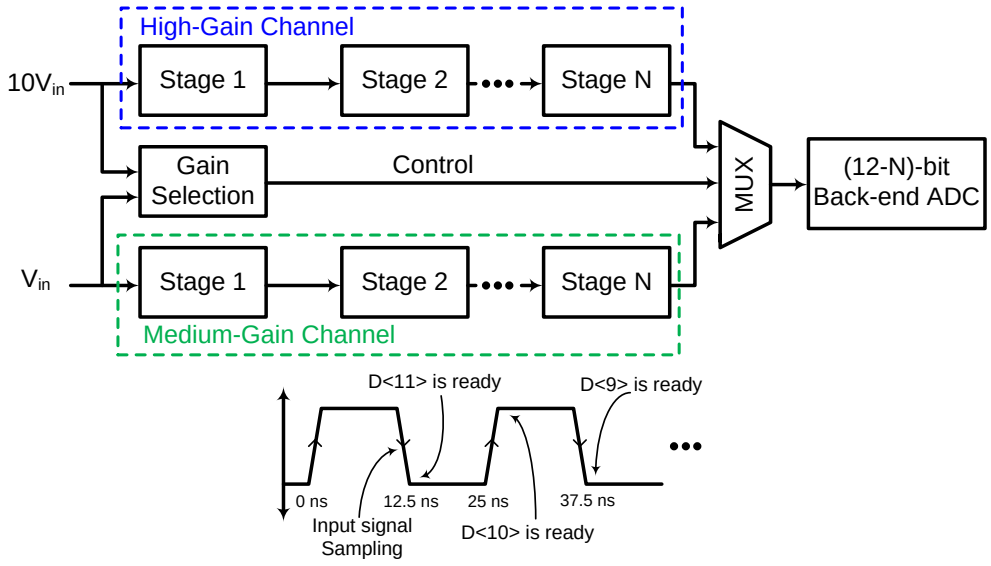

Figure 3.16: Gain selection system: D$<11:0>$ is the reconstructed 12-bit ADC output; D$<11>$ is the bit from Stage 1, D$<10>$ from Stage 2 etc.

For the upgrade, there will be no external trigger system and the data for all samples must be transmitted. This requires the ADC to sample the input at 40 MS/s and the optimal gain to be chosen on the fly.

Figure 3.16 shows the general block diagram of a system based on the current ADC prototype that implements gain selection. For simplicity, a two-channel system is shown. The ADC prototype is a pipeline architecture so the final reconstructed digital output is available only *after* a delay of a few clock cycles. Gain selection requires the detection of saturation in the high gain channel and then switching to the lower gain channel. The high and low gain channels are separated by a factor of ten, similar to the existing architecture.

A simple solution uses a single discriminator (comparator) on the sampled signal in front of the highest gain channel, which imposes a switch to a lower gain input if the signal is too close to

saturation (based on a single sample). This approach requires two sample and holds at the ADC input, one for a $1\times$, medium gain channel and one for a $10\times$, high gain channel, resulting in a sample depth of one (the OTA for the Stage 1 MDAC can be shared between the two sample and holds). This implementation of gain selection leads to limited precision at the onset of large signals, due to the limited bandwidth of the sampling network and the shape (width) of the signal. The signal from a saturated (high gain) channel can have a very high slew rate, which may result in a large error for the sampled value. Since the value for the sampling capacitor is set by kT/C noise requirements [55], the size of the sampling switches determines the input bandwidth. The switches in the ADC input sampling network are sized to sample a full-scale sine-wave signal at the Nyquist frequency of 20 MHz. Larger switches increase power consumption on the clock drivers. The maximum slew rate of the input signal that can be sampled with the required 12-bit accuracy is given by

$$\text{Maximum Slew Rate } SR_{max} = V_{FS}(2\pi f_{max}) \tag{3.2}$$

where $V_{FS} = 1.2$ V, $f_{max} = 20$ MHz for the current design, and therefore $SR_{max} = 1.5 \times 10^8$ V/s.

Figure 3.17 shows two different pulse shapes with their respective slew rates. For simplicity, the input signal is assumed to be saturated if it is larger than the ADC full-scale of ± 1.2 V. The signal is said to be slightly saturated if it just goes above the ADC full-scale, and highly saturated if it is very much larger. In practice, protection diodes prevent the ADC input signal from going much beyond the supply voltage of 2.5 V. The value of the highly saturated signal at 10 ns in Figure 3.17 is still *within* the ADC full-scale range. However, the slew rate of the highly saturated pulse is

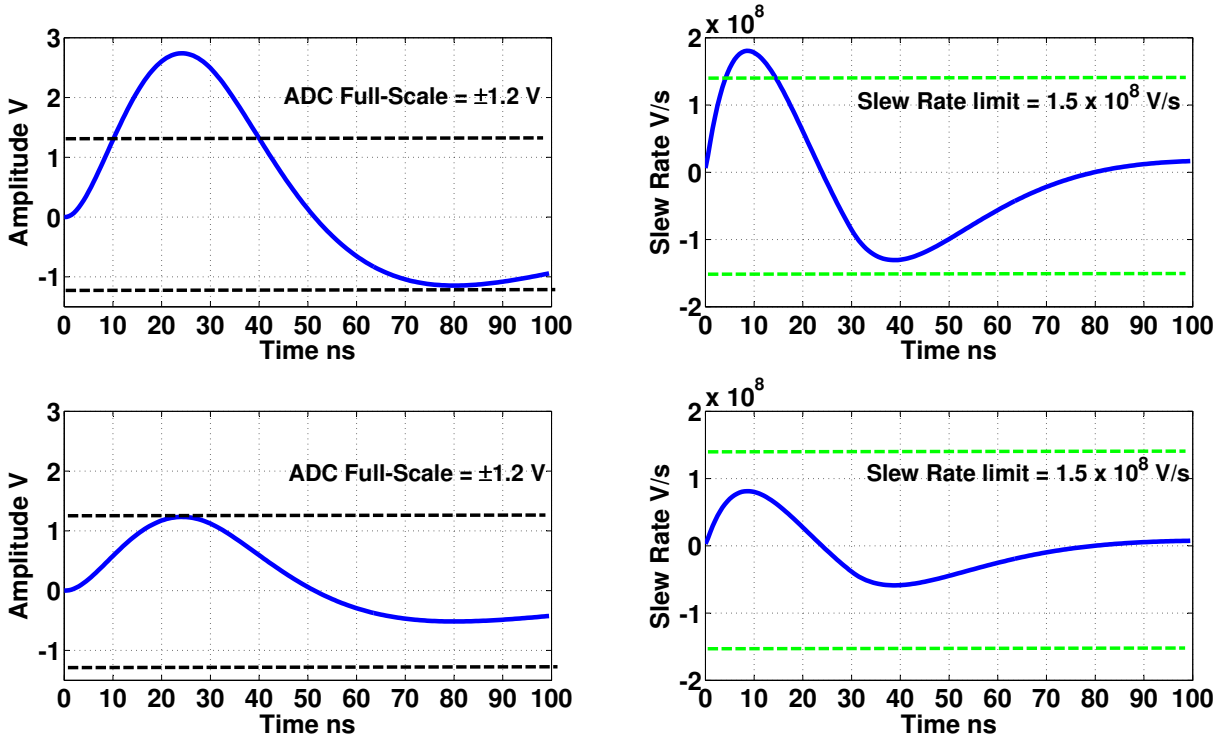

Figure 3.17: High gain channel output with a highly saturated pulse (top-left), and corresponding slew rate (top-right). A slightly saturated pulse (bottom-left) and its slew rate (bottom-right) are shown for comparison.

larger than the maximal slew rate supported by the input sampling network SR_{max}. Therefore, the sampled value will be inaccurate. This illustrates how the solution of using a single comparator, at the input sample and hold, to detect saturation and then switching between channels, leads to limited precision.

A second solution is to switch to the lower gain if the signal saturates or the slew rate is too large. To implement this solution, the comparator, as described in the previous case can be used, but circuitry to determine the slew rate of the input signal needs to be added. If, at the sampling instant, the slew rate of the input signal is higher than a threshold, the lower gain channel samples are used for digitization. Since the slew rate is only used to switch between the gains, it does not need to be measured with 12-bit accuracy. However, it does determine the point where the gains switch, and thus the usable part of the dynamic range of the high gain channel. To ensure the correct gain channel is used, the switch to a lower gain should occur well before the signal in the high gain channel comes close to its maximum. The point at which this switch happens can be determined as a function of the slew rate accuracy and threshold. With a lower slew rate accuracy, a lower threshold is needed and hence more of the dynamic range of the higher gain channel is lost. These parameters could be adjusted for optimal performance. Due to the inherent pipeline delay, and the fact that adjacent input samples are 25 ns apart (the sampling clock is 40 MHz), a digital approach to determine the input signal slew rate is not feasible. Determining the slew rate in an analog fashion (using differentiators) with the necessary accuracy would require complex circuitry and could significantly increase the power consumption.

A simple and robust solution, which is independent of the signal shape and slew rate, is to

detect saturation with a comparator in front of the first stage of the high gain channel (as before). When saturation is detected, the N samples in high gain channel stages 1 to N are ignored. The lower gain channel is then used to digitize the N samples before saturation was detected, as well as the future samples. This procedure requires a memory depth of $N > 1$ (as shown in figure 3.16). By ignoring the N samples before saturation in the high gain channel, the samples that may suffer from limited precision due to the high slew rate are avoided.

3.4.1 Gain Selection Measurements

In the prototype chip, two discriminators are implemented for each gain (00: signal saturated with negative value, 01: signal within range, 11: signal saturated with positive value). The discriminator memory is implemented outside the chip for flexibility in the study of the gain selection algorithm. It is necessary to determine the minimum depth of the discriminator memory required for the gain selection algorithm. As the gain selection is made only after a certain number of sampling clock cycles, the length of discriminator memory defines the length of the parallel analog pipelines for the signal path, i.e. the number of parallel MDACs which must exist in the final chip to do the gain selection.

The setup used for the gain selection experiments is shown schematically in Figure 3.18. A pulse generator is used to generate an approximation of the signal from a calorimeter cell. The pulse is then subjected to a fast bipolar $CR-(RC)^2$ shaping and injected into the medium and high gain channels through two amplifiers. As shown in Figure 3.3, each ADC channel has two comparators at its input to perform gain selection.

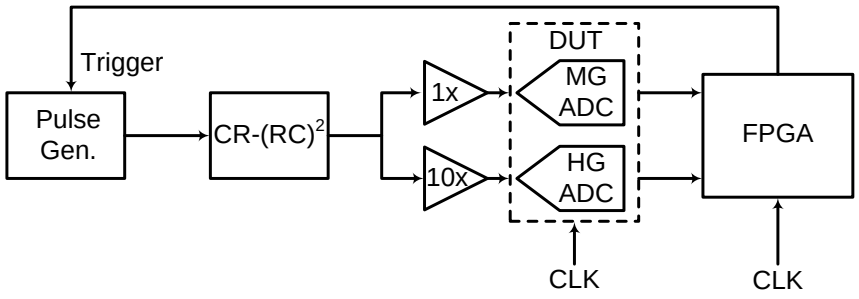

Figure 3.18: Measurement setup for gain selection.

For the gain selection study, the phase of the pulse generator was synchronized to the ADC sampling clock through the FPGA, with an option to change the phase of the input signal with respect to the sampling clock, making a fine reconstruction of the pulse shape possible. Figure 3.19 shows reconstructed pulse shapes measured by the medium-gain and high gain channels with $\tau = RC = 20$ ns.

To verify the operation of the gain selection setup and to confirm the depth of the discriminator memory required to perform the gain selection detailed above, the following procedure was followed:

- The output of the high gain channel is collected continuously and the gain selection comparators are used to determine if the high gain is in saturation.
- Without the signal, the background mean μ and standard deviation σ of the channel output (in terms of the ADC LSBs) are determined. The start of the pulse is defined as the first sample which is $\mu + n\sigma$ above the background, where n is varied from one to three.
- If the high gain channel is saturated, the number of samples from the start of the pulse until

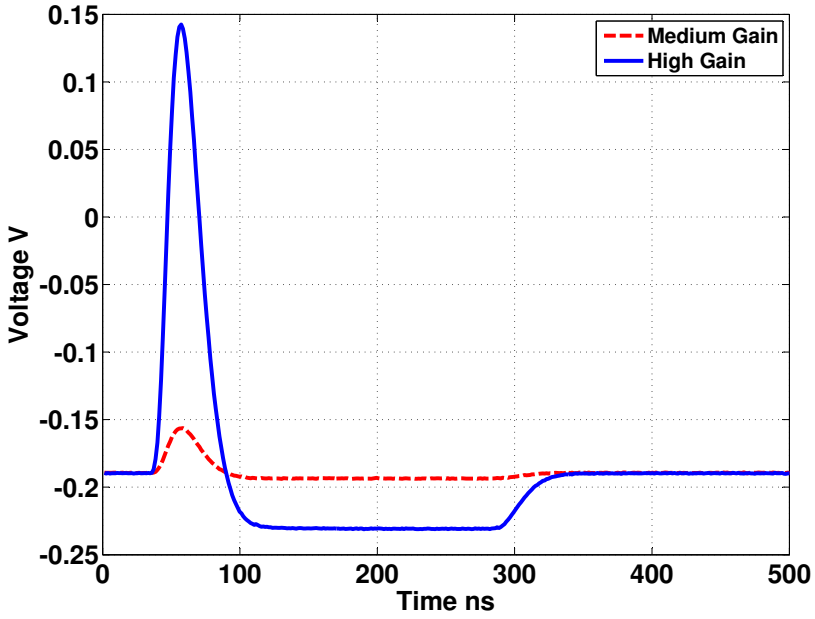

Figure 3.19: Reconstructed medium and high gain pulses.

saturation is noted. For the simpler approach, this gives the depth N of the required discriminator memory and hence the depth of the required analog pipeline (number of parallel MDACs).

In the first experiment, a high amplitude signal with a fast rise time was applied to the high gain channel to saturate it fully. This is similar to the situation in the top row of Figure 3.17. Figure 3.20 shows the required memory depth for two different phase relationships between the pulse shape and the ADC sampling clock. As can be seen from the figure, at most three points need to be stored.

In the next experiment, a signal was applied to the high gain channel with an amplitude that was just over the saturation point of the high gain channel (as in the bottom row of Figure 3.17).

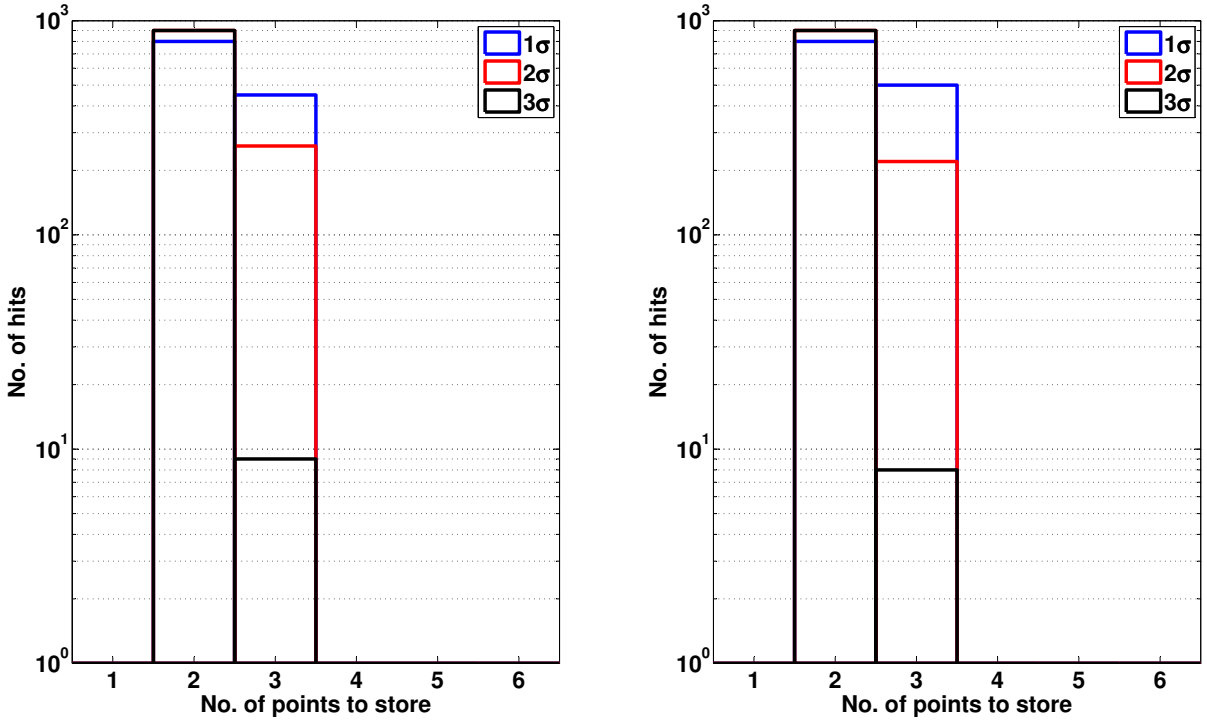

Figure 3.20: Required memory depth for a highly saturated signal when pulse and sampling clock are: (left) in phase, (right) out of phase by 12.5 ns. The curves are labeled by $n \times \sigma$, the threshold used to determine the start of the pulse.

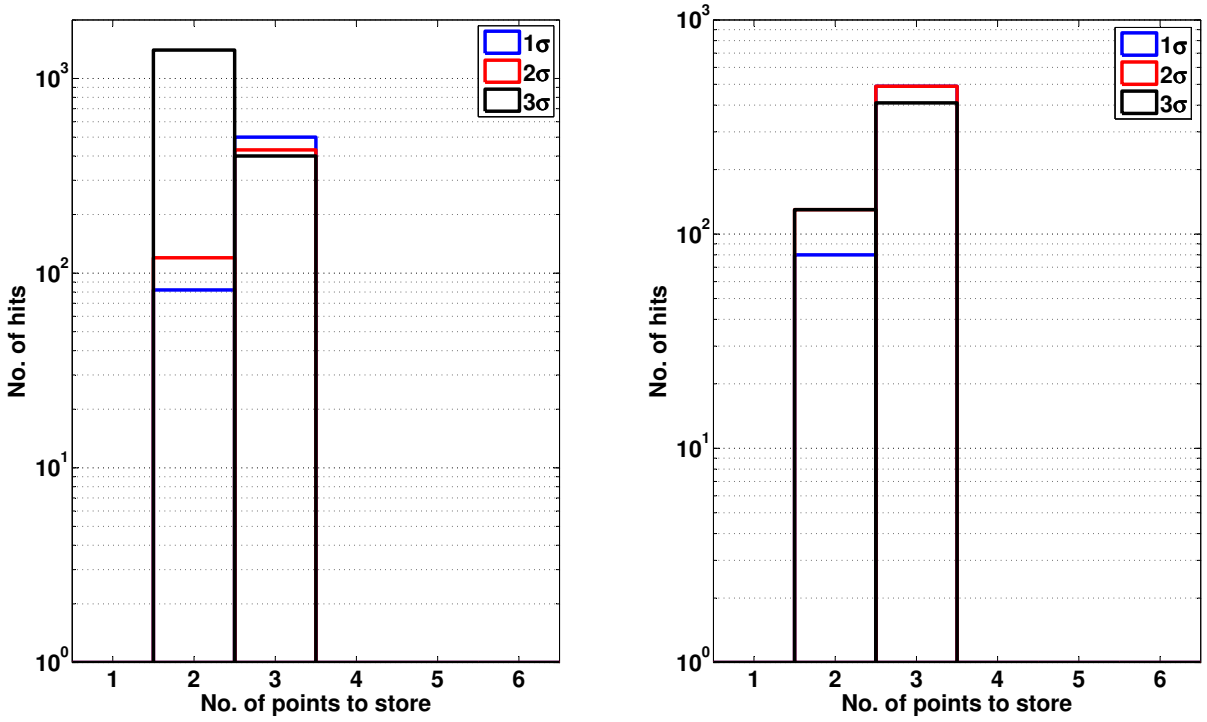

Figure 3.21: Required memory depth for a slightly saturated signal when pulse and sampling clock are: (left) in phase, (right) out of phase by 12.5 ns.

Figure 3.21 shows the required memory depth for two different phase relationships between the pulse shape and the ADC sampling clock. As before, the required memory depth is three samples. From Figures 3.20and 3.21, the maximum memory depth required for τ = RC = 20 ns is three samples.

The time constant τ of the pulse can vary from one calorimeter cell to another due to variations in the cell capacitances. Figure 3.22 shows the required depth for two different pulse shapes with $\tau = 10$ ns and $\tau = 40$ ns. The maximum required memory depth can be as high as four samples. These tests confirm that a memory depth of four samples is sufficient to avoid problems associated with slew rates of the input signal and to perform accurate gain selection.

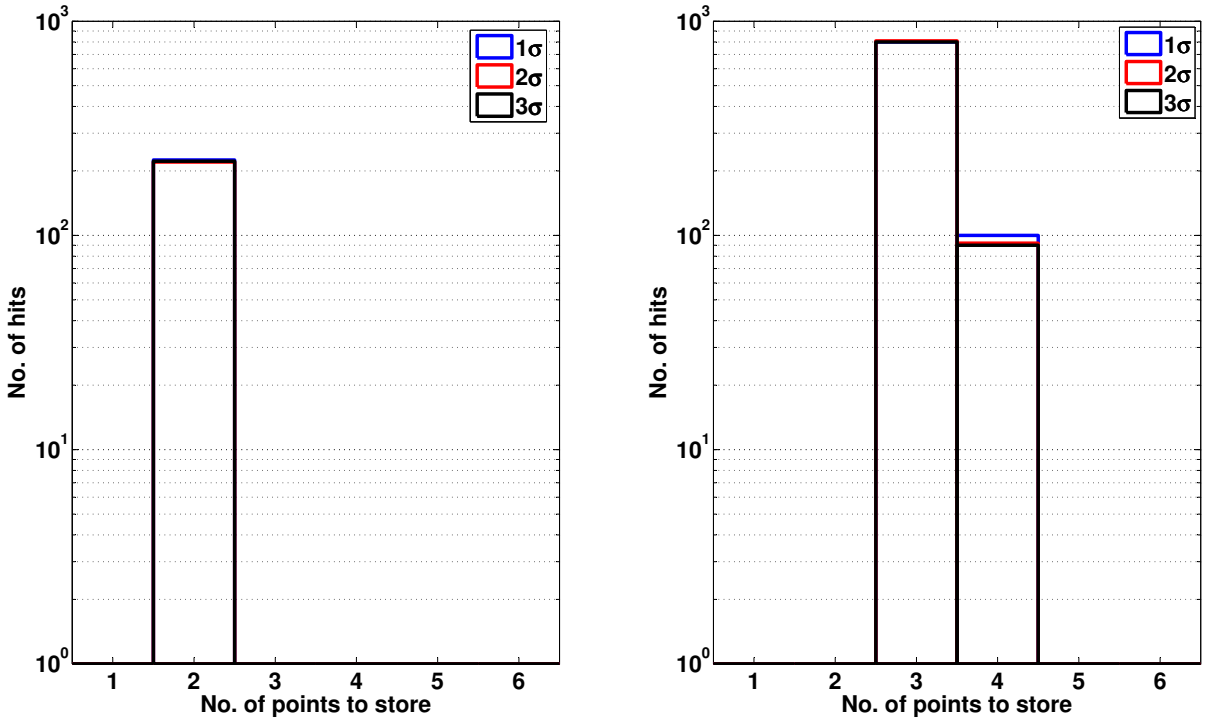

Figure 3.22: Required memory depth for: (left) $\tau = 10$ ns: (right) $\tau = 40$ ns.

3.4.2 Gain Selection Algorithm

The various possibilities for performing the gain selection are:

1. **Fully Digital Gain Selection**: Implement three complete ADC channels, one for each of the three gains, with the gain selection performed after the digitization is complete. The final ADC word that is transmitted contains the digital word from the appropriate channel and its gain scale. This leads to three independent 12-bit ADC channels per 16-bit dynamic range. For a quad-ADC, this adds challenges in terms of crosstalk, power and clock distributions.

2. **Partial Digital Gain Selection**: Implement three partial ADC channels, sharing the back-end stages using an analog multiplexer. In this case, each gain channel would have a certain number of independent MDACs stages, followed by an analog multiplexer that enables the three channels to share the back-end stages. In order to meet the 16-bit dynamic range requirement, three partial channels, each with four independent MDACs followed by an analog MUX and a common back-end, are required to perform the gain selection.

3. **Single 16-bit Dynamic Range ADC**: Implement one 16-bit dynamic range ADC channel with 12-bit precision. The ADC noise performance needs to be 16-bit accurate while the linearity needs to be only 12-bit accurate. This solution avoids gain selection entirely as there is only a single ADC channel. To meet the 16-bit noise requirements, the input sampling capacitance of the ADC would need to be > 70 pF, presenting a very large capacitive load to the ADC input signal driver. Also, the power of the first stage MDAC would need to be increased dramatically to achieve the required 16-bit performance. However, the additional

power required by the 16-bit channel over a 12-bit channel is offset by reducing the number of external amplifiers and full or partial ADC channels from three to one.

The primary advantage of the fully digital approach is its flexibility. and the fact that it is independent of the signal shape In the partial channels approach, the memory depth depends on the signal shape. Since in a conventional pipeline ADC successive pipeline stages are progressively smaller and lower power, the amount of area and power savings provided by reusing the back-end stages in the partial channels approach is small. Furthermore, the chip complexity is not very much reduced when compared to the fully digital approach. For these reasons, a fully digital gain selection is a promising approach for future implementations.

3.5 Summary

The design of a radiation-hard dual-channel 12-bit 40 MS/s Pipeline ADC with extended dynamic range was presented, for use in the readout electronics upgrade for the ATLAS Liquid Argon Calorimeters at the CERN LHC. The ADC was confirmed to be radiation tolerant beyond the required specifications. Various gain selection experiments were performed with the prototype to investigate possible gain selection procedures for future implementations of this design.

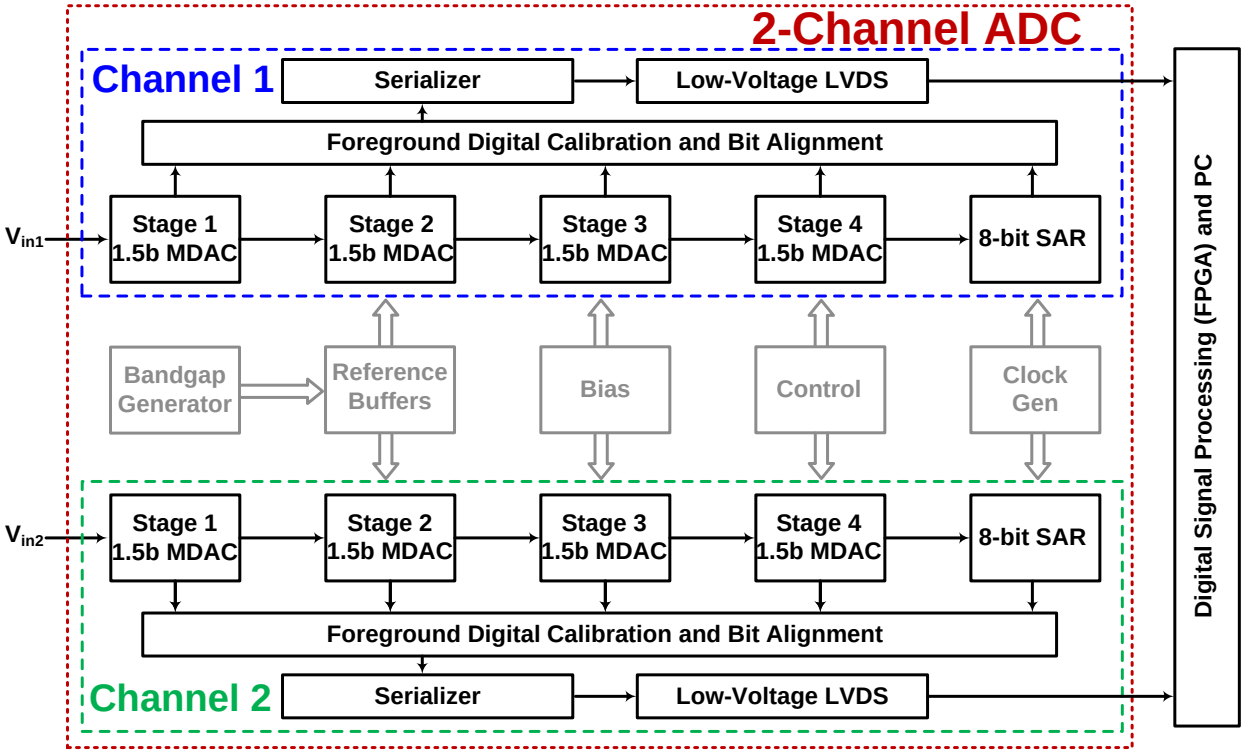

Figure 3.23: Block diagram of 2-channel 12-bit 40MS/s Pipeline ADC.

3.6 2-Channel 12-bit 40MS/s Pipeline-SAR ADC[3]

As the next version of the ADC prototype, a complete 2-channel 12-bit 40MS/s Pipeline-SAR ADC was designed. Fig. 3.23 shows the block diagram of the 2-channel ADC prototype. Each channel consists of 4 MDAC stages, similar to the previous prototype. An 8-bit 40MS/s Successive Approximation Register (SAR) ADC replaces the lower-order stages of the Pipeline ADC beyond the 4^{th} stage in a power-efficient manner. The 4 MDACs in the ADC are scaled for power optimization.

The 8-bit SAR is a synchronous design, whose comparator timing is controlled by a externally-

[3]The design was done in collaboration with Jaroslav Ban of Nevis Laboratories, Columbia University.

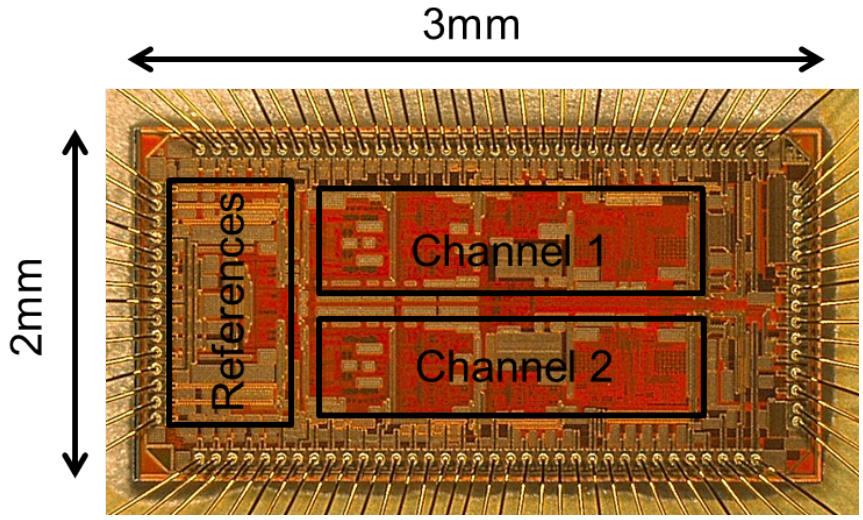

Figure 3.24: Die photo: 2-channel Pipeline-SAR ADC.

fed 640MHz clock. The raw bits of the MDAC stages and the SAR are collected by the on-chip Digital Processing Unit (DPU), which performs bit-alignment and on-chip foreground digital calibration. The calibrated bits are then fed to the serializer that is fully synthesized using digital logic and driven off-chip using a Low-Voltage DIfferential Signaling (LVDS) Driver [4]. A 640MHz clock is required for the serializer and LVDS timing, which is the same clock used for the SAR timing.

The ADC consists of complete reference generation and distribution. A band-gap reference[5] is used to generate a 0.6V reference from which all reference voltages required by the chip are generated.

The dual channel ADC was fabricated in IBM 130nm CMOS process. Fig. 3.24 shows the ADC die photograph which measures $6mm^2$. The dual-channel ADC was bonded in a QFN 72-pin package, mounted on a socket and tested on a PCB, as shown in Fig. 3.25. The data from the LVDS

[4]The LVDS IP block was provided as part of the design kit
[5]IP block was provided by CERN designers.

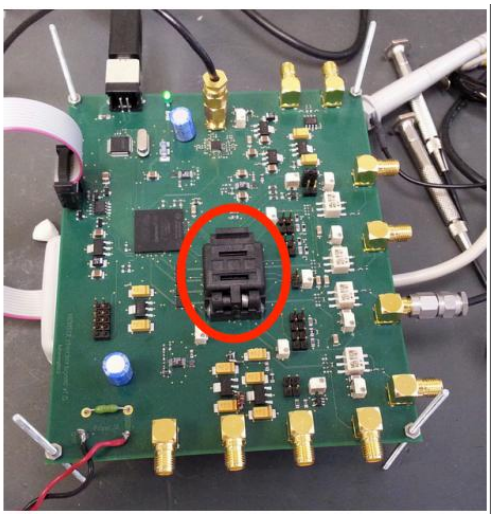

Figure 3.25: ADC test setup.

drivers are collected by the on-board FPGA, de-serialized and sent to the PC for further processing. Foreground digital calibration of MDAC stage gains is performed by the on-chip digital processing unit.

3.6.1 Measurement Results[6]

Fig. 3.26 shows the output FFT of a single channel, after foreground digital calibration, for a 10MHz full-scale input sinusoid. The ADC has an SFDR, SNDR, SNR and ENOB of 79dB, 67dB, 69dB and 11-bits at 10MHz.

To evaluate the radiation hardness of the dual-channel ADC design, the ADC was soldered onto the specially designed board shown in Fig. 3.27. The radiation test PCB measures 10 inches by 4.5 inches. It is desired to continuously monitor the ADC performance while the chip is being irradiated. In the previous version of the prototype, the ADC performance during irradiation could

[6]The measurement results were obtained in collaboration with Tim Andeen, Rex Brown and Jaroslav Ban of Nevis Laboratories, Columbia University.

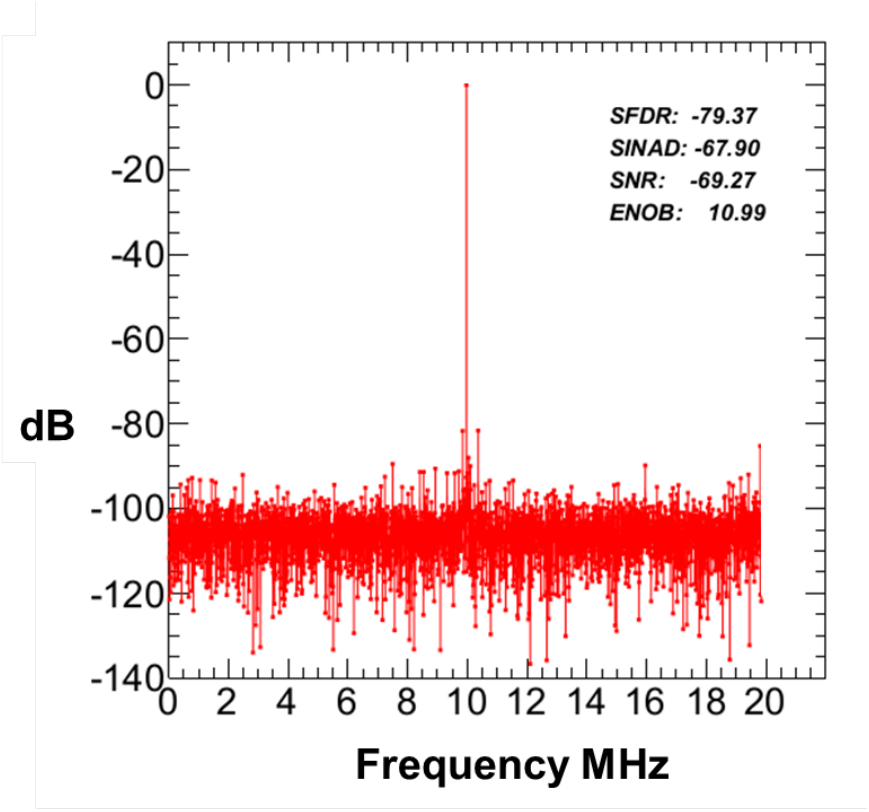

Figure 3.26: Single channel output FFT for 10MHz input signal.

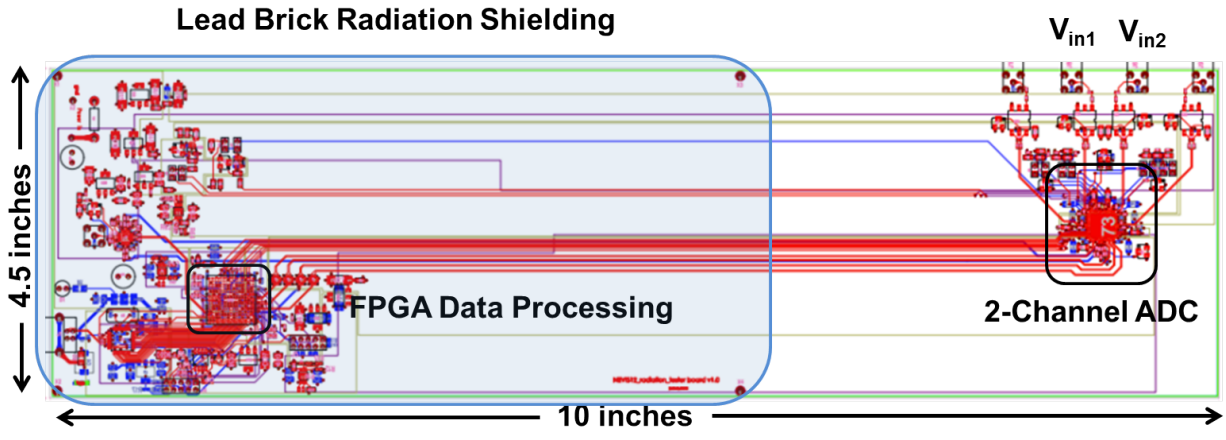

Figure 3.27: ADC radiation test PCB layout.

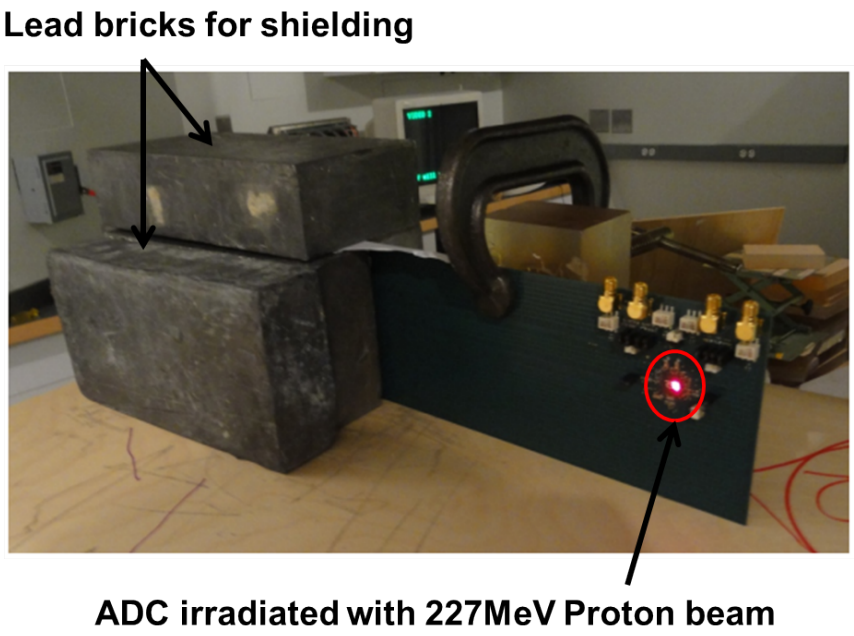

Figure 3.28: ADC radiation test setup.

not be monitored. The ADC is soldered onto one corner of the board, while all the auxiliary circuits needed for data processing like the FPGA, PC-USB control chips etc. are mounted on another corner of the board. The ADC is irradiated by a 227MeV proton beam, while the auxiliary circuits (FPGA, control chips etc.) which are not radiation hard are protected from the beam using thick lead bricks.

Fig. 3.28 shows the radiation test setup. The red dot on the board shows the 227MeV proton beam that is focused onto the ADC chip. The auxiliary circuits required for data collection and processing are shielded from the radiation within the thick lead bricks as shown. The ADC FFT performance during irradiation was continuously monitored using a PC.

Fig. 3.29 shows the ADC effective no. of bits (ENOB) during the course of irradiation. It can be seen that the ADC ENOB degrades only very gradually as the chip is being irradiated, thus

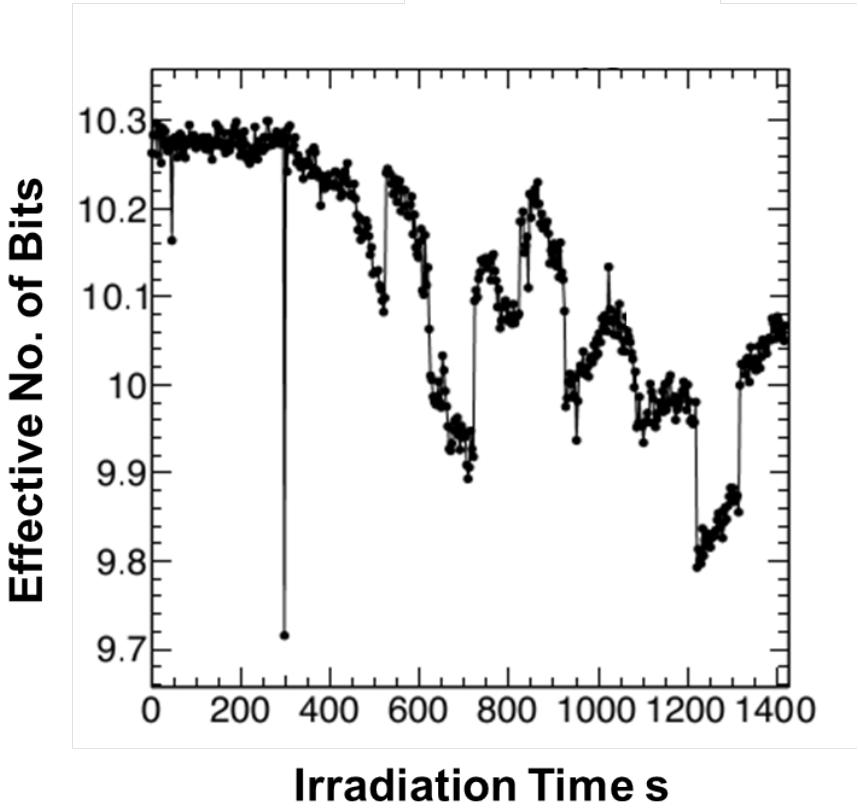

Figure 3.29: ADC radiation performance: Effective no. of bits (ENOB) as a function of irradiation time.

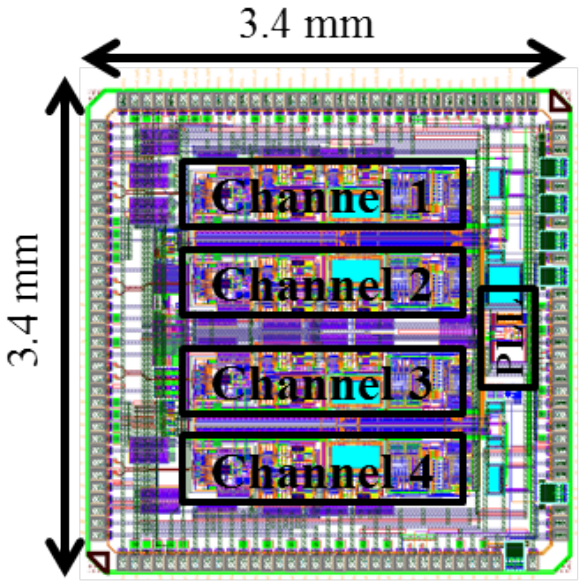

Figure 3.30: Layout photograph of 4-channel Pipeline-SAR ADC.

establishing the radiation hardness of the design[7]. The ADC was subjected to a total integrated radiation dose equivalent to more than 10 times that expected during operation of the LHC upgrade from the Phase-I upgrade in 2018 through the end of Phase-II around 2028.

3.7 4-Channel 12-bit 40MS/s Pipeline-SAR ADC[8]

The next version of the prototype was the design of a 4-channel 12-bit 40MS/s Pipeline-SAR ADC. Fig. 3.30 shows the layout photograph of the quad channel ADC. The chip has an integrated Phase-locked Loop (PLL) for high frequency (640MHz) clock generation and measures $13mm^2$.

[7]The sudden dip in ENOB at 300s is attributed to a bug in the data capture setup

[8]The design was done in collaboration with Jaroslav Ban of Nevis Laboratories, Columbia University.

Chapter 4

Ultra-Low Voltage Mixed-Signal Design: Switched-Mode Signal Processing[1]

This chapter introduces Switched-Mode Signal Processing, a new design paradigm that achieves rail-to-rail signal swings with high linearity at ultra-low supply voltages. Switched-Mode Signal Processing represents analog information in terms of pulse widths and replaces the output stage of OTAs with power-efficient rail-to-rail Class-D stages, thus producing Switched-Mode Operational Amplifiers (SMOAs).

4.1 Background

The powerful digital processing engines required in today's systems comprise a large fraction (by area) of the silicon integrated circuits (ICs) and thus dictate the direction of CMOS technology

[1]This work was done in collaboration with Baradwaj Vigraham of Columbia University.

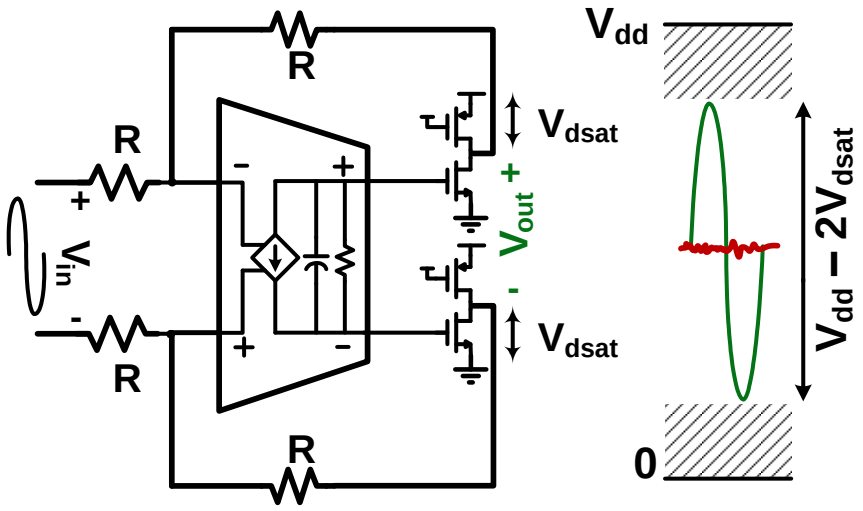

Figure 4.1: Typical 2-stage class-A OTA R-R feedback amplifier.

scaling. As the scaling continues, supply voltages (V_{dd}) and intrinsic gain of the transistors continue to drop rapidly and exhibit more *switch-like* operation, best suited for digital circuits. However, traditional voltage-mode analog circuits demand *current-source-like* operation and hence, scale poorer than digital circuits. This translates to higher power consumption and thus, lower battery life in the context of mobile communication. Specifically, representing signal information in *voltage-domain* is proving to be extremely challenging with reduced signal-to-noise ratios due to reduced supply voltages.

4.2 Limited Voltage Headroom in Scaled CMOS Technologies

The constant CMOS technology scaling, driven aggressively by digital circuits, has led to a steady decrease in the power supply voltage for analog circuits. This in turn has led to limited voltage headroom for the design of analog circuits. To illustrate the effect of supply scaling on the design

of conventional analog circuits, Fig. 4.1 shows a typical 2-stage class-A OTA configured as an R-R negative feedback amplifier. The amplifier consists of a 1^{st} stage integrator followed by a class-A output stage.

The maximum signal swing (single-ended peak-to-peak) V_{out} at the output of the amplifier is limited by the voltage headroom required by the output stage transistors which are biased in saturation. This maximum signal swing is limited to $V_{dd} - 2V_{dsat}$, with V_{dsat} typically 150mV or more. The voltage headroom required by the output stage severely limits the signal swing, which reduces from 1.5V at a supply of 1.8V to just 0.3V at a supply of 0.6V, a 5 times decrease in signal swing or a 13.5dB loss in maximum available signal power at 0.6V.

The power consumed by the amplifier of Fig. 4.1 is the sum of the power consumed by the 1^{st} stage integrator, which is noise-limited and dominates at low supply voltages (due to the limited signal swing) and the power consumed by the output stage, which is efficiency limited and dominates at high supply voltages. The power consumed can be shown to be [56]

$$P_{OTA} = P_{diss1} + P_{diss2} = 4kTB \times SNR \left(4\alpha + \frac{\beta V_{dsat}}{V_{pp}}\right) \frac{V_{dd}}{V_{pp}} \tag{4.1}$$

where SNR is the required signal to noise ratio at the amplifier output, α and β are circuit dependent proportionality constants, V_{pp} is the peak output signal swing and V_{dd} is the supply voltage. It can be seen from 4.1 that the power consumed by the 1^{st} stage integrator rises quadratically with reducing signal swing V_{pp}. Equally distributing the available noise margins between the resistors and OTA in the R-R amplifier of Fig. 4.1, the proportionality constants can be shown to be $\alpha = 4$ and $\beta = 32$.

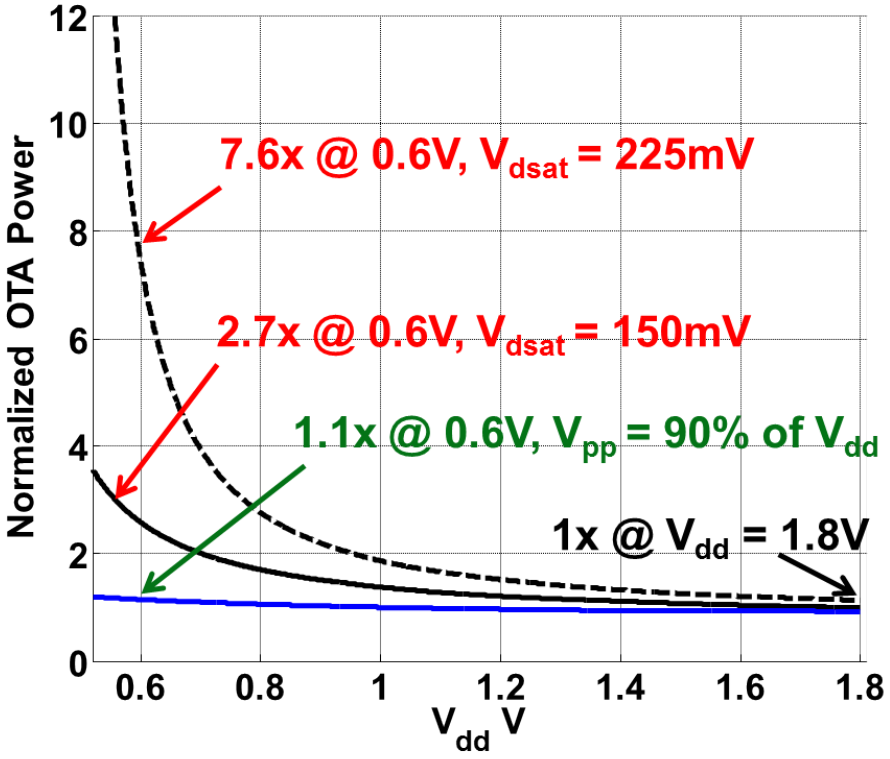

Figure 4.2: Amplifier power consumption as a function of the power supply voltage.

Fig. 4.2 shows the normalized power consumption of the OTA of Fig. 4.1, for a fixed SNR, as a function of the power supply voltage. It can be seen that for a V_{dsat} of 150mV, a 2.6 times increase in the OTA power consumption is required to achieve a particular SNR at 0.6V, when compared to the power consumption at 1.8V. Typically, the output signal swing of conventional OTAs is further backed-off due to distortion requirements. As can be seen from Fig. 4.2, for a V_{dsat} of 225mV, this required power increase shoots up to 7.6 times at 0.6V. Thus, limited signal swing at scaled supply voltages makes it very challenging to achieve high SNRs with a low power consumption using conventional analog design techniques.

4.3 Switched-Mode Operational Amplifiers (SMOAs)

SMOAs are introduced as a new class of time-domain based amplifiers that can achieve close to rail-to-rail swings in scaled supply voltages [57,58]. As shown in Fig. 4.2, if the amplifier is able to support a 90% supply signal swing at its output, then almost no extra power is required to achieve a particular SNR at low supply voltages.

The proposed SMOAs are 2-stage operational amplifiers. Fig. 4.3 shows the architecture of the proposed SMOA. The 1^{st} stage of the SMOA consists of an integrator, identical to that of the class-A OTA in Fig. 4.1. But, the output stage of the SMOA consists of a pulse-width modulator. The output stage of the SMOA, namely the pulse-width modulator, transforms signal information at its input, from the voltage domain, and encodes it in pulse widths at its output. Pulse-width modulation works by comparing the input signal to a reference ramp signal, called the PWM reference that is periodic at F_{PWM} the PWM reference frequency, and outputting either a 1 or a

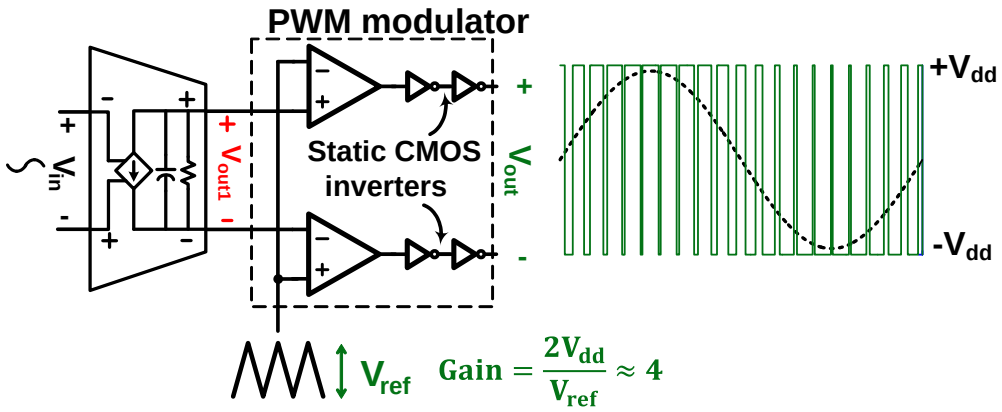

Figure 4.3: Proposed switched-mode operational amplifier.

0. The outputs of the SMOA are switched binary (V_{dd} or 0) signals that are buffered by static CMOS inverters to drive the amplifier load. The following sections describe the advantages of the proposed SMOAs.

4.3.1 Advantages of SMOAs

Rail-to-rail Signal Swing

Since SMOAs encode signal information in pulse widths at their output, the maximum signal swing of SMOAs is limited only by the minimum pulse width that the circuits can represent. The peak output swing of the SMOA can be easily shown to be $V_{dd}(1-2t_{min}F_{PWM})$, where t_{min} is the minimum pulse width that the SMOA can represent and F_{PWM} is the PWM reference frequency. In 65nm CMOS, at a V_{dd} of 0.6V, with t_{min} of 150ps and F_{PWM} of 300MHz, the peak signal swing can be as high as 90% of V_{dd}, a 3$\times$ improvement in signal swing when compared to the classical OTA of Fig. 4.1.

The peak signal swing of SMOA depends only on the minimum representable pulse width t_{min}.

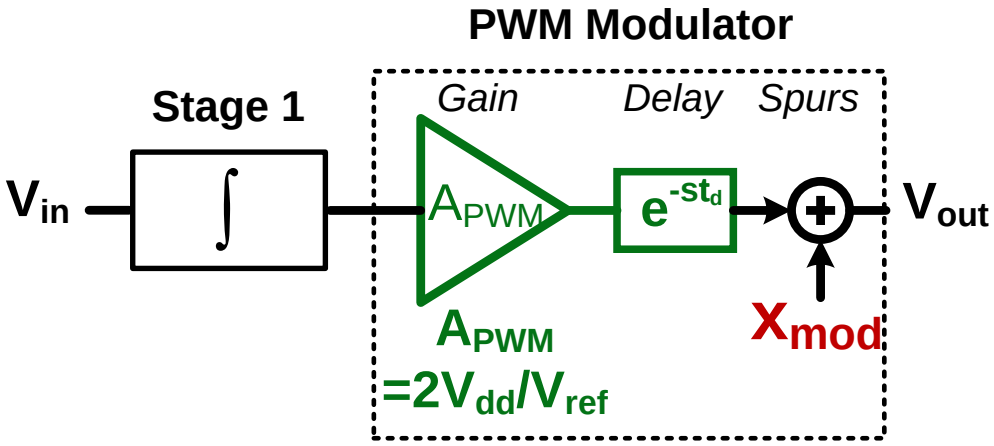

Figure 4.4: Small-signal model of SMOA.

Since, with technology scaling, transistors become faster and faster. Thus, t_{min}, and the peak signal of SMOAs as a consequence, also improve with technology scaling.

Output Stage Gain

The output stage of the SMOA, which is a pulse-width modulator, can be configured to provide a signal path gain > 1. Due to this signal path gain, when the SMOA output V_{out} swings rail-to-rail, the signal swing at the input of the PWM modulator V_{out1}, which is also the output of the 1^{st} stage integrator, is attenuated by this gain. The gain of the PWM modulator is set by the ratio of its supply voltage V_{dd} to the amplitude of its reference ramp signal V_{ref}. For a PWM gain of 4, as V_{out} swings rail-to-rail $\pm$0.6V, the signal swing at V_{out1} is only $\pm$0.15V. Thus, due to the absence of voltage headroom issues at V_{out1}, conventional design techniques can be used for the design of the 1^{st} stage integrator.

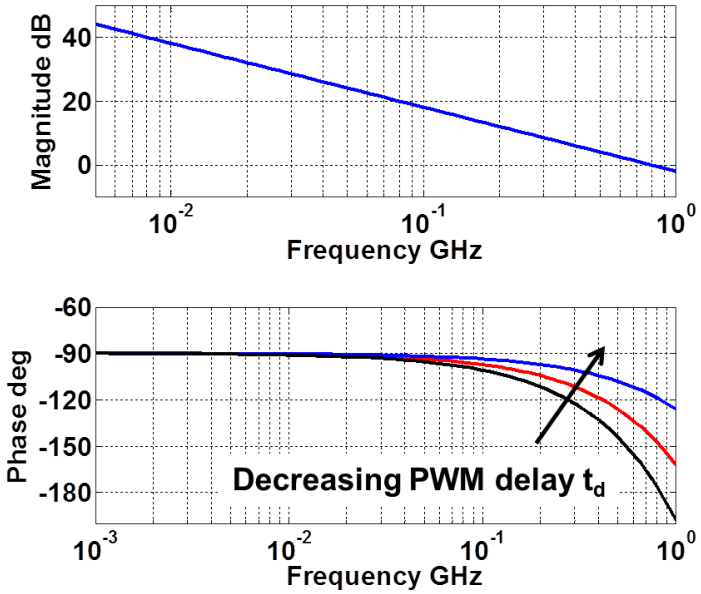

Figure 4.5: SMOA magnitude (top) and phase (bottom) responses.

4.3.2 SMOA Model

Fig. 4.4 shows the small-signal model of the SMOA. The SMOA can be modeled as an ideal integrator, which represents the 1^{st} stage integrator, followed by the PWM modulator. The PWM modulator can by itself be modeled by a gain block A_{PWM} which represents the PWM modulator's gain, in cascade with a delay block t_d, the delay of the PWM modulator. The term x_{mod} represents the PWM modulation spurs and will be explained in the next section.

The AC magnitude response of the SMOA (Fig. 4.5) shows that the integrator gain is augmented by the gain of the PWM output stage, which is flat with frequency. The phase of the SMOA starts at -90°, due to the integrator action and then begins to linearly roll-off with frequency due to the delay of the PWM modulator. Thus, in order to maximize the SMOA stable bandwidth when used in a closed-loop configuration, the delay of the PWM modulator, which provides a phase

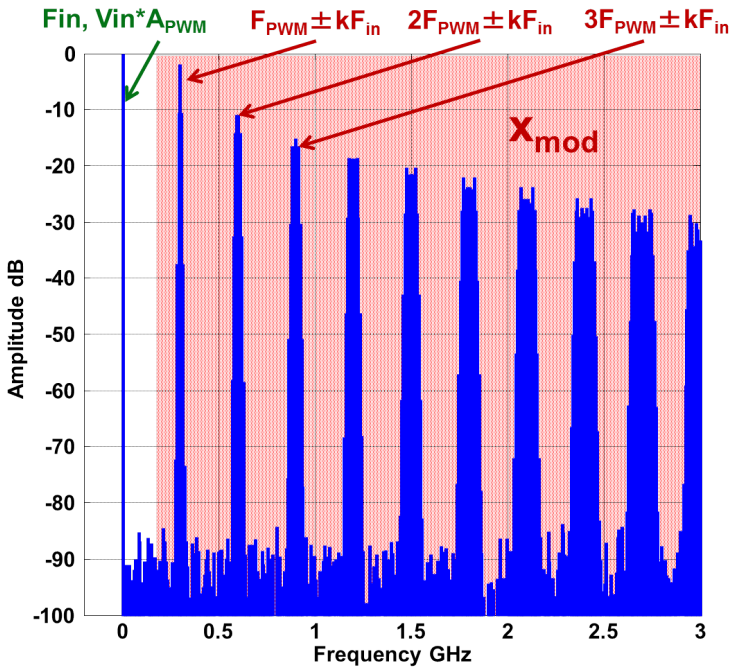

Figure 4.6: PWM modulator output spectrum for F_{PWM} = 300MHz.

shift similar to that of the non-dominant pole in classical-OTAs, must be minimized. But, since the delay of the PWM modulator scales with technology, the stable bandwidth of the SMOA also improves with technology.

4.3.3 SMOA Output Spectrum and Multi-phase PWM Modulation

The output of the SMOA, which is a pulse-width modulated stream, is periodic at the PWM reference frequency F_{PWM} and contains modulation spurs at integrals multiples of F_{PWM}. Fig. 4.6 shows the output spectrum of the PWM modulator for an F_{PWM} of 300MHz. The in-band signal spectrum is clean, consisting of the signal tone with no distortion, while the out-of-band spectrum shows the presence of the modulation spurs at integral multiples of F_{PWM} [59]. In order to obtain

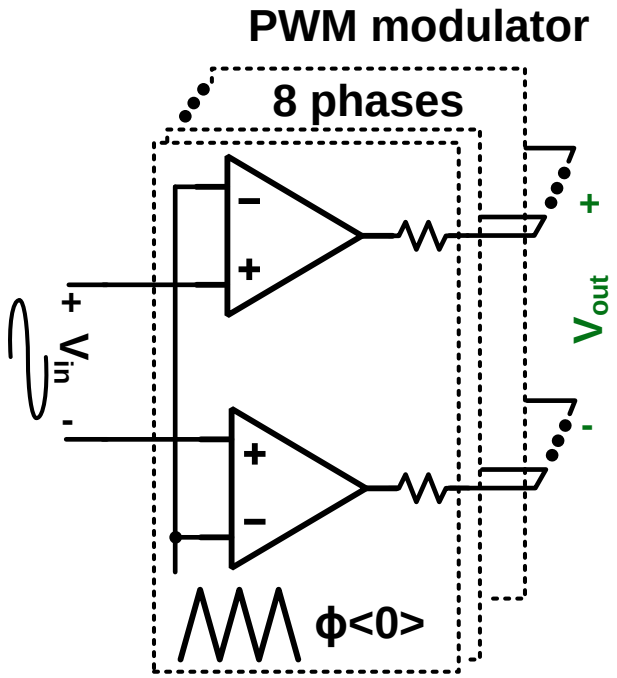

Figure 4.7: 8-phase PWM modulator with F_{PWM} = 300MHz.

a broadband linear spectrum, these modulation spurs need to be pushed far away from the desired signal band.

One common way to push the modulation spurs far away from the signal band is through the use of multi-phase PWM. In multi-phase PWM, a number of PWM modulators, each running at F_{PWM}, say 8 for example, are operated with their PWM reference ramp signals staggered in phase by $2\pi/8$ or 45° and their outputs are combined to obtain the final signal, as shown in Fig. 4.7. Ideally, provided the gain and phases across the various PWM modulators are matched, the 1^{st} modulation spur is pushed to $8F_{PWM}$. It should be noted that since the low frequency input signal combines in phase at the output of the PWM modulators, the various modulators can be scaled down in power.

Fig. 4.8 shows the output spectrum of an 8-phase PWM modulator with an F_{PWM} = 300MHz.

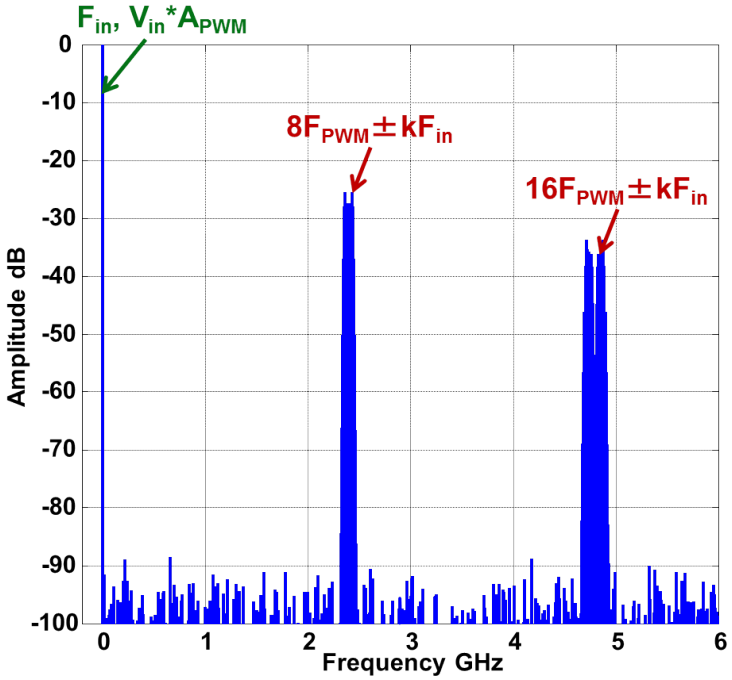

Figure 4.8: 8-phase PWM modulator output spectrum for F_{PWM} = 300MHz.

It can be seen that the first significant modulation spur is pushed to 2.4GHz. To push modulation spurs to 2.4GHz, a single-phase PWM modulator could also be used with an F_{PWM} = 2.4GHz, instead of an 8-phase modulator. But, a high F_{PWM} reduces the maximum signal swing at the output of the SMOA, which reduces to just 28% of the supply for F_{PWM} = 2.4GHz and t_{min} = 150ps. Hence, an 8-phase SMOA architecture is chosen for the presented SMOA implementation.

4.4 Programmable-Gain Amplifier using SMOAs

To illustrate the various advantages of SMOAs, a programmable-gain amplifier (PGA) is implemented using the proposed SMOAs. Fig. 4.9 shows the architecture of the PGA implemented using the proposed SMOA. The R-R PGA has a programmable gain of 0dB, 6dB, 9dB and 12dB which

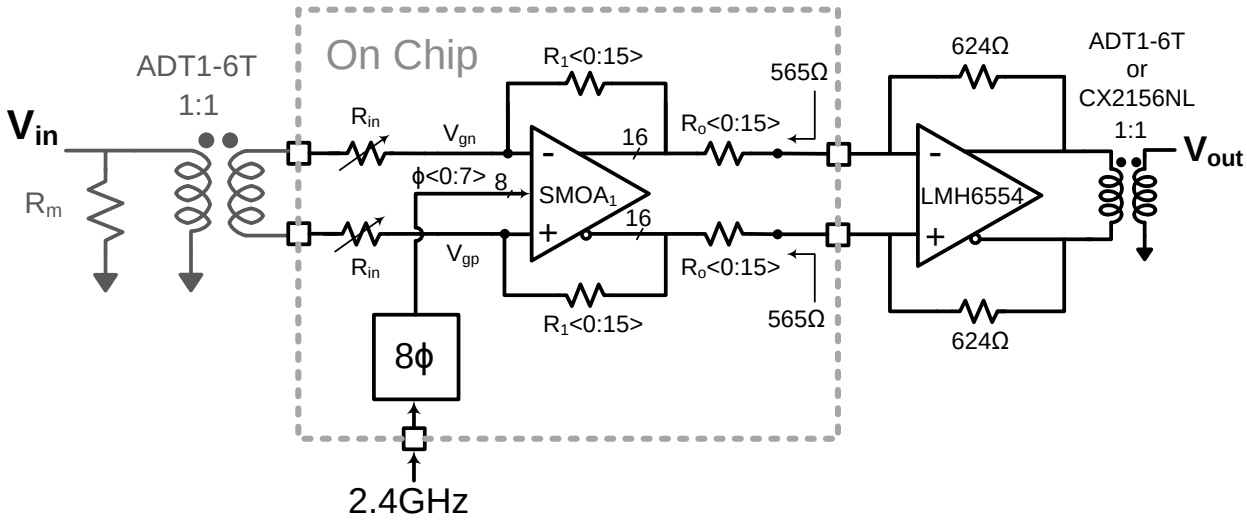

Figure 4.9: PGA implemented using proposed SMOA.

is controlled by changing the input resistor R_{in}. SMOA$_1$ is implemented as an 8-phase SMOA with each SMOA phase operating at 300MHz. The outputs of the SMOA are switched binary signals. Finite impulse response filtering on the SMOA outputs [60], i.e. delaying and adding signals, can be very efficiently performed using digital delay cells due to the switched nature of SMOA outputs. 2-tap FIR filtering produces a frequency notch at 2.4GHz, thus pushing the first significant modulation spur to 4.8GHz. The 8-phase SMOA along with the 2-tap FIR filtering produces the 16 signal streams shown in Fig. 4.9.

4.4.1 8-phase SMOA Architecture

Fig. 4.10 shows the architecture of the 8-phase SMOA, along with the scaled passives. Each SMOA phase consists of the SMOA unit cell and resistors. Since the low frequency signal adds in phase across the 8 SMOA phases, each of the 8 SMOA unit cells and passives are scaled in power and impedance respectively. The SMOA unit cells further include the 2-tap FIR filtering. The 8

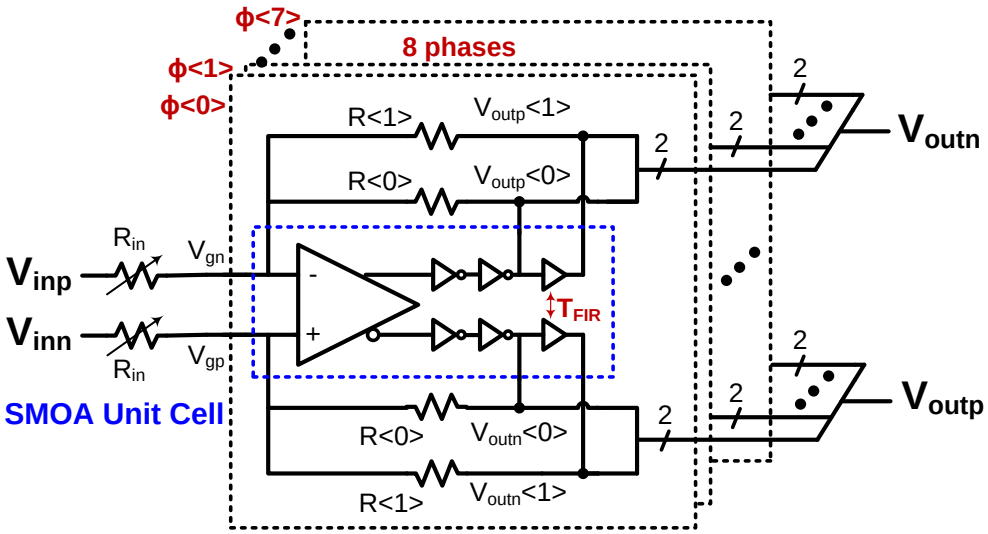

Figure 4.10: 8-phase SMOA architecture.

clock phases are generated on-chip by dividing an externally-fed 2.4GHz clock. With an F_{pwm} of 300MHz, the first modulation spurs appear at 2.4GHz, and with continuous-time FIR filtering, the spurs are pushed further to 4.8GHz. When the 16 binary signal streams at the SMOA output are summed, they form a 17-level signal at the SMOA input V_{gp} and V_{gn}. This is very beneficial for SMOAs in feedback, as it avoids large voltage jumps at the input of the SMOAs, thus preserving their linear behavior.

4.4.2 SMOA Unit Cell Circuit Design

Fig. 4.11 shows the circuit implementation of a single unit of the 8-phase SMOA. The SMOA 1^{st} stage consists of an integrator while the 2^{nd} stage is a pulse-width modulator whose outputs are switched (either V_{dd} or 0) waveforms. The 8 1^{st} stage integrators are scaled appropriately to meet the noise requirements. The following sections describe the circuit design of the SMOA in more detail.

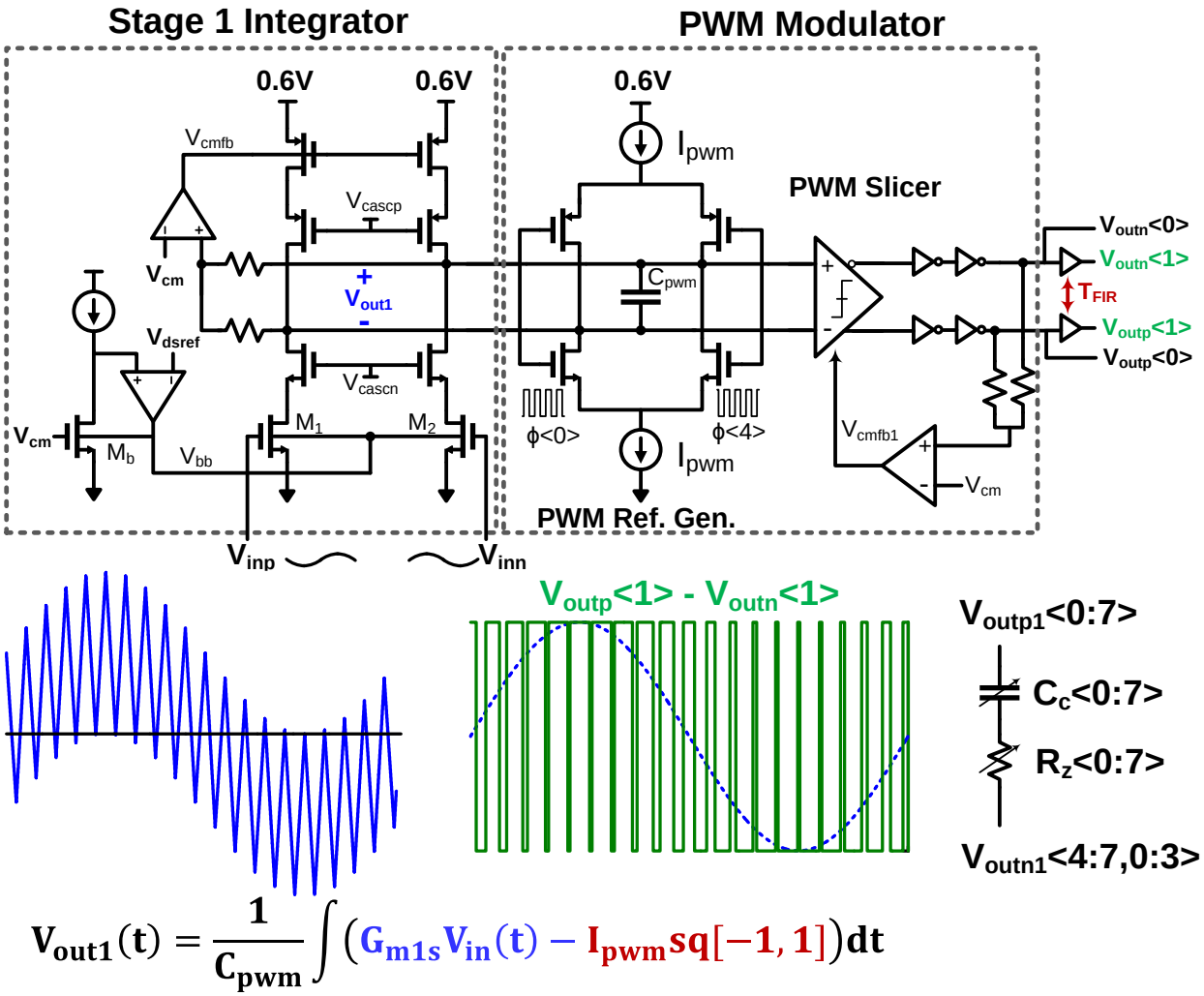

Figure 4.11: (a) SMOA unit cell shown along with the UGB limiting network.

1^{st} Stage Integrator

To enable ultra low voltage operation down to 0.6V, the 1^{st} stage integrator shown in Fig. 4.11 is implemented as a pseudo-differential telescopic cascode amplifier without a tail current source. The bias current in the trans-conductor is set by controlling the body bias of transistor M_1 and M_2 [61]. The gate of transistor M_b is biased at $V_{dd}/2$ (which is approximately the bias at the gates of M_1 and M_2 in Fig. 4.11 when the SMOA is used in a closed-loop configuration). An amplifier A adjusts the body voltage V_{bb} of M_b to force its drain-source voltage to equal an externally supplied reference V_{dsref}. Body-mirroring is feasible when the threshold voltage of the transistors is close to $V_{dd}/2$. A dedicated common-mode circuit is used to provide common-mode rejection at the integrator output. The trans-conductor has a DC gain of close to 40dB in simulation.

Pulse-Width Modulator Design

Converting an analog (voltage/current) signal into a pulse-width modulated stream entails two operations: the first is the generation of a PWM reference ramp signal, against which the input analog signal is compared; the second is the comparison that outputs a pulse-width modulated signal. In the current SMOA implementation, the PWM reference ramp is generated by charging and discharging a capacitor C_{pwm}, with a current I_{pwm}, connected to the output of the 1^{st} stage integrator using a current-steering differential pair as shown in Fig. 4.11. The output signal current of the integrator is also steered onto the same capacitor. The current-steering pair is controlled by one of the 8 clock phases of the SMOA. This arrangement accomplishes two functions with

consummate ease: the generation of the PWM reference ramp signal and the subtraction of the analog signal and the PWM reference signal.

To support rail-to-rail signal swings at the SMOA output, the PWM modulator should provide some gain ($K > 1$) to the signal component. As explained in Section 4.3.2, the signal path gain of the PWM modulator is set by the ratio of the peak-to-peak voltage of the PWM reference ramp signal to the supply voltage V_{dd}. The peak-to-peak amplitude of the PWM reference ramp is controlled by changing the current I_{pwm}. Although a capacitor C_{pwm} is shown explicitly in Fig. 4.11, in practice, the PWM reference ramp is generated by charging and discharging the parasitic capacitors present at the output of the integrator. The PWM reference amplitude is set to provide a gain of ≈ 4 for the PWM modulator, at a supply of 0.6V.

The PWM modulator, as explained in Section 4.3.2, can be modeled in the small-signal sense as a gain block in cascade with a delay t_d which is the delay of the PWM modulator. The delay t_d provides an additional phase shift in the signal path, thus forming a non-dominant pole in the SMOA, with the dominant pole formed at the output of the 1^{st} stage integrator. In order to guarantee SMOA stability with sufficient phase and gain margins when used in a closed-loop configuration, the phase shift due to the delay must be minimized, which requires minimization of t_d. In SMOAs, pulse-width modulation is performed by the use of a continuous-time comparator connected to the output of the integrator (PWM continuous-time slicer in Fig. 4.11). SMOAs use natural PWM, where the input signal is compared in continuous-time with the PWM reference ramp signal.

The continuous-time slicer (Fig. 4.12) consists of a cascade of 3 differential pairs followed

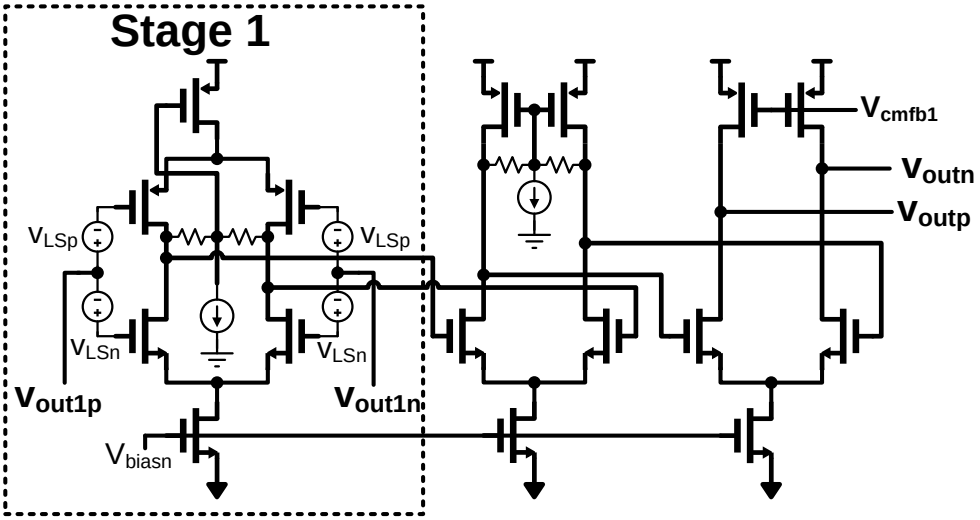

Figure 4.12: Continuous-time PWM slicer.

by static inverters to drive the output load. The delay of the continuous-time slicer, and hence the PWM modulator, is set primarily by the gain-bandwidth of its 1^{st} stage, which needs to be made large by design to minimize t_d. Also, since each SMOA requires a PWM modulator for each of its 8 phases, achieving this large gain-bandwidth in a power-efficient manner is critical to minimizing the SMOA power consumption. The 1^{st} stage of the PWM slicer is implemented as a CMOS (NMOS and PMOS) differential pair, interfaced to the output of 1^{st} stage integrator through a DC level-shifting network. A dedicated common-mode feedback network sets the SMOA output common-mode to $\approx V_{dd}/2$.

Unity-Gain Bandwidth (UGB) Limiting Capacitors

Since the PWM modulator gain is flat with frequency and its delay provides an increasing phase shift with frequency, the addition of a UGB limiting network at the output of the 1^{st} stage integrator is necessary to stabilize the SMOA in feedback. This network should limit the bandwidth of the

1^{st} stage integrator and also provide a zero to compensate the phase shift due to the delay of the PWM modulator.

The bandwidth of 1^{st} stage integrator is limited by adding a series RC network to its output to form the dominant pole and a stabilizing zero, as shown in Fig. 4.11. The simplest way of connecting this RC network to the output of the 8 integrators would be between $V_{outp1} < 0 >$ and $V_{outn1} < 0 >$, $V_{outp1} < 1 >$ and $V_{outn1} < 1 >$ etc. But such an arrangement would capacitively load the PWM current source in Fig. 4.11. Thus in order to achieve a particular PWM ramp amplitude, due to the increased capacitive loading at the output of the integrator, the PWM reference current I_{pwm} would need to increase. This in turn increases the noise contribution of the PWM current source and also increases its power consumption. In order for the UGB-limiting series RC network to be transparent to the PWM current source, the network is connected to appear in common-mode for the PWM current source but in differential mode for the input signal, as shown in Fig. 4.11. The PWM clock phases $\phi < 0,3 >, \phi < 1,4 >$ etc. are 180° out-of-phase. By connecting the UGB limiting RC network between the nodes $V_{outp1} < 0 >$ and $V_{outn1} < 3 >$, $V_{outp1} < 1 >$ and $V_{outn1} < 4 >$ etc., it forms a dominant pole at the output of G_{m1s} without loading the PWM current source. This enables the use of a smaller, and hence lower noise, I_{pwm} for a given peak-to-peak PWM reference amplitude. The location of the pole and zero are nominally made tunable around 10MHz and 100MHz respectively.

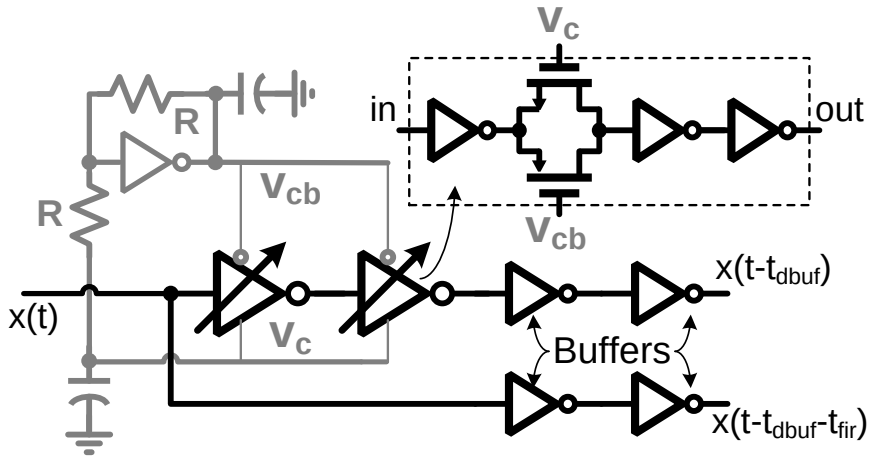

Figure 4.13: Implementation of the FIR delay cell.

Continuous-time FIR Delay Cells

Due to the 8-phase implementation of the proposed SMOAs and a PWM reference frequency F_{PWM} of 300MHz, the dominant modulation spur ideally appears at 2.4GHz. The switched nature of PWM signals enables the use of simple inverter-based delay cells for FIR filtering. Continuous-time FIR filtering with delay cells is further employed to provide a notch at 2.4GHz, thus pushing the dominant spurs to 4.8GHz. To obtain a notch at 2.4GHz, an FIR delay of $t_{FIR} = 1/(4.8\text{GHz}) = 208.33\text{ps}$ is required, which is easily achieved using on-chip delay cells. A 4-phase SMOA implementation, with the same F_{PWM} of 300MHz, and a 4-tap FIR filter could also be used the realize the same dominant spur frequency (4.8GHz) using 3 delay cells ($t_{FIR} = 1/(4.8\text{GHz})$). This would add additional phase shift to the signal path ($t_d = t_{dPWM} + 0.5t_{FIR}$ in Fig. 4.4) and limit the maximum achievable UGB of the SMOA. Additionally, taking the narrow-band nature of FIR notches in to account, an 8-phase SMOA implementation with a 2-tap FIR notch at 2.4GHz was preferred over a 4-phase, 4-tap FIR architecture.

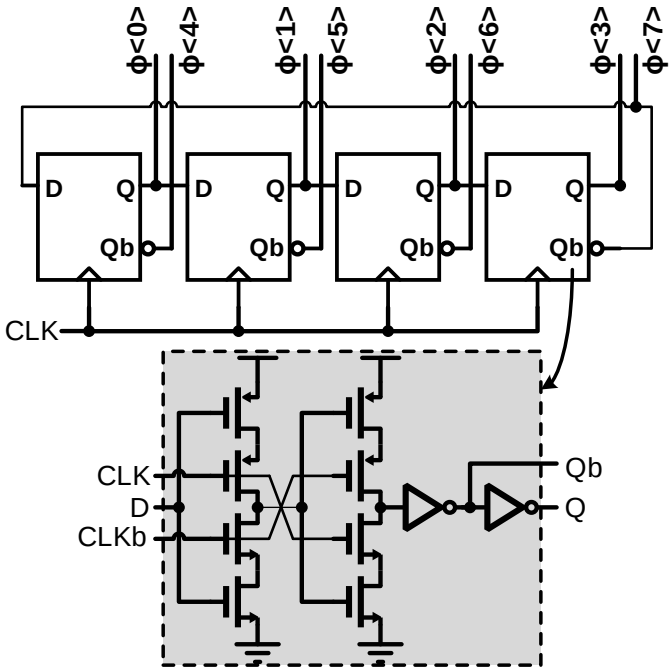

Figure 4.14: Multiphase clock generator.

To obtain a notch at 2.4GHz, a delay of 208ps is required. To maximize the output signal swing, the SMOA is desired to process pulse-widths as small as 150ps. Since it is not possible to delay a 150ps wide pulse by 208ps using a single stage delay cell, a cascaded two-stage approach is implemented. Fig. 4.13 shows the implementation of the FIR delay cell for a single differential-half of the SMOA output (for a single phase). The FIR delay is controlled by the tuning voltage v_c, which is set by an on-chip current-steering DAC (digital-to-analog converter).

Multi-phase Clock Generator

The different clock phases for the 8-phase SMOAs are obtained by division from an externally-fed 2.4GHz clock. Fig. 4.14 shows the implementation of the 8-phase clock generator. The different

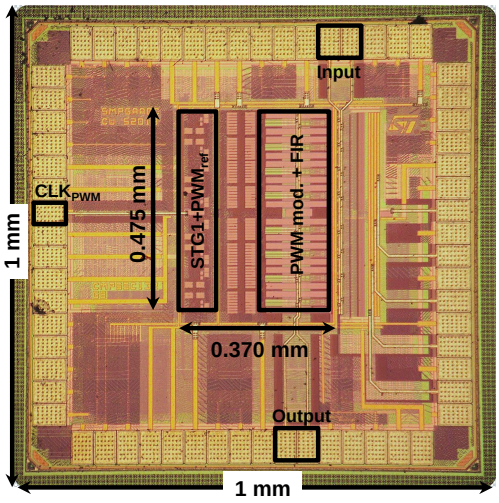

Figure 4.15: PGA die photo.

clock phases are obtained by using a Johnson counter built with transmission-gate based D-flip-flops. Each of the 8 phases are made tunable using delay cells (Fig. 4.13) to enable calibration for PWM phase mismatches.

4.5 Measurement Results

The PGA was fabricated in a 65nm CMOS technology. The die, shown in Fig. 4.15 measures 0.18mm^2 and operates from a 0.6V supply. The die was bonded in a 48-pin QFN package and soldered on a PCB and tested. The measurement setup is shown in Fig. 4.9. The input signal interfaces to the PGA through a transformer. An external 2.4GHz clock source is divided to generate the required clock phases. The output of the PGA drives an off-chip trans-impedance amplifier (LMH6554) *without* any signal attenuation, which then drives a transformer and is fed to the spectrum analyzer for spectral measurements.

To evaluate the large signal swing capabilities of SMOAs, the dynamic performance of the

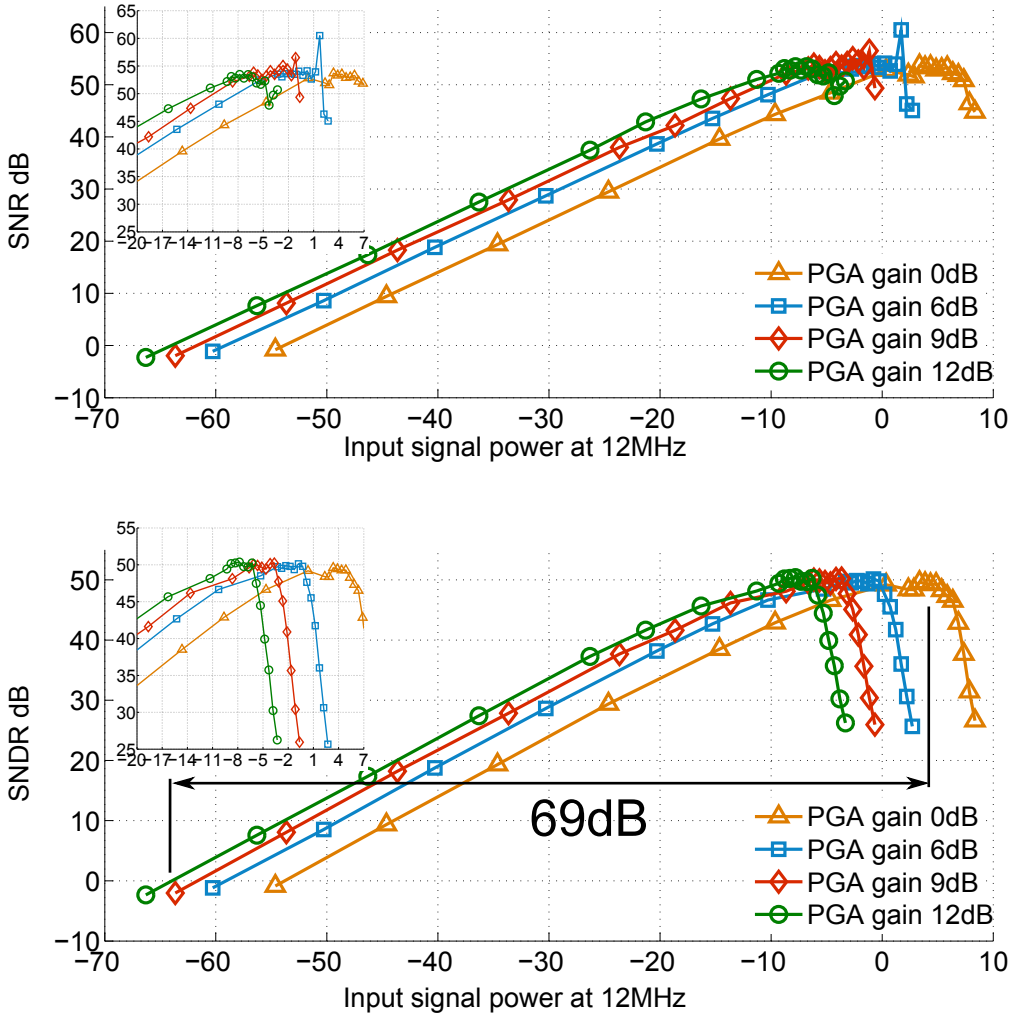

Figure 4.16: PGA dynamic performance vs. input signal amplitude at 12MHz.

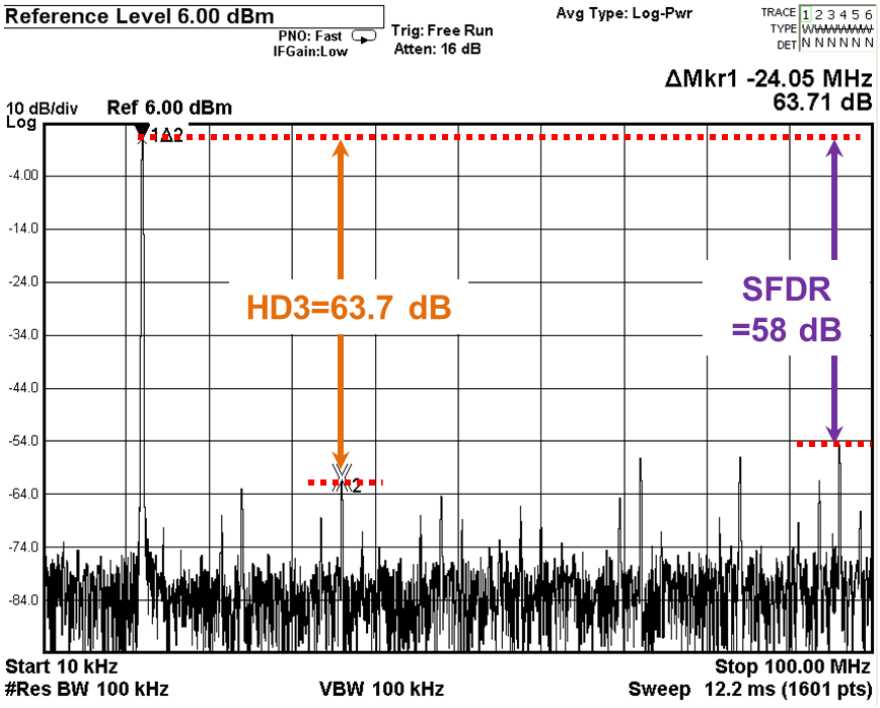

Figure 4.17: PGA in-band (0 - 100MHz) output spectrum for 0dB gain setting.

PGA, namely its SNR and SNDR were plotted as a function of the input signal amplitude at 12MHz (Fig. 4.16) for different PGA gain settings. The PGA has a peak SNR of 55dB and a peak SNDR of 50dB at an input full-scale of +4dBm, and a dynamic range of 69dB. The input full-scale swing is 80% of the supply at 0.6V, owing to the high signal swing capabilities of SMOAs.

Fig. 4.17 shows the in-band (0 - 100MHz) output spectrum of the PGA for a 25MHz full-scale input. The PGA has a peak SFDR of 58dB. Ideally, using an 8-phase SMOA with each phase running at 300Mhz pushes the modulation spurs to 2.4GHz, which due to further 2-tap FIR filtering are further pushed to 4.8GHz.

Fig. 4.18 shows the full (0 - 2GHz) output spectrum. Due to mismatches in the various SMOA phases, residual modulation spurs are observed at integral multiples of F_{PWM} = 300MHz.

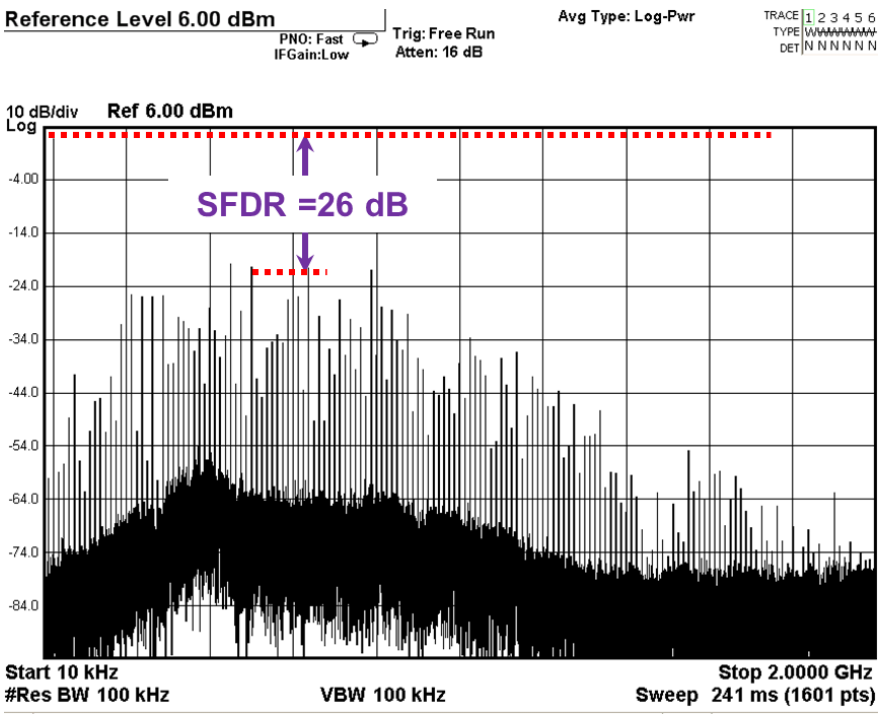

Figure 4.18: PGA full (0 - 2GHz) output spectrum for 0dB gain setting.

Table 4.1 summarizes the performance of the PGA. The PGA consumes 6.6mW from a 0.6V supply, while achieving a dynamic range of 69dB.

Table 4.1: PGA Performance Summary

Supply Voltage	0.6V
Technology	65nm CMOS
Area	$0.18mm^2$
Input Full-Scale (FS)	$1V_{ppd}$ (+4dBm)
Gain	0-12dB
Dynamic Range	69dB
Power	6.6mW

Chapter 5

Conclusions and Future Work

Chapter 2 of this thesis introduced current pre-charging techniques to generate the reference in MDACs of pipeline ADCs. Accurate reference-voltage buffers are power hungry and their design is particularly challenging in zero-crossing based circuits due to the stringent settling requirements. A Current Reference Pre-charge (CRP) technique with Constant Reference Loading (CRL) was proposed, that replaced traditional power hungry voltage reference buffers with power efficient current sources, leading to power and area savings. A Dynamic Reference Loading (DRL) technique was proposed that further reduced the effective reference capacitor loading. This leads to more relaxed noise requirements on the ZCD, when compared to CRL, and also reduces the net noise contribution of the reference path. The presented proof-of-concept ADCs had an excellent FOM, when compared to state-of-the-art ADCs, especially since competing works do not include the power consumed by the reference buffer.

Chapter 3 of the thesis described the design of a radiation-hard dual-channel 12-bit 40 MS/s

Pipeline ADC with extended dynamic range, for use in the readout electronics upgrade for the ATLAS Liquid Argon Calorimeters at the CERN LHC. The ADC was confirmed to be radiation tolerant beyond the required specifications. Various gain selection experiments were performed with the prototype to investigate possible gain selection procedures for future implementations of this design and a fully digital gain selection was found to be a promising approach for future implementations. It was found that an analog memory depth of four was required to perform gain selection and hence a fully digital approach is chosen to implement gain selection in the final version of the prototype.

The steady reduction in the supply voltage with CMOS technology scaling has severely limited the performance of voltage-based conventional analog design techniques. Chapter 4 of this thesis proposed Switched-Mode Signal Processing, a new design paradigm that achieves rail-to-rail signal swings with high linearity at ultra-low supply voltages. Switched-Mode Signal Processing represents analog information in terms of pulse widths and replaces the output stage of OTAs with power-efficient rail-to-rail Class-D stages, thus producing Switched-Mode Operational Amplifiers (SMOAs). The presented programmable-gain amplifier implemented using the proposed SMOA showed excellent linearity performance at low supply voltages, leveraging the increased timing accuracy available in scaled CMOS technologies.

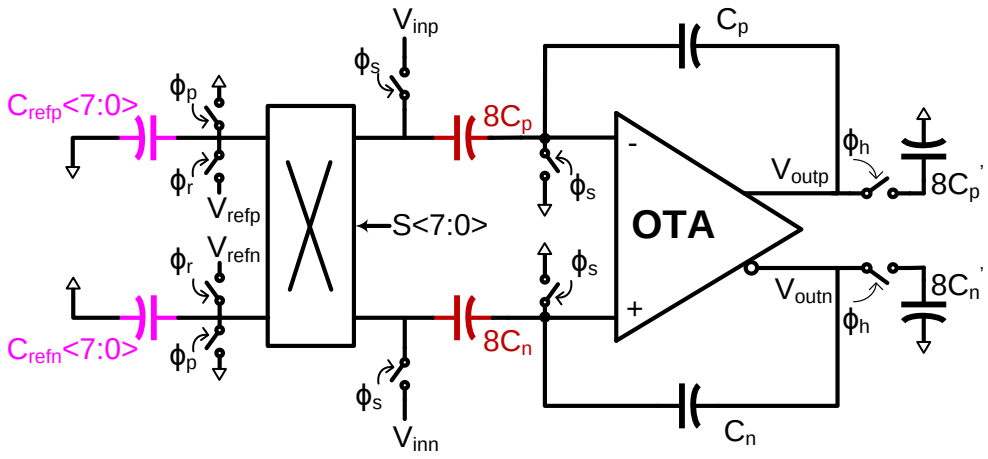

Figure 5.1: Series reference pre-charged MDAC.

5.1 Future Work

5.1.1 Series Reference Pre-charged MDAC

The constant reference loading pre-charge technique, proposed in Chapter 2, decreased the effective feedback factor of the MDAC during the amplification phase, thus increasing the noise contribution of the ZCD. Dynamic reference loading reduced this feedback factor reduction but does not completely eliminate it. But, by using a series reference pre-charged architecture, this feedback factor reduction can be completely eliminated, while still keeping the reference charge drawn signal independent.

Fig. 5.1 shows the series reference pre-charged OTA-based MDAC, while the residue characteristic and the timing diagram are shown in Fig. 5.2.

Fig. 5.3 shows the MDAC redrawn during the sample phase ϕ_s. The input signal is sampled across the capacitors $8C_p$ and $8C_n$. At the start of ϕ_s, the 8 separate reference capacitors $C_{ref} < 7:0 >$ are discharged during a reset phase ϕ_p. This reset phase clears any signal depen-

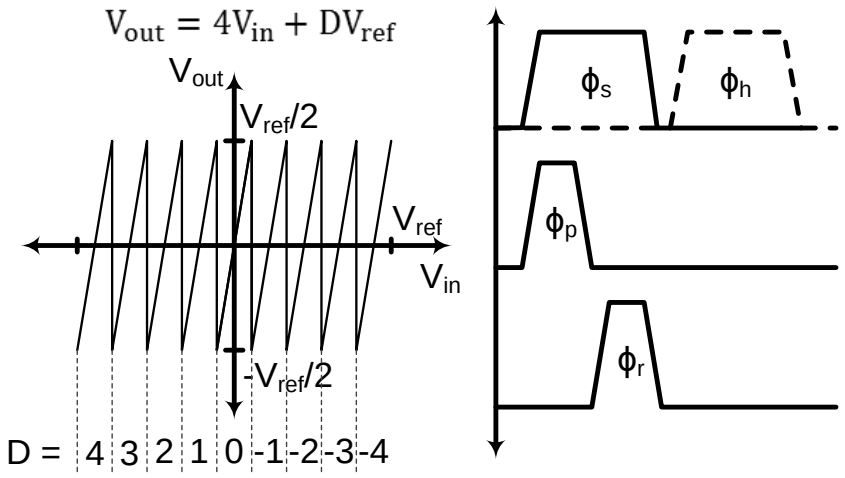

Figure 5.2: Residue and timing diagram.

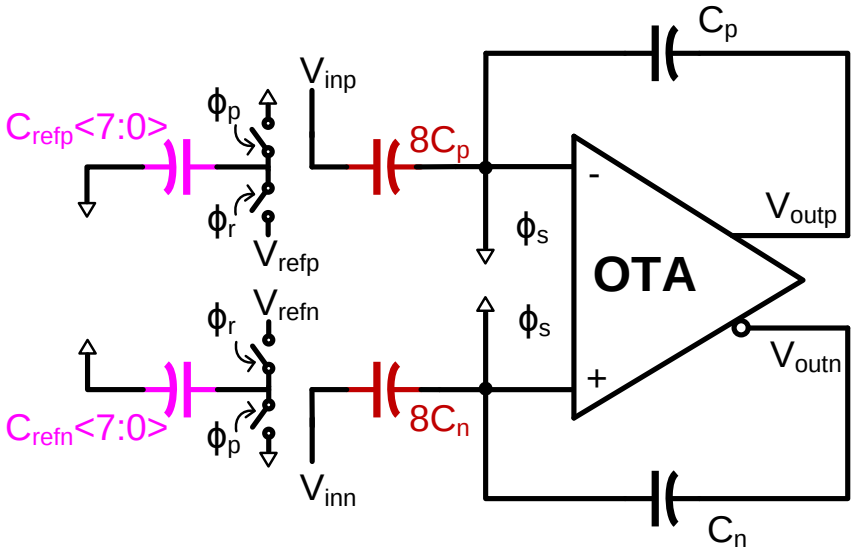

Figure 5.3: Series reference pre-charged MDAC during the sample phase.

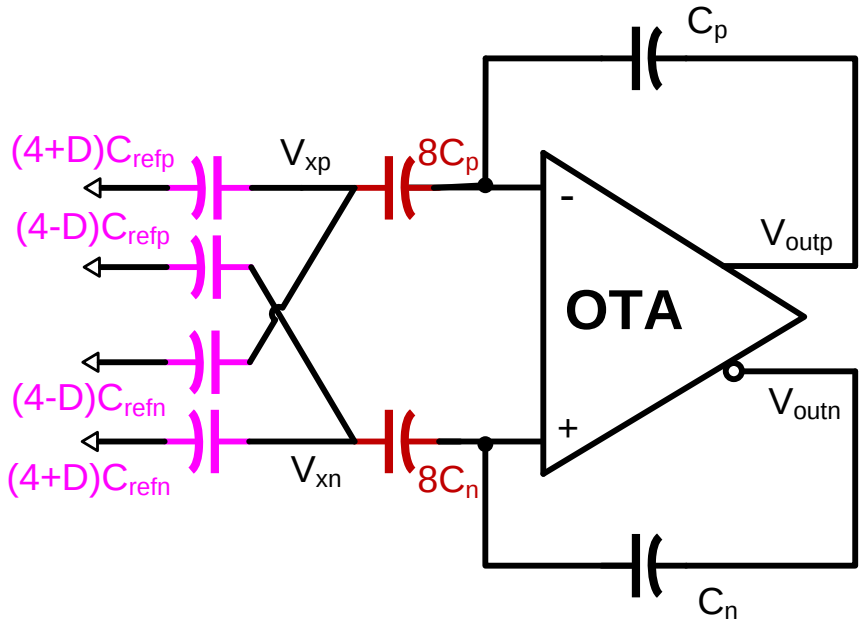

Figure 5.4: Series reference pre-charged MDAC during the hold phase.

dent charge from the reference capacitors. The reference capacitors are then pre-charged to the reference voltage during ϕ_r, in parallel with input signal sampling.

Fig. 5.4 shows the MDAC redrawn during the hold phase ϕ_h. Based on the subADC decisions D, the reference capacitors are connected in series with the signal capacitors to complete the charge transfer and implement the MDAC transfer characteristic. This series arrangement does not lead to any reduction in the MDAC feedback factor. This MDAC architecture can also be applied to ZCB MDACs to improve the noise performance of the ZCD.

Potential challenges for the implementation of the series reference pre-charged MDAC are the reference capacitor discharge during the short reset phase ϕ_p and non-linearity due to switch parasitic on nodes V_{xp} and V_{xn}.

5.1.2 Improving the Performance of SMOAs

In the presented SMOAs in Chapter 4, modulation spurs are present at the SMOA output due to mismatch between the various SMOA phases. To obtain a broadband linear spectrum, calibration routines have to be implemented to remove all mismatches between the SMOA phases, thus pushing the modulation spurs far away from the signal band.

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