Noise Optimization for High-Bandwidth Ion Channel Recordings

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Submitted in partial fulfillment of the

requirements for the degree

of Doctor of Philosophy

in the Graduate School of Arts and Sciences

COLUMBIA UNIVERSITY

2013

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Abstract

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Single-molecule measurements often exhibit weak signals and fast kinetics, making them particularly challenging to record with high fidelity. This thesis presents an analysis of voltage-clamp current recordings of single ion channels, and concludes that considerable improvements in signal-to-noise ratios can be achieved by minimizing all parasitic capacitances associated with these measurements. A custom integrated amplifier in a $0.13\mu m$ complementary metal oxide semiconductor (CMOS) process is designed for high-bandwidth ion channel recordings, and systems are designed to closely incorporate this amplifier with solid-state nanopore sensors, lipid membranes, and biological ion channels. The low capacitance of these integrated platforms reduces noise at high frequencies, enabling signals to be measured up to ten times faster than had been previously achieved. In addition to improving signal quality, the small physical size of these integrated systems portends the arrival of massively parallel high-performance ion channel recording systems for drug discovery and biomolecular sensing applications.

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Acknowledgments

None of this work would be possible without the help and support of all of my colleagues, friends, and family. I am particularly in debt to my advisor, Kenneth Shepard, whose energy, ideas, and enthusiasm inspired me to come to Columbia and motivated me throughout my time in graduate school.

During my first year at Columbia, Peter Levine and Ping Gong were immensely helpful in introducing me to many of the electrochemical systems that I would eventually use, and as I progressed through graduate school I have always remembered and appreciated their extraordinary patience.

I have benefited greatly from discussions and assistance from all of the members of the Shepard group, including Siddharth Ramakrishnan, Cory Dean, Sebastian Sorgenfrei, Matt Johnston, Inanc Meric, Simeon Realov, Ryan Field, Haig Norian, Jared Roseman, Noah Sturcken, Paul Pan, Michael Lekas, Dan Bellin, Steve Warren, Hasti Amiri, Jaebin Choi, Anthony Erlinger, Aditya Girish, Dan Fleischer, and Ria Miranda. The number of people across the Columbia campus who helped me over the past few years is truly too many to name, but I am indebted to every one.

Professor Marija Drndic at the University of Pennsylvania was instrumental in this work, for shaping the early stages of this project, for frequently welcoming me into her lab, and for making all of our solid-state nanopore results possible. Many people at Penn had important contributions to this thesis. I have learned a great deal from Meni Wanunu and Ken Healy, as well as Kimberly Venta, Vishva Ray, and Chris Merchant. Every time that I got off the train in Philadelphia with a suitcase full of electronics, I was received more

graciously than I had any right to expect.

I am very grateful to Anubhav Tripathi, Harvey Silverman, and William Patterson at Brown University, whose teaching, generosity and advice have been invaluable.

Before graduate school I was lucky to work with many talented indivuduals at Analog Devices and MediaTek Wireless. I offer a special thanks to Hasnain Akram for introducing me to Columbia Engineering's distance learning program, where, for a time, we were both students.

I thank John Kymissis, Jing Ju, and Charles Zukowski for their time and contributions as members of my thesis committee.

Many thanks to all of my friends from Westfield, Providence, Somerville, and New York for keeping me appropriately distracted. And especially to Karla, for knowing about every free event in New York City and filling my time outside the lab with art, music, food, and companionship. Finally, thanks are not nearly enough for my parents, sister, and grandparents, but I thank them for absolutely everything.

Chapter 1

Introduction

Many of the boundaries of modern science can be thought of as issues of scale, where our understanding of the world breaks down in the face of new phenomena which are larger, faster, slower, or weaker than were studied before. Sometimes these boundaries may be limits of our collective imagination, but often they are simply the measurement limits of the available scientific instruments and techniques. In biological systems, there are limits to studying both very large and very small systems. At the large end, the complexity and diversity of living things challenges our ability to catalog the meaningful common structures and behaviors among them all. At the small end, we struggle to characterize the multitude of weak stochastic interactions that build on one another to shape the world around us.

Studying molecular-scale features of any system often challenges the limits of what we can reliably measure. Physically smaller systems tend to produce weaker signals. These weak signals eventually run into the inherent error in any finite physical measurement. Taking advantages of improved materials, tools, and techniques, these detection limits regularly improve, allowing more precise measurements of well-known systems, and new detection of ever weaker phenomena.

The modern scientific literature contains many examples of signals successfully isolated and recorded from single biomolecules. Single-molecule measurements are attractive not only for their extremely high sensitivity but also for the insight that they offer into molec-

ular diversity that is masked in ensemble measurements. That biological single-molecule measurements are possible at all is a relatively recent development. Currents through single membrane ion channels were recorded in the 1970s [1], and optical single-molecule imaging came of age in the 1990s [2]. Today, a range of single-molecule imaging techniques are in common use, based on combinations of optical, mechanical, and electronic modes of sensing [2–6].

All of these single-molecule sensing modalities have benefited greatly from the rapid progress of the modern semiconductor industry [7, 8]. The first single-molecule recordings were produced in 1976, the same year as the Cray-1 supercomputer. Vacuum tubes had already ceded to discrete transistors, but integrated circuits were in their infancy, and personal computers were virtually non-existant. Integrated circuit progress paved the road for the extremely low-noise image sensors that enable today's single-molecule fluorescence studies, and high-performance personal computers have greatly improved the usability of all of these ultra-sensitive platforms (Today's universal and flexible digital data acquisition is in stark contrast to the first single-channel traces, which were documented as "pen records replayed from analogue tape" [1]).

Due to the fundamental tradeoff between noise amplitude and temporal resolution, many single-molecule measurements are limited to observing very slowly-changing signals. In particular, optical techniques generally cannot directly resolve single-molecule changes that occur on sub-millisecond timescales, as imaging times must accommodate the relatively slow rate of photon emission from a single fluorophore. In contrast, non-optical techniques that offer direct transduction to ion or electron flux can enable studies of dynamic single-molecule processes on microsecond or nanosecond timescales. Although the signals from natural and synthetic ion channels are considered weak from an electronics standpoint, they can represent a flux of millions or billions of ions per second. However, in practice ion channel recordings have been constrained to observing much slower signals, owing to comparatively high background noise.

This thesis will discuss the fundamental limits of noise and temporal resolution in

ion channel recordings, and present a new measurement platform which achieves lower noise and higher measurement bandwidth by merging nanopore sensors and ion channels with a modern custom integrated circuit, thus reducing critical parasitic electronic elements and improving the signal-to-noise ratio.

1.1 Thesis outline

Chapter 2 provides an introduction to ion channels and nanopore sensors, with a focus on the simplified physical and behavioral models that will be useful in optimizing their electronic measurement. Fundamental aspects of electronic signal-to-noise ratios are also reviewed, as well as the classical voltage-clamp electronic circuit that is often used for weak transient current recordings.

Chapter 3 presents an integrated complementary metal oxide semiconductor (CMOS) amplifier designed for nanopore and ion channel recordings. The amplifier chip contains eight independent voltage-clamp preamplifier channels, and it is implemented in an $0.13 - \mu m$ mixed-signal CMOS process.

Chapter 4 discusses measurements of solid-state nanopore sensors using the new CMOS preamplifier. By integrating the preamplifier within the experimental fluid chamber, parasitic capacitance is considerably lower than alternative arrangements, reducing noise and enabling recordings with very fine temporal resolution. Also presented is a method to fabricate solid-state nanopores which pass directly through the CMOS die itself.

Chapter 5 introduces a monolithic arrangement which assembles lipid membranes in direct contact with the surface of the active CMOS amplifier die. High-quality single-channel gating currents are recorded from ion channels incorporated in these membranes.

Chapter 6 summarizes the original contributions of this work to the fields of micro-electronics, electrophysiology, and biosensors. Possibilities for further improvements and expansions of the work presented here are also considered.

Chapter 2

Background, Review, and Analysis

2.1 Introduction

Among the various classes of single-molecule sensors, ion channels and nanopores represent some of the highest-bandwidth systems available to date, with temporal resolution commonly on the order of tens of microseconds. These systems produce weak ionic currents, and their useful signal bandwidths are generally constrained not by small-signal frequency response but by the signal-to-noise ratio (SNR). The development of patch-clamp recording techniques [9] has been accompanied by detailed treatments of noise in ion-channel recordings [3], but such discussions often specifically address scenarios with signal amplitudes of 10 pA or less, for which relevant bandwidths are typically less than 10 kHz. However, there are many examples of natural and synthetic ion channels which can produce much larger signals than this. Nanopore sensors, in particular, are commonly operated in higher salt concentrations and at higher voltage bias than physiological conditions. Protein nanopores regularly contain current signals as large as $100-300\ pA$ [10,11], while solid-state nanopores can produce signal amplitudes upwards of 4 nA [12].

Understanding the limits of signal detection in ion channel recordings requires a combined understanding of the channels themselves, their electrochemical environments, and the electronic amplifiers used to measure them. This chapter reviews important theoretical and practical aspects of each of these systems with an eye towards optimizing the noise floor

at high frequencies. In addition to objectively improving the signal-to-noise ratio, this will enable single-channel recordings with finer temporal resolution than have previously been achieved.

2.2 Ion channels

Cell membranes are complex systems which perform a wide range of critical functions in living things [13]. In addition to serving as the mechanical boundary of a cell or an organelle, these thin lipid films are the home of many proteins which naturally perform highly specialized sensing and signaling functions.

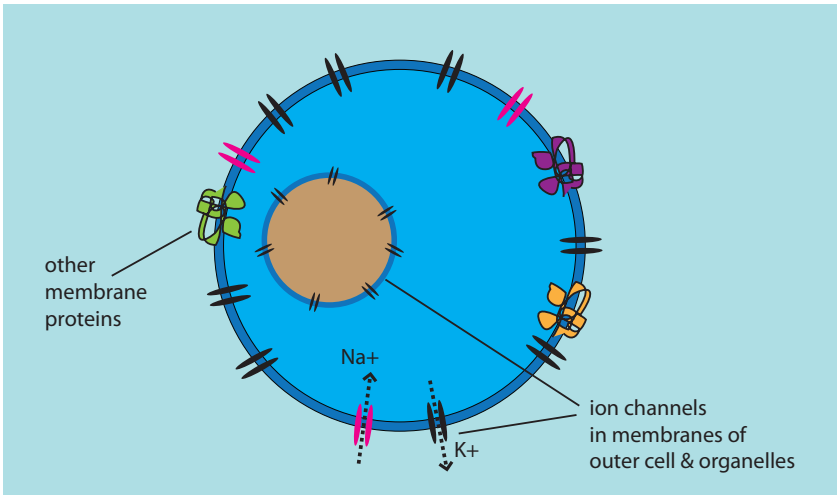

Figure 2.1: Schematic illustration of ion channels in cellular membranes.

These membranes are composed of amphiphilic molecules with a hydrophilic head attached to a lipid tail; hydrophobic forces lead the membrane to preferrentially assemble into two layers (a lipid bilayer), and the inner hydrophobic lipid tails make the membrane largely impermeable to water. This allows a cell to maintain a different chemical environment than its surrounding medium; however, there are many metabolic and signaling functions which require molecules to transport across the membrane. There are many classes of proteins which assist with this transport, of which ion channels are one ubiquitous and well-studied category.

An ion channel is a protein which spans a lipid membrane and allows aqueous dissolved ions (such as potassium, sodium, and chloride, among others) to cross the hydrophobic barrier of the membrane [14]. Ion channels can actively open and close in response to stimuli, and they may be selective, preferrentially allowing only specific types of ions to pass. When a channel is open, the motion of ions through it is driven by external energy gradients, not by the channel itself. The opening and closing of an ion channel is thus often referred to as *gating*, which contrasts it to other types of membrane proteins which may expend energy continuously to transport molecules across the membrane.

The passive nature of transport through an ion channel makes it a very efficient signaling mechanism; because cells can maintain a semi-isolated internal chemical environment, there can be steady-state electric fields and concentration gradients across the thin lipid membrane. As a result, when a single ion channel opens, thousands or millions of ions per second may flow in or out of it. The precise ion current level depends on both the environmental conditions and the properties of the channel protein itself. This fast transport allows cells to quickly change their electrochemical potential, leading to action potentials which drive many intercellular processes in the nervous system.

The study of ion channels and action potentials is the core of the field of electrophysiology. In its infancy, electrophysiology was limited to measuring changes in the extracellular potential of living tissue. This mode of recording is important for many physiological applications, but to study ion channels at a molecular level, researchers often prefer techniques which directly measure the ionic *current* through a patch of a cellular membrane, rather than the voltage across it.

Despite the large number of ions that can flow through individual open channel proteins, these ionic currents are very weak compared to typical electrical currents in solid-state electronic materials. It took many years before appropriate instruments and biophysical techniques were developed to reliably record the activity of single ion channels. The combination of techniques which were eventually successful are referred to as *patch-clamp* recording, for which Erwin Neher and Bert Sakmann were awarded the Nobel Prize in 1991.

The patch-clamp technique combines excellent isolation of a small patch of a cell membrane with low-noise voltage-clamp electronics, and has become the gold standard for ion channel studies.

Patch clamp recordings of cell membranes can often resolve gating transitions of single ion channels, and these recordings have yielded many critical insights into the biophysical functions of proteins in cell membranes. The precision with which ion channels can be recorded has led them to remain an important area of study for many years, both from a pure research standpoint as well as for commercial drug development. However, electronic measurement noise remains a limiting factor, constraining the time resolution of single-channel recordings and leaving many fast-gating and low-conductance channels beyond the reach of today's single-channel techniques.

2.3 Nanopore sensors

A more recent spin-off from the world of electrophysiology is the nanopore sensor. A nanopore is a statically-open ion channel; it is a nanoscale hole in an insulating membrane between two electrolytes. A voltage bias is applied across the two sides of the membrane, and a steady-state ionic current develops through the pore. The distinguishing feature of a nanopore sensor is that the molecule under investigation is not the ion channel itself; instead, one measures the effect that another nearby molecule has on the nanopore's ionic current. The analyte molecule may block the opening of the channel, or it may pass entirely through the pore, travelling from one side of the membrane to the other.

Conceptually, this sensing strategy can be considered to be a single-molecule adaptation of a Coulter counter [15,16], which uses modulations in the conductance of a micro-scale electrolyte channel to count and characterize cells and particles in solution. At the same time, the physical arrangement of a nanopore has a great many similarities to single-ion-channel recordings, and indeed the first demonstration of a nanopore sensor was achieved using a transmembrane protein in a lipid bilayer [10]. Many of the tools for nanopore sensors are thus inherited from electrophysiology platforms.

Considered in comparison to other single-molecule sensing platforms, nanopores produce very large output signals [17]. For example, many popular optical single-molecule techniques rely on fluorescence, but the brightest fluorophores emit only several throusand photons per second. By contrast, the ionic current signals from a nanopore correspond to the coordinated motion of millions or billions of ions.

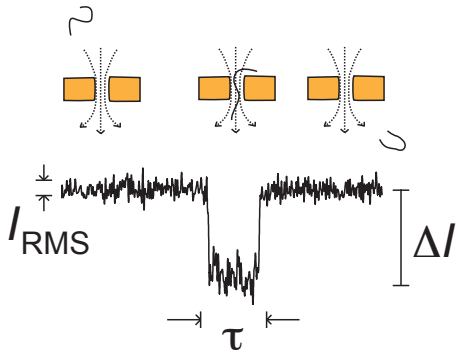

Figure 2.2: Typical signal output from a nanopore sensor.

Nanopore sensors have since been implemented with a range of different materials, including several types of ion channel proteins [10,11,18], solid-state dielectrics [19], polymer films [20], and even atomically-thin sheets of graphene [21–23].

The types of signals recorded from nanopore sensors tend to have similar features, despite differences in their physical construction. Current (I) signals from nanopores are usually transient and described by their depth (ΔI) and duration (τ) (Fig. 2.2). An important distinction between nanopores and ion channels is that the timescale of ion channel signals are related to the gating conformations of the channel protein itself, while the durations of nanopore signals can be traced to the transport rates of the analyte molecules in solution.

Nanopores have often been used to measure nucleic acid polymers such as DNA. The ability of a nanopore sensor to produce a relatively large output signal corresponding to a single molecule of DNA is a function of its nanoscale geometry. The diameter d of a pore can range from $1 - 100\ nm$, and due to Debye charge screening in the electrolyte [24], the ionic current is highly insensitive to charge sources more than a few nanometers from

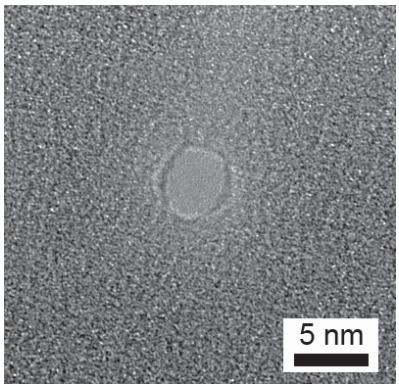

Figure 2.3: Transmission electron microscope image of a solid-state nanopore in a silicon nitride membrane.

the pore. A simplified electrical model of a nanopore is to treat it as a resistive cylinder of diameter d and length h, which contains mobile dissolved ions with a volume concentration σ_{ions} and mobility μ_{ions} similar to the bulk ion concentration. By this model, the baseline bias current can be described by [25]:

$$I_{bias} = V_{bias} \times \sigma_{ions} \times \mu_{ions} \times \frac{\pi d^2}{4h} \tag{2.1}$$

As a first-order approximation, we can assign a long molecule of DNA an effective length L_{DNA}, electrophoretic mobility μ_{DNA}, and electrostatic cross-sectional area A_{DNA} in which it excludes mobile ions. Together the mobility and length will result in a characteristic transit time τ and the presence of the molecule in the pore will result in a change in the measured ionic current. Together, this means the total number (n) of unit charges (q) collected per molecule is:

$$n_{signal} \approx \frac{\Delta I \times \tau}{q} \approx \sigma_{ions} A_{DNA} \frac{1}{q} \frac{\mu_{ions}}{\mu_{DNA}} \frac{L_{DNA}}{h} \tag{2.2}$$

Since $\mu_{ions} \gg \mu_{DNA}$, we can see that a nanopore provides gain through the multiplying effect that a comparatively slow-moving DNA molecule has on the nearby concentration of higher-mobility salt ions.

We note that the pore diameter d affects I_{bias} but not n_{signal}. As a result, d primarily affects the background signal level. If the pore is much larger than the effective cross-section of a translocating molecule, then the noise associated with the bias current can

quickly obscure the signal. Typically the most sensitive nanopores have diameters of 5 nm or less. The finite thickness h of the membrane also diminishes the geometric sensitivity of the pore, with the membrane thickness playing a role similar to the channel length of a transistor, with an inverse relationship between h and I_{bias}. Fabricating nanopore sensors in membranes such as graphene [21–23] and ultra-thin Si_3N_4 [12] produce gain and bandwidth improvements analogous to those achieved by FET channel length scaling [26, 27].

One of the earliest recognized potential applications for nanopore sensors was nucleic acid sequencing [28]; conceivably, the identity of bases in a linear nucleic acid could be inferred via the recorded ionic current as the molecule passed through a nanopore. However, managing the short timescales of nanopore sensor outputs has been a major obstacle to achieving this vision.

2.4 Signals and Noise

'Noise' can mean many different things. In the context of data acquisiton and signal processing, noise refers to undesirable and often unpredictable elements which compete with a target signal. However, not all noise sources are alike, and before proceeding we will make a distinction between interference, sensor variability, and intrinsic noise.

By 'interference', we refer to corruption of a measurement by unrelated signals or power sources, such as the appearance of 60 Hz tones from AC power lines and fluorescent lighting; the unintended coupling of digital logic into sensitive analog paths; or electronic interconnects behaving as antennae and picking up nearby radio frequency signals.

By 'sensor variability' we refer to errors that result from the fact that even nominally identical measurements can differ. Two solid-state nanopores may not have the same dimensions; time may have elapsed; chemical conditions such as pH and temperature may have changed; a laboratory technique may not have been applied identically.

Under ideal experimental conditions, both interference and sensor variability can be reduced to arbitrarily small levels. But the third category of noise sources, 'intrinsic noise', is fundemental to the recorded signal. Reducing it will require attention to the physical

design of the sensor as well as the electronic signal path used to measure it.

Assuming a linear time-invariant system in which we are measuring an electrical current $I(t)$, the noise can be considered as being simply added to the signal of interest:

$$I(t) = I_{signal}(t) + I_{noise}(t) \tag{2.3}$$

$I_{noise}(t)$ is stochastic and its value cannot be predicted for any particular moment in time. However, we can describe I_{noise} in the frequency domain by its power spectral density $S_n(f)$. In the time domain, we will model it as having a normal distribution with mean zero and standard deviation I_{rms}. The width of this distribution is a function of the power spectral density as well as the temporal resolution (τ_{min}) of the recording, which is related to the measurement bandwidth ($B \approx \frac{1}{2\times\tau_{min}}$):

$$I_{rms}(B) = \sqrt{\int_0^B S_n(f)df} \tag{2.4}$$

Note that this describes a relationship between the expected noise amplitude and the measurement bandwidth, and that since $S_n(f) > 0$, I_{rms} increases monotonically with B. In any given system, faster measurements usually carry intrinsically higher noise. But it is important to remember that the measurement bandwidth B simply limits the rate at which we choose to observe $I(t)$; the physical signal may very well contain features faster than τ_{min}, which will be obscured by the choice of B.

2.4.1 Signal-to-Noise Ratio (SNR)

An important metric to consider in a noisy system is the relative magnitude of the signal and noise. There are several different conventions for describing the signal-to-noise (SNR).

In electronic communications, where frequency-domain operations are common, one usually expresses the SNR in terms of a power ratio:

$$SNR = \frac{P_{signal}}{P_{noise}} = \frac{i^2_{signal}}{i^2_{noise}} = \frac{v^2_{signal}}{v^2_{noise}} \tag{2.5}$$

But in other contexts, including ion channel and nanopore literature, where time-domain measurements are more common, SNR is often expressed as a ratio of *amplitudes*

rather than power:

$$SNR = \frac{i_{signal}}{i_{noise}} = \frac{\Delta I}{I_{RMS}} \tag{2.6}$$

To be consistent with electrophysiology literature, in this work we will express SNR as a ratio of amplitudes, rather than power, unless otherwise noted.

2.4.2 Pulse Detection Limits

Ion channel and nanopore signals can often be considered to contain a series of current pulses, each corresponding to a channel gating transition (in the case of an ion channel) or an interaction with a single analyte molecule (in the case of a nanopore). Thus before the events can be analyzed, their presence or absence must be detected. It is helpful to consider the limits of detecting simple time-domain current pulses in the presence of background noise.

Accurate signal detection implies both the successful identification of actual events as well as the avoidance of false events, i.e. noise fluctuations incorrectly reported as signals.

Spurious Events

At some specific moment in time (t_0), $I_{noise}(t_0)$ can theoretically have any value, except that larger values are increasingly unlikely. (As above, we assume I_{noise} has zero mean.) Quantifying this likelihood is important when one attempts to detect rare signal pulses; if a brief pulse is observed in $I(t)$, it is always possible that it arose from I_{noise} rather than I_{signal}.

For an event detection threshold $\phi = \Delta I_{thresh}/I_{rms}$, a Gaussian noise process will produce an expectedrate of false events (λ_f), given by [3]:

$$\lambda_f = k \times B \times e^{-0.5\times(\frac{\Delta I_{thresh}}{I_{rms(B)}})^2} \tag{2.7}$$

where k is a constant in the range of 0.849 to 1.25, B is the signal bandwidth, ΔI_{thresh} is the minimum detectable event amplitude, and $I_{rms}(B)$ is the root-mean-squared amplitude of the noise.

If true events are infrequent, or if high bandwidths are used, a larger detection threshold is needed to prevent false detections from overwhelming the actual event rate. For example, with data presented in later chapters, we will use an detection threshold equal to five standard deviations from the baseline signal level ($\phi = \Delta I_{thresh}/I_{rms} = 5$). Since the signal should be larger than the threshold, this dictates that for a given dataset a bandwidth B should be chosen such that $I_{rms}(B) < \frac{\Delta I}{5}$. In this case we would expect to see false events at a rate of approximately $3B \times 10^{-6} Hz$. For example, signal bandwidths of $1kHz$ and $1MHz$ would yield approximately one false event every 5 minutes or 300 milliseconds, respectively.

Maximizing Event Detection

Separate from the expected rate of spurious events, there are often some number of real events which remain undetected below the noise floor. When we have the freedom to select an optimal measurement bandwidth, the important metric for the detectability of a current pulse is its total energy rather than its amplitude or duration alone [29].

The optimal bandwidth for missing the fewest real events is a function of τ as well as the shape of the noise spectrum [3]. The power spectral density of a rectangular pulse of amplitude $A = \Delta I$ and duration τ is:

$$S_n(f) = A^2\tau^2 sinc^2(f\tau) \tag{2.8}$$

This is a difficult expression to work with analytically. However, we can recognize that the pulse contains a total energy $E = A^2 \times \tau$, which is spread roughly evenly across the spectrum from $0Hz$ to $\frac{1}{\tau}\ Hz$. Thus we can coarsely approximate it as:

$$S_n(f) \approx \begin{cases} A^2\tau^2 & f < \frac{1}{\tau} \\ 0 & otherwise \end{cases} \tag{2.9}$$

We can further approximate that a low-pass filter with a cutoff frequency $B \ll \frac{1}{\tau}$ will reduce the total pulse energy to $E' = \int_0^B S_n(f)df = A^2\tau^2 B$. The pulse will additionally be distorted by the filter to a new duration of $\tau' \approx \frac{1}{B}$. Thus it will have been reduced to a

new amplitude $\Delta I' = \sqrt{E' \times B} = \sqrt{(A^2\tau^2 B) \times B}$, and we can approximate the amplitude of a bandwidth-limited rectangular pulse as:

$$A' = \begin{cases} A\tau B & B < \frac{1}{\tau} \\ A & otherwise \end{cases} \tag{2.10}$$

As discussed, a reasonable metric for pulse detection SNR is to compare the amplitude of the pulse to the expected amplitude of the noise. Since both the amplitude (A') and the noise (I_{rms}) are functions of B, we can expect the SNR to be a function of bandwidth as well. We would like to choose B to optimize the SNR, but the optimal B varies with the characteristics of the noise power spectral density $S_n(f)$:

If the noise power spectral density scales as $S_n(f) \propto 1/f$, then $I_{rms}(B)$ is roughly constant. In this regime, since noise is constant while the signal power is monotonically increasing, optimal detection occurs when the bandwidth is maximized. Here the noise limitation will appear as spurious events rather than undetected events.

When the noise power density is constant, $I_{rms} \propto \sqrt{B}$. This implies that at low bandwidths, where $A' \propto B$, the signal increases faster than the noise, while at high bandwidths, where $A' = A$, the signal is constant but the noise continues to increase. Thus in this scenario for optimal detection we should set $B \approx 1/\tau$.

On the other hand, if the noise power spectral density is increasing with frequency, then it is possible that $I_{rms}(B)$ will increase more steeply than $A'(B)$. The noise and signal amplitudes would increase equally with bandwidth if $S_n(f) \propto f$, in which case $I_{rms}(B) \propto A'(B) \propto B$. If $S_n(f)$ increases more steeply than f, pulse detection worsens with any increase of bandwidth.

In a later discussion we will see that high-bandwidth voltage-clamp current recordings often have noise power spectral density which increases with frequency. From the analysis above, we can conclude that a first-order estimate of the optimal measurement bandwidth B' will be the *lesser* of two values:

1. The bandwidth of the signal pulses, $B' \approx 1/\tau$.

2. The onset of a regime in which the noise power spectral density increases faster than $S_n(f) \propto f$.

2.4.3 Bandwidth-Dependent SNR

For a more precise determination of SNR as a function of measurement bandwidth, we can build a simplified mathematical model for $SNR(B)$. Previous nanopore and ion channel studies [12,30,31] defined the signal amplitude as ΔI, the average change in current due to a gating transition or an analyte molecule arriving at a nanopore. This leads to a signal-to-noise metric of $SNR(B) = \frac{\Delta I}{I_{rms}(B)}$.

We can further modify this expression to model the signal in time as well as amplitude; we will consider a rectangular signal pulse of amplitude ΔI with a duration τ. In the previous discussion it was shown that such a pulse contains a total energy $E = (\Delta I)^2 \times \tau$. Once again, rather than work with *sinc* functions, we can make an approximation. Here, rather than assume an abrubt band-limited spectral density, we can approximate the pulse energy as:

$$E' \approx \frac{\Delta I^2 \tau}{1 + \frac{1}{\tau B}} \approx \frac{E}{1 + \frac{1}{\tau B}} \tag{2.11}$$

which then allows us to modify the SNR expression to:

$$SNR(B, \tau) \approx \frac{\Delta I}{I_{rms}(B)} \times \frac{1}{\sqrt{1 + \frac{1}{\tau B}}} \tag{2.12}$$

This new expression more appropriately captures the fact that signal is dynamic, so SNR is no longer a monotonically decreasing function of measurement bandwidth. Once again it is helpful to emphasize that B is a freely chosen parameter, unlike ΔI and τ which are determined by physical laws.

2.4.4 Noise-Limited Bandwidth

As discussed, in a DC-coupled measurement the time-domain noise $I_{rms}(B)$ increases monotonically with bandwidth. Thus if one defines a maximum acceptable noise amplitude $I_{rms-max}$, the noise spectral density $S_n(f)$ leads to a single maximum bandwidth B_{max}

such that $I_{rms}(B) \leq I_{rms-max}$ for $B < B_{max}$:

$$I_{rms-max} = \sqrt{\int_0^{Bmax} S_n(f)df} \tag{2.13}$$

It can be more useful to relate B_{max} to the minimum acceptable SNR, rather than I_{rms}. For example, using the simple $SNR_{min} = \Delta I / I_{rms-max}$, we can adjust the relationship to:

$$SNR_{min} = \frac{\Delta I}{\sqrt{\int_0^{Bmax} S_n(f)df}} \tag{2.14}$$

A graphical representation of the relationship between $S_n(f)$ and B_{max} is shown in Fig. 2.4. If an explicit expression for $S_n(f)$ is known, these expressions can be rearranged to give a closed-form definition of B_{max}. This will be done in later sections.

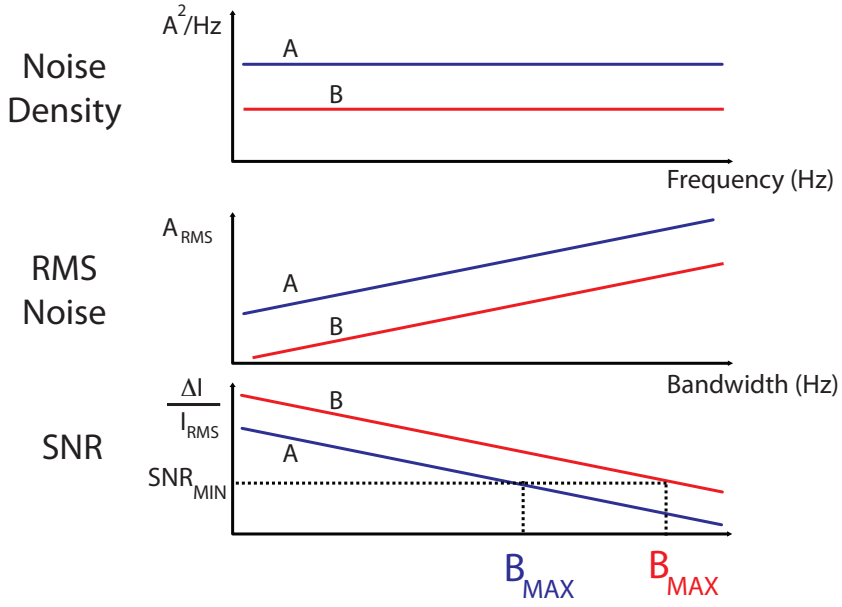

Figure 2.4: Maximum signal bandwidth as limited by the signal-to-noise ratio. When the noise density decreases from Scenario A to Scenario B, the RMS noise decreases at all frequencies, SNR increases at all bandwidths, and acceptable SNR is maintained at higher bandwidths.

2.4.5 Input-Referred Noise

Typically one measures a signal (along with any noise) at the output of a series of linear amplifiers and filters. Elements in the signal chain will amplify or filter anything presented

to their input, whether it originated from a signal or noise source. Thus a noise source may contribute differently to the measured output noise depending on where in the signal path it is introduced.

Signals measured at the output are referred to their corresponding input signals by dividing by the gain in the signal path. The same can be done for noise spectral density:

$$S_{n-input}(f) = \frac{S_{n-output(f)}}{G^2(f)} \tag{2.15}$$

where $G(f)$ is the signal amplitude gain between the input and output. This expression is true regradless of what path the noise followed to reach the output, and this concept can be applied to systems with multiple noise sources and amplification stages. When there are multiple independent noise sources, each source is individually input-referred by the gain between it and the input. The input-referred noise density is given by:

$$S_{n-input}(f) = \sum_i \frac{S_i(f)}{G_i^2(f)} \tag{2.16}$$

An example generic single-molecule signal chain illustrated in Fig. 2.5. Here, the input-referred noise is given by:

$$S_{n-input}(f) = S_{n-specificity}(f) + \frac{S_{n-interference}(f)}{(A_T(f))^2} + \frac{S_{n-detector}(f)}{(A_T(f) \times \frac{1}{Y_D(f)})^2} + \frac{S_{n-amplifier}(f)}{(A_T(f) \times \frac{A_D(f)}{Y_D(f)} \times A_A(f))^2} \tag{2.17}$$

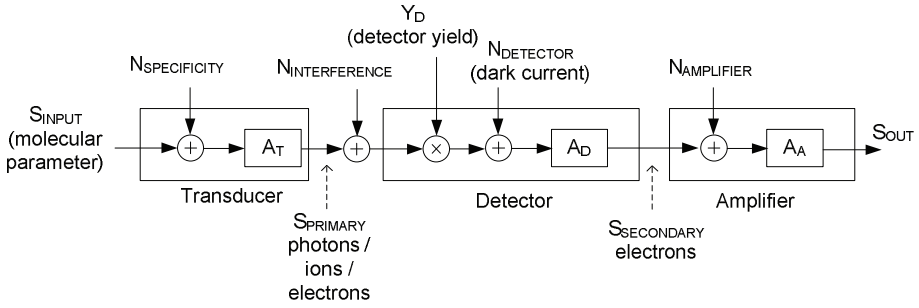

Figure 2.5: Schematic of a single-molecule sensor signal path, showing several gain elements and noise sources.

For these reasons, noise sources closer to the input tend to contribute more to $S_{n-input}(f)$. In optimized electrophysiology instruments it is often (though not always) true

that all dominant noise sources are physically located at the input of the transimpedance preamplifier. It is also useful to note that although in practice it is common to design a signal chain with a gain that is constant over frequency ($G(f) = G_{DC}$), this is merely a convenience for later analysis. If the important noise sources occur early in the signal chain, changing the frequency response of amplifiers and filters after them does not change the input-referred noise density.

2.5 Physical Noise Sources

The noise level of a measurement can be purely empircal; measuring $S_n(f)$ does not require knowing the physical noise sources. But in order to design a system for low-noise measurements, it is necessary to consider the physical origins of the noise. Generally speaking, noise sources arise either from the coupling of thermal energy into the signal path, or from components of the signal which are fundamentally discrete.

All electrical resistors and interconnects exhibit thermal noise, also called Johnson noise, whose power spectral density is proportional to the absolute temperature and can be described by

$$S_P(f) = 4kT \, \frac{W}{Hz} \tag{2.18}$$

where k is boltzmann's constant, and T is the absolute temperature. This thermal noise *power* does not depend on the value of the resistor, but the real electrical resistance ($R = Re\{Z\}$) of an element determines how this thermal power manifests as an electronic signal; for a lumped 2-terminal resistor model it can equivalently be expressed as a voltage $S_V(f) = 4kTR \, \frac{V^2}{Hz}$ or as a current $S_I(f) = \frac{4kT}{R} \, \frac{A^2}{Hz}$.

Because electrons are discrete particles, electrical currents consist of discrete charge movements. If charge carriers travel across a unidirectional barrier, such as a diode or an asymmetric ion channel [32], then at short timescales, the current can be modeled as stochastic arrivals of independent and discrete charge packets. This scenario yields a noise

spectral density of:

$$S_I(f) = 2qI \ \frac{A^2}{Hz} \tag{2.19}$$

The drain current (I_D) of a transistor will fluctuate, and thus by input-referring this noise through its small-signal transconductance (g_m), a transistor will have some equivalent input voltage noise. Weakly-inverted metal oxide field effect transistors (MOSFETs) and bipolar junction transistors (BJTs) exhibit shot noise [33], and thus their equivalent input voltage noise is:

$$S_V(f) = \frac{2qI_D}{g_m^2} \ \frac{V^2}{Hz} \tag{2.20}$$

Similarly, a Junction Field Effect Transistor (JFET) exhibits thermal noise in its channel (R_C) [34] and thus its equivalent input voltage voltage noise is:

$$S_V(f) = \frac{4kT}{g_m^2 R_C} \ \frac{V^2}{Hz} \tag{2.21}$$

Both thermal and shot noise have spectral density which is constant over frequency, but not all noise sources share this property. Many electronic elements also exhibit noise which has a $S_n(f) \propto 1/f$ relationship [35]. This arises from the existance of many uncorrelated fluctuations on different timescales, such as varying chemical surface states or electronic scattering sites. Often the strength of $1/f$ noise is related to the physical volume of an electronic element; in a given technology, smaller components will produce larger $1/f$ fluctuations.

Noise can also have power density which increases with frequency, such as the thermal noise from a capacitor C made from an insulating material with a dielectric loss factor $\tan\delta$ [36]:

$$S_I(f) = 8\pi f kTC \tan\delta \ \frac{A^2}{Hz} \tag{2.22}$$

As discussed earlier, the input-referred noise contribution of each physical element will be shaped by its location in the signal path. The process of referring a noise source through earlier frequency-dependent gain elements can also change the shape of its input-referred noise spectrum.

2.6 Transimpedance amplifiers

This work focuses on measurements of weak current signals in which the first amplification stage has the largest impact on the overall noise floor. There are a range of transimpedance amplifier topologies which are designed to amplify a weak current signal and express it as a higher-power voltage signal [33, 37]. An ideal transimpedance amplifier has both a low input impedance and a low output impedance, making it particularly suitable for wideband signal amplification.

2.6.1 Ideal Voltage-Clamp Amplifier

The classical transimpedance amplifier consists of an operational amplifier with a resistor in negative feedback, as shown in Fig. 2.6. The operational amplifier applies current through its feedback resistor in order to maintain a constant voltage at the input node. The input terminal of the operational amplifier draws no current, and thus all of the signal current flows through the feedback path. The output voltage is related to the input current by $V_{out} = V_{clamp} + (I_{in} \times Z_F)$. This can be called a *voltage-clamp* amplifier because its feedback loop actively clamps the input to a constant voltage.

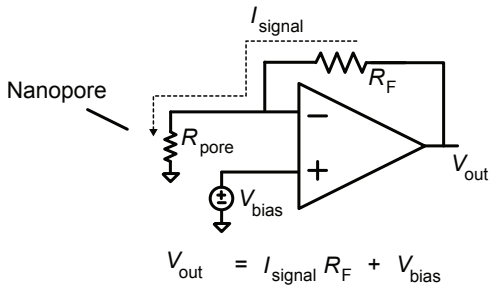

Figure 2.6: Circuit model of an ideal classical transimpedance amplifier.

2.6.2 Practical Voltage-Clamp Amplifier Considerations

In any practical implementation of a transimpedance amplifier, there are a number of non-idealities that must be considered carefully. A complete discussion of these nonidealities [33]

is beyond the scope of this work, but the main elements which impact the bandwidth and noise of the circuit are presented here.

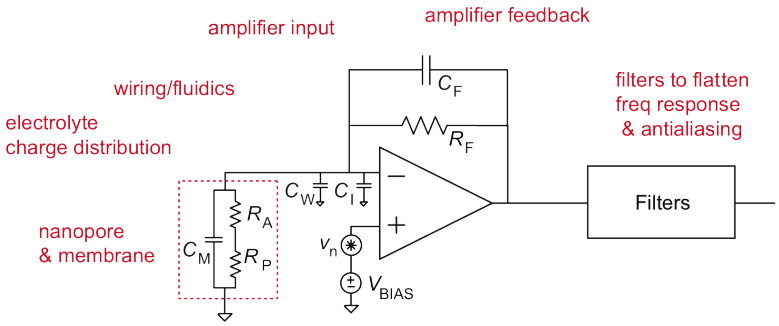

Figure 2.7: Schematic of a transimpedance amplifier showing several non-ideal elements which contribute to the noise floor of the system.

Open Loop Gain

While in many situations it is reasonable to assume that an operational amplifier has infinite open-loop gain, in practice this is not true. At DC, a commercial amplifier will often have gain A_{OL} of several thousand or million V/V, but its open-loop gain decreases at higher frequencies, eventually reaching a frequency known as the *unity gain bandwidth* at which point the open-loop gain is 1. Operational amplifiers are often designed to have a single dominant pole, so that their high-frequency response is characterized by a 90° phase shift, declining open loop gain, and a constant gain-bandwidth (GBW) product. At moderate frequencies, the open loop gain $A_{OL}(f) = \frac{GBW}{f}$.

A stable voltage-clamp preamplifier has a flat gain response at low frequencies, and a -3dB frequency of $f_c = 1/(2\pi R_F C_F)$. The finite gain-bandwidth of the operational amplifier requires that in order to avoid oscillation, the loop gain be reduced at high frequencies, by placing f_c no higher than [38]:

$$f_c \leq \sqrt{\frac{GBW}{2\pi R_F(C_I + C_W + C_M + C_S)}} \tag{2.23}$$

Designing a stable high-bandwidth amplifier can require high power dissipation and careful design, but compensated amplifiers with GBW as high as 1 GHz are fairly common.

Rearranging the above expressions, we can say that in order for the feedback loop to remain stable,

$$GBW \geq f_c^2 \times 2\pi R_F(C_I + C_W + C_M + C_S) = \frac{2\pi R_F(C_I + C_W + C_M + C_S)}{(2\pi R_F C_F)^2} \tag{2.24}$$

Finite open-loop gain is unavoidable, but we can see from these expressions that parasitic input capacitances threaten the feedback stability and require f_c to be decreased. The lower closed-loop transimpedance gain at frequencies above f_c means that elements later in the signal chain make increasingly significant contributions to the input-referred noise.

Amplifier Input Capacitance

The operational amplifier has some input capacitance (C_I) due to transistor gate capacitance, internal interconnects, and electrostatic discharge (ESD) protection circuits. With careful design, this can be reduced to single-digit pF, but it will never be zero. The input capacitance of a transistor is proportional to its physical size, but reducing the size of the transistor can mean lower GBW and larger v_n. Since C_I appears in the noise expressions as a sum with other parasitics, there are diminishing returns to reducing it below a certain level. For a given parasitic capacitance, minimum noise is usually achieved when the amplifier input is roughly matched to the other capacitances ($C_I \approx (C_W + C_M + C_S)$) [29], but in all scenarios lower parasitic capacitance will yield lower noise.

Input Bias Current

Although an ideal operational amplifier has infinite input impedance, an actual amplifier will draw non-zero input current. This may arise from leakage into the gate of the first transistor, or from reverse-biased electrostatic discharge (ESD) protection diodes in the amplifier. The input bias current adds a DC offset to the signal, which can be subtracted out during calibration. But a more pressing consequence is usually the shot noise contributed by the leakage current, which adds $S_I(f) = 2qI_{leakage}$ to the input-referred noise density.

Offset Voltage

The operational amplifier will have some offset voltage, due to device mismatch and unbalanced differential inputs circuits. Offset is not usually a primary concern in these applications, as it does not add any noise and can be easily subtracted from the output, unless it has a strong temperature dependence or drift.

Dynamic Range

An amplifier will operate within a finite power supply, and thus the output voltage is constrained to a maximum value of V_{DD}. For a linear and constant transimpedance gain R_F, this implies that the maximum measurable current is V_{DD}/R_F. The minimum measurable current will be dictated by the noise floor.

Amplifier Voltage Noise

The operational amplifier is an active element and thus it adds noise in addition to amplifying the voltage presented at its input. In this topology the amplifier voltage noise manifests as fluctuations in the *clamp voltage*, which is applied across the device under test along with the DC bias. If the power spectral density of the amplifier input voltage noise is a constant $e_n = S_v(f) = v_n^2$ (with units V^2/Hz), this results in a current noise power spectral density of:

$$S_n(f) = v_n^2 \times (2\pi f(C_I + C_W + C_M + C_S))^2 \tag{2.25}$$

If we additionally consider the $1/f$ component of the voltage noise density, then $S_v(f) = A_n/f + v_n^2$ and the input-referred current noise power density becomes:

$$S_n(f) = (A_n(2\pi\Sigma C)^2 \times f) + (v_n^2(2\pi\Sigma C)^2 \times f^2) \tag{2.26}$$

where $\Sigma C = (C_I + C_W + C_M + C_S)$. Thus it is possible for amplifier voltage to create either $S_n(f) \propto f$ or $S_n(f) \propto f^2$, depending on the scenario. Parameters which decrease $1/f$ voltage noise will decrease the frequency at which this transition occurs. Generally speaking, requirements for low v_n will put a lower bound on the *power consumption* of the

amplifier, while requirements for low A_n will put a lower bound on the *physical size and input capacitance* of the amplifier.

Feedback Network Capacitance

The ideal transimpedance amplifier has a constant gain R_F across all frequencies, set by the real impedance of the element in its feedback path. Unfortunately, high-value resistors often have non-negligible parasitic capacitances, meaning that they are only resistive up to some frequency.

In a discrete board-level design, the primary parasitic for resistors is shunt capacitance across the two terminals of the device. For example, if a discrete 1 $G\Omega$ resistor has a shunt capacitance of 0.1 pF, it is only resistive below $f_1 = \frac{1}{2\pi f R_F C_F} = 1.6\ kHz$. Depending on the conditions, this may or may not itself limit performance, as some nonzero C_F is required for stability, as discussed previously.

For resistors in an integrated semiconductor process, the primary concern is usually distributed capacitance to the silicon substrate [39], rather than capacitance between the two terminals. For this reason integrated linear resistors greater than several hundred $k\Omega$ are uncommon, and wherever possible they are usually substituted with capacitors, nonlinear elements, or active circuitry.

Reference & Power Supply Voltage Noise

It is important to recognize that the current noise passed through each capacitive element in the circuit is a result of the differential voltage noise across it. For C_F this is always simply the amplifier voltage noise v_n, but for elements C_M, C_W, and C_I it is actually the power sum of the amplifier voltage noise along with any voltage reference and power supply noise: $v_{n-effective} = \sqrt{\Sigma_i\ v_i^2}$. Thus it is very important that all power supplies and voltage references be strongly decoupled to the clamp voltage.

Access Resistance

There will often be some non-zero resistance R_A in series with the DUT. This adds an effective voltage noise density $v_n^2 = 4kTR_A$, and additionally increases the input impedance of the amplifier, which reduces its bandwidth. Absent any series-resistance compensation, the bandwidth will be limited to $f_2 = \frac{1}{2\pi R_A C_M}$. Above f_2, the signal current will simply be absorbed by the parasitic device capacitance, rather than flow into the transimpedance amplifier. Patch-clamp amplifiers often include some degree of positive feedback to compensate for device series resistance [3].

Membrane Capacitance

Ion channels and nanopores are inevitably accompanied by some membrane capacitance C_M, which can be modeled as a parallel plate capacitor formed by dissolved ions accumulating on either side of the thin membrane that hosts the channels. The effective capacitance will be slightly lower than predicted by the exact geometry of the membrane, due to Debye screening in the electrolyte. But in moderate salt concentrations the Debye length is 1 nm or less, while device membrane thickness is on the order of 5 nm for lipid membranes and 10-50 nm for solid-state nanopores. Thus the parallel plate approximation is often accurate enough.

As discussed in other sections, this parasitic membrane capacitance can contribute to feedback loop instability, increased noise, and decreased signal bandwidth.

Wiring Capacitance

Wires connecting the measurement to the amplifier are usually physically much larger than the device being measured, leading the wiring to introduce significant capacitance. Shielded or coaxial cables introduce wiring capacitance of 10-30 pF per foot, and thus typically short unshielded wires are preferable for sensitive current measurements.

Data Acquisition

After amplifying the current signals, they will typically be digitized for storage and further analysis. It is important to avoid introducing more noise when digitizing the signal. There are two main concerns for digitization noise: aliasing and quanitzation noise.

Basic Nyquist sampling theory states that a discrete sampling frequency of f_s can only represent a signal bandwidth of $f_s/2$. If a uniformly sampled signal has signals outside this range, *aliasing* will occur and all of the signal power will be folded into the $f_s/2$ bandwidth. Aliasing concepts apply for noise density as well as signals, and thus in order to maintain a low noise spectral density it is important that the signal path be adequately filtered before being digitized.

To avoid noise aliasing, a low-pass filter should be added to the signal path before sampling. All filters have a finite cutoff slope, and thus the filter's corner frequency should be positioned *below* $f_s/2$ by a reasonable margin. Higher-order filters have steeper slopes in their cutoff bands, allowing the corner to be placed somewhat closer to $f_s/2$. Analog Bessel filters are popular for time-domain anti-aliasing low-pass filters because they maintain a constant group delay for their entire passband. The normalized response of a 4th-order Bessel low-pass filter is:

$$\left| H\left(\pi \frac{f}{f_c}\right) \right| = |H(\omega)| = \frac{105}{\sqrt{\omega^8 + 10\omega^6 + 135\omega^4 + 1575\omega^2 + 11025}} \tag{2.27}$$

where f_c is the cutoff frequency of the Bessel filter.

Quantization error is the the round-off error associated with representing a continuous signal amplitude with a discrete number. Technically this error is correlated with the signal, but in many practical scenarios quantization error can be modeled as an independent noise source. Assuming a uniform amplitude error profile, the error power is spread evenly across the Nyquist bandwidth, and the spectral voltage noise density associated with sampling is approximately:

$$S_{v-Q}(f) \approx \frac{V_{LSB}^2}{12 \times (f_s/2)} \tag{2.28}$$

where $V_{LSB} = \frac{V_{FS}}{2^N}$ is the ΔV which corresponds to the smallest quantization step and f_s

is the sampling frequency. When an N-bit converter with a full scale range V_{FS} is placed at the output of a transimpedance amplifier with constant $Z_{gain} = R_F$, the contribution of quantization noise to the input-referred noise density is:

$$S_n(f) = S_{v-Q}(f) \times (\frac{1}{Z_{gain}})^2 \approx (\frac{V_{FS}}{2^N})^2 \frac{1}{6f_s} (\frac{1}{R_F})^2 \tag{2.29}$$

2.6.3 Patch clamp amplifiers

Taking into account these practical voltage-clamp considerations, a simplified voltage-clamp circuit used in commercial patch-clamp amplifiers [40] is shown in Fig. 2.8. In order to achieve a low I_{BIAS}, small $v_n \times C_{IN}$, and moderate bandwidth, patch clamp amplifiers often implement a discrete JFET differential voltage amplifier. To improve the DC voltage gain, this JFET input stage is followed by an integrated circuit operational amplifier.

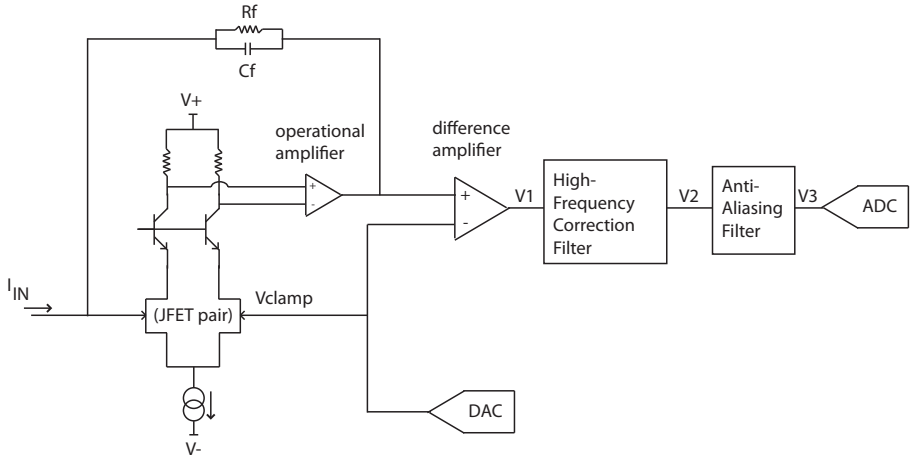

Figure 2.8: Circuit schematic of a discrete voltage-clamp preamplifier circuit commonly used in modern patch-clamp amplifiers.

As discussed, the initial transimpedance stage has reduced gain above $f_c = 1/(2\pi R_F C_F)$, and thus it is followed by a filter to extend the useful bandwidth, and an anti-aliasing filter prior to digitization. f_c is typically at a frequency lower than 1kHz, implying that meaningful millisecond-scale signals are actually being passed through C_F rather than R_F. The frequency response of these three signal stages is shown in Fig. 2.9. Typical feedback resistor values used in patch clamp amplifiers range from $R_F = 500\Omega$ for whole-cell and

nanopore recordings, to $R_F = 50G\Omega$ for single ion channel recordings. If the DC current is low enough, the feedback resistance can be removed entirely, which is the basis of capacitive-feedback headstages [40,41] used for some single-channel patch-clamp recordings. Although this improves the low-frequency noise density, with R_F removed entirely C_F needs to be reset periodically, which causes transients that can interfere with data acquisition.

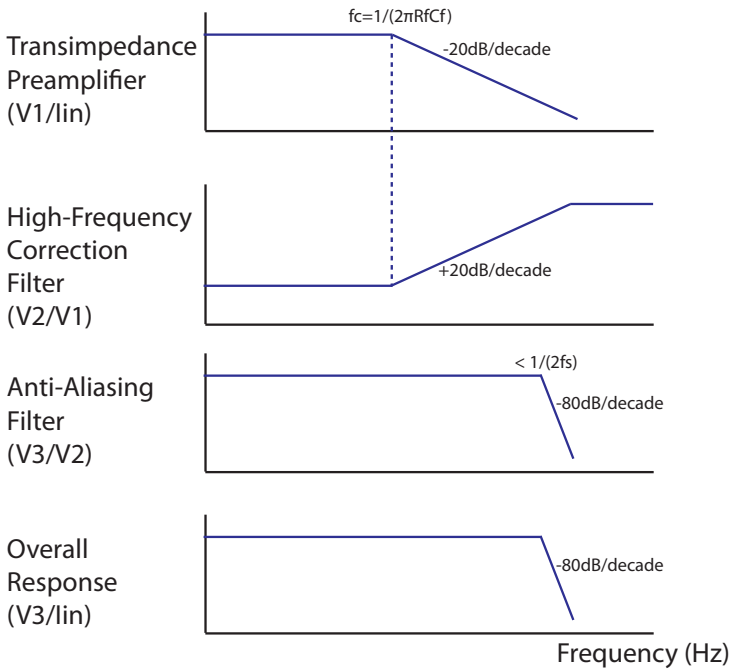

Figure 2.9: Illustration of the frequency response of a patch clamp amplifier, including its high-frequency correction filter and anti-aliasing filter, as discussed in the text. The signals I_{in} and V_{1-3} refer to Fig. 2.8

Patch-clamp amplifiers typically also include additional circuitry to compensate for some of the parasitic resistances and capacitances discussed above. (For a more thorough discussion of capacitance compensation and series-resistance compensation see Sigworth et al [40,42].) Generally these compensation circuits can only compensate the signal amplitude; input-referred noise is either unaffected or made worse by the compensation circuitry.

2.6.4 Voltage-Clamp Noise Model

The electronic open-circuit input-referred current noise for a voltage-clamp amplifier with nothing attached to its input is:

$$S_{n-open}(f) = 2qI_{bias} + \frac{4kT}{R_F} + (v_n(f) \times 2\pi f \sum C)^2 \frac{A^2}{Hz} \tag{2.30}$$

where I_{bias} is the input bias current into the negative operational amplifier terminal, $\sum C = (C_I + C_W + C_M + C_S)$, and $v_n(f)$ is the equivalent input voltage of the operational amplifier. (This expression assumes zero dielectric loss.)

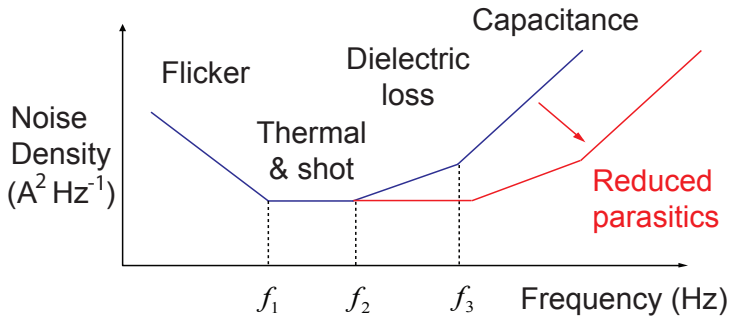

Figure 2.10: The noise power spectral density of a voltage-clamp recording often has several distinct regimes, in which different physical noise sources dominate. If parasitic capacitances are reduced, high frequency noise density will decrease proportionately.

When a device is attached to the input (Fig. 2.7), the sensor contributes its own noise as well as interacting with the feedback loop, and the input-referred current noise becomes

$$S_n(f) = \frac{A_I I^2}{f} + 2qI_{leakage} + \frac{4kT}{R_F} + \frac{4kT}{R_S} + (v_n(f) \times 2\pi f \sum C)^2 \frac{A^2}{Hz} \tag{2.31}$$

where R_S is the resistance of the sensor, and A_I is the sensor's flicker noise current coefficient. (Once again this expression assumes no dielectric loss.)

At different frequencies the dominant sources of noise will change, and we can refer to the frequencies of these transitions as noise corners ($f_1 - f_3$ in Fig. 2.10). However, it should be noted that these frequencies are simply the *intersection* of two different noise spectra, rather than the inherent shape of the noise density. If a noise source is early

in a signal chain, the *output*-referred noise will be shaped by the small-signal frequency response of later stages, but in an optimized system the input-referred noise corners $f_1 - f_3$ are entirely separate from small-signal frequency considerations.

It is clear that minimizing noise will consist of reducing leakage currents, reducing capacitances, reducing amplifier voltage noise, and maximizing transimpedance gain (R_F). However, achieving these goals will come with tradeoffs, and minimizing the total noise will require equal attention to the sensor construction, amplifier design, and the physical interfaces between them.

Maximum Voltage-Clamp Noise-Limited Bandwidth

As discussed earlier, for a given signal amplitude and minimum tolerable signal-to-noise ratio, the spectral noise floor will dictate the maximum signal bandwidth (B_{max}) that can be supported. With explicit expressions now derived for $S_n(f)$ for a voltage-clamp preamplifier, we can derive an expression for B_{max} in each of the noise regimes in Fig. 2.10.

If the current noise is dominated by 1/f noise such that $S_n(f) \approx A_I/f$, the maximum bandwidth is a function of discussed parameters along with the *minimum* required signal frequency f_{min}:

$$B_{max} \approx f_{min} \times e^{-\frac{1}{A_I}\frac{\Delta I^2}{SNR_{min}^2}} \tag{2.32}$$

If thermal noise of some resistance R_T is dominant, the maximum bandwidth is:

$$B_{max} \approx \frac{\Delta I^2}{SNR_{min}^2}\frac{R_T}{4kT} \tag{2.33}$$

If shot noise from a DC bias current I_{bias} dominates the noise density, the maximum bandwidth is:

$$B_{max} \approx \frac{\Delta I^2}{SNR_{min}^2}\frac{1}{2qI_{bias}} \tag{2.34}$$

If there is prominent dielectric noise from a capacitance C_{lossy} with loss tangent δ, the maximum bandwidth is:

$$B_{max} \approx \frac{\Delta I}{SNR_{min}}\frac{1}{\sqrt{4\pi kTC_{lossy}\tan\delta}} \tag{2.35}$$

And if capacitive noise is dominant, the maximum bandwidth is one of the following, depending on whether the operational amplifier is in a regime in which it exhibits a flicker-noise dominated $S_v(f) = A_v/f$, or a flat-band voltage noise $S_v(f) = v_n^2$:

$$B_{max} \approx \frac{\Delta I}{SNR_{min}} \frac{1}{\sqrt{2A_v}} \frac{1}{\pi(C_I + C_W + C_M + C_S)} \tag{2.36}$$

$$B_{max} \approx \left(\frac{\Delta I \sqrt{3}}{SNR_{min} \times 2\pi(C_I + C_W + C_M + C_S)v_n} \right)^{\frac{2}{3}} \tag{2.37}$$

Chapter 3

Design of A Low-Noise CMOS Transimpedance Preamplifier

3.1 Introduction

Low-noise transimpedance preamplifiers are well-travelled territory in analog microelectronics, particularly in the context of photodiode preamplifiers. However, compared to the market for optical communications, electrophysiology equipment commands much less commercial interest, and for the past thirty years the state-of-the-art ion channel recording systems have remained discrete modules constructed from off-the-shelf semiconductor components, rather than high-performance integrated semiconductors which dominate so many markets.

Recently, as nanopore and ion channel measurements have gained momentum for commercial molecular biology applications [43–45], there has been increased interest in integrated electrophysiology platforms for higher system density and parallelism [46]. Yet integrated transimpedance amplifiers designed for very low-current DC-coupled measurements [47–50] have often struggled to match the noise and bandwidth metrics of the best discrete amplifiers [40, 51], due to prioritization of power or area over noise as well as the unavailability of high-quality large-value resistors in integrated semiconductors.

If these impediments to a low noise integrated amplifier solution can be overcome, reductions in the physical size of electrophysiology amplifiers can also be accompanied by reductions in parasitic capacitances, which can in turn reduce noise levels and improve the available signal bandwidth in ion channel recordings.

3.2 Chapter Summary

This chapter discusses the design and implementation of a CMOS preamplifier optimized for low-noise DC-coupled current measurements, in a standard $0.13\mu m$ CMOS process. Eight independent channels are included on a $3mm \times 3mm$ prototype chip, with each preamplifier occupying $0.2mm^2$. The design supports DC - 1 MHz signal bandwidth, and has a dynamic range of 15 nA while achieving input-referred noise levels of $3.2pA_{RMS}$ and $24pA_{RMS}$ at 100 kHz and 1 MHz, respectfully.

3.3 Amplifier Topology

The amplifier circuit resembles a traditional operational amplifier based transimpedance stage, whose gain is determined by a high-value feedback resistor R_F. But several adaptations have been made to adapt this arrangement to a modern CMOS process.

The amplifier is designed to work within the standard $1.5V$ single-supply voltage range of commercial $0.13\mu m$ CMOS logic. Rather than a passive feedback resistance R_F, the circuit utilizes an acive low-noise transconductance, which is based around a low-noise current divider. To improve interference rejection and maximize dynamic range, the output signal is converted to a fully-differential analog voltage. A simplified single-ended equivalent schematic is shown in Fig. 3.2.

3.3.1 Feedback Network

As discussed, to minimize noise it is common for electrophysiology amplifiers to have a gain ranging from $50M\Omega$ to $50G\Omega$. However, producing an acceptable passive feedback network

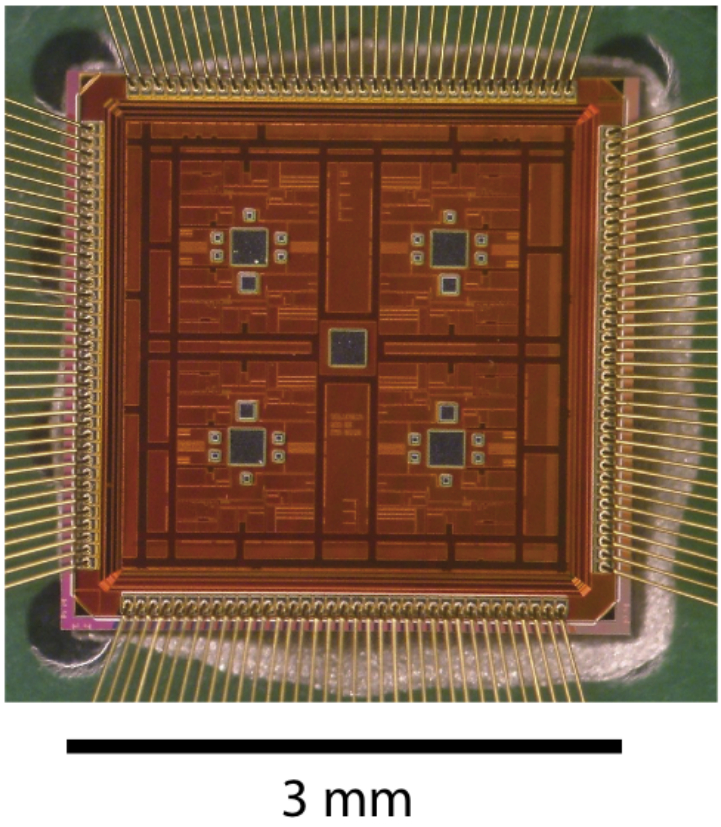

Figure 3.1: Die photo of the 8-channel low-noise current preamplifier.

on a CMOS chip for this application has proven to be challenging. Capacitors are readily available in integrated circuits, but reset transients of a pure capacitive feedback topology are troublesome. High-value linear resistors are impractical due to large areas and high parasitic capacitances.

To satisfy the above requirements, a topology was adapted which places a low-noise linear current source in the feedback path. This current source follows a $k\Omega$ resistor with a unique low-noise current divider based on a pair of ratioed PMOS transistors, shown in Fig. 3.3. To a first order, the current divider ratio depends only on the proportional sizes of the two transistors, and not their impedance. It is able to conduct bidirectional DC-coupled current signals; when sourcing current the PMOS transistors are weakly inverted, and when sinking current the current flows through forward-biased junction diodes. The

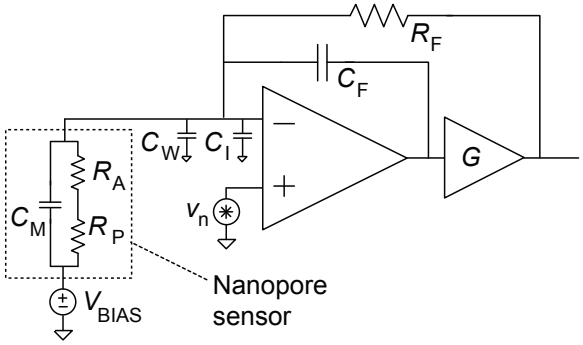

Figure 3.2: Circuit topology of the low-noise transimpedance amplifier.

output current is given by $I_{OUT} = \frac{V_{IN}}{R}\frac{W_1}{W_2}$, and thus the circuit behaves similarly to a linear resistor with $R_F = R\frac{W_2}{W_1}$. Component values were chosen to be $R = 50\ k\Omega$ and $\frac{W_2}{W_1} = M = 200$, yielding a nominal equivalent $R_F = 100\ M\Omega$.

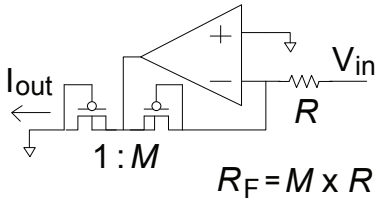

Figure 3.3: Circuit model of a low-noise current source.

The overall feedback loop is closed at the circuit board level rather than on the amplifier die. This arrangement does not impact the noise performance but was helpful in the initial debug and tuning of the system.

3.3.2 Operational Amplifier

The main voltage amplifier is a folded-cascode operational transconductance amplifier, as depicted in Fig. 3.4. The amplifier was designed to meet a range of criteria, including:

- Single-supply 1.5V operation
- Rail-to-rail output
- Sub-pA input leakage current

- Low equivalent input voltage noise
- Low input capacitance
- High gain-bandwidth product and acceptable phase margin

Compromises were made during the design, as some of these criteria are in contention, such as the desire to have both high bandwidth (suggesting large input transistors) and low input capacitance (suggesting small input transistors).

The differential input stage is a pair of PMOS transistors, whose properties are the most critical to the noise performance of the OTA. The input pair was constructed with thick-oxide transistors rather than the native thin-oxide, to eliminate gate leakage. They are sized at $\frac{W}{L} = \frac{800\mu}{240n}$ and biased with $160\mu A$. For nominal simulations, this results in $V_{gs} = 430mV$, below the V_t of $520mV$, placing the transistors in weak inversion. This is desirable as it reduces the effective gate capacitance and yields higher g_m/I_d than strong inversion. As biased, the input pair transistors each have $g_m = 3.45mS$ and $C_{gg} = 760fF$.

The input pair is folded into a cascode pair which drives a source-degenerated current mirror, and the second stage is a cascode-compensated [33] common source amplifier. Achieving a high output impedanc from the cascode stage using a supply voltage of only 1.5V was challenging, leading to the use of source degeneration resistors for the PMOS current mirror rather than an additional transistor pair. The OTA is compensated with a cascode-connected capacitor, providing consistent phase margin across a range of bias currents, and allowing a reasonable compensation capacitor value of 4.5 pF.

The OTA has a a gain-bandwidth product of 114 MHz with a phase margin of 56 degrees. Its equivalent input voltage noise is $5.2nV/\sqrt{Hz}$, with a $1/f$ corner below 100 kHz. The entire operational amplifier consumes 1 mA from a 1.5V supply. Each OTA occupies an area of approximately $0.02mm^2$, including the compensation capacitor. For simplicity of design, the same OTA is used in both the integrator and the feedback transconductor.

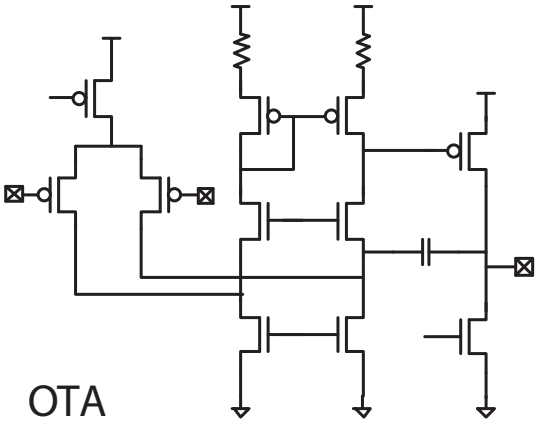

Figure 3.4: Folded-cascode operational transconductance amplifier.

3.3.3 Output Buffer

A fully-differential output buffer is included after the main integrator stage. This buffer serves both to convert the single-ended integrator output signal to a fully differential output, and to isolate the high-speed integrator from any larger off-chip capacitive loads which would degrade its phase margin. The fully-differential output helps to suppress interference and ground loops, as well as doubling the dynamic range of the preamplifier.

The output buffer is a load-compensated current-mirror design, which ensures it will be stable with any load. It is designed with a fairly low open-loop gain, and it has a continuous-time common-mode feedback path which regulates its output to a mid-rail common-mode.

The buffer consumes $900\mu A$ from the 1.5 V supply, and with a load of 8 pF it has a gain-bandwidth product of 55 MHz and a phase margin of 70 degrees. Differential resistive feedback is wrapped around the amplifier so that it has a closed-loop gain of approximately 6, which it is able to maintain to a bandwidth of approximately 10 MHz. The input-referred noise of the closed-loop buffer is $17nV/\sqrt{Hz}$ with a 1/f noise corner at 60 kHz. The 1/f noise is dominated by the OTA transistors, but above the noise corner the majority (72%) of the white noise power actually is generated by the feedback resistors rather than the transistors within the buffer OTA.

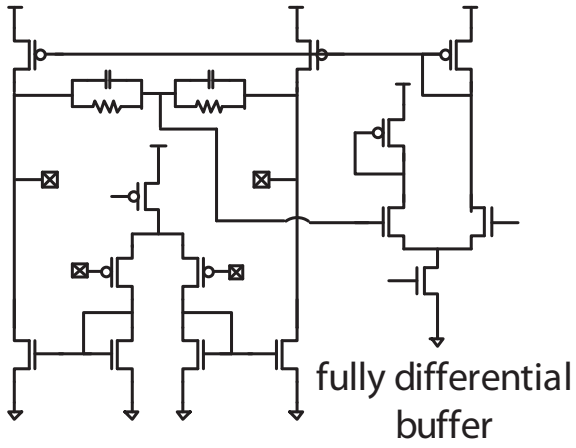

Figure 3.5: Fully-differential load-compensated output buffer.

3.3.4 Negative Capacitance

One factor which limits the stability of a closed-loop transimpedance circuit is the feedback pole at $\frac{1}{2\pi R_F \sum C}$, which worsens the phase margin and requires either that the feedback path zero at $\frac{1}{2\pi R_F C_F}$ be placed at a lower frequency, or that the GBW of the OTA be increased.

To improve this situation, a range of positive-feedback compensation circuits have been proposed [52], which inject current to bootstrap the input capacitance. For small amounts of positive feedback, this serves to reduce the effective small-signal capacitance and push the feedback pole to a higher frequency. For larger amounts of positive feedback, eventually the system will become unstable, so there is a limit to this technique, but at the margin it can help to boost the effective gain-bandwidth of the system.

For these purposes a programmable active negative capacitance bootstrap is included with each channel of the CMOS amplifier. The negative capacitance is formed with a capacitor in positive feedback around an operational amplifier. The voltage amplifier is formed with the same OTA as previously described, in a non-inverting voltage buffer configuration with a closed-loop gain of 3. The feedback capacitance is a digitally programmable bank of 8 binary-weighted capacitors, with a full scale range of 8 pF. With a gain of 3, this produces a programmable range of negative capacitance from 0 to -24 pF. If not in use, the circuit

can be fully powered down and disconnected from the integrator input.

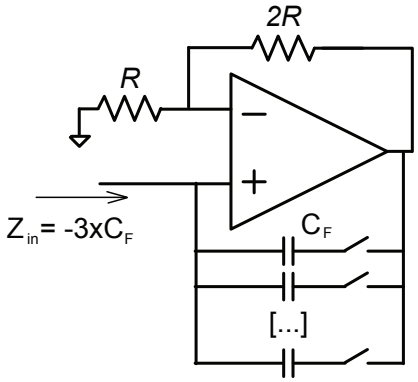

Figure 3.6: Digitally programmable negative capacitance.

In practice, while this bootstrap circuit can increase the bandwidth of the first TIA stage, it increases the effective input noise because it senses the main amplifier's voltage noise and amplifies it as if it were a signal. In most of the applications explored with this amplifier the limiting factor has been noise, rather than bandwidth, and so the negative capacitance circuit has been disconnected.

3.4 Other Features

3.4.1 Digital Control Interfaces

The chip has a number of analog elements which are digitally programmable, such as powering on and off each channel, or selecting the integration capacitance (C_F). These digital functions are enabled by four 32-bit digitally buffered scan chains. These scan chains are implemented using standard complementary 1.5V logic. Each element of the scan chains has an output latch allowing its value to be held constant while new values are shifted through the chain. A short delay line between each scan site protects the system against hold-time violations.

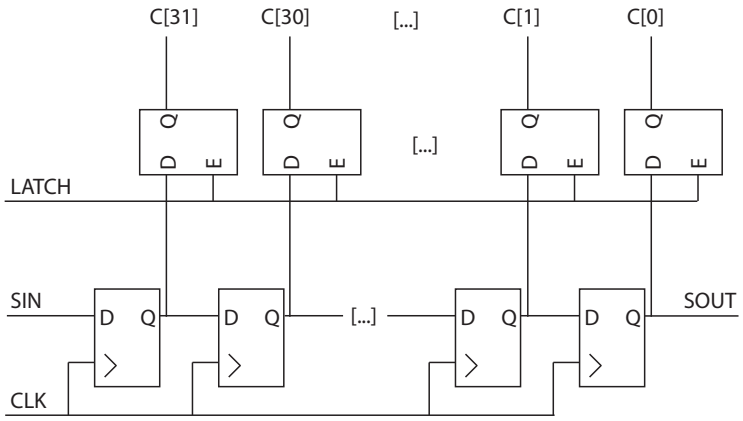

Figure 3.7: Digital control logic.

3.4.2 ESD & Isolation

Pins which interface outside the chip are usually equipped with protection circuits that help guard against electrostatic discharge (ESD), whose high voltages may damage the chip. However, these circuits typically involve large-area reverse-biased p-n junctions, with leakage currents on the order of pA or nA. Such leakage currents comparable to the expected signal levels, and would contribute offset and shot noise. In this design ESD protection circuitry was removed from signal paths which carry less than 1μA.

All of the circuits on the chip were also designed entirely with triple-well n-channel transistors, rather than bulk n-channel transistors. This helps to control cross-coupling from digital switching and from other channels, and it also allows the substrate to be biased independently from the signal ground. This would be an important in an arrangement with sensors that pass fully through the die [53], since the backside of the chip would be in contact with a biased electrolyte.

3.4.3 On-chip electrodes

To reduce capacitance associated with circuit board wiring, and to improve the density of the overall system, exposed metal electrodes were placed in the middle of the die next to the input of each preamplifier channel. These electrodes utilize the same lithography layers

as the bondpad I/O ring. However, in order to facilitate post-processing the chip to replace the standard alluminum metallization with a more favorable material, several design rules were waived.

The parasitics associated with on-chip electrodes can be approximated by a simple parallel plate capacitance between the electrode metal and the silicon substrate. In the metallization for this chip design, the top metal layer ("LM") is approximately $5.5\mu m$ from the silicon surface, through a series of dielectric materials consisting largely of silicon dioxide. Assuming a dielectric constant of 3.9, this leads to a parasitic capacitance of $6.3\mu F/cm^2$. This implies a parasitic capacitance to ground of 16 fF for a $50x50\mu m$ electrode, or 63 fF for a $100x100\mu m$ electrode. These values represent 2-8% of the amplifier input capacitance, and thus the electrodes themselves contribute only marginally to the high-frequency noise floor.

Post-processing of these electrodes will be discussed in more detail in Chapter 4.

3.5 Physical Layout

The full prototype amplifier die can be seen in Fig. 3.1. The layout of a single ampliier channel can be seen in Fig. 3.8, and a photograph of the same area is shown in Fig. 3.9. The full transimpedance amplifier (including the OTA, feedback network, output buffer, and input electrode) occupies $0.5mm \times 0.4mm$, while the optional negative capacitance and supporting digital circuitry add an additional $0.3mm \times 0.4mm$.

3.5.1 Reserved Nanopore Areas

This chip was designed with the potential for physical integration of solid-state nanopores into the CMOS die. As such, areas were reserved adjacent to the preamplifier channels which contained neither active transistors nor metal wiring. Additionally in these areas the metal fill (for planarization) was excluded. This will be discussed in more detail in Chapter 4.

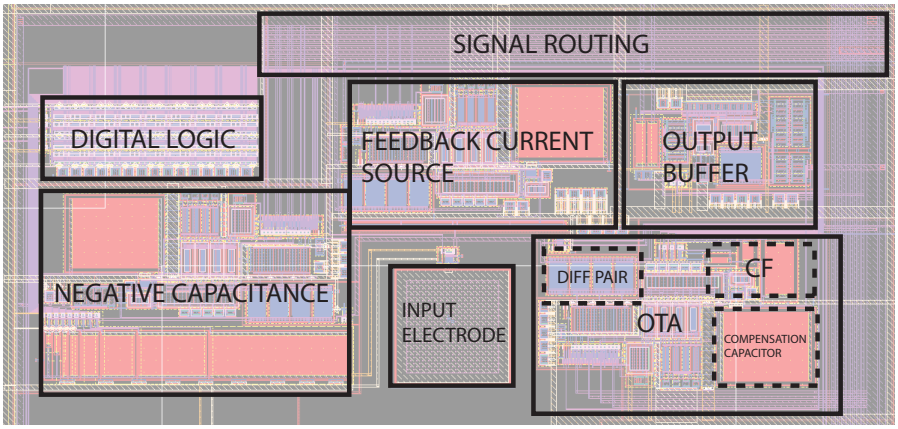

Figure 3.8: Design layout of one amplifier channel, with key functional blocks labeled.

3.5.2 Packaging

The chip was packaged in a 272-pin ball grid array (BGA) package. Its 140 I/O pads were wirebonded to a custom plastic laminate, and the wirebonds were covered with a doughnut epoxy encapsulation which left the majority of the die surface exposed, including the on-chip electrodes described above. This is a similar packaging as has been used previously for electrochemical CMOS sensor chips [54].

3.6 Circuit Board

3.6.1 System Overview

The entire amplifier system incorporates the preamplifier chip with a number of supporting electronic subsystems. A diagram of the entire system is shown in Fig. 3.10, and a photograph can be seen in Fig. 3.11.

3.6.2 Power & Biasing

The CMOS chip requires several supporting power regulation and simple bias circuits on the circuit board. The chip utilizes a 1.5 V DC power supply, and additionally requires several current biases and a mid-rail virtual ground voltage reference.

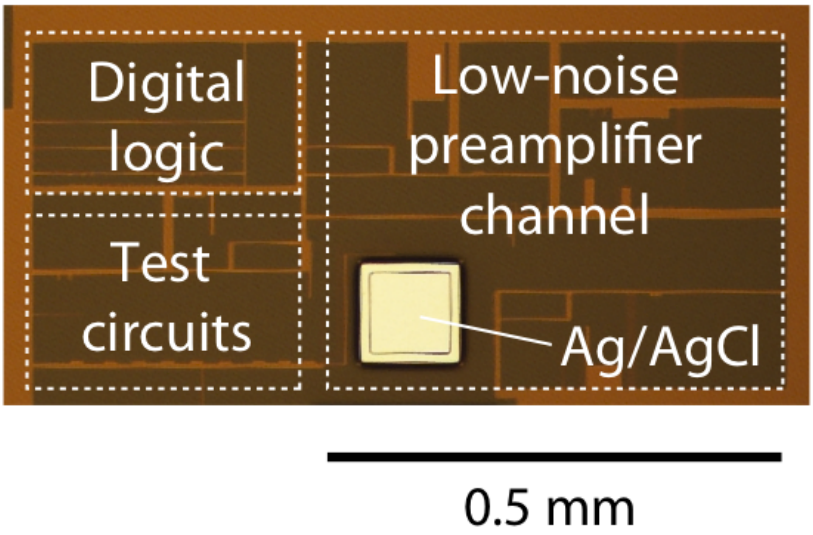

Figure 3.9: Micrograph of one channel of the fabricated amplifier.

The current biases serve to determine the Class A biasing of the operational amplifiers on the chip, and thus indirectly the current bias will modulate the bandwidth and noise performance of the system. However, the current bias inputs are only DC references, and are heavily filtered through the current mirror and with on-chip decoupling capacitors. The off-chip current bias pins are ratioed to sink approximately $75\mu A$. On the circuit board these bias currents are provided with LM334 floating current sources.

More critical for optimal performance are the voltage supply and voltage references. While all voltage references are nominally decoupled at high frequencies, in practice there will be noise density between different voltage domains. The chip is referenced to a mid-rail reference, but many parasitic capacitances exist on the chip between signals and VDD or VSS. The noise power of between the power supplies and the voltage reference effectively adds to the equivalent voltage noise of the amplifier (v_n). Thus maintaining very low noise density for both the power supply and the voltage reference is critical, especially at moderate to high frequencies where the capacitive noise may dominate.

The 1.5 V power is regulated from 4 AAA batteries by an LT1763 voltage regulator, which has a noise density of approximately $35nV/\sqrt{Hz}$ above $1kHz$. This is additionally

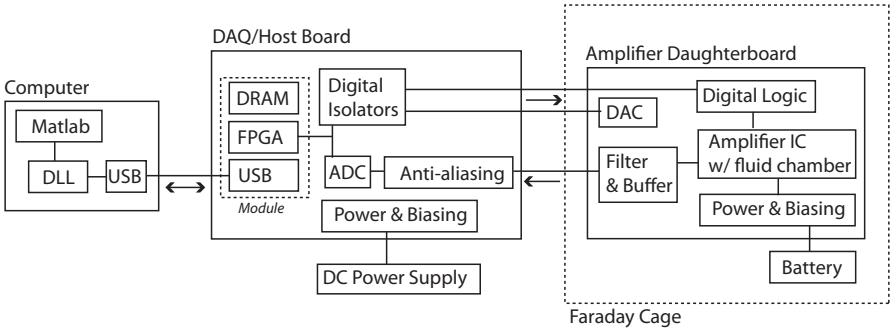

Figure 3.10: High-level diagram of the data acquisition components and interconnections.

filtered with a simple low-pass filter of $1\Omega//1000\mu F$, with a corner frequency of $160Hz$; with this filter, the power supply voltage noise is reduced below $1nV/\sqrt{Hz}$ for frequencies above 10 kHz. The 0.75 V virtual ground reference is simply generated from a resistive divider from the 1.5 V rail followed by an additional RC low-pass filter. 200Ω resistors are used in the divider, prioritizing voltage noise over power and offset considerations.

3.6.3 Closing the Feedback Loop

The amplifier chip was designed anticipating that the feedback loop would be closed off-chip. This is inefficient from a design area and I/O pin perspective, but it provides flexibility to tune the amplifiers for several different applications.

The differential outputs of the amplifier are buffered by non-inverting amplifier stages, which provides a constant and reasonably low capacitance load to the on-chip differential buffer. The buffered signals are then routed both to the DC feedback path and to the frequency correction filter.

For the DC feedback, the differential signal is converted back to a single-ended signal and referenced to the 0.75 V virtual ground. It is then converted to a current feedback signal by the the $k\Omega$ resistor R from Fig. 3.3, and attenuated by the on-chip current divider. The ultimate performance of the feedback loop does is not degraded by the off-chip signal path, as only the parasitics at the on-chip current divider output are relevant, and the DC feedback is only active up to a frequency of $f_c = \frac{1}{2\pi R_F C_F}$, which is approximately 10 kHz for typical

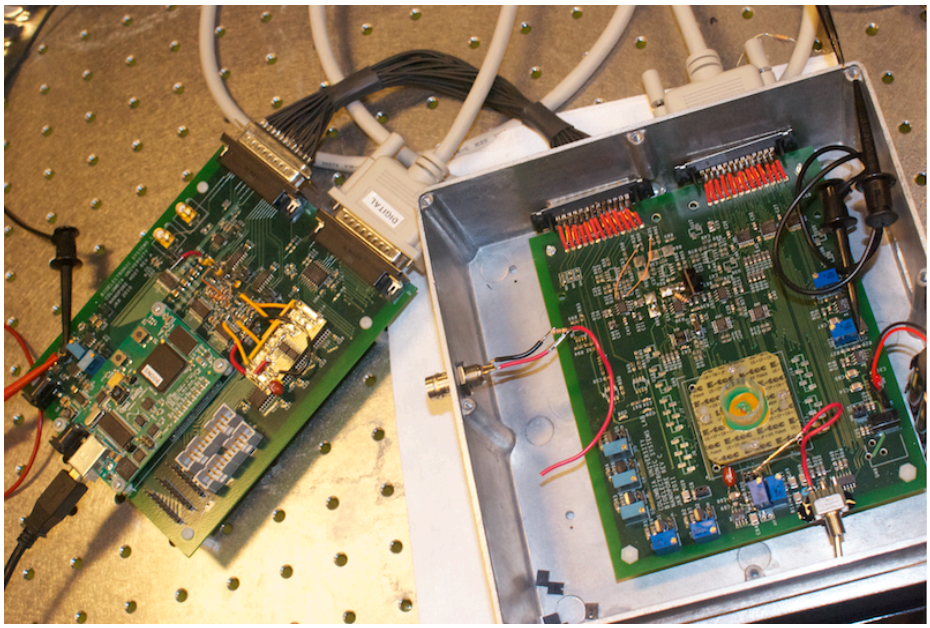

Figure 3.11: Photograph of host and amplifier daughterboard. The host board contains a USB interface, FPGA module, and data converters. The amplifier board is placed in an aluminum faraday cage and hosts all of the sensitive analog subsystems as well as the amplifier with attached fluid cell.

values used in the experiments discussed in Chapter 4.

3.6.4 Frequency Response Correction

As discussed previously (and illustrated in Fig. 2.9) the gain of the initial transimpedance stage is determined by $R_F//C_F$. In order to measure signals above this frequency, a board-level filter provides gain to result in an overall flat frequency response to a higher frequency.

This filter is realized with the fully-differential topology shown in Fig. 3.13. It is important that this filter be implemented with an amplifier with very low noise and high bandwidth, as it is applying high gain to weak signals at high frequencies. Ultimately the response of this filter will be limited by the gain-bandwidth product of its operational amplifer. For $f > f_c$, the required closed-loop gain will be approximately $G = G_{DC} \times \frac{f}{f_c}$. Thus to extend the bandwidth to a frequency f_1 requires an operational amplifier with $GBW = G_{DC} \times \frac{f_1^2}{f_c}$. Equivalently, for a given GBW a corrected frequency response can be maintained up to $f_c = G_{DC} \times \frac{f_1^2}{GBW}$. To extend the bandwidth from $f_c = 10kHz$ to

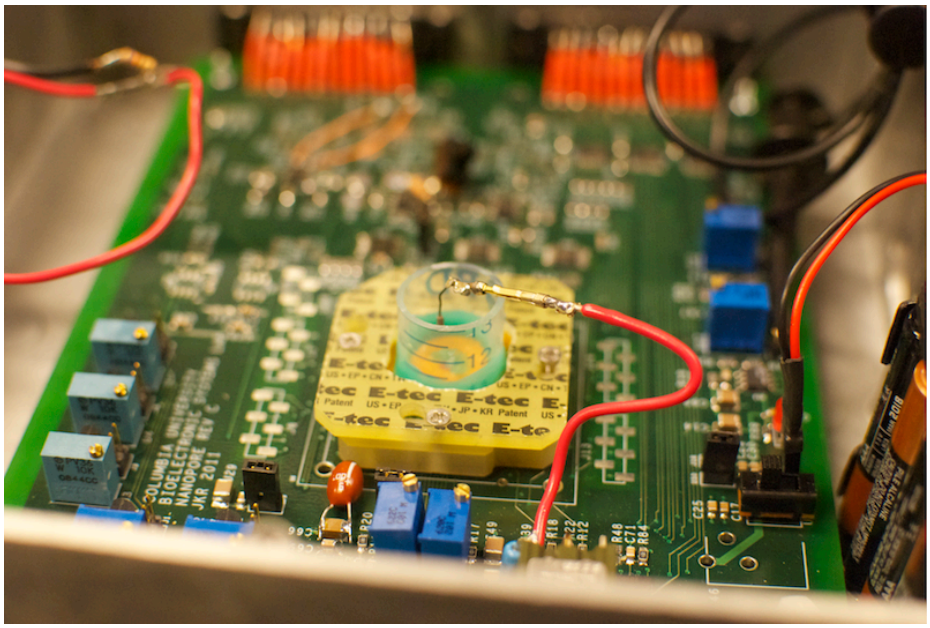

Figure 3.12: Photograph of the small open fluid chamber constructed on the surface of the amplifier die.

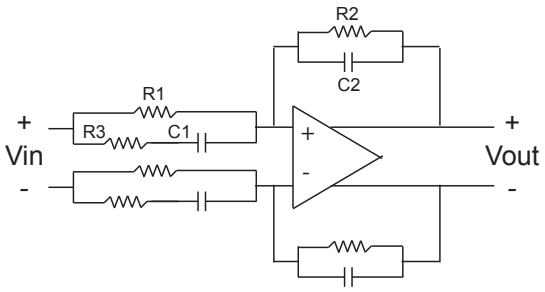

Figure 3.13: Differential Frequency Correction Filter

$f_1 = 1MHz$ with DC unity gain, then, requires a GBW of at least 100 MHz. This filter is implemented with an AD8139 fully differential amplifier, which has $GBW \approx 300MHz$ and $v_n = 2.25nV/\sqrt{Hz}$.

3.6.5 Anti-Aliasing and Sampling

In this design a 4th-order differential Bessel filter is implemented as an anti-aliasing filter. The corner frequency of the Bessel filter is nominally 1 MHz, preparing the signal to be sampled at rates between 2.5 MS/s and 4 MS/s.

Expressions for quantization noise were discussed in Chapter 2. In this prototype, with $V_{FS} = 5V$, $N = 12bits$, $f_s = 4MS/s$, and $Z_{gain} = 100M\Omega$, the input-referred quantization noise is $6.2 \times 10^{-30} \frac{A^2}{Hz}$ (or $2.5 \times 10^{-15} \frac{A}{\sqrt{Hz}}$), equivalent to the thermal current noise from a $2.5G\Omega$ resistor and two orders of magnitude lower than the anticipated input-referred noise of the CMOS preamplifier described here.

3.6.6 Digital Datapath

After the signal is acquired by the ADC, the digital data is transferred through an FPGA into a local hardware buffer. The hardware buffer is important to allow the data sample rate to be isolated from the latency and protocol overhead of the data transfer to a personal computer. The buffer and digital datapaths are implemented in an interface module (Opal Kelly XEM3010) which combines an FPGA (Xilinx Spartan-3) and memory (32MB SDRAM) with a high-speed USB 2.0 interface. Stored in 2-byte words at 4 MS/s, the 32MB SDRAM is able to create a local FIFO holding 4 seconds of data, protecting against data loss as a result of latency in the USB interface.

The data is acquired via a custom graphical user interface written in Matlab. The interface allows for a real-time preview of the acquired data, and storage of the acquired traces to the computer's hard disk. Separate software performs signal processing and analysis of the acquired data, at a later time.

3.6.7 Shielding & Isolation

As discussed earlier, in addition to reducing the fundamental wideband noise floor it is critical to to minimize interference from external sources coupling into the preamplifier signal path. As such, the hardware was designed to have maximum isolation between the analog preamplifier circuitry and all other systems.

The digital interface is designed with galvanically isolated buffers, so that the amplifier chip does not share power and ground paths with the FPGA or computer.

The preamplifier is located on its own circuit board, which is powered by 4 AAA

batteries. This preamplifier is located within its own small faraday cage. The fully differential preamplifier output, helps to mimimize external coupling. In addition the preamplifier is placed on a vibration-isolated air table, to reduce mechanical vibrations which can couple into the amplifier through the slight movements of wires and electrolytes within an experiment.

3.7 Measured Performance

The measured frequency response of the preamplifier is shown in Fig. 3.14. Prior to the frequency correction filter, the gain is constant at $106M\Omega$ from DC to approximately 11 kHz, after which it decreases at -20dB/decade. After the frequency correction, the gain is constant from DC - 1 MHz. Response above 1 MHz is attenuated by the anti-aliasing filter.

The measured open-circuit input-referred current noise density is shown in Fig. 3.17. The 1/f noise corner is below 1 kHz, and is due to the buffer and filter amplifiers following the transimpedance stage. A white noise floor of $10fA/\sqrt{Hz}$ is evident at moderate frequencies, corresponding to the shot noise from leakage current in the feedback transconductor. At high frequencies, the noise density increase appropriately with f^2 corresponding to voltage noise $v_n = 5.1nV/\sqrt{Hz}$ and a total capacitance of $1.2pF$. No f-proportional regime is evident in this trace, as the voltage noise 1/f corner is below the intercept of the constant and f^2 noise regimes.

The power consumption of the chip was measured to be 3 mA per channel from a 1.5 V supply.

Test current signals were injected into the amplifier by applying a triangle voltage wave across an 0.1pF capacitor. An example output is shown in Fig. 3.16, when a 5kHz $35pA_{p-p}$ was injected. At the full 1MHz bandwidth, the SNR is low, but that does not mean the signal is not present; digitally low-pass filtered to 100kHz, the levels are much clearer at the expense of coarser temporal resolution.

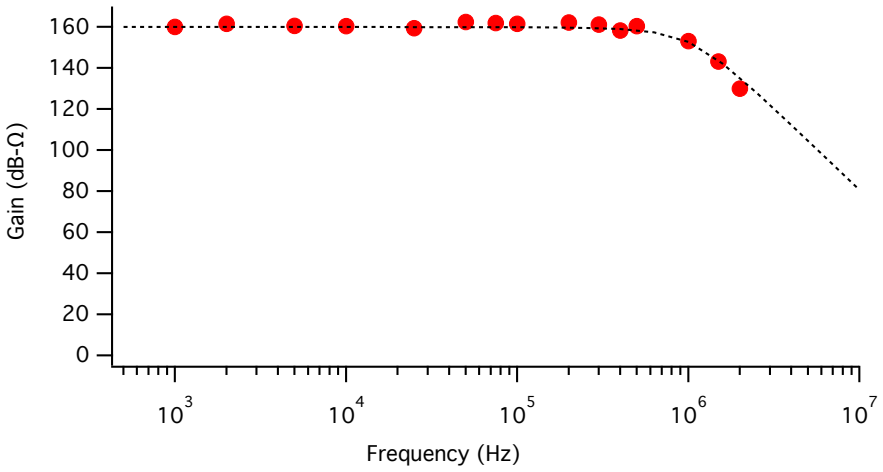

Figure 3.14: Measured transimpedance gain of the amplifier. The dotted line shows the expected response of a constant-gain 100MΩ amplifier followed by a 4th order Bessel lowpass filter at f_c=1MHz.

3.7.1 Comparison to Alternative amplifiers

The measured baseline noise spectrum of the custom integrated amplifier compared favorably with a similar open-headstage configuration of an Axopatch 200B (Fig. 3.15-3.18). At measurement bandwidths below 10 kHz, the noise of the Axopatch was lower than that of the new amplifier, owing to the $10fA/\sqrt{Hz}$ white-noise density of the CNPs on-chip current source as compared to $5.7fA^2/\sqrt{Hz}$ from a discrete $500M\Omega$ feedback resistor in the Axopatch. However, for $B > 10kHz$, the new system delivered much lower noise. For the highest bandwidth supported by the Axopatch ($100kHz$), the CMOS amplifier had a noise floor of $3.2pA_{rms}$, compared to $9pA_{rms}$ for the Axopatch. At the highest bandwidth characterized for the integrated amplifier ($1MHz$), the noise level was $24pA_{rms}$, in contrast with $247pA_{rms}$ modeled by extrapolating the Axopatch response beyond its supported range.

Several other examples of integrated transimpedance amplifiers for nanopore or ion channel measurements exist [47–50, 55, 56]. However, thus far other demonstrated systems have emphasized low power and small area in their designs, and the result is generally worse noise performance than popular discrete patch-clamp systems. The exception to this trend is [48], which demonstrated impressive noise density but used a non-traditional control loop

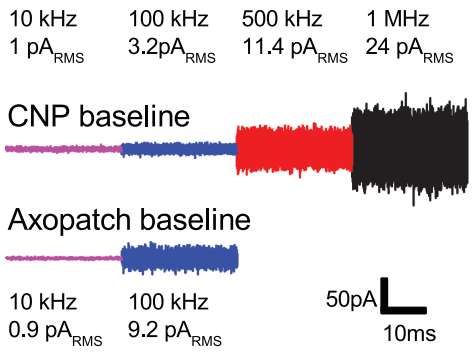

Figure 3.15: Baseline noise traces, with nothing attached to the amplifier input. Comparable traces from an Axopatch 200B patch clamp amplifier are included for the bandwidths that it supports.

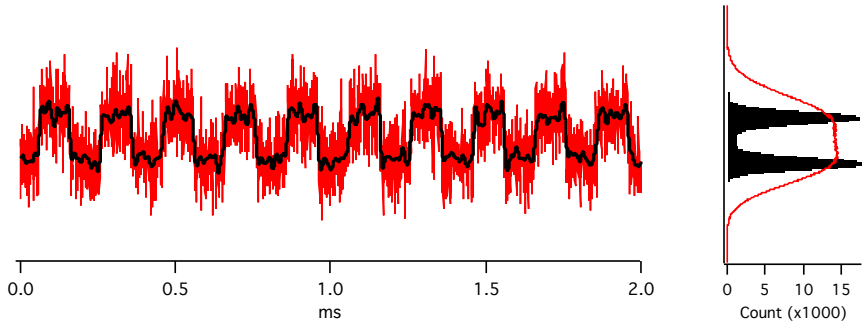

Figure 3.16: Measured signal output for a $35pA_{p-p}$ 5kHz square wave injected into the input of the amplifier by applying a triangle voltage waveform across an 0.1pF capacitor. The red trace represents the full 1MHz signal bandwidth, while the black trace has been digitally filtered to B=100kHz. The inset shows histograms of 2 seconds of each trace.

topology that suffers from low dynamic range at moderate frequencies.

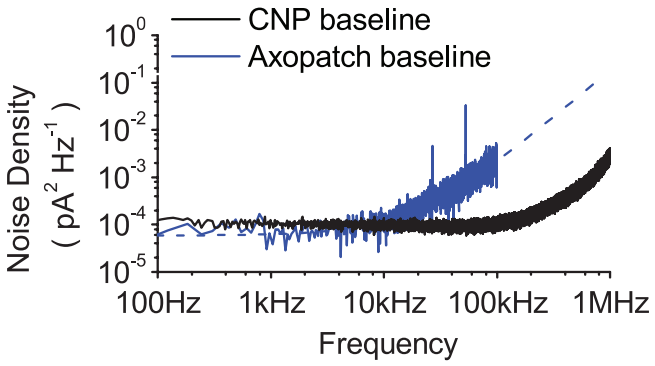

Figure 3.17: Input-referred noise PSD of the amplifier, with nothing attached to its input.

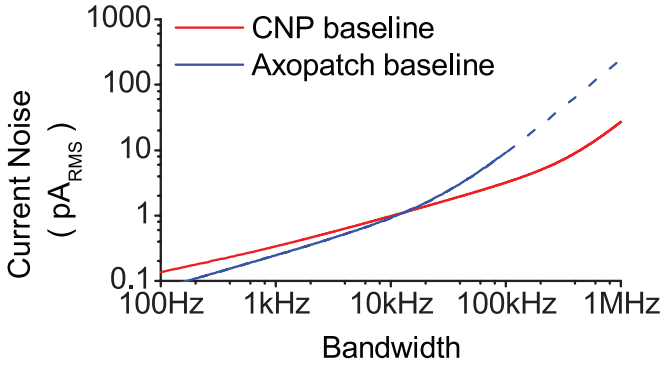

Figure 3.18: Input-referred noise RMS, with nothing attached to its input.

Chapter 4

Integration of Solid-State Nanopores with CMOS Preamplifiers

4.1 Introduction

One main advantage of solid-state nanopores, in contrast with transmembrane proteins, is the potential for co-integration of sensors with active electronic elements. Solid-state nanopores are frequently demonstrated in materials common to the semiconductor industry, and visions of massively parallel solid-state pores tailored with active electrodes, addressable arrays, and local readout electronics are common. Yet in the decade since their introduction, no examples of this type of integration have been published. This chapter discusses methods of combining the integrated CMOS amplifier from Chapter 3 with solid-state nanopores. By reducing parasitic capacitances in the measurement, the temporal resolution of solid-state nanopore recordings can be improved by at least an order of magnitude, and by taking advantage of the overlap in materials and construction between integrated circuits and solid-state nanopores, nanopore sensors can be monolithically integrated into active electronic substrates.

4.2 Chapter Summary

This chapter introduces a low-noise measurement platform which integrates a complementary metal-oxide semiconductor (CMOS) preamplifier with solid-state nanopores in thin silicon nitride membranes. First, an arrangement is discussed which exposes the amplifier directly to the electrolyte. With this platform we achieved a signal-to-noise ratio exceeding five at a bandwidth of 1 MHz, which to our knowledge is the highest bandwidth nanopore recording to date. We demonstrate transient signals as brief as 1 s from short DNA molecules, which enabled us to observe multiple distinct configurations of a short DNA molecule during its passage through a solid-state nanopore. Finally, a demonstration is made of one method to drill nanopores directly through a CMOS amplifier die, which is an important early step towards the massively-parallel, electronically-active solid-state nanopore sensor platforms of popular imagination.

4.3 Low-Capacitance Measurement Platform

An important limitation to practical nanopore measurements is the connection between the ionic environment and the electronic measurement system. The physical size of the nanopore support chip, fluid chamber, electrodes, and electronic amplifier are each much larger than the sensor itself, and determine both the size of the overall system and the magnitudes of parasitic elements which interfere with the measurement.

To address these limitations, we constructed a compact measurement platform built around the integrated CMOS amplifier introduced in Chapter 3. Rather than connecting a wire between an amplifier circuit board and an Ag/AgCl electrode, we fabricated a silver microelectrode on the surface of the CMOS amplifier itself. We then constructed a fluid chamber directly over the surface of the amplifier, into which we placed a solid-state nanopore chip. A second Ag/AgCl electrode was placed in the opposing chamber above the nanopore. An illustration of this system is shown in Fig. 4.1. This design considerably reduced parasitic capacitance at the amplifier input, resulting in lower high-frequency noise

than traditional platforms which rely on external patch clamp amplifiers.

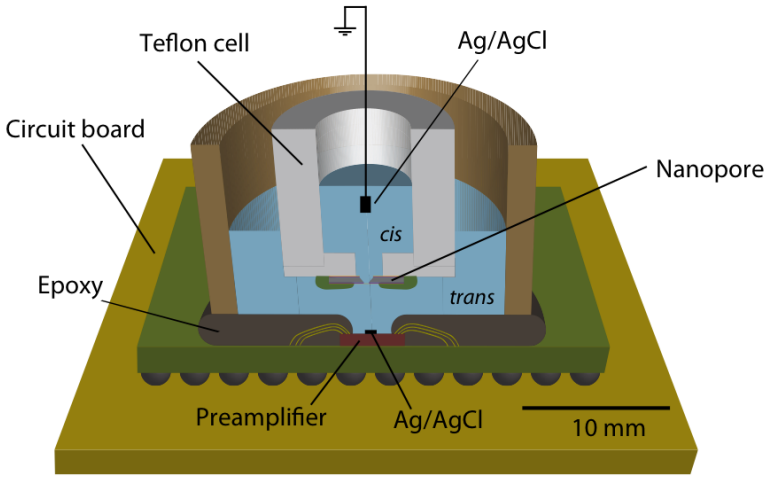

Figure 4.1: Solid-state nanopore measurement cell.

4.3.1 Amplifier Packaging & Fluid Chamber

The amplifier was packaged in an arrangement which prioritized access to the microelectrodes on the surface of the die. The 140 pins on die were wirebonded to a 272-pin ball-grid array (BGA) package. Dam-and-fill doughnut epoxy encapsulation (Hysol FP4451 dam and FP4650 fill) covered the exposed gold wirebonds, leaving the die surface exposed.

A watertight fluid chamber was constructed by fastening a 1 cm segment from a polypropylene tube to the top of the BGA package using polydimethylsiloxane (PDMS, Sylgard 184, Dow Corning). The volume of this fluid chamber was approximately 1 mL, though experiments were commonly performed with $500\mu L$ of electrolyte or less. Fluid was exchanged in and out of the chamber with simple pipettes.

The preamplifier with its attached fluid chamber was mounted in a compression-mount BGA socket (Emulation Technologies) on its supporting circuit board (discussed in Chapter 3), which was placed in a small aluminum faraday cage.

4.3.2 Ag/AgCl Microelectrodes

After packaging the die and constructing the fluid chamber, the aluminum top metal was chemically etched from the exposed electrodes by pipetting $500\mu L$ of acidic aluminum etchant (Type A, Transene) into the fluid chamber for several minutes, followed by multiple rinses with deionized water. This procedure removes the aluminum, exposing the underlying titanium nitride adhesion and diffusion barrier layer.

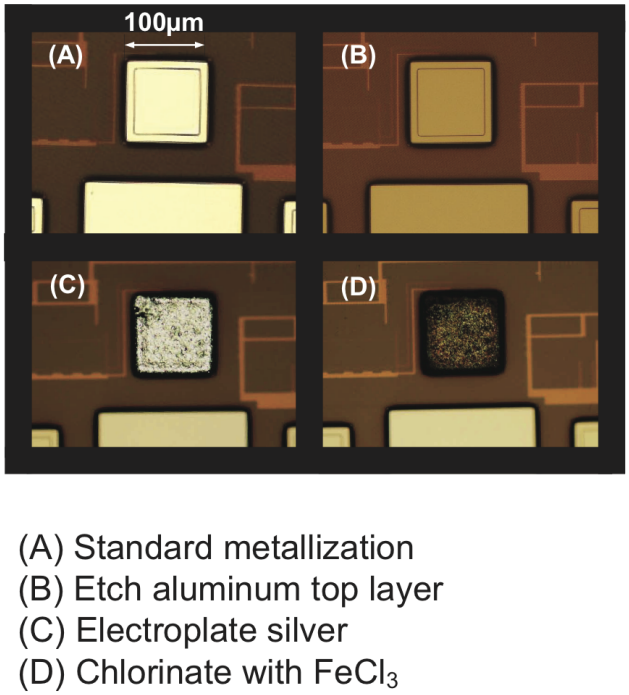

Figure 4.2: Aluminum pads are replaced with electroplated silver and chlorinated to form Ag/AgCl microelectrodes.

After removing the aluminum, a thick layer silver was electrochemically deposited. The chip was mounted in its circuit board, powered on, and digital logic was applied to short-circuit the amplifier feedback element C_F, clamping multiple channels electrodes at a constant voltage and providing a path for them to sink several microamperes of current. A small volume (less than 1 mL) of silver electroplating solution containing potassium silver cyanide (Transene), was added to the fluid chamber, and a silver wire counterelectrode was attached to a Keithley 2400 I-V meter and placed in the solution. The voltage was

adjusted to achieve a counterelectrode current of $1\mu A$ for several minutes, resulting in a deposition of approximately $10\mu m$ of silver onto each electrode. After electroplating, the chamber was rinsed multiple times with deionized water. No seed layer was applied, and the electroplating occurred directly onto the the TiN diffusion barrier beneath the original aluminum. Due to the absence of a seed layer, constant-voltage electroplating was found to provide better uniformity than constant-current; however the electrodes remained quite rough. In this application this did not cause any problems, and at the margin it likely improved performance by increasing the surface area of the electrode.

The silver microelectrodes were converted to Ag/AgCl pseudo-reference electrodes by applying a drop of $10\mu L$ 50 mM $FeCl_3$ to the surface for 30 seconds [57], creating a thin coating of silver chloride on the surface of the electroplated silver. After several hours of experiments, or several buffer exchanges, the chlorination typically needed to be repeated. (Based on the size of the electrodes and current levels involved, the expectation is that the AgCl was depleted largely by dissolution into the buffer, rather than by electrolysis.) We found that the chlorination could be repeated multiple times before the silver electrode was exhausted. Images of an electrode at several steps during this process are shown in Fig. 4.2.

4.3.3 Die Surface Passivation

Integrated circuits are often passivated with fairly thick dielectric layers, which protect the chip metallization from corrosion. In addition, an organic polymer such as polyimide is used to relieve mechanical stress induced from chip packaging. In the CMOS process utilized here, these layers together form approximately $6\mu m$ of insulation above the top metal interconnect layer. If an ionic buffer is applied to the surface of the chip, this forms an approximate parallel-plate capacitance between the chip wiring and the fluid. The metal wiring is not fully dense, but this capacitance is not negligible; an upper bound estimate is $C = \epsilon 0 \times \epsilon r \times (2mm)^2/6\mu m = 24pF$.

To reduce this capacitance, additional passivation was added to the chip surface.

After doughnut encapsulation, the epoxy-based photoresist SU-8 was patterned over the majority of the surface, excluding the electrode areas. Under yellow light, a drop of SU-8 2015 (Microchem) was manually applied to the surface of the amplifier die, filling the $300\mu m$-deep cavity formed by the epoxy dam. A light vacuum was applied in a dessicator for 15 minutes, followed by an overnight softbake in an oven at 80°C. The chip was exposed in an MJB-3 UV contact aligner using a chrome-on-glass mask, $2,000mW/cm^2$ dose, and 360 nm long-pass UV filter (Omega Optical). A post-exposure-bake for 30 minutes at 50°C and development in SU-8 Developer (Microchem) yielded a layer of SU-8 between $200300\mu m$ thick with $300\mu m \times 300\mu m$ square openings surrounding the $100\mu m \times 100\mu m$ electrodes.

The small $300\mu m$ opening around the input electrode corresponds a capacitance no greater than 0.5 pF; the thicker passivation of the remainder of the chip contributes a similar amount. Thus the parasitic capacitance from the ionic liquid to the surface of the CMOS chip is reduced to less than 1 pF.

Additionally, for the experiments described here, KWIK-CAST silicone was manually applied to cover the unused channels of the amplifier, leaving only one preamplifier electrode exposed to the electrolyte.

4.3.4 Nanopore Fabrication

In order to demonstrate the advantages of improved nanopore instrumentation, it is important to select pores which have high conductance and low parasitic capacitance. Nanopores in ultrathin silicon nitride membranes were fabricated in a similar manner as described elsewhere [12]. Briefly, a $500\mu m$-thick silicon wafer with $< 100 >$ crystal orientation and $5\mu m$ of thermal oxide was coated with 25 nm of low-stress chemical vapor deposition silicon nitride (SiN). Standard UV photolithography was used to pattern square openings on one side of the wafer, through which the nitride and oxide were etched using SF_6 plasma. The photoresist was stripped, and an anisotropic KOH etch followed by removal of the oxide layer in buffered hydrofluoric acid resulted in approximately $50\mu m \times 50\mu m$ free-standing windows on the reverse side of the wafer.

A film of poly-(methyl methacrylate) (PMMA, Microchem) was spun onto the membrane side of the window, and electron-beam lithography was used to pattern a small square opening of $500nm \times 500nm$ or smaller. A SF_6 plasma etch locally thinned the SiN in this region to $10 - 15nm$. The confined area of this ultrathin region helped to limit the capacitance of the membrane and maintain its mechanical integrity. The PMMA was removed by incubation in acetone. A single nanopore was drilled through the thinned region of the nitride membrane using a JEOL 2010F HR-TEM. Fabricated pores were $2 - 6nm$ in diameter.

4.3.5 Mounting the Nanopore Cell

The nanopore chip was cleaned in piranha acid using a procedure described previously [58]. After rinsing and drying the membrane, it was immediately mounted onto a custom Teflon fluid cell using KWIK-CAST silicone elastomer (World Precision Instruments). The elastomer served to seal the edges of the chip, and additionally helped to reduce parasitic capacitance by limiting the area of the silicon chip exposed to the electrolyte. The silicone was carefully painted over the majority of the membrane-facing side of the chip, leaving an exposed area of less than $1mm^2$ area around the membrane, shown in Fig. 4.3.

The resulting membrane capacitance can be modeled by $C_M = \Sigma_i(\epsilon_0 \times \epsilon_r \times A_i/d_i)$, where ϵ_0 is the permittivity of free space, ϵ_r is the relative permittivity of the dominant dielectric, A_i is the area of fluid contact, and d_i is the thickness of the dielectric. An estimate of the elements of C_M for the lowest-capacitance devices considered here is the following:

Table 4.1: Membrane Capacitance Estimates

Description	Area	Thickness	ϵ_r	C_M
Ultra-thin SiN	$(500nm)^2$	10 nm	7	0.002 pF
SiN membrane	$(40\mu m)^2$	25 nm	7	4 pF
SiN-SiO2 exposed to trans chamber	$\pi/4 \times (450\mu m)^2$	5 μm	4	1.1 pF
Silicone-SiN-SiO2	$(5mm)^2$	1 mm	4	0.9 pF
Total				6 pF

It is worth observing that the total C_M here is nearly 2 orders of magnitude lower

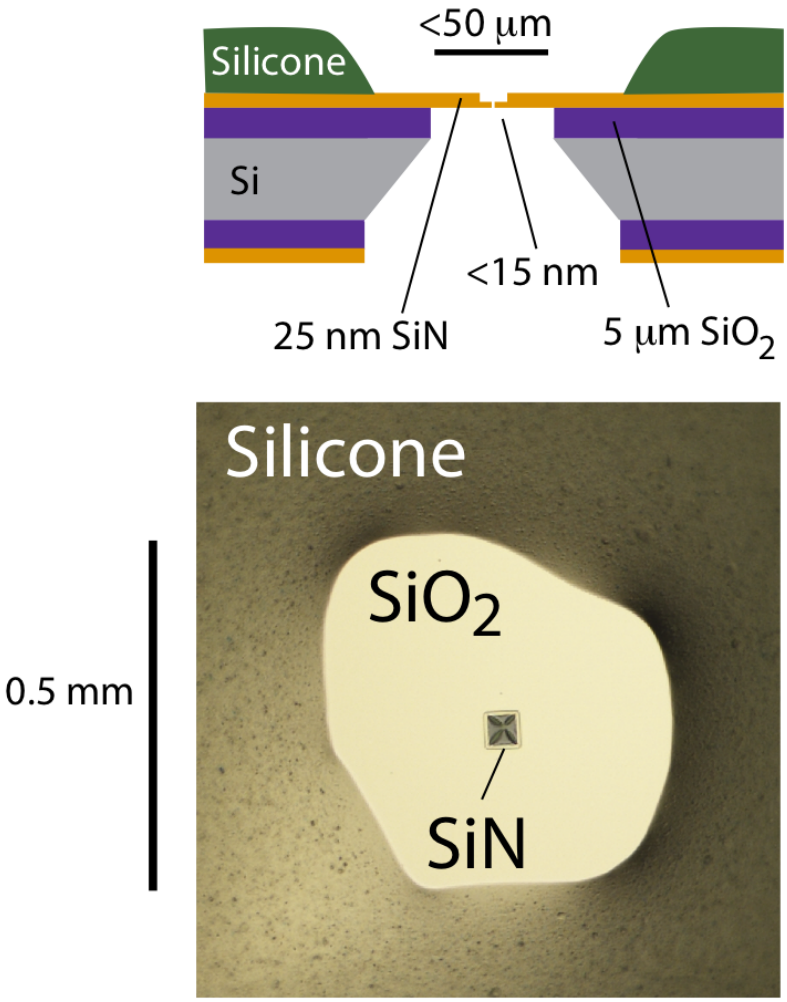

Figure 4.3: Solid-state nanopore support chip, and illustrated cross-section.

than early solid-state nanopores, which had $C_M > 300pF$ [59]. Yet even this lower capacitance is not a fundamental limit, and these capacitive elements are entirely independent of the properties of the nanopore itself. By making passivation layers thicker and and exposed areas smaller, there remains an opportunity to reduce C_M by an additional order of magnitude or more, into the realm of 0.5pF or less. These optimizations would yield immediate SNR improvements at high bandwidth.

4.3.6 Voltage Bias Topology

Often, voltage-clamp current measurements are arranged such that one side of the device under test is grounded, and the applied voltage is determined by varying the voltage clamp of the transimpedance amplifier. However, given that the CNP utilizes a single-supply amplifier, the TIA is already clamped to a mid-rail virtual ground potential. For convenience, rather than vary the TIA clamp potential, the voltage was adjusted on the opposite electrode of the nanopore cell. The bias voltages are generally set at constant potentials, and with both the virtual ground and the nanopore bias appropriately decoupled to ground, this change in bias topology has no appreciable impact on the noise and bandwidth of the system.

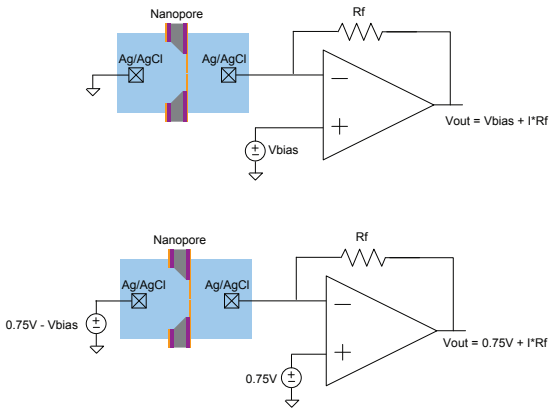

Figure 4.4: Single-supply voltage bias arrangement.

4.3.7 Total Capacitance

As discussed in Chapter 2 The relevant metric for input capacitance is a sum of several elements, some of which are characteristic of the electronics and some of which are characteristic of the nanopore support chip. To assist with comparisons of the presented arrangement with more conventional measurement setups, an estimated breakdown of these contributions is shown in Table 4.2

In prior work, reductions in C_M have led to significant improvements, but in re-

Table 4.2: Total Capacitance Estimates

	C_I	C_F	C_W	C_M	Total
Axopatch 200B (early SiN pores)	15pF	1pF	4pF	300pF	320pF
Axopatch 200B (improved SiN pores)	15pF	1pF	4pF	10pF	30pF
This work	1pF	0.15pF	0.25pF	6pF	7.4pF

cent publications the decreasing membrane capacitance has caused the amplifier input to represent an increasing fraction of the total capacitance.

4.4 Measured Open Pore Noise

With the measurement cell assembled as described and a nanopore connected, the noise inevitably rises above the baseline amplifier noise floor. The nanopore contributes flicker and thermal noise, while the fluid cell and nanopore support chip add capacitance. Since the nanopore membrane sizes vary, and the elastomer mounting was done by hand, there was considerable variation in the observed capacitance. With the lowest-capacitance devices ($C_M = 6pF$ as above), we measured noise of 12.9 pA_{RMS} and 155 pA_{RMS} for bandwidths of 100 kHz and 1 MHz, respectively. Representative time-domain traces are shown in Fig. 4.5, compared to the equivalent bandwidth signal recorded on an Axopatch 200B patch clamp amplifier in resistive-feedback mode with a similar nanopore attached. For B = 100 kHz, there was more than a factor-of-two reduction in input-referred noise power for the CNP as compared to the Axopatch ($I^2_{CNP}/I^2_{axopatch}$). If the Axopatch could be measured at higher bandwidths, there would have been a factor-of-six noise power difference at B = 1 MHz.

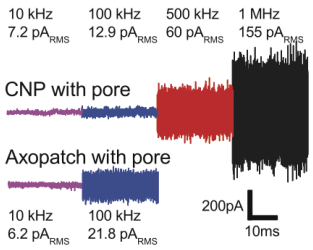

Figure 4.5: Traces with pore attached.

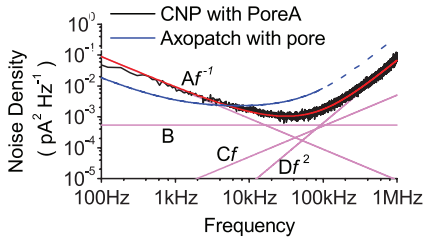

Figure 4.6: Power spectral density with nanopore.

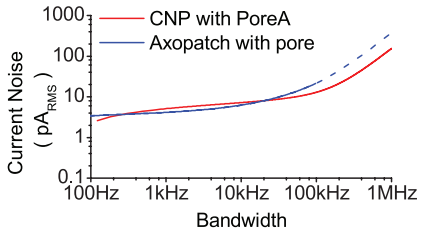

Figure 4.7: Root-mean-squared noise with nanopore.

Aside from the overall lower noise at high frequencies, we observed that polynomial fits to the noise power spectrum (Fig. 4.6) did not contain a substantial linear component at moderate frequencies ($> 1kHz$), which dominated the high-frequency noise in earlier reports [30, 31]. This is likely attributable to the high-quality dielectric properties of the thermal SiO_2 passivation of the nanopore support chip.

4.4.1 SNR and Maximum Signal Bandwidth

To determine the bandwidths that can be supported, we calculated the SNR for each pore as a function of signal bandwidth (Fig. 4.8 - 4.9). For pore A, SNR was maintained above 10 beyond 600 kHz bandwidth and above 5 beyond 1 MHz. For pore B, SNR values of 10 and 5 were maintained up to 160 kHz and 320 kHz, respectively.

The minimum tolerable SNR will vary, but to avoid substantial false event detection rates it can be reasonable to require a signal level several times larger than the RMS noise level, as discussed in Chapter 2. For the purpose of considering the maximum noise-limited bandwidth, we assumed a minimum SNR of 5 would be required. With this assumption,

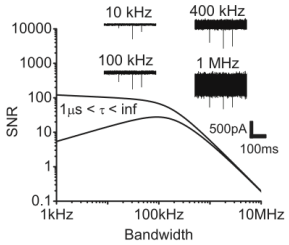

Figure 4.8: SNR for Pore A

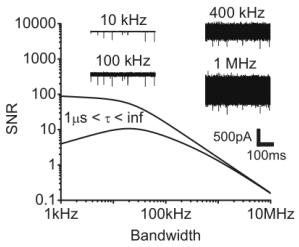

Figure 4.9: SNR for Pore B

in the limit of very small C_M, the baseline amplifier noise floor corresponded to usable measurement bandwidth of several megahertz (Fig. 4.10).

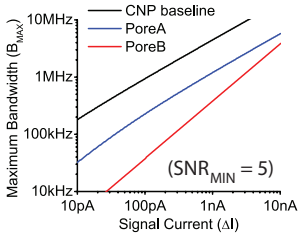

Figure 4.10: Supported signal bandwidth as a function of signal amplitude

4.5 Nanopore Trace Analysis

The data were processed using custom Matlab software. Traces were generally digitally filtered with a 128- or 512-tap finite-impulse-response low-pass filter to a desired signal bandwidth, while retaining the $2-4$ MS/s sample rate. Events were typically identified with a two-state thresholding algorithm in Matlab, but for traces with low SNR, a modified

algorithm was used to identify the events: First, samples were identified whose value is more than 5 standard deviations below the mean open pore current. Next, a local search found the nearest sample points at which the signal was above the open pore current. Finally, event edge times were assigned at the first and last points in these bounds that the signal was more than 4 standard deviations from the baseline current.

By using a detection threshold 5 standard deviations from the mean, we would expect to see a spurious event rate of approximately $\lambda_F = 3 \times 10^{-6} \times B$, according to the analysis in Chapter 2. For a bandwidth of 1 MHz, this corresponds to acceptable event detection as long as events occur more often than a few times per second. Determining the event start and end points with a lower threshold than their initial identification has no impact on the false event rate.

4.6 Demonstrating Very Brief DNA Blockades

As an example of the short timescales observable with the CNP, we considered a current trace measured for pore B with 25 base pair double-stranded DNA (Fig. 4.11). The pore was biased at 600 mV, digitized at 2.5 MS/s, and then digitally filtered to both 500 kHz and 100 kHz bandwidths. The 500 kHz trace represents the maximum bandwidth for which $SNR > 5$ in these conditions ($\Delta I = 1.3nA$, n = 1,307 events). The data was also filtered to B=100 kHz as a comparison to the supported bandwidth of other platforms. In a 500-ms period, 29 individual molecules translocated through the pore, each producing a pulse ranging in duration from 1.2 μs to 30.2 μs. Digital samples were separated by intervals of 0.4 μs, but the signal rise and fall times were 1 μs and 5 μs for the 500 kHz trace and 100 kHz trace, respectively. Accordingly, events shorter than 10 μs were clearly visible in the 500 kHz trace, but their amplitude was attenuated at 100 kHz. Similarly sized oligomers have been previously measured with solid-state nanopores [60, 61], but observed pulse durations regularly saturate at the $10 - 100$ μs temporal resolution of the measurements. In some prior instances, experiments have been performed at $0°C$, increasing the viscosity of the electrolyte and slowing the kinetics of surface interactions. In contrast, we collected the

data presented here at room temperature $(20 - 23°C)$.

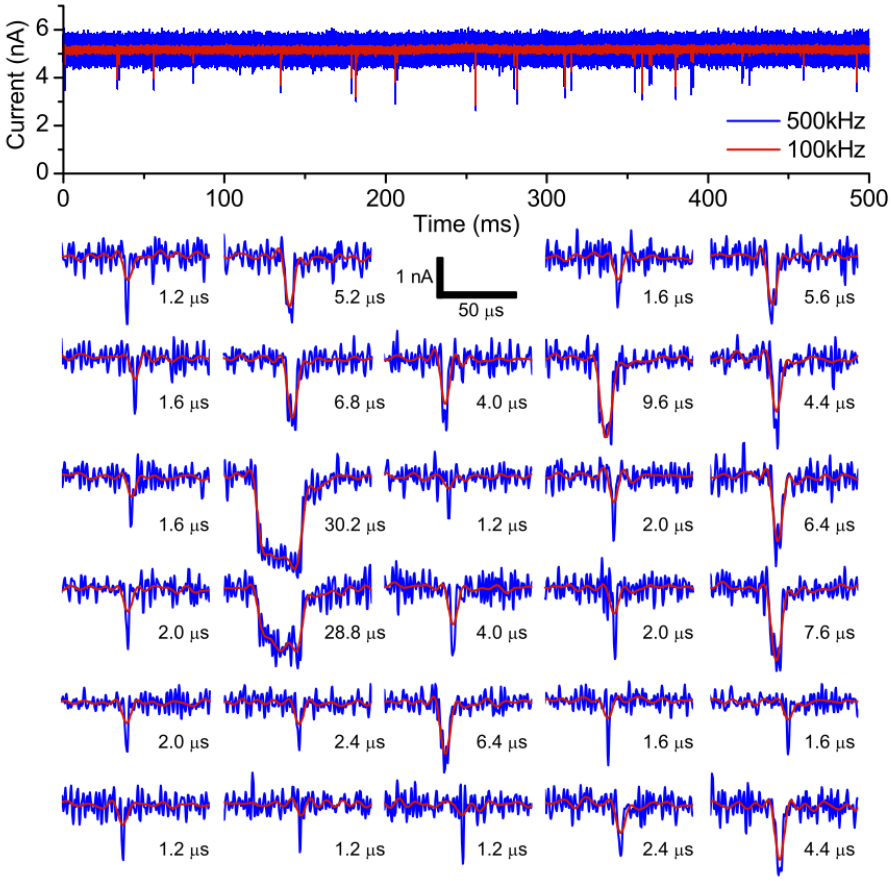

Figure 4.11: Measurement of very fast signals, with 25bp at 600mV

4.7 Short DNA Translocation Statistics

The fine temporal resolution of the new measurement platform allowed us to consider the statistics of shorter duration events than have been previously characterized. At 3.5 nm diameter, pore B was small enough that oligomer translocation times were dominated by surface interactions rather than electrophoretic forces [62, 63], producing a wide range of event durations. We analyzed a dataset with 50bp dsDNA and pore B at several bias voltages and signal bandwidths, as a demonstration of the impact of measurement bandwidth on the observed features of nanopore events.

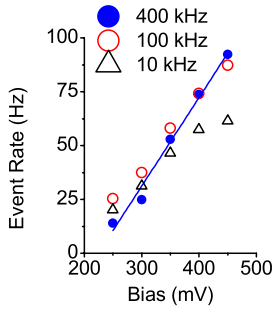

Figure 4.12: Observed event rate as a function of bias voltage, for 50bp dsDNA.

We observed a linear event rate trend with bias voltage that indicated a diffusion-limited capture regime above an energy barrier [64] of 200 mV (Fig. 4.12). Although the observed event rates were similar at 400 kHz and 100 kHz bandwidths, the apparent durations and depths of brief events were quite different. Events as short as 2 μs were clearly distinguished at 400 kHz, whereas at 100 kHz events faster than 10 μs were strongly attenuated and distorted [65]. This had a marked effect on the observed statistics of the events, exaggerating the duration of short events in the 100 kHz dataset (Fig. 4.13). Above 400 mV, we continued to observe events below the nominal 2.5 μs response of the 400 kHz filter (Fig. 4.14), implying that some of the observed pulses were likely sub-microsecond events that could be better resolved if the membrane capacitance (and in turn $I_{RMS}(B)$) were further decreased.

4.8 Identifying Intra-event Features

Although it is simplest to characterize nanopore current blockades as elementary pulses, it is generally acknowledged that, absent noise and bandwidth limitations, the current would be observed to vary within individual blockades owing to changes in the local structure and position of the captured molecule. Previous experiments have distinguished multiple current levels that correspond to folded polymers [66], duplex dissociation [67], distinct regions in a single polymer [68] or conformations of adjacent protein complexes [69]. Similarly, for small-diameter nanopores, both molecular-dynamics simulations [63] and experiments [62]

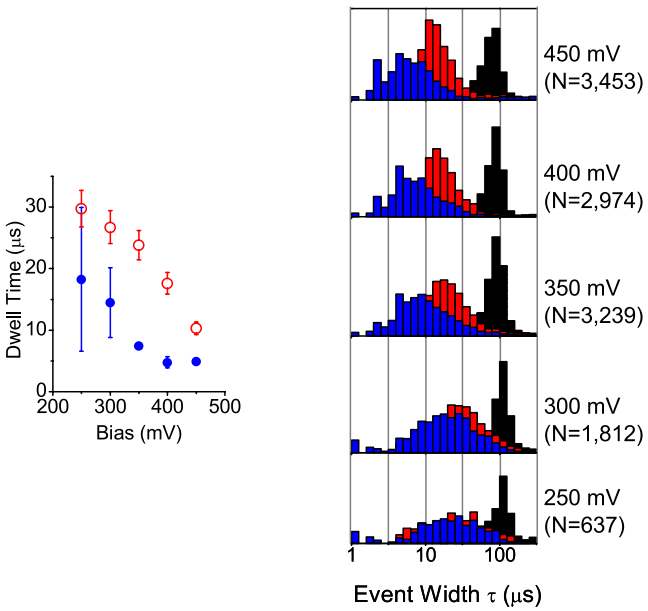

Figure 4.13: Observed event durations as a function of bias voltage.

have observed that even brief translocation events consist of several sequential processes. We extended the dataset from pore B with 50 bp dsDNA to 500 mV bias. At this high voltage, we commonly observed translocations with an initial shallow blockage followed by a deeper tail immediately before completion (Fig. 4.15).

A reasonable explanation for this intra-event structure is a multistate process (Fig. 4.16). First, a diffusing molecule is captured by the nanopore in a sideways orientation, which does not permit translocation, leading to shallow blockade. Then, after the molecule reorients lengthwise, it fully enters the pore and causes a deeper blockade. We observed this event structure more frequently at higher voltage bias, which is consistent with the model of an inflexible molecule becoming trapped near the pore opening by high electric fields and frictional forces (duplex DNA has a persistence length of 50 nm, and thus a 15-nm-long 50 bp molecule can be approximated as a rigid rod).

In this dataset, due to the short length of the DNA fragments the deeper tail was often faster than 10 μs, and it was commonly obscured in low-bandwidth measurements. We analyzed the event tails by computing the mean current of the final 2 μs of each event, and

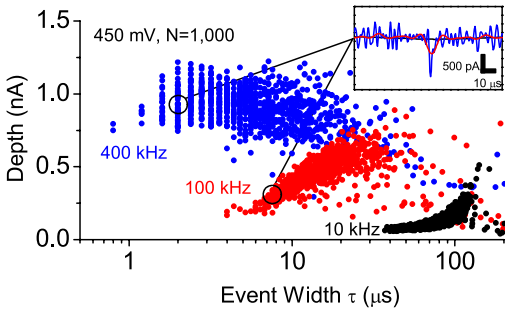

Figure 4.14: A scatter plot of event duration and amplitude, for 50bp dsDNA at 450mV bias.

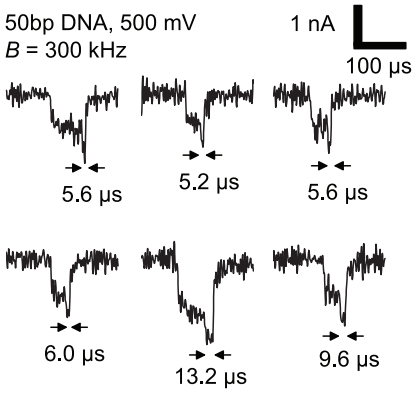

Figure 4.15: Typical traces observed with 50bp dsDNA at 500mV bias.

we concluded that the depth of the tail was distinct from the depth of the event as a whole (Fig. 4.17). The depth of the last 2 μs exhibited a linear relationship with bias voltage, whereas the remainder of the event did not (Fig. 4.18). This supports the hypothesis that the deeper tail signaled the passage of the molecule through the pore, and that in strong electric fields it became increasingly likely that a molecule would be trapped at the mouth of the pore before translocating through it.

4.9 Monolithic Solid-State Nanopores Through a CMOS Die

During the design of the integrated CMOS amplifier circuit (Chapter 3), several areas were reserved for post-fabrication of solid-state nanopores drilled directly through the die itself [53]. After receiving the completed chips, nanopores would be drilled through a thin

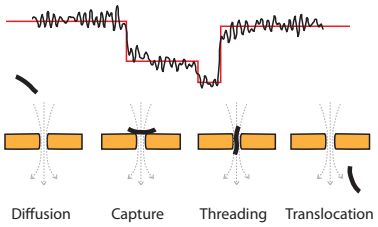

Figure 4.16: An illustration of the hypothesized DNA capture process of small molecules by a solid-state nanopore. At high bias voltages, a molecule may spend longer trapped at the mouth of the pore before successfully translocating, leading to a multi-state blockade event.

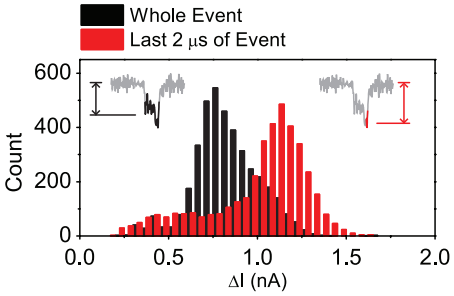

Figure 4.17: Histograms of the blockade depth of whole events, as compared to the depth of their final 2μs, with 50bp dsDNA at 500mV bias.

dielectric membrane formed from one of the existing passivation layers in the CMOS process.

In these reserved areas all metals have been blocked, leaving an 8 μm stack of dielectrics from the chips interconnect layers. This stack consists largely of alternating layers of borosilicate glass fill and silicon nitride capping layers. The post-fabrication procedure consists of steps to etch away most of the dielectric stack from the top side as well as remove the silicon substrate from the back side, isolating one Si_3N_4 layer as a thin suspended membrane. A cross-section of the final micromachined structure is illustrated in Fig. 4.19.

To begin the membrane fabrication process, a layer of chromium is thermally evaporated onto the top of the chip. Local openings are patterned in the chromium with UV photolithography, and in these areas the majority of the dielectric stack is etched using an inductively-coupled $CHF_3 + O_2$ plasma.

A film of PECVD Si_3N_4 is deposited onto the back side of the die, and square

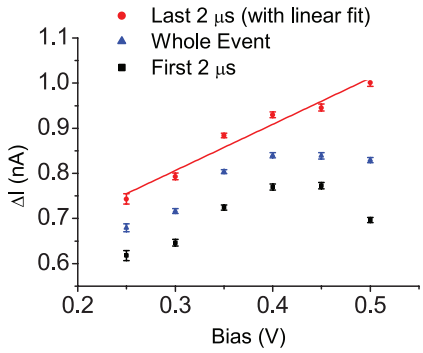

Figure 4.18: Median event depths of whole blockage events, along with the depth of their first and last 2μs, as a function of bias voltage. Only the final 2μs are a linear function of bias voltage.

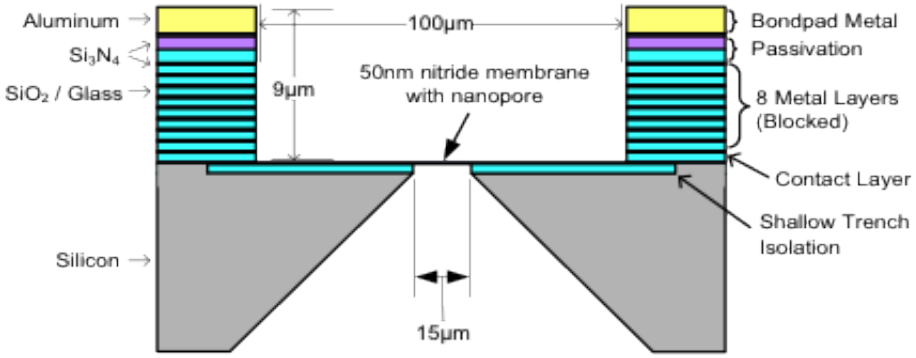

Figure 4.19: An illistrated cross-section of solid-state nanopores drilled directly through silicon nitride membranes embedded in CMOS amplifier chips.

openings are patterned in the nitride, aligned with the desired window areas on the top side of the chip. The die is mounted in a custom PDMS single-sided etching cell, and the silicon substrate is etched using a heated KOH solution. The chip is manufactured on a wafer aligned to the $< 100 >$ crystal plane, and the KOH etch results in an inverted pyramid cavity whose sidewalls are $< 111 >$ planes. The etch terminates when it reaches the dielectrics on the top side of the chip.

The removal of the silicon substrate results in a small $(15 \times 15\mu m)$ suspended dielectric membrane consisting of the bottom few layers of the interconnect passivation, which have already been thinned by the previous top-side plasma etch. The exposed window is now a three-level stack of $SiO_2 - Si_3N_4 - SiO_2$. A short dip in buffered hydrofluoric acid

is used to remove the SiO2 from both sides and release a single 50nm Si_3N_4 layer as a suspended membrane. Figure 4.20 shows images of a die at several points in this process.

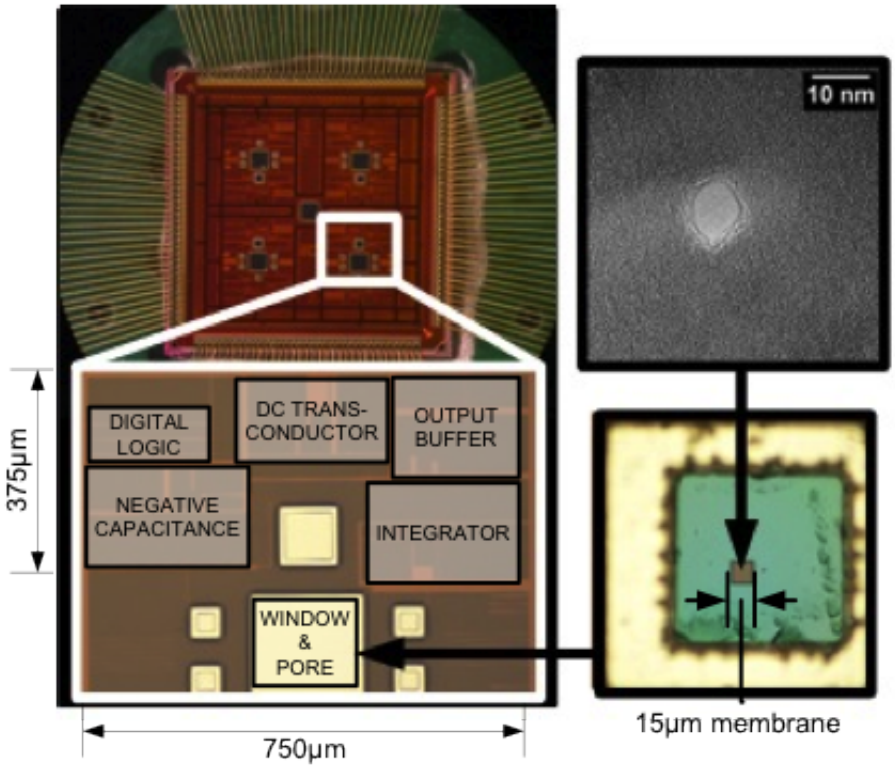

Figure 4.20: Images of a 50nm-thick silicon-nitride membrane isolated from the dielectric stack of the custom CMOS amplifier chip, along with a TEM image of a nanopore drilled through the membrane.

Using an HR-TEM as described previously, nanopores were drilled through the 50nm membranes in the amplifier dice. Fig. 4.21 shows a selection of several of these pores. The minimum pore size was approximately 6nm in diameter, which was constrained by the thickness of the membrane; the electron beam focus limits the aspect ratio and pore precision. Typically smaller pores are enabled by membranes which are 25nm or thinner.

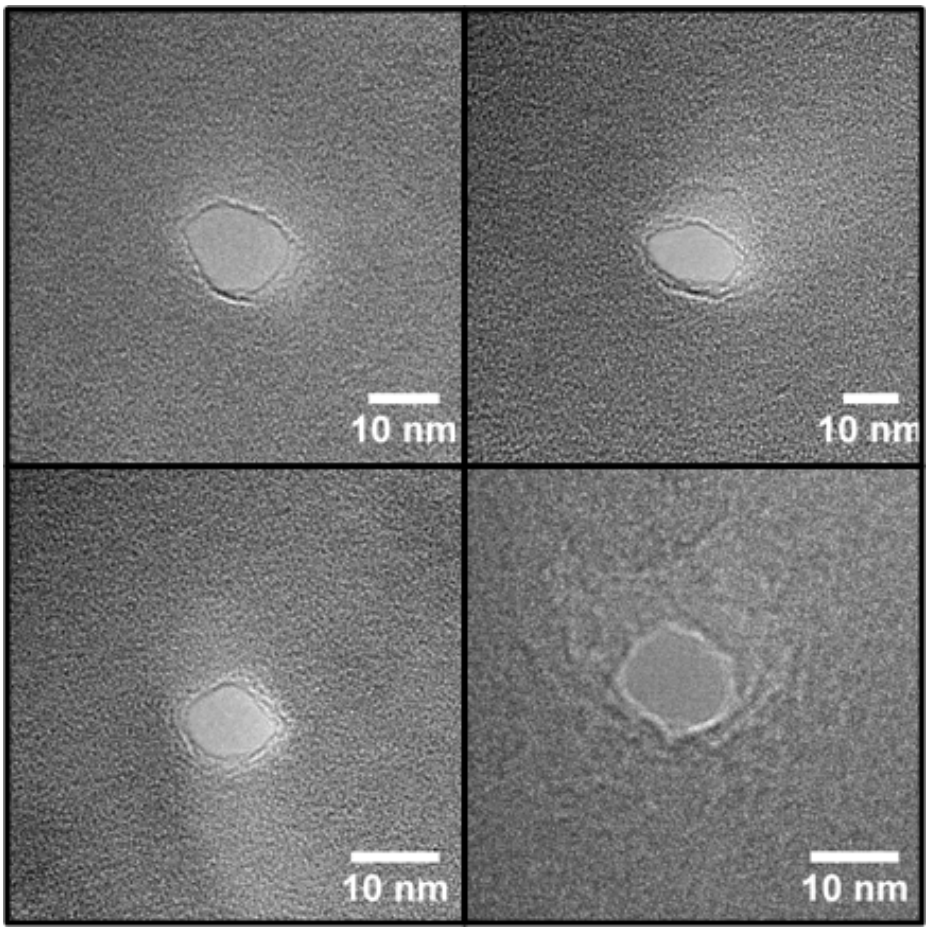

Figure 4.21: Transmission electron microscope (TEM) images of several nanopores drilled through silicon nitride membranes in a CMOS die.

Chapter 5

Integration of Lipid Bilayers and Biological Ion Channels with CMOS Preamplifiers

5.1 Introduction

In early ion channel recording platforms [70, 71], signal quality was limited by properties of the experimental setup, such as poor isolation of membrane patches, large membrane areas, and macroscale fluidic systems. However, after several decades of incremental improvements to both the geometry and materials of patch-clamp [72] and reconstituted lipid bilayer systems [73], it is now often true that ion channel instrumentation is capable of producing higher quality signals than commercially available patch-clamp electronics [40] are capable of capturing.

In addition, the low sample throughput of traditional ion channel recording systems is increasingly a bottleneck for drug discovery applications [44], and for the scalability of biological nanopore sensors.

Here we will discuss a new platform which forms lipid bilayers over microwells fabricated on the surface of a high-performance CMOS amplifier chip. This approach simultane-

ously improves the noise, bandwidth, and density limits of ion channel recording platforms, and thus it promises not only commercial relevance, but also scientific potential for higher-resolution ion channel recordings than have been made to date.

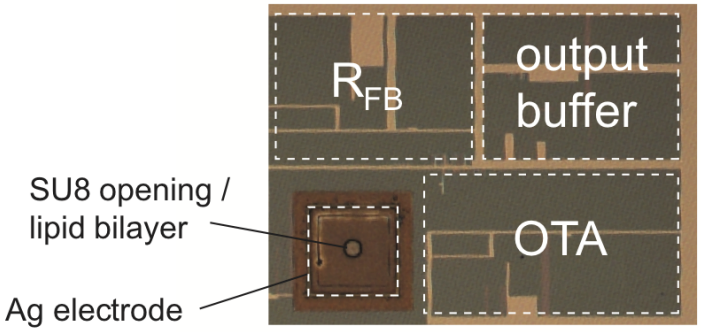

Figure 5.1: CMOS amplifier channel with a post-fabricated SU-8 microwell for a lipid bilayer

5.2 Chapter Summary

Here we present a platform for high-resolution ion channel recordings which physically combines the CMOS amplifiers introduced in Chapter 3 with biomimetic reconstituted lipid membranes. Silver/silver-chloride (Ag/AgCl) microelectrodes and hydrophobic microwells are lithographically patterned on the surface of the amplifier die, and lipid bilayers are formed over the surface of these wells. We demonstrate single-channel recordings of several varieties of biological ion channels in these membranes, including scenarios in which single-channel resolution is maintained to very high signal bandwidths. These results provide a window into the high signal fidelity and channel densities which can be achieved by leveraging existing complementary metal-oxide-semiconductor (CMOS) microelectronics for advanced ion channel sensing platforms.

5.3 CMOS Lipid Bilayer Fabrication

Starting with the custom low-noise CMOS amplifier chip described in Chapter 3, we set out to post-fabricate isolated lipid bilayers directly attached to the amplifier surface. Many

lipid bilayer platforms suspend lipids over a hole in a thin membrane [74]; however, this can require complex fluidics to create multichannel systems. Here, we deposited thin-film silver electrodes onto the amplifier input, followed by hydrophobic SU-8 microwells, onto which we painted lipid membranes [75, 76]. A micrograph of the final structure is shown in Fig. 5.1, and a cross-section is illustrated in Fig. 5.2.

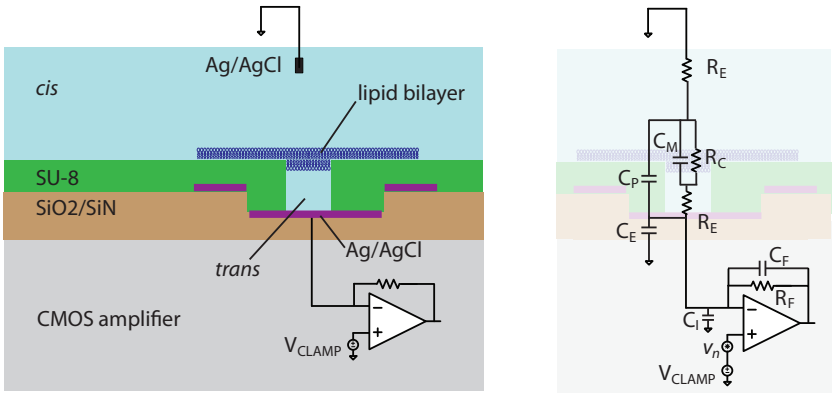

Figure 5.2: An illustrated cross-section of a lipid bilayer support on the CMOS chip, along with an equivalent circuit model.

Silver Electrodes

To provide an appropriate electrochemical interface to the electrolyte, the aluminum metallization was replaced with a silver film. Photoresist (S1813, Shipley) was patterned on the die, leaving several aluminum electrodes exposed. The aluminum was chemically removed from these pads (Al Etchant Type A, Transene), followed by electron beam evaporation of 5nm Ti and 250nm Ag. After lift-off (Remover PG, Microchem), each amplifier has a thin silver film covering its input electrode. Images of the electrodes before and after this procedure are shown in Fig. 5.3.

SU8 Microwells

Following patterning of silver electrodes, a 5 μm layer of the epoxy-based photoresist SU-8 was patterned over the majority of the chip, with small 20 μm diameter openings positioned

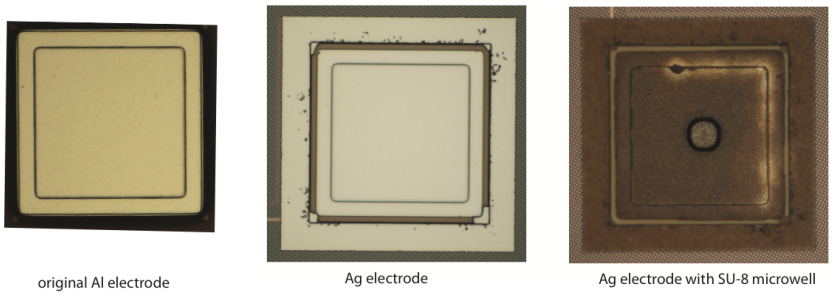

Figure 5.3: modified electrodes

over each of the amplifier channels' input electrodes. These microwells are similar to an approach previously used with thin film electrodes on passive glass substrates, connected to external amplifiers [75, 76].

The one-sided geometry of these microwells means that after each is covered by a lipid membrane, they are electrically isolated; multiple wells can be addressed in parallel, with independent *trans* Ag/AgCl electrodes and one shared *cis* reservoir. The extremely small volume of the *trans* chamber (≈ 1.6 picoliters) is also attractive; however, one downside is that the *trans* chamber is inaccessible for solution perfusion after a bilayer is formed.

Electrode Chlorination

In order to create silver-chloride (Ag/AgCl) microelectrodes, the surface of the silver needs to be converted to silver-chloride. This can be done either with electrochemical chlorination, or exposure to a chlorinating chemical such as sodium hypochlorite (bleach). Both methods were tried successfully, however we found that a short 30-second exposure to a 5 μL droplet of bleach produced a more stable potential and lower access resistance than electrically chlorinating the electrodes.

Electrode Lifetime

The total mass of available silver determines the total charge ($Q = I_{DC} \times t$) which can be measured over the lifetime of the sensor, which can be a concern with thin-film Ag/AgCl

electrodes [57, 77]. The entire $100\mu m \times 100\mu m \times 250\ nm$ electrode contains approximately 21 ng of silver, which, fully converted to AgCl, would correspond to a charge transfer of 19 μC. This places an upper bound of the electrode lifetime of approximately 2 days at 100pA DC bias. In practice, the electrode lifetime is less than the full stored charge, as AgCl is lost to dissolution and the electrode transfer resistance rises towards the end of its lifetime.

Additionally, only a fraction of the silver is directly exposed to the microwell, while the remainder is covered with SU-8. Using only the fully-exposed silver area, the lifetime would be only 0.6 μC, or 100 minutes at 100pA; however, some of the rest of the silver is likely still available to the solution from the side despite being covered on the top [77]. During testing, each electrode commonly lasted several hours before exhibiting increased resistance.

One of the concerns about microscale Ag/AgCl electrodes is that AgCl can be depleted simply from dissolution into the electrolyte [57]. However, in this arrangement the *trans* chamber has a volume of only 1-2 picoliters. With $K_{SP} = 1.8 \times 10^{-10}$, 2 pL of water would become saturated with AgCl after dissolving just 50 femtograms of AgCl. This is a negligible percentage of the available electrode mass.

Lipid Bilayer Formation

A fluid chamber was constructed around the amplifier, and filled with 200 μL electrolyte (1M KCl, 10mM EDTA, 5mM Tris, pH 8.0, unless otherwise noted). Before introducing lipids, an Ag/AgCl pellet was placed in the *cis* chamber, and a 100 $M\Omega$ resistor was placed in series with the bias voltage source to avoid saturating the amplifier. The bias was varied, open circuit continuity was confirmed, and the liquid junction potential offset was calibrated. Less than 0.5 μL of a diphytanoyl phosphatidylcholine solution (10 mg/mL DPhPC in n-decane) was painted on the surface of the amplifier using an air bubble at the tip of a micropipette. After confirming a $G\Omega$ seal resistance, the $100M\Omega$ series resistance was removed from the *cis* electrode. Bilayer formation was confirmed by inferring the

membrane capacitance from the noise spectrum; bilayers typically formed in less than 1 minute, and contributed at least 1 pF to the total capacitance.

5.4 System Modelling

The specific capacitance of DPhPC is approximately 0.45 $\mu F/cm^2$ [78]. For a membrane diameter $\approx$ 20 μm, this implies a membrane capacitance $C_m \approx 1.4pF$. We observed ion channel activity with 1 $pF < C_m < 2$ pF, which suggests some degree of variability in the exact microwell diameter, as well as the size of the annulus of thicker lipids and solvent at the edges of the well.

Knowing the geometry of the electrodes and microwells, we can build a simple electrical model for the parasitics of the measurement (Fig. 5.2).

The parasitic capacitance from the $100\mu m$ electrode to the Si substrate (C_E) is approximately $50fF$. The parasitic capacitance between the remainder of the electrode and the electrolyte (C_p) is $70fF$. The electronic input capacitance of the amplifier (C_I) is $1pF$, and the feedback capacitance (C_F) is $0.15pF$. Letting $C_m = 1.5pF$, this adds up to a total of $\Sigma C \approx 3pF$.

5.5 Noise Performance

The baseline input-referred noise with a bilayer formed is shown in Fig. 5.4, alongside the baseline open-headstage noise (blue dotted line, from Chapter 3). The black dotted line is a polynomial fit to the measured spectrum. Below 10 kHz, the bilayer does not affect the noise spectrum. Above 10 kHz, a new source of noise with $S_n(f) \propto f$ is evident, and at several hundred kHz it is evident that there has been a small increase in the f^2 noise as well. The f^2 noise is explained by the addition of capacitances C_m, C_E, and C_P (Fig. 5.2). The f noise is attributable to dielectric loss in the ionic capacitances in the measurement ($C_m + C_P$).

If a 4th-order Bessel low-pass filter is applied at various cutoff frequencies, this

bilayer baseline noise corresponds to noise of 1 pA_{rms} at 10 kHz, 4.4 pA_{rms} at 100 kHz, 11.8 pA_{rms} at 250 kHz, and 61 pA_{rms} at 1 MHz. These numbers can be compared to alternate lipid bilayer platforms, although many of these systems often all rely on the same discrete patch-clamp amplifiers (notably the Axopatch 200B [79], Axon Instruments). The highest-performance ion channel systems generally have lower noise below 10kHz, due to operation with higher transimpedance gain [73, 80] or capacitive feedback [72, 81]. At higher frequencies, only a patch clamp system with specifically customized electronics [82] demonstrated noise density comparable to the new integrated system.

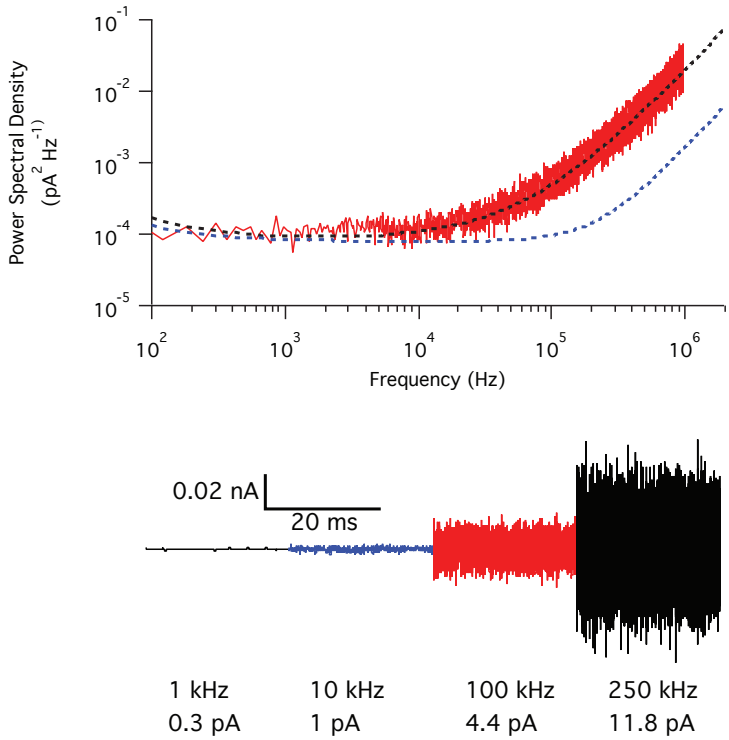

Figure 5.4: Baseline noise with CMOS-anchored lipid bilayer. The black dotted line is a fit to the meausured specturm (red), and the blue dotted line shows the dry open-headstage noise for comparison. Time traces of the bilayer baseline are shown at several bandwidths.

5.6 Ion Channel Recordings

5.6.1 Gramicidin

Gramicidin is an antibiotic compound which interacts with bacterial cell membranes [83–86], increasing their permeability and often killing the bacteria. Gramicidin produces transient dimer channels in lipid bilayers, forming a junction between two molecules on either side of the membrane. This structure makes the formation of gramicidin channels strong evidence for a true lipid bilayer rather than a thicker amorphous or multilayer structure. Gramicidin ion channels spontaneously form and dissociate after some period of time, irrespective of voltage, yielding stepwise conductance changes in voltage-clamp recordings.

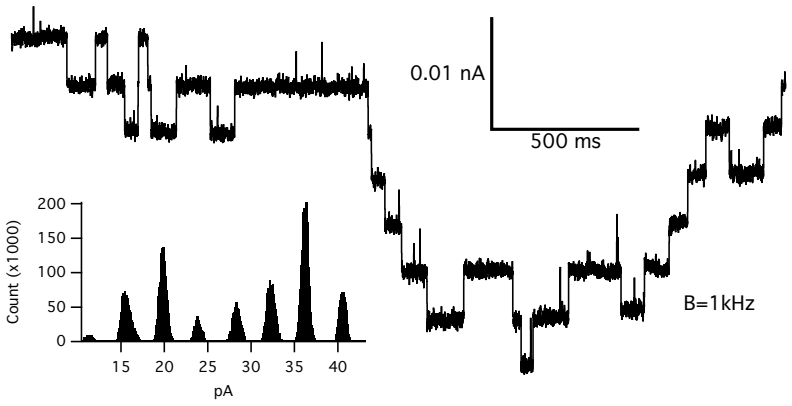

Figure 5.5: Gramicidin channels recorded on the new platform, digitally low-pass filtered to B=1kHz. Inset is an all-points histogram of the displayed trace.

To produce gramicidin recordings on the new integrated platform, prior to forming a bilayer <0.5μL gramicidin solution (1μg/mL in ethanol) was added to the 200μL electrolyte so that it would be present in both the *cis* and *trans* chambers. After painting the bilayer, random stepwise current fluctuations were observed. An example recording of gramicidin is shown in Fig. 5.5, showing several simultaneously gating channels.

5.6.2 Alamethicin

Alamethicin is a 20-amino-acid peptide which can form homomeric ion channels in lipid membranes. Its channel formation is voltage-dependent, it has comparatively large single-channel conductance, and it interacts with a wide range of lipid membranes, making it a useful model system for studying the biophysics of voltage-gated ion channels [87, 88].

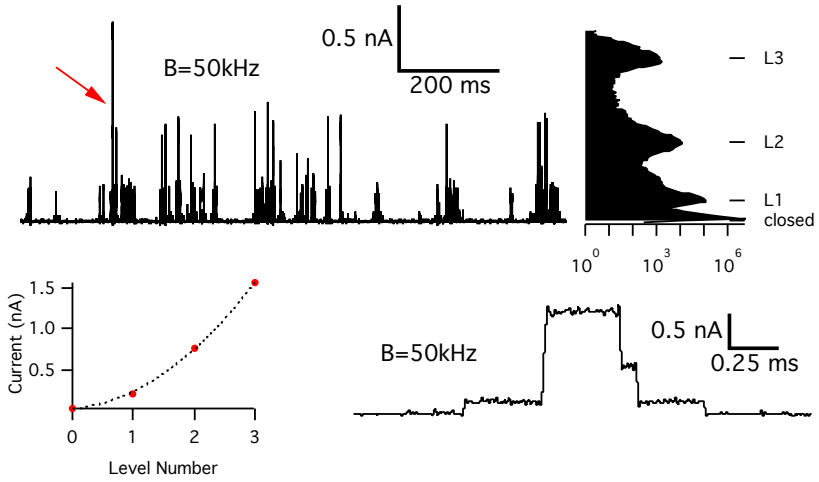

Figure 5.6: Single alamethicin channel bursts. These traces have been digitally filtered to B=50kHz.

Each channel formed by alamethicin consists of an integer numbers of peptides, with larger aggregates producing larger diameter channels and correspondingly higher conductance. In single-channel recordings of alamethicin, stepwise bursts are often observed which correspond to sequential insertions of peptides into a single aggregate.

Fig. 5.6 shows a trace of single alamethicin channel bursts. After forming lipid bilayers on the amplifier chip, 1 μL of 10 μg/mL alamethicin in ethanol was added to the *cis* chamber. Shortly after adding the peptides, channel current bursts appeared at negative bias voltages. Within each burst, discrete quadratically-spaced levels are clearly visible, characteristic of alamethicin.

The relatively high conductance of alamethicin channels provides a useful model system to demonstrate high-bandwidth ion channel recordings. Unlike single-channel record-

ings of most other channels, temporal resolution of alamethicin recordings is often limited by the electronic amplifiers rather than the experimental setup [73, 75, 89]. In high salt concentrations, Alamethicin conductance steps can be as large as several hundred pA [87], suggesting in a fully optimized measurement these transitions would observable at MHz signal bandwidths. Fig. 5.7 shows expanded images of the transitions from Fig. 5.6, at both 50 kHz and 1 MHz signal bandwidth. At 50 kHz, rise and fall times are approximately 10 μs, while at 1 MHz they are 500 ns. At the lower bandwidth the second conductance state in the rising transition is entirely washed out, while at the high bandwidth fast flickering states as short as $3\mu s$ are visible. By contrast, in the falling transitions the higher bandwidth confirms that 50 kHz was sufficient to resolve all of the major conductance steps. Here the sharpness of the conductance steps makes it clear that the channel conductance changes occur in mere nanoseconds.

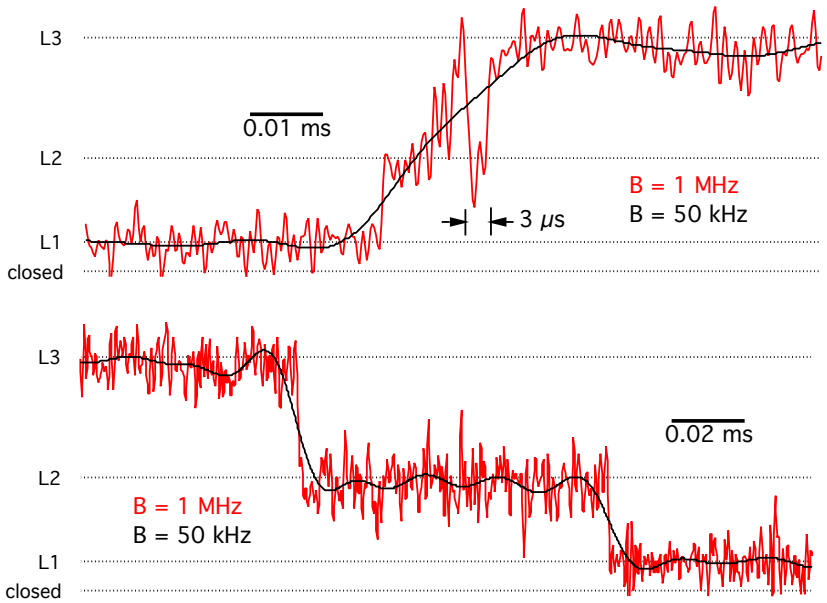

Figure 5.7: Alamethicin conductance steps resolved at 1 MHz bandwidth. These traces are expanded from the transitions in Fig. 5.6

5.6.3 Alpha Hemolysin

Alpha hemolysin (α-HL) is a well-studied bacterial toxin which forms homomeric ion channels in cell membranes [90]. The pores formed by α-HL are relatively high-conductance and non-selective, and they are stable under a wide range of conditions [91]. Like other ion channels, α-HL can exhibit gating, but in many conditions it can remain continuously open for minutes or hours at a time. Thanks to these properties, α-HL has attracted significant attention as a biological nanopore sensor [10, 28, 92]. A statically-open α-HL channel has a diameter of approximately 1.4 nm at its smallest constriction; even very small molecules can measurably modulate its ionic conductance.

It has been shown that polyethylene glycol (PEG) molecules can modulate the conductance of an α-HL channel, and that each length PEG molecule causes a distinct blockage depth. When a range of PEG molecule sizes are present together in solution, a histogram of events' blockage produces discrete levels, each of which corresponds to one length PEG molecule [76, 93–95].

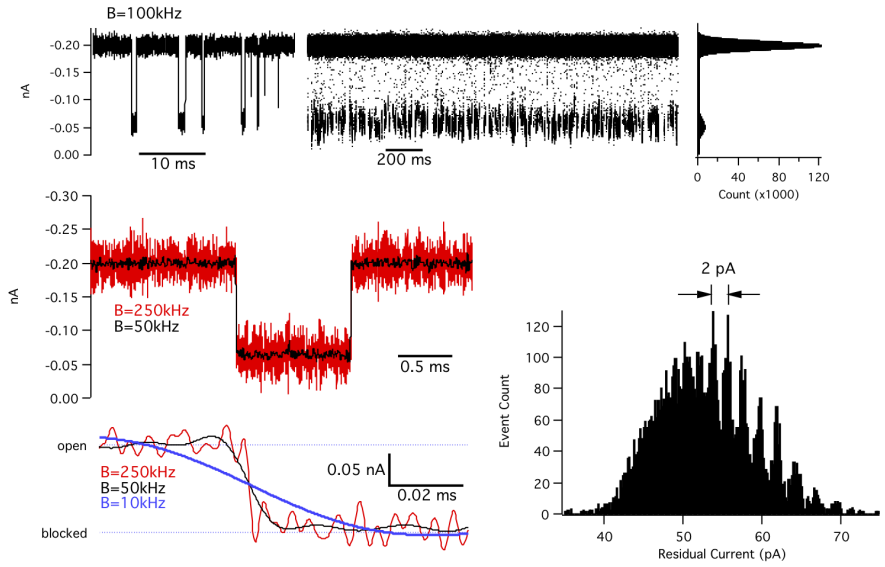

Figure 5.8: A single α-HL channel exposed to polydisperse polyethylene glycol.

Fig. 5.8 shows a trace measured with a single α-HL channel in a lipid bilayer on

the CMOS chip, in the presence of PEG-1500 containing a range of molecular weights. In 4M KCl, after forming a bilayer α-HL monomers were added to the *cis* chamber to a final concentration of approximately 0.25 $\mu g/mL$. The potential was held at +50mV for several minutes until the current increased from zero to 200 pA, indicating the insertion of a single α-HL channel. The *cis* chamber was then flushed with fresh 4M KCl containing polydisperse PEG (1,400-1,600 g/mol).

The signal exhibited transient blockages, of approximately 75% of its open state current. The trace was processed to characterize the depth and duration of these blockages. After filtering the signal to a bandwidth of 100 kHz, events were identified as blockages more than 50 pA from the open pore current. The depth of each event was characterized as the average current level excluding the first 50 μs and the last 10 μs of the pulse. Fig.5.8 shows a histogram of the levels of the 7,642 events for which $\tau > 0.5\ ms$ found in 6 minutes of data. Similar to prior demonstrations [76, 93–95], the histogram shows distinct peaks, each corresponding to a distinct PEG molecule length.

The procedure of determining the depth of each pulse by averaging all of its points is equivalent to a low-pass filter; the remaining expected error should correspond to the integrated noise to a bandwidth of roughly $B = 1/(2\tau)$, where τ is the duration of the pulse. In the histogram of these events, the peaks are separated by approximately 2 pA and each peak has a FWHM of approximately 1.2 pA. This suggests a standard deviation of approximately 0.5 pA, which is only moderately higher than the RMS current noise for B = 1 kHz. Thus it is reasonable to believe that the width of these histogram peaks is largely determined by the low-frequency noise of the amplifier, rather than by the channel current itself. Thus, while the pulses themselves can be clearly identified at several hundred kHz, steps that improve the low-frequency noise density of the amplifier, or lengthen the pulses, would be expected to improve the ability to distinguish between the PEG polymer lengths.

Distinguishing between PEG sizes in this application offers similar challenges to distinguishing between bases in a nanopore DNA sequencing application. While the presence or absence of an analyte molecule is marked by a large signal, the amplitudes that distinguish

between different molecules may be significantly smaller. For the PEG signals in Fig. 5.8, the presence of a molecule could be distinguished from the background noise in as little as 2 μs; however, to correctly identify its molecular weight it would need to remain in the pore for 500 μs.

Chapter 6

Conclusions

6.1 Summary of contributions

This dissertation describes a range of efforts related to the design and evaluation of high-performance microsystems for ion channel measurements. The overarching goals of this work were to reduce the physical size and improve the temporal resolution of ion channel and nanopore recordings. In order to achieve these goals, a custom low-noise integrated circuit transimpedance amplifier was designed in 0.13-μm CMOS. The low input capacitance of this custom circuit was particularly beneficial at high frequencies, where parasitic capacitance is a dominant source of noise in voltage-clamp recordings. Systems were designed to introduce this amplifier directly into an electrochemical environment, providing a compact and low-capacitance measurement cell. This new amplifier was applied to solid-state nanopore sensors, and solid-state nanopore signals were successfully recorded at lower noise and finer temporal resolution than had been previously achieved. A procedure was also developed to drill solid-state nanopores directly through a CMOS die. The surface of the same amplifier was then adapted to host microscale lipid membranes, into which bacterial ion channels were introduced, and single-channel currents successfully recorded.

6.1.1 Original Contributions

This work has made several original contributions to the fields of microelectronics, biosensors, and electrophysiology, including:

- The highest-bandwidth nanopore recordings demonstrated to date ($SNR > 5$ at $B = 1MHz$).
- The first reported single-ion-channel recordings using a fully integrated transimpedance preamplifier.
- The first ion channel current preamplifier to incorporate a thin-film Ag/AgCl microelectrode.
- The first demonstrated solid-state nanopore drilled through a CMOS die.
- A derivation of a closed-form expression for the maximum achievable nanopore signal bandwidth in the presence of various parasitic impedances.
- A highly scalable and low-noise platform for ion channel recordings that assembles lipid bilayers in contact with an integrated semiconductor amplifier.
- The highest-bandwidth recordings of single biological ion channels demonstrated to date ($B = 1\ MHz$).

6.1.2 Publications

These contributions have resulted in the following peer-reviewed publications:

1. Rosenstein, J., Ramakrishnan, S., Roseman, J., & Shepard, K.L. Single Ion Channel Recordings with CMOS-Anchored Lipid Membranes, *in preparation*
2. Rosenstein, J. K., Wanunu, M., Merchant, C. A., Drndic, M., & Shepard, K. L. (2012). Integrated nanopore sensing platform with sub-microsecond temporal resolution. Nature Methods, 9(5). doi:10.1038/Nmeth.1932

3. Rosenstein, J., & Shepard, K. L. (2012). High-throughput biology in the time domain: Improving temporal resolution of single-molecule sensors. 2012 IEEE International Symposium on Circuits and Systems (ISCAS), 22912294. doi:10.1109/ISCAS.2012.6271752

4. Rosenstein, J., Sorgenfrei, S., & Shepard, K. L. (2011). Noise and Bandwidth Performance of Single-Molecule Biosensors. Custom Integrated Circuits Conference (CICC).

5. J. Rosenstein, V. Ray, M. Drndic, K. L. S. (2011). Nanopore DNA Sensors in CMOS with On-Chip Low-Noise Preamplifiers. International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS), 874877.

6. Rosenstein, J., Ray, V., Drndic, M., & Shepard, K. L. (2011). Solid-State Nanopores Integrated with Low-Noise Preamplifiers for High-Bandwidth DNA Analysis. IEEE/NIH Life Sciences Systems and Applications Workshop (LiSSA), 5962.

6.2 Future work

Reduce Noise Further

As discussed in Chapter 2, high-frequency voltage-clamp noise density is a function of $v_n \times \Sigma C$. The advantages of the systems described here have come from reducing ΣC, while actually tolerating a slightly higher v_n than can be achieved with types of semiconductors unavailable in standard CMOS processes (such as III-V semiconductors and junction field effect transistors). If one could combine the low-capacitance systems described here with these specialty semiconductors, it could potentially produce a system with $v_n = 1\ nV/\sqrt{Hz}$ and $\Sigma C = 1\ pF$. In theory this would have a noise floor five to ten times lower than achieved here, and the baseline noise could be as low as $I_{rms} = 0.12\ pA_{rms}$ for $B = 100\ kHz$, or $I_{rms} = 3.6\ pA_{rms}$ for $B = 1\ MHz$.

Extend Bandwidth Further

Typically patch clamp recordings have been performed with signal bandwidths on the order of 10 kHz or less. On a few rare occasions [82, 96] the bandwidth was extended beyond

100 kHz. The presented work showed that there are scenarios in which nanopores and ion channels can be recorded much faster than this, but 1 MHz this is not a fundamental limit. It is very reasonable to expect that 10 MHz bandwidth can be achieved for certain conditions.

In a plausible best-case scenario, if we imagine an amplifier with $v_n = 1\ nV/\sqrt{Hz}$ and a system with $\Sigma C = 1\ pF$, this would correspond to integrated noise of approximately 115 pA_{rms} for $B = 10\ MHz$. This is beyond acceptable levels for most single-channel applications, but it might still find use for solid-state nanopore applications [97] and whole-cell gating current studies [96].

Multichannel Operation

The CMOS amplifier design presented here contains 8 channels, yet data was only presented which utilized one channel at a time. This is not a limitation of the electronics, but rather the fluidics. The inputs to each amplifier must be well isolated from one another, meaning multichannel operation would require isolated *trans* fluid chambers. This is fairly straightforward for the lipid bilayer systems described here, but it is less obvious how such isolation would be achieved for the solid-state nanopores. Achieving highly parallel recordings is one of the primary commercial motivations for the integration of nanopores and ion channels with CMOS electronics, and thus it would be well worth the time to consider what fluidic arrangements would provide both the micron-scale density and $G\Omega$ isolation that this would require.

Maximize Channel Density

The maximum channel density is a function of the fluidics, as described above, but also of the area of the CMOS electonics. The amplifier presented here is approximately 0.2 mm^2, but this is not optimized for area. Within each channel, roughly 1/3 is the OTA, 1/3 is the feedback network, and 1/3 is the output buffer. A system-level solution could likely be found which eliminates the output buffer. The existing feedback network is not optimized

for area, and could be significantly reduced in size. Roughly half of the area of the OTA is occupied by the compensation capacitor, which could be eliminated by moving to a single-state load-compensated OTA.

Thus without significant technology changes, the area of each channel could likely be reduced to 20% of its current area, leaving 0.04 mm^2, or $200\mu m \times 200\mu m$. This would yield 2,500 channels per cm^2. At that point, power consumption concerns could easily dominate, since achieving the noise levels presented here would probably still require $> 1\ mW/channel$, or $> 1.6\ W$ total. These power levels could heat the electrolyte significantly.

Assuming thermal concerns can be addressed, the remaining circuit area requirement is determined by the need for low $1/f$ voltage noise in the OTA. Circuit techniques or alternate technologies which exhibit lower A_n/f voltage noise per transistor area would allow a smaller channel footprint for a given noise budget.

Functional Monolithic Solid-State Nanopores

We have shown that it is possible to fabricate solid-state nanopores drilled directly through a CMOS die. However, we have not yet demonstrated successful experiments with measurements of nanopore signals from a pore drilled through the same die as its amplifier. Our attempts fell short largely due to issues with fabrication yield and pore cleaning. A successful demonstration here should be possible, but it will require wafer-level fabrication and meticulous cleanroom standards.

Automate Bilayer Formation

The lipid bilayer demonstrations here were performed by manually pipetting and painting lipids over the hydrophobic aperture. A higher-throughput automated system would strongly benefit from some mechanism of automated bilayer formation on the chip [74].

Extend to Live Cell Patch Clamp

Of the wide variety of ion channels, relatively few are available for reconstitution into planar lipid membranes. More commonly, ion channel studies are performed with patch clamp recording on channels heterologously expressed in *in vitro* cell lines. Incorporating the technologies presented here with live cells would would be extremely valuable [98, 99], and require additional fluidics, patch clamp apertures, and automation. Some combination of a parallel planar patch clamp [43] with planar microelectronics would be a logical path to take.

Add Parasitic Compensation

It would be valuable to introduce programmable compensation circuitry for parasitic capacitances and series resistance, as are commonly included in patch clamp systems [42]. This would require some careful analog design and more area per channel than a simple uncompensated voltage-clamp stage, but it is quite doable and several examples exist in the literature [99]. Maintaining adequate parasitic cancellation to MHz bandwidths may require some modifications to the compensation circuits common for lower-bandwidth recordings [42].

6.3 Final thoughts

The history of electrophysiology continues to be one of leapfrogging advances in electronic measurement systems and physiological techniques. The low-noise current measurement platforms developed here can be considered to be just one more step in a long lineup of improved ion channel interfaces. On a technological level, I hope that these demonstrations highlight the enormous potential for improving today's rudimentary interfaces between electronics and biology. Any modern doctoral thesis related to nanotechnology seems empty without a refence to Richard Feynman, and on a philosophical level I hope that my research serves as one more small reminder that what we can build or measure today is not all that

there is; even after all these years, there is still plenty of room at the bottom [100].

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