Advanced Integration of Devices Enabled by Laser Crystallization of Silicon

Vincent W. Lee

Submitted in partial fulfillment of the
requirements for the degree
of Doctor of Philosophy
in the Graduate School of Arts and Sciences

COLUMBIA UNIVERSITY

2012

ABSTRACT

Advanced Integration of Devices Enabled by Laser Crystallization of Silicon

Vincent W. Lee

The push for higher levels of performance drives research and innovation in all areas of electronics. Thus far, shrinking circuit sizes and development of new material systems have satisfied this need. Continued scaling and material improvements have become increasingly difficult; simultaneously, more functionality is needed in smaller spaces. Advanced integration techniques provide a solution by engineering together previously incompatible systems.

The fabrication of high-performance devices typically requires high temperature processing steps. Since fabrication occurs sequentially, the high temperature prevents the direct integration of two high-performance layers, as completed devices cannot withstand the processing temperatures of subsequent steps. There are significant challenges to integrating process-incompatible systems, and techniques such as wafer bonding, heteroepitaxial growth, and various thin film technologies have shown limited success.

In this work, advanced integration is achieved through laser crystallization processes. Unique to laser methods is the ability to locally heat the surface of a material while keeping the underlying substrate at room temperature. This property allows for high performance electronic materials to be integrated with substrates of different functionalities. This thesis focuses on three key components for advanced integration: 1. Laser-crystallized electronic devices, 2. Relevant substrates for integration, and 3. The feasibility of integrating of laser-crystallized devices with low-temperature

substrates.

Two types of laser-crystallized devices are explored. Thin-film, laser-crystallized silicon transistors are fabricated at low-temperatures and exhibit high mobilities above 400 cm^2/Vs. Vertical structure diodes built from laser-crystallized silicon outperformed epitaxially-grown diodes of the same geometry.

Light emitting diode (LED) arrays are fabricated from compound semiconductor substrates and tested for display applications. These LED arrays are envisioned to sit underneath the laser-crystallized devices, enabling new applications where both high brightness and high performance transistors are needed. Substrates of low-κ dielectric material are also of interest, as they are widely used for their low capacitance properties. Preliminary results suggest that laser crystallization of silicon can be successfully performed on a low-κ dielectric.

In addition to enabling new device architectures, it is important for laser crystallization methods to leave the underlying layers unaffected. Simulations of the laser irradiation process predict substrate temperatures to reach only 70°C even when the surface reaches the melting temperature of silicon (1400°C). Integration feasibility is further investigated with measurements on conventional front-end field effect transistors. When comparing properties from wafers with and without laser processing, no changes in transistor characteristics are observed.

In all three components of work, proof-of-principle devices and concepts lay out the groundwork for future investigation. The developed technologies have promising applications in both the microelectronics and display industry. In particular, the integration of LEDs and laser-crystallized silicon enables a high-brightness microdisplay platform for head-mounted displays, pico projectors, and head-up displays.

Table of Contents

List of Figures

List of Tables

Acknowledgments

I would first like to thank my advisor, Professor Ioannis Kymissis, for his support and guidance throughout my years here. His positive energy and always helpful feedback kept me going forward. Second, the support and friendship of all the current and past members in the Columbia Lab for Unconventional Electronics have been amazing. In particular, I'd like to thank Dr. Nadia Pervez, Dr. Brian Tull, Dr. Zhang Jia, Dr. Yu-Jen Hsu, John Sarik, Haig Norian, Jonathan Beck, Marshall Cox, Shyuan Yang, and Hassan Edrees for all the lengthy discussions and various contributions to my work.

I would like to thank all the members of Professor James Im's research group. In particular, Dr. Alexander Limanov - without his help and willingness to continuously try failed laser experiments this thesis would not be possible. In addition, I owe thanks to Adrian Chitu and Gabriel Ganot for their help with additional experiments and laser simulation work.

I would like to thank all of the collaborators who contributed material, samples, measurements, and time to various projects. Dr. Chung Lam, Dr. Edward Kiewra, Dr. Asit Ray, and Professor Robert Laibowitz for wafers and measurement support in the 3DIC project. Professor Robert Laibowitz and Dr. Noel Russell for low-κ dielectric material. And lastly, Dr. Christian Witt for providing wafers in the recrystallization of copper.

I would also like to thank everyone who was involved in the OLED/CMOS integration project. In particular, Zeynep Basaran, who took on this challenging project over several summers, and developed the project from a CMOS chip and board to

a nearly fully integrated process. In addition, Dr. Ajay Balankutty, Keith Dronson, and Haig Norian for CMOS design and tape-out help, version 1 of the test circuit board, and shared knowledge of his SU-8 encapsulation process, respectively.

My girlfriend, Nancy Twu, for all her love, support, and understanding.

Finally, the love and support of my family. My mom and dad, and my two brothers.

To my Mom and Dad

Chapter 1

Introduction

1.1 Background and Motivation

Much of the advancement in the electronics and semiconductor industry can be attributed to the shrinking of transistor gate lengths and resulting increase of transistor density and performance. While significant efforts continue on fulfilling Moore's Law, the doubling of transistor density every two years, shrinking is increasingly difficult, motivating research in alternative technologies such as advanced integration techniques [1][2][3][4].

Many categories of semiconductors are widely utilized for various applications, including silicon, compound semiconductors, oxide semiconductors, amorphous silicon, and organic semiconductors. Each group has distinct performance advantages, leading to their adoption in different industries. For example, crystalline silicon has been strongly optimized for high performance computing, while III-V compound semiconductors have a direct band gap, making them very efficient light emitters. Organic and oxide semiconductors have very low process temperatures and are compatible with many substrates such as plastic and glass.

Advanced integration of different materials enables new platforms by allowing for more functionality in the same space. However, integration of different material sys-

tems is difficult because of incompatible fabrication processes and substrates, as well as material issues such as lattice matching and chemical compatibility. Various integration techniques have been demonstrated for limited systems through the use of shape self-assembly [5], wafer bonding [6], and heteroepitaxy growth [7][8]. Several of these have been demonstrated in the laboratory, but with limited yields and no commercial success to date. Wafer bonding and gluing of compound semiconductor wafers to apertured and thinned silicon wafers has also recently been demonstrated [9], but suffers from a range of practical problems including poor bonding due to the limited thermal budget and mismatched coefficients of thermal expansion. Heteroepitaxial growth of compound semiconductor devices on pre-fabricated silicon circuitry is a promising approach, but it is limited by the availability of compatible growth processes. Metal alloy bump bonding is used to make small arrays of IR detectors on transparent substrates, but the general applicability of this strategy is limited [10]. Perhaps the most encouraging strategy is recent work showing the use of small indium bonds to attach a silicon wafer with an LED array [11]. However, like metal alloy bump bonding, the ultimate level of integration and device yield is limited by the size and reliability of the bonding process.

In many cases, the significant challenge to integration is making processes compatible. Many of the high performance materials such as silicon and compound semiconductors require high temperature processes (600-1000°C) during growth or device fabrication, but cannot withstand these temperatures in post-processing. For example, silicon transistors typically have several high temperature growth and dopant activation steps (up to 1000°C), but after these initial steps, temperatures cannot exceed 400°C or the device characteristics may shift. This is problematic when a post-processing step such as growing a second layer of silicon or growing other materials (III-Vs) is desired, since all of these processes will exceed the 400°C threshold.

One promising technique allowing for better process compatibility is laser crystallization. A high power laser can shoot short pulses or a continuous wave at a material,

exposing it to energies high enough to induce phase transitions or crystallize amorphous material at the surface, but leaving the underlying substrate at about room temperature and unaffected. In a typical laser crystallization process, the irradiated film can reach melting temperatures for the film (1400°C for silicon), but because the exposure area is localized and the pulse duration is short, only the top surface is transformed.

Laser crystallization is proposed as a means to monolithically integrate multiple high performance materials. This is significant for currently incompatible systems such as silicon on compound semiconductors and multi-layered high performance silicon. New devices fabricated monolithically with these systems can enable breakthroughs in both displays and microelectronics.

1.2 Diodes, Light Emitting Diodes, and Field Effect Transistors

Three devices are discussed throughout this thesis: diodes, light emitting diodes (LEDs), and field effect transistors (FETs) [12][13].

1.2.1 Diodes

A diode is a two-terminal electronic device which allows electrical current to pass in only one direction. Modern day diodes are built from n-type and p-type semiconductor materials. To produce n-type materials, silicon is doped with a group V donor element. When the group V element is activated within the silicon lattice, it donates an extra electron to the silicon, and the electron freely moves around and conducts electricity. Phosphorus and arsenic are typical donor atoms for silicon. For p-type material, silicon is doped with a group III acceptor element, typically boron. Within a silicon lattice, the group III element is missing an electron and can accept an electron from silicon. This creates a void in the silicon where an electron is missing, also

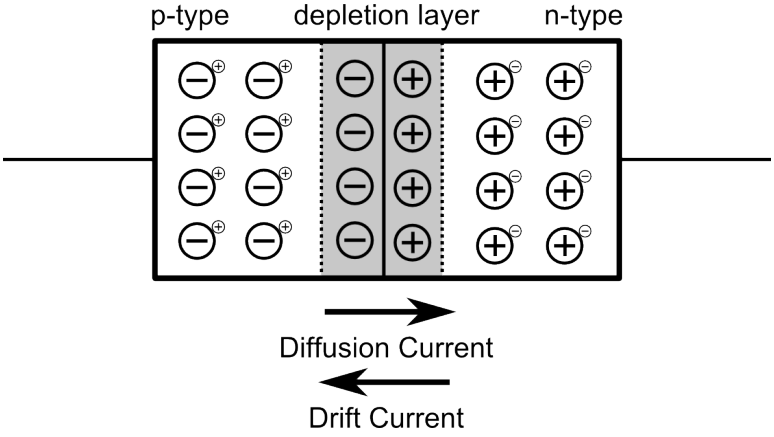


Figure 1.1: Schematic drawing of p-n junction showing its depletion region and drift and diffusion currents.

known as a hole. Holes are positively charged due to lack of an electron, and can also conduct electricity. As electrons hop from a filled state to a hole, it can appear as if the hole is moving in the opposite direction of the electron. Thus, both n-type and p-type materials can conduct electricity, but n-type preferentially conducts with electrons and p-type preferentially conducts with holes.

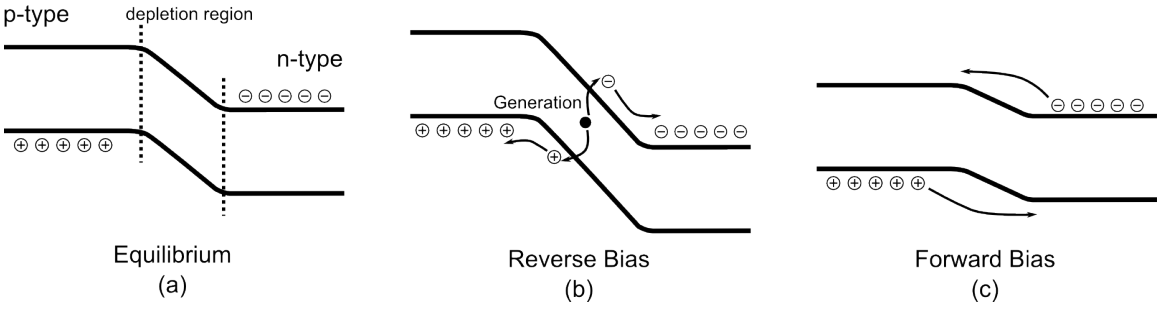


Figure 1.2: Band diagram for a p-n junction diode in (a) equilibrium state, (b) reverse bias, and (c) forward bias.

Placing p-type and n-type materials together forms a p-n junction, and the semiconductor diode. Because one side of the junction has a high concentration of delocalized of holes, and the other side has a high concentration of delocalized of electrons,

the mobile electrons and holes diffuse across the junction and recombine to form a depletion region, fig. 1.1. As more of these electrons and holes recombine, an electric field forms within the depletion region and induces a drift current in the opposite direction of the diffusion current. In equilibrium, the diffusion current and the drift current are in equal and opposite directions. Schematically, the p-n junction has a band diagram similar to fig. 1.2a.

When biased with an external potential, the equilibrium between diffusion current and drift current is disturbed. In reverse bias, a negative voltage is applied to the p-side of the diode causing the depletion width widens and no current is allowed to pass except for a very small component caused by thermal generation, 1.2b. In forward bias, the depletion width shrinks and the electrons and holes on the n-side and p-side now have enough energy to pass through the depletion region and conduct current, fig. 1.2c. A typical current-voltage characteristic of a diode is shown in fig. 1.3, governed by the following equations [12]:

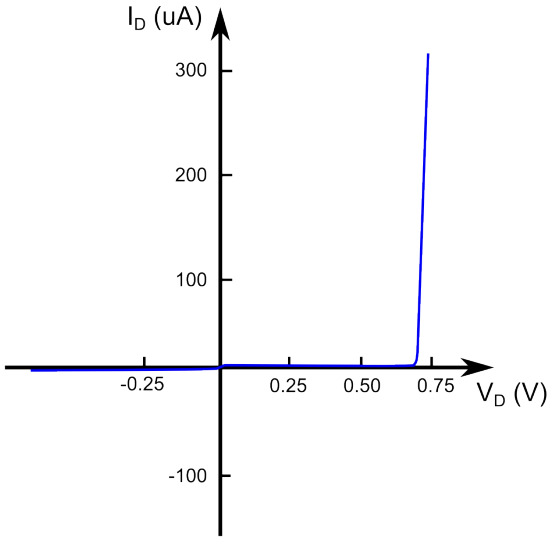


Figure 1.3: Typical Current-Voltage characteristic of a semiconductor diode. Adapted from reference [12]

$I_D = I_0(e^{V_D/V_{th}} - 1)$

where $I_0 = qn_i^2A[(D_p/N_dW_n) + (D_n/N_aW_p)]$ for short-base diodes, where minority carriers crossing the p-n junction do not recombine before reaching the contacts, and $I_0 = qA[(D_pp_{n0}/L_p) + (D_nn_{p0}/L_n)]$ for long-base diodes, where minority carriers crossing the p-n junction do recombine before reaching the contacts.

The non-linear characteristics of diodes can be used in simple switching applications, rectifying applications such as the conversion of alternating current signals to direct current, or clamping circuits such as electrostatic discharge circuits.

1.2.2 Light Emitting Diodes

Light emitting diodes (LEDs) are a subset of diodes, which as the name implies, emit light. Instead of silicon, LEDs are typically fabricated from III-V compound semiconductor materials, such as aluminum gallium arsenide, or indium gallium nitride. When compared to silicon, which has an indirect band gap, aluminum gallium arsenide (AlGaAs) and indium gallium nitride(InGaN) have the direct band gaps required for efficient light output. Modern LEDs are heterojunctions, consisting of multiple AlGaAs or InGaN films. By adjusting the ratio of aluminum to gallium or indium to gallium in these materials the band gap can be adjusted. The Al/Ga or In/Ga ratios in the multilayer heterojunction structure of the LED is engineered to confine and induce recombination in a specific layer and thus control the wavelength of light output. Fig. 1.4 shows the band diagram for an LED heterojunction. This is similar to the diode band diagram in the previous section, except electrons and holes are now confined in a layer between the p-type and n-type layers, the intrinsic active layer. This active layer is engineered for a particular band gap to produce a particular peak light emission wavelength.

A representative cross sectional image of a LED is shown in fig. 1.5. Each layer in the heterojunction is annotated in the image. The n-AlGaAs and p-AlGaAs confine electrons and holes to the intrinsic-AlGaAs where recombination occurs and photons

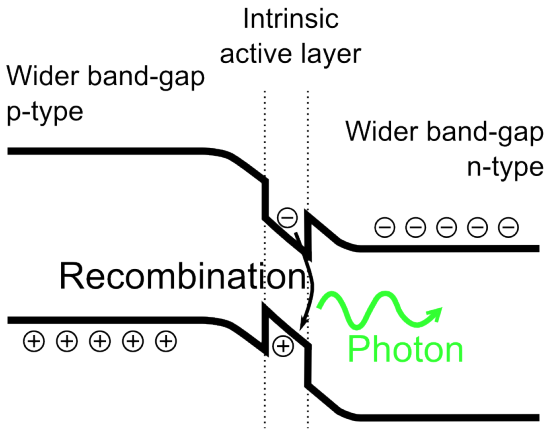


Figure 1.4: Band diagram of LED heterojunction. Electrons and holes are confined within the middle region where recombination occurs and photons are emitted.

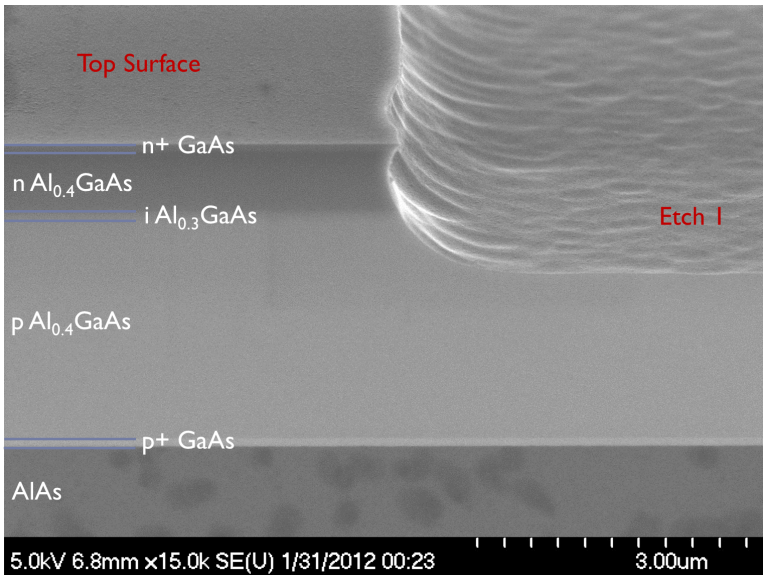


Figure 1.5: Cross sectional scanning electron micrograph of LED heterojunction. The n-AlGaAs and p-AlGaAs have a larger band gap. Electrons and holes in the intrinsic-$Al_{0.3}GaAs$ layer where light emission occurs.

are emitted.

LEDs are commercially available with wavelengths from ultraviolet to infrared and used in an ever-increasing range of applications. Some of these applications include display backlights, camera flash lighting, solid-state lighting, and water purification.

1.2.3 Metal Oxide Semiconductor Field Effect Transistors

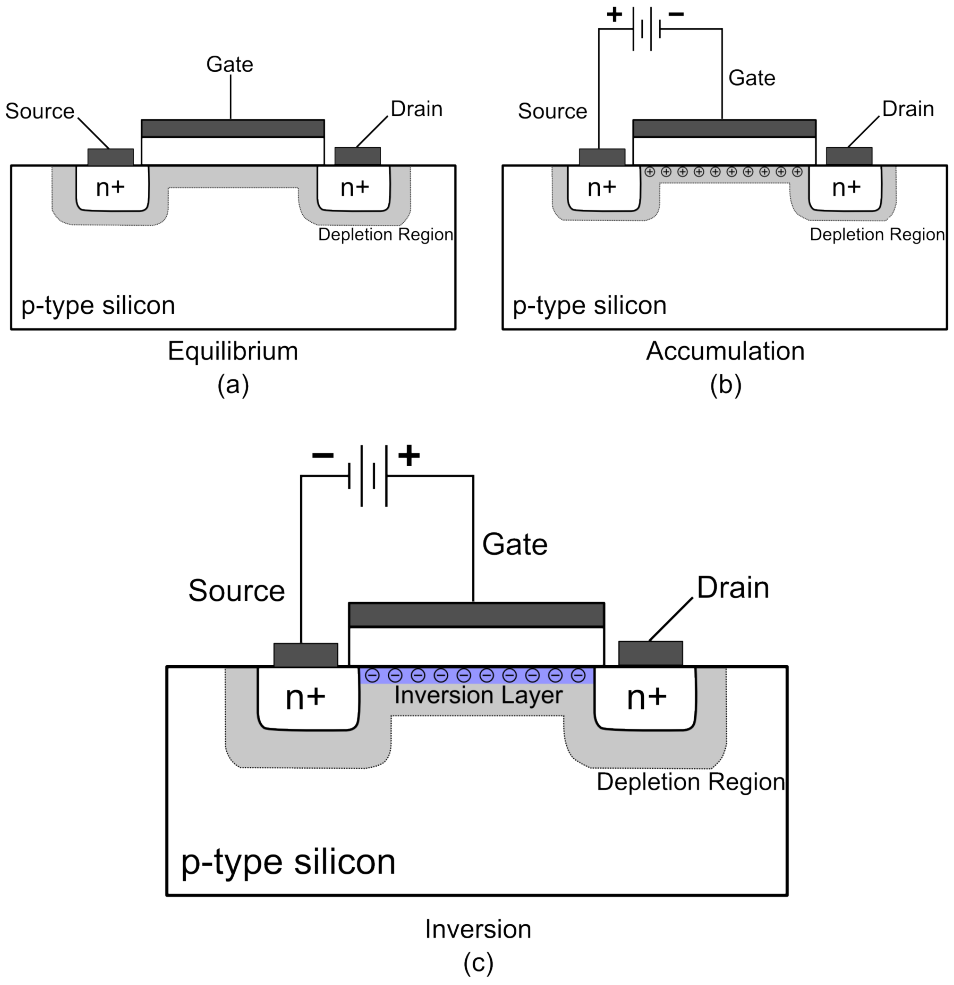


Figure 1.6: Standard n-channel MOSFET structure in (a) equilibrium, (b) accumulation when a negative gate bias is applied, and (c) inversion when a positive gate bias is applied.

Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) are the most ubiquitous electronic device, appearing in almost all electronics. In a standard n-channel MOSFET, fig. 1.6, the source and drain regions are heavily n-doped in a p-type semiconductor. Above the p-type channel region is a gate dielectric and gate metal. When the MOSFET is off, electrical conduction between the source and drain is blocked by the back-to-back p-n junctions. When a negative bais is applied to the gate, accumulation of holes occurs in the channel as these holes are attracted to the semiconductor/dielectric interface. Again, because of the back-to-back p-n junction, current cannot conduct between the source and drain even with this accumulated hole layer.

As a positive bias is applied, the depletion region underneath the channel expands, shown in fig. 1.6c. After a certain threshold voltage, an inversion layer of mobile electrons is formed in the channel. An electrical conduction path between the source and drain appears in this inversion scenario, and can be controlled with the bias at the gate.

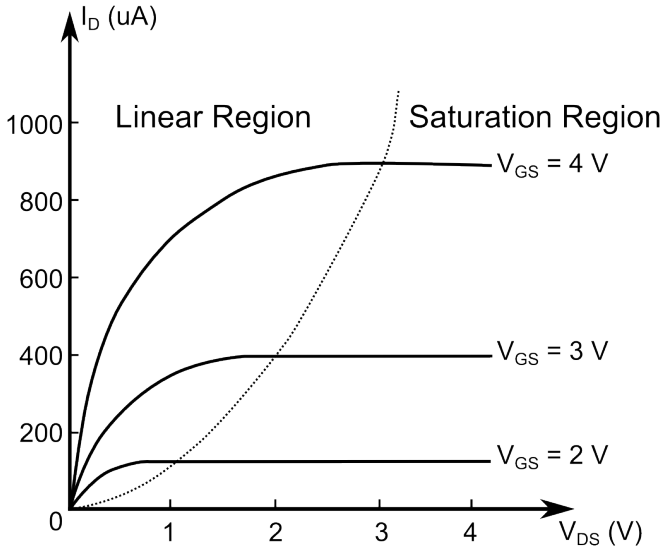


Figure 1.7: Typical current-voltage characteristics of an n-channel MOSFET. Adapted from reference [12]

At small biases between the source and drain, the current increases linearly with the applied voltage. In the linear region, the channel behaves similar to a resistor. As the bias increases between the source and drain, the channel on the drain side becomes smaller as the gate has less of an effect. Eventually, this reaches the saturation region of device operation where increases in source and drain bias do not change the current. Fig. 1.7 shows a typical n-channel MOSFET current-voltage characteristic with the regions of operation marked [12]. The source-drain current can be calculated with the equations below for the different regions.

Cutoff: $I_{DS} = 0$

when $(V_{GS} \leq V_{Tn})$

Linear: $I_{DS} = (W/L)\mu_n C_{ox}[V_{GS} - V_{Tn} - (V_{DS}/2)]V_{DS}$

when $(V_{GS} \geq V_{Tn}, V_{DS} \leq V_{GS} - V_{Tn})$

Saturation: $I_{DS} = (1/2)(W/L)\mu_n C_{ox}(V_{GS} - V_{Tn})^2$

when $(V_{GS} \geq V_{Tn}, V_{DS} \geq V_{GS} - V_{Tn})$

Similarly, p-channel devices can be fabricated by changing the substrate to n-type doping, and the source and drain contacts to heavily doped p-type material. The device operation voltages are then opposite. Instead of applying a positive voltage at the gate for inversion, a negative voltage past the threshold voltage is applied and the inverted, mobile charges are now holes. The regions of operation, linear and saturation, are similar for p-channel and n-channel, and the p-channel FET equations are given below.

Cutoff: $I_{SD} = 0$

when $(V_{SG} \leq |V_{Tp}|)$

Linear: $I_{SD} = (W/L)\mu_p C_{ox}[V_{SG} - |V_{Tp}| - (V_{SD}/2)]V_{SD}$

when $(V_{SG} \geq |V_{Tp}|, V_{SD} \leq V_{SG} - |V_{Tp}|)$

Saturation: $I_{SD} = (1/2)(W/L)\mu_p C_{ox}(V_{SG} - |V_{Tp}|)^2$

when $(V_{SG} \geq |V_{Tp}|, V_{SD} \geq V_{SG} - |V_{Tp}|)$

When both n-channel and p-channel devices are fabricated on the same substrate and used together in circuit designs, this is called Complementary Metal Oxide Semiconductor (CMOS) technology. MOSFETs and more specifically CMOS technologies appear in essentially all electronic devices and are the basic building block for digital circuits as switches and for analog circuits as amplifiers.

1.3 Objectives and Approach

This thesis focuses on monolithically-integrating normally process-incompatible materials to make systems with extended functionality. Reconciling the low process temperatures of certain materials with the necessity for high quality crystalline materials makes laser crystallization an attractive route towards this advanced integration. Chapter 2 discusses a specific laser crystallization method (sequential lateral solidification), the fabrication of high mobility thin film silicon transistors using this method, and characterization of these devices. Chapter 3 covers the fabrication of LED arrays, their potential uses in display and non-display applications, and their eventual integration with laser crystallized silicon transistors to form active-matrix circuits. Three dimensional integrated circuits, specifically the building and characterization of vertical diode devices, and the effects of laser crystallization on underlying devices are examined in chapter 4. Finally, chapter 5 discusses the application of laser annealing to other material systems, in particular sequential lateral solidification on low-κ dielectrics and its relevance to back-end three dimensional integrated circuits, and laser crystallization of copper for reduced wire resistivity.

Chapter 2

Sequential Lateral Solidification of Silicon for Thin Film Transistors

2.1 Introduction

Single crystal silicon is the predominant semiconductor material used in microelectronics due to its high performance and extensive optimization history. However, the methods of obtaining single crystals are limited; both the float-zone and Czochralski processes grow ingots from molten silicon. This poses a challenge to integration with other substrates if a single crystal silicon layer is desired on top of another material. What is needed is a method of growing the highest quality silicon possible without effect to the underlying substrate.

The use of laser energy as a means to crystallize amorphous silicon has long been established given the success in obtaining highly crystalline silicon through a low temperature process [14][15][16][17]. The laser energy can be adjusted to create partial melting conditions or fully melted amorphous films [18][19]. In partial melting, the laser melts only the top surface, leaving the lower material solid. The solid amorphous film then nucleates the crystallization, resulting in very small grains. In the complete melting regime, the laser fully melts the amorphous silicon film. Nucleation and

grain growth occur at random at the molten silicon/substrate interface, and again only produces small grains. In a narrow energy window between partial melting and complete melting is the regime called super lateral growth [18]. Here, the laser energy density is just below what is necessary for complete melting, and the scattered, non-molten, solid seeds at the bottom of the molten silicon film act as preferential nucleation sites, leading to larger grains upon cooling. Excimer Laser Annealing (ELA) takes advantage of this regime and offers fairly large crystal sizes and electron mobilities of approximately 100 cm^2/Vs, but relies on this non-equilibrium process and narrow energy density window.

Sequential Lateral Solidification (SLS) is a laser crystallization method which operates in the complete melting regime where process tolerances are much larger, and at the same time can produce large grains of polycrystalline silicon with electron mobilities up to 500 cm^2/Vs.

2.2 Sequential Lateral Solidification Methods

Sequential Lateral Solidification (SLS) is a pulsed-laser crystallization method which combines laser irradiation through a patterned mask with precise submicrometer translations of a sample stage [21][22][23]. The shape of the laser irradiation is controlled by a reticle in the beam path and affects the microstructural quality of the laser-crystallized material. Three popular types of SLS are two-shot SLS, line-scan SLS, and dot-SLS. Of the three, two-shot SLS makes polycrystalline silicon material with the lowest mobility, but covers a large area with two laser shots versus the thousands of laser shots required for other laser annealing methods [24][25]. Line-scan SLS produces material with high mobility in a directional manner, and transistors with channels in the correct orientation have much higher mobilities [26][27][28]. Dot-SLS makes an area of nearly single crystal material with electron mobilities above what is achievable by line-scan SLS [29]. However, with dot-SLS, only the single crystal

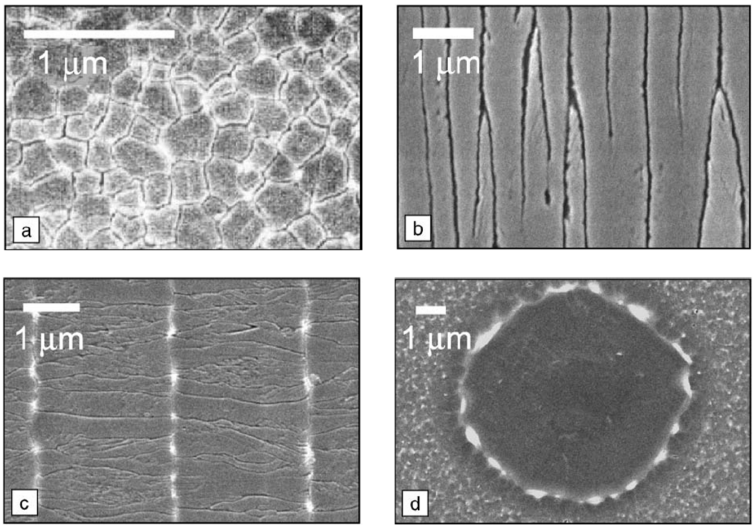


Figure 2.1: Scanning electron micrographs of defect-etched samples following laser annealing. (a) Excimer Laser Annealing method. (b) Line-Scan SLS. (c) Two-Shot SLS. (d) Dot SLS. [20]

regions in the total area are useful. The resulting materials obtained from these methods are compared in fig. 2.1 where the scanning electron microscope images show the relative microstructures [25]. For electronic devices, electron mobility is an important characteristic of a material and can be partially determined from the microstructure quality, fig. 2.2 [30]. For comparison, the mobility of amorphous silicon devices is approximately 1 cm^2/Vs, and devices fabricated with excimer laser annealing have mobilities of approximately 100 cm^2/Vs.

Line-scan SLS offers the best option in advanced integration work since it produces a uniform, high mobility material over a large area. Fig. 2.3 shows the process flow for line-scan SLS. The process begins with a thin-film of amorphous silicon which is then irradiated with a long and thin laser beam. This 30-300 ns beam is typically 2-3 μm wide and can be as long as 1 meter. The exposed amorphous silicon is fully melted into a liquid state and allowed to cool. As the cooling proceeds, the interfaces to the liquid region cool faster and thus crystallize first. The grains nucleate from

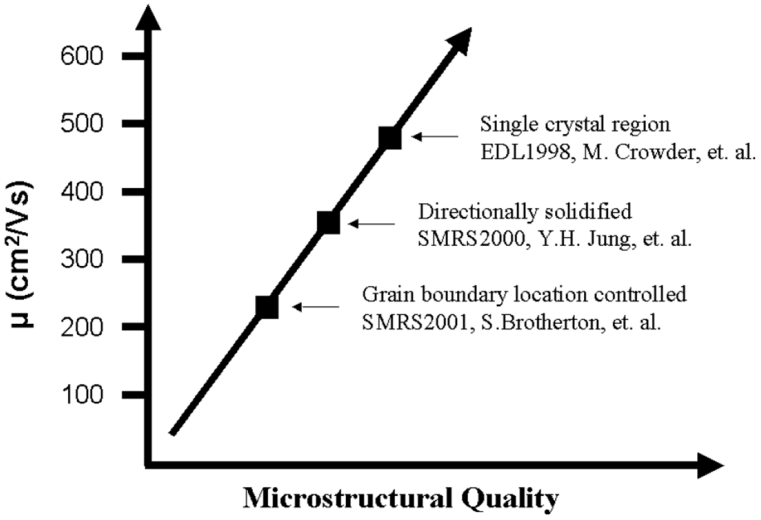


Figure 2.2: Electron mobilities of materials prepared with different SLS methods. Grain boundary location controlled, or Two-Shot SLS. Directionally Solidified, or Line-Scan SLS. Single Crystal Region, or Dot SLS. [30]

the edges and grow to meet in the middle, fig. 2.3, step 3. There is now a small area of polycrystalline silicon. The sample stage is then translated less than half the laser width, and the sample is exposed to a second laser pulse. This time, the laser melts half of the polycrystalline silicon formed in the first step, and half of the original amorphous silicon film. As the newly formed liquid area cools, grains are again seeded from the solid edges. Because this region overlaps with the previous laser pulse, one edge of the liquid area seeds directly from the polycrystalline silicon, fig. 2.3, step 5. The crystals grow preferentially in the direction of the stage translation, forming elongated grains, fig. 2.3, step 6. This process repeats until the whole area has been transformed from amorphous silicon to polycrystalline silicon. Fig. 2.4 and 2.5 show line-scan SLS material before and after a grain boundary defect etch to highlight the grain boundaries. Fig. 2.6, a transmission electron micrograph, shows the directional elongation of the grains.

Another important aspect of laser crystallization is the refractory layer, placed be-

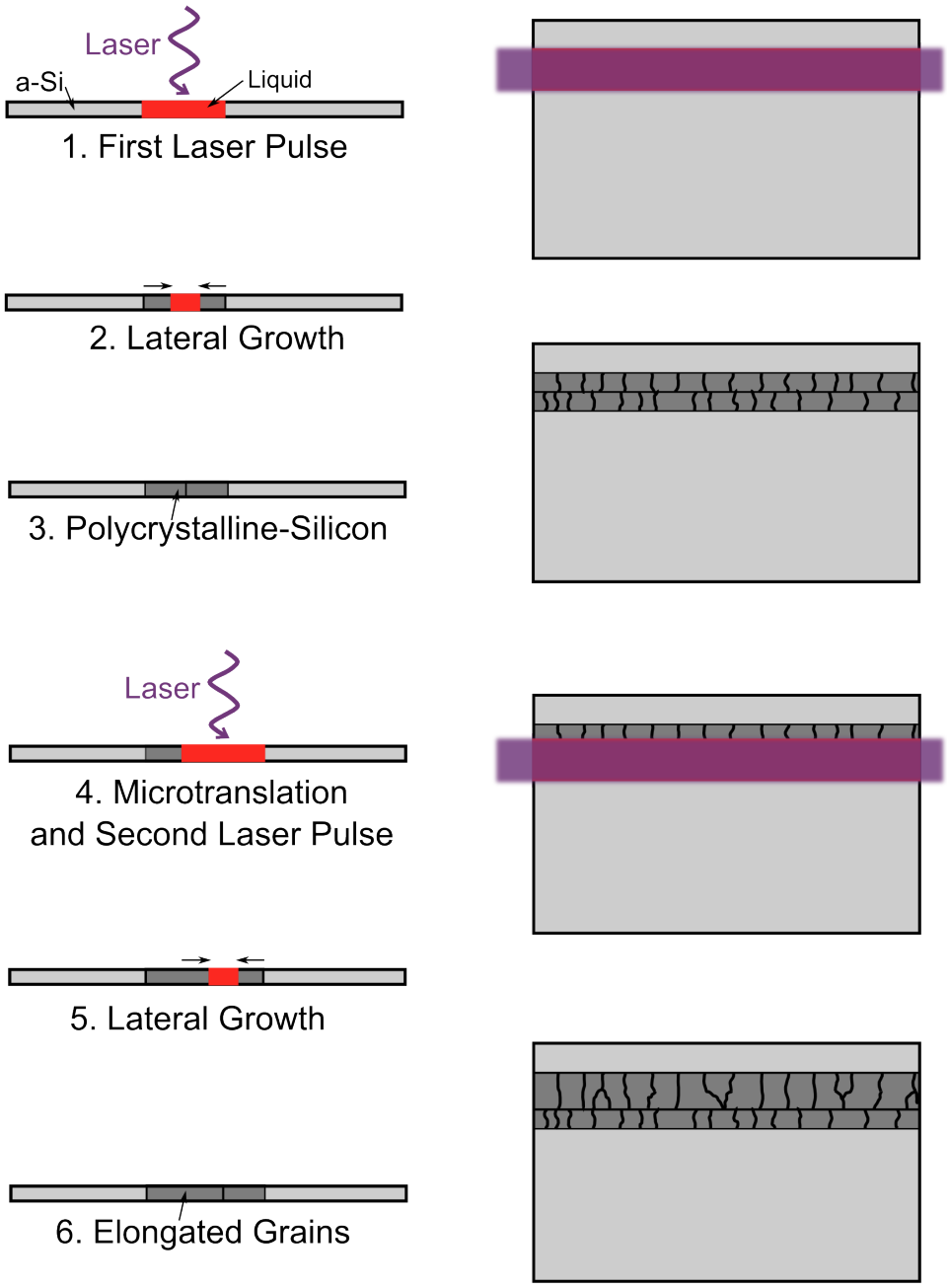


Figure 2.3: Cross section (left column) and top view (right column) of line-scan sequential lateral solidification (SLS) process flow.

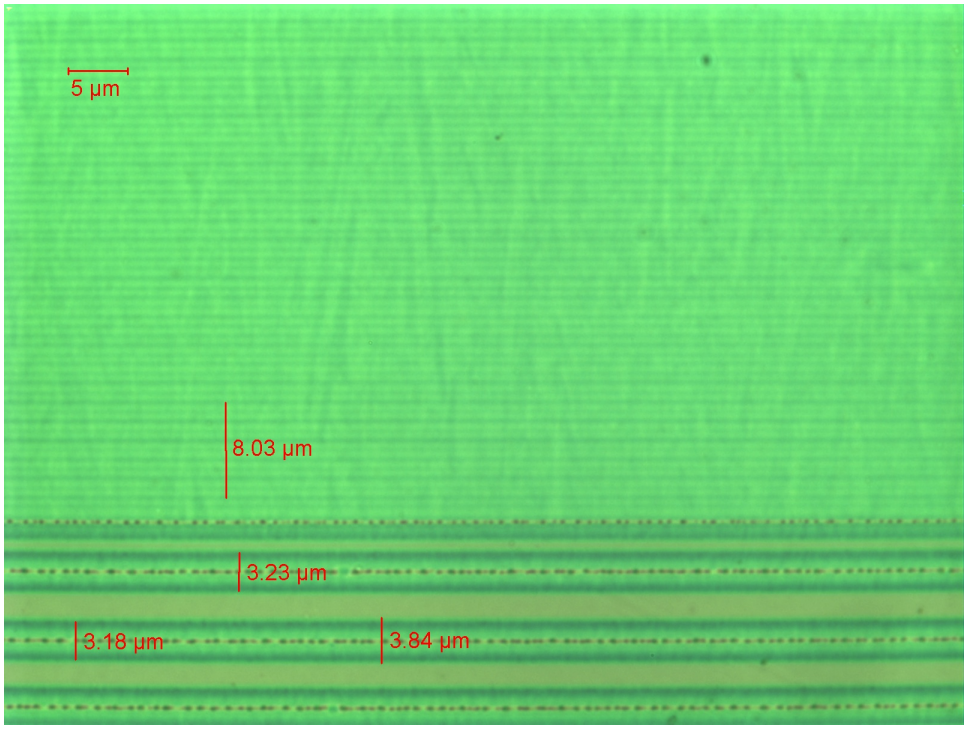


Figure 2.4: Micrograph of line-scan SLS method. Bottom of micrograph shows a single laser beam with a width of around 3.5 μm. Top of micrograph shows typical Line-Scan SLS material.

tween the substrate and laser crystallization layer. This refractory layer can withstand the heat of the molten top film and buffers the heat from the underlying substrate, fig 2.7. Typically 500 nm to 1 μm of silicon dioxide is used to protect the substrate and keep it cool throughout the laser process.

2.3 Laser Crystallization Simulations

Sequential lateral solidification becomes particularly interesting when applied to a stack of multiple materials such as silicon on top of a III-V substrate. In order to use SLS on silicon with lower temperature substrates, the bottom layers must stay cool enough to maintain their properties and avoid damage of the substrate. SLS on

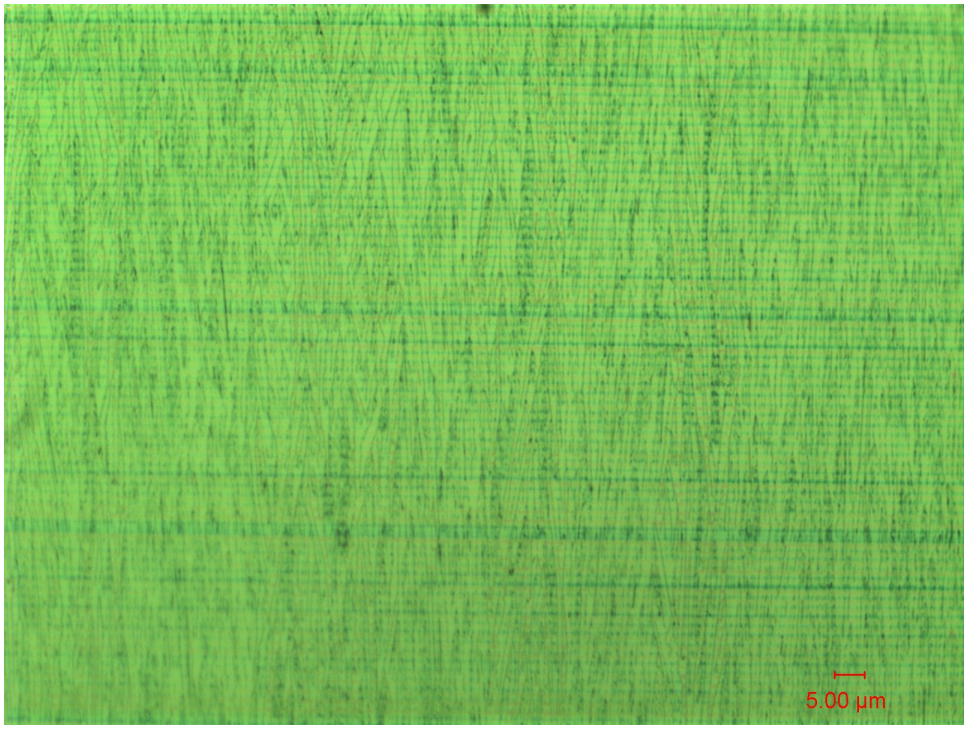


Figure 2.5: Micrograph of line-scan SLS method after a 5 second SECCO defect etch to highlight grain boundaries.

silicon is currently commercialized for glass substrates which can support up to 600°C [31][32][33], and laser processes have also been demonstrated on a variety of substrates including polymers which have a temperature limit of only 150-200°C [34][35][36].

Simulations of the laser process were performed using a finite-difference model method [37]. The simulated structure, shown in fig. 2.8, contains 1 μm of silicon dioxide and 100 nm of amorphous silicon. The two planes of interest are the surface temperature at the very top of the amorphous silicon, and the interface temperature between the SiO_2 buffer and the underlying substrate. As discussed in later chapters, the underlying substrate, containing devices such as III-V LEDs or and completed front-end CMOS transistors, cannot withstand high temperature processing.

The simulation begins with a 308nm laser pulse with 30 ns pulse duration starting at time = 0 seconds. The results of this simulation are shown in fig. 2.9, 2.10 and

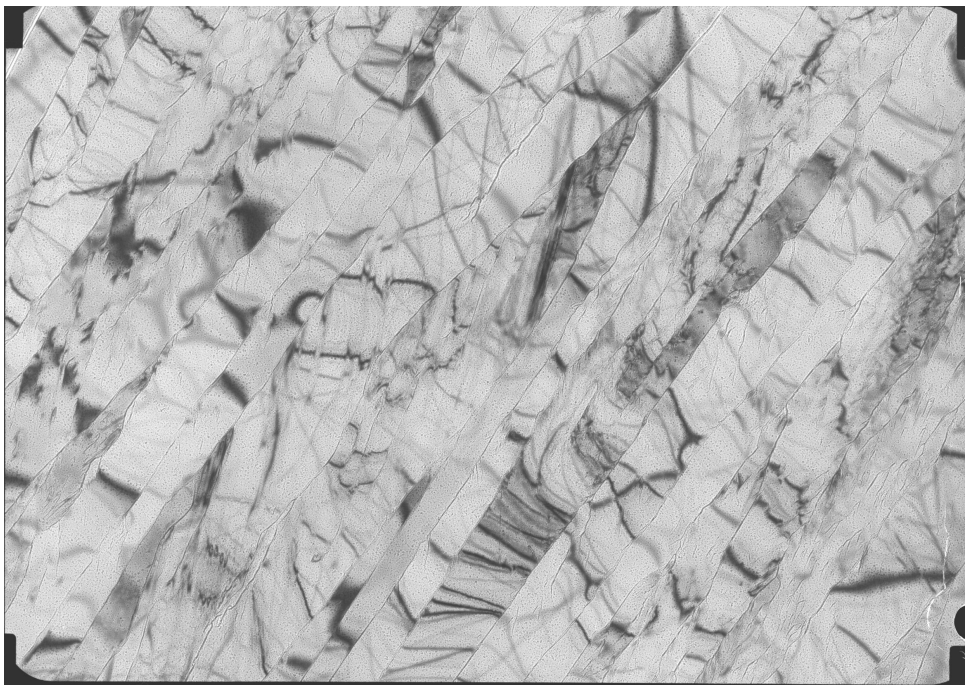


Figure 2.6: Transmission electron micrograph of high aspect ratio grains in a typical line-scan SLS material. Total size of the micrograph is 9.89 μm x 6.95 μm.

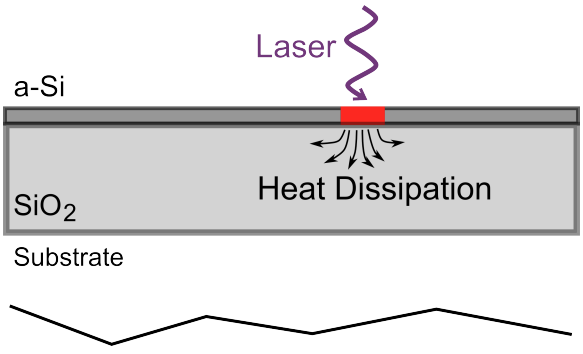


Figure 2.7: Schematic cross section showing the importance of the buffer layer between the laser-crystallized film and the substrate for heat dissipation.

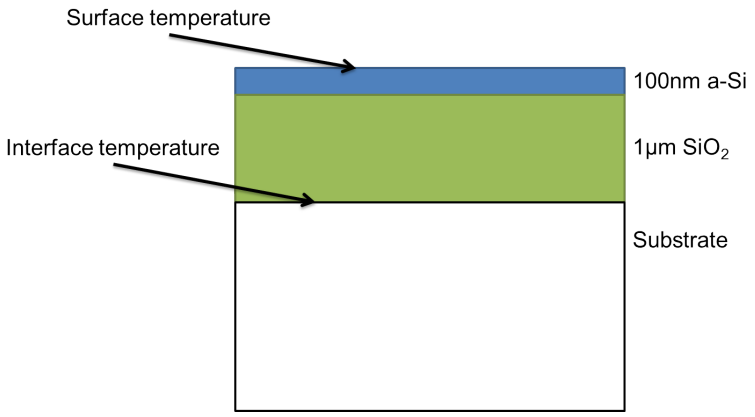


Figure 2.8: Simulated structure of 100 nm of silicon on top of 1 μm of silicon dioxide. Schematic points to the two points of interest: the surface temperature and the interface temperature between the SiO_2 buffer and the underlying substrate.

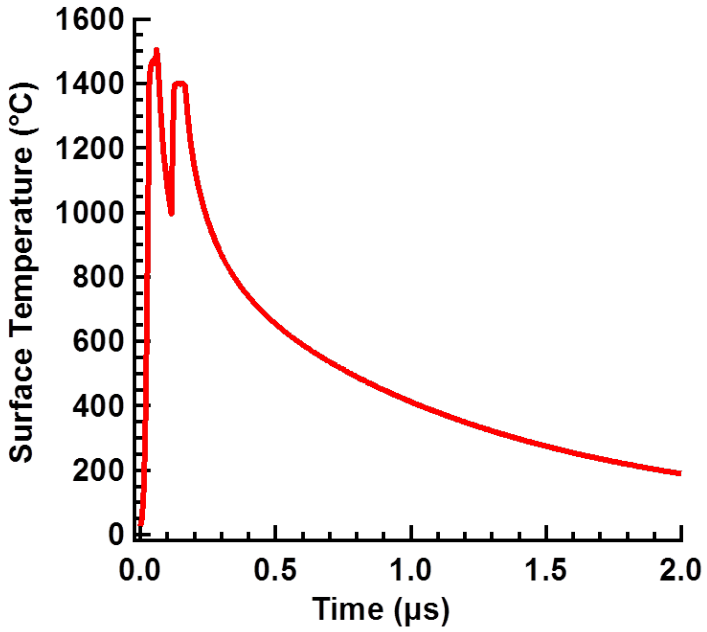


Figure 2.9: Surface temperature of silicon film during laser processing. Temperature quickly reaches the silicon melt temperature and cools to below 200°C after 2 μs.

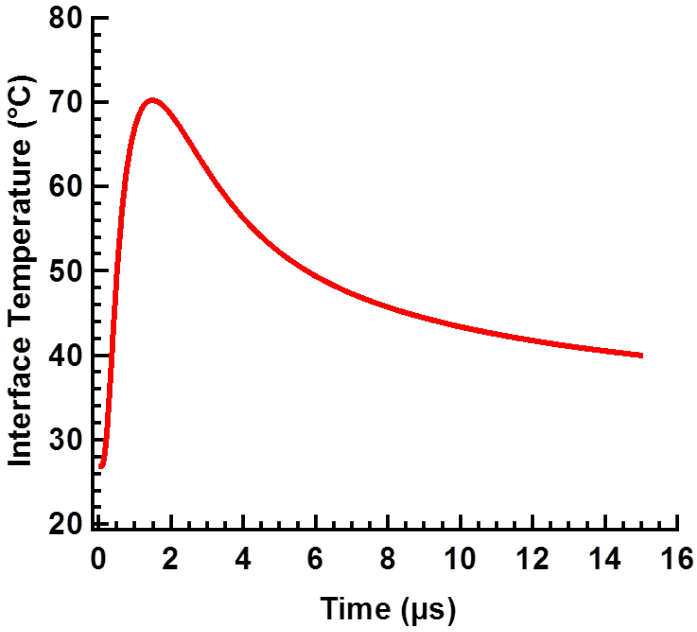


Figure 2.10: Interface temperature between SiO_2 and substrate. The substrate sees a maximum temperature of 70°C during the entire crystallization process.

2.11. As expected at the surface, fig. 2.9, the silicon film reaches its melting point very quickly when exposed to the laser. At a wavelength of 308nm, 99.995% of the laser energy is absorbed by the 100 nm of silicon [38][39]. This prevents the laser from heating the substrate and prevents ultraviolet exposure of the substrate. This also implies that the substrate is only heated by diffusive heat energy through the buffer layer from the molten silicon. The film then cools; the second observed increase in temperature, just before 2 μs can be attributed to the release in latent heat as the film solidifies from liquid to solid. After solidification, the surface cools very quickly and reaches 200°C after 2 μs.

The simulated interface temperature, shown in fig. 2.10, reaches a maximum of 70°C at around 1.5 μs. This is the maximum temperature that the substrate encounters during the laser crystallization process. Again, the materials cool exponentially and reach about 40°C by 15 μs. Experimentally, the laser is pulsed at 100 Hz, or 10

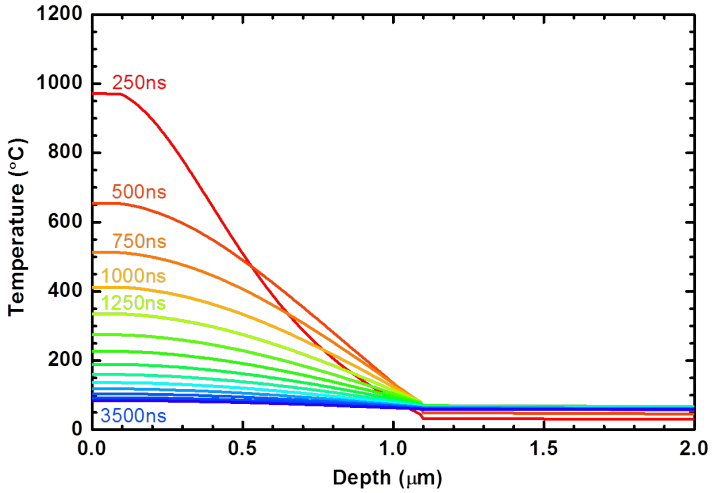


Figure 2.11: Temperature profile of simulated sample up to 3500 ns during laser processing. Most of the heat used to melt the amorphous-Si is dissipated in the SiO_2 buffer layer before it reaches the substrate below.

ms. This gives the substrate ample time to return to room temperature before the subsequent laser pulse. In industrial systems, laser pulses are around 5000 Hz, or 200 μs, again enough time for the substrate to cool back to room temperature between laser pulses.

2.4 Thin Film Transistors using Sequential Lateral Solidification

2.4.1 Fabrication of TFTs

The thin film transistor fabrication process begins with an electron beam deposition of 1 μm of SiO_2 and 100 nm of Si. The deposition chamber has a base pressure of 10^{-7} torr to ensure low gas incorporation and the substrate is held at 400°C during

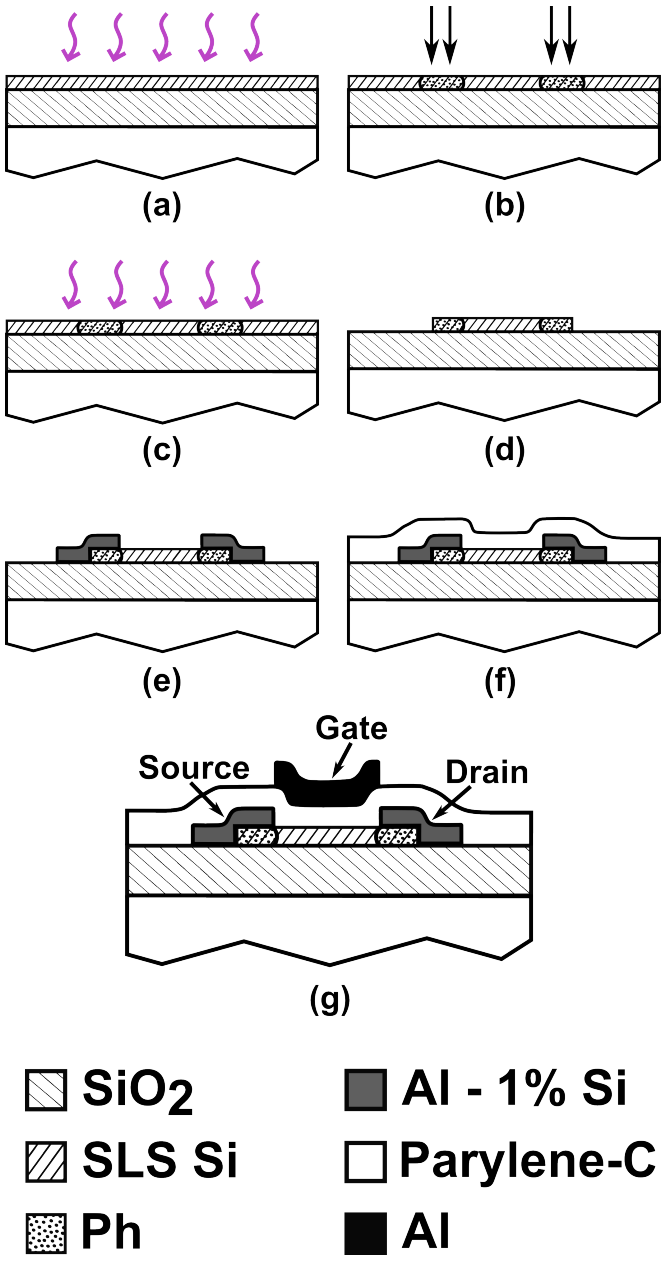


Figure 2.12: Process flow for fabrication of lateral thin film transistors. (a) Laser crystallization of amorphous silicon. (b) Ion implantation for source and drain electrodes. (c) Activation of ion implanted dopants. (d) Definition of silicon active area. (e) Deposition of source and drain electrodes. (f) Deposition of gate dielectric. (g) Deposition of gate metal for completed transistor device.

deposition for improved film quality. Next, line-scan sequential lateral solidification (SLS) laser processing is performed with a 308 nm XeCl excimer laser, fig. 2.12a. In the experimental setup, the laser beam is 6 cm x 1.5 μm, with energies above $300mJ/cm^2$ for complete melting. Each translation of the stage is half the width of the beam, or 0.75 μm. This allows the melted silicon to seed crystal growth from the grains grown in the previous pulse. More information on the line-scan SLS process can be found above and in Sposili, et.al. [21]

Select areas are ion implanted with 1x10^{15} cm^{-2} of phosphorus at 10 keV to form contact areas for the source and drain, fig. 2.12b. These dopants are then activated with a 1000°C, 2 second, rapid thermal annealing process to ensure all implanted dopants are activated, fig. 2.12c. The silicon active areas are then patterned and etched with a SF_6 plasma, fig. 2.12d. Aluminum source and drain contacts are thermally evaporated and patterned using a lift-off process, fig. 2.12e. Contacts are then annealed at 350°C in argon for 1 hour. A 200 nm film of parylene-C is used as a gate dielectric, fig. 2.12f, and finally an aluminum gate metal is evaporated and patterned, fig. 2.12g. A micrograph of the completed devices is shown in fig. 2.13.

2.4.2 Characterization of TFTs

With line-scan SLS, grain growth propagates in the direction of the sample stage translation, and thus transistor characteristics are dependent on the orientation of the transistor channel with respect to the grain boundaries. The two extremes are tested, one where the grain boundaries are parallel to the channel conduction path, and the second where the grain boundaries are perpendicular to the conduction path. All electrical tests are performed on an Agilent 4155C semiconductor analyzer.

Fig. 2.14 and 2.15 show current-voltage characteristics for two SLS transistors of different sizes with grain boundaries parallel to the direction of current conduction. The extracted mobility for these two devices is approximately 400 cm^2/Vs to 450 cm^2/Vs. These mobility numbers agree with results in the literature for devices

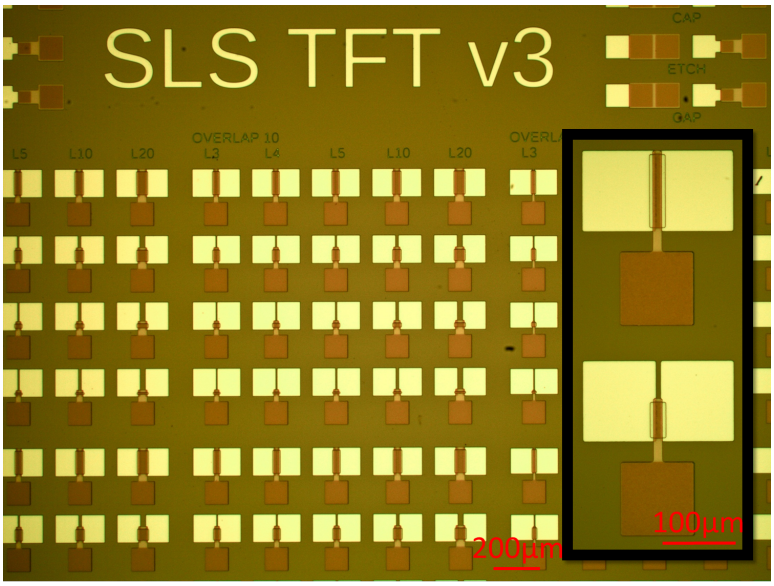


Figure 2.13: Micrograph of completed thin film silicon transistors.

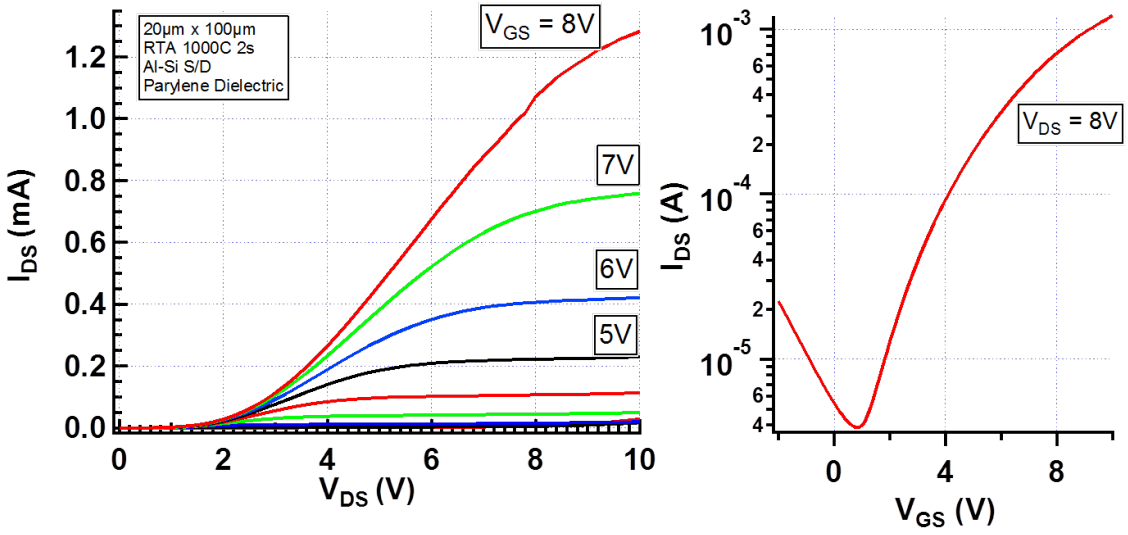


Figure 2.14: Drain current vs drain voltage (I_{DS} vs. V_{DS}) and transfer characteristics (I_{DS} vs. V_{GS}) of SLS TFT device with grain boundaries parallel to conduction channel. Device length and width is 20 μm x 100 μm.

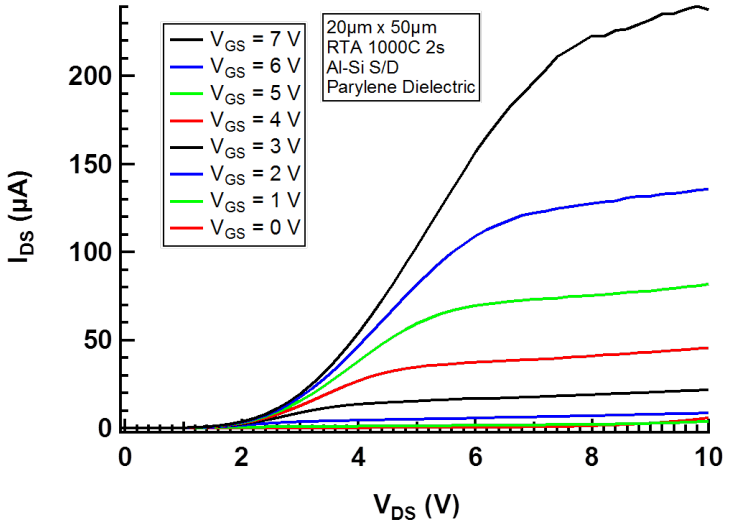


Figure 2.15: Drain current vs drain voltage (I_{DS} vs. V_{DS}) of SLS TFT device with grain boundaries parallel to channel. Device length and width is 20 μm x 50 μm.

made from this type of sequential lateral solidification.

Fig. 2.16 shows the current-voltage characteristics for an SLS transistor with the grain boundaries perpendicular to the direction of current conduction. In this case, there are many grain boundaries between the source and drain which results in lower current levels [40]. The extracted mobility for this transistor with perpendicular grain boundaries is about 180 cm^2/Vs, about 2.5 times lower than the mobility in the parallel case.

Even though the ion implant dose is designed to produce highly doped ohmic contacts, it is clear from the electrical characteristics of all devices that the contact resistance is much higher than expected. Van der Pauw measurement structures are fabricated to investigate the effectiveness of the source and drain doping to correct this problem.

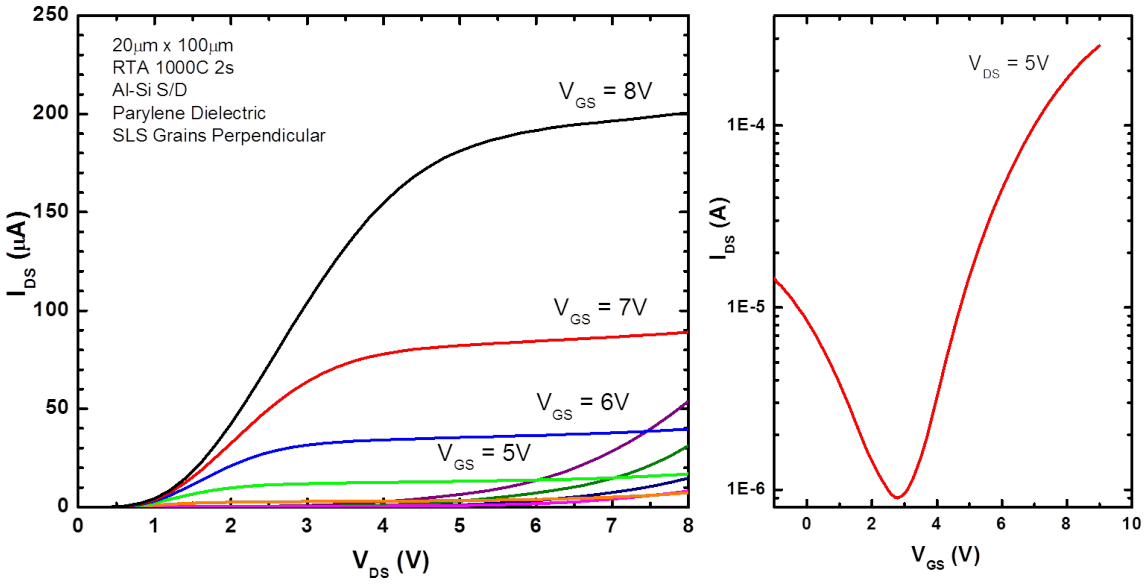


Figure 2.16: Drain current vs drain voltage (I_{DS} vs. V_{DS}) and transfer characteristics (I_{DS} vs. V_{GS}) of SLS TFT device with grain boundaries perpendicular to channel. Device length and width is 20 μm x 100 μm.

2.4.3 Van der Pauw Sheet Resistance

The van der Pauw method takes measurements on an arbitrarily-sized square of semiconductor material that is electrically contacted at the four corners. Fig. 2.17a shows a micrograph of this structure and 2.17b provides a labeled schematic. The designed van der Pauw test uses a 150 μm x 150 μm square of doped semiconductor with four 100 μm x 100 μm metal pads in each of the four corners. To perform the measurement, an electrical current is pushed between contacts 1 and 2, and voltage is measured between contacts 3 and 4. Next, a current is pushed between contacts 3 and 4, and voltage is measured between contacts 1 and 2. This is repeated for the six other combinations and the sheet resistance is calculated based on the equations below.

$$R_{12,34} = V_{34}/I_{12}$$

$$R_{34,12} = V_{12}/I_{34}$$

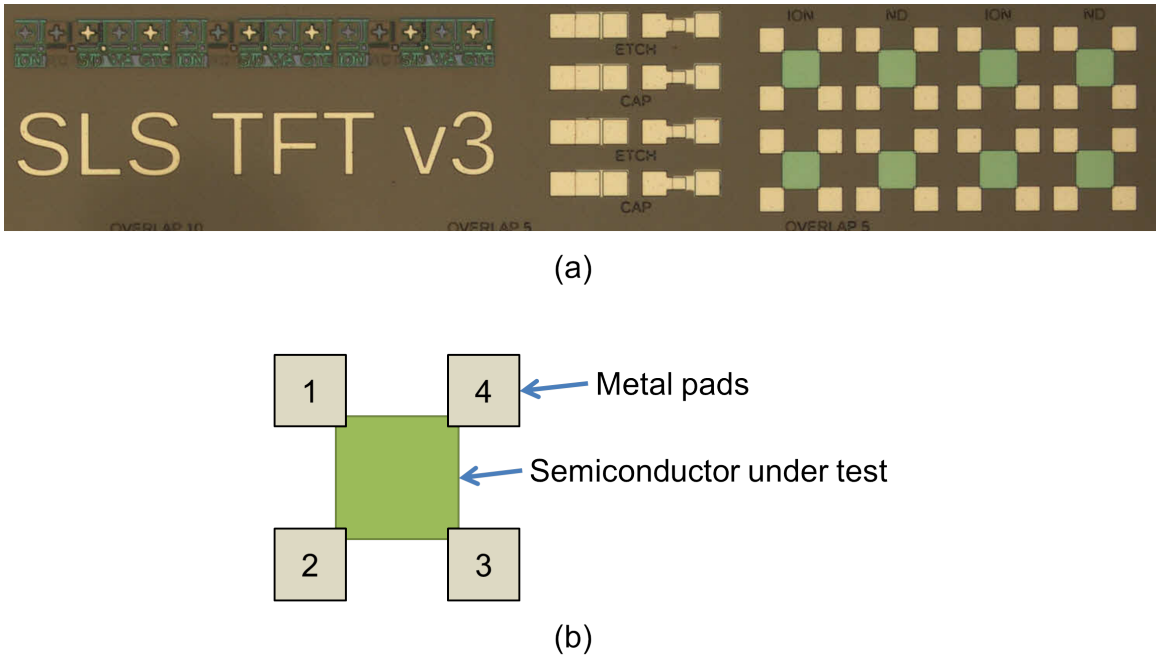


Figure 2.17: (a) Micrograph of test structures incorporated on SLS TFT samples including alignment marks, capacitance test structures, via etch test structures, and van der Pauw test structures. (b) Schematic of van der Pauw test structure showing the placement and numbering of the four metal pads.

$$R_{vert} = (R_{12,34} + R_{34,12} + R_{21,43} + R_{43,21})/4$$
$$R_{horiz} = (R_{23,41} + R_{41,23} + R_{32,14} + R_{14,32})/4$$

When $R_{vert} = R_{horiz} = R$

$$R_s = \pi R/ln(2)$$

A low-temperature method can improve the contact resistance and serve as an alternative to the high temperature rapid thermal anneal (RTA). Past work has shown laser activation [41][42][43][44] and flash lamp annealing [45][46][47][48] as viable methods for dopant activation.

In this work, a non-melt laser process is developed for activating the implanted dopants, fig. 2.12c. The laser energy is set just below the melting point for polycrys-

Table 2.1: Van der Pauw Sheet Resistance Data (Ohms/Square)

Implant Dose (cm^{-2})	**Activation Method**	**Sheet Resistance Along Grains**	**Sheet Resistance Perpendicular to Grains**
10^{15}	RTA	104	632
10^{15}	Laser 15X	150	250
10^{15}	Laser 30X	120	280
10^{15}	Laser 45X	132	263
10^{16}	RTA	140	332
10^{16}	Laser 10X	72	126
10^{16}	Laser 20X	64	117

talline silicon, but causes explosive crystallization for amorphous silicon. In this case, the surface temperature reaches approximately 1300°C. Each area is irradiated between 15-45 times with the pulsed laser to allow the dopants enough time to activate with minimal diffusion. Each of these laser-pulsed samples is then measured using the van der Pauw method to obtain the sheet resistance and the relative amount of activation, and the properties are compared against those of samples prepared with rapid thermal annealing. Results are summarized in table 2.1.

Using the van der Pauw measurement, expected improvements in the sheet resistance are observed as the ion implant dose is increased, and significant improvements in sheet resistance are realized when switching from RTA activation to a non-melt laser activation. The modified process with a higher ion implant dose of 10^{16} cm^{-2} and a non-melt laser activation step with 20 pulses per area is expected to improve transistor characteristics.

2.5 Conclusions

Sequential lateral solidification is a process that creates high quality silicon at low process temperatures. Simulations of the desired device structure show that even as the top layer of amorphous silicon melts, the underlying substrate stays below 70°C. Further, a transistor process is developed to fabricate lateral devices with mobilities above 400 cm^2/Vs along a conduction path parallel to the SLS-induced grain boundaries. These transistors suffer from problems with contact resistance, which is investigated with the van der Pauw method and improved with a non-melt laser dopant activation method. Overall, a thin film of high-mobility silicon transistors was fabricated at temperatures below 400°C in a process compatible with low-temperature compound semiconductors and back-end-of-line silicon substrates.

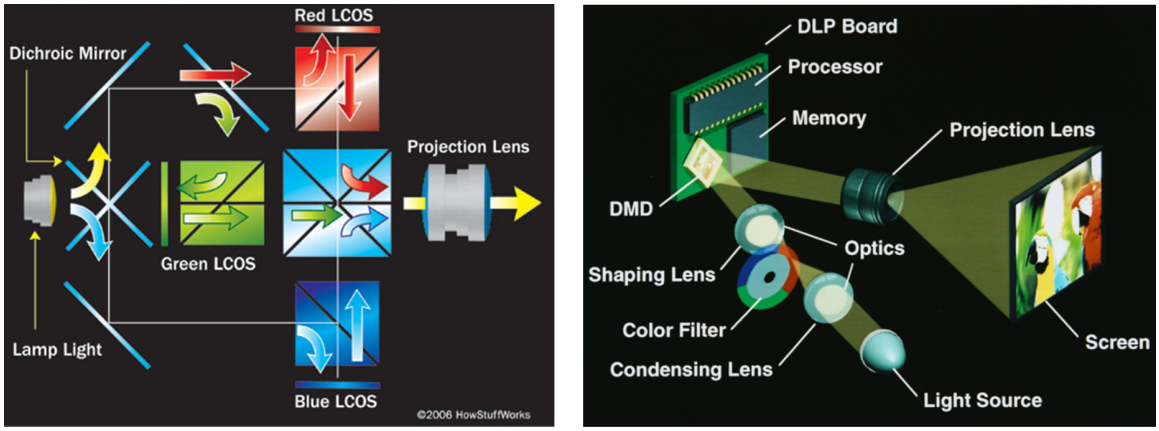
Chapter 3

Light Emitting Diode Array

3.1 Introduction

Light emitting diodes (LEDs) have luminous efficiencies that surpass virtually all other light sources [49]. Consequentially, discrete LEDs have been applied to a range of applications in which non-structured illumination is required, such as solid-state lighting [50] and display backlights [51][52][53]. Today, the majority of commercial applications for LEDs do not require patterning at a chip level. However, some applications, such as outdoor billboards or LCD-TV backlights, use discrete LEDs as the light source as well as the image source by stringing together rows and columns of discrete LEDs to create an image. The objective is to photolithographically pattern the LEDs on the wafer level to achieve high resolution structured light sources in the microscale for use as a microdisplay platform.

Monolithically patterned LED arrays have been demonstrated for several applications including microdisplays [54][55][56][57][58][59][60], fluorescence detection [61], directly powered high voltage AC solid state lighting [62][54][63], mask-free lithography [64], other display concepts [65][66], and biomedical applications [67]. The LED arrays fabricated by Gong et al. have been demonstrated in the visible and ultraviolet wavelengths in form factors up to 64 x 64 pixels in a passively addressed



(a) (b)

Figure 3.1: Light path of typical projection systems. (a) Liquid crystal on silicon based system. (b) Digital micromirror based system

scheme, and up to 32 x 32 pixels in a flip-chip bonded actively addressed scheme [61]. A representative blue device from Gong et al. has a maximum power density of 43 W/cm^2 at a current density of 4000 A/cm^2. Combining the high brightness of LEDs and the ability to pattern them into dense arrays enables opportunities in a variety of display applications (microdisplays, head-mounted displays, head-up displays, pico projectors, and projectors) and non-display applications (real-time three dimensional scanning, depth mapping, three-dimensional printing, and new user interfaces).

Projection displays are a good example of where LED arrays can be used as both the light and image source. Modern projection systems, fig. 3.1, typically have three parts: a light source, a spatial light modulator (SLM), and a system of projection lenses. The spatial light modulator rejects light from regions of the image which are intended to be dark, structuring the light into the desired pattern. This light rejection reduces the overall system efficiency; the light source operates at full intensity at all times, regardless of the image being projected.

In larger projectors, the light source is typically a high intensity discharge (HID)

lamp, which is able to provide the high illuminance required. HID lamps have also been used in smaller projectors, but recent improvements in LED brightness and efficiency has allowed the use of three high power LEDs (red, green, and blue) as the light source. The higher efficiency, smaller size, and sequential color selectivity of LEDs has enabled the development of more efficient smaller projectors and pico-projectors. A liquid crystal display (LCD), digital micromirror device (DMD), or liquid crystal on silicon (LCoS) engine typically provides the light modulation and either transmits or rejects light for a given pixel. The varying degrees of light blocking and time modulation allow for grayscale and also defines the contrast ratio. The modulated light is then projected through a series of lenses to reimage the SLM onto a screen.

As an alternative to these traditional projection systems, we demonstrate the use of structured LED arrays as both the light source and image generator, in which each individual LED serves as a pixel. Through monolithic integration, we can fabricate a dense, high resolution LED array to serve as our image source. Light is then generated by individual LEDs in the array only when and where it is needed for the image. This results in less wasted light and higher energy efficiency. An additional advantage of LED arrays compared to current projection technologies is the elimination of color filters and polarizing optics. This can increase the overall light path efficiency by up to 300%. Finally, by physically combining the light source and image generator into one component, the total number of system components is significantly reduced, shrinking the overall form factor and allowing for even smaller projectors.

Grossmann et al. has proposed the use of organic LED (OLED) displays as a projection light source [68][69]. Using OLED displays offers many of the same advantages as LED arrays, including increased contrast and higher system efficiency versus traditional spatial light modulator based systems. Organic LED systems have a unique ability to display full color on one substrate. However, they cannot compete with inorganic LEDs on luminous efficiencies and peak brightness. State-of-the-art

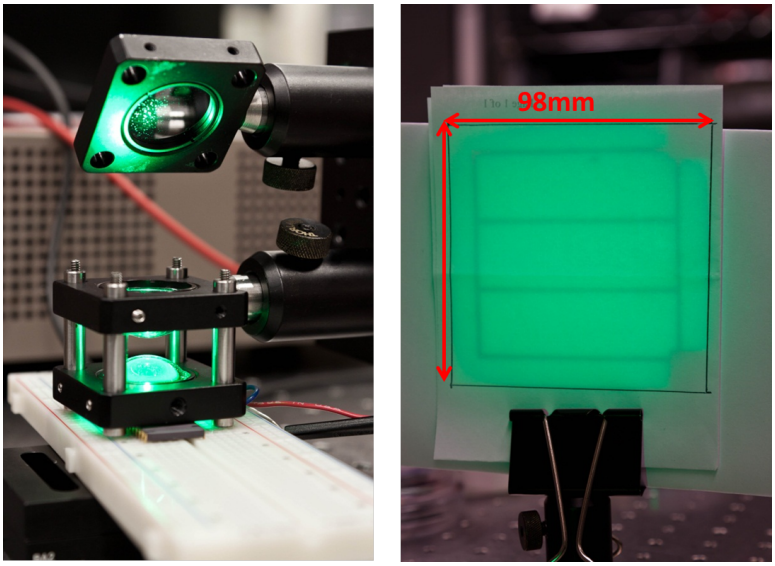


Figure 3.2: Cree EZ1000 LED in a projection format. Left: Simple two optic magnifying setup. Right: Projected image with 100X linear magnification, easily viewable in ambient light.

OLED devices have a brightness up to 6,000 cd/m^2 whereas state-of-the-art compound semiconductor LED devices can have brightnesses above 20,000,000 cd/m^2.

This chapter describes the fabrication, characterization, and advantages of inorganic, compound semiconductor based LED arrays.

3.2 Design

Advances in heatsinking and device design have allowed the development of large area, high drive power LEDs capable of both high efficiency and high luminance. Based on the brightness levels achieved by commercial discrete LEDs, we can estimate the viability of using LED pixels as a projection source can be estimated. Cree's XLamp has a current density of 35 A/cm^2 and a luminous intensity of 17.2 cd in a 980 μm x 980 μm emissive area, which corresponds to a brightness of 17,000,000 cd/m^2 [70]. Assuming an array of pixels with a 15 μm x 15 μm pitch and a 50% fill factor, it is

possible to make a 1920 x 1080 array in an area of 29 mm x 16 mm. Given a source brightness of 17,000,000 cd/m^2, an image can be magnified by 120X and achieve a projected display size of 13 feet with a brightness of 500 cd/m^2.

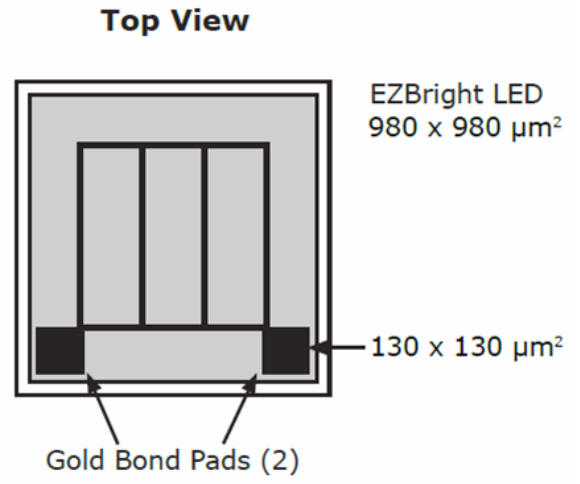


Figure 3.3: Drawing of Cree EZ1000 LED. Bond pad structure and LED size shown. [70]

Fig. 3.2 shows the use of a Cree EZ1000 LED in a projection format. The LED is wirebonded onto a package and placed in front of a simple two optic magnifying setup. This setup re-focus the LED features shown in the data sheet, fig. 3.3 left, obtaining a linear magnification of 100X, fig. 3.2 right.

The spectrum of the Cree Green EZ1000 is shown in fig. 3.4, with a peak wavelength of 520 nm. Optical power was measured with a calibrated Newport 818-UV silicon photodetector approximately 2 mm from the device to obtain the optical power density at the source, and later measured at the projected image to obtain the optical power density of the projection. Fig. 3.5 shows the optical power density both at the source and magnified 100X. Because the magnification is 100X, the optical power density decreases by 10000X. The optical coupling loss is approximately 10X due to the optics setup.

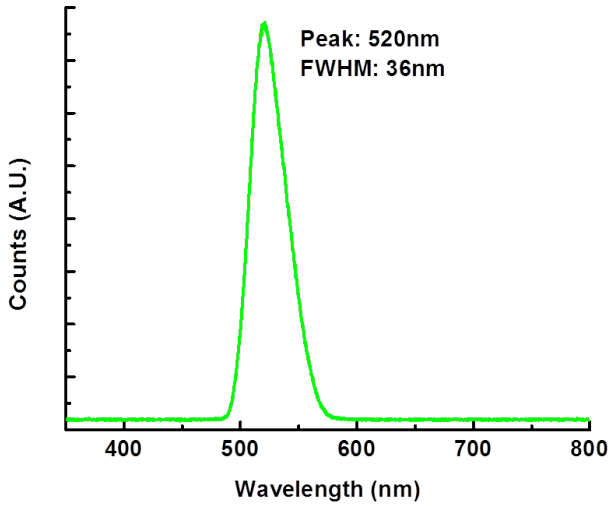


Figure 3.4: Spectrum of Cree Green EZ1000 with a peak wavelength of 520nm.

3.3 Fabrication

The LED array fabrication process starts with a commercially obtained GaAs wafer from Bandwidth Semiconductor with the epitaxially grown layers shown in Table 3.1. The design is the same as used by Kim et al. [71][72]. A semi-insulating AlAs layer of 1500 nm is grown on a 10^{18} cm^{-3} n-doped GaAs wafer. Next, a 100 nm p+ GaAs layer is grown to serve as a current spreading layer for the LED stack. The next layer of 2500 nm, 10^{18} cm^{-3} p-type doped AlGaAs serves as the p-confinement and p-contact. This p-type AlGaAs layer has ample thickness to allow for process tolerances when etching the mesa structure to define the LED. The n-confinement is provided by the 700 nm of 10^{18} cm^{-3} n-type AlGaAs layer which is above the undoped AlGaAs active layer. A 100 nm n+ GaAs layer provides the required current spreading and a good ohmic contact to subsequent metal depositions.

The fabrication was performed using a five mask process. The top and cross section views are shown in fig. 3.6 and 3.7. The first mask pattern (Etch 1) defines

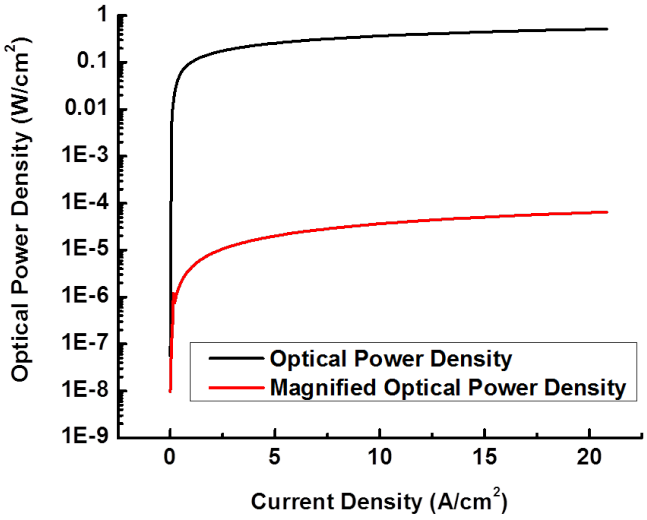


Figure 3.5: Optical power density of the source LED and optical power density of 100X magnified LED image.

Table 3.1: LED Layer Structure

Layer	**Thickness (nm)**	**Type and Concentration (cm^{-3})**
GaAs	100	N+ 10^{19}
$Al_{0.4}GaAs$	700	N 10^{18}
$Al_{0.3}GaAs$	100	Undoped
$Al_{0.4}GaAs$	2500	P 10^{18}
GaAs	100	P+ 10^{19}
AlAs	1500	Undoped
GaAs	Substrate	N+ 10^{18}

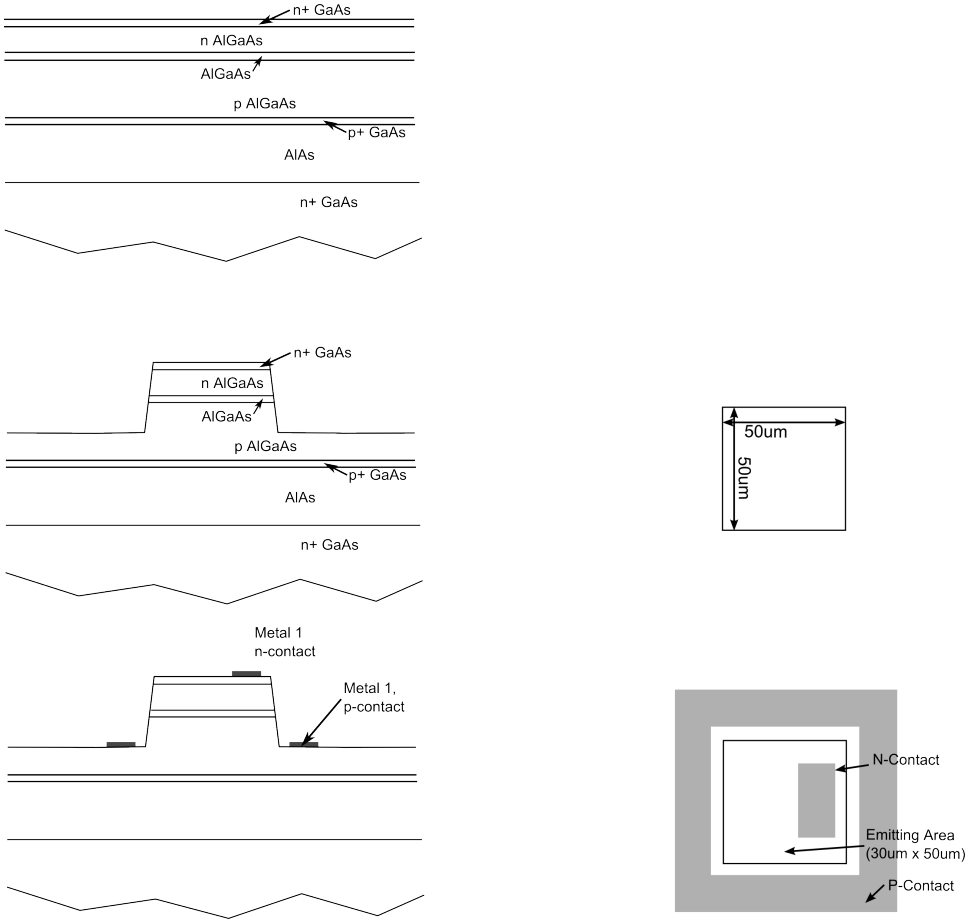


Figure 3.6: First three steps of LED array fabrication process. Left side shows cross section, right side shows top view of the respective step.

the mesa etch areas which are then etched with a 24:1 citric acid to a 30% hydrogen peroxide solution [73][74][75]. The etch solution was prepared by dissolving 12g of citric acid monohydrate into 12mL of deionized water. Since the dissolution of citric acid monohydrate into water is an endothermic reaction, the solution was allowed enough time to cool to room temperature before performing the etch. The hydrogen peroxide is mixed into the citric acid solution 15 minutes prior to the etching of the patterned wafer. After the etch solution is prepared, the patterned sample is etched for 13 minutes resulting in an etch depth of approximately 1.4 μm. A cross sectional

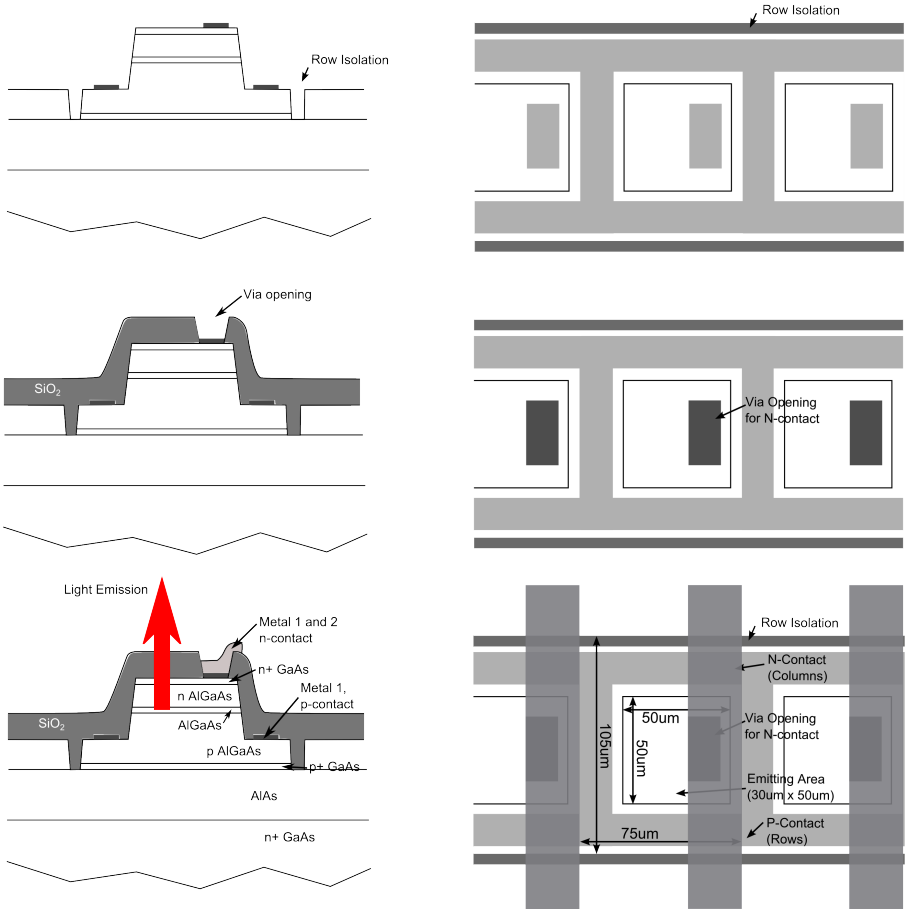


Figure 3.7: Final three steps of LED array fabrication process. Left side shows cross section, right side shows top view of the respective step.

scanning electron micrograph of this first etch is shown in fig. 3.8.

A layer of 50 nm chromium / 500 nm gold (Metal 1) was thermally evaporated and patterned with a standard lift-off process to define the n and p contacts. The p-contact is on the bottom of the mesa and also defines the rows. The n-contact is on the top of the mesa and allows for testing of individual devices.

A second etch step (Etch 2) cuts a trench between each row to electrically isolate individual rows using the same citric acid and hydrogen peroxide solution as the first mesa etch. Without careful control of this etch process, the resulting device will

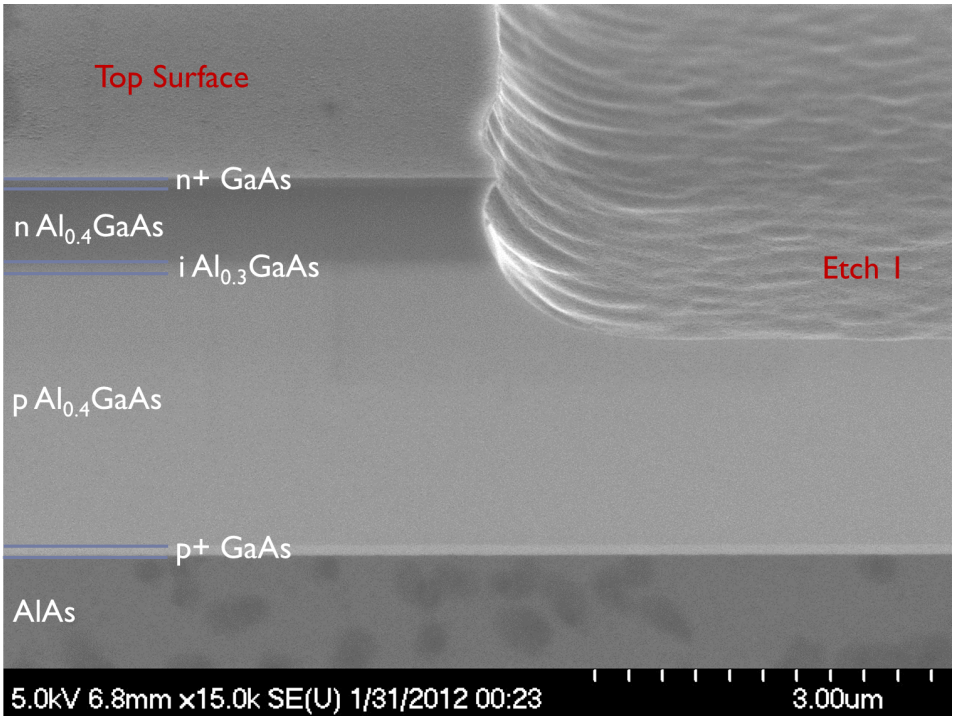


Figure 3.8: Cross sectional scanning electron micrograph of sample after the first etch process. This shows the different epitaxial layers and the correct etch depth.

be a directly-addressed LED array rather than the desired passive-matrix. In the directly-addressed case, each column is addressed as a single element; the LEDs in each column cannot be electrically separated because of cross-talk through the highly doped p+ GaAs layer. Essentially, all of the LEDs share a common p-side electrode. This can be seen in fig. 3.9 where the perimeter of the bond pads light up as well, showing the severity of the cross-talk. [76]

Because of photoresist cleaning steps between mask levels, a gallium oxide film is likely formed, preventing the continued etching of the row isolation trench. By performing a 20 second buffered oxide etch (20:1) before etching, the gallium oxide layer can be cleared allowing the row isolation etch to complete properly. Fig. 3.10 shows the cross section of a sample where the row isolation etch has reached the desired level. This can also be verified optically by using a short depth of focus

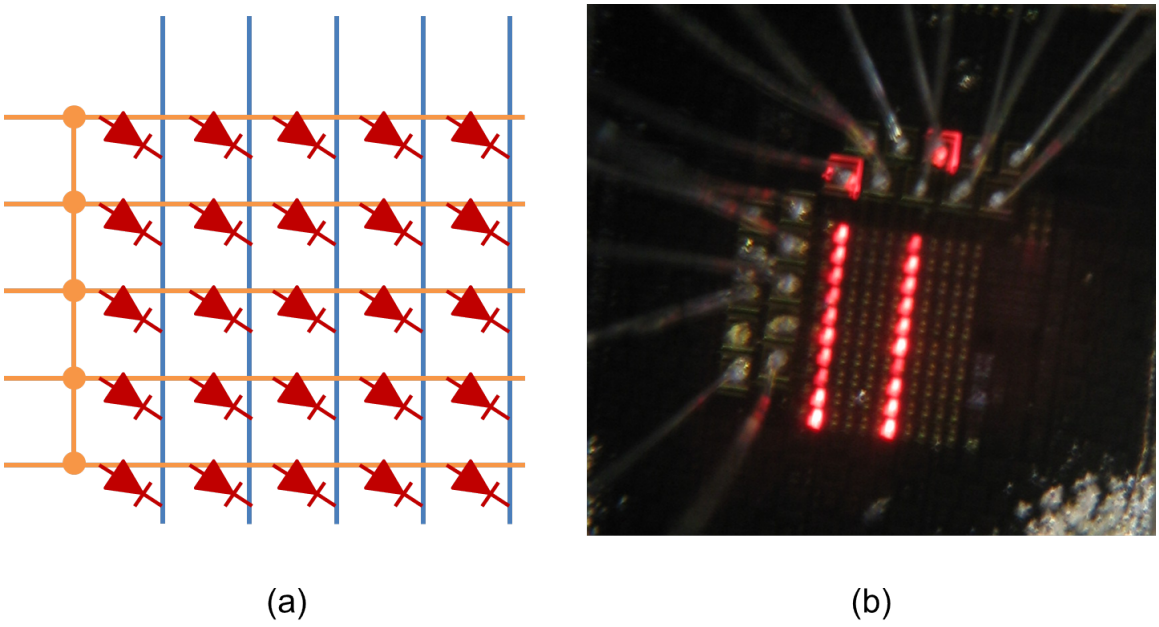


Figure 3.9: (a) Schematic of LED array with row cross-talk issues. The rows are all connected together through the p+ GaAs layer. (b) Micrograph of LED array with cross-talk issue. Each column is addressed as a single element rather than 10 individual elements. Cross-talk extends to the bond pads shown by the perimeter of the bond pad lighting up.

microscope objective and seeing a change in focus on each layer, fig. 3.11.

To complete the passive matrix device, 500 nm of SiO_2 is sputtered and patterned as an interlayer dielectric, and a second metal layer is deposited and patterned to form column lines and bond pads. A micrographs of the final device is shown in fig. 3.12 and fig. 3.13 shows a circuit schematic and four arbitrary pixels in the passive-matrix.. These devices are then wire-bonded to a dual in-line package for ease of measurement and coated with parylene-C, a polymer layer, to protect and strengthen the wirebonds, fig. 3.14. [77]

The dimensions of the LED array are conservatively designed. Each pixel is 50 μm x 50 μm, and the metal square p-contact surrounding the mesa has a width of 15

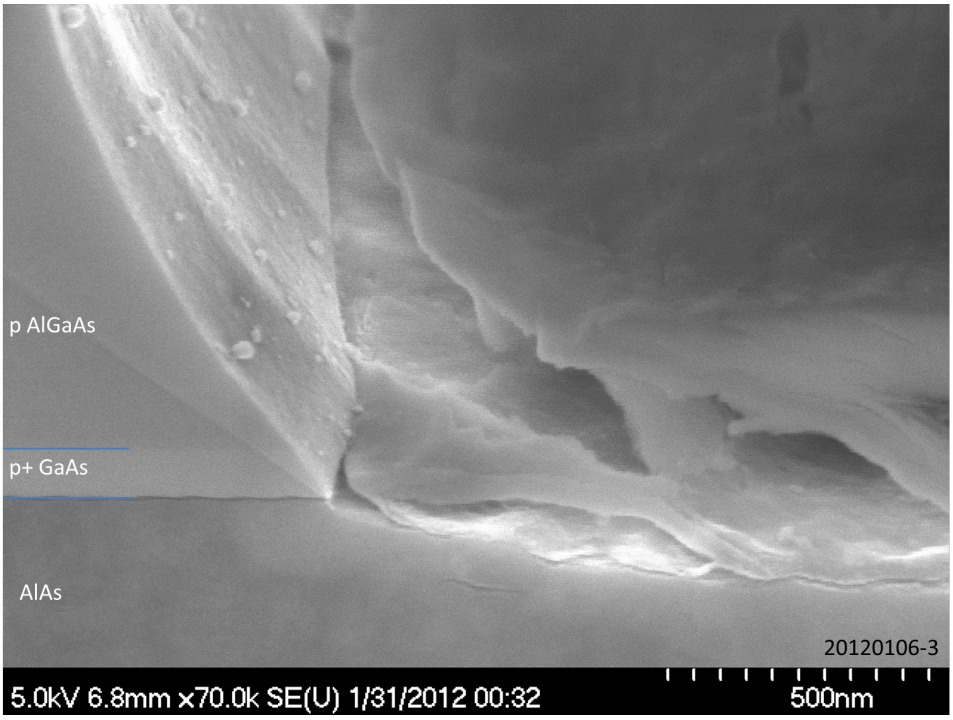


Figure 3.10: Cross sectional scanning electron micrograph of sample after second etch process. This shows the different epitaxial layers and the correct etch depth, right past the p+ GaAs to isolate each row.

μm. The rectangular n-contact is 15 μm x 30 μm and the via holes and column lines are patterned on top of that area. The center to center pitch dimension is 75 μm in the rows and 105 μm in the columns, corresponding to a fill factor of 19%. These numbers can be improved with use of a higher resolution lithography system and less conservative pixel design.

3.4 LED Characterization

All electrical measurements were taken using an Keithly 2400 source measure unit. Optical power was measured with a calibrated Newport 818-UV silicon photodetector approximately 2mm from the device.

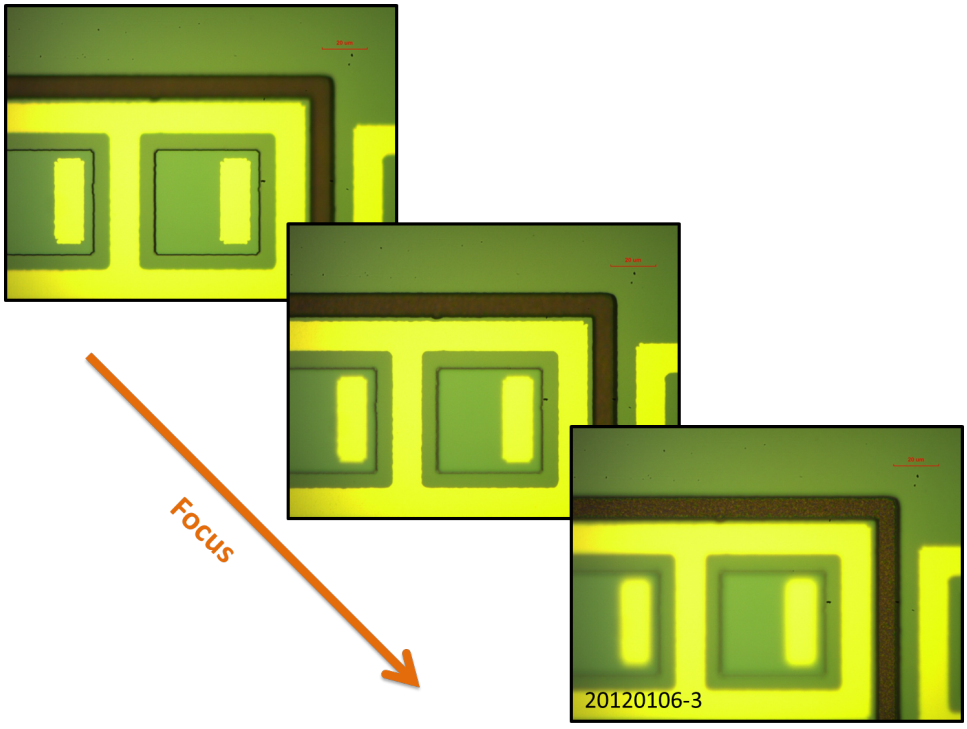


Figure 3.11: Three micrographs showing shift in focus on each of the etched layers. This provides a rough quick check of etch depth.

A typical current-voltage characteristic is shown in fig. 3.15 with a turn-on voltage around 7 V at a current of 2 mA. The higher turn-on voltage is partially due to the small size of the LED [56][78]. The optical power-current characteristics, figure 3.16, are nearly linear at the source after 100 A/cm^2 with each column driven as high as 1000 A/cm^2. Corresponding optical power density at the maximum current density is 1.14 W/cm^2. The maximum current density is limited by the resistivity of the metal lines and the contact resistance to the devices. The heat generated from these series resistances eventually causes the column of devices to fail before reaching the limits of individual LEDs. These issues can be solved with further refinement of processing and choosing metals with matching work functions.

The spectral characteristics of an LED pixel, measured with an Ocean Optics USB4000 spectrometer, are shown in fig. 3.17. The undoped AlGaAs active region

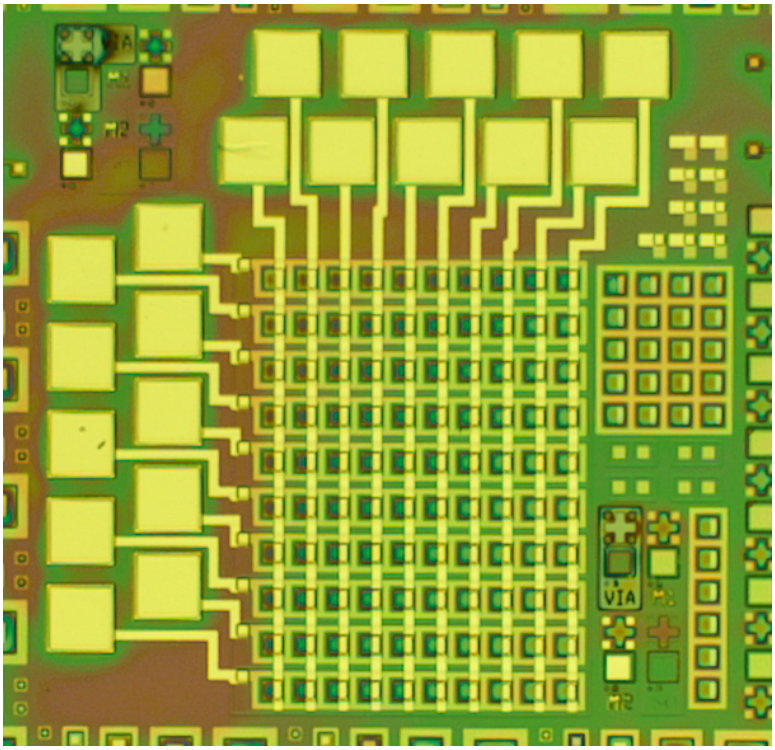


Figure 3.12: Micrograph of 10 x 10 LED array fabricated with a five photomask process. Each LED is 50 μm x 50 μm.

has a peak emission wavelength at 694 nm with a full width half max of 18 nm. This spectral output is a highly saturated red and has 1931 CIE coordinates of x = 0.71, y = 0.29. The secondary peaks at 660 nm and 890 nm do not have a noticeable effect on color point. These minor peaks can be attributed to direct band-to-band recombination of GaAs and the other AlGaAs materials.

3.5 Projection Methods

The LEDs are placed in an optical setup (fig. 3.18) to assess their projection capabilities. The LED light is focused through two plano-convex lens and projected onto a screen approximately 12 inches away. This setup produces a linear magnification

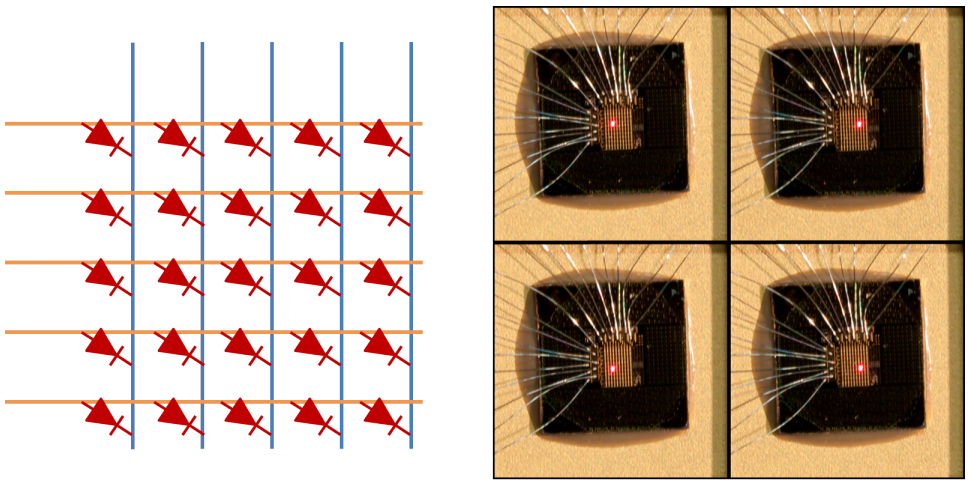


Figure 3.13: A 10x10 passive-matrix. Each LED is individually controlled by addressing the associated row/column. (a) Circuit schematic of the passive-matrix. (b) Photographs of LED passive-matrix array with four arbitrary pixels addressed.

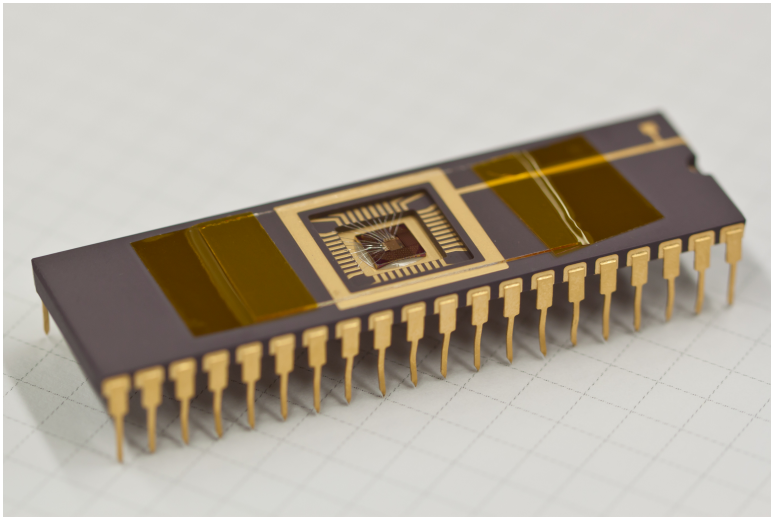


Figure 3.14: Photograph of LED array in a dual-in-line package for testing.

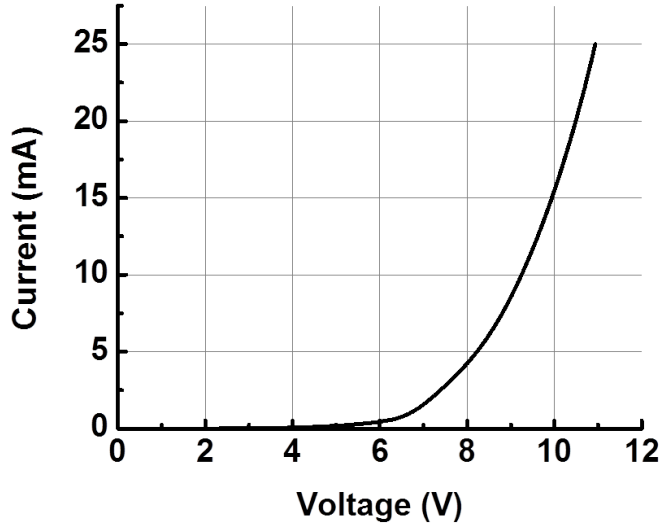


Figure 3.15: Typical current-voltage characteristic of a 50 μm x 50 μm LED pixel.

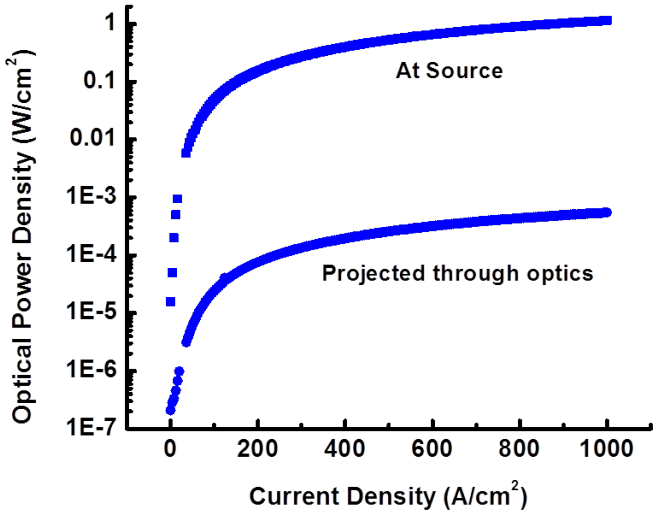


Figure 3.16: Typical optical power density vs input current density characteristics of a 50 μm x 50 μm LED pixel at the source and projected through optics.

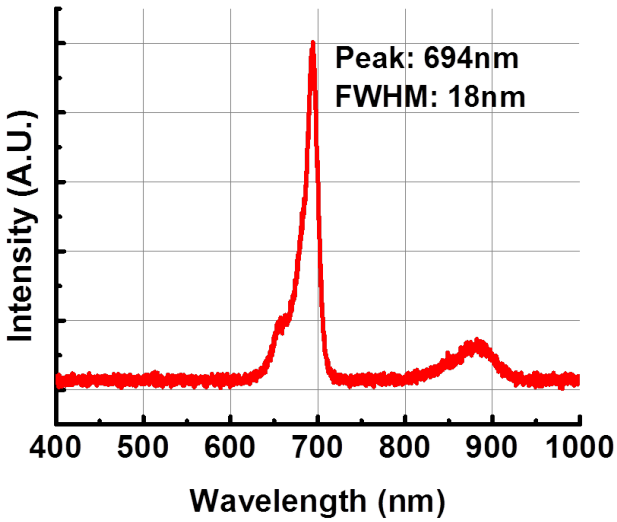


Figure 3.17: Spectrum of the LED pixel. The peak wavelength is 694nm, governed by the undoped AlGaAs recombination layer.

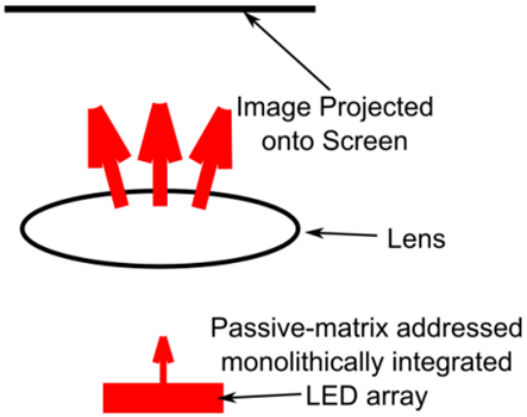


Figure 3.18: Schematic drawing of LED experimental setup which consists of the LED passive matrix focused through two optics onto an image plane.

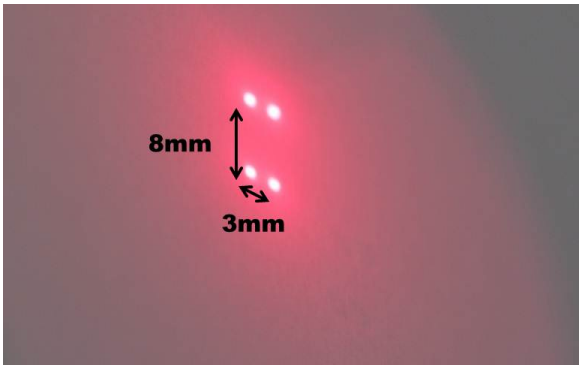


Figure 3.19: Photograph of four LED pixels magnified by 20X and projected onto a screen. On the array, these four pixels are spaced is approximately 400 μm x 150 μm

of the pixels by 20X. The optical power density projected through the lens versus current density is shown by the blue dotted lines in fig. 3.16. At 1000 A/cm^2, we have an optical power density of 0.055 mW/cm^2. In this scenario, the optical coupling loss is approximately 5X due to the non-optimized optics setup. Fig. 3.19 shows four pixels magnified and projected.

To achieve full color projection, more complex optical setups are required. Fortunately, these methods have been well established with existing projection technologies. Two proposed schemes for using three monolithically integrated LED arrays are shown in fig. 3.20. The first scheme, similar to many three liquid crystal display (3LCD) designs, uses a crossed dichroic prism with the RGB LED arrays on three of the four sides. The beam is combined in the dichroic cube and then projected through lenses in the front. The second scheme uses a prism originally designed for 3CCD cameras and later adopted by LCoS projection technologies.

In both of these structures, the dichroic filters can transmit 90% to 95% of the desired light and reflect nearly 100% of the undesired light. With these efficient optical systems, most of the light emitted from the LED array can be captured and projected onto the screen. Also important in both these systems is the relative alignment of each LED array. The convergence of RGB pixels is required along all six-axes

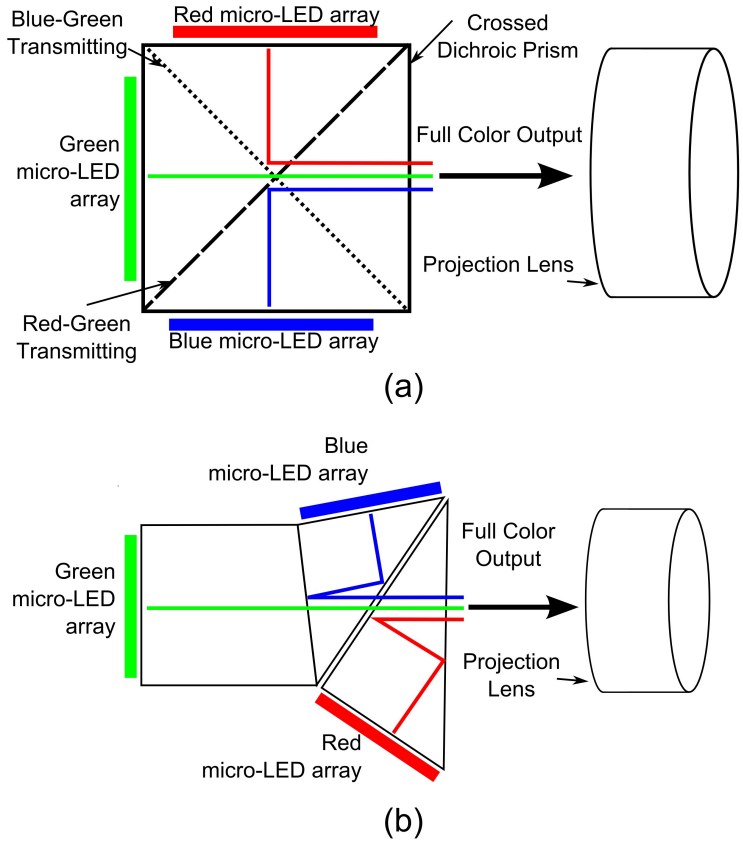


Figure 3.20: Two proposed projection schemes using three separate LED arrays, red, green, and blue. (a) Projection scheme commonly used for 3LCD projectors. (b) Projection scheme commonly used for LCoS projectors.

$(x, y, z, \theta, \phi, \psi)$, similar to the requirements for 3LCD and LCoS projection technologies. Many mechanisms are already in production for 3LCD and LCoS and can be applied to these LED arrays.

Both full color schemes require three separate LED arrays which can add to total cost and size. By using a single LED array, the size of the total device can be made much smaller to enable new applications, such as embedded pico projectors. Starting with a blue or ultraviolet LED array fabricated in a similar way to the red LED array described above, a full color LED array can be produced by adding a conversion layer.

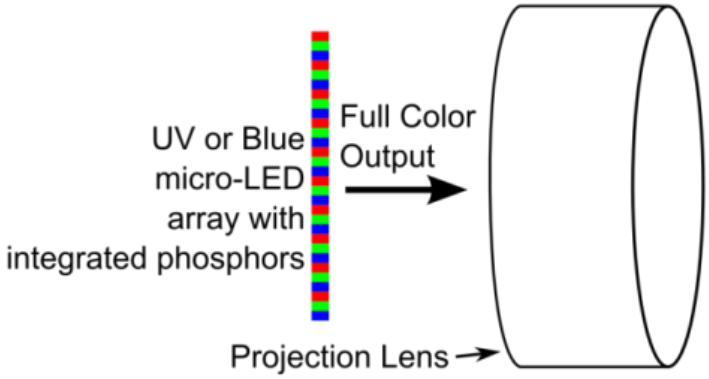


Figure 3.21: Proposed projection scheme using a single LED array and a color down-conversion layer consisting of red, green, and blue phosphors.

The color conversion layer can be several phosphors with individual color filters as pixels, or individually patterned red, green, and blue down-conversion phosphors. With either of these color conversion layers, a single chip, full color LED array can be fabricated. Keeping within the theme of projection technologies, this full-color LED array can be integrated into portable devices with a single lens system, fig. 3.21. This can also be further translated to other application areas where a small, bright, energy efficient light engine is needed.

3.6 Directly Addressed vs. Passive Matrix vs. Active Matrix

Using just the LED array, directly-addressed and passive-matrix displays can be built. In a directly-addressed display, each LED is directly associated with an external connection. For example, fig. 3.22 shows a directly-addressed clock with 28 LED devices needing a minimum of 29 external connections. This offers the simplest scheme, but the number of bonds increases at the same rate as the number of LEDs.

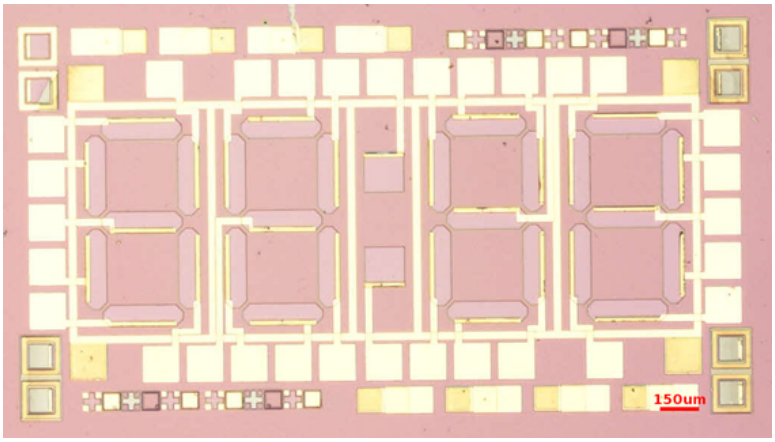


Figure 3.22: Proposed projection scheme using a single LED array and a color down conversion layer consisting of red, green, and blue phosphors.

In a passive-matrix display, LEDs are addressed in a row-column scheme and only a single row is on at a given time, fig. 3.13a. As a passive matrix, the fabricated device has 100 LEDs and requires 20 external connections. To address the entire display, each row is flashed sequentially at a refresh rate of 60 Hz. The two primary limitations of passive matrix drive schemes are lower perceived brightness and resistive losses in the row lines. Because a row is only on for a small portion of the entire frame time, the perceived brightness is the peak brightness divided by the number of rows. For example, an LED display with a 20M cd/m^2 starting brightness and 1000 rows would have a perceived brightness of only 20,000 cd/m^2. The second issue is the resistive loss across the row lines. As the number of columns increases, the resistive losses in a row line increases proportionally. With several hundred columns, the power lost in the row lines becomes higher than the power used to drive the LEDs.

An active matrix drive scheme solves both of these problems, but materials which are efficient light emitters do not form high performance transistors, and materials that make high performance transistors typically do not emit light. Thus, many integration methods have been proposed for joining LEDs and transistors [11][79][80][81][82]. These however suffer from a range of problems including poor

bonding, mismatched thermal expansion coefficients or lattice constants, or size constraints limiting the ultimate level of integration.

The combination of the LED array from this chapter and the silicon circuitry from chapter 2 addresses all of these issues and allows us to fabricate a very high brightness microdisplay platform which is fundamentally different from other display technologies. Other emissive displays, such OLED microdisplays, offer many of the same efficiency benefits, but do not offer the absolute brightness achievable by compound semiconductor LEDs.

3.7 Conclusions

In this chapter, commercial LEDs were used to demonstrate the feasibility of high brightness display made from compound semiconductors. The green LED in section 3.2 easily achieved a 100X linear magnification in normal ambient lighting conditions. Directly-addressed and passively-addressed monolithically integrated LED arrays were fabricated and demonstrated as monochrome display elements.

Using higher power devices and improved coupling from the source to the optics, a brightness of 100,000,000 cd/m^2 is possible, allowing the formation of large screen image sizes directly from an emissive light source. A full color microdisplay platform using three LED arrays can be realized using currently available projector optics and the described architecture platform, and full color from a single LED array can be realized using color filters or down-conversion phosphors.

The LED array developed in this chapter will be integrated with the laser crystallized silicon transistors discussed in chapter 2 to form an active-matrix microdisplay capable of achieving very high brightnesses and efficiencies.

Chapter 4

Laser Crystallization for Three-Dimensional Integrated Circuits

4.1 Introduction to Three Dimensional Integrated Circuits

Scaling of conventional CMOS circuits becomes increasingly expensive and difficult as devices are pushed towards fundamental physical limits. As this limit is approached, three dimensional integrated circuits (3DIC) are being explored as a way to augment the functionality of traditional CMOS devices [83][84]. Broadly defined, 3DICs are microchips which contain two or more active layers of devices on a single chip. In contrast, in traditional CMOS design, only a single transistor layer is built on the silicon wafer in front-end-of-line (FEOL) processes. After fabricating these transistors, many layers of wiring are required to connect the circuit components, which are commonly referred to as back-end-of-line (BEOL) processes. The goal of 3DICs is to integrate multiple active device layers on a single chip by making new devices in

back-end processes while keeping front-end processes unchanged.

Integrating devices on the back-end can alleviate space constraints on the front-end, reduce the number of long wire runs, and perform functions that may not be otherwise possible. For example, back-end devices can be used to interface with external components either through high-voltage switches or photodetectors for optical interconnects. 3DICs are currently being explored through two methods: 1. Wafer bonding using Through Silicon Vias [85][86][87] or Through Chip Interfaces [88], or 2. Monolithic integration of thin film transistors using low-temperature polycrystalline silicon [89], carbon nanotubes [90], or oxide semiconductors [91]. Wafer bonding can offer high quality CMOS devices, but also increases costs and complexity by requiring a second CMOS chip and processes such as wafer thinning and alignment.

Three dimensional integrated circuits built monolithically can be more cost effective, but require high performance devices and processes compatible with back-end-of-line tolerances. Developed in this chapter is a vertical via structure which is laser crystallized to produce large grain polycrystalline material and then used to fabricate diodes. Additionally, in the context of 3DICs, front-end transistors processed with and without laser processing are compared to determine the effects of the laser irradiation on the front-end.

4.2 Laser Crystallization of Via Structures

In contrast to the more traditional lateral devices described in chapter 2, this chapter focuses on a vertical semiconductor structure. The fabrication of this structure begins by depositing a film of silicon dioxide. The SiO_2 is then etched to form via holes which are then filled with amorphous silicon. Fig. 4.1 and 4.2 show a schematic cross section and scanning electron micrograph of this structure. The cross sectional SEM image also shows possible voids in the amorphous silicon from the deposition process.

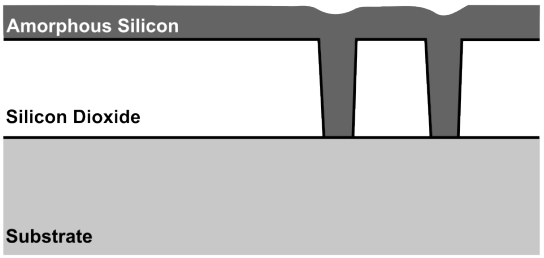


Figure 4.1: Schematic cross section of initial via structure on tungsten. Via holes are etched into silicon dioxide and filled with amorphous silicon.

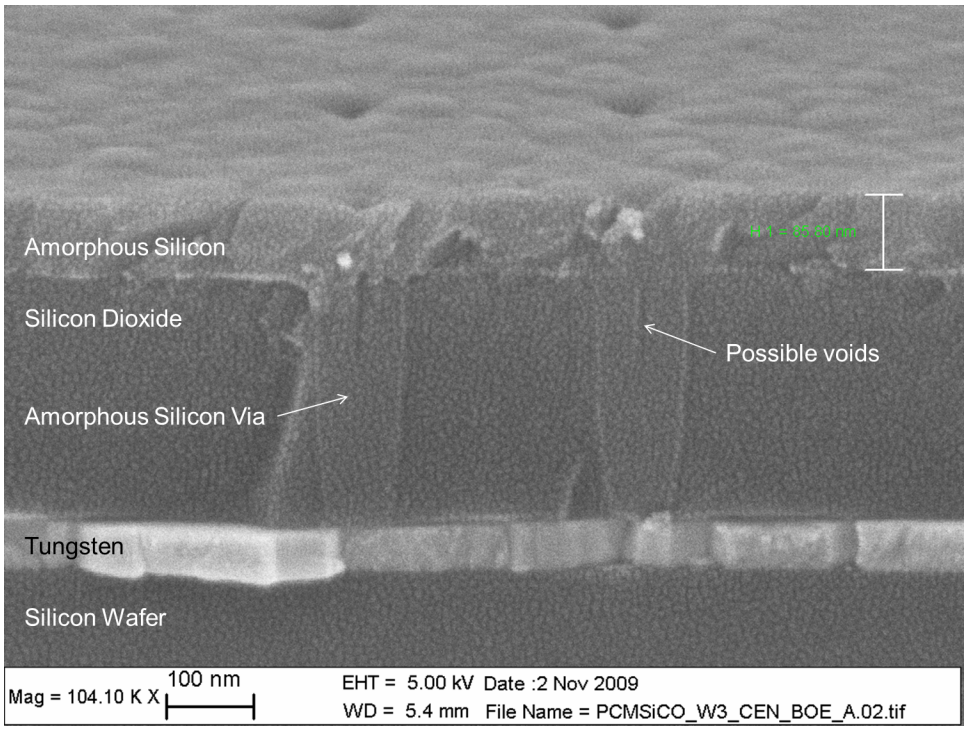


Figure 4.2: Cross section scanning electron micrograph of an amorphous silicon-filled via hole.

4.2.1 Laser Crystallization of Silicon Via on Tungsten

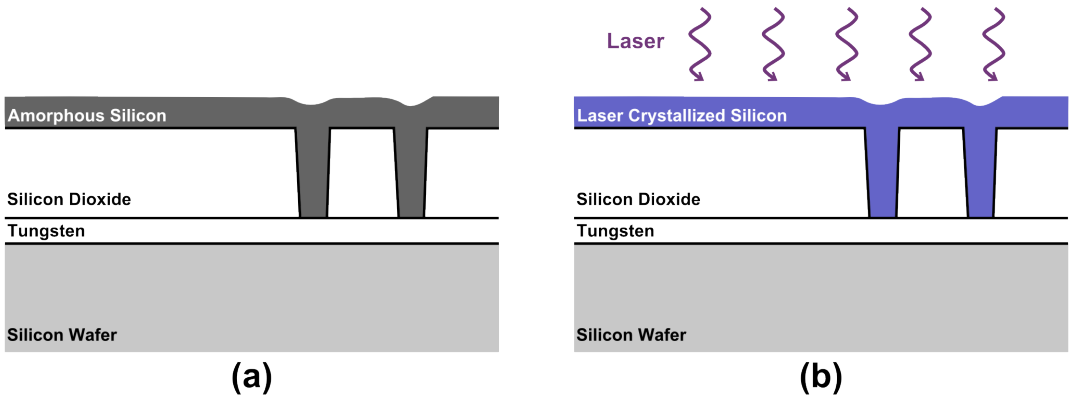


Figure 4.3: Process flow for fabrication of vertical structures. (a) Amorphous silicon deposited in silicon dioxde vias. (b) Laser crystallization of amorphous silicon.

In typical silicon CMOS back-end, the vertical structures described above would likely be built on copper. However, copper has a lower melting temperature than silicon. During the laser crystallization step, as the silicon in the via hole melts and crystallizes, the copper underneath would also melt with unknown consequences. Tungsten is an alternative back-end compatible material with a higher melting temperature than copper, and in the overall process flow would be deposited and patterned before the deposition of the silicon diode and amorphous silicon. As a proof of concept for laser crystallization on tungsten, test samples consisting of a blanket tungsten film on a silicon wafer were used. Silicon dioxide is deposited and etched to form via holes, and amorphous silicon is deposited to fill the via hole, fig. 4.3a.

The vertical column of amorphous silicon and the overburden, the extra amorphous silicon covering the surface, is irradiated with a single laser shot, fig. 4.3b. The laser used is a XeCl excimer laser with a wavelength of 308 nm. The pulse length can be adjusted through a pulse duration extender from roughly 30 ns to 300 ns. The laser beam is shaped through projection optics and a quartz photomask with

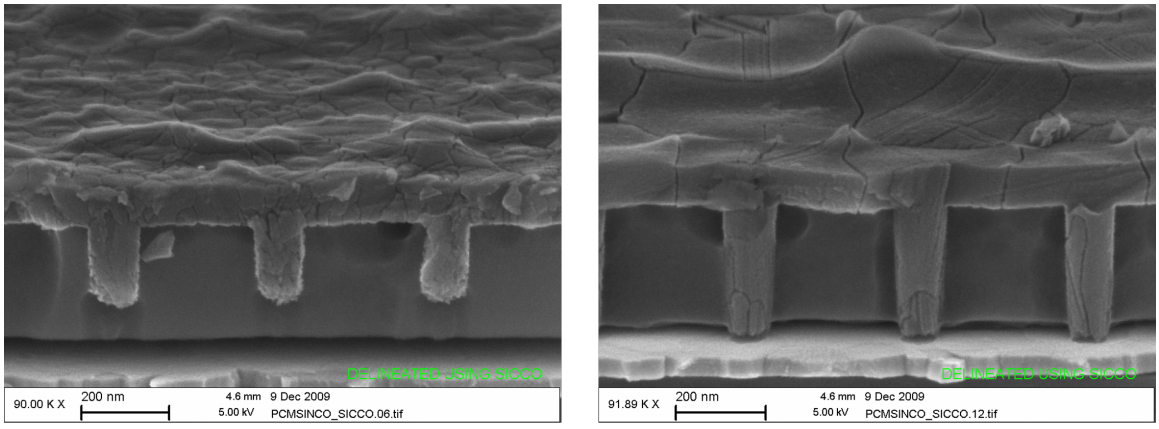


Figure 4.4: Cross sectional scanning electron micrographs of laser crystallized vias with two laser energies, (a) lower $800 mJ/cm^2$ laser energy, (b) higher 1800 mJ/cm^2 laser energy.

a 1 mm x 1 mm opening. The sample is exposed 1 mm x 1 mm at a time and a high precision motorized stage stitches together individual 1 mm x 1 mm squares to cover the entire area of interest. As described in chapter 2, the silicon oxide serves as a buffer layer, keeping the laser energy and most of the heat at the top surface. In addition, the short pulse duration and limited exposure area allows the wafer to cool back to room temperature before the next laser shot.

The laser energy can be adjusted to melt the entire vertical column of amorphous silicon. At a lower laser dose of 800 mJ/cm^2, the amorphous silicon column is melted about half of the way down, fig. 4.4a. This cross sectional SEM image shows extensive nucleation of very small grains that propagate through to the surface. This type of explosive crystallization is undesirable since it leaves behind amorphous silicon in the via hole and generates a small grain microstructure, which typically leads to low carrier mobility.

At a higher 1800 mJ/cm^2 dose, the amorphous silicon via is melted the full depth of the hole, fig. 4.4b. In the nanoseconds after the amorphous silicon melts, crys-

tallization begins at the bottom of the via hole. Because the underlying tungsten does not offer a seed template, the molten silicon begins crystallizing randomly at the bottom of the via hole, forming small polycrystalline grains. As the silicon continues to cool, grain growth propagates to the surface, with visibly larger grains at the top of the via hole. This is also evident in the microstructure of the top surface where there are much larger grains in 4.4b versus the lower laser energy sample, fig. 4.4a.

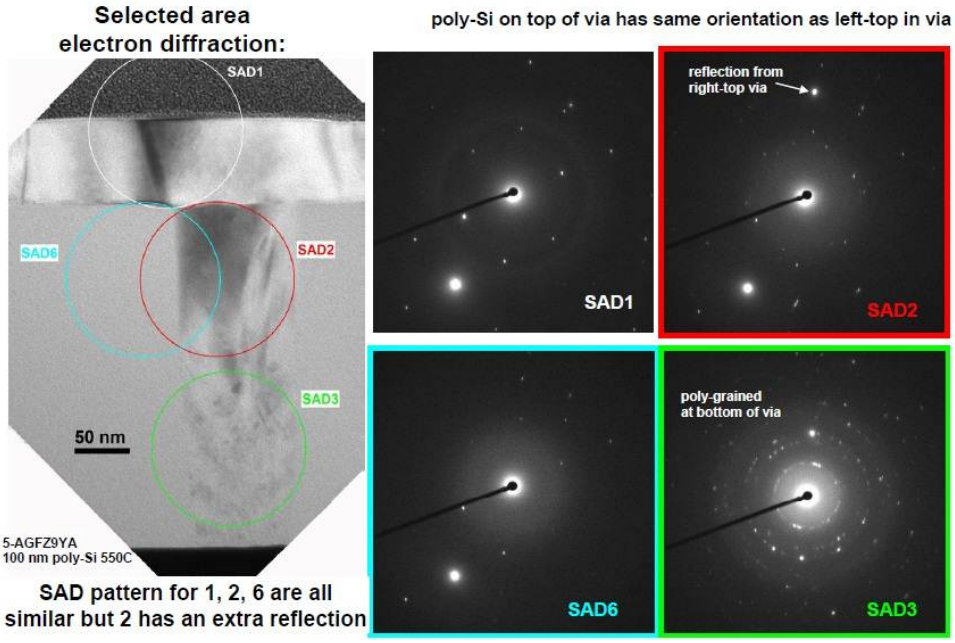


Figure 4.5: Transmission electron micrograph of laser crystallized via on tungsten. Selected-area-diffraction shows small polycrystalline grains near the bottom which merge into larger grains near the top of the via.

Transmission electron microscopy also verifies the information from the SEM image, fig. 4.5. The selected-area-diffraction (SAD) images provides information on the crystalline state of each area. At the bottom of the via hole, SAD3, a polycrystalline small-grain microstructure is observed. Further up at the top of the via hole, SAD6, and at the surface, SAD1, similar microstructures are observed, suggesting this is one continuous crystal. SAD2, another region at the top of the via, has a similar

diffraction pattern to SAD6 and SAD1, but has an extra reflection from the top right of the via hole where there is a different grain. These selected-area-diffraction images verify the microstructure observed with SEM of smaller polycrystalline grains at the bottom of the via hole which then merge into larger grains seen through SEM.

4.2.2 Laser Crystallization of Silicon Via on Silicon Wafer

A similar proof-of-concept can be done with a silicon wafer underneath the amorphous silicon via instead of the tungsten. This starting structure is not as relevant for 3DIC since the vertical via structure would not be built in the back-end. However, using a silicon wafer as a seed layer allows the laser crystallized-via hole to inherit the crystallinity of the wafer. Similar methods are also being pursued by other groups [92][93].

Fig.4.6 of a silicon via on a silicon wafer tells a similar story to the previous SEM images of silicon via on tungsten. Fig.4.6a and 4.6b shows vias exposed to two laser energies, both of which are below the energy required to fully melt the silicon-filled column. In both images, there are small polycrystalline grains which begin to merge on the way up to the surface. This is in contrast to the silicon in the via hole in fig. 4.6c, which has been melted to the bottom. In this case, the molten silicon has a single crystal silicon wafer as a seed layer and thus grows with the same crystallinity as the wafer. Here, fewer grain boundaries are observed on the top surface since each via hole is made up of a single grain.

The crystal structures of the via holes are further studied through transmission electron microscopy in fig. 4.7 and 4.8. In fig. 4.7, we see a bright field image of the via hole along with several diffraction patterns. These diffraction patterns are measured on the silicon wafer, within the via hole, and at the surface. All three of the diffraction patterns are the same and verify that the silicon in the via hole is seeded from the silicon wafer.

A high resolution transmission electron micrograph in fig. 4.8 zooms in on the

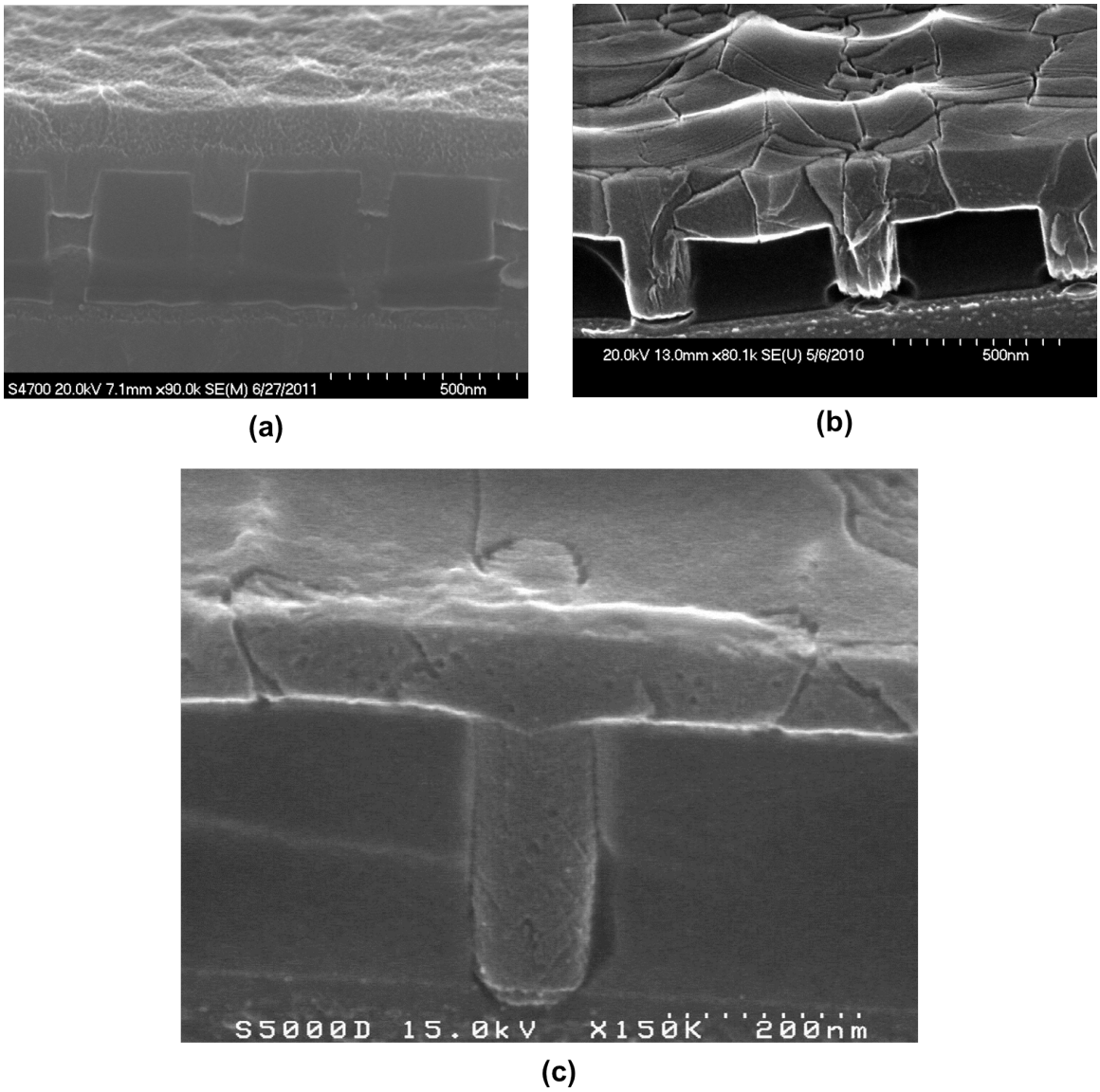


Figure 4.6: Cross sectional scanning electron micrographs of laser crystallized silicon vias on a silicon wafer produced with varying laser energies. (a) 675 mJ/cm^2 (b) 1350 mJ/cm^2 (c) 1800 mJ/cm^2. At energy (c) the laser melts the silicon all the way to the bottom of the via and seeds crystallization from the single crystal silicon wafer.

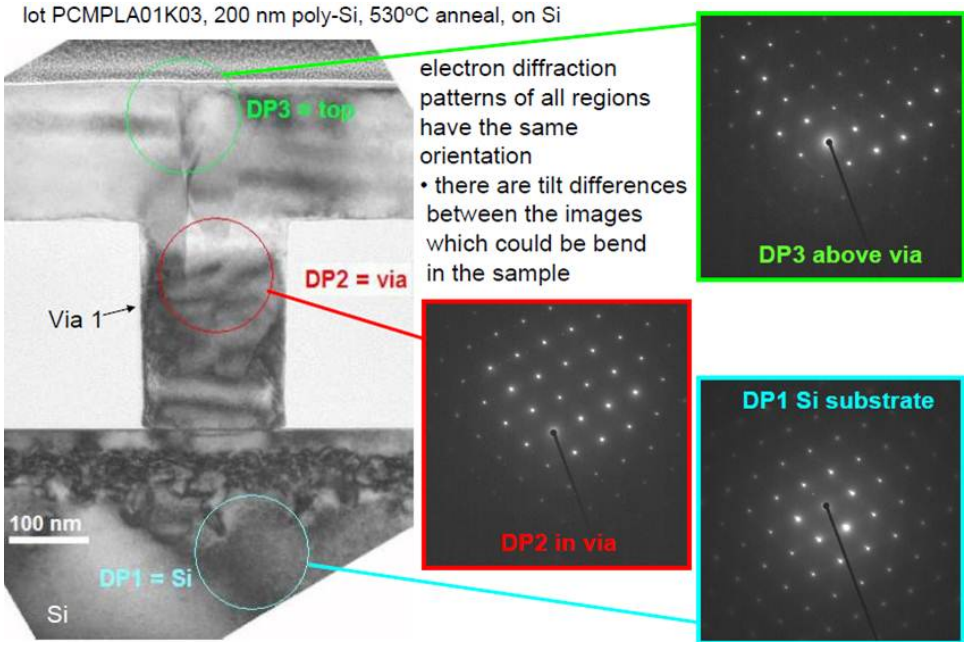


Figure 4.7: Transmission electron micrograph of laser crystallized silicon via, on a silicon wafer. Selected-area-diffraction shows that all regions have the same crystal orientation, seeded from the silicon wafer.

silicon wafer and silicon via interface. Again, from the bright field and diffraction images, we see a direct seeding of the silicon via from the single crystal wafer.

4.3 Fabrication of Version One Diodes

Using the laser crystallized via holes seeded directly from a single crystal silicon wafer, high quality electronic devices are expected since the via holes also have good crystallinity. Diodes devices are fabricated on a p-doped silicon wafer. This serves as both the p-side of the diode device and the silicon seed. The amorphous silicon via holes are then formed using the process described in section 4.2 and laser-crystallized to form the active area of the diode. After a chemical mechanical polishing, the diodes are implanted with arsenic as the n-dopant and rapid thermal annealed to activate

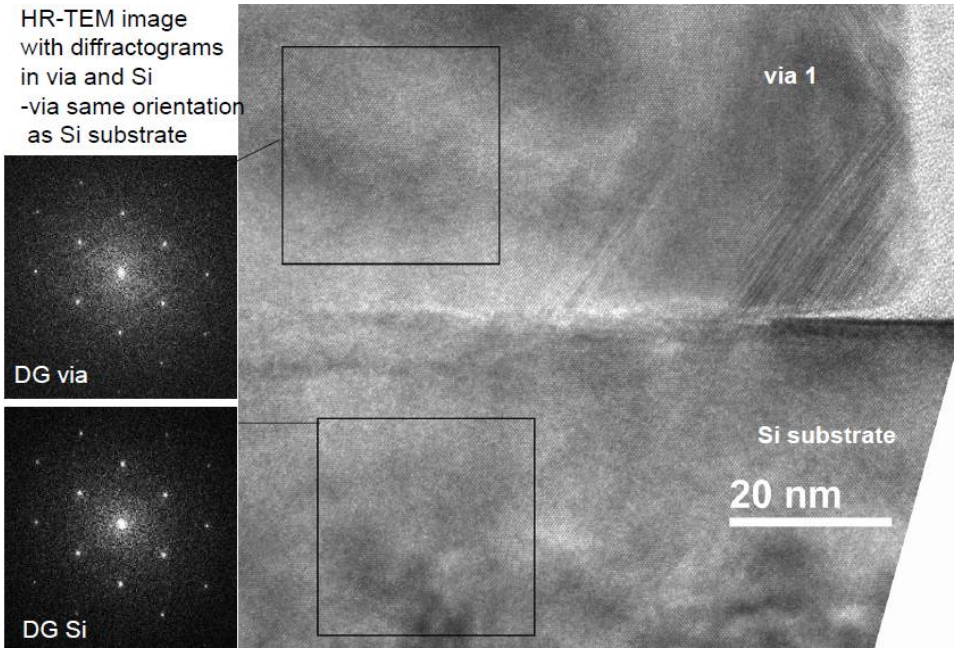


Figure 4.8: A high resolution transmission electron micrograph of laser crystallized via on tungsten. TEM diffraction images on the left show that the via region is seeded directly from the silicon wafer.

the dopants. Finally, a large aluminum contact is thermally deposited to allow for electrical contact to the diodes. The aluminum contact is 150 μm in diameter and covers approximately 25,000 diodes. A schematic cross section is shown in fig. 4.9 and a top view micrograph is shown in fig. 4.10.

4.3.1 Characterization of Version One Diodes

Samples were prepared with varied ion implant energies of arsenic between 50 keV and 150 keV. Changing the energy of the ion implantation changes the depth to which the arsenic ions are deposited and thus also the length of diode. Electrical characterization of the diodes was performed on an Agilent 4155 semiconductor analyzer. Preliminary current-voltage characteristics of these diodes are shown in fig 4.11. As expected, the higher implant energy results in an increase in current due to the shortened diode

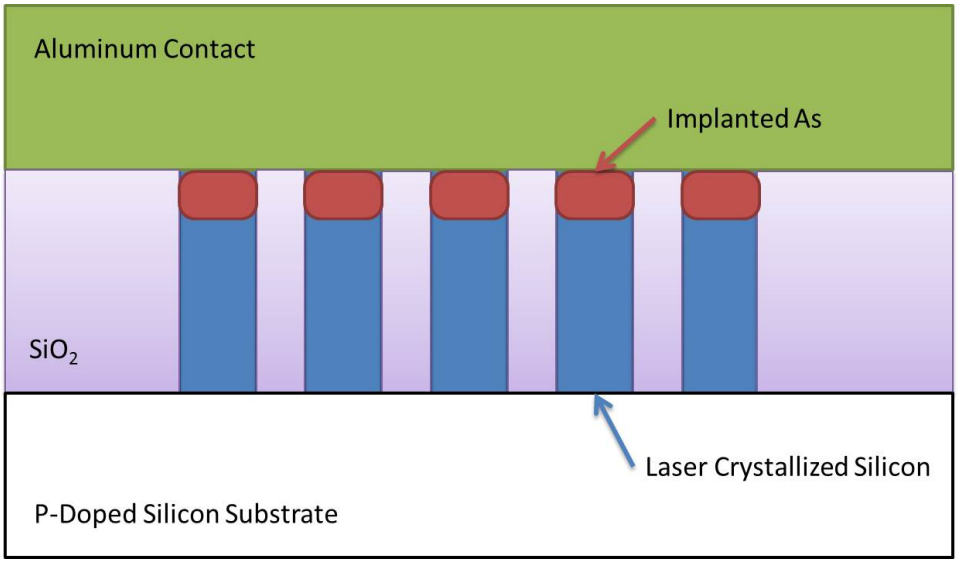


Figure 4.9: Schematic cross section of version one laser crystallized diodes formed in via holes. Diodes are electrically probed through the aluminum contact and the silicon wafer.

length. However, the high turn-on voltage and low currents imply there is poor electrical contact to the diodes.

4.4 Fabrication of Version Two Diodes

Building upon the preliminary diode results from the previous section, a second iteration of diodes was fabricated, achieving improvements in contacting individual diodes and electrical contact to the diodes. Fig. 4.12 shows the full process flow for this second iteration of diodes. The process begins similarly to previous described work with a layer of silicon dioxide on a silicon wafer, fig. 4.12a. The height of the silicon dioxide defines the height of the vertical structure. Following an etch of the silicon dioxide and deposition of amorphous silicon, laser energy transforms amorphous silicon to large grain polycrystalline silicon, seeded from the single crystal wafer, fig. 4.12b and 4.12c. The overburden polycrystalline silicon which protected the underlying layers

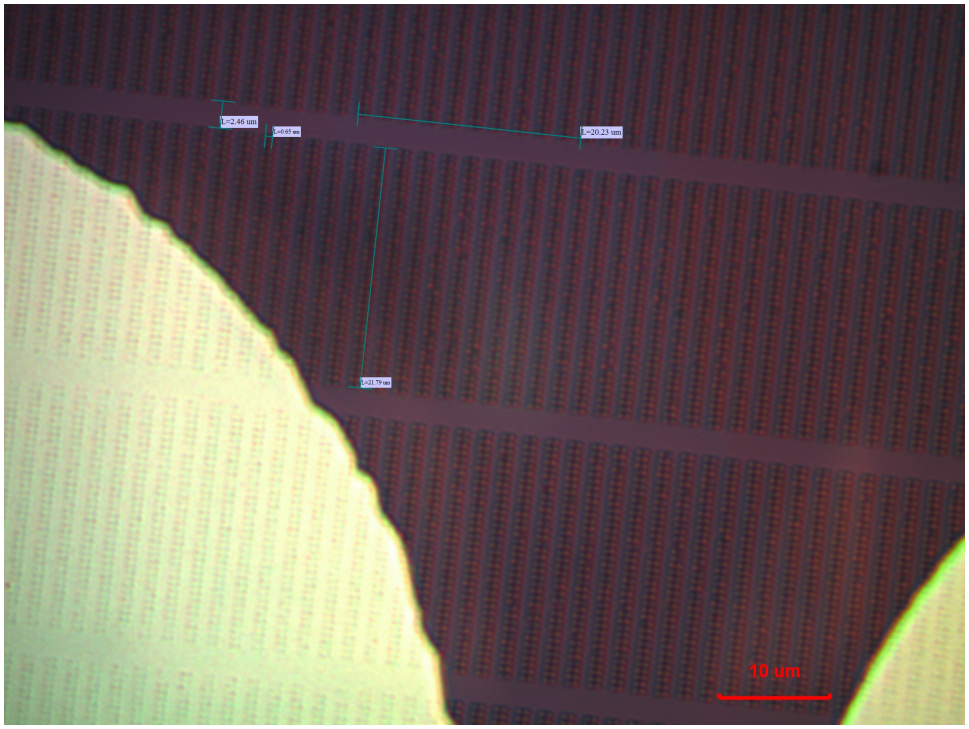


Figure 4.10: Micrograph of version one diodes formed in via holes contacted by a large aluminum metal layer. The 150 μm diameter aluminum pad has contact with approximately 25,000 diodes.

from laser exposure is now chemically mechanically polished leaving only the laser crystallized silicon in the via holes, fig. 4.12d. An etch-back of the via hole is then performed to open space for a metal contact, fig. 4.12e. Finally, an implant of boron forms the p-doped side of the diode, and tungsten metal contacts are deposited for electrical contact, fig. 4.12f and 4.12g. Following these steps, the first copper layer is deposited to contact the tungsten metal on top, and separately, the n+ doped layer underneath the vertical structure. This allows for testing solely from the top surface.

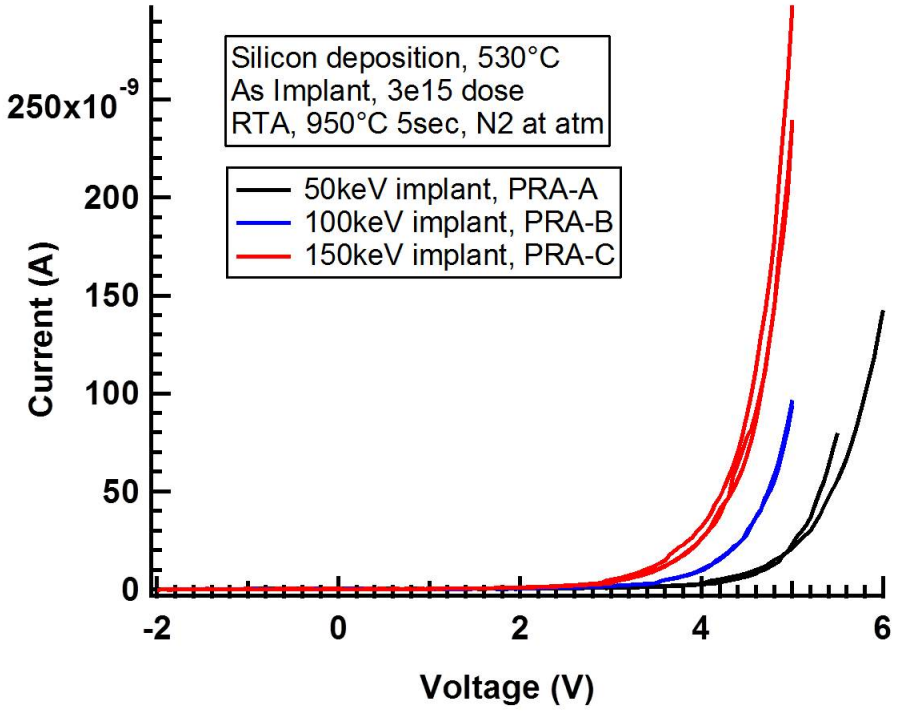


Figure 4.11: Current-Voltage characteristics of version one diodes. Aluminum metal layer is approximately 150 μm in diameter, contacting 25,000 diodes. Curves shift with changes in the arsenic implant energy.

4.4.1 Characterization of Version Two Diodes

Multiple diode devices are measured from two different wafers. Fig. 4.13 shows the current-voltage characteristics for these diodes. Based on the mask design, each measurement probes two diodes in parallel. We can see from the I-V characteristics that the turn-on voltage is around 0.7 V, and the laser crystallized diodes show very consistent behavior across each wafer and across multiple wafers. In addition, the high on-currents point to high quality material within the via structure.

For comparison, epitaxial diodes are fabricated using the same structure as described above. Instead of laser crystallization, the epitaxial diodes use a high tem-

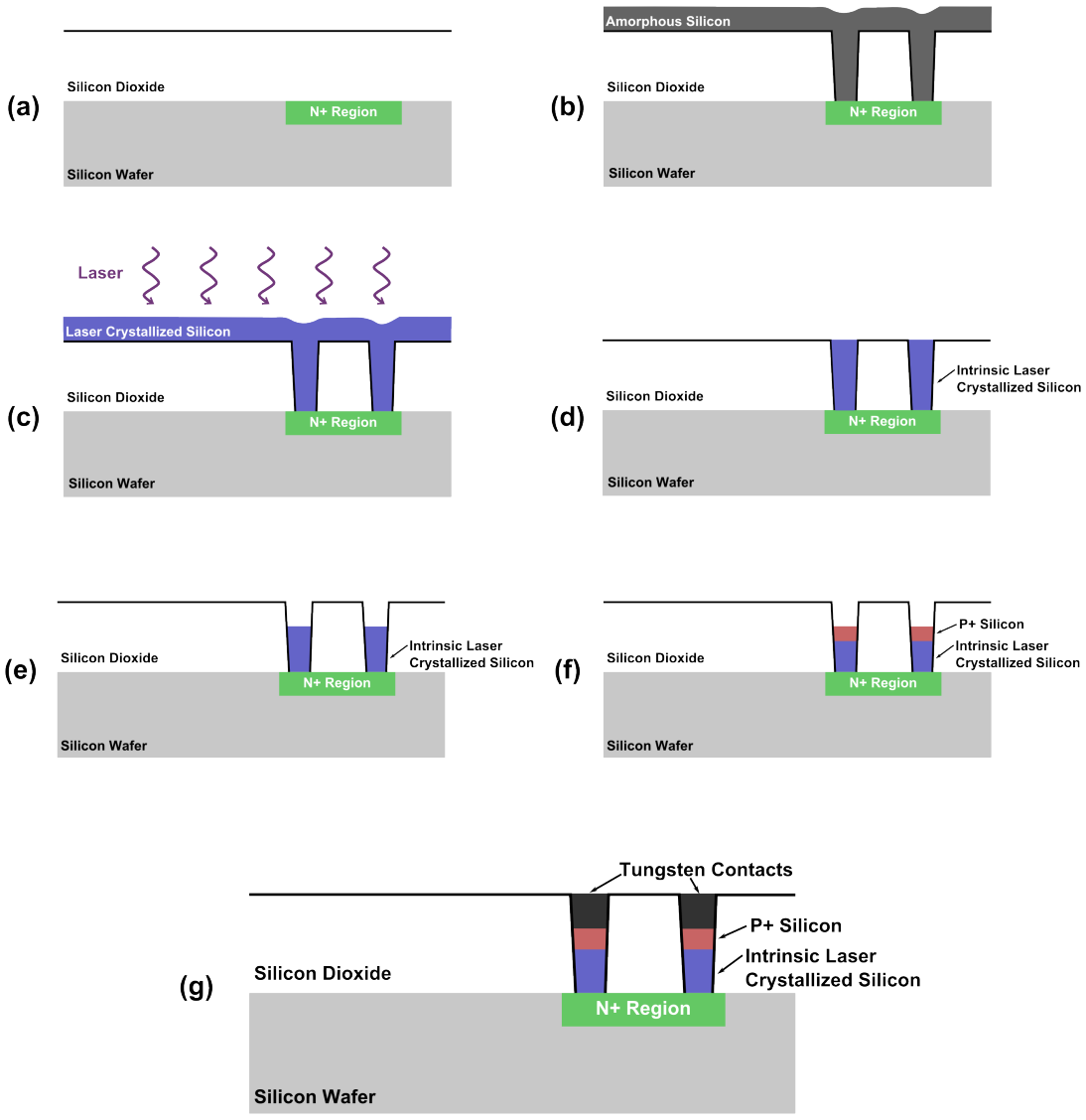


Figure 4.12: Process flow for fabrication of version two vertical diodes. (a) Ion implantation and silicon dioxide deposition. (b) Via opening etch for vertical structures and amorphous silicon deposition. (c) Laser crystallization. (d) Chemical mechanical polishing. (e) Etch back of laser crystallized silicon. (f) Ion implantation of p+ side. (g) Deposition of tungsten contacts.

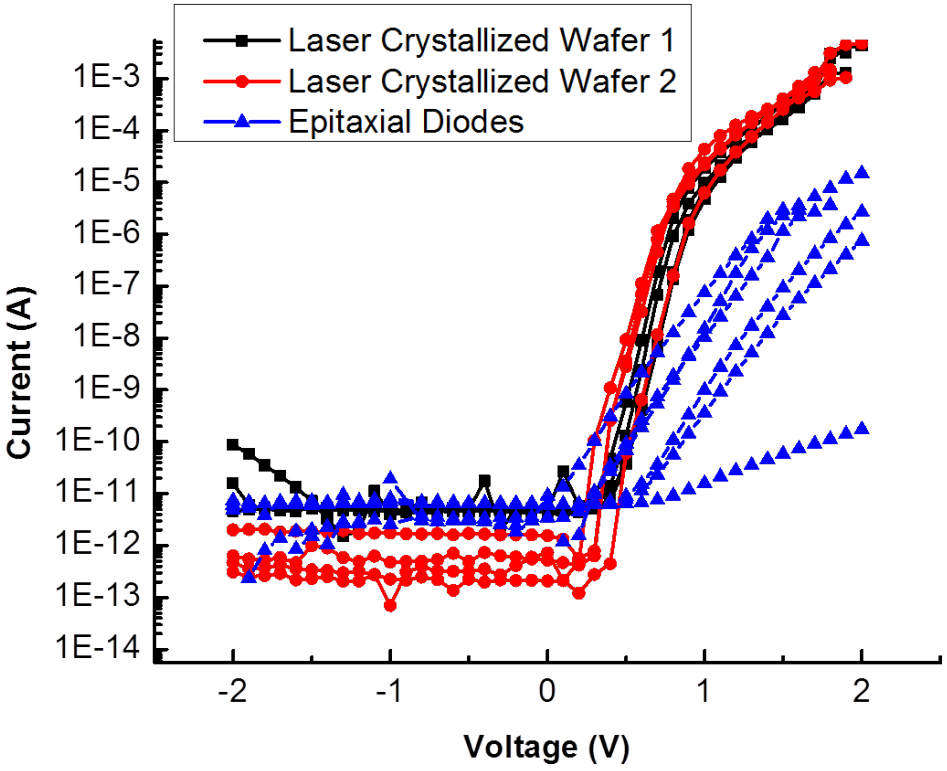


Figure 4.13: Current-Voltage characteristics of version two laser crystallized diodes compared with epitaxially grown diodes. Laser crystallized diodes are more consistent and exhibit a much higher on-current.

perature process to grow silicon through the via hole, seeded from the wafer. When characterized electrically, the epitaxially grown diodes are 100 to 10,000 times lower in current, and have little consistency across multiple devices. Additionally, the high temperature epitaxial growth method would be difficult to integrate into a 3DIC structure since the thermal cycles will cause drastic changes in previously fabricated devices.

4.5 Front-End CMOS devices

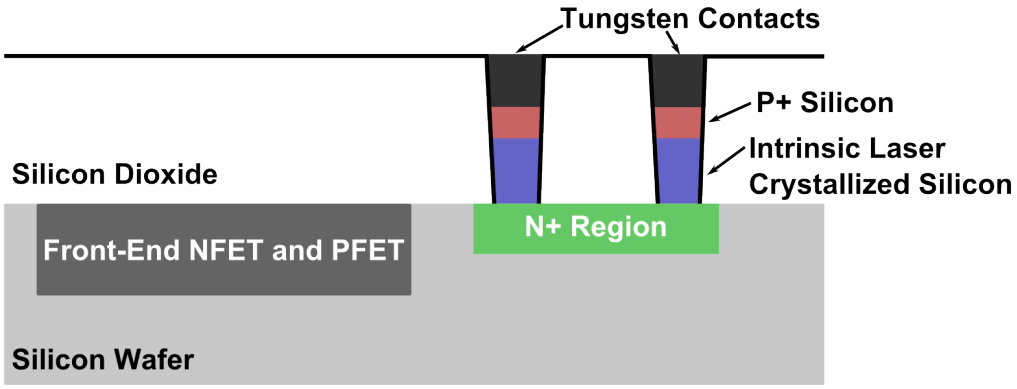


Figure 4.14: Cross sectional schematic of laser crystallized diodes integrated directly on standard NFET and PFET front-end transistors.

The goal of three dimensional integrated circuits is to integrate devices built on the back-end along with traditional front-end devices. Building additional devices on the back-end requires special processing methods such as laser crystallization, during which it is important to ensure that the laser will not change or damage the circuits fabricated in the front-end. In chapter 2, simulations showed that a 1 μm silicon dioxide thermal buffer kept the underlying substrate below 70°C during laser processing. Past literature has also shown laser crystallization to work without damage to low-temperature substrates, such as polymers [94][95][96].

Building full front-end devices offers the most direct method of characterizing the effects of laser exposure. The device structure in fig. 4.14 is similar to previous diode device structures, except full front-end n-channel and p-channel field effect transistors are fabricated beneath the silicon dioxide layer. Front-end transistors which do and do not see laser processing are directly compared to check whether transistor characteristics have shifted.

Six wafers are fabricated, three without laser processing and three with laser processing. On each of the wafers, twenty n-channel transistors and twenty p-channel transistors are measured. Three significant characterization parameters are extracted for each of the measured transistors: oxide thickness (t_{ox}), threshold voltage ($V_T - Sat$), and drain current in saturation ($I_D - Sat$). These three parameters are used to track the uniformity and shifts in characteristics, if any.

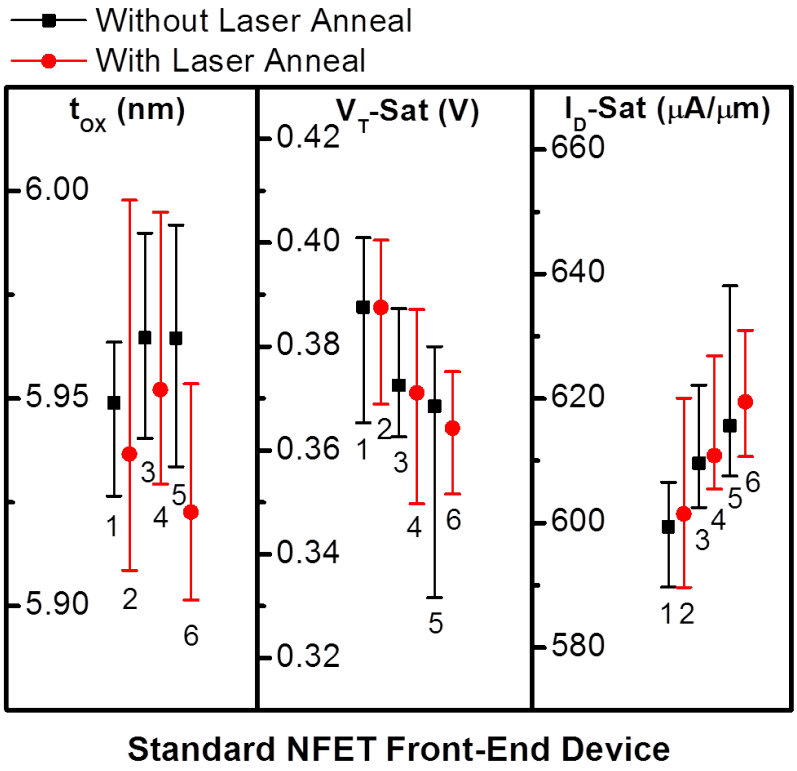


Figure 4.15: Fundamental device characteristics (t_{ox}, $V_T - Sat$, $I_D - Sat$) measured across six wafers with and without laser anneal. Twenty NFET devices were measured for each wafer. Each vertical line marks the median and two end-points of the twenty devices. Black lines are wafers without laser annealing. Red lines are wafers with laser annealing.

Fig. 4.15 shows the three tracked parameters across all six wafers. The black lines reference wafers which have not been laser processed, and red lines reference to wafers with laser processing. Each of the lines represents the range of all twenty measured transistors, marking the median and two end points. Given equivalent spreads in the data for the wafers with and without laser processing, laser annealing does not show any measurable effects on NFET transistors. With and without laser annealing, the t_{ox}, $V_T - Sat$, and $I_D - Sat$ parameters all fall in the same expected range. Additionally, we can consider the six wafers in pairs, where each pair undergoes thermal processes distinct from the other two pairs. Wafers 1 and 2, 3 and 4, and 5 and 6 are paired. In each pair, there is one wafer which has not been laser crystallized (wafers 1, 3, 5), and one wafer that is laser crystallized (wafers 2, 4, 6). When looking at the $V_T - Sat$ and $I_D - Sat$ parameters in fig. 4.15, it is clear that the thermal parameters cause a shift in the tracked parameters, while the laser crystallization has no observable effect.

The same parameters, t_{ox}, $V_T - Sat$, and $I_D - Sat$, are also tracked for p-channel transistors (PFET) in fig. 4.16. As expected, the p-channel devices are less uniform than the n-channel devices, but the parameters with and without laser annealing show similar trends. In the t_{ox} parameter, wafers 1 and 2, 3 and 4, and 5 and 6 are very similar. Again, these pairs of wafers have slightly different thermal conditions, but in all cases, the laser annealing does not have any noticeable impact. The data spread across wafers is larger for $V_T - Sat$ and $I_D - Sat$ and individual device data points are plotted in figures 4.17 and 4.18.

Fig. 4.17 shows $V_T - Sat$ for the twenty measured PFET transistors from each wafer. Although the threshold voltage parameter is spread across 0 V to -0.3 V, the difference between non-laser crystallized (black) and laser crystallized (red) devices is negligible. A similar plot for $I_D - Sat$ of PFET transistors is shown in fig. 4.18. The $I_D - Sat$ for PFETs parameter exhibited the largest spread of data across all the n-channel and p-channel devices measured. Removing one or two of the outliers puts

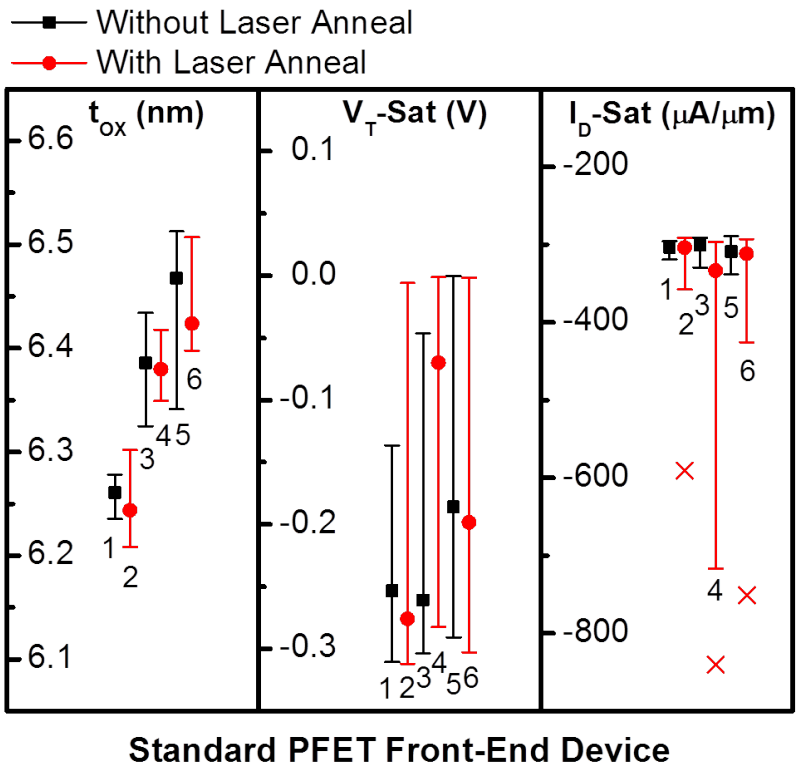


Figure 4.16: Fundamental device characteristics (t_{ox}, $V_T - Sat$, $I_D - Sat$) measured across six wafers with and without laser annealing. Twenty PFET devices are measured for each wafer. Each vertical line shows marks median, and two end-points of the twenty devices. Black lines are wafers without laser annealing. Red lines are wafers with laser annealing.

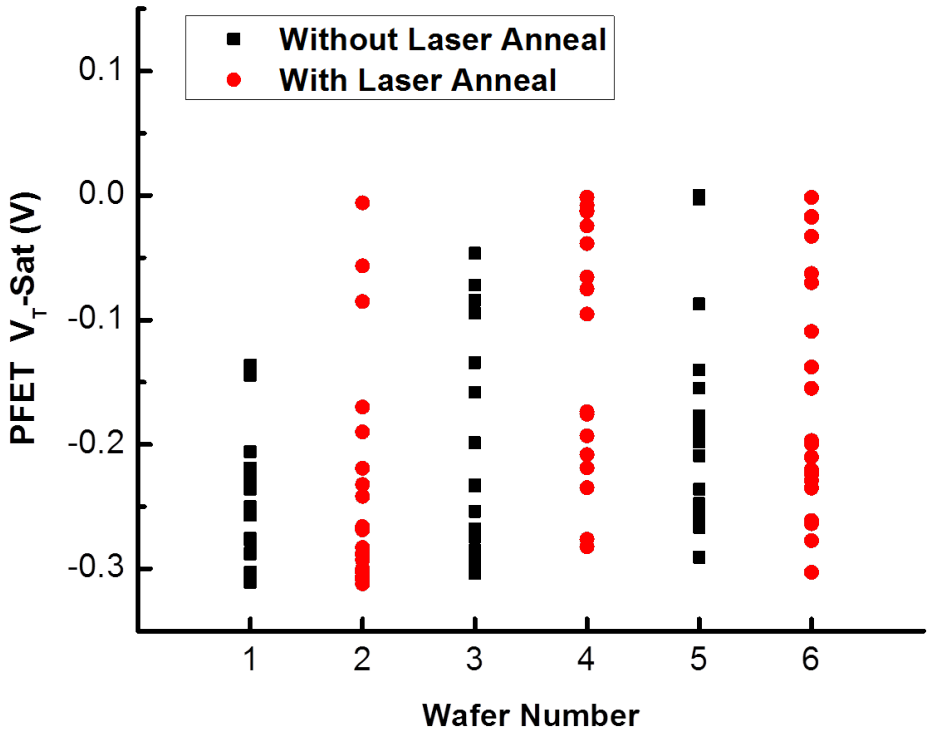


Figure 4.17: $V_T - Sat$ of PFET devices measured across six wafers, with twenty transistors per wafer. Black lines are wafers without laser annealing. Red lines are wafers with laser annealing. Wafers show a similar spread of data points with and without laser annealing.

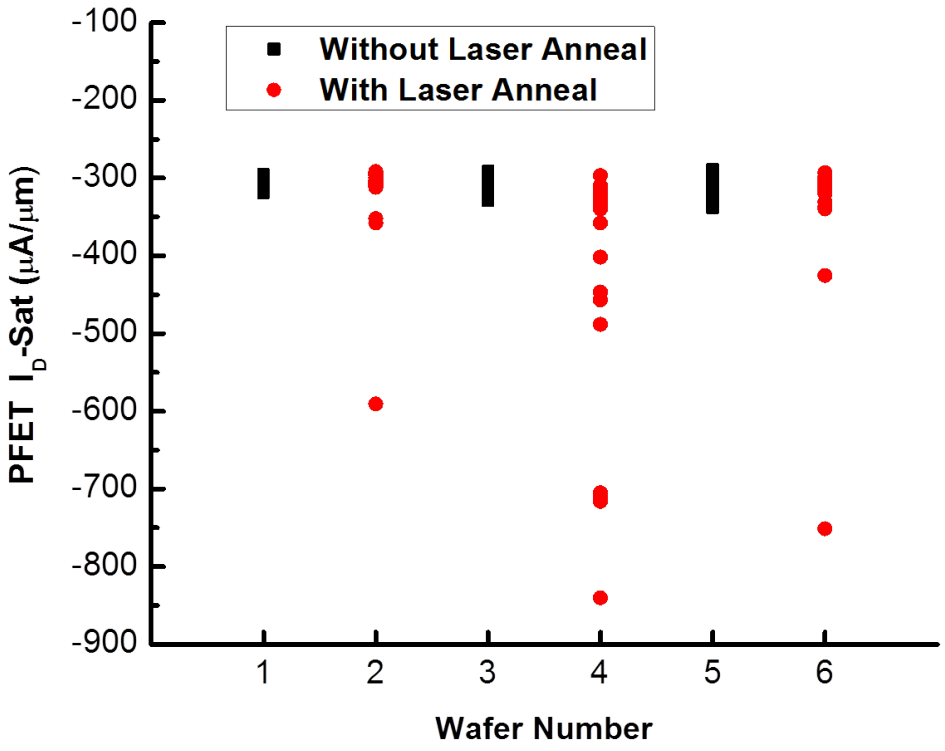


Figure 4.18: $I_D - Sat$ of PFET devices measured across six wafers, with twenty transistors per wafer. Black lines are wafers without laser annealing. Red lines are wafers with laser annealing. There are several outliers in the wafers with laser annealing, but the majority of devices fall within the same range.

wafer 2 and 6 in a similar range to the non-laser crystallized wafers, but wafer 4 still falls outside of the expected range. This may be caused by other fabrication issues unique to this wafer and specific to its p-channel devices.

Through the direct measurement of both n-channel and p-channel front-end transistors, the laser crystallization process overall showed no effect on the front-end characteristics. For 3DIC, the measured oxide thickness (t_{ox}), threshold voltage ($V_T - Sat$), and drain current in saturation ($I_D - Sat$) parameters show that the process developed for the laser crystallized diodes is compatible for adding active layers above standard CMOS.

4.6 Conclusions

To commercialize monolithically-integrated 3DICs, a method of fabricating high quality devices directly on conventional CMOS is needed. Laser crystallization serves this functionality by enabling high quality materials with low-temperature process windows. Building upon the lateral devices demonstrated in chapter 2, vertical devices were fabricated and tested in this chapter. The crystallinity of laser-crystallized polycrystalline silicon is characterized using scanning electron microscopy and transmission electron microscopy on two different substrates, tungsten and single crystal silicon. In both cases, amorphous silicon in the via hole is melted to the bottom of the hole and is seeded from the underlying substrate. When using the single crystal silicon wafer as the substrate, the silicon via holes seeded from the wafer exhibit single crystal growth throughout the via.

Two iterations of diodes are fabricated within this vertical structure and characterized. Both versions of diodes show rectification behavior, and the second iteration of diodes outperform the epitaxially grown diodes of the same device geometry.

Simulations from chapter 2 and past literature have shown the compatibility of laser processes with 3DIC designs. In this chapter, this conclusion is tested directly

using conventional front-end devices. Both n-channel and p-channel front-end devices are fabricated, and characteristic parameters of the transistors are compared for wafers with and without laser annealing. All device parameters fall within the expected range, and there are no significant changes in front-end device characteristics even with upper layers are exposed to laser irradiation.

Diode characteristics and front-end uniformity prove that laser crystallization is a suitable method for 3DIC. This paves the way for new architectures and designs, including fabrication of vertical transistors, where devices with different functions or size constraints can be placed on the back-end without disturbing conventional front-end devices. In addition, since laser crystallization methods are available and fully developed for flat panel display manufacturing, industrial tools up to 1.3 m x 1.5 m are readily available and can be adapted to uniformly process 300 mm or even 400 mm wafers.

Chapter 5

Laser Crystallization of Alternative Material Systems

5.1 Introduction

Laser crystallization is a unique processing methodology that can induce highly localized and drastic transformations to a material in very short time frames. Energy from the laser heats only the top surface of the exposed material to very high temperatures, leaving the bottom layers at temperatures well within process tolerances. This was shown in chapters 2 and 4 with the successful crystallization of a topmost silicon layer without damage to underlying devices. The same principle of laser annealing can be applied to other material stacks where localized crystallinity is desired, using different buffer materials or crystallizing materials other than silicon. Two particular systems of interest to microprocessor foundries are crystallized silicon on low-κ dielectrics, and crystallized copper for low resistivity interconnects.

5.2 Laser Crystallization on Low-κ Dielectrics

In modern microprocessors, the back-end-of-line processes serve as wiring layers to connect front-end transistors. There are two materials in back-end processes: metal for the wiring, and interlayer dielectric to electrically separate the wires. As front-end devices shrink, the back-end wire separation must scale correspondingly to interface with the front-end. The decrease in distance between two neighboring wires increases the capacitance, which affects the speed of the circuit, power consumption, and capacitive cross talk.

Capacitance, the measure of a material's ability to store charge, is given by

$C = \kappa\epsilon_0 A/d$

where κ is the relative dielectric constant of a material, ϵ_0 is the permittivity of free space, A is the area that is shared between the two conductors, and d is the distance between them.

There are two options to decrease capacitance based on the equation above. The area can be reduced, but this also significantly increases the resistance of the wires. The only other option is to reduce the dielectric constant, κ, which is the path taken by the semiconductor industry. While SiO_2 was used in the past, low-κ dielectrics, which have dielectric constants below silicon dioxide ($3.9\epsilon_0$), are now ubiquitous in modern day back-end CMOS processes [97][98]. The question at hand is whether low-κ dielectric materials are compatible with laser crystallization processes and can replace SiO_2 as a buffer layer.

Industry-relevant low-κ dielectric wafers are obtained from IBM Research and Tokyo Electron. A 100 nm thick amorphous silicon film is deposited using electron beam evaporation with the substrate at 400°C. The final test stack consists of silicon wafer, 300 nm - 500 nm of low-κ dielectric, and 100 nm of amorphous silicon.

Laser-crystallized amorphous silicon on low-κ dielectrics is shown for a non-porous film with $\kappa = 3.1$, in fig. 5.1, and a porous film with $\kappa = 2.4$ - 2.6, in fig. 5.2. Both micrographs show good crystallization of the amorphous silicon and the expected grain

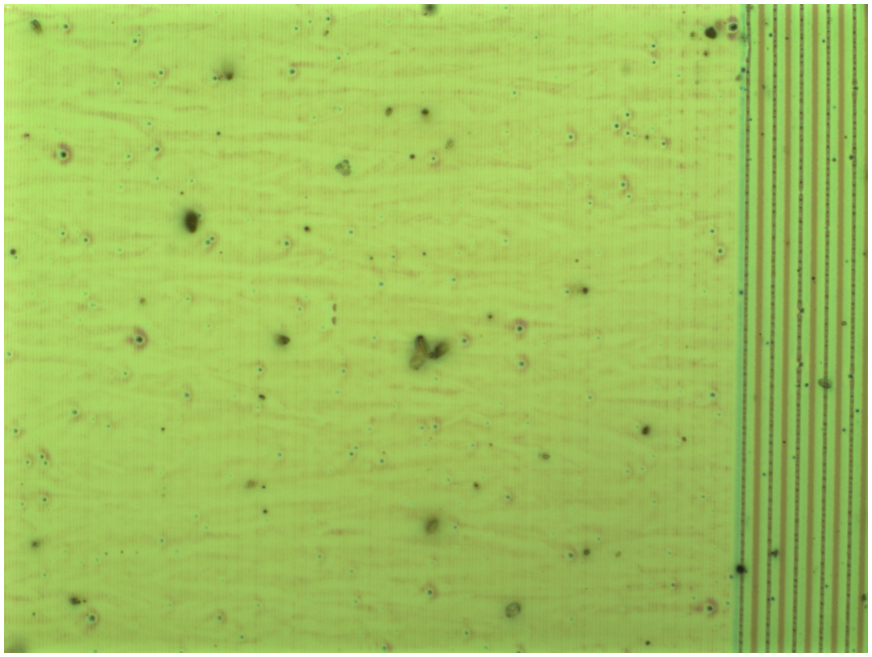


Figure 5.1: Micrograph of SLS of silicon on a low-κ dielectric wafer. The non-porous dielectric material is 300 - 500 nm thick and has a $\kappa = 3.1$.

structure from the line-scan SLS method described in chapter 2 [99]. Based on past work, the highly crystalline microstructure is expected to produce good transistors. SLS on other low-κ films was also attempted but resulted in film explosion during the laser crystallization process. This explosion is due to gas trapped during deposition of either the low-κ dielectrics or amorphous silicon.

The use of low-κ dielectrics as the thermal buffer layer in laser crystallization is advantageous over SiO_2 because the lower dielectric constants result in lower capacitance. Assuming the properties of the entire material system behave as expected, no additional layers are needed in the material stack. Like other 3DIC techniques, this allows for more devices on the back-end which can relieve the burden on the front-end. Several aspects of the low-κ system require further studies, including the low-κ/amorphous silicon interface, the effect of laser process on the dielectric properties of the low-κ material, and the thermal buffering properties of low-κ dielectrics

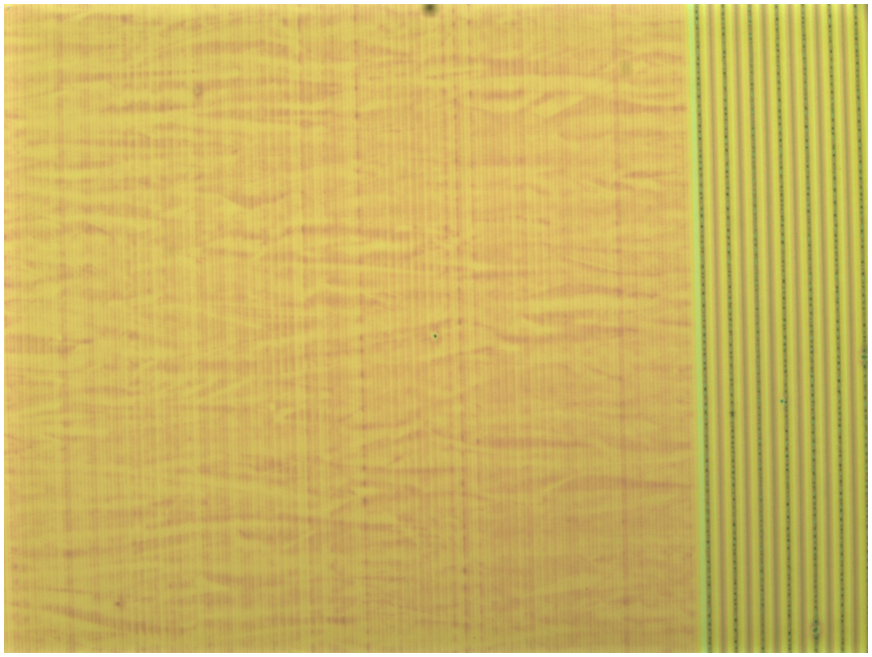


Figure 5.2: Micrograph of SLS of silicon on a low-κ dielectric wafer. The porous dielectric material is 300 - 500 nm thick and has a κ = 2.4 - 2.6.

and their effect on front-end transistor characteristics.

5.3 Laser Crystallization of Copper Interconnects

Aside from the low-κ dielectrics described in section 5.2, the back-end processes include metal lines which connect the front-end transistors. In recent years, copper has replaced aluminum as the metal of choice due to its higher conductivity and thus the ability to make narrower lines of the same resistance [100][101][102]. However, as front-end transistors get smaller and the dimensions of back-end copper interconnects scale proportionally, resistivity increases exponentially, deviating from bulk properties, fig. 5.3 [103][104][105][106].

The exponential increase in resistivity with decreasing line width can be attributed to microstructural changes at small dimensions. The transmission electron micro-

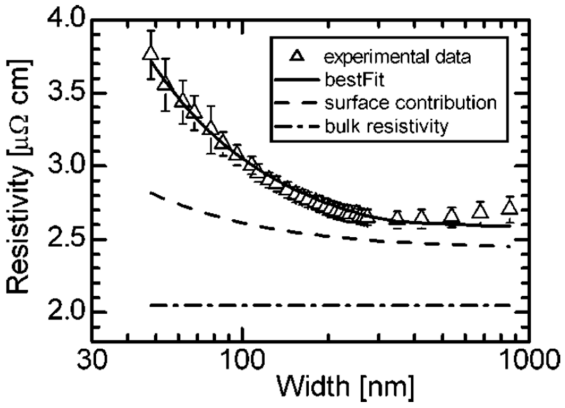


Figure 5.3: Resistivity of 50 nm height copper lines versus width. As lines become narrower, the experimentally measured resistivity in the wires increases dramatically. Fig. from reference [104].

graphs in fig. 5.4 show how the microstructure changes from a columnar form to small grains as the line narrows, which dramatically increases the resistivity [107]. This increased resistivity is a problem for circuit designers as higher resistivity lines need to be compensated with additional signal repeater circuits, which take up additional area on the front-end. Increased resistivity also has implications on transmission delays and the overall microprocessor speed.

Like silicon described in previous chapters, the microstructure of the copper can be modified using a laser recrystallization process. Changing the microstructure affects the resistivity; larger grains are desired for decreased resistivity.

Copper is deposited using industry standard tools and chemistries, then exposed to a 1 mm x 1 mm XeCl excimer laser shot for approximately 300 ns. As in previous chapters where amorphous silicon is exposed to the laser, the copper overburden absorbs nearly all of the laser energy, locally melting only the top film [108][109][110][111]. After laser crystallization, the process was interrupted to analyze the copper microstructure. A cross sectional schematic is shown in fig. 5.5. The device is similar to the vertical structures fabricated in chapter 4, but here the vertical structures

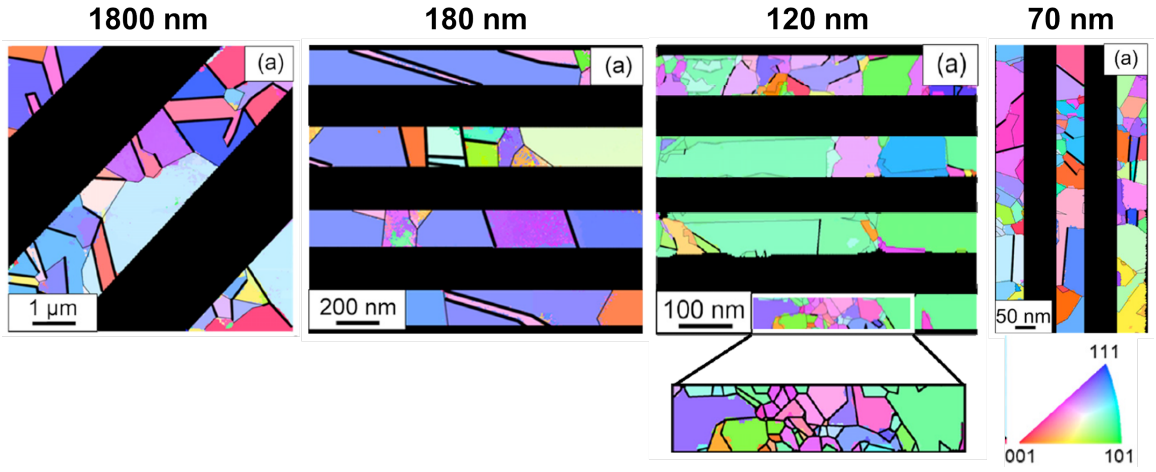


Figure 5.4: Diffraction Scanning Transmission Electron Microscopy (D-STEM) images adapted from reference [107]. Shows images for four copper line widths (1800 nm, 180 nm, 120 nm, and 70 nm), and the effect of line width on the copper microstructure.

are filled with copper instead of silicon. The next process steps would be a chemical mechanical polish of the overburden copper film and continuation of back-end processing.

Promising initial results, fig. 5.6, demonstrate the ability of the laser to fully melt the copper film and change its grain structure. The micrographs show elongated grains which begin at the edge of the laser-irradiated region, extending 5.9 μm - 8.1 μm in length depending on the energy of the laser, between 850 - 1000 mJ/cm^2. In addition, the center of the laser irradiated region contains randomly scattered nucleation sites, forming a pebble-like microstructure. The final copper microstructures obtained show many similarities to laser crystallized silicon.

With these preliminary results, samples are being fabricated to test the electrical properties of the laser-recrystallized copper in different line widths. The attainment of elongated grains from a single laser shot suggests that a stepped laser process such as line-scan SLS could further induce preferential grain growth along a single

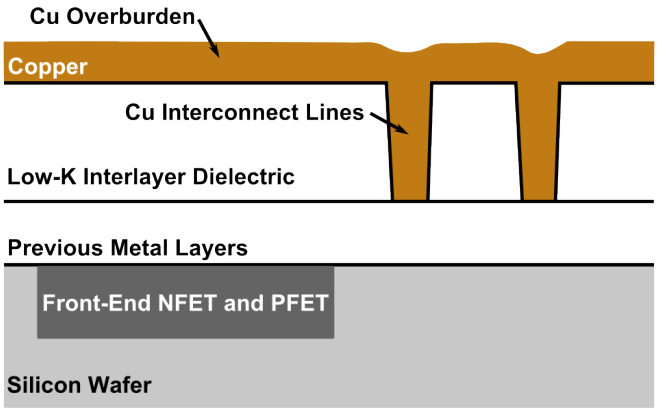


Figure 5.5: A simplified schematic cross section of copper interconnect lines with overburden. This structure is laser recrystallized to change the microstructure within the interconnect lines.

direction. A line-scan process paired with design rules for wire run direction could yield significant improvement in resistivity, especially in the narrowest interconnect line widths.

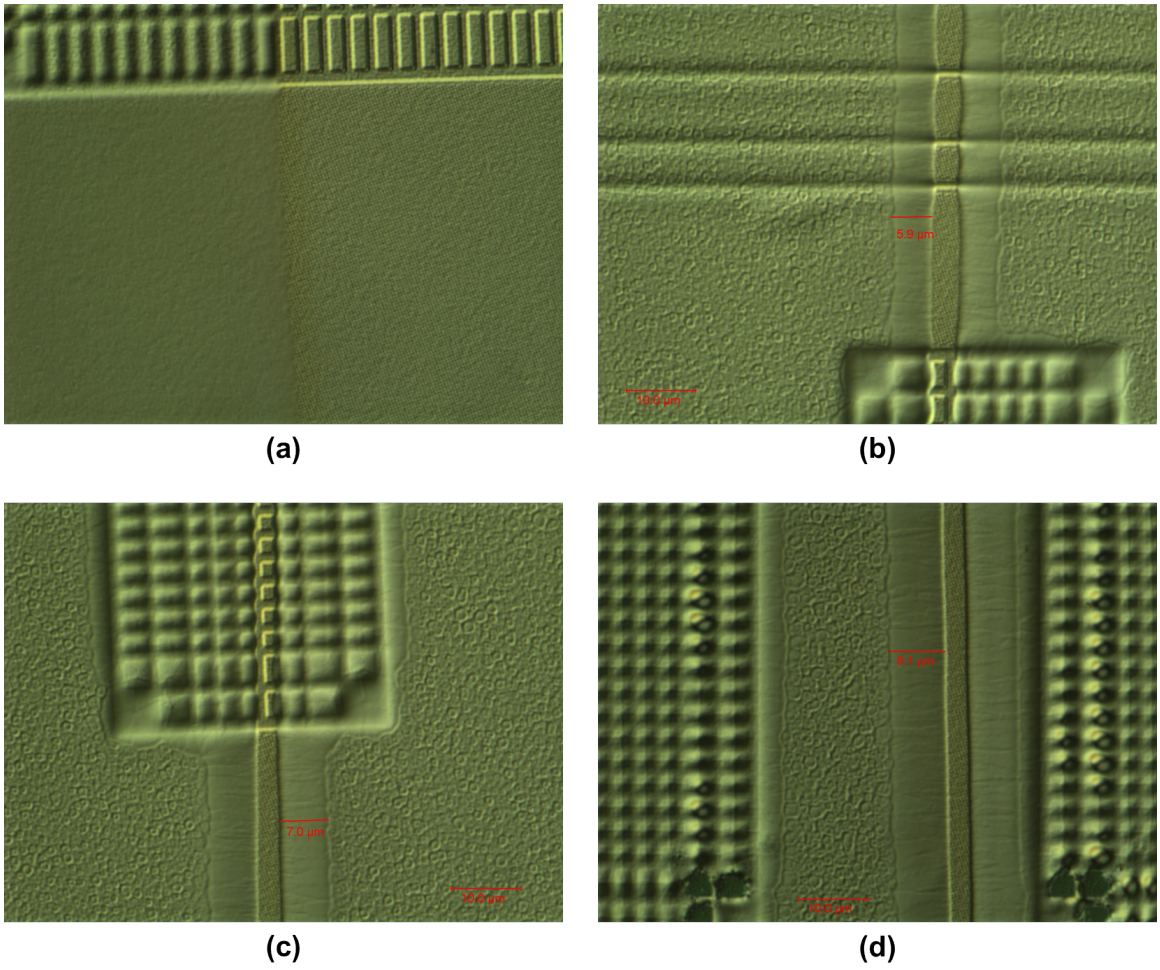


Figure 5.6: Single shot laser recrystallization of copper on a wafer. Laser energy varies from lowest (a) to highest (d). (a) Below melting threshold. (b)-(d) Above melting threshold, 850 - 1000 mJ/cm^2. The formation of elongated grains from the edge of the laser exposure area is observed.

Chapter 6

Conclusions and Future Work

6.1 Contributions of This Work

This thesis successfully demonstrates the three key components required for using laser crystallization as a method for advanced integration: 1. Laser-crystallized devices, 2. Relevant substrates for integration, and 3. Results showing the viability of integration of the two without damage to the substrate.

Lateral and vertical silicon devices are fabricated using laser crystallization processes. The lateral transistors exhibit high mobilities of above 400 cm^2/Vs, and are fabricated at process temperatures compatible with many substrates, including conventional front-end silicon and compound semiconductors. Vertical silicon structures demonstrate the ability of laser crystallization to enable new device structures using different substrates as seed material. The diodes fabricated with single crystal silicon seeded from silicon wafers outperform epitaxially-grown diodes of the same geometry.

Separately, a process for building LED arrays is developed and characterized. Given of the extreme brightness of LEDs and the ability to structure the light output using the developed photolithographic method, display applications, in particular projection displays, are explored. The processes used to fabricate the laser-crystallized thin film transistors in chapter 2 and the LED arrays in chapter 3 are designed

to be fully compatible. This allows for the monolithic integration of the brightest controllable light source, LEDs, with high mobility, line-scan SLS transistors, and enables applications such as active-matrix displays where both are required.

To investigate the effects of using laser crystallization for all these integration concepts, finite-difference simulations are performed and show substrate temperatures to remain well within process tolerances throughout the laser process. A more direct measurement is also performed on wafers with conventional front-end transistors, 300 nm of SiO_2, and 100 nm of amorphous silicon. After the amorphous silicon is laser-crystallized, the front-end transistor parameters are measured. Several important device characteristics are tracked across wafers with and without laser processing. The parameters show no measurable shifts in either n-channel or p-channel front-end devices, demonstrating the viability of using laser crystallization for three dimensional integrated circuits.

Finally, new concepts are developed using industry relevant low-k dielectrics as a thermal buffer instead of silicon dioxide in sequential lateral solidification, and preliminary work with the crystallization of copper is performed to improve back-end wiring performance, both of which extend the applicability of laser crystallization.

6.2 Future Work

The technology developed in this thesis has been explored in several key application areas, with future work planned for all of these areas.

6.2.1 Lumiode: High Brightness Microdisplays

Work from chapter 2 on laser crystallized thin film transistors and chapter 3 on integrated LED arrays is being integrated to form the base of a new startup company, Lumiode. The core innovation is the ability to build a microdisplay platform which when fully developed can achieve both a very small form factor and very high bright-

ness. This can then be used towards display applications (head-mounted displays, projectors, head-up displays) and non-display applications (3D scanning, new user interfaces). The focus is on fully developing an integrated process for fabrication of high performance silicon circuitry with optoelectronic III-V compound semiconductors, fig. 6.1, combining the advantages from both material sets. This method is uniquely suited to transform the display industry by enabling the integration of LED arrays and control circuits on a single substrate.

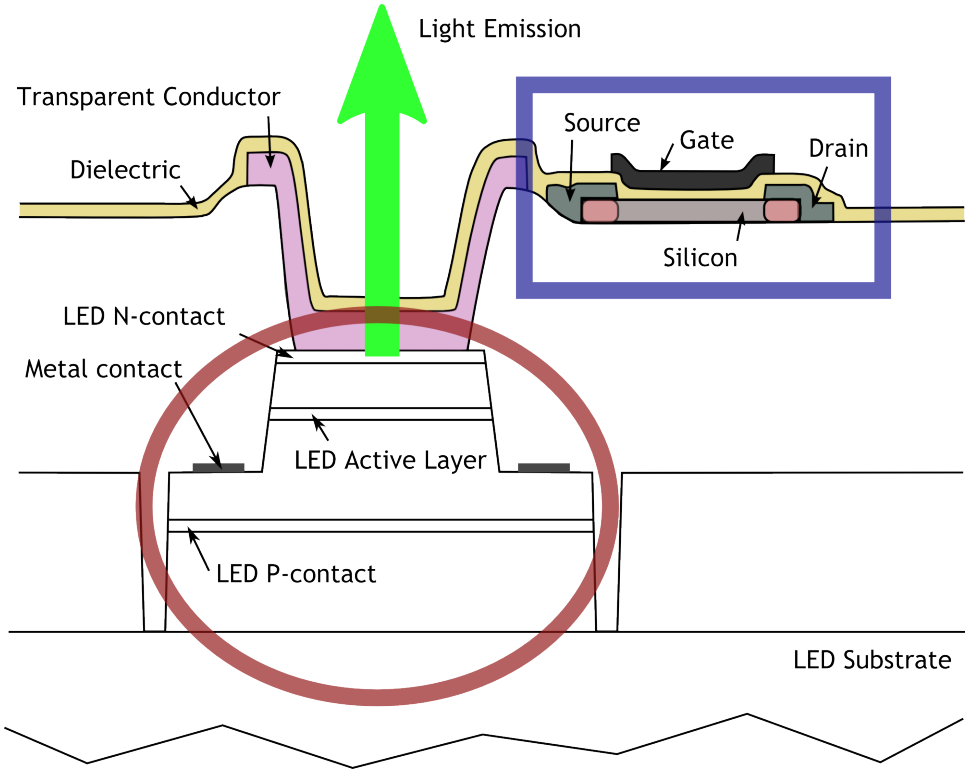


Figure 6.1: Integration of SLS thin film transistor process, from chapter 2, with LED array process, from chapter 3. The monolithically integrated system incorporates advantages of both systems.

The LED work presented in chapter 3 is built on an aluminum gallium arsenide wafer which emits red light. However, green, blue, and ultraviolet LEDs rely on the gallium nitride system of materials. Planned future work is based on indium gallium

nitride wafers which emit in the green and ultraviolet wavelengths. A facility with chlorine-plasma based etch chemistry has been identified and work with these wafers has started [112][113][114]. Fig. 6.2 shows a cross section of the first etched wafer. Further characterization and optimization is being performed.

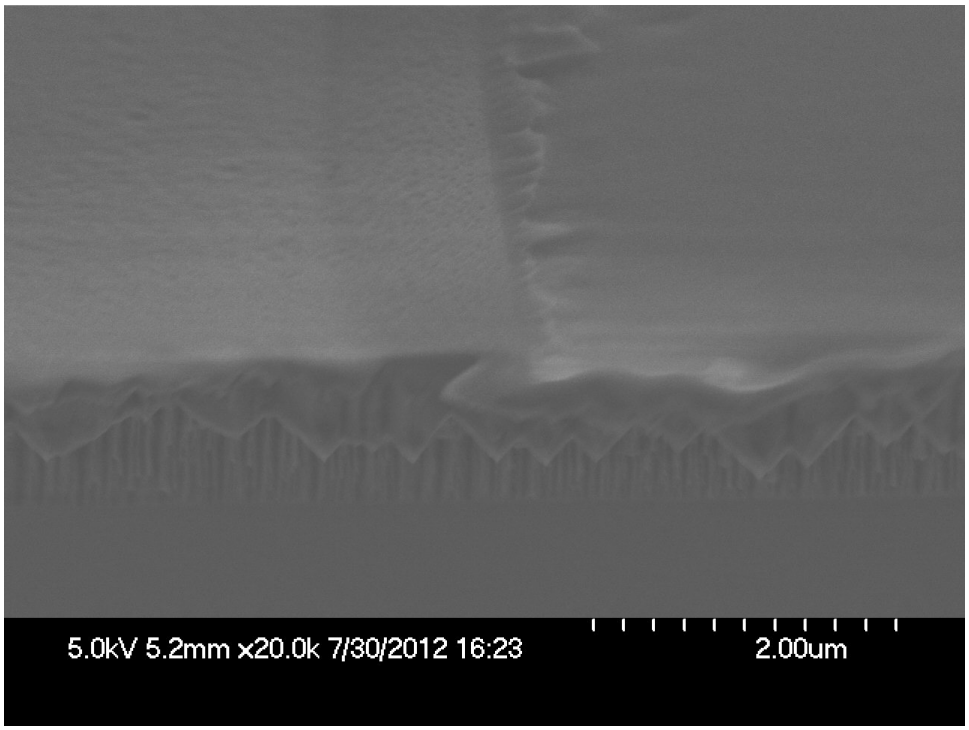


Figure 6.2: Cross sectional scanning electron micrograph of green LED wafer.

Other key technical questions include:

- What combination of laser annealing energy and contact metal minimizes contact resistance?
- How does the LED array process scale with pixel size and increasing resolution?
- How do transistor device characteristics scale with size?
- What is the minimum transistor length that can be fabricated?
- What is the uniformity of the SLS transistors after the laser process?

- How do grain boundary defects affect transistor performance?

6.2.2 Three-Dimensional Integrated Circuits

The work on three-dimensional integrated circuits shows promise and will be continued through active collaborations between the Columbia Laboratory for Unconventional Electronics and IBM. Chapter 4 discussed the use of laser crystallized silicon material for diodes, and showed no effect of the laser process on standard front-end CMOS devices. Work going forward will continue optimization of the diode process and integration of this vertical device architecture with other front-end CMOS devices to form a fully functional system.

Having diode devices enables applications where simple rectification is needed, but the vertical architecture concept can be further advanced by fabricating field effect transistor devices. Starting with the same vertical column structure of laser crystallized silicon, a wrap-around gate dielectric and gate electrode can be fabricated. With a wrap-around gate, the transistor channel length is defined by the height of the vertical structure, and the transistor channel width is defined by the diameter of the vertical structure. The beginning of the process would be very similar to the vertical diodes described in chapter 4, where amorphous silicon is deposited in via holes etched into silicon dioxide. The amorphous silicon will then be laser crystallized into the polycrystalline material, which will form the active material for the transistor. After chemical mechanical polishing of the polycrystalline silicon surface, the supporting silicon dioxide is etched away, leaving only the laser crystallized polycrystalline pillars. A gate dielectric is then grown around the diameter and a gate electrode deposited. Finally, a last electrode can be deposited on the top surface to form the drain electrode of the device. The full transistor is then complete with a gate electrode wrapping around the vertical laser crystallized silicon and source and drain electrodes on the top and bottom.

Other possible device architectures include building lateral transistor structures

from chapter 2 further into the back-end, for example, directly on low-k dielectrics for non-critical integrated circuits. This concept can be extended to building many stacked active layers with the proper thermal buffer between each layer. When designed properly, this could offer a virtually unlimited number of active layers with high mobility transistors, leaving the front-end area to be used only for the functions which require very high mobilities. In addition, other specialized functionality can be built into the back-end such as transistors which support high voltage switching or photo-detecting devices for interfacing with the external environment.

6.2.3 Crystallization of Copper

Investigations on laser recrystallization of copper will continue at GlobalFoundries. Early work shows the viability of laser annealing as a method to change the copper microstructure. Future work includes examination of the change in microstructure caused by the laser melting and recrystallization through cross sectional microscopy techniques. Direct measurements of resistivity in copper wires of varying widths will be made to determine the electrical characteristics of the new microstructure. Investigation of heat transfer to the front-end transistor devices, similar to work described in Chapter 4, will be performed to ensure there are no adverse effects on standard CMOS transistors. Finally, work will continue on varying parameters in the laser crystallization method, such as using scanning laser techniques to preferentially grow long grains along the direction of electrical conduction.

Appendix A

Integration of Foundry CMOS with Organic Light Emitting Diodes

A.1 Introduction

Integrated circuit design has become increasingly complex to meet the demands of expanded functionality, smaller transistor sizes, and increased levels of integration. This trend is apparent in microchip design and manufacturing where multi-core processors, integrated memory controllers, graphics processing unit, etc., all fit on a single die [115]. In the design phase, there are many simulation, layout, and error-checking software tools to help troubleshoot errors, but debugging a failure after fabrication is a much more challenging problem.

Ideally, when debugging a CMOS chip, the exact state of each signal within the chip is known. With knowledge of all the internal states, chip designers can apply a software patch or revise a processor design to find and fix any issues. In addition to debugging problems, knowing the signal states is a means of verifying the authenticity of the original design. With global outsourcing of fabrication facilities, there is a chance that designs can be modified maliciously and if undetected, can lead to security issues.

A traditional CMOS debugging technique is scan-design, which attempts to probe as many internal states as possible. In this technique, long strings of registers operate in two modes. In scan-mode, the registers are connected in a long chain as initial condition data is inputted into the chip. In run-mode, the clock signal is run once, and the registers feed the initial conditions to the logic circuits and simultaneously store the output data from the logic circuits. The registers are then placed again in scan-mode, and the output data is read-out as the next set of initial conditions are inputted. [116]

This method does not use many input/output pads, but these circuits are built directly on the front-end and utilizes valuable active device area. Additionally, since this is a serial process, the initial conditions and data need to be scanned in and out. This ultimately limits the speed at which this test can run and the number of internal states that can be probed.

By integrating organic LEDs with silicon circuits, we can use the light emitted from organic LEDs to optically probe many internal signals at once in a parallel fashion. This offers a means of high-throughput testing as thousands of points can be read at a single time. The overall device is similar to the organic LED-based microdisplays from eMagin and MicroOLED where OLEDs are built directly on CMOS circuits.

In this work, a microchip was designed and fabricated with a commercial foundry service to investigate opportunity for using OLEDs as a chip testing platform. Test boards were built, and preliminary fabrication work of OLEDs on the custom CMOS chip was executed.

A.2 Circuit Design and Layout

A test chip was taped out in 65 nm technology fabricated at UMC. Various test circuits were built to test the functionality of the chip and the viability of using OLED as a method for debug testing. Fig. A.1 shows a micrograph of the completed custom

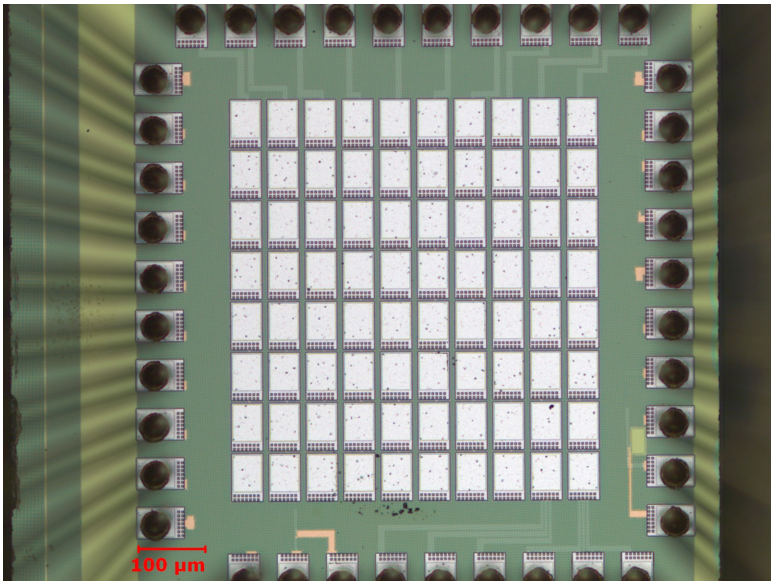


Figure A.1: Micrograph CMOS chip which supports direct integration with Organic Light Emitting Diodes.

designed CMOS chip. The periphery consists of 39 wirebond pads for connection with external circuits. The center of the chip consists of an 8 x 10 array of bond pads which interface with the organic LED materials later deposited.

Fig. A.2 and A.3 annotate each part of the chip layout and the different test circuits for each section. The CMOS chip has five different test circuits, three OLED test circuits and two tests of individual current mirrors. The orange, red, and blue outlines highlight the 8 x 8 array driven using current mirrors, 2 x 5 array driven using a digital NAND gate, and 2 x 3 array directly-addressed from corresponding wirebond pads, respectively. The light blue and green outlines highlight the two individual current mirror test circuits.

The CMOS chip is wirebonded into a standard 40-pin quad-flat no-leads (QFN) package based on the bonding digram in fig. A.4. The designed CMOS chip has 39 bond pads, each with its own electrostatic discharge (ESD) protection circuits. The bottom row has 9 bond bads versus 10 for all other rows to allow for easy identification

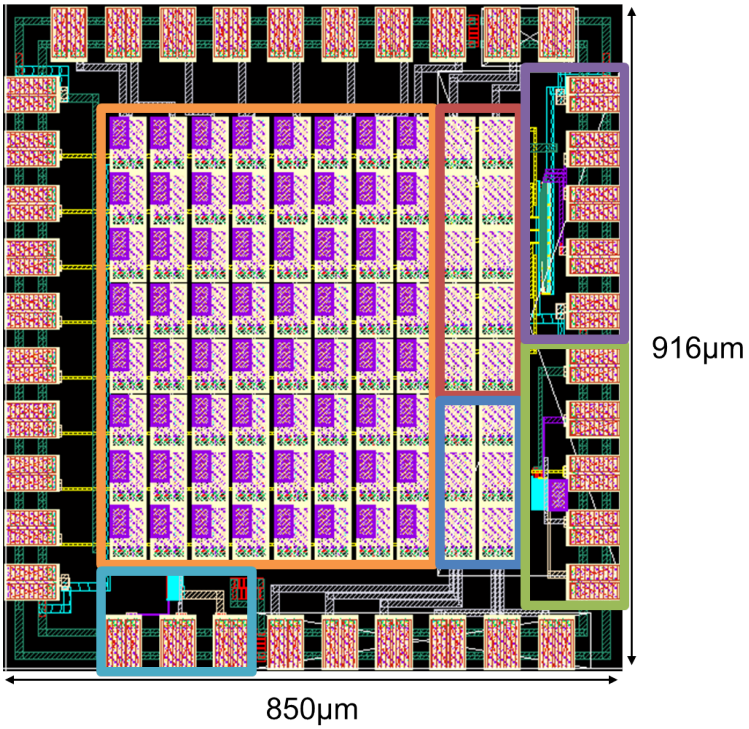


Figure A.2: Full layout with outlines for each section of the chip. Fabricated chip includes test circuits, and three different driving schemes.

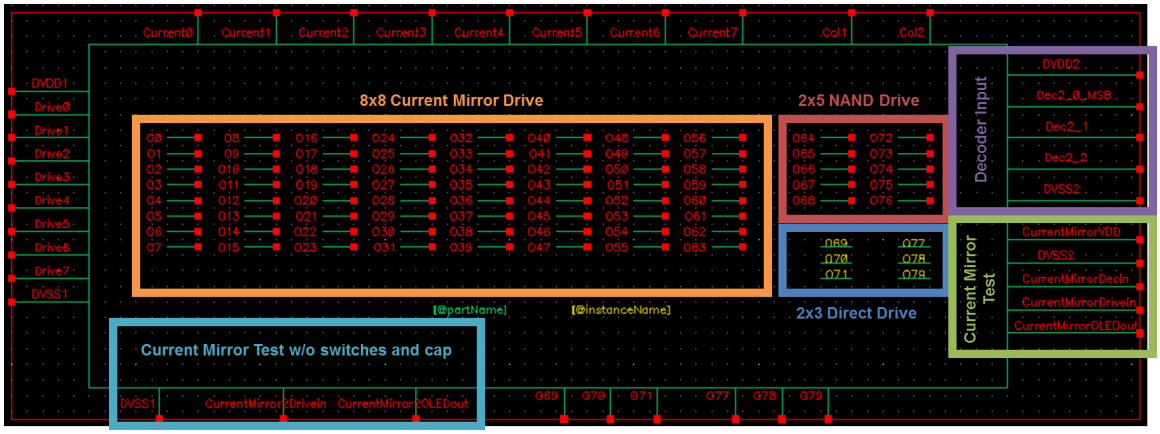


Figure A.3: Full symbol with all parts and input/output pins marked.

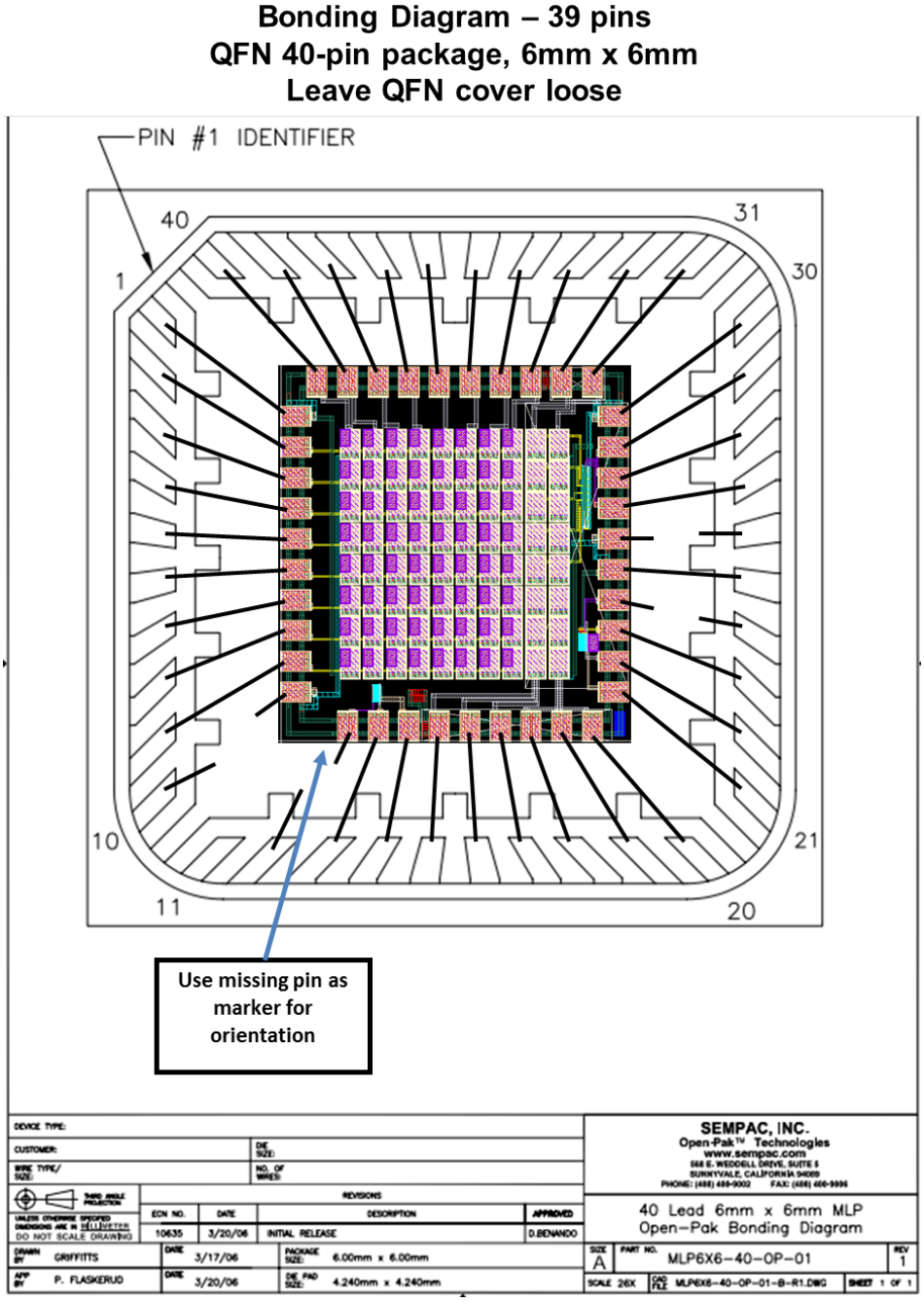


Figure A.4: Bonding diagram matching CMOS chip with pins on a 40-pin QFN package. Missing pin on bottom left corner is used as an orientation marker.

of chip orientation.

Pin definitions and corresponding numbers on the QFN package are given in table A.1. The chip is designed with two separate power domains, roughly split left side and right side. Power domain 1 supplies power for the 8 x 8 current mirror drive circuits, and one of the individual test circuits. Power domain 2 supplies power for the 2 x 5 digital drive, 2 x 3 directly addressed drive, and the second individual test circuit. A typical supply voltage of 2.5 V is required. When testing, power is only supplied to one side of the chip.

A.2.1 Directly Addressed

The first of three OLED driving schemes is the simplest. Bond pads 15-20 are directly wired to an OLED opening, labeled O69-71 and O77-79. These allow for direct electrical testing of a single OLED and collection of important electrical characteristics, such as current-voltage characteristics. Each of the bond pads, including the OLED openings, have ESD protection circuits. The directly addressed pads are in power domain 2.

A.2.2 Current Mirror

The second of three OLED driving schemes is based on an analog current mirror. This driving technique runs the 8 x 8 array which occupies the majority of the chip. This type of circuit is similar to OLED active-matrix display driving techniques. For each OLED opening, there are two inputs (Current_Drive_In, and Digital_In) and one output (OLEDout). Digital_In is an enable bit which turns on the switches to activate the current mirror circuit. This input is connected across the entire row, labeled Drive 0-7 on pin definitions. Setting this enable pin to high (2.5 V) turns on the current mirror circuit for the whole row and allows an analog current to be programmed into the mirror circuit.

The current mirror is designed with a 40:2 ratio. This is designed for a 5 μA input

Table A.1: Pin Definitions of CMOS Chip

Pin Name	**Pin Number on QFN Package**	**Definition**
DVDD1	1	VDD power domain 1 (typically 2.5 V)
DVSS1	10 & 12	VSS power domain 1 (typically 0 V)
Drive 0 - 7	2 - 9	Digital row input for current mirror switches
Current 0 - 7	40 - 33	Current column inputs for current mirrors
CurrentMirror2DriveIn	13	Test current mirror without switches or capacitor (Current Drive Input)
CurrentMirror2OLEDout	14	Test current mirror without switches or capacitor (Current Drive Output)
DVDD2	30	VDD power domain 2 (typically 2.5 V)
DVSS2	24 & 26	VSS power domain 2 (typically 0 V)
Col 1 - 2	32 - 31	Digital column signal for NAND gates
Dec_2_0_MSB	29	Most significant bit of decoder input
Dec_2_1	28	2nd bit for decoder input
Dec_2_2	27	Least significant bit of decoder input
O69 - 71, O77 - 79	15 - 20	Direct Drive OLED inputs
CurrentMirrorVDD	25	Test circuit for current mirror (VDD input)
CurrentMirrorDecIn	23	Test circuit for current mirror (Digitial switch input)
CurrentMirrorDriveIn	22	Test circuit for current mirror (Current Drive input)
CurrentMirrorOLEDout	21	Test circuit for current mirror (Current output)

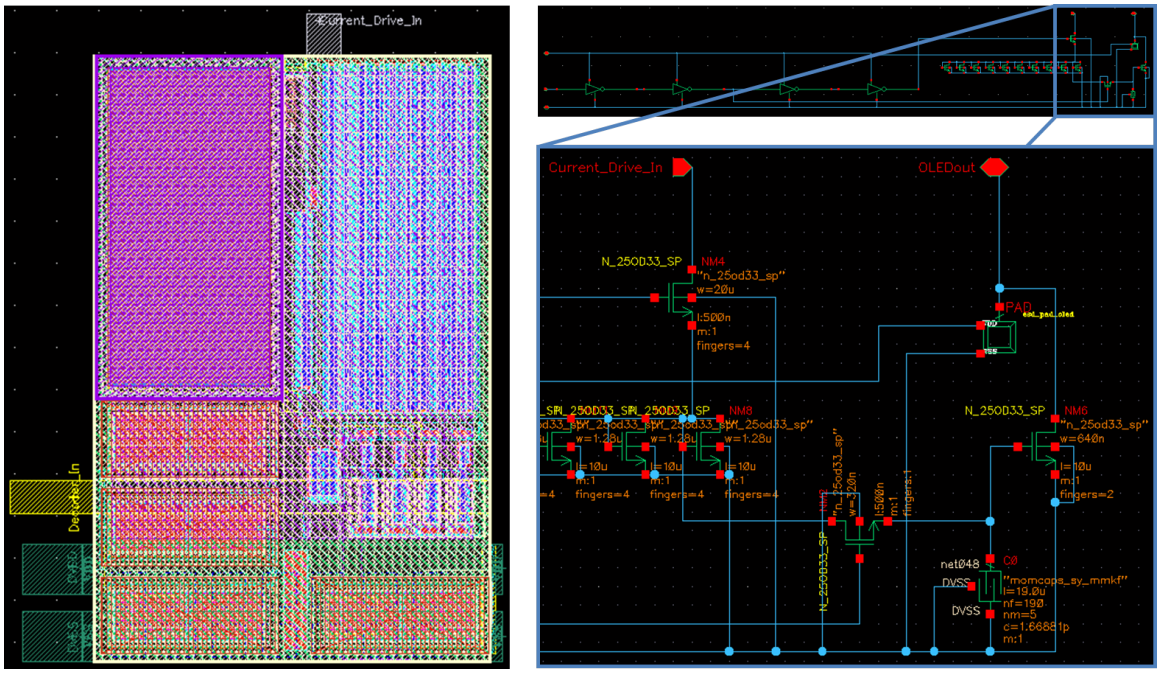


Figure A.5: Layout of current mirror circuit (left). Circuit schematic of current mirror (right).

current which outputs a 250 nA current for the OLED. This number was chosen as the optimal OLED current density for the size of the OLED opening.

Finally, an inverter delay chain is placed between the switches to ensure the capacitor stays charged when the switches are toggled.

The designed usage for the 8 x 8 current mirror array is as follows:

1. Current 0-7 is set to desired values for the first row.

2. Drive 0 is enabled (set to high, 2.5 V). This enables the first row to accept current input data.

3. Current 0-7 is set to desired values for each of the pixels. This programs the pixels and stores the desired current value in the pixel storage capacitor.

4. Drive 0 is disabled (set to 0 V), and Current 0-7 is set to the desired values for

the next row of pixels.

5. Drive 1 is enabled, and the values of Current 0-7 is programmed into the second row of pixels.

6. This continues for all following rows to program the entire 8 x 8 array. Drive 0-7 are pulsed continuously to supply new pixel values to the array.

In addition to the current mirrors used for driving the 8 x 8 OLED matrix, there are two individual current mirrors to verify functionality. These two circuits are on pins 12-14 and pins 21-25. As noted in the symbol drawing (Fig. A.3) and the pin definition table (Table A.1), pins 12-14 include only the current mirror without supporting switch transistors or storage capacitor, whereas pins 21-25 include the exact circuit used on the OLED openings.

A.2.3 NAND Digital Drive

The third OLED driving scheme uses all digital signals to turn the OLEDs on and off. This serves to simulate the environment on a standard CMOS chip where the signals of interest being probed are signals from a logic gate. Fig. A.6 shows the layout and circuit schematic for this NAND digital driving scheme. The circuit schematic consists of a single AND gate and an inverter. The AND gate emulates a debug logic signal. The inverter serves as a buffer between the logic signal and the output for the OLED. This drive scheme allows input of two digital signals to turn the OLED on or off.

A decoder was also designed and incorporated to reduce the number of wirebonds required. The decoder layout and schematic is shown in fig. A.7. The decoder uses 3 inverters and 8 AND gates. There are three inputs, Dec_2_0, Dec_2_1, and Dec_2_0 corresponding to the three binary bits and five outputs (in-use) corresponding to the five rows in the 2 x 5 NAND Drive matrix.

The designed usage for the 2 x 5 current mirror array is as follows:

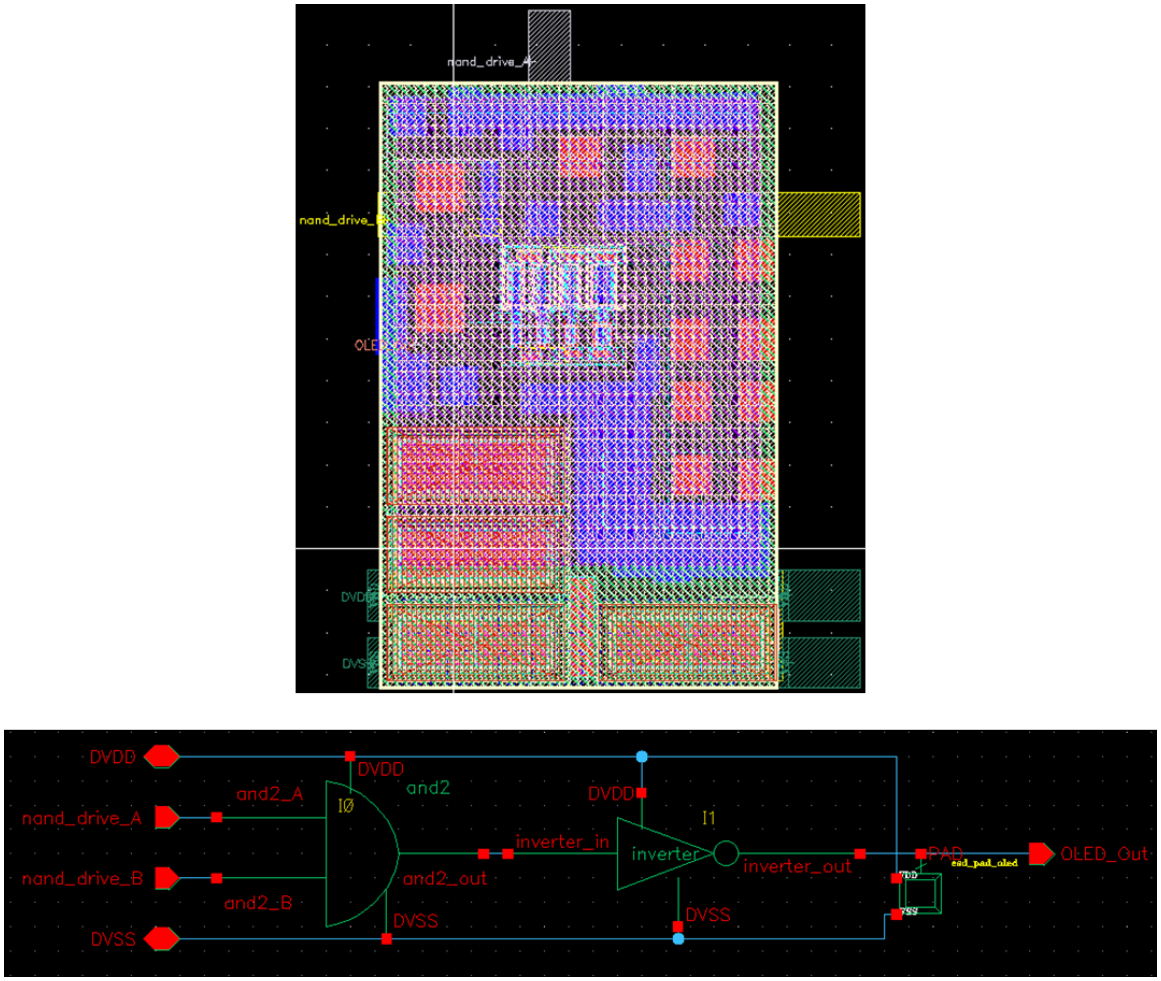


Figure A.6: Layout of NAND circuit (top). Abstracted circuit schematic of NAND with OLED bond pad (bottom).

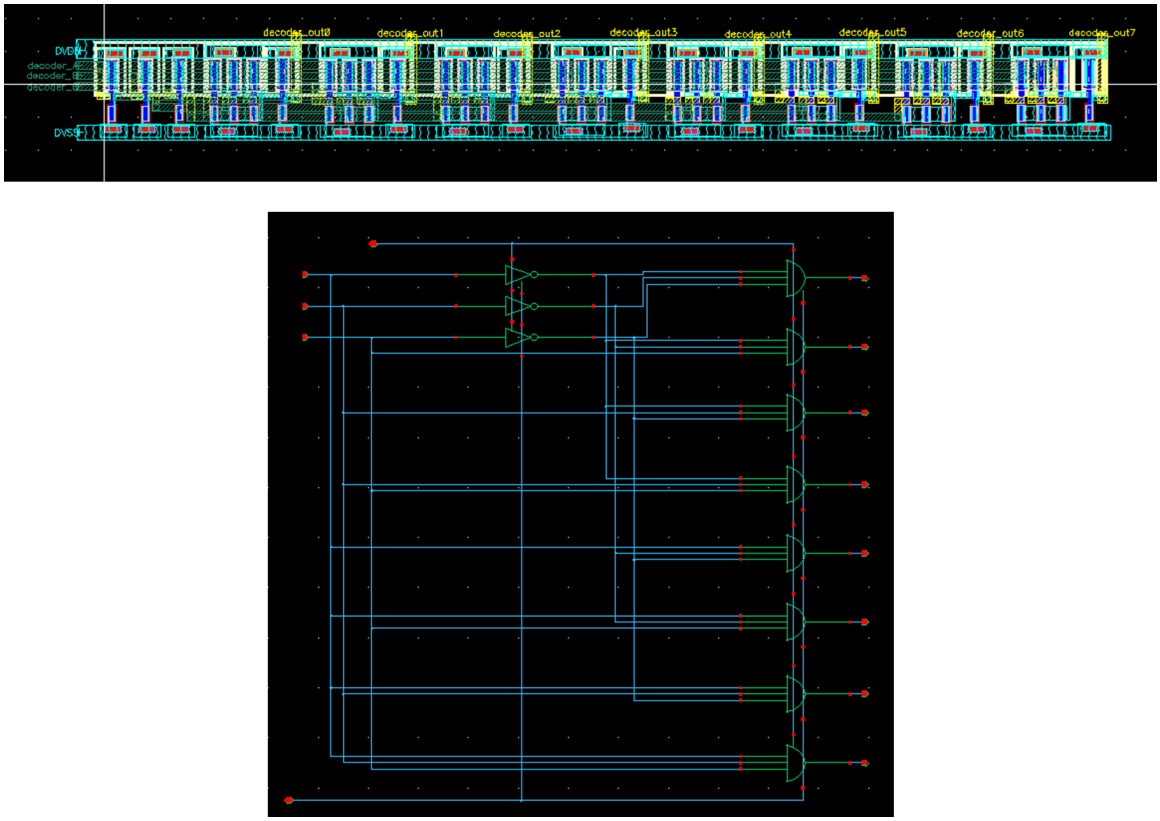


Figure A.7: Layout of decoder circuit (top). Circuit schematic of decoder circuit (bottom).

1. Col 1-2 is set to the desired digital values for the first row, either 0 V or 2.5 V.
2. Decoder bits, Dec_2_0_MSB, Dec_2_1, and Dec_2_2 are set to (0, 0, 0) switching the first row on.
3. Decoder bits are then set to (1, 1, 1) and Col 1-2 is set to desired digital values for second row.
4. Deocder bits are set to (0, 0, 1), enabling the second row.
5. This sequence continues for the five available rows.

Parts of this circuit can be tested using a probe station to probe the OLED

openings and apply the desired voltage stimulus to Col 1-2 and the decoder inputs.

A.3 Test Circuit Board Design

A test bed was designed to test each of the different drive techniques described in the section above. The test bed is based around the Arduino Mega microcontroller platform. The Arduino platform offers a simple programming interface and the Mega-version offers the necessary number of outputs to control each section of the designed CMOS chip.

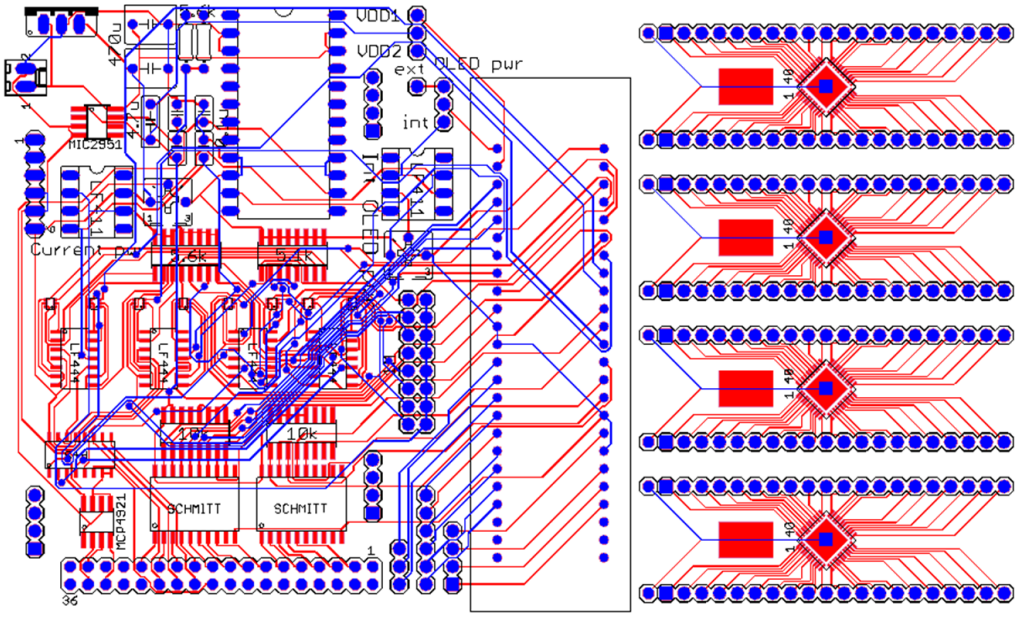


Figure A.8: Printed Circuit Board as designed. PCB interfaces with Arduino control and connects through a 40-pin Zero-Insertion-Force socket to interface with CMOS chip. On the right are four QFN to DIP printed circuit boards.

A custom printed-circuit-board (PCB), shown as designed in fig. A.8, interfaces the Arduino Mega with a 40-pin Zero-Insertion-Force (ZIF) socket. A ZIF socket was used to allow for fast changes between test samples. Many of the components on the

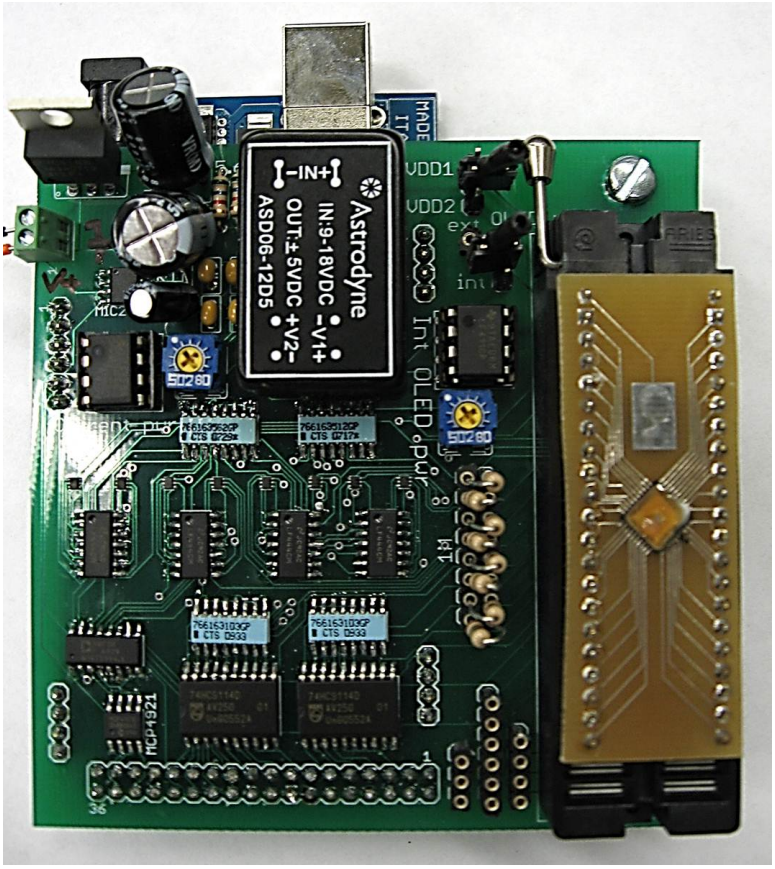


Figure A.9: Photograph of test board. CMOS chip in QFN package shown at top, soldered to a DIP interface board. Electronics are fully controlled with an Arduino Mega microcontroller.

PCB are surface mounted to reduce the space required and there are several areas where jumpers are used to select certain test options. A PCB was designed to convert the QFN packaged CMOS chip to a dual-in-line (DIP) package. This board design is again shown in fig. A.8, on the right side of the layout.

A photograph of the full test bed, fig. A.9, displays all three pieces. The Arduino Mega lies underneath a custom PCB for power and interface controls, and a 40-pin QFN to 42-pin DIP adapter with a fully processed CMOS chip is soldered on.

A.4 Experimental Results

The CMOS chips are wirebonded into the QFN package by an external wirebonding source. After wirebonding, chips are only handled in the packaged state. The QFN package is first soldered into the QFN to DIP adapter. Then wirebonds are protected using an SU-8 process in order to keep the organic materials from shorting the wirebond signals. Lastly, the organic materials are deposited across the top of the whole package.

A.4.1 Wirebond Protection

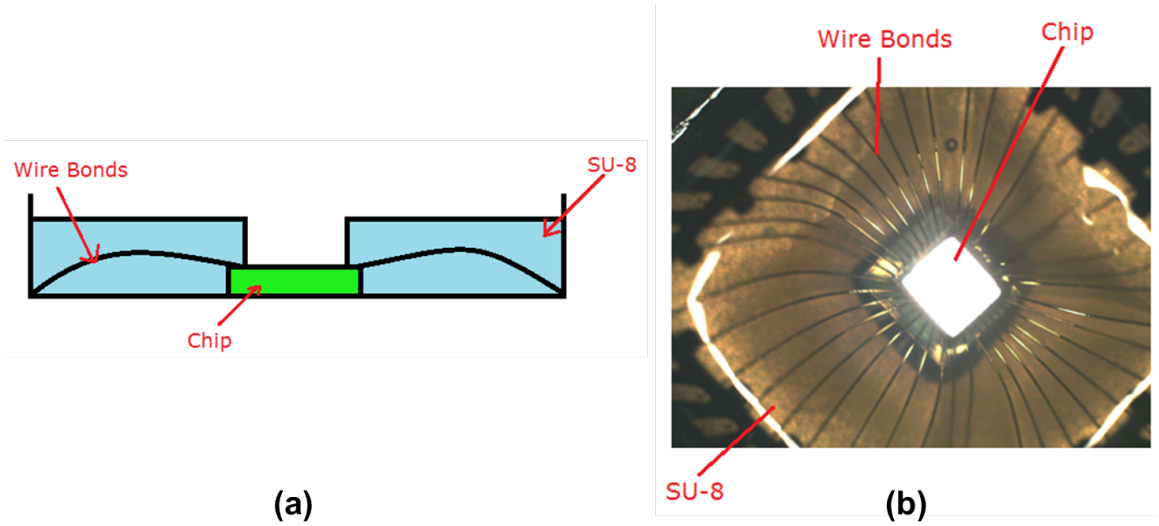


Figure A.10: (a) Cross sectional schematic of CMOS chip wirebonded into QFN package. The wirebonds are covered with SU-8 and an opening is defined to expose the CMOS surface. (b) Micrograph of SU-8 on chip with defined opening.

Because shadow masking and other masking techniques are not possible with the wirebonds already in place, an encapsulation process is developed to seal the wirebonds for further processing while keeping the center of the CMOS chip open, fig. A.10. SU-8 is an epoxy-based photo-imagable polymer which allows for very

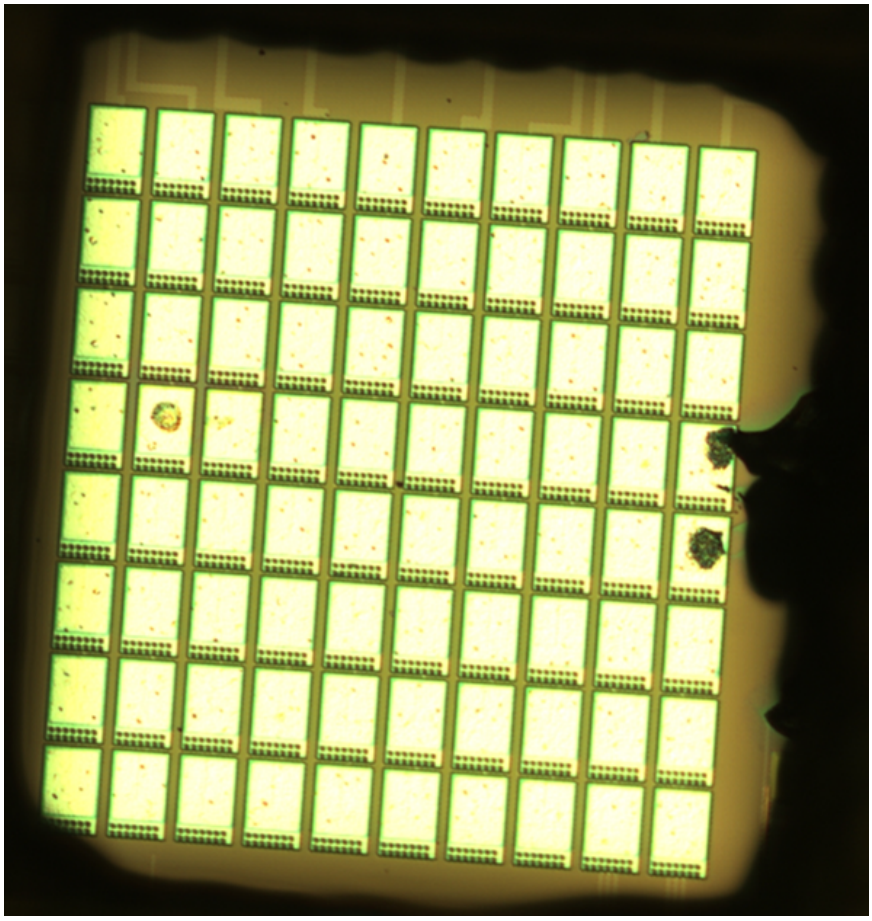


Figure A.11: Micrograph of SU-8 on chip with defined opening.

thick, high aspect ratio features. The SU-8 is first carefully dropped onto the surface of the chip and allowed to flow around all the wirebonds in a first pre-bake step. The adapter board - QFN package - CMOS chip stack is then placed in a mask aligner and exposed with a custom photomask to define the center opening. After a UV exposure, the SU-8 is developed and the center part of the chip is exposed. Further bakes are performed to finish curing of the SU-8. Fig. A.11 shows the surface of a CMOS chip with the SU-8 covering and protecting the surrounding wirebonds.

Table A.2: Material Stack for Organic LED

Material	**Thickness (nm)**	**Purpose**
Gold	40	Cathode
E105	80 - 100	Hole Transport Layer
Alq3	80 - 100	Electroluminescent Layer
Magnesium/Silver	10	Hole Injection Layer
Aluminum on CMOS bond pad	Substrate	Anode

A.4.2 Organic LED Fabrication

After wirebond protection, the CMOS chip is placed in a thermal evaporator and organic materials are deposited to complete the OLED stack. Table A.2 summarizes a simple OLED stack. At the bottom is the initial aluminum layer on the surface of the chip. This layer is used as the anode of the OLED. Next, a magnesium and silver alloy is deposited as a Hole Injection Layer. This is followed by two organic layers which makes up the electroluminescent and hole transport layers. Lastly, a thin layer of gold is deposited as a transparent cathode.

The organic layers are deposited twice as thick as the typical stack due to initial shorting issues. Looking at the OLED openings in the optical profilometer, fig. A.12 and A.13, the topography of the aluminum metal is visible. The passivation layer, as expected, is approximately 800 nm, but the roughness on the OLED openings is much larger than expected. On most of the OLED openings there are aluminum spikes which are 100 nm or taller. The thicker organic material layers helps prevent shorting from these aluminum spikes.

Initial current-voltage curves from the organic devices are shown in fig. A.14. These device exhibit limited diode characteristics but do not emit light. Further work is needed to optimize the OLED stack and refine fabrication steps for a fully integrated OLED and CMOS device.

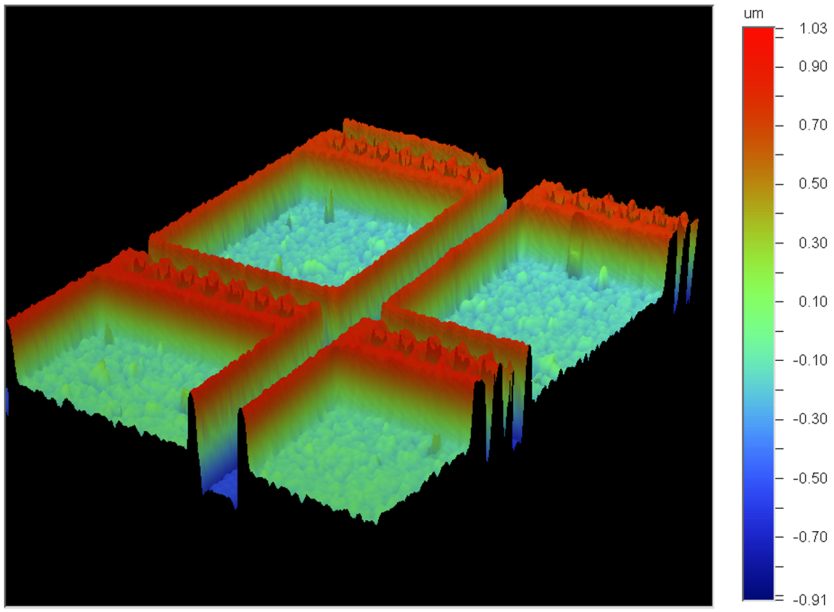


Figure A.12: Optical profilometer image of multiple bond pads. Total height difference is about 2 μm.

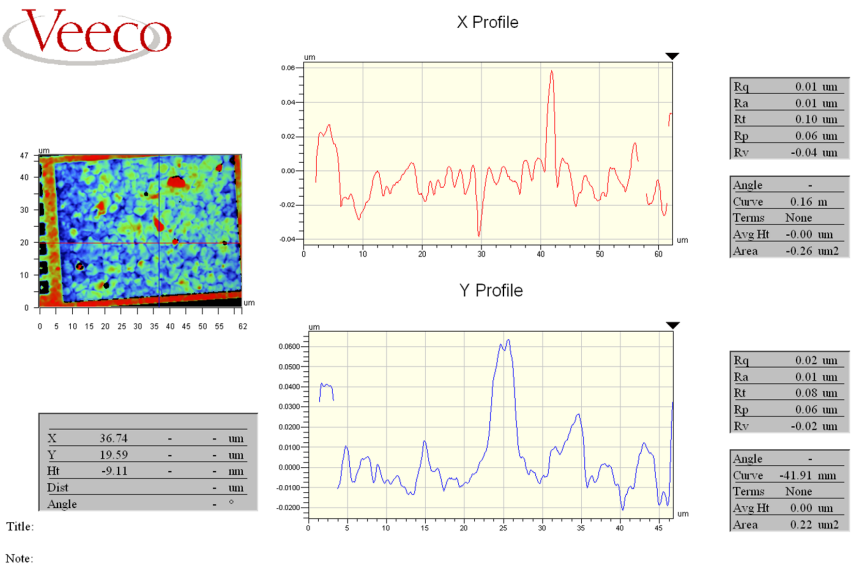


Figure A.13: Optical profilometer image of bond pad surface. Total height difference is about 0.1 μm.

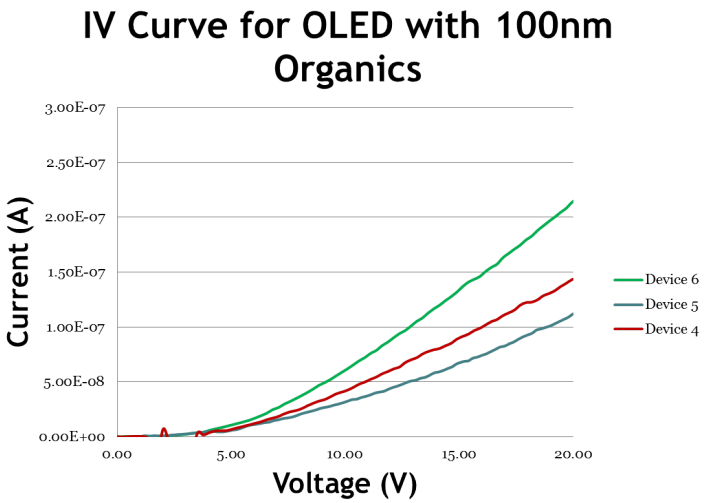


Figure A.14: Initial current-voltage characteristics of OLED devices.

A.5 Conclusion and Future Work

In this appendix, a custom CMOS chip was designed to test the viability of integrating OLEDs with conventional CMOS as a means of debugging silicon circuits. The CMOS chip was designed with several driving methods, emulating the signals typically found on microprocessors. New processes were developed to protect the wirebonds during further thermal deposition of materials, and a preliminary OLED stack was integrated and tested.

Further improvements can be made on both the OLED material stack and process steps. The final electrode is currently a transparent gold layer, which has issues in covering the topology of the CMOS chip. This can be improved by adding a transparent conductor, such as Indium Tin Oxide, following the gold layer. A second improvement can be made by adding a chemical mechanical polishing step to remove the passivation layer and smooth out the 100nm spikes on the aluminum bond pads. Both additional steps will help improve the yield and uniformity of results of this concept.

Bibliography

[1] K. J. Kuhn, "Considerations for Ultimate CMOS Scaling," *IEEE Transactions on Electron Devices*, vol. 59, pp. 1813–1828, July 2012.

[2] K. J. Kuhn, "CMOS scaling for the 22nm node and beyond: Device physics and technology," in *Proceedings of 2011 International Symposium on VLSI Technology, Systems and Applications*, pp. 1–2, IEEE, Apr. 2011.

[3] K. Kuhn, "CMOS scaling beyond 32nm: challenges and opportunities," *Design Automation Conference, 2009. DAC'09. 46th ...*, pp. 310–313, 2009.

[4] D. Buchanan, D. Frank, K. Ismail, G. Sai-Halasz, R. Viswanathan, H.-J. Wann, and S. Wind, "CMOS scaling into the nanometer regime," *Proceedings of the IEEE*, vol. 85, pp. 486–504, Apr. 1997.

[5] J. Smith, "Fluidic self-assembly of microstructures and its application to the integration of GaAs on Si," *Proceedings IEEE Micro Electro Mechanical Systems An Investigation of Micro Structures, Sensors, Actuators, Machines and Robotic Systems*, pp. 279–284, 1994.

[6] W. P. Giziewicz and C. G. Fonstad, "Optoelectronic integration using aligned metal-to-semiconductor bonding," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 20, no. 3, p. 1052, 2002.

[7] G. Balakrishnan, S. Huang, L. R. Dawson, Y.-C. Xin, P. Conlin, and D. L. Huffaker, "Growth mechanisms of highly mismatched AlSb on a Si substrate," *Applied Physics Letters*, vol. 86, no. 3, p. 034105, 2005.

[8] G. Balakrishnan, A. Jallipalli, P. Rotella, S. Huang, A. Khoshakhlagh, A. Amtout, S. Krishna, L. R. Dawson, and D. L. Huffaker, "Room-Temperature Optically Pumped (Al)GaSb Vertical-Cavity Surface-Emitting Laser Monolithically Grown on an Si(1 0 0) Substrate," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 12, pp. 1636–1641, Nov. 2006.

[9] M. Ogihara, H. Fujiwara, M. Mutoh, T. Suzuki, T. Igari, T. Sagimori, H. Kurokawa, T. Kaneto, H. Furuta, I. Abiko, and M. Sakuta, "LED array integrated with Si driving circuits for LED printer printhead," *Electronics Letters*, vol. 42, no. 15, p. 881, 2006.

[10] E. P. G. Smith, L. T. Pham, G. M. Venzor, E. M. Norton, M. D. Newton, P. M. Goetz, V. K. Randall, A. M. Gallagher, G. K. Pierce, E. A. Patten, R. A. Coussa, K. Kosai, W. A. Radford, L. M. Giegerich, J. M. Edwards, S. M. Johnson, S. T. Baur, J. A. Roth, B. Nosho, T. J. Lyon, J. E. Jensen, and R. E. Longshore, "HgCdTe focal plane arrays for dual-color mid- and long-wavelength infrared detection," *Journal of Electronic Materials*, vol. 33, pp. 509–516, June 2004.

[11] J. Day, J. Li, D. Y. C. Lie, C. Bradford, J. Y. Lin, and H. X. Jiang, "III-Nitride full-scale high-resolution microdisplays," *Applied Physics Letters*, vol. 99, no. 3, p. 031116, 2011.

[12] R. T. Howe and C. G. Sodini, *Microelectronics: An Integrated Approach*. Prentice Hall Upper Saddle River, NJ, 2008.

[13] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*. John Wiley & Sons, 2007.

[14] R. Bergmann and J. Werner, "The future of crystalline silicon films on foreign substrates," *Thin Solid Films*, vol. 403-404, pp. 162–169, Feb. 2002.

[15] T. Sameshima, S. Usui, and M. Sekiya, "XeCl Excimer laser annealing used in the fabrication of poly-Si TFT's," *IEEE Electron Device Letters*, vol. 7, pp. 276–278, May 1986.

[16] L. Mariucci, a. Pecora, R. Carluccio, and G. Fortunato, "Advanced excimer laser crystallization techniques," *Thin Solid Films*, vol. 383, pp. 39–44, Feb. 2001.

[17] A. Voutsas, "Advances in laser annealing technology for poly-Si material engineering and ultra-high-performance device fabrication," in *10th IEEE International Conference of Advanced Thermal Processing of Semiconductors*, pp. 183–191, IEEE, 2002.

[18] J. S. Im, H. J. Kim, and M. O. Thompson, "Phase transformation mechanisms involved in excimer laser crystallization of amorphous silicon films," *Applied Physics Letters*, vol. 63, no. 14, p. 1969, 1993.

[19] M. Hatano, S. Moon, M. Lee, K. Suzuki, and C. P. Grigoropoulos, "Excimer laser-induced temperature field in melting and resolidification of silicon thin films," *Journal of Applied Physics*, vol. 87, no. 1, p. 36, 2000.

[20] P. van der Wilt, M. Kane, A. Limanov, A. Firester, L. Goodman, J. Lee, J. Abelson, A. Chitu, and J. S. Im, "Low-Temperature Polycrystalline Silicon Thin-Film Transistors and Circuits on Flexible Substrates," *MRS Bulletin*, vol. 31, pp. 461–465, Jan. 2006.

[21] R. S. Sposili and J. S. Im, "Sequential lateral solidification of thin silicon films on SiO2," *Applied Physics Letters*, vol. 69, no. 19, p. 2864, 1996.

[22] J. S. Im, R. S. Sposili, and M. a. Crowder, "Single-crystal Si films for thin-film transistor devices," *Applied Physics Letters*, vol. 70, no. 25, p. 3434, 1997.

[23] H. Kahlert, B. Burghardt, F. Simon, and M. Stopka, "High resolution optics for thin Si-film crystallization using excimer lasers: present status and future development," in *Proceedings of SPIE*, vol. 5004, p. 20, 2003.

[24] M. Crowder, M. Moriguchi, Y. Mitani, and a.T. Voutsas, "Parametric investigation of SLS-processed poly-silicon thin films for TFT applications," *Thin Solid Films*, vol. 427, pp. 101–107, Mar. 2003.

[25] P. van der Wilt, "A hybrid approach for obtaining orientation-controlled single-crystal Si regions on glass substrates," *Proceedings of SPIE*, vol. 6106, no. Im, pp. 61060B–61060B–15, 2006.

[26] J. S. Im, M. A. Crowder, R. S. Sposili, J. P. Leonard, H. J. Kim, J. H. Yoon, V. V. Gupta, H. Jin Song, and H. S. Cho, "Controlled Super-Lateral Growth of Si Films for Microstructural Manipulation and Optimization," *physica status solidi (a)*, vol. 166, pp. 603–617, Apr. 1998.

[27] Y. Jung, J. Yoon, M. Yang, W. Park, H. Soh, H. Cho, A. Limanov, and J. Im, "Low Temperature Polycrystalline Si TFTs Fabricated with Directionally Crystallized Si Film," *MRS Proceedings*, vol. 621, Mar. 2000.

[28] D. S. Knowles, J.-y. Park, C. Im, P. Das, T. Hoffman, B. Burfeindt, H. Muenz, A. Herkommer, P. C. van der Wilt, A. B. Limanov, and J. S. Im, "P-59: Thin-beam Crystallization Method for Fabrication of LTPS," *SID Symposium Digest of Technical Papers*, vol. 36, no. 1, p. 503, 2005.

[29] M. Crowder, P. Carey, P. Smith, R. Sposili, H. Cho, and J. Im, "Low-temperature single-crystal Si TFTs fabricated on Si films processed via sequential lateral solidification," *IEEE Electron Device Letters*, vol. 19, no. 8, pp. 306–308, 1998.

[30] B. A. Turk, P. C. Van der Wilt, R. S. Sposili, A. B. Limanov, and J. S. Im, "Optimization of sequential lateral solidification processes for high performance TFT applications," *202nd Meeting of the Electrochemical Society*, p. 1, 2002.

[31] M. Kang, S. Kim, and H. Kim, "Improved Uniformity of Sequential Lateral Solidification Thin-Film Transistors," *Electron Device Letters, IEEE*, vol. 32, no. 6, pp. 767–769, 2011.

[32] S.-J. Lee, S.-W. Lee, K.-E. Lee, M.-S. Yang, W.-S. Shin, M.-C. Jun, Y.-S. Yang, and Y.-K. Hwang, "Electrical characterization of polycrystalline silicon thin film transistors crystallized by a new alignment sequential lateral solidification process," *Physica Scripta*, vol. 83, p. 055802, May 2011.

[33] M. Exarchos, D. Moschou, G. Papaioannou, D. Kouvatsos, a. Arapoyanni, and a.T. Voutsas, "On the study of p-channel thin-film transistors fabricated by SLS ELA crystallization techniques," *Thin Solid Films*, vol. 517, pp. 6375–6378, Oct. 2009.

[34] Y. Kim, C. Chung, S. Yun, J. Moon, D. Park, D. Kim, J. Lim, Y. Song, and J. Lee, "Large-grain polycrystalline silicon film by sequential lateral solidification on a plastic substrate," *Thin Solid Films*, vol. 493, pp. 192–196, Dec. 2005.

[35] M. G. Kane, L. Goodman, A. H. Firester, P. C. van der Wilt, A. B. Limanov, and J. S. Im, "100-MHz CMOS circuits directly fabricated on plastic using sequential laterally solidified silicon," *Journal of the Society for Information Display*, vol. 15, no. 7, p. 471, 2007.

[36] F. Lemmi, W. Chung, S. Lin, P. Smith, T. Sasagawa, B. Drews, A. Hua, J. Stern, and J. Chen, "High-Performance TFTs Fabricated on Plastic Substrates," *IEEE Electron Device Letters*, vol. 25, pp. 486–488, July 2004.

[37] J. P. Leonard and J. S. Im, "Stochastic modeling of solid nucleation in supercooled liquids," *Applied Physics Letters*, vol. 78, no. 22, p. 3454, 2001.

[38] M. a. Green and M. J. Keevers, "Optical properties of intrinsic silicon at 300 K," *Progress in Photovoltaics: Research and Applications*, vol. 3, no. 3, pp. 189–192, 1995.

[39] G. E. Jellison, "Optical absorption of silicon between 1.6 and 4.7 eV at elevated temperatures," *Applied Physics Letters*, vol. 41, no. 2, p. 180, 1982.

[40] Y. Jung, J. Yoon, M. Yang, W. Park, H. Soh, H. Cho, A. Limanov, and J. Im, "The Dependence of Poly-Si TFT Characteristics on the Relative Misorientation Between Grain Boundaries and the Active Channel," *MRS Proceedings*, vol. 621, Mar. 2000.

[41] E. Persidis, H. Baur, F. Pieralisi, P. Schalberger, and N. Fruehauf, "Area laser crystallized LTPS TFTs with implanted contacts for active matrix OLED displays," *Solid-State Electronics*, vol. 52, pp. 455–461, Mar. 2008.

[42] K. K. Ong, K. L. Pey, P. S. Lee, a. T. S. Wee, X. C. Wang, and Y. F. Chong, "Dopant activation in subamorphized silicon upon laser annealing," *Applied Physics Letters*, vol. 89, no. 8, p. 082101, 2006.

[43] C. H. Poon, B. J. Cho, Y. F. Lu, M. Bhat, and A. See, "Multiple-pulse laser annealing of preamorphized silicon for ultrashallow boron junction formation," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 21, no. 2, p. 706, 2003.

[44] S. Whelan, V. Privitera, M. Italia, G. Mannino, C. Bongiorno, C. Spinella, G. Fortunato, L. Mariucci, M. Stanizzi, and a. Mittiga, "Redistribution and electrical activation of ultralow energy implanted boron in silicon following laser annealing," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 20, no. 2, p. 644, 2002.

[45] F. Lanzerath, D. Buca, H. Trinkaus, M. Goryll, S. Mantl, J. Knoch, U. Breuer, W. Skorupa, and B. Ghyselen, "Boron activation and diffusion in silicon and strained silicon-on-insulator by rapid thermal and flash lamp annealings," *Journal of Applied Physics*, vol. 104, no. 4, p. 044908, 2008.

[46] W. Skorupa, T. Gebel, R. a. Yankov, S. Paul, W. Lerch, D. F. Downey, and E. a. Arevalo, "Advanced Thermal Processing of Ultrashallow Implanted Junctions Using Flash Lamp Annealing," *Journal of The Electrochemical Society*, vol. 152, no. 6, p. G436, 2005.

[47] T. Gebel, "Flash lamp annealing with millisecond pulses for ultra-shallow boron profiles in silicon," *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, vol. 186, pp. 287–291, Jan. 2002.

[48] T. Ito, T. Iinuma, A. Murakoshi, H. Akutsu, K. Suguro, T. Arikado, K. Okumura, M. Yoshioka, T. Owada, Y. Imaoka, H. Murayama, and T. Kusuda, "10-15 nm Ultrashallow Junction Formation by Flash-Lamp Annealing," *Japanese Journal of Applied Physics*, vol. 41, pp. 2394–2398, Apr. 2002.

[49] E. F. Schubert and J. K. Kim, "Solid-state light sources getting smart.," *Science*, vol. 308, pp. 1274–8, May 2005.

[50] D. Steigerwald, J. Bhat, D. Collins, R. Fletcher, M. Holcomb, M. Ludowise, P. Martin, and S. Rudaz, "Illumination with solid state lighting technology," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 8, no. 2, pp. 310–320, 2002.

[51] E. Jang, S. Jun, H. Jang, J. Lim, B. Kim, and Y. Kim, "White-light-emitting diodes with quantum dot color converters for display backlights.," *Advanced materials (Deerfield Beach, Fla.)*, vol. 22, pp. 3076–80, July 2010.

[52] L.-s. L. C. D. Panels, H.-j. Chiu, and S.-j. Cheng, "LED Backlight Driving System for Large-Scale LCD Panels," *IEEE Transactions on Industrial Electronics*, vol. 54, pp. 2751–2760, Oct. 2007.

[53] C.-H. Lee, A. Sazonov, A. Nathan, and J. Robertson, "Directly deposited nanocrystalline silicon thin-film transistors with ultra high mobilities," *Applied Physics Letters*, vol. 89, no. 25, p. 252101, 2006.

[54] Z. Y. Fan, J. Y. Lin, and H. X. Jiang, "III-nitride micro-emitter arrays: development and applications," *Journal of Physics D: Applied Physics*, vol. 41, p. 094001, May 2008.

[55] Z. Gong, Y. F. Zhang, P. Kelm, I. M. Watson, E. Gu, and M. D. Dawson, "InGaN micro-pixellated light-emitting diodes with nano-textured surfaces and modified emission profiles," *Applied Physics A*, vol. 103, pp. 389–393, Mar. 2011.

[56] C.-W. Jeon, K.-S. Kim, and M. Dawson, "Fabrication of Two-Dimensional InGaN-Based Micro-LED Arrays," *Physica Status Solidi (a)*, vol. 192, pp. 325–328, Aug. 2002.

[57] H. M. Ku, C. Y. Huang, C. Z. Liao, and S. Chao, "Epitaxial Lateral Overgrowth of Gallium Nitride for Embedding the Micro-Mirror Array," *Japanese Journal of Applied Physics*, vol. 50, p. 04DG07, Apr. 2011.

[58] Z. J. Liu, K. M. Wong, C. W. Keung, C. W. Tang, and K. M. Lau, "Monolithic LED Microdisplay on Active Matrix Substrate Using Flip-Chip Technology," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 15, pp. 1298–1302, July 2009.

[59] H. Choi, C. Jeon, and M. Dawson, "High-Resolution 128 x 96 Nitride Microdisplay," *IEEE Electron Device Letters*, vol. 25, pp. 277–279, May 2004.

[60] P. Holm, W. Rhyne, B. Gable, S. Rogers, K. Jachimowicz, F. Richard, and D. Ackley, "Two-dimensional LED arrays for virtual display image sources," *IEEE Transactions on Electron Devices*, vol. 46, pp. 897–904, May 1999.

[61] Z. Gong, D. Massoubre, J. McKendry, H. X. Zhang, C. Griffin, B. Guilhabert, E. Gu, J. M. Girkin, M. D. Dawson, B. R. Rael, and R. K. Henderson, "Flip-chip, micro-pixellated InGaN light-emitting diode arrays: attractive sources for micro-displays, colour conversion, and fluorescence detection," *Physica Status Solidi (C)*, vol. 6, pp. S848–S851, June 2009.

[62] J.-P. Ao, "Monolithic Integration of GaN-based LEDs," *Journal of Physics: Conference Series*, vol. 276, p. 012001, Feb. 2011.

[63] S. X. Jin, J. Li, J. Y. Lin, and H. X. Jiang, "InGaN/GaN quantum well interconnected microdisk light emitting diodes," *Applied Physics Letters*, vol. 77, no. 20, p. 3236, 2000.

[64] C. W. Jeon, E. Gu, and M. D. Dawson, "Mask-free photolithographic exposure using a matrix-addressable micropixellated AlInGaN ultraviolet light-emitting diode," *Applied Physics Letters*, vol. 86, no. 22, p. 221105, 2005.

[65] L. Zhu, C. W. Ng, N. Wong, K. Y. Wong, P. T. Lai, and H. W. Choi, "Fiber-coupled Emissive Micro-Light-Emitting Diode Arrays," *SID DigestDigest*, pp. 526–529, 2009.

[66] M. B. Spitzer, "Fabrication of dense optoelectronic device arrays," in *Proceedings of SPIE*, vol. 2397, pp. 249–258, SPIE, 1995.

[67] V. Poher, N. Grossman, G. T. Kennedy, K. Nikolic, H. X. Zhang, Z. Gong, E. M. Drakakis, E. Gu, M. D. Dawson, P. M. W. French, P. Degenaar, and M. a. a. Neil, "Micro-LED arrays: a tool for two-dimensional neuron stimulation," *Journal of Physics D: Applied Physics*, vol. 41, p. 094014, May 2008.

[68] C. Grossmann, R. Stefan, U. Vogel, and G. Notni, "Ultra Small OLED Pico Projector," *Optik & Photonik*, no. 2, pp. 34–36, 2009.

[69] C. Grossmann, U. Vogel, U. Lippmann, S. Riehemann, and G. Notni, "Ultra Compact Projection System for Mobile Application," *SID Digest*, pp. 1774–1776, 2009.

[70] I. Cree, "Cree EZ1000 LEDs Datasheet CPR3CR Rev. A," 2006.

[71] S. Kim, E. Saeedi, D. Meldrum, and B. Parviz, "Self-Assembled Heterogeneous Integrated Fluorescence Detection System," in *Nano/Micro Engineered and Molecular Systems, 2007. NEMS'07. 2nd IEEE International Conference on*, pp. 927–931, IEEE, 2007.

[72] E. Saeedi, S. S. Kim, and B. A. Parviz, "Self-assembled inorganic micro-display on plastic," in *2007 IEEE 20th International Conference on Micro Electro Mechanical Systems (MEMS)*, no. January, pp. 755–758, IEEE, 2007.

[73] J.-H. Kim, D. H. Lim, and G. M. Yang, "Selective etching of AlGaAs/GaAs structures using the solutions of citric acid/H[sub 2]O[sub 2] and de-ionized H[sub 2]O/buffered oxide etch," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 16, p. 558, Mar. 1998.

[74] T. Kitano, "Selective wet etching for highly uniform GaAs/Al[sub 0.15]Ga[sub 0.85]As heterostructure field effect transistors," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, vol. 15, p. 167, Jan. 1997.

[75] G. C. DeSalvo, "Citric Acid Etching of GaAs[sub 1x]Sb[sub x], Al[sub 0.5]Ga[sub 0.5]Sb, and InAs for Heterostructure Device Fabrication," *Journal of The Electrochemical Society*, vol. 141, no. 12, p. 3526, 1994.

[76] V. W. Lee and I. Kymissis, "A directly addressed monolithic LED array as a projection source," *Journal of the Society for Information Display*, vol. 18, no. 10, p. 808, 2010.

[77] V. W. Lee and I. Kymissis, "75.2: A Passive-Matrix Inorganic LED Array as a Projection Source," *SID Display Week Conference*, pp. 1–3, 2012.

[78] S. X. Jin, J. Shakya, J. Y. Lin, and H. X. Jiang, "Size dependence of III-nitride microdisk light-emitting diode characteristics," *Applied Physics Letters*, vol. 78, no. 22, p. 3532, 2001.

[79] S.-B. Shin, K.-I. Iijima, J.-I. Chiba, H. Okada, S. Iwayama, and A. Wakahara, "Integration of Micro-Light-Emitting-Diode Arrays and Silicon Driver for Heterogeneous Optoelectronic Integrated Circuit Device," *Japanese Journal of Applied Physics*, vol. 50, p. 04DG12, Apr. 2011.

[80] J. J. D. McKendry, B. R. Rae, Z. Gong, K. R. Muir, B. Guilhabert, D. Massoubre, E. Gu, D. Renshaw, M. D. Dawson, and R. K. Henderson, "Individually Addressable AlInGaN Micro-LED Arrays With CMOS Control and Subnanosecond Output Pulses," *IEEE Photonics Technology Letters*, vol. 21, pp. 811–813, June 2009.

[81] K. Geib, K. Choquette, D. Serkland, A. Allerman, and T. Hargett, "Fabrication and performance of two-dimensional matrix addressable arrays of integrated vertical-cavity lasers and resonant cavity photodetectors," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 8, pp. 943–947, July 2002.

[82] H. Wang, J. Luo, K. Shenoy, Y. Royter, C. Fonstad, and D. Psaltis, "Monolithic integration of SEEDs and VLSI GaAs circuits by epitaxy on electronics," *IEEE Photonics Technology Letters*, vol. 9, pp. 607–609, May 1997.

[83] B. Rajendran, "Sequential 3D IC Fabrication Challenges and Prospects," *VLSI Multi-level Interconnect Conference*, 2006.

[84] P. Batude, M. Vinet, A. Pouydebasque, C. Le Royer, B. Previtali, C. Tabone, J. Hartmann, L. Sanchez, L. Baud, V. Carron, and Others, "Advances in 3D CMOS sequential integration," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, no. 110, pp. 1–4, IEEE, 2009.

[85] J. Lin, W. Chiou, K. Yang, H. Chang, Y. Lin, E. Liao, J. Hung, Y. Lin, P. Tsai, Y. Shih, T. Wu, W. Wu, F. Tsai, Y. Huang, T. Wang, C. Yu, C. Chang, M. Chen, S. Hou, C. H. Tung, S. Jeng, and D. C. Yu, "High density 3D integration using CMOS foundry technologies for 28 nm node and beyond," in *2010 International Electron Devices Meeting*, pp. 2.1.1–2.1.4, IEEE, Dec. 2010.

[86] a. Mercha, G. Van der Plas, V. Moroz, I. De Wolf, P. Asimakopoulos, N. Minas, S. Domae, D. Perry, M. Choi, a. Redolfi, C. Okoro, Y. Yang, J. Van Olmen, S. Thangaraju, D. S. Tezcan, P. Soussan, J. Cho, a. Yakovlev, P. Marchal, Y. Travaly, E. Beyne, S. Biesemans, and B. Swinnen, "Comprehensive analysis of the impact of single and arrays of through silicon vias induced stress on high-k / metal gate CMOS performance," *2010 International Electron Devices Meeting*, pp. 2.2.1–2.2.4, Dec. 2010.

[87] Y. S. Kim, A. Tsukune, N. Maeda, H. Kitada, A. Kawai, K. Arai, K. Fujimoto, K. Suzuki, Y. Mizushima, T. Nakamura, T. Ohba, T. Futatsugi, and M. Miyajima, "Ultra thinning 300-mm wafer down to 7-m for 3D wafer Integration on 45-nm node CMOS using strained silicon and Cu/Low-k interconnects," in *2009 IEEE International Electron Devices Meeting (IEDM)*, pp. 1–4, IEEE, Dec. 2009.

[88] P. Benkart, a. Kaiser, a. Munding, M. Bschorr, H.-J. Pfleiderer, E. Kohn, a. Heittmann, H. Huebner, and U. Ramacher, "3D Chip Stack Technology Using Through-Chip Interconnects," *IEEE Design and Test of Computers*, vol. 22, pp. 512–518, June 2005.

[89] R. Ishihara and N. Golshani, "Monolithic 3D-ICs with single grain Si thin film transistors," *on Silicon (ULIS),*, 2011.

[90] N. Patil, A. Lin, H.-S. P. Wong, and S. Mitra, "Monolithic three-dimensional integrated circuits using carbon nanotube FETs and interconnects," in *2009 IEEE International Electron Devices Meeting (IEDM)*, pp. 1–4, IEEE, Dec. 2009.

[91] M.-J. Lee, C. B. Lee, S. Kim, H. Yin, J. Park, S. E. Ahn, B. S. Kang, K. H. Kim, G. Stefanovich, I. Song, S. Kim, J. H. Lee, S. J. Chung, Y. H. Kim, C. S. Lee, J. B. Park, I. G. Baek, C. J. Kim, and Y. Park, "Stack friendly all-oxide 3D RRAM using GaInZnO peripheral TFT realized over glass substrates," *2008 IEEE International Electron Devices Meeting*, pp. 1–4, Dec. 2008.

[92] Y.-h. Son, S. J. Baik, S. Jeon, J.-w. Lee, G. Hwang, Y. G. Shin, and E. Yoon, "Highly Manufacturable Device Isolation Technology Using Laser-Induced Epitaxial Growth for Monolithic Stack Devices," *IEEE Transactions on Electron Devices*, vol. 58, pp. 3863–3868, Nov. 2011.

[93] Y. Son, J. Lee, P. Kang, M. Kang, J. Kim, S. Lee, Y. Kim, I. Jung, B. Lee, S. Choi, and Others, "Laser-induced Epitaxial Growth (LEG) Technology for High Density 3-D Stacked Memory with High Productivity," in *VLSI Technology, 2007 IEEE Symposium on*, pp. 80–81, IEEE, 2007.

[94] M. Kane, L. Goodman, A. Firester, P. van der Wilt, A. Limanov, and J. Im, "CMOS-on-Plastic Technology using Sequential Laterally Solidified Silicon Thin-Film Transistors," in *2006 IEEE International Solid State Circuits Conference - Digest of Technical Papers*, vol. 93, pp. 1092–1098, IEEE, 2006.

[95] Y.-H. Kim, J. Moon, C.-H. Chung, S. Yun, D.-J. Park, J. Lim, Y.-H. Song, and J. Lee, "Performance Improvement of Ultralow Temperature Polycrystalline

Silicon TFT on Plastic Substrate by Plasma Oxidation of Polycrystalline Si Surface," *IEEE Electron Device Letters*, vol. 27, pp. 896–898, Nov. 2006.

[96] D. P. Gosain, "Excimer laser crystallized poly-Si TFTs on plastic substrates," *Proceedings of SPIE*, vol. 4426, no. May 2010, pp. 394–400, 2002.

[97] T. Schiml, S. Biesemans, G. Brase, L. Burrell, A. Cowley, K. Chen, A. Von Ehrenwall, B. Von Ehrenwall, P. Felsner, J. Gill, F. Grellner, F. Guarin, L. Han, M. Hoinkis, E. Hsiung, E. Kaltalioglu, P. Kim, G. Knoblinger, S. Kulkarni, A. Leslie, T. Mono, T. Schafbauer, U. Schroeder, K. Schruefer, T. Spooner, D. Warner, C. Wang, R. Wong, E. Demm, and P. Leung, "A 0.13 μm CMOS platform with Cu/low-k interconnects for system on chip applications," in *2001 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No.01 CH37184)*, vol. 12, pp. 101–102, Japan Soc. Appl. Phys, 2001.

[98] K. Banerjee, a. Amerasekera, and G. Dixit, "The effect of interconnect scaling and low-k dielectric on the thermal characteristics of the IC metal," *International Electron Devices Meeting. Technical Digest*, no. 2, pp. 65–68, 1996.

[99] V. W. Lee, G. S. Ganot, A. B. Limanov, J. S. Im, and I. Kymissis, "T5.20: Sequential Lateral Solidification of Silicon on Low-K Dielectrics for 3D Integrated Circuits," in *Materials Research Society Fall Meeting*, 2011.

[100] A. Pratt, "Overview of the Use of Copper Interconnects in the Semiconductor Industry," *Advanced Energy*, 2004.

[101] P. C. Andricacos, "Copper On-Chip Interconnections," *The Electrochemical Society Interface*, vol. 8, no. 1, p. 6, 1999.

[102] A. Loke, T. Nogami, V. Dubin, R. Kavari, G. Ray, and S. Wong, "Microstructure and reliability of copper interconnects," *IEEE Transactions on Electron Devices*, vol. 46, pp. 1113–1120, June 1999.

[103] J. VanOlmen, S. List, Z. Tokei, L. Carbonell, S. H. Brongersma, H. Volders, E. Kunnen, N. Heylen, I. Ciofi, A. Khandelwal, J. Gelatos, T. Mandrekar, and P. Boelen, "Cu Resistivity Scaling Limits for 20nm Copper Damascene Lines," in *2007 IEEE International Interconnect Technology Conferencee*, pp. 49–51, IEEE, 2007.

[104] W. Steinhogl, G. Schindler, G. Steinlesberger, M. Traving, and M. Engelhardt, "Comprehensive study of the resistivity of copper wires with lateral dimensions of 100 nm and smaller," *Journal of Applied Physics*, vol. 97, no. 2, p. 023706, 2005.

[105] W. Steinhögl, G. Schindler, G. Steinlesberger, and M. Engelhardt, "Size-dependent resistivity of metallic wires in the mesoscopic range," *Physical Review B*, vol. 66, pp. 1–4, Aug. 2002.

[106] R. Havemann, "Line width dependence of copper resistivity," in *Proceedings of the IEEE 2001 International Interconnect Technology Conference (Cat. No.01EX461)*, no. c, pp. 227–229, IEEE, 2001.

[107] K. J. Ganesh, a. D. Darbal, S. Rajasekhara, G. S. Rohrer, K. Barmak, and P. J. Ferreira, "Effect of downscaling nano-copper interconnects on the microstructure revealed by high resolution TEM-orientation-mapping.," *Nanotechnology*, vol. 23, p. 135702, Apr. 2012.

[108] P. B. Johnson and R. W. Christy, "Optical Constants of the Noble Metals," *Physical Review B*, vol. 6, pp. 4370–4379, Dec. 1972.

[109] G. P. Pells and M. Shiga, "The optical properties of copper and gold as a function of temperature," *Journal of Physics C: Solid State Physics*, vol. 2, pp. 1835–1846, Oct. 1969.

[110] S. Roberts, "Optical Properties of Copper," *Physical Review*, vol. 118, pp. 1509–1518, June 1960.

[111] L. G. SCHULZ, "The Optical Constants of Silver, Gold, Copper, and Aluminum I The Absorption Coefficient k," *Journal of the Optical Society of America*, vol. 44, p. 357, May 1954.

[112] H. Hong, C. Chao, J. Chyi, and Y. Tzeng, "Reactive ion etching of GaN/InGaN using BCl3 plasma," *Materials Chemistry and Physics*, vol. 77, pp. 411–415, Jan. 2003.

[113] J.-M. Lee, S.-W. Kim, and S.-J. Park, "Dry Etching of GaN/InGaN Multiquantum Wells Using Inductively Coupled Cl[sub 2]/CH[sub 4]/H[sub 2]/Ar Plasma," *Journal of The Electrochemical Society*, vol. 148, no. 5, p. G254, 2001.

[114] T. Maeda, J. Lee, R. Shul, J. Han, J. Hong, E. Lambers, S. Pearton, C. Abernathy, and W. Hobson, "Inductively coupled plasma etching of IIIV semiconductors in BCl3-based chemistries," *Applied Surface Science*, vol. 143, pp. 174–182, Apr. 1999.

[115] R. Low, "Microprocessor Trends: Multicore, Memory and Power Developments," *Embedded Computing*, no. September, 2005.

[116] N. H. E. Weste and D. Harris, *CMOS VLSI Design: A Circuits and System Perspective*. Pearson Eduation, Inc., 2005.