EVOLUTION OF THE NON-VON SUPERCOMPUTER

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ABSTRACT

NON-VON is a very high performance experimental supercomputer, portions of which are now being implemented at Columbia University. If our efforts are successful, it should be possible to construct NON-VON machines of various sizes that could ultimately support the extremely rapid execution of a wide range of information processing tasks relevant to the defense community in a highly cost-effective manner. This paper briefly sketches the most important aspects of the NON-VON architecture, identifies a few of our current architectural objectives, and describes the phased hardware implementation plan we have adopted for the next three years.

INTRODUCTION

NON-VON [Shaw, 1980; Shaw, 1982] is a massively parallel non-von Neumann supercomputer architecture that has been under investigation at Columbia since 1980. The machine was originally designed to provide highly efficient support for the kinds of symbolic information processing tasks that seem to arise frequently in the context of large-scale artificial intelligence and database management applications. While such tasks remain our primary focus, we have since come to suspect that the NON-VON architecture may prove applicable to such diverse application areas as signal processing, physical simulation, and low-level computer vision as well. The architecture should provide a common basis for the construction of very high performance machines having a wide range of physical sizes, extending from compact embedded systems to centralized large scale supercomputers.

This paper identifies a few of our current architectural objectives, and describes the phased hardware implementation plan we have adopted for the next three years. Due to space limitations, software considerations will not be discussed in this paper, despite the fact that they have occupied a large fraction of our time.

PROJECT GOALS

The following goals are central to the NON-VON Project:

1. The experimental construction of working prototypes of the NON-VON family of machines, in an attempt to validate certain innovative architectural principles that could have important practical implications.
2. The development of languages, translators, and operating systems capable of effectively exploiting the potential parallelism of such machines without the introduction of prohibitive software complexity.
3. The implementation of a modest corpus of working applications software that demonstrates NON-VON's potential advantages in the context of different kinds of computational tasks.

Our approach to the solution of the hardware-related aspects of these goals involves:

1. The extensive intermingling of processing and memory resources, supporting massive "fine granularity" parallelism.

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2. The construction of machines based on heterogeneous interconnection topologies, and incorporating both "large" and "small" processing elements.

3. The provision of hardware support for both SIMD and MIMD control regimes, to support a wide range of parallel algorithms involving different modes of inter-processor communication.

STAGED DEVELOPMENT OF THE NON-VON MACHINE

During the coming three-year period, we plan to proceed in several stages toward the satisfaction of our long-range goals. Our (partially overlapped) three-stage development strategy is designed to minimize the risk involved in developing a highly unconventional supercomputer. We plan to begin by implementing and testing a relatively simple machine which nonetheless incorporates what we regard as the most essential elements of a full-scale NON-VON supercomputer. Architectural enhancements are to be added in stages, yielding incremental increases in power and generality without the introduction of an unmanageable increase in conceptual or engineering complexity at any single stage.

NON-VON 1

The first version we intend to implement, which we call NON-VON 1, comprises three subsystems: the Primary Processing Subsystem (PPS), the Secondary Processing Subsystem (SPS) and the Control Processor (CP). Briefly, the PPS incorporates a large number of simple, highly area-efficient Small Processing Elements (SPE's), configured as a binary tree. Each SPE is much smaller than a conventional microprocessor, allowing between 8 and 16 SPE's to be embedded within a single custom nMOS integrated circuit chip. We have recently completed and are now in the process of testing and debugging, a circuit containing just one SPE, from which we hope to gain valuable information at the functional and electrical levels. Each SPE contains an eight-bit comparator unit, a one-bit ALU, a 64-byte local random access memory, and a small amount of logic for enabling and disabling the SPE and for communicating with other SPE's in the PPS.

The CP is a conventional general purpose computer that broadcasts instructions to be executed simultaneously by all PE's in the PPS. Because only a single CP will be incorporated in the NON-VON 1 prototype, the machine will be limited to single instruction stream, multiple data stream (SIMD) applications, in which a the CP sends instructions to be executed in "lock step" by all processing elements. (As we shall see, this restriction is to be relaxed in later versions of the machine.)

The SPS is based on a number of "intelligent disks" whose individual disk heads are each associated with a small amount of hardware capable of dynamically examining the data that pass underneath them, and passing selected records along to the PPS in a highly parallel fashion. Although the SPS is a key part of the NON-VON architecture, we have not yet begun to implement this subsystem. For this reason, our NON-VON 1 prototype will be limited to the execution of SIMD algorithms in which the argument and result do not exceed the capacity of the PPS.

Unlike more recent versions of the architecture, NON-VON 1 performs all arithmetic and logical operations except for comparison (which has special importance in most NON-VON algorithms) in a bit-serial fashion, and is rather limited its choice of operands for most instructions. Because only one SPE is embedded on our initial prototype NON-VON 1 chip, a relatively low priority was placed on the minimization of silicon area; detailed measurements of the NON-VON 1 layout have, however, formed the basis for the highly efficient floor plans now under development for use in later versions.

For the sake of completeness, it is probably worth mentioning at this point that the name NON-VON 2 was assigned to an interesting architectural exercise that we do not currently plan to carry beyond the "paper-and-pencil" stage, although its

essential ideas may well influence future NON-VON designs.

NON-VON 3

The machine we now call NON-VON 3 forms the basis for much of the work we plan to do during the next three years. Like NON-VON 1, our NON-VON 3 prototype will include no disk drives and only a single control processor, and will thus capable of executing only SIMD algorithms in which the data does not exceed the capacity of the PPS. The machine will be similar in most respects to the original NON-VON 1 design, but will incorporate a number of improvements suggested by the results of our initial experiments in chip design and software development. In particular, the NON-VON 3 SPE will feature:

1. An area-efficient eight-bit ALU to replace the one-bit ALU incorporated in the prototype NON-VON 1 SPE chip.
2. Fewer local registers, based on NON-VON 1 area measurements and software simulation results.
3. A far better floor plan, formulated using precise measurements taken from the prototype chip.
4. A generalization of certain NON-VON 1 instructions to support the more efficient execution of many common instruction sequences.

The NON-VON 3 instruction set is nearly identical to, and with few exceptions, more general than the one employed in NON-VON 1. Some of the additions in fact correspond to commonly used macros in our existing NON-VON 1 software. Before adopting this instruction set, however, we were careful to insure that all existing NON-VON 1 software could be simply and mechanically translated into NON-VON 3 instructions, so that none of our work to date would be lost. Such a translator should be completed shortly. Translated programs will take advantage of some, but not all of NON-VON 3's enhancements. In the future, of course, NON-VON 3 software will be written using NON-VON 3 instructions, allowing the exploitation of all of these features.

NON-VON 4

The NON-VON 1 and 3 machines should serve to validate many of our most important architectural ideas, yielding major performance improvements on a number of problems amenable to SIMD execution. The more sophisticated NON-VON 4 architecture, though, is intended to provide for the highly efficient execution of a much wider range of computational tasks than NON-VON 1 and 3. The most significant enhancements we expect to incorporate in NON-VON 4 involve the addition of a few thousand large processing elements (LPE's) within the top portion of the PPS tree, all interconnected in a high-bandwidth interconnection network, and each capable of serving as a control processor for an independent PPS subtree. This should give NON-VON 4 the capacity for multiple instruction stream, multiple data stream (MIMD) and multiple SIMD (MSIMD) operations, multi-tasking and multi-user applications, and such problems as physical simulation for which the top of the NON-VON 3 tree would otherwise represent a significant communication bottleneck.

We hope to realize an additional multiplicative factor in total throughput by reducing the effective instruction cycle time (which is equal to the time required for parallel inter-SPE communication) far below the estimated two microseconds projected for NON-VON 1 and 3. Among the techniques we plan to employ to achieve such an improvement are a separation of instruction broadcast and inter-SPE data communication functions, the provision of a wider instruction broadcast data path, local caching of instructions, and tree pipelining of blocks of instructions during transfer to the local caches. Rough initial estimates suggest that these techniques might reduce average instruction cycle time by as much as a factor of four or five.

Another important feature of the NON-VON 4 design is the incorporation of a large number of standard, commercially available dynamic RAM chips, which we expect to couple tightly to the

individual PPS chips. While we expect this RAM to be used in several different ways within the NON-VON 4 machine, one of its most important functions would be as a high bandwidth "swapping memory", allowing data to be very rapidly transferred to and from the many local RAM's embedded within the PPS.

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