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Image Lag Optimisation in a 4T CMOS sensor for the JANUS camera on ESA's JUICE mission to Jupiter

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ABSTRACT

The CIS115, the imager selected for the JANUS camera on ESA's JUICE mission to Jupiter, is a Four Transistor CMOS Image Sensor (CIS) fabricated in a 0.18 μm process. 4T CIS (like the CIS115) transfer photo generated charge collected in the pinned photodiode to the sense node through the Transfer Gate. These regions are held at different potentials and charge is transferred from the potential well under the pinned photodiode to the potential well under the sense node through a voltage pulse applied to the transfer gate. Incomplete transfer of this charge can result in image lag, where signal in previous frames can manifest itself in subsequent frames, often appearing as ghosted images in successive readouts, seriously affecting image quality in scientific instruments, which must be minimised. This is important in the JANUS camera, where image quality is essential to help JUICE meet its scientific objectives.

Image lag investigation in this paper compare results pre and post Total Ionizing Dose and documents a decrease in image lag following Total Ionizing dose below device full well capacity, scaled with dose. This paper also presents two techniques to minimise image lag within the CIS115. An analysis of the optimal voltage for the transfer gate voltage is detailed where optimisation of this TG "ON" voltage has shown to minimise image lag in both an engineering model, gamma and proton irradiated devices. Secondly, a new readout method of the CIS115 is described, where following standard image integration, the PPD is biased to the reset voltage level (VRESET) through the transfer gate to empty charge on the PPD and has shown to reduce image lag in the CIS115

Keywords: CMOS Sensors, Image Sensors, Image Lag

1. INTRODUCTION

The pinned photodiode (PPD) is used in 4T CMOS devices to collect photo-generated charge that is then transferred to the sense node (SN) across the transfer gate (TG) for readout. The potentials present on these elements can control the way in which charge is transferred out of the device for readout. Incomplete transfer of this charge can result in image lag. This image lag can present itself in the form of charging lag or discharging lag [1]. Discharging lag is the most common lag phenomena observed, presented as ghosting in subsequent readout frames when illumination on the sensor is rapidly decreased from one frame to the next. Charging lag on the other hand can result in low illumination regions of the image being lost to 'charging' of the photodiode potential well when the image sensor is held at reset for long periods of time before readout. It has been reported that sources of lag can occur from potential barrier/pockets present at the PPD TG interface, trapping of majority carriers by defects present in the PPD or under the TG, or from spill back from the SN to the PPD [2, 3].

1.1 CIS115

The Teledyne e2v technologies CIS115 is the sensor that will be included in the JANUS camera for ESA's JUICE mission to Jupiter, shown in Figure 1. It is a 3 Megapixel 4-Transistor Complementary Metal Oxide Semiconductor (CMOS) device fabricated in TowerJazz Semiconductor's 0.18 μm process with a 2000 x 1504 pixel region divided into four areas (2000 rows by 376 columns), manufactured with back thinned epitaxial silicon with a thickness of approximately 10 μm [4]. The 4T pixel architecture utilises a pixel size of 7 μm and is capable of sampling rates up to 10 MPixel second⁻¹.

This device has been characterised in the following studies [4, 5] and in this paper, image lag is presented for the CIS115, pre and post TID for four devices. In addition to this, image lag is presented for a range of transfer gate 'on' voltages for

a proton and gamma irradiated device. Lastly a novel readout method for the CIS115 for image lag reduction is suggested and Charge Transfer Efficiency (CTE) presented using this readout.

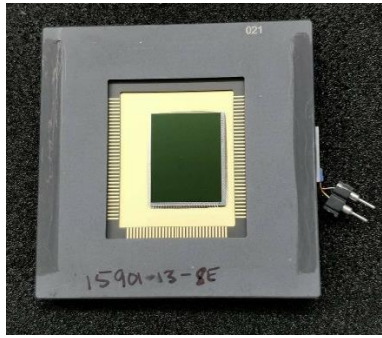


Figure 1: CIS115 Image Sensor fabricated by Teledyne e2v, the image sensor for the JANUS camera on JUICE

2. CHARGE TRANSFER IN 4T CMOS

As mentioned in Section 1, photo-generated charge collected on the PPD is transferred across the TG to the SN for readout. The baseline readout sequence for the CIS115 is shown in **Figure 3**, with the baseline times in **Table 1**. The CIS115 employs a typical readout pattern like most 4T CMOS devices where during an integration time; charge is collected on the device. A row is selected on the device for readout through the row address (R_ADDR) and by pulsing the transfer gate (t_{TRA}); signal is transferred from the PPD on the pixel to the FD ready to be read out. These pixels are then read out during t_{READ} by cycling through the column addresses (C_ADDR) required and digitising the analogue outputs of the detector (t_{DATA} times in t_{READ} , the readout time). A more detailed analysis on device readout can be found in [4].

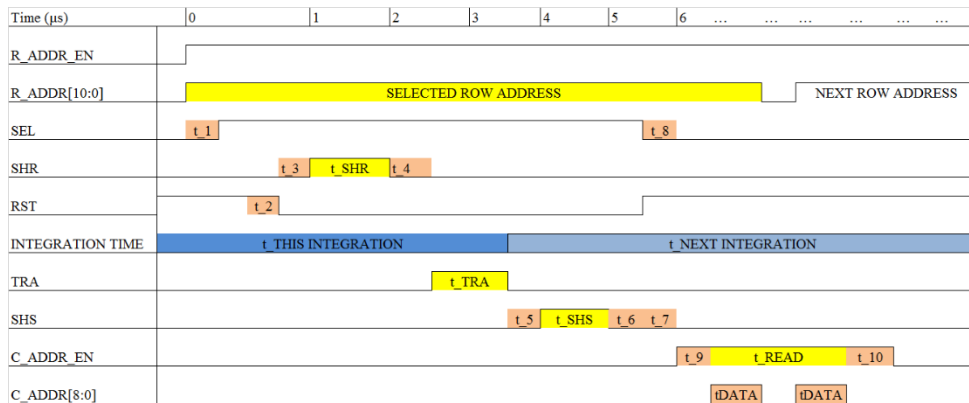


Figure 2: The baseline row read timing diagram for the CIS115 adapted from [6], timing explanation shown in Table 1

| Timing | Definition | Typical Value | Unit |
|--------|---|---------------|------|
| t_1 | Minimum setup time from stable row address to the select (SEL) rising edge. Reset (RST) must be high during this time and for the following t_2 | 0.5 | μs |
| t_2 | Hold time on RST to avoid a soft reset from SEL feed through | 100 | ns |
| t_3 | Suggested time between RST falling edge and t_SHR | 0.4 | μs |
| t_4 | Suggested time between t_SHR and t_TRA | 0.5 | μs |
| t_5 | Suggested time between t_TRA and t_SHS | 0.5 | μs |
| t_6 | Suggested time between t_SHS and SEL falling edge | 0.5 | μs |
| t_7 | Suggested time between SEL falling and column address (C_ADDR_EN) rising edges | 0.5 | μs |

| | | | |
|--|--|-------|----|
| t_8 | Minimum setup time between SEL falling edge and row address change | 0.5 | μs |
| t_9 | Setup time of C_ADDR_EN to new column address input | ~100 | ns |
| t_10 | Hold time from last column address to C_ADDR_EN falling edge | ~100 | ns |
| t_SHR | Pulse width to sample the reset level | 1.0 | μs |
| t_TRA | Photodiode to sense node transfer pulse width | 1.0 | μs |
| t_SHS | Pulse width to sample the signal after integration | 1.0 | μs |
| t_READ | Time to read out 376 columns | 66.25 | μs |
| t_DATA | Data time per pixel | 161 | μs |
| t_THIS INTEGRATION / t_NEXT INTEGRATION | Effective integration time | ~132 | μs |

Table 1: Typical timing values for the CIS115 timing diagram

2.1 Potential Profile of the CIS115

In order for charge to be transferred in pixel from the PPD to the FD in any 4T CMOS image sensor, they must be held at varying potentials. In a perfect device, electrons can be completely transferred if the PPD potential well is sufficiently lower than the transfer gate transistor and FD and/or with an infinite t_{TRA} transfer time [7]. However, in real devices this is not possible due to the lower voltages employed in CIS devices and due to the time constraints on image readout. The CIS115 therefore is operated at voltages that have been determined by Teledyne e2v as ‘optimal’ for device operation, presented alongside the recommended timings for the device in [6].

Figure 3 shows the potential diagram of the PPD, TG and FD in two device operational states. In the first instance (a), the TG is off, being held at 0 V. In the second instance (b), the TG is ‘on’ (and held in this state for time: t_{TRA}) and is pulsed at ‘VTRA high’ voltage (suggested to be 3.15 V to 3.45 V, with typical value being 3.3 V). In both instances, the FD is held at a reference voltage (VREFR), which is recommended by Teledyne e2v to be between 2.8 V and 3.0 V. The pinning voltage of the device characterises the PPD potential and can typically be estimated using the method shown in [8]. These tests are typically carried out for characterisation of every device at the Open University.

Primary characterisation of all CIS115 devices carried out at the Open University sets the ‘VTRA high’ voltage (VTRA) to be 3.3 V and the sense node reference voltage (VREFR) to be 2.9 V. These are included in **Figure 3**, and is used in most of testing.

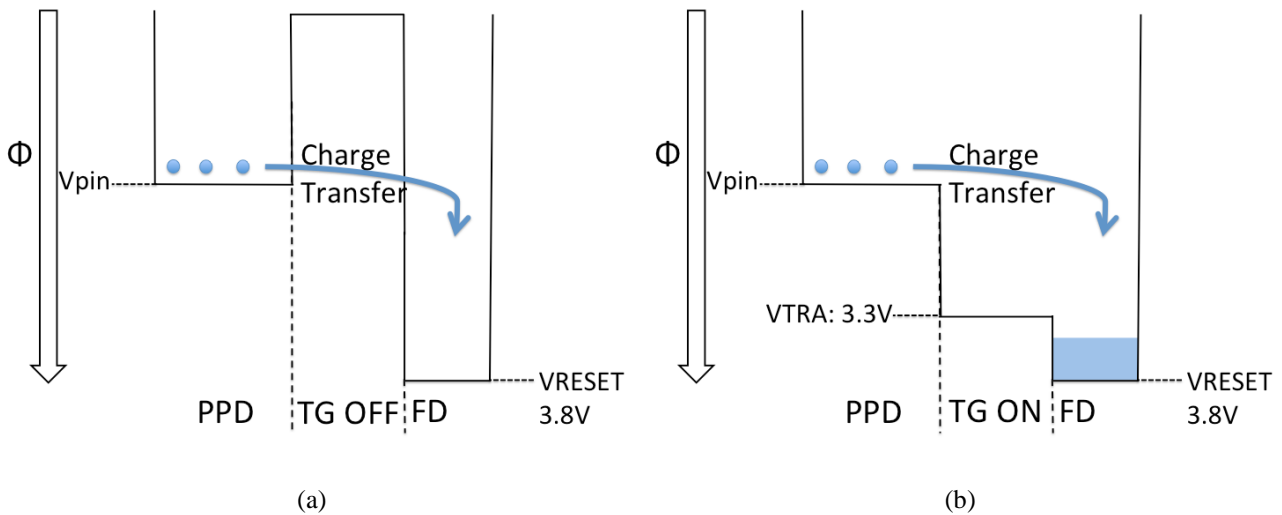


Figure 3: Potential Diagram for CIS115

2.2 Charge Transfer Inefficiency

Charge Transfer Inefficiency in an image sensor pixel is referred to as the ratio of signal lost during transfer to the initial signal charge [9]. There are many sources of image lag in a CMOS imager and as mentioned in Section 1 some major sources of image lag in 4T CMOS devices arise from

- Potential barriers or pockets present at the PPD/TG interface
- Trapping of majority carriers by defects present in the PPD or under the TG
- Spill back from the SN to the PPD

In the transfer of the electrons from the PPD to the FD, electrons that do not possess the necessary energy/speed to pass through the transfer gate [10] or become trapped in these regions will fail to be transferred to the FD in the t_{TRA} and will not be read out.

Charge transfer of these electrons can be improved via technology optimisation, pixel operation optimisation and pixel design optimisation [10]. Since we cannot change the technology contained in the device or the pixel design of the device, image lag improvements can occur through pixel operation optimisation. Changes in the TG ‘on’ time (t_{TRA}), transfer gate voltage setting (V_{TRA}) or alterations in the readout method will alter the image lag performance of the CIS115 and is discussed in the upcoming sections.

3. IMAGE LAG TESTING

Image lag testing is carried out at the Open University and identical methods are used for standard image lag testing of all devices used for this study. All image lag tests were carried out with the bias voltages shown in **Table 2** and at a temperature of -50 °C.

| Bias or clock name | Nominal Level | Description |
|--------------------|---------------|--|
| VREFR | 2.9 V | Reset level power supply for pixels |
| VTRA | 3.3 V | Supply used to drive the TG control gate |
| VANA | 3.6 V | Analogue power supply to read circuits/ output buffers |
| VRESET | 3.8 V | Select and reset driver supply to row drivers |
| VPIX | 3.3 V | Source follower power supply for pixels |

Table 2: Bias Voltages for CIS115

3.1 Test Method

Preliminary image lag testing for the CIS115 employed a specific readout method to collect image lag data. In order to reduce the computational expense in analysis, the CIS115 is read out in a 2000 by 1504 windowed mode. In this windowed mode, the device is readout occurs for ten different captures. Each of the ten individual readouts is repeated 50 times, averaged to minimise readout noise. The first five of these captures occurs with a pulsed LED illumination and the final five occur with no direct illumination incident on the sensor. This will permit the discharging lag performance of the device to be investigated through comparison of the signal level of the frames of illumination and the subsequent non-illuminated frames on the sensor. This differs from an investigation into charging that, that would investigate signal in the first illuminated frame.

The Devices Under Test (DUTs) shown in **Table 3** involved all devices being characterised before and after their respective irradiative source.

| CIS115 Device | Environment | Testing |
|---------------|--|---|
| 15901-10-13 | EOL Protons: $1 \times 10^{10} \text{ p cm}^{-2}$ (10 MeV equivalent). | Image Lag characterisation pre and post radiation, varied transfer gate voltage (VTRA) lag characterisation |
| 15901-10-03 | Twice EOL gamma (200 krad) | Image Lag characterisation pre and post radiation, varied VTRA lag characterisation |
| 15901-17-02 | Half EOL gamma (50 krad) | Image Lag characterisation pre and post radiation |
| 15901-10-11 | Half EOL gamma (50 krad) | Image Lag characterisation pre and post radiation |
| 15901-17-13 | EOL gamma (100 krad) | Image Lag characterisation pre and post radiation |
| 15901-17-19 | EOL gamma (100 krad) | Image Lag characterisation pre and post radiation |
| 15901-13-08 | - | PPD reset Image Lag characterisation (see 3.2) |

Table 3: Devices used for Image Lag analysis testing

Testing on the proton End Of Life (EOL) device and the twice EOL gamma also involve repeating standard image lag characterisation varying the transfer gate voltage. 15901-10-13 employs VTRA settings from 2.02 V to 3.5 V in approximately 0.05 V increments, whilst 15901-10-03 employs VTRA settings from 2.02 V to 2.7 V.

3.2 Photodiode Reset

During the readout method of the CIS115 as shown in **Figure 2**, an additional step in readout can be included to minimise lag on the device. This method involves resetting the photodiode following a normal readout of the device. The alteration of the CIS115 readout sequence is shown in **Figure 4** and is used on a non-irradiated device 15901-13-08 as shown in Table 1. The PPD is reset through pulsing the transfer gate ‘on’ whilst the reset gate is held high. This empties the leftover charge present on the PPD following integration following integration and readout. This reset does not improve the signal transferred during readout, and only empties the charge present on the PPD following illumination and readout; therefore, it will be required to be used in parallel with other image lag improvement techniques.

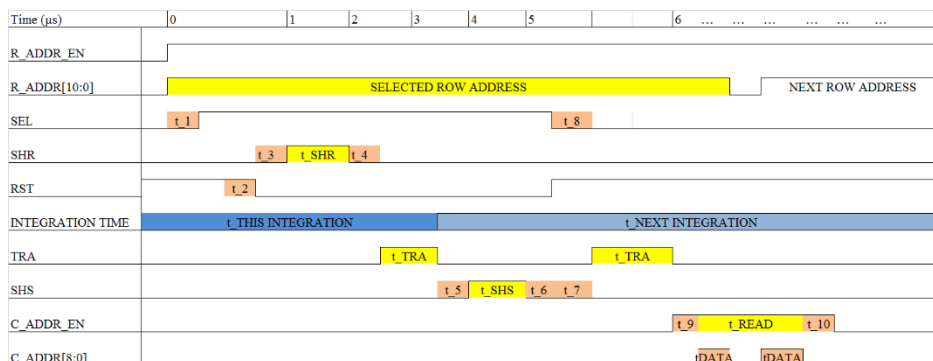


Figure 4: CIS115 Altered Timing Diagram with a reset of the photodiode through the pulsing of the transfer gate after charge readout adapted from [6]

4. RESULTS AND DISCUSSION

4.1 Image Lag Characterisation

The DUTs shown in Table 3 have been characterised for image lag performance pre and post gammas as shown in Figure 8 for the lag (signal present in the first non-illuminated readout frame) against the signal level in the final frame of illumination (Frame 5). This Frame 5 illumination has been shown in units of V. Each of these devices has a specific value for conversion factor that has been calculated through a mean variance curve responsivity calibration. Further details on how this calibration is carried out can be found in [11]. **Table 4** shows the calibration for the DUTs involved in the studies.

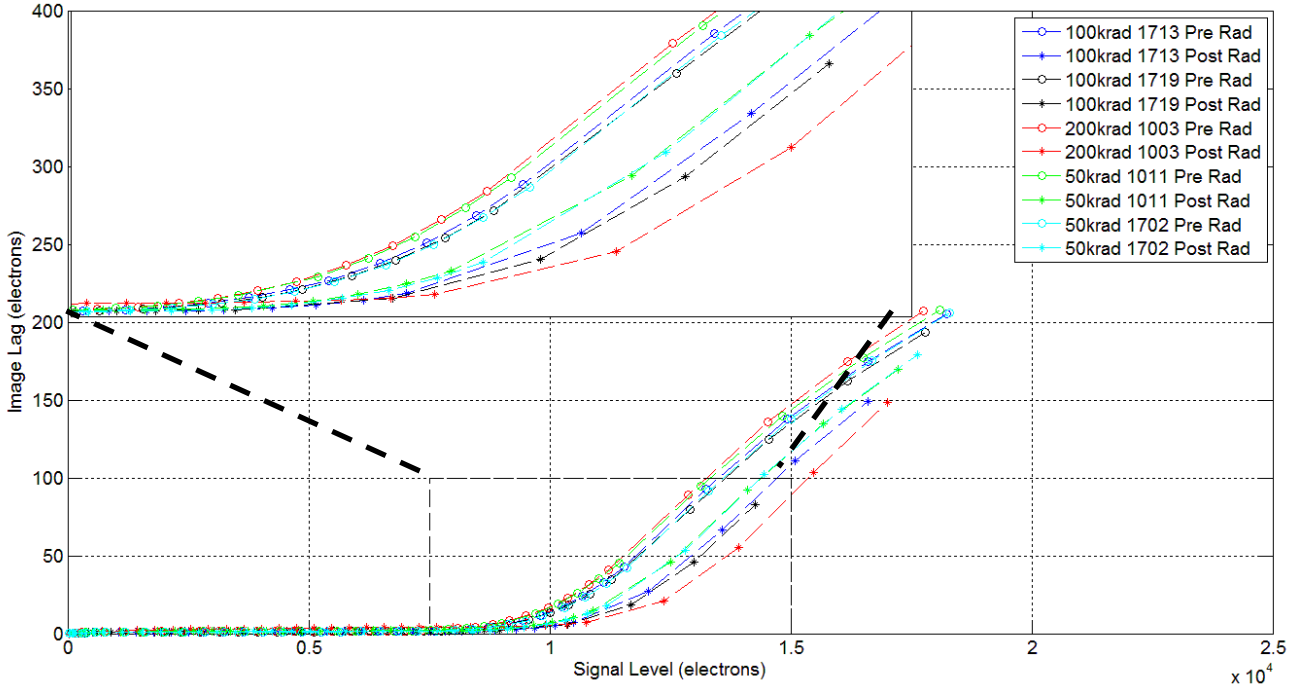


Figure 5: Image Lag in electrons vs Signal level in electrons on gamma irradiated detectors pre and post irradiation

| DUT | Mean Variance Charge to Voltage conversion Factor (CVF) ($\mu\text{V}/e^-$) | |
|-------------|---|--------------------------|
| | Beginning of Life | After Radiation Campaign |
| 15901-10-13 | 60.10 | 59.94 |
| 15901-10-03 | 59.75 | 59.03 |
| 15901-17-02 | 59.71 | 58.11 |
| 15901-10-11 | 58.67 | 57.44 |
| 15901-17-13 | 59.84 | 58.61 |
| 15901-17-19 | 58.62 | 57.26 |

Table 4: Mean Variance Charge to Voltage conversion Factor (CVF) ($\mu\text{V}/e^-$) for the DUTs

Using the results presented in **Figure 5** demonstrates there has been a shift in the knee point in the graph (the point at which the lag rapidly increases) that correlates to TID. In order to extrapolate this 'knee point' extra analysis on the data is required. By looking at the change in linearity of the device with respect to a fitted straight line (fitted to data points well below knee point) one can obtain the 'knee point' by assessing when the difference between the data and the best fit line is greater than 10% via an iterative method. From this extra analysis, the knee point of each of the DUTs from **Figure**

5 can be obtained. These are shown in **Figure 6**. It is evident that there is a correlation between the TID and the amount of shift observed in the knee point of the data. **Figure 6** documents a linear fit can be obtained from the knee points of the graph. This presents an equation that passes through the origin that can be used to map the lag performance of the device up to twice EOL gamma dose.

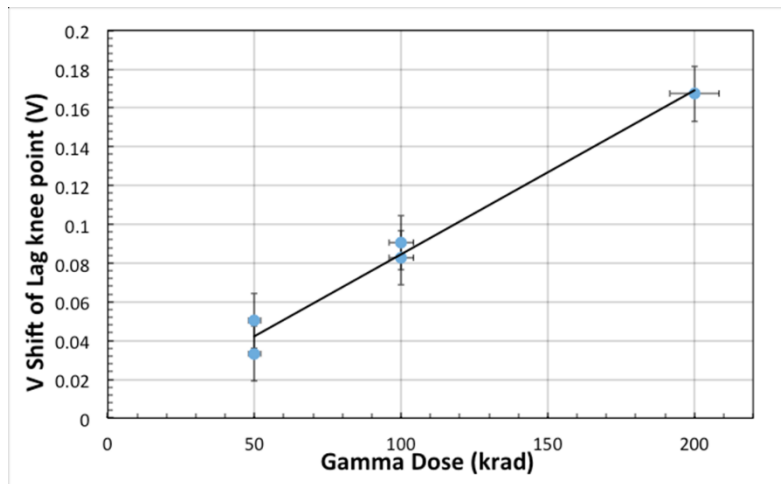


Figure 6: Voltage shift of knee point observed in the devices pre and post radiation with respect to the respective gamma dose (Si) the DUT received

At a gamma dose of zero, one can expect no change in the knee point of a plot like those shown in **Figure 5**. Therefore, plotting a trend line on **Figure 6** that goes through the origin a fit can be obtained for the change in knee point with respect to gamma, where the expected shift in the knee point of the image lag (at doses below 200 krad) at varied gamma doses can be obtained. This can be used to infer the ‘improvement’ in the image lag performance of the device following TID. This knee point shift on the transfer gate voltage can therefore be equated to $0.834 \text{ mV krad}^{-1} \pm 0.07 \text{ mV krad}^{-1}$.

4.2 Varying Transfer Gate Voltage

Using the test method that has been shown in 3.1 devices 15901-10-13 and 15901-10-03 are characterised for image lag using a range of transfer gate voltages. It is suggested that changing the transfer gate voltage will alter the position of the TG on level shown in **Figure 3** (b), with better charge transfer achievable with optimum transfer gate voltage selection. To obtain the data presented in **Figure 7**, where signal level is shown at varied ‘illumination’ levels data fitting was required. Equations were fitted to the image lag data presented at each transfer gate voltage studied to be able to obtain a value of image lag at:

- 5000 electrons
- 7500 electrons
- 10000 electrons
- 15000 electrons

For device 15901-10-13 these can be seen in Figure 7 where the lag is presented over the range of transfer gate voltages used in this study. From the figure it is evident that there is a ‘best’ region of operation of transfer gate voltage for the device, within the region of approximately 2.5 V to 2.7 V.

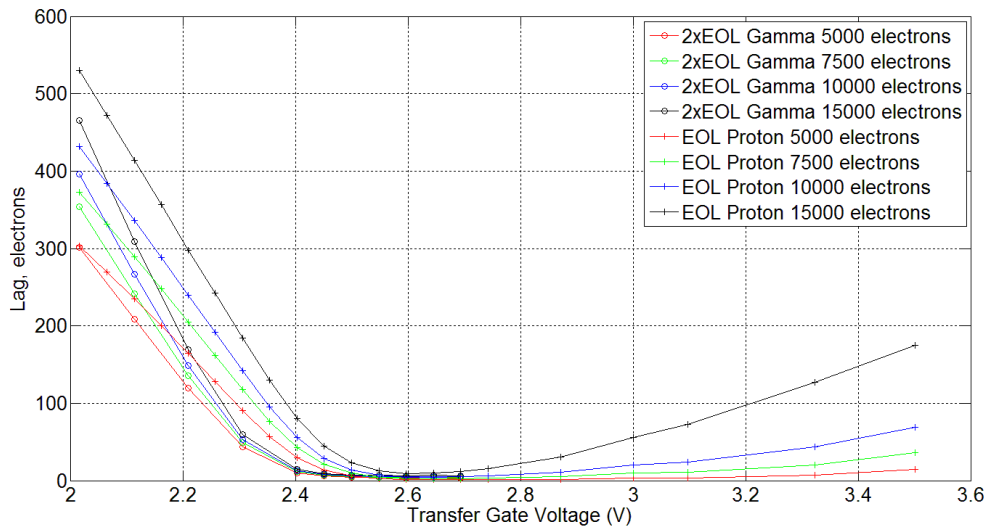


Figure 7: Image lag in electrons against the setting of the transfer gate on voltage (V) for device 15901-10-13 (proton EOL) and 15901-10-03 (gamma twice EOL)

Similarly, studying these image lag over this voltage range for the twice EOL gamma device (15901-10-03) the image lag at varied signal levels is presented alongside the proton EOL data in **Figure 7**. Similarly, to device 15901-10-13, there is an apparent region of lowest lag performance however this appears to occur over a larger voltage range of between 2.4 V and 2.7 V, which contains the ‘best region’ found for the proton EOL device.

4.3 Photodiode Reset

Figure 8 shows the image lag performance of a non-irradiated device (15901-13-08) employing the new readout method described in 3.2. Ran at a voltage of 2.69 V for a non-irradiated device, the maximum signal level in electrons reached was approximately 19,000 electrons signal. At this signal level the image lag, that is the signal present in the first readout frame of no direct illumination, was roughly six electrons.

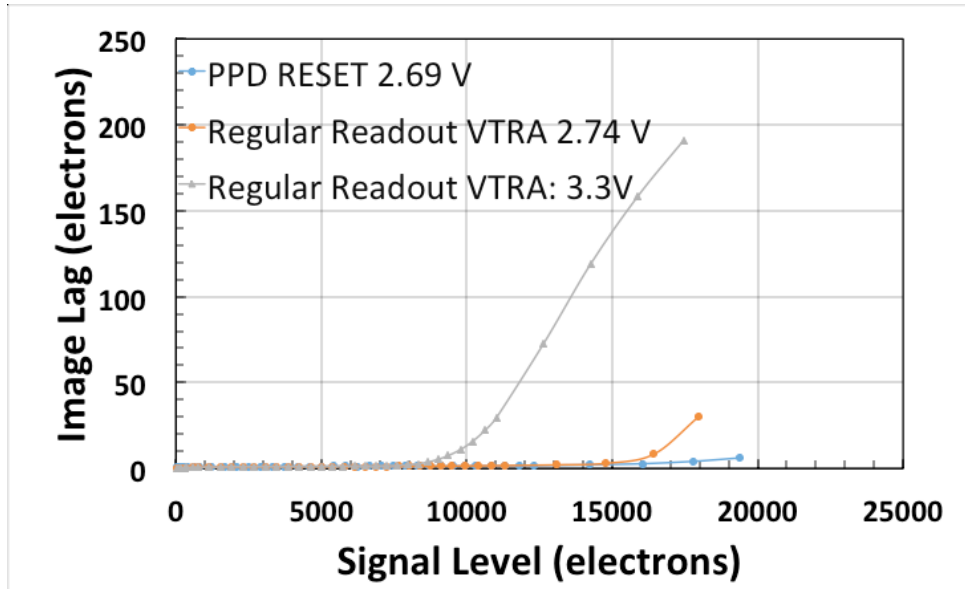


Figure 8: Signal level vs Lag in electrons for device 15901-13-08 using the photodiode-reset method

5. CONCLUSIONS

Image lag ‘knee point’ has shown to change with respect to TID in the CIS115, with the shift in the knee point shown to be $0.83598 \text{ mV krad}^{-1}$. This means that image lag is lower at a higher signal level when comparing levels before and after irradiation. Furthermore, best characteristics for device operation to minimise lag in the CIS115 is shown to be in the region of 2.5 V to 2.7 V. A selection of transfer gate voltage in this region would result in the best operational characteristics for the CIS115, even including the shift on the transfer gate voltage following TID. The novel readout method involving the reset of the PPD has shown to decrease the image lag compared to standard readout and transfer gate voltage, with 15,000 electrons signal giving on average over 100 electrons image lag compared to approximately 2 electrons with the lower VTRA and novel readout method.

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