Monolithic integration of Giant Magnetoresistance (GMR) devices onto standard processed CMOS dies

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A B S T R A C T

Giant Magnetoresistance (GMR) based technology is nowadays the preferred option for low magnetic fields sensing in disciplines such as biotechnology or microelectronics. Their compatibility with standard CMOS processes is currently investigated as a key point for the development of novel applications, requiring compact electronic readout. In this paper, such compatibility has been experimentally studied with two particular non-dedicated CMOS standards: 0.35 μm from AMS (Austria MicroSystems) and 2.5 μm from CNM (*Centre Nacional de Microelectrònica*, Barcelona) as representative examples. GMR test devices have been designed and fabricated onto processed chips from both technologies. In order to evaluate so obtained devices, an extended characterization has been carried out including DC magnetic measurements and noise analysis. Moreover, a 2D-FEM (Finite Element Method) model, including the dependence of the GMR device resistance with the magnetic field, has been also developed and simulated. Its potential use as electric current sensors at the integrated circuit level has also been demonstrated.

1. Introduction

The Giant Magnetoresistance (GMR) effect is a magnetic coupling mechanism that can be obtained in some multilayer structures. In these devices, at room temperature, the resistance of the very thin films (typically, multilayers of few nanometer thick CoFe and Cu films) is a function of the external magnetic field, at optimal levels for being used as sensors. The technological advances in GMR since 1990s were driven by the magnetic recording industry (reading heads of hard disk drives), but the spatial resolution, low field detection (down to few pT) at room temperature, and large area/scale production availability (200 mm wafers at large scale, thus low price) offered by this technology opened a wide range of new fields of application, mainly related to the measurement of small magnetic fields using miniaturized devices [1].

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Magnetoresistive structures have been continuously improved recently. Two of them turned to be particularly successful in a major range of applications: spin-valves (SV) and magnetic tunnel junctions (MTJ). An SV is a GMR structure consisting of two ferromagnetic layers (one of them with a pinned magnetic moment and the other with a free rotatable magnetic moment), separated by a nonmagnetic conductor spacer, usually Cu. A bias current is applied parallel to the layers, in a current in-plane (CIP) scheme. An MTJ also consists of two ferromagnetic layers, but separated by an oxide isolation layer. In this case, a bias current flows perpendicular to the device's plane (CPP) and crosses the isolating barrier by tunnel effect. In both cases, an external magnetic field changes the relative orientation of the magnetization vectors and, consequently, the resistance [2].

These structures are successfully deposited on different types of substrate such as silicon, glass, alumina, flexible substrates or patterned wafers. The fabrication of devices based on these structures can be achieved in a few lithographic steps, compatible with microelectronics clean room fabrication. In the case of CPP based devices, an additional step is required for dealing with the bottom electrode. We should also mention that such structures

involve materials that are not standard in typical CMOS processes (Cu, Ni, Fe, Co, Mn, etc.), what is a challenge, usually requiring additional facilities [2]. Deposition of these structures can be accomplished by ion beam deposition (IBD) or by sputtering. In any case, the substrate temperature does not exceed 120 °C. Thus, both processes can be directly masked with photoresist without damaging the substrate. In the case of MTJ, and depending on the selected isolation oxide, a final heat treatment between 200 and 300 °C for 1 h can be required to promote improved material texture and crystallization [2].

Being a key point for the development of advanced GMR based devices, few efforts have been dedicated to the investigation of the compatibility of GMR technology with semi-dedicated or non-dedicated CMOS processes. NonVolatile Electronics (NVE) was the first company in merging both technologies by using a dedicated 1.5 μm BiCMOS technology [3a]. Later, Han et al. used chips made by 0.25 μm NSC (National Semiconductor Corporation) BiCMOS technology [3b], by applying a post-process that employed reactive ion etching for via opening through the passivation, so allowing access to the buried metal layers.

Therefore, combining the design rules for CMOS chips with the techniques for GMR device microfabrication allows the full integration of these sensors, for example, in scenarios requiring non-intrusive monitoring of the electric current in integrated strips by indirect measurement of the magnetic field. Analog (hybrid technology) approaches have been successfully applied to the current measurement in industrial applications [4]. Advantages presented by GMR sensors over its competitors (mainly Hall effect and anisotropic magnetoresistance (AMR) based sensors) are their greater sensitivity, higher level of integration and the possibility of measurement of fields parallel to the surface of the integrated circuit. This is very interesting for substituting built-in current sensors (BICS) by off-line non-intrusive integrated circuits (IC) current sensors [5]. Some work has been previously reported in the literature regarding the application of GMR sensors to the electrical current measurement at IC level, starting from standard Si wafers. In this sense, we initially demonstrated the applicability of spin-valve structures to the measurement of integrated low electric currents (below 1 mA, [6]). Kim Le Phan and coworkers also developed MTJ based current sensors for IC testing applications [7].

Finally, we should mention that, in addition to microelectronics, other research fields such as biotechnology are also seeking full monolithic integration of GMR and CMOS technologies in order to initiate new qualitative steps toward the integration of electronics (e.g., bias and conditioning circuits, signal processing, memory elements, etc.) together with the sensors [8].

In this paper, the fabrication of spin valve based magnetic field sensing devices directly onto processed chips (from non-dedicated CMOS standard technologies) is described. Such structures were selected due to their higher technological maturity. In order to analyze the scope of the proposal and identify associated handicaps, two different cases were studied. In the first one, a processed chip from Austria Microsystems (AMS) 0.35 μm technology was considered. Then, a processed wafer of a 2.5 μm experimental CMOS technology from the *Centre Nacional de Microelectrònica* (IBM-CNM, CSIC, Barcelona, Spain) was also used. The obtained devices were then characterized and their performances were evaluated.

2. Design and fabrication

The consortium Europractice offers different CMOS technologies for both fundamental and applied researches. Different 0.35 μm based technologies can be found in its portfolio. Due to its popularity, Austria MicroSystems was selected.

On the other hand, CNM25 is a 2.5 μm technology developed at CNM-IMB, with 2P and 2M layers onto 100 mm wafers of (1 1 0) epi-P-silicon [9]. The main advantages in this case are as follows—first, the process, if needed, can be partially customized and, second, a whole wafer (100 mm-diameter) is dedicated. This opposes the small area chips available from AMS, since these are shared among many users for a 300 mm-diameter wafer.

2.1. AMS CMOS 0.35 μm

In this case processed unpackaged standard 0.35 μm CMOS dies were considered (2.5 mm × 1.5 mm, AMS 0.35 μm C35B3C3 3M/2P) [10]. In order to make use of the standard microelectronics fabrication facilities (photoresist spin coating, photolithography system, sputtering machines, etc.), the die was mounted on a specially arranged cavity defined by reactive ion etching (RIE) of Si on a standard wafer. For the GMR films deposition, a rectangular region was defined on a clear zone [(see Fig. 1(a)]. . The surface cleaning process involved isopropyl acetate (IPA) and deionized water only, without need of any additional etching step. Four lithographic steps were required for the microfabrication of the GMR devices. In the first one (L1SVL), the spin valve stack (Ta (20 Å)/NiFe(30 Å)/CoFe(20 Å)/Cu(22 Å)/CoFe(25 Å)/MnIr(60 Å)/Ta

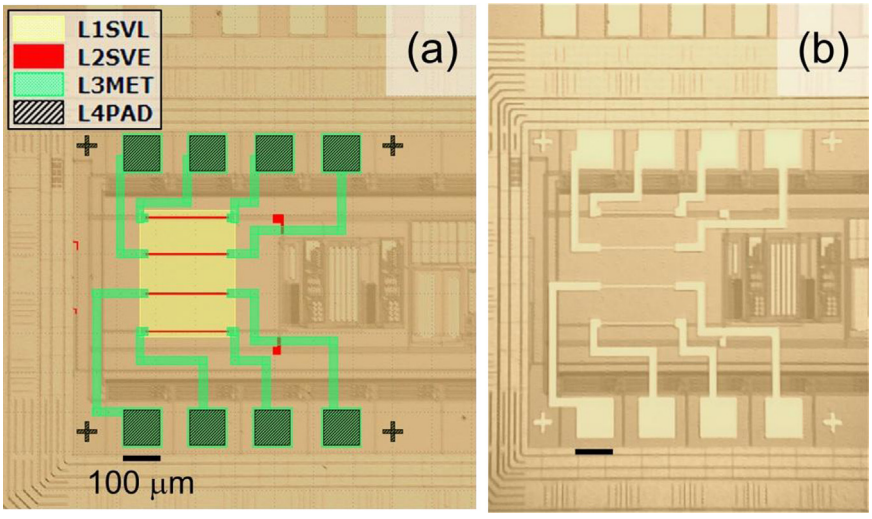

Fig. 1. Micrographs of the AMS chip with spin valves: (a) detailed masks, and (b) finalized process.

(40 Å), as described in [6]), was deposited in a wide rectangular region (defined by lithography). This rectangle covers the region where all the spin valve sensors will be defined later. It also minimizes electrical shorts along the chip topography (several micrometers in depth) by reducing metal deposition over the chip surface. This first lithographic step also was used to define alignment marks for the multilevel microfabrication. The spin valve material was then patterned (L2SVE) in 3 μm × 200 μm strips by ion milling, so defining the sensors. We used a crossed axis configuration, with the easy axis aligned with the short dimension, for improving the linearity [6]. Contacts were then defined by patterning 300 nm thick AlSiCu films (L3MET). The chip was then passivated with sputtered 400 nm-thick SiO_2, and the pads were open by lift-off (L4PAD). The final result can be observed in Fig. 1(b). The obtained chip was then wire bonded and encapsulated in a DIP-40 chip carrier, for characterization.

2.2. CNM CMOS (2.5 μm)

Considering this technology, the GMR sensors were integrated in a processed 100 mm wafer. The wafer consisted of 24 dies of 15 mm × 15 mm (their functionality is irrelevant for our purpose). Each of these dies had a rectangular region (3.5 mm × 3.2 mm) with test structures [See Fig. 2 (a)], including metal (contact layers) structures.

Four lithographic steps were also required in this case. In the first one (L1SVL), the spin valve stack [6] was deposited and patterned by lift-off in the regions of interest. In this case, we had access to the underlying mask marks, and the alignment was straightforward. The devices were then patterned (L2SVE) in 3 μm × 200 μm strips by ion milling. As observed in Fig. 2 (a), some devices were deposited onto (isolating layer between) metallic strips (upper devices) and other directly onto free (isolated) substrate (lower devices). All the devices were connected with AlSiCu strips (L3MET). The chip was then passivated with sputtered SiO_2, and the pads were open by lift-off (L4PAD), also accessing to the current strips. The final result can be observed in Fig. 2 (b) and (c). The obtained chips were then wire bonded and encapsulated in a DIP-40 chip carrier, for characterization.

3. Results and discussion

For the GMR devices characterization, a suitable workbench has been employed, consisting of a GPIB controlled setup with a personal computer, a power supply (Agilent E3600), a standard air coil magnetometer (GmW 3470), a programmable current source (Keithley 220), a data acquisition switch unit (HP 34970A) and a multimeter (Agilent 34401A).

3.1. Magnetic characterization

In order to initially check the correct device functionality, the independent resistance values were measured for each different device, as a function of the applied magnetic field, from −7 Oe to +7 Oe, where the devices behave linear [6]. The electric current generating the magnetic field at the electromagnet was driven following a hysteresis-detecting loop scheme. The considered magnetic field range falls in the linear region of the used spin valve structures and perfectly matches our applications' requirements. Results are shown in Fig. 3. By linear data fitting, we have extracted, for each case, the nominal resistance R_0 (resistance at null field) and the sensitivity magnetoresistive factor (S_B as a function of the magnetic field and S_I as a function of the driven current). So obtained results are shown in Table 1.

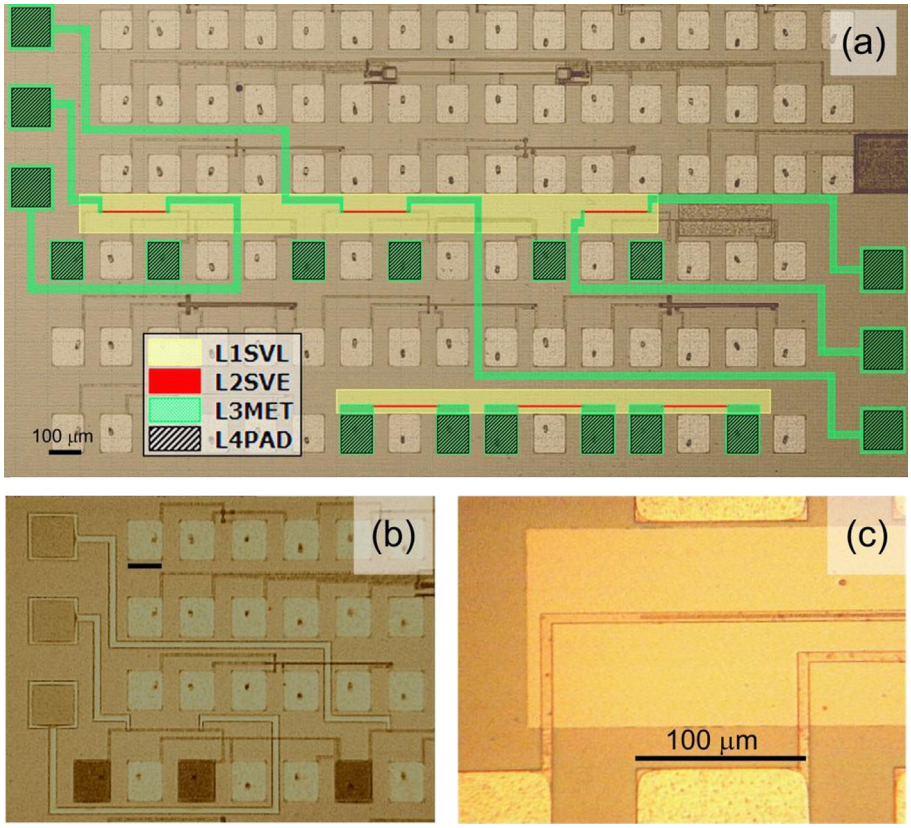

Fig. 2. Micrographs of the CNM chip with spin valves: (a) detailed masks, (b) general view of the finalized process, and (c) detail of a spin-valve onto a metallic strip.

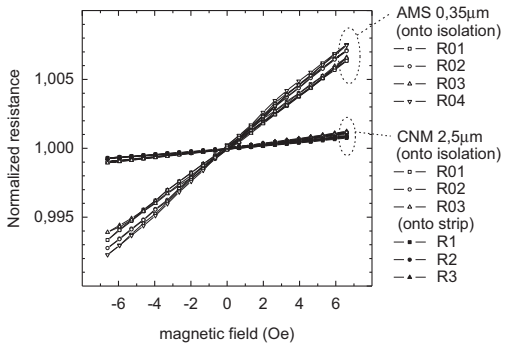

Fig. 3. Resistance of the deposited spin valve against the external magnetic field.

Table 1
Experimental parameters.

	AMSCMOS 0.35 µm	**CNM** CMOS 2.5 µm	
	onto isolation	onto isolation	onto current strip
R_0 (Ω, avgd.)	1660 ± 150	1858 ± 8	2103 ± 30
S_B (Ω/Oe)	1.76 ± 0.24	0.30 ± 0.01	0.25 ± 0.01
S_I (Ω/mA)	N.A.	N.A.	0.229 ± 0.008

As observed, tolerances are smaller for spin valves deposited onto 2.5 µm technology devices, due to the lower lithography misalignments during the deposition and patterning post-process associated to a wafer-level process. Regarding the sensitivity, it is lower for the spin valves deposited onto the 2.5 µm technology devices due to the lower quality of the surface. Spin valves deposited onto AMS chips have comparable sensitivity to analog devices deposited directly onto silicon wafers [6]. Moreover, one can observe that spin valves deposited on top of current strips have their sensitivity also reduced and the value of the nominal resistance increased.

3.2. Noise measurements

For low noise applications of GMR devices, as is the case, particular attention has to be paid to noise level in order to determine the signal-to-noise ratio (SNR) and the proper solution for the conditioning electronic circuit to be employed. As well known, GMR devices display $1/f$ noise [11]. Amplitude spectral density (ASD) level of noise of the considered devices was measured at the frequencies of interest by using a National Instruments data acquisition (DAQ) card (24 bit of resolution, 200 kHz bandwidth and noise spectral density of 8 nV/$\sqrt{\text{Hz}}$ at 1 kHz) and a low-noise amplifier (2 nV/$\sqrt{\text{Hz}}$ noise in a frequency band from 0.3 Hz to 100 kHz and voltage gain of 1000). Devices and bias batteries were shielded. A LabView program was used for controlling the system and obtaining the ASD. The results are shown in Fig. 4, for different DC bias currents. Besides the $1/f$ behavior, one can observe that devices deposited onto strips from CNM chips display lower noise level and the devices deposited onto AMS chips display higher noise level. By curve fitting, the amplitude of the noise level for a specific case (e.g.: 100 Hz, $i = 1$ mA; suitable for typical sensor applications) has been extracted. By comparing so obtained values with sensitivity parameters (from Table 1) it can be concluded that, after all, the signal-to-noise ratio is kept roughly constant for every considered device, independently from the particular technology.

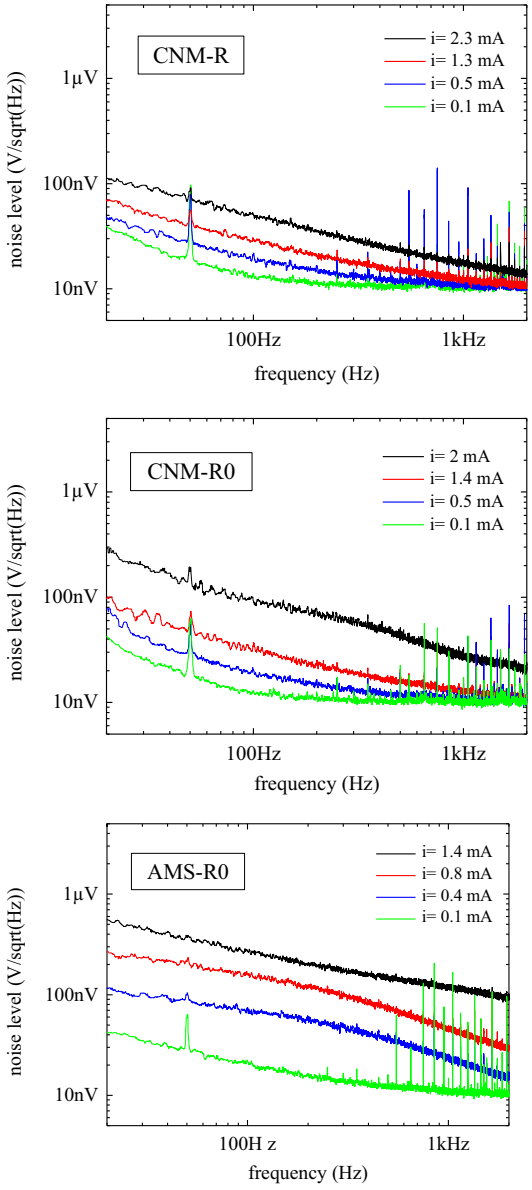

Fig. 4. Noise level (amplitude spectral density, ASD) at several bias currents for the different devices: CNM-R, spin valve onto current strip in a CNM chip; CNM-R0, spin valve onto free substrate in a CNM chip; AMS-R0, spin valve onto free substrate in an AMS chip.

3.3. Electric current measurement

The CNM 2.5 µm technology based samples included useful test structures that were used for demonstrating the potential of GMR structures for off-line measurement of the electric current in integrated circuits. In this case, these structures consisted of metallic strips of 5 µm × 330 µm, onto which the spin valves were deposited (see Fig. 2).

3.3.1. Static characterization

A current was driven through the strips by means of a current source and the resistance of the sensing elements was measured. Results are shown in Fig. 5. As explained before, from linear fits, the nominal resistance and the sensitivity magnetoresistive factor (in this case as a function of the current) were extracted. The obtained parameters are shown in Table 1.

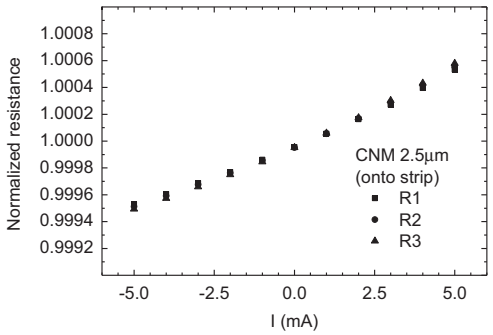

Fig. 5. Resistance of the deposited spin valve against the driven current in a CNM 2.5 µm technology chip.

As indicated before, the sensitivity of these devices is low when compared with those obtained with dedicated processes [6]. Nevertheless, the SNR is maintained, and the level of detectivity can be estimated in 50 µA, or lower if an alternate current biasing scheme is considered.

3.3.2. *FEM (finite element method) simulation*

As a supporting tool, 2D-FEM simulations were performed. In this sense, for the considered spin valve structure, and without excitation, pinned (easy axis) and free layers are arranged in a crossed axis configuration (at 90°). The response of this structure is given by [1]:

$$\Delta R = \frac{1}{2}\left(\frac{\Delta R}{R}\right) R_{sqr} \frac{iW}{h} \cos(\theta_p - \theta_f) \quad (1)$$

where $(\Delta R/R)$ is the maximum magnetoresistance level (7–9%), R_{sqr} is the sensor sheet resistance (15–20 Ω/□), W is its width, h is the thickness, i is the sensor current, and θ_p and θ_f are the angles of the magnetization angle of pinned and free layers, respectively. Assuming uniform magnetization for the free and pinned layers, for a linearized output, $\theta_p = \pi/2$ and $\theta_f = 0$.

When low to moderate magnetic fields are considered (as it is the case), Eq. 1 can be reinterpreted as [12]:

$$R = R_0 + S_B \bullet B \quad (2)$$

where R_0 is the spin valve resistance at zero magnetic field, S_B is the linear magnetoresistive parameter and B is the magnetic field component in the direction of the pinned layer. R_0 and S_B can be experimentally obtained from standard linear fits for being included in the model (from Fig. 2 and Table 1).

For the numerical modeling we used the FEM-based COMSOL Multiphysics software package. This package is the current evolution of the well-known FEMLab, which has already been successfully applied to the modeling of general physical problems including the calculation of GMR sensing structures in electrical and biotechnology applications [13].

The considered model, as displayed in Fig. 6, includes the main characteristics of the system, where the dimensions have been carefully considered. The bottom part of the section is silicon and the top part of the section is air. When an electrical current density flows through the aluminum strap, a magnetic field is generated, as shown in Fig. 6(a). The spin valve lies into this magnetic field, as easily observed. The shape of the field lines depends on the width of the current strap. In Fig. 6(a), a 10 µm width strap particularization is shown. The spin valve is modeled as a homogeneous region with field dependent resistivity. COMSOL allows considering point-dependent magnitudes, so resistivity of the spin valve can be expressed as $\rho(x,y)$, so taking into account field distributions. The resistance is then obtained by integration. Simulations

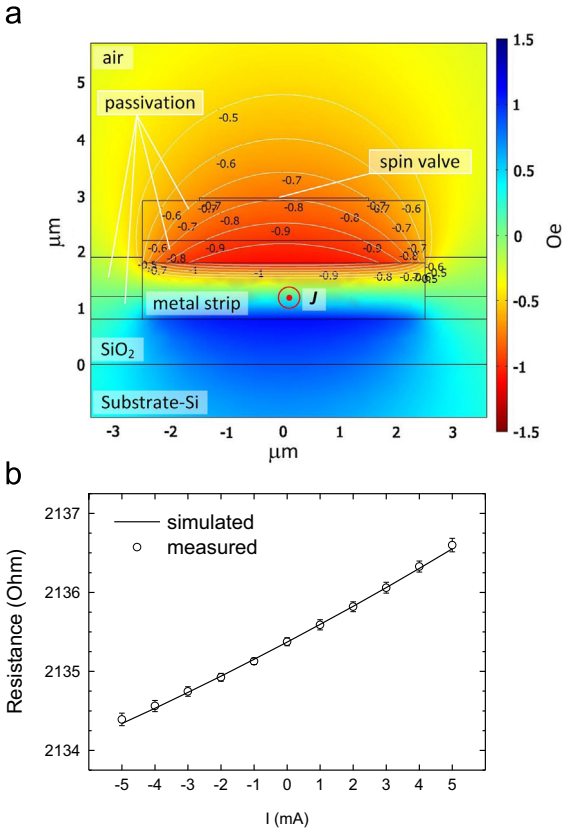

Fig. 6. 2D-FEM model of the CNM 2.5 µm based devices as current sensors: (a) model description including magnetic field distribution, (b) resistance of the spin valve against the driven current: experimental data and simulation results.

were performed by considering real parameters of the device, and the results are shown in Fig. 6(b). As observed, simulated results perfectly reproduce experimental data. It should be noted that the availability of precise FEM models is highly important for integration studies in order to reduce as much as possible the number of required prototypes in a design process.

3.3.3. *Frequency analysis*

Finally, for quantifying the bandwidth of the devices, AC measurements were performed. The characterization setup comprised a signal source (HP, 33120A), a power supply (Tektronix, PS2521G) and an oscilloscope (Tektronix, TDS3034). A moderate sinusoidal current of 20 mA-peak was driven through the current tracks of the different devices, with a frequency ranging from DC to 1 MHz. The devices were fed with a 1 mA DC current, and the alternate voltage taken from the output. The results are shown in Fig. 7, including different signal forms.

Theoretical bandwidth of GMR mechanisms is above 1 GHz [2], so frequency limitations are due, in this case, to undesired couplings. With a proper design, the bandwidth of these devices can be extended up to the MHz range [6].

4. Conclusions

The deposition of spin valve structures directly onto two different technologies based CMOS chips has been demonstrated in this paper. The characterization of so obtained devices has proven their high performance. With near future applications in mind, the noise level has been evaluated, displaying no major constrains regarding the SNR. A 2D-FEM model has also been developed, including the magnetic field dependence of the spin

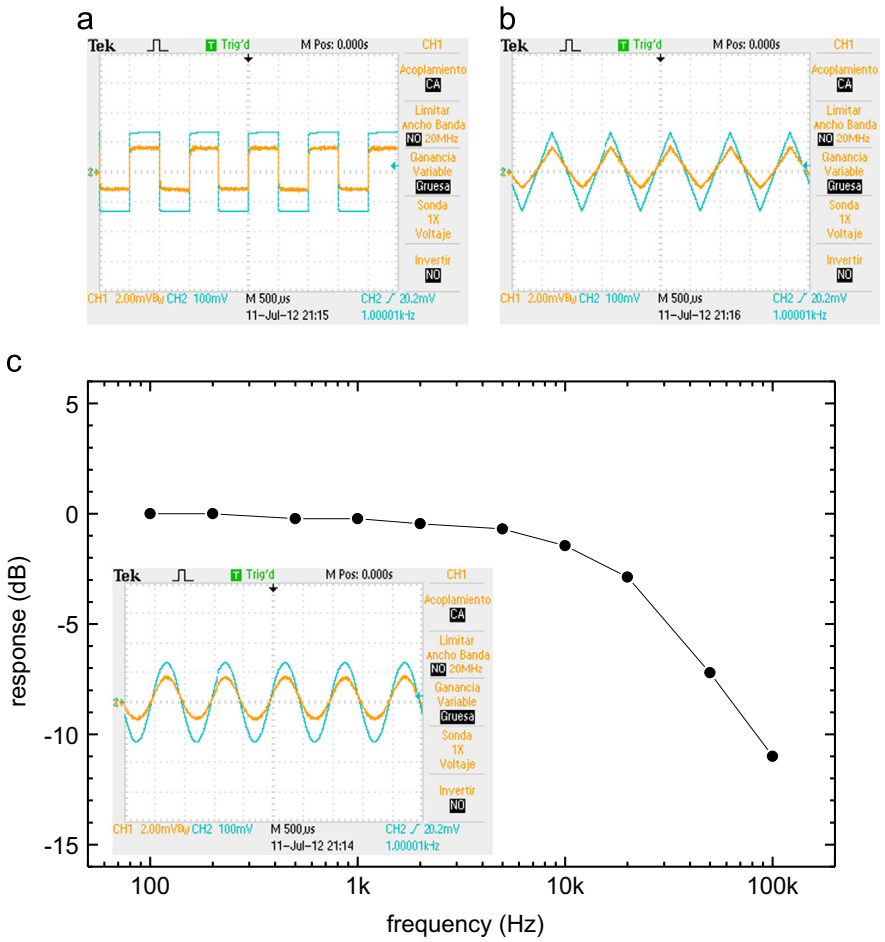

Fig. 7. AC behavior of the CNM 2.5 μm based devices as current sensors: (a) output for a square wave (1 kHz) driven current, (b) output for a triangular wave (1 kHz) driven current, and (c) frequency response to a sinusoidal driven current and output for such a wave at 1 kHz.

valves resistance in order to be used as a supporting tool in the design of systems involving similar technologies.

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