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Offset-Compensated Comparator with Full-Input Range in 150nm FDSOI CMOS-3D Technology

M. Suárez and V.M. Brea
Dept. of Electronics and Computer Science
University of Santiago de Compostela
Santiago de Compostela
E-15706, Spain
Email: manuel.suarez.cambre@usc.es

Carlos Domínguez Matas*, Ricardo Carmona**
Gustavo Liñán** and Ángel Rodríguez-Vázquez**
*AnaFocus
**Instituto de Microelectrónica de Sevilla (IMSE-CNM)
Sevilla, Spain

***Abstract*— This paper addresses an offset-compensated comparator with full-input range in the 150nm FDSOI CMOS-3D technology from MIT- Lincoln Laboratory. The comparator discussed here makes part of a vision system. Its architecture is that of a self-biased inverter with dynamic offset correction. At simulation level, the comparator can reach a resolution of 0.1mV in an area of approximately 220μm^2 with a time response of less than 40ns and a static power dissipation of 1.125μW.**

I. Introduction

Imagers and Vision systems are among the most difficult challenges for mixed-signal design. The design of imaging systems (sensors + readout + data conversion + controller + drivers) on CMOS chips has been making good progress during the last decade [1], [2], [3], [4]. The main design target for CMOS imaging chips is reproducing images with given accuracy and speed. The target of a vision system is different. Similar to imagers, they have 2-D light intensity maps as inputs. However, their outputs are not images, but reaction commands. Vision applications require to complete the full "sense → process → analyze → make decision" cycle. It involves large amount of data, especially in applications where high-resolution or high frame-rate are essential. Making a real-time decision, e.g. for controlling an autonomous moving device, also requires low latency from the system, which makes the analysis of the large input data set even more demanding.

The industrial state-of-the-art considers vision systems as seeing computers or computers that see. This is reflected on the architecture typically used for them, namely: an imager (image sensor) to acquire and digitize the sensory data and a host processor to handle this huge amount of raw data. Such brute-force approach does completely ignore the specifics of the data, the ways how interesting pieces of information emerge from the data, and hence results in highly inefficient systems. Not only conventional computer architectures are inadequate. Conventional algorithmic solutions used in these architectures are also inadequate. This fact has been highlighted in a very recent paper published in Vision System Design [5]. It states that brute force pattern matching, the conventional approach adopted by many system developers, is not the right tool in many applications. Instead, a majority of smart camera applications can be solved using only a small number of image processing algorithms that can be learned quickly and used very effectively. During the last few years authors have worked on mapping these simple algorithms (thresholds, blob analysis, edge detection, average intensity, binary operators,) onto dedicated computer hardware architectures composed of simple processors with mostly local interactions. Different system-on-chip solutions have been devised and realized on conventional single-wafer CMOS technologies [6], [7], [8]. These chips consist of 2-D arrays of multi-functional pixels which perform full parallel-processing of the incoming image flow to allow very high operation speed. However, a drawback of this architectural solution is that the fill factor decreases hence impacting the spatial resolution and the optical sensitivity.

This drawback can be precluded by resorting to the use of 3D integration technologies and splitting the multi-functional feature of the pixels among several layers: for sensors, for analog read-out and mixed-signal pre-processing; for memory and for digital processing. In such an architecture, the herein reported comparator plays the significant role of making the transition between images and digital codes and hence between the layers located near to the sensors and those located near to the digital processor.

This paper introduces an offset-compensated comparator with full-input range in the 150nm FDSOI CMOS-3D technology from MIT-Lincoln Laboratory. Section II outlines the challenges in the design of the vision architecture and the comparator. Section III addresses the comparator itself. Finally, the main conclusions from the work are drawn.

II. System architecture, Pixel and Comparator Challenges

Fig. 1 shows a schematic representation of a generic 3D architecture for vision. In our case, we have four layers, namely: one sensor layer which is bump bounded to a three-tier structure composed of a mixed-signal layer (Tier 3), a memory buffer (Tier 2) and a digital processing layer. The last three layers are interconnected via Through-Silicon-Vias with 3μm × 3μm pitch. Fig. 2 shows a block diagram of

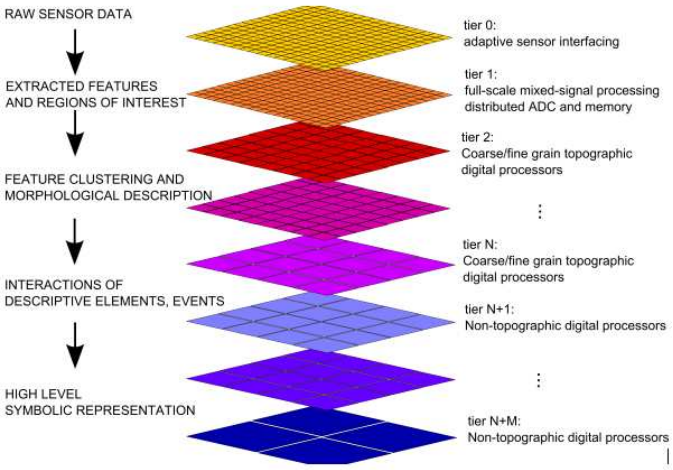

Fig. 1. A generic 3D architecture for a vision system.

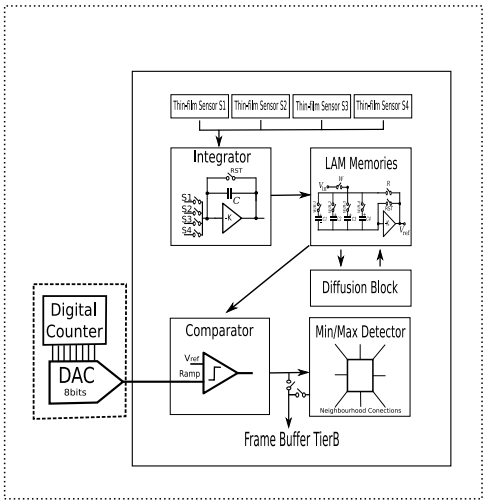

Fig. 2. Block diagram of a cell in the mixed-signal layer of the vision system where the herein reported comparator is allocated.

each cell in the mixed-signal layer whose functions are the following:

- Interfacing a photodiode through a trans-impedance amplifier.
- Analog storage of different samples of the input signal as needed to perform multi-scale image processing.
- Voltage-to-time transformation by comparing pixel the input voltage provided by the trans-impedance amplifier to a digitally-codified ramp.
- Spatial filtering of the input image to obtain the information needed to extract multiple scales.

The target is an architecture suitable for vision applications. The pixel-level parallelism with pixel per cell assignment is key to achieve this goal, leading to a more compact, less power-hungry and faster system than solutions based on conventional computers. Nevertheless, the challenges in the design flow abound.

Focussing on the comparator shown in Fig. 2, the vision system imposes a set of constraints:

- The cell should be as small as possible in order to attain a high resolution in a compact area. In our design, the targeted area for a cell is 50μm $\times$ 50μm. The comparator cannot occupy more than 15μm $\times$ 15μm.
- In terms of input range, the larger the better, as it makes it easier the design of its driving blocks (the trans-impedance amplifier, or LAM memories in Fig.2).
- In terms of resolution, 8 bits are needed. The trans-impedance amplifer determines that those 8 bits have to be reached within 800mV, what forces a resolution of 3mV in the comparator.
- The comparison time is given by the rate at which the trans-impedance amplifier provides the signal to be converted. Such a time is around 400ns.
- In the search for a battery-operated vision system, the power dissipation has to be minimized too.

III. Comparator Design

A. Architecture

A first taxonomy of comparators sorts them out in discrete- and continuous-time comparators [9]. The comparator introduced here belongs to the former type.

Many architectures are possible to realize a continuous-time comparator. Architectures with input differential pairs combined with output current mirrors are posed as the most straightforward approach. Many topologies are possible here. Nevertheless, in order to reach a wide input range, a complementary input differential pair, i.e. a PMOS and an NMOS differential pair, are needed. Also, in order to have enough resolution, (in our case below 3mV), cascode topologies as output current mirrors in conjunction with offset cancellation techniques are a must. All the above leads to cumbersome circuits, making it difficult to comply with the area constraint on the comparator (less than 15μm $\times$ 15μm).

Another family of comparators utilize the inverter as the fundamental building block. A particular realization is the so-called self-biased inverter. Fig. 3 displays its schematic view. The circuit implements voltage comparison with offset compensation through dynamic biasing. The circuit needs two non-overlapped clock signals. During the first phase, when the switch controled by $phiR$ is on and the one driven by $phiC$ is off, the value $V_{in1} - V_{QP}$ is stored between the capacitor plates. V_{QP} means the quiescent (also known as switching) point of the inverter. This is the value reached when the input and the output are shorted together. During the second phase, when $phiR$ is off and $phiC$ is on, the comparison between V_{in1} and V_{in2} occurs. The sampling of V_{QP} guarantees that the comparison is performed regardless its exact value, what ideally makes the comparator insensitive to mismatch. The sign of $V_{in1} - V_{in2}$ determines if the output of the comparison will be at the right or at the left of the quiescent point of the inverter. The comparator resolution, i.e. the minimum detectable differential signal at its input, is also enhanced with several gain stages in cascade. This is formulated in Eq. (1).

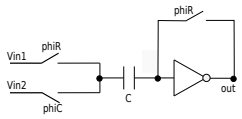

Fig. 3. Self-biased inverter as comparator.

$$\Delta_s = |V_{off}|_{res} + V_{DD}/\prod_i k_{si} \quad (1)$$

The parameter k_{si} is the gain of every stage, expressed as the product of its transconductance and its output impedance: $k_{si} = g_{mi}.r_{oi}$. The offset is kept at a residual value.

On the other hand, the high substrate resistivity of the SOI technology keeps substrate coupling and latch-up effects at negligible levels. Thus in the SOI technology, the variations caused by the digital circuits in the sensitive analog nodes in a mixed-signal design are very low when compared to the conventional bulk CMOS technology without any special technique like guard rings or differential topologies.

B. Transistor Realization in 150nm FDSOI CMOS Technology

The 150nm FDSOI CMOS-3D technology from MIT-Lincoln Laboratories offers resistors and capacitors as primitives of design. Besides, two types of transistors are available: transistors with low threshold voltage (lvt) and with medium threshold voltage (mvt).

Fig. 4 depicts three possible transistor realizations of the inverter of Fig. 3. Fig. 5 shows simulations run on the three circuits. The left hand-side figure displays the dc response of the three implementations. The right hand-side figure shows the gain around the quiescent point of every inverter. The transistor dimensions are those labeled on Fig. 4. Such sizes, given in microns, have been set to achieve high gain.

The gain of an SOI conventional CMOS inverter is lower than that obtained on bulk CMOS. The reason is found in the floating-body effects of the SOI technology [10]. The high electric fields near the drain generated with high V_{ds} voltages produce impact ionization. For an NMOS, the new generated electrons are collected at the drain terminal. The new generated holes are accumulated in the floating-body of the SOI. The lack of a body terminal prevents the holes from flowing out of the body. When the number of holes is sufficiently high, the potential body increases as much as to make the holes flow into the source terminal. As a consequence, there appears a sharp increase in I_{ds}, decreasing the output impedance (r_o), and thus the gain factor $k_s = g_m.r_o$. The sharp increase of I_{ds}, known as the kink effect, occurs when V_{ds} is sufficiently high. This is the case of conventional CMOS inverters, where values above the V_{ds} needed for the kink effect to happen are reached. Stacked transistors (e.g. cascode topologies) decrease the V_{ds} voltage swings in the transistors, avoiding the kink effect and enhancing the output impedance, hence the gain factor $k_s = g_m.r_o$. The simulations shown in Fig. 5 show that the parameter $k_s = g_m.r_o$ is very low in the 150nm FDSOI technology for a conventional CMOS inverter. The gain is

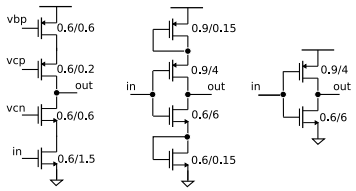

Fig. 4. Three transistor-level realizations for the inverter of Fig. 3. Left to right: the dual-cascode, the diode-connected and the classical two-transistor inverter.

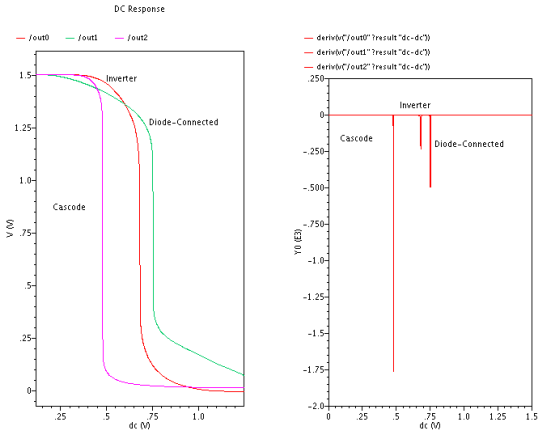

Fig. 5. Simulation results on the three different alternatives displayed on Fig. 4 for the inverter of Fig. 3.

improved with stacked transistors in the diode-connected and the dual-cascode inverters. The latter does not only yield the highest gain (around 1.8×10^3), but it also produces outputs much closer to the logic levels, making it the choice for the inverter realization of Fig. 3.

Our comparator makes part of an 8-bit single slope A/D converter. Its function is to compare the signal to be converted ($Vref$) with a ramp ($Vramp$). Fig. 6 sketches the concrete realization of our comparator. It works with the bottom-sampling technique, reducing the errors caused by clock feedthrough and charge injection. In so doing, the feedback NMOS switch controled by $phiR$ goes from HI to LO slightly before the transmission gate driven by $phiRD$. Subsequently, when both $phiR$ and $phiRD$ are LO, $phiC$ goes HI, and the comparison takes place. With this technique the charge injection and feedthrough errors present in the circuit come only from the feedback switches.

The two NAND gates are used as additional gain stages. They are implemented in complementary logic. Besides, the two NAND gates allow for external control over the end of comparison (end of A/D conversion) with the switching of EOC. During the reset, when $phiC$ is set to LO, the output from the first NAND goes HI regardless the output from the first gain stage, leading to a negligible dc power dissipation. Likewise, with the signal $End-Ramp$ set to LO, the static power dissipation in the second NAND gate and the subsequent inverter comes from leakage currents only.

The transmission gates allow for full-input range, from

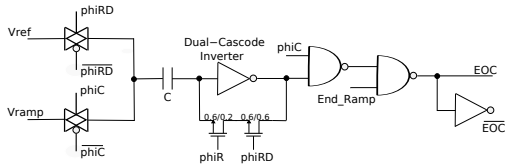

Fig. 6. Comparator of the 3D multi-layer vision architecture.

gnd to V_{DD} (1.5V). The feedback switches are realized with NMOS transistors. The reason is that the quiescent point is 500mV (see Fig.4), thus an NMOS switch suffices to transmit such a voltage. The two NMOS switches of the self-biased inverter are to balance the trade-off between charge injection/feedthrough and leakage currents. They are sized to keep a good enough trade-off between charge injection/feedthough errors (need for low area) and low leakage (need for a low W/L ratio). The use of mvt transistors in all the switches and transmission gates keeps leakage currents at a negligible level.

C. Performance Data

The parameter C is key to achieve a high performance comparator. Larger C values make charge injection and feedthrough errors be low. Thus, it is possible to have better resolution with larger C values. Nevertheless, larger C values give larger areas and longer reset cycles. The designer should choose the minimum possible C value. In our comparator, C=150fF is the minimum value capable of reaching 8 bits of resolution in the single-slope A/D converter, (3 mV in the comparator within a range of 800mV). The value of C=150fF leads to an area of less than 220μm^2.

The response time gives rise to another challenge through the resolution-speed trade-off given by Eq. (2).

$$V_{DD} = \Delta_d.k_d(T_c) \tag{2}$$

Δ_d is the dynamic resolution, k_d the dynamic gain, and T_c the comparison time. Eq. (2) states that for a comparator to reach a higher resolution, (smaller Δ_d values), higher dynamic gains (k_d) are needed. The comparator needs a certain time T_c to attain such gains.

Fig. 7 shows the speed-resolution trade-off for C=150fF. As expected, better resolutions lead to longer T_c's. At simulation level, our comparator reaches a resolution of 0.1mV in less than 40ns. T_c is measured as the time it takes the comparator to restore a logic level starting from the biasing point of the self-biased inverter. The reset time, i.e. the transition from a logic level back to the biasing point, takes around 130ns. Usually, a new comparison occurs after a new reset cycle. Nevertheless, in the A/D converter it is also possible to perform 256 comparisons with only one reset cycle. The fact that one of the inputs (the ramp) to the comparator be varying leads to an increase in T_c. This time is also the width of every voltage step of the ramp, which was found to be 150ns.

The static power in the comparator comes mainly from the dual-cascode inverter, consuming 0.75μA, hence 1.125μW.

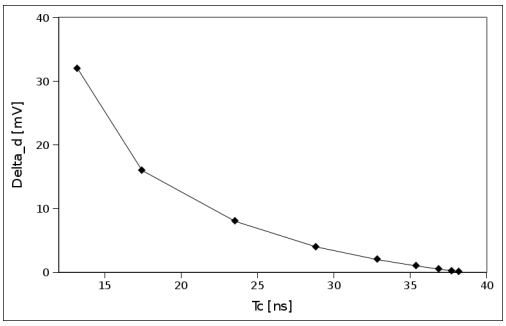

Fig. 7. Resolution-speed trade-off for the comparator with C=150fF.

The static power in the NAND gates and the final inverter comes only from the leakage currents, being negligible.

IV. Conclusion

This paper has addressed the design of an offset-compensated comparator with full-input range in the 150nm FDSOI CMOS-3D technology from the MIT-Lincoln Laboratory. The comparator makes part of an 8-bit single-slope A/D converter on a vision chip. Such a chip has been submitted to fabrication in October 2009. The comparator is implemented with a self-biased inverter using dynamic biasing to enhance resolution as the first stage. Two more gain stages realized with NAND gates are added in order to enhance resolution, to shorten the comparison time, and to control the end of comparison. The inverter of the first stage is realized with a dual-cascode topology due to the low value of the parameter $k_s = g_m.r_o$ in the targeted technology. In order to keep the residual offset at a low value, the bottom-sampling technique along with mvt transistors for implementing switches have been employed. At simulation level, the resolution of our comparator reaches 0.1mV for full-input range [0,V_{DD}] in an area of approximately 220μm^2 with a time response of less than 40ns and a static power of 1.125μW.

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