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1V CMOS Subthreshold Log-Domain Pulse Duration Modulators

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Abstract. A new CMOS circuit strategy for very low-voltage Pulse-Duration Modulators (PDM) is proposed. Optimization of voltage supply scaling below the sum of threshold voltages is based on Instantaneous Log Companding processing through the MOSFET operating in weak inversion. A 1V VLSI PDM circuit for very low-voltage audio applications such as Hearing Aids is presented, showing good agreement between simulated and experimental data.

Keywords: Low-Voltage, CMOS, Subthreshold, Log, PDM

1. Introduction

Pulse-Duration Modulation (PDM) processing is of special interest in output power stages for Class-D driving of low-impedance loads. Particularly, portable low-power VLSI system-on-a-chip applications like Hearing Aids require this type of signal modulation in order to extend battery life. Unfortunately, most existing CMOS solutions do not allow good-enough low-voltage compatibility for real single battery cell operation (down to 1.1V) [1, 2, 3], requiring supply multipliers which tend to decrease power efficiency, and increase both external components and Si area overhead as well. Other reported proposals make extensive usage of resistors or bipolar devices [4, 5]. A novel very low-voltage CMOS circuit strategy for PDM is presented here in the frame of the general Instantaneous Companding theory[6, 7, 8, 9]. The proposed implementation is based on the MOS transistor operating in the weak inversion region to optimize both the voltage supply scaling and the current consumption.

2. Principle of Operation

In general, a PDM signal (y_{out}) can be obtained from a 1-bit comparison between the base-band input (y_{in}) and a higher frequency triangle

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waveform (y_{tri}) as depicted in Figure 1. The signal y_{tri} may be generated by integrating a constant reference (y_{const}), which is periodically inverted according to an output window (y_{thmin},y_{thmax}).

(Place for Figure 1)

Due to the very low-voltage capabilities wanted for the circuit, a Log Companding approach is selected here to compress the internal voltage dynamic range. At this point, the MOS transistor operating in subthreshold region is proposed as the main basic building block to implement such type of signal processing. In particular, the Gate-Driven (GD) law from the general study presented by these authors in [10] will be used here as the companding function (F):

$$I = F(V) = I_S e^{-\frac{V_{TO}+nV_{bias}}{nU_t}} e^{\frac{V}{nU_t}} \qquad I_S = 2n\beta U_t^2 \tag{1}$$

where the Threshold Voltage (V_{TO}), Current Factor (β), Subthreshold Slope (n) and Specific Current (I_S) are defined according to the EKV device model [11]. Now, the externally linear description in the y-domain (i.e. current I) of Figure 1 must be translated into the compressed internal signal (i.e. voltage V). Since comparators are easily implemented in current mode, efforts are focused on the synthesis in the compressed V-domain of the following integrator equation:

$$\frac{dI_{tri}}{dt} = \pm\frac{I_{const}}{\tau} \qquad I_{thmin} < I_{tri} < I_{thmax} \tag{2}$$

where τ stands for a generic Time Constant. After applying the Companding function F from (1), the above state-space equation is translated to:

$$\frac{dV_{tri}}{dt} = \pm\frac{nU_t}{\tau} e^{\frac{V_{const}-V_{tri}}{nU_t}} \tag{3}$$

In case of storing the compressed signal V_{tri} across a grounded linear capacitor (C), expression (3) can be understood as a non-linear transconductance driving C:

$$\underbrace{C\frac{dV_{tri}}{dt}}_{I_{cap}} = \pm I_{tun} e^{\frac{V_{const}-V_{tri}}{nU_t}} \qquad I_{tun} \doteq \frac{nU_t C}{\tau} \tag{4}$$

where I_{tun} stands for the tuning current, which controls the period of the triangular oscillator (T_{tri}) according to:

$$T_{tri} = 2\frac{nU_t C}{I_{tun}} \left(\frac{I_{thmax} - I_{thmin}}{I_{const}} \right) \tag{5}$$

3. Low-Voltage CMOS Implementation

The integrator equation in (4) can be implemented through the basic building blocks developed by these authors in [10], which are a generalization of [12]. However, in our particular case of constant input (I_{const}), a more compact realization is proposed in Figure 2, where all marked MOS pairs are assumed to operate in weak inversion saturation.

(Place for Figure 2)

The triangle generator is displayed at the upper part of the figure and built through transistors M1 to M18. This oscillator consists of: the input compressor M1 generating the compressed constant input V_{const}, the non-linear transconductance pair M4-M5 driving the integrator capacitor C, and the output expander M2 that generates the triangle waveform I_{tri}. In order to obtain the desired I_{tri}, the expander requires the same reference level V_{ref} of the compressor (i.e. same source voltages between M1 and M2). Such low-impedance voltage copy is supplied by M3 and M12. Transistor M11 is used to ensure proper operation of grounded devices M12 and M13. Oscillation is forced by the feedback window comparator M15-M16, which alternatively changes the sign of the slope stored in a D-type flip-flop (DFF). A safe startup signal (V_{start}) should be required at the flip-flop for a proper initialization. Such memory element sets the charge and discharge phases of the capacitor C by switching the mirror M9-M10, so $I_{cap} = \pm I_{D4}$. The resulting Log compressed and expanded triangle waveform can be seen in Figure 3.

(Place for Figure 3)

An operational transresistance amplifier, made of devices M19 to M24 in the lower part of Figure 2, is also included to ensure low-enough input impedance. Such feature is of special interest in case of requiring an additional V/I conversion of the incoming signal, which can be performed with just a simple series resistor (and eventually a decoupling capacitor) as indicated in the same figure in dashed lines. The output PDM signal (V_{PDM}) is computed from the 1-bit voltage quantization of $(I_{tri} - I_{in})$. A proper quiescent bias $I_{bias} = (I_{thmax} + I_{thmin})/2$ must be designed to obtain a 50% PDM output in silence. Also, a typical structure for audio applications is depicted in Figure 2, where a digital buffer stage is fed by the V_{PDM} signal to operate the output receiver in Class D.

4. Design Example

Based on the circuit strategy proposed in previous section, a 100KHz Class-D output stage for 1.1V VLSI Hearing-Aids-on-a-chip has been implemented. In this case, a single slope (i.e. sawtooth) oscillator has been built with design parameters $I_{bias} = 1\mu$A, $I_{tun} = 100$nA, $C = 5$pF and $I_{th} = 4\mu$A. The complete PDM circuit has been integrated in a 1.2μm VLSI CMOS double-metal double-polySi process as depicted in Figure 4, where device area is about 0.10mm^2 without considering digital power buffers. Both BSIM3 simulated and experimental performances are reported in Table I under actual battery supply operation (1.1V to 1.5V). All boxed devices in Figure 2 were sized at $10 \times \frac{40\mu m}{3\mu m}$ to ensure weak inversion operation for the wanted range of currents. On the other hand, the remaining MOS transistors were designed with aspect ratios as long as allowed by the supply voltage to improve Drain-current matching between devices, so output offsets. In this sense, both Montecarlo simulations and experimental data return duty-cycle deviations (2σ) of less than 1%. Due to the target application in the field of Hearing Aids (i.e. low temperature-range, low-voltage supplies and receivers impedances $> 50\Omega$), the resulting static-power consumption is quite acceptable (i.e. $< 100\mu$A). In case of requiring narrower duty-cycle deviations, some feedback can be applied from the output buffers to the input of the proposed modulator in order to provide a self-biasing mechanism, like [13]. Finally, an electrical PDM stimulus sample and the corresponding acoustic output at the receiver are displayed in Figure 5. The harmonic distortion measured is quite satisfactory for integrated audio applications.

(Place for Figure 4)

(Place for Table I)

(Place for Figure 5)

5. Conclusions

The new CMOS design strategy proposed to implement PDM modulators allows strong voltage supply scaling-down below $V_{TON}+|V_{TOP}|$. A compact circuit structure has been reported working at very low

current. The circuit was fully integrated in standard CMOS technology and its experimental data was found in good agreement with simulation. As a result, this modulator is suitable for very low-voltage VLSI audio applications like Hearing-Aids-on-a-chip (1.1V to 1.5V).

Acknowledgements

Research partially supported by Spanish CICYT-TIC97-1159, CICYT-TIC99-1084 and European ESPRIT-FUSE-23068 projects.

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List of Tables

Table I. Typical results of the modulator at room temperature.

Parameter	Simulated	Experimental	Units
Min. Supply Voltage	1.1	1.1	V
Max. $V_{TON}+\|V_{TOP}\|$	1.3	1.2	V
Power Consumption	45	<50	μW
PDM Factor	2.6	2.7	μs/μA
Input Full Scale	4	3.9	μA_{pp}
Dynamic Range	>70	>63	dB
THD @90% Full Scale	<2.8	<3	%
Pulse Frequency	102	104	KHz
Duty-cycle Deviations (2σ)	<1	<1	%

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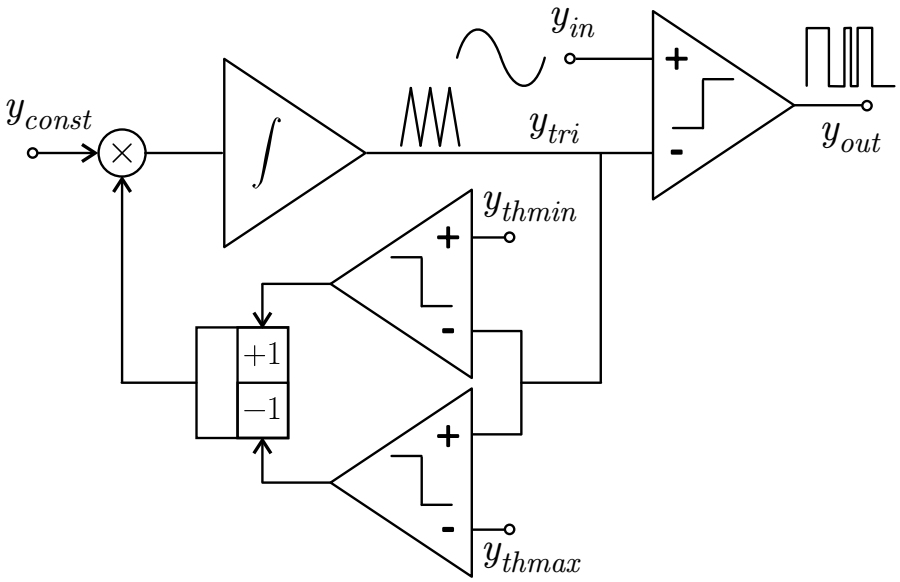

Figure 1. General design approach for PDM generation.

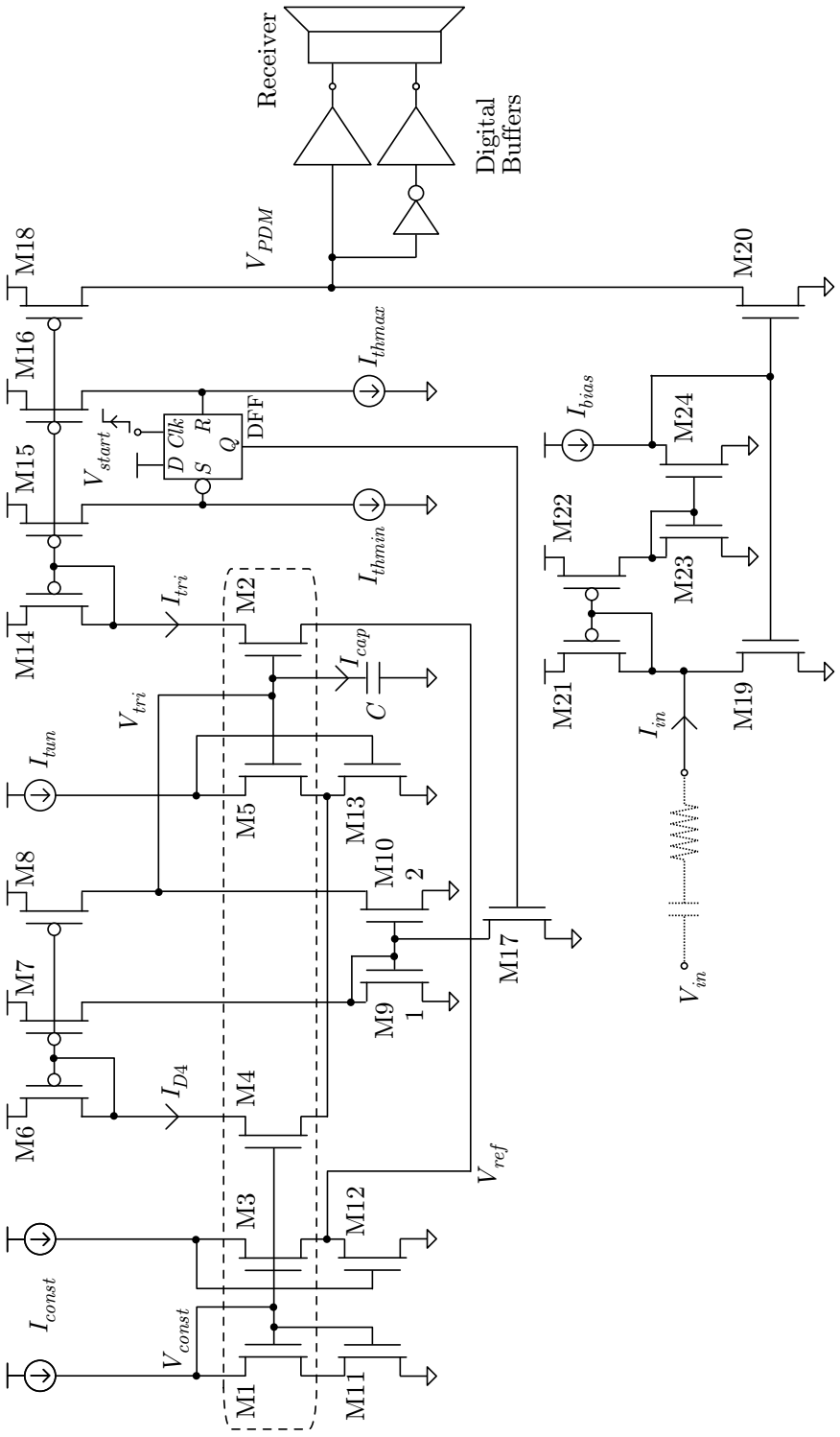

Figure 2. Simplified schematic of the PDM modulator.

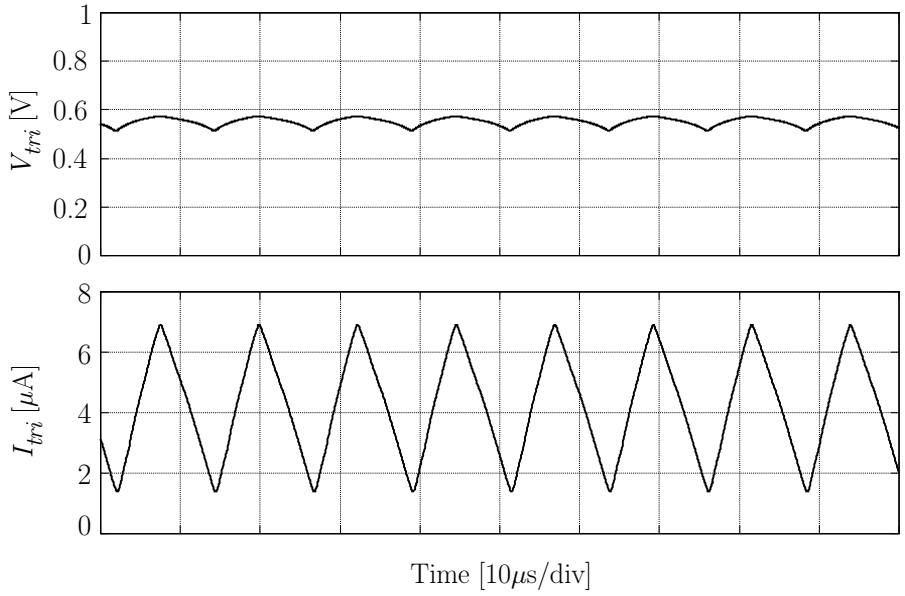

Figure 3. Simulated voltage across integrator capacitor (upper) and output current (lower) operating at 1.0V supply.

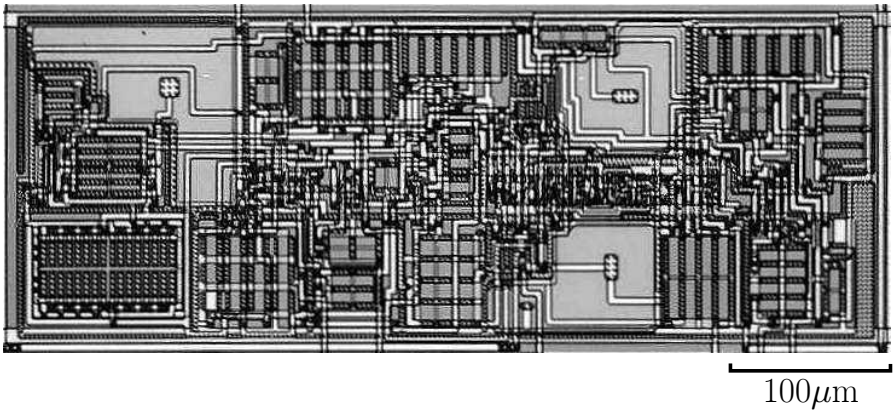

Figure 4. Microscope photograph of the PDM modulator.

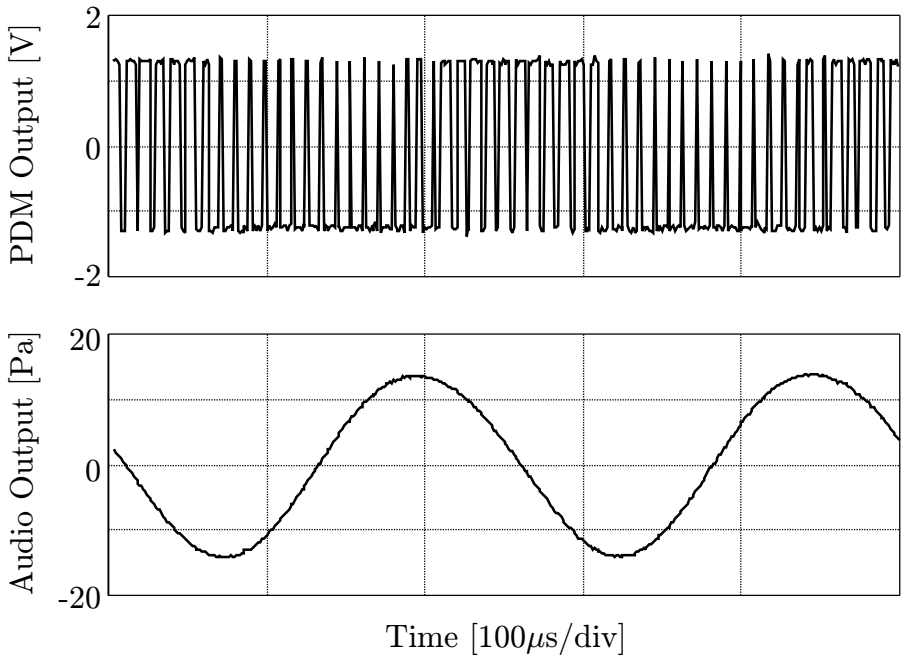

Figure 5. Experimental differential PDM and acoustic audio signal at receiver for I_{in}=2μA$_{pp}$@4KHz.

Keywords: Low-Voltage, CMOS, Subthreshold, Log, PDM

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