Low power LVDS transceiver for AER links with burst mode operation capability

Carlos Zamarreño-Ramos, Teresa Serrano-Gotarredona, Bernabé Linares-Barranco
Instituto de Microelectrónica de Sevilla IMSE-CNM, CSIC and Universidad de Sevilla
41012 Sevilla, E-mail: bernabe@imse.cnm.es

***Abstract*— This paper presents the design and simulation of an LVDS transceiver intended to be used in serial AER links. Traditional implementations of LVDS serial interfaces require a continuous data flow between the transmitter and the receiver to keep the synchronization. However, the serial AER-LVDS interface proposed in [2] operates in a burst mode, having long times of silence without data transmission. This can be used to reduce the power consumption by switching off the LVDS circuitry during the pauses. Moreover, a fast recovery time after pauses must be achieved to not slow down the interface operation. The transceiver was designed in a 90 nm technology. Extensive simulations have been performed demonstrating a 1 Gbps data rate operation for all corners in post-layout simulations. Driver and receiver take up an area of 100x215 μm^2 and 100x140 μm^2 respectively.**

I. Introduction

Computer capabilities for processing data have evolved at such high speed that the state of the art was unbelievable a few years ago. However, the sequential inspiration of the classic approach is not appropiate for certain applications (i.e. real-time vision processing). A possible solution to improve the processing efficiency is to emulate the human brain structure: a huge amount of computational units (neurons) with low processing capability, but massively interconnected between them. However, the physical interconnection of neurons in 2-D silicon systems is practically limited to a few neighbours.

AER (Address Event Representation) [1] is a neuromorphic protocol which allows the communication of a large array of neurons to another array using a reduced number of physical connections. The protocol operation is shown in Fig. 1. In the sender side, the neurons activity is encoded in their spike frequency; an arbitrer+encoder circuit translates the neuron spikes into digital addresses which are sent through a digital bus. In the receiver side, a decoder circuit sends a spike to the neuron which is identified with the received address. Receiver neurons just have to integrate the input spikes to reconstruct the activation state of the sender neurons. Communication between chips is performed using a classic four phase handshaking protocol. The AER allows a real-time virtual connectivity between two sets of n neurons placed in different chips using $log_2(n) + 2$ physical wires.

However, one of the main drawbacks of present AER systems is poor scalability. The size of AER parallel connectors and buses makes present state of the art AER multichip systems bulky and difficult to scale up [3]. A word serial protocol has been proposed [4], but it is not easily scalable to build large multichip AER systems. In this paper we propose to move from the parallel AER bus to a bit-serial LVDS AER link. The bits of each address are serialized and transmitted using just a single physical LVDS channel. LVDS standard combines the serial transmission with low power consumption and high speed data rates [5]. The high speed capability of the LVDS link allows us to transmit the bits of each AER address serialized in a single wire while preserving the transmission throughput.

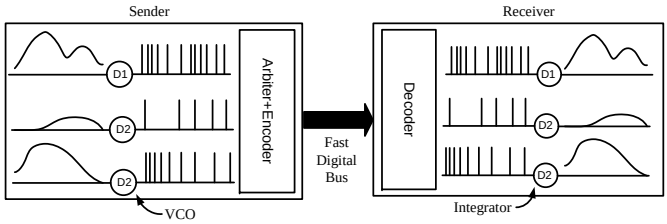

Fig. 1. AER link with parallel bus

II. The bit-serial AER LVDS link

Fig. 2 shows the block diagram of the bit-serial AER LVDS link proposed in [2]. The transmitter reads the input parallel AER data and implements the 4-phase handshaking protocol with the Request and Acknowledge signals. Moreover, the transmitter generates a Request signal for the receiver to get the permission to send new AER data. When the Acknowledge is received, the address is serialized into a pair of wires and two bits of preamble are added to the address. The receiver detects this preamble and gets ready to begin with the deserialization process. Finally, the data flow is coded in a Manchester format with the time reference given by a master clock.

The deserializer needs to extract the master clock used for the transmission to decode the input data flow. The Manchester codification always generates a transition in the transmitted data in the middle of the clock period. A CDR (Clock and Data Recovery) circuit is used to extract the master clock from the data. This signal is used to decode the Manchester data and put them into a parallel format. As the data flow generated by the AER chips is asynchronous, there can be long pauses without data transmission. Therefore, the deserializer has some kind of memory to save the extracted clock frequency during inactive periods.

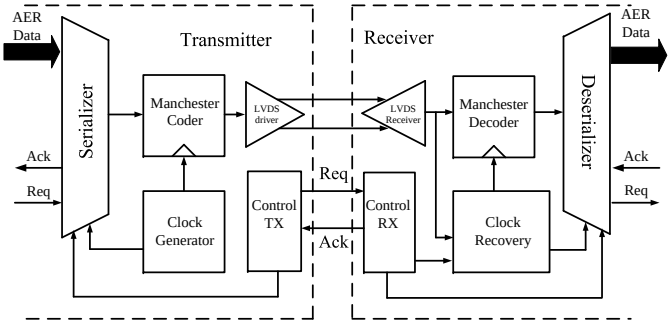

Fig. 2. Block Diagram of the bit serial AER LVDS link

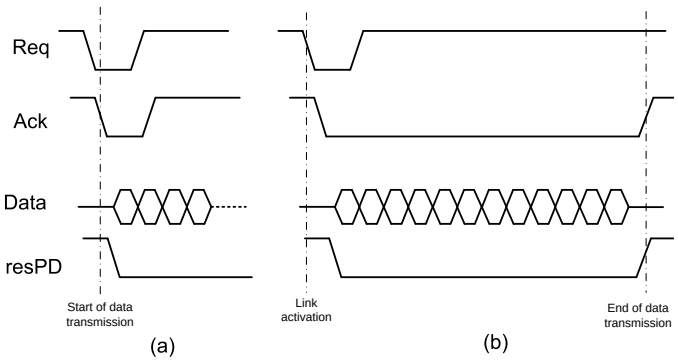

Fig. 3. (a) Classic AER protocol (b) Modification

The LVDS standard defines the physical layer of the serial AER link. It uses a differential data transmission scheme with low swing voltages to enable the low power and high frequency operation. The transmitter is configured as a switched-polarity current generator. A differential load resistor at the receiver end provides current-to-voltage conversion and optimum line matching at the same time. Another resistor can be optionally included at the transmitter side in order to reduce the effect of spurious reflected waves due to imperfect line termination, package and PCB parasitics, crosstalk, etc... The standard specifies a 250-450 mV output differential amplitude and a common mode range of 1.125-1.375 V. The minimum amplitude tolerated at the receiver is about 100 mV and a high input common mode range is required.

III. The AER protocol modification

The idea to reduce the power consumption in the serial AER LVDS interface is to switch off the LVDS circuitry during the pauses. The transmitter makes the decision of turning off the LVDS driver when there are no input data to transmit. When a pause occurs, the differential LVDS output lines evolve to the same voltage because there is no current flowing through the termination resistor. In this case, the LVDS receiver gives an uncertain output that depends on its input offset voltage and the noise. For this reason, a modification to the traditional AER protocol is required to detect the pauses, turn off the receiver and force a constant output for the deserializer.

Fig. 3 (a) presents the traditional AER protocol. In this case, the transmitter sets a low level in the Request line when new data are ready to transmit. If the receiver can manage this data and it is not busy, it gives back an acknowledgement, allowing the transmitter to begin with the data transmission. When the Request signal returns to high level, the Ack signal also does the same and new AER addesses can be transmitted.

The protocol modification proposed is shown in Fig. 3 (b). The basic idea to enable the burst mode operation is to keep the Acknowledge signal at low level until the data transmission and reception have finished. This way, the receiver gets activated when the Acknowledge line has a falling edge and must be disabled when a rising edge occurs. During the transmission process, no new Request pulses are allowed, implementing also a flow control mechanism. Signal resPD is generated by the deserializer and indicates the end of a data transmision with its rising edge.

The falling edge of the Request signal activates the transmitter and the LVDS outputs evolve to a certain well-known logic value (zero in this case). After a propagation delay, this request signal is sensed at the receiver side and, if the receiver is ready to receive new data, it is also turned on. The only requirement to the channel delay is that the LVDS outputs must be stable at its zero value when the receiver is activated. Therefore, the propagation delay of the Request path must be longer than in the LVDS one. The Request and Acknowledge signals must be propagated through two digital pads (one in the transmitter and other in the receiver). This time is very much longer than the time that the LVDS needs to recover from pauses.

The generation of the Acknowledge by the receiver can be done by the structure shown in Fig. 4. FF1 is a flip flop active with the falling edge of the clock signal and a reset input. FF2 is active with the rising edge and a preset input. FF1 and FF2 are configured as oscillators controlled by the signals req and resPD, respectively. Combining both outputs, "ack" has a falling edge when the "req" signal does and a rising edge when "resPD" does. "ack" remains constant at low level during the whole transmission process. "req-rx" is a signal generated by the deserializer and it is at low level when the receiver is waiting for the parallel part of the AER chip to read the address received. In this situation the receiver can not accept new transmissions and "ack" generation must be suspended.

IV. Driver design

A typical LVDS transmitter behaves as a current source with switched polarity [6]. The output current flows through the load resistance, establishing the correct differential output voltage swing. Depending on the input data, the polarity of the current source is set to positive or negative using some MOS switches. The output common-mode is controlled by a feedback loop. It senses the output common-mode, compares it to a reference and acts over the current sources. The voltage reference is generated by a bandgap circuit with high precision.

The main contribution to the power consumption in a LVDS driver comes from the current sources that are switched. If a

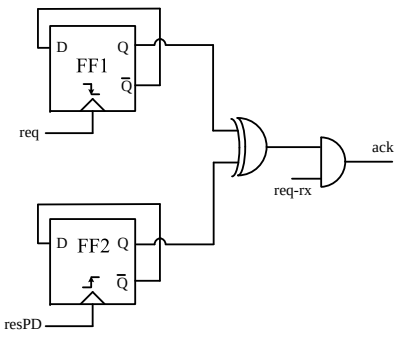

Fig. 4. Ack generation at the receiver side

350 mV differential amplitude is desired and the load resistor is typically around 50 Ω (the parallel of the two 100 Ω resistors located in the driver and receiver), current sources of 7mA are needed. This current source can be switched off during the pauses to save power. However, two design considerations must be taken into account to achieve real burst mode operation capability:

- When the driver is switched off, the output common-mode must be preserved until the new data transmission. When no current is flowing through the load resistor, the common mode evolves without control of the feedback circuitry. If the common-mode information is lost, it takes a long time to recover it because the control circuit must be very slow for stability issues.
- As high speed data are going to be transmitted through the driver, the switching mechanism must be fast enough to not slow down the event transmission rate. That is why very fast switchable current sources are required to operate with high data rates. Moreover, switching current sources of large value with low transient times cause current peaks that can affect to the stability of the common mode. This must be minimized for a proper operation.

Fig. 5 shows the schematic of the proposed LVDS driver optimized for burst mode operation. The digital controller generates the input signals for the switches and the enable signal enTX when new data is ready to transmit. When the driver is enabled, the bias voltages PBIAS and NBIAS are forced by the CMFB (Common Mode Feedback) circuit. In this configuration, the driver works in the same way than the one reported in [6] and the output common mode is controlled by the CMFB circuit. When the driver is disabled, these bias voltages are pulled up or down by specific circuitry, switching off the current sources. These bias voltages are given by the CMFB circuit during the driver normal operation.

The resistors R_s are used to sense the output common voltage. The value of these resistors must be high enough to not degrade impedance matching, so a $50k\Omega$ value was used. This internal high impedance node can be also used to maintain the output common mode voltage during the pauses. Voltage VREF will be imposed by a voltage buffer. This block

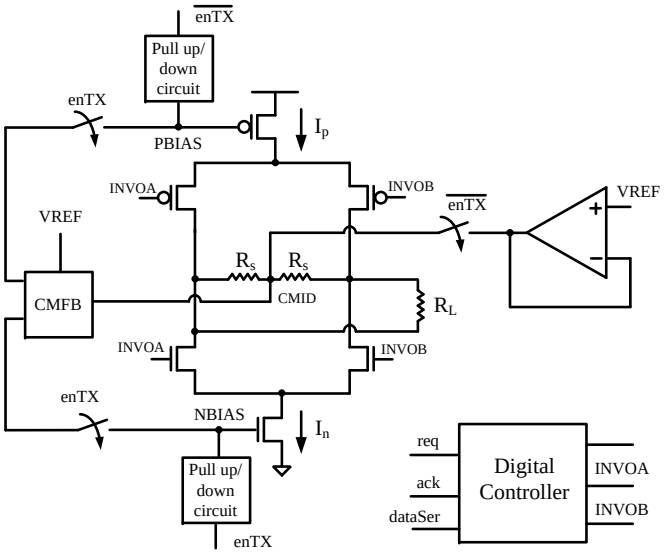

Fig. 5. LVDS driver for burst mode operation

does not need to be very fast, so it can be designed to have low power consumption. The CMFB circuit always sees a constant voltage at its input. Then, the information contained in PBIAS and NBIAS about the output common mode and the differential amplitude is mantained until the arrival of new data.

Fig. 6 (a) shows the schematic of the CMFB circuit used in this design. The input differential pair compares the filtered version of the common mode voltage sensed in the driver with the reference VREF. The current imbalance generated by the comparator is mirrored to the current sources of the driver with a gain K=50. If the feedback loop is stable, the steady state will converge to a common mode equal to the reference. The gain K is chosen high to keep the power consumption much lower than in the LVDS driver. $R_c = 200K\Omega$ and $C_c = 7{,}5pF$ form a first order low pass filter that ensures a phase margin around 60º for the feedback loop. To achieve a differential amplitude of V_{od}, the bias voltage of the CMFB circuit must be:

$$I_{bias} = \frac{2V_{od}}{KR_L} \tag{1}$$

The passive pull up/down circuits used in the design and its basic operation are shown in Fig. 6 (b) [7]. The dashed line component represents the parasitic capacitor associated with the gate node of the PMOS and the NMOS transistors. Capacitors C_p are used to pull up/dwn the gate voltage of the transistors with drastically reduced transition time and minimizing the current peaks generated by the switching. When the driver is turned on, the gate voltages are imposed by the CMFB circuit (V_{ON} voltage). When a pause starts, the signals enTX and enTXnot change and there is a charge distribution between the parasitic capacitor C_{pp} and C_p. This causes a change in the gate voltage that can be calculated writing the charge conservation equations before and after the

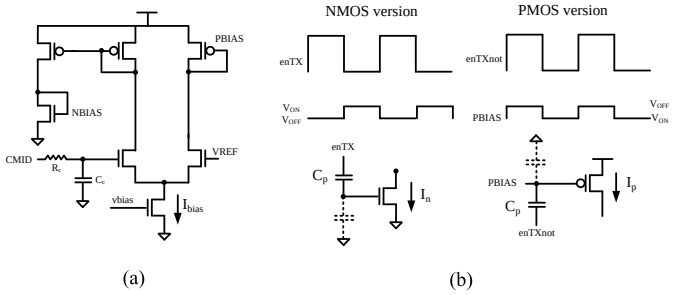

Fig. 6. (a) Common mode control circuit (b) Passive pull up/down technique

switching, resulting in:

$$\Delta V = |V_{ON} - V_{OFF}| = \frac{C_{pp}}{C_p + C_{pp}} V_{DD} \tag{2}$$

V. Receiver design

The classical LVDS receiver is based on a hysteresis comparator to avoid glitches in the output signal due to the input noise. The classic architecture of a hysteresis comparator, shown in Fig. 7 (c), uses a positive feedback loop to get enough gain and speed to convert the LVDS signal into a rail-to-rail one. The hysteresis range can be controlled by the aspect ratios of the PMOS transistors as shown in equation 3. However, the input common-mode range is limited in this architecture to keep the differential pair and the feedback loop transistors in saturation. A preamplifier can be added at the input of the comparator to increase the common-mode range and relax the specifications of the comparator, as shown in Fig. 7 (a).

$$\Delta V_{hys} = \frac{2\left(\sqrt{\alpha}-1\right)}{\sqrt{1+\alpha}} \sqrt{\frac{2I_b}{\mu_n C_{ox}\left(W/L\right)_{IN}}} \tag{3}$$

where $\alpha = (W/L)_5/(W/L)_7$. A ΔV_{hys} = 80mV was chosen in this design.

Fig. 7 (b) represents the architecture of the preamplifier [6]. The folded-cascode configuration allows a large gain-bandwith product independent on the input common-mode. The output of the PMOS input differential pair is set to a low DC voltage via the folded cascode structure, so the input stage operation becomes less sensitive to the input common-mode. Moreover, the internal node of the cascode configuration provides a low impedance output node that pushes the internal pole to high frequencies. The load resistances to the output stages determine the gain, the output common-mode and the bandwith of the amplifier, so they have to be carefully designed. However, as the comparator can be designed with lower aspect ratio devices because of the preamplifier addition, the load capacitance can be minimized reducing the impact of the resistors in the frequency response. For this design, with $I_{b1} = 1mA$ and $I_{b2} = 1{,}3mA$, a 707 Ω resistor was chosen.

$$V_{out,CM} = V_{DD} - R\left(I_{b2} - \frac{I_{b1}}{2}\right) \tag{4}$$

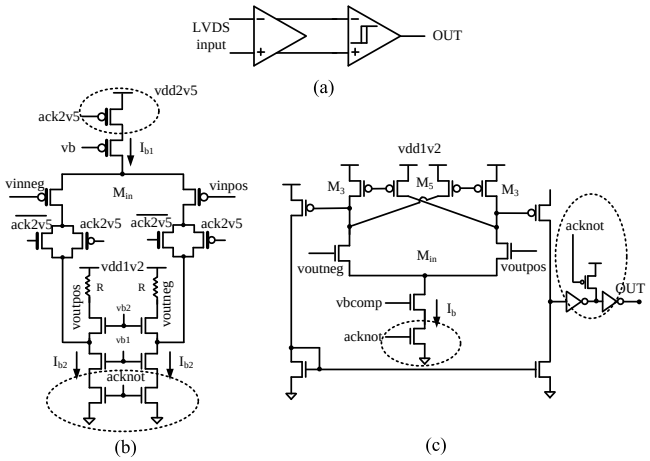

Fig. 7. (a) Receiver architecture (b) Preamplifier (c) Hysteresis comparator

$$Gain = -g_{m,IN} R \tag{5}$$

The power consumption of the receiver is mainly due to the bias currents of the preamplifier and the comparator. These two circuits are not needed during the pauses if the comparator output is forced to have a constant value (zero in this design). Therefore, their bias can be disabled during the pauses using the information given by the "Ack" signal. The receiver must operate normally when this signal is at low level and be switched off when it is at high level. The switches marked in Fig 7 are used to turn off the bias currents during the pauses, switching the transistors by their sources. As this is a low impedance node, the transition times between on and off are very small and a real burst mode operation can be achieved. The only drawback is that these switches must have a very low on resistance because the current flowing through them is high.

The ST 90nm technology used in this design has several types of transistors. The standard transistor uses a supply voltage of 1-1.2V and has the minimum gate length. There are also transistors with thick gate oxide that work with a 2.5V voltage supply, intended to be used for I/O applications. As the LVDS standard specifies excursions in the differential voltage until 1.5V, it is impossible to generate or decode an LVDS signal with the standard transistors. Therefore, the 2.5V transistors are mandatory for the driver implementation. A significant amount of power can be saved in the receiver by mixing the high voltage transistors with the standard ones[8].

As we discussed before, the voltage at the output of the preamplifier differential pair is low to allow a wide common mode range operation. This permits to use standard low voltage transistors in the folded-cascode stage. Moreover, the standard transistor has a shorter channel length and higher transition frequency, so the gain-bandwidth product can be enhanced with lower currents. As the preamplifier output is limited to 1.2V, the comparator can be totally designed with low voltage transistors.

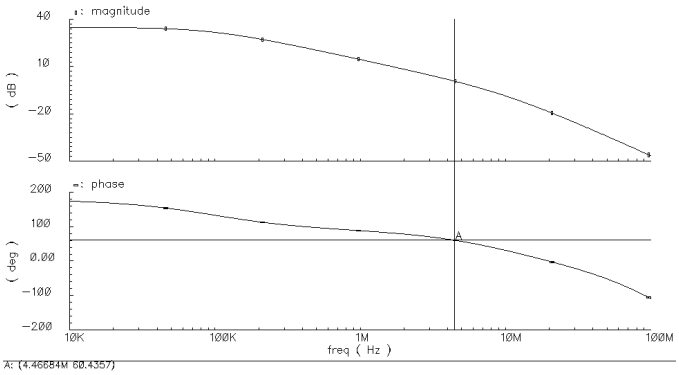

Fig. 8. Open Loop common-mode frequency response

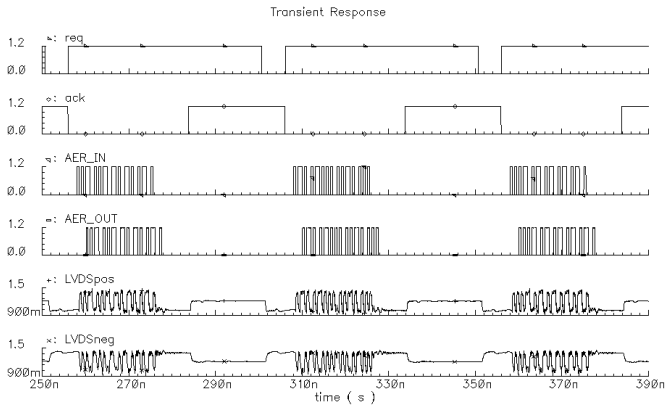

Fig. 9. Transient simulation of the AER LVDS transceiver

VI. Simulation results

The proposed architecture for the AER-LVDS transceiver has been implemented in a 90 nm STMicroelectronics technology and simulated to verify its performance. The LVDS channel was modelled in the simulation using a lossy transmission line. It was modelled using the "Transmission Line Model Generator (LMG)" tool provided by Cadence. The simulations were performed with the ESD protection circuitry and a simple LRC model for the package to check the robustness of the architecture. The influence of the bonding inductance associated with the supply voltage lines was also taken into account.

The driver common-mode stability is given by the frequency reponse of the feedback control loop. A large enough gain in the open loop response is necessary to ensure that the difference between the output common-mode and the bandgap reference is small. Moreover, as the control loop exhibits a low pass type response, a phase margin larger than 45-50º would be desirable in order to avoid excessive overshoot in the common-mode response. Fig. 8 shows the AC simulation performed to the check the open loop transfer function for the common-mode control loop. A gain around 35 dB and a phase margin of 60º can be observed. Both quantities are enough for our design requirements and guarantee the closed loop stability.

Fig. 9 shows the post-layout simulation for the transceiver operation. "req" and "ack" signals are the lines used to implement the AER protocol. As it was discussed before, the ack signal serves as transmission enable signal and remains at low level during the whole transmission process. "AER_IN" and "AER_OUT" represent the serial input and output signals, respectively. The transmission is carried out properly except for the delay caused by the channel propagation time. "LVDSpos" and "LVDSneg" are the LVDS signals. The data rate was 1Gbps for a Manchester code, so pulses of 500ps width are being transmitted.

Fig. 10 shows the current consumption in the burst-mode operation. Signal "vdd2v5TX" represents the current consumption through the 2.5V supply in the transmitter. The current during the pauses are about 380μA and it is mainly due to

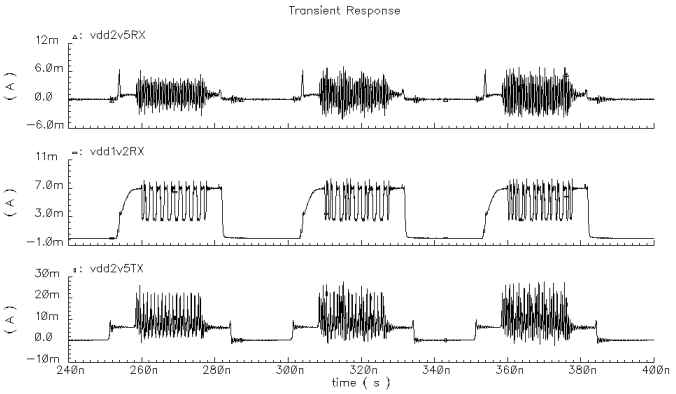

Fig. 10. Current consumption in the driver and receiver

the common-mode feedback control circuit that remains active. The mean current is 9.643mA in the regular operation with the driver switching with the input signal. Signals "vdd2v5RX" and "vdd1v2RX" are the currents that the receiver draws from the 2.5V and 1.2V supply voltages, respectively. In this case, the sleep current is 15.38μA for "vdd2v5RX" and 15.86μA for the "vdd1v2RX". The mean currents when the receiver is on are given by 1.136 mA for the 2.5V supply and 5.285mA for the 1.2V one.

The operation of the driver current sources switching circuits can be seen in Fig. 11. "enTX" is the signal used in the driver to switch on the circuit when new AER addresses are ready to be sent. When at high level, the gate voltages of the current sources present in the driver are imposed by the common-mode control circuit. If a pause is detected, "enTX" has a falling edge and it produces the charge distribution described in section IV, rising the PMOS bias voltage and decreasing the NMOS bias voltage. These transistors are OFF in this situation and the current flowing through them is negligible.

Another important issue is to study the impact of the process and mismatch variations over the transceiver performance. The process variations affect mainly to the impedance matching and the differential amplitude, due to the drift of the

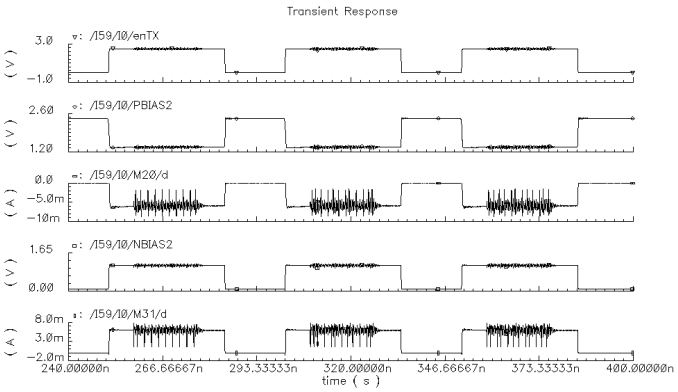

Fig. 11. Current source switching scheme operation

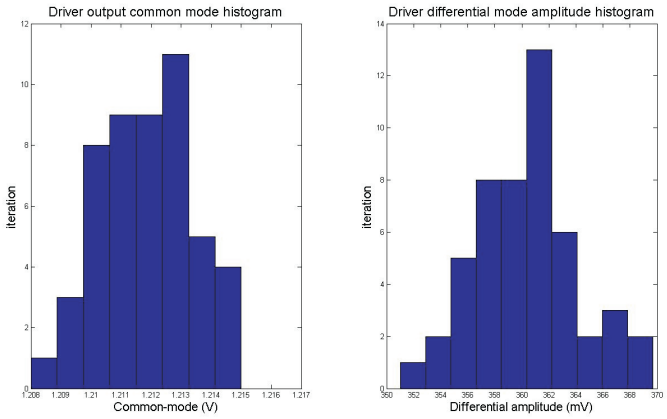

Fig. 12. Montecarlo simulation results

TABLE I
CORNER ANALYSIS

MOS	RC	V_{dd}(V)	T(°C)	V_d (mV)	V_{cm} (V)
TT	Typ	Typ	27	345.1	1.219
FF	Min	$+5\,\%$	80	374.3	1.224
SS	Max	$-5\,\%$	0	320.2	1.211
SS	Max	$-5\,\%$	80	318.6	1.207
FS	Max	$+5\,\%$	0	335.4	1.2
FS	Min	$-5\,\%$	80	357.4	1.23
SF	Max	$+5\,\%$	0	327.8	1.2
SF	Min	$-5\,\%$	80	347.0	1.27

termination resistance and the driver bias current. A double termination scheme with two 100 Ω resistors at the receiver and the transmitter sides were used to reduce the effect of the reflected waves caused by the imperfect impedance matching.

To minimize differential amplitude variations, the bias current in Fig. 6 (a)was generated using the bandgap voltage and a poly resistance, having $I_b = V_{BG}/R_{poly}$. The termination impedance was also implemented using the same type of resistor. The termination resistor in the transmitter will have the same process variations. The resistor in the receiver do not have be correlated, but, as it is in parallel with the transmitter one, the error in the equivalent resistance is reduced. Then, a significant reduction in the differential amplitude variation can be achieved by usign this technique. Table I shows the differential amplitude and the output common-mode obtained in the corner simulation.

The mismatch impacts on the output common-mode definition due to offset in the differential pair that senses and compares the common-mode with the reference. Montecarlo simulations show that the output common mean is around 1,21 V, with $\sigma_{CM} = 1{,}753\ mV$. The differential mode mean was $360{,}2\ mV$ and $\sigma_{diff} = 3{,}8\ mV$. Fig. 12 shows the histograms for the output differential amplitude and common-mode.

VII. CONCLUSION

A novel LVDS transceiver architecture intended to be used in serial AER-LVDS links was designed on a 90nm technology. The circuit saves power respect to traditional implementations switching off the LVDS circuitry during data pauses, taking advantage of the asynchronous data flow generated by AER chips. The circuit has been implemented up to the layout level and intensive post-layout simulations were performed in order to check the system operation. The transceiver is able to operate at 1Gbps data rate in all the technology corners and mismatch conditions with low power consumption. This circuit, combined with the one reported in [2], will allow serial high speed LVDS AER data transmission for AER systems with optimized power consumption.

ACKNOWLEDGMENT

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