Design of a CMOS closed-loop system with applications to bio-impedance measurements

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A B S T R A C T

This paper proposes a method for impedance measurements based on a closed-loop implementation of CMOS circuits. The proposed system has been conceived for alternate current excited systems, performing simultaneously driving and measuring functions, thanks to feedback. The system delivers magnitude and phase signals independently, which can be optimized separately, and can be applied to any kind of load (resistive and capacitive). Design specifications for CMOS circuit blocks and trade-offs for system accuracy and loop stability have been derived. Electrical simulation results obtained for several loads agree with the theory, enabling the proposed method to any impedance measurement problem, in special, to bio-setups including electrodes.

1. Introduction

Impedance is a useful parameter for determining the properties of matter [1]. Today, many research goals are focused to measure the impedance of biological samples. There are several major benefits of measuring impedances in medical and biological environments: first, most biological parameters and processes can be monitored using its impedance as marker [2–5]. Second, bio-impedance measurement is a non-invasive technique and, third, it represents a relatively cheap technique in labs. Impedance Spectroscopy (IS) in cell cultures [6] and Electrical Impedance Tomography (EIT) in bodies [7] are examples of the impedance utility in this field.

For the problem of measuring a given impedance Z_x, with magnitude Z_{xo} and phase ϕ, several methods have been reported. Commonly, these methods require excitation and processing circuits. Excitation is usually done with Alternating Current (AC) sources, while processing steps are based on coherent demodulation principle [1] or synchronous sampling [8]. In both, processing circuits must be synchronized with excitation signals, as a requirement for the technique works, obtaining the best noise performance when proper filter functions (High-Pass (HP) and Low-Pass (LP)) are incorporated. Block diagrams for both are illustrated in Figs. 1 (a) and (b), respectively. The main drawback for the Ackmann method [1] is that the separated channels for in-phase and quadrature components must be matched to avoid large phase errors. Synchronous sampling proposed by Pallás avoids two channels and demodulation, by selecting accurate sampling times, and adding an HP filter in the signal path to prevent low-frequency noise and sampler interferences. Both work as feed-forward systems: the signal generated on Z_x is amplified and then processed. The setups for bio-impedance measurements usually include electrodes between their components as sensor interface between the electronic instrumentation and the bio-samples, so when excitation signals are applied, the electrodes' performance could be considered as part of the load is being excited from driving circuits point of view. A detailed description of the electrode models for biological measurement can be found in [5]. The presented work proposes a closed-loop method for bio-impedance measurement based on the AC voltage source application, with constant amplitude, to impedance under test (ZUT). This method can be applied to electrode-based sensor systems, solving the main problems of using electrodes and their impedance frequency dependence in the following forms: first, limiting by design the voltage applied to electrodes. This allows biasing the electrodes at the linear operation region. Second, it permits incorporating the frequency dependence of the electrode impedance to design equations, making easier the selection of the working frequency and allowing the optimization of the system performance, since it could be possible to set the frequency for optimum system

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response. Once these electrode constrains are considered, the proposed circuits deliver magnitude and phase impedance signals directly in easy from to be acquired: a time constant voltage, for magnitude, and the duty cycle of a digital signal, for phase.

This paper in organized as follows: Section 2 describes the proposed CMOS closed-loop system for impedance measurement. In Section 3, the main circuits employed for impedance measurement are reported. Design system considerations for loop stability are given in Section 4. Simulation results for several types of loads and setups will prove the correct performance of the proposed system in Section 5. Conclusions are underlined in Section 6.

2. Proposed impedance measure system

The proposed circuits for the measurement of impedance magnitude, Z_{xo}, consider an AC current excitation signal, with ω frequency. The circuits are designed to work maintaining a constant amplitude across the load (V_{xo}=cte), known as Potentiostat (Pstat) condition. The proposed circuit block diagram, shown in Fig. 2, has the following as main components: an Instrumentation Amplifier (IA), a rectifier, an error amplifier, and a current oscillator with programmable output current amplitude. The voltage gain of the instrumentation amplifier passband is α_{ia}. The rectifier works as a full wave peak-detector,

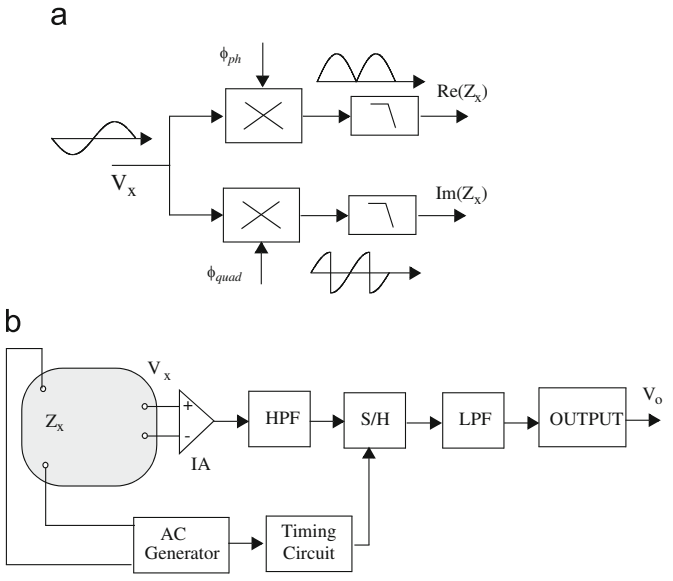


Fig. 1. (a) Coherent demodulation. (b) Synchronous sampling.

sensing the V_o peak-to-peak voltage value. Its output is a time constant voltage, V_{dc}, with α_{dc} gain ($V_{dc}=\alpha_{dc}\alpha_{ia}V_{xo}$). The error amplifier, with α_{ea} gain, will compare the DC signal with a reference, V_{ref}, to amplify the difference. The current oscillator generates the AC current to excite the load. It is composed of an external AC voltage source, V_s, an Operational Transconductance Amplifier (OTA) with g_m transconductance, and a four-quadrant voltage multiplier with K constant. The voltage generated by V_s, V_{so},sinωt, is multiplied by V_m, and current converted by the OTA. The equivalent transconductance from the magnitude voltage signal, V_m, to the excitation current, i_x, is $G_m=g_m\cdot V_{so}\cdot K$. A simple analysis of the full system gives the approximated expression for the voltage amplitude at V_x

$$V_{xo}=\frac{V_{ref}}{\alpha_{ia}\cdot\alpha_{dc}} \tag{1}$$

when condition

$$Z_{xo}G_m\alpha_{ea}\alpha_{ia}\alpha_{dc}\gg 1 \tag{2}$$

is satisfied. It is defined the system closed-loop gain as $\alpha_o=Z_{xo}G_m\alpha_{ia}\alpha_{dc}\alpha_{ea}$. Voltage in Eq. (1) remains constant if α_{ia} and α_{dc} remain constant too. Hence, Pstat condition is fulfilled if condition in Eq. (2) is true. Considering the relationship between the current i_x and the magnitude voltage V_m ($i_{xo}=G_m$, V_m), the impedance magnitude is

$$Z_{xo}=\frac{V_{xo}}{G_m}\cdot\frac{1}{V_m} \tag{3}$$

Eq. (3) shows that from voltage V_m, the impedance magnitude Z_{xo} can be calculated, since V_{xo} and G_m are known from Eq. (1) and the design parameters. The impedance phase could also be measured with V_ϕ signal in Fig. 2, by considering the input voltage oscillator, V_s, in phase with the i_x current. This signal can be squared or converted into a voltage digital signal, to be used as time reference or sync signal (V_{xd}). The V_o voltage is also converted into a squared waveform (V_{od}) by means of a voltage comparator. If these two signals feed the input of an EXOR gate, a digital signal will be obtained, V_ϕ, called phase voltage, whose duty cycle, δ, is directly proportional to the phase to be measured.

From Eq. (2), the range of Z_{xo} magnitude value must be known in order to be satisfied. However, depending of the set-up for measuring employed, the Z_{xo} can include different parasitics. In four-wire based systems, these effects are minimized by the high input impedance amplifier, but in two-wire ones, the amplifier output voltage delivers the contribution of both impedances, namely from the set-up and ZUT, so Z_{xo} must be known and quoted before to define the circuit specifications. Fig. 2 illustrates a two-wire system. The impedance to be measured should be placed between electrodes e_1 and e_2.

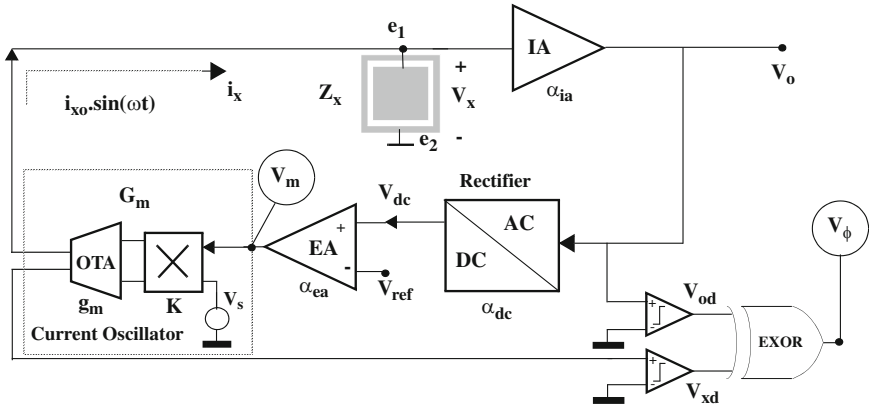


Fig. 2. Proposed circuit blocks for impedance sensing. Magnitude and phase are obtained from signals V_m and V_ϕ, respectively.

The amplitude of the input voltage instrumentation amplifier, V_{xo}, can be now limited, thanks to the feedback loop, enabling the proposed system for impedance measures based on electrodes [5], as is the case of bio-impedance measure systems [9]. Changes with frequency in magnitude of electrode impedances can be incorporated to Z_{xo} in order to satisfy Eq. (2).

Absolute errors at impedance magnitude measurements will be dependent on circuit parameters α_{ia}, α_{dc} and G_m, as expressed in Eqs. (1) and (3). These error sources are similar and common for other impedance techniques [1,2]. Also, phase errors have an additive contribution from the instrumentation amplifier phase response, which have to be considered. In many applications, the relative impedance changes, evaluated after system calibration, contain the most relevant information and relax the circuit performance specifications. Errors in the aforementioned parameters could limit the system performance.

3. CMOS circuit design

The circuits required to implement the blocks in Fig. 2 have been designed in a 0.35 μm CMOS technology for 3 V power supply. Design parameters were adjusted initially for 10 kHz frequency, with $Z_{xo}=100\,k\Omega$. The parameters chosen were $\alpha_o=100$, $\alpha_{ia}=10$, $\alpha_{dc}=0.25$, $\alpha_{ea}=500$, $G_m=1.2$ uS, and $V_{ref}=20$ mV. The Z_{xo} value can belong only to impedance to be measured or include also the set-up contribution. In all cases, its minimum value must be known to fulfil Eq. (2).

3.1. Instrumentation amplifier

The instrumentation amplifier circuit schematic is shown in Fig. 3. It is a two-stage amplifier: a transconductance input stage and a trans-resistance output stage, where filtering functionality has been included. The passband frequency edges were designed according to the frequency range common to impedance measurements and spectroscopy analysis [10]. The low-pass filter corner was set at approximately 1 MHz frequency, with R_2 and C_2 circuit elements, while the high-pass filter corner at 100 Hz, with G_{mhp} and C_1 components for its implementation. Special care was given to common-mode rejection ratio derived from possible electrode mismatch, input noise performance and low-power supply consumption. The frequency response, magnitude and phase are illustrated in Fig. 4, for an input voltage of amplitude 10 mV and $\alpha_{ia}=10$. It can be observed how phase response is not constant at the passband, increasing phase errors at the edges. This additive effect can be corrected by calibration. Also, gain is not constant at bandpass edges, which could decrease the closed-loop gain (α_o) and increase the errors at impedance magnitude.

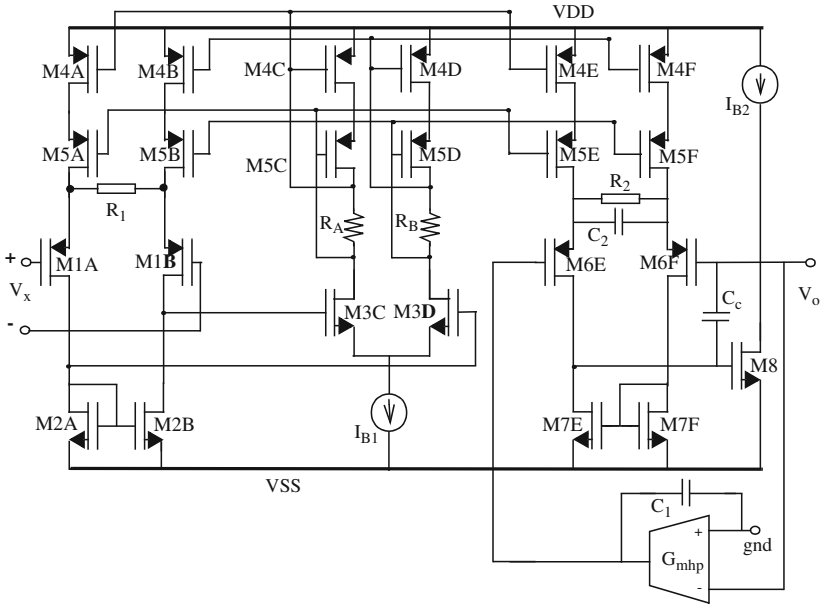
3.2. The rectifier and error amplifier

The full wave rectifier in Fig. 5a was developed by the authors, and it is based on pass transistors (MP, MN) to load the capacitor C_r at the nearest voltage of V_o. The two comparators detect when the input signal is higher (lower) than V_{op} (V_{om}) in each instant, charging then the C_r capacitors to the V_o peak (positive or negative) value. Settling time for comparators must be small for fast voltage input resolution. The discharge of C_r is done by current sources, I_{dis}, and has been set to 1 mV voltage ripple in a time period. Fig. 5b illustrates the waveforms obtained by electrical simulations for the upper and lower rectified signals at 10 kHz, for $C_r=20$ pF, $I_{dis}=200$ pA. In spectroscopy analysis, when frequency changes in a given range, the discharge current should be programmed at each frequency to fulfil the estimated 1 mV voltage ripple in the rectifier output voltage. At the output voltages, V_{om} and V_{op}, a differential-to-single amplifier [14] was added for single rail conversion. Its output, V_{dc}, has a gain α_{dc} respect to rectifier input amplitude, V_o.

To compare the rectifier output voltage V_{dc} with V_{ref}, the difference is amplified, creating the magnitude voltage signal, V_m, which has information on impedance magnitude. A simple two-stage operational amplifier, in open loop configuration, is employed for error amplification [14]. The voltage signal V_{dc} must be as near as possible to V_{ref}.

3.3. The current controlled circuit

For i_x amplitude programming, a four-quadrant multiplier and an OTA were designed. Both are placed in series as shown in Fig. 6.



Transistor sizes (μm/μm) and components

M1A-B	200/2
M2A-B	10/10
M3C-D	100/2
M4A-F	100/1.5
M5A-F	20/1.5
M6E-F	200/2
M7E-F	100/2
M8	66/1
G_{mhp}	200nS
C_1	15.9pF
C_2	1.9pF
R_1	1kΩ
R_2	10kΩ
Cc	5pF
I_{B1}	70μA
I_{B2}	40μA

Fig. 3. CMOS instrumentation amplifier schematic.

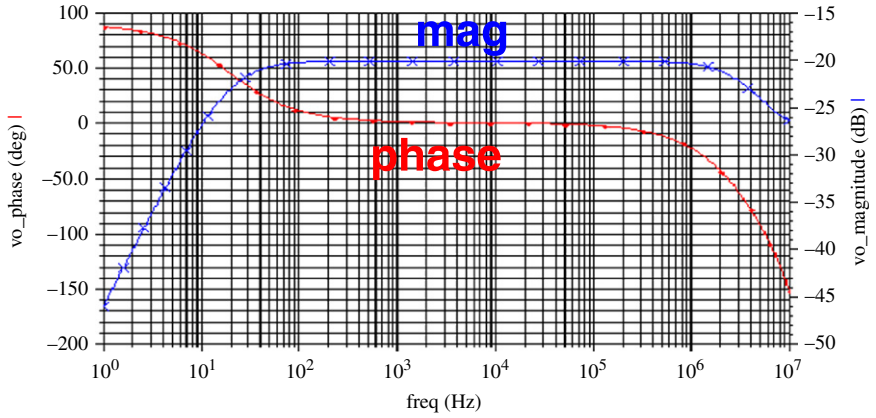


Fig. 4. Instrumentation amplifier magnitude and phase frequency response for 10 mV input amplitude.

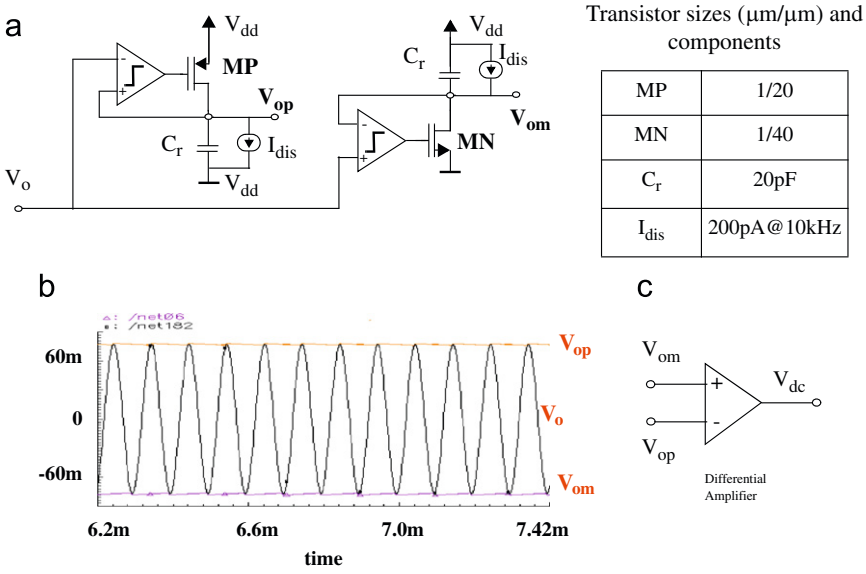


Fig. 5. (a) Full-wave rectifier schematic. (b) Electrical simulations at 10 kHz. V_{op} and V_{om} are the upper and lower rectified signals, respectively. (c) Differential-to-single voltage amplifier.

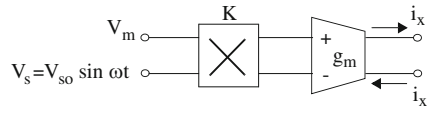


Fig. 6. Blocks of the current controlled circuit: a multiplier in series with an OTA.

The external AC voltage source is first multiplied by the voltage V_m. The result is later converted to AC current for load excitation.

The schematic of the four-quadrant multiplier circuit is shown in Fig. 7 [11]; this was selected because inputs are AC signals, its topology is simple, it has reduced number of transistors and can work at low-voltage low-power conditions. It has two inputs: the external AC voltage generator, V_s, and the voltage magnitude, V_m. The multiplier output waveforms are shown in Fig. 8. In this figure, the AC signal V_s has 200 mV of amplitude at 10 kHz frequency, and it is multiplied by a DC signal, V_m, in the range [0,200 mV]. The differential output is given by

$$V_{out} = V_{out1} - V_{out2} = 2R\sqrt{k_n k_p} V_m V_s = K V_m V_s \quad (4)$$

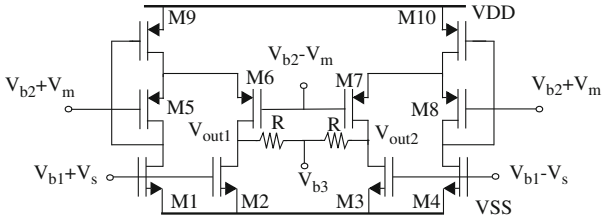
where K is the constant of the multiplier, and k_n and k_p the transconductance parameters for M1 and M6 transistors.

The operational transconductance amplifier employed has the schematic in Fig. 9 [10]. The cascode output stage reduces the load effect due to large ohmic values in loads (Z_{xo}). Typical output resistance for cascode output stages is greater than 100 MΩ, so errors expected due to load resistance effects will be small.

3.4. The comparator

The voltage comparator selected is shown in Fig. 10 [14]. A chain of inverters have been added at its output for fast response and regeneration of digital levels. The comparator is employed both for rectifying the AC signal and squaring the sinusoidal voltage signals for obtaining full range digital signal at the EXOR gate inputs.

From the design data an amplitude is obtained for the voltage V_x of 8 mV over the load Z_x. In electrode-based measurements, V_{xo} has typically low and limited values (tens of mV) to control its expected electrical performance [5]. This condition is preserved by design, thanks to the voltage limitation imposed by the Pstat operation mode, and can be tuned by changing the value of V_{ref} (in our case 20 mV), as it is derived from Eq. (1).



Transistor sizes (μm/μm) and components

M1-M4	2/2
M5-M8	6/2
M9-M10	40/2
R	5kΩ

Fig. 7. Multiplier circuit. V_{b1}, V_{b2} and V_{b3} are bias voltages.

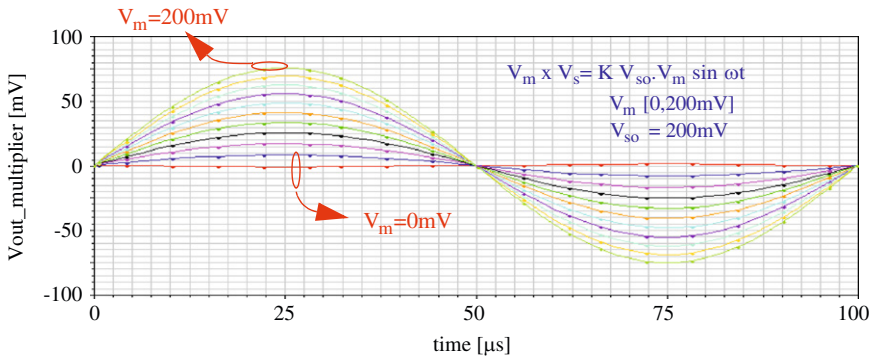
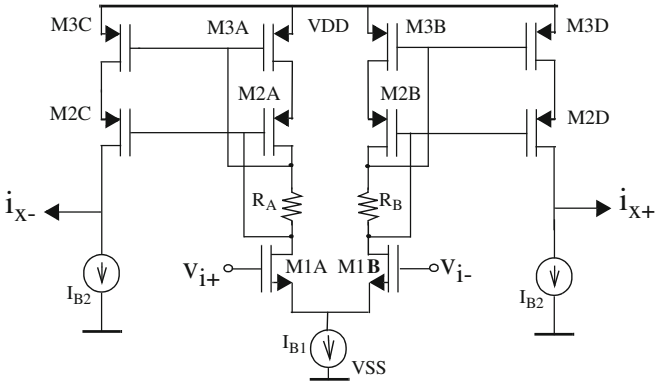


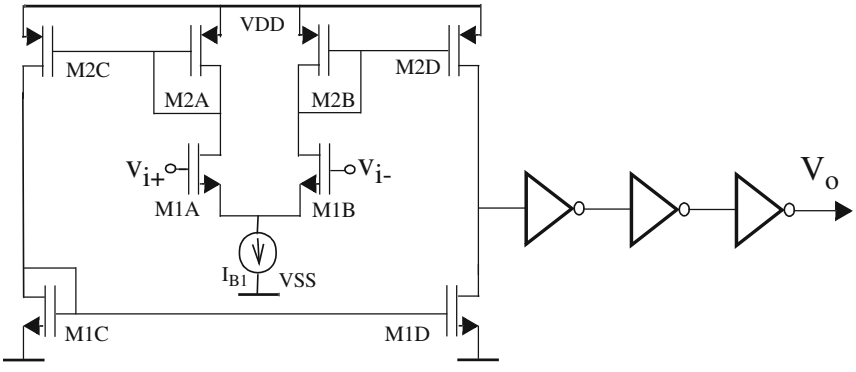
Fig. 8. Simulated multiplier output voltage waveforms.



Transistors sizes (μm/μm) and components

M1A-B	5/5
M2A-D	20/1.5
M3A-D	20/1.5
R_A,R_B	20kΩ
I_{B1}	0.530μA
I_{B2}	0.265μA

Fig. 9. OTA circuit schematic.



Transistor sizes (μm/μm) and components

M1A-B	10/0.5
M2A-D	1/5
M3A-B	1/5
I_{B1}	15μA

Fig. 10. Comparator circuit schematic.

4. System design considerations

Due to the high loop gain for satisfying condition in Eq. (2), it is necessary to study the stability of the system. In steady-state, eventual changes produced at the load can generate variations at the rectifier output voltage, which will be amplified α_{ea} times, leading to out of range for some circuits. To avoid this, some control mechanism should be included in the loop. A first order low-pass filter was selected at the error amplifier output. This LPF in Fig. 11 acts as a delay element, avoiding an excessive fast

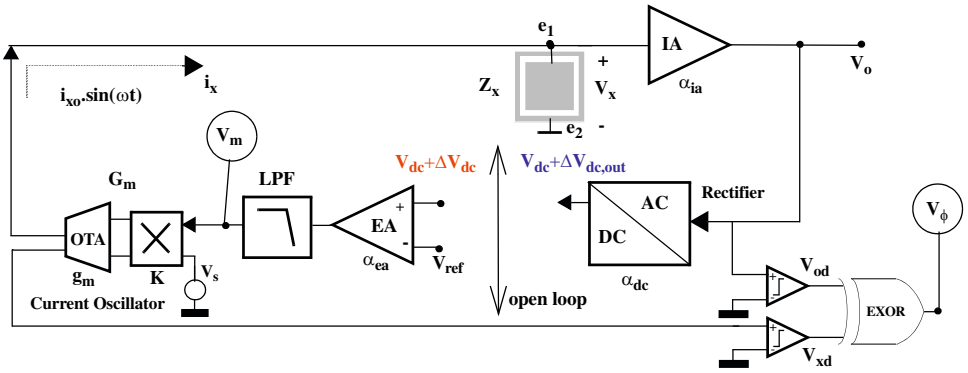


Fig. 11. Open loop system for steady-state stability analysis.

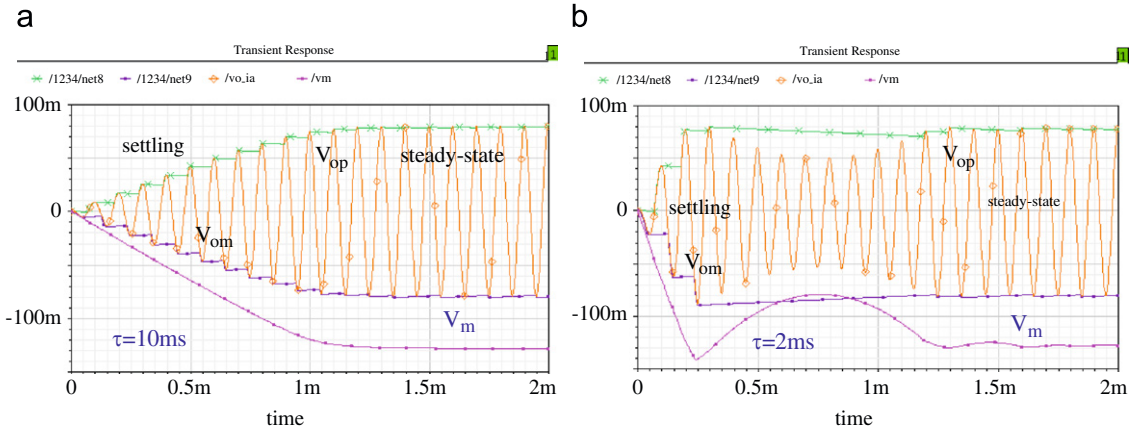


Fig. 12. Start-up transient from $V_m=0$ to its steady-state, for (a) $\tau=10$ ms and (b) $\tau=2$ ms, at $f=10$ kHz.

response in the loop, by setting a dominant pole. For a given ΔV_{dc} voltage increment, in a period of time of the AC signal, the gain of the loop must be below unity. To analyse the response of the loop to a $\Delta V_{dc}(t)$ voltage increment, we cut the loop between the rectifier and error amplifier. The corresponding voltage response will be

$$\Delta V_{dc,out} = Z_{xo} G_m \alpha_{ea} \alpha_{ia} \alpha_{dc} (1-e^{-t/\tau}) \Delta V_{dc} \tag{5}$$

For a gain below unity in a period of time $t=$T, the output voltage increment of the rectified signal must be lesser than the corresponding input voltage changes, $\Delta V_{dc,out} < \Delta V_{dc}$; hence,

$$1 < Z_{xo} G_m \alpha_{ea} \alpha_{ia} \alpha_{dc} (1-e^{-t/\tau}) \tag{6}$$

which means an LPF time constant given by

$$\tau > \frac{T}{\ln\left(\frac{\alpha_o}{\alpha_o - 1}\right)} \tag{7}$$

This condition makes the filter design dependent on ZUT through the parameter Z_{xo}, which should be quoted in order to apply the condition in Eq. (7) properly. For example, if we take $\alpha_o = 100$, for a 10 kHz working frequency, the period is $T=0.1$ ms, and $\tau < 9.94991$ ms. If $\tau = R_F \cdot C_F$ in a discrete first order filter realization, for $C_F=20$ pF, it corresponds to $R_F=500$ MΩ. Preserving by design large α_o values, imposed by Eq. (2), the working frequency will define the values of τ in LPF. For load dependent values on α_o, as the case of living cells on top of electrodes, Eq. (7) should consider the biggest value of α_o for quoting the worst case design. The stability problem is also present at the start-up operation, for each new measure. In this situation, reset is applied to the system by initializing to zero the filter capacitor. Measurement process starts from $V_m=0$, and after several periods of time it is found to achieve steady-state. This is the time required to load the capacitors C_r, at rectifier, up to their steady-state value. This can be observed at the waveforms in Fig. 12, for $\tau=10$ ms and $\tau=2$ ms, where the settling transient at the rectifier envelops are also represented. When signal V_o (IA output) found the value of 80 mV, the loop starts working. In the first case ($\tau=10$ ms), is satisfied condition in Eq. (7). It can be observed how if $\tau=2$ ms, transient to final value is not well controlled. The number of periods required for settling is N_c and the time required to perform a measure is defined as $T.N_c$. The influence of the input noise of the instrumentation amplifier over the output signal (V_m) will be reduced as a consequence of this LP filtering process.

5. Simulation results

A first set of electrical simulations was performed at 10 kHz frequency, using for Z_x resistive (100 kΩ), RC (100 kΩ||159 pF) and capacitive (159 pF) loads. Fig. 13 shows the waveforms obtained using spectre electrical simulator for excitation signals, V_x and i_x, and the resulting signals derived to obtain magnitude, V_m, and phase, V_ϕ. The amplifier output voltage V_o is nearly constant and equal to 80 mV for all loads, fulfilling the Pstat condition ($V_{xo}=V_o/\alpha_{ai}=8$ mV), while i_x has an amplitude adapted to load for each case. The V_m value gives the expected magnitude of Z_{xo} using Eqs. (1) and (3) in all cases, as shown in Table 1. The measure duty cycle allows the calculus of the Z_x phase. The 10 kHz frequency has been selected because the phase shift introduced by the instrumentation amplifier is close to zero, minimizing its influence on phase calculations. This and other deviations from ideal performance derived from process parameters variations

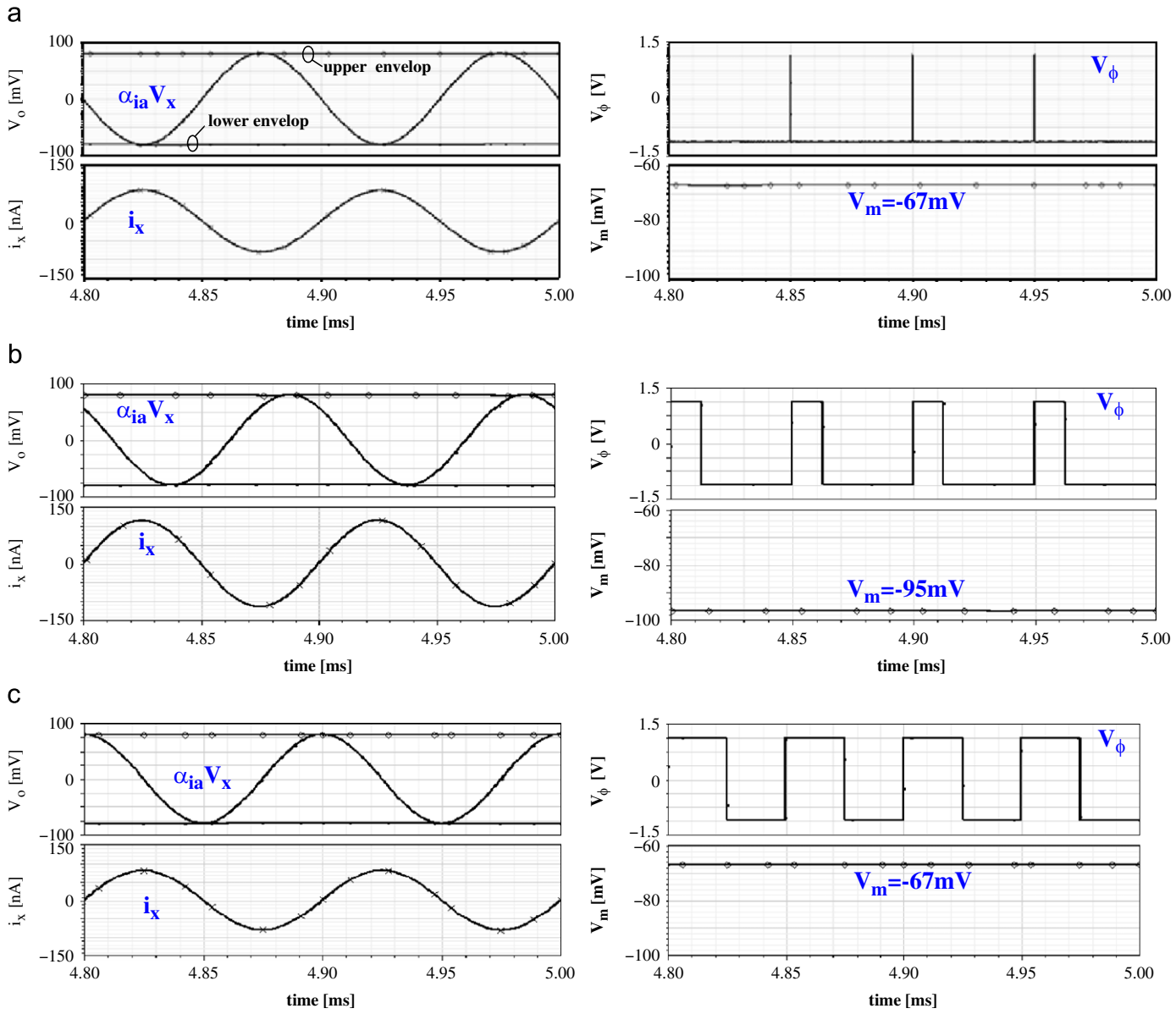


Fig. 13. Waveforms obtained by electrical simulations: V_x and i_x are the voltage and current excitation signals. V_m and V_ϕ are the voltage signals obtained from measurement circuits using (a) R_x=100 kΩ. (b) R_xC_x=(100 kΩ||159 pF) and (c) C_x=159 pF.

Table 1
Simulation results at 10 kHz for several Z_x loads.

Z_x	V_m [mV]	δ	Z_{xo} [kΩ]		ϕ [°]	
	sim	sim	sim	teo	sim	teo
case R	67.15	0.005	99.28	100.0	00.93	0
case RC	94.96	0.247	70.20	70.70	44.44	45
case C	67.20	0.501	99.21	100.0	90.04	90

Table 2
Simulation results for $R_x||C_x$ load. (C_x=15.9 pF, f=100 kHz, ϕ_{IA}(100 kHz)=2.3°, G_m=1.6 µS.

R_x [kΩ]	V_m [mV]	δ [us]	V_{xo} [mV]	Z_{xo} [kΩ]	ϕ [°]
10	491.0	0.24	7.8	9.92	6.34
20	251.2	0.40	7.8	19.43	12.1
50	112.7	0.83	7.9	43.60	27.6
100	69.7	1.34	7.9	70.80	43.9
200	55.2	1.85	7.9	89.53	64.3
500	50.4	2.27	7.9	97.97	79.4
1000	49.7	2.42	7.9	99.35	84.8

should be adjusted by calibration. Errors in both parameters are within the expected range (less than 1%).

Another parallel RC load has been simulated. In this case, the working frequency is 100 kHz, C_x=15.9 pF, and the values of R_x are in the range [10 kΩ, 1 MΩ]. The results are listed in Table 2 and represented in Fig. 14. Excellent agreement was obtained for both magnitude and phase with the theory.

A four-wire system for Z_x measurements is shown in Fig. 15a. This kind of set-up can be useful in electrical impedance tomography (EIT) of a given object [7], decreasing the electrode impedance influence (Z_{e1} to Z_{e4}) on the output voltage (V_o), thanks to the instrumentation amplifier high input impedance. The model used for the electrode in Fig. 15c considers the double layer capacitance (C_p), the charge transfer resistance (R_p) and the spreading resistance (R_s) of an electrode-solution system [5].

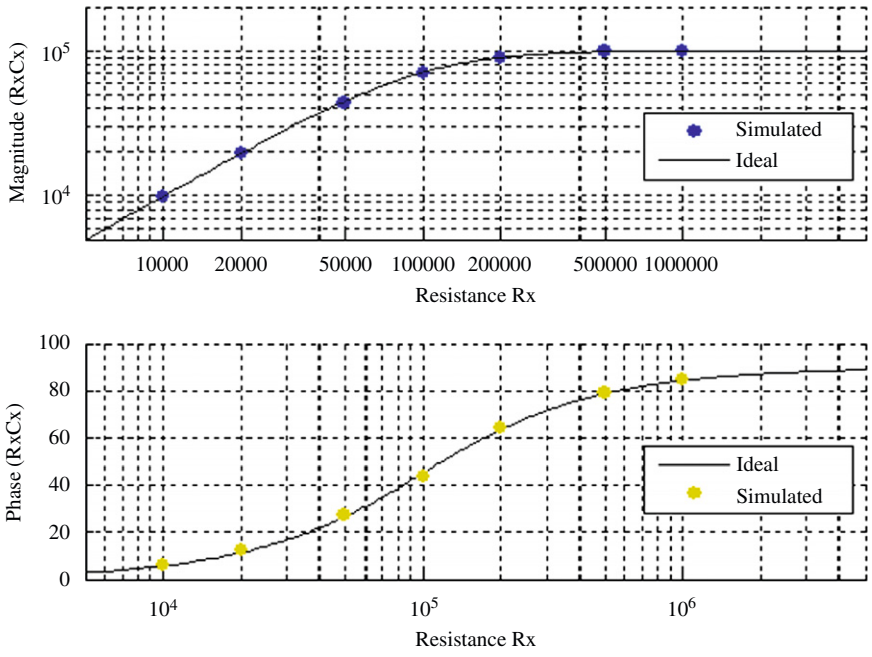


Fig. 14. Magnitude and phase obtained from electrical simulations for $R_x||C_x$ using $C_x=15.9$ pF and R_x belongs to [10 kΩ, 1 MΩ] at $f=100$ kHz.

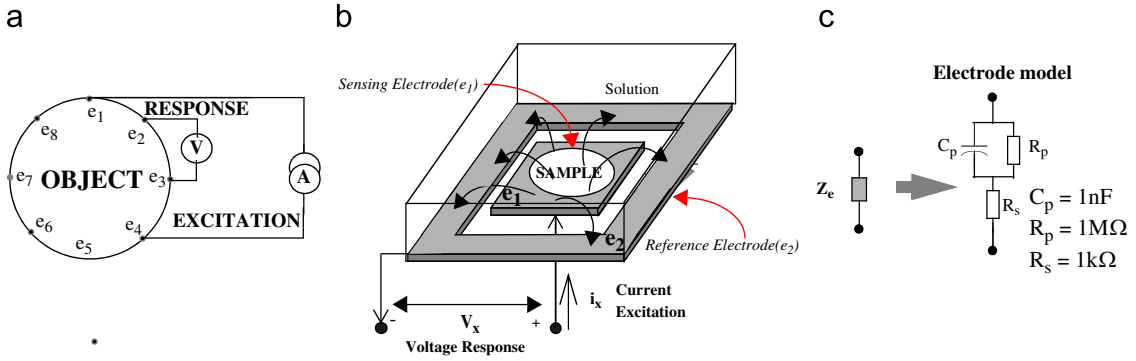


Fig. 15. (a) Eight-electrode configuration for Electrical Impedance Tomography (EIT) of an object. (b) Two-electrode system with a sample on top of electrode 1 (e_1). The equivalent circuit employed uses $R_{SAMPLE}=100$ kΩ. Z_x includes Z_{e1}, Z_{e2} and R_{SAMPLE} resistance. (c) Electrical model for the electrode.

Table 3
Simulation results for four-electrode setup and a load $Z_x=100$ kΩ.

frequency [kHz]	Z_{xo} [kΩ]		ϕ [°]	
	sim	teo	sim	teo
0.1	96.17	92.49	11.70	13.67
1	99.40	100.00	1.22	1.90
10	99.80	100.00	−0.20	−0.12
100	99.70	100.00	−4.10	−3.20
1000	95.60	96.85	−40.60	−32.32

Parameters values have been taken from [3]. Using a 100kΩ load at 10 kHz frequency, the voltage at Z_x load matches the amplitude of $V_{xo}=8$ mV, and the calculus of the impedance value at 10 kHz frequency ($Z_{xo}=99.8$ kΩ and $\phi=0.2°$) is correct. The same load is maintained in a wide range of frequencies (100 Hz to 1 MHz), achieving the magnitude and phase listed in Table 3. The main deviations are present at the amplifier bandpass frequency edges due to lower and upper −3 dB frequency corners. It can be observed the phase response measured and the influence due to amplifier frequency response in Fig. 4. In this case, for spectroscopy analysis, discharge current, I_{dis}, in full wave rectifier has been selected to fulfil 1 mV output voltage ripple. In a similar way, the equivalent transconductance G_m and the time constant at LPF in Fig. 11 should be programmed to each working frequency.

A two-electrode system is employed in Electric Cell substrate Impedance Spectroscopy (ECIS) [6] as a technique capable of obtaining basic information on single or low concentration of cells. The main drawback of two-wire systems is the output signal corresponds to the series of two electrodes and the load, being necessary to extract the load from the measures [12,13]. Fig. 15b shows a two-electrode set-up in which the load or sample (100 kΩ) has been measured in the frequency range of [100 Hz, 1 MHz]. Circuit parameters were adapted to satisfy the $\alpha_o=100$ condition, since Z_{xo} will change from around 1 MΩ to 100 kΩ when passing from tens of Hz to MHz frequencies, due to electrode impedance dependence. The simulation data obtained are shown in Table 4. At 10 kHz frequency, magnitude Z_{xo} becomes 107.16 kΩ, because it includes two electrodes in series. The same effect occurs for phase, now becoming 17.24°. Results are shown in Table 4 for the frequency range considered. The accuracy observed is better at the mid-bandwidth. Again, errors in magnitude and phase increase at the bandpass corners of the instrumentation amplifier.

Table 4
Simulation results for two-electrode setup and a load $Z_x = 100\,k\Omega$.

frequency [kHz]	Z_{xo} [kΩ]		ϕ [°]	
	sim	teo	sim	teo
0.1	1058.8	1087.8	−40.21	−19.00
1	339.35	344.70	−56.00	−62.88
10	107.16	107.33	−17.24	−17.01
100	104.80	102.01	−6.48	−5.09
1000	104.24	102.00	−37.80	−32.24

In both cases, when using electrodes, the equivalent circuit described in [3] was employed for the electrode model. This circuit represents a possible and real electrical performance of electrodes in some cases. In general, the electric model for electrodes will depend on the electrode-to-sample [12,13] and/or medium [5] interfaces and should be adjusted to each test problem. In this work, a real electrical electrode model was used to confirm the adequate performance of the proposed CMOS measurement system.

6. Conclusions

This paper proposes the design of a CMOS system for impedance measurement, useful for sensing biological samples, thanks to the possibility of including the electrode specifications at the design process. The proposed system works using Pstat condition to control the voltage amplitude on the sensing electrodes, and can be designed to work at several frequencies. New feedback circuit implementations for both exciting the load and delivering measure signals are proposed. Input offset and noise amplifier are attenuated, thanks to high-pass and low-pass filter functions, respectively. Design trade-offs for system accuracy and stability have been derived. Electrical simulations prove the correct circuit performance, obtaining magnitude and phase errors below 1% for several frequencies and measurement setups.

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