# Pathological Element-Based Active Device Models and Their Application to Symbolic Analysis

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Abstract—This paper proposes new pathological element-based active device models which can be used in analysis tasks of linear(ized) analog circuits. Nullators and norators along with the Voltage Mirror-Current Mirror (VM-CM) pair (collectively known as pathological elements) are used to model the behavior of active devices in voltage-, current- and mixed-mode, also considering parasitic elements. Since analog circuits are transformed to nullor-based equivalent circuits or VM-CM pairs or as a combination of both, standard nodal analysis can be used to formulate the admittance matrix. We present a formulation method in order to build the Nodal Admittance (NA) matrix of nullor-equivalent circuits, where the order of the matrix is given by the number of nodes minus the number of nullors. Since pathological elements are used to model the behavior of active devices, we introduce a more efficient formulation method in order to compute small-signal characteristics of pathological element-based equivalent circuits, where the order of the NA matrix is given by the number of nodes minus the number of pathological elements. Examples are discussed in order to illustrate the potential of the proposed pathological elementbased active device models and the new formulation method in performing symbolic analysis of analog circuits. The improved formulation method is compared with traditional formulation methods, showing that the NA matrix is more compact and the generation of non-zero coefficients is reduced. As a consequence, the proposed formulation method is the most efficient one reported so far, since the CPU-time and memory consumption is reduced when recursive determinant-expansion techniques are used to solve the NA matrix.

#### I. INTRODUCTION

YMBOLIC analysis is a powerful tool which is used to model the behavior of a circuit in terms of symbolic parameters [1]-[9]. Symbolic expressions not only give better insight on the behavior of the circuit, but can also be used in synthesis and optimization procedures [3], [4], [6], [10]. Traditionally, the behavior of active devices is modeled with voltage- or current-controlled voltage or current sources. Then, symbolic methods, such as: tree enumeration methods, signalflow-graph methods, parameter extraction methods, numerical interpolation methods and determinant expansion methods [2]-[4] are used in order to compute the symbolic expressions.

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Particularly, matrix-based formulation methods such as: nodal analysis, Modified Nodal Analysis (MNA) or tableau analysis, use the element stamp procedure to fill the admittance matrix. However, for the case of nodal analysis, only compatible elements can be introduced. This disadvantage has been overcome by the MNA technique, in which additional columns and rows are incorporated into the admittance matrix and the non-compatible elements are readily included by using a stamp [2]-[4]. However, not only the size of the admittance matrix increases with the inclusion of controlled sources, since it depends on the number of node voltages and on the branch currents associated to the type of elements contained in the circuit, but the number of non-zero coefficients into this matrix is also increased. As a consequence, the CPU-time and memory consumption used to solve the system of equations increases [4], [8].

Let Y be a square matrix given by

$$Y = \begin{pmatrix} Y_{1,1} & \cdots & Y_{1,j} & \cdots & Y_{1,q} \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ Y_{i,1} & \cdots & Y_{i,j} & \cdots & Y_{i,q} \\ \vdots & \ddots & \vdots & \ddots & \vdots \\ Y_{q,1} & \cdots & Y_{q,j} & \cdots & Y_{q,q} \end{pmatrix}$$
(1)

The determinant of (1) can be obtained by applying Laplace expansion as

$$|Y| = \sum_{i=1}^{q} Y_{i,j} (-1)^{i+j} |Y_{Y_{i,j}}|$$
 (2)

$$|Y| = \sum_{i=1}^{q} Y_{i,j} (-1)^{i+j} |Y_{Y_{i,j}}|$$
 (3)

where  $Y_{i,j}$  is a non-zero coefficient of the matrix Y in the most sparse row i or column j, and  $|Y_{Y_{i,j}}|$  is the minor with respect to  $Y_{i,j}$ , which is also a determinant and can be computed using the same rules. From (1), (2) and (3) it can be inferred that for a full matrix, the computational complexity of the symbolic calculation of the determinant of (1), is O(q!) [11], where q is the rank of the matrix. This cost can be significantly reduced, e.g. by exploiting matrix sparsity, that is directly given by the number of non-zero coefficients. Therefore, the complexity of the solution algorithm depends on the size of the matrix and of the number of non-zero coefficients. On the other hand, the determinant of (1) can also be obtained by applying

$$|Y| = Y_{i,j}(-1)^{i+j}|Y_{Y_{i,j}}| + |Y_{\overline{Y}_{i,j}}|$$
(4)

where  $|Y_{\overline{Y}_{i,i}}|$  is a matrix obtained from (1) by setting  $Y_{i,j} = 0$ . Note that (2) and (3) are special cases of (4). Based on (4), the determinant of (1) can be represented with compact graphs by using the Determinant Decision Diagrams (DDDs) concept [12]-[14]. Each non-zero coefficient of the matrix is considered as one distinct symbol and each of them is represented into DDDs as one non-terminal vertex. Because DDDs are based in the manipulation of non-zero coefficients in order to expand the determinant of (1), the complexity to compute the determinant of a full matrix with an optimal order of the non-zero coefficients is given by  $O(q \cdot 2^{q-1})$  [11]. But even if modern simplification during generation techniques, that only calculate the dominant part of the symbolic solution, are going to be applied to the solution of (1), the computational complexity of best algorithms still grow exponentially with matrix size and the number of non-zero coefficients [15], [16]. Therefore, the CPU time and memory consumption of modern symbolic analysis algorithms is dramatically improved by applying formulation techniques of network equations yielding small and sparse matrices.

Regarding formulation methods, new stamps associated to the four types of controlled sources as well as for the nullors, op-amps, transistors and impedance converters, have been proposed in [17], [18]. Unlike the classical stamps which are deduced directly from the behavior of the active devices by using Kirchhoff's current law [2], [4], the new stamps have been obtained by using the concept of matrix port-equivalence and limit-variables [17], [18]. However, although controlled sources can directly be used into the nodal analysis method, infinity-limits can only be applied once fully-symbolic smallsignal characteristics of analog circuits are computed [19]. Therefore, valuable computer resources will be wasted in generating symbolic terms that will be pruned when the limits are applied on the symbolic analysis results. Other limitations of this method are: the size of the Nodal Admittance (NA) matrix depends on the number of nodes as independent variables. the number of non-zero coefficients into the NA matrix is increased and as a consequence, the solution of the system of equations is more complex.

On the other hand, since its introduction in 1964 by Carlin [20], the nullor has proven its usefulness in the areas of modeling, synthesis and analysis of analog circuits in several levels of abstraction [21]-[28]. Despite some active devices can be ideally modeled with the nullor, still other elements, like resistors, must be added to the equivalent circuit to adequately model the behavior of some active devices, such as: the normal and inverting second generation current conveyors (CCII± and ICCII±) with single or multiple outputs [29], [30]. As a consequence, the number of non-zero coefficients into the equivalent NA matrix is increased. More recently, the Voltage Mirror-Current Mirror (VM-CM) pair has been shown to be useful to ideally model active devices with voltage and current reversing properties, without requiring additional resistors [31]-[36]. The VM-CM pair has also a NA matrix stamp which has been obtained by using the limit-variable method [33], [34]. However, only the modeling of active devices with unity-gain has been introduced and although the VM-CM pair has mainly been used to synthesize

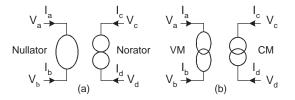


Fig. 1. Pathological elements: (a) Nullator and norator, (b) Voltage and current-mirrors

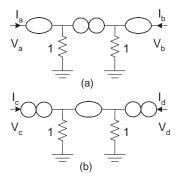


Fig. 2. Nullor-based (a) VM and (b) CM equivalents

analog circuits, it exhibits some drawbacks when it is used for symbolic analysis purposes. The major drawback is that the stamp of the VM-CM pair introduces the transconductance gain  $G_m$  into the NA matrix and it must be taken as a limit to infinity once symbolic expressions are computed. Besides this, the parasitic elements of the synthesized active devices are not considered [32]-[36]. Therefore, in order to compute fully-symbolic expressions of pathological element-based equivalent analog circuits, the nullor properties along with the VM-CM pair properties, should be taken into account in the formulation process.

In this paper, the modeling of linear active devices by using nullators, norators, VM-CM pairs or as a combination of them, is introduced. Moreover, parasitic elements associated to active devices are also considered inside the proposed models. Furthermore, because pathological elements are used to model the behavior of active devices, a new method to formulate the NA matrix is also introduced. Experimental results demonstrate that the proposed models together with the formulation method, offer a significant improvement over previous approaches reported so far [1]-[9], [17]-[19], [24]-[38]. We also observe that the NA matrix is more compact, the generation of cancellation-terms is reduced, and if DDDs are used to solve the system of equations, only few non-terminal vertices are required, reducing the CPU-time and memory consumption during the solution of the NA matrix [8]-[14].

#### II. NULLOR AND VM-CM CONCEPTS

The nullor is an ideal element which is composed of a nullator (*O*), connected in the input-port and a norator (*P*), connected in the output-port, as shown in Fig. 1a [20], [25]. The nullator does not allow current to flow through it, and the voltage across its terminals is zero

$$V_b = V_a = arbitrary, \quad I_b = I_a = 0$$
 (5)

For the norator, an arbitrary voltage can exist across its terminals and an arbitrary current can flow through it

$$V_d \neq V_c = arbitrary, \quad I_d = -I_c = arbitrary \quad (6)$$

The nullator and norator form the nullor, which can also be implemented with inverting characteristics by using the VM-CM pair. Its symbol is shown in Fig. 1b [31], [32], [34]. This pair is also an ideal element and it is composed of a VM at the input port and a CM at the output port. The VM imposes two constraints on its voltage and current, given by

$$V_b = -V_a = arbitrary, \quad I_b = I_a = 0$$
 (7)

The CM also imposes two constraints, given by

$$V_d \neq V_c = arbitrary, \quad I_d = I_c = arbitrary$$
 (8)

To efficiently model the behavior of active devices, the VM and the CM will be used as two-terminal elements, as shown in Fig. 1b, which are also known as grounded mirror elements [32]-[36]. The ideal behavior of the VM and CM can be modeled with nullators, norators and resistors, as shown in Fig. 2 [30], [31], and the two constraints associated with VMs and CMs can easily be obtained by analyzing these equivalent circuits. Further, if any terminal of the VM or CM is connected to ground, it is equivalent to a nullator or norator element, respectively.

To perform symbolic analysis of analog circuits, the behavior of the active devices can be modeled with pathological elements. Then, a formulation method along with a solution method are executed, where the nullator, norator, VM and CM properties are taken into account [37], [38]. Suppose that an electronic network with q nodes, is composed by passive elements and p pathological elements, as shown in Fig. 3a. The system of equations of the pathological element-equivalent network is obtained by applying a standard nodal analysis and given by (1). To reduce the size of the NA matrix, (5), (6), (7) and (8) must be applied. For this reduction process, we have two cases that are discussed as follows.

#### A. Nullator and norator trees

According to (5), the voltage level in the two nodes of a nullator is the same. Since each node of a nullator represents one column into the NA matrix, all the coefficients from the two columns should be added, yielding a single column. This process is generalized for the case of nullator trees, as shown in Fig. 3b. Therefore, all the coefficients  $Y_{i,j}$  of (1) associated with the set of nodes of a nullator tree,  $m = \{j, a, b, ...c\}$ , must be added as

$$Y_{i,min\{m\}} = \sum Y_{i,m}, \quad \forall i = 1...q$$
 (9)

where  $Y_{i,min\{m\}}$  is the new coefficient of the reduced matrix in the *i*-th row. Besides, if any node of a nullator is grounded, the column of the NA matrix which is associated with the ungrounded node of the nullator must be deleted. As a consequence, (1) is reduced to (10)

$$Y_{q\times(q-p)} = \begin{pmatrix} Y_{1,1} & \cdots & Y_{1,q-p} \\ \vdots & \ddots & \vdots \\ Y_{q,1} & \cdots & Y_{q,q-p} \end{pmatrix}$$
(10)

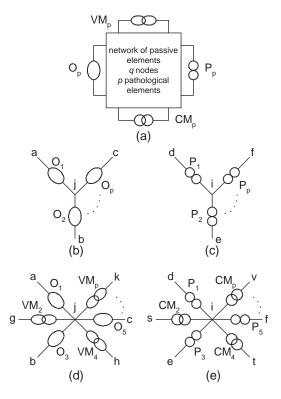


Fig. 3. (a) Analog network (b) Nullator tree, (c) Norator tree, (d) Nullator-VM tree. (e) Norator-CM tree

For the case of a norator element, it is also connected between two nodes and each node represents one row in the NA matrix. According to (6) and because the current that flows from one node to another through a norator is the same, all the coefficients from the two rows in the NA matrix must be added to obtain a single row. This process is also generalized for the case of norator trees, as shown in Fig. 3c. Thus, all the coefficients  $Y_{i,j}$  of (10) associated with the set of nodes of a norator tree,  $n = \{i, d, e, ... f\}$ , must be added as

$$Y_{min\{n\},j} = \sum Y_{n,j}, \quad \forall j = 1...(q-p)$$
 (11)

where  $Y_{min\{n\},j}$  is the coefficient of the reduced matrix in the *j*-th column. Otherwise, if any terminal of a norator is connected to ground, the row of the NA matrix which is represented by the other node of the norator must be deleted [24], [37], [38]. Hence, when the NA matrix is built from nullor-equivalent circuits, the order of the system of equations is given by  $(q - p) \times (q - p)$ .

#### B. Nullator-VM and norator-CM trees

In the general case when nullors and VM-CM pairs are used to model the behavior of active devices, the formulation method should take into account the inverting properties of the VM-CM pair. Similar to the nullator, the nodes of a VM are related to the columns of the admittance matrix, but with opposite characteristics. According to (7), two columns in the NA matrix should be subtracted in order to obtain a single column. This reduction process can also be generalized by considering nullator-VM trees, as shown in Fig. 3d. In this

way, all the coefficients  $Y_{i,j}$  of (1) associated with the set of nodes of a nullator-VM tree,  $m = \{j, a, b, ...c\}$  and  $r = \{g, h, ...k\}$ , must be added as

$$Y_{i,min\{m,r\}} = \sum Y_{i,m} - \sum Y_{i,r}, \quad \forall i = 1...q$$
 (12)

where  $Y_{i,min\{m,r\}}$  is the new coefficient of the reduced matrix in the i-th row. As a result, (1) is reduced to (10). Similar to the norator, the nodes of a CM are related to the rows of the admittance matrix, but with opposite characteristics. According to (8), two rows in the NA matrix should be subtracted in order to obtain a single row. Again, this reduction process can also be generalized by considering norator-VM trees, as shown in Fig. 3e. Therefore, all the coefficients  $Y_{i,j}$  of (10) associated with the set of nodes of a norator-VM tree given as  $n = \{i, d, e, ... f\}$  and  $w = \{s, t, ... v\}$ , must be added as

$$Y_{min\{n,w\},j} = \sum Y_{n,j} - \sum Y_{w,j}, \quad \forall j = 1...(q-p)$$
 (13)

where  $Y_{min\{n,w\},j}$  is the coefficient of the reduced matrix in the j-th column. As a consequence, when the NA matrix is built from pathological element-based equivalent circuits, the order of the system of equations is given by  $(q-p) \times (q-p)$ . However, although (9), (11), (12) and (13) can be used to obtain the NA matrix of pathological element-based circuits, valuable computer resources are still wasted in the generation of (1) and later on (10). An improved formulation method of pathological element-based equivalent circuits will be presented in Section V.

To reduce the number of non-zero coefficients in the equivalent NA matrix, the behavior of an active device should be modeled with pathological elements as simple as possible, avoiding the use of floating resistors. This is because a grounded resistor has only one entry in the NA matrix, whereas a floating resistor has four entries. Further, from (9), (11), (12) and (13) one can see that the coefficients of (1) are always added or subtracted during the reduction process in order to obtain the new coefficients. As a consequence, the number of non-zero coefficients of the equivalent NA matrix is usually smaller than the number of non-zero coefficients generated by other formulation methods, like the MNA method.

# III. PATHOLOGICAL ELEMENT-BASED ACTIVE DEVICE MODELING

According to the voltage-current relationships of the nullor, a nullator can model a node with high-impedance, if it is floating, or a node with low-impedance, if any terminal of the nullator is grounded [27], [28]. For the norator, it can model both impedance levels: high or low, depending of the signal to be measured. Thus, by considering the impedance characteristics along with the gain-equations of operational amplifiers, and by applying the nullor properties, several active devices can adequately be modeled with the nullor, as shown in Fig. 4. Some of these active device models are well known [39]-[44], but the nullor-based models of the OTRA, COA, FOTRA, CFB-OTA and OFC are reported herein for the first time in the literature. As an example, the nullor-based model of the OFC is derived as follows; the OFC is a hybrid

amplifier which can process voltage and current signals at its input and output ports. According to the gain equation in the input port, the voltage in the positive terminal is equal to the voltage in the negative terminal. Also, since a voltage signal is applied in the positive terminal of the OFC, its input impedance must be ideally infinity. Thus, by using the nullator properties, the input port of the OFC can be modeled with a floating nullator, as shown in Fig. 4. For the output port, both terminals are processing current signals and therefore, they must have ideally an infinity impedance level. Again, by considering the gain equation, the impedance levels of the output terminals and the norator properties, the output port of the OFC can adequately be modeled with a floating norator. Furthermore, the OFC is basically a transresistance amplifier with low and high impedance levels, respectively. Since, the negative terminal in the input port of the OFC can only process current signals, its behavior is better modeled by using a floating norator. Afterwards, this current signal is transformed to voltage by using a grounded resistor, which models the transresistance gain of the OFC. Finally, by applying the nullator properties, the voltage signal is obtained in the Wterminal of the OFC. In the same manner, positive/negativetype first-, second- and third-generation inverting and noninverting current conveyors with a single or multiple outputs can also be modeled with the nullor [22], [29], [39]. Therefore, standard nodal analysis can be applied in order to compute fully-symbolic expressions of analog circuits [37], [38].

The VM-CM pair, recently introduced as an universal active element [34], can be used to reduce the number of circuitelements in the nullor-based operational amplifier models shown in Fig. 4. For instance, we can identify the nullorbased model of the CM shown in Fig 2b, in several amplifiers of Fig. 4, which are surround with a dashed line. Therefore, by substituting the equivalent model from Fig. 2b in Fig. 4, some operational amplifier models can be compacted, as shown in Fig. 5. In an analogous manner, some types of current conveyor models introduced in [29] can be improved, as shown in Fig. 6. The grounded resistors in Figs. 4, 5 and 6 model the gain of the operational amplifiers and along with nullators, norators, VMs or CMs, they are also used to transform current to voltage or vice-versa. Further, parasitic resistors and capacitors can easily be included in the inputoutput terminals of Figs. 4, 5 and 6. For instance, a CFOA is characterized by  $R_x$  in the x-terminal,  $R_y$  and  $C_y$  in the y-terminal,  $R_z$  and  $C_z$  in the z-terminal (here,  $R_m$  is the parallel of  $R_z$  and  $C_z$ ). Therefore, a more realistic model can be built, as shown in Fig. 7. Note, however, that although floating pathological element-based active device models have been introduced [32], [36], they can not be used without the limit-variables, whose negative impact for symbolic analysis has been discussed above and will be illustrated in Section V.

# IV. FORMULATION METHOD FOR NULLOR-BASED EQUIVALENT CIRCUITS

The behavior of active devices can be modeled with grounded resistors, nullators and norators, as shown in Fig. 4, and by substituting the VMs and CMs in Figs. 5 and 6 by

Active Device	Gain Equation	Nullor-based Model	Name
V-• + V <sub>out</sub>	$V_{out} = A_v(V^+ - V^-)$	V <sup>+</sup> • V <sub>out</sub>	Operational Amplifier ( <b>Opamp</b> )
V-•	$I_{out} = g_m(V^+-V^-)$	V+	Operational Transconductance Amplifier (OTA)
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	$V_{w} = A_{v}(V^{+}-V^{-})$ $I_{z} = -I_{w}$	V <sup>+</sup> •	Operational Floating Amplifier ( <b>OFA</b> )
$I_{p} \longrightarrow \begin{matrix} + & V_{out} \\ I_{n} \longrightarrow \end{matrix}$	$V_{out} = R_m (I_p - I_n)$	$\begin{array}{c c} & & & \\ & & & \\ I_p & & & \\ & & & \\ I_n & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & \\ & & & \\ & &$	Operational Transresistance Amplifier ( <b>OTRA</b> )
$I_{p} \longrightarrow \begin{matrix} + \\ - \end{matrix}$	$I_{out} = \frac{g_2}{g_1} \left( I_p - I_n \right)$	$\begin{array}{c c} & & & \\ \hline \end{array}$	Current Operational Amplifier (COA)
$I_{p} \longrightarrow \begin{array}{c} + & z \\ \downarrow^{I_{z}} V_{z} \\ \downarrow^{I_{m}} V_{w} \end{array}$	$V_{w}=R_{m}(I_{p}-I_{n})$ $I_{z}=-I_{w}$	$\begin{bmatrix} I_p & & & & \\ I_p & & & & \\ I_n & & & & \\ & & & & \\ & & & & \\ & & & & $	Floating OTRA (FOTRA)
V-	$V_{out}=-R_{m}I_{a}$ $V^{+}=V^{-}$	V+• Rm Vw	Current Feedback Operational Amplifier (CFOA)
V <sup>+</sup>	$I_{out} = \frac{g_2}{g_1} I_a$ $V^+ = V^-$	$\begin{array}{c} V^{+} \bullet \\ \\ V \\ \downarrow \\ a \\ g_{1} \underbrace{\S}_{\underline{\underline{\underline{\underline{\underline{\underline{\underline{\underline{\underline{\underline{\underline{\underline{\underline{\underline{\underline{\underline{\underline{\underline$	Current Feedback OTA (CFB OTA)
$V^{+} \longleftarrow + \qquad z \longleftarrow V_{z}$ $V^{-} \stackrel{I_{a}}{\longrightarrow} - \qquad w \longleftarrow V_{w}$	$V_w = R_m I_a$ $V^+ = V^ I_z = -I_w$	V+	Operational Floating Conveyor ( <b>OFC</b> )

Fig. 4. Nullor-based operational amplifiers

$$\begin{array}{c} I_{p} \longrightarrow \\ OTRA \\ I_{n} \longrightarrow \\ \end{array}$$

$$\begin{array}{c} I_{p} \longrightarrow \\ \\ I_{p} \longrightarrow \\ \end{array}$$

$$\begin{array}{c} I_{p} \longrightarrow \\ \\ \end{array}$$

$$\begin{array}{c} I_{p} \longrightarrow \\ \end{array}$$

Fig. 5. Pathological element-based operational amplifier models

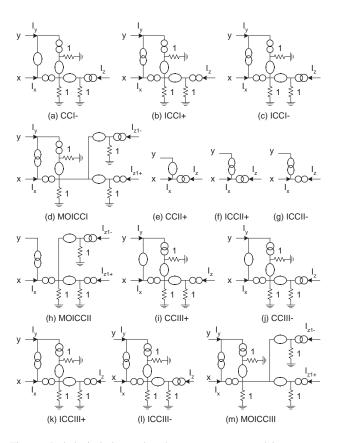


Fig. 6. Pathological element-based current conveyor models

Fig. 7. Pathological element-based CFOA model including parasitic elements

their nullor-based models shown in Fig. 2. As a consequence, a fully connected nullor-equivalent circuit is obtained. It follows that before computing symbolic small signal characteristics, a formulation method must be applied to obtain the system of equations given by

$$J = YV \tag{14}$$

where J is the current vector, Y is the NA matrix and V represents the vector of nodal voltages. The proposed formulation method along with a detailed application example are described in the next subsections.

# A. Generation of tables for nullators, norators, independent current sources and admittances

- 1) Replace each active device by its nullor-based model.
- Group and store nullators, norators, independent current sources and admittances in tables, including their symbols and nodes.
- From the nullor-equivalent circuit, obtain a set of nodes ordered in ascending form (0 is assigned to the reference node).

$$SetNode = \{q_1, q_2, ... q_i\}$$

### B. Computing norator and nullator indexes

The nodes of the nullators and norators must be manipulated to generate two vectors, namely: P (norator vector) and O (nullator vector). These vectors have the indexes associated to the column and row variables of the NA matrix. The procedure to compute the indexes is done as follows

- 1) Group each pair of nodes of a norator and nullator as a set and store it in the vector *P* or vector *O*, respectively.
- 2) Compare the nodes of each set with every set of nodes into the same vector (*P* or *O*). If a node is duplicated in two sets, they must be joined into a single set and ordered in ascending form.
- 3) Compare each node  $q_i$  of *SetNode* with every set of nodes of the vector P (alternatively O).
  - If a node of *SetNode* matches the first node of any set of nodes of the vector *P* (alternatively *O*), the set of nodes must be reordered according to the position of the node in *SetNode*.
  - If a node q<sub>i</sub> of SetNode does not match with the nodes of any set of nodes of the vector P (alternatively O), q<sub>i</sub> must be included into the vector P (alternatively O) and placed in the same position as in SetNode.

4) Delete the set of nodes of the vector *P* (alternatively *O*), if the reference node is one of its nodes.

The final vectors are given as

$$O = [O_1, O_2, ...O_i], P = [P_1, P_2, ...P_i]$$

where  $O_j = \{a_1, a_2...a_x\}$  along with  $P_i = \{b_1, b_2...b_x\}$  are the sets of nodes, and  $a_x$  along with  $b_x$  are the nodes of the sets.

### C. Construction of the NA matrix

Manipulating the indexes of the admittances and the vectors *O* and *P*, the NA matrix is done as follows

- 1) Compare the nodes of every set of nodes of the vector *O* with the pair of nodes of the admittances.
  - If node  $a_x$  of a set  $O_j$  matches with any node of some floating admittances, include the nodes along with the names of the admittances into a list called  $Col_{\{Oj\}} = [\{a_x, [k, ad_1], ...[k, ad_n]\}]$ , where  $ad_n$  is the name of the n-th admittance and k is the nonmatching node of  $ad_n$ .
  - If node  $a_x$  matches the node of some grounded admittances, include the node  $a_x$  and the admittance names as  $Col_{\{Oj\}} = [\{a_x, ad_1, ...ad_n\}].$
- 2) Compare each node  $b_x$  of every set  $P_i$  with the nodes of each set of the list  $Col_{\{Oj\}}$ , in order to generate each coefficient  $Y_{i,j}$  of the NA matrix
  - If  $b_x = a_x$ , all the admittances in the set of  $Col_{\{Oj\}}$  are added in  $Y_{i,j}$  with positive sign.
  - If b<sub>x</sub> = k, only the admittance connected to the k
    node is added in Y<sub>i,j</sub> with negative sign.

#### D. Generation of the vectors V and J

Each node of the sets in vector *O*, represents a nodal voltage. Therefore, the voltage vector is obtained as

$$V = [V_{O1}, V_{O2}, ... V_{Oj}]^T$$
(15)

Each set in vector P, represents an entry of a current source

$$J = [P_1, P_2, ... P_i]^T (16)$$

To fill (16), each node of  $P_i$  must be compared with the nodes (k, l) of a current source.

- If  $b_i = k$ , add the current source with negative sign in (16), according to the position of  $P_i$  in the vector P.
- If  $b_i = l$ , add the current source with positive sign in (16), according to the position of  $P_i$  in the vector P.

Hence, for any analog circuit modeled with nullor elements, the equivalent circuit has q nodes and p nullor elements, thus, the size of the admittance matrix is equal to  $(q-p) \times (q-p)$ .

#### E. NA matrix formulation using nullor-based models

To illustrate the NA matrix formulation using nullor-based models, let us consider the symbolic analysis of the ICCII+based inverting low-pass filter shown in Fig. 8a [45]. If the nullor-based VM and CM models shown in Fig. 2 are used in the ICCII+ model in Fig. 6f, then a nullor-equivalent circuit

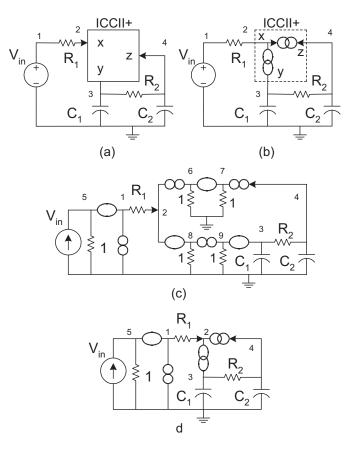


Fig. 8. (a) Inverting low-pass filter, the output is the node 3 (b) Stamp model (c) Nullor-based model (d) Pathological element-based model

0	Node	P	Node	Adm.	Node	Current	Node
						sources	
$O_1$	1,5	$P_1$	1,0	1	5,0	$V_{in}$	0,5
$O_2$	2,8	$P_2$	2,6	$g_1$	1,2		
$O_3$	3,9	$P_3$	4,7	1	6,0		
$O_4$	6,7	$P_4$	8,9	1	7,0		
				1	8,0		
				1	9,0		
				$C_1$	3,0		
				$C_2$	4,0		
				$q_2$	3,4		

for Fig. 8a is generated, as shown in Fig. 8c. Following the proposed formulation method described above, the set of nodes is given by

$$SetNodes = \{1, 2, 3, 4, 5, 6, 7, 8, 9\}$$
 (17)

The nullators, norators, admittances and independent current sources are stored as two-terminal elements in Table I. The nodes of the nullators and norators are grouped and stored in the vectors O and P, respectively

$$O = [\{6,7\}, \{2,8\}, \{3,9\}, \{1,5\}]$$

$$(18)$$

$$P = [\{4,7\}, \{1,0\}, \{8,9\}, \{2,6\}]$$
 (19)

Each node in (17) is compared with all the nodes of the set of nodes in (18) and (19). In this way, the sets are ordered in

ascending form and the nodes of (17) which are not considered in the vectors O and P are readily included

$$O = [\{1, 5\}, \{2, 8\}, \{3, 9\}, \{4\}, \{6, 7\}]$$
 (20)

$$P = [\{1,0\}, \{2,6\}, \{3\}, \{4,7\}, \{5\}, \{8,9\}]$$
 (21)

Because the reference node is included in the first set of nodes in (21), this set must be removed. Thus, the final vectors are obtained as

$$O = [\{1, 5\}, \{2, 8\}, \{3, 9\}, \{4\}, \{6, 7\}]$$
 (22)

$$P = [\{2,6\}, \{3\}, \{4,7\}, \{5\}, \{8,9\}]$$
 (23)

According to the Step 1 from subsection IV-C, the lists  $Col_{\{Oj\}}$  are obtained by manipulating the admittances along with their nodes given in Table I and the indexes of (22), which are given as

$$Col_{\{O_1\}} = [\{\mathbf{1}, [2, g_1]\}, \{\mathbf{5}, 1\}]$$

$$Col_{\{O_2\}} = [\{\mathbf{2}, [1, g_1]\}, \{\mathbf{8}, 1\}]$$

$$Col_{\{O_3\}} = [\{\mathbf{3}, [4, g_2], C_1\}, \{\mathbf{9}, 1\}]$$

$$Col_{\{O_4\}} = [\{\mathbf{4}, [3, g_2], C_2\}]$$

$$Col_{\{O_5\}} = [\{\mathbf{6}, 1\}, \{\mathbf{7}, 1\}]$$

$$(24)$$

In order to generate all the coefficients  $Y_{i,j}$  of the NA matrix, the nodes  $b_i$  of (23) must be compared with the nodes of (24). For instance, to obtain the element  $Y_{3,4}$ , each node of the third set in (23) should be compared with each node of  $Col_{\{O_4\}}$ , thus,  $Y_{3,4}=g_2+sC_2$ . On the other hand, the vector V is obtained from (22) and given by

$$V = [V_{1,5}, V_{2,8}, V_{3,9}, V_4, V_{6,7}]^T$$
 (25)

Finally, the vector J is obtained by comparing each node of (23) with the node pair of the independent current source shown in Table I and given by

$$J = [0, 0, 0, V_{in}, 0]^T (26)$$

Thus, the system of equations becomes

$$\begin{bmatrix} 0 \\ 0 \\ 0 \\ V_{in} \\ 0 \end{bmatrix} = \begin{bmatrix} -g_1 & g_1 & 0 & 0 & 1 \\ 0 & 0 & g_2 + sC_1 & -g_2 & 0 \\ 0 & 0 & -g_2 & g_2 + sC_2 & 1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{1,5} \\ V_{2,8} \\ V_{3,9} \\ V_4 \\ V_{6,7} \end{bmatrix}$$

The output voltage is taken at  $V_{3,9}$  and is given by

$$H(s) = -\frac{1}{C_1 C_2 R_1 R_2 s^2 + (C_1 + C_2) R_1 s + 1}$$
 (28)

V. EXTENDED FORMULATION METHOD FOR PATHOLOGICAL ELEMENT-BASED EQUIVALENT CIRCUITS

Pathological element-based active device models have been shown in Section II. Thus, according to the pathological element-equivalent circuits, the NA matrix can be formulated. A. NA matrix formulation by applying limit variables

To illustrate the evolution towards a more efficient NA matrix formulation method for symbolic analysis purposes, let us consider again the analysis of the ICCII+-based inverting low-pass filter in Fig. 8a [45], by using the limit variables method [33], [34]. For this case, the VM-CM-based ICCII+ model from Fig. 6f is used in Fig. 8a, as shown in Fig. 8b. The stamp of the VM-CM pair shown in Fig. 1b [33], is given as

$$\begin{array}{ccc}
 a & b \\
 c & G_m & G_m \\
 d & G_m & G_m
\end{array}$$
(29)

where  $G_m$  is the transconductance gain of the VM-CM pair considered as a voltage-controlled current source (VCCS). In this manner, by applying (29) and by using the voltage source stamp in Fig. 8b, the system of equations is given by

$$J = \begin{bmatrix} g_1 & -g_1 & 0 & 0 & 1\\ -g_1 & g_1 + G_m & G_m & 0 & 0\\ 0 & 0 & g_2 + sC_1 & -g_2 & 0\\ 0 & G_m & -g_2 + G_m & g_2 + sC_2 & 0\\ 1 & 0 & 0 & 0 & 0 \end{bmatrix} V$$
(30)

where

$$J = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ V_{in} \end{bmatrix}, V = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ i_{Vin} \end{bmatrix}$$
 (31)

The fully-symbolic transfer function of the inverting low-pass filter with node 3 considered as output node is given by

$$-\frac{G_m}{C_1C_2R_2(1+G_mR_1)s^2+(C_1+C_2)(1+G_mR_1)s+G_m}$$
(32)

However, once this expression has been generated, it must still be reduced by taking the limit to infinity of  $G_m$  in (32) [17], [18], [32], [33], [34]. The resulting symbolic expression is the same as the one given by (28). Furthermore, it can be inferred that the size of (30) depends on the number of nodes of the original circuit. Therefore, not only the size of the matrix and the number of non-zero elements has not been reduced with respect to the nullor-based formulation method, but a limit to infinity must be applied. Hence, this formulation method does not show any advantage with respect to nullor-based models.

# B. NA matrix formulation by using pathological element-based models

By using nullor-based models, the original circuit is transformed to a nullor-equivalent circuit and then standard nodal analysis can be applied to formulate the system of equations and to compute symbolic expressions. However, the order of the NA matrix is given by the number of nodes minus the number of nullors, which becomes large if the nullor-based models are also more complex. The reason for this disadvantage is that grounded resistors are used to model the

inverting behavior of some operational amplifiers and current conveyors, as shown in Fig. 4 and in [29]. To avoid the problem of using large nullor-equivalents in active devices with inverting characteristics, the use of pathological element-based models is proposed. The main idea of using pathological elements is to obtain more compact active device models, but with their same original behavior. As a consequence, the order of the system of equations and the number of non-zero coefficients should be reduced. Let us consider again the circuit shown in Fig. 8a and the current conveyor model shown in Fig. 6f. The pathological element-based equivalent circuit is shown in Fig. 8d and by applying standard nodal analysis, the system of equations is obtained as

To reduce the order of (33), the nullor and VM-CM pair properties mentioned in Section II should be applied. According to the nullator properties, the coefficients of the fifth column are added to the first column. From Fig. 8d and by considering the voltage-constraint of the VM,  $V_2 = -V_3$ , the coefficients of the second column should be subtracted from the third column. For the norator connected between node 1 and ground, the first row in (33) should be deleted. Finally, because a CM is connected between nodes 2 and 4 and by applying its current-constraint, the coefficients of the fourth row are subtracted from the second row. So, the NA matrix of Fig. 8b in (33) is reduced to

$$\begin{bmatrix} 0 \\ 0 \\ V_{in} \end{bmatrix} = \begin{bmatrix} -g_1 & g_2 - g_1 & -g_2 - sC_2 \\ 0 & g_2 + sC_1 & -g_2 \\ 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{1,5} \\ V_{-2,3} \\ V_4 \end{bmatrix}$$
(34)

As can be seen, not only the order of the NA matrix is much lower when using the pathological element-based ICCII+ model compared to traditional stamps and nullor-equivalents, but the number of non-zero coefficients is also reduced. For example, the order in (30) is 5 with 12 non-zero coefficients; the order in (27) is 5 with 11 non-zero coefficients, but using the pathological elements the order of the NA matrix is reduced to 3 with only 6 non-zero coefficients, as given by (34). This is a good advantage of using pathological elements in active devices with inverting properties, e.g. the ICCII+. Therefore, the fully-symbolic transfer function of the inverting low-pass filter is computed by considering  $V_{-2,3}$  as output and yielding the same function in (28). Since  $V_2 = -V_3$ , a non-inverting low-pass filter is also obtained if the node 2 is the output, as shown in [45]. A systematic method to obtain (34) is very convenient if active devices are modeled with pathological elements instead of only nullors, as shown in Fig. 5 and Fig. 6, since the formulation method described in Section IV can not be applied. Therefore, a formulation method is required that considers the inverting properties of the VM-CM pair during the formulation process. The new proposed formulation method is described as follows.

C. Generation of tables for nullator-VM, norator-CM, independent current sources and admittances

- Replace each active device by its pathological elementbased model.
- 2) Group and store nullators along with VMs, norators along with CMs, admittances and independent current sources in a table, including their symbols and nodes. From the two constraints given by (7) and (8), the nodes of each VM and CM must be included with their signs, but one should be careful of not to duplicate a node with different signs. In this case, the sign of the nodes of a VM or a CM must be inverted, in order to obtain a uniform agreement of signs.
- 3) Compute the set of nodes ordered in ascending form:  $SetNode = \{q_1, q_2, ... q_i\}$  (0 is the reference node).

#### D. Computing Norator, Nullator, VM and CM indexes

The nodes of nullators, norators, VMs and CMs are manipulated to generate two vectors, namely: P-CM (norator-CM vector) and O-VM (nullator-VM vector), as follows

- 1) Group each pair of nodes of a norator, nullator, VM and CM as a set and store it in the vector P CM or O VM, respectively.
- 2) Compare the nodes of each set with every set of nodes into the same vector (P-CM or O-VM). If a node is duplicated in two sets, they are joined into a single set and ordered in ascending form, but without considering the negative sign of the node numbers.
- 3) Compare each node  $q_i$  of SetNode with every set of nodes of the vector P-CM (alternatively O-CM)
  - If a node of SetNode matches the first node of any set of nodes of the vector P - CM (alternatively O-VM) (without considering the negative sign of the node), the set of nodes must be placed according to the position of the node in SetNode.
  - If a node of *SetNode* does not match with the nodes of any set of nodes of the vector P-CM (alternatively O-VM),  $q_i$  must be included into the vector P-CM (alternatively O-VM) and placed in the same position as in *SetNode*.
- 4) Delete the set of nodes of the vector P-CM (alternatively O-VM), if the reference node is within the set of nodes.

The final vectors are given as:  $O-VM=[O_1,O_2,...O_j]$  and  $P-CM=[P_1,P_2,...P_i]$ , where  $O_j=\{\pm a_1,\pm a_2...\pm a_x\}$  and  $P_i=\{\pm b_1,\pm b_2...\pm b_x\}$  are the set of nodes, and  $a_x$  along with  $b_x$  are the nodes of the sets.

#### E. NA matrix formulation

Manipulating the indexes of admittances along with the vectors O - VM and P - CM, the NA matrix is built as follows

- 1) Compare the nodes of every set of nodes of the vector O VM with the pair of nodes of the admittances.
  - If the node  $|a_x|$  of a set  $O_j$  match with any node of some floating admittances, include the nodes along

with the names of the admittances into  $Col_{\{Oj\}} = [\{a_x, [k, ad_1], ... [k, ad_n]\}].$ 

- If the node  $|a_x|$  match the node of some grounded admittances, include the node  $a_x$  and the admittances as  $Col_{\{O_j\}} = [\{a_x, ad_1, ...ad_n\}].$
- 2) Compare each node  $\pm b_x$  of every set  $P_i$  with the nodes of each set of the list  $Col_{\{Oj\}}$ , in order to generate each coefficient  $Y_{i,j}$  of the NA matrix.
  - If  $b_x = a_x$ , all the admittances in the set of  $Col_{\{Oj\}}$  are added in  $Y_{i,j}$  with positive sign.
  - If  $b_x = -a_x$ , all the admittances in the set of  $Col_{\{Oj\}}$  are added in  $Y_{i,j}$  with negative sign.
  - If  $b_x = k$ , only the admittance connected to the node k is added in  $Y_{i,j}$  with negative sign.
  - If  $b_x = -k$ , only the admittance connected to the node k is added in  $Y_{i,j}$  with positive sign.

### F. Generating V and J vectors

The voltage vector is obtained from the vector O - VM

$$V = [V_{O1}, V_{O2}, ... V_{Oj}]^T (35)$$

Each set  $P_i$  in the vector P-CM represents an entry of current sources

$$J = [P_1, P_2, ... P_i]^T (36)$$

To fill (36), each node  $|b_i|$  of the set  $P_i$  must be compared with the nodes (k, l) of a current source.

- If  $|b_i| = k$ , add the current source with negative sign in (36), according to the position of  $P_i$  in vector P CM.
- If  $|b_i| = l$ , add the current source with positive sign in (36), according to the position of  $P_i$  in vector P CM.

Hence, for any analog circuit modeled with pathological elements, the equivalent circuit has q nodes and p pathological elements, thus, the size of the admittance matrix is equal to  $(q-p)\times(q-p)$ . Comparing the two proposed formulation methods, that introduced in Section IV, and that described above, we can conclude that the former can be considered a particular case of the latter.

### G. NA matrix formulation by applying the proposed method

To show the usefulness of the pathological element-based models of active devices and the potential of the proposed symbolic formulation method introduced in the previous sections, we consider again the symbolic analysis of the ICCII+based inverting low-pass filter shown in Fig. 8d [45]. Following the proposed formulation method, all the two-terminal elements are stored in Table II. The set of nodes is obtained from Fig. 8d and given by

$$SetNodes = \{1, 2, 3, 4, 5\}$$
 (37)

According to subsection V-D and from Table II, the final vectors O-VM and P-CM are obtained as

$$O - VM = [\{1, 5\}, \{-2, 3\}, \{4\}]$$
(38)

$$P - CM = [\{2, -4\}, \{3\}, \{5\}]$$
 (39)

TABLE II
TWO-TERMINAL ELEMENTS FROM FIG. 8D.

O-VM	Node	P-CM	Node	Adm.	Node	Current source	Node
$O_1$	1,5	$P_1$	1,0	$g_s$	5,0	$V_{in}$	0,5
$VM_2$	3,-2	$CM_2$	2,-4	$g_1$	1,2		
				$g_2$	3,4		
				$C_1$	3,0		
				$C_2$	4,0		

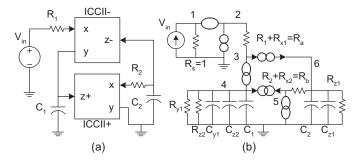


Fig. 9. (a) Non-inverting band-pass and low-pass filter taken from [45] (b) Pathological element-based model

According to subsection V-E, the nodes of the admittances given in Table II along with the indexes of (38) are manipulated to obtain the lists  $Col_{\{O_i\}}$  as

$$Col_{\{O_1\}} = [\{\mathbf{1}, [2, g_1]\}, \{\mathbf{5}, g_s\}]$$

$$Col_{\{O_2\}} = [\{\mathbf{-2}, [1, g_1]\}, \{\mathbf{3}, [4, g_2], C_1\}]$$

$$Col_{\{O_3\}} = [\{\mathbf{4}, [3, g_2], C_2\}]$$

$$(40)$$

Later on, each node of (39) is compared with each node of (40) and therefore, the admittance matrix given by (34) is obtained with  $g_s=1$ . The voltage vector is obtained from (38) as

$$V = [V_{1.5}, V_{-2.3}, V_4]^T \tag{41}$$

and finally, the current vector is obtained by comparing each node of (39) with the nodes of the current source in Table II and given by

$$J = [0, 0, V_{in}]^T (42)$$

#### VI. ILLUSTRATIVE EXAMPLE

As a second example to compare the existing and proposed formulation methods, lets us consider the non-inverting bandpass and low-pass filter using ICCII± shown in Fig. 9a [45]. The behavior of each active device is modeled with its pathological element-equivalent as shown in Figs. 6f and 6g augmented with parasitic elements. The equivalent circuit is illustrated in Fig. 9b. Following the proposed formulation method, the names and nodes of the nullators, norators, VMs, CMs, admittances and independent current sources are stored in Table III. From Fig. 9b, the set of nodes is obtained as

$$SetNodes = \{1, 2, 3, 4, 5, 6\}$$
 (43)

From Table III, the nodes of the nullators, VMs, norators and CMs are grouped and stored in the vectors O-VM and P-CM, respectively

$$O - VM = [\{-3, 4\}, \{0, -5\}, \{1, 2\}] \tag{44}$$

 $\begin{tabular}{ll} TABLE~III\\ Two-terminal~elements~from~Fig.~9b. \end{tabular}$ 

O-VM	Node	P-CM	Node	Adm.	Node	Current	Node
						source	
$O_1$	1,2	$P_1$	2,0	$g_s$	1,0	$V_{in}$	0,1
$VM_2$	4,-3	$P_2$	3,6	$g_a$	2,3		
$VM_3$	0,-5	$CM_3$	5,-4	$g_b$	5,6		
				$g_{z1}$	6,0		
				$g_{z2}$	4,0		
				$g_{y1}$	4,0		
				$C_1$	4,0		
				$C_2$	6,0		
				$C_{z1}$	6,0		
				$C_{z2}$	4,0		
				$C_{y1}$	4,0		

$$P - CM = [\{5, -4\}, \{3, 6\}, \{2, 0\}]$$
 (45)

The set of nodes in (44) and (45) are ordered with respect to the nodes of (43), and the nodes  $q_i$  of (43) which are not considered in the set of nodes in (44) and (45), are included in the vectors O - VM and P - CM, respectively

$$O - VM = [\{1, 2\}, \{-3, 4\}, \{-5, 0\}, \{6\}]$$
 (46)

$$P - CM = [\{1\}, \{2, 0\}, \{3, 6\}, \{-4, 5\}] \tag{47}$$

The reference node is included into the third and second set of nodes in (46) and (47), hence, they should be deleted. Thus, the final vectors are given by

$$O - VM = [\{1, 2\}, \{-3, 4\}, \{6\}]$$
(48)

$$P - CM = [\{1\}, \{3, 6\}, \{-4, 5\}] \tag{49}$$

By manipulating the admittances along with their nodes given in Table III and the indexes of (48), the lists  $Col_{\{Oj\}}$  are given as

$$\begin{split} &Col_{\{O_1\}} = [\{\mathbf{1},g_s\},\{\mathbf{2},[3,g_a]\}] \\ &Col_{\{O_2\}} = [\{\mathbf{-3},[2,g_a]\},\{\mathbf{4},g_{z2},g_{y1},C_{z2},C_{y1},C_1\}] \\ &Col_{\{O_3\}} = [\{\mathbf{6},[5,g_b],g_{z1},C_{z1},C_2\}] \end{split} \tag{50}$$

Afterwards, each node  $\pm b_i$  of every set  $P_i$  in (49) is compared with the nodes of (50). For instance, let us consider the set  $P_3 = \{-4, 5\}$ . In order to obtain the coefficient  $Y_{3,2}$ , each node of the set  $P_3$  is compared with each node of  $Col_{\{O_2\}}$ , thus,  $Y_{3,2} = -g_{y1} - g_{z2} - s(C_{y1} + C_{z2} + C_1)$ . Vector V is obtained by using (48) and given by

$$V = [V_{1,2}, V_{-3,4}, V_6]^T (51)$$

Vector J is obtained by comparing each node of (49) with the pair of nodes of the independent current source shown in Table III and given by

$$J = [V_{in}, 0, 0]^T (52)$$

Therefore, the system of equations from Fig. 9b by using pathological element-based models becomes

$$J = \begin{bmatrix} g_s & 0 & 0 \\ -g_a & -g_a & g_b + g_{z1} + sC_b \\ 0 & -g_{y1} - g_{z2} - sC_a & -g_b \end{bmatrix} V$$
(53)

TABLE IV COMPARISON OF FORMULATION METHODS.

Formulation method	Size	Non-zero coefficients
MNA with controlled sources	$8 \times 8$	20
MNA with limit-variables	$6 \times 6$	15
Nodal analysis with nullor-equivalent	$6 \times 6$	13
Nodal analysis with pathological elements	$3 \times 3$	6

TABLE V
CPU-TIME AND MEMORY CONSUMPTION USED TO SOLVE THE SYSTEM OF EQUATIONS.

Equation	CPU-time (ms)	Memory (bytes)	DDD nodes	DDD paths
(53)	1	136,648	5	2
(56)	30	2,029,036	11	2
(57)	10	271,852	12	4
(58)	10	271,852	10	2

where  $C_a = C_{y1} + C_{z2} + C_1$  and  $C_b = C_{z1} + C_2$ . The low-pass response with both polarities can be obtained by solving (53) to  $V_{-3,4}$  and considering that  $V_3 = -V_4$ , as already provided in (54). The band-pass response is available at node  $V_6$  and given by (55). If parasitic elements are not considered, then ideal transfer functions are computed [45].

The system of equations of the circuit shown in Fig. 9a, has also been formulated with

- MNA by using controlled sources
- MNA by applying limit-variables stamp
- Nodal analysis by using nullor-equivalents

The system of equations for each formulation method is given by: (56), where  $\beta_1$ ,  $\beta_2$  and  $\mu_1$  are the gains of the controlled sources; (57), where,  $G_{m1}$ ,  $G_{m2}$  are the transconductance gains of the VM-CM pairs and (58), where the formulation method introduced in Section IV has been applied. Comparisons between the size of the admittance matrix and the generation of non-zero coefficients according to the formulation methods are summarized in Table IV. Therefore, we can see that by applying the formulation method described in Section V, the size of the admittance matrix is reduced. Further, we also note that some cancelling terms are generated with the formulation methods described in Table IV, whereas with the new formulation method, the generation of cancelling terms is reduced. For instance, (53) is cancellation-free and (34) has only one cancelling term. Furthermore, if controlled sources are used to model the behavior of ICCII± and the MNA method is applied, twenty non-zero coefficients are generated. Otherwise, if the proposed formulation method is executed, only six non-zero coefficients are generated.

To validate the efficiency of our formulation methods in terms of CPU-time and memory consumption, the four system of equations from Fig. 9a given by Eqs. (53), (56), (57) and (58) have been solved by applying DDD method. The solution method was run on a 3.06-GHz Intel Xeon 4 Cores machine with 2GB RAM. Table V shows the average CPU-time and memory consumption required during solution of the system of equations for each formulation method. In this way, less CPU-time and memory consumption are required to solve (53) instead of (56). Also, from Table IV, twenty

$$V_3 = -V_4 = \frac{g_a g_b}{C_a C_b s^2 + (C_a (g_b + g_{z1}) + C_b (g_{y1} + g_{z2})) s + g_b (g_a + g_{y1} + g_{z2}) + g_{z1} (g_{y1} + g_{z2})}$$
(54)

$$V_{6} = \frac{g_{a}(g_{y1} + g_{z2} + C_{a}s)}{C_{a}C_{b}s^{2} + (C_{a}(g_{b} + g_{z1}) + C_{b}(g_{y1} + g_{z2}))s + g_{b}(g_{a} + g_{y1} + g_{z2}) + g_{z1}(g_{y1} + g_{z2})}$$
(55)

$$\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ V_{in} \end{bmatrix} = \begin{bmatrix} g_a & -g_a & 0 & 0 & 0 & 0 & 0 & 1 \\ g_a & -g_a & 0 & 0 & 0 & -1 & 0 & 0 \\ -g_a & g_a & 0 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & g_{y1} + g_{z2} + sC_a & -\beta_2 g_b & \beta_2 g_b & 0 & 0 & 0 \\ 0 & 0 & 0 & g_b & -g_b & 0 & 1 & 0 \\ -\beta_1 g_a & \beta_1 g_a & 0 & -gb & g_b + g_{z1} + sC_b & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \\ i_{vcvs_1} \\ i_{v_{in}} \end{bmatrix}$$

$$(56)$$

$$\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ V_{in} \end{bmatrix} = \begin{bmatrix} g_a & -g_a & 0 & 0 & 0 & 1 \\ -g_a & g_a + G_{m1} & G_{m1} & 0 & 0 & 0 \\ 0 & 0 & g_{y1} + g_{z2} + sC_a & G_{m2} & 0 & 0 \\ 0 & 0 & 0 & g_b + G_{m2} & -g_b & 0 \\ 0 & -G_{m1} & -G_{m1} & -g_b & g_b + g_{z1} + sC_b & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \\ i_{v_{in}} \end{bmatrix}$$
(57)

$$\begin{bmatrix} V_{in} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -g_a & g_a & 0 & -g_b & g_b + g_{z1} + sC_b & 0 \\ 0 & 0 & g_{y1} + g_{z2} + sC_a & 0 & 0 & 1 \\ 0 & 0 & 0 & g_b & -g_b & 1 \\ 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{1,2} \\ V_{3,7} \\ V_{4,8} \\ V_{5,11} \\ V_6 \\ V_{9,10} \end{bmatrix}$$
(58)

non-terminal vertices are required to represent (56) by means of DDDs. Otherwise, if the proposed formulation method is executed, only six non-terminal vertices are necessary to represent (53) with DDDs. As a consequence, the complexity in the generation of non-terminal vertices along with the CPU-time and memory consumption used during the solution of (53) are reduced, as shown in Table V [8], [12], [13], [14].

Our experiences show that if the behavior of active devices are adequately modeled with pathological elements, the size of the system of equations and the number of non-zero coefficients are always smaller than those generated with other formulation methods. In the worst case, there are analog circuits that by the manner of how they are connected, the pathological element-based model is reduced to its nullor-based equivalent model and, however, the proposed formulation method from Section V still can be applied. This is the case of the OTRA, COA and FOTRA when the negative terminal is floating, for instance. Additionally, in the proposed pathological elementbased models, parasitic elements can be considered while maintaining a lower order of the NA matrix than by applying the limit-variables method or nullor-equivalents, for which the system of equations is large and as already shown in Subsection V-A a limit to infinity is always required in order to simplify the symbolic expressions.

On the other hand, the proposed formulation methods are based on the manipulation of the interconnection relationships of the pathological elements. Therefore, if pathological element-based models of new active devices are complex, (i.e. a large number of floated or grounded resistors are used to model the behavior of active devices), the size of the NA matrix and the number of non-zero coefficients increases. As a consequence, the CPU-time and memory consumption used to solve the system of equations with any solution method is also increased. A limitation of the proposed formulation methods is that floating pathological element-based active device models cannot be included into the formulation process. In this case, stamps of floating pathological elements can be used, but a limit to infinity must be again applied to reduce the symbolic expressions.

#### VII. CONCLUSIONS

In this paper, we proposed novel pathological element-based active device models and new approaches to formulate the NA matrix of analog circuits. Nullators, norators VMs and CMs properties were used in order to model the behavior of several active devices, eventually including parasitic elements. The significant advantage of our proposed symbolic formulation method is that the NA matrix can quickly be constructed by manipulating the relationship between the indexes of the pathological elements and admittances. It was demonstrated that the new approximation achieves a considerable reduction not only in the order of the system of equations, but also in the generation of non-zero coefficients into the NA matrix, which have been compared with the formulation methods given in Table IV. The formulation method described in Section V can be easily implemented within a design automation tool and from Table V we can conclude that the compacted NA matrix

improves the CPU-time and memory consumption during the solution process.

#### REFERENCES

- [1] L. O. Chua and P. M. Lin, Computer-Aided Analysis of Electronic Circuits. N. J.: Prentice Hall, 1975.
- [2] J. Vlach and K. Singhal, Computer Methods for Circuit Analysis and Design. Norwell, MA: Kluwer, 1993.
- [3] G. Gielen and W. Sansen, Symbolic Analysis for Automated Design of Analog Integrated Circuits. USA: Kluwer Academic Publishers, 1991.
- [4] F. V. Fernández, A. Rodríguez-Vázquez, J. L. Huertas, and G. Gielen, Symbolic Analysis Techniques: Applications to Analog Design Automation. Piscataway, NJ: IEEE Press, 1998.
- [5] R. Rutenbar, G. Gielen, and B. A. Antao, Computer-Aided Design of Analog Integrated Circuits and Systems. NY: Wiley, 2002.
- [6] Z. Qin, S. X.-D. Tan, and C.-K. Cheng, Symbolic Analysis and Reduction of VLSI Circuits. USA: Springer, 2005.
- [7] M. Fakhfakh, E. Tlelo-Cuautle, and F. Fernández, *Design of Analog Circuits Through Symbolic Analysis*. Bentham Sciences Publishers, 2010.
- [8] G. Gielen, H. Walscharts, and W. Sansen, "ISAAC: a symbolic simulator for analog integrated circuits," *IEEE J. Solid-State Circuits*, vol. 24, no. 6, pp. 1587–1597, December 1989.
- [9] F. V. Fernández, A. Rodríguez-Vázquez, and J. L. Huertas, "Interactive AC modeling and characterization of analog circuits via symbolic analysis," *Analog Integrated Circuits and Signal Processing*, vol. 1, no. 3, pp. 183–208, November 1991.
- [10] R. Castro-López, O. Guerra, F. V. Fernández, and A. Rodríguez-Vázquez, "Synthesis of a Wireless Communication Analog Back-End Based on a Mismatch-Aware Symbolic Analysis," *Analog Integrated Circuits and Signal Processing*, vol. 40, no. 3, pp. 215–233, September 2004.
- [11] G. Shi, "Computational complexity analysis of determinant decision diagram," *IEEE Trans. on Circuits and Systems II: Express Briefs*, pp. 1– 5, Doi:10.1109/TCSII.2010.2067791, September 2010.
- [12] C. Shi and S. Tan, "Canonical symbolic analysis of large analog circuits with determinant decision diagrams," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 19, no. 1, pp. 1–18, January 2000.
- [13] S. Tan, "Symbolic analysis of analog circuits by boolean logic operations," *IEEE Trans. on Circuits and Systems II: Express Briefs*, vol. 53, no. 11, pp. 1313–1317, November 2006.
- [14] W. Verhaegen and G. Gielen, "Efficient DDD-based symbolic analysis of linear analog circuits," *IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 49, no. 7, pp. 474–487, July 2002.
- [15] P. Wambacq, F. Fernández, G. Gielen, W. Sansen, and A. Rodríguez-Vázquez, "A family of matroid intersection algorithms for the computation of approximated symbolic network functions," in *Proc. IEEE International Symposium on Circuits and Systems*, vol. 4, pp. 806–809, 1996.
- [16] S.-D. Tan and C.-J. R. Shi, "Efficient approximation of symbolic expressions for analog behavioral modeling and analysis," *IEEE Trans.* on Computer-Aided Design of Integrated Circuits and Systems, vol. 23, pp. 907–918, June 2004.
- [17] D. G. Haigh, T. J. Clarke, and P. M. Radmore, "Symbolic framework for linear active circuits based on port equivalence using limit variables," *IEEE Trans. on Circuits and Systems I: Regular Papers*, vol. 53, no. 9, pp. 2011–2024, September 2006.
- [18] D. G. Haigh and P. M. Radmore, "Admittance matrix models for the nullor using limit variables and their application to circuit design," *IEEE Trans. on Circuits and Systems I: Regular Papers*, vol. 53, no. 10, pp. 2214–2223, October 2006.
- [19] C. Sánchez-López, F. V. Fernández, and E. Tlelo-Cuautle, "Generalized admittance matrix models of OTRAs and COAs," *Microelectronics Journal*, vol. 41, no. 8, pp. 502–505, August 2010.
- [20] H. J. Carlin, "Singular network elements," *IEEE Trans. on Circuit Theory*, vol. CT-11, no. 3, pp. 67–72, March 1964.
- [21] J. A. Svoboda and R. J. Wojcik, "Sensitivity analysis of RLC nullor networks," *International Journal of Circuit Theory and Applications*, vol. 10, pp. 139–150, April 1982.
- [22] J. A. Svoboda, "Using nullors to analyse linear networks," *International Journal of Circuit Theory and Applications*, vol. 14, no. 3, pp. 169–180, July 1986.

- [23] A. Carlosena and G. S. Moschytz, "Nullators and norators in voltage to current mode transformations," *International Journal of Circuit Theory* and Applications, vol. 21, no. 4, pp. 421–424, July/August 1993.
- [24] H. Floberg, Symbolic analysis in analog integrated circuit design. USA: Kluwer Academic Publishers, 1997.
- [25] H. Schmid, "Approximating the universal active element," *IEEE Trans. on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 47, pp. 1160–1169, November 2000.
- [26] P. Kumar and R. Senani, "Bibliography on nullors and their applications in circuit analysis, synthesis and design," *Analog Integrated Circuits and Signal Processing*, vol. 33, no. 1, pp. 65–76, October 2002.
- [27] C. Sánchez-López and E. Tlelo-Cuautle, "Behavioral model generation for symbolic analysis of analog integrated circuits," in *Proc. IEEE International Symposium on Signals, Circuits and Systems*, pp. 327–330, 2005
- [28] C. Sánchez-López and E. Tlelo-Cuautle, "Behavioral model generation of current-mode analog circuits," in *Proc. IEEE International Sympo*sium on Circuits and Systems, pp. 2761–2764, 2009.
- [29] E. Tlelo-Cuautle, C. Sánchez-López, and D. Moro-Frías, "Symbolic analysis of (MO)(I)CCI(II)(III)-based analog circuits," *International Journal of Circuit Theory and Applications*, vol. 38, pp. 649–659, August 2010.
- [30] E. Tlelo-Cuautle, C. Sánchez-López, E. Martínez-Romero, and S. X.-D. Tan, "Symbolic analysis of analog circuits containing voltage mirrors and current mirrors," *Analog Integrated Circuits and Signal Processing*, vol. 65, no. 1, pp. 89–95, October 2010.
- [31] A. M. Soliman and R. A. Saad, "On the voltage mirrors and the current mirrors," *Analog Integrated Circuits and Signal Processing*, vol. 32, no. 1, pp. 79–81, July 2002.
- [32] R. A. Saad and A. M. Soliman, "A new approach for using the pathological mirror elements in the ideal representation of active devices," *International Journal of Circuit Theory and Applications*, vol. 38, no. 2, pp. 148–178, March 2010.
- [33] R. A. Saad and A. M. Soliman, "Use of mirror elements in the active device synthesis by admittance matrix expansion," *IEEE Trans. on Circuits and Systems I: Regular Papers*, vol. 55, no. 9, pp. 2726–2735, October 2008.
- [34] A. M. Soliman and R. A. Saad, "The voltage mirror-current mirror pair as a universal element," *International Journal of Circuit Theory and Applications*, Online Doi:10.1002/cta.596, April 2009.
- [35] A. M. Soliman, "Adjoint network theorem and floating elements in the NAM," *Journal of Circuits, Systems and Computers*, vol. 18, no. 3, pp. 597–616, May 2009.
- [36] A. M. Soliman, "Pathological representation of the two-output ccii and iccii family and application," *International Journal of Circuit Theory* and Applications, Online Doi:10.1002/cta.664, April 2010.
- [37] C. Sánchez-López, D. Moro-Frías, and E. Tlelo-Cuautle, "Improving the formulation process of the system of equations of analog circuits," in *Proc. International Workshop on Symbolic and Numerical Methods, Modeling and Applications to Circuit Design*, pp. 102–106, 2008.
- [38] E. Tlelo-Cuautle, E. Martínez-Romero, C. Sánchez-López, and S. X.-D. Tan, "Symbolic formulation method for mixed-mode analog circuits using nullors," in *Proc. IEEE International Conference on Electronics*, Circuits and Systems, pp. 856–859, 2009.
- [39] J. A. Svoboda, "Current conveyors, operational amplifiers and nullors," IEE Proceedings G Circuits, Devices & Systems, vol. 136, no. 6, pp. 317–322, December 1989.
- [40] R. Cabeza, A. Carlosena, and L. Serrano, "Unified approach to the implementation of universal active devices," *Electronics Letters*, vol. 30, pp. 618–620, January 1994.
- [41] R. Cabeza and A. Carlosena, "Analog universal active device: Theory, design and applications," *Analog Integrated Circuits and Signal Pro*cessing, vol. 12, pp. 153–168, February 1997.
- [42] J. Huijsing, "Operational floating amplifier," *IEE Proceedings G Circuits, Devices & Systems*, vol. 137, pp. 131–136, April 1990.
- [43] J. Huijsing, "Design and applications of the operational floating amplifier (ofa): the most universal operational amplifier," *Analog Integrated Circuits and Signal Processing*, vol. 4, pp. 115–129, September 1993.
- [44] S. Mahmoud, A. Madia, and A. Soliman, "Low-voltage cmos current feedback operational amplifier and its application," *ETRI Journal*, vol. 29, pp. 212–218, April 2007.
- [45] A. M. Soliman, "The inverting second generation current conveyors as universal buildings blocks," *International Journal of Electronics and Communications*, vol. 62, pp. 114–121, February 2008.