# Improving positive and negative bias illumination stress stability in parylene passivated IGZO transistors

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Citation: Appl. Phys. Lett. **109**, 051606 (2016); doi: 10.1063/1.4960200

View online: https://doi.org/10.1063/1.4960200

View Table of Contents: http://aip.scitation.org/toc/apl/109/5

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# Improving positive and negative bias illumination stress stability in parylene passivated IGZO transistors

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(Received 23 May 2016; accepted 21 July 2016; published online 5 August 2016)

The impact of a parylene top-coating layer on the illumination and bias stress instabilities of indium-gallium-zinc oxide thin-film transistors (TFTs) is presented and discussed. The parylene coating substantially reduces the threshold voltage shift caused by continuous application of a gate bias and light exposure. The operational stability improves by 75%, and the light induced instability is reduced by 35%. The operational stability is quantified by fitting the threshold voltage shift with a stretched exponential model. Storage time as long as 7 months does not cause any measurable degradation on the electrical performance. It is proposed that parylene plays not only the role of an encapsulation layer but also of a defect passivation on the top semiconductor surface. It is also reported that depletion-mode TFTs are less sensitive to light induced instabilities. This is attributed to a defect neutralization process in the presence of free electrons. *Published by AIP Publishing.*
[http://dx.doi.org/10.1063/1.4960200]

The application of multicomponent oxide thin-film transistors (TFTs) like indium-gallium-zinc oxide (IGZO) TFTs has been limited by environmental effects. The impact of channel surface-adsorbed species on bias stress instability has been reported by many authors.[1,2] The degradation is attributed to $O_2$ and $H_2O$ interaction at the air-exposed semiconductor surface, particularly relevant when a typical staggered bottom-gate structure is considered.[3] To protect oxide TFTs from atmosphere, different materials have been used as passivation layers, such as $Al_2O_3$,[4] $SiO_x$,[5] polyimide,[5] SU-8,[6] $SiN_x$,[7] and parylene.[8] Parylene specifically has also been widely used as an encapsulation layer on printed circuit boards and in biomedical applications using other semiconductor technologies.[9] The selection of parylene as a coating material for IGZO TFTs brings several advantages: It is a protective conformal polymer with low moisture absorption (<0.1% after 24 h (Ref. 10)). It is transparent, being thus compatible with transparent electronics. The ability to deposit parylene at room temperature makes it very desirable for flexible electronics.

Although oxide semiconductors are transparent, some studies show that the light induced electrical characteristics changes for wavelengths below band gap, and a well-known effect of the negative shift of the threshold voltage ($\Delta V_{th}$) occurs under light exposure.[11] This instability has been attributed to the interaction of light with traps located near the TFT channel or in the semiconductor bulk. Takechi *et al.* reported that these traps are light-induced oxygen interstitials.[12] The trapped charges enhance the TFT conductance and remain for a long period of time leading to a persistent photoconductivity (PPC). Görrn *et al.*[13] and Gosain *et al.*[14] also attributed the light induced changes to adsorbed oxygen that becomes charged by photogenerated electron/hole pairs. Ionization of the oxygen vacancies has also been proposed to explain the PPC effect.[15] Zhou *et al.* showed that the wavelength of light and the thickness of the passivation layer have a direct influence on the light-induced instabilities.[4] It is noteworthy that most of the reported oxides TFTs are enhancement-mode devices, which indeed brings immediate advantages to design high-gain circuits only with n-type transistors with minimum complexity. Still, depletion-mode operation is also desirable, e.g., to use as inverter loads.[16] As will be seen in this work, depletion-mode TFTs can be good candidates for display applications, owing to their reliability under illumination.[17]

This paper reports our findings on how the combination of parylene passivation and depletion-mode operation can improve the stability of IGZO TFTs under both bias and illumination stress. By using non-coated devices as reference, degradation mechanisms are identified.

TFTs have a staggered bottom gate structure. The inset of Fig. 1(a) shows a schematic diagram of a structure with a parylene top-layer. The aspect ratio is W/L = 160 $\mu$m/20 $\mu$m. Both semiconductor and source-drain electrode layers were deposited by radio frequency magnetron sputtering without intentional substrate heating on top of a 100 nm thick $SiO_2$ dielectric layer grown by plasma-enhanced chemical vapor deposition (PECVD) on highly doped n-type Si wafers. The semiconductor film (36 nm thick) was sputtered using a multicomponent ceramic target of IGZO 2:1:2 ($In_2O_3$:$Ga_2O_3$:ZnO molar ratio) in an Ar+$O_2$ atmosphere using a power density of 4.9 W/cm$^2$ and a deposition pressure of 0.3 Pa. The Mo electrodes (60 nm thick) were sputtered in pure Ar atmosphere from a metallic Mo target. All layers were patterned by photolithography and lift-off techniques. The devices were then submitted to a thermal treatment on a hot plate at 200 °C for 1 h.[18] Some devices were left non-passivated as reference and one additional set of transistors was passivated using a 1 $\mu$m

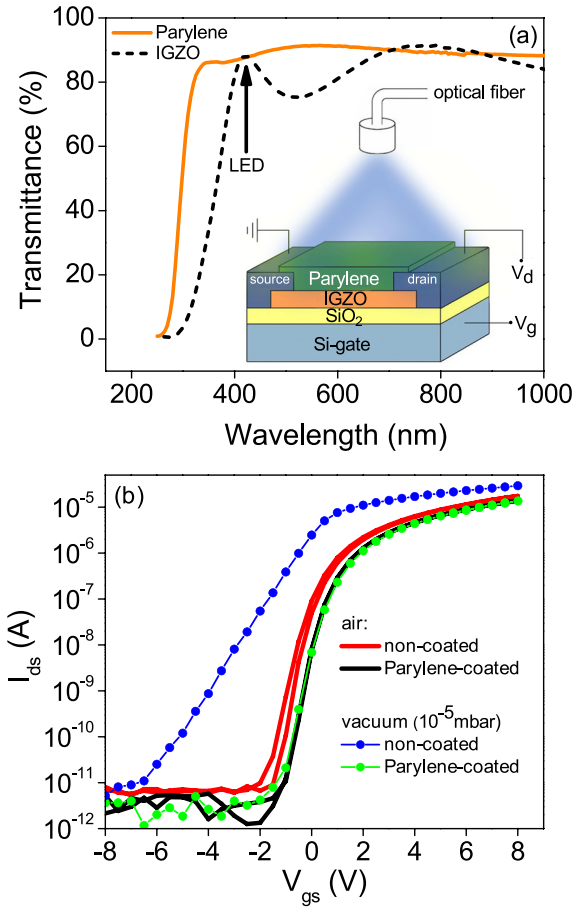


FIG. 1. (a) Optical transmittance of parylene and IGZO as function of light wavelength. The inset shows parylene-passivated IGZO-$SiO_2$ TFT schematic and light experiment setup. (b) Transfer characteristics for the parylene-passivated and non-passivated TFTs in air and vacuum ($10^{-3}$ Pa).

thick chemical vapor deposited parylene-C (poly (monochloro-*p*-xylylene)). An adhesion promoter consisting of Sylane A-147 from Specialty Coating was used in order to improve the adhesion between parylene-C and the active layer.[19] Parylene deposition was achieved through a chemical vapor deposition (CVD-PDS-2010) tool. Parylene coating is highly conformal, assuring a complete coverage of the air exposed semiconductor. Parylene layers were also deposited on quartz glass for optical transmittance measurements. In the visible and near UV window (350 and 1000 nm), the parylene layer has a transparency of 90% (see Fig. 1(a)). The electrical characterization was carried out using a Keithley 4200-SCS semiconductor parameter analyzer. Positive gate bias stress (PBS) was performed at RT and in dark, applying a gate-to-source voltage ($V_{gs}$) of 5 V, while keeping source and drain grounded.

Both parylene-coated and non-coated TFTs were illuminated by using a LED (fiber-coupled light emitting diode by Thorlabs) with peak wavelength at 420 nm. The optical power incident on the device was 0.5 mW cm$^{-2}$. For negative bias illumination stress (NBIS), this optical stimulus was superimposed to $V_{gs} = -15$ V. A schematic of the device configuration for electrical stress/illumination tests is shown in the inset of Figure 1(a).

Figure 1(b) compares the TFT transfer curves of non- and parylene-coated devices measured in air and under vacuum. Field-effect mobility ($\mu_{FE}$) is extracted at drain-to-source voltage ($V_{ds}$) of 0.1 V, and subthreshold swing ($SS$) is taken as the minimum value of $d(\log(I_{ds})/(V_{gs}))^{-1}$. Typical electrical parameters extracted for parylene-coated devices are $V_{th} \approx -0.8$ V, $\mu_{FE} = 10.2$ cm$^2$/V s, and $SS = 0.3$ V/dec. The threshold voltage is usually extracted by the linear extrapolation of the transfer curve to the voltage axis. To overcome the problem of non-linearity of transfer characteristics, $V_{th}$ is taken at the voltage corresponding to Ids = 20 nA. The time evolution of $V_{th}$ under a constant current provides a good estimation of the $\Delta V_{th}$.

The parylene-coated TFTs show identical transfer curves in both environments and a negligible clockwise hysteresis, consistent with a residual amount of charge trapping at the channel/dielectric interface. This behavior confirms that parylene prevents the diffusion of atmospheric species into the IGZO layer. In contrast, non-coated TFTs when measured in vacuum show a rapid shift of the transfer curves to larger negative voltage and a significant degradation on the subthreshold slope. These changes are fully reversible suggesting that vacuum removes weakly bonded oxygen species out of the semiconductor layer, i.e., its conductance depends on a compositional equilibrium between the semiconductor itself and the surrounding environment.

The effectiveness of the parylene encapsulation is explored through PBS experiments. Devices were tested after fabrication (as-fabricated) and after storage for 7 months in air and dark conditions (aged devices). During the PBS experiments, they were submitted to a continuous gate voltage of 5 V. Fig. 2(a) shows a set of consecutive transfer curves measured as function of time for a non-coated TFT in air. The transfer characteristics shift toward positive $V_{gs}$, resulting in $\Delta V_{th} = 2.2$ V. The parylene-coated device shows a similar trend but with a smaller magnitude of $\Delta V_{th} = 0.4$ V, as shown in Fig. 2(b). After 7 months of storage, parylene-coated transistors do not reveal significant changes with respect to the as-fabricated devices. Fig. 3 compares the relative changes in $V_{th}$ with time for non- and parylene-coated TFTs, showing the effects of ageing and atmosphere. Coated devices are more stable with respect to PBS as well as to ageing. In terms of stability, parylene-coated devices in air outperform the non-coated ones under vacuum, suggesting that parylene acts as a passivation layer. Positive $\Delta V_{th}$ with unchanged $SS$ value under PBS is explained by an electron charge trapping mechanism. The operational stability is quantified by fitting the time dependence of $\Delta V_{th}$ with a stretched-exponential time dependent (SE) model as

$$\Delta V_{th} = V_0 \left\{ 1 - \exp\left[ -\left( \frac{t}{\tau} \right)^{\beta} \right] \right\}, \qquad (1)$$

where $V_0 = |\Delta V_{th}|$ at the infinite time, $t$ is the stress time, $\beta$ is a dispersion parameter, and $\tau$ a characteristic time that measures how fast the threshold voltage moves with time. $\tau$ can be used as a figure of merit to quantify operational stability. The change in threshold voltage $\Delta V_{th}$ for non-coated TFTs and parylene coated devices was fitted with the SE model. In order to assess ageing effects on device stability, TFTs were measured immediately after fabrication and 7 months later.

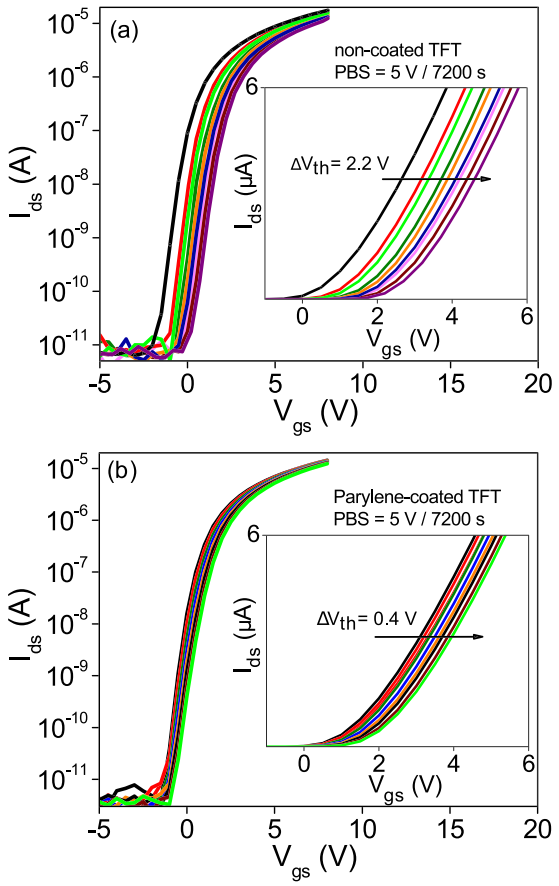


FIG. 2. Typical threshold voltage shift evolution of transfer characteristics for (a) non-passivated TFT, (b) parylene-passivated device, at $V_{ds} = 0.1$ V under PBS = 5 V in air, at RT. Data representation on linear scale is shown in the inset.

Table I shows the values of $\beta$ and $\tau$ for the TFTs studied here. For fresh produced and non-coated devices, $\beta$ varies from 0.4 (in vacuum) to 0.6 (in air). For aged and coated devices, $\beta$ remains unchanged. Moreover, parylene coated devices show values of $\tau$ one order of magnitude higher than non-coated transistors, reinforcing their improved stability.

The effects of light exposure (420 nm) associated with negative bias stress (i.e., NBIS) on non- and parylene-coated

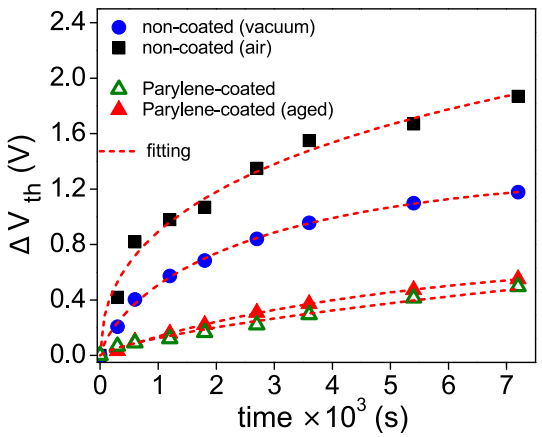


FIG. 3. Comparison of the threshold voltage shift evolution of parylene-coated device with non-coated TFT under PBS = 5 V, operating in air and vacuum at RT. The measured data are well fitted with stretched exponential equation. Fitting parameters are shown in Table I.

TABLE I. Comparison of the threshold voltage shift $\Delta V_{th}$, characteristic trapping time $\tau$, dispersion parameter $\beta$, and recovery time of TFTs.

| TFTs | $\Delta V_{th}$ (V) | $\tau$ (s) | $\beta$ | Recovery |
|---|---|---|---|---|
| Non-coated (in air) | 2.2 | $1.1 \times 10^4$ | 0.6 | >2 days |
| Non-coated (in vacuum) | 1.1 | $1.8 \times 10^5$ | 0.4 | ~17 h |
| Parylene-coated (as fabricated) | 0.4 | $1.9 \times 10^5$ | 0.5 | ~17 h |
| Parylene-coated (aged 7 months) | 0.5 | $1.5 \times 10^5$ | 0.5 | ~17 h |

TFTs are shown in Figs. 4(a) and 4(b), respectively. $V_{th}$ is extrapolated from the linear portion of the transfer curves. The inset shows $\Delta V_{th}$ extracted for each transfer curve and recovery of $V_{th}$ after removing NBIS. It shows an exponential trend. NBIS causes several effects: (i) a threshold voltage shift, (ii) an increase in the subthreshold slope, and (iii) at long exposure times (t = 100 s) the appearance of a hump on the transfer curves. NBIS has a pronounced effect on the non-coated transistor. The parylene-coated TFT have shown $\Delta V_{th} = -3.7$ V, which is relatively small compared to $\Delta V_{th} = -5.2$ V. Furthermore, the degradation on *SS* is also smaller for the parylene coated TFTs. In summary, the parylene-coated device is less sensitive to light. This cannot be attributed to a difference in the optical power. As shown previously, the parylene coating layer has a transparency higher than 90% for wavelengths close to 420 nm.

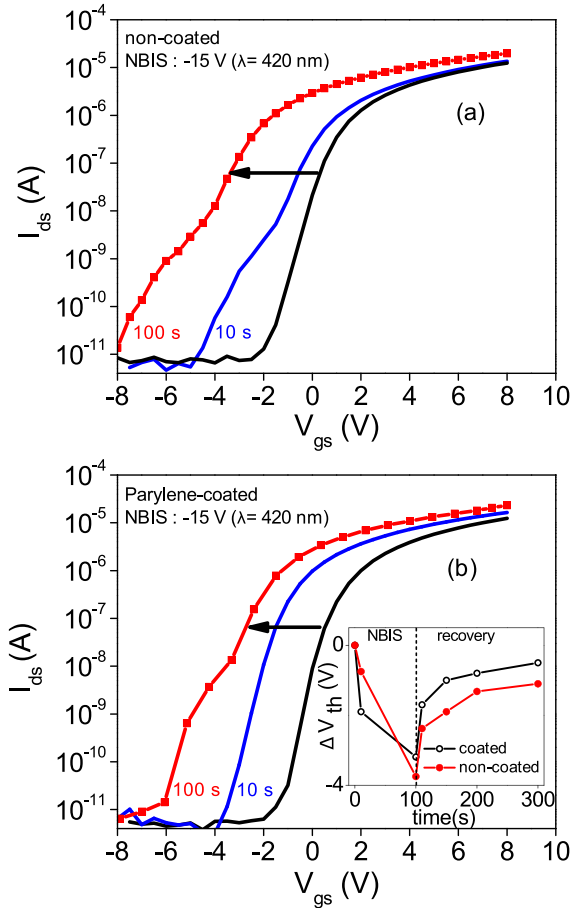


FIG. 4. Typical transfer characteristics ($V_{ds} = 0.1$ V) for (a) non-coated and (b) parylene-coated TFTs under NBIS at $V_{gs} = -15$ V after 10 s and 100 s. The inset shows the threshold voltage shift as function of time followed by recovery.

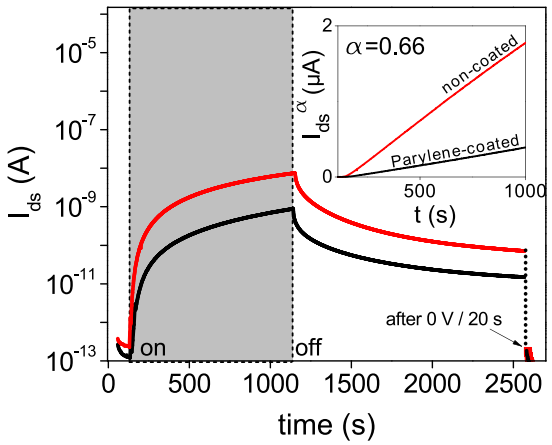


FIG. 5. Drain-source current transient of parylene-coated and non-coated TFTs under NBIS at $V_{gs} = -15$ V followed by the recovery process in the dark (while keeping $V_{gs} = -15$ V). The gray section indicates the duration of light exposure (on). The inset shows sublinear power law dependence of the light-induced instability ($\alpha \sim 0.66$). Removing negative gate bias for 20 s accelerates the recovery of $I_{ds}$ for both devices.

It is widely accepted that the light-induced instability on the IGZO-TFT is due to generation of new dopant species. This can be caused by the photoionization of the deep oxygen vacancy ($V_O$) to shallow ionized oxygen vacancies ($V_O^{2+}$).[20] The formed $V_O^{2+}$ will be pulled to the channel-dielectric interface by application of negative gate bias stress. This defect conversion increases IGZO free carrier concentration and consequently brings a negative shift of $V_{th}$. Nomura *et al.*[21] reported that there is a high density of these $V_O$ defects located in a depth of 2 nm from the top surface layer of the IGZO. Reinforcing this, the authors also demonstrated that the effect of these defects is more pronounced for TFTs with thinner IGZO layers. An adhesion promoter consisting of Sylane A-147 was used to improve the adhesion between parylene-C and the active layer. We propose this adhesion promoter modifies the IGZO surface through oxygen bonding and effectively neutralizing/reducing the oxygen vacancies near the surface. This view is supported by other studies reporting that Sylane A-147 reacts with OH groups on a $Ta_2O_5$ surface.[19] To gain insight into the kinetics of light induced changes, the time dependence of the drain-source current under simultaneous negative bias stress ($V_{ds} = 0.1$ V, $V_{gs} = -15$ V) and illumination was also recorded, as shown in Fig. 5. For the non-coated TFT, the photo-induced current increases nearly 5 orders of magnitude (in 1000 s). The inset of Fig. 5 shows the plot of the current as power-law dependence on time ($I_{ds}^{\alpha} \propto t$). A perfect straight line is obtained when $\alpha = 0.66 \approx 2/3$. Sublinear power-law dependences with $\alpha = 2/3$ have already been reported for defects generated or transformed by irradiation at $Si/SiO_2$ interfaces.[22,23]

Light-induced conductivity persists long after the light stimulus is removed. The light-induced current slowly decays to the original values (prior to illumination), following an exponential decay with a time scale of hours (~6 h). The original conductivity recovery is accelerated when the transistor is operating in accumulation (for a depletion mode device like the one reported here, this simply means having $V_{gs} = 0$ V). That is, our findings show that free carriers in the channel can neutralize the light-induced dopants ($V_O^{2+}$). In fact, the combination of light duration at a certain intensity associated with zero bias value duration can be then optimized to achieve performance enhancement.[17]

In summary, the electrical stability and device reliability under bias stress of devices demonstrate excellent performance after 7 months storage in dark. This is attributed to the effective blocking of atmospheric species diffusion to/from IGZO provided by the parylene layer. This coating also neutralizes defects at the channel surface, leading to less light-induced instability compared with non-coated TFTs. In addition, being depletion-mode devices, a fast recovery process is observed for our TFTs when left unbiased in dark.

This work was funded by National Funds through FCT–Portuguese Foundation for Science and Technology under the SFRH/BDP/99136/2013 grant, Project Nos. UID/CTM/50025/2013 and EXCL/CTM-NAN/0201/2012 FEDER funds through the COMPETE 2020 Programme. The work has also received funding from the European Communities 7th Framework Programme under Grant Agreement No. ICT-2013-10-611070 (i-FLEXIS Project) and from H2020 Program under ICT-03-2014-644631 (ROLL-OUT Project).

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