Bulk-driven flipped voltage follower.

Yasutaka Haga
Izzet Kale

School of Electronics and Computer Science

Bulk-Driven Flipped Voltage Follower

Yasutaka Haga and Izzet Kale
Applied DSP & VLSI Research Group, School of Electronics and Computer Science,
University of Westminster, London, United Kingdom
y.haga@westminster.ac.uk, kalei@westminster.ac.uk

***Abstract*— A voltage buffer so-called the bulk-driven flipped voltage follower is presented. This proposal is based on the Flipped Voltage Follower (FVF) technique, but a bulk-driven MOSFET with the replica-biased scheme is utilized for the input device to eliminate the DC level shift. The proposed buffer has been designed and simulated with a 0.35μm CMOS technology. The input current and capacitance of our proposal are 1.5pA and 9.3fF respectively, and with 0.8V peak-to-peak 500kHz input, the total harmonic distortion is 0.5% for a 10pF load. This circuit can operate from a single 1.2V power supply and consumes only 2.5μA.**

I. INTRODUCTION

Voltage buffers play an essential role in analog and mixed-signal circuits and processing systems, where they are widely used for driving large capacitive loads at high speeds. The ideal performance of a voltage buffer is not only to drive the large load as fast as possible but also with minimal power consumption, which means that the buffer needs to have high slew rate and low static power consumption. Today, it is evident that the Flipped Voltage Follower (FVF) proposed by R. G. Carvajal *et al* in [1] is one of the closest to the ideal voltage buffer, as many recent proposals are utilizations and/or modifications of the FVF [2]-[5].

Recently, the new version of the class-AB FVF that is free from the DC level-shift has been proposed by Ramirez-Angulo *et al* [5]. In this paper, we present a much simpler technique which can eliminate the DC level shift and convert into class AB operation, whilst preserving the advantages of the FVF approach– low-power consumption with high-power drive.

II. PREVIOUS ESSENTIAL WORKS

This section covers a brief review of voltage followers and the bulk-driven MOSFETs used in a differential pair, which we have utilized and forms the essential part of our proposal.

A. Voltage followers

Figure 1 illustrates two types of voltage followers. Figure 1(a) is the conventional type of a voltage follower, which is also known as a source follower [6]-[7]. The input device MP01 is biased with the drain current of *IREF*, therefore the gate-to-source voltage $V_{GS\,\mathrm{MP01}}$ becomes constant if the body-effect is neglected, and therefore the output voltage V_{OUT} is equal to $V_{IN} + V_{GS\,\mathrm{MP01}}$. Figure 1(b) illustrates the FVF, in which V_{OUT} is also shifted up by $V_{GS\,\mathrm{MP01}}$ from V_{IN}, however, in contrast to Figure 1(a), the beauty of the FVF is that it has current sourcing and sinking capabilities at the output, which can lead to delivering both high-power driving as well as low-power consumption simultaneously.

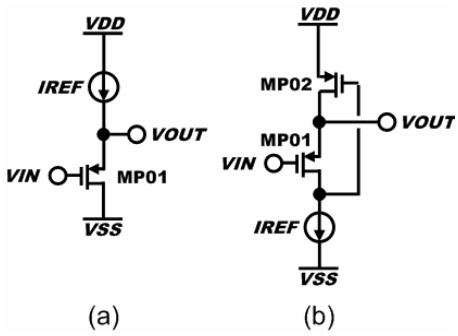

Figure 1. Voltage followers (a) common-drain amplifier (volotage follower) and (b) FVF proposed in [1]

B. Bulk-driven MOSFETs used in differential pairs

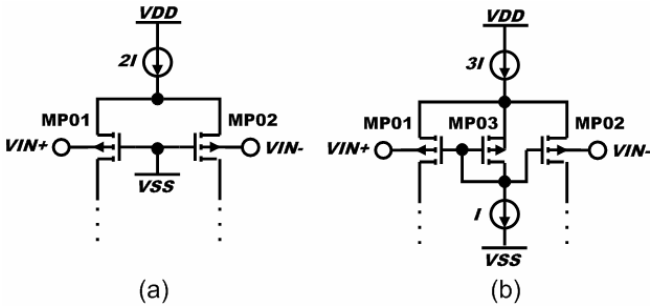

Figure 2. Bulk-driven differential pair (a) pMOS input pair and (b) the replical-biased scheme proposed in [10]

In low-voltage rail-to-rail operational amplifier designs, there exists a design technique called the bulk-driven approach. The traditional design technique for rail-to-rail operational amplifiers is the deployment of complementary differential pairs with the tail current being controlled with current switches to keep the g_m constant [8]. However, due to the fact that the mobility ratio of the complementary pairs (μ_n/μ_p) is process- and temperature dependent, causing the g_m

variation to deviate by approximately 12% [9], there exist circuit topologies which use only a single type of the differential pair, where one of them is the bulk-driven one. Figure 2(a) illustrates a bulk-driven differential pair that uses p-type devices only.

The primary problem of Figure 2(a), however, is that the transconductance of a bulk-driven MOSFET (g_{mbs}) is dependent on the bulk-to-source voltage (V_{BS}). The level-1 model of the g_{mbs} is given by:

$$g_{mbs} = \gamma\,(2\beta I_{DS})^{0.5} / 2\,(2|\Phi_F| - V_{BS})^{0.5} \qquad (1)$$

where γ is the bulk-threshold parameter, β is the small-signal transconductance parameter, I_{DS} is the drain current, and $2|\Phi_F|$ is the surface potential.

To overcome the concern of g_{mbs} dependency over the V_{BS}, Blalock *et al* [10] proposed the Replica-Biased Scheme (RBS) as illustrated in Figure 2(b). The pMOS identified as MP03 is the replica device biasing the gates of the pair. Since the bulk of MP03 is shorted with its source, the V_{BS} of the pair is kept at zero.

We have noted the advantage from Blalock's approach namely that the condition of $V_{BS} = 0$ is kept constant, meaning $V_B = V_S$, and we chose to apply this to the FVF illustrated in Figure 1(b) to remove the DC level shift.

III. Proposed Bulk-Driven Flipped Voltage Follower

Figure 3 illustrates our proposal of the modified FVF, which we have named as "Bulk-Driven Flipped Voltage Follower (BDFVF)". As mentioned in the previous section, this is the FVF for which the input device has been modified to a bulk-driven MOSFET biased by the replica circuit to eliminate DC level shift.

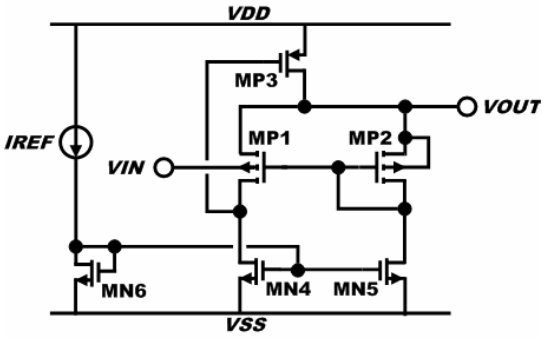

Figure 3. Bulk-driven flipped voltage follower (class-A)

The operation principle of the BDFVF of Figure 3 is very simple to follow. MP1, MP3, and MN4 form the FVF. MP1 is the input device, which its bulk is utilized to feed the input. MP2 and MN5 are the replica devices for MP1 and MN4 respectively. Note that the bulk of MP2 is physically shorted to its source, which is the output node. Since the gate of MP1 is biased with the diode-connected MP2, as well as the drain current of MP1 and MP2 are equally set to *IREF*, V_B and V_S of MP1 becomes virtually shorted (i.e. $V_{BSMP1} = 0$), and in effect the output voltage V_{OUT} becomes equal to V_{IN}.

Our proposal of Figure 3 works well, however since it is class-A type there is a limitation in its sink capability to 2*IREF*, which leads to poor pull capability in driving large loads at high speed. To overcome this problem, we have modified the circuit of Figure 3 to class-AB type as shown in Figure 4.

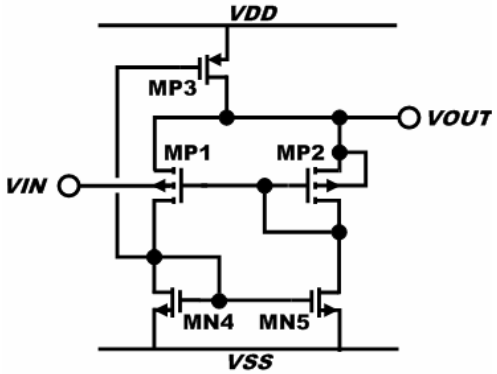

Figure 4. Proposed class-AB bulk-driven flipped voltage follower

The difference of Figure 4 from Figure 3 is that only MN4 has been modified to diode-connected instead of the constant bias to *IREF*. In this way, MP1 and MP2 can also have the same drain current and hence the replica-biased scheme remains valid. This simple change has lead to significant improvement in the sink capability of the output without the need of widening MN4 or MN5 or increasing *IREF*. In the next section, simulation results are provided.

IV. Simulated Results

A. Overall Performance

Using the BSIM3 MOSFET models of a 0.35µm CMOS process, we designed and simulated the BDFVF of Figure 4. Table I shows the simulation results summarizing the overall performance.

TABLE I. Simulation Results of the Overall Performance of the Class AB DBFVF Circuit of Figure. 4

Parameter	Simulated results
3dB frequency	2.8MHz
Total current consumption (when IL=0)	2.5µA
Slew rate (VDD=2V, VSS=0V, CL=10pF, VIN=1V↔2V)	1.9V/µs
PSRR+ / PSRR-	41.7dB / 42.0dB (dc to 100kHz)
1/*f* noise at 1kHz	880nV/√Hz
THD (Vpp=0.8V VDD=1.5V, VSS=0V, CL=10pF)	0.0747% when f=1kHz 0.0794% when f=100kHz 0.501% when f=500kHz
Input voltage range (VDD=2V, VSS=0V)	1V to 2V For offset ≤ 10mV
Load regulation	±15µA for offset ≤ 10mV
Input current	1.5pA
Input capacitance	9.3fF
Unless stated, the set up condition is: VDD=1.2V, VSS=0V, VIN=1V, CL=10pF, IL=0µA	

Figure 5 illustrates the simulated plot of V_{OUT} versus V_{IN} with the setup of *VDD* = 2V and *VSS* = 0V. The simulation

results indicate that the offset between V_{OUT} and V_{IN} was 10mV for the input range from 1V to 2V.

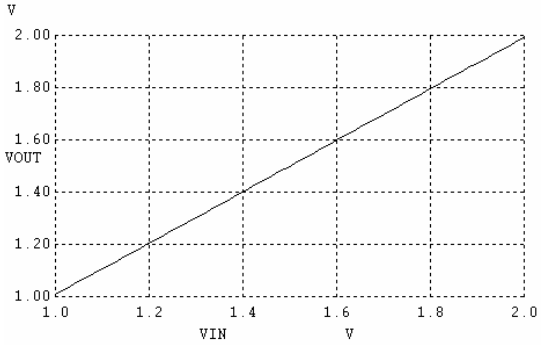

Figure 5. V_{OUT} vs V_{IN} (*VDD*=2V, *VSS*=0V)

Figure 6 illustrates the simulated plot of V_{OUT} with a sinusoidal V_{IN} input with 0.8V peak-to-peak magnitude and 500kHz frequency, and with the set up of *VDD* = 2V, *VSS* = 0V, and CL = 10pF. The simulation results indicate that the Total Harmonic Distortion (THD) was 0.5%.

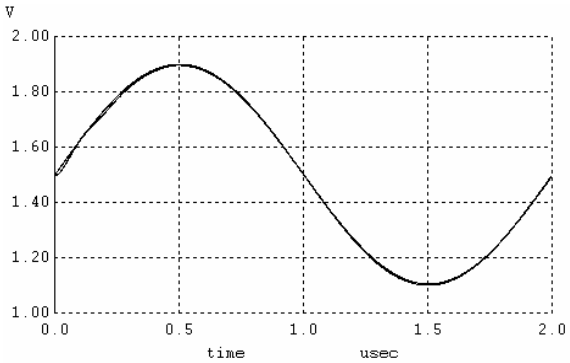

Figure 6. V_{OUT} and V_{IN} with 0.8Vpp 500kHz sinusoidal input (*VDD*=2V, *VSS*=0V, CL=10pF)

Figure 7 illustrates the simulated plot of V_{OUT} regulation capability against the load current I_L. With the setup of *VDD* = 1.5V, *VSS* = 0V, and V_{IN} =1V, the simulation results indicate that V_{OUT} kept on regulated within 10mV until the load current reaches to ±15µA.

B. Input impedance

Using bulk-driven MOSFETs in a differential pair of the operational amplifier is known to be a disadvantage in input current and capacitance [11]. In this sub-section, we present the theoretical overview as well as the simulated results to state that this disadvantage is not the case with the BDFVF.

1) Input current

With a bulk-driven MOSFET as an input device, the input signal is fed into the pn-junction of the MOSFET. The current through the pn-junction I_{Dpn} is modeled by Equation 2 [12]-[13]:

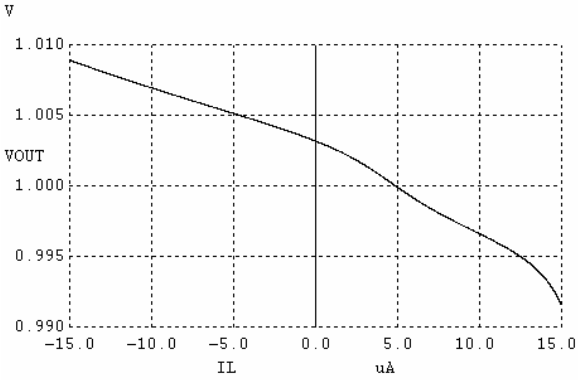

Figure 7. Load regulation (*VDD*=2V, *VSS*=0V, V_{IN}=1V)

$$I_{Dpn} = I_S \exp(V_D/V_T) \quad (2)$$

where I_s is the pn-junction current, which is also known as the scale current, when the voltage across the pn-junction V_D is zero. V_T is the thermal voltage, which is modeled as

$$V_T = kT/q \quad (3)$$

where k is the Boltzmann constant (=1.38 x 10^{-23}JK^{-1}), T is the temperature in Kelvin, and q is the charge of an electron (=1.602 x 10^{-19}C). At room temperature, V_T is approximately 26mV.

I_s can be described as in Equation 4:

$$I_s \propto A_D [(1/N_A) + (1/N_D)] \quad (4)$$

where A_D is the area of the diode junction, and N_A and N_D are the doping concentrations of the acceptors and donors respectively.

In the case of a bulk-driven differential pair, the input current is expected to be large because of the bulk being forward-biased. On the other hand for BDFVF, a large input current is not expected since the aim is to achieve a virtual short between the input and output. To affirm this theoretical consideration further, we have simulated deploying the setup used for arriving at Figure 5 to observe the offset behavior and the input current, as shown in Figure 8 and 9 respectively.

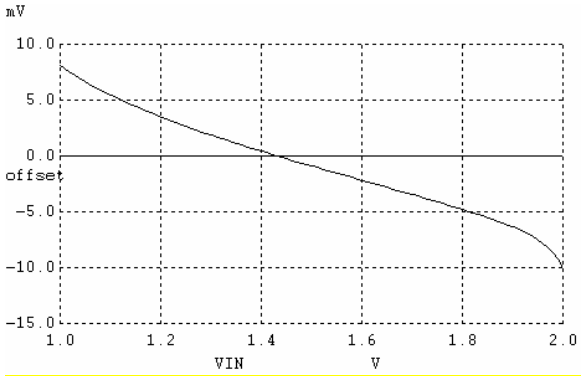

Figure 8. Offset voltage of Figure 5

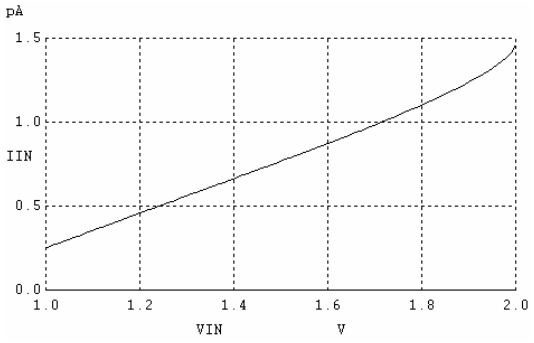

Figure 9. Input current (*VDD*=2V, *VSS*=0V)

The simulated result of Figure 9 shows that the input current remains at less than 1.5pA.

2) Input capacitance

The capacitance of the pn-junction C_j can be modeled by Equation 5 [11]-[13]:

$$C_j = C_{j0} / (1+(V_{SB}/\phi_0))^{0.5} \quad (5)$$

In the case of a bulk-driven differential pair, the input capacitance is expected to be large because of the bulk being forward-biased. On the other side for BDFVF, a large input capacitance is not expected since the aim is to achieve a virtual short between the input and output. To affirm this theoretical consideration further, we have set up the simulation condition as shown in Figure 10.

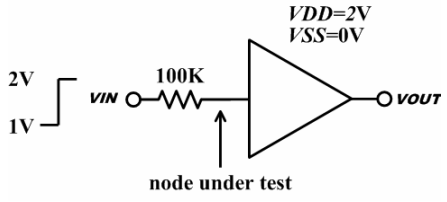

Figure 10. Simulation setup for the input capacitance

The simulated plot of the setup in Figure 10 is given in Figure 11.

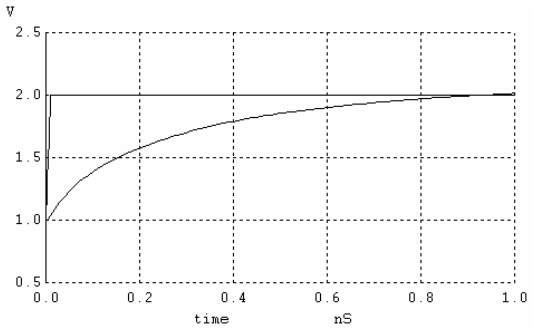

Figure 11. Simulation results for the Figure 10 setup

From Figure 11, the time constant τ was found to be 0.93ns. Hence, the input capacitance was determined as 9.3fF (τ=RC).

V. CONCLUSION

A new type of FVF called BDFVF has been presented. This proposal utilizes a bulk-driven MOSFET with the replica-biased scheme as the input device to eliminate the DC level shift. The theoretical overview of the input current and capacitance has been provided, and the simulation results showed that the input current and capacitance are in the pico-amp and femto-Farad ranges. The attractive and advantageous performances of the FVF, such as high-power driving and low-power consumption were retained. The BDFVF is a powerful block of the FVF family which is free of level shift.

REFERENCES

[1] R. G. Carvajal, J. Ramírez-Angulo, A. J. López-Martin, A. Torralba, J. A. G. Galán, A. Carlosena, and F. N. Chavero, "The Flipped Voltage Follower: A Useful Cell for Low-Voltage Low-Power Circuit Design," *IEEE trans on Circuits and Design I*, vol 52, no. 7, pp. 1276 – 1291, July 2005

[2] I. Padilla, J. Ramirez-Angulo, R. G. Carvajal, A. J. Lopez-Martin, A. Carlosena, "Compact implementation of linear weighted CMOS transconductance adder based on the flipped voltage follower*," IEEE proc. ISCAS 2006*, pp. 4281 – 4284, May 2006

[3] I. Padilla-Cantoya, J. E. Molinar-Solis, G. O. Ducoudary, "Class AB Low-Voltage CMOS Voltage Follower," *IEEE Proc. MWSCAS 2007*, pp. 887 – 890, August 2007

[4] T. Y. Man, K. N. Leung, C. Y. Leung, P. K. T. Mok, and M. Chan, "Development of Single-Transistor-Control LDO Based on Flipped Voltage Follower for SoC," *IEEE trans on Circuits and Design I*, pp. 1392 – 1401, Vol 55, No. 5, June 2008

[5] J. Ramirez-Angulo, S. Gupta, R. G. Carvajal, A. J. Lopez-Martin, "New Improved CMOS Class AB Buffers Based on Differential Flipped Voltage Followers," *IEEE proc. ISCAS 2006*, pp. 3914 – 3917, May 2006

[6] P. E. Allen and D. R. Holberg, "CMOS analog circuit design," Oxford Univeristy Press, 2nd ed., 2002

[7] B. Razavi, "Design of Analog CMOS Integrated Circuits", International Edition, McGraw-Hill, 2001

[8] R. Hogervorst, R. J. Wiegerlink, P. A. L. de Jong, J. Fonderie, R. F. Wassenaar, and J. H. Huijsing, "CMOS low-voltage operational amplifiers with constant-*gm* rail-to-rail input stage," *IEEE Proc. ISCAS '92*, vol. 6, pp. 2876-2879, May 1992

[9] J. M. Carrillo, J. F. Duque-Carrillo, G. Torelli, and J. L. Ausin, "Constant-gm constant-slew-rate high-bandwidth low-voltage rail-to-rail CMOS input stage for VLSI cell libraries," *IEEE J. of Solid-State Circuits*, vol. 38, no. 8, August 2003

[10] B. J. Blalock, H. W. Li, P. E. Allen, and S. A. Jackson, "Body-driving as a low-voltage analog design technique for CMOS technology," *IEEE Southwest Symp. on Mixed-Signal Design (SSMSD) 2000*, pp. 113-118, February 2000

[11] B. J. Blalock, P. E. Allen, and G. A. Rincon-Mora, "Designing 1-V op amps using standard digital CMOS technology," *IEEE Tans. Circuits and Systems – II: Analog and Digital Signal Processing*, pp. 769-780, vol. 45, no. 7, July 1998

[12] D. A. Johns and K. Martin, "Analog Integrated Circuit Design," John Wiley & Sons Inc., 1997

[13] A. S. Sedra and K. C. Smith, "Microelectronic Circuits", Fifth Edition, Oxford University Press, 2004